DESIGN OF CONTINUOUS TIME CIRCUITS USING CURRENT MODE BUILDING BLOCKS

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I hereby declare that the thesis entitled "**Design of Continuous Time Circuits using Current Mode Building Blocks**" is an original work carried out by me under the supervision of Dr. Rajeshwari Pandey, Professor, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi. This thesis has been prepared in conformity with the rules and regulations of the Delhi Technological University, Delhi. The research work reported and results presented in the thesis has not been submitted either in part or full to any other university or institute for the award of any other degree or diploma.

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CERTIFICATE

This is to certify that the work embodied in the thesis entitled "**Design of Continuous Time Circuits using Current Mode Building Blocks**" by **Priyanka Gupta (2K14/PhD/EC/10)** in partial fulfillment of requirements for the award of Degree of **DOCTOR OF PHILOSOPHY** in **Department of Electronics and Communication Engineering, Delhi Technological University** is an authentic record of student's own work carried by her under my supervision. In my opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. This is further certified that this work has not been submitted to any other Institute or University for the award of any other diploma or degree.

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ABSTRACT

The information being processed in electric networks may be denoted through node voltages or through branch currents. An analog circuit is termed as voltage mode (VM) circuit when the information is expressed through voltage levels at different nodes, whereas if branch currents represent the signal, the circuit are termed as a current mode (CM) circuit. Current mode processing has received significant attention in the field of analog circuit design due to advantages offered over voltage mode circuits. This has resulted in emergence of various current mode analog building blocks which is evident from vast available literature. Voltage differencing buffered Amplifier (VDBA) is an active block of relatively recent origin which uses voltage differencing as input stage. In circuit implementation of VDBA its transconductance (g_m) can be controlled through bias current which helps in electronic tuning of design parameters of the applications build around this active block. This leads to ease of circuit integration. The VDBA, therefore, has evolved as a promising choice for analog applications and this has led the author to explore analog circuit designing using VDBA.

A variety of VDBA implementations are available in literature but a VDBA providing high transconsuctance gain (g_m) and bandwidth (BW) with low power consumption has not been explored and leads to a significant research gap. So a low power, high performance VDBA using differential flipped voltage followers is presented.

In consumer and industrial applications variety of physical quantities are measured using transducers as input unit. The low level differential output of transducer is to be amplified faithfully, eliminating the common mode noise, for further processing. This is accomplished by using instrumentation amplifiers (IA) at input stage. The IAs are always designed for high differential gain along with high common mode rejection ratio

(CMRR). A high CMRR voltage mode IA employing single VDBA is proposed which works on much lower power supply as compared the existing designs.

Electronic filters are essential building blocks of electronic systems. In this thesis, three applications namely (i) a first order APF (ii) a SISO multifunctional filter and (iii) a MISO universal filter are proposed. An APF in inverting/non-inverting configuration using a VDBA has been proposed which provides voltage output at low impedance with electronically tunable voltage gain. A second order VM multifunction generalized filter topology employing single VDBA is presented next which can be configured to provide low pass, high pass, and band pass responses with appropriate admittance selection. The proposed topology is a suitable choice for high quality factor implementation. The third filter topology is a MISO universal biquad filter designed using two VDBAs, two capacitors and a grounded resistor.

Non-linear signal processing applications have also been explored in this thesis. A four quadrant analog multiplier (FQAM) using the quarter square algebraic identity is proposed first. A low power squaring is the next proposition which is followed by a low power square rooting circuit.

Sinusoidal oscillators are the integral part of electronic circuit design. The oscillators find extensive usage in communication systems, control systems, measurement and instrumentation systems. In this work, a single phase, three quadrature phase and two multiphase sinusoidal oscillators have been proposed using VDBA/DO-VDBA.

All the proposed designs are functionally verified through the virtuoso ADE tool or SPICE environment is used for simulation work. Some of the propositions are verified experimentally also.

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ABBREVIATIONS

all pass filter	APF
operational transconductance amplifier	OTA
analog building blocks	ABBs
analog design environment	ADE
band pass filter	BPF
band stop filter	BSF
bandwidth	BW
common mode rejection ratio	CMRR
condition of oscillation	CO
current controlled CDBA	CC-CDBA
current controlled CDTA	CCCDTA
current controlled current conveyor	CCC
current controlled current through transconductance amplifier	CCCTTA
current conveyor	CC
current differencing buffered amplifier	CDBA
current differencing transconductance amplifier	CDTA
current feedback operational amplifier	CFOA
current follower	CF
current follower transconductance amplifier	CFTA
current mode	CM
current mode instrumentation amplifier	CMIA
current through transconductance amplifier	CTTA
design rule check	DRC
differential difference amplifier	DDA

differential difference OFA	DDOFA
differential flip voltage follower	DFVF
dual output VDBA	DO-VDBA
dynamic threshold MOSFET	DTMOS
flip voltage follower	FVF
floating gate MOSFET	FGMOS
four quadrant analog multiplier	FQAM
four terminal floating nullor	FTFN
frequency of oscillation	FO
fully balanced VDBA	FB-VDBA
fully differential flip voltage follower	FD-FVF
high pass filter	HPF
input common mode range	ICMR
instrumentation amplifier	IA
layout vs. schematic check	LVS
low pass filter	LPF
multiphase	MP
multiple inputs multiple output	MIMO
multiple inputs single output	MISO
Number of inputs and outputs: single input single output	SISO
operational floating amplifier	OFA
operational transresistance amplifier	OTRA
quadrature phase	QP
single input multiple outputs	SIMO
single phase	SP

total harmonic distortion	THD
transadmittance mode	TAM
transadmittance mode IA	TAMIA
transconductance amplifier	TA
transfer function	TF
transimpedance IA	TIMIA
transimpedance mode	TIM
unity gain BW	UGB
voltage differencing buffered amplifier	VDBA
voltage differencing inverted buffered amplifier	VDIBA
voltage differencing transconductance amplifier	VDTA
voltage mode	VM
voltage mode instrumentation amplifier	VMIA
Z copy VDBA	ZC-VDBA

CHAPTER 1

1.1 Introduction

Nowadays in electronic systems, storage and signal processing are done in digital domain [1]. However, the real-world signals are represented in the analog domain and therefore analog signal processing serves as an interfacing medium between the two. The analog signal processing requires a number of applications such as filters, amplifiers, comparators, sample and holding circuit, digital-analog convertor and analog-digital convertor.

In lumped electric networks, the information being processed may be denoted through node voltages or through branch currents [1]. An analog circuit is termed as voltage mode (VM) circuit when the information is expressed through voltage levels at different nodes, whereas if branch currents represent the signal, the circuit is termed as a current mode (CM) circuit [2]. A VM circuit is supposed to deliver large swing in output voltage keeping minimum power consumption. It results into a high impedance node design. The parasitic capacitance in the VM circuit needs charging and discharging with the full swing for signal processing, which confines the slew rate and speed [3]. The CM circuit is a low impedance node network, making it a low time constant circuit that improves speed and slew rate. It is well established in the literature [1], [2], [4] that a CM circuit may function with lower voltage supply [5] and at a given supply, the CM circuit possess higher dynamic range in comparison to its VM counterpart. The simple architecture of CM circuits makes it more attractive compared to VM circuits. It leads to smaller die area.

These advantages led researchers to explore CM circuits which are manifested in the form of several analog building blocks (ABBs) and are presented in [1], [5]–[53] and

references cited therein. The current conveyor (CC) [6] is an amalgam of current/voltage circuit and is most widely explored ABB. The different generations of CC were named as CCI, CCII [7], [34]–[39] and CCIII [8]. They were introduced in the years 1968, 1970 and 1995 respectively and the three generations of CC differ in terms of terminal characteristics. A variety of modifications in the basic conveyor structure, for more effective utilization, led to the introduction of various CC based newer elements [9]–[19]. An operational transconductance amplifier (OTA) [20], is a three terminal block and the output current is the multiplication of transconductance gain and difference of input voltages. To be compatible with VM circuits, it becomes essential to translate the output current into a voltage signal. A four terminal block having port relations analogous to CCII followed by a voltage buffer is the current feedback operational amplifier (CFOA) [21], [22], [41]. The operational floating amplifier (OFA) [24], differential difference amplifier (DDA) [26], differential difference OFA (DDOFA) [25] and four terminal floating nullor (FTFN) [23] are few examples of fully balanced structures and hence are more immune to noise. The circuit element operational transresistance amplifier (OTRA) [5], [42], [43] is a three terminal ABB and a current controlled voltage source. A simplified version of the OTRA is current differencing buffered amplifier (CDBA) [27], consisting of a current differencing unit [52] and a voltage buffer. Another block having current differencing unit as an input section and being explored widely is the current differencing transconductance amplifier (CDTA) reported in [29]. In current controlled CDBA (CC-CDBA) [28] and current controlled CDTA (CCCDTA)[30], [53], the circuit parameters are controlled electronically. In the current follower transconductance amplifier (CFTA) [31], the current follower (CF) is followed by a transconductance amplifier (TA) and is suited for CM circuits as its input and output signals are current. A different

class of CM ABBs has evolved recently, having a TA as the input stage. One block of this class is voltage differencing transconductance amplifier (VDTA) [32]. The second important block receiving great attention for circuit designing is voltage differencing buffered amplifier (VDBA) [33].

The VDBA was first conceptualized by Biolek *et al.* [1] as a block consisting of a TA followed by a buffer. This block can provide both current and voltage outputs at an appropriate impedance level thereby providing design flexibility. Additionally, in-circuit implementation of VDBA, its transconductance (g_m) can be controlled through bias current which helps in the electronic tuning of design parameters of the applications build around this ABB. This leads to ease of circuit integration. The VDBA, therefore, has evolved as a promising choice for analog applications [33], [54]–[67] and this has led the author to explore analog circuit designing using VDBA.

1.2 Available Literature

An extensive literature review is carried out which advises that the available literature on VDBA may be categorized as the work associated with

- VDBA Implementations [33], [54]–[67]
- VDBA Applications [33], [54]–[91]

1.2.1 VDBA Implementations

Various implementation of VDBA and its variants are available in the literature. The CMOS implementation of VDBA has been presented in [33] and [65]. The floating gate MOSFET (FGMOS) based VDBA implementation is proposed by Ninawe *et al.* [55] and a dynamic threshold MOSFET (DTMOS) based VDBA structure is presented in [56] which operates at ultra low power supply (0.2 V). To further enhance the versatility

of these blocks, some modifications in the internal structure have been proposed by researchers leading to its variants like voltage differencing inverted buffered amplifier (VDIBA) [57]–[60]. In VDIBA the output unit consists of an inverted voltage buffer. In dual output VDBA (DO-VDBA) [61] alteration is done to get the output voltages in inverted/non-inverted forms simultaneously. Another amendment is done to have the current and voltage outputs with both signs and the circuit is termed as a fully balanced VDBA (FB-VDBA) [61]–[63]. One more variant termed as Z copy VDBA (ZC-VDBA) is reported by Guney *et al.* in [64], in which two z terminals of same polarity exists. The VDBA using BiCMOS technology is implemented by Onjan *et al.* [66]. Design and analysis of tunable VDIBA with enhanced performance is presented in [67]. These structures along with their salient features have been summarized in Table 1.1.

Table 1.1 Literature summary of different VDBA structures

Reference No.	Block	Technology (µm)	Power Supply (V)	No of transistors + passive components	Linear input voltage range of TA (V)	Linear input voltage range of Buffer (V)	Transconductance (µS) at bias current (I_B) (µA)	Buffer transfer ratio	3 dB BW of TA (MHz)	3 dB BW of Buffer (MHz)	Power consumption (µW)
[33]	VDBA	0.35	±1.5	16 MOS	± 0.2	-1.5 to 1.1	748 I_B not reported	1	--	--	970
[54]	VDBA	0.18	±2	29 MOS + 2Resistor +1 Capaitor	--	± 0.25	79 at I_B = 120	1	69	49.5	1.4×10^3
[55]	VDBA	0.18	±1.35	12 MOS +4FGMOS	± 0.4	--	483 I_B not reported	0.97	385	--	745
[56]	VDBA	0.18	± 0.2	7 MOS +9 DTMOS	- 0.145 to 0.2	- 0.145 to 0.2	0.064 I_B not reported	1	3.7×10^{-3}	--	6.22×10^{-3}
[57]	VDIBA	0.09	± 0.6	12 MOS +3 Resistor	± 0.05	- 0.5 to 0.2	3.58×10^3 at I_B = 220	0.944	334	3.75×10^3	4.54×10^3
[58]	VDIBA	Commerical ICs	± 5	--	--	--	--	--	--	--	--

[59]	VDIBA	0.18	±0.75	5 MOS +1 FGMOS	±0.25	-0.75 to 0.5	582 at I_B=100	0.985	92.47	1.58 ×10^3	1.5×10^3
[60]	VDIBA	0.18	± 0.4	13 MOS +2 FGMOS	±0.3	-0.4 to 0.16	223 at I_B=50	0.981	1.124 ×10^3	2.35 ×10^3	569
[61]	DO-VDBA	0.18	± 1.2	8 MOS	±0.1	± 0.25	500 at I_B =50	0.962/ 0.926 at two outputs	160	--	--
	FB-VDBA	0.18	± 1.2	16 MOS	±0.1		1.025×10^3 at I_B = 50	.--	51	--	-
[62]	FB-VDBA	Commercial ICs	±5	--	--	--	0.1×10^6 I_B not reported	--	--	--	--
[63]	FB-VDBA	0.35	±0.75	10 MOS + 14 BJT	± 0.05	± 0.4	3.5×10^3 at I_B=100	0.986	23	1.3×10^3	1.6×10^3
[64]	ZC-VDBA	0.18	± 0.9	28 MOS	± 0.5	- 0.5 to 0.7	50 at I_B= 47	0.953	884/ 926 at two outputs	487	690.3
[65]	VDBA	0.25	± 2	17	± 0.10	± 0.10	500 at I_B =40	0.991	--	145	--
[66]	DO-VDBA	0.35	±0.75	7 MOS+6 BJT	--	--	580 at I_B=15	--	--	--	--
[67]	VDIBA	0.18	± 0.6	12 MOS + 2 Resistor	± 0.50	--	1024 at I_B=150	1.07	263	--	560

It may be observed from Table 1.1 that though a variety of VDBA structures exist but a VDBA providing high g_m and bandwidth (BW) with low power consumption has not been explored and leads to a significant research gap.

1.2.2 VDBA Applications

In the available literature VDBA is used for designing numerous signal processing and generating applications as summarized below:

i) Active immittance simulators [68]–[77]

ii) Filters [33], [54]–[60], [62]–[68], [78]–[84]

iii) Signal generators [61], [82], [85]–[91]

i) Active immittance simulators

An inductor is an essential and integral part of any electronic circuit. But due to large area requirement, weight, cost and electronic tunabilty, on chip design of inductor is not possible. This can be fixed by simulating the inductor using the ABBs. A VDBA with two passive elements are used to realize a lossless grounded inductance simulator in [68]. A grounded lossy parallel inductance simulation is presented in [69]. A resistorless floating inductance simulator employing two VDBAs with a capacitor is presented in [70]. One series and one parallel active floating lossy inductance simulators are presented by [71]. A floating lossy series type inductance simulator having electronic tunability, using two VDBAs is presented in [72]. A variable lossy series inductance simulator using a single VDBA is presented in [73].

Further, to obtain large valued capacitors using small capacitors, few capacitance multiplier structures have also been presented in the literature. A capacitance multiplier using single VDBA, a capacitor and a grounded resistor is proposed in [74]. Two capacitance multipliers with a grounded capacitor and a VDBA having electronic tunability are realized in [55] and [56]. Tunable floating capacitance multiplier using single FB-VDBA, a capacitor and a resistor is realized in [77].

ii) Filters

Filters find widespread usage in communication and instrumentation systems and are the essential building block in analog signal processing. These are frequency selective networks that allow a specified range of frequencies to be passed known as filter pass band, while attenuate frequencies outside this range known as filter stop band. In literature, the categorization of filters is done in several ways as:

-Filter transmission characteristic: low pass filter (LPF), high pass filter (HPF), band pass filter (BPF), band stop filter (BSF) and all pass filter (APF),

-Slope of the stop band: first, second and higher order filters,

-Input and output signals: CM, VM, or transimpedance mode (TIM) or transadmittance mode (TAM) filters,

-Number of inputs and outputs: single input single output (SISO), single input multiple outputs (SIMO), multiple inputs single output (MISO) and multiple inputs multiple output (MIMO).

A number of filter applications exists in literature using VDBA and its variants [33], [54]–[60], [62]–[68], [78]–[84]. The available literature on filters using VDBA and its variant is summarized in Table 1.2.

Table 1.2 Literature summary for filters using VDBA

Reference	No. of ABB	Order	Type	Standard filter Function	Mode	Passive elements (R+C)	Supply voltage (V)	Independent ω_0 and Q_0	Output impedance	Power Consumption (mW)	Technology used
[57]	3 VDIBA	3	SISO	LPF	VM	0+3	0.6	--	Low	12.3	0.09 µm CMOS
[58]	1 VDIBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	1+2	0.9	No	High	--	0.18 µm CMOS
[59]	2 VDIBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	0+2	0.75	No	Low	2.8	0.18 µm CMOS FGMOS
[60]	2 VDIBA	2	MISO	LPF, BPF, HPF	VM	0+2	0.4	No	Low	1.1	0.18 µm FGMOS
[67]	2 VDIBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	1+2	0.6	Yes	Low	--	0.18 µm CMOS
[79]	1 VDIBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	1+2	0.9	No	High	10.5	0.18 µm CMOS
[82]	1 VDIBA	1	SISO	APF	VM	0+1	--	Yes	Low	--	OPA860

[84]	2 VDIBA	2	MISO	BPF, HPF	VM	1+2	0.6	No	Low	--	0.045 µm CMOS
	2 VDBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	0+2	1.5	No	Low	0.97	0.18 µm CMOS
[33]	2 VDBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	1+2	1.5	Yes	Low	0.97	0.18 µm CMOS
[55]	2 VDBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	1+2	1.35	No	Low	1.5	0.18 µm CMOS FGMOS
[56]	2 VDBA	2	MISO	LPF, BPF, HPF, BSF	VM	2+2	0.2	No	Low	13x 10^{-6}	0.18 µm CMOS DTMOS
[65]	1 VDBA	1	SISO	APF	VM	0+2	2	--	Low	--	0.25 µm CMOS
[66]	2 VDBA	2	SISO	APF	VM	0+2	0.75	Yes	Low	--	0.35 µm CMOS BiCMOS
[68]	1 VDBA	2	SISO	BPF	VM	2+2	5	Yes	Low	--	OPA 860
[78]	1 VDBA	2	MISO	LPF, BPF, HPF	VM	2+2	0.9	No	High	0.45	0.18 µm CMOS
[83]	2 VDBA	2	MISO	LPF, BPF, HPF, APF, BSF	VM	1+2	0.6	No	Low	--	OPA860
[54]	3 ZC-VDBA	2	SIMO	HPF,BPF, LPF	VM	0+2	2	No	Low	4.2	0.18 µm CMOS
[64]	2 ZC-VDBA	2	SIMO	LPF, BPF, HPF	CM	0+2	0.9	No	High	1.48	0.18µm CMOS
[62]	2 FB-VDBA	2	SIMO	LPF, BPF, HPF	VM	4+2	5	No	Low	--	SPICE Model of OPA860
[63]	1 FB-VDBA	1	SISO	APF	VM	1+1	0.75	--	Low	1.6	0.35 µm CMOS
[81]	1 FB-VDBA	1	SISO	APF	VM	1+1	5	--	Low	--	OPA860
[80]	1 DO-VDBA	2	SIMO	LPF, BPF, HPF, APF, BSF	CM	2+2	1.2	No	Low	--	OPA860

From the existing literature, it is observed that all the structures are VM except those presented in [64] and [82] which are CM filters. Filters proposed in [57], [63], [65], [66], [68], [81], [82] provide only single response, those in [54], [56], [60], [62], [64], [78] provide multiple responses and the structures of [33], [55], [58], [59], [79] are universal filters. The voltage output in [64], [78], [79] is available at high impedance, not a suitable choice for cascading purpose. Further, only a few configurations [33], [66] provide independent tuning of pole frequency (ω_0) and quality factor (Q_0). The filters proposed in [33], [54], [55], [59], [62], [64], [66], [78], [79], [82] are designed using off shelf ICs and use large supply voltage.

Circuit structures using single ABB lead to low power designs. Circuit design with moderate component spread is always a preferred choice from the integration viewpoint. Further, independent tuning of ω_0 and Q_0 is a desirable feature. It is observed from Table 1.2 that limited structures qualify for all the above features and this led the author to explore such filter structures.

A universal filter provides all five responses using a single circuit. From Table 1.2, it is observed that few universal structures are available. The structures of [33], [55], [59], [67], [79], [80], [82], [83] are MISO and the availability of output voltage at low impedance node is desirable with the independent tuning of ω_0 and Q_0. From Table 1.2, it is seen that only a few structures met up with these requirements which motivated the author to explore such design.

An APF, also termed as phase shifter, is a two port network that allows all input signal frequencies to pass with altered phases. Though a variety of first order APF using different ABBs exist but limited literature is available on VDBA based first order APF [65], [81], [82]. This gap was tapped as a possibility to explore new VDBA based APF design.

iii) Oscillators

Sinusoidal oscillators are the integral part of electronic circuit design. The oscillators find extensive usage in communication systems, control systems, measurement and instrumentation systems. In literature, the sinusoidal oscillators are classified on the basis of:

- Phase: single phase (SP) oscillator, quadrature phase (QP) oscillator or a multiphase (MP) oscillator,

- Order of characteristic equation: second order and higher order oscillators.

Circuits which provide sinusoidal oscillations at a single frequency and at a single output are termed as SP oscillators. The QP oscillators provide two quadrature phased outputs at single frequency and find vast application in communication. The MP oscillators provide multiple equally phased oscillations of a single frequency. The widespread usage of the MP oscillators [34]–[53] in telecommunication systems; power electronics, instrumentation and control systems are well known. Few sinusoidal oscillators using VDBA and its variant [61], [82], [85]–[91] have been proposed in literature which are summarized below in Table 1.3.

Table 1.3 Literature summary for oscillator using VDBA

Reference No.	No. of ABB	Order	Passive components R+C	Independent control of FO and CO	Supply Voltage (V)	Output phase	Output node impedance	Technology used
[90]	2 VDIBA	2	1+2	Yes	0.9	SP	Low	CMOS 0.18 µm
[87]	1 VDBA	3	2+3	Yes	1.5	QP	Low	CMOS 0.35 µm
[88]	2 VDBA	3	1+3	Yes	1.5	QP	Low	CMOS 0.18 µm
[89]	2 VDBA	3	1+3	Yes	0.9	QP	One phase – High ,One Phase - Low	CMOS 0.18 µm
[91]	2 VDBA	2	1+2	Yes	1.5	QP	Low	CMOS 0.35 µm
[85]	2 FB-VDBA	2	7+4	Yes	--	QP	Low	OPA860
[86]	1 FB-VDBA	2	1+2	Yes	5	QP	Low	OPA860
[61]	2 DO-VDBA	2	3+2	Yes	1.2	MP	Low	OPA860
[82]	2 VDIBA	2	0+2	Yes	0.9	QP	1 phase – High, 1 Phase – Low	CMOS 0.18 µm
			1+2	Yes		MP	2 Phase – High 2 Phase – low	

*FO- Frequency of oscillation, CO- Condition for oscillation.

It may be noted that very limited literature is available on oscillators; therefore, additional topologies may be explored.

1.3 Objectives

Following objectives are set after identifying the research gaps through extensive literature review:

1. To design a low power VDBA that provides high transconductance gain (g_m) with high bandwidth (BW).
2. To develop VDBA based high CMRR instrumentation amplifier.
3. To develop a new filter configuration using single ABB with moderate component spread; having independent tuning of ω_0 and Q_0. Further, to explore the possibility of designing universal filter configuration and first order all pass filter.
4. To realize non-linear functions like multiplication, squaring and square rooting using VDBA.
5. To design sinusoidal oscillators.

1.4 Thesis Organization

Chapter 1

This chapter presents a brief on the evolution of CM ABBs and their significance in signal processing applications. Further, a detailed review of existing literature on VDBA, its variants and their applications are presented to identify the research gap.

Chapter 2

In this chapter detailed study of CMOS based VDBA and DO-VDBA is presented to lay the ground for further reported work. Characterization of CMOS VDBA and DO-VDBA circuits has been carried out through SPICE simulations using 0.18 μm CMOS technology node. These realizations are used for functional verification of proposed

work in the thesis. The VDBA realization using commercially available IC AD844 is presented further to be is used for experimental verification of proposed structures.

Chapter 3

A low power VDBA structure is presented in this chapter. Detailed DC and AC analyses of the proposed structure are presented. The structure is further verified through pre and post layout simulations and is tested for its robustness and sensitivity through PVT and Monte Carlo analyses.

Chapter 4

This chapter presents VDBA based linear applications. A high CMRR instrumentation amplifier using a single VDBA is presented first which is followed by filter applications. Three filter applications are developed out of which the first order APF and second order SISO multifunction filter are designed using single ABB whereas the MISO universal filter is designed using two VDBAs. The effect of device non-ideality on instrumentation amplifier and filter parameters has been analyzed. Sensitivity analyses are also carried out to find the dependence on the passive elements. The workability of all propositions is verified through simulations.

Chapter 5

This chapter is devoted to non-linear applications of VDBA. A multiplier, a squaring circuit and a square rooting circuit are developed wherein the multiplier employs two DO-VDBAs while the later ones use single VDBA only. The functionality of all three propositions is confirmed through simulations. Post layout simulations are also included for squaring and square rooting circuits.

Chapter 6

This chapter delves into the designing of signal generators. A new structure for the realization of a single phase sinusoidal oscillator using a single VDBA is presented first. Three quadrature phase and two multiphase sinusoidal oscillators are also proposed. The functionality of proposed structures is tested through simulation and experimental work.

Chapter 7

In Chapter 7, the presented work is summarized and concluded with a thought on the prospective future scope.

CHAPTER 2

2.1 Introduction

The conceptual model of VDBA was first proposed in [1] by biolek et.al. The VDBA consists of an input voltage differencing stage and the output current is equal to transcoductance times the voltage difference of stage one. Further a voltage terminal at low impedance is also available, thus adding design flexibility. Thus it can be understood as a tansconductance amplifier (TA) followed by a voltage buffer. Bias dependent transcoductance adds the feature of electronic tunabilty of circuit parameters. Thus the VDBA has emerged as a promising choice for both VM and CM analog applications in recent past.

In this chapter, ideal VDBA and DO-VDBA are discussed first followed by their non-ideal models. A detailed analysis of the CMOS realizations of VDBA [33] and DO-VDBA [61] which are used in this thesis is presented next. In this chapter, a CFOA based implementation of VDBA is also proposed. All these VDBA structures are characterized using SPICE simulations. The MOSFET based resistor realization [92] has also been presented which is utilized in some of the proposed structures.

2.2 The Ideal VDBA and DO-VDBA

The VDBA is a four terminal block as shown in Figure 2.1 which is ideally characterized by the matrix (2.1).

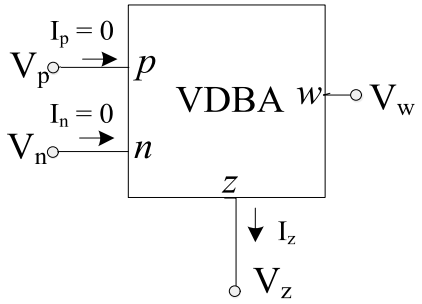


Figure 2.1 Symbol of VDBA

$$\begin{bmatrix} I_z \\ V_w \\ I_p \\ I_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & g_m & -g_m \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ V_p \\ V_n \end{bmatrix} \tag{2.1}$$

It may be observed from (2.1) that the *p* and *n* are the high impedance voltage input terminals whereas the *z* is the high impedance current output terminal providing a current which is g_m times input voltage difference. The *w* terminal replicates the voltage of *z* terminal at low impedance.

The VDBA can be modified to DO-VDBA simply by the addition of a voltage inverter. This adds flexibility to circuit design and is useful for differential mode signal operations. The symbol for DO-VDBA is shown in Figure 2.2.

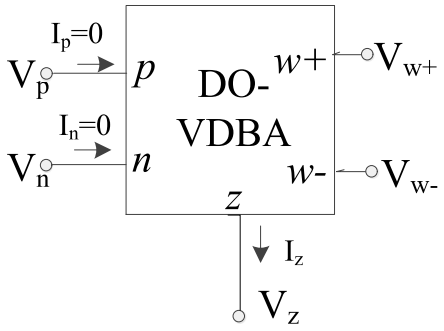


Figure 2.2 Symbol of DO-VDBA

Terminal characteristics of DO-VDBA may be expressed as

$$\begin{bmatrix} Iz \\ Vw+ \\ Vw- \\ Ip \\ In \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & g_m & -g_m \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} Vz \\ Iw+ \\ Iw- \\ Vp \\ Vn \end{bmatrix} \tag{2.2}$$

2.3 Non-Ideal Model

The VDBA and DO-VDBA characterized by (2.1) and (2.2) respectively describe their ideal behavior and do not account for various non-idealities associated with the active blocks.

The non-idealities in a VDBA may arise from:

i. The parasitic related to *p, n* and *z* terminals

ii. Tracking error in transconductance gain

iii. Tracking error in unity voltage transfer ratio from port *z* to *w*

The non-ideal model of VDBA is shown in Figure 2.3 wherein the parasitic resistance and capacitance associated with a terminal '*i*' are denoted as R_i and C_i respectively such that '*i*' may represent any of p, n and z terminals. Considering the non-idealities, the VDBA terminal characteristics get modified as

$$\begin{bmatrix} I_z \\ V_w \\ I_p \\ I_n \end{bmatrix} = \begin{bmatrix} 1/Z_z & 0 & \alpha g_m & -\alpha g_m \\ \beta & 0 & 0 & 0 \\ 0 & 0 & 1/Z_p & 0 \\ 0 & 0 & 0 & 1/Z_n \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ V_p \\ V_n \end{bmatrix} \tag{2.3}$$

Where α and β represent the non-ideal transconductance gain and non-ideal buffer transfer ratio respectively and should ideally be equal to unity.

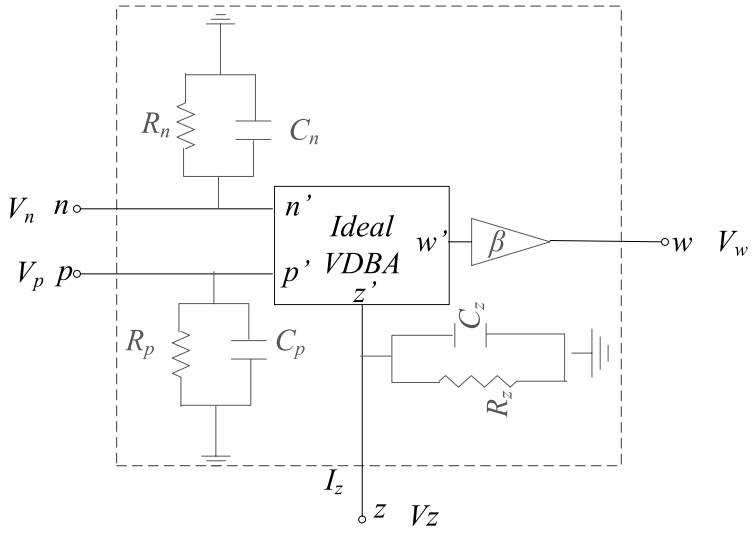


Figure 2.3 Non-ideal model of VDBA

Taking the non-idealities due to tracking errors into consideration the DO-VDBA terminal characteristics get modified as

$$\begin{bmatrix} Iz \\ Vw+ \\ Vw- \\ Ip \\ In \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \alpha_p(s)g_m & -\alpha_n(s)g_m \\ \beta_p(s) & 0 & 0 & 0 & 0 \\ -\beta_n(s) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} Vz \\ Iw+ \\ Iw- \\ Vp \\ Vn \end{bmatrix} \tag{2.4}$$

2.4 Implementation of VDBA

In this section, the CMOS implementation of VDBA [33] which is used for verification of applications proposed in this work is discussed.

The complete schematic of the VDBA [33] is shown in Figure 2.4 wherein the circuit consisting of transistors (M_1-M_9) represents the TA unit and that consisting of (M_{10}-M_{16}) is the voltage buffer circuit.

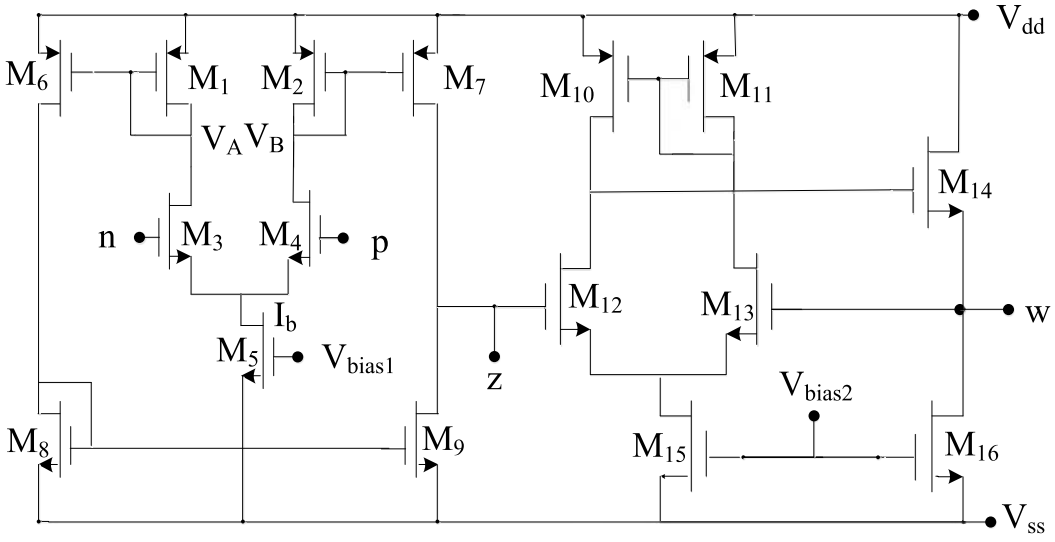
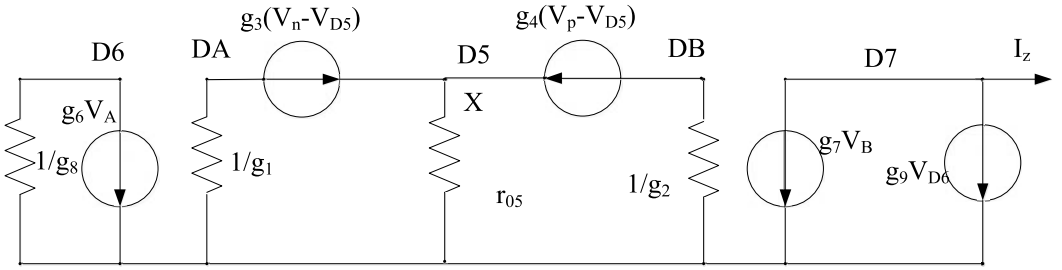
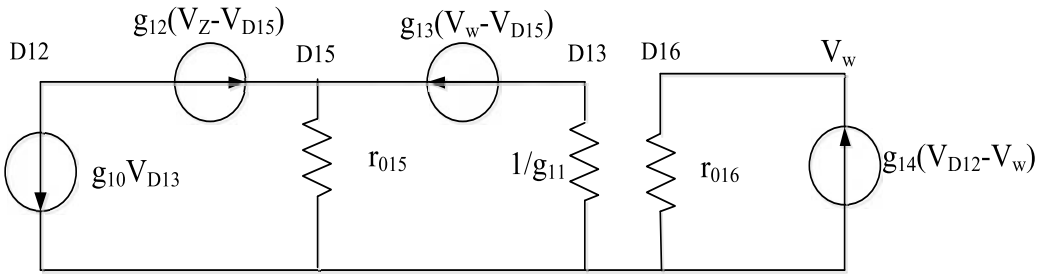


Figure 2.4 CMOS VDBA [33]

The small signal equivalent of CMOS VDBA of Figure 2.4 is drawn in Figure 2.5. The small signal equivalent circuits of TA and buffer are shown in Figures 2.5 (a) and (b) respectively, where D_i represents the drain of i^{th} transistor and g_i is corresponding transconductance.



(a)



(b)

Figure 2.5 Small signal equivalent of (a) TA and (b) buffer

The nodal equations at nodes D5, DA, DB, D6 and D7 can be expressed by (2.5)-(2.9) respectively.

$$g_3 V_n + g_4 V_p = (g_3 + g_4) V_X \tag{2.5}$$

$$-g_1 V_A = g_3 (V_n - V_X) \tag{2.6}$$

$$-g_2 V_B = g_4 (V_p - V_X) \tag{2.7}$$

$$-g_8 V_{D6} = g_6 V_A \tag{2.8}$$

$$-g_7 V_B - g_9 V_{D6} = I_z \tag{2.9}$$

Substituting V_{D6} from (2.8), (2.9) modifies to

$$-g_7 V_B + \frac{g_6 g_9}{g_8} V_A = I_z \tag{2.10}$$

By considering $g_2 = g_7$ and $g_6 = g_9 = g_8 = g_1$, and using (2.6) and (2.7) and (2.10), the I_z may be expressed as

$$g_4 (V_p - V_x) - g_3 (V_n - V_x) = I_z \tag{2.11}$$

From (2.5) and (2.11), the I_z may be expressed as

$$g_4 V_p - g_3 V_n + \frac{(-g_4 + g_3)(g_3 V_n + g_4 V_p)}{(g_4 + g_3)} = I_z$$

(2.12)

$$I_z = \frac{2 g_3 g_4}{(g_3 + g_4)} (V_p - V_n)$$

(2.13)

Thus the g_m may be obtained as

$$g_m = \frac{I_z}{(V_p - V_n)} = \frac{2 g_3 g_4}{(g_3 + g_4)}$$

(2.14)

Further the small signal analysis of buffer can be carried out to establish relation between V_w and V_z.

The nodal equation at node D16 of Figure 2.5 (b) is expressed as

$$g_{14} r_{016} V_{D12} = (1 + g_{14} r_{016}) V_w$$

(2.15)

Assuming $g_{14} r_{016} >> 1$, (2.15) may be rewritten as

$$V_{D12} = V_w$$

(2.16)

Similarly, the nodal equations at node D15, D12, D13 can be respectively expressed as

$$g_{12}(V_z - V_{D15}) = -g_{13}(V_w - V_{D15})$$

(2.17)

$$-g_{10}V_{D13} = g_{12}(V_z - V_{D15})$$

(2.18)

$$-g_{11}V_{D13} = g_{13}(V_w - V_{D15})$$

(2.19)

From (2.18) and (2.19)

$$\frac{g_{12}}{g_{10}}(V_z - V_{D15}) = \frac{g_{13}}{g_{11}}(V_w - V_{D15})$$

(2.20)

Considering $g_{10}=g_{11}$ and $g_{12}=g_{13}$, and substituting the value of V_{D15} from (2.17)

$$V_z - \frac{V_z + V_w}{2} = V_w - \frac{V_z + V_w}{2}$$

(2.21)

$$V_z = V_w$$

(2.22)

2.4.1 Simulation Results

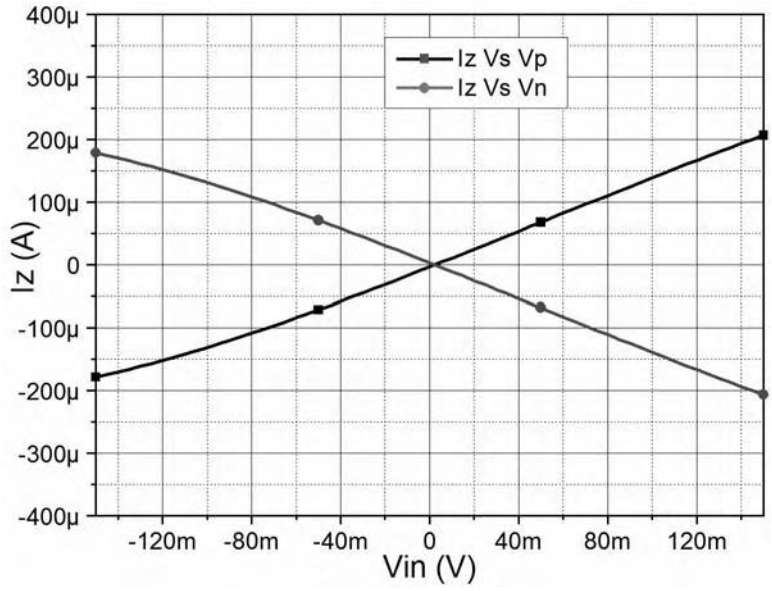
The functionality of VDBA is verified through SPICE simulations using TSMC 0.18 μm process parameters. The supply voltages are set to ± 0.9 V. The bias voltages V_{bias1} and V_{bias2} are taken as 0.5 V and -0.25 V respectively. The VDBA shown in Figure 2.4 is simulated for the aspect ratios listed in Table 2.1.

Table 2.1 Aspect ratio of VDBA of Figure 2.4

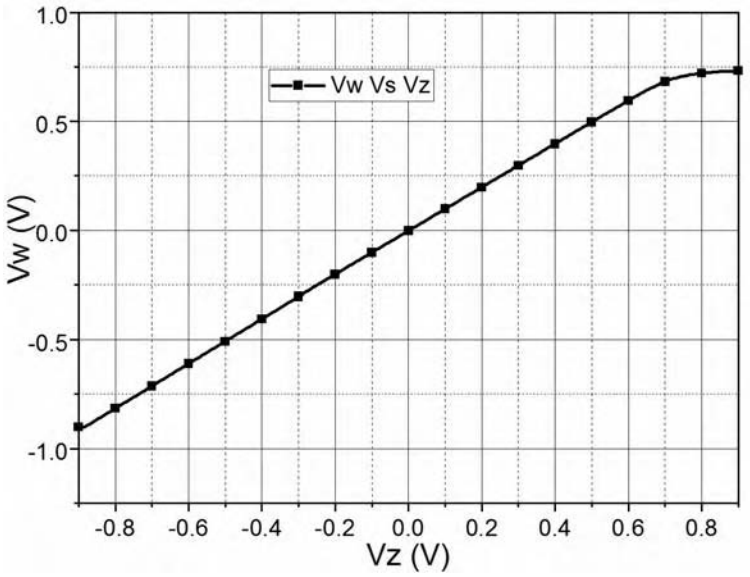
Transistor	W(µm)/L(µm)
M_1-M_4, M_{12}-M_{13}, M_{15}-M_{16}	3.6/0.18
M_5	1.8/0.36
M_6-M_7	10.8/0.36
M_8-M_9	3.6/0.36
M_{10}-M_{11}, M_{14}	7.2/0.18

2.4.1.1 DC Characteristics

The DC characteristics obtained from the simulations are depicted in Figure 2.6. The variation of I_z with V_p and V_n is shown in Figure 2.6 (a). Similarly, the variation in V_w with respect to (w.r.t) V_z is depicted in Figure 2.6 (b). It may be witnessed that V_w follows V_z linearly for a voltage range of (-0.7 V to 0.7 V). Thus the terminal relations of VDBA are verified.



(a)

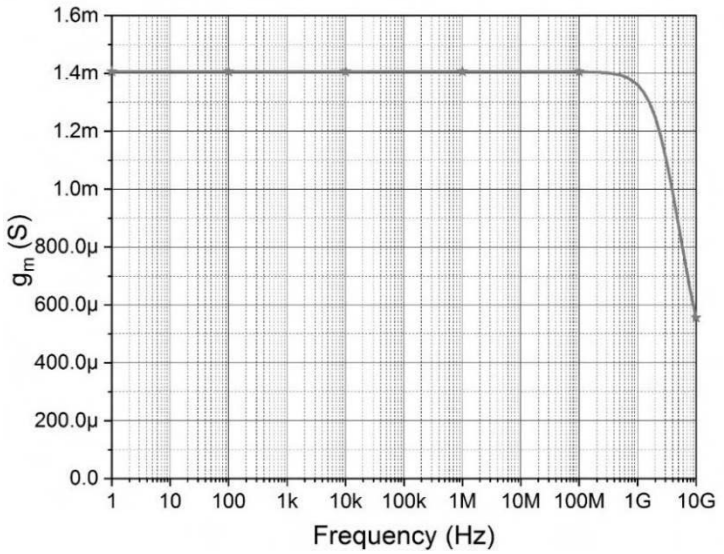


(b)

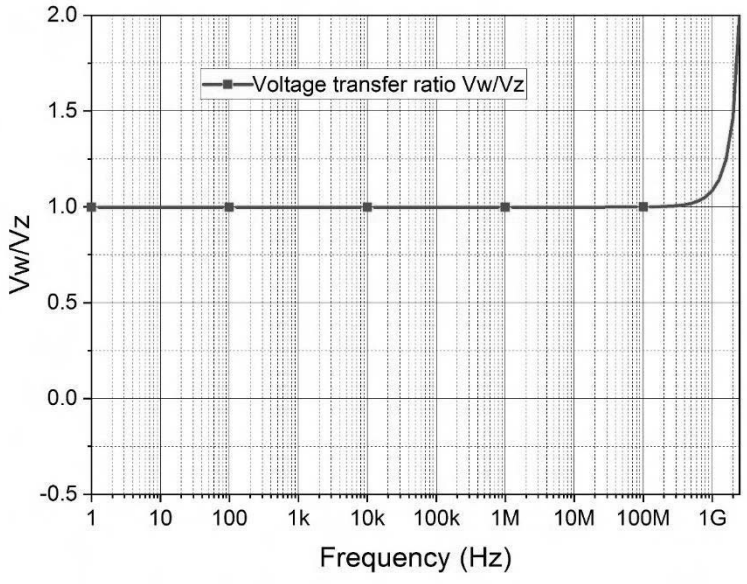
Figure 2.6 DC characteristics of (a) TA and (b) buffer

2.4.1.2 AC Characteristics

This subsection presents the verification of the AC behavior of the VDBA. The simulated frequency response for TA is shown in Figure 2.7 (a). For the given settings the g_m is obtained as 1.4 mS and the bandwidth of the TA unit is observed to be 3 GHz. The frequency response of buffer is depicted in Figure 2.7 (b) and the unity gain BW (UGB) is observed to be 560 MHz.



(a)



(b)

Figure 2.7 AC characteristics of (a) TA and (b) buffer

2.5 Implementation of DO-VDBA

In this section, the CMOS implementation of DO-VDBA [61] which is used for verification of few applications proposed in this work is discussed.

The CMOS DO-VDBA [61] is shown in Figure 2.8 that uses single ended transconductance input stage and two simple voltage inverters. The small signal equivalents of TA and buffer of DO-VDBA are depicted in Figure 2.9. The D_i represents the drain of i^{th} transistor and g_i is corresponding transconductance. The R_b represent the resistances of the current source I_{bias}.

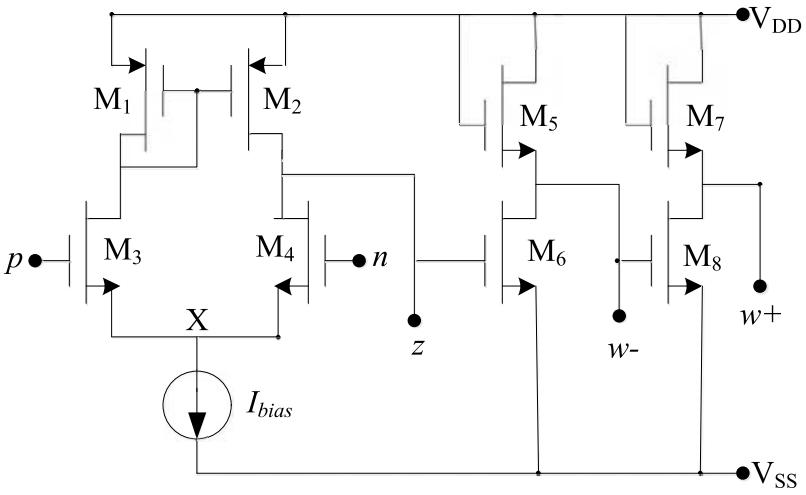
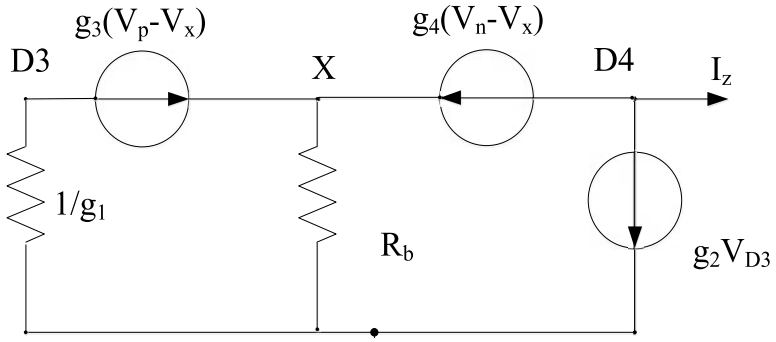
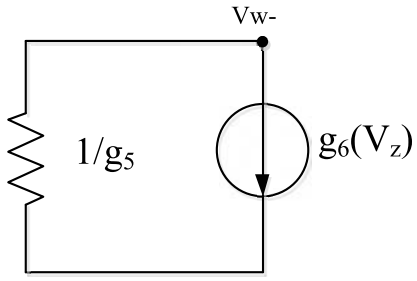


Figure 2.8 CMOS implementation of the DO-VDBA [61]



(a)



(b)

Figure 2.9 Small signal equivalent model of (a) TA and (b) inverting buffer

By applying KCL at node X, D3 and D4 respectively the following equations are obtained by assuming $g_3+g_4 >> 1/R_b$

$$g_3V_p + g_4V_n = (g_3 + g_4)V_X \tag{2.23}$$

$$g_1 V_{D3} = g_3 (V_p - V_X)$$

(2.24)

$$-g_4 (V_n - V_X) - g_2 (V_{D3}) = I_z$$

(2.25)

Substituting the value of V_{D3} and V_x from (2.23) and (2.24) in (2.25) and considering $g_2 = g_1$, the I_z can be written as

$$\frac{2g_3 g_4}{(g_3 + g_4)} (V_p - V_n) = I_z$$

(2.26)

Thus the g_m of DO-VDBA may be expressed as

$$g_m = \frac{I_z}{(V_p - V_n)} = \frac{2g_3 g_4}{(g_3 + g_4)}$$

(2.27)

Similarly for Figure 2.9 (b), to obtain the relation for inverter, the nodal equation can be written as

$$V_{W-} = -\frac{g_6}{g_5} V_z$$

(2.28)

Considering $g_6 = g_5$

$$V_{W-} = -V_Z$$

(2.29)

Similarly for buffer comprising of M_7 and M_8 considering $g_7 = g_8$ the output of w_+ terminal can be written as

$$V_{W+} = V_Z \tag{2.30}$$

2.5.1 Simulation Results

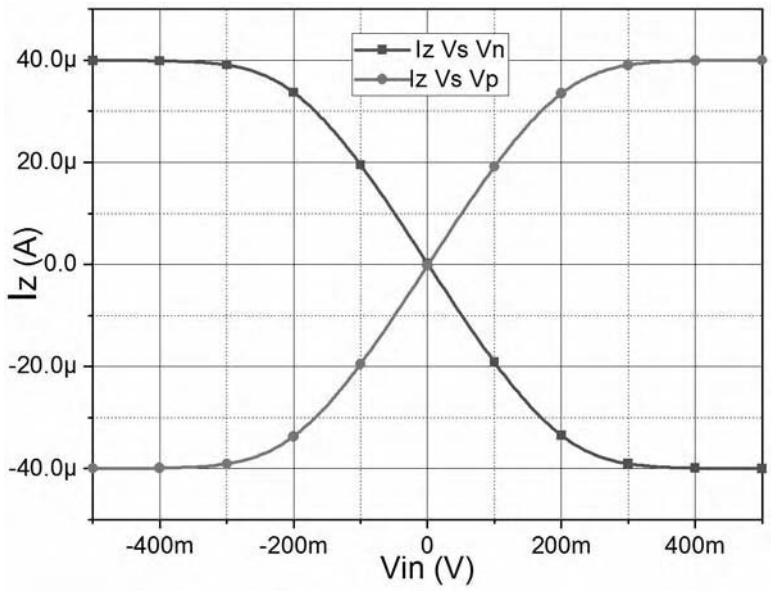
The functionality of DO-VDBA is confirmed through SPICE simulations using TSMC 0.18 µm process parameters. The bias current I_{bias} is set to 40 µA. The supply voltages are set to ±1 V. The DO-VDBA shown in Figure 2.8 is simulated for transistor aspect ratios enlisted in Table 2.2.

Table 2.2 Aspect ratio of DO-VDBA of Figure 2.8

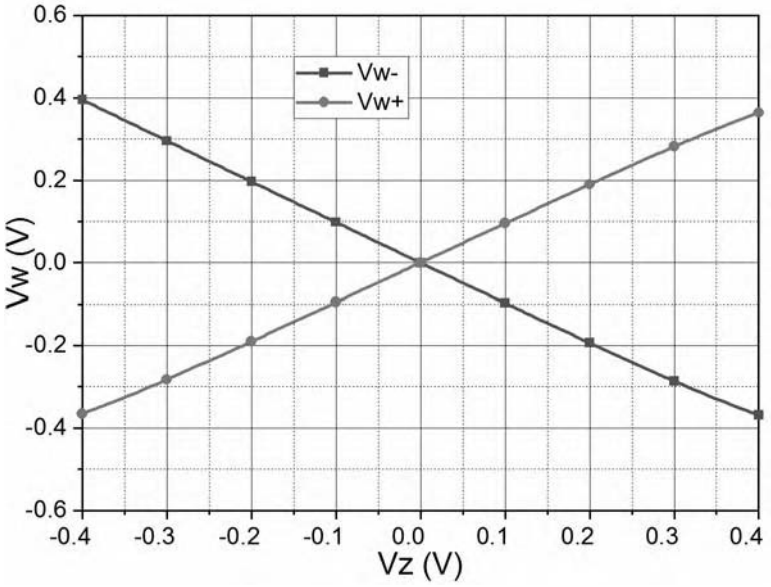
Transistor	W(µm)/L(µm)
M_1-M_4	7.2/1.8
M_5-M_8	27/.54

2.5.1.1 DC Characteristics

The DC characteristics obtained from simulations are depicted in Figure 2.10. The variation of I_z with V_p and V_n is shown in Figure 2.10 (a). Similarly the variation in V_{w+}/V_{w-} (w.r.t) V_z is shown in Figure 2.10 (b).



(a)

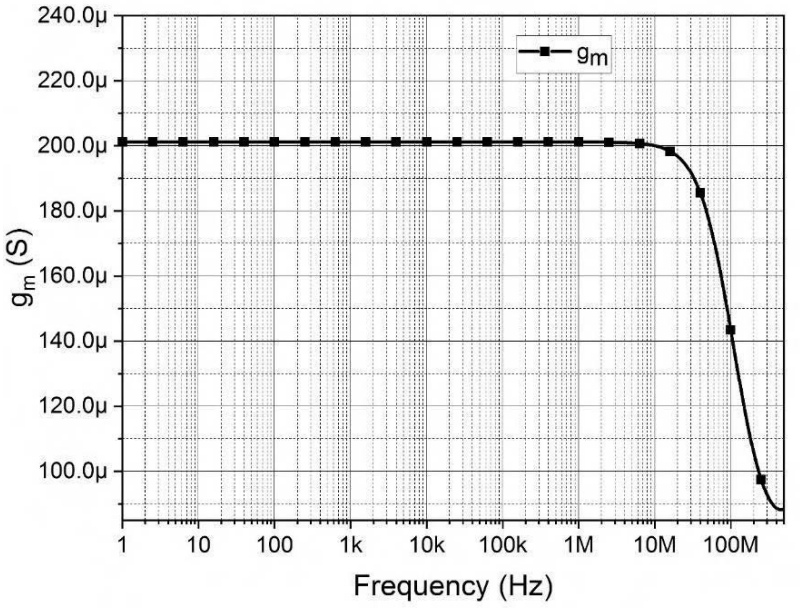


(b)

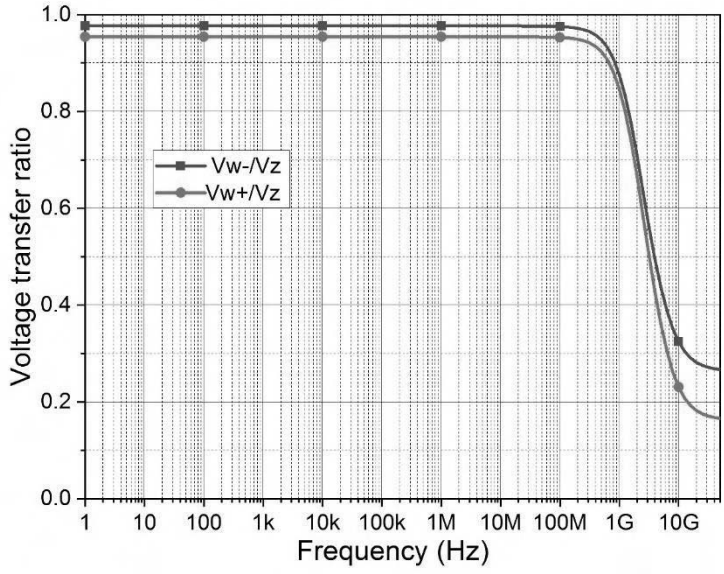
Figure 2.10 DC characteristics of (a) TA and (b) buffer

2.5.1.2 AC Characteristics

The frequency response of TA is depicted in Figure 2.11 (a) and the 3 dB frequency for the same is obtained as 103 MHz. Further, Figure 2.11 (b) shows the frequency response of the buffer. The simulated unity gain BW is observed to be 200 MHz.



(a)



(b)

Figure 2.11 AC characteristics of (a) TA and (b) buffer

2.6 The CFOA based Implementation of VDBA

This section describes the VDBA realization using CFOA which is available as off the shelf IC AD 844. The symbol of CFOA is shown in Figure 2.12 and the terminal relations are described by $I_y = 0$, $V_x = V_y$; $I_z = I_x$, $V_w = V_z$.

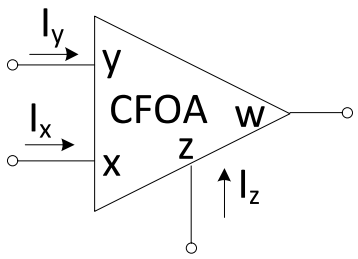


Figure 2.12 CFOA symbol

A VDBA can be realized using two CFOAs and a resistor R_g connected as shown in Figure 2.13.

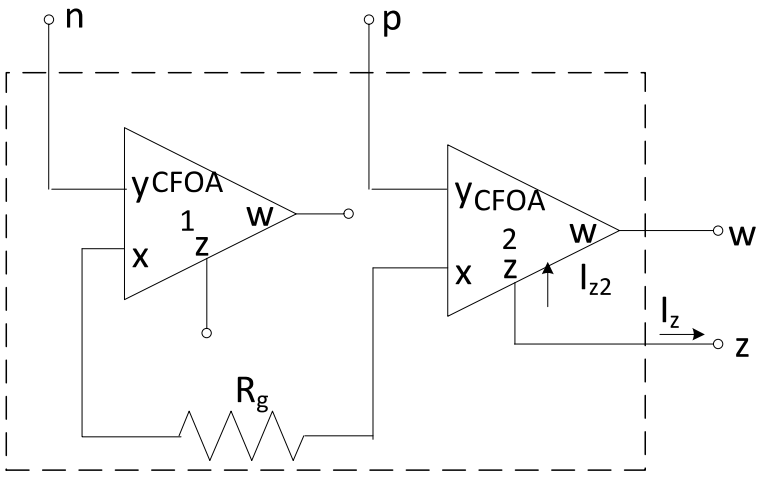


Figure 2.13 Proposed CFOA based VDBA

Using terminal characteristics of CFOA the port relations of VDBA of Figure 2.4 can be verified. The voltages at the '*x*' terminals of the CFOA 1 and CFOA 2 can be written as (2.31) and (2.32) respectively

$$V_{x1} = V_n \tag{2.31}$$

$$V_{x2} = V_p \tag{2.32}$$

The current at x terminal of second CFOA, denoted by $I_{x2,}$ is obtained as

$$I_{x2} = \frac{V_n - V_p}{R_g} \tag{2.33}$$

From Figure 2.13 it may be found that

$$I_z = -I_{z2} \tag{2.34}$$

From terminal characteristic of CFOA and (2.34), the output current I_z is computed as

$$I_z = \frac{V_p - V_n}{R_g} \tag{2.35}$$

As per the port relation of VDBA the current at *z* terminal is transconductance times the input differential voltage, thus from (2.35) it may be concluded that

$$g_m = \frac{1}{R_g} \tag{2.36}$$

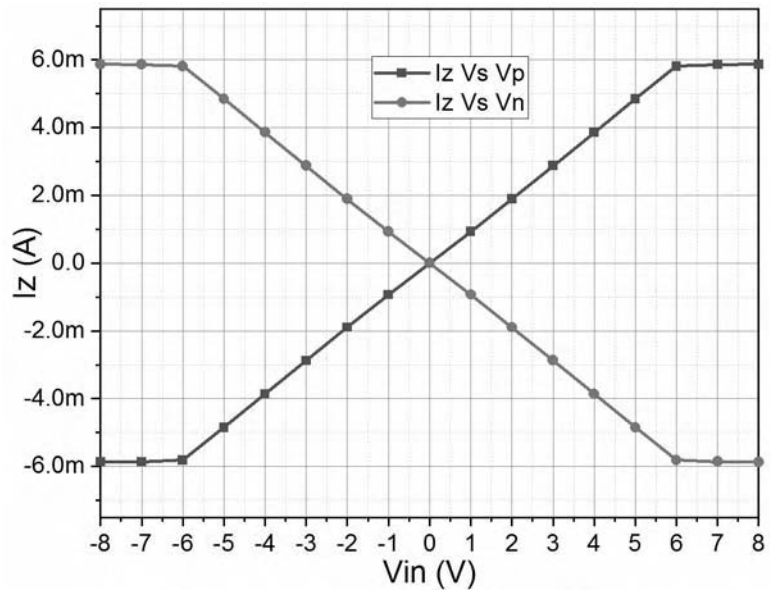
Thus the g_m of CFOA based VDBA is obtained as $1/R_g$.

2.6.1 Simulation Results

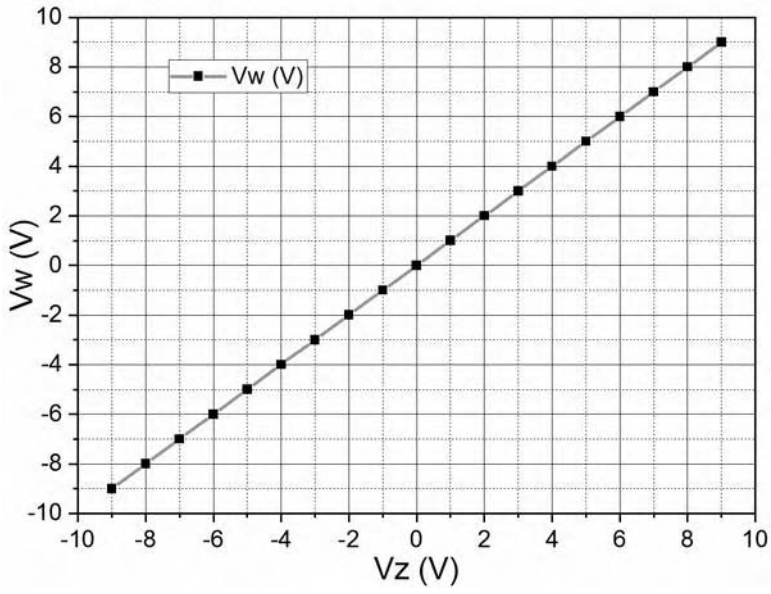
The terminal characteristics VDBA realized using CFOAs is verified through simulation using IC AD844. The supply voltages are set as ±12 V. The value of R_g is considered as 1 kΩ.

2.6.1.1 DC Characteristics

The DC characteristics of the CFOA based VDBA, obtained from simulations are depicted in Figure 2.14. The variation of I_z with V_p and V_n is shown in Figure 2.14 (a). Similarly, the variation in V_w w.r.t V_z is shown in Figure 2.14 (b).



(a)

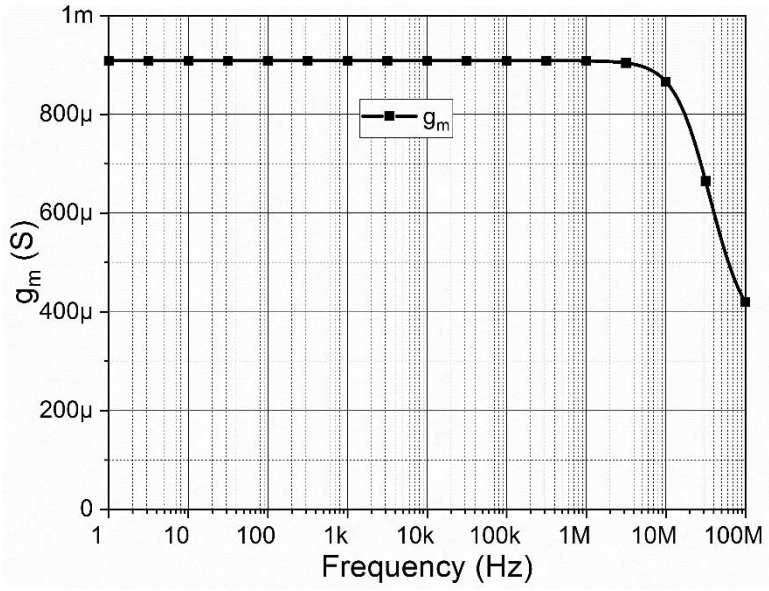


(b)

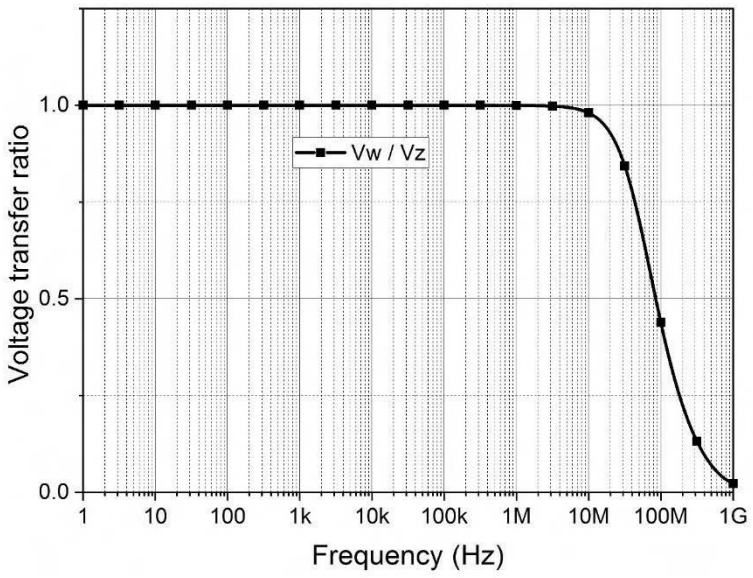
Figure 2.14 DC characteristics of (a) TA and (b) buffer

2.6.1.2 AC Characteristics

The AC characteristics of TA and buffer are depicted in Figures 2.15 (a) and (b) respectively. The 3 dB frequency of TA is obtained as 20 MHz and the unity gain BW is observed to be 10 MHz.



(a)



(b)

Figure 2.15 AC characteristics of (a) TA and (b) buffer

The statistics observed from the simulations of VDBA and DO-VDBA are given in Table 2.3.

Table 2.3 Parameters of VDBA and DO-VDBA

Parameters	**VDBA**		**DO-VDBA**
Technology used	CMOS 0.18 µm	Off the shelf IC AD844	CMOS 0.18 µm
Supply Voltages (V)	±0.9	±12	±1
Tuning Availability	Through V_{bias1}	--	Through I_{bias}
Linear Input Range of TA (mV)	±120	± 6000	±200
Linear Input Range of Buffer (V)	±0.7	±9	±0.4
Offset Current at Z-terminal (µA)	-3	0.19	0.19
Offset voltage at W-terminal (V)	2.6×10^{-3}	0	48×10^{-9} and 32×10^{-9}
Power Dissipation (mW)	1.56	325	6.58
g_m (µS)	1400	900	200
3dB BW (MHz)	3000	34	103
Vw+/Vz, Vw-/Vz	0.99	0.99	0.97, 0.95
UGB(MHz)	560	49	200

2.7 The NMOS Based Resistor Realization

This section briefly describes grounded resistor implementation based on two diode connected MOS transistors [92] as depicted in Figure 2.16.

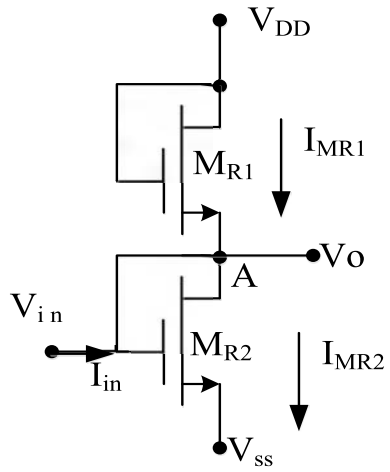


Figure 2.16 The NMOS based resistor (R) realization

Considering equal device dimensions of both transistors M_{R1} and M_{R2} and denoting the same by W_{MR}/L_{MR}, the nodal equation at node A can be expressed as

$$I_{in} = I_{MR2} - I_{MR1} \tag{2.15}$$

Using relation of drain current in saturation region the I_{in} can be expressed as

$$I_{in} = \frac{1}{2} K_R \left[\{V_{in} - V_{SS} - V_{TH}\}^2 - \{V_{DD} - V_{in} - V_{TH}\}^2 \right] \tag{2.16}$$

where $K_R = \mu_n C_{ox} \frac{W_{MR}}{L_{MR}}$ represents the process transconductance parameter. The μ_n and C_{ox} are mobility of electron and gate oxide capacitance respectively and V_{TH} is the threshold voltage of the transistor.

Considering $V_{DD} = -V_{SS}$

$$R = \frac{V_o}{I_{in}} = \frac{1}{2K_R (V_{DD} - V_{TH})} \tag{2.17}$$

It may be observed from (2.17) that the required resistance value may be obtained by varying the supply voltages. For verification of the concept, the nmos based resistor of Figure 2.16 is simulated for aspect ratio of $\frac{3.6\,\mu m}{1.8\,\mu m}$. The simulated values of resistor for different values of supply voltage thus obtained are shown in Figure 2.17.

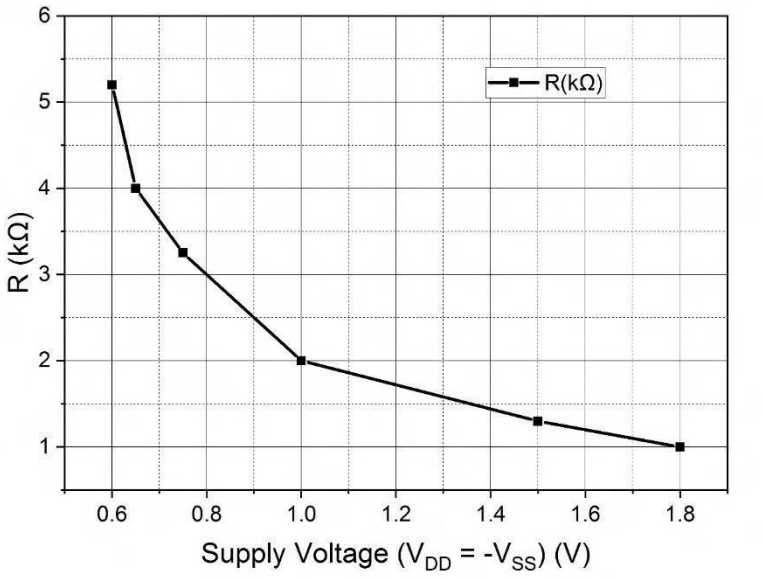


Figure 2.17 R Vs Supply voltage

2.8 Conclusion

This chapter is devoted to the basic understanding of the VDBA. The CMOS based VDBA and DO-VDBA structures which are used for circuit implementation in this thesis are described first. The non-idealities of VDBA and DO-VDBA are also discussed, which would be helpful in the performance evaluation of applications designed using these ABBs. Both the structures are characterized next using SPICE simulations. The CFOA based VDBA is also proposed which would come handy for experimental verification of the proposed circuits. The active resistor realization in VDBA based circuits is also presented in this chapter.

CHAPTER 3

3.1 Introduction

Portable electronic gadgets having a wide range of functionalities and longer battery operation are need of time. These requirements directly map into downscaling of CMOS processes and operations at lower supply voltages. In literature various techniques have been presented to meet reduced supply voltage requirements for digital and analog circuit design. The current-mode processing, using MOS transistors in the triode/ sub-threshold region, use of FGMOS/DTMOS and flip voltage follower (FVF) [93] are commonly followed practices for analog circuit design. The FVF is gaining the attention of researchers as a building block due to its ability to operate at low supply voltage. Differential flip voltage follower (DFVF) and fully differential flip voltage follower (FD-FVF) are other FVF structures which enhance the circuit performance in terms of increased slew rate and current driving capability [93]–[95].

A low power, high performance VDBA using differential flipped voltage followers (DFVF) has been presented in this chapter. The proposed structure is capable of providing high g_m at relatively low bias currents and relatively higher BW when compared to available VDBAs.

3.2 Differential Flipped Voltage Follower

For a better understanding of the proposed structure, the DFVF is first described briefly in this section. An *n* channel DFVF cell has been depicted in Figure 3.1 which comprises of three transistors. The transistors M_A and M_B form a source follower wherein the gate of M_A serves as input node and *x* is the output node. The current through M_A is kept constant independent of current at node *x* resulting in the constant gate to source voltage (V_{GS}) of M_A and thus the voltage at node *x* follows the node

voltage V_n. This source follower is known as FVF [93]. A differential FVF can be structured by adding an extra transistor M_C at node *x*. As the impedance at node *x* is very low [95] its voltage remains approximately constant for large input signals. A differential voltage $(V_p\text{-}V_n)$ generates current variations in M_C and hence in M_B too. Thus the DFVF is able to deliver a large amount of current when a differential voltage signal is applied to its input.

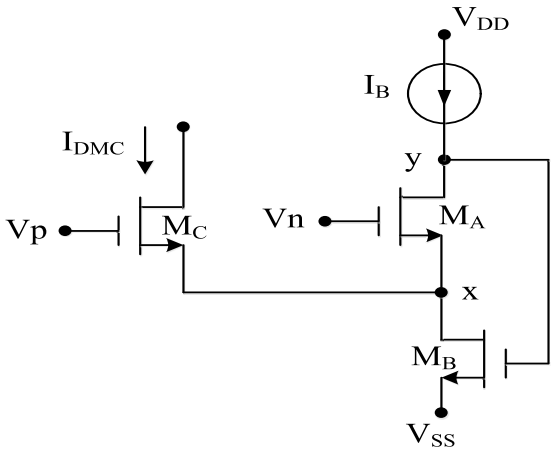


Figure 3.1 The DFVF structure [95]

3.3 Proposed Structure

This section presents the design of the proposed VDBA followed by its small signal analysis. In this work, the TA and the buffer used for designing the VDBA are implemented using DFVFs. Complete schematic of the proposed low voltage VDBA is shown in Figure 3.2 which consists of a TA block (M_1-M_8) and a voltage buffer (M_9-M_{14}). The TA is implemented using two DFVFs and a current mirror is used as an active load. In the TA circuit, output drain currents (I_{DM5} and I_{DM6}) are proportional to the differential input voltages $(V_p\text{-}V_n)$ and $(V_n\text{-}V_p)$ respectively and I_z is the difference between I_{DM5} and I_{DM6}. If M_1, M_2, M_5 and M_6 are completely matched transistors and a common mode signal is applied (i.e. V_p=V_n) then I_{DM5} = I_{DM6} = I_{B1}. A variation in

differential input voltage (V_p-V_n) results in proportionate variations in output currents (I_{DM5} and I_{DM6}) [93], [94].

The voltage buffer in the proposed configuration is designed using two complementary DFVFs. The buffer circuit offers low output impedance with moderate output voltage swing [95]. When the input signal V_z increases with respect to the output voltage V_w, nodes A and B, as shown in Figure 3.2 also follow this variation. Thus, the source to gate voltage of M_{14} increases whereas the gate to source voltage of M_{13} decreases. This causes the current through $M_{14,}$ to increase, and the current through M_{13} to decrease. This generates a positive output current which in turn increases the output voltage V_w until it reaches a value V_z. A similar explanation may be presented when the input voltage decreases with respect to the output voltage V_w.

The input common mode range (ICMR) is an important parameter for TA and is defined as the difference of upper ($V_{IC\ Max}$) and lower ($V_{IC\ Min}$) voltage limits for which the transistors remain in the saturation region. The $V_{IC\ Max}$ should ensure that the transistors M_7 and M_5 remain in saturation and may be computed as

$$V_{IC\,Max} = V_{DD} - \left|V_{OV\_M7}\right| + V_{TH\_M5} \tag{3.1}$$

Similarly, the $V_{IC\ Min}$ should be sufficient enough to keep M_3 and M_5 in saturation, thus, $V_{IC\ Min}$ may be expressed as

$$V_{IC\,Min} = -V_{SS} + V_{OV\_M3} + V_{OV\_M5} + V_{TH\_M5} \tag{3.2}$$

Thus the ICMR expressed as V_{ICMR} is given by

$$V_{ICMR} = V_{ICMax} - V_{ICMin} \tag{3.3}$$

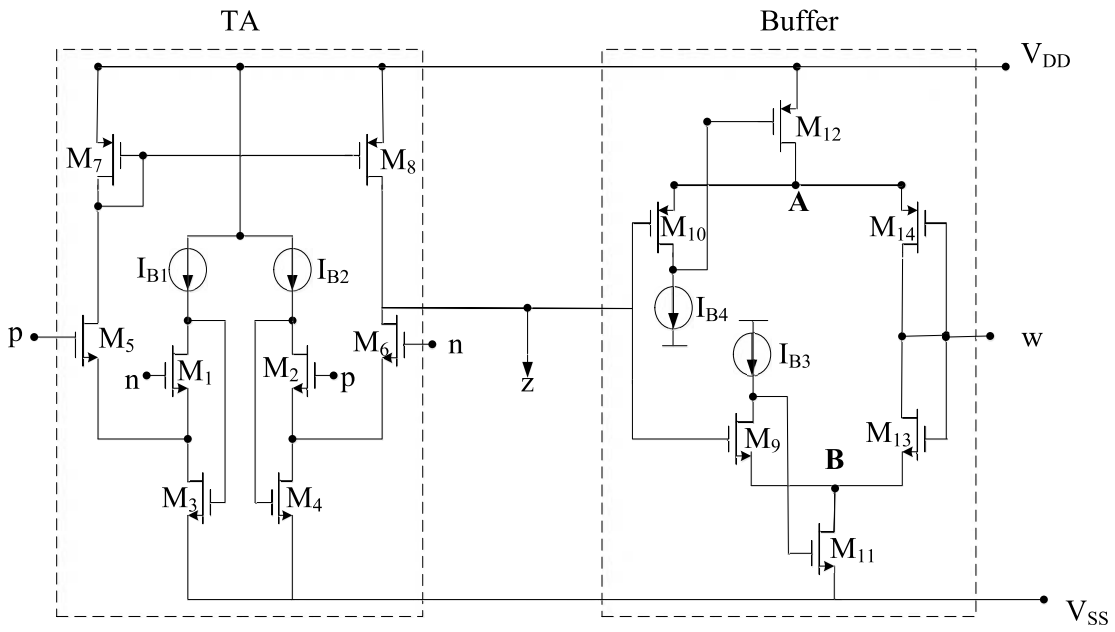


Figure 3.2 Proposed VDBA

3.3.1 Small Signal Analysis

This section presents the mathematical formulation for g_m of TA followed by the buffer transfer ratio using small signal analysis. Low frequency small signal model of the transistor is used for analysis and the body effect is neglected.

The small signal equivalent of TA is shown in Figure 3.3 where D_i represents the drain of i^{th} transistor and g_i is corresponding transconductance. The g_i is given by $\sqrt{2I_{Bi}\mu_n C_{ox}\left(W/L\right)_k}$ where I_{Bi} is the bias current of i^{th} transistor. The R_{b1} and R_{b2} represent the resistances of the current sources I_{B1} and I_{B2} respectively. The source resistances can be considered to be equal ($R_{b1} = R_{b2} = R_b$) if I_{B1} and I_{B2} are considered as equal ($I_{B1} = I_{B2} = I_B$).

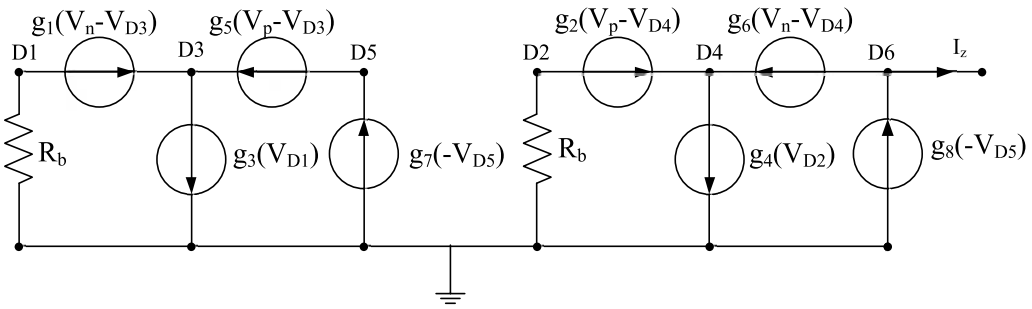


Figure 3.3 Small signal model of TA

Nodal equations at node D1, D3 and D5 may respectively be exp ressed as

$$V_{d1} = g_1 R_b (V_{d3} - V_n)$$

(3.4)

$$g_1(V_n - V_{d3}) + g_5(V_p - V_{d3}) = g_3 V_{d1}$$

(3.5)

$$g_5 V_p - g_5 V_{d3} = g_7 V_{d5}$$

(3.6)

Considering conductance of M_1, M_3 and M_5 to be equal and $R_b >> 1$, the V_{d5} may be obtained as

$$V_{d5} = (V_p - V_n)\frac{g_5}{g_7}$$

(3.7)

Similarly, applying KCL at D2, D4 and D6 and eliminating node voltages the output current I_z may be deduced as

$$I_z = g_8 V_{d5} - g_6(V_n - V_{d4})$$

(3.8)

Considering conductances of M_2, M_4, M_6, M_7 and M_8 to be same and eliminating V_{d4} and V_{d5}, the I_z may be expressed as

$$I_z = (g_5 + g_6)(V_p - V_n)$$

(3.9)

Thus the transconductnce of TA, defined as ratio $I_z/(V_p-V_n)$ and represented by g_m, can be expressed as

$$g_m = (g_5 + g_6)$$

(3.10)

Small signal equivalent for the buffer is drawn in Figure 3.4 and is used to establish the relation between V_w and V_z. The R_{b3} and R_{b4} represent resistances of the current source I_{B3} and I_{B4} respectively. Since $I_{B3} = I_{B4}$ their respective source resistances are considered to be equal ($R_{b3} = R_{b4} = R_b$).

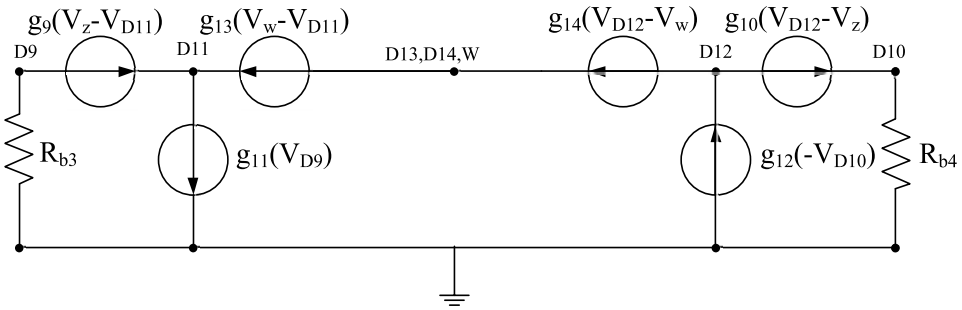


Figure 3.4 Small signal model of buffer

The KCL at D9, D11, D12, D13, may respectively be written as:

$$-g_9 R_b (V_z - V_{d11}) = V_{d9}$$

(3.11)

$$g_9 V_z + g_{13} V_w = (g_9 + g_{13}) V_{d11} + g_{11} V_{d9}$$

(3.12)

$$g_{10} V_z + g_{14} V_w = (g_{10} + g_{14}) V_{d12} - g_{12} V_{d10}$$

(3.13)

$$(g_{13}+g_{14})V_w = g_{14}V_{d12} + g_{13}V_{d11}$$

(3.14)

$$-g_{10}R_b(V_z - V_{d12}) = V_{d10}$$

(3.15)

Substituting the value of V_{d9} from (3.11) in (3.12) results in

$$V_z(g_9 + g_9 g_{11}R_b) + g_{13}V_w = V_{d11}(g_9 + g_{13} + g_9 g_{11}R_b)$$

(3.16)

By eliminating V_{d10} from (3.13) and (3.15) gives

$$V_z(g_{10} + g_{10}g_{12}R_b) + g_{14}V_w = V_{d12}(g_{10} + g_{14} + g_{10}g_{12}R_b)$$

(3.17)

Assuming $g_9=g_{10}=g_{13}=g_{14}=g_x$ and $g_{11}=g_{12}=g_y$, (3.13), (3.16) and (3.17) can be written as (3.18), (3.19) and (3.20) respectively.

$$V_w = \frac{V_{d11} + V_{d12}}{2}$$

(3.18)

$$V_z(1 + g_y R_b) + V_w = V_{d11}(2 + g_y R_b)$$

(3.19)

$$V_z(1 + g_y R_b) + V_w = V_{d12}(2 + g_y R_b)$$

(3.20)

Solving (3.18)-(3.20) the output voltage V_w may be expressed as

$$V_w = V_z$$

(3.21)

Hence it may be concluded that the output voltage V_w of the buffer follows its input voltage V_z.

3.3.2 Simulation Results

The proposed VDBA is characterized through simulations using Cadence Virtuoso analog design environment (ADE) spectre tool at 0.18 µm generic process design kit (GPDK) CMOS technology. The supply voltages of ± 0.7 V are used for simulations. The layout of the proposed VDBA with physical verification checks such as design rule check (DRC) and layout vs. schematic check (LVS) is shown in Figure 3.5 which occupies active die area of 18.95 µm × 31.96 µm. Both pre and post layout simulations are carried out which have been described in the following subsections. Dimensions of the MOS transistors used are enlisted in Table 3.1.

Table 3.1 Dimensions of the MOS transistors used

Transistor	W(µm)/L(µm)
M_1-M_6, M_9, M_{11}, M_{13}	3.6/0.18
M_7-M_8, M_{10}, M_{12}, M_{14}	7.2/0.18

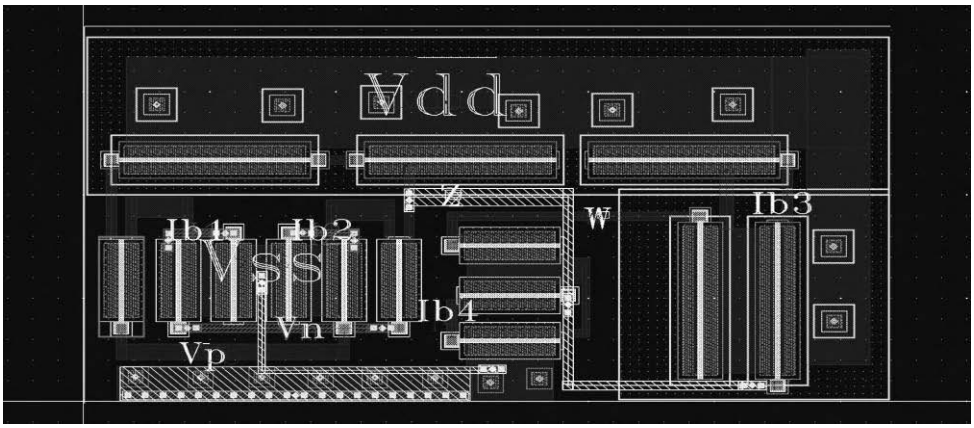
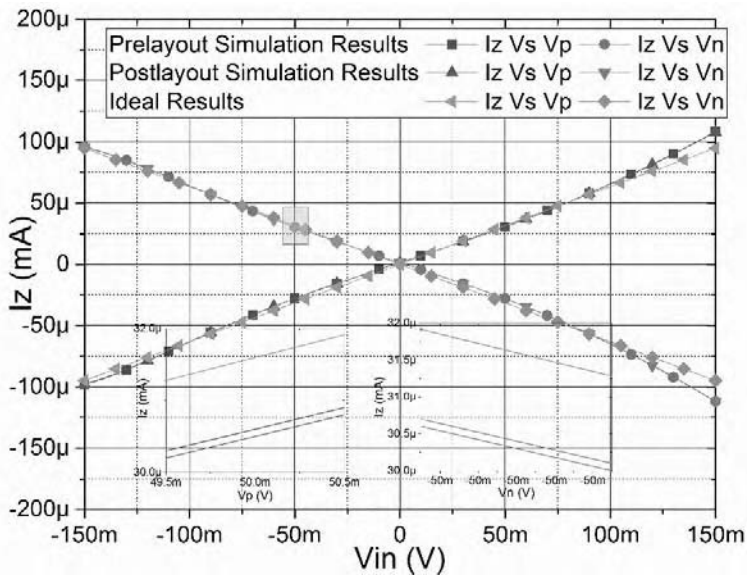


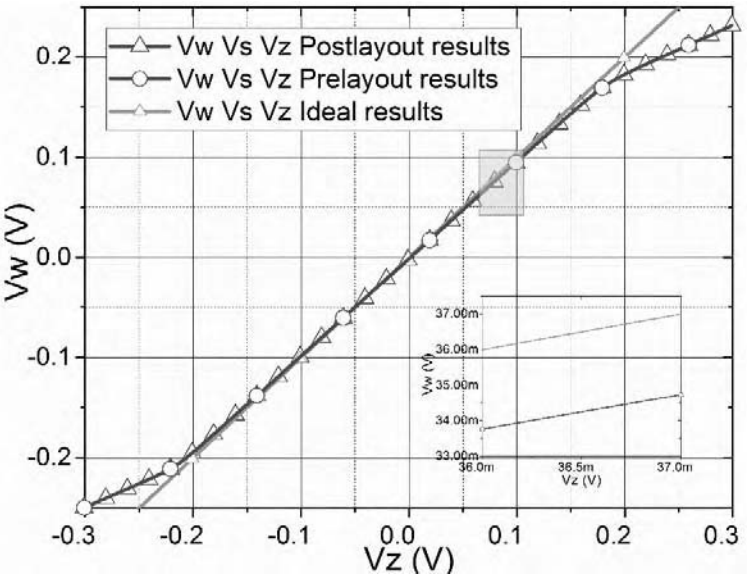
Figure 3.5 The layout of the proposed VDBA

The DC characteristics of the proposed VDBA for ideal, schematic and post layout driven simulations are shown in Figure 3.6. Figure 3.6 (a) shows the variation in I_z with respect to the applied input voltage (V_p, V_n) and the plot of V_w with respect to change in V_z is depicted in Figure 3.6 (b). An enlarged section of each characteristic is also shown in the inset in respective figures to highlight the difference between pre and post

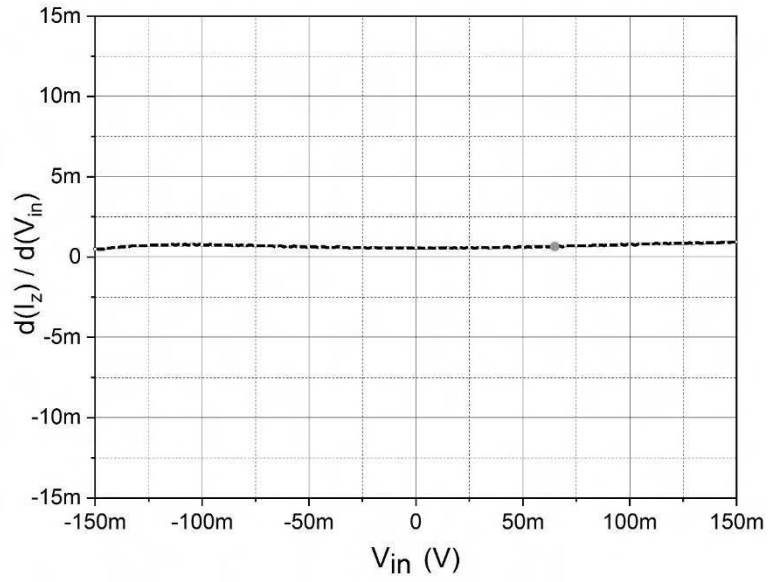
layout simulations. It is observed that post layout driven simulations closely follow the schematic driven simulations. Further, it is observed that the linear input range for the TA is observed to be ±150 mV whereas that for the buffer is ±200 mV. The plot of ICMR of TA obtained from Figure 3.6 (a) is depicted in Figure 3.6 (c). The variation of g_m with respect to I_B is depicted in Figure 3.6 (d). It may be observed that the g_m varies from 411.8 µS to 1.374 mS for the corresponding bias current range of 10 µA to 75 µA.



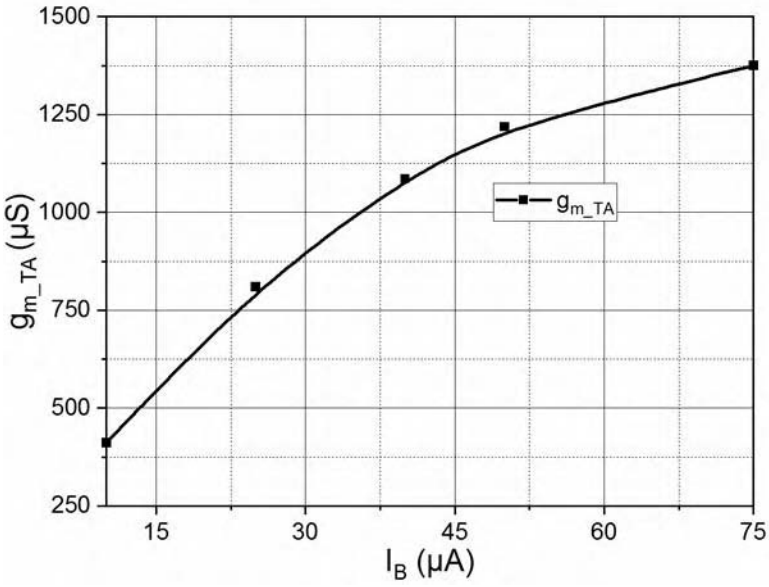
(a)



(b)



(c)

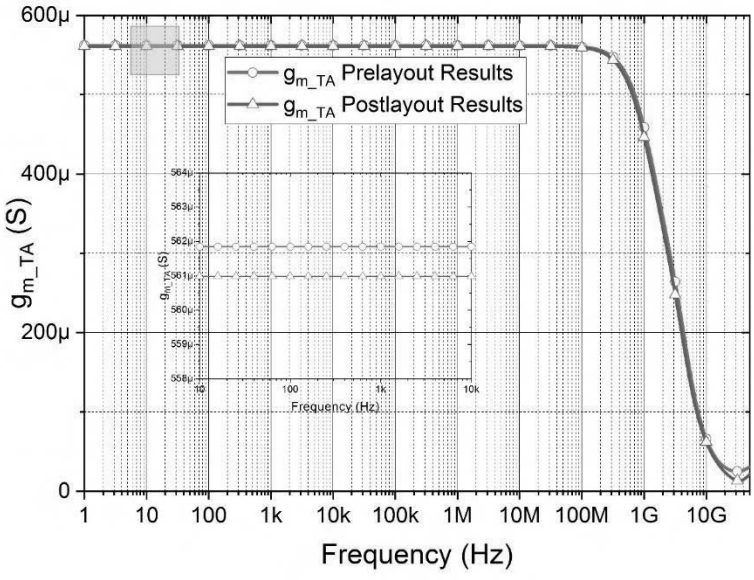


(d)

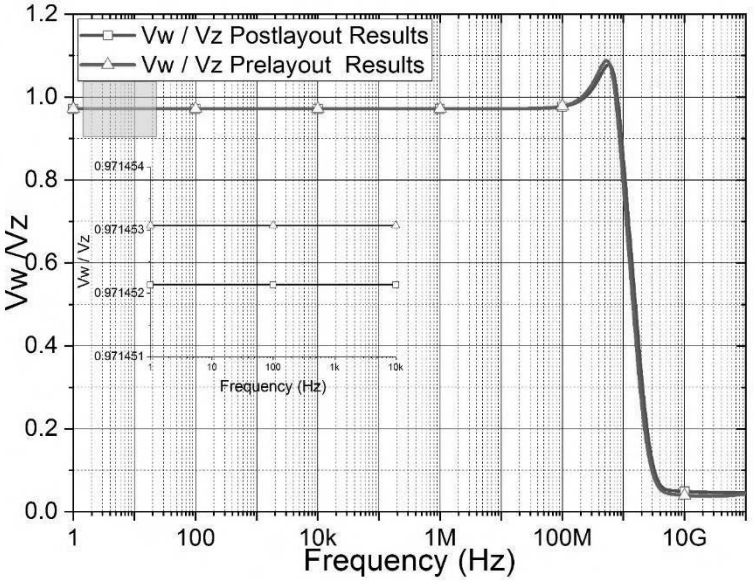
Figure 3.6 The DC characteristics (a) I_z variation w.r.t V_p and V_n, (b) V_w variation w.r.t V_z, (c) the ICMR plot and (d) the g_m variation w.r.t I_B

Both pre and post layout AC responses of the proposed VDBA are depicted in Figure 3.7. The AC responses for TA are shown in Figure 3.7 (a). The g_m values for schematic and post layout driven simulations are observed to be 561.8 µS and 561 µS

respectively and corresponding 3 dB frequencies are recorded to be 1.48 GHz and 1.36 GHz.



(a)



(b)

Figure 3.7 The frequency response of the (a) TA and (b) buffer

The buffer AC responses for pre and post layout simulations are shown in Figure 3.7 (b) and their respective transfer ratios are found to be 0.9714 and 0.9710 with BW as 1.23 GHz and 1.13 GHz respectively. The inset in each figure shows an

enlarged section of the characteristic. The slight difference in pre and post layout simulated VDBA parameters may be attributed to the circuit parasitic.

It may be observed from Figure 3.7 (b) that a peak appears in the AC characteristic of the buffer which may lead to ringing and needs to be compensated. The analysis presented below suggests that the presence of complex pole results in peaking and the same may be compensated by connecting a compensating resistance R_X across gate and source of M_9 and similarly across M_{10}. High frequency small signal equivalent of the uncompensated/ compensated buffer considering device capacitances is drawn in Figure 3.8 which is used to find the voltage transfer ratio. It may be noted that R_X connected through dotted lines are to be included in small signal equivalent of the compensated structure only.

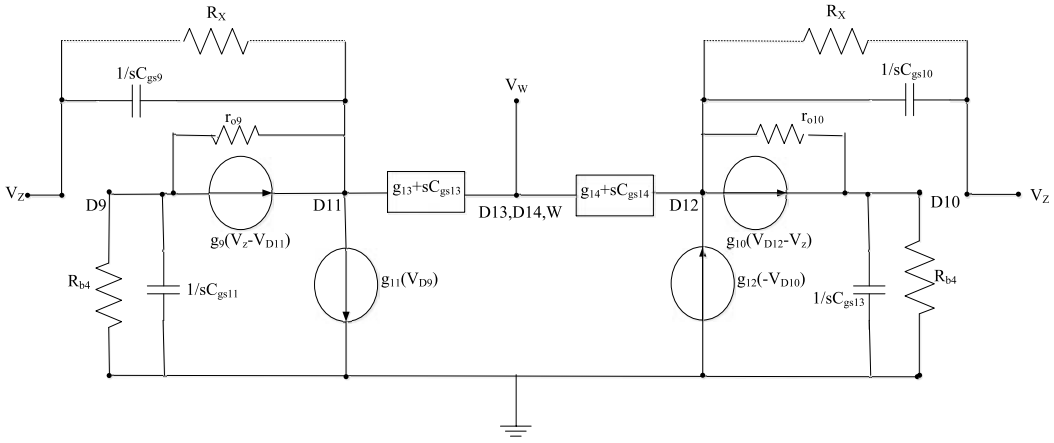


Figure 3.8 High frequency small signal model of uncompensated/compensated buffer

Applying KCL at node D9 and D11 of small signal equivalent of uncompensated buffer, we get

$$V_{D9}\left(\frac{1}{R_b}+\frac{1}{r_{09}}+sC_{gs11}\right)=V_{D11}\left(\frac{1}{r_{09}}+g_9\right)-g_9V_Z \tag{3.22}$$

$$V_{D9}(\frac{1}{r_{09}}-g_9)=V_{D11}(\frac{1}{r_{09}}+g_9+sC_{gs9}+\frac{1}{r_{011}}+g_{13}+sC_{gs13})-(g_9+sC_{gs9})V_Z-V_W(g_{13}+sC_{gs13})$$

(3.23)

Assuming $r_{o9} = r_{o11} = r_o$, $C_{gs9} = C_{gs11} = C_{gs13} = C_{gs}$,, $g_9 = g_{11} = g_{13} = g_m$ the (3.22) and (3.23) are respectively approximated as

$$V_{D9}(\frac{1}{R_b}+\frac{1}{r_o}+sC_{gs})=V_{D11}(\frac{1}{r_o}+g_m)-g_mV_Z$$

(3.24)

$$V_{D9}(\frac{1}{r_o}-g_m)=V_{D11}(\frac{1}{r_o}+g_m+sC_{gs}+\frac{1}{r_o}+g_m+sC_{gs})-(g_m+sC_{gs})V_Z-V_W(g_m+sC_{gs})$$

(3.25)

Eliminating V_{D9} from (3.24) and (3.25),

$$V_Z(s^2C_{gs}^2+sC_{gs}(\frac{1}{R_b}+\frac{1}{r_o}+g_m)+g_m{}^2+\frac{g_m}{R_b})=$$
$$V_{D11}\{s^2C_{gs}^2+2sC_{gs}(\frac{1}{R_b}+\frac{1}{r_o}+g_m)+2(\frac{g_m}{R_b}+\frac{1}{R_br_o}+\frac{g_m}{r_o}+\frac{1}{r_o^2})\}-V_W(g_m+sC_{gs})(sC_{gs}+\frac{1}{R_b}+\frac{1}{r_o})$$

(3.26)

A similar expression may be derived for M_{10}, M_{12} and M_{14}, considering $r_{o10} = r_{o12} = r_o$, $C_{gs12} = C_{gs10} = C_{gs14} = C_{gs}$ and $g_{10} = g_{12} = g_{14} = g_m$ and will result in the following equation

$$V_Z\{s^2C_{gs}^2+sC_{gs}(\frac{1}{R_b}+\frac{1}{r_o}+g_m)+g_m{}^2+\frac{g_m}{R_b}\}=$$
$$V_{D12}\{2s^2C_{gs}^2+2sC_{gs}(\frac{1}{R_b}+\frac{2}{r_o}+g_m)+2(\frac{g_m}{R_b}+\frac{1}{R_br_o}+\frac{g_m}{r_o}+\frac{1}{r_o^2})\}-V_W(g_m+sC_{gs})(sC_{gs}+\frac{1}{R_b}+\frac{1}{r_o})$$

(3.27)

The KCL at node W gives

$$V_W=\frac{V_{D11}+V_{D12}}{2}$$

(3.28)

Using (3.26), (3.27) and (3.28) the voltage transfer ratio can be written as

$$\frac{V_W}{V_Z}=\frac{s^2+s(\frac{1}{C_{gs}R_b}+\frac{1}{C_{gs}r_o}+\frac{g_m}{C_{gs}})+\frac{{g_m}^2}{C_{gs}^2}+\frac{g_m}{C_{gs}^2R_b}}{s^2+s((\frac{1}{C_{gs}R_b}+\frac{3}{C_{gs}r_o}+\frac{g_m}{C_{gs}})+\frac{{g_m}^2}{C_{gs}^2}+\frac{g_m}{C_{gs}^2R_b}+\frac{g_m}{C_{gs}^2r_o}+\frac{2r_o+R_b}{C_{gs}^2R_b{r_o}^2}}$$

(3.29)

Now the zeros and poles of the transfer function can be found as

$$z_{1,2}=\frac{-(\frac{1}{R_b}+\frac{1}{r_o}+g_m)\pm\sqrt{-3{g_m}^2-\frac{2g_m}{R_b}+\frac{2}{R_br_o}+\frac{2g_m}{r_o}+\frac{1}{{r_o}^2}+\frac{1}{{R_b}^2}}}{2C_{gs}}$$

(3.30)

$$p_{1,2}=\frac{-(\frac{1}{R_b}+\frac{3}{r_o}+g_m)\pm\sqrt{-3{g_m}^2-\frac{2g_m}{R_b}-\frac{2}{R_br_o}+\frac{2g_m}{r_o}+\frac{5}{{r_o}^2}+\frac{1}{{R_b}^2}}}{2C_{gs}}$$

(3.31)

Considering $1/R_b$ *and* $1/r_o$ to be small values, the poles can be approximated as

$$z_{1,2}=\frac{(g_m)(-1\pm\sqrt{-3})}{2C_{gs}}=\frac{-1\pm1.732i}{2}\frac{g_m}{C_{gs}}\ ,\quad |z_{1,2}|=\frac{g_m}{C_{gs}}$$

(3.32)

$$p_{1,2}=\frac{(g_m)(-1\pm\sqrt{-3})}{2C_{gs}}=\frac{-1\pm1.732i}{2}\frac{g_m}{C_{gs}}\ ,\quad |p_{1,2}|=\frac{g_m}{C_{gs}}$$

(3.33)

Equation (3.33) clearly shows the existence of a complex pole in buffer voltage transfer ratio due to which peaking is observed in buffer response. This peaking can be eliminated using resistive compensation by placing a resistance R_X across the gate and source of M_9 and M_{10} transistor each as shown in Figure 3.8 with dotted lines. Using the small signal equivalent of compensated buffer and applying KCL at node D9 and D11 we get

$$V_{D9}(\frac{1}{R_b}+\frac{1}{r_{09}}+sC_{gs11})=V_{D11}(\frac{1}{r_{09}}+g_9)-g_9V_Z$$

(3.34)

$$V_{D9}(\frac{1}{r_{09}}-g_9)=V_{D11}(\frac{1}{r_{09}}+g_9+sC_{gs9}+\frac{1}{r_{011}}+g_{13}+sC_{gs13}+\frac{1}{R_X})-$$
$$(g_9+sC_{gs9}+\frac{1}{R_X})V_Z-V_W(g_{13}+sC_{gs13})$$

(3.35)

Assuming $r_{o9} = r_{o11} = r_o$, $C_{gs9} = C_{gs11} = C_{gs13} = C_{gs}$,, $g_9 = g_{11} = g_{13} = g_m$ the (3.34) and (3.35) are approximated as (3.36) and (3.37) respectively.

$$V_{D9}(\frac{1}{R_b}+\frac{1}{r_o}+sC_{gs})=V_{D11}(\frac{1}{r_o}+g_m)-g_mV_Z$$

(3.36)

$$V_{D9}(\frac{1}{r_o}-g_m)=V_{D11}(\frac{1}{r_o}+g_m+sC_{gs}+\frac{1}{r_o}+g_m+sC_{gs}+\frac{1}{R_X})-$$
$$(g_m+sC_{gs}+\frac{1}{R_X})V_Z-V_W(g_m+sC_{gs})$$

(3.37)

Eliminating V_{D9} from (3.36) and (3.37) results in

$$V_Z(s^2C_{gs}^2+sC_{gs}(\frac{1}{R_b}+\frac{1}{r_o}+g_m+\frac{1}{R_X})+g_m{}^2+\frac{g_m}{R_b}+\frac{1}{R_X}(\frac{1}{R_b}+\frac{1}{r_o})=$$
$$V_{D11}\{2s^2C_{gs}^2+2sC_{gs}(\frac{1}{R_b}+\frac{2}{r_o}+g_m+\frac{1}{R_X})+2(\frac{g_m}{R_b}+\frac{1}{R_br_o}+\frac{g_m}{r_o}+\frac{1}{r_o{}^2})\}-V_W(g_m+sC_{gs})(sC_{gs}+\frac{1}{R_b}+\frac{1}{r_o})$$

(3.38)

A similar expression may be derived for M_{10}, M_{12} and M_{14} and is given as

$$V_Z(s^2C_{gs}^2+sC_{gs}(\frac{1}{R_b}+\frac{1}{r_o}+g_m+\frac{1}{R_X})+g_m{}^2+\frac{g_m}{R_b}+\frac{1}{R_X}(\frac{1}{R_b}+\frac{1}{r_o})=$$
$$V_{D12}\{2s^2C_{gs}^2+2sC_{gs}(\frac{1}{R_b}+\frac{2}{r_o}+g_m+\frac{1}{2R_X})+(\frac{2g_m}{R_b}+\frac{2}{R_br_o}+\frac{2g_m}{r_o}+\frac{1}{r_o{}^2}+\frac{1}{R_X}(\frac{1}{R_b}+\frac{1}{r_o}+g_m{}^2)\}-$$
$$V_W(s^2C_{gs}^2+sC_{gs}(\frac{1}{R_b}+\frac{1}{r_o}+g_m)+\frac{g_m}{R_b}+\frac{g_m}{r_o})$$

(3.39)

Now applying KCL at node W gives

$$V_W = \frac{V_{D11} + V_{D12}}{2} \tag{3.40}$$

Using (3.38), (3.39) and (3.40), the transfer function of compensated buffer can be written as

$$\frac{V_W}{V_Z} = \frac{s^2 + s\left(\frac{1}{C_{gs}r_o} + \frac{1}{C_{gs}R_B} + \frac{g_m}{C_{gs}} + \frac{1}{R_X}\right) + \frac{g_m^2}{C_{gs}^2} + \frac{g_m}{C_{gs}^2 R_b} + \frac{1}{R_X C_{gs}^2}\left(\frac{1}{R_B} + \frac{1}{r_o}\right)}{s^2 + s\left(\left(\frac{1}{C_{gs}R_b} + \frac{3}{C_{gs}r_o} + \frac{g_m}{C_{gs}} + \frac{1}{C_{gs}R_X}\right) + \frac{g_m^2}{C_{gs}^2} + \frac{g_m}{C_{gs}^2 R_B} + \frac{g_m}{C_{gs}^2 r_o} + \frac{2r_o + R_B}{C_{gs}^2 R_B r_o^2} + \frac{1}{R_X C_{gs}^2}\left(\frac{1}{R_b} + \frac{1}{r_o}\right)\right.} \tag{3.41}$$

The zeros and poles of (3.21) can be computed as

$$z_{1,2} = \frac{-\left(\frac{1}{R_b} + \frac{1}{r_o} + g_m + \frac{1}{R_X}\right) \pm \sqrt{-3g_m^2 - \frac{2g_m}{R_b} + \frac{2}{R_b r_o} - \frac{2}{R_X r_o} + \frac{2g_m}{r_o} + \frac{1}{r_o^2} + \frac{1}{R_b^2} + \frac{2g_m}{R_X} + \frac{1}{R_X^2} - \frac{2}{R_b R_X}}}{2C_{gs}} \tag{3.42}$$

$$p_{1,2} = \frac{-\left(\frac{1}{R_b} + \frac{3}{r_o} + g_m + \frac{1}{R_X}\right) \pm \sqrt{-3g_m^2 - \frac{2g_m}{R_b} - \frac{2}{R_b r_o} - \frac{2}{R_X r_o} + \frac{2g_m}{r_o} + \frac{5}{r_o^2} + \frac{1}{R_b^2} + \frac{2g_m}{R_X} + + \frac{1}{R_X^2} + \frac{2}{R_b R_X}}}{2C_{gs}} \tag{3.43}$$

considering $g_m r_o >> 1$ and $g_m R_b >> 1$, the poles can be written as

$$z_{1,2} \approx \frac{-\left(g_m + \frac{1}{R_X}\right) \pm \sqrt{-3g_m^2 + \frac{2g_m}{R_X} + \frac{1}{R_X^2}}}{2C_{gs}} \tag{3.44}$$

$$p_{1,2} = \frac{-\left(g_m + \frac{1}{R_X}\right) \pm \sqrt{-3g_m^2 + \frac{1}{R_X^2} + \frac{2g_m}{R_X}}}{2C_{gs}} \tag{3.45}$$

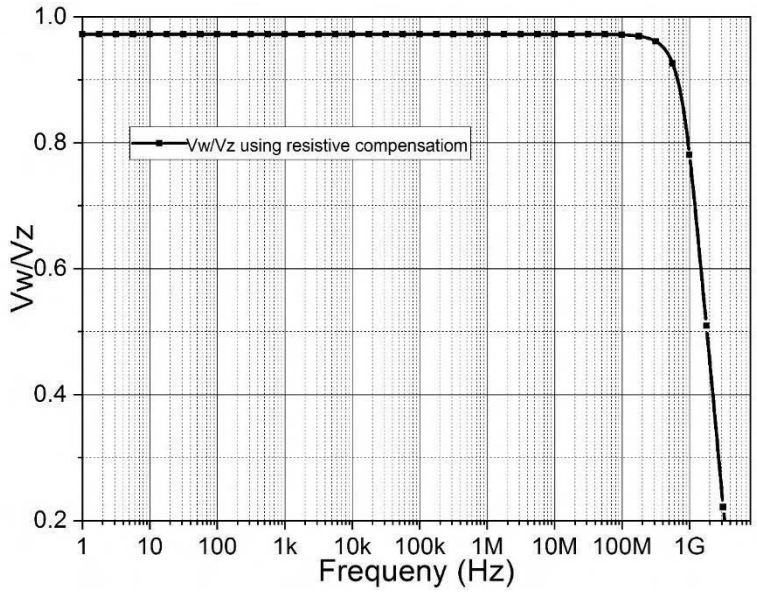
It may be noted that the magnitude of the imaginary part is reduced and so the peaking can be reduced [22] and if R_X is so chosen that $g_m \approx 1/R_X$, then imaginary part can be set to zero.

$$z_{1,2} \approx \frac{-(g_m + \frac{1}{R_X}) \pm \sqrt{-3g_m{}^2 + \frac{2g_m}{R_X} + \frac{1}{R_X{}^2}}}{2C_{gs}} = \frac{-g_m}{C_{gs}},\ |z_{1,2}| = \frac{g_m}{C_{gs}} \tag{3.46}$$

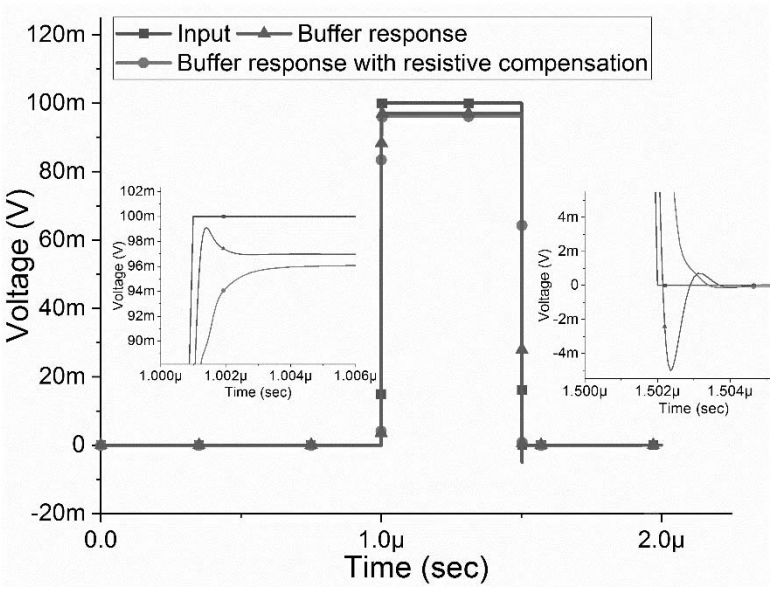
$$p_{1,2} = \frac{-(g_m + \frac{1}{R_X}) \pm \sqrt{-3g_m{}^2 + \frac{1}{R_X{}^2} + \frac{2g_m}{R_X}}}{2C_{gs}} = \frac{-g_m}{C_{gs}},\ |p_{1,2}| = \frac{g_m}{C_{gs}} \tag{3.47}$$

It may be deduced from (3.47) that by using resistive compensation the imaginary part of pole frequency in (3.33) gets nullified. So the proposed compensated buffer is simulated by taking R_X = 15 kΩ and the obtained frequency response is shown in Figure 3.9. It clearly depicts the effectiveness of peak compensation method. The BW of compensated buffer is observed to be 1.22 GHz.

The transient behavior of uncompensated and compensated structures is also examined by plotting step responses as shown in Figure 3.9 (b). It may be noted from the step response of uncompensated buffer that the peak present in frequency domain manifests in overshoot both in high to low and low to high transitions of input pulse as shown in zoomed in sections in insets. With compensation in place, the overshoots for both the transitions are visibly eliminated.



(a)

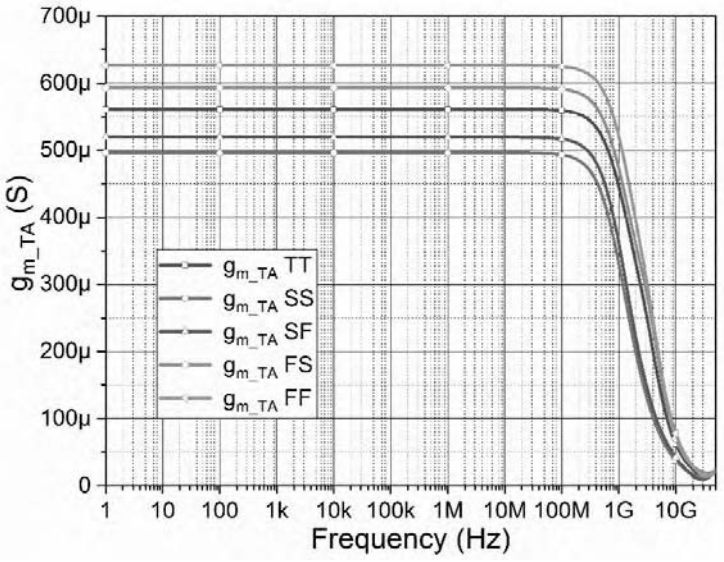


(b)

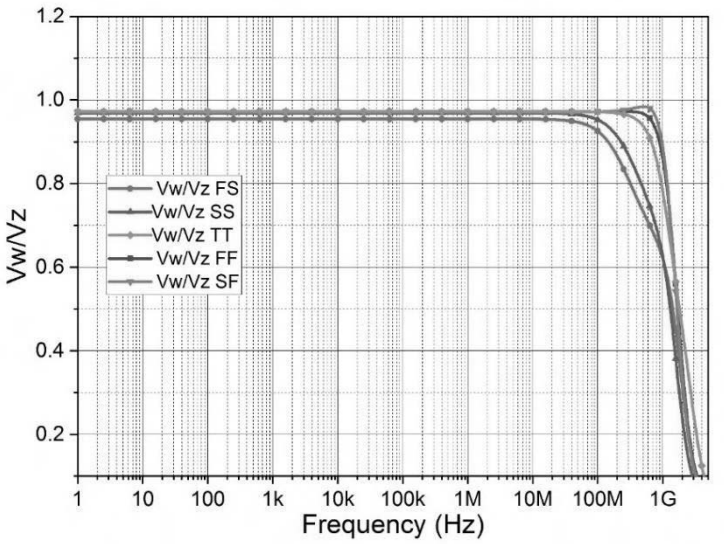
Figure 3.9 (a) Frequency response and (b) Step response of the compensated buffer

The process variables may fluctuate randomly around their ideal values in fabrication. These random variations result in an uncertain behavior of the circuit. Further, it is expected that the circuit parameters should exhibit little dependence on temperature (T) and their variation with supply voltage (V) should be well known. Therefore, the

proposed structure is simulated at different corners and corresponding frequency responses for the TA and buffer are shown in Figure 3.10 (a) and 3.10 (b) respectively. The performance of the proposed structure at different supply voltages is shown in Figure 3.11 (a) and Figure 3.11 (b). Further, the circuit performance in the temperature range −25 °C to 50 °C is depicted in Figure 3.12 (a) and 3.12 (b) while supply voltages are fixed at ± 0.7 V.

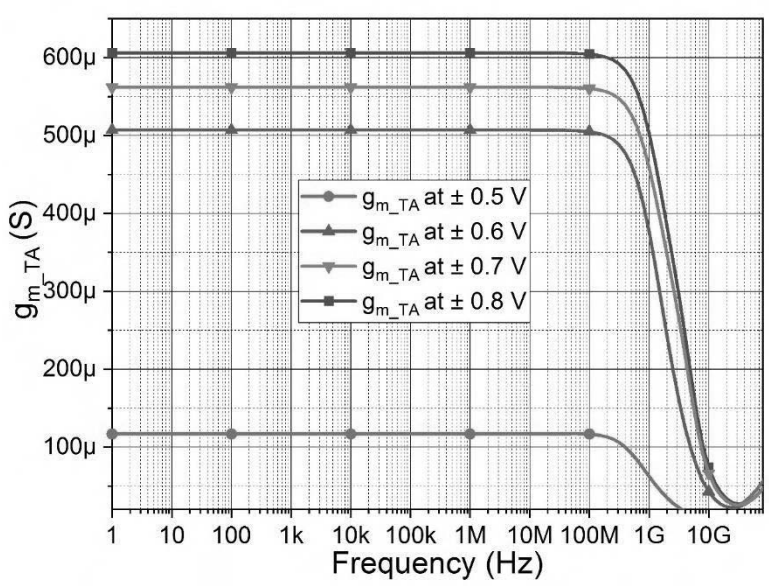


(a)

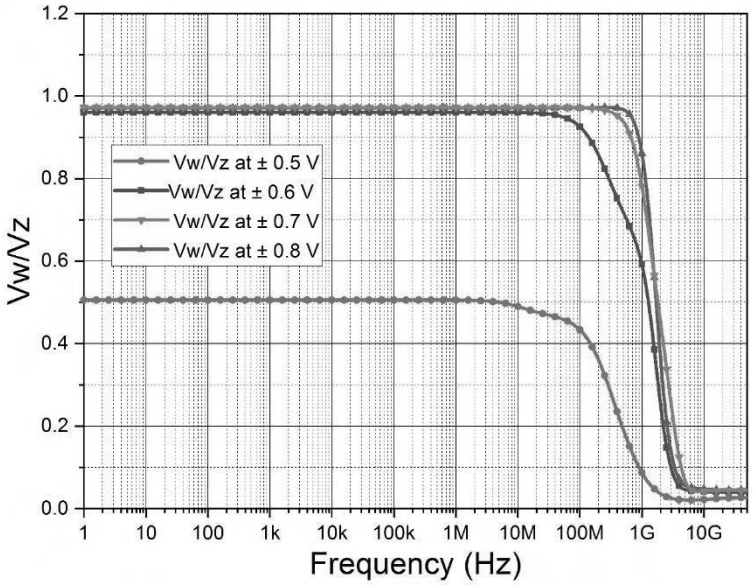


(b)

Figure 3.10 Post layout frequency responses of (a) TA and (b) buffer, at different corners

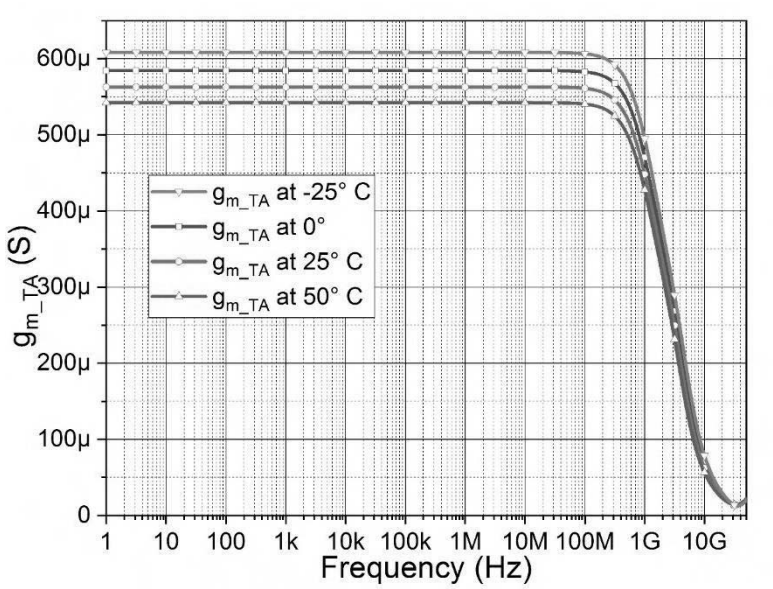


(a)

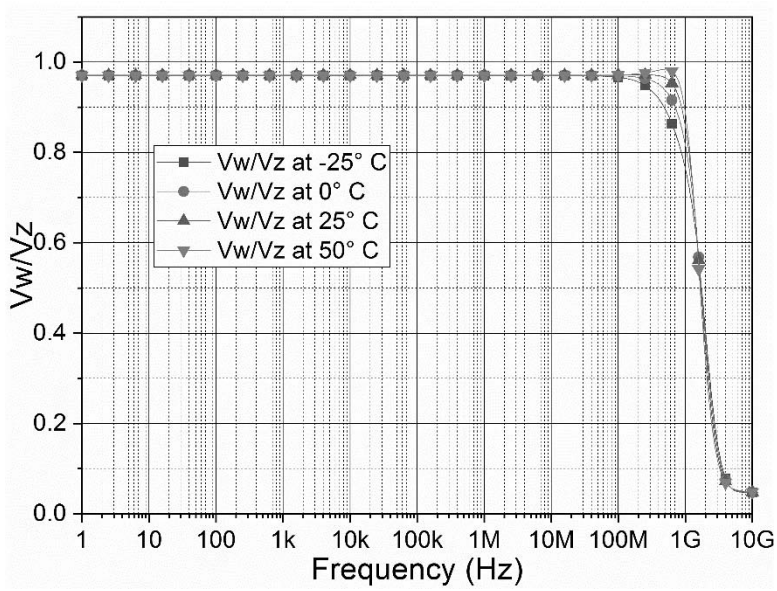


(b)

Figure 3.11 Post layout simulation of (a) TA and (b) buffer at different supply voltages



(a)

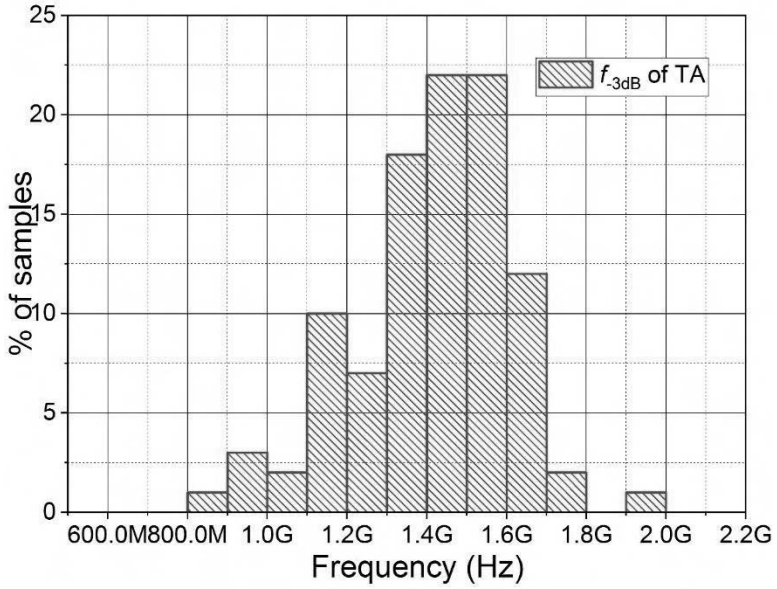


(b)

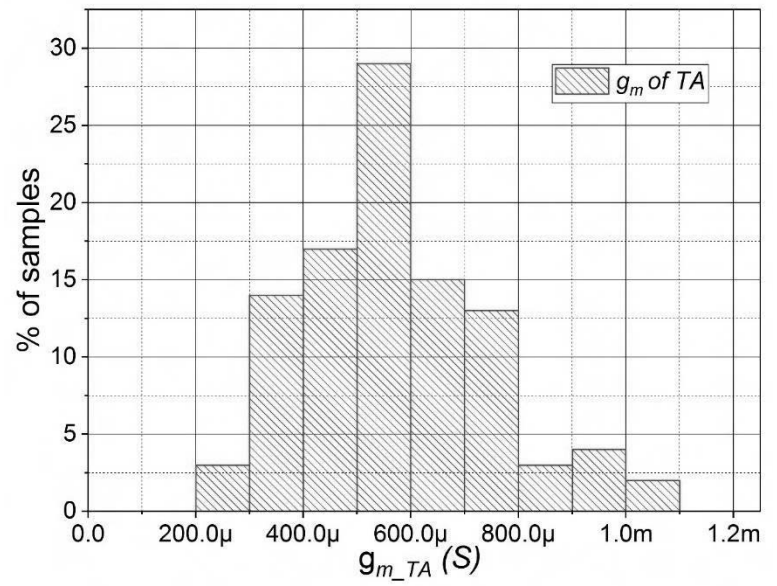
Figure 3.12 Post layout simulation of (a) TA and (b) buffer at different temperatures

To check the robustness of the proposed VDBA, Monte Carlo statistical analysis has been carried out for a 5 % deviation in the aspect ratio of all the transistors. The derived histograms after 100 simulations run for the proposed topology are shown in

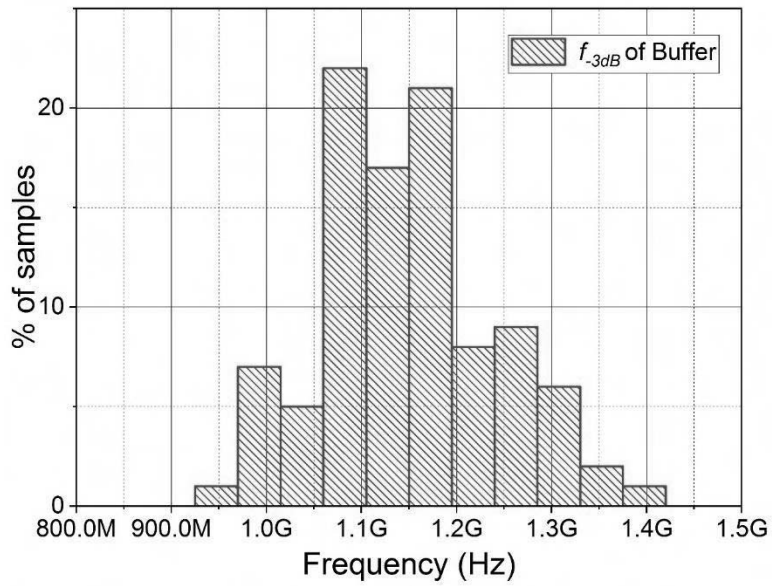
Figure 3.13. The simulated average values of BW for TA and buffer are 1.41 GHz and 1.15 GHz respectively with corresponding standard deviation of 0.19 GHz and 0.1 GHz as shown in Figures 3.13 (a) and (c). Also, the average values of g_m and voltage transfer ratio are observed to be 570 µS and 0.978 respectively and shown in Figures 3.13 (b) and (d). The results obtained from the Monte Carlo histograms confirm that the proposed VDBA has low sensitivity.



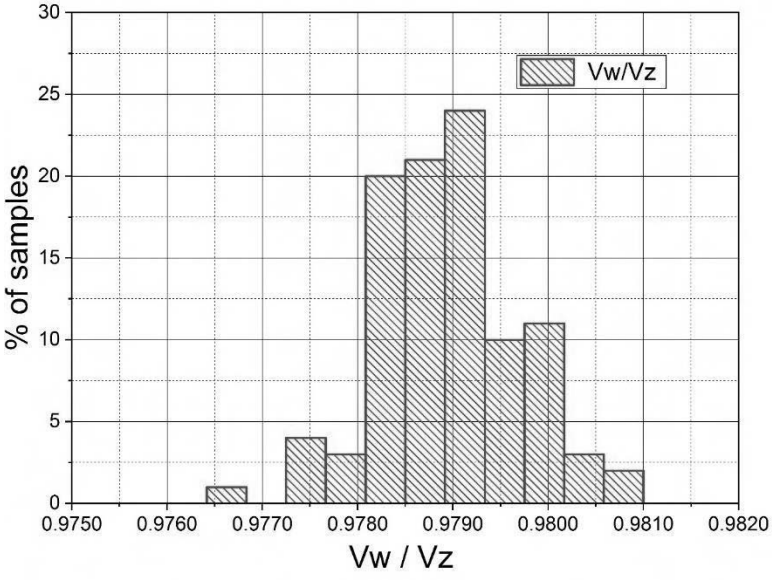
(a)



(b)



(c)



(d)

Figure 3.13 Histograms of proposed VDBA (a) 3dB frequency of TA, (b) Transconductance of TA (g_m), (c) 3dB frequency of buffer and (d) Voltage transfer ratio (V_w/V_z)

3.4 Conclusion

A low voltage, low power high performance VDBA designed using DFVF cell is presented. Low frequency small signal analysis is presented for mathematical

formulation of transconductance and buffer transfer ratio. The proposed VDBA is characterized through pre and post layout simulations using Cadence Virtuoso at GPDK 0.18 μm CMOS technology with supply voltages of ±0.7 V. A wide range of transconductance variation is obtained by varying bias current. A resistive compensation technique is used to compensate the peak in frequency response of the buffer and detailed mathematical formulation of the same is also presented. To show the effect of parameter variations and transistor aspect ratio variation PVT and Monte Carlo analyses have been presented.

CHAPTER 4

4.1 Introduction

Having described and characterized an existing VDBA [33] in chapter 2 and presented a new VDBA circuit in chapter 3 we now present the applications of VDBA. The VDBA can be used as a basic building block to design linear and non-linear analog circuit applications. This chapter presents VDBA based linear applications. A high common mode rejection ratio (CMRR) instrumentation amplifier (IA) using single VDBA is presented first which is followed by filter applications. Three filter applications are developed out of which the first order APF and second order SISO multifunction filter are designed employing single ABB whereas the MISO universal filter is designed using two VDBAs.

4.2 Instrumentation Amplifier

In consumer and industrial applications variety of physical quantities such as temperature, light sensitivity, humidity etc. are required to be measured using transducers. The low level differential output of the transducer is to be amplified faithfully, eliminating the common mode noise for further processing. This is accomplished by using instrumentation amplifiers at the input stage as IAs are always designed for high differential gain along with high CMRR. CMRR is defined as the ratio of the differential gain to the common mode gain. Thus high gain and CMRR are important features of an IA.

An extensive review suggests that no VDBA based IA is available in the open literature, though a variety of IAs designed using different ABBs exist. The available literature on IAs [96]–[125] can be classified according to input signal sensed from the transducer and the output signal provided by the IA for further processing. Thus the IAs sensing

voltage (current) and producing voltage (current) are termed as VMIA (CMIA). Similarly, the IAs with current (voltage) sensing and voltage (current) producing capabilities are classified as transadmittance mode IA (TAMIA) / transimpedance IA (TIMIA). All existing IAs are summarized in Table 4.1with their salient features.

Table 4.1 Comparison of the proposed work with the previously reported work

Reference No.	No. of ABB	Passive Component (R+C)	Input Impedance	Output impedance	Mode	Power Supply (V)	Differential gain	3 dB of A_d	CMRR	3 dB of CMRR
[103]	4 Op Amp	6	High	Low	VM	--	1	--	>70 dBs at 100 KHz	--
[104]	3 Op Amp	7	High	Low	VM	3.3 (single)	2	--	62	65 KHz
[105]	5 Op Amp	5	High	Low	VM	--	Unity	--	> 60 dBs	Upto 200 KHz
[107]	2 CCII+	3	High Low	High High	VM TIM	--	40dB-10dB	1.5-2.3 MHz	100 dB	3 KHz
[108]	3 CCII+	2	High	High	VM	--	100, 17.8, 1.92	1.44 MHz	95 dB	65 KHz
[109]	2 CCII+	2	High	High	VM	--	10, 20, 30, 40(dB)	--	>70 dB at 100 KHz	--
[110]	2 CCII+	2	High	High	VM	--	29, 24, 19(dB)	591.6 KHz	95	2 KHz
[112]	3 CCCII	--	High	High	VM TAM	±2.5	14, 19.6, 25	10 MHz	147	35 KHz
[113]	2 CCCII	1 Active Resistor	High	High	VM	±3.3	16.7 , 21, 25.4 , 28.7	70.1 MHz	142	--
[114]	3 OTRA	5	Low	Low	TIM	±1.5	48, 42, 26	--	64.5	10KHz
[115]	2 OFCC	4	High	High	VM	--	40, 20, 4, 2	1.2 MHz	76	185 KHz

[117]	MOS	--	Low	High	CM	±0.8	19.5 , 33.2	>10.18 MHz	91	--
[118]	1 Op Amp + 1 CC	6	High	High	VM	-	34, 26, 20	>1 MHz	120	--
[119]	1 CFOA	4	High	Low	CM	±1	40, 33.97, 20	--	48	--
[120]	6 CCII+ & 1 Op Amp	3	High	Low	VM	±1.5	116	--	145	--
[121]	6 CCII+ & 1 Op Amp	3	High	Low	VM	±1.5	120	--	149	--
[122]	2 CCII+ & 1 Op Amp	3	High	Low	VM	--	--	--	50	--
[123]	2 CC & 2 Op Amp	2	High	High	VM	--	40, 20, 0	1.5 – 2.97 MHz	55	10 KHz
[124]	2 DVCC	2	High	High	VM	±1.8	12.1 dB	--	102	6.13MHz
[125]	1 DVCC	2	High	High	VM	±1.5	0-12 (dB)	8 MHz	--	--
Proposed	1 VDBA	1	High	Low	VM	±0.9	0,6,10 (dB)	38 MHz	198 dB	2.81 MHz

From Table 4.1 it is observed that [103]–[105], [109], [112], [114], [120]–[123] are using multiple ABBs which leads to large power consumption. In numerous VMIA topologies [107]–[113], [115], [117], [118], [123]–[125] the output is available at high impedance node which hampers the circuit cascadability. A large number of passive components are used in [103]–[107], [114]–[119], [125]. The CMRR for the structures of [104], [105], [119], [122], [123], [125] is found to be low. The CMRR is found to be sensitive to resistor mismatching and the gain is limited by constant gain bandwidth product in [107], [112], [113], [118]. Except [124], all the configurations are limited to

low bandwidth.

Thus in this chapter, a high CMRR VMIA employing single VDBA and a resistor is proposed which works on much lower power supply as compared to the existing designs.

4.2.1 Proposed IA

The proposed IA is shown in Figure 4.1 and using terminal equations of VDBA its differential gain (A_d) can be expressed as

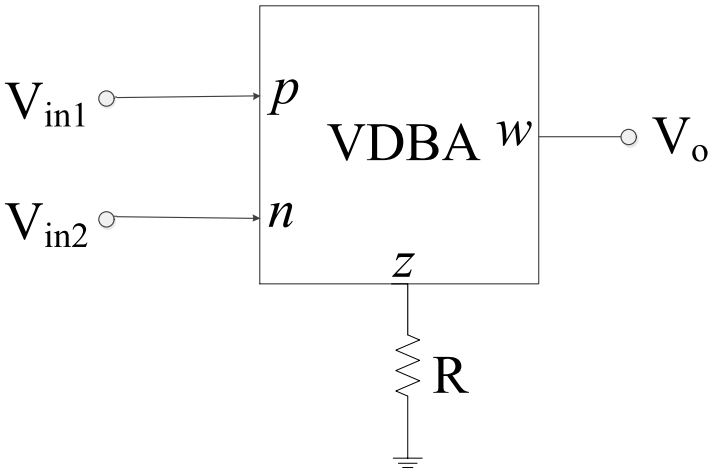


Figure 4.1 The proposed IA

$$A_d = \frac{V_o}{(V_{in1} - V_{in2})} \tag{4.1}$$

4.2.1.1 Non-Ideal Analysis

This section is devoted to analyzing the behavior of proposed IA in presence of non-idealities of VDBA. Figure 4.2 shows the non-ideal model of proposed IA.

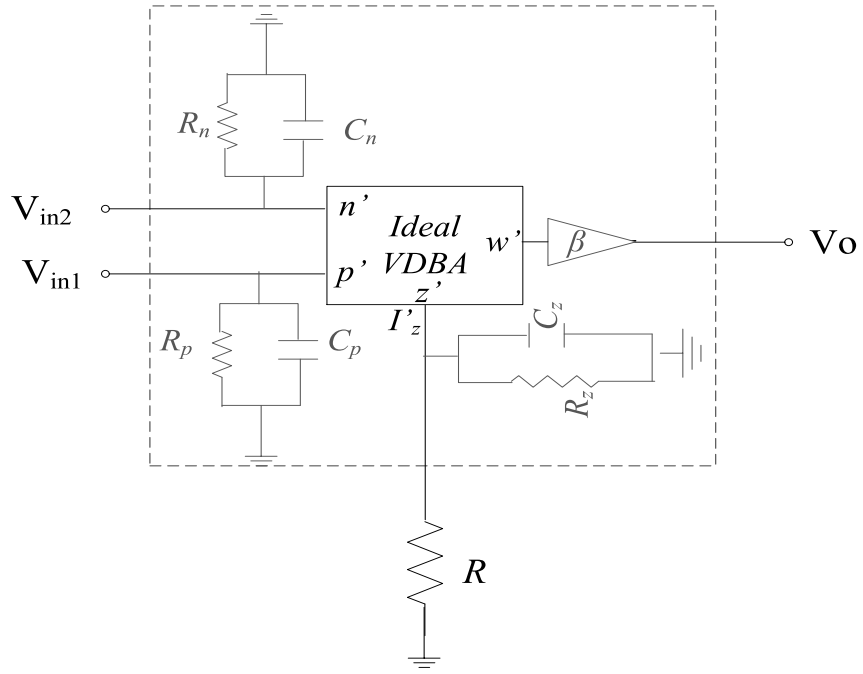


Figure 4.2 Non-ideal IA

Under non-ideal conditions, the output voltage is given by

$$V_o = \beta R_{eq} g_{mo} \left(\frac{V_p}{1 + s/\omega_{gm1}} - \frac{V_n}{1 + s/\omega_{gm2}} \right) \tag{4.2}$$

where

$$R_{eq} = R // R_z // 1/sC_z = \frac{1}{sC_z + \left(\frac{R + R_z}{RR_z} \right)} \tag{4.3}$$

Considering $\omega_{gm1} = \omega_{gm2} = \omega_{gm}$, the A_d can be expressed as

$$A_d = \frac{V_o}{V_p - V_n} = R_{eq} g_{mo} \varepsilon_{uc} \tag{4.4}$$

where ε_{uc} is uncompensated error and is given by

$$\varepsilon_{uc} = \frac{\beta}{\left(1 + s/\omega_{gm1}\right)} \tag{4.5}$$

By using $V_p = V_n = V_c$, the common mode gain (A_c) can be written as

$$A_c = \frac{V_o}{V_c} = \beta R_{eq} g_{mo} \left(\frac{1}{1 + s/\omega_{gm1}} - \frac{1}{1 + s/\omega_{gm2}} \right) \tag{4.6}$$

The CMRR can be computed as

$$CMRR = \frac{A_d}{A_c} = \frac{2 + s\left(\frac{1}{\omega_{gm1}} + \frac{1}{\omega_{gm2}}\right)}{s\left(\frac{1}{\omega_{gm2}} - \frac{1}{\omega_{gm1}}\right)} \tag{4.7}$$

Equation (4.7) would result in high CMRR as the values of ω_{gm1} and ω_{gm2} remain close to each other.

4.2.1.2 Noise Analysis

The noise limits the minimum signal level that a circuit can process with acceptable quality. Therefore the effect of noise on the proposed circuit needs to be analyzed. Output and input noise spectral densities for the proposed IA are formulated using VDBA of Figure 2.4 and representing the transconductance of i^{th} transistor as g_{mi}.

The input noise of M_3 and M_1 can be written as

$$\overline{V_{n,in}^2}\Big|_{M3,1} = \frac{2}{3}\times 4KT\left[\left(\frac{g_{m3}+g_{m1}}{g_{m3}^{\ 2}}\right)\right] \tag{4.8}$$

Where K represents the Boltzman's constant and T denotes the temperature.

The noise of M_6 and M_8 when referred to gate of M_6 can be expressed as

$$\overline{V_{n}^2}\Big|_{M6,8} = \frac{2}{3}\times 4KT\left[\left(\frac{g_{m6}+g_{m8}}{g_{m6}^{\ 2}}\right)\right] \tag{4.9}$$

With reference to the V_{in} it should be divided by A_{v1}^2, where A_{v1} represents the voltage gain of M_3. So input noise of M_6 and M_8 is expressed as

$$\overline{V_{n,in}^2}\Big|_{M6,8} = \frac{1}{A_{v1}^2}\times\frac{2}{3}\times 4KT\left[\left(\frac{g_{m6}+g_{m8}}{g_{m6}^{\ 2}}\right)\right] \text{ where } A_{v1}= g_{m3}/g_{m1}. \tag{4.10}$$

Total input noise of TA stage ($V_{n,in}|_{M1\text{-}M9}$) is expressed as

$$\overline{V_{n,in}^2}\Big|_{M1-M9} = 2\times\left(\frac{2}{3}\times 4KT\left[\left(\frac{g_{m3}+g_{m1}}{g_{m3}^{\ 2}}\right)\right] + \frac{1}{A_{v1}^2}\times\frac{2}{3}\times 4KT\left[\left(\frac{g_{m6}+g_{m8}}{g_{m6}^{\ 2}}\right)\right]\right) \tag{4.11}$$

Similarly the input noise for M_{10}-M_{13} and M_{15}-M_{16} can be expressed as (4.12) and (4.13) respectively, where A_{v2} is g_{m12}/g_{m10}

$$\overline{V_{n,in}^2}\Big|_{M10-13} = 2\times\frac{2}{3}\times 4KT\left[\left(\frac{g_{m10}+g_{m12}}{g_{m12}^{\ 2}}\right)\right] \tag{4.12}$$

$$\overline{V_{n,in}^2}\Big|_{M15,16} = \frac{1}{A_{v2}^2} \times \frac{2}{3} \times 4KT\left[\left(\frac{g_{m15} + g_{m16}}{g_{m15}^{\ 2}}\right)\right] \tag{4.13}$$

The total input noise can be found by adding (4.11), (4.12) and (4.13) with the noise density of resistor R (4KTR), and is expressed as (4.14).

$$\overline{V_{n,in}^2} = 2 \times \frac{2}{3} \times 4KT\left[\begin{array}{l}\left(\frac{g_{m3} + g_{m1}}{g_{m3}^{\ 2}}\right) + \left(\frac{g_{m6} + g_{m8}}{g_{m6}^{\ 2}}\frac{g_{m1}^{\ 2}}{g_{m3}^{\ 2}}\right) + \frac{3}{4}R \\ \left(\frac{g_{m12} + g_{m10}}{g_{m12}^{\ 2}}\right) + 0.5\left(\frac{g_{m15} + g_{m16}}{g_{m15}^{\ 2}}\frac{g_{m10}^{\ 2}}{g_{m12}^{\ 2}}\right)\end{array}\right] \tag{4.14}$$

Thus the output noise can be obtained by multiplying the gain of IA to the input noise.

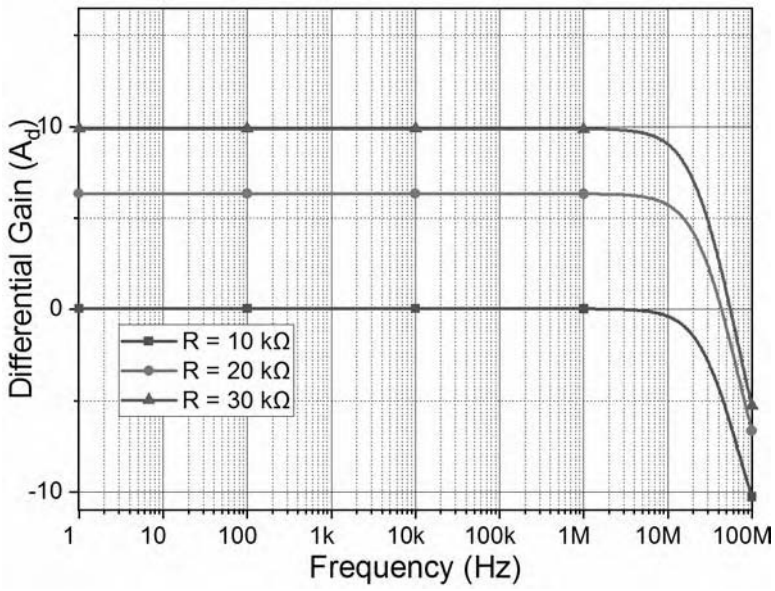
$$\overline{V_{n,out}^2} = g_m R \overline{V_{n,in}^2} \tag{4.15}$$

$$\overline{V_{n,out}^2} = 2 \times \frac{2}{3} \times 4KTg_m R\left[\begin{array}{l}\left(\frac{g_{m3} + g_{m1}}{g_{m3}^{\ 2}}\right) + \left(\frac{g_{m6} + g_{m8}}{g_{m6}^{\ 2}}\frac{g_{m1}^{\ 2}}{g_{m3}^{\ 2}}\right) + \frac{3}{4}R \\ \left(\frac{g_{m12} + g_{m10}}{g_{m12}^{\ 2}}\right) + 0.5\left(\frac{g_{m15} + g_{m16}}{g_{m15}^{\ 2}}\frac{g_{m10}^{\ 2}}{g_{m12}^{\ 2}}\right)\end{array}\right] \tag{4.16}$$

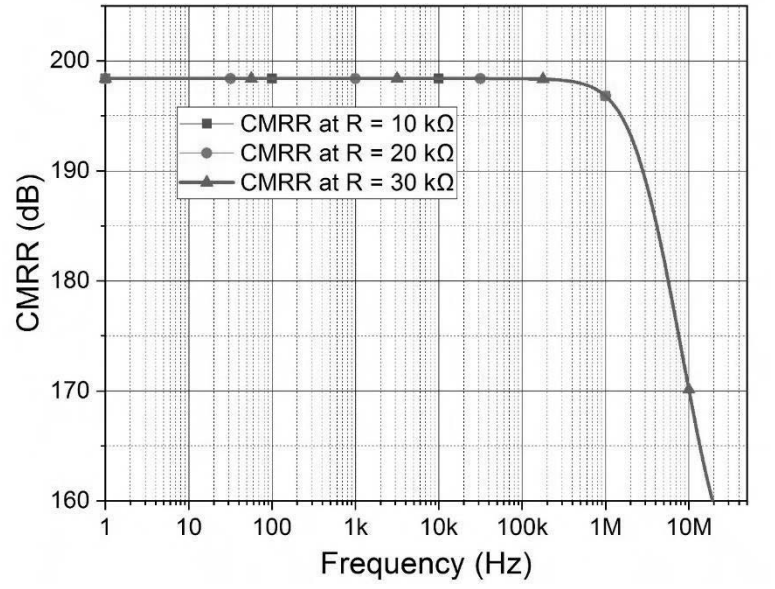
4.2.1.3 Simulation Results

The performance of the proposed IA is demonstrated through SPICE simulations using VDBA of Figure 2.4. The bias voltages V_{bias1} and V_{bias2} of -0.42 V and -0.075 V are applied. Figure 4.3 (a) and (b) show the simulated frequency responses for differential gain and CMRR respectively by selecting resistor R to be 10 kΩ, 20 kΩ and 30 kΩ. The simulated 3 dB frequency for the proposed IA is observed to be 38 MHz. The

simulated value of CMRR is obtained as 198 dB and corresponding 3 dB frequency is 2.81 MHz.



(a)

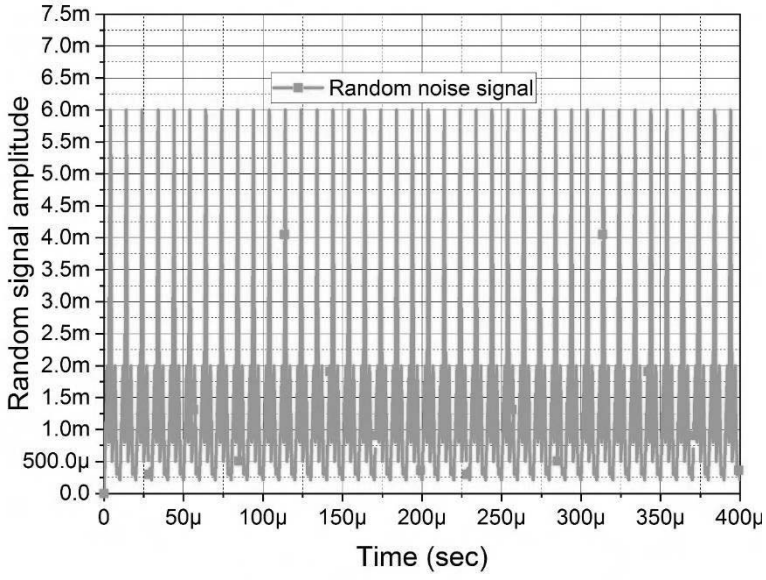


(b)

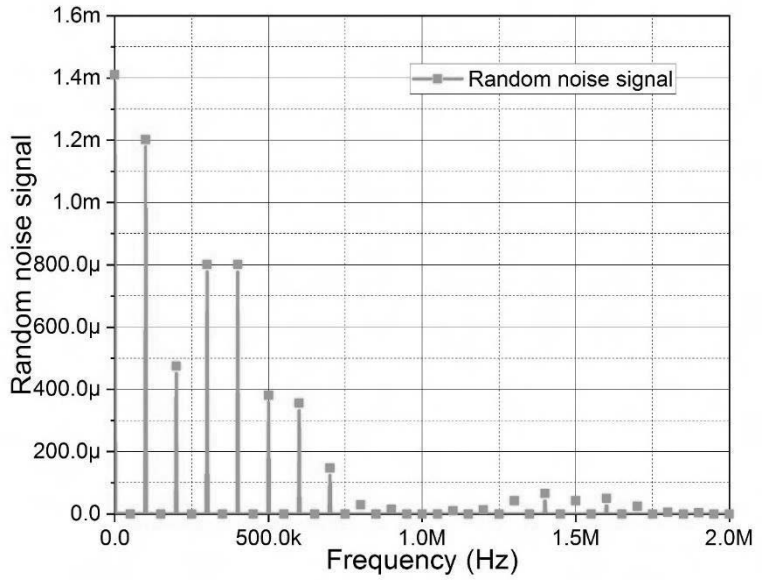
Figure 4.3 (a) Differential gain and (b) CMRR

The transient analysis of the circuit is carried out to show that the unwanted signals present at the input get rejected at the output of the IA. For this purpose, a random signal is superimposed over 20 mV, 500 kHz differential signal. This combined signal is

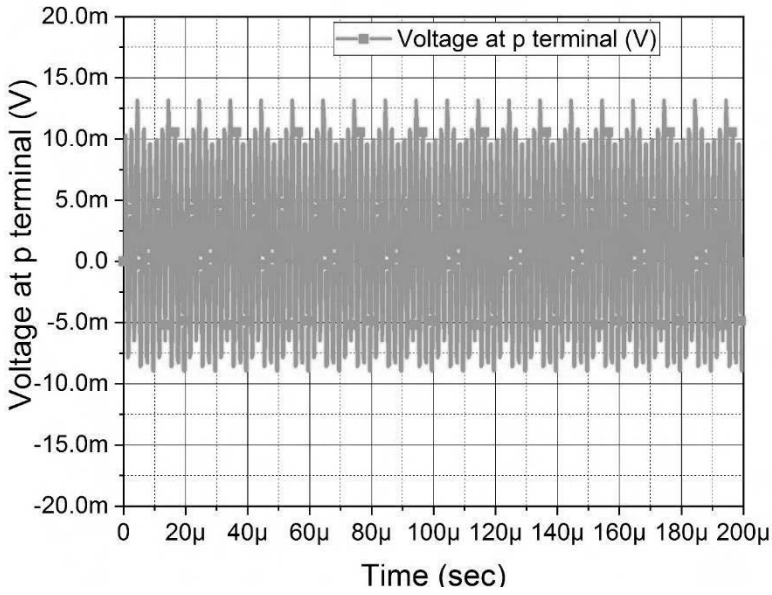
applied to the input of the IA. The differential gain of the amplifier is chosen to be unity. The input transient signal and corresponding frequency spectrum of the input signal are shown in Figure 4.4 respectively.



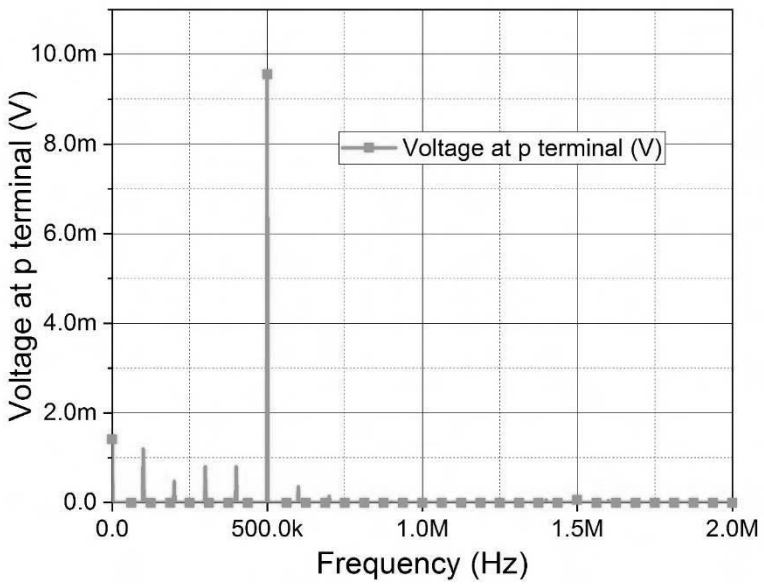
(a)



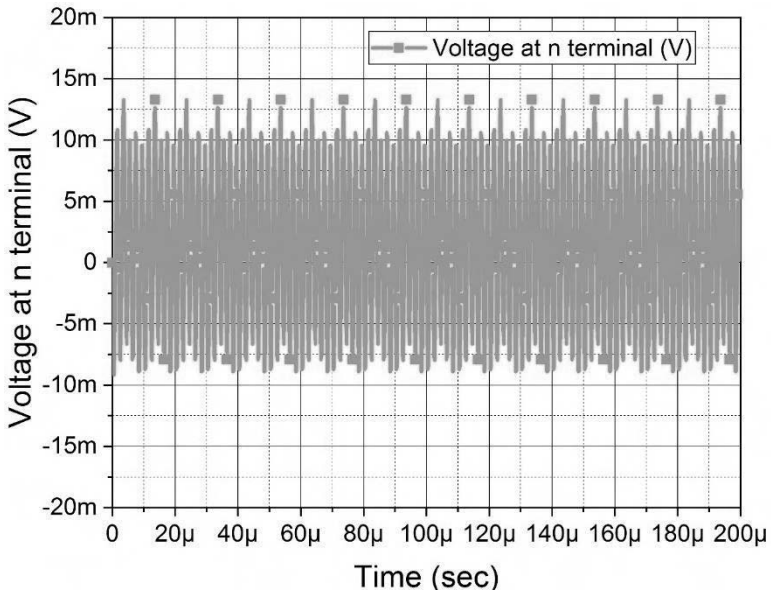
(b)


Voltage at p terminal (V)
Voltage at p terminal (V)
20.0m
15.0m
10.0m
5.0m
0.0
-5.0m
-10.0m
-15.0m
-20.0m
0
20µ
40µ
60µ
80µ
100µ
120µ
140µ
160µ
180µ
200µ
Time (sec)

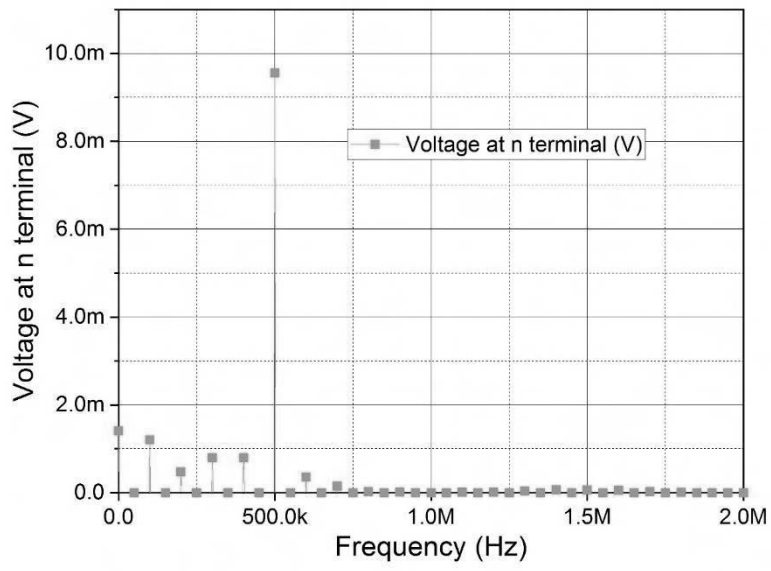
(c)


Voltage at p terminal (V)
Voltage at p terminal (V)
10.0m
8.0m
6.0m
4.0m
2.0m
0.0
0.0
500.0k
1.0M
1.5M
2.0M
Frequency (Hz)

(d)



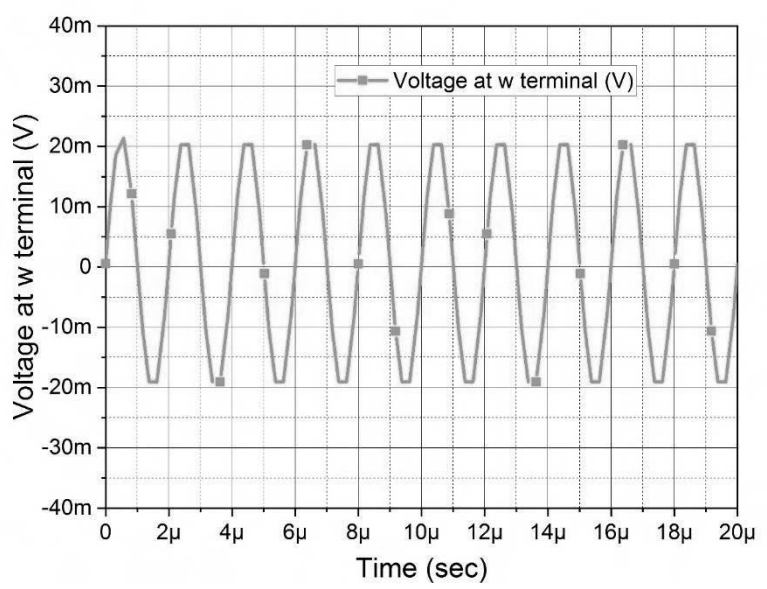
(e)



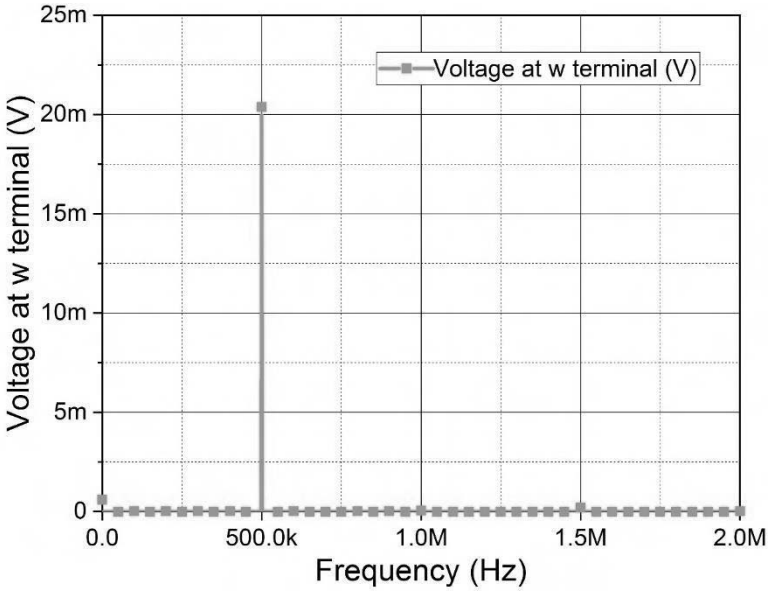
(f)

Figure 4.4 Input signal (a) Random Noise Transient, (b) Noise Frequency spectrum; Overall signal at p terminal (c) Transient, (d) Frequency spectrum; and Overall signal at n terminal (e) Transient, (f) Frequency spectrum

The output transient is shown in Figure 4.5 (a) with its spectrum in Figure 4.5 (b). It is clearly visible from the output transient that random signal is suppressed and the desired 500 kHz frequency signal is faithfully reproduced.



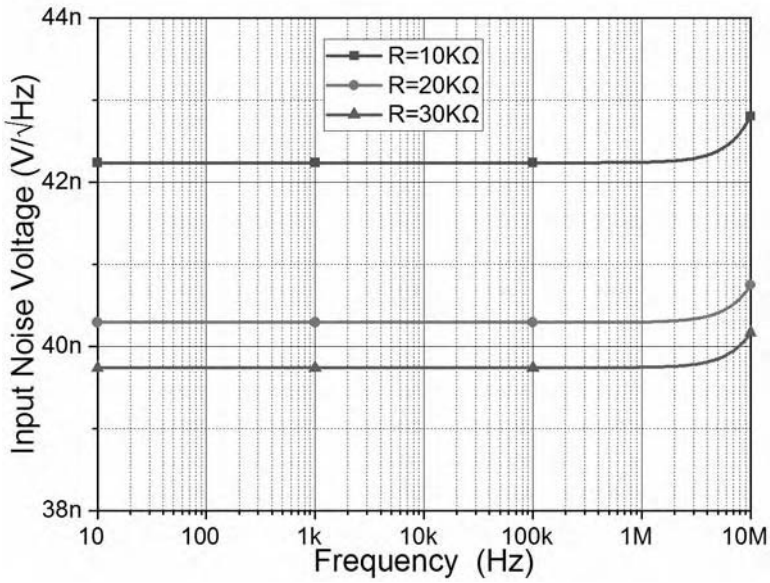
(a)



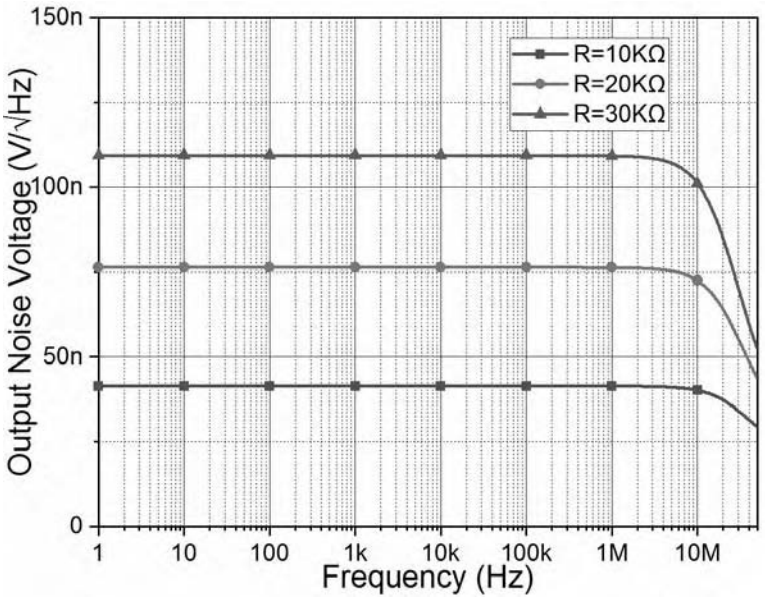
(b)

Figure 4.5 Output signal (a) transient and (b) frequency spectrum

The noise performance of the proposed topology is also examined through SPICE simulations. The input and output noise spectrums at different values of R are depicted in Figure 4.6 (a) and Figure 4.6 (b) respectively. The simulated input noise density value found to be and is in close approximation with the theoretical values of 39.5 nV/√Hz.



(a)

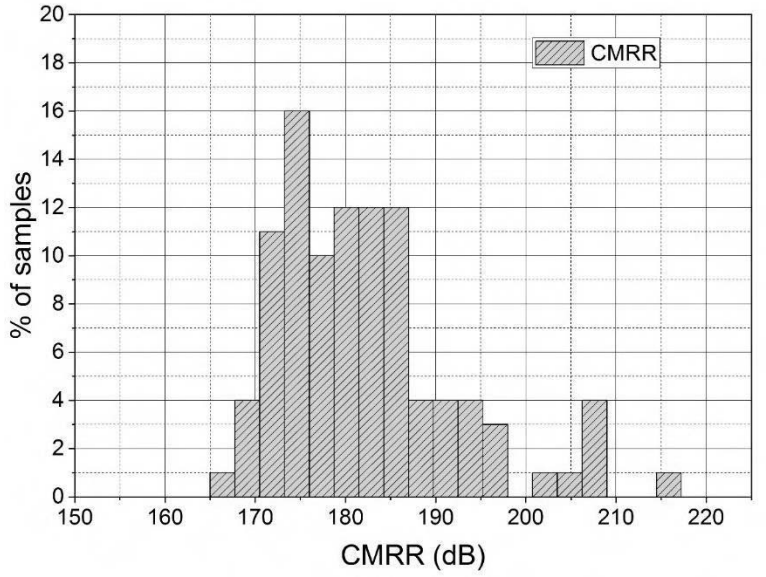


(b)

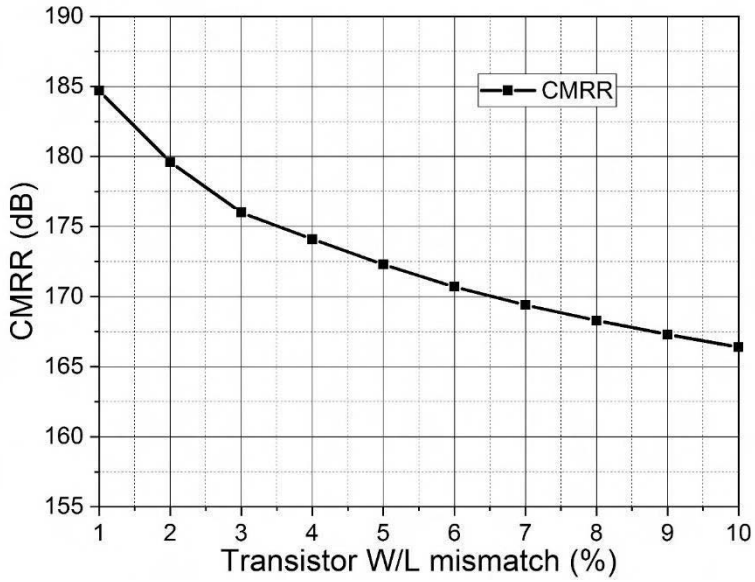
Figure 4.6 (a) Input Noise and (b) Output Noise

To investigate the effect of mismatches on the CMRR performance of the proposed circuit, Monte Carlo simulations are performed by considering 5 % deviations in mobility (μ_o), oxide thickness (t_{ox}) and threshold voltage (V_{TH}) of transistors. The derived histogram after 100 simulation runs for the proposed topology is shown in Figure 4.7 (a). The average value of 182 dB for the CMRR is observed. Further, the

effect of mismatch between the W/L of the M_3 and M_4 (differential pair) is also observed through simulations and the results obtained are shown in Figure 4.7 (b).



(a)

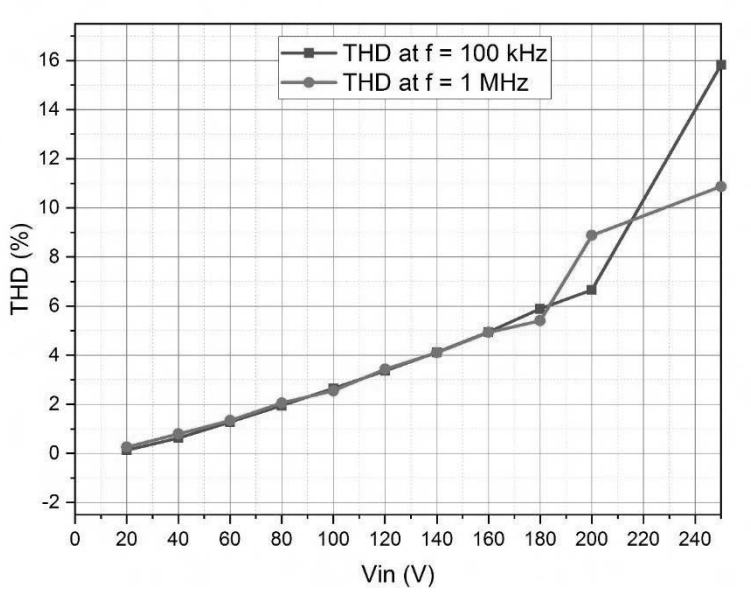


(b)

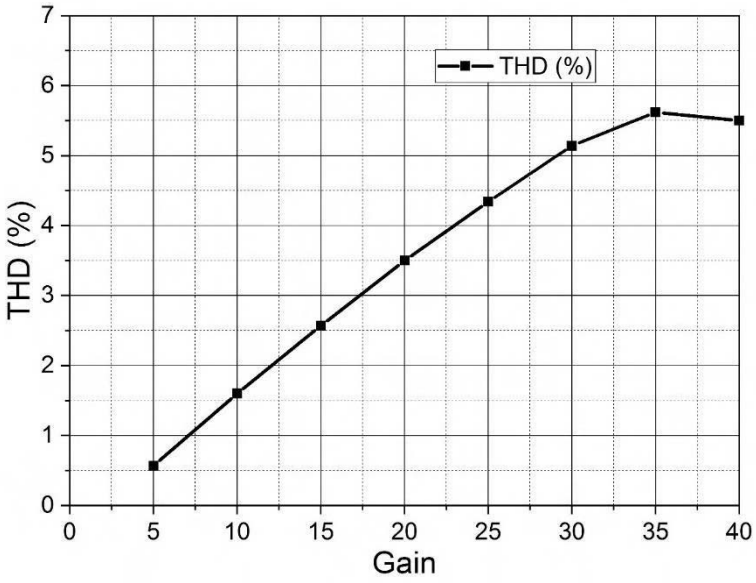
Figure 4.7 (a) Monte Carlo Analysis for CMRR and (b) CMRR Vs W/L mismatch of M_3 and M_4

To evaluate the linearity of proposed IA, the total harmonic distortion (THD) simulations are carried out. The variation of THD input signal at the frequencies of 100 kHz and 1 MHz is shown in Figure 4.8 (a). Further, the variation of THD w.r.t the

gain is depicted in Figure 4.8 (b). It may be observed that the THD remains below 6 % for input signal < 180 mV and gain value of 40.



(a)



(b)

Figure 4.8 (a) THD Vs V_{in} and (b) THD Vs Gain

4.3 Electronics Filters

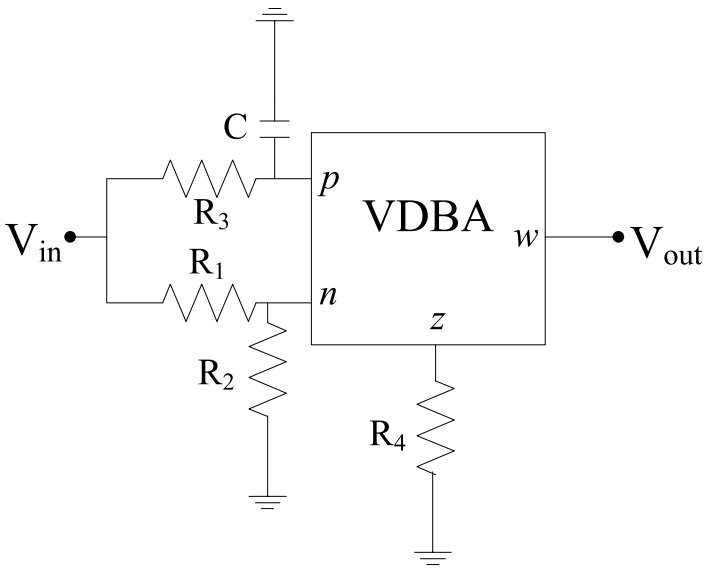
Filters are the essential building block in analog signal processing and find widespread usage in instrumentation and communication systems. These are frequency selective networks that allow a specified range of frequencies to be passed known as filter pass band, while attenuates frequencies outside this range known as filter stop band.

In this chapter three filter configurations have been proposed. A first order APF using a single VDBA is presented first which can be configured to provide both inverting and non-inverting outputs. The second topology is a single VDBA based SISO biquad filter which can be used to design LPF, HPF and BPF functions with appropriate selection of component. It can provide high Q with moderate component spread. The third proposed topology is a MISO universal filter which provides different responses with appropriate input selection.

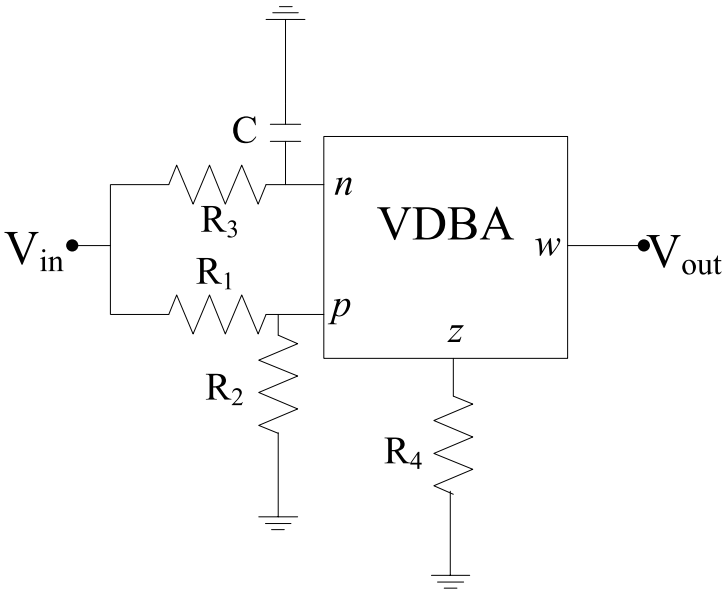
4.3.1 Proposed First Order APF

An APF is a two port network that allows all input signal frequencies to pass with altered phases. An APF is also termed as a phase shifter. The phase variation can be designed as per the requirement of the application. It is usually used in communication and instrumentation such as to match the phases in systems, to produce delays in circuits and to create 90° phase shifts for quadrature modulators etc.

The proposed first order APF consists of a VDBA, a grounded capacitor and four resistors two of which are grounded. It can be configured either as non-inverting or inverting APF. Figure 4.9 (a) and (b) show the non-inverting and inverting APF respectively.



(a)



(b)

Figure 4.9 The proposed First order (a) non-inverting and (b) inverting APF configurations

Using routine analysis the transfer function (TF) $H_1(s)$ of proposed non-inverting APF can be expressed as

$$H_1(s)=\frac{V_{out}}{V_{in}}=g_m R_4 \frac{R_1(1-sCR_3\frac{R_2}{R_1})}{(R_1+R_2)(1+sCR_3)} \tag{4.17}$$

Considering R_1=R_2 the transfer function modifies to

$$H_1(s) = \frac{V_{out}}{V_{in}} = \frac{g_m R_4}{2} \frac{(1 - sCR_3)}{(1 + sCR_3)}$$

(4.18)

Similarly, the TF for the inverting APF represented as $H_2(s)$ can be obtained as

$$H_2(s) = \frac{V_{out}}{V_{in}} = -\frac{g_m R_4}{2} \frac{(1 - sCR_3)}{(1 + sCR_3)}$$

(4.19)

The structure provides a gain of (g_mR4/2) which can be set to unity, by selecting g_mR4 = 2, if required. The phase angles are calculated as $\angle H_1(s) = -2\tan^{-1}(\omega CR_3)$ and $\angle H_2(s) = \pi - 2\tan^{-1}(\omega CR_3)$ for non-inverting and inverting configurations respectively.

4.3.1 1 Non-Ideal Analysis

In this subsection taking non-idealities of VDBA into consideration, the non-inverting APF of Figure 4.9 (a) gets modified as depicted in Figure 4.10.

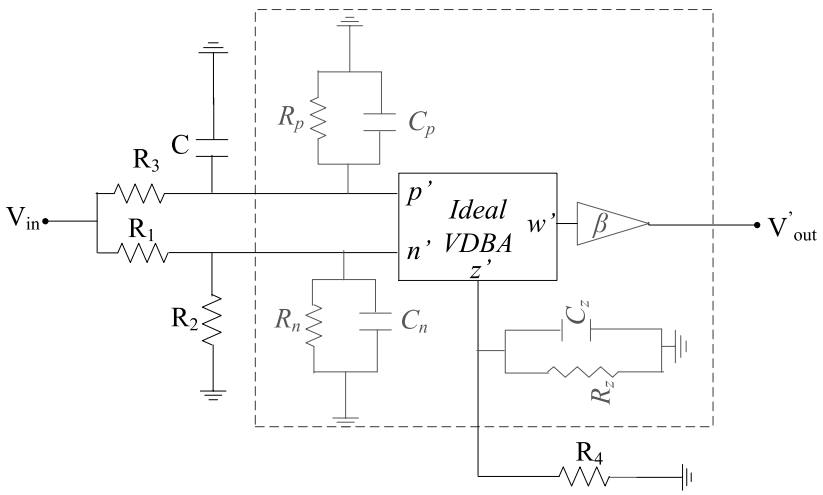


Figure 4.10 Non-Ideal structure of non-inverting APF

Analyzing Figure 4.10 the $V_p^{'}$ and $V_n^{'}$ ca be written as (4.20) and (4.21) respectively.

$$V_p^{'} = \frac{1}{sR_3(C+C_p)+1+\frac{R_3}{R_p}} V_{in}$$

(4.20)

$$V_n^{'} = \frac{1}{sR_1C_n+2+\frac{R_1}{R_n}} V_{in} \qquad \text{; assuming } R_1=R_2$$

(4.21)

From the terminal characteristics of non-ideal VDBA, $I_z^{'}$ may be obtained as

$$I_z^{'} = \alpha g_m(V_p^{'}-V_n^{'}) = \frac{\alpha g_m(1-s(R_3C+R_3C_p-R_1C_n))}{\left(sR_3(C+C_p)+1+\frac{R_3}{R_p}\right)\left(sR_1C_n+2+\frac{R_1}{R_n}\right)} V_{in}$$

(4.22)

Using nodal equation the I_z' can also be written as

$$I_z^{'} = \frac{V_z^{'}\left(sR_zC_z+1+\frac{R_4}{Rz}\right)}{R_4}$$

(4.23)

Equating (4.22) and (4.23), the $V_z^{'}$ can be obtained as

$$V_z^{'} = \frac{\alpha g_m R_4(1-s(R_3C+R_3C_p-R_1C_n))}{2\left(sR_3(C+C_p)+1+\frac{R_3}{R_p}\right)\left(\frac{sR_1C_n}{2}+1+\frac{R_1}{2R_n}\right)\left(sR_zC_z+1+\frac{R_4}{Rz}\right)} V_{in}$$

(4.24)

Further, the output voltage $V_{out}^{'}$ with non-idealities can be expressed as

$$V_{out}^{'} = V_w^{'} = \beta V_z^{'}$$

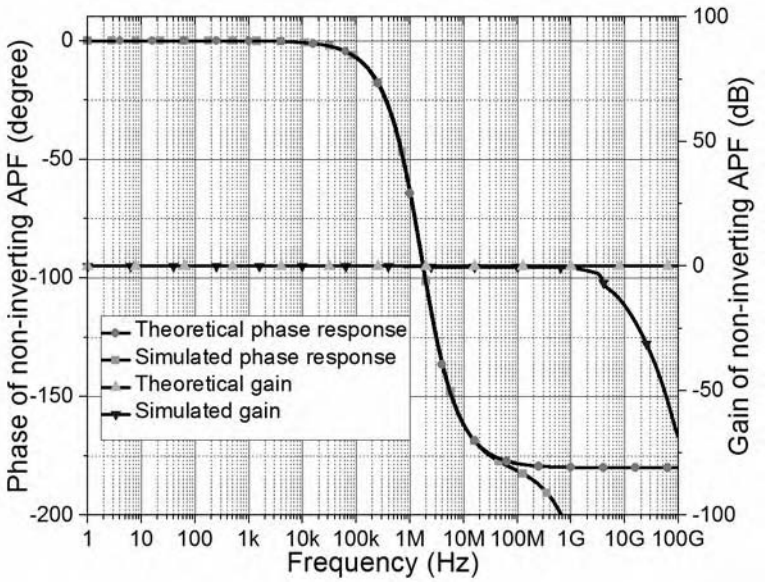
(4.25)

$$\frac{V_{out}^{'}}{V_{in}} = \alpha\beta\frac{g_m R_4}{2}\frac{(1-s(R_3C+R_3C_p-R_1C_n))}{\left(sR_3(C+C_p)+1+\frac{R_3}{R_p}\right)\left(sR_1C_n/2+1+\frac{R_1}{2R_n}\right)\left(sR_zC_z+1+\frac{R_4}{Rz}\right)} \quad (4.26)$$

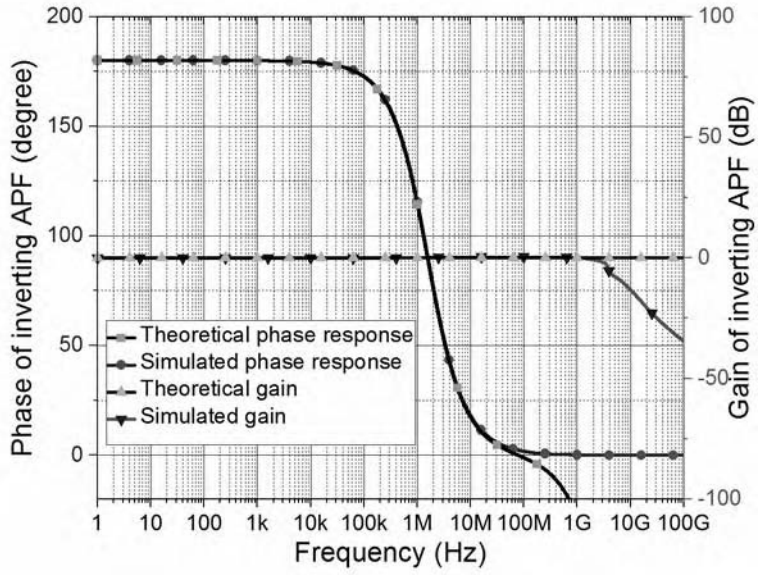
It may be observed that non-ideality of VDBA affects the TF of the proposed APF but selecting $C >> C_p(C_n)/C_z$, and $R_3 << R_p$, $R_1 << R_n$, $R_4 << R_z$, the first term in denominator becomes the dominant pole and the effects of parasitics may be ignored.

4.3.1.2 Simulation Results

The behavior of the proposed APF is validated through SPICE simulation using VDBA of Figure 2.4. The proposed inverting and non-inverting APF configurations are simulated for a right phase frequency of f_0 = 1.59 MHz for which component values are taken as C = 100 pF, R_i (i=1, 2 and 3) = 1 kΩ and R_4 = 1.5 kΩ. The frequency response of the proposed filter topologies both inverting and non-inverting is depicted in Figure 4.11 (a) and Figure 4.11 (b) respectively. It is pertinent to mention here that the proposed VDBA based voltage mode APF outperforms in AC behavior as compared to the traditional Op-Amp amp based VM APF. The high frequency performance of the Op-Amp based circuits is limited due to constant gain-bandwidth product and low slew rate of the Op-Amps.



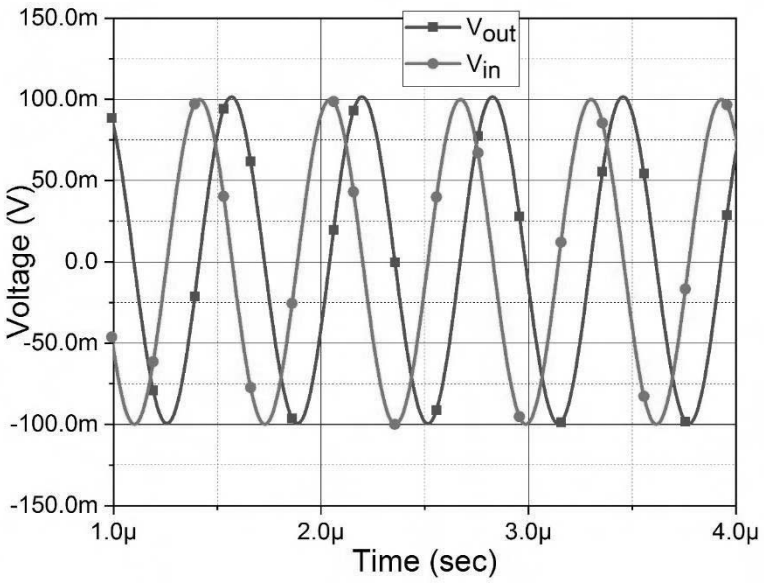
(a)



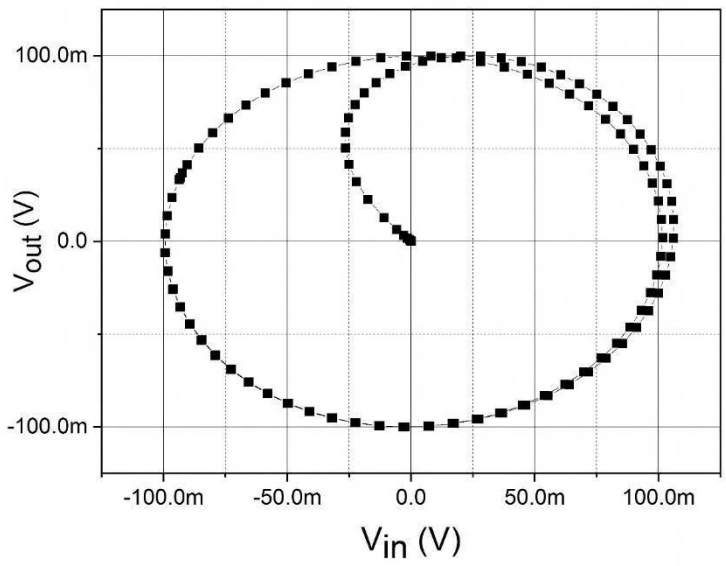
(b)

Figure 4.11 The frequency response of (a) non-inverting APF and (b) inverting APF

The proposed APF is simulated for the transient response at an input frequency of 1.59 MHz as shown in Figure 4.12 (a). Figure 4.12 (b) confirms the 90° phase shift.



(a)

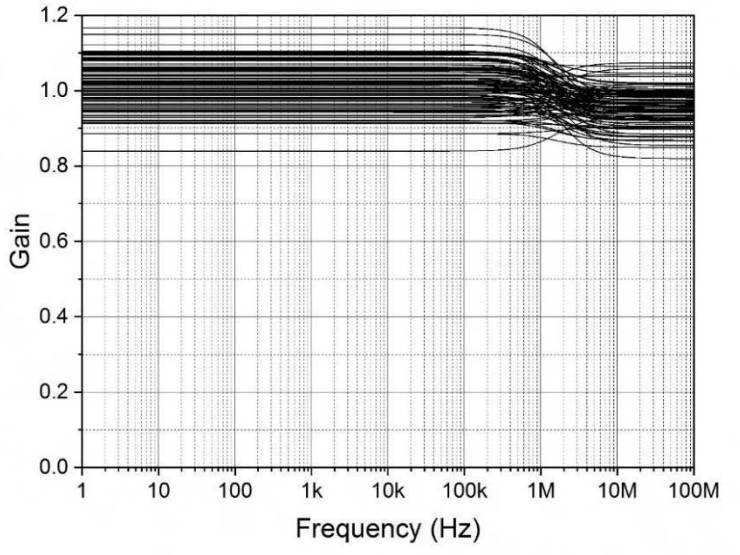


(b)

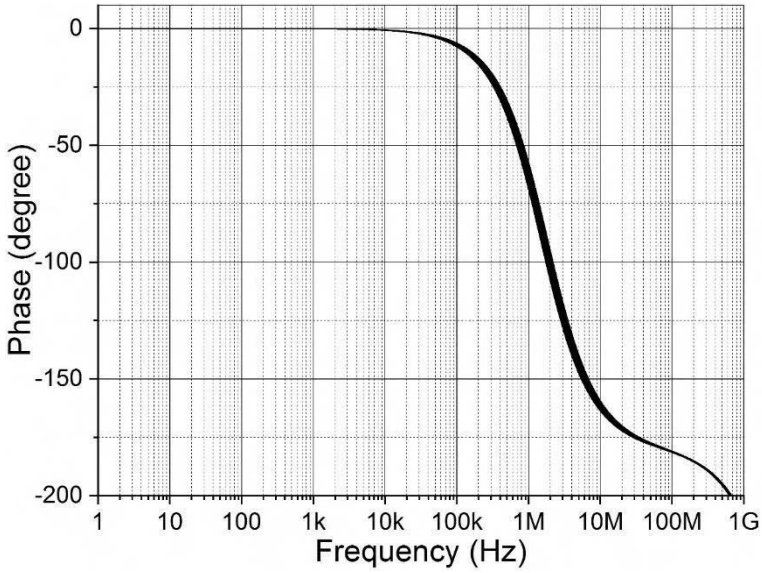
Figure 4.12 (a) Transient response of non-inverting APF and (b) Lissajous pattern at right phase frequency

The effect of component variation on frequency response is studied through Monte Carlo simulations with 5 % tolerance band for all the resistors and capacitor. The simulated gain and phase responses are shown in Figure 4.13 (a) and Figure 4.13 (b) respectively. Further Figure 4.13 (c) and Figure 4.13 (d) show the results in the form of

histograms for gain and phase respectively. The statistical results so obtained are summarized in Table 4.2.



(a)



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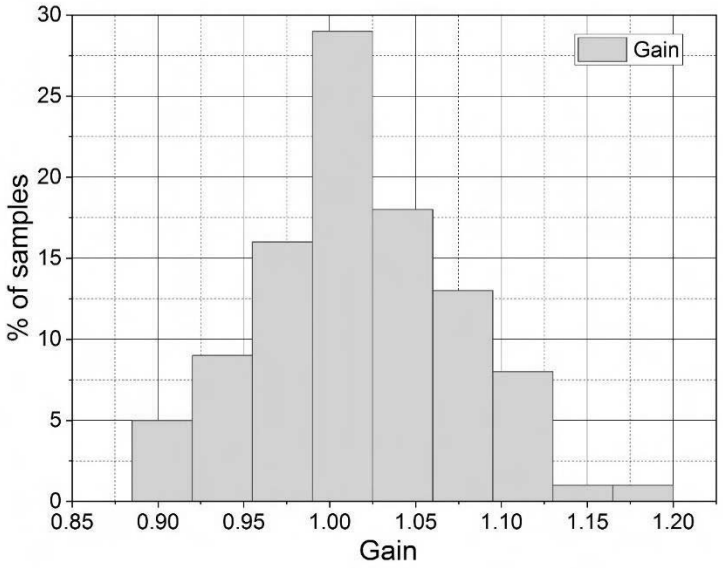
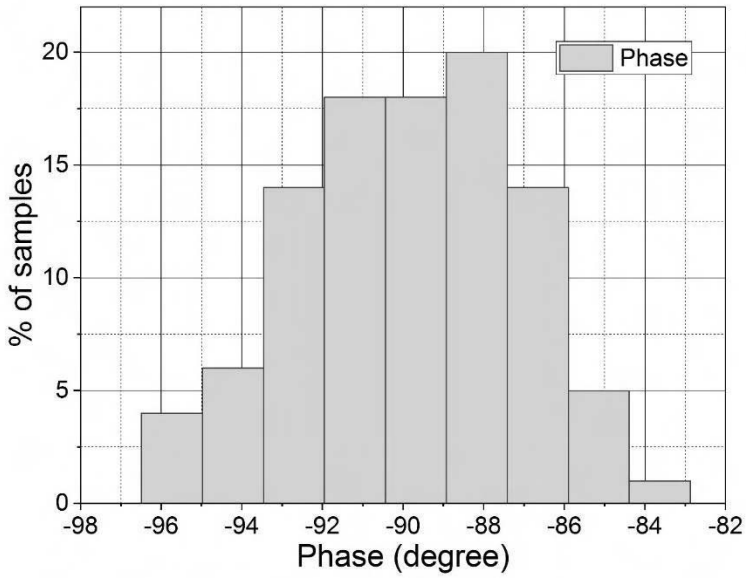


(c)



(d)

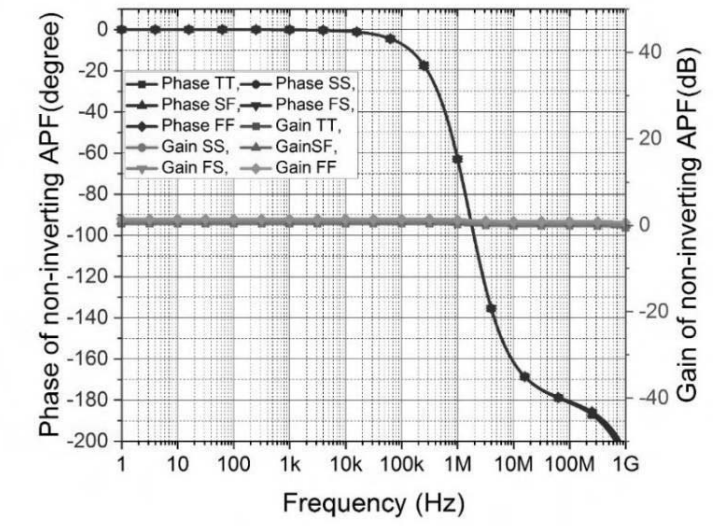
Figure 4.13 Monte Carlo analysis for (a) gain and (b) phase responses; Monte Carlo histograms for (c) gain and (d) phase of the proposed non-inverting APF

Table 4.2 Statistical results observed through Monte Carlo histograms

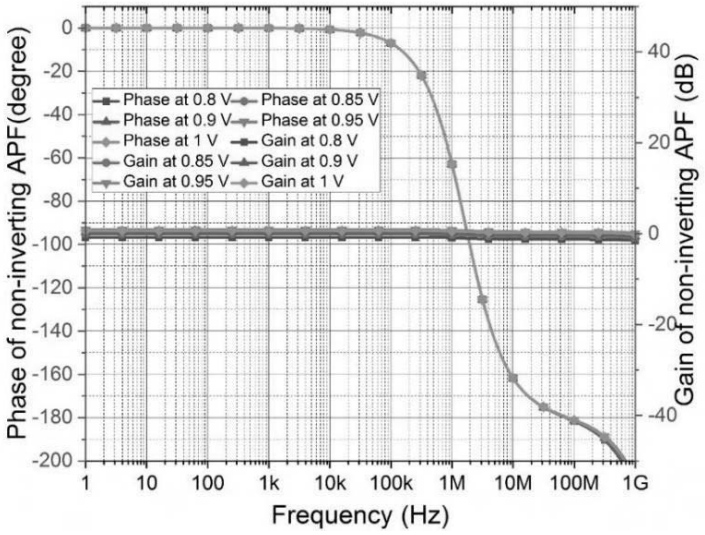
Type of Response	Statistical Results			
	Number of samples	Mean	Median	Standard Deviation
Magnitude(Gain)	100	1.018	1.017	0.056
Phase	100	-89.82°	-89.86°	2.75°

It can be concluded from Table 4.2 that the proposed APF has very low sensitivity to component variations.

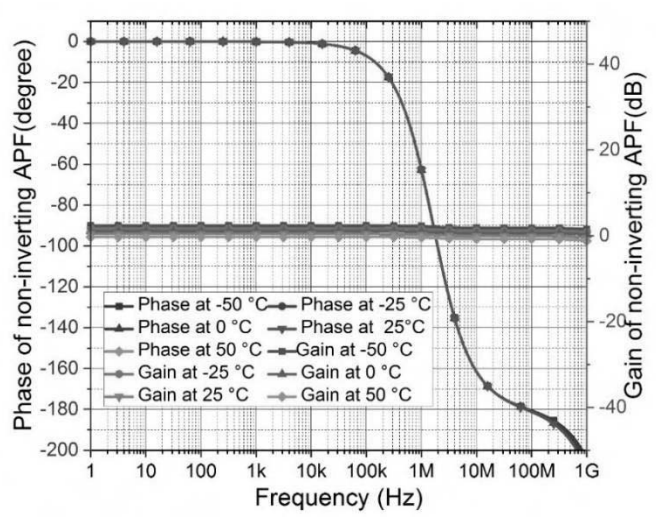
The frequency response of the proposed APF is also investigated under process corners, supply voltage, and temperature variations. The simulated magnitude and phase responses at the five different corners are shown in Figure 4.14 (a). The frequency responses when the supply voltage is varied from 0.8 V to 1 V in steps of 0.05 V are depicted in Figure 4.14 (b). Similarly, the temperature dependence of the proposed structure is shown in Figure 4.14 (c). It may be observed that the process corners, supply and temperature variation have a very low impact on the proposed APF.



(a)



(b)



(c)

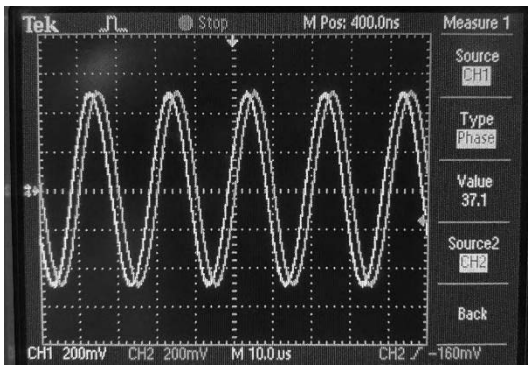
Figure 4.14 Gain and Phase response of non-inverting APF at different (a) corners, (b) supply voltages and (c) temperatures

4.3.1.3 Experiment Results

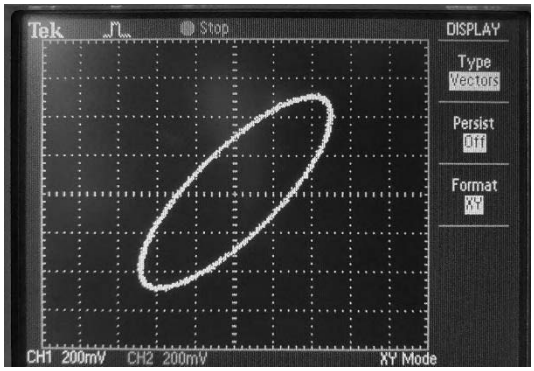
The CFOA based VDBA shown in Figure 2.13 is used to obtain the experimental results. The supply voltages are taken as ±12 V. To test the proposed APF experimentally an input sinusoidal signal having amplitude as 1 V is applied and the signal frequency is varied to get a phase shifted outputs. The frequency settings and corresponding results have been summarized in Table 4.3. The experimental outputs have been depicted in Figure 4.15 in accordance to Table 4.3.

Table 4.3 The frequency settings and corresponding results

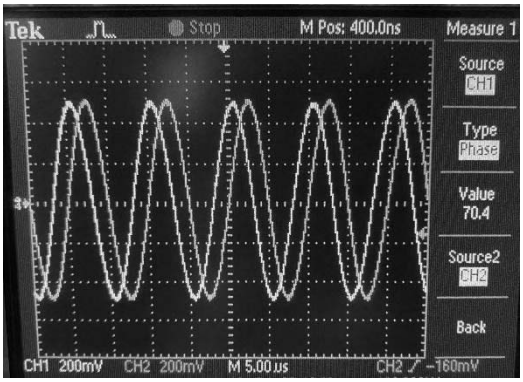
Signal Frequency (kHz)	Time domain response	Lissajous pattern	Phase Shift	
			Theoretical	Experimental
50	Fig. 4.15(a)	Fig. 4.15(b)	-35°	-37°
100	Fig. 4.15 (c)	Fig. 4.15(d)	-65°	-70.4°
250	Fig. 4.15 (e)	Fig. 4.15(f)	-115°	-125°



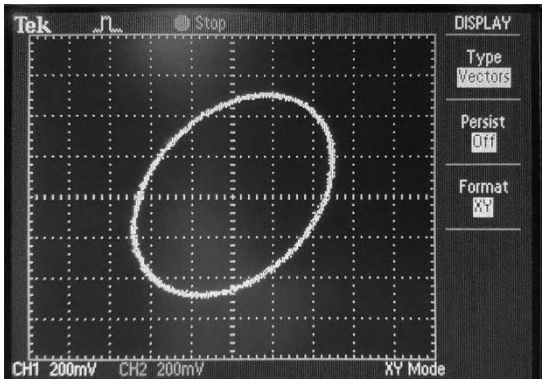
(a)



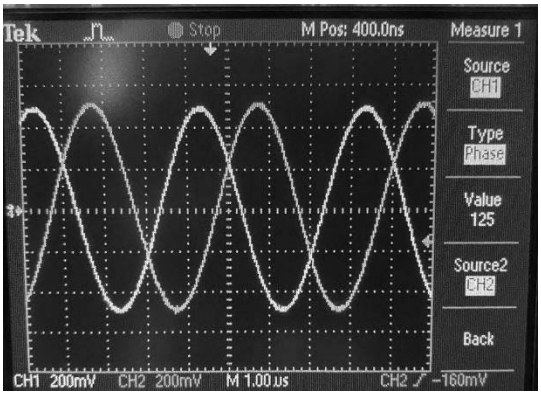
(b)



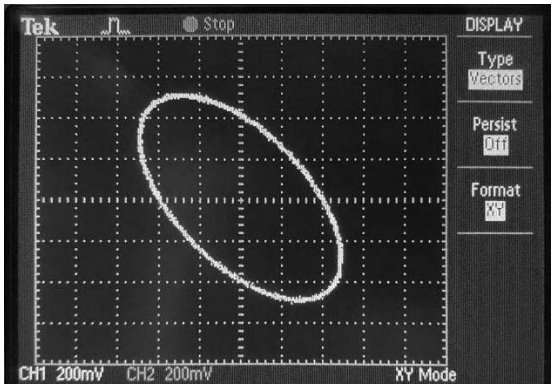
(c)



(d)



(e)



(f)

Figure 4.15 Time domain responses and corresponding Lissajous patterns obtained experimentally at frequencies of (a) and (b) 50 kHz, (c) and (d) 100 kHz and (e) and (f) 250 kHz.

4.3.2 Proposed SISO Multifunction Filter

The second topology is a SISO multifunction filter as shown in Figure 4.16. It uses a single VDBA. The proposed topology is used to realize three (LPF, HPF and BPF) filter configurations with suitable admittance selection.

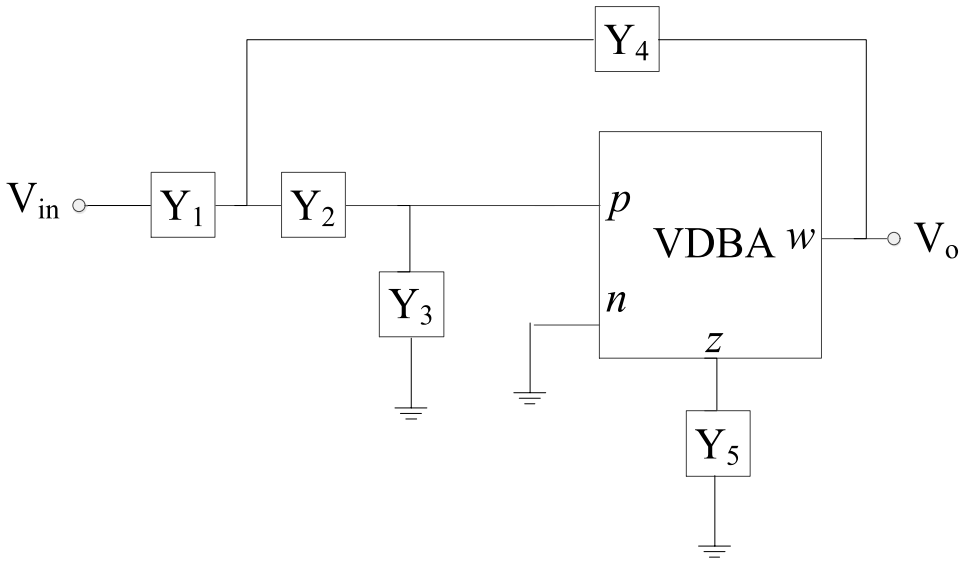


Figure 4.16 The proposed SISO multifunction filter

Using routine circuit analysis its voltage TF may be obtained as (4.27)

$$\frac{Vo}{Vin}=\frac{KY_1\ Y_2}{Y_1\ Y_2+Y_1\ Y_3+Y_2\ Y_3+Y_2\ Y_4(1-K)+Y_3\ Y_4} \tag{4.27}$$

where $K=\frac{g_m}{Y_5}$ (4.28)

The three filter responses can be realized through proper selection of admittances, as summarized in Table 4.4.

Table 4.4 Selection of admittance for specific filter response

Filter Response	Y_1	Y_2	Y_3	Y_4	Y_5
LPF	G_1	G_2	sC_3	sC_4	G_5
HPF	sC_1	sC_2	G_3	G_4	G_5
BPF	G_1	sC_2	G_3+sC_3	G_4	G_5

With the admittance choices given in Table 4.4, the TF for the LPF, HPF and BPF can be derived as

$$\left(\frac{V_O}{V_{in}}\right)_{LPF} = \frac{K\dfrac{G_1G_2}{C_3C_4}}{s^2 + s\left(\dfrac{C_3(G_1+G_2)+G_2C_4(1-K)}{C_3C_4}\right)+\dfrac{G_1G_2}{C_3C_4}} \tag{4.29}$$

$$\left(\frac{V_O}{V_{in}}\right)_{HPF} = \frac{Ks^2}{s^2 + s\left(\dfrac{G_3(C_1+C_2)+G_4C_2(1-K)}{C_1C_2}\right)+\dfrac{G_3G_4}{C_1C_2}} \tag{4.30}$$

$$\left(\frac{V_O}{V_{in}}\right)_{BPF} = \frac{Ks\dfrac{G_1}{C_3}}{s^2 + s\left(\dfrac{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4C_2(1-K)}{C_2C_3}\right)+\dfrac{G_3(G_1+G_4)}{C_2C_3}} \tag{4.31}$$

The ω_0, Q_0 and filter gain (H_0) for the three responses may be obtained from equation (4.29-4.31) and for equal component values are enlisted in Table 4.5.

Table 4.5 Parameters of the specific filter response for equal component values

Filter Response	ω_0	Q_0	H_0
LPF	G/C	1/(3-K)	K
HPF	G/C	1/(3-K)	K
BPF	√2G/C	√2/(5-K)	K/(5-K)

4.3.2.1 Sensitivity Analysis

The sensitivity of network parameters to its circuit components is an important performance criterion. The sensitivities of ω_0 and Q_0 of the proposed SISO filter topology with respect to passive components are summarized in Table 4.6.

Table 4.6 Passive Sensitivity Analysis

Filter Response	Passive Component (Y)	$S_Y^{\omega_0}$	$S_Y^{Q_0}$
LPF	G_1	$\frac{1}{2}$	$\frac{1}{2}-\frac{C_3G_1}{C_3(G_1+G_2)+G_2C_4(1-K)}$
	G_2	$\frac{1}{2}$	$\frac{1}{2}-\frac{C_3G_2+C_4G_2(1-K)}{C_3(G_1+G_2)+G_2C_4(1-K)}$
	C_3	$-\frac{1}{2}$	$\frac{1}{2}-\frac{C_3(G_1+G_2)}{C_3(G_1+G_2)+G_2C_4(1-K)}$
	C_4	$-\frac{1}{2}$	$\frac{1}{2}-\frac{C_4G_2(1-K)}{C_3(G_1+G_2)+G_2C_4(1-K)}$
HPF	C_1	$-\frac{1}{2}$	$\frac{1}{2}-\frac{C_1G_3}{G_3(C_1+C_2)+G_4C_2(1-K)}$
	C_2	$-\frac{1}{2}$	$\frac{1}{2}-\frac{C_2(G_3+G_4(1-K))}{G_3(C_1+C_2)+G_4C_2(1-K)}$
	G_3	$\frac{1}{2}$	$\frac{1}{2}-\frac{G_3(C_1+C_2)}{G_3(C_1+C_2)+G_4C_2(1-K)}$
	G_4	$\frac{1}{2}$	$\frac{1}{2}-\frac{G_4C_2(1-K)}{G_3(C_1+C_2)+G_4C_2(1-K)}$
BPF	G_1	$\frac{1}{2}-\frac{1}{2}\frac{G_3G_4}{G_3(G_1+G_4)}$	$\frac{1}{2}\frac{G_1}{(G_1+G_4)}-\frac{G_1(C_2+C_3)}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4C_2(1-K)}$
	G_3	$\frac{1}{2}$	$\frac{1}{2}-\frac{G_3C_2}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4C_2(1-K)}$
	G_4	$\frac{1}{2}-\frac{1}{2}\frac{G_3G_1}{G_3(G_1+G_4)}$	$\frac{1}{2}\frac{G_4}{(G_1+G_4)}-\frac{G_4(C_3+C_2(1-K))}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4C_2(1-K)}$
	C_2	$-\frac{1}{2}$	$\frac{1}{2}-\frac{C_2(G_1+G_3)+G_4C_2(1-K)}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4C_2(1-K)}$
	C_3	$-\frac{1}{2}$	$\frac{1}{2}-\frac{C_3(G_1+G_4)}{C_3(G_1+G_4)+C_2(G_1+G_3)+G_4C_2(1-K)}$

From the Table 4.6 it is observed that the three proposed configuration have low sensitivity to parameter variations as passive sensitivities are <= 0.5 in magnitude.

4.3.2.2 Non-Ideal Analysis

This subsection presents the effect of non-idealities of VDBA on the behavior of the proposed SISO filter topology. Considering VDBA non-idealities, the non-ideal model for proposed SISO multifunction filter topology is shown in Figure 4.17.

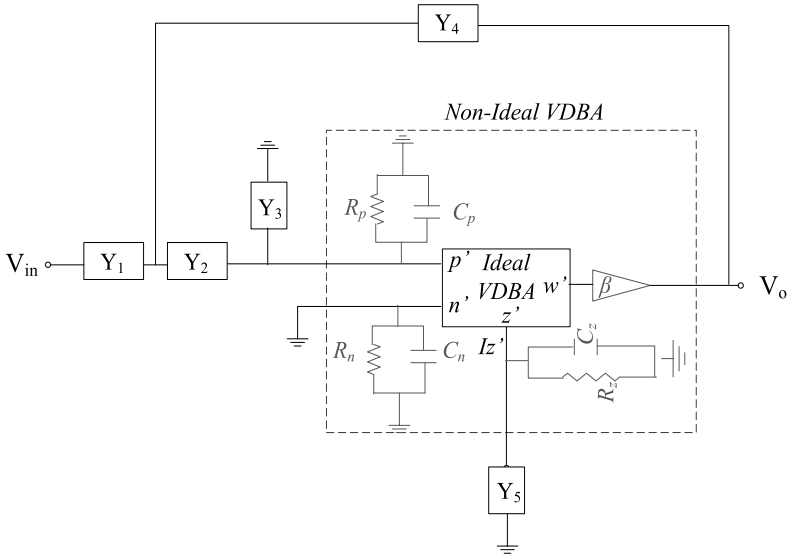


Figure 4.17 Non-ideal structure of SISO multifunction filter

Using routine analysis the TF for the non-ideal structure may be written as

$$\left.\frac{V_o}{V_{in}}\right|_{non-ideal} = \frac{\beta K' Y_1 Y_2}{Y_1 Y_2 + Y_1 Y_3^{'} + Y_2 Y_3^{'} + Y_2 Y_4 + Y_3^{'} Y_4 - K' \beta Y_2 Y_4} \tag{4.32}$$

where $K' = \frac{g_m}{Y_5^{'}}$. (4.33)

Analyzing Figure 4.17, the Y_5' and Y_3' can be expressed as (4.34) and (4.35) respectively.

$$Y_5^{'} = Y_5 + G_z + \frac{1}{sC_z}$$

(4.34)

$$Y_3^{'} = Y_3 + G_p + \frac{1}{sC_p}$$

(4.35)

The TF for LPF, HPF and BPF under non-ideal conditions may be derived as (4.36), (4.37) and (4.38) respectively.

$$\left(\frac{V_O}{V_{in}}\right)_{LPF\_n} = \frac{K'\beta \dfrac{G_1 G_2}{(C_3 + C_p)C_4}}{s^2 + s\left(\dfrac{(C_3 + C_p)(G_1 + G_2) + G_2 C_4(1 + G_p/G_2 - K'\beta)}{(C_3 + C_p)C_4}\right) + \dfrac{(G_1 + G_2)G_p + G_1 G_2}{(C_3 + C_p)C_4}}$$

(4.36)

$$\left(\frac{V_O}{V_{in}}\right)_{HPF\_n} = \frac{K'\beta s^2 \dfrac{C_1 C_2}{C_1 C_2 + (C_1 + C_2)C_p}}{s^2 + s\left(\dfrac{(G_3 + G_p)(C_1 + C_2) + G_4 C_2(1 - K'\beta + C_p/C_2)}{C_1 C_2 + (C_1 + C_2)C_p}\right) + \dfrac{(G_3 + G_3)G_4}{C_1 C_2 + (C_1 + C_2)C_p}}$$

(4.37)

$$\left(\frac{V_O}{V_{in}}\right)_{BPF\_n} = \frac{K'\beta s \dfrac{G_1}{(C_3 + C_p)}}{s^2 + s\left(\dfrac{(C_3 + C_p)(G_1 + G_4) + C_2(G_1 + G_p + G_3) + G_4 C_2(1 - K'\beta)}{C_2(C_3 + C_p)}\right) + \dfrac{(G_3 + G_p)(G_1 + G_4)}{C_2(C_3 + C_p)}}$$

(4.38)

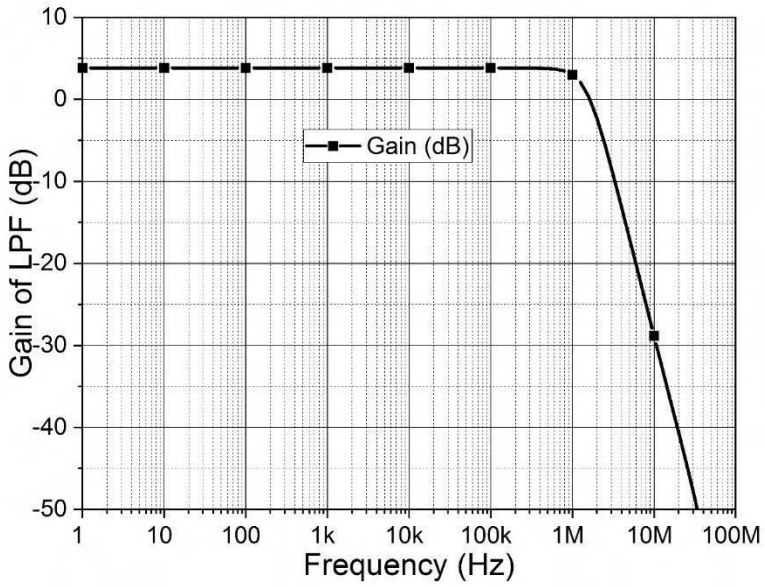
It is clear that non-idealities of VDBA introduce parasitic poles and zeros in the TFs causing some discrepancies from the ideal behaviour. Since $Y_3 >> (G_p+sC_p)$, $G_5 >> (G_z+sC_z)$ and approximating β to unity, these deviations may be rendered ineffective.

4.3.2.3 Simulation Results

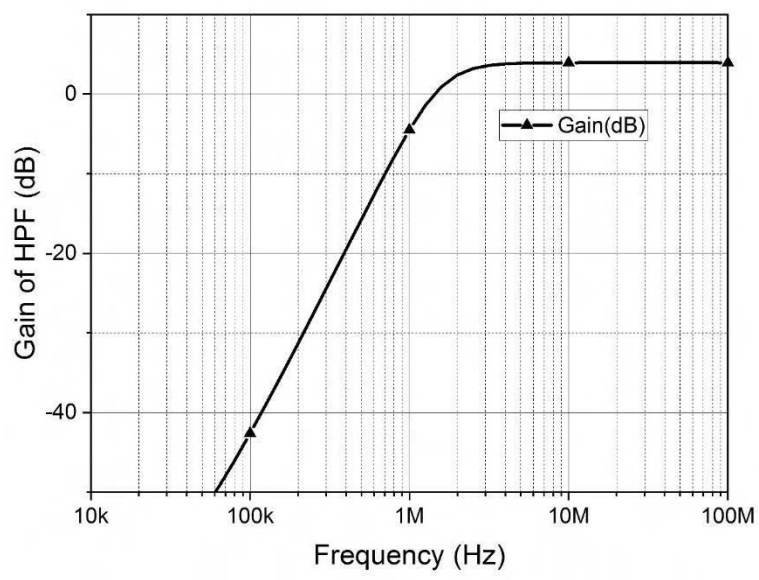
The theoretical propositions of the proposed filter topology is validated through SPICE simulation. For simulations, the VDBA shown in Figure 2.4 is used. The three filter configurations are designed for Butterworth responses for f_0 of 1.59 MHz and corresponding frequency responses are shown in Figure 4.18. The component values chosen for different responses are enlisted in Table 4.7.

Table 4.7 Component values chosen for various responses

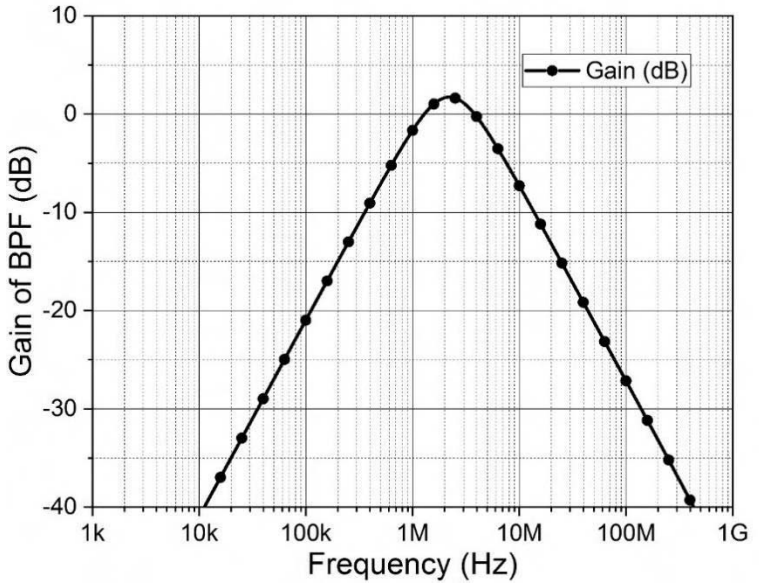
Response type	Resistance Values (kΩ)		CapacitanceValues (pF)	f_0 theoretical (MHz)	f_0 simulated (MHz)
LPF	$R_1 = R_2 = 1$	$R_5 = 1.2$	$C_3 = C_4 = 100$	1.59	1.57
HPF	$R_3 = R_4 = 1$	$R_5 = 1.2$	$C_1 = C_2 = 100$	1.59	1.62
BPF	$R_1 = R_3 = R_4 = 1$	$R_5 = 2.25$	$C_2 = C_3 = 100$	2.25	2.22



(a)



(b)



(c)

Figure 4.18 Frequency responses of proposed (a) LPF, (b) HPF and (c) BPF

Further, the electronic tunability of f_0 of BPF is depicted in Figure 4.19 (a) while Q_0 is kept fix as 0.707. The components chosen for the same are given in Table 4.8. The proposed VDBA-based SISO multifunction filter is similar to Op-Amp based Sallen-Key filter. However, the frequency response of proposed configuration is far more superior as compared to Op-Amp based SISO filter due to well-known high frequency limitations of Op-Amp.

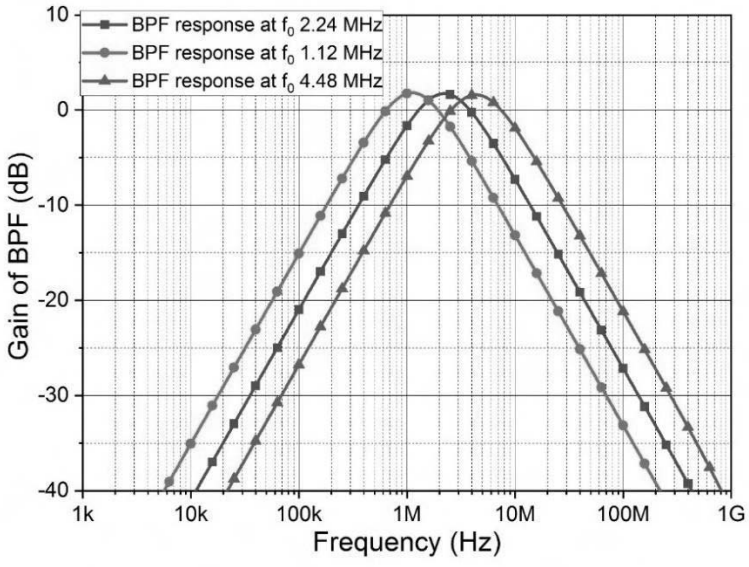
Table 4.8 Component values used for f_0 tunability

f_0 (MHz)	Components			Q_0
	$R_1=R_2=R_3$ (kΩ)	R_5 (kΩ)	$C_2= C_3$ (pF)	
1.12	2	2.25	100	0.707
2.24	1	2.25	100	0.707
4.48	0.5	2.25	100	0.707

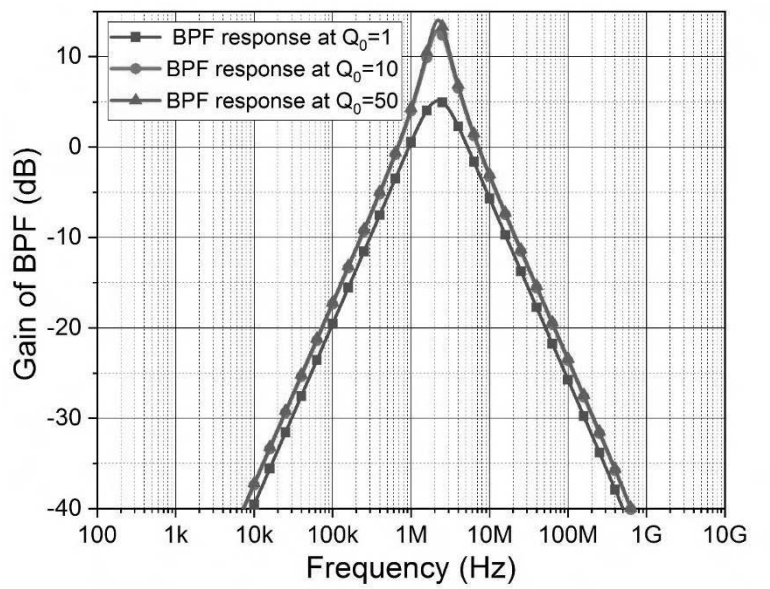
The independent tunability of Q_0 with R_5 is can be observed from Figure 4.19 (b). The center frequency f_0 is chosen to be 2.24 MHz. The component values are chosen and the Q_0 so obtained are given in Table 4.9. It may be noted from Table 4.9 that a small change in R_5 results in large variation in Q_0 value.

Table 4.9 Component values used for independent tunability of Q_0

f_0 (MHz)	Components			Q_0
	$R_1=R_2=R_3$(kΩ)	$C_2=C_3$ (pF)	R_5 (kΩ)	
2.24	1	100	2.69	1
2.24	1	100	3.64	10
2.24	1	100	3.7	50



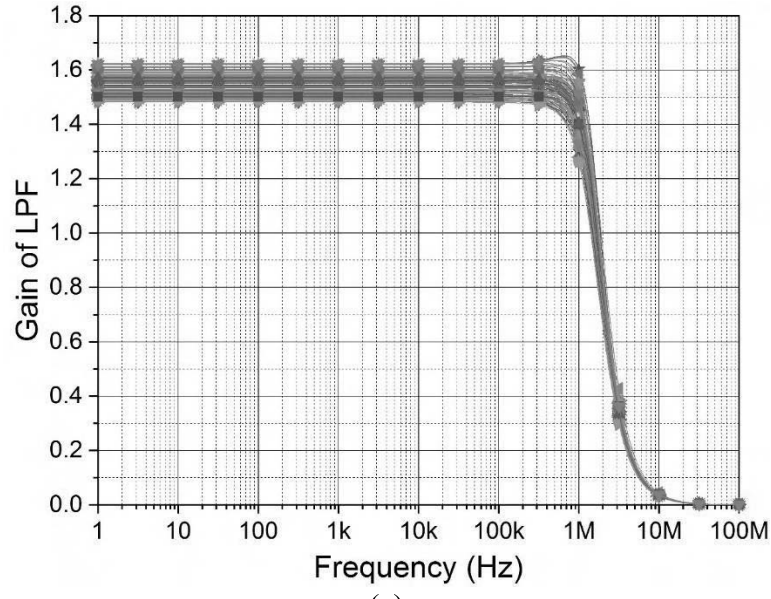
(a)



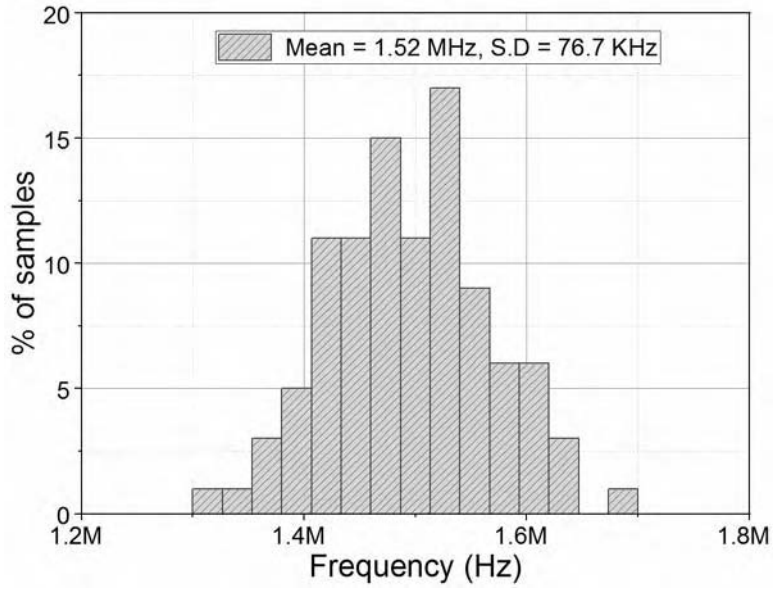
(b)

Figure 4.19 (a) BPF response for independent tunability of (a) f_0 and (b) Q_0

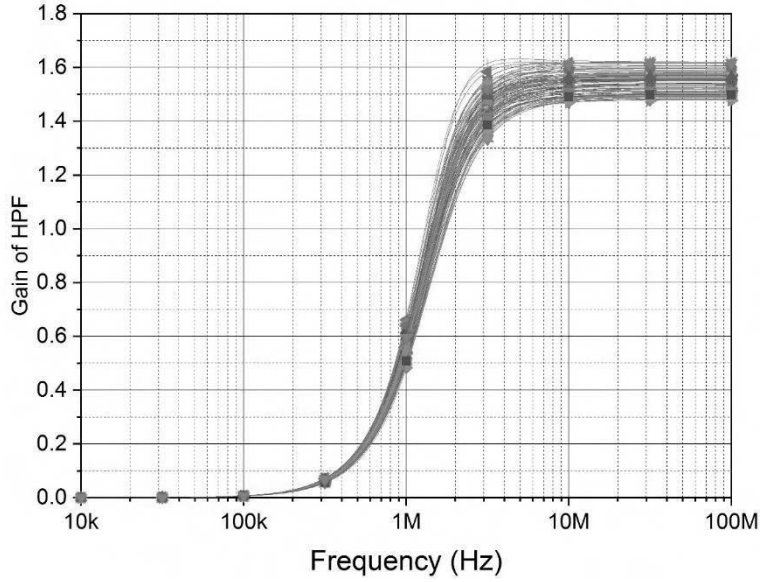
The effect of component variation on frequency response is studied through Monte Carlo simulations with 5 % tolerance band for all the resistors and capacitors. The derived Monte Carlo simulations and their respective histogram after 100 simulation runs are shown in Figure 4.20 respectively. The standard deviation (S.D) of f_0 is noted to be 37.7 kHz, 76.7 kHz and 66.4 kHz for BPF, LPF and HPF configuration respectively. Thus the proposed filter topology has low sensitivity.



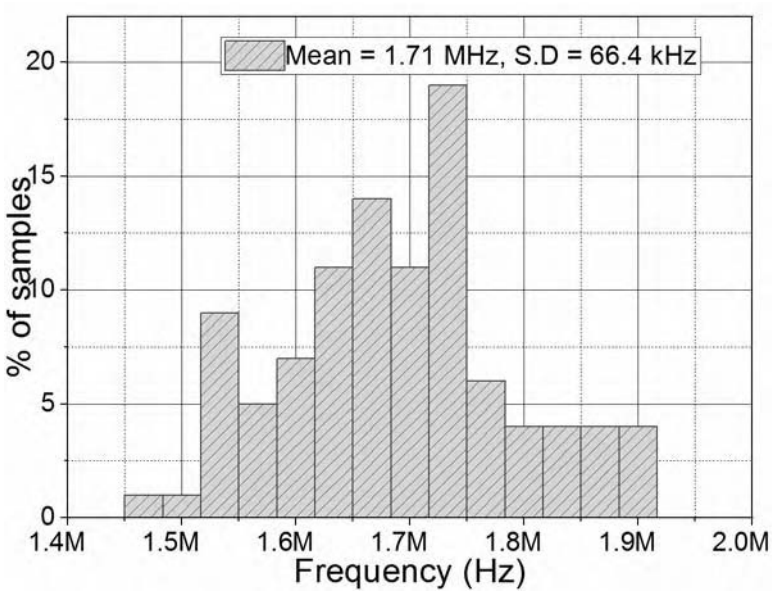
(a)


Mean = 1.52 MHz, S.D = 76.7 KHz
% of samples
Frequency (Hz)
0
5
10
15
20
1.2M
1.4M
1.6M
1.8M

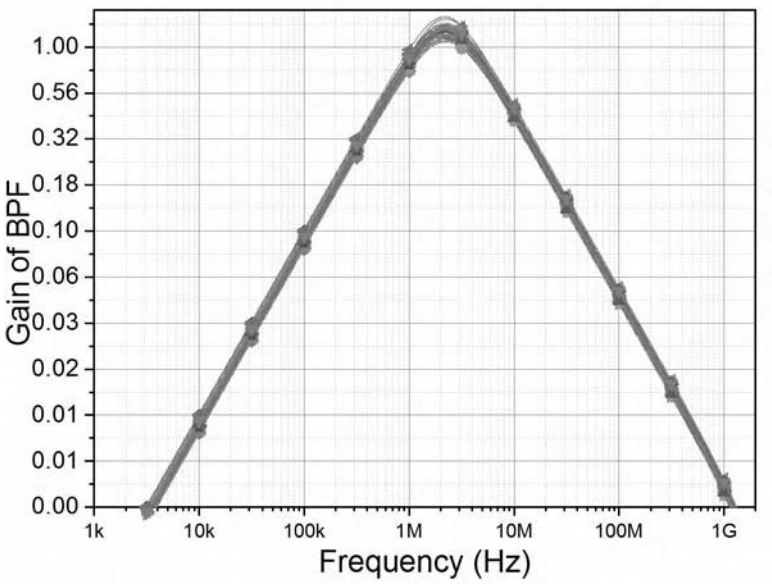
(b)


Gain of HPF
Frequency (Hz)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
10k
100k
1M
10M
100M

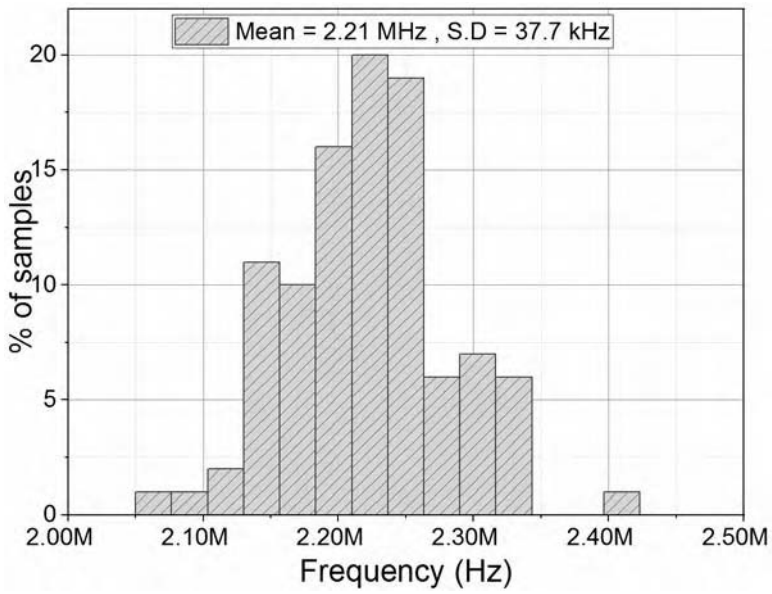
(c)


Mean = 1.71 MHz, S.D = 66.4 kHz
% of samples
0
5
10
15
20
1.4M
1.5M
1.6M
1.7M
1.8M
1.9M
2.0M
Frequency (Hz)

(d)


Gain of BPF
1.00
0.56
0.32
0.18
0.10
0.06
0.03
0.02
0.01
0.01
0.00
1k
10k
100k
1M
10M
100M
1G
Frequency (Hz)

(e)



(f)

Figure 4.20 Monte Carlo analysis, Frequency response and corresponding histogram of (a) and (b) LPF, (c) and (d) HPF, (e) and (f) BPF

4.3.3 Proposed MISO Universal Filter

The proposed MISO universal filter is depicted in Figure 4.21. It consists of two VDBAs, two capacitors and a grounded resistor. In proposed topology the capacitor nodes are lifted by applied input voltages.

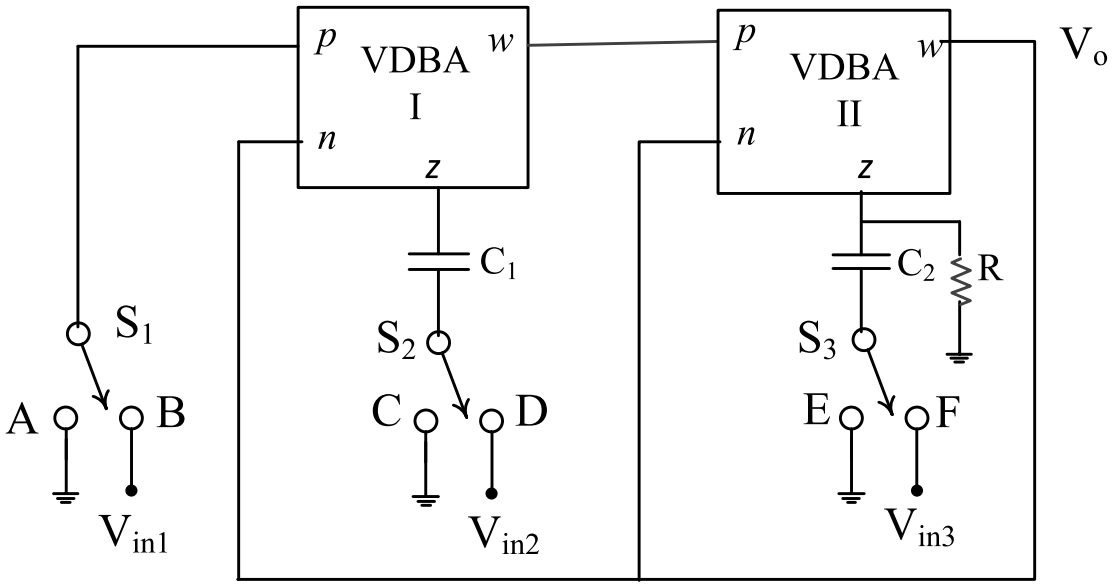


Figure 4.21 Proposed universal MISO filter

The output of the proposed MISO universal filter using routine analysis, considering S_1, S_2 and S_3 switches in B, D and F position respectively, can be expressed as

$$V_o = \frac{V_{in1} g_{m1} g_{m2} + V_{in2} sC_2 g_{m2} + V_{in3} s^2 C_1 C_2}{s^2 C_1 C_2 + sC_1 (g_{m2} + \frac{1}{R}) + g_{m1} g_{m2}} \tag{4.39}$$

It is observed from (4.39) that the proposed filter can realize all five standard responses through proper input selection via appropriate switch settings as summarized in Table 4.10.

Table 4.10 Selection of input for specific filter response

Response	V_{in1}	V_{in2}	V_{in3}	S_1	S_2	S_3	TF
LPF	V_{in}	0	0	B	C	E	$\frac{g_{m1} g_{m2}}{s^2 C_1 C_2 + sC_1 (g_{m2} + \frac{1}{R}) + g_{m1} g_{m2}}$
HPF	0	0	V_{in}	A	C	F	$\frac{s^2 C_1 C_2}{s^2 C_1 C_2 + sC_1 (g_{m2} + \frac{1}{R}) + g_{m1} g_{m2}}$
BPF	0	V_{in}	0	A	D	E	$\frac{sC_2 g_{m2}}{s^2 C_1 C_2 + sC_1 (g_{m2} + \frac{1}{R}) + g_{m1} g_{m2}}$
BSF	V_{in}	0	V_{in}	B	C	F	$\frac{g_{m1} g_{m2} + s^2 C_1 C_2}{s^2 C_1 C_2 + sC_1 (g_{m2} + \frac{1}{R}) + g_{m1} g_{m2}}$
APF	V_{in}	$-V_{in}$	V_{in}	B	D	F	$\frac{g_{m1} g_{m2} - sC_2 g_{m2} + s^2 C_1 C_2}{s^2 C_1 C_2 + sC_1 (g_{m2} + \frac{1}{R}) + g_{m1} g_{m2}}$

The ω_0 and Q_0 of the proposed VM MISO universal filter are given by (4.40) and (4.41) respectively.

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{4.40}$$

$$Q_0 = \sqrt{\frac{C_2}{C_1}\frac{g_{m1}g_{m2}}{\left(g_{m2}+\frac{1}{R}\right)^2}}$$

(4.41)

It is obvious from (4.40) and (4.41) that ω_0 and Q_0 can be tuned independently. Further, higher value of Q_0 can be achieved by varying the capacitor ratio C_2/C_1, keeping ω_0 constant. It may be observed that the ω_0 and Q_0 are electronically tunable.

4.3.3.1 Sensitivity Analysis

The sensitivities of ω_0 and Q_0 of the proposed filter with respect to passive elements and the transconductance (g_m) of VDBAs may be expressed as

$$S_{g_{m1}}^{\omega_0} = S_{g_{m2}}^{\omega_0} = 0.5$$
$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -0.5,$$
$$S_R^{\omega_0} = 0$$
$$S_{g_{m1}}^{Q_0} = S_{C_2}^{Q_0} = -S_{C_1}^{Q_0} = 0.5$$
$$, S_{g_{m2}}^{Q_0} = -S_R^{Q_0} = 0.5\frac{1/R}{g_{m2}+1/R}$$

(4.42)

Equation (4.42) shows that all sensitivities of ω_0 and Q_0 are ≤ 0.5 in magnitude. Therefore proposed VM MISO universal filter is insensitive to parameter variations.

4.3.3.2 Non-Ideal Analysis

Considering the non-idealities of VDBA, the proposed filter structure of Figure 4.20 gets modified as Figure 4.22.

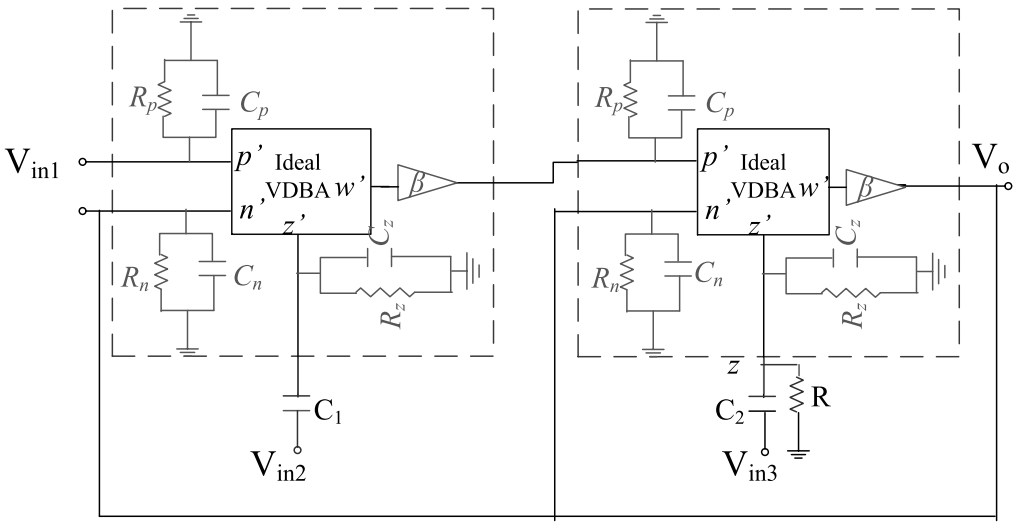


Figure 4.22 Non-ideal structure of proposed VM universal MISO filter

Routine analysis of non-ideal filter gives the output-input relation as

$$V_{o\_n}=\frac{V_{in1}\alpha_1\alpha_2\beta_1\beta_2 g_{m1}g_{m2}+V_{in2}\alpha_2\beta_1\beta_2 sC_2 g_{m2}+V_{in3}\beta_2(s^2C_{eq1}C_2+\frac{sC_2}{R_{z1}})}{s^2C_{eq1}C_{eq2}+s(C_{eq1}\alpha_2\beta_2 g_{m2}+\frac{C_{eq1}}{R_{eq2}}+\frac{C_{eq2}}{R_{z1}})+\alpha_1\alpha_2\beta_1\beta_2 g_{m1}g_{m2}+\frac{1}{R_{eq2}R_{z1}}+\frac{\alpha_2\beta_2 g_{m2}}{R_{z1}}} \tag{4.43}$$

The pole frequency (ω_{0_n}) and quality factor (Q_{0_n}) of the proposed VM MISO universal filter under non-ideal conditions are given by

$$\omega_{0\_n}=\sqrt{\frac{\alpha_1\alpha_2\beta_1\beta_2 g_{m1}g_{m2}+\frac{1}{R_{eq2}R_{z1}}+\frac{\alpha_2\beta_2 g_{m2}}{R_{z1}}}{C_{eq1}C_{eq2}}} \tag{4.44}$$

$$Q_{0\_n}=\sqrt{\frac{C_{eq2}C_{eq1}R_{eq2}R_{z1}(\alpha_1\alpha_2\beta_1\beta_2 g_{m1}g_{m2}R_{eq2}R_{z1}+1+\alpha_2\beta_2 R_{eq2}g_{m2})}{(\alpha_2\beta_2 g_{m2}C_{eq1}R_{eq2}R_{z1}+C_{eq2}R_{z1}+C_{eq2}R_{eq2})^2}} \tag{4.45}$$

Where $C_{eq1}= C_1+C_{z1}$, $C_{eq2}= C_2+C_{z2}$. R_{eq2} is R // R_{z2}. By selecting $C_1 >> C_{z1}$; $C_2 >> C_{z2}$ and $R << R_{z2}$, (4.44) and (4.45) will be equal to (4.40) and (4.41) respectively.

4.3.3.3 Simulations Results

The proposed filter circuit is characterized through simulations using VDBA proposed in chapter 3. The bias currents I_{B1} and I_{B2} are set to 15 µA resulting in g_m = 561.8 µS while I_{B3} and I_{B4} are taken as 5 µA.

The proposed VM MISO universal filter is designed for f_0 = 8.9 MHz and Q_0 = 0.707. The capacitor values are selected as $C_1 = C_2$ = 10 pF and the corresponding value of R is computed as 4.3 kΩ. The ideal and simulated frequency responses of the proposed MISO universal topology are depicted in Figure 4.23. The simulated value of f_0 is 8.8 MHz which is approximate to the theoretical value. Figures 4.24 (a) and (b) show the gain and phase response of APF and BSF respectively.

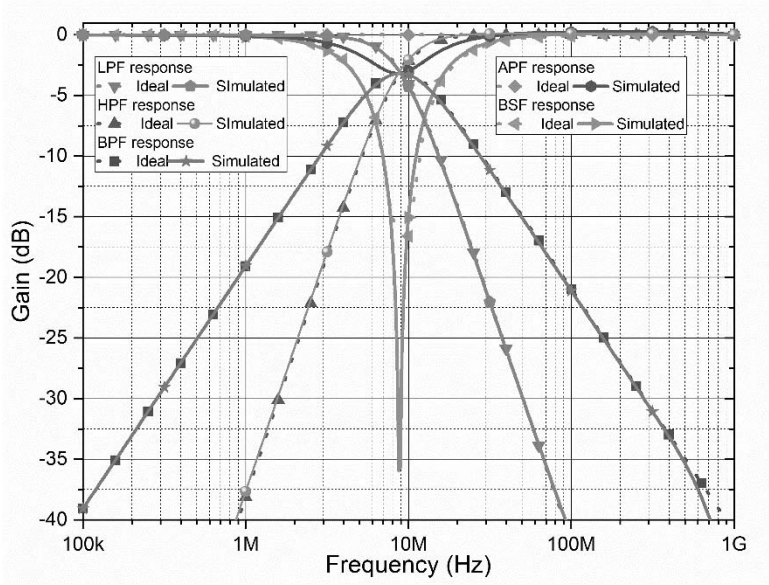
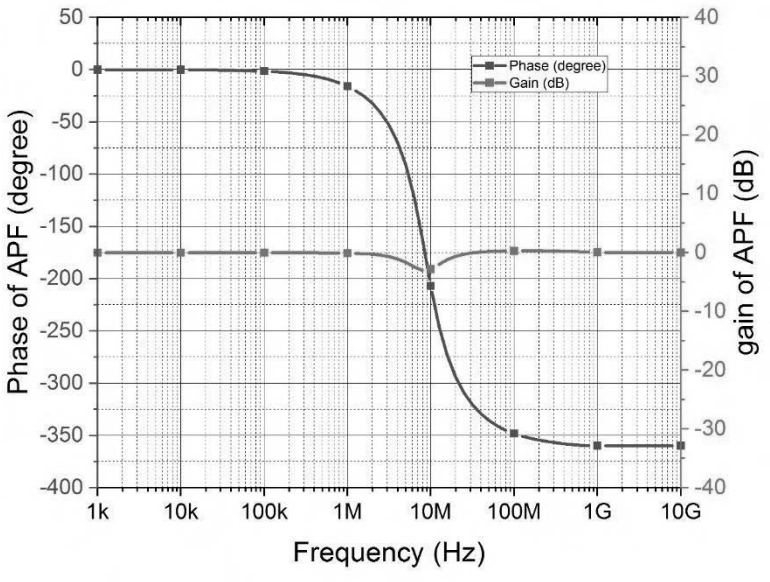
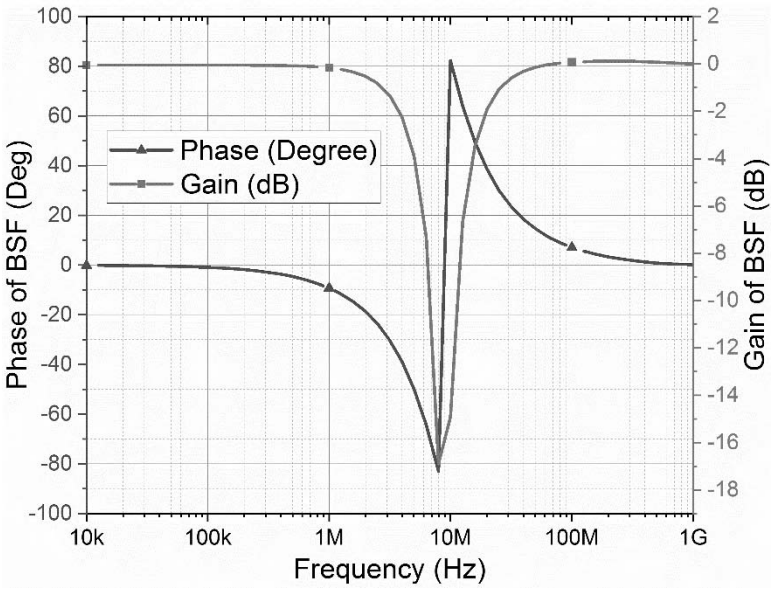


Figure 4.23 Frequency response of VM MISO universal filter



(a)



(b)

Figure 4.24 Gain and phase responses of the (a) APF and (b) BSF

The electronic tunability of f_0 of BPF through I_B variation is depicted in Figure 4.25 (a) while Q_0 is set as 0.707. Higher values of Q_0 can be achieved by varying the ratio of C_2/C_1 as shown in Figure 4.25 (b). It may also be observed that the higher value of Q_0 is attainable without affecting the f_0. The values of Q_0 for different values of C_1 and C_2 have been summarized in Table 4.11. The ideal and simulated results of f_0 at different

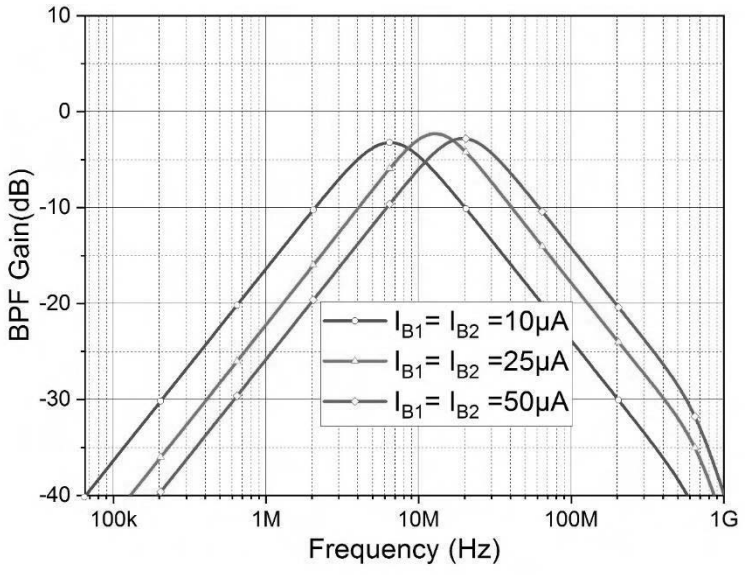
bias currents have been summarized in Table 4.12 and are plotted in Figure 4.26 (c). It is observed from Table 4.12 that the % error remains well within 3%.

Table 4.11 Component values for independent Q_0 tunability

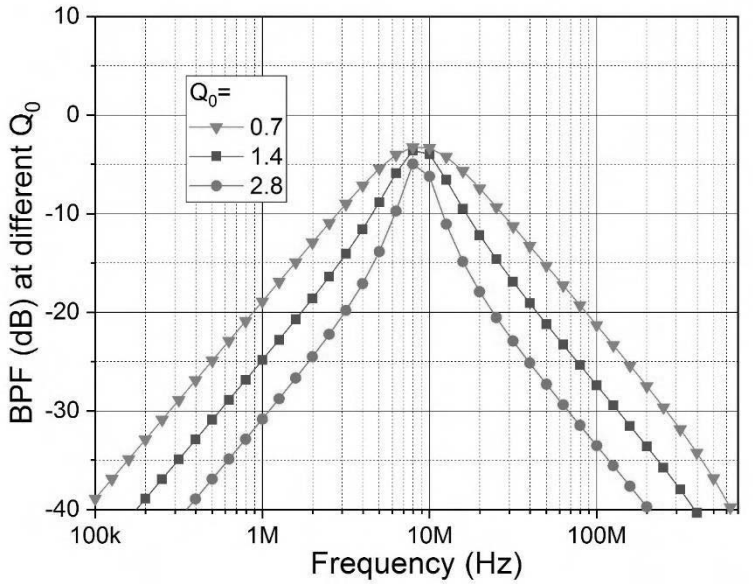
Sr. No	g_m (µS)	R (kΩ)	C_1 (pF)	C_2 (pF)	f_0 (MHz)		Q_0
					Theoretical	Simulated	
1	561.8	4.3	10	10	8.9	8.8	0.7
2	561.8	4.3	5	20	8.9	8.78	1.4
3	561.8	4.3	2.5	40	8.9	8.7	2.8

Table 4.12 The bias current and g_m values for f_0 tunability

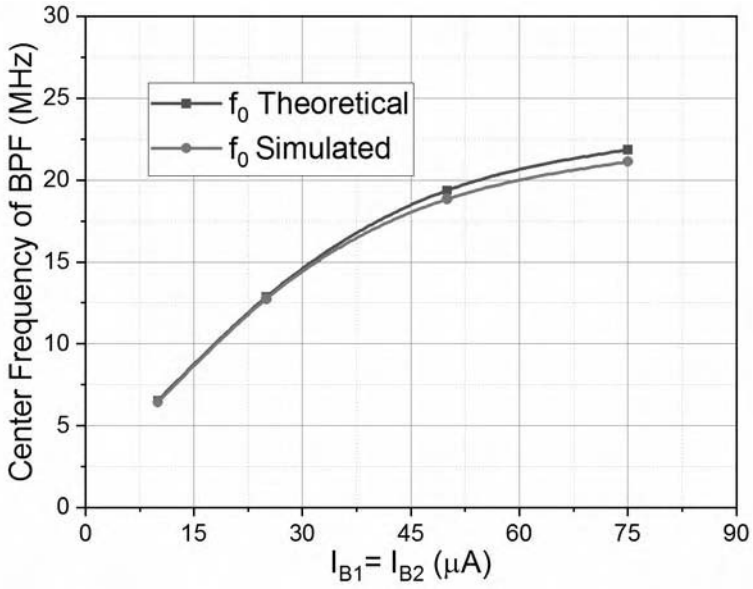
Sr. No	I_{B1}= I_{B2} (µA)	g_m (µS)	f_0 (Theoretical) (MHz)	f_0 (Simulated) (MHz)	% error
1	10	411.8	6.54	6.45	1.39
2	25	913.18	12.87	12.75	0.93
3	50	1218.6	19.37	18.84	2.7



(a)



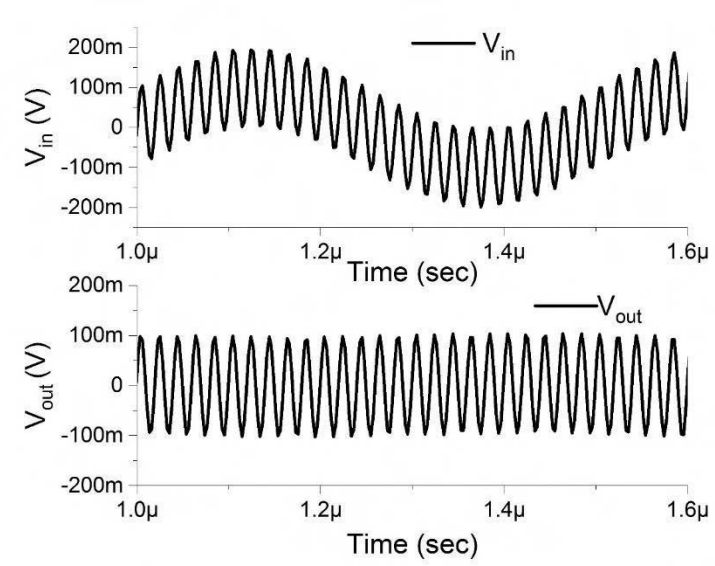
(b)



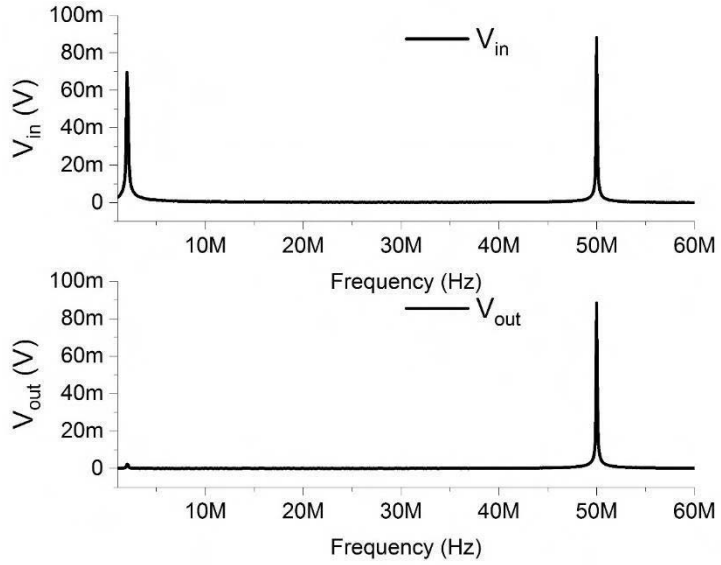
(c)

Figure 4.25 (a) BPF response depicting electronic tunability of f_0, (b) The Q_0 variation with capacitor ratio (C_2/C_1) and (c) The f_0 variation with I_B

To carry out the transient analysis of the proposed HPF a multitone signal having frequencies 2 MHz and 50 MHz is applied. The input and output signals in the time domain and their spectrums are shown in Figures 4.26 (a) and (b) respectively. For the sake of brevity transient analysis only for proposed HPF is shown, though appropriate results are obtained for other structures as well.



(a)

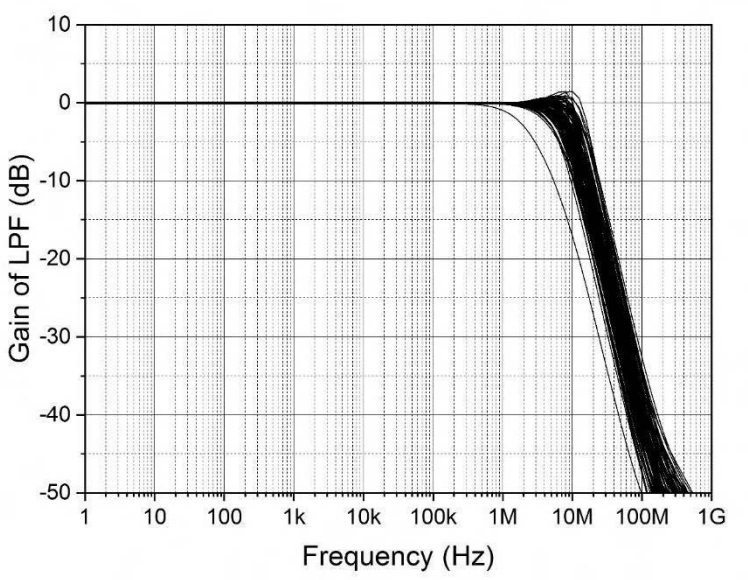


(b)

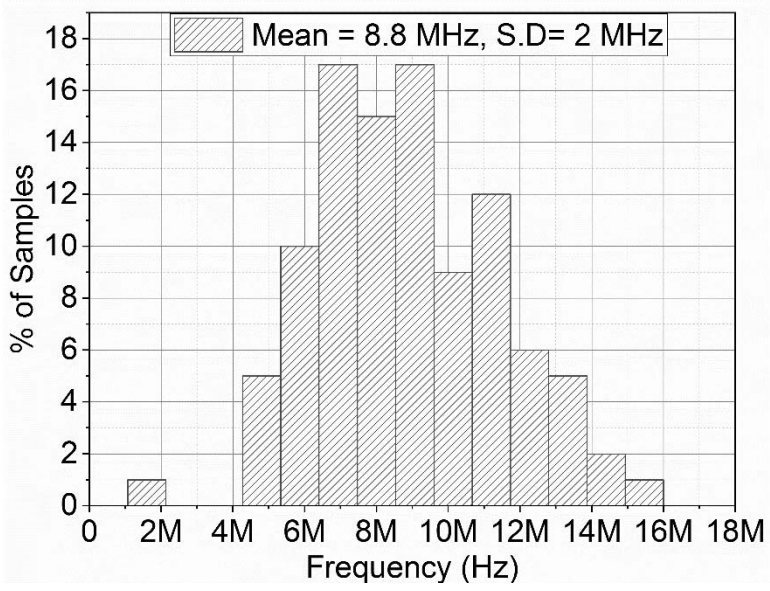
Figure 4.26 (a) Transient input and output of HPF and (b) spectrum of input and output of HPF

The Monte Carlo analysis is carried out for all passive elements with 5% tolerance limit. It is observed that proposed universal MISO filter topology has reasonable sensitivity characteristics. For the sake of brevity, the frequency response and the derived histogram after 100 simulation runs for LPF are shown in Figure 4.27 (a) and (b)

respectively. The simulated mean of f_0 is observed to be 8.8 MHz with a standard deviation of 2 MHz.



(a)



(b)

Figure 4.27 Monte Carlo (a) Frequency response of LPF and (b) Histogram

4.3.3.4 Post Layout Simulation Results

The layout of proposed filter is drawn for a filter having design specifications as f_0 = 17.8 MHz and Q_0 = 0.707, which is shown in Figure 4.28. The responses obtained

through pre and post layout simulations for the designed universal topology are shown in Figure 4.29 (a) and (b) respectively. The simulated f_0 value is 17.5 MHz as against the pre layout simulated value of 17.6 MHz. Thus there exists a close agreement between the pre and post simulation values.

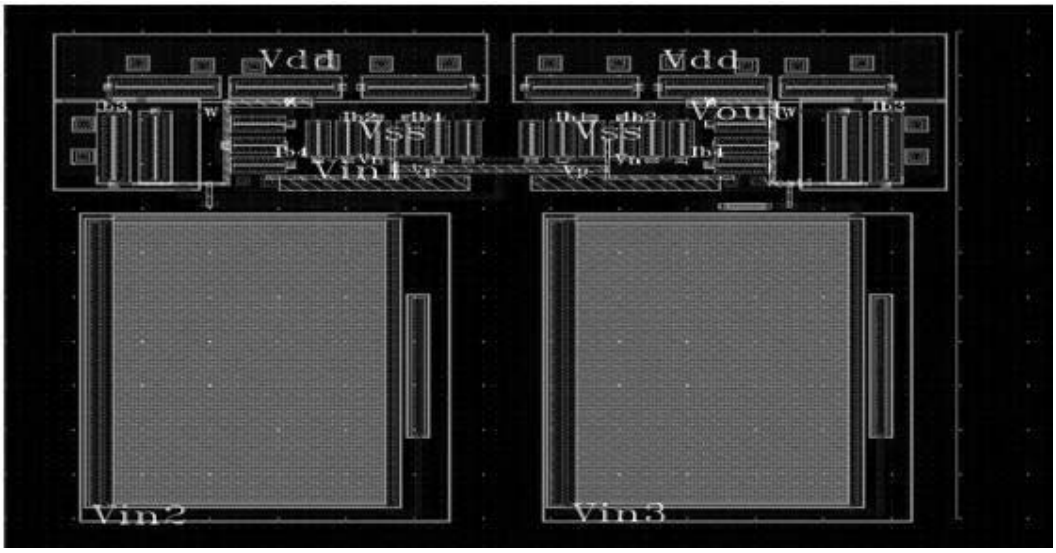
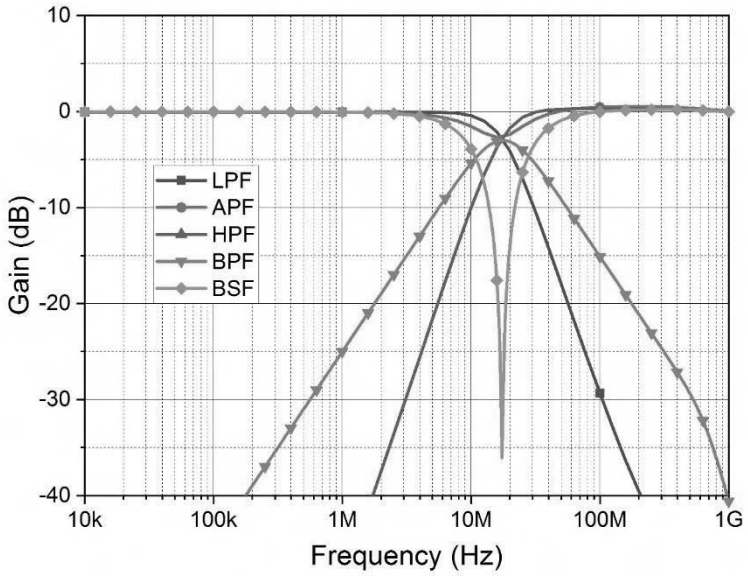
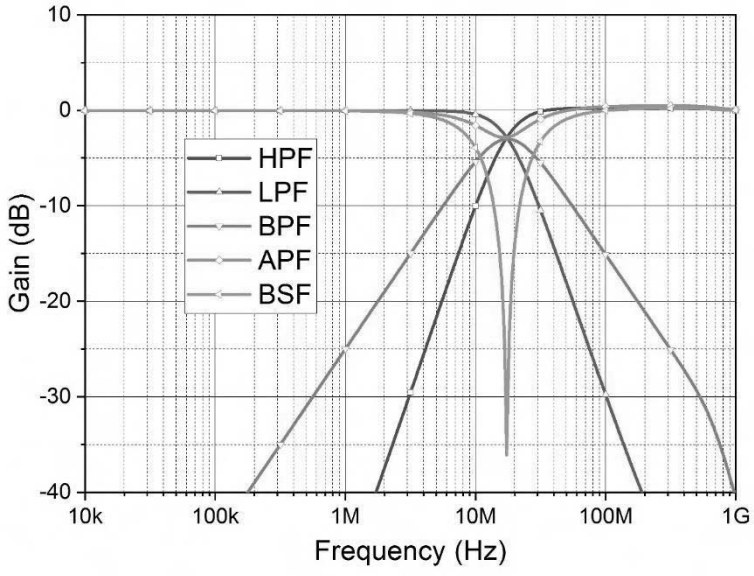


Figure 4.28 Layout of the proposed MISO universal filter



(a)



(b)

Figure 4.29 (a) Pre layout and (b) Post layout, frequency response of proposed MISO universal filter

4.4 Conclusion

In this chapter linear applications of VDBA are presented. An instrumentation amplifier is presented first which is followed by designs of electronic filters. The proposed IA consists of a single VDBA and a single grounded resistor. A detailed theoretical analysis followed by noise analysis is carried out. The gain of the proposed amplifier can be electronically tuned through transconductance. The performance of the circuit is confirmed through SPICE simulations. The proposed IA possesses high CMRR and wide bandwidth with quite low value of THD.

Three filter configurations are proposed next. A first order APF using single VDBA which can be configured in inverting/non-inverting configuration has been proposed first. The proposed APF provides voltage output at low impedance with electronically tunable voltage gain. A VM multifunction generalized filter topology using single VDBA is the next proposition. The topology can synthesize LPF, HPF and BPF by selecting proper admittance. The topology is apt for high Q_0 implementation. The

passive sensitivities are found to be low. The third filter topology is a MISO universal biquad filter designed using two VDBAs, two capacitors and a grounded resistor. The pole frequency of the proposed structure can be controlled independently of quality factor. The functional verification of the first two structures is done through SPICE simulations and the MISO topology is demonstrated obtained using Cadence Virtuoso ADE tool with 0.18 μm GPDK parameters through pre and post layout simulation results. The theoretical and the simulated results of all the application proposed in this chapter are observed to be in close agreement.

CHAPTER 5

5.1 Introduction

Analog signal processing applications can be categorized in two classes (i) linear and (ii) non-linear circuits. In linear the output varies linearly with the input whereas in non-linear circuits the output possesses a non-linear relation with the input signal. Rectifier, clipper, clamper, sample and hold circuit, multipliers etc. are some of the examples of non-linear circuits. Non-linear operations on analog signals are required in communication, instrumentation and measurement, and control system design. Literature survey reveals that non-linear signal processing through VDBA has not been explored. Therefore this chapter is devoted to non-linear applications of VDBA. In this chapter three non-linear applications using VDBA have been developed. A four quadrant analog multiplier (FQAM) using the quarter square algebraic identity is proposed first. A squaring circuit is presented next which is followed by a third application namely a square rooting circuit.

5.2 Analog Multiplier

Analog multipliers are used extensively for non-linear applications such as a modulator, equalizer, frequency doublers, and neural computing [126]. Analog multipliers can be classified as (i) one, (ii) two and (iii) four quadrant multipliers. If both the inputs are positive, it is said to be one quadrant. In two quadrant multiplier, one input is held positive and the other may take both positive and negative values. In four quadrant multipliers, both inputs can take either positive or negative values. In two and four quadrant multipliers, the output preserves the polarity relationship. A variety of analog multipliers are available in the literature [127]–[138] using different ABBs and are summarized in Table 5.1.

Table 5.1 Comparison of previously reported analog multipliers

Reference No.	ABB	Number of ABBs	Number of extra transistors	Passive resistors	Four quadrant	Input range	output range	Supply voltage(V)	Type of Input signal	Type of Output signal	Power dissipation (mW)	3 dB Frequency(MHz)
[127]	CCCII+	2	0	0	No	--	--	±5	Current	Current	--	20
[128]	OTA	3	0	0	Yes	±0.8mA	±.8mA	±10	Current	Current	--	155
[129]	Op Amp	5	0	8	Yes	2.62V	±200mV	±2.4	Voltage	Voltage	--	0.840
[130]	CCCII	1	0	1	No	--	--	±2.5	Current	Current	3.82	-
		1	0	1	Yes	--	--	±2.5	Current	Current	3.82	--
[131]	CDBA	1	6	0	Yes	±250mV	±180mV	±5	Voltage	Voltage	--	82.3
[132]	CDBA	1	4	0	Yes	±1V	±0.6V	±5	Voltage	Voltage	--	10
[133]	CDTA	2	0	0	Yes	--	--	±5	Current	Current	--	30
[134]	OTA	4	16	0	Yes	±100mV	±15mV	±1	Voltage	Voltage	0.588	3960
[135]	OTA	3	0	0	Yes	±1Ma	±1mA	±10	Current	Current	--	162
[136]	CTTA	1	0	0	Yes	±150µA	±40uA	±1.5	Current	Current	1.83	53.1
[137]	OTRA	1	4	0	Yes	±300mV	±100mV	±1.5	Voltage	Voltage	0.830	8
[138]	OTRA	1	6	0	Yes	±200mV	±350mV	±1.5	Voltage	Voltage	--	25
Proposed	DO-VDBA	2	10	0	Yes	±50mV	±15mV	±1	Voltage	Voltage	0.627	220

It is observed from Table 5.1 that

- The multipliers presented in [129], [131], [132], [134], [137], [138] are VM whereas structures presented in [127], [128], [130], [133], [135], [136] are CM multipliers.
- Structures of [127]–[129], [133], [134] use a large number of ABBs.
- Multipliers of [129], [130] use passive components which is not suitable for integrated circuits.
- Voltage output is available at a high impedance in [134] .
- Large power supply voltages are required in [127]–[133], [136].

- The work presented in [127] and one of the structures in [130] are two quadrant multiplier.

Therefore in this chapter, an FQAM is designed to have a voltage output at a low impedance node.

5.2.1 Proposed FQAM

The proposed FQAM is realized using the generalized quarter square algebraic identity which is expressed as (5.1) and its block diagrammatic representation is shown in Figure 5.1.

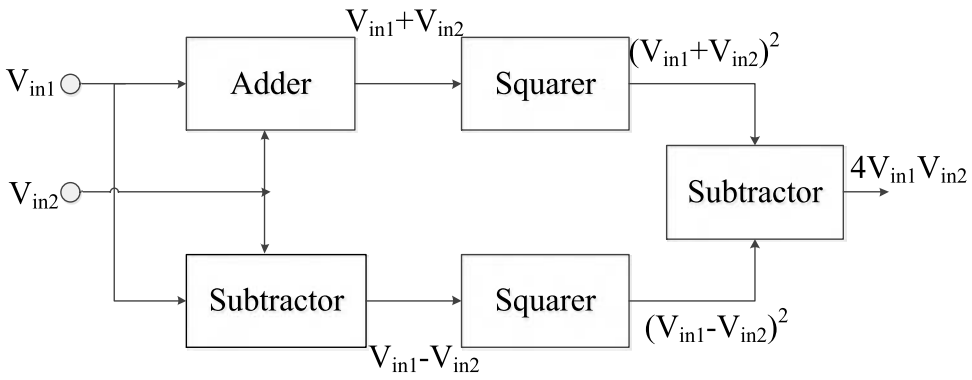


Figure 5.1 Block diagram of quarter square algebraic identity

$$(V_{in1}+V_{in2})^2-(V_{in1}-V_{in2})^2=4V_{in1}V_{in2} \tag{5.1}$$

It may be observed from (5.1) that FQAM based on quarter square algebraic identity can be designed with the help of adder, subtractor and squarer circuits arranged as depicted in Figure 5.1. The proposed DO-VDBA based FQAM is shown in Figure 5.2. The circuit comprising of DO-VDBA I and resistance R_1 represents an adder whereas DO-VDBA II along with resistance R_2 performs the subtraction operation.

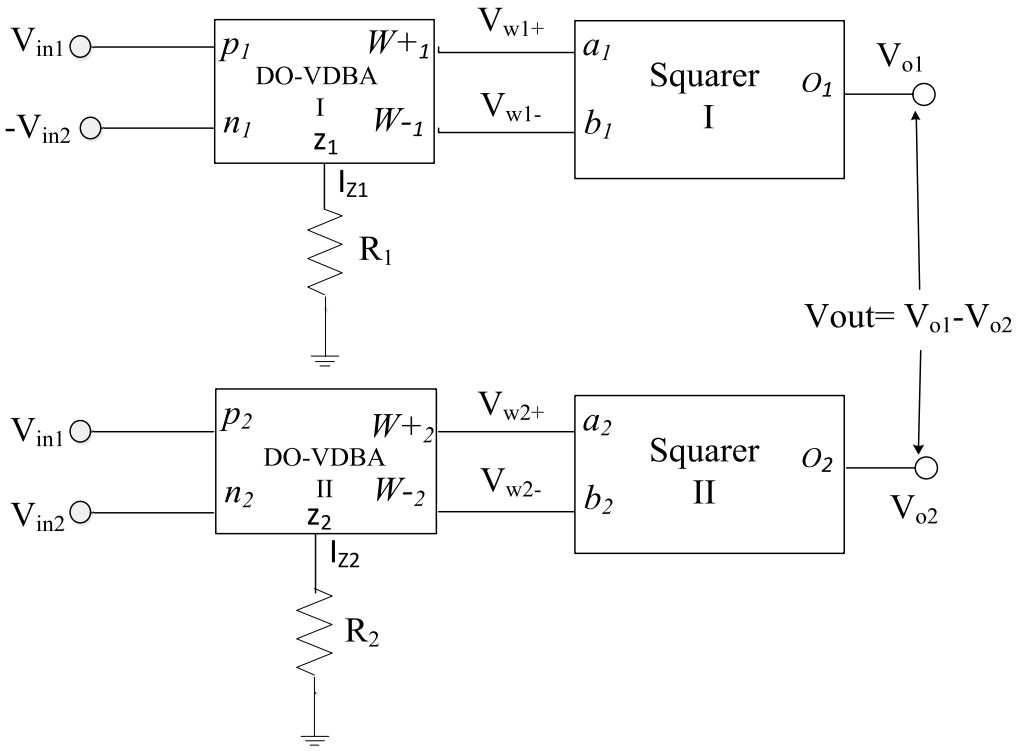


Figure 5.2 Proposed VDBA based FQAM

The voltage outputs of DO-VDBA I and DO-VDBA II, considering $R_2 = R_1 = R$, are expressed as (5.2) and (5.3) respectively.

$$V_{w1+} = -V_{w1-} = g_{mv}R(V_{in1} + V_{in2}) \tag{5.2}$$

$$V_{w2+} = -V_{w2-} = g_{mv}R(V_{in1} - V_{in2}) \tag{5.3}$$

where the transconductances of both the DO-VDBAs are considered to be equal and are represented by g_{mv}.

It may be seen from (5.2) that V_{w1+} is proportional to the sum of the input voltages whereas V_{w1-} is an inversion of V_{w1+}. Equation (5.3) shows that buffered outputs of DO-VDBA II are proportional to the difference of input voltages with opposite polarities.

The squarer block [128] used in the proposed FQAM is shown in Figure 5.3 which consists of three transistors namely M_{s1}, M_{s2} and M_{s3}. The *a* and *b* represent its two input terminals and *o* is the output terminal. In the analysis of squarer, it is assumed that M_{s1} and M_{s2} are perfectly matched and the aspect ratio of M_{s3} is considered to be twice as that of M_{s1} and M_{s2}. Further, all the three transistors are biased in the saturation region.

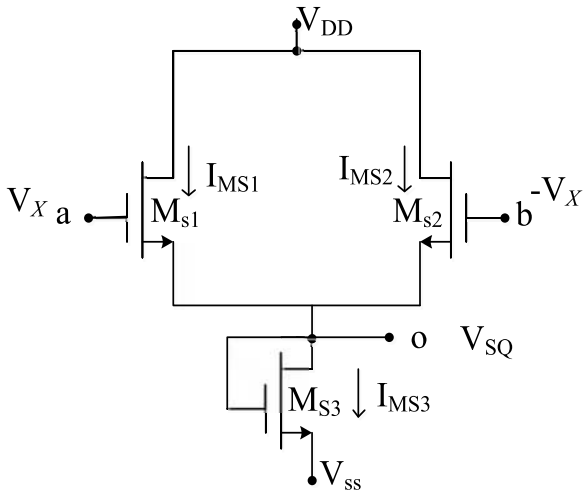


Figure 5.3 Squarer circuit [128]

From Figure 5.3, current through transistor M_{S3} can be written as

$$I_{MS3} = I_{MS1} + I_{MS2} \tag{5.4}$$

The drain current for the NMOS transistor in saturation is given as

$$I_d = \frac{K}{2}(V_{gs} - V_{TH})^2 \tag{5.5}$$

Where $K=\mu_{on}C_{ox}(W/L)$ represents process transconductance parameter. For chosen device dimensions the process transconductance parameter of transistors as related as

$K_{MS1}=K_{MS2}=K=0.5K_{MS3}$

(5.6)

Assuming that an input V_x is applied at terminal *a* and - V_x at terminal *b* then (5.4) can be written as

$$K(V_{SQ}-V_{SS}-V_{TH3})^2=\frac{K}{2}[(+V_x-V_{SQ}-V_{TH1})^2+(-V_x-V_{SQ}-V_{TH1})^2]$$

(5.7)

where V_{SQ} represents the voltage of node *o* and is output of the squarer circuit.

Thus the V_{SQ} may be derived as

$$V_{SQ}=-\frac{V_x^{\,2}}{2(V_{SS}+2V_{TH})}+\frac{V_{SS}}{2}$$

(5.8)

where V_{TH1}, V_{TH2} and V_{TH3} are considered to be equal and denoted by V_{TH}.

Using (5.5) and (5.6) current through transistor M_{S3} can be written as

$$I_{MS3}=K(V_{SQ}-V_{SS}-V_{TH})^2$$

(5.9)

Now putting the value of V_{SQ} from (5.8) in (5.9),

$$I_{MS3}=\frac{K(V_x^4+2V_x^2(V_{ss}+2V_{TH})^2+(V_{ss}+2V_{TH}))}{4(V_{ss}+2V_{TH})^2}$$

(5.10)

For small signals, $V_x^4\approx 0$, therefore

$$I_{MS3} = \frac{K}{2} V_x^{\,2} + \frac{K}{4}(V_{SS} + 2V_{TH})^2$$

(5.11)

Further using transistor relation, I_{MS3} is computed as

$$I_{MS3} = g_{ms3} V_{SQ}$$

(5.12)

where g_{ms3} represents the transconductance of transistor M_{S3}.

$$V_{SQ} = \frac{I_{MS3}}{g_{ms3}}$$

(5.13)

Substituting I_{MS3} from (5.11), the V_{SQ} is computed as

$$V_{SQ} = \frac{K}{2g_{ms3}} V_x^2 + \frac{K}{4g_{ms3}}(V_{ss} + 2V_{TH})^2$$

(5.14)

Equation (5.14) suggests that the V_{SQ} is proportional to the square of the input voltage (V_x).

Thus the output of squarer I of Figure 5.2 can be expressed as

$$V_{o1} = \frac{K}{2g_{ms3}}(V_{in1} + V_{in2})^2 + \frac{K}{4g_{ms3}}(V_{ss} + 2V_{TH})^2$$

(5.15)

And the output of squarer II is given by

$$V_{o2} = \frac{K}{2g_{ms3}}(V_{in1} - V_{in2})^2 + \frac{K}{4g_{ms3}}(V_{ss} + 2V_{TH})^2$$

(5.16)

The output voltage V_{out} can be determined as

$$V_{out} = V_{o1} - V_{o2} \tag{5.17}$$

Substituting the values of V_{o1} and V_{o2} from (5.15) and (5.16), the V_{out} may be obtained as

$$V_{out} = \frac{K}{2g_{ms3}} g_{mv}^2 R_1^2 ((V_{in1} + V_{in2})^2 - (V_{in1} - V_{in2})^2) = CV_{in1}V_{in2} \tag{5.18}$$

In (5.18), *C* represents the constant of proportionality and can be expressed as

$$C = \frac{2K}{g_{ms3}} g_{mv}^2 R_1^2 \tag{5.19}$$

Thus, it may be concluded from (5.18), the V_{out} is proportional to the multiplication of the two input signals.

From the integration view point, it is always preferred to implement a passive resistor using MOSFETs. The resistance R_1 and R_2 in Figure 5.2 can be realized using MOSFETs as shown in Figure 2.14. The required value of $R_1 = R_2 = R$ can be obtained using (2.17).

Substituting the value of R from (2.17), the V_{out} may be expressed as

$$V_{out} = \frac{2K}{g_{ms3}} \left(\frac{g_{mv}}{2K_R (V_{DD} - V_{TH})} \right)^2 \left((V_{in1} + V_{in2})^2 - (V_{in1} - V_{in2})^2 \right) = CV_{in1}V_{in2} \tag{5.20}$$

And the C of (5.19) can thus be expressed as

$$C = \frac{2K}{g_{ms3}}\left(\frac{g_{mv}}{2K_R(V_{DD}-V_{TH})}\right)^2 \tag{5.21}$$

5.2.1.1 Non-Ideal Analysis

In the analysis so far, the DO-VDBA characteristics are considered to be ideal. However, in CMOS implementation of DO-VDBA, transconductance and voltage tracking errors may exist due to device mismatch which may lead to deviation from the ideal behavior. Therefore the effects of non-ideal behavior of DO-VDBA need to be considered on performance of the proposed FQAM configuration. Including the non-idealities of DO-VDBA, discussed in section 2.3, the outputs of DO-VDBA I and DO-VDBA II of Figure 5.2 get modified and are represented respectively as (5.22)-(5.25).

$$V_{w1+\_n} = \frac{\beta_p g_{mv}(\alpha_p V_{in1} + \alpha_n V_{in2})}{2K_R(V_{DD}-V_{TH})} \tag{5.22}$$

$$V_{w1-\_n} = -\frac{\beta_n g_{mv}(\alpha_p V_{in1} + \alpha_n V_{in2})}{2K_R(V_{DD}-V_{TH})} \tag{5.23}$$

$$V_{w2+\_n} = \frac{\beta_p g_{mv}(\alpha_p V_{in1} - \alpha_n V_{in2})}{2K_R(V_{DD}-V_{TH})} \tag{5.24}$$

$$V_{w2-\_n} = -\frac{\beta_n g_{mv}(\alpha_p V_{in1} - \alpha_n V_{in2})}{2K_R(V_{DD}-V_{TH})} \tag{5.25}$$

Considering $\beta_{n=}\ \beta_p = \beta$,

$$V_{w1+\_n} = \frac{\beta g_{mv}(\alpha_p V_{in1} + \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} = -V_{w1-\_n}$$

(5.26)

$$V_{w2+\_n} = \frac{\beta g_{mv}(\alpha_p V_{in1} - \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} = -V_{w2-\_n}$$

(5.27)

Using (5.20), (5.26) and (5.27), the output voltage of the FQAM in presence of non-idealities of DO-VDBA can be written as

$$V_{out\_n} = \left(\frac{K}{2g_{ms3}} \left(\frac{\beta g_{mv}}{2K_R(V_{DD} - V_{TH})} \right)^2 \right) \left((\alpha_p V_{in1} + \alpha_n V_{in2})^2 - (\alpha_p V_{in1} - \alpha_n V_{in2})^2 \right)$$

(5.28)

$$V_{out\_n} = \frac{K}{2g_{ms3}} \left(\frac{\beta g_{mv}}{2K_R(V_{DD} - V_{TH})} \right)^2 \left(4\alpha_p \alpha_n V_{in1} V_{in2} \right)$$

(5.29)

For $\alpha_p = \alpha_n = \alpha$, the resultant output voltage may be expressed as

$$V_{out\_n} = (\alpha\beta)^2 C V_{in1} V_{in2}$$

(5.30)

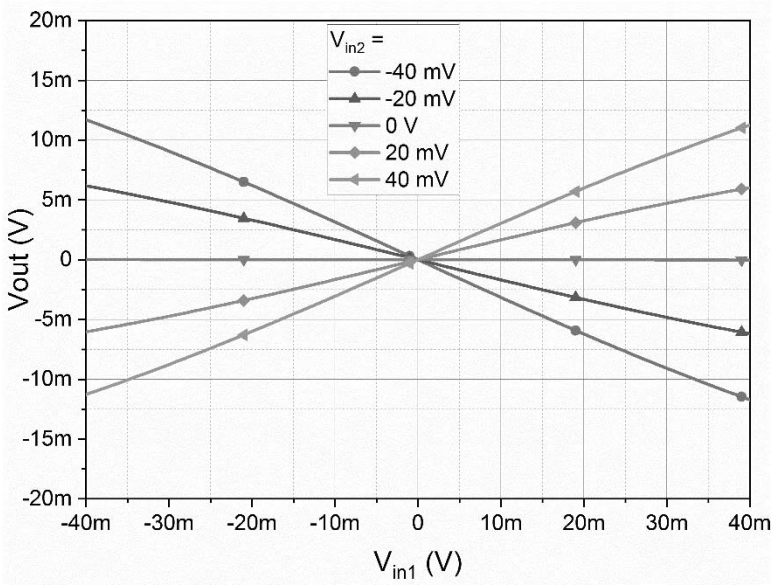
However, the deviation caused in the output due to tracking errors may be ignored as the values of α and β approaches to unity.

5.2.1.2 Simulation Results

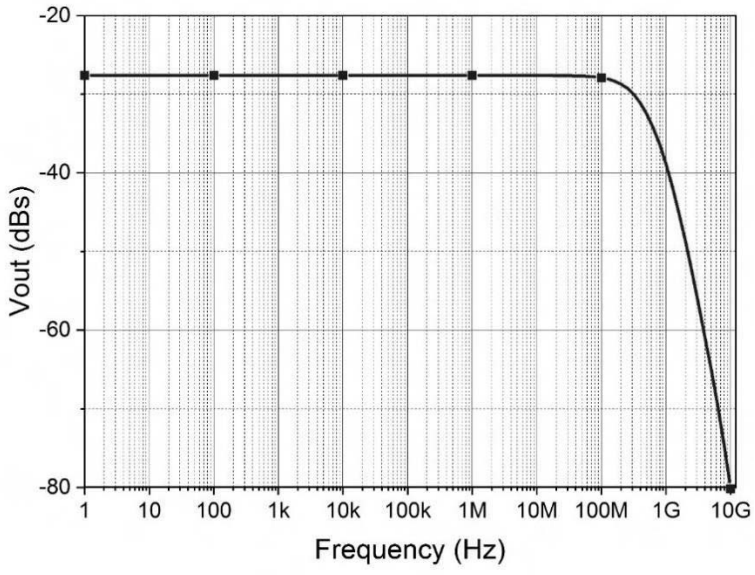
The working of the proposed FQAM circuit is confirmed through SPICE simulations. The DO-VDBA shown in Figure 2.8 is used for simulations. The aspect ratios for

DO-VDBA transistor are set to 0.36 (µm)/0.18 (µm) for M_1 to M_4 and 21.6 (µm)/0.72 (µm) for M_5 to M_8 respectively, whereas the W/L for the squarer are kept as 5.4 (µm)/0.27 (µm) for M_{S1}, M_{S2} and 10.8(µm)/0.27(µm) for M_{S3}. The supply voltages used are ±1 V. The value of the I_{bias} is set to 40 µA.

The DC characteristics of the proposed FQAM is depicted in Figure 5.4 (a) with the variation of V_{in1} from -40 mV to 40 mV. Figure 5.4 (a) verifies that the proposed circuit is an FQAM. The simulated frequency response for output voltage is presented in Figure 5.4 (b). The BW of the proposed FQAM circuit is found to be 220 MHz. The simulated power consumption of proposed FQAM is obtained as 0.627 mW.



(a)



(b)

Figure 5.4 (a) DC characteristics and (b) AC characteristics

The THD is a measure to estimate the degree to which a system is non-linear. Therefore the THD for proposed FQAM is also observed as a function of input signal amplitude. For this, V_{in2} is supplied with a constant dc voltage of 50 mV while a sinusoidal signal is applied at V_{in1}. The THD is measured for different input amplitude values and is plotted in Figure 5.5 for sinusoidal signals of three different frequencies namely 100 kHz, 10 MHz and 150 MHz respectively. It is found that THD remains < 3 % for the proposed FQAM for all three cases.

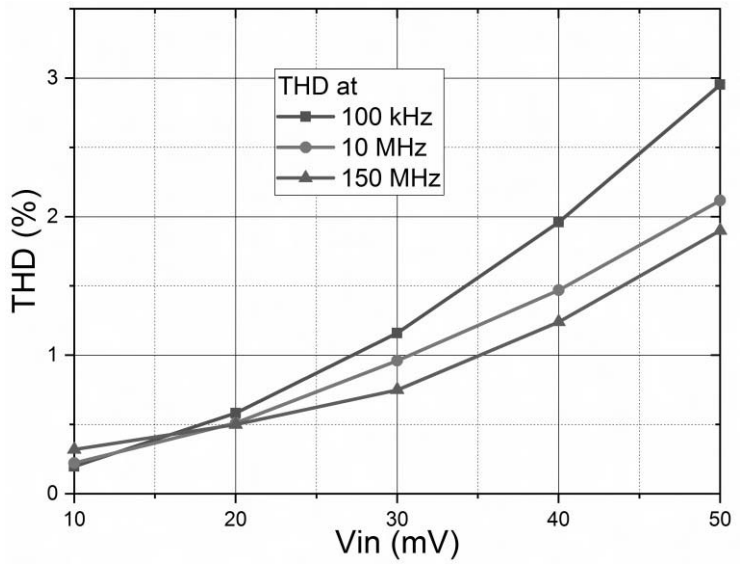
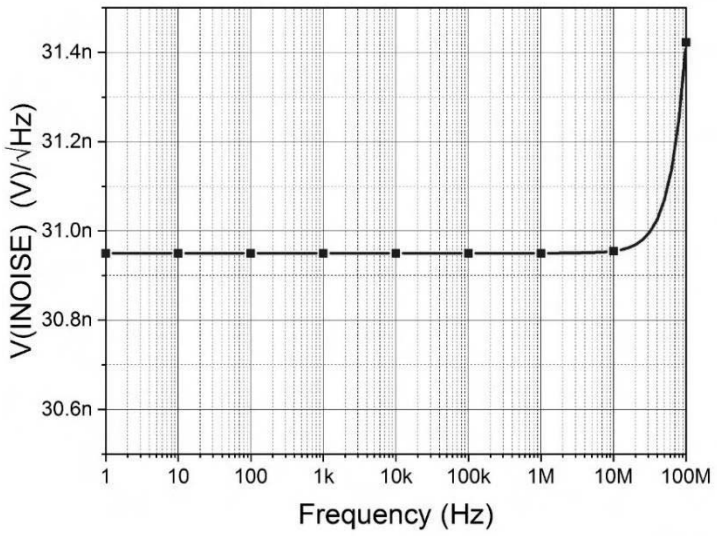
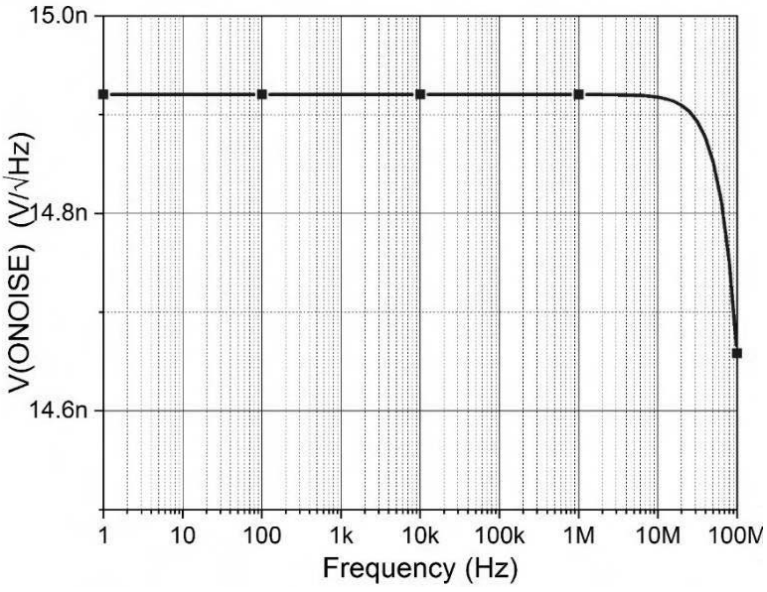


Figure 5.5 THD vs V_{in1}

The effect of noise on the proposed circuit is also examined for simulation settings of V_{in1} =100 mV AC signal while V_{in2} is taken as 80 mV DC. The equivalent input and output noise densities with varying input frequencies are plotted in Figure 5.6 (a) and Figure 5.6 (b) respectively. It is observed that the proposed FQAM has low noise densities.



(a)



(b)

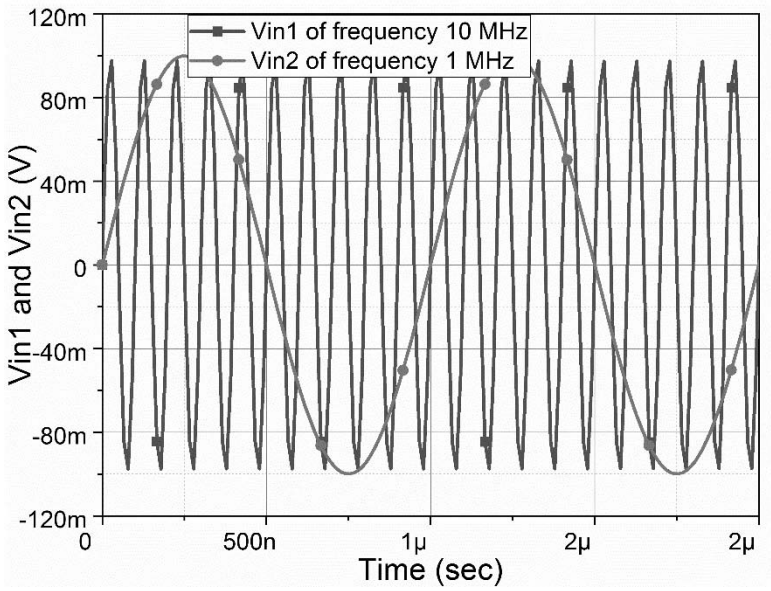
Figure 5.6 (a) Input Noise and (b) Output Noise

5.2.1.3 Applications of Proposed FQAM

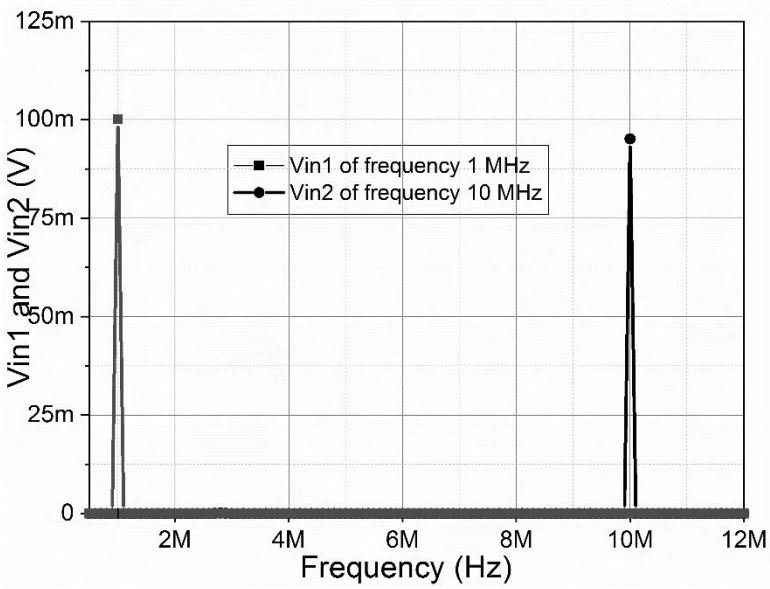
In this subsection, two applications of the proposed FQAM are presented. An amplitude modulator is presented first which is followed by a rectifier circuit.

Amplitude Modulator

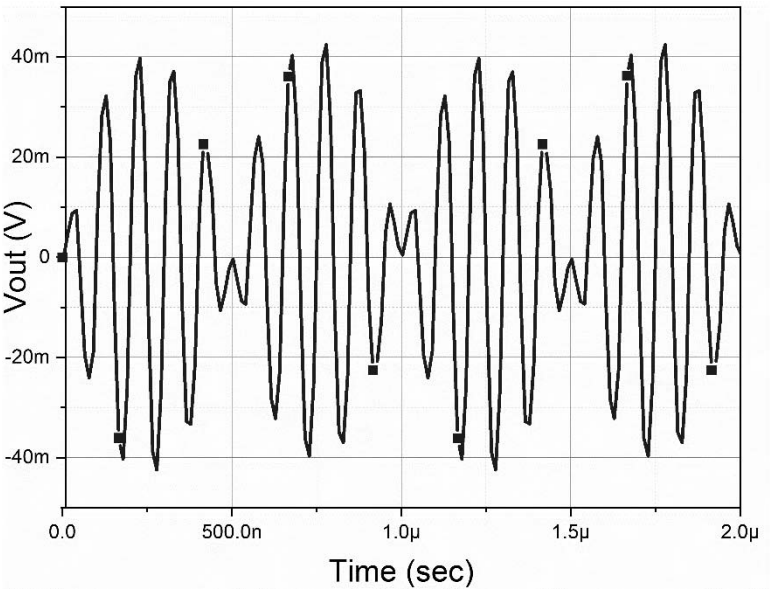
An amplitude modulator can be designed using FQAM by applying the carrier and modulating signals to the two inputs of an FQAM respectively. To validate the functionality of the designed amplitude modulator, two sinusoids of 100 mV/10 MHz and 100 mV/1 MHz were applied at V_{in1} and V_{in2} respectively. The input transient and its spectrum are shown in Figures 5.7 (a) and (b) respectively. The amplitude modulated output and corresponding spectrum are depicted in Figures 5.7 (c) and (d) respectively. The output frequency spectrum has two frequency components of 9 MHz and 11 MHz thereby confirming the modulation operation.



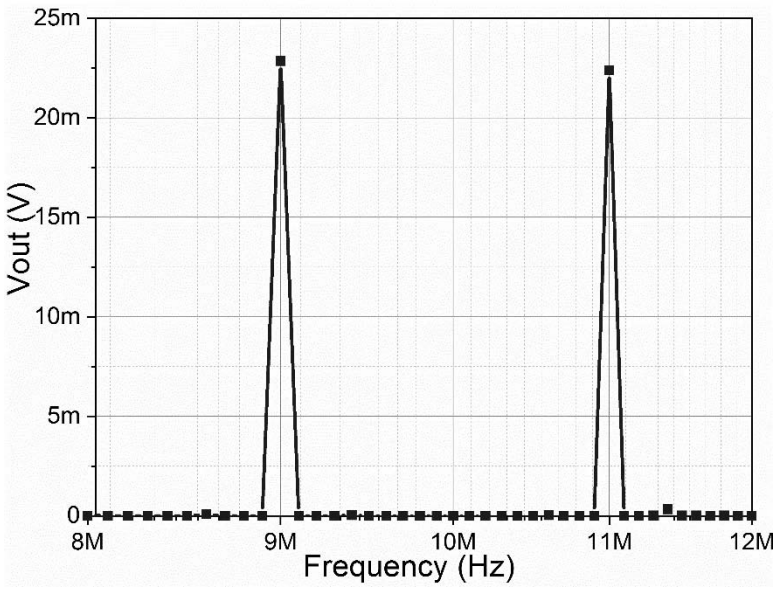
(a)


125m
100m
75m
50m
25m
0
Vin1 and Vin2 (V)
Vin1 of frequency 1 MHz
Vin2 of frequency 10 MHz
2M
4M
6M
8M
10M
12M
Frequency (Hz)

(b)


40m
20m
0
-20m
-40m
Vout (V)
0.0
500.0n
1.0µ
1.5µ
2.0µ
Time (sec)

(c)

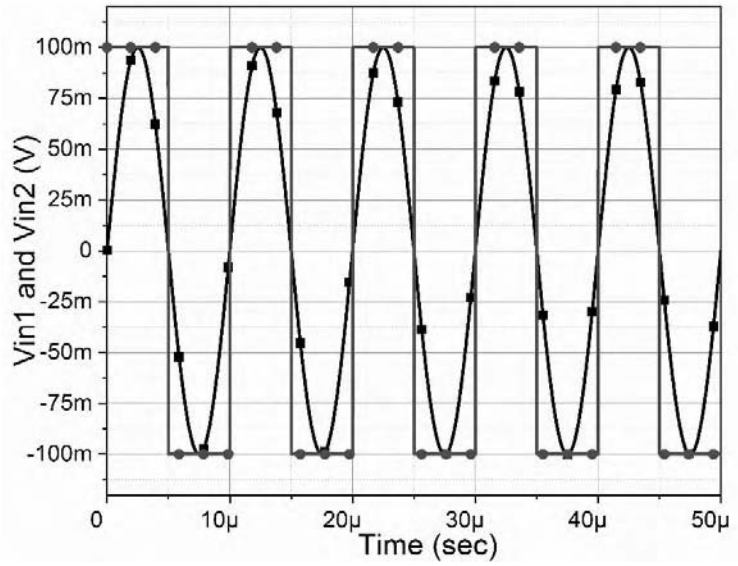


(d)

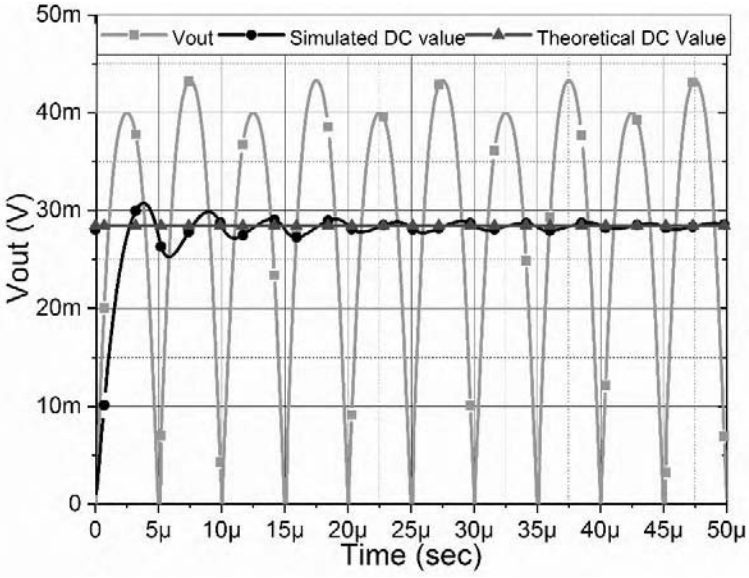
Figure 5.7 (a) Input transient, (b) Frequency spectrum of input signal, (c) Output transient and (d) Frequency spectrum of output signal

Rectifier

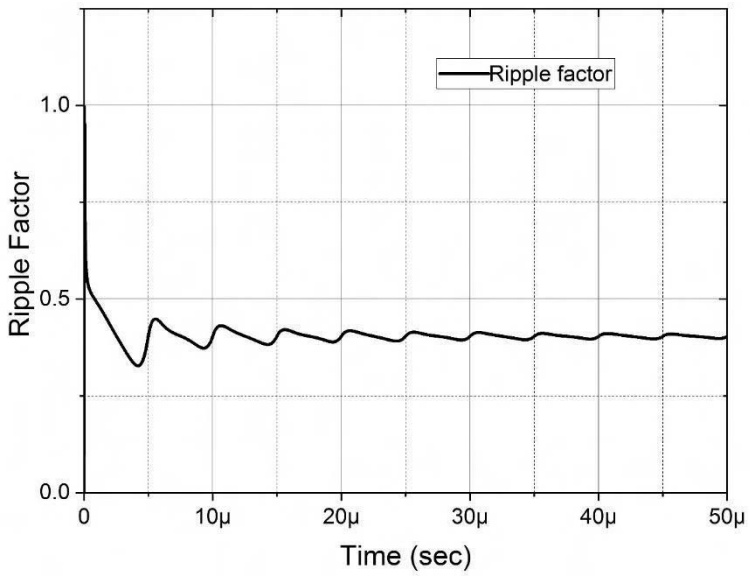
A rectifier can be implemented using a multiplier by applying a square wave at one of its inputs and the signal to be rectified at the other input while keeping frequency of both the inputs to be same. To verify the workability of the rectifier, designed using the above principle, two inputs namely a sinusoidal signal and a square wave of 100 mV/100 kHz each were applied to the respective input terminals of the FQAM. The input transient is shown in Figure 5.8 (a) and the rectified output is presented in Figure 5.8 (b). The simulated DC value is found to be 28.54 mV which is in the close approximation of the calculated value of 28.42 mV. The simulated ripple factor curve is shown in Figure 5.8 (c). The steady state value of the ripple factor is observed to be less than 0.5 which is in agreement to the theoretical result of a full wave rectifier.


100m
75m
50m
25m
0
-25m
-50m
-75m
-100m
Vin1 and Vin2 (V)
0
10µ
20µ
30µ
40µ
50µ
Time (sec)

(a)


Vout
Simulated DC value
Theoretical DC Value
50m
40m
30m
20m
10m
0
Vout (V)
0
5µ
10µ
15µ
20µ
25µ
30µ
35µ
40µ
45µ
50µ
Time (sec)

(b)



(c)

Figure 5.8 Time domain representation of (a) input signals, (b) output signal and (c) ripple factor

5.3 Squaring Circuit

A squaring circuit is extensively used to realize mathematical functions such as frequency doubling, finite impulse response filtering, peak detection of amplitude and square law detection etc. [139]. Several implementations of squaring circuit using different ABBs are available in the literature [133], [137], [138], [140]–[146]. out of which [133], [144] are CM structures, [141], [145] provide TAM output, [143] is a TIM squaring circuit. Only [137], [138], [140], [142], [143], [146] are VM circuits which are compiled with their salient features in Table 5.2.

Table 5.2 Comparison of existing VM squaring circuits

Reference No.	ABB	No. of ABB	Passive component used	Technique	Mode of operation	Output impedance	Power supply(V)	Power consumption(mW)	Technology used	Post Layout Simulations
[137]	OTRA	1	Nil	Multiplier based	VM	Low	±1.5	0.83	0.5 µm CMOS	No
[138]	OTRA	1	Nil	Multiplier based	VM	Low	±1.5	Not reported	0.5 µm CMOS	No
[140]	Op-Amp	1	1R	Direct	VM	Low	±5	Not reported	Of shelf Op-Amps with nmos in 1.75 µm CMOS technology	No
[142]	CDBA	1	1R	Direct	VM	Low	±5	Not reported	0.35 µm CMOS	No
[143]	OTA	4	Nil	Direct	VM	High	±1.7	Not reported	Bipolar PR200 and NR200	No
[146]	CCII	1	1R	Direct	VM	High	±5	Not reported	Off-shelf Op-Amps with nmos in 1.75 µm CMOS technology	No
Proposed work	VDBA	1	1R	Direct	VM	Low	±0.7	0.11	0.18 µm CMOS	Yes

It is observed from Table 5.2 that

- A squaring circuit can be implemented either using a multiplier with same inputs [137], [138] or using other direct methods as proposed in [140], [142], [143], [146].
- The topologies of [143], [146] provide voltage output at high impedance which makes cascading difficult.
- Structures of [143] use multiple ABBs.
- The supply voltages of ±1.5 V or above are used in [137], [138], [140], [142], [143], [146].
- Power consumption of some of the structures [137] is very high.

Therefore, a low power squaring circuit using a single VDBA is proposed in this chapter which provides voltage output at a low impedance node.

5.3.1 Proposed Squaring Circuit

The proposed squaring circuit consists of a VDBA, a resistance R and two completely matched NMOS transistors (M_{S1} and M_{S2}) as shown in Figure 5.9 which are biased in the linear region. The input voltage (V_{in}) is applied at the drain of M_{S1} whereas the drain of M_{S2} is driven by inverted input voltage ($-V_{in}$). The V_g represents the gate voltage applied externally to control the operation of the transistors and the squared output voltage is represented as V_{SQ_out}.

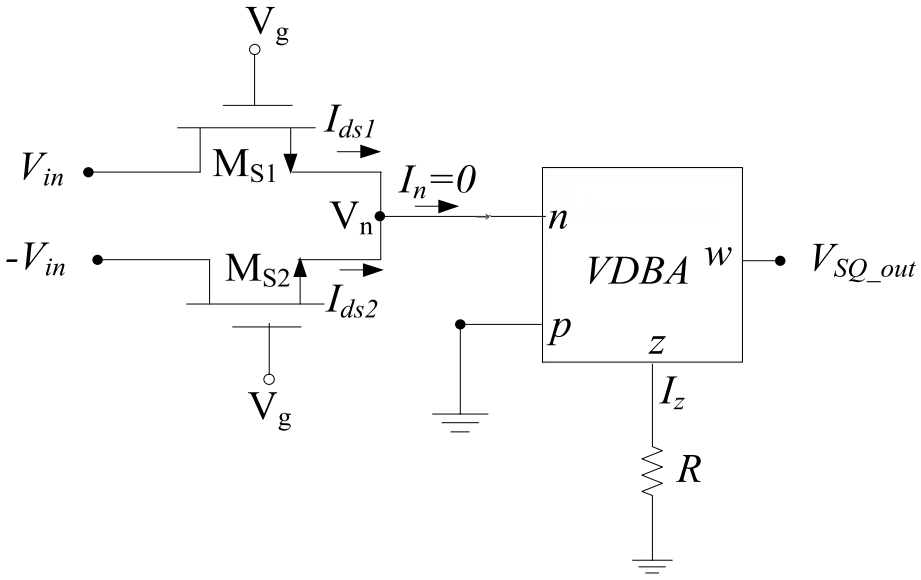


Figure 5.9 Proposed squaring circuit

Using routine analysis the drain current through transistor M_{S1} operating in the linear region is given by

$$I_{ds1} = K\left[\left(V_{gs} - V_{TH}\right)\left(V_{in} - V_n\right) - \frac{\left(V_{in} - V_n\right)^2}{2}\right] \tag{5.31}$$

The V_{gs} and V_{ds} are the gate to source and drain to source voltages respectively and V_{TH} is the threshold voltage.

The V_{gs} for a transistor can be written as

$$V_{gs} = V_g - V_n \tag{5.32}$$

Similarly, the current through M_{S2} can be expressed as

$$I_{ds2} = K\left[\left(V_{gs} - V_{TH}\right)\left(-V_{in} - V_n\right) - \frac{\left(-V_{in} - V_n\right)^2}{2}\right] \tag{5.33}$$

Ideally, *n* being infinite resistance terminal, the current through this terminal is zero, which results in

$$I_{ds1} = -I_{ds2} \tag{5.34}$$

Substitution of I_{ds1} and I_{ds2} in equation (5.34), gives

$$V_n^2 - 2(V_g - V_{TH})V_n - V_{in}^2 = 0 \tag{5.35}$$

V_n can therefore be computed as

$$V_n = (V_g - V_{TH})\left\{1 \pm \sqrt{1 + \frac{V_{in}^2}{(V_g - V_{TH})^2}}\right\} \tag{5.36}$$

Since V_{in} is small, using binomial series expansion, (5.36) can be written as

$$V_n = (V_g - V_{TH})\left\{1 \pm \left(1 + \frac{1}{2}\frac{V_{in}^2}{(V_g - V_{TH})^2}\right)\right\} \tag{5.37}$$

And the only practical solution of (5.35) is

$$V_n = -\frac{1}{2}\frac{V_{in}^2}{(V_g - V_{TH})} \tag{5.38}$$

From characteristics equation of VDBA, V_z can be written as

$$V_z = -g_m R V_n \tag{5.39}$$

and hence the output of the squaring circuit V_{SQ_out} may be expressed as

$$V_{SQ\_out} = \frac{g_m R}{2}\frac{V_{in}^2}{(V_g - V_{TH})} = C_1 V_{in}^2 \tag{5.40}$$

where, $C_1 = \frac{g_m R}{2(V_g - V_{TH})}$ is the constant of proportionality and it can be controlled either through external resistor R or electronically through transconductance of the VDBA. Thus the output voltage is directly proportional to the square of the applied input voltage.

The resistance R of Figure 5.9 can be realized using MOSFETs as shown in Figure 2.16. This way the proposed squaring circuit is completely MOS implementable.

5.3.1.1 Non-Ideal Analysis

Using non-ideal model of VDBA the squaring circuit of Figure 5.9 can be redrawn as shown in Figure 5.10.

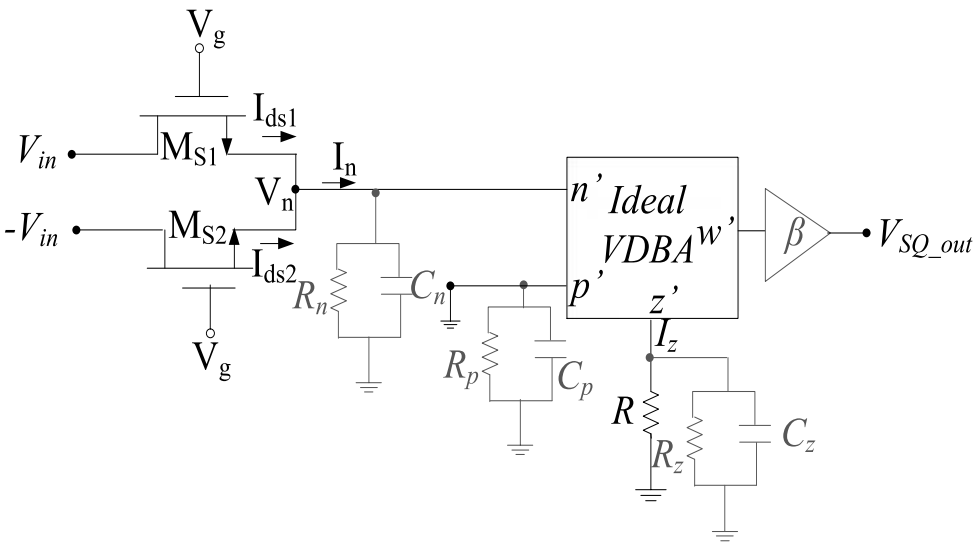


Figure 5.10 Non-ideal model of squaring circuit

Under these conditions, the resistance R gets modified to R_{eq} given by

$$R_{eq} = R // R_z // X_{C_z} = \frac{1}{\left(\frac{R_1 + R_z}{R_1 R_z}\right) + sC_z} \tag{5.41}$$

The currents at node *n* can be expressed as

$$I_n = \frac{V_n'}{Z_n} = I_{ds1} + I_{ds2} \tag{5.42}$$

Where $Z_n = R_n // X_{C_n} = \frac{R_n}{1 + sR_nC_n}$ (5.43)

Thus the output of the squaring circuit in presence of non-idealities $V_{SQ\_out\_n}$ can be obtained as

$$V_{SQ\_out\_n} = \frac{1}{2}\beta\alpha g_m \frac{1}{\left(\frac{R+R_z}{RR_z}\right)+sC_z}\frac{V_{in}^2}{(V_g - V_{TH}) + X/2}$$

(5.44)

where $X = \frac{1}{KZ_n}$

(5.45)

since X << (V_g-V_{TH}) and R_z >> R, $V_{SQ\_out\_n}$ can be approximated as

$$V_{SQ\_out\_n} = \frac{1}{2}\beta\alpha g_m R \frac{1}{1+sC_zR}\frac{V_{in}^2}{(V_g - V_{TH})} = C_{1\_n}V_{in}^2$$

(5.46)

Where C_{1_n} is the modified constant of proportionality in presence of VDBA non-idealites and is given by (5.47)

$$C_{1\_n} = \frac{1}{2}\beta\alpha g_m R \frac{1}{1+sC_zR}\frac{1}{(V_g - V_{TH})}$$

(5.47)

Thus the bandwidth of the proposed circuit is found to be $1/RC_z$.

5.3.1.2 Simulation Results

The CMOS implementation of the VDBA proposed in chapter 3 is used for simulations. The supply voltage of ± 0.7 V is used for simulations. All the bias currents used in VDBA of Figure 3.2 are set as 10 µA. The V_g for squaring is set to 0.62 V. The value of R is chosen to be 0.7 kΩ, in order to make the proportionality constant C_1 to be unity. The layout of the proposed squaring circuit with physical verification checks namely

DRC and LVS check is shown in Figure 5.11 which occupies an active die area of 19 µm × 37 µm. Both pre and post layout simulations are carried out which have been described in this subsections.

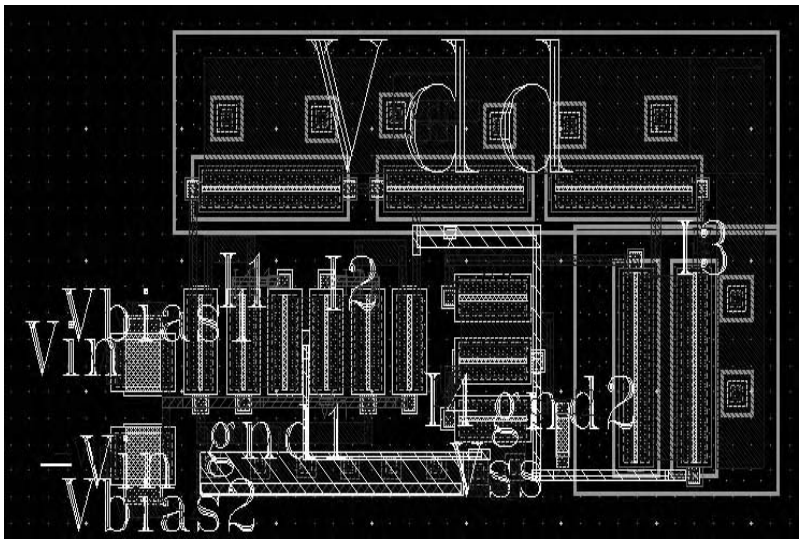


Figure 5.11 Layout of squaring circuit

The theoretical, schematic driven and post-layout DC transfer characteristics of the proposed squaring circuit are shown in Figure 5.12 wherein the V_{in} is swept from -150 mV to 150 mV. It may be observed that simulated results are in close agreement with the theoretical values.

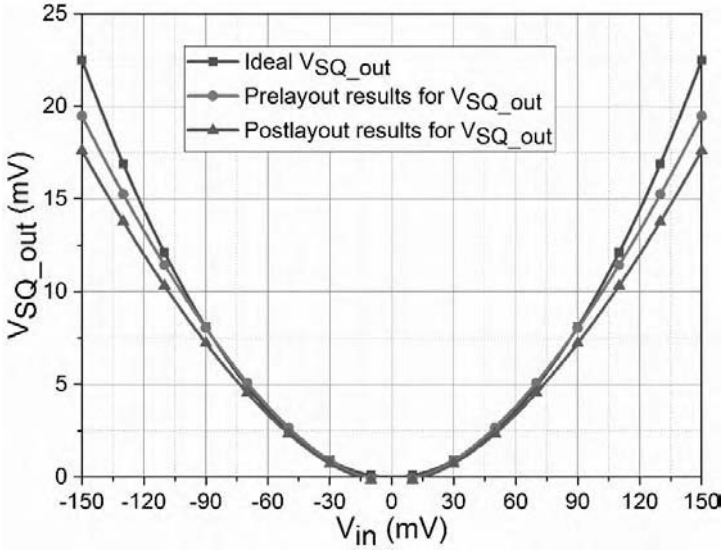


Figure 5.12 DC characteristics of squaring circuit

The proposed structure was also tested for AC behavior. Both pre and post layout frequency responses of the squaring circuit are shown in Figure 5.13 wherein a 100 mV signal is applied at the input. The pre and post layout 3 dB frequencies for squaring circuit are obtained as 3.77 MHz and 3.72 MHz.

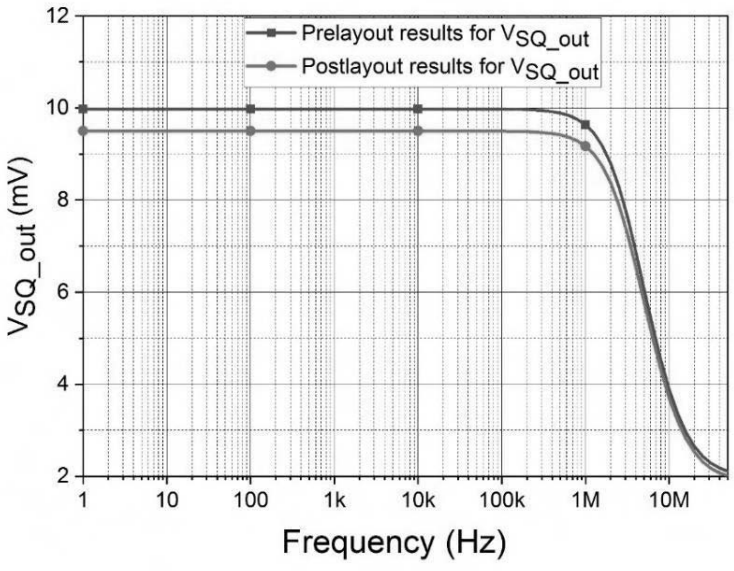
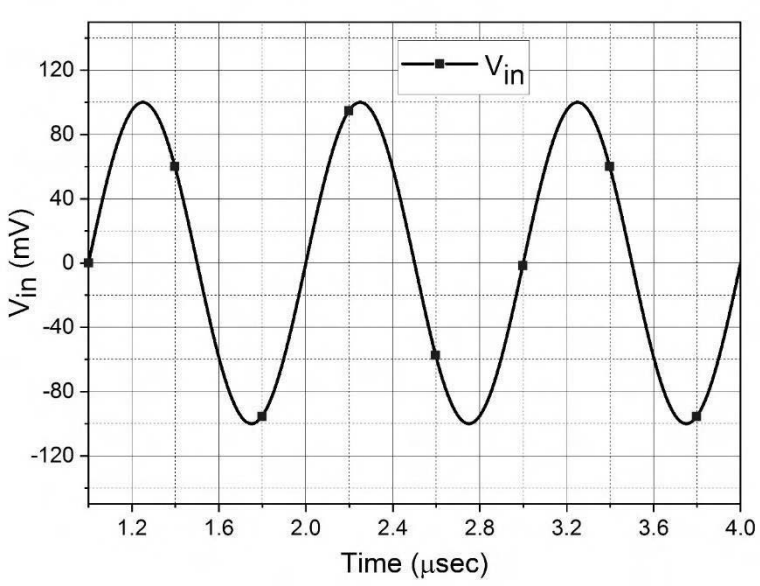
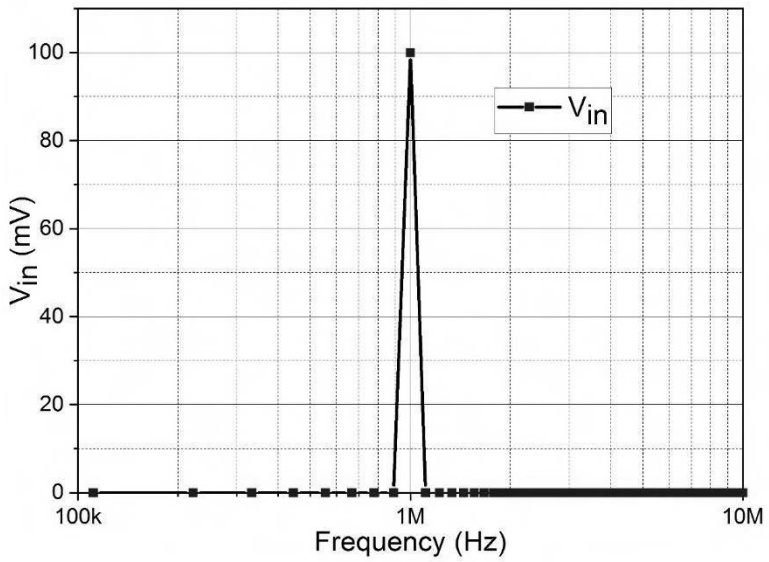


Figure 5.13 AC characteristics of squaring circuit

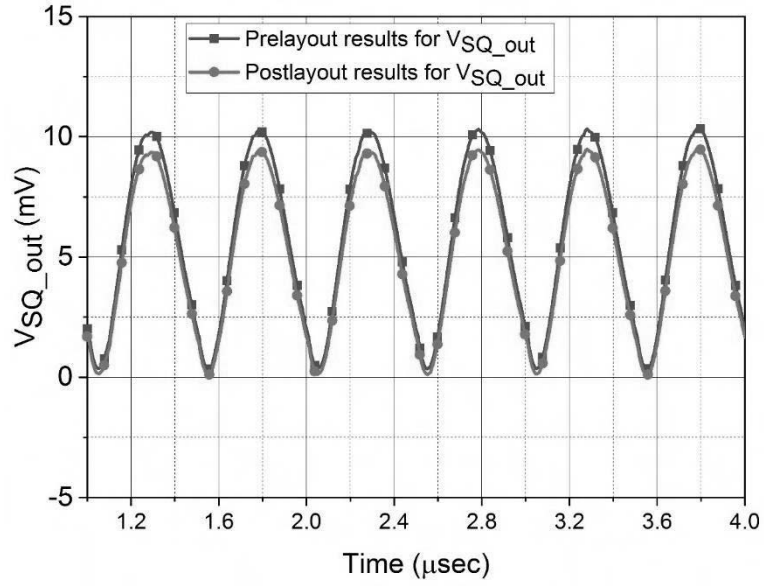
The transient analysis is also carried out for the proposed circuit. A sinusoid of 1 MHz/ 200 mV peak to peak amplitude as shown in Figure 5.14 (a) is used as input and its spectrum is shown in Figure 5.14 (b). The transient output and corresponding spectrum are presented in Figure 5.14 (c) and (d) respectively. As expected the output frequency is twice of the input frequency.


Vin
120
80
40
0
-40
-80
-120
Vin (mV)
1.2
1.6
2.0
2.4
2.8
3.2
3.6
4.0
Time (μsec)

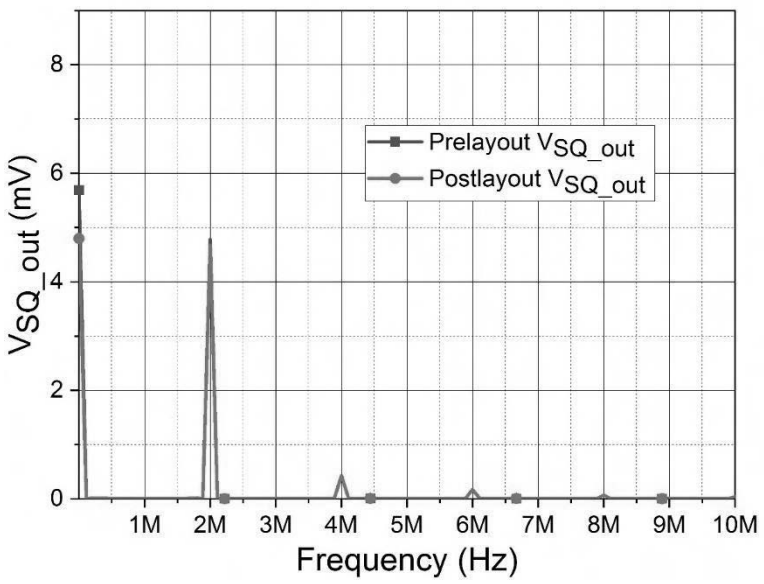
(a)


Vin
100
80
60
40
20
0
Vin (mV)
100k
1M
10M
Frequency (Hz)

(b)



(c)

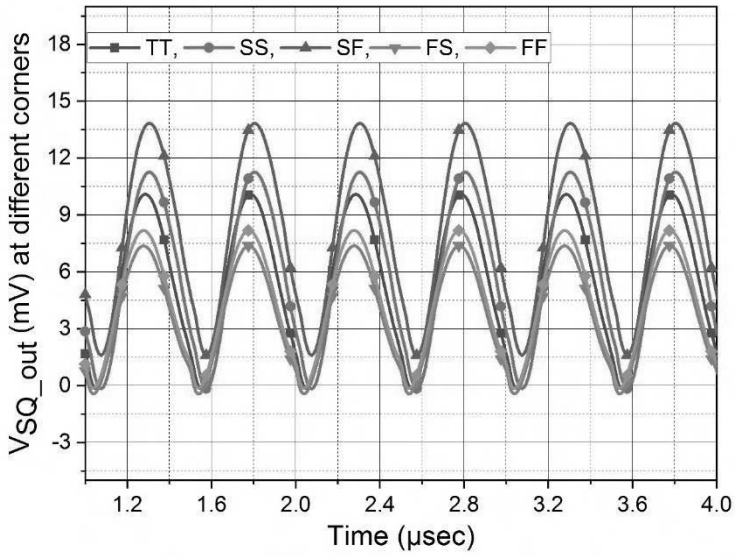


(d)

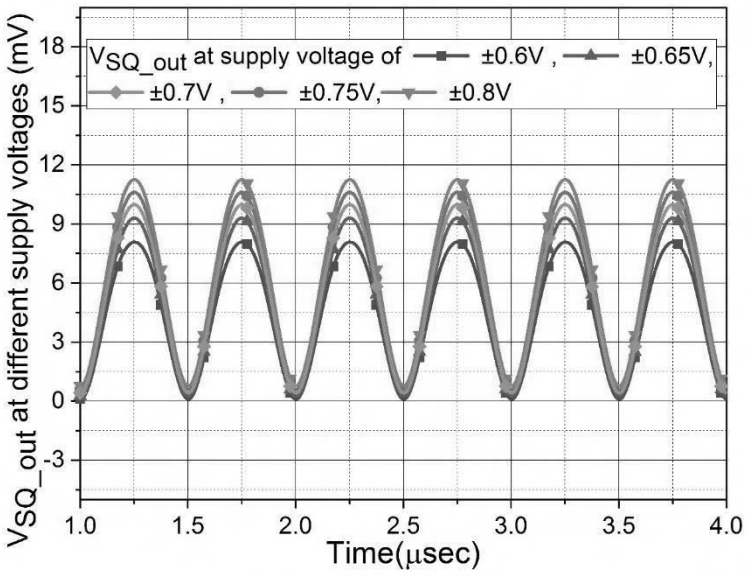
Figure 5.14 (a) Sinusoidal input, (b) spectrum of the input, (c) transient output and (d) the output spectrum for the squaring circuit

The transient performance of the proposed squaring circuit is investigated under PVT variations. The transient responses at different corners obtained through post layout simulations, wherein inputs are taken the same as used in the transient analysis section, are shown in Figure 5.15 (a). To determine the effect of supply voltage on output, the

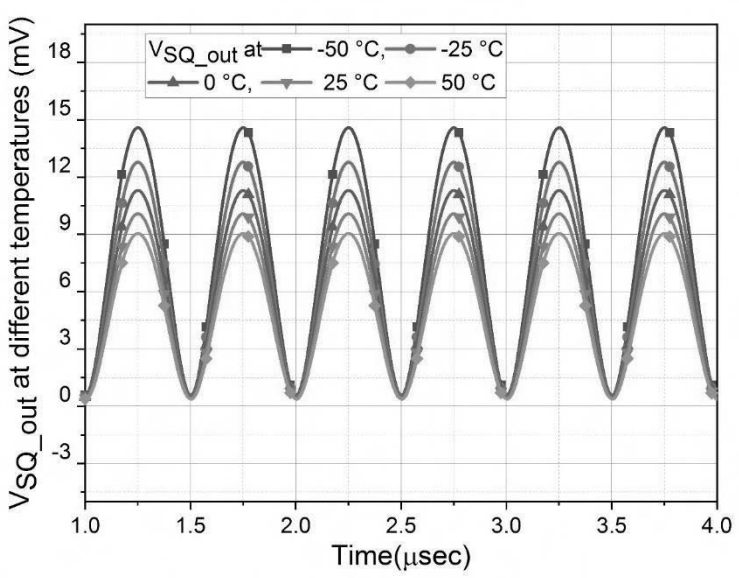
transient responses are obtained from post-layout simulations, at different supply voltages ranging from ± 0.6 V to ± 0.8 V in steps of 0.05 V and are depicted in Figure 5.15 (b). Further, the proposed structure is simulated at different temperature values varying from −50 °C to 50 °C in steps of 25 °C at ± 0.7 V supply voltages. Figure 5.15 (c) shows the post-layout results for temperature variations.



(a)



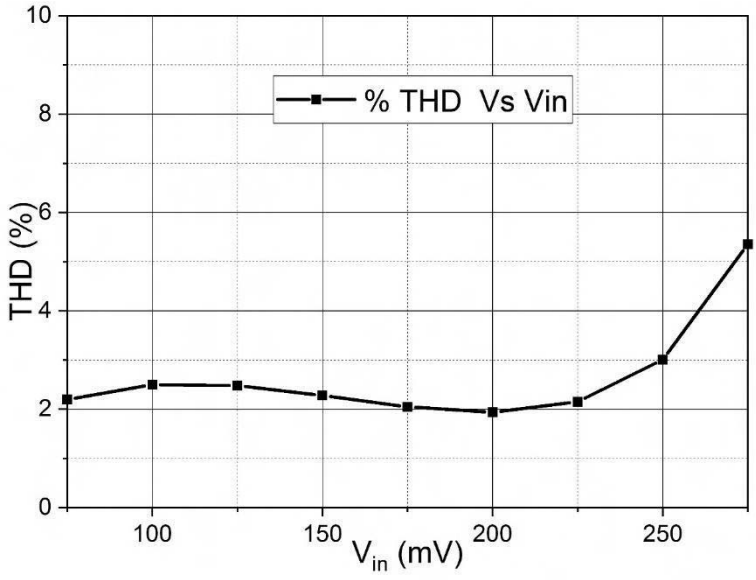
(b)



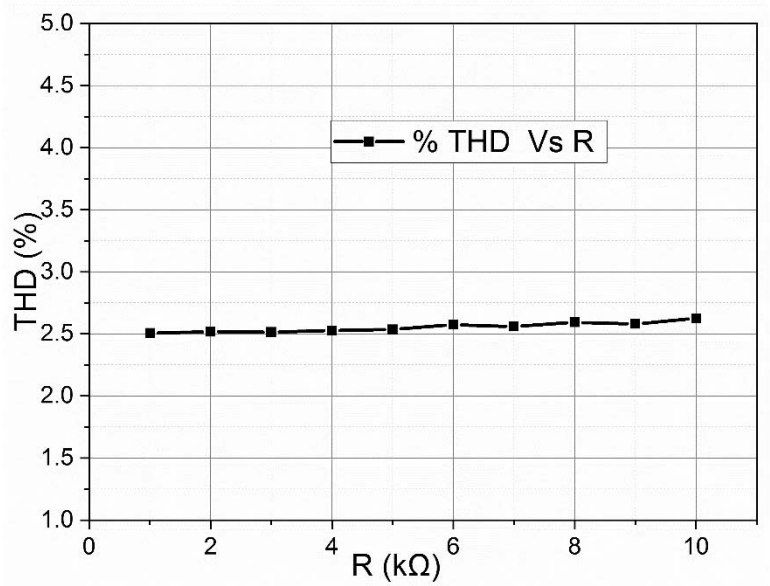
(c)

Figure 5.15 Transient output of squaring circuit at different (a) corners, (b) supply voltages and (c) temperatures

For the proposed squaring circuit, the variation in THD is plotted in Figure 5.16 (a) against the variation in input signal amplitude. The variation in THD with respect to variation in resistance R is depicted in Figure 5.16 (b). It is found that for the entire input range the maximum THD remains below 3 % of the proposed squaring circuit.



(a)



(b)

Figure 5.16 (a) THD Vs V_{in} and (b) THD Vs R

5.4 Square Rooting Circuit

A square rooting circuit is used for calculating the root mean square value of any arbitrary waveform and linearization of a signal measured by a differential flow meter [147]. Square rooting is also required to determine impedances under sinusoidal excitation, as well as in case of obtaining three vectors from a three-phase power system [148].

Several implementations of square rooting circuit using different ABBs are available in the literature [133], [141], [142], [145], [146], [149]–[152] out of which [133], [150], [152] are CM structures, [149] provides TAM output, [145] is a TIM square rooting circuit. Only [141], [142], [146], [150], [151] are VM circuits which are compiled with their salient features in Table 5.3.

Table 5.3 Comparison of existing VM square rooting circuits

Reference	ABB	No. of ABB	Passive component	Technique	Output Impedance	Power supply(V)	Power Consumption (mW)	Technology	Post Layout Simulations
[141]	OTA	3	Nil	Divider based	High	±5	10	CMOS Technology node Not reported.	No
[142]	CDBA	1	1R	Direct	Low	±5	Not reported	0.35 µm CMOS	No
[146]	CCII	1	1	Direct	High	±6	Not reported	AD844 and CMOS transistor arrays CD4007.	No
[150]	CCCII	2	3R	Direct	High	±2.5	50.4	Bipolar PR100N and NR100N	No
[151]	OTRA	1	1R	Divider based	Low	±1.5	1.05	0.25 µm CMOS	No
This work	VDBA	1	Nil	Direct	Low	±0.7	0.11	0.18µ CMOS	Yes

From Table 5.3, it is observed that

- The topologies of [146], [150] provide voltage output at high impedance which makes cascading difficult.
- Structures of [141], [150] use multiple ABBs.
- Work presented in [150] uses a large number of passive components.
- The supply voltages of ±1.5 V or above are used in [141], [142], [146], [150], [151].
- Power consumption of some of the structures [141], [150], [151] is very high.

Therefore, in this chapter, a low power square rooting circuit is designed using a single VDBA and providing voltage output at low impedance is proposed.

5.4.1 Proposed Square Rooting Circuit

The proposed square rooting circuit consisting of a VDBA and an NMOS transistor (M_{SR}) operating in the triode region, biased through gate bias voltage V_g, as depicted

in Figure 5.17. The input voltage V_{in} is applied at *n* terminal thereby producing a negative voltage at *z* terminal which in turn keeps M_{SR} in the triode region.

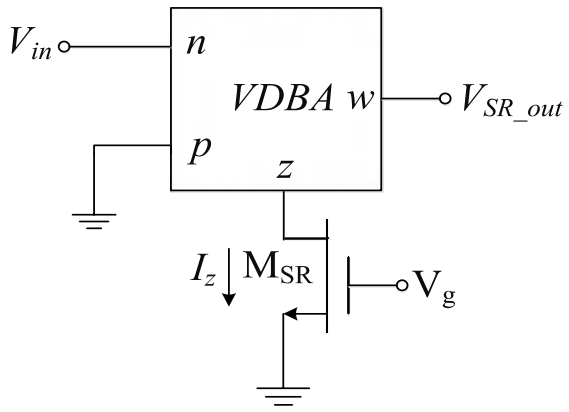


Figure 5.17 Proposed square rooting circuit

As the M_{SR} is biased in triode region so the current through M_{SR} is written as

$$I_z = K\left[\left(V_{gs} - V_{TH}\right)\left(V_z\right) - \frac{\left(V_z\right)^2}{2}\right] \tag{5.48}$$

Using the port relation of VDBA the current through z terminal (I_z) be expressed as

$$I_z = -g_m V_{in} \tag{5.49}$$

Further, the square rooting output denoted by V_{SR_out} can be written as

$$V_{SR\_out} = V_z \tag{5.50}$$

From (5.48), (5.49) and (5.50), we may write

$$K\left[\left(V_{gs}-V_{TH}\right)\left(V_{SR\_out}\right)-\frac{\left(V_{SR\_out}\right)^2}{2}\right]=-g_m V_{in}$$

(5.51)

The first term $\left(V_{gs}-V_{TH}\right)$ can be approximated to zero if V_{gs} is chosen to be approximately equal to V_{TH}. So from (5.51), V_{SR_out} can be computed as

$$V_{SR\_out}=\pm\sqrt{\frac{2g_m V_{in}}{K}}=C_2\sqrt{Vin}$$

(5.52)

were C_2 is the constant of proportionality and is defined as $-\sqrt{\frac{2g_m}{K}}$. Only for this value of C_2 the M_{SR} will be biased in triode region. It is evident from (5.52) that the output voltage is proportional to the square root of the input applied.

5.4.1.1 Non-Ideal Analysis

In this subsection, the investigation of square rooting circuit in the presence of the VDBA non-idealities is presented and the deviation from ideal behavior is also enumerated. The non-ideal squaring rooting circuit is depicted in Figure 5.18.

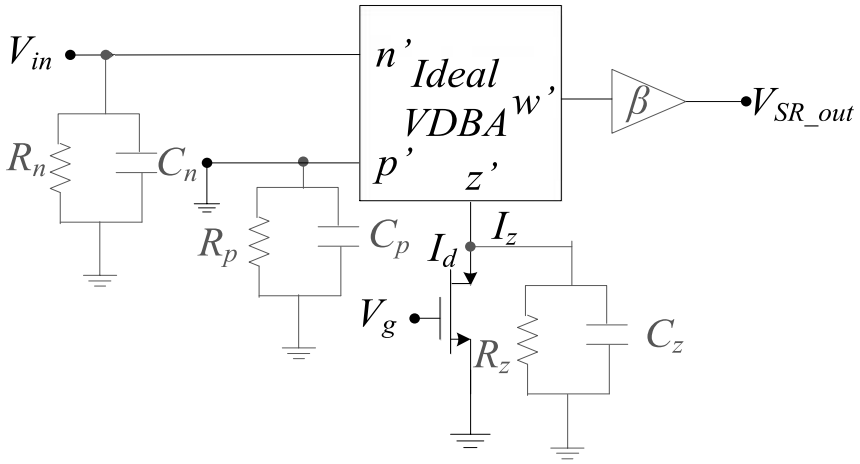


Figure 5.18 The non-ideal model for the square rooting circuit

Performing routine analysis the drain current through M_{SR} is obtained as

$$I_d = K\left[\left(V_{gs} - V_{TH}\right)\left(V_z\right) - \frac{\left(V_z\right)^2}{2}\right] \tag{5.53}$$

Considering the resistance of M_{SR} in linear region to be R_{on} the I_d in terms I_z can be expressed as

$$I_d = -I_z \frac{R_z \,//\, 1/sC_z}{R_z \,//\, 1/sC_z + R_{on}} \tag{5.54}$$

$$I_d = -\alpha g_m V_{in} \frac{R_z/(R_z + R_{on})}{1 + sC_z R_z R_{on}/(R_z + R_{on})} \tag{5.55}$$

From (5.53) and (5.55)

$$\left[\left(V_{gs} - V_{TH}\right)\left(V_z\right) - \frac{\left(V_Z\right)^2}{2}\right]K = -\alpha g_m V_{in} \frac{R_z/(R_z + R_{on})}{1 + sC_z R_z R_{on}/(R_z + R_{on})} \tag{5.56}$$

As V_{gs}-V_{TH} is ≈0, and R_z>> R_{on} , (5.56) modifies to

$$\frac{\left(V_Z\right)^2}{2} K = \alpha g_m V_{in} \frac{1}{1 + sC_z R_{on}} \tag{5.57}$$

$$V_Z = -\sqrt{\frac{2}{K} \alpha g_m V_{in} \frac{1}{1 + sC_z R_{on}}} \tag{5.58}$$

And from terminal characteristics of VDBA

$$V_{SR\_out} = \beta V_z \tag{5.59}$$

Substituting V_z from (5.58) in (5.59)

$$V_{SR\_out} = -\beta\sqrt{\frac{2}{K}\alpha g_m V_{in}\frac{1}{1+sC_zR_{on}}} = C_{2\_n}\sqrt{V_{in}} \tag{5.60}$$

Here C_{2_n} represents the constant of proportionality under non-ideal conditions and is given by

$$C_{2\_n} = -\beta\sqrt{\frac{2}{K}\alpha g_m \frac{1}{1+sC_zR_{on}}} \tag{5.61}$$

5.4.1.2 Simulation Results

The proposed circuit is characterized through both pre and post layout simulations using 0.18 µm GPDK MOS technology node using Cadence Virtuoso ADE tool. The VDBA proposed in chapter 3 is used for simulations. The supply voltage of ± 0.7 V is used for simulations. All the bias currents used are set as 10 µA. The V_g for square rooting circuit is set as 0.49 V. The layout of the proposed circuit is shown in Figure 5.19 which occupies active die area of 22 µm × 32 µm.

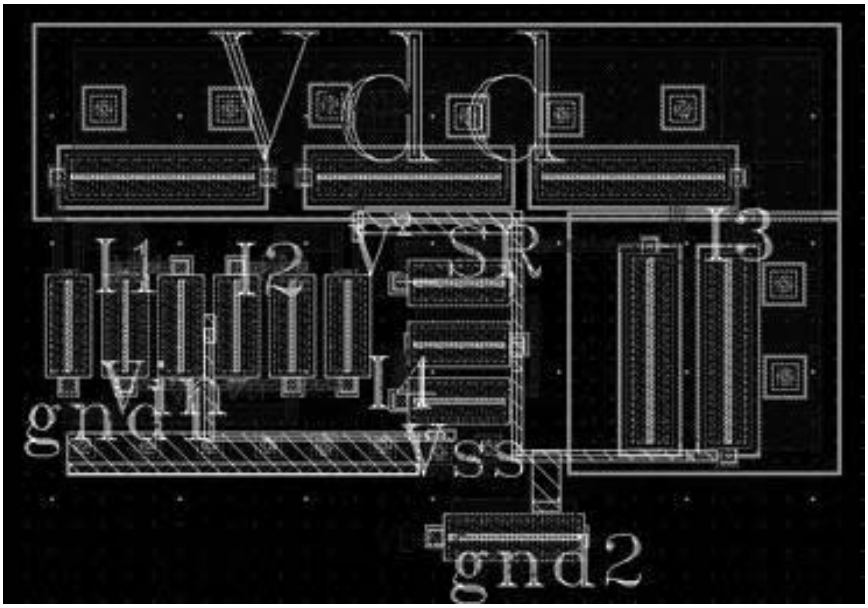


Figure 5.19 Layout of proposed square rooting circuits

The theoretical, schematic driven and post layout DC characteristics for the proposed circuit are shown in Figure 5.20. The DC transfer characteristics are obtained for $V_{in} > 0$. The pre and post layout DC characteristics are in line with theoretical results for an approximate input signal range of 0-50 mV.

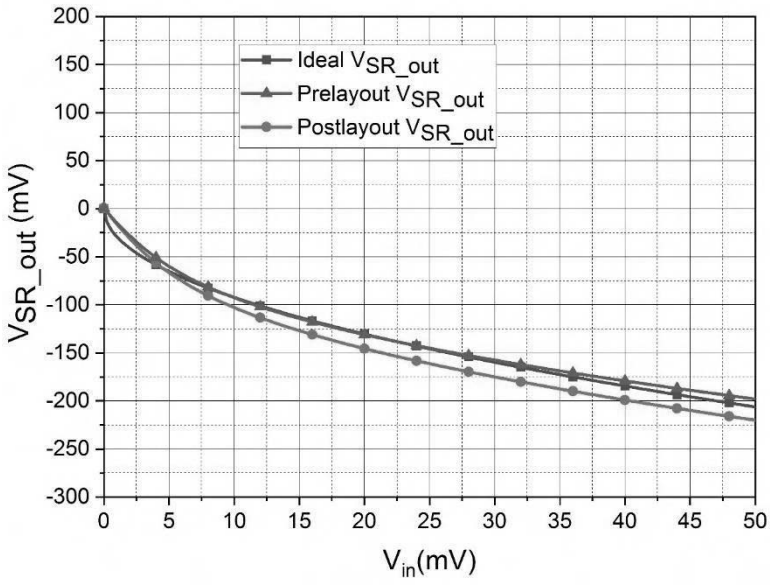


Figure 5.20 DC characteristics of square rooting circuit

The proposed structure is tested for AC behavior next. The pre and post layout frequency responses for the proposed square rooting circuit with an input applied signal

of 10 mV are presented in Figure 5.21. The pre and post layout 3 dB frequencies for square rooting circuit are observed 90 MHz and 89.7 MHz respectively.

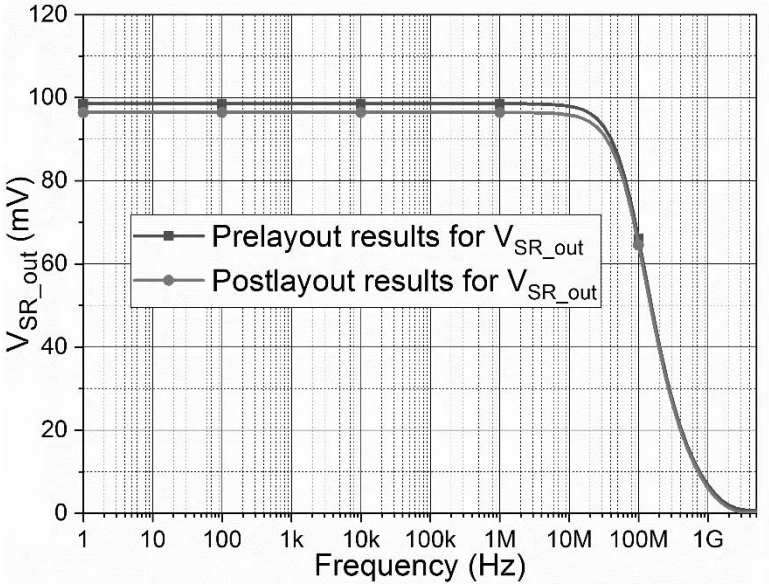
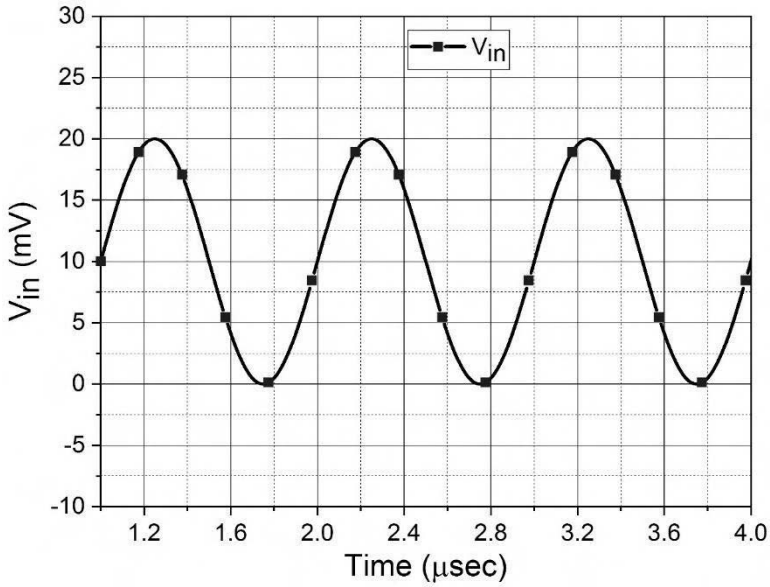
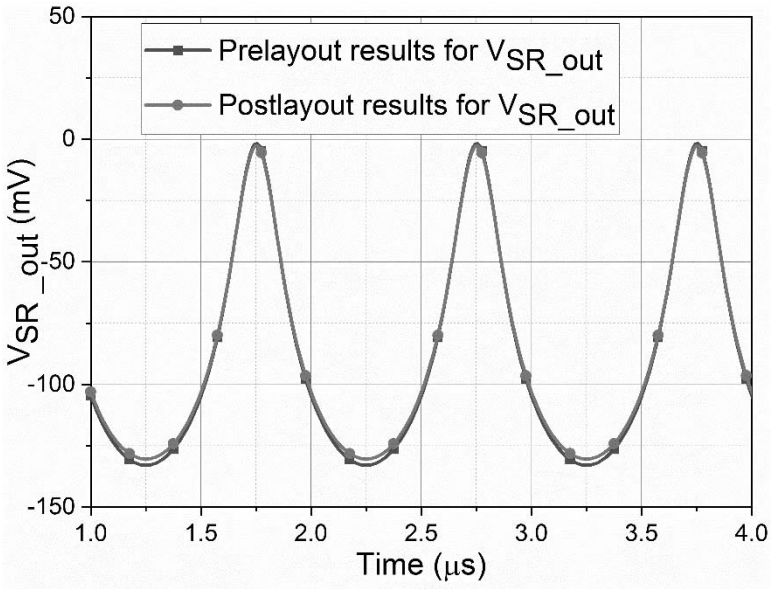


Figure 5.21 AC characteristics of square rooting circuit

For the square rooting circuit, an input sinusoidal signal of 1 MHz/ 20 mV peak to peak depicted in Figure 5.22 (a) is used and Figure 5.22 (b) shows the output.



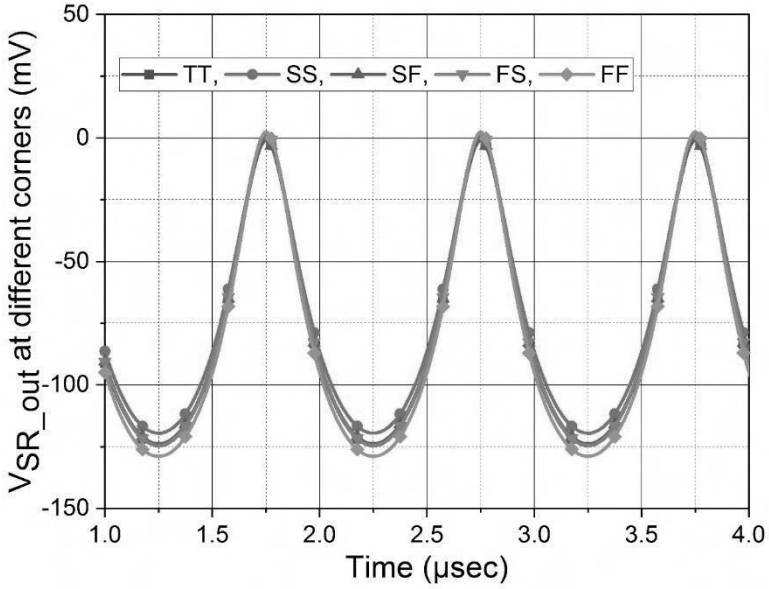
(a)



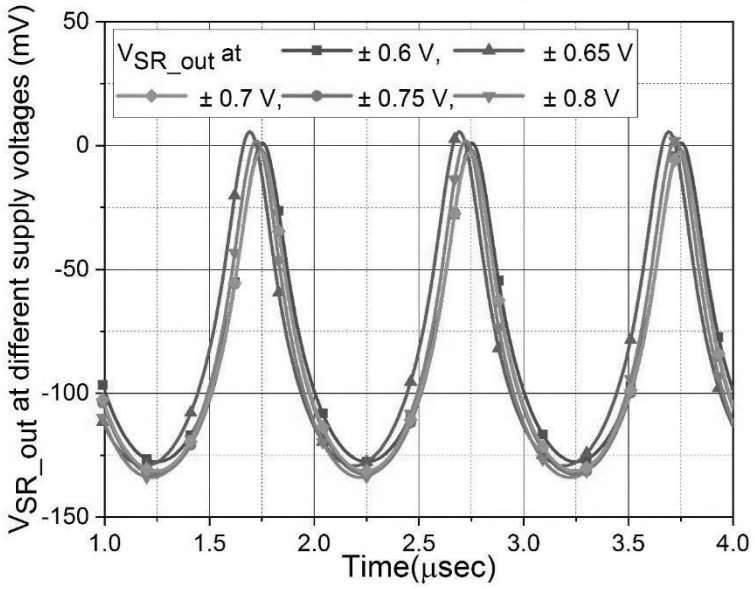
(b)

Figure 5.22 (a) Sinusoidal input and (b) the corresponding output of the square rooting circuit

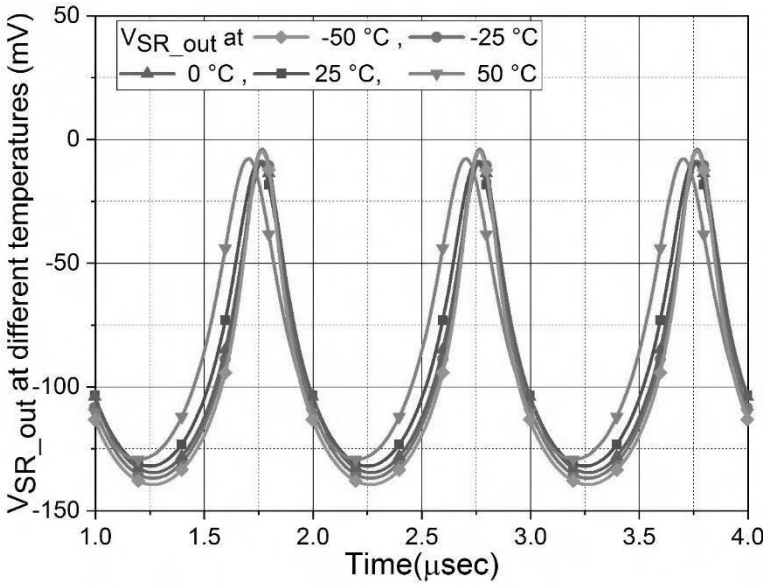
The transient performance is investigated under PVT variations also for the same input as depicted in Figure 5.22 (a). The transient responses at different corners are shown in Figure 5.23 (a). To check the variation of output with supply voltage, the transient responses for square rooting circuits are obtained from post-layout simulations, at different supply voltages ranging from ± 0.6 V to ± 0.8 V and are depicted in Figure 5.23 (b). Further, the proposed square rooting circuit is simulated at different temperature values varying from −50 °C to 50 °C at ± 0.7 V supply voltages. The post layout result for temperature variations are shown in Figure 5.23 (c). These results suggest that the proposed structure works well under PVT variations also.


TT,
SS,
SF,
FS,
FF
V_{SR_out} at different corners (mV)
Time (µsec)
50
0
-50
-100
-150
1.0
1.5
2.0
2.5
3.0
3.5
4.0

(a)


V_{SR_out} at
± 0.6 V,
± 0.65 V
± 0.7 V,
± 0.75 V,
± 0.8 V
V_{SR_out} at different supply voltages (mV)
Time(µsec)
50
0
-50
-100
-150
1.0
1.5
2.0
2.5
3.0
3.5
4.0

(b)



(c)

Figure 5.23 Transient output of square rooting circuit at different (a) corners, (b) supply voltages and (c) temperature

5.5 Conclusion

In this chapter, non-linear applications of VDBA are explored. A voltage mode FQAM based on quarter square algebraic identity employing DO-VDBA is proposed first. The theoretical propositions have been verified through SPICE simulations using 0.18 μm CMOS process parameter. The simulated THD for this circuit is well below 3 %. Applications like amplitude modulator and rectifier are presented using proposed FQAM to show its applicability and obtained results are in total agreement with the theory.

Low power squaring and square rooting topologies using single VDBA are proposed next. The proposed structures facilitate easy cascading as their output voltages are available at low impedance terminals. The workability of the proposed circuits was established using pre and post layout simulations using the Cadence Virtuoso tool. Both the circuits are tested under PVT variations also. The power consumption of proposed structures is quite low making them suitable for low power applications.

The results obtained through simulations for all the structures are found to be in corroboration with the theoretical proposition. All the proposed circuits are MOS implementable and are thus suitable from the integrated circuit view point.

CHAPTER 6

6.1 Introduction

The signal generators are the important class of circuits which are used in communication, instrumentation, testing and control applications. Signal generators are used to produce signals with specified characteristics like shape, period/frequency, phase etc. Broadly signal generators are categorized as (i) linear and (ii) non-linear oscillators. The linear oscillators are also termed as sinusoidal oscillators. Sinusoidal signals can be obtained either through appropriate shaping of triangular waveform or by using an amplifier and a frequency selective network in a positive feedback loop. This chapter presents the VDBA based sinusoidal oscillators which are designed using the second approach and the same has been described in brief in the following section.

6.2 Basic Principle

The generic structure of a sinusoidal oscillator is depicted in Figure 6.1 which consists of an amplifier and a frequency selective network connected in a positive feedback loop. In Figure 6.1 the x_i, x_o and x_f represent the input, output and feedback signals respectively. The *A(s)* represents the gain of the amplifier whereas *β(s)* is the transfer ratio of frequency selective feedback network. The closed loop gain $A_f(s)$ of this system may be computed as

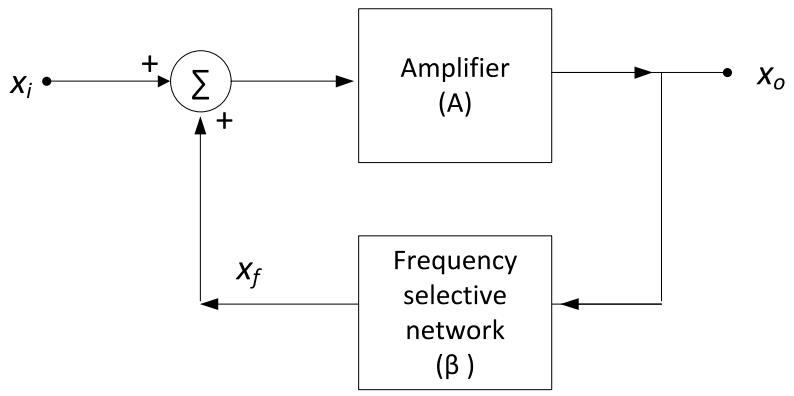


Figure 6.1 Block diagrammatic representation of the sinusoidal oscillators

$$A_f(s)=\frac{A(s)}{1-A(s)\beta(s)}$$

(6.1)

The characteristic equation (CE) of this positive feedback system is given by

$$1-A(s)\beta(s)=0$$

(6.2)

The term $A(s)\beta(s)$ represents the loop gain L(s) of this feedback system. If at a particular frequency (ω_0) the loop gain gets unity then the closed loop gain will be infinite. This implies that an output will be available in this system without applying any input and therefore this circuit will produce oscillations of that specific frequency (ω_0). This is known as Barkhuasen criterion of oscillations.

This chapter is devoted to the design of VDBA based sinusoidal oscillators. In all six sinusoidal oscillators are presented out of which one is single phase (SP), three structures are quadrature phase (QP) and two are multiphase (MP) sinusoidal oscillators.

6.3 Single Phase Oscillator (SPO)

The Proposed SP oscillator is shown in Figure 6.2 which consists of a single VDBA, three resistors and two grounded capacitors.

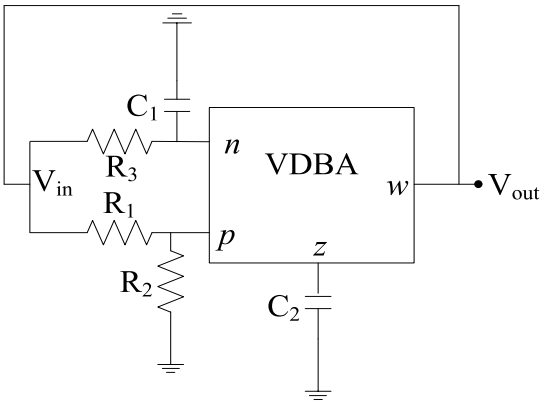


Figure 6.2 Proposed SP oscillator

The CE for the proposed SPO is obtained as

$$s^2 C_1 C_2 R_3 (R_1 + R_2) + s(C_2 (R_1 + R_2) - C_1 g_m R_3 R_2) + g_m R_1 = 0 \tag{6.3}$$

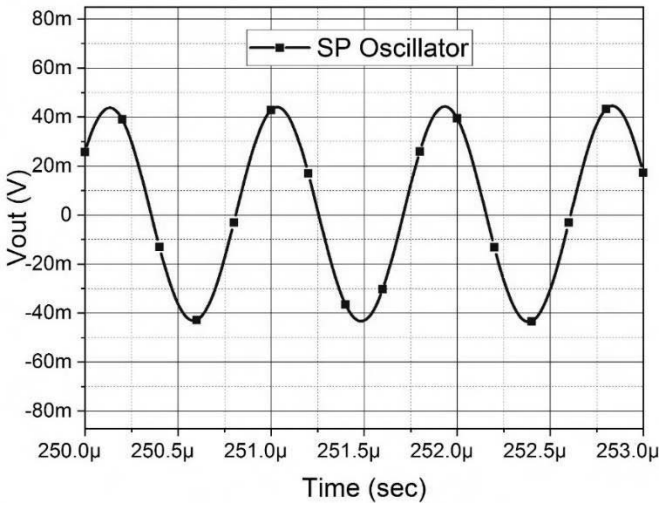
The Condition of oscillation (CO) and frequency of oscillation (FO) can be obtained as (6.4) and (6.5) respectively.

CO: $C_2 (R_1 + R_2) = C_1 g_m R_2 R_3$ (6.4)

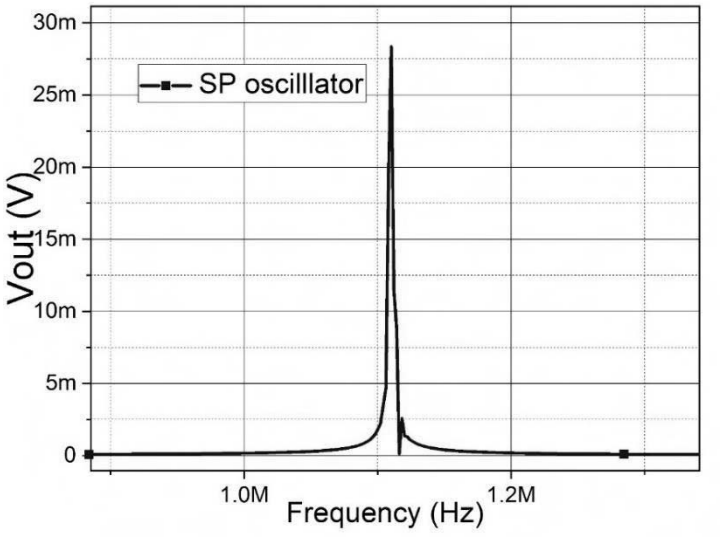
FO: $\omega_0 = \sqrt{\dfrac{g_m R_1}{C_1 C_2 R_3 (R_1 + R_2)}}$ (6.5)

6.3.1 Simulation Results

The proposed SP oscillator is verified through SPICE simulations using VDBA of Figure 2.4. The component values are taken as $R_1 = R_2 = 1$ kΩ, $R_3 = 1.5$ kΩ, $C_1 = C_2 = 100$ pF. The steady state output of proposed SP oscillator followed by its spectrum are shown in Figures 6.3 (a) and (b) respectively. The simulated frequency is observed as 1.05 MHz which is in close approximation to the theoretical value of 1.06MHz. The THD for the configuration is observed to be 3.5%.



(a)

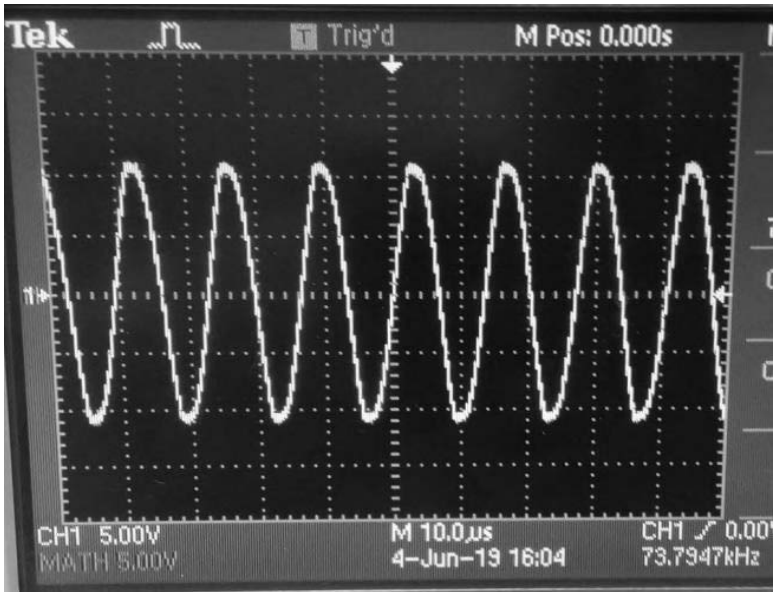


(b)

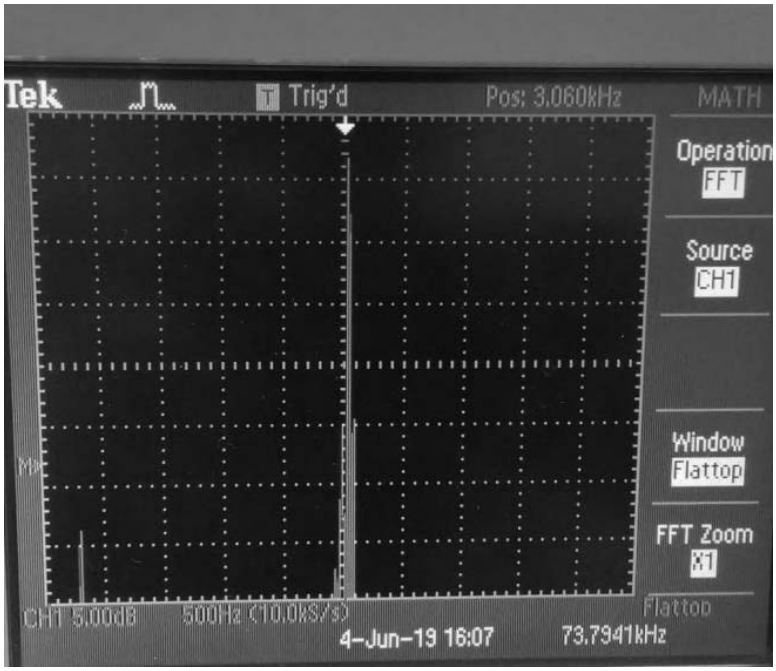
Figure 6.3 (a) Steady state output and (b) Spectrum of SP oscillator

6.3.2 Experimental Results

The experimental results of SP oscillator are obtained using CFOA based VDBA of Figure 2.13. The supply voltages are taken as ±12 V. The components are taken as R_1= R_2 =10 kΩ , R_3 = 20 kΩ, C_1 = C_2 =100 pF and g_m (=1/R_g) is set as 100 µS. The steady state output of proposed SP oscillator and its spectrum are shown in Figures 6.4 (a) and (b) respectively. The FO is observed as 74 kHz as against the theoretical value of 79 KHz.



(a)



(b)

Figure 6.4 (a) Steady state response and (b) Spectrum of SP oscillator

6.4 Quadrature Phase Oscillator (QPO)

Quadrature phase oscillators (QPO) provide two single frequency outputs which are in quadrature phase. QPOs are widely used in communication, instrumentation and power

electronics. Three QP oscillator topologies have been proposed in this thesis which have been described in following subsections.

6.4.1 Topology I

The proposed QP topology I is designed using DO-VDBA and consists of an inverting and non-inverting integrators in closed loop configuration as shown in Figure 6.5. The proposed topology uses two grounded capacitors only.

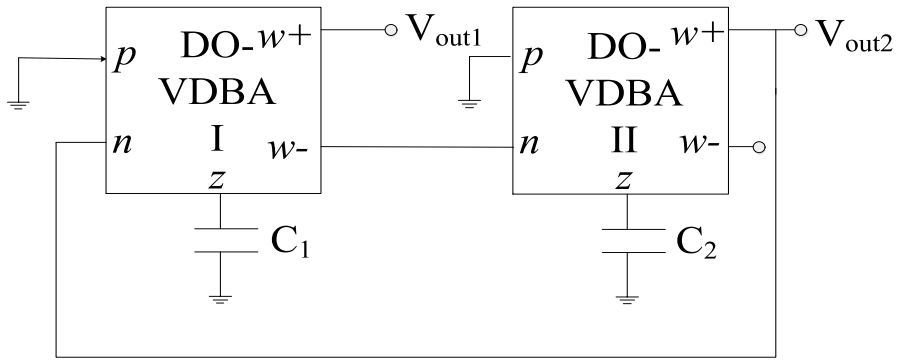


Figure 6.5 Proposed QP topology I

The CE of the proposed QP topology I is

$$\frac{C_1 C_2}{g_{m1} g_{m2}} s^2 + 1 = 0 \tag{6.6}$$

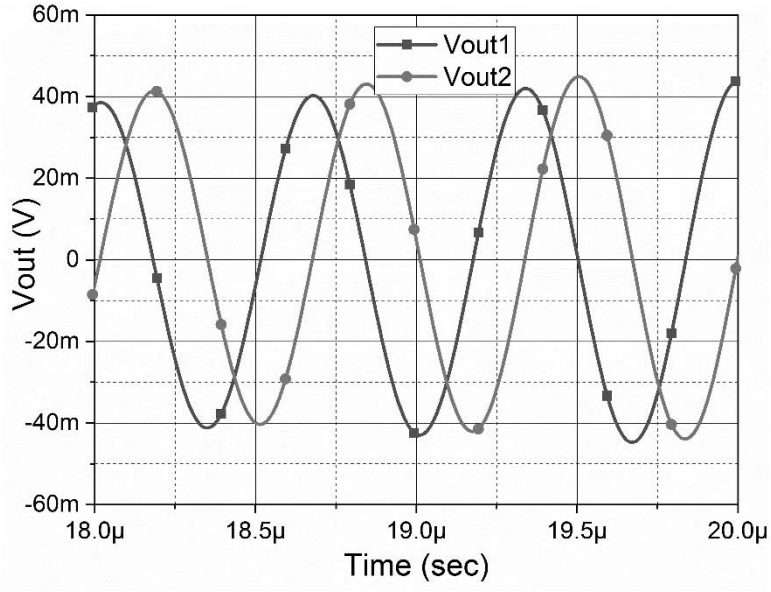
The FO from (6.6) can be determined as

$$\text{FO: } \omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{6.7}$$

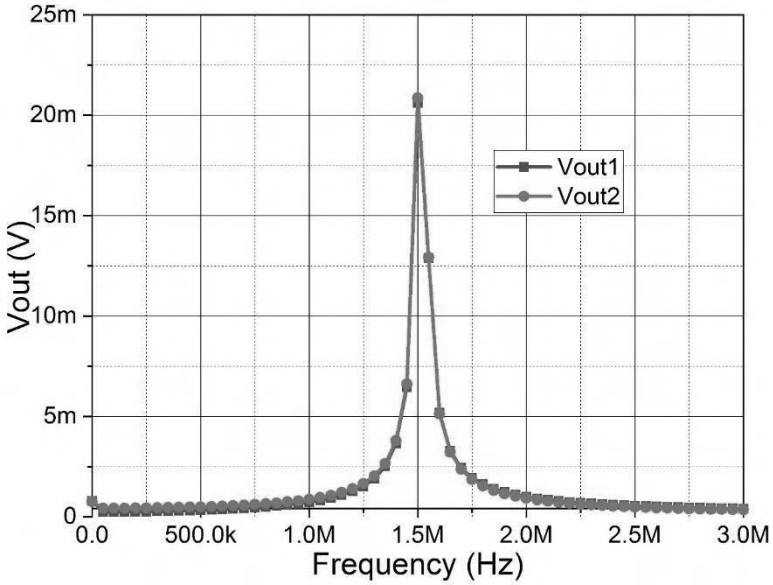
It is worth observing that the FO can be tuned by varying the biasing current thus enabling electronic tuning of the circuit.

6.4.1.1 Simulation Results

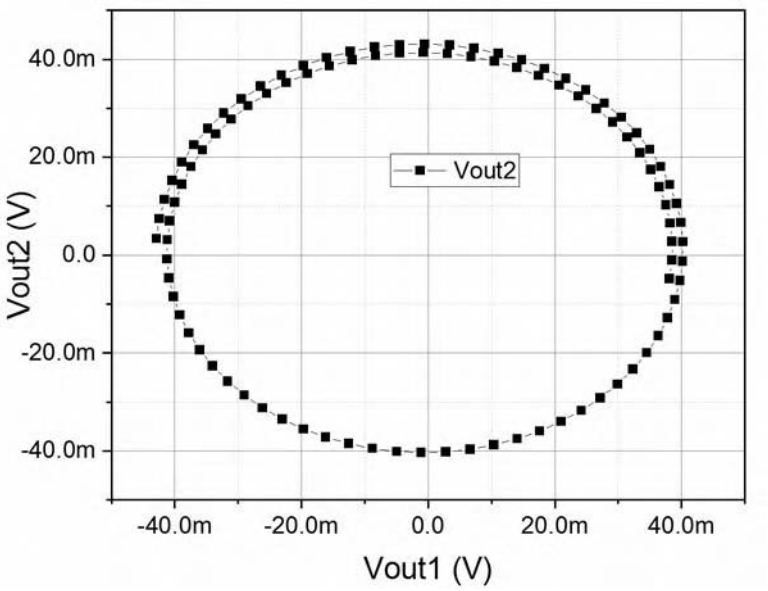
The proposed QP topology I is verified through SPICE simulations using DO-VDBA shown in Figure 2.8. The QP oscillator is designed for an FO of 1.59 MHz for which capacitance values are chosen as 20 pF each and the value of g_m is set as 200 µS. The simulated FO is observed to be 1.5 MHz against the theoretical value 1.59 MHz. The simulated steady state output and corresponding frequency spectrum are shown in Figures 6.6 (a) and (b) respectively. The Lissajous pattern is shown in Figure 6.6 (c) which confirms the quadrature nature of outputs. The THD for this configuration is found to be 3.2%.



(a)



(b)



(c)

Figure 6.6 (a) Steady state output, (b) Spectrum and (c) Lissajous pattern of QP topology I

6.4.2 Topology II

The QP topology II is designed by using a cascaded connection of proposed APF of Figure 4.9 (a) and a lossless inverting integrator. The proposed structure is shown in Figure 6.7.

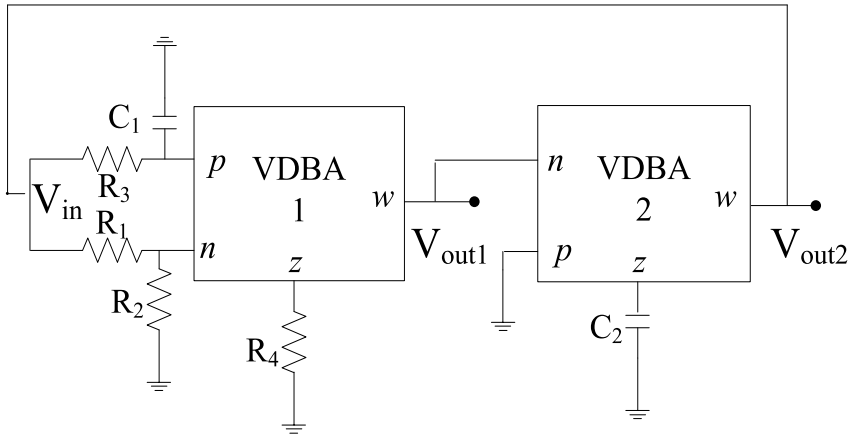


Figure 6.7 Proposed QP topology II

Considering g_mR_4=2, the CE of proposed topology II may be obtained as

$$s^2C^2R_3 + sC(1-g_mR_3) + g_m = 0 \tag{6.8}$$

From CE of the proposed circuit the CO and FO can be deduced as given by (6.9) and (6.10) respectively.

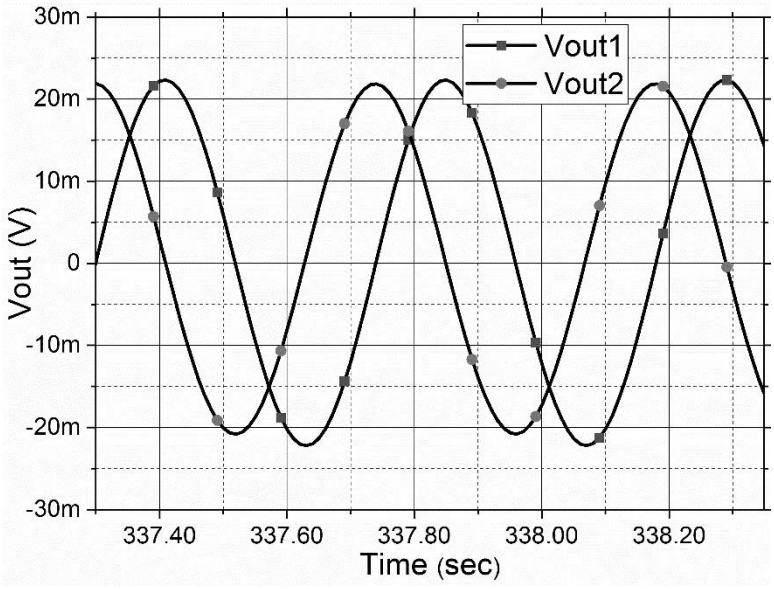
CO: $g_mR_3 = 1$ (6.9)

FO: $\omega_0 = \frac{1}{R_3C} = \frac{g_m}{C}$ (6.10)

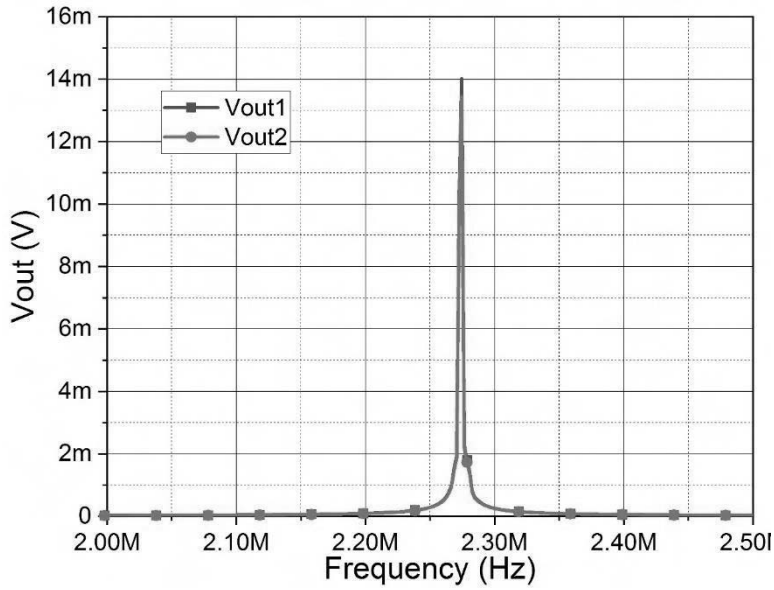
6.4.2.1 Simulation Results

The proposed QP topology II is verified through SPICE simulations using VDBA of Figure 2.4. The component values are R_1 = R_2 = 1 kΩ, R_3 = 0.72 kΩ, R_4 =1.5 kΩ, C_1 = C_2 =100 pF. The steady state output of proposed QP topology II followed by its spectrum are shown in Figures 6.8 (a) and (b) respectively. The simulated value of FO is observed to be 2.27 MHz against the theoretical value of 2.20 MHz and the THD is

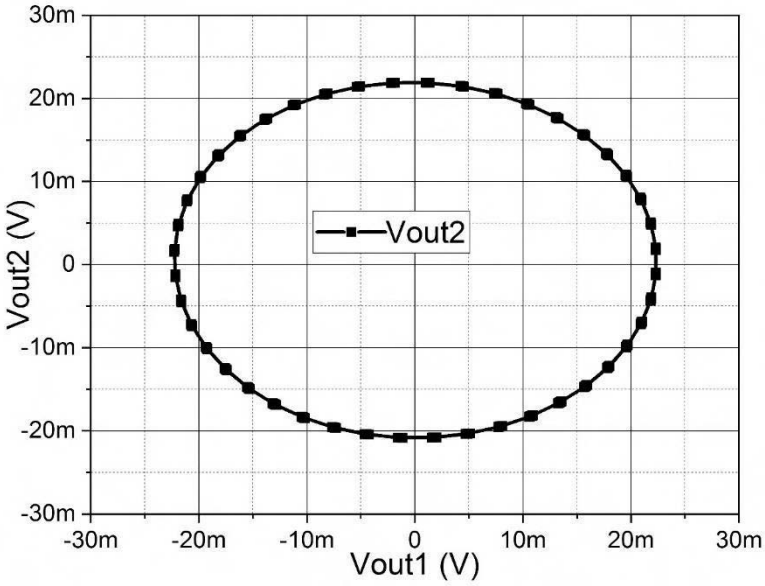
observed to be 3.1%. Figure 6.8(c) shows the Lissajous pattern of QP oscillator topology II which verifies the quadrature nature of V_{out1} and V_{out2}.



(a)



(b)

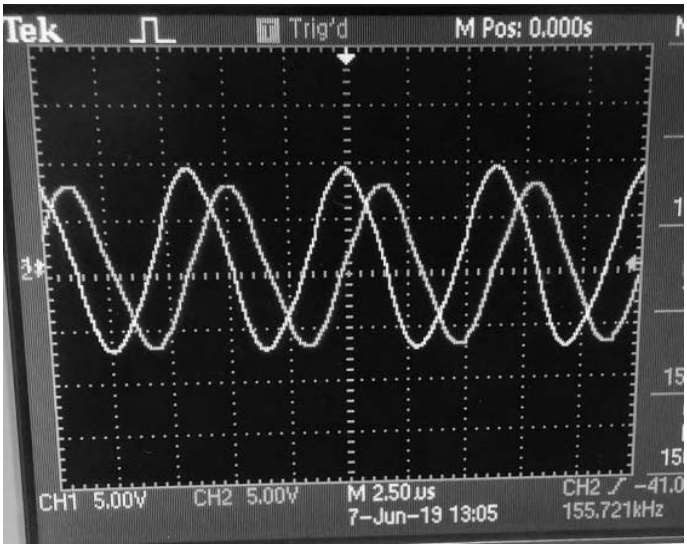


(c)

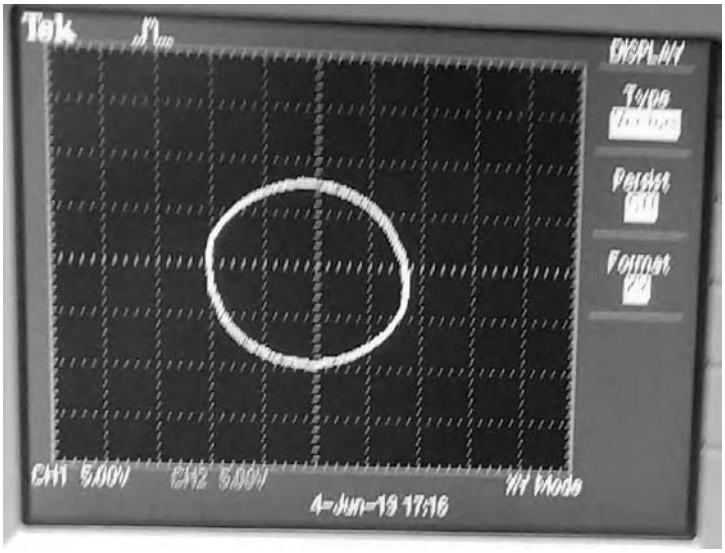
Figure 6.8 (a) Steady state output, (b) spectrum and (c) Lissajous pattern of QP topology II

6.4.2.2 Experiment Results

The experimental results of proposed QP topology II are obtained using CFOA based VDBA shown in Figure 2.13. The supply voltages are taken as ±12 V . The components, for a theoretical FO of 159 kHz, are chosen as $R_1 = R_2 = R_3 = 10$ kΩ , $R_4 = 22$ kΩ, $C_1 = C_2 = 100$ pF and g_m (=1/R_g) is set as 100 μS. The measured FO for this topology is 155.7 kHz which is quite close to the theoretical value. The steady state response of proposed structure is shown in Figure 6.9 (a). To show the quadrature nature of the outputs, Lissajous pattern is also obtained as depicted in Figure 6.9 (b).



(a)



(b)

Figure 6.9 (a) Steady state response and (b) Lisssajous pattern of QP topology II

6.4.3 Topology III

The QP topology III is designed using APFs proposed in chapter 4. This topology, as shown in Figure 6.10, is a close loop connection of an inverting and a non-inverting APF configurations.

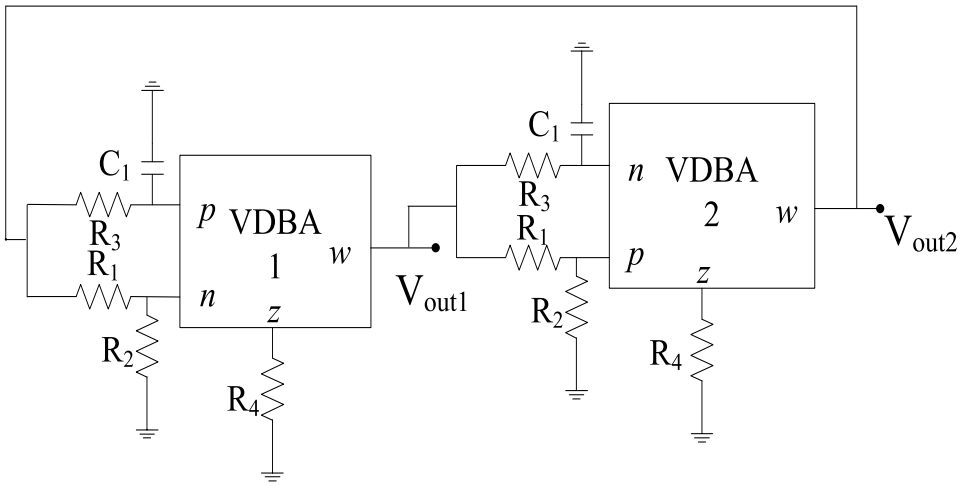


Figure 6.10 The QP Topology III

Considering g_mR_4= 2, the CE for the topology III is obtained as

$$s^2C^2R_3^2+1=0 \tag{6.11}$$

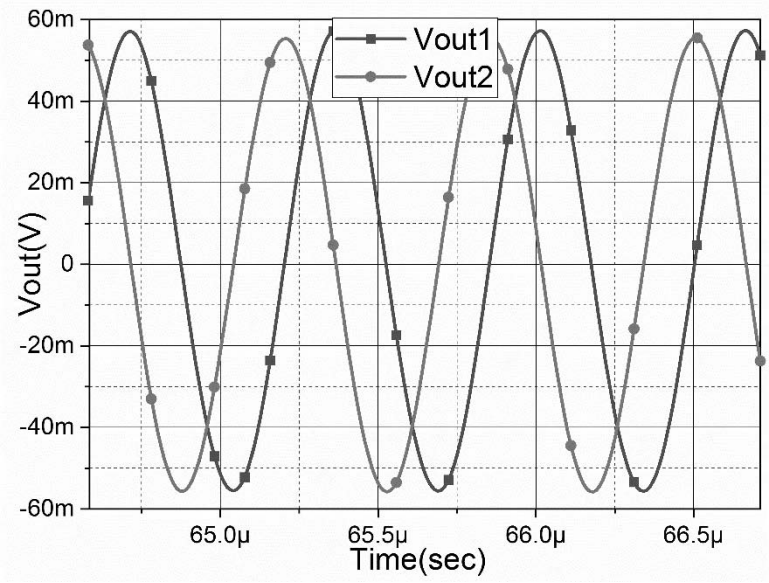
The FO can be written as

$$\text{FO: } \omega_0=\frac{1}{R_3C} \tag{6.12}$$

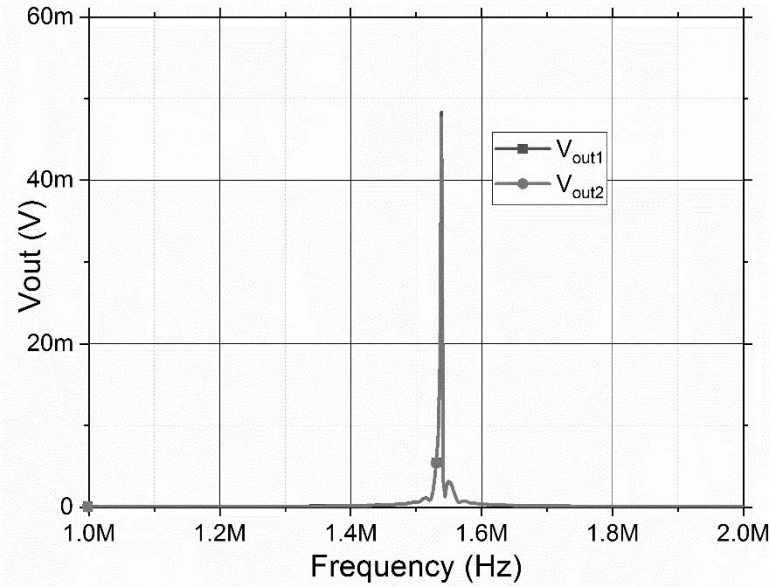
6.4.3.1 Simulation Results

The QP topology III is simulated through SPICE using VDBA shown in Figure 2.4. The QP topology III is simulated for component setting of R_1 = R_2 =R_3 = 1 kΩ, R_4 =1.5 kΩ, C_1 =100 pF for each APF. The steady state response of the proposed topology followed by its spectrum are shown in Figures 6.11 (a) and (b) respectively. The simulated FO is observed to be 1.54 MHz against the theoretical values of 1.59MHz. The Lissajous pattern is shown in Figure 6.11 (c) which confirms that V_{out2}

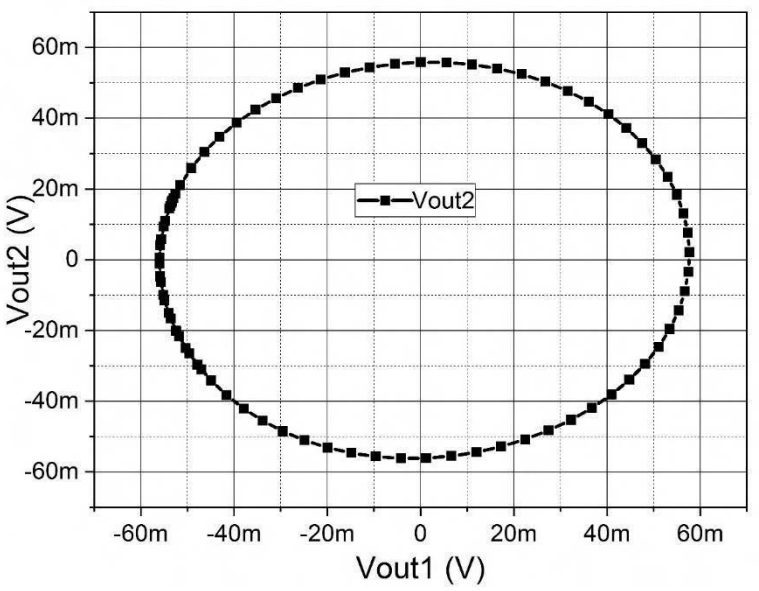
is 90°phase shifted as compared to V_{out1}. The THD for the configuration is found to be 4.3%.



(a)



(b)

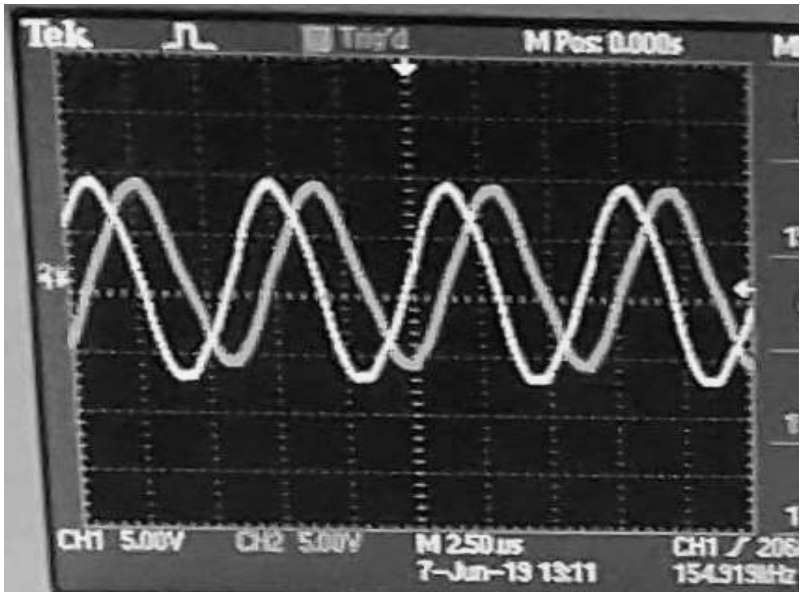


(c)

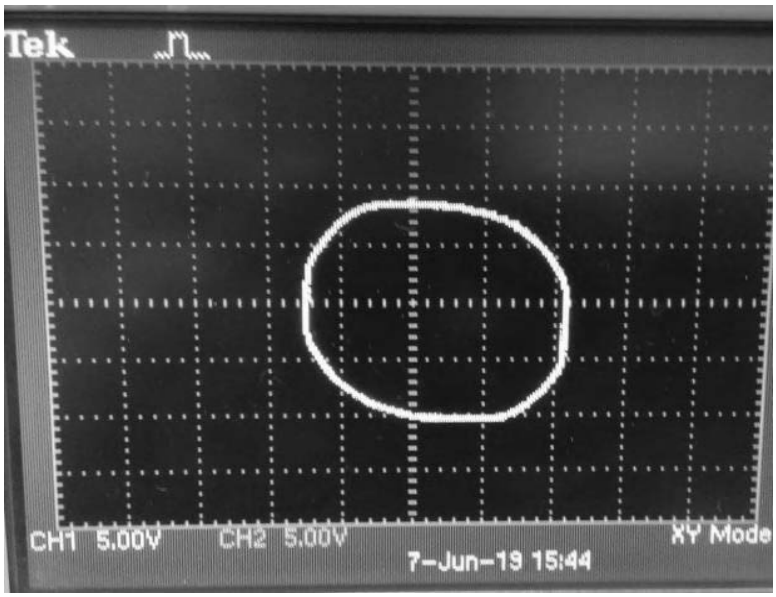
Figure 6.11 (a) Steady state output, (b) Spectrum and (c) Lissajous pattern of QP topology III

6.4.3.2 Experiment Results

The experimental results of QP topology III are obtained using CFOA based VDBA shown in Figure 2.13. The supply voltages are taken as ±12 V. The values of the components are taken as $R_1 = R_2 = R_3 = 10$ kΩ, $R_4 = 22$ kΩ , $g_m (=1/R_g) = 100$ μS and $C_1 = 100$ pF, for each APF. The FO measured is 154.9 kHz which is against the theoretical value of 159 kHz. The steady state response of the proposed QP topology III is shown in Figure 6.12 (a). To show the quadrature nature of the outputs, the lissajous pattern is also obtained in Figure 6.12 (b).



(a)



(b)

Figure 6.12 (a) Steady state response and (b) Lisssajous pattern of QP topology III

6.5 Multiphase Oscillator (MPO)

The multiphase oscillators (MPO) provide n (n≥3) outputs equally spaced in phase and find extensive applications in the field of communications and power electronics. These

MPOs can be designed using n (n≥3) cascaded phase shifting networks in closed loop to get n equally spaced phases. In general first order low pass filters or first order all pass filters are used as phase shifting networks. Two MPO topologies have been presented in this thesis which are based on generic approach of using all pass networks. The first topology utilizes (n+1) VDBAs to produce n phase oscillations whereas the second topology utilizes only n VDBAs to produce n phases. For the sake of easy comprehension the APF based generic approach has been presented first followed by proposed designs in following subsections.

6.5.1 Generic Approach

The MPO can be designed by cascading n APF stages and an inverter in the feedback network [48] as shown in Figures 6.13.

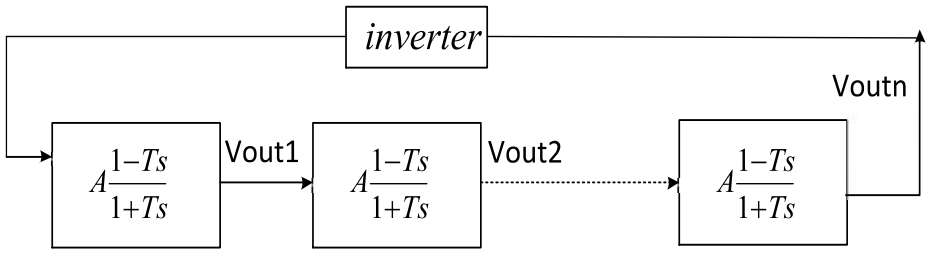


Figure 6.13 Generic Approach of MPO

Let G(s) represents the TF of an APF which can be written as

$$G(s) = A\left(\frac{1-Ts}{1+Ts}\right) \tag{6.13}$$

where 1/T represents the corner frequency of the APF.

Each APF provides an identical phase shift denoted by ϕ which can be written as

$$\phi = -2\tan^{-1}(\omega T)$$

(6.14)

Thus each APF can introduce a phase shift between 0 to 180° as frequency ω varies from 0 to ∞.

The loop gain L(s) for the block diagram of Figure 6.13 may be expressed as

$$L(s) = -[G(s)]^n$$

(6.15)

Substituting G(s) from (6.15), the L(s) may be rewritten as

$$L(s) = -A^n\left(\frac{1-Ts}{1+Ts}\right)^n$$

(6.16)

The Barkhausen criterion for producing sustained oscillations at ω_0,the loop gain and total phase may be expressed by (6.17)and (6.18) respectively.

$$L(j\omega_o) = -A^n\left(\frac{1-j\omega_o T}{1+j\omega_o T}\right)^n = 1$$

(6.17)

$$\angle L(j\omega_o) = n\phi + \pi = 2\pi$$

(6.18)

Thus the phase shift of each APF network is given by

$$\phi = \frac{\pi}{n}$$

(6.19)

The CO for the system may be obtained as

CO: A=1

(6.20)

Equating (6.14) and (6.19) the FO can be computed as

$$\text{FO}: \ \omega_o = \frac{1}{T}\tan\left(\frac{\pi}{2n}\right)$$

(6.21)

6.5.2 Topology I

The proposed MP topology I as shown Figure 6.14, is implemented using the APF proposed in chapter 4. It can produce n equally spaced phases where n can take any value ≥3.

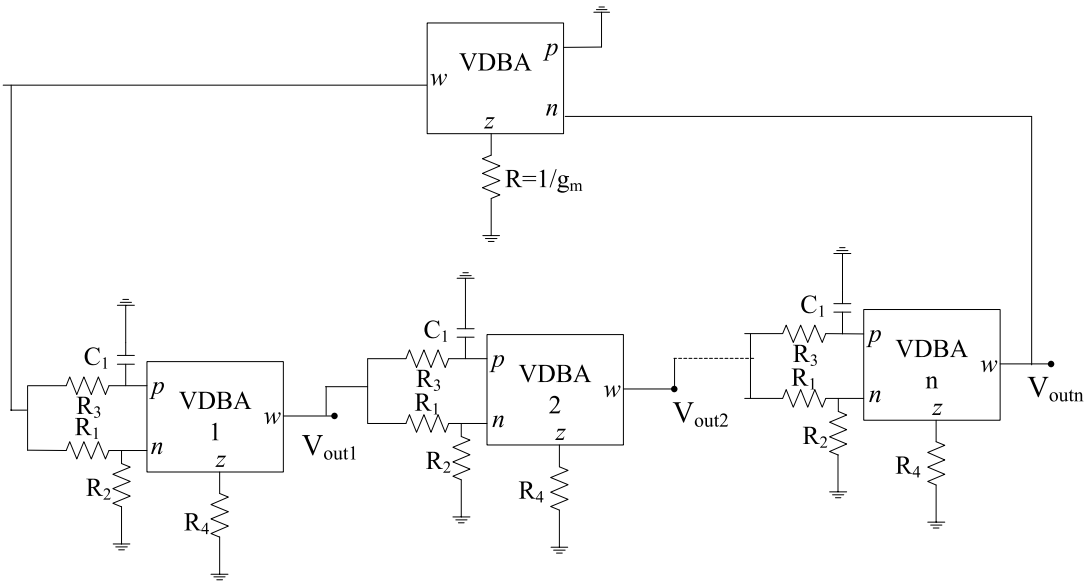


Figure 6.14 MP topology I

Using (6.20) and (6.21) the CO and FO for n=3 can be obtained as (6.22) and (6.23) respectively.

$$\text{CO}: \ g_m R_4 = 2$$

(6.22)

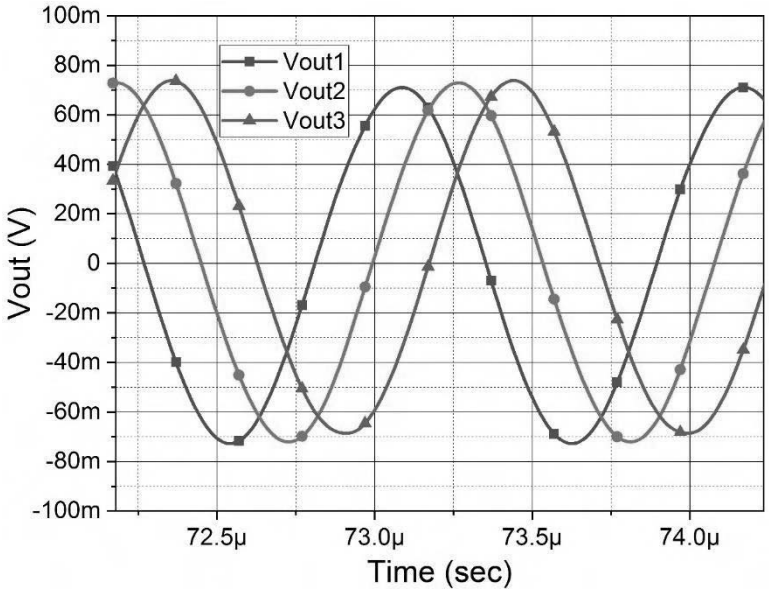
FO: $$\omega_o = \frac{1}{R_3 C}\tan\left(\frac{\pi}{6}\right)$$

(6.23)

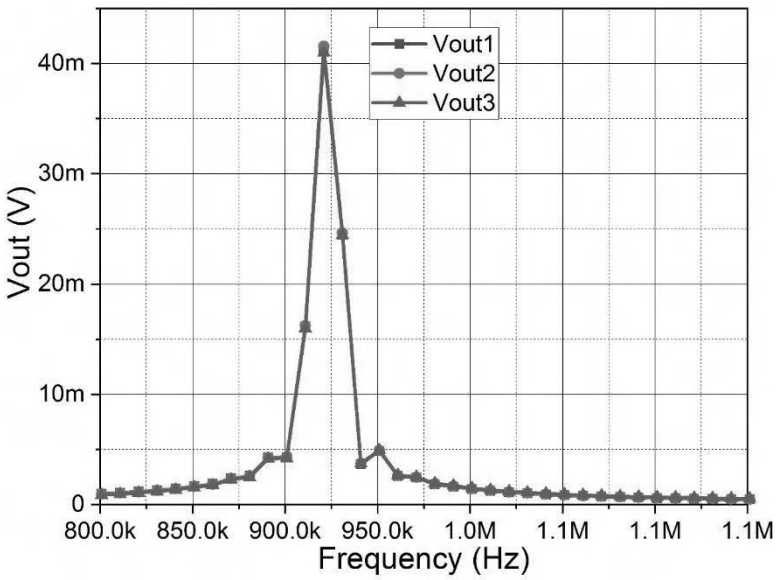
It is worth noting that the CO and FO for the proposed topology I can be controlled independently.

6.5.2.1 Simulation Results

The MP topology I is simulated for n=3 using resistors R_1, R_2 and R_3 = 1 kΩ with C_1 = 100 pF. The R_4 is kept 1.5 kΩ to keep the unity gain of APF. The Figure 6.15 (a) shows the steady state response and the corresponding spectrum is depicted in Figure 6.15 (b). The simulated FO is observed to be 918 kHz which is very close to the theoretical value of 920 kHz. The THD found was 1.3%.



(a)



(b)

Figure 6.15 (a) Steady state output and (b) Spectrum of MP topology I

6.5.2.2 Experiment Results

The experimental results are also obtained for the proposed topology using CFOA based VDBA shown in Figure 2.13. The supply voltages are taken as ±12 V. The components are taken as $R_1 = R_2 = R_3 = 10$ kΩ, $R_4 = 22$ kΩ, $C_1 = 100$ pF and g_m (=1/R_g) is set to 100 μS for each APF. The FO measured is 89.3 kHz which is in close approximation to the theoretical value of 92 kHz. The steady state response of proposed MP oscillator is shown in Figure 6.16.

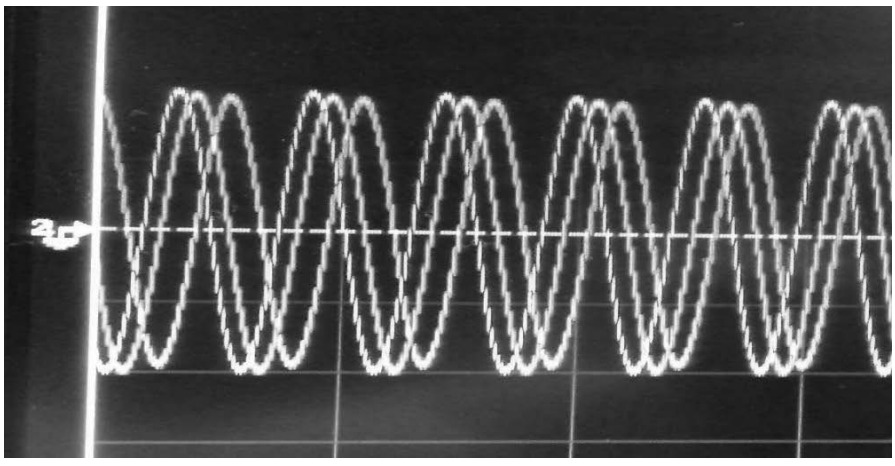


Figure 6.16 Steady state response of MSO

6.5.3 Topology II

The MPO topology II is designed using DO-VDBA based APF [82]. It consists of n stages of first order APF and the inverted output from w+ terminal of DO-VDBA N is fed back to the n terminal of DO-VDBA 1, as shown in Figure 6.17.

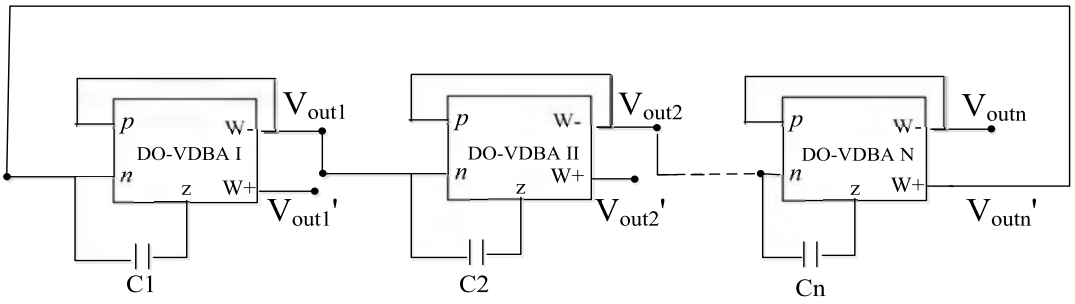


Figure 6.17 MP topology II.

The transfer function of each APF using DO-VDBA is given by

$$G(s) = \left(\frac{1 - sC/g_m}{1 + sC/g_m} \right)$$

(6.24)

The FO can be enumerated as

$$\omega_o = \frac{g_m}{C} \tan\left(\frac{\pi}{2n} \right)$$

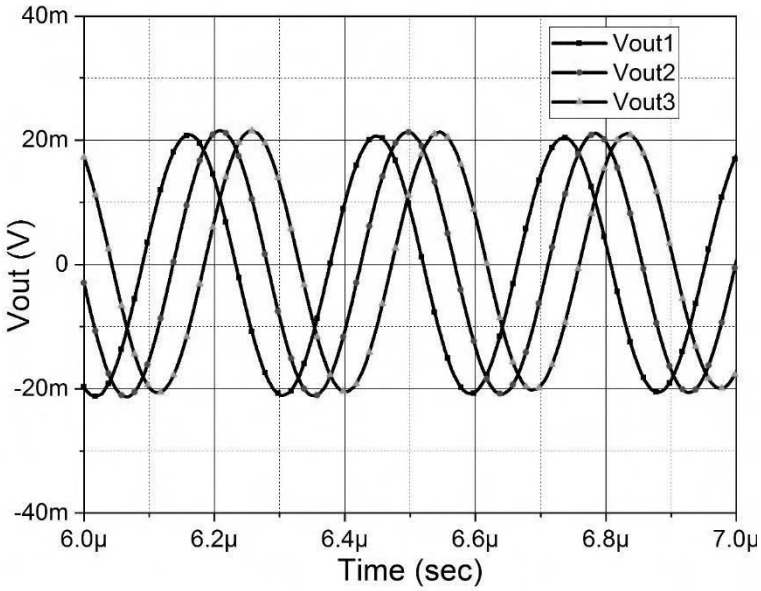
(6.25)

It may be observed from (6.25) that the FO can be varied either by changing the value of C or can be electronically tuned through g_m by varying the bias current.

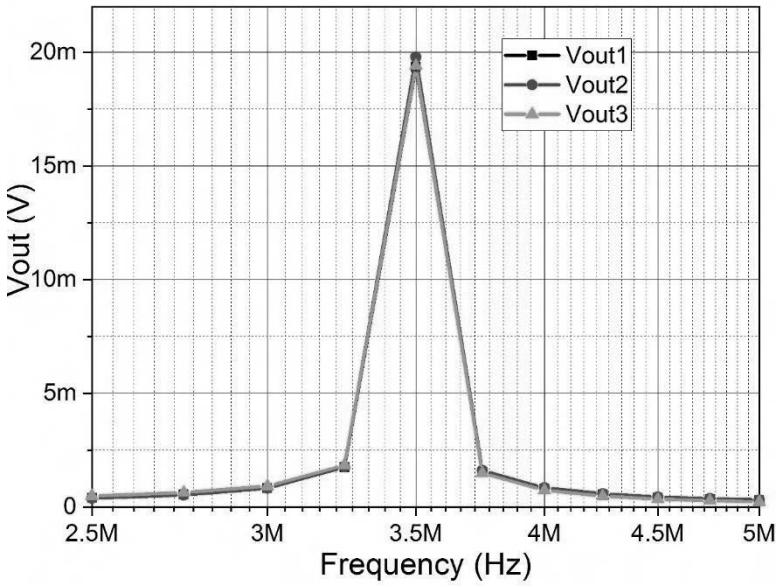
6.5.3.1 Simulation Results

The DO-VDBA of Figure 2.8 is used for simulations. A simulation setup is arranged to get the output of the MP oscillator topology II for n=3. The value of C is chosen to be 5 pF and the value of g_m is set to 200 µS. Figure 6.18 (a) shows the steady state output and Figure 6.18 (b) shows the frequency spectrum. The simulated FOs is found to be

3.5 MHz against the theoretical value is 3.6 MHz. The simulated THD is observed to be 0.78%.



(a)

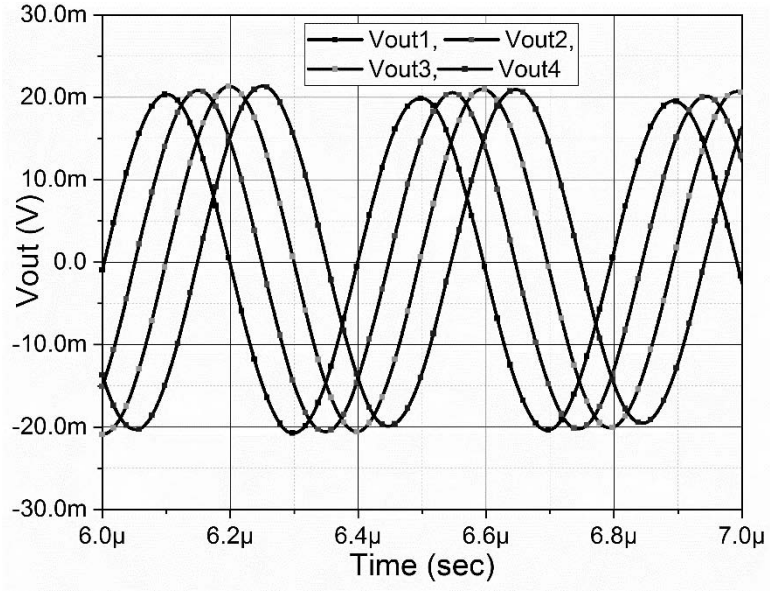


(b)

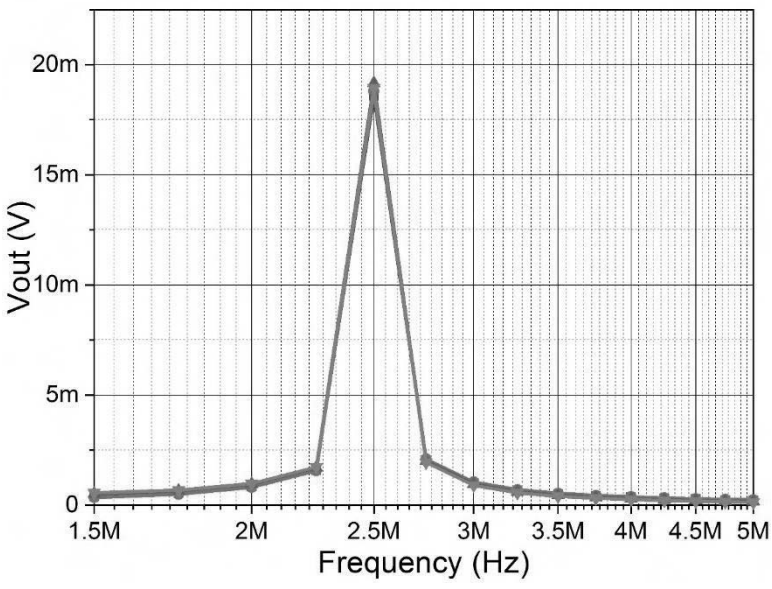
Figure 6.18 (a) Time domain output and (b) spectrum of 3 phase MP topology II

Next, the proposed MP topology II was simulated for n = 4 with C = 5pF and g_m = 200 µS. Figure 6.19 (a) depicts the steady state output with its frequency spectrum

in Figure 6.19 (b). The simulated FO is obtained as 2.5 MHz against the theoretical value of 2.6 MHz and the THD is found to be 1.19%.



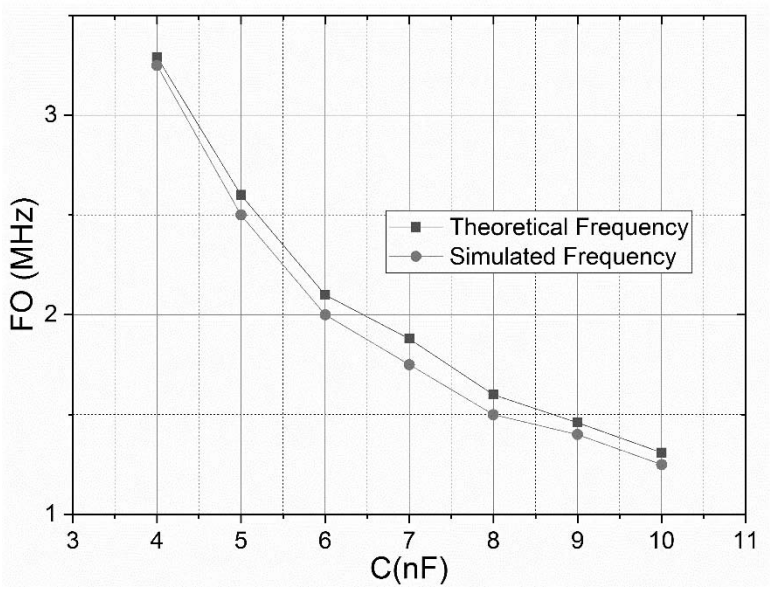
(a)



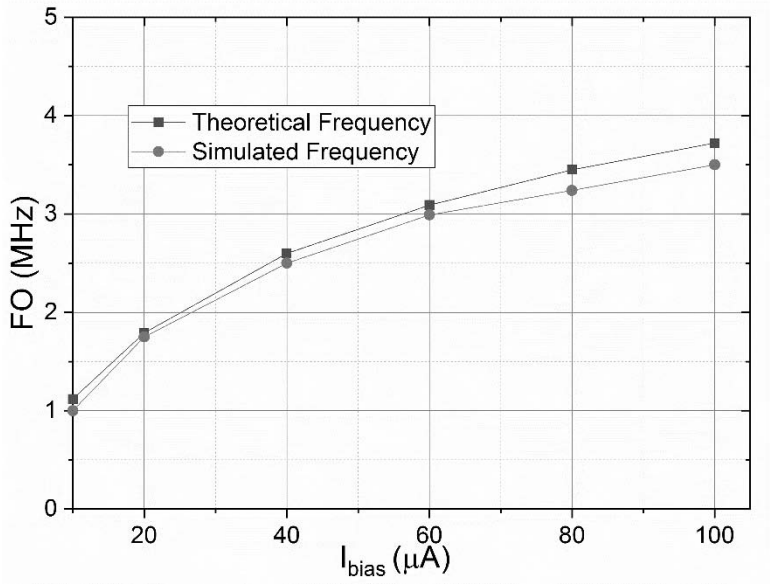
(b)

Figure 6.19 (a) Time domain output and (b) spectrum of 4 phase MP topology II

The values of FO can be controlled through capacitance or g_m of DO-VDBA which in turn be controlled through bias current. The frequency variation for n=4 through C is shown in Figure 6.20 (a) and by varying I_{bias} is shown in Figure 6.20 (b). It is observed that the value of FO closely follow the corresponding theoretical values.



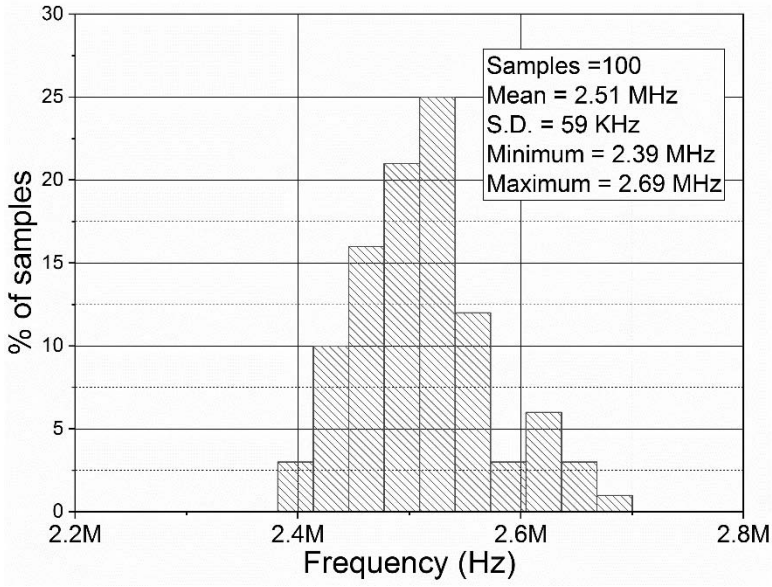
(a)



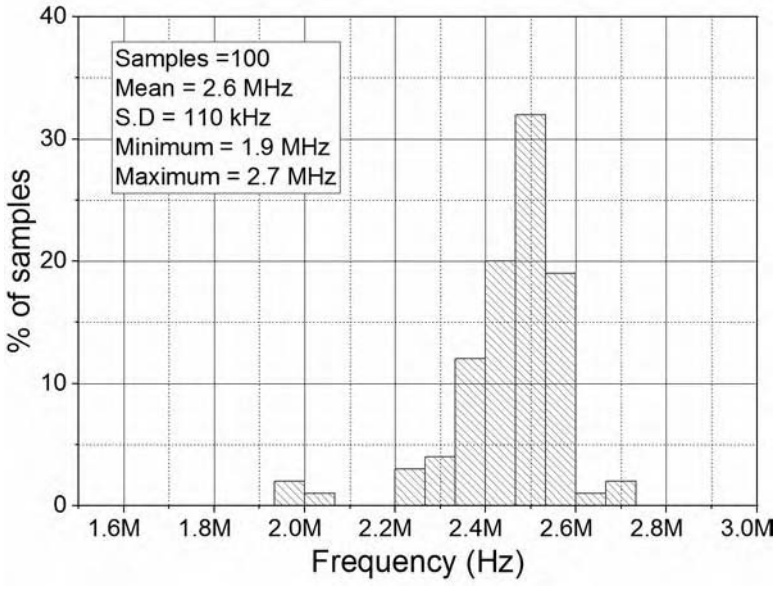
(b)

Figure 6.20 (a) FO Vs C and (b) FO Vs I_{bias}

To check the robustness of the proposed MP oscillator topology II, Monte Carlo simulations are performed and the resultant histograms have been shown in Figure 6.21. First, a 5% variation in the value of C is allowed, followed by 5% deviation in mobility (μ_o), threshold voltage (V_{TH}) and oxide thickness (t_{ox}) to investigate the effect of mismatch on the frequency of oscillation. The value of FO remains in approximation to its theoretical value of 2.6 MHz and hence almost unaffected by the variations.



(a)



(b)

Figure 6.21 Monte Carlo simulation results

6.6 Conclusion

This chapter is dedicated to the design of various sinusoidal oscillators using VDBA/DO-VDBA. A SP, three QP and two MP sinusoidal oscillators have been proposed. The workability of the proposed sinusoidal oscillators is confirmed from the simulations. The observed values of FOs are in close approximation to the theoretical values. In all the structures the FOs and COs are independently controllable. The proposed structures are also verified through experimental results wherein off the shelf IC AD844 is used to realize the VDBA.

This thesis presents the design and implementation of various analog signal processing circuits employing VDBA as an ABB. This chapter summarizes the major findings and conclusions of the study described in the various chapters of this thesis.

7.1 Summary of work done in this Thesis

The first chapter describes the background, motivation and the objectives of the thesis. A detailed literature review of various implementations of the VDBA and its variants followed by a review of the numerous signal processing applications designed using VDBA is presented next which helped in identifying the research gaps.

In chapter 2, the CMOS based VDBA and CMOS based DO-VDBA realization are studied and characterization is done through SPICE at 0.18 μm TSMC parameters. The CFOA based VDBA is also proposed in this chapter and characterized through SPICE simulation using IC AD844. These simulated structures set the foundation for the validation of all proposed designs. The VDBA and DO-VDBA are also studied in presence of non-idealities to give a base to study the behavior of various applications proposed in this thesis under non-ideal conditions. The MOS based resistor implementation is also included which may be used for chip area saving and to achieve electronic tuning in some of the proposed circuits.

In chapter 3, a low power high performance VDBA designed using DFVF cell is presented. The mathematical formulation of transconductance and buffer transfer ratio is carried out using low frequency small signal analysis. The proposed VDBA is characterized through pre and post layout simulations using Cadence Virtuoso at GPDK 0.18 μm CMOS technology node. A wide range of transconductance variation is obtained by varying bias current. A resistive compensation technique is used to

compensate the peak in frequency response of the buffer and detailed mathematical formulation of the same is also presented. The PVT and Monte Carlo analyses have been presented to show the effect of parameter variations and transistor aspect ratio variations.

Linear applications of VDBA are presented in Chapter 4. An instrumentation amplifier is presented first which is followed by designs of electronic filters. The proposed IA consists of a VDBA and a single grounded resistor. A detailed theoretical analysis followed by noise analysis is carried out. The gain of the proposed amplifier can be electronically tuned through transconductance. The performance of the circuit is confirmed through SPICE simulations. The proposed IA possesses high CMRR and wide bandwidth with quite low value of % THD.

In electronic filters, three applications namely (i) a first order APF (ii) a SISO multifunctional filter and (iii) a MISO universal filter are proposed. An APF in inverting/non-inverting configuration using a VDBA has been proposed. The proposed circuit uses four resistors and a grounded capacitor. The proposed first order APF provides voltage output at low impedance with electronically tunable voltage gain. A second order VM multifunction generalized filter topology employing single VDBA is presented next. LPF, HPF and BPF configurations are synthesized with proper selection of admittance. The proposed topology is a suitable choice for high quality factor implementation. The third filter topology is a MISO universal biquad filter designed using two VDBAs, two capacitors and a grounded resistor. The pole frequency of the proposed structure can be controlled independently of quality factor. The Monte Carlo and PVT analyses are also performed using simulations and found that proposed applications possess low sensitivities. Workability of the first two filter structures has been verified through SPICE simulations. The MISO topology is demonstrated through

pre and post layout simulations are obtained using Cadence Virtuoso with 0.18 μm GPDK parameters. The theoretical and the simulated results of all the applications proposed are observed to be in close agreement.

In Chapter 5, a FQAM based on quarter square algebraic identity is proposed. The structure is suitable for integration as passive resistor may suitably be implemented using MOSFETs. THD is found to be well below 3%. Applications like amplitude modulator and rectifier are designed using the proposed structure to show its applicability. Low power squaring and square-rooting circuits using single VDBA are also proposed in this chapter. The proposed structures facilitate easy cascading as their output voltages are available at low impedance terminals. The workability of the proposed applications are established using pre and post layout simulations using Cadence Virtuoso. The PVT analyses are also carried out for proposed structures. The power consumption of proposed structures is quite low making them suitable for low power applications

Chapter 6 is dedicated to the design of various sinusoidal oscillators using VDBA/DO-VDBA. A SP, three QP and two MP sinusoidal oscillators have been proposed. In all the structures the FOs and COs are independently controllable. The workability of the proposed sinusoidal oscillators is demonstrated using simulations. The observed values of FOs are in close approximation to the theoretical values. The proposed structures are also verified through experimental results wherein the VDBA is realized with off the shelf IC AD844. Table 7.1 compiles the work presented in this thesis.

Table 7.1 Summary of work presented in the thesis

Chapter	Structure	No. of ABB	Analysis	Ind. Tuning	Layout	Experimental
1	Introduction and Background of Analog Building Blocks and Literature Review					
2	Basics VDBA and DO-VDBA and its Characteristics					
	Proposed VDBA using CFOA (AD844)					
3	VDBA	1	Monte Carlo, PVT	--	Yes	No
4 Linear Applications	Instrumentation Amplifier	1 VDBA	Non-ideality, Monte Carlo, Noise Analysis	--	No	No
	First order APF	1VDBA	Non-ideality, Sensitivity, Monte Carlo	Yes	No	Yes
	SISO Multifunction Filter	1 VDBA		Yes	No	No
	MISO universal Filter	2 VDBA		Yes	Yes	No
5 Non-Linear Applications	Multiplier	2 DO-VDBA	Non-ideality, Monte Carlo, PVT	--	No	No
	Squaring Circuit	1 VDBA		--	Yes	No
	Square rooting Circuit	1 VDBA		--	Yes	No
6 Signal Generators	SPO	1 VDBA	--	Yes	No	Yes
	QPO topology I	2 DO-VDBA		Yes	No	No
	QPO topology II	2 VDBAs		Yes	No	Yes
	QPO topology III	2 VDBA		Yes	No	Yes
	MPO topology I	N+1 VDBA		Yes	No	Yes
	MPO topology II	N VDBA	Monte Carlo	Yes	No	No
7	Conclusion and Future Scope					

7.2 Future Scope

This era of portable electronic equipments has motivated the researchers to develop low voltage high performance mixed-mode signal processing circuits. The CM processing has evolved as a favorable solution for the development of such circuits. An extensive literature review suggests that various CM ABB have been proposed in the past and VDBA is one of recent origin. These blocks are characterized with different port relations and impedance properties. The systems to be designed may impose specific requirements depending upon the application and on the basis of these impositions,

appropriate ABB needs to be selected. The VDBA is the most promising choice for voltage mode and transconductance mode applications as the VDBA has two output nodes; one current terminal with high impedance and a low impedance voltage output terminal, which provides design flexibility.

Research is an ongoing process and new explorations and propositions are inevitable. It is well known that power and chip area budgeting are the prime concern of modern VLSI industry which gives an insight for future work which can be addressed immediately such as

-The implementation of the VDBA or other ABBs using technologies like FinFET / CNTFET etc to achieve the low supply voltage requirements and hence, lower consumption of power.

-The designs need to be optimized for active and passive elements with usage of grounded elements.

-Exploring more of MOS-C structures for chip area saving.

To sum up, still a lot can be done in analog signal processing to achieve high performance of active elements for further research. [148]

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