PROJECT REPORT ON

COMPARISON OF VARIOUS ADDER IMPLEMENTATIONS ON CMOS 90nm TECHNOLOGY USING CADENCE VIRTUOSO AND LTspice

SUBMITTED BY

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Submitted for the Major Project –II Presentation in Fourth Semester for the Degree Of Masters of Technology (2018-2020) in VLSI Design and Embedded Systems

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CERTIFICATE

This is to certify that, Mr. Suman Kumar has completed his Major project- II entitled "COMPARISON OF VARIOUS ADDER IMPLEMENTATIONS ON CMOS 90nm TECHNOLOGY USING CADENCE VIRTUOSO AND LTspice" for partial fulfilment of the requirements for the award of the Master of Technology degree in VLSI Design and Embedded Systems from Delhi Technological University, New Delhi under my supervision during the academic session 2018-2020.

APPROVAL FOR SUBMISSION

Prof. Dinesh Kumar
Professor

Dept. of ECE

ABSTRACT

Adders form an almost imperative component of every contemporary integrated circuit. Since mobile industry is rapidly growing thus speed, area and power efficient arithmetic units are required to satisfy the market needs. The prerequisite of the adder is that it is predominantly fast and secondarily efficient in chip area. Several types of adders are available in practice; each type is used for meticulous purpose based on their performance and features. In this paper, the multiplexer based full adder is implemented in the design of various adders. These adders are compared on the basis of their execution parameters i.e. delay and power distribution by using conventional full adder, Gate level design full adder and a multiplexer based full adder.

Adders play a key role in arithmetical operations and used in computational devices. We have proposed a design of four different adders, which relatively requires power and delay. Additionally the proposed design is more efficient in power dissipation. Even though a full adder is being designed with efficient power dissipation but there is always the scope of improvement in terms of reduction in power dissipation. To overcome this issue we have designed different adders and compare the power dissipation of different adders and reached to optimum solution from the alternatives. we have compared various limits for the proposed and existing mechanisms using different tools.

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1) INTRODUCTION

A full adder is used for computation of addition of numbers. This is a digital logic circuit manufactured using semiconductors and constitutes in the part of integrated circuits. In computers or other types of processors, it is utilized to calculate addresses. In the ALU it is used as a basic component. It can be built for many numerical representations like excess-3 or binary coded decimal. Adders are categorized into two types based on number of input bits: half-adder and full-adder.

The half-adder circuit has two inputs: 'A' and 'B', which add two input digits and generate a carry and sum. The full-adder circuit has three inputs: 'A', 'B' and 'C', which add the three input numbers and generate a carry and sum.

Half Adder Function :

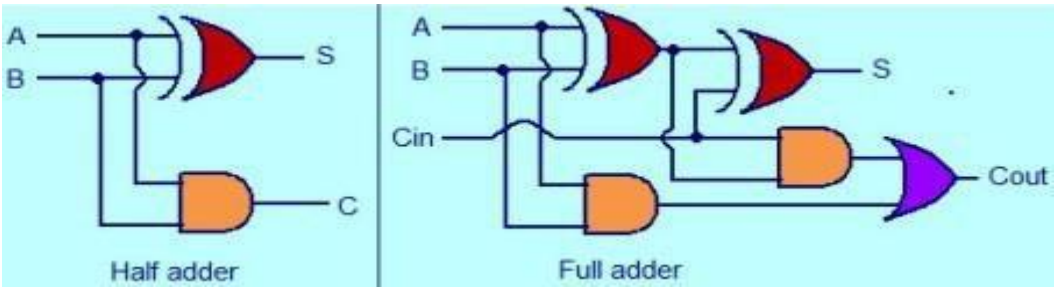


Figure i. Half Adder and Full Adder

0+0 =0.

0+1 =1.

1+0 =1.

1+1 = 10.

Single-bit additions is used and reflect the additions. For 1+1 = 10, the summust be re-written as a two bit output. Additions for different combinations of bits can be written as

0+0=00.

0+1=01.

1+0=01.

1+1=10.

The result coming‘1’from ‘10’ is carry-out. ‘SUM’ is the “xor” output of single bit combinations and ‘CARRY’ is the carry-out.

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table i. Half Adder & Full Adder Truth Table

Since it has been figured out from the expression that single bit adder can be easily implemented with the use of ‘XOR’ Gate for ‘SUM’ as result and an ‘AND’ Gate for the ‘Carry’ result. If we are required to sum, 2 eight-bit bytes together, this task can be accomplished with the aid of different full-adder logic. The half-adder is beneficial when we are required to sum one binary digit numbers. When we want to make a three binary digit

adder or if we decide to construct a four binary digit adder, do it again. The functionality of adder computation would be rapid, but development time is cumbersome.

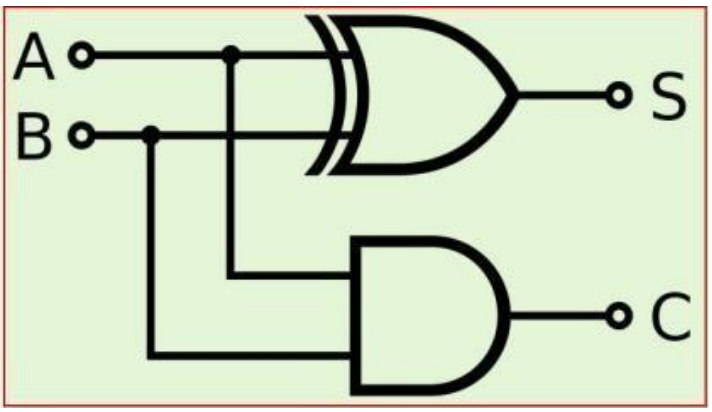


Figure ii. Half Adder Logic Circuit

Full Adder: Full adder is more complex to configure in comparison with a half-adder. It can be distinguished based on the number of inputs as the full adder consists of three inputs and two outputs, while half adder consists of only two inputs and two outputs. To deign full-adder logic, we bind 8 full-adder in conjunction to construct a byte-wide adder. We transfer the carry out bit from one adder to the next adder as carry in.

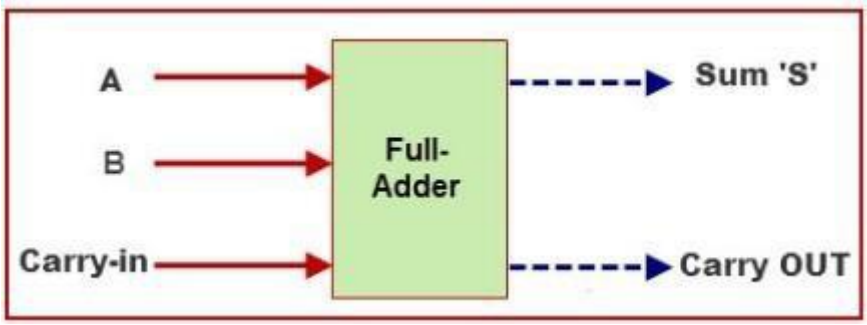


Figure iii.Full Adder Circuit

a) Basic Gates:

AND GATE:

Logic Symbol of 2 inputs AND Gate with A and B & output as out.

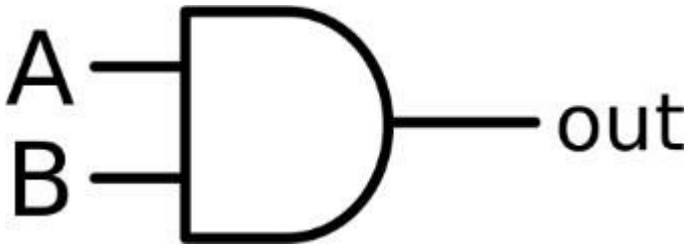


Figure iv. AND Gate Symbol

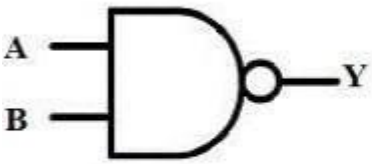
Truth table of AND gate here output is taken F Boolean Expression.:-

(F = A * B = A.B).

Inputs		Output
A	B	F=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Table ii. Truth Table AND Gate

NAND GATE:



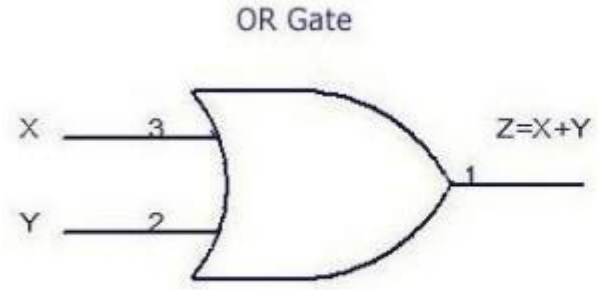
Inputs		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure v. Nand Gate Symbol and Truth Table

Boolean Expression of NAND Gate: Y=NOT(A AND B) =NOT(A * B)

OR GATE:

Truth table and logic diagram of OR Gate



TRUTH TABLE

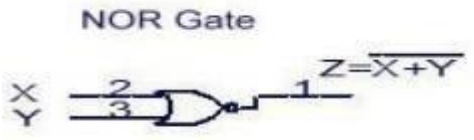
INPUTS		OUTPUT
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

Figure vi. Gate Symbol and Truth Table

Boolean expression for OR Gate Z=X+Y

NOR GATE:

Truth table and logic diagram of NOR Gate



TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

Figure vii. NOR Gate Symbol and Truth Table

Boolean expression of NOR Gate Z=NOT(X OR Y) =NOT(X+Y)

b) Power Dissipation Using Simulation Results:

AND GATE

Circuit diagram of AND Gate

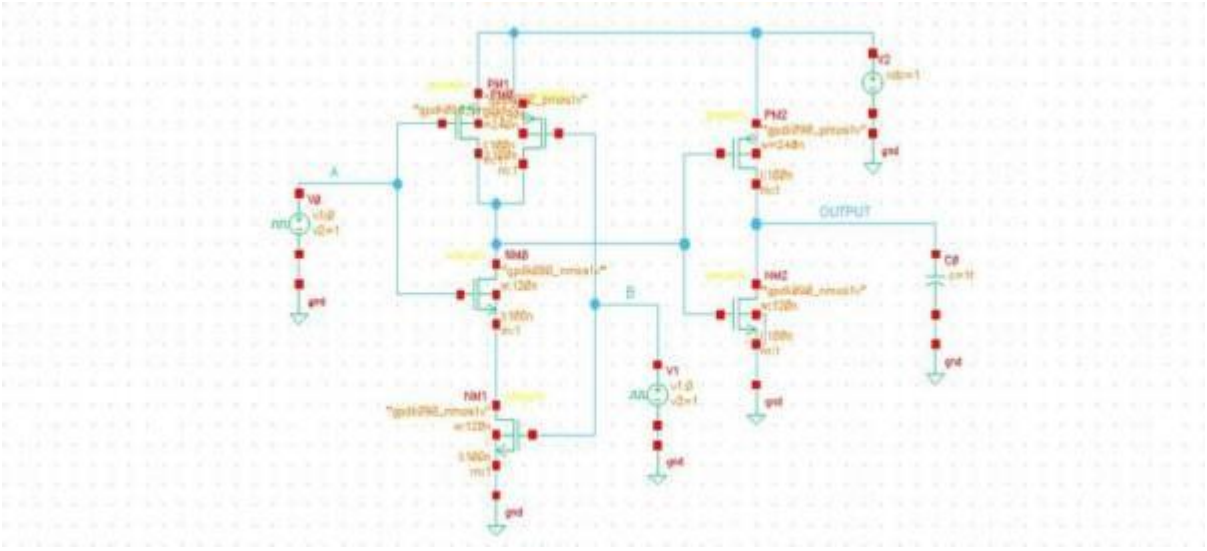


Figure viii. AND Gate circuit

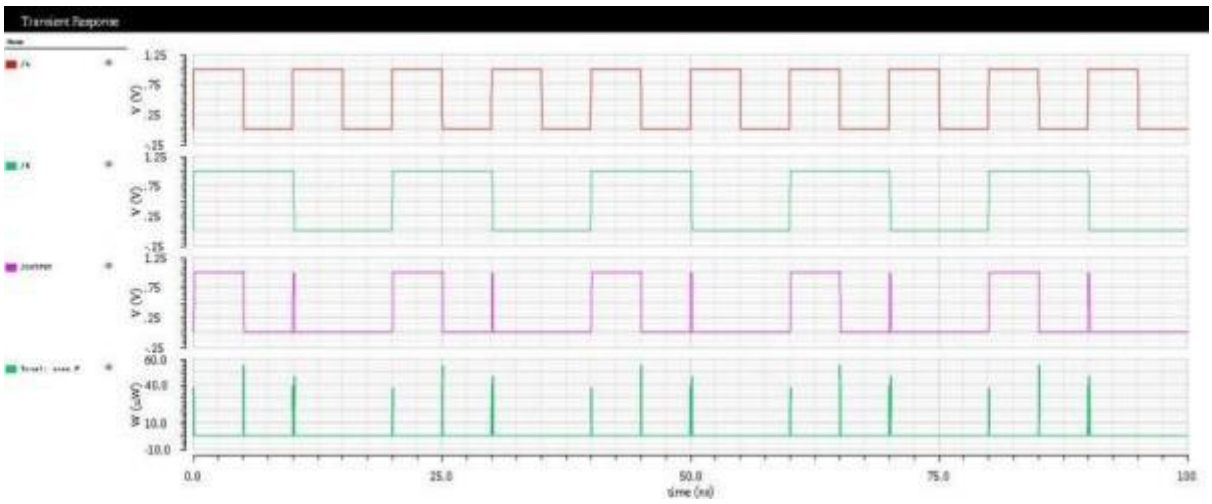


Figure ix. AND Gate Power Dissipation

Power Dissipation and functionality of AND Gate in graph Shown below

From the graph above we can say that power is dissipated mostly when there is transition at output of AND Gate from 0 to 1 or 1 to 0.

NAND GATE:

Circuit diagram of NAND Gate

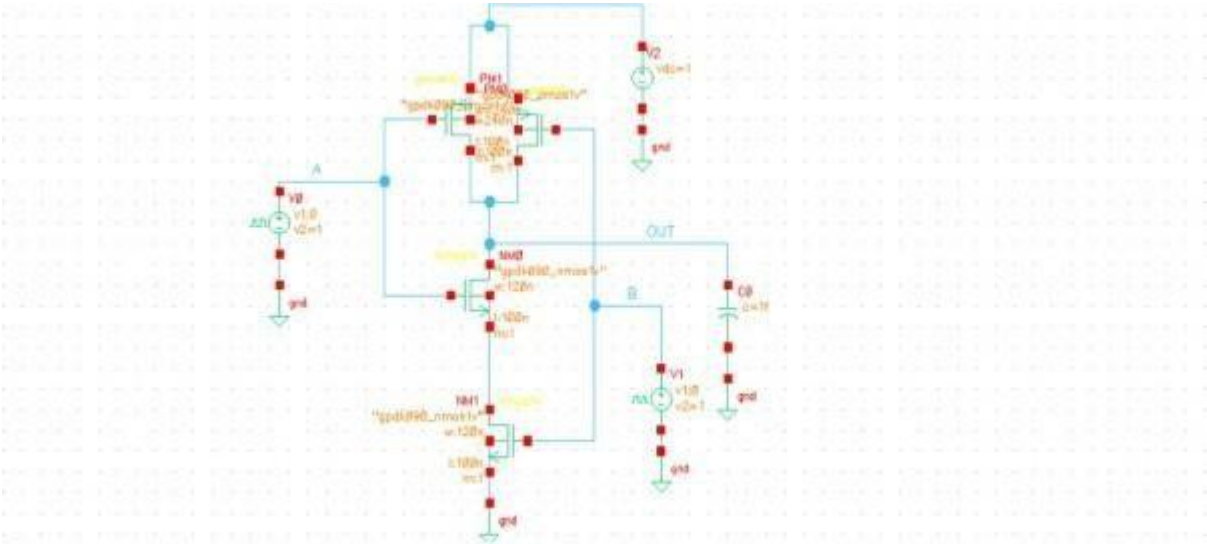


Figure x.NAND Gate Circuit

Power Dissipation and functionality of NAND Gate in graph Shown below:

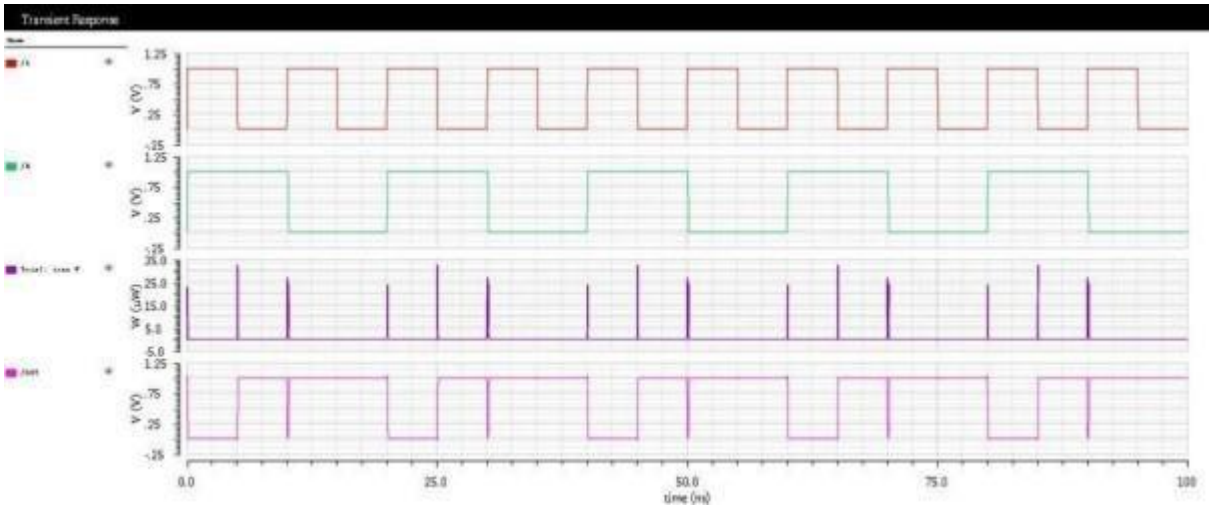


Figure xi. NAND Gate Power Dissipation

From the graph above we can say that power is dissipated mostly when there is transition at output of NAND Gate from 0 to 1 or 1 to 0.

OR GATE:

Circuit diagram of OR Gate

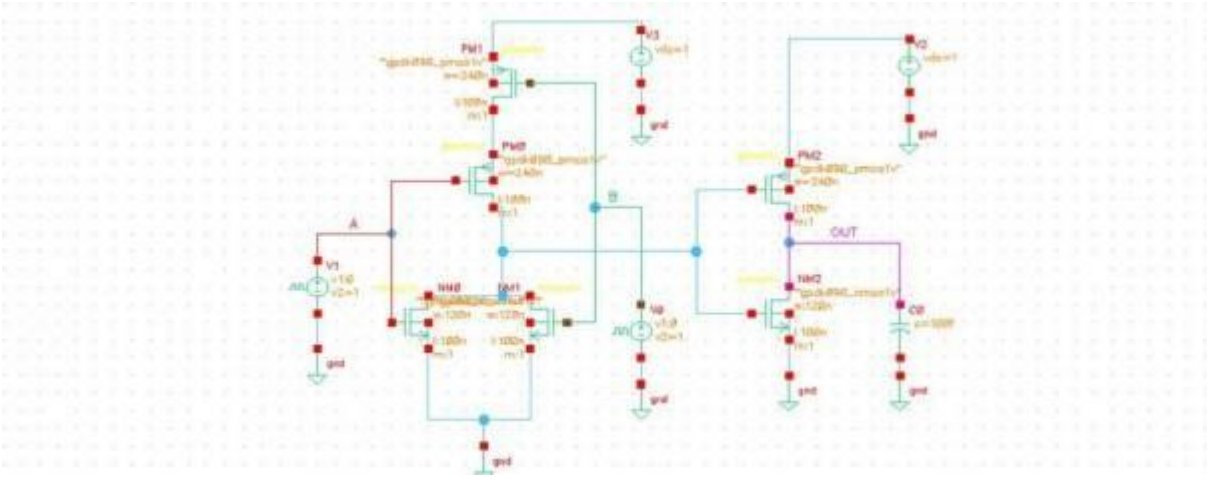


Figure xii. OR Gate Circuit

Power Dissipation and functionality of OR Gate in graph Shown below:

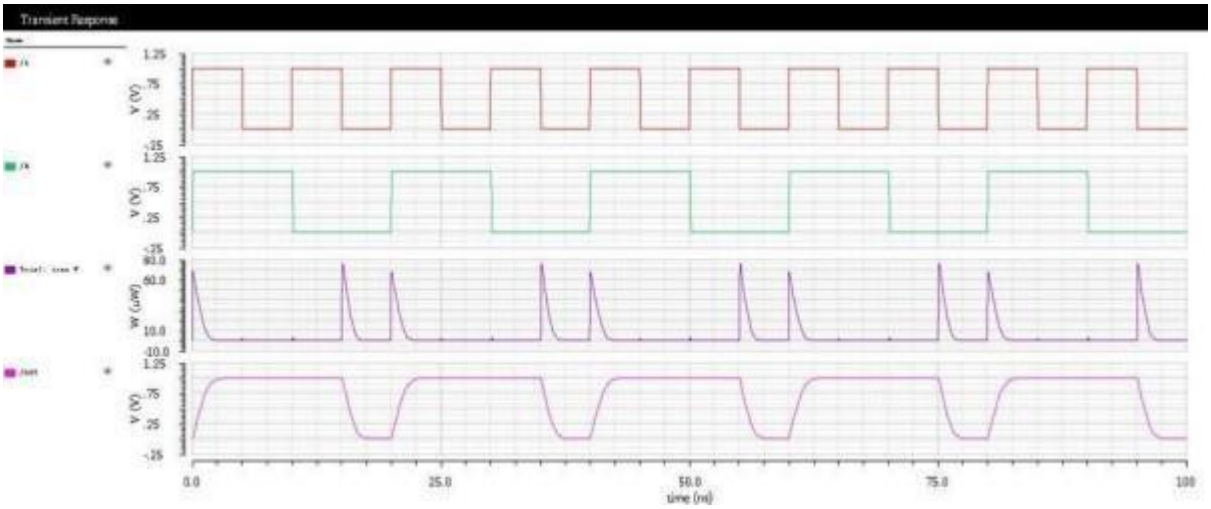


Figure xiii. OR Gate Power Dissipation

From the graph above we can say that power is dissipated mostly when there is transition at output of OR Gate from 0 to 1 or 1 to 0.

NOR GATE:

Circuit diagram of NOR Gate

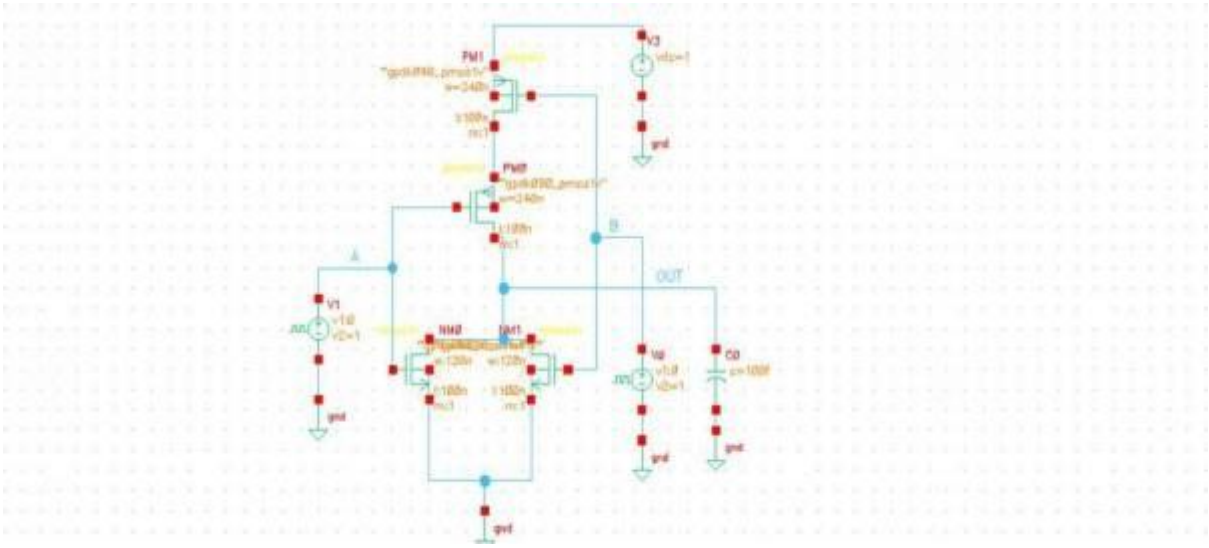


Figure xiv.NOR Gate Circuit

Power Dissipation and functionality of NOR Gate in graph Shown below

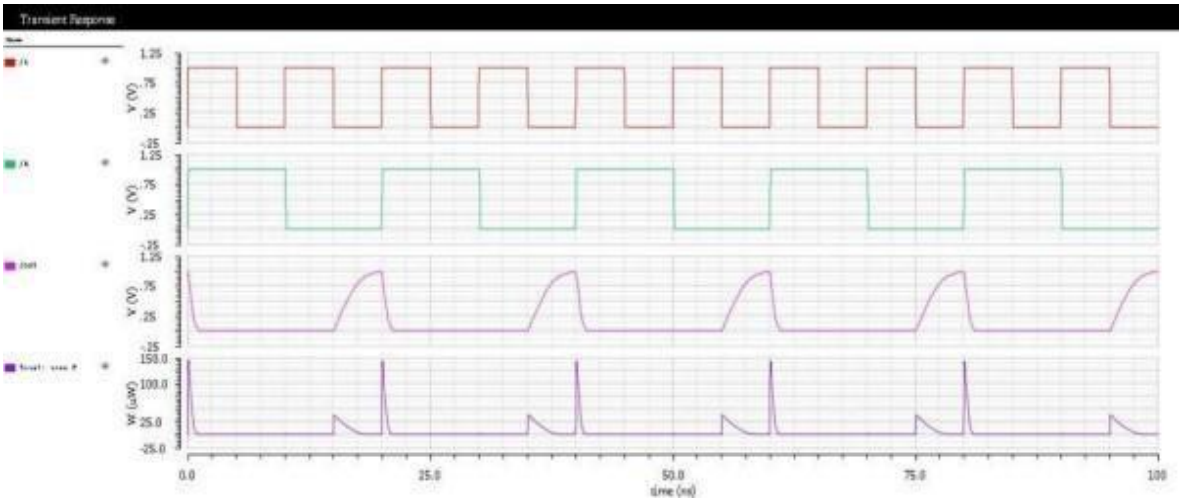


Figure xv.NOR Gate Power Dissipation

From the graph above we can say that power is dissipated mostly when there is transition at output of NOR Gate from 0 to 1 or 1 to 0.

2) POWER DISSIPATIONTYPES

The power dissipation in a semi-conductor based device consists of two components.:–

a) Dynamic Power Dissipation.:-

This is said to be switching dissipation, and as its name reflects it happens for signals that experiences the “CMOS” circuit changes its logic output. As of now energy is brought from the power supply gracefully to energize the yield hub capacitance. Power supply charges up of the output capacitance

resulting in shift from 0V to maximum voltage. Taken into notice an inverter example power brought from the power supply is disseminated in form of heat in pMOS transistor while nMOS dissipates heat.

Capacitance at the external node of the CMOS logic gate comprises of following parts.:-

Output node capacitance: Drain diffusion area is the key factor.

Total interconnect capacitance: For reduction in technology node it impacts the difference.

Driven gate input capacitance: Gate oxide capacitor due to silicon dioxide layer is the key factors.

For calculating the avg. power integrated energy is used. To charging the external node capacitance to maximum voltage is the first step. The next step is to discharge the total output voltage to ground level with no rise and fall time and time period T.

b) Static Power Dissipation:-

It is also called leakage power. For geometries less than 90nm, leakage power behaves as the prominent dissipater while bigger dimension has switching as the key factor. Power reduction methods can be used to reduce both types of power.

Total power consists of various process depending on factors such as rise to fall and fall to rise.

Other factors are capacitor, voltage, and the CMOS structure itself.

Dynamic power is addition from 2 sources. Switching activity and short circuit dissipation are the sources. Switching activity happens when charge up and charge down internal and wire capacitors. Short-circuit dissipation is consumption of power by momentary short circuit connection between Vdd and GND.

Pswitching = m*f*C*Vdd2.

Where m = activity.

f = frequency.

C =capacitor value & Vdd = the voltage supply.

Pshort-circuit = Isc*Vdd*f.

Here Isc is the short circuit current.

Dynamic power dissipation gets decreased by minimizing switching activity & clock frequency. These influence consummation; supplemented by decreasing capacitor value and voltage source.

Dynamic power gets decreased by selecting faster slew components which consume less dynamic power. Leakage power is dependent on Vdd, Vth, and transistor's area.

PLeakage = f (Vdd, Vth, W/L).

Where Vdd = the supply voltage. Vth = the threshold voltage.

W = the transistor width. L = the transistor length.

Leakage Power:

The power dissipated by the sub threshold currents are termed as leakage power.

Sub threshold Current:

The sub threshold current always flow from source to drain despite of Vgs being smaller to component threshold voltage. It occurs because of the carrier flow in weak inversion.

When Vgs is smaller to Vth of the component then sub threshold current comes into the picture.

c) Power Dissipation Reduction Method

Reduce supply voltage

Decreasing voltage behaves as a constructive process to decrease power dissipation. For 2 times decrease in voltage source results in decrease in power dissipation in 4 times and it does not equire any specific circuit.

This gets removed by reducing the threshold voltage.

Physical capacitance

The dynamic power dissipation of the circuit directly depends on the physical capacitance being switched. So, over and above reducing voltage, lesser capacitance gets to obtain lesser consumption.

Increase in the threshold voltage

Surge in the Vth of the device maintains the gate to source voltage of the NMOS transistor safely lower than Vt of nMOS.

Scaling causes sub threshold leakage currents to play huge role in net power consumption. (MTCMOS) has grown being an encouraging method used for shorten leakage power.

3) D FLIP FLOPWORKING:

The D-type Flip Flop leads to the significant contribution of the clocked flip-flops. This confirms of inputs S & R cannot be equal to '1' simultaneously. The D-type flip flop is constructed of a gated SR flip-flop with a not gate attached between the S and the R. These contributions are to be brought in consideration a solitary D (Data) input.

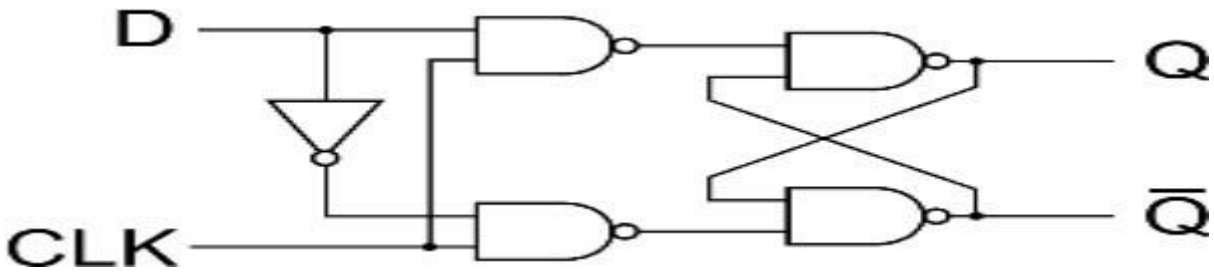


Figure xvi. D Flip-Flop Circuit

Q(n)	D	Q(n+1)
0	0	0
0	1	1
1	0	1
1	1	1

Figure xvii. Truth Table of D Flip Flop

In place of the "Set" signal an input “D” is used to carry the single information. A not gate is used to construct correlative "Reset" input along these lines. These lines make a level-sensitive D- type flip-flop from a level- sensitive “SR”-lock where (S = D) and (R != D) forms the diagram.

The data or D-type Flip Flop is constructed utilizing a couple of consecutive SR latches. Where inputs are associating a “NOT Gate” between the S and the R inputs to allow for a singular D (information) input. The fundamental D flip flop circuit can be improved further by including a subsequent SR flip-flop to its output that is enacted on the corresponding clock sign to create an "Master Slave D flip-flop" gadget.

A latch doesn't have a trigger sign to convert state while flip flop consistently do so. The D “flip flop” being an edge activated circuit which moves D information to output on clock rise or fall triggering. Data Latches are level delicate gadgets, for example, the data latch and the transparent latch.

a) Flip Flop working using cadence virtuoso

Circuit Diagram:

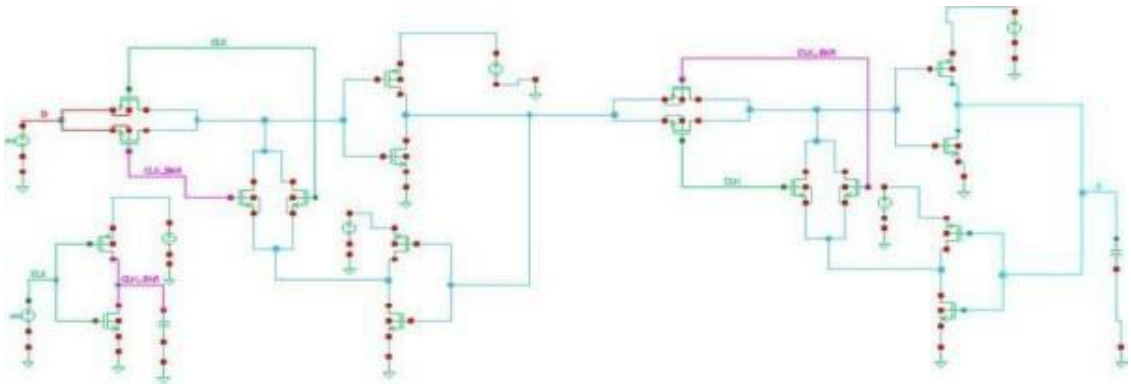


Figure xviii. D Flip Flop Virtuoso Circuit Diagram

Simulation Results:

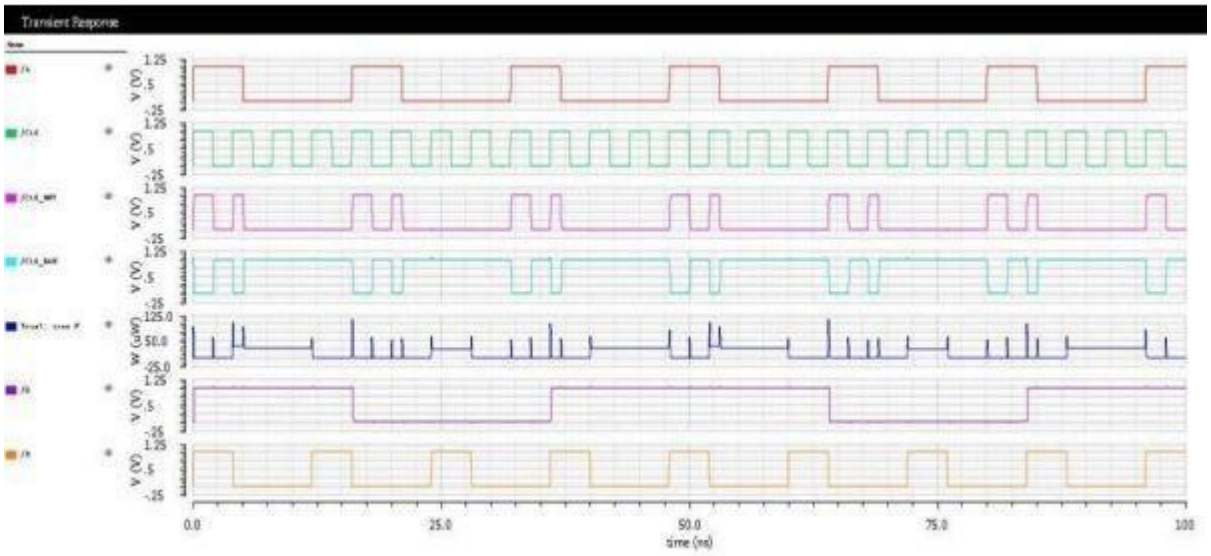


Figure xix. Power Dissipation D Flip-Flop

b) Flip Flop working using verilog

Verilog Code:

```
// Module Name: Without_clkgating

module Without_clkgating(clk,s,r,s1,r1,q,qb,q1,qb1);. /*Without clk gating.*/

parameter HOLD=2'b00, SET=2'b10, RESET=2'b01,

/*Without clk gating.*/

INVALID=2'b11;.

input clk,s,r;

/*Without clk gating.*/

output reg q; output reg s1,r1; output reg q1; output qb1,qb;

always@(posedge clk ) begin
```

```
q<=1'b0;



q1<=1'b0;

case({s,r})

HOLD:q<=q; RESET:q<=0;. /*Without clk gating.*/

SET:q<=1; INVALID:q<=1'bx;

default:q<=q; endcase.

s1 <= q; r1 <= ~q;

case({s1,r1})

HOLD:q1<=q1; RESET:q1<=0; SET:q1<=1;.

INVALID:q1<=1'bx;

default:q1<=q1; endcase.

end

assign qb=~q; assign qb1=~q1; endmodule
```

RTL CIRCUIT:

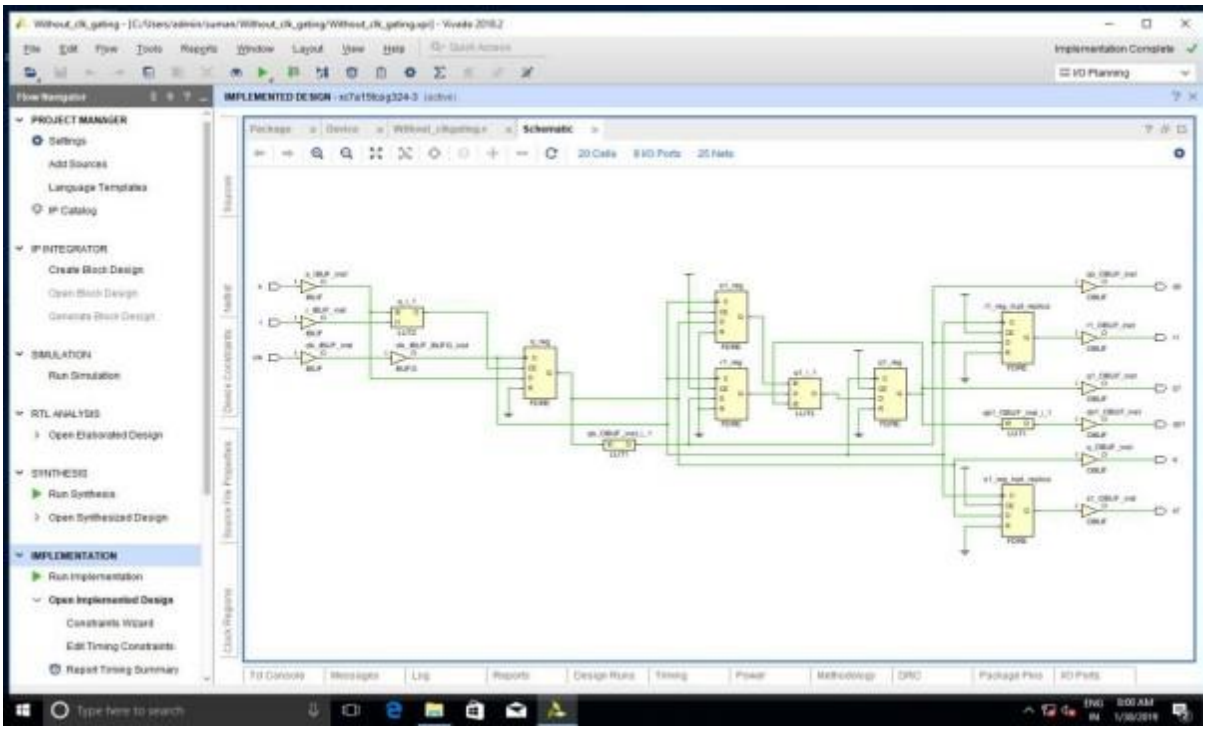


Figure xx. RTL Circuit

POWERDISSIPATION:

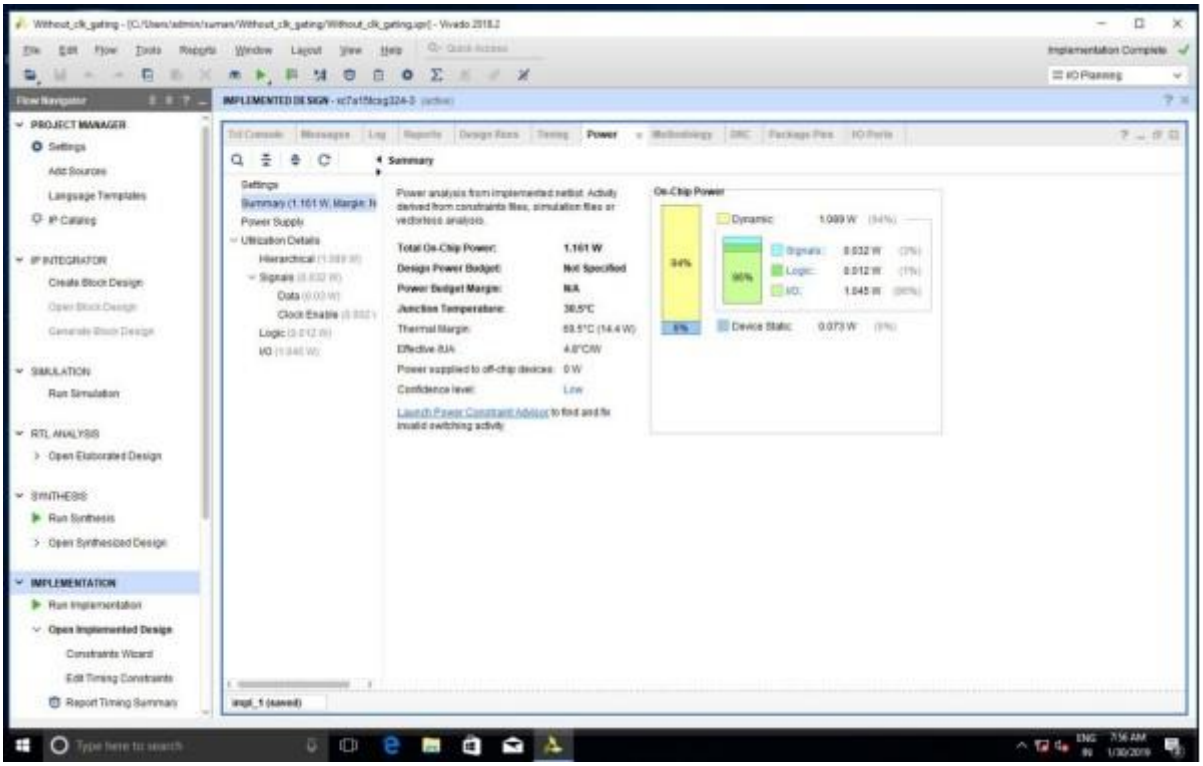


Figure xxi. Power Dissipation using Verilog

4) LITERATURE AND SURVEY

Bassem Alhalabi observed that that a novel Low-Power Multiplexer-Based 1-piece full adder cell that utilizes 12 semiconductors (MBA-12T) is introduced here. MBA- 12T is tried alongside four other low-power 10-transitor l-bit full adders that were appeared of consisting over 26% in power-investment funds over the traditional 28- semiconductor CMOS cell. The testing comprises of mimicking utilizing H-Spice under 6 frequencies, and 6 distinct burdens. MBA-12T displayed that in any event 23% in power-reserve funds over the least force devouring 10- semiconductor cell and at least 64% in speed improvement.

Nidhi observed that a low force full adder cell planned with transmission entry gateway and pass-transistor logic styles that lead to have a decreased space, power and slow down. They contrasted 28T customary CMOS full-adders with 14T and 16T full adder cell, regarding speed, power utilization and space. All the full adders were planned with an O.25um CMOS innovation, and were tried utilizing a tannerv13.0 .After reproducing CMOS and pass transistor rbased full adder,looked at the normal force consumption.16T based Full adder expended 98% less power contrasted with 28T traditional CMOS full adder.

Prasanth observed that adders are normally found in the basic way of many structure squares of microchip and advanced sign processor chips. A quick and precise activity of computerized framework is enormously impacted by the exhibition of occupant adders. The most significant for estimating the nature of adder structures are calculation time and area.

Ravi observed that addition being most fundamental tasks in Digital Signal Processing (DSP). Application does incorporate Fast Fourier Transform (FFT), Digital channels, multipliers and so on uses DSP. With the headways in innovation, research is as yet proceeding to structure an adder which operates in glimmer of time. Being this kind of rapid adder is Carry Save Adder (CSA). In this paper he has planned High Speed Carry Save Adder (CSA) utilizing Carry Look forward adder in the last stage as opposed to utilizing ordinary ripple carry adder with the goal that speed increments by27.5%.

Amit observed that the decrease in the working voltage assume a significant job in improving the presentation of the coordinated circuits. Aside from that lesser power utilization, decreased region and littler size of semiconductors are additionally the essential elements in the structure measures and manufacture of the frameworks. His article approaches towards the expanding execution of the frameworks by contrasting various kinds of adder circuits. In this article, another circuit has been structured utilizing the TG innovation. In view of various boundaries like normal force utilization and postponement power dissipation is high in CLA adder.

Shruti observed that Arithmetic Logic Units being one of the indispensable unit by and general purpose processors and significant wellspring of power dissipation. In their paper they have shown an enhanced Arithmetic and Logic Unit using an upgraded carry select adder. Carry select adders have been considered as the best in their class as far as power and slow down. In this setting a full adder advanced as far as force has been utilized in blending a carry select adder. Joined with the new adder structure, there is a generous enhancement regarding force and postponement. The absolute gadget force and chain of command power has been diminished to 12.50 % and 53.38 % separately. 3.0 % decrease in all out consummation time has additionally been watched. The circuit has been incorporated on kintex FPGA through Xilinx 14.3 utilizing 28 nm innovation in Verilog HDL and results has been mimicked on Modelsim 10.3c. The structure is confirmed utilizing System Verilog on QuestaSim in UVMcondition.

Rashmi observed that as the time pass by, the technology is enhaning. Faster ans smaller chips with greater intricacy in the structure and usage are brought in picture. Consequently productive adder on a VLSI based circuit plays a bigger role. In this paper we essentially manage the development of fast adder circuits. CMOS and GDI logical are utilized for different adders. It's necessities on different dimensions like power and delay are measured. From the outputs got and the investigation, brought a reasonable conclusion of KSA being fast.

Pritam observed that as the chip area is getting diminished because of coming of innovation, power dissemination has become a significant problem to the circuit designers at the hour of structuring an integrated circuit. The key factors of power dissemination are the static power and dynamic power. A serial adder, being the key part of any processor micro-architecture, is a sufferer to the large power flow. In their paper, they have mediated on the options for supervising both static and dynamic power flow by executing the LECTOR based clock gating technique on the sequential elements of serial adder. LECTOR assists to minimize the static power. It does not allow charge flow between the power lines and gated clock. This minimizes the dynamic power by removing the unnecessary switching of system clock.

5) DIFFERENT ADDER CIRCUITS:

By analyzing adder by using different circuits i.e. Carry Look Ahead Adder, Gate Level Design Adder, Ripple Carry Adder, Full Adder implementation UsingMux.

Comparison of different adder gives different power dissipation and delay and power delay product. The power, area and speed trade-offs is considered to get the best desired performance as per the priority. In adder to reduce power dissipation we need to reduce circuit for getting sum and carry thus reduces an additional area. This trade-off between power and area is considered to reach out to the best possiblecircuit.

a) Full Adder

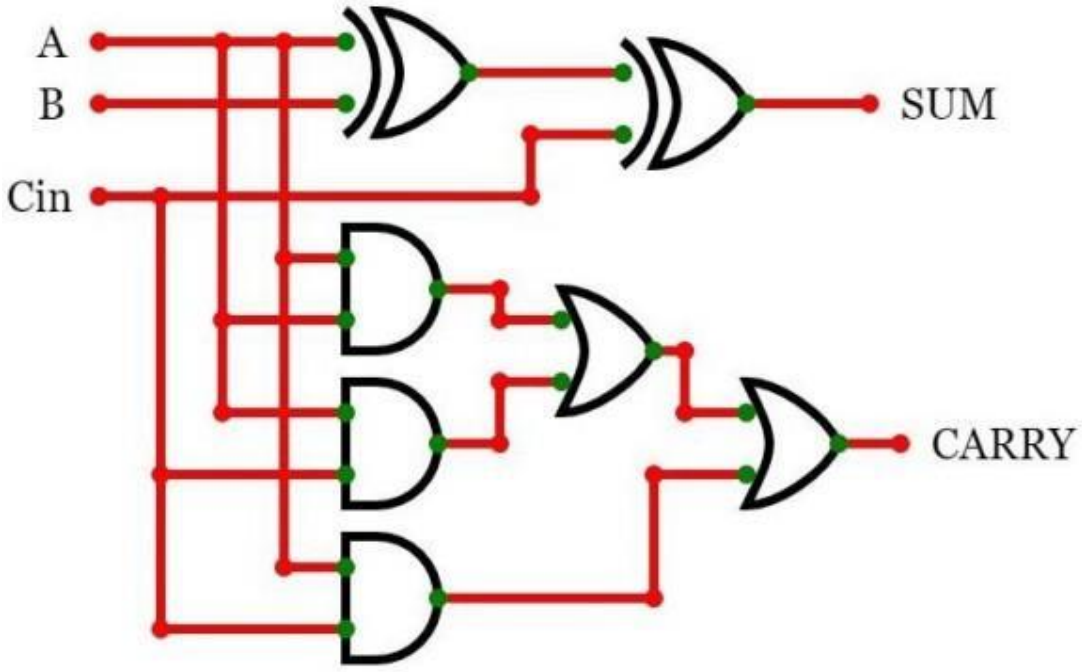


Figure xxii. Full Adder

Boolean expression:-

SUM=(A XOR B) XOR Cin;.

CARRY=((A AND B) OR (B AND Cin)) OR (A AND Cin);

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table iii. Truth Table Of Full Adder

b) Gate-Level

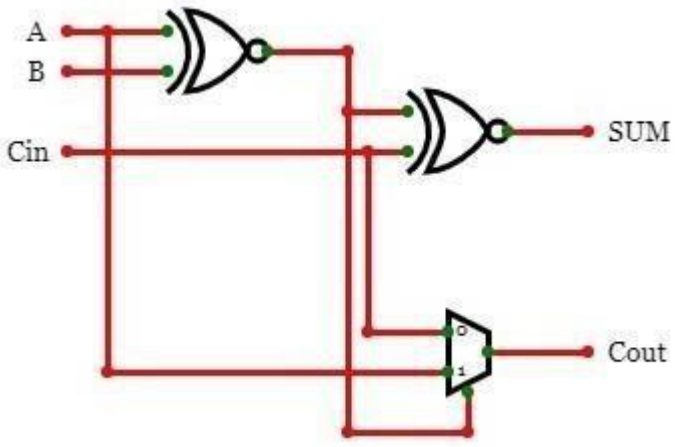


Figure xxiii. Gate Level Design Adder

Boolean expression:-

SUM=(A XNOR B) XNOR Cin;.

Cout=((A XOR B) AND Cin) OR ((A XNOR B) AND A);

c) 12-Transistor 1-Bit Full Adder Circuit

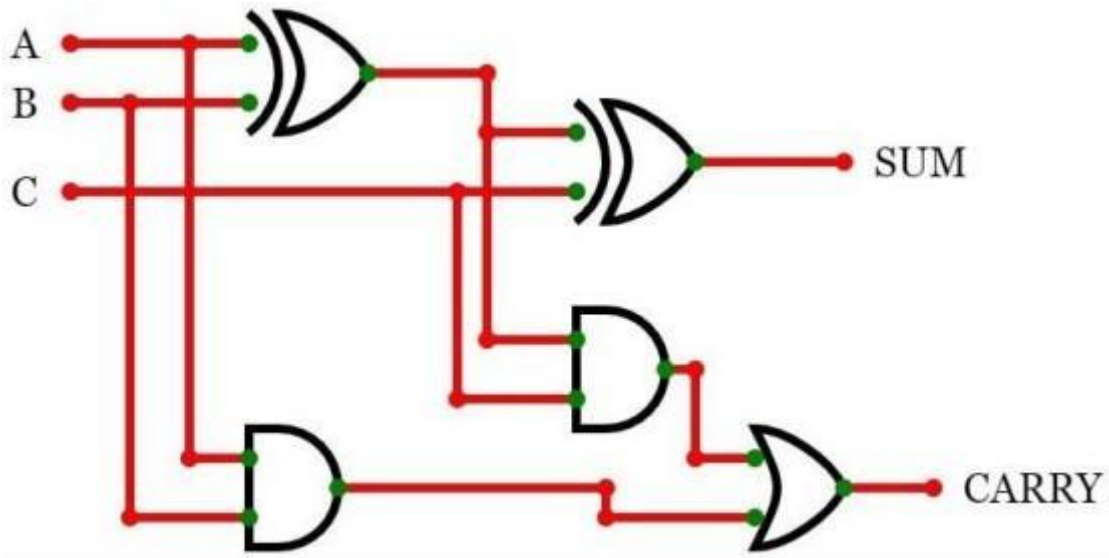


Figure xxiv. Transistor 1-Bit Full Adder

Boolean expression:-

SUM = (A XOR B) XOR C;.

CARRY=((A XOR B) AND C) OR (A AND B);

d) Multiplexer based carry select modified tree

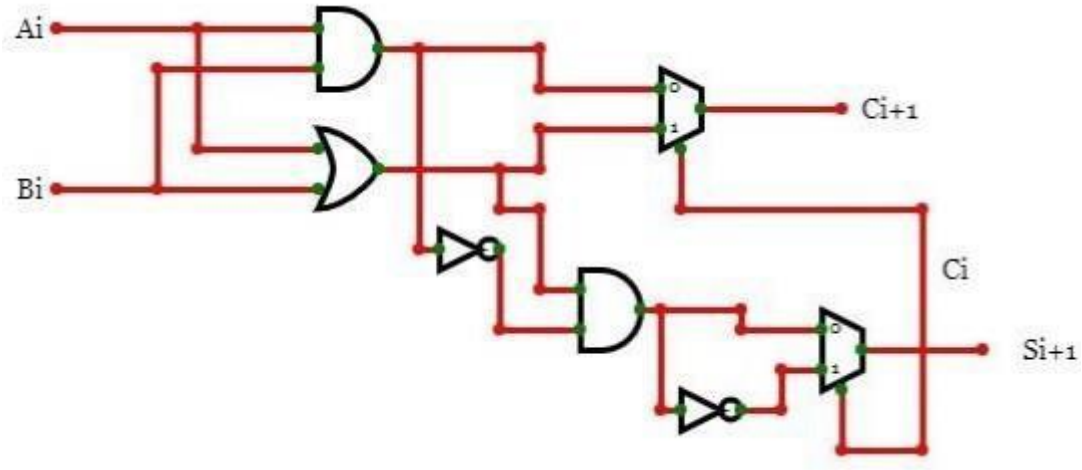


Figure xxv.Mux Based Adder

Boolean expression:-

Si+1=((Ai AND Bi) AND (INV Ci)) OR ((Ai OR Bi) AND Ci);

Ci+1=((Ai NAND Bi) AND (Ai OR Bi))AND (INV Ci)) OR (INV ((Ai NAND Bi) AND (Ai OR Bi)) AND Ci);

6) ADDER SIMULATION:

The given input for all the circuits has been taken same in the order given as follows:

Signal	V1(V)	V2(V)	Time Period(ns)	Rise Time(ps)	Fall Time(ps)	Pulse Width(ns)
B	0	1	5	250	250	2
C	0	1	10	500	500	4
A	0	1	20	500	500	9

Table iv.Input Of Adder

a) Cadence Virtuoso Results

FULL ADDER:

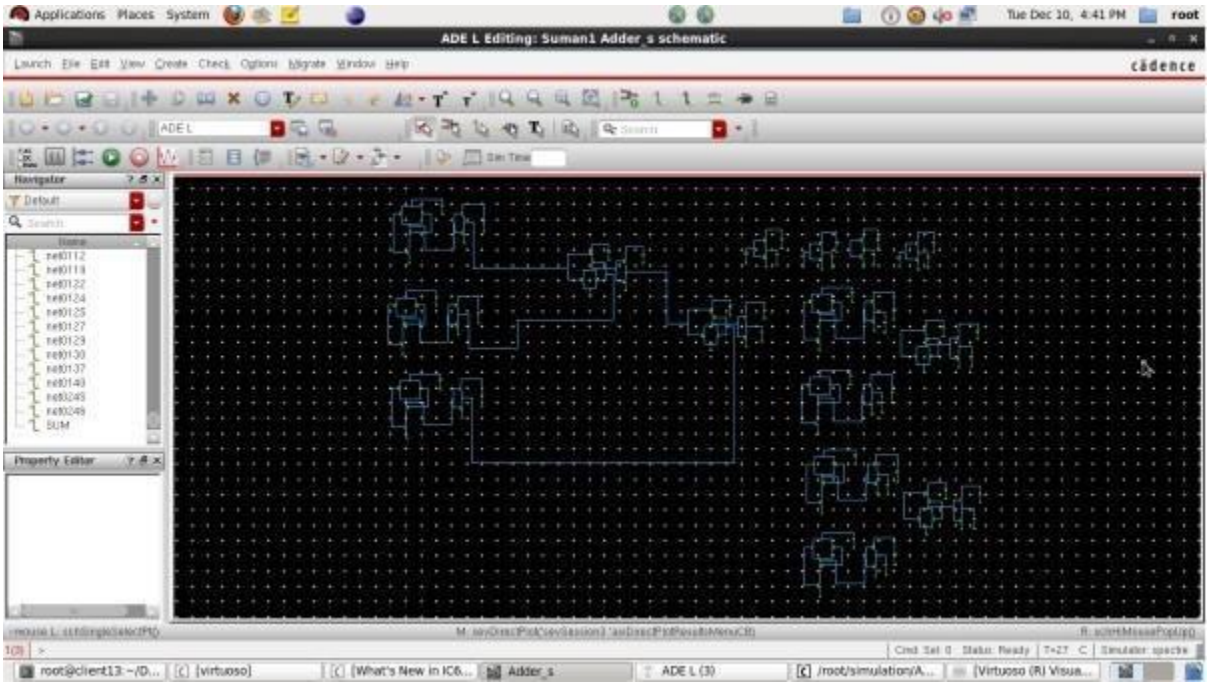


Figure xxvi. Schematic Diagram Full Adder

OUTPUT GRAPH:

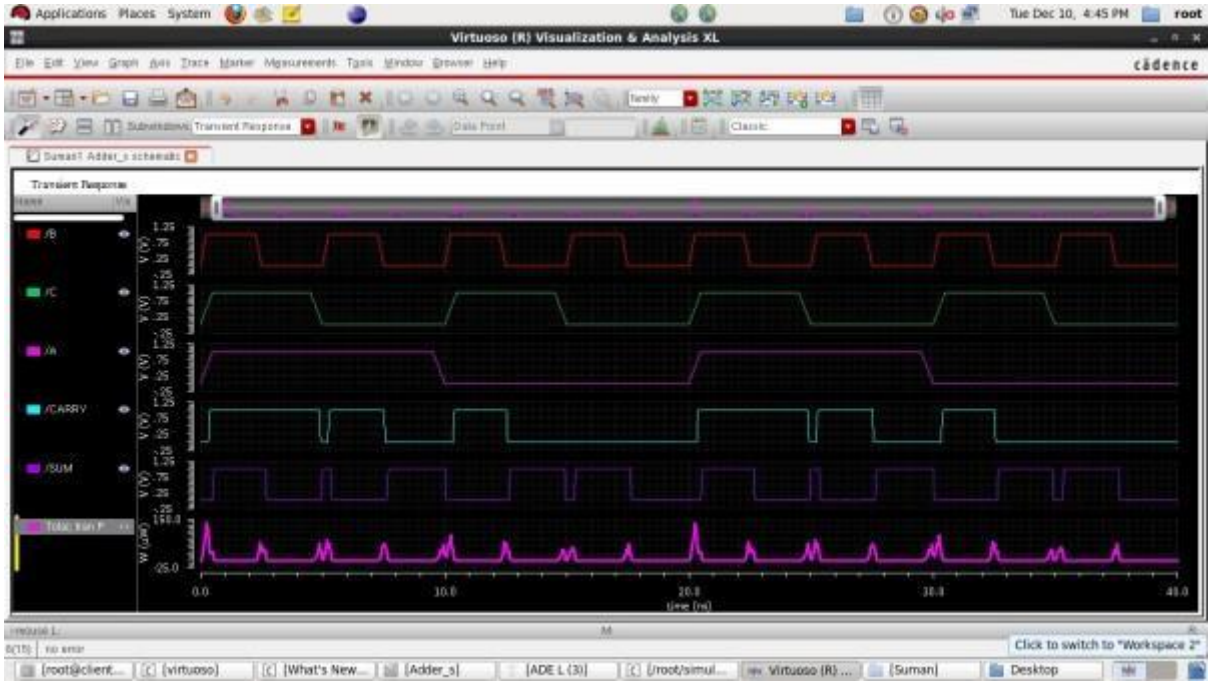


Figure xxvii. Graph Full Adder

Signal	Delay(second)
Sum	327.7 E-12
Carry	155.9 E-12

Table v. DelayFull Adder

Signal	Maximum Power(Watt)	Average Power(Watt)
Sum	1.009	472.0 E-3
Carry	1.000	451.0 E-3

Table vi. Power Dissipation Full Adder

GATE LEVEL DESIGN OF FULL ADDER:

Signal	Delay(second)
Sum	332.5 E-12
Carry	13089 E-12

Table viii. Delay Gate Level Design

Signal	Maximum Power(Watt)	Average Power(Watt)
Sum	1.006	432.0 E-3
Carry	1.000	306.0 E-3

Table vii. Power Dissipation Gate Leve Design

SCHEMATIC DIAGRAM:

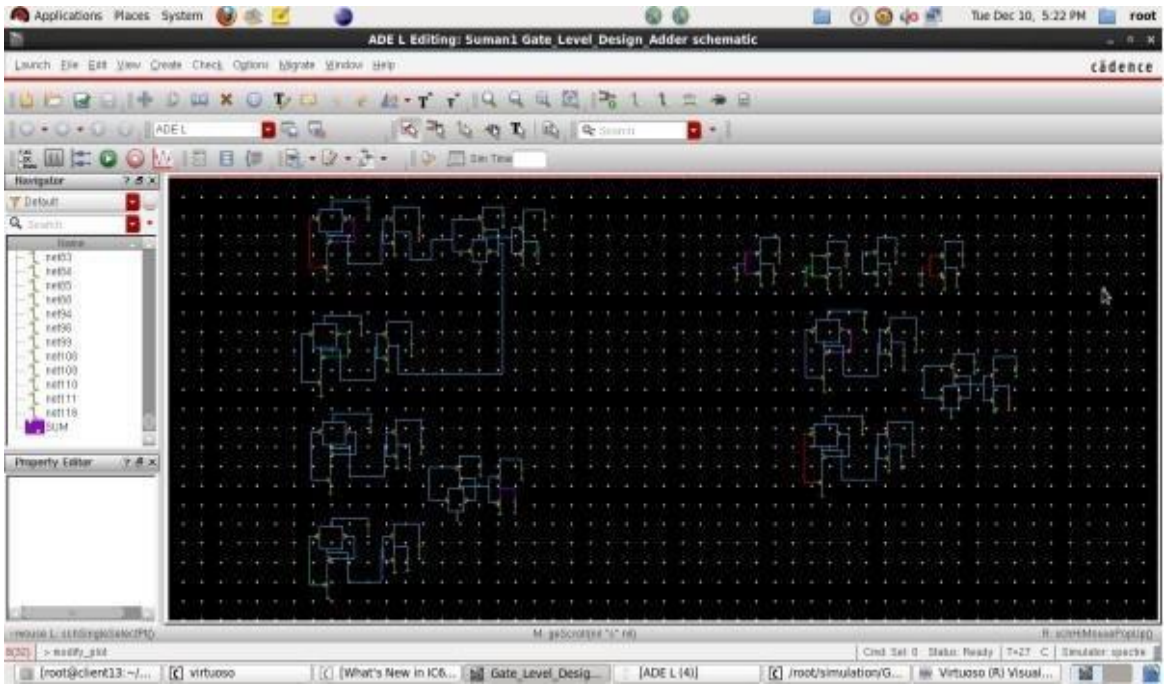


Figure xxviii. Gate Level Design Full Adder Circuit

OUTPUT:

Figure xxix. Gate Level Design Adder Graph

b) LTspice Simultions:

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table ix. Full Adder Truth Table

Carry input is not being provided in half adder.

In arithmetic logic unit part which is the core of any processor adder plays a very important role. Using any sort of modification if we become able to reduce the power dissipation then it will be huge advantage for us. Power and timing analysis plays major role in vlsi industry.

Full Adder Circuit:

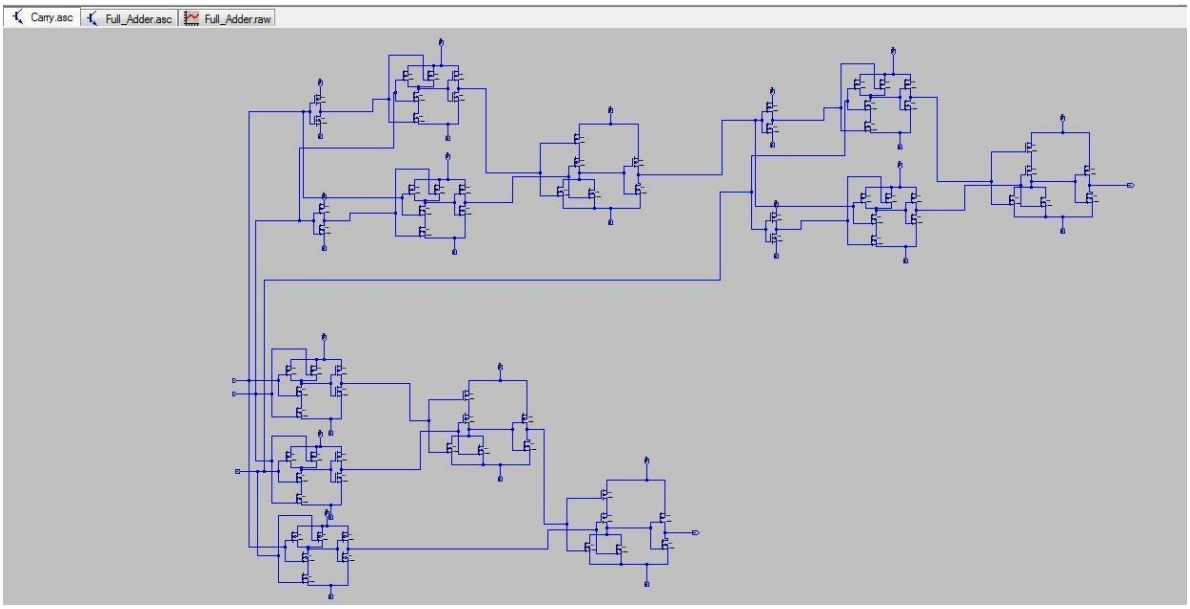


Figure xxx. LT Spice Full Adder Circuit

Full Adder Graph:

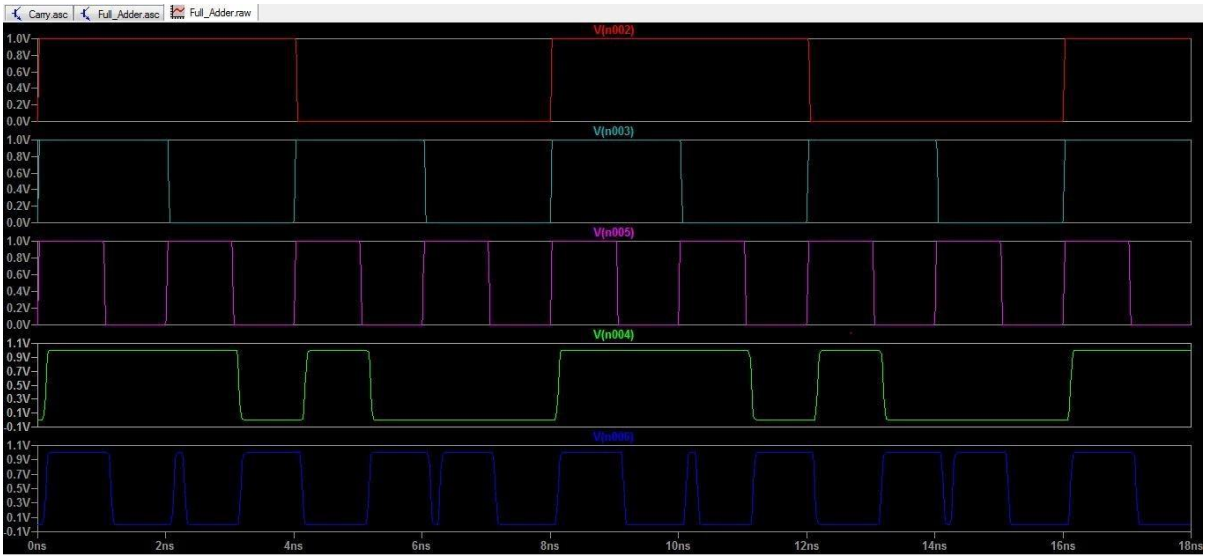


Figure xxxi. LT Spice Full Adder Graph

Full Adder Power Carry Graph:

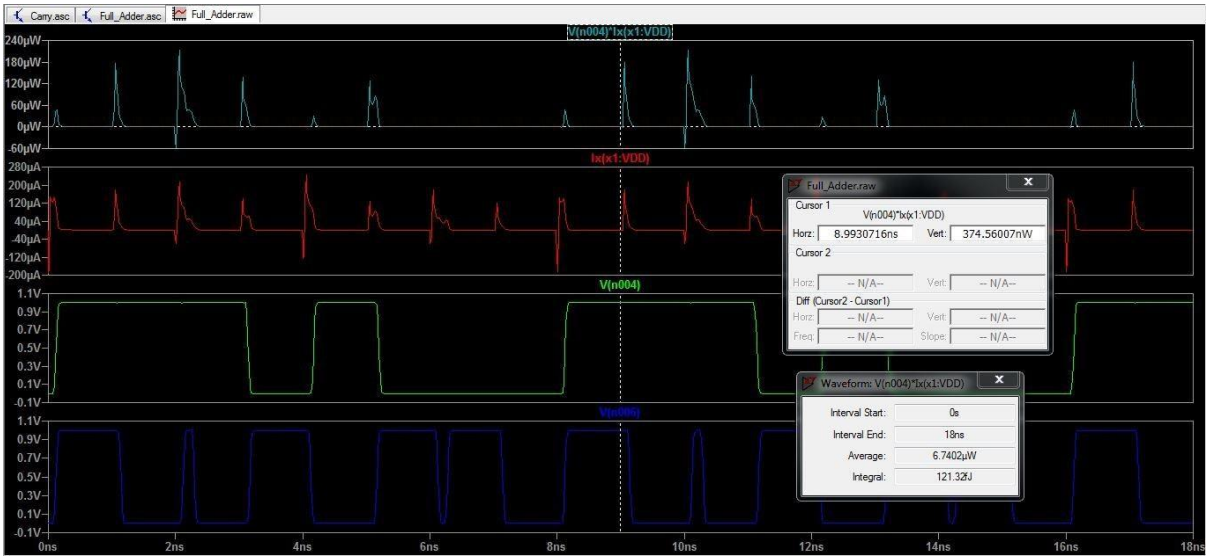


Figure xxxii. LT Spice Full Adder Carry Graph

Full Adder Power Sum Graph:

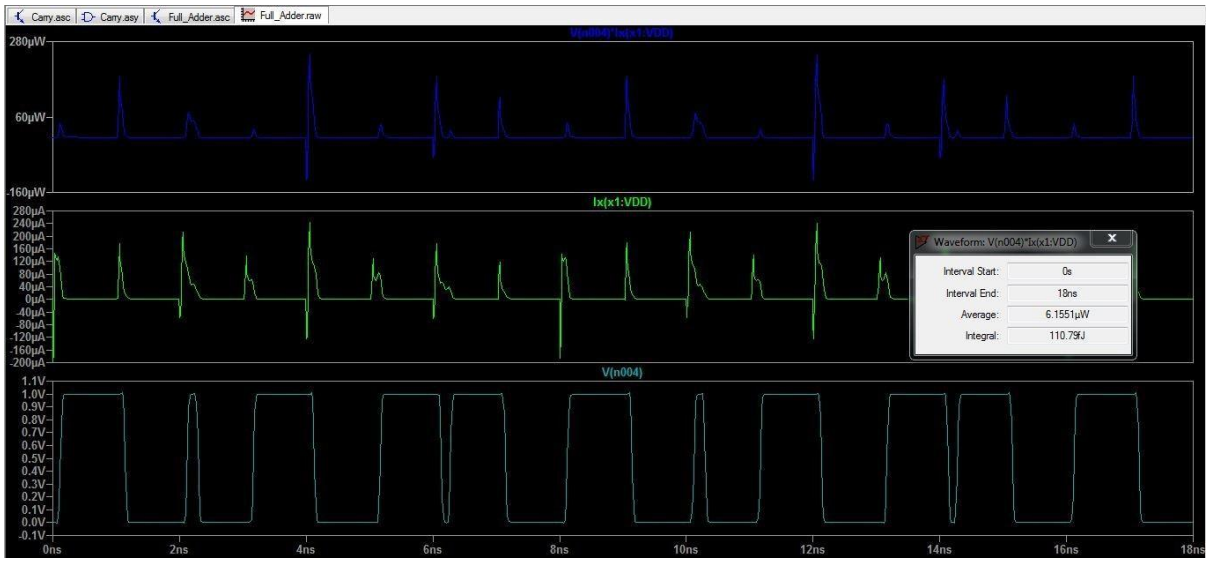


Figure xxxiii. LT Spice Full Adder Sum Graph

Outputs	Average Power	Total Energy	Total Interval
SUM	6.1551μW	110.79fJ	18nS
CARRY	6.7402μW	121.32fJ	18nS

Table x. Full Adder LT Spice power of Sum and Carry

Full Adder Symbol:

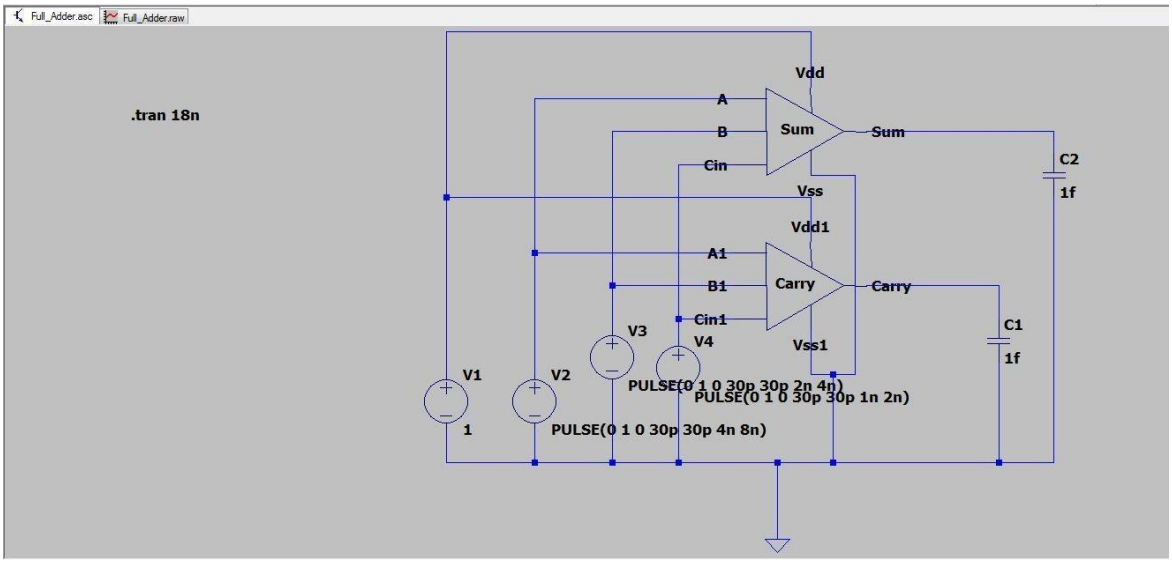


Figure xxxiv. LT Spice Full Adder Symbol

Gate Level Design Circuit:

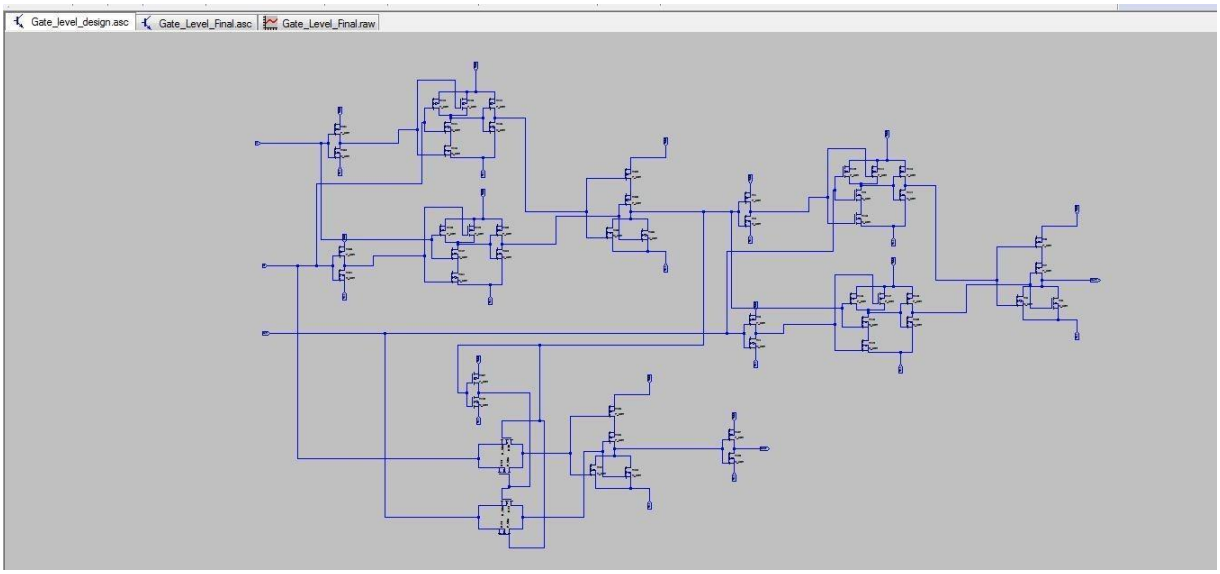


Figure xxxv. LT Spice Gate Level Design Circuit

Gate Level Design Graph:

Figure xxxvi. LT Spice Gate Level Design Graph

Gate Level Design power Graph:

Figure xxxvii. LT Spice Gate Level Design Power Grph

Outputs	Average Power	Total Energy	Total Interval
SUM	2.1025µW	37.845fJ	18nS
CARRY	2.2093µW	39.7674fJ	18nS

Table xi. Power Graph Gate Level Deign Circuit

Gate Level Design Symbol:

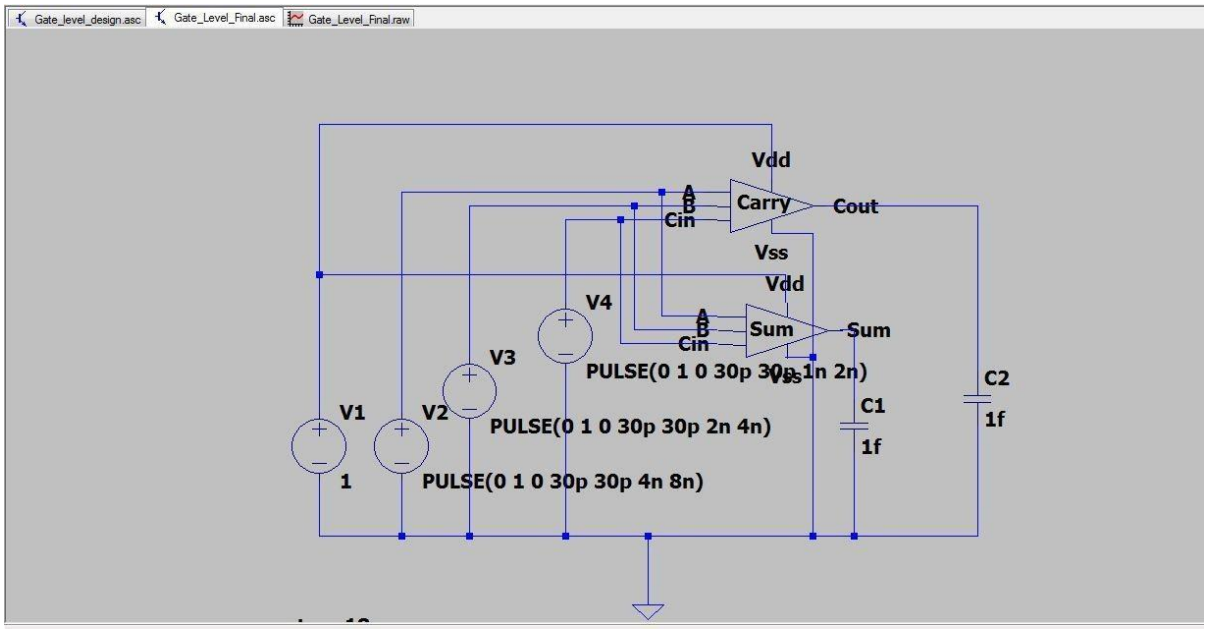


Figure xxxviii. LT Spice Gate Levl Dsign Symbol

12 Transistor Full Adder Circuit:

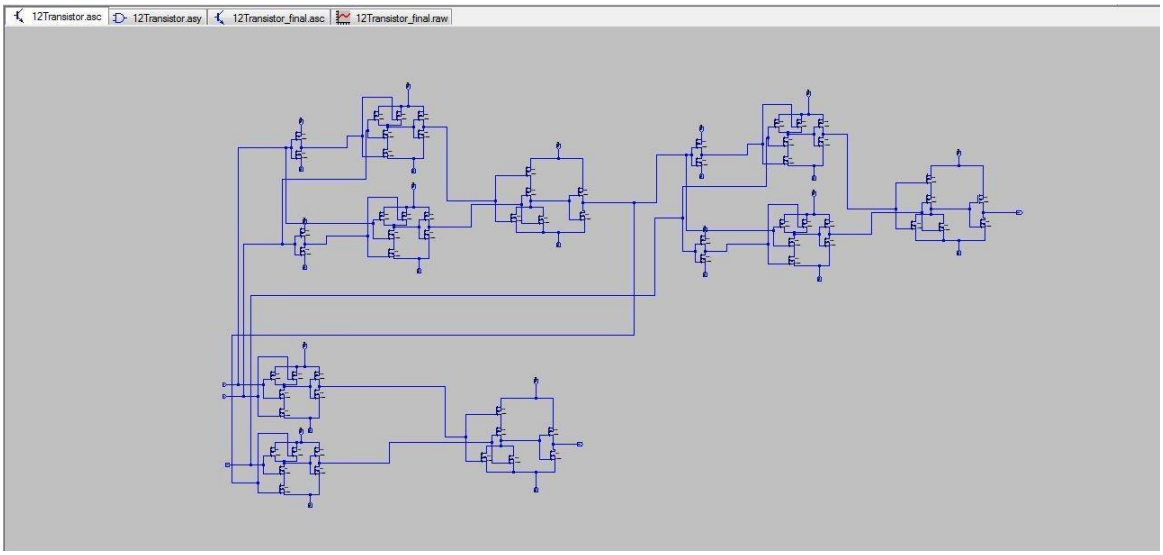


Figure xxxix. LT Spice 12 Transistor Full Adder Circuit

12 Transistor Full Adder Graph:

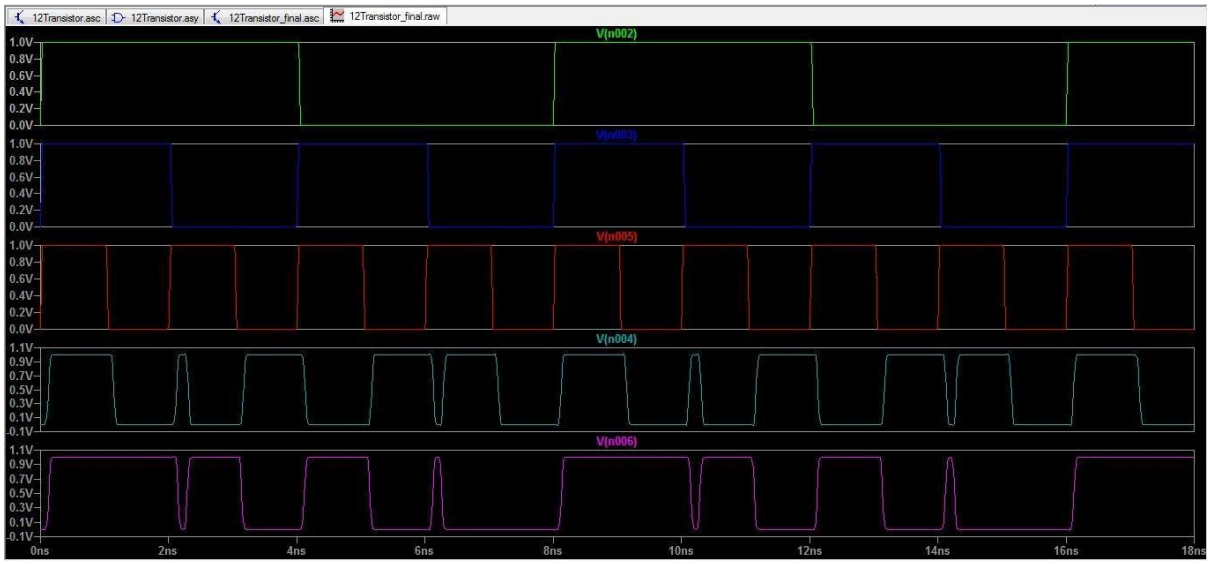


Figure xl. LT Spice 12 Transistor Full Adder Graph

12 Transistor Full Adder Power Sum Graph:

Figure xli. LT Spice 12 Transistor Full Adder Power Sum Graph

12 Transistor Full Adder Power Carry Graph:

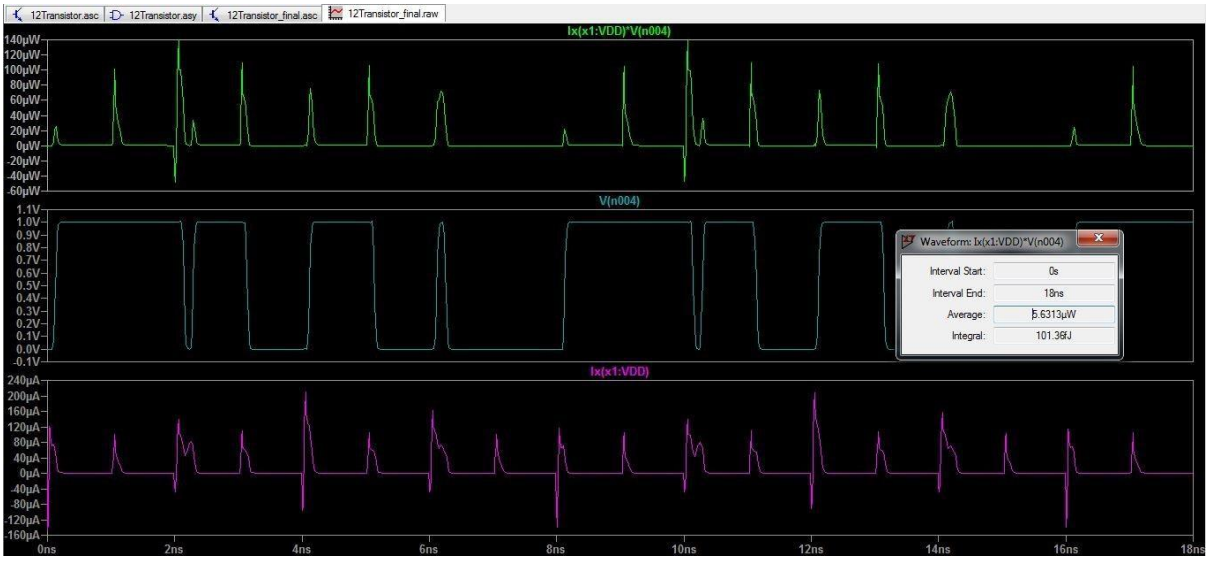


Figure xlii. LT Spice 12 Transistor Full Adder Carry Graph

Outputs	Average Power	Total Energy	Total Interval
SUM	5.9963µW	107.938fJ	18nS
CARRY	5.6313µW	101.36fJ	18nS

Table xii. LT Spice 12 Transistor Power Dissipation

The Circuit has been give the common input and power has been taken into observation.

It implies less power dissipation than full adder while more than gate level design.

12 Transistor Full Adder Symbol:

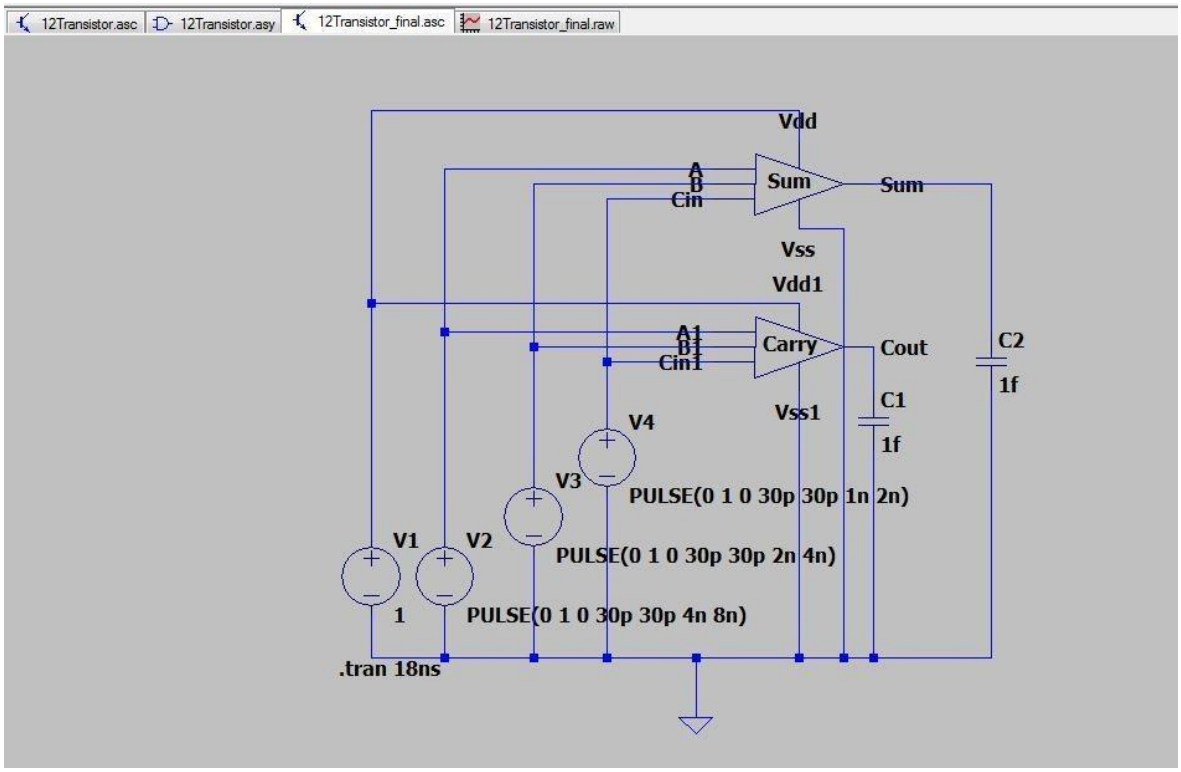


Figure xliii. LT Spice 12 Transistor Full Adder Symbol

7) TIMING ANALYSIS:

a) Setup Timing and Hold Timing

Set up Time is the least value of time that input must be kept stable prior the triggering of clock such that input get reliably sampled using the trigger. This applies to the synchronous circuits such as the Flip Flop.

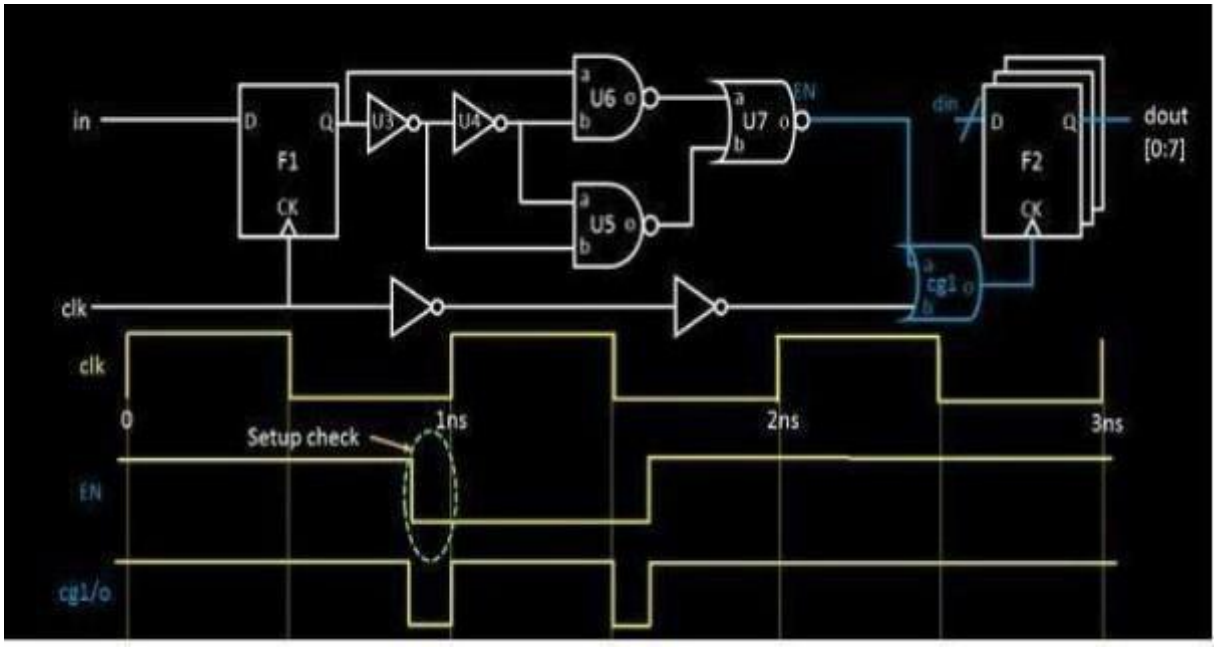


Figure xliv. Set Up Time

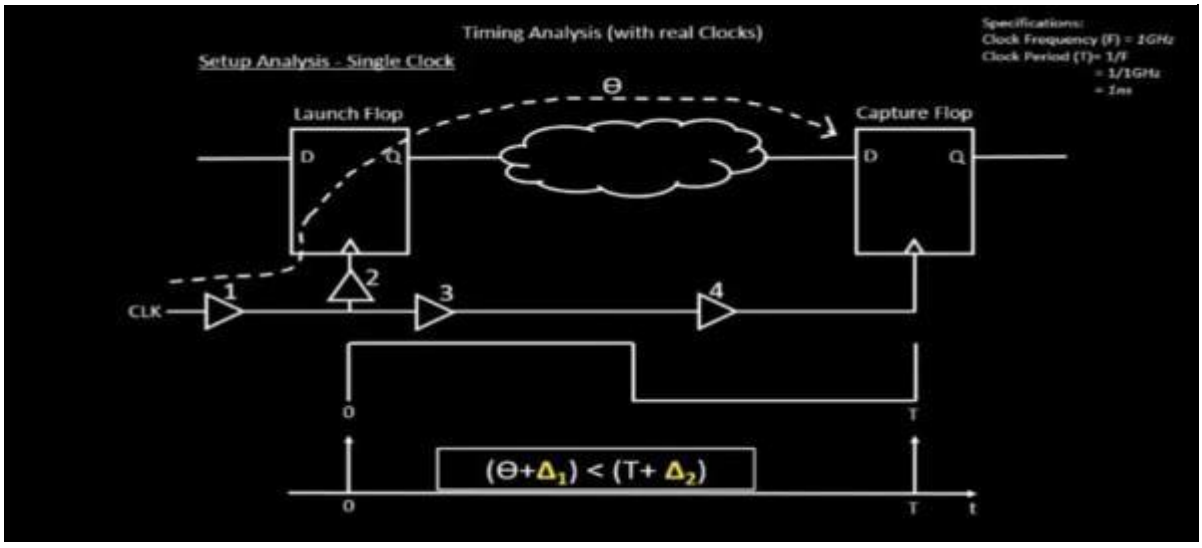


Figure xlv. Set Up Timing Constraints

Hold time is the least value of time that input must be held stable post triggering of clock such that the input can get reliably sampled. This applies to synchronous circuits such as Flip Flops.

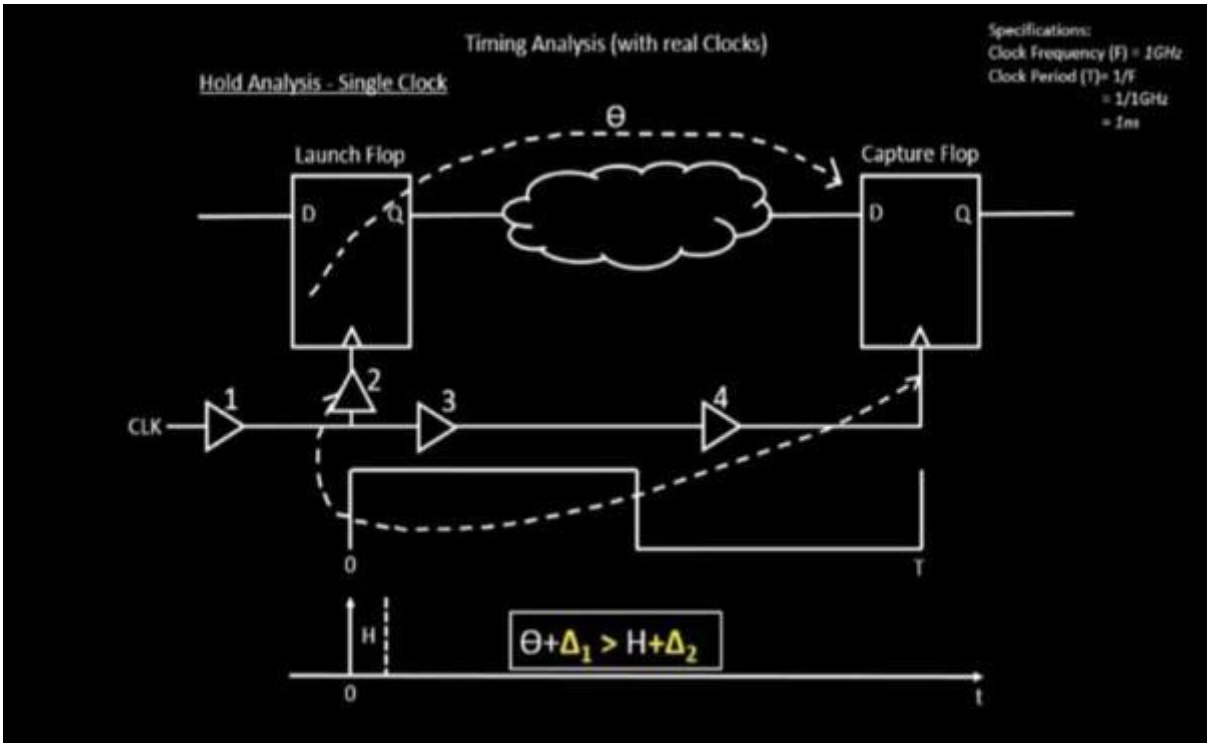


Figure xlvi. Hold Time Timing Constraints

b) Launch and Capture Flops:

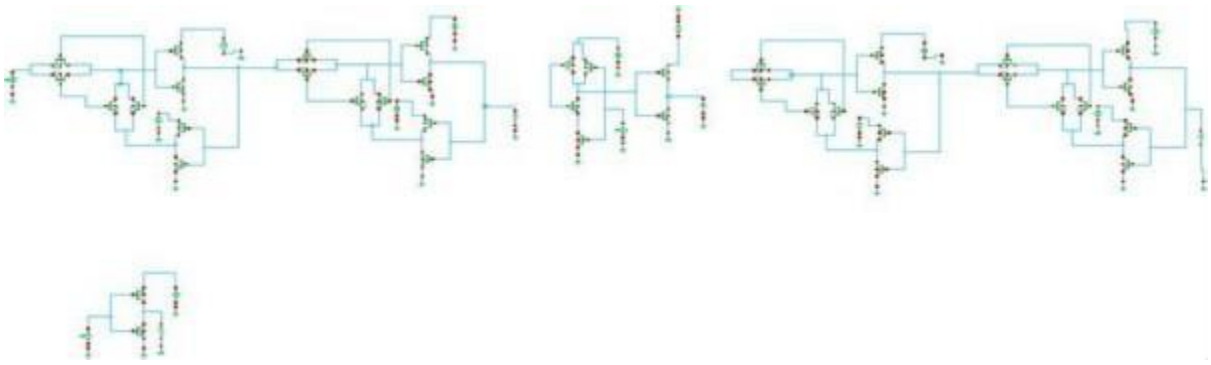


Figure xlvii. Launch and Capture Flop Circuit

Here we are supposed to analyze whether the circuit is working properly in any flip flop. Clock is the key factor in analyzing whether the signal reaching from one flop to another flop follows their timing constraint. For circuits giving data at incorrect time will lead to give false data at the time of requirement thus ending up to be a filed system. Processor or different memory based circuit made of flip flop required the timing constraints to be analyzed before - hand reaching the market.

Launch as the name suggests here is a circuit which transmits the data and taken as a reference of source. Capture being the part of circuit which captures the data and the checking point is over here whether the functionality is correct.

The circuit has been taken in parts in different images in order to get the gist of the circuit Launch Flop has been drawn in this part of the circuit.

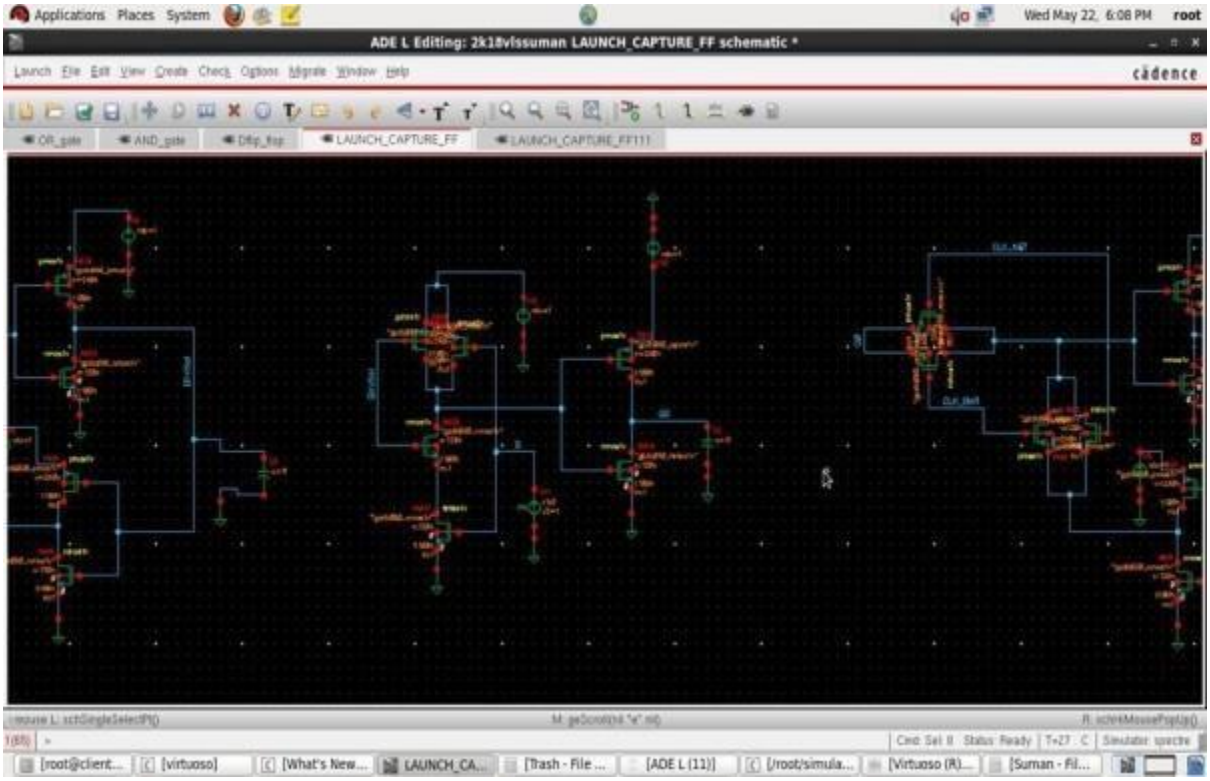


Figure xlviii. Launch Circuit

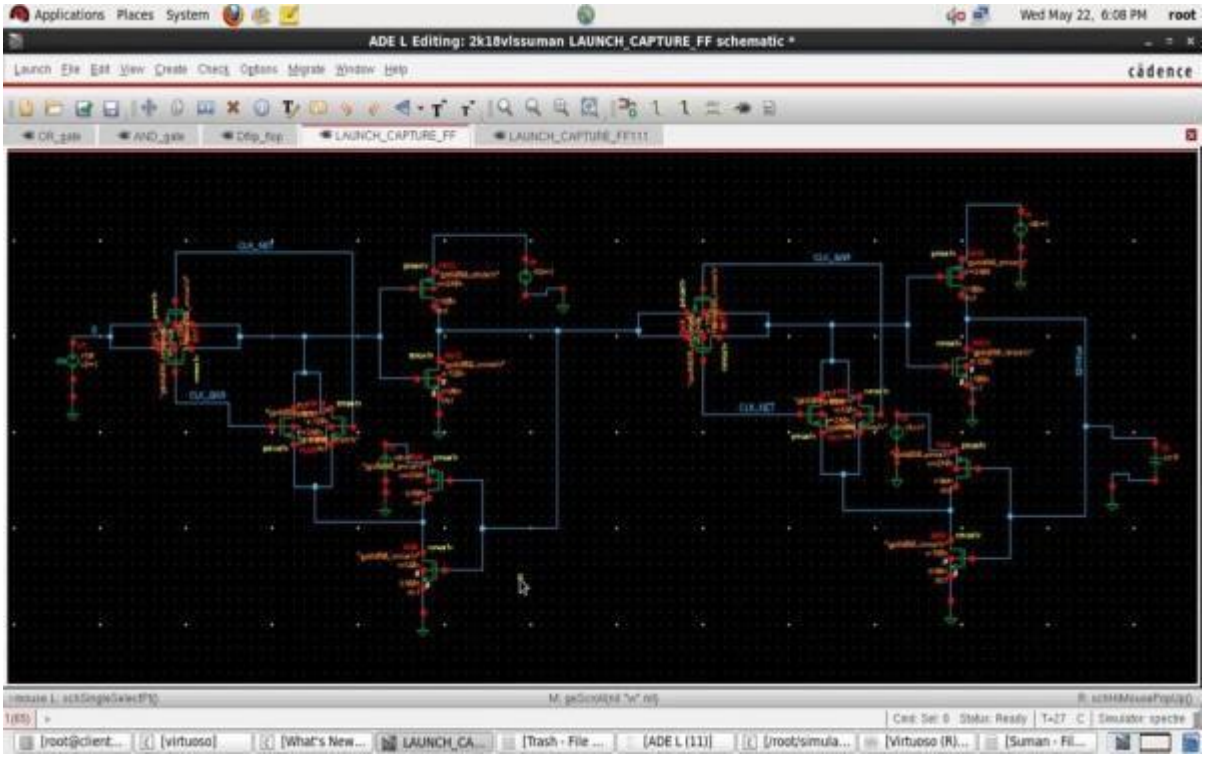


Figure xlix. Combinational Circuit

Combinational Circuit has been drawn in the below image which is adding the power dissipation and delay while Setup and Hold Time Analysis. Capture Flop has been drawn in this image from where it is compared to measured Setup time in timing analysis and it is the last part of Launch Capture Flop.

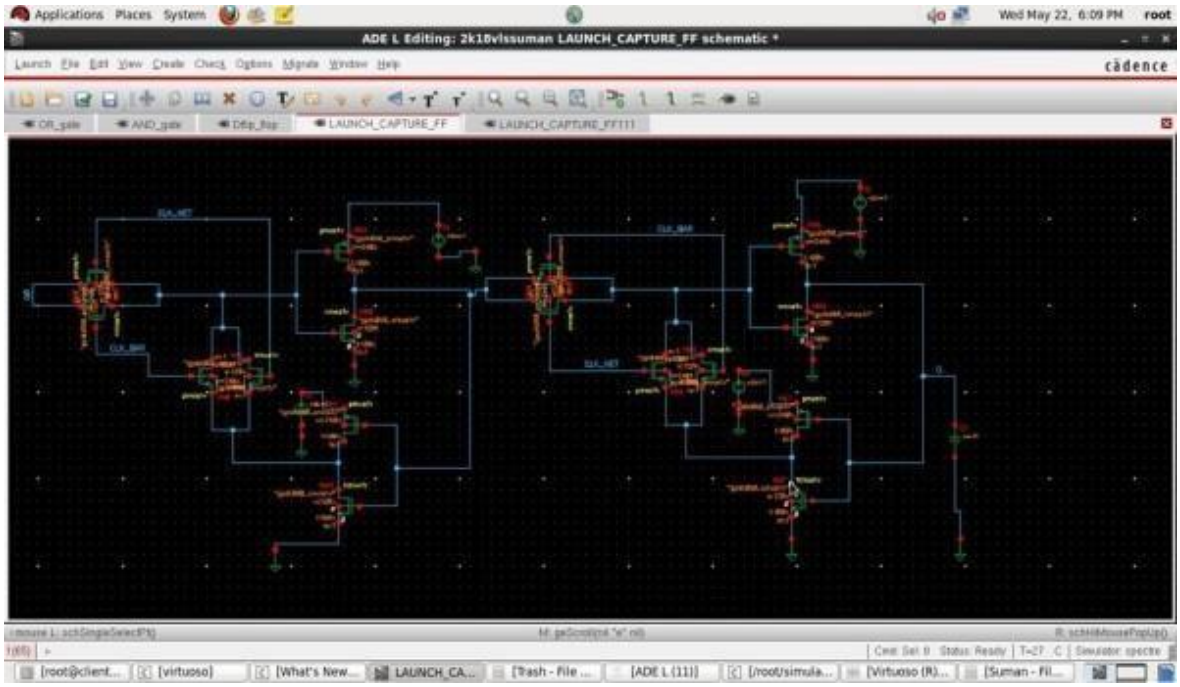


Figure l. Capture Circuit

8) CONCLUSION AND FUTURE SCOPE:

From the above experiments in which we implemented different adder (i.e. Full Adder, Gate Level Design of Full Adder) and calculated total power dissipation and delay. Processor has the challenges of trade-off between area, power and speed. Here we are increasing area by adding control circuits. The power dissipation of Gate Level Design of Full Adder amount to reduction of power dissipation in compared to Full. Then, we go for further trade-offs between area and power. Carry input is not being provided in half adder.

In arithmetic logic unit part which is the core of any processor adder plays a very important role. Using any sort of modification if we become able to reduce the power dissipation then it will be huge advantage for us. Power and timing analysis plays major role in vlsi industry.

In Gate Level Design Adder as we can see that there is a huge reduction in power dissipation. Power dissipation plays a major role in selection of full adder in arithmetic logic unit. The power dissipation of Gate Level Design Adder has been reduced to 2.1025μW for sum in compare to Full Adder having power of 6.1551μW for sum in compare to Full W which results in 66% power dissipation reduction.

In Future since market has high demand of portable device and the enhancement in battery technology is not at par with VLSI Industry. There is high demand of technologists to reduce power dissipation of processor. The demand of speed has been increased up to Ghz. For such a high speed processor there is high power dissipation in clock. Thus adder with high speed and less power dissipation will play a big picture. For different operation it gives different power dissipation or even less delay or both at the same time. Adder operation is a very basic part which is likely used for all arithmetic operations.

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