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B.Tech Electrical Engg. & Electrical & Electronics Engg. *7th SEMESTER*

SUPPLEMENTARY EXAMINATION *(Feb-2019)*

EE -405-Digital Signal Processing

Time: 3:00 Hours ***Maximum Marks:40***

Note: Q.1 & Q.2 are compulsory, answer any 3 other questions from the remaining
Assume suitable missing data, if any
Attempt all parts of a question at one place *(Marks may not be awarded otherwise)*

1 [a] Find the step response of the system whose impulse response is:
$h(n) = (1/3)^n$ 2

[b] Investigate the BIBO stability of system whose impulse response is:
$h(n) = 2^n u(5-n)$ 2

[c] The signal $x(t)=10\cos(10\pi t)$ is sampled @8 samples/sec. Plot the amplitude spectrum for $|\Omega| \leq 30\pi$ (*both in continuous time and sampled mode*). Investigate whether the original signal can be recovered from samples? 4

2 [a] The input to a causal LTI system is:
$x[n] = u[-n-1]+(1/2)^n u[n]$; the *z* transform of the output of the system is:

$$Y[z]=\frac{-\frac{1}{2}z^{-1}}{\left(1-\frac{1}{2}z^{-1}\right)(1+z^{-1})}$$

Determine H[z], the z-transform of the impulse response and y[n]. 4

[b] Consider the following system function:

$$H[z]=\frac{z}{\left(z-\frac{1}{4}\right)\left(z+\frac{1}{4}\right)\left(z-\frac{1}{2}\right)}$$

For the different possible ROC, determine the causality, stability and the impulse response of the system. 4

3 Draw neat diagrams of direct structure-I, direct structure-II for DSP implementation of PID controller. Write their implementing difference equations for both the forms and compare the structure on count of time delays, multipliers, summing junctions and signal distribution points. Modify the equations to realize the structure as transposed form. 8

4 [a]Through timing diagram (SoC/EoC) demonstrate the interfacing of A/D converter with DSP. Explain the auto-sequencing feature of A/D converter and briefly discuss the application to two closed loop (*DC voltage & Current loop*) control of a grid connected voltage source inverter by appropriately programming the $CHSELSEQ_n$ registers and MAXCONV register. 4

P.T.O.

[b] Explain the modes of operation of GP timers of F2407 DSP through neat timing diagrams. Briefly discuss their role for generation of PWM signals for inverter and converter systems. 4

5 Using bilinear transformation design IIR Butterworth Low Pass Filter with 3dB attenuation at a frequency of 2000 rad/sec and 14dB attenuation at 4818 rad/sec. The sampling frequency is 1kHz. Develop the IIR structure for direct structure-II realization. 8

6 Devise a scheme for closed speed control of BLDC motor. The PWM control of the inverter is realized through PWM timer. Draw a neat block diagram of the scheme employing F2407 DSP showing the sensed parameters (*current and speed*) of the system. Use PI controller (Rectangular approximation) for current estimation based on speed error. List out the different modules of the algorithm, and draw a neat detailed flowchart of the algorithm. Initialize all the F2407 DSP registers of the units utilized, to realize the PWM frequency of 10kHz, when CPU is clocking @150MHz. Use interrupts to configure the real time loop and for sampling the data. 8