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THIRD SEMESTER **B.Tech. (EP)**

SUPPLEMENTARY EXAMINATION ***February-2019***

EP-207: Digital Electronics

(Engineering Analysis and Design)

Time: 3:00 Hours ***Max. Marks : 40***

Note : Ques.1 is compulsory. Attempt 4 questions in all. All questions carry equal marks. Assume suitable missing data, if any.

Q.1. (a) Differentiate between Sequential Logic Circuit and a Combinational Logic Circuit. [2]

(b) Show how to connect NAND gates to get an AND gate and OR gate. [2]

(c) Compare SRAM and DRAM in terms of cost, size, speed and application. [2]

(d) A count recorded by a counter at its output is 1010. What is the time delay required for the next count change? Given: Turn On Delay = 30 ns and Turn Off Delay = 10 ns. [2]

(e) Describe Fan-In and Fan-out in context with the TTL Logic Families? [2]

Q.2. (a) Explain the working of a 4-bit Successive Approximation Analog to Digital Converter. Define Monotonicity with reference to ADC. [5]

(b) Perform the BCD Addition and XS-3 Addition of the following two numbers: 2256 and 1044. [5]

Q.3. (a) Design a non-sequential counter such that it generates the sequence of mentioned states (2,6,4,3) using D Flip-flops. Also check for the bush condition. [5]

(b) Design and discuss Bidirectional Shift Registers with a suitable example in each case of Left Shift and Right Shift. [5]

Q.4. (a) We can expand the word size of a RAM by combining two or more RAM chips. Draw a block diagram to show how we can use 8 x 4 RAM chips to obtain a 8 x 8 RAM. [5]

(b) Convert SR flip-flop to T flip-flop and obtain the conversion table, the corresponding logic diagram and the equations relating the input and outputs of the 2 flip-flops. [5]

Q.5. (a) Write a VHDL Code for 3 to 8 line decoder using DataFlow Modeling. [5]

(b) Implement the following function using a multiplexer:

$F(A, B, C, D) = \Sigma (0, 1, 3, 6, 7, 11, 15)$ [5]