VOLTAGE DIFFERENCING CURRENT CONVEYOR AND ITS APPLICATIONS IN IMPLEMENTATION OF AMPLIFIERS AND FILTERS

A

DISSERTATION

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IN
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Candidate's Declaration

I, **Robin Jain**, Roll No. **2K13/C&I/12**, student of **M.Tech** (**Control & Instrumentation**), hereby declare that the dissertation titled "**Voltage differencing current conveyor and its applications in implementation of amplifiers and filters**", under the supervision of **Prof. Pragati Kumar** of Electrical Engineering Department, Delhi Technological University, in partial fulfilment of the requirement for the award of the degree of Master of Technology, has not been submitted elsewhere for the award of any degree.

I hereby solemnly and sincerely affirm that all the particulars stated above by me are true and correct to the best of my knowledge and belief.

Place: Delhi **Robin Jain**

Date: .07.2015 **2K13/C&I/12**

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Certificate

This is to certify that the dissertation entitled **"Voltage differencing current conveyor and its applications in implementation of amplifiers and filters"** submitted by **Robin Jain** in completion of major project dissertation for Master of Technology degree in **Control and Instrumentation** at Delhi Technological University is an authentic work carried out by him under my supervision and guidance.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Place: Delhi
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Abstract

Ever since the introduction of current conveyors as basic building block in analog signal processing, many other active building blocks have been introduced so far. This has become possible because of the developments in the semiconductor manufacturing technologies (both bipolar as well as CMOS). During the last two decades various modifications have been done in the architecture of the current conveyor and many derivatives of this block have appeared in the literature. Voltage differencing current conveyor (VDCC) combines the features of a current conveyor and an operational transconductance amplifier. Voltage differencing current conveyor can be used to perform the entire regular signal processing applications (summation, differencing, scalar multiplication, amplifiers and filters etc.). The present work deals with the signal processing applications of the voltage differencing current conveyor in amplifiers and filters. A novel multifunction filter with tunability properties similar to the Tow-Thomas biquad filter has also been proposed. All the circuits presented in the dissertation have been simulated in PSPICE.

Contents

List of figures

List of tables

List of symbols, abbreviations

S.No.	Symbols	Descriptions
1.	g_m	Transconductance
2.	Z_i	Input Impedance
3.	V_i or V_{in}	Input Voltage
4.	V_o or V_{out}	Output Voltage
5.	I_i or I_{in}	Input Current
6.	I_o or I_{out}	Output Current
7.	V_{SS}	Source Supply Voltage
8.	V_{DD}	Drain Supply Voltage
9.	I_b	Bias Current
10.	VDCC	Voltage Differencing Current Conveyor
11.	OTA	Operational Transconductance Amplifier
12.	CDBA	Current Differencing Buffer Amplifier
13.	OMA	Operational Mirrored Amplifier
14.	CMOS	Complementary Metal Oxide Semiconductor
15.	DVCC	Differential Voltage Current Conveyor
16.	CC	Current Conveyor
17.	CCC	Current Controlled Conveyor
18.	CFOA	Current Feedback Operational Amplifier
19.	FTFN	Four Terminal Floating Nullor
20.	DDCC	Differential Difference Current Conveyor
21.	CFTA	Current Follower Transconductance Amplifier
22.	CDTA	Current Differencing Transconductance Amplifier
23.	Op-Amp	Operational Amplifier

24.	CCII	2^{nd} generation Current Conveyor
25.	DXCCII	Dual-X Current Conveyor
26.	VM	Voltage Mode
27.	CM	Current Mode
28.	THD	Total Harmonic Distortion
29.	TTF	Tow-Thomas Filter
30.	HPF	High Pass Filter
31.	LPF	Low Pass Filter
32.	BPF	Band Pass Filter
33.	KHN	Kerwin-Huelsman-Newcomb
34.	NIC	Negative Impedance Converter
35.	SISO	Single Input Single Output
36.	MISO	Multiple Input Single Output
37.	SIMO	Single Input Multiple Output
38.	MIMO	Multiple Input Multiple Output
39.	BW	Bandwidth
40.	Q	Quality Factor
41.	f_o	Pole Frequency or 3 dB Frequency
42.	IC	Integrated Circuit
43.	SR	Slew Rate
44.	GI	Grounded Inductor
45.	FI	Floating Inductor

Chapter 1
Introduction

1.1 Introduction:

The present work deals with voltage differencing current conveyor (VDCC) and its applications in implementation of amplifiers and filters in analog signal processing. There have been various major developments in the area of analog circuits and signal processing which have taken place during the past four decades. There is a bulk of material available about the various active blocks developed before current conveyors. In this dissertation we present voltage differencing current conveyor (VDCC) and its applications as amplifiers and filters in analog signal processing.

Introduction of current conveyor was imperative because of limitations posed by the traditional operational amplifier (op-amp) which is a highly versatile element. With op-amps, many circuits, both non-linear and linear, have been realized [1]. Extensive research has been carried out from mid-sixties to mid-eighties on the design of various non-linear and linear analog circuits using operational amplifiers. Since op-amp based circuits employ RC elements, their monolithic integrated circuit (IC) implementation was difficult because precise tuning of the time constant RC was difficult to implement. Moreover their limited performance due to less BW, slew rate (SR) etc. necessitated the lookout for other active blocks [2]. Switched capacitor circuit was the one solution where the resistor was replaced by a periodically switched capacitor but it posed problems like clock feed through and aliasing etc. [3].

In eighties, operational transconductance amplifier (OTA) was introduced. The OTA-C circuits employ only capacitors and transconductors to build several functional circuits and thus, don't require any resistors; moreover, their internal structure is also without resistor. In OTA circuits, the transconductance can be controlled electronically through an external DC bias voltage or current making its gain variable.

The developments in digital circuit design particularly, CMOS digital circuits, have led to concurrent developments in analog circuits. Several developments in the field of IC technology pose various challenges to the analog system with their fast growing digital counterparts. This has resulted in continued research on efficient analog circuit designs especially voltage-mode

(VM) and current-mode (CM) techniques and circuits for evolution of elegant and efficient solutions to many contemporary problems in mixed-mode circuit design problems.

1.2 Analog and digital signal processing:

The signal processing operations involved in many applications like communication systems, instrumentation, biomedical signal processing and control systems etc. can be implemented in two different ways

(1) Digital or discrete time method and

(2) Analog or continuous time method

The analog approach to signal processing was dominant for several years and it uses passive elements such as capacitors, resistors and active elements of various kinds viz BJTs, MOSFETs and different types of controlled sources realized with them. With the advent of digital computer and later microprocessor, the digital signal processing has become dominant these days. In analog signal processing, the solutions are obtained in real time. In contrast digital signal processing relies on numerical calculations. The method may or may not give results in real time. The digital approach has two main advantages over analog approach

(1) Repeatability: The same signal processing operation can be repeated again and again giving same results, while in analog systems there may be parameter variation due to change in temperature or supply voltage.

(2) Flexibility: Same hardware can be used to do several kind of signal processing operation, while in the core of analog signal processing one has to design a system for each kind of operation.

Digital signal processing has several other advantages like, better noise immunity than analog signals. They are much cheaper and compact than their analog counterpart. Digital signals can be encrypted so that only the intended receiver can decode it. It enables transmission of signals over a long distance and multi-directional transmission simultaneously [4].

Taking these advantages into account, we are forced to look for digital solutions rather than analog in VLSI systems. Not with standing these advantages, analog circuits are essential in many of today's complex, high performance systems. This is because the signals are analog in nature. Practically all signals in the physical world are continuous in both time and amplitude

and hence always analog techniques will be required for conditioning of such signals before they can be processed by digital signal processing circuits (sampling and quantization etc.). Therefore analog circuits act as a bridge between the real world and digital systems.

1.3 Voltage mode and current mode signal processing:

Over the past couple of decades the area of analog signal processing has been viewed in terms of the dominant variables of a circuit viz voltage and current. Any electrical circuit is always characterized by both 'current' and 'voltages'. The circuit in which the input as well as the output variables are voltages, has been referred to as voltage mode circuit. Similarly, the circuit in which the input as well as the output are current is generally called current mode circuit. The important features of these are given below [5].

Voltage mode circuits -

(i) The active elements used are of VCVS types.

(ii) The transistors being used in these devices generally are operated at higher values of biasing voltages.

(iii) There is a vast amount of literature available on various design techniques for amplifiers, filters and oscillators which were implemented using vaccum tubes.

(iv) The dynamic range of these circuits is limited by the biasing voltage and the forward drop of the conducting active devices.

(v) Limited high frequency operating range because of parasitics of the active devices being used.

(vi) Slew rate limitations because of the input differential amplifier in most of the voltage mode active devices.

Current mode circuits –

(i) The active elements used are VCCS/CCCS types.

(ii) Lower supply voltage operation is possible (±1.5V is a common supply voltage for CMOS devices).

(iii) Simple architecture of the overall circuit because of smaller number of components (current can be added without any external active devices).

(iv) Circuits have higher dynamic ranges (because the current and voltages are exponentially related in a BJT, thus the currents can change over 5-6 decades while the voltage change needed to achieve this is very small).

(v) Because of small voltage swings (of the order of few hundred millivolts) at different nodes of the circuit, the parasitic capacitors at these nodes become ineffective and thus high speed operation is possible.

1.4 Outline of the work presented in the dissertation:

In this dissertation, the first chapter covers the basic concepts of analog and digital signal processing. The voltage mode (VM) and current mode (CM) processing has also been discussed. The second chapter covers the basic description of VDCC and its applications in analog signal processing in implementation of amplifiers. In the third chapter, grounded inductors and floating inductors have been discussed and verified by filter design applications using PSPICE simulation. In the fourth chapter, single VDCC based biquad filters (LP, HP and BP) have been designed and simulated using PSPICE which verifies the workability of VDCC in analog signal processing. In the fifth chapter, we have proposed two multifunction biquad filters that are based on the use of two integrators connected in cascade in an overall feedback loop (KHN filter and Tow-Thomas filter) and simulated using PSPICE.

1.5 References:

1. Smith, K.C. and Sedra, A. S., “The current conveyor: a new circuit building block. IEEE Proc. CAS, 1968, vol. 56, no. 3, p. 1368-1369.
2. Dalibor Biolek, Raj Senani, Viera Biolkova, Zdenek Kolka,“Active elements for analog signal processing : Classification, Review and New Proposals” Radioengineering, Vol. 17, No. 4, December 2008.
3. Schaumann, R. and Valkenberg, M. E. “Design of Analog Filters”, Oxford University Press, 2004.
4. Igor M., “New Circuit Principles for Integrated Circuits”, Part 2: Special Function Blocks for Analog Current Signal Processing, PhD Thesis, Brno University of Technology, 2010.
5. Analog IC Design: The Current-Mode Approach.

Chapter 2

Voltage differencing current conveyor and its general applications

2.1 Introduction:

In this present chapter we discuss in detail about an active building block namely voltage differencing current conveyor (VDCC) and its application in signal processing as amplifiers and impedance converters. This active device was first proposed by Biolek, Senani, Biolkova and Kolka [1].

A CMOS implementation of VDCC has been proposed by Kacar, Yesil, Minaei and Kuntman [2]. It transfers both voltage and current to its relevant terminals. It is suitable for the design of several active filters, biquads, grounded and floating inductor simulators etc.

This chapter deals with the CMOS implementation of VDCC given in [2]. The complete characterization of VDCC using TSMC CMOS 0.18μm process technology has been presented here. The following applications have also been presented-

(i) Voltage amplifier
(ii) Current Amplifier
(iii) Transresistance amplifier
(iv) Transconductance amplifier
(v) Negative impedance converter (NIC)

PSPICE simulations have been carried out to verify the workability of all these circuits.

2.2 Voltage differencing current conveyor (VDCC):

2.2.1 Block diagram representation of VDCC:

The circuit symbol of the active element VDCC is shown in figure 2.1, where N and P are input terminals and Z, X, W_P and W_N are output terminals of VDCC. All these terminals exhibit high impedance, except the X terminal [2].

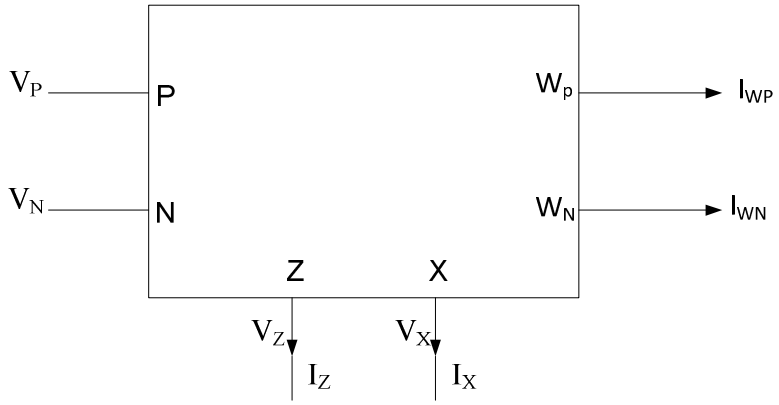


Figure 2.1 Block diagram of VDCC [2]

The port relations of an ideal VDCC shown in figure 2.1 can be characterized by

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \tag{2.1}$$

Above matrix equation shows that the first stage is realized by a balanced operational transconductance amplifier (OTA) to convert the input voltages differences ($V_P - V_N$) into the output current (I_Z) with transconductance gain of g_m and the second stage is realized by a current conveyor (CC) to transfer the X-terminal current to W_N and W_P terminals. For a balanced CMOS transconductance amplifier (OTA) the parameter g_m can be given as

$$g_m = \sqrt{I_{B1}\mu_n C_{ox}(\frac{W}{L})_1} \tag{2.2}$$

where C_{OX} is the gate-oxide capacitance per unit area, μ_n is the mobility of the carrier for NMOS transistors, L is the effective channel length, W is the effective channel width, and I_{B1} is bias current [2].

VDCC is an active block which is the combination of OTA and MOCCII as shown in figure 2.2.

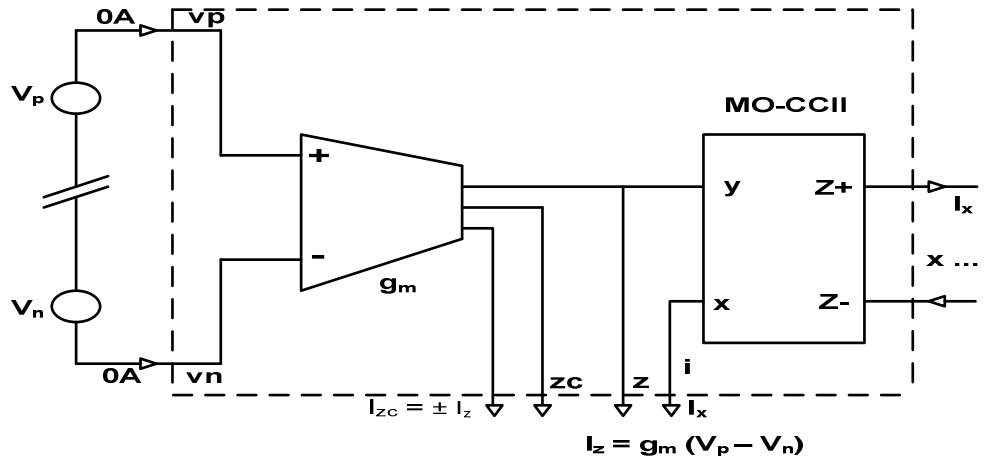


Figure 2.2 Internal structure of VDCC [1]

2.2.2 CMOS implementation of the VDCC:

CMOS realization of voltage differencing current conveyor (VDCC) is shown in figure 2.3 which has been simulated using model parameters shown in appendix.

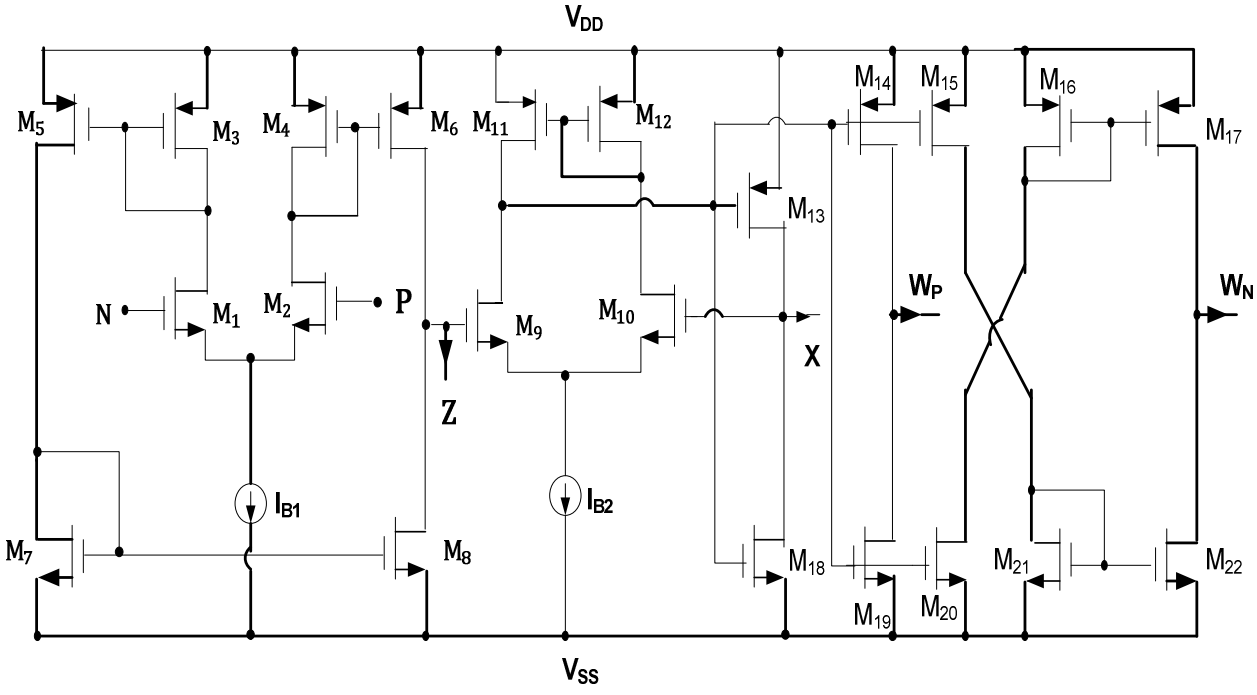


Figure 2.3 COMS implementation of the VDCC [2]

2.2.3 Simulation results:

The CMOS schematic diagram is shown in figure 2.3, which was simulated in PSPICE using TMSC CMOS 0.18 µm process model parameters. The aspect ratios of the MOS transistors are given in table 2.1. The supply voltages are chosen as V_{DD} = -V_{SS} = 0.9 V, I_{B1} = 50 µA and I_{B2} = 100 µA. The following analysis has been carried out

(i) DC sweep (to obtain the linearity for various current and voltage transfers) (fig.2.4 to fig.2.6)

(ii) AC sweep (to obtain the bandwidth of the device) (figure 2.7 to figure 2.9)

(iii) Transient analysis (figure 2.10)

The terminating impedances used in characterization of the VDCC were R_Z = 12KΩ, R_X = 5KΩ, R_{WP} = 5 KΩ, R_{WN} = 5KΩ. The input signal was taken as 50mV applied at P terminal and N terminal was grounded.

Table 2.1 Aspect ratios for the VDCC of figure 2.3 [2]

Transistors	W/L (µm)
$M_1 – M_4$	3.6/1.8
$M_5 – M_6$	7.2/1.8
$M_7 – M_8$	2.4/1.8
$M_9 – M_{10}$	3.06/0.72
$M_{11} – M_{12}$	9/0.72
$M_{13} – M_{17}$	14.4/0.72
$M_{18} – M_{22}$	0.72/0.72

Different parameters are obtained by PSPICE simulation of VDCC are listed as

Transconductance g_m = 273.13 µA/V

Power consumption = 0.846 mW

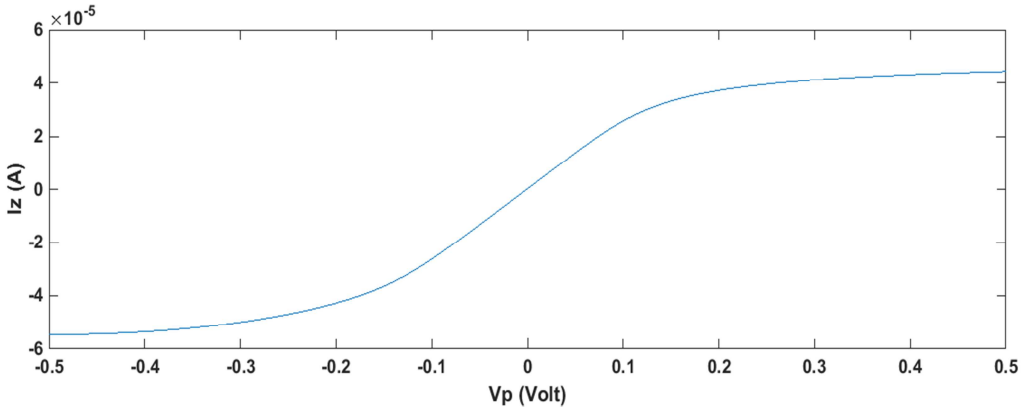


Figure 2.4 DC characteristic of current at Z terminal of VDCC

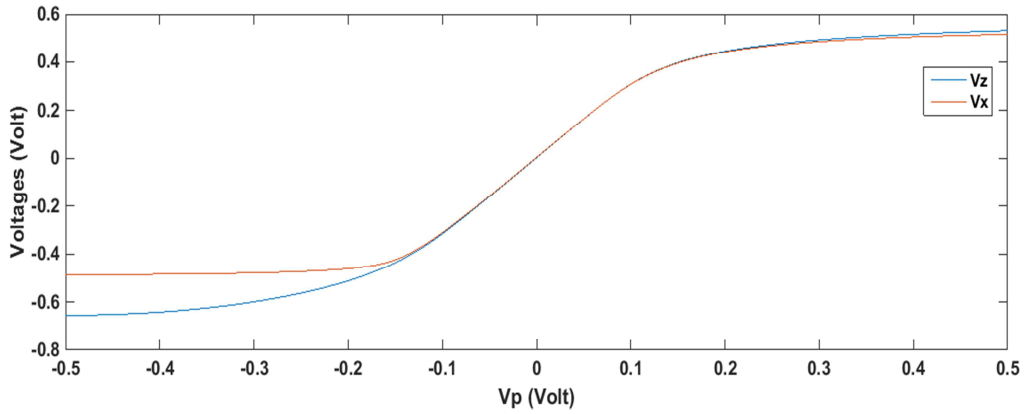


Figure 2.5 DC characteristics of voltage at Z and X terminal of VDCC

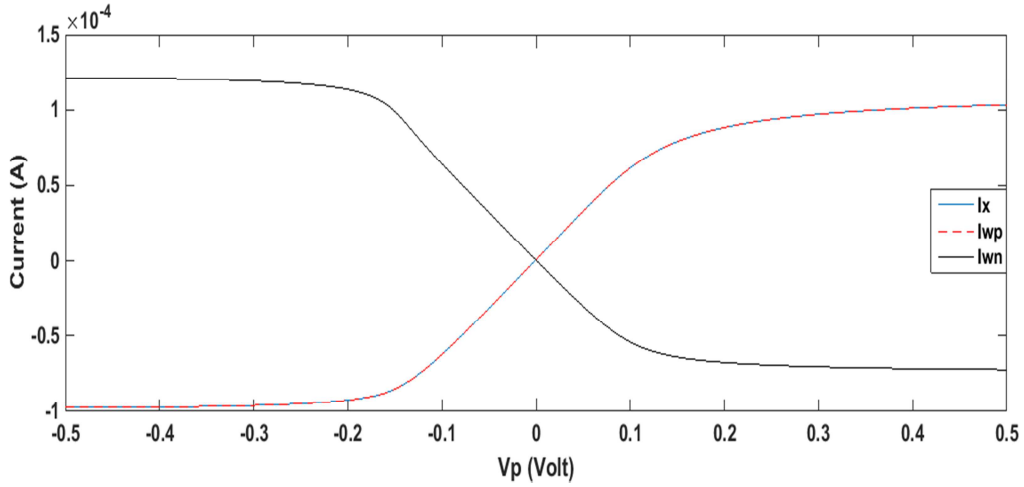


Figure 2.6 DC characteristics of current at X, W_P and W_N terminal of VDCC

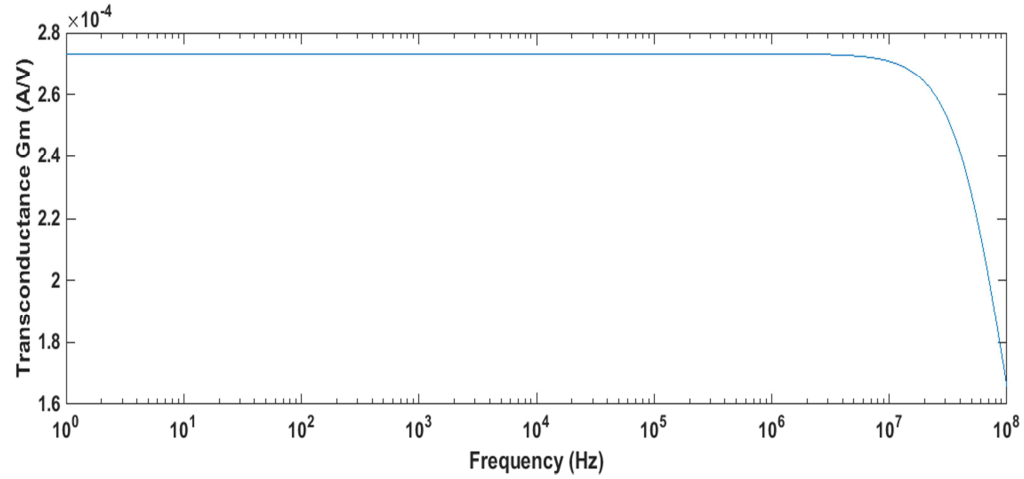


Figure 2.7 Input AC characteristic (transconductance) of VDCC

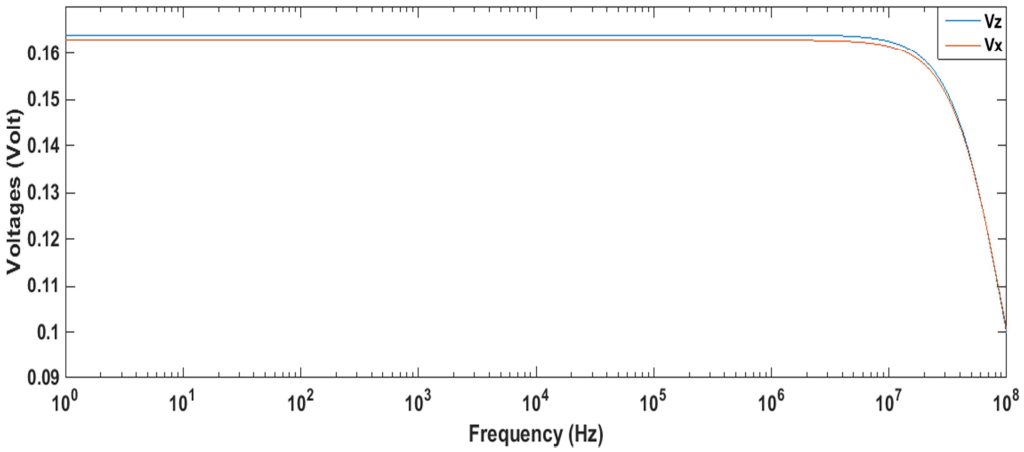


Figure 2.8 AC characteristic of voltage at Z and X terminal of VDCC

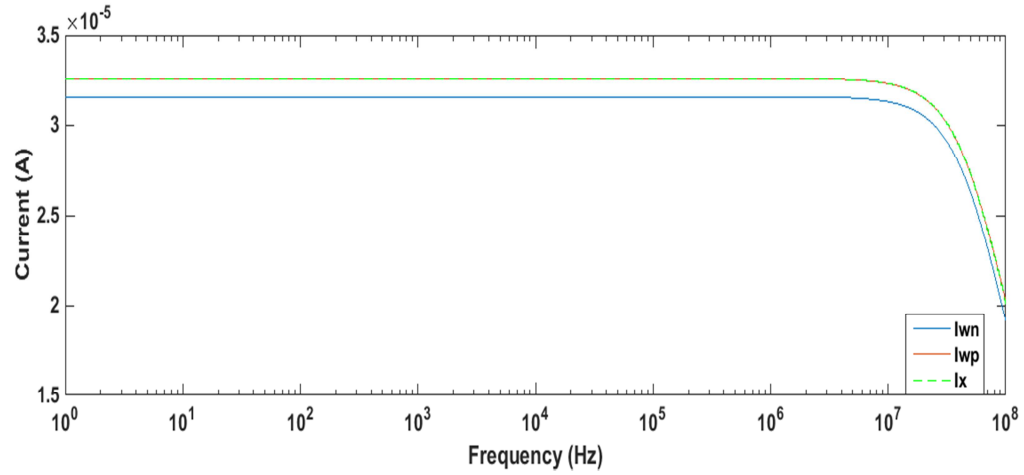
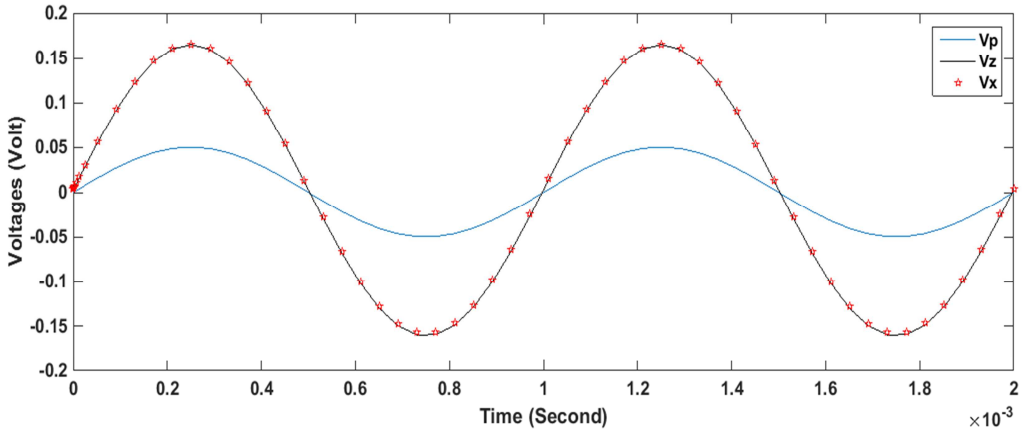
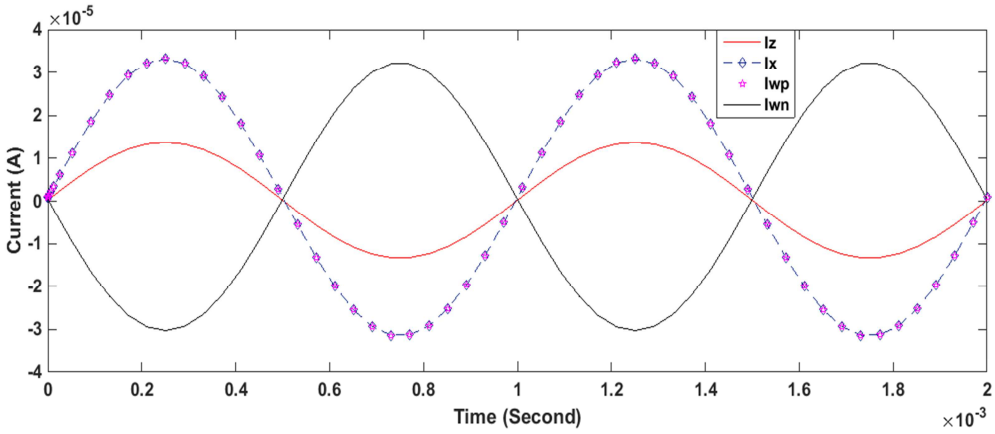


Figure 2.9 AC characteristic of current at X, W_P and W_N terminal of VDCC



(a)



(b)

Figure 2.10 Transient analysis of all terminals of VDCC

2.3 Application of VDCC as an amplifier:

An amplifier gives the output that is scaled version of an input signal. Broadly, it can be classified on the basis of their circuit configuration and methods of operation. In real world, sensors like thermocouple, piezo-electric etc. have small output signal. So by using amplifier their outputs can be amplified to drive the further circuitry such as lamp etc.

Gain is basically the ratio of the output divided by the input. An amplifier can be classified on the basis of polarity of input and output. In non-inverting amplifier, output signal has same sign to the input signal. Similarly, inverting amplifier gives polarity of the output signal opposite to the input signal.

2.3.1 Current amplifier and transresistance amplifier:

VDCC based current amplifier is shown in figure 2.11. In this circuitry, if W_P is used as a output terminal then it is called as non-inverting current amplifier. In contrast, if W_N is used as a output terminal then its characteristic likes an inverting current amplifier. By using single VDCC, it can be designed for the both inverting and non-inverting amplifier but this case is not found in the Op-amp. In the case of operational amplifiers, separate circuit is designed for both types of amplifier. So, the main advantage of VDCC based current amplifier is that only choosing the output terminal gives the opposite polarities i.e. non-inverting and inverting characteristics. VDCC based amplifier has also some other advantages over operational amplifier based

amplifier circuits such as less power consumption, high slew rate, large bandwidth and less power supply requirement etc. [2].

A simplified current amplifier circuit of figure 2.11 is shown in figure 2.12. In this, OTA is used as a resistor which gives the less use of passive elements and also provides electronic tunability. Current gain is the ratio of output current to the input current. The current gain for the figure 2.11 is described as follows-

For non-inverting amplifier –

$$\frac{I_{WP}}{I_i} = \frac{g_m R_1 R_2}{R_3} \tag{2.3}$$

For inverting amplifier –

$$\frac{I_{WN}}{I_i} = -\frac{g_m R_1 R_2}{R_3} \tag{2.4}$$

The current gain for the figure 2.12 is defined as follows -

For non-inverting amplifier -

$$\frac{I_{WP}}{I_i} = \frac{1}{g_m R} \tag{2.5}$$

For inverting amplifier –

$$\frac{I_{WN}}{I_i} = -\frac{1}{g_m R} \tag{2.6}$$

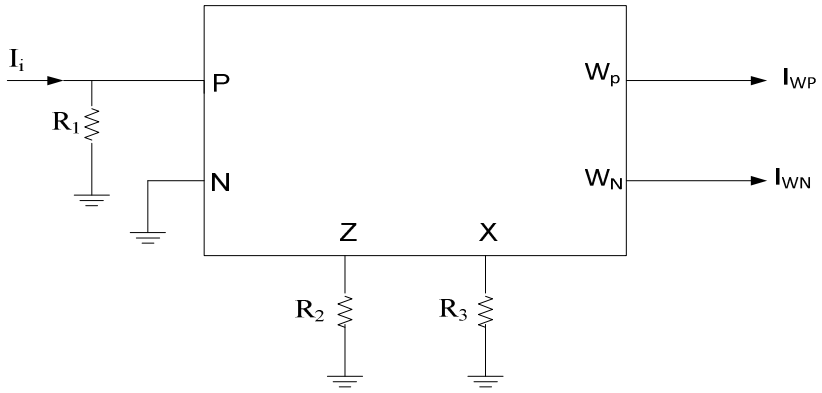


Figure 2.11 VDCC based current amplifier

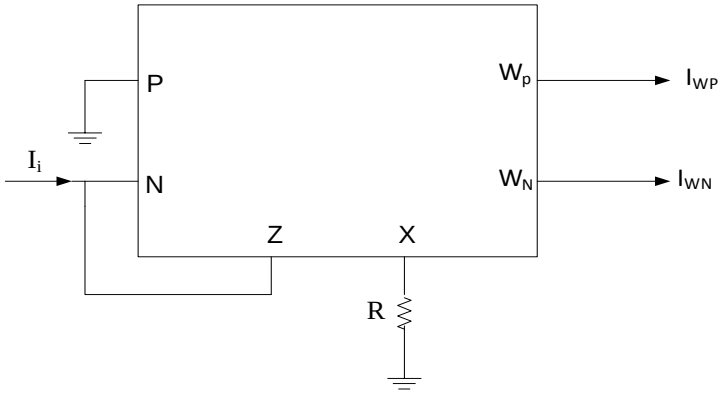


Figure 2.12 Simplified current amplifier using VDCC

Transresistance gain is the ratio of output voltage to the input current. If output is taken at X terminal in terms of voltage then it is called as transresistance amplifier. The transresistance gain for figure 2.11 is given by

$$\frac{V_X}{I_i} = g_m R_1 R_2 \tag{2.7}$$

From figure 2.11, it is clear that we can get two types of amplifiers from single circuit i.e. current amplifier and transresistance amplifier. This is the unique advantage of VDCC.

2.3.1.1 Simulation results:

The amplifier shown in figure 2.11 and 2.12 were simulated in PSPICE. The bias currents are taken as I_{B1} = 50µA (g_m = 273.13µA/V) and I_{B2} = 100µA. The value of resistors are taken as R_1 = 11KΩ, R_2 = 8KΩ, R_3 = 8KΩ in figure 2.11 which indicate current gain equals to 3 and transresistance gain is equals to 24KΩ. The time and frequency responses of the figure 2.11 as current amplifier are shown in figure 2.13 and figure 2.14 respectively. Similarly, frequency response of the figure 2.11 as transresistance amplifier is shown in figure 2.15.

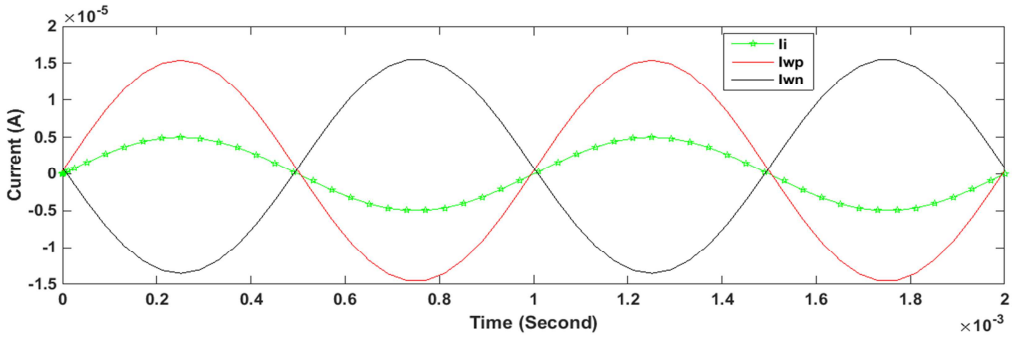


Figure 2.13 Time response of current amplifier circuit shown in figure 2.11

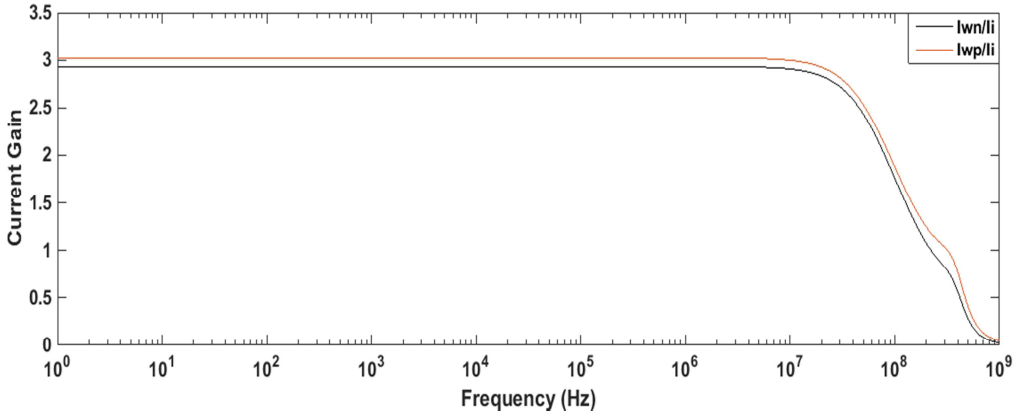


Figure 2.14 Frequency response of the current amplifier shown in figure 2.11

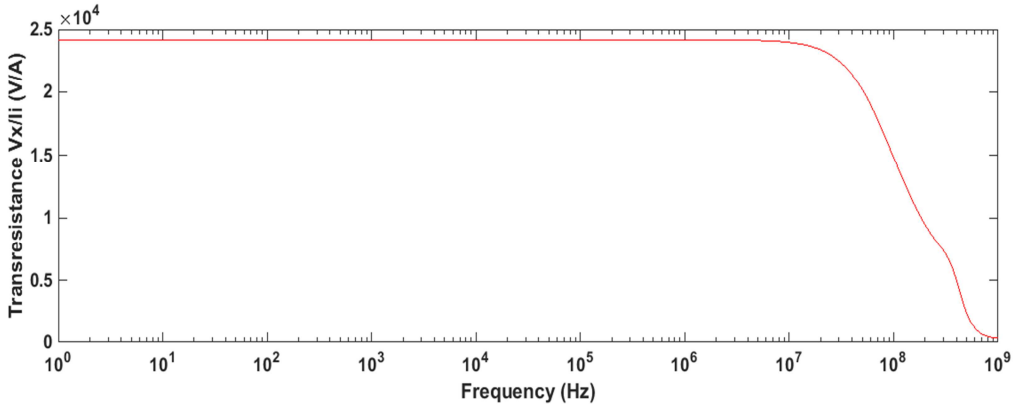


Figure 2.15 Frequency response of the transresistance amplifier shown in figure 2.11

The value of resistor was taken as R = 1.22KΩ in figure 2.12 which indicate current gain equals to 3. The time and frequency responses of the figure 2.12 are shown in figure 2.16 and figure 2.17 respectively.

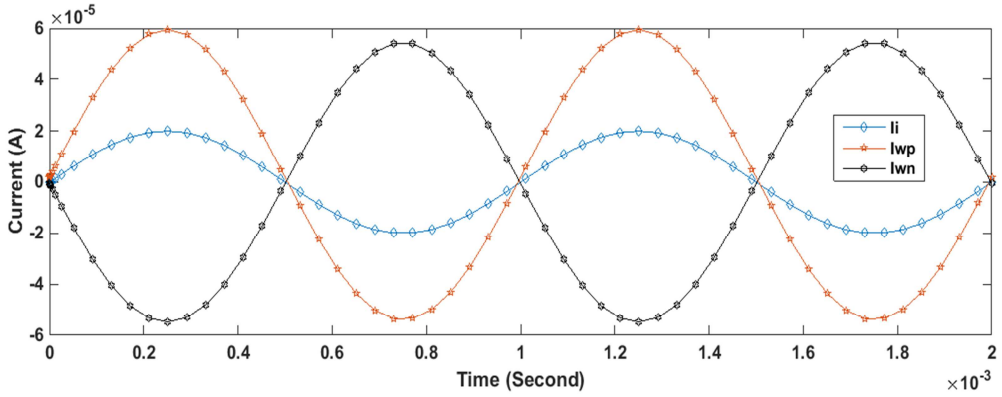


Figure 2.16 Time response of current amplifier circuit shown in figure 2.12

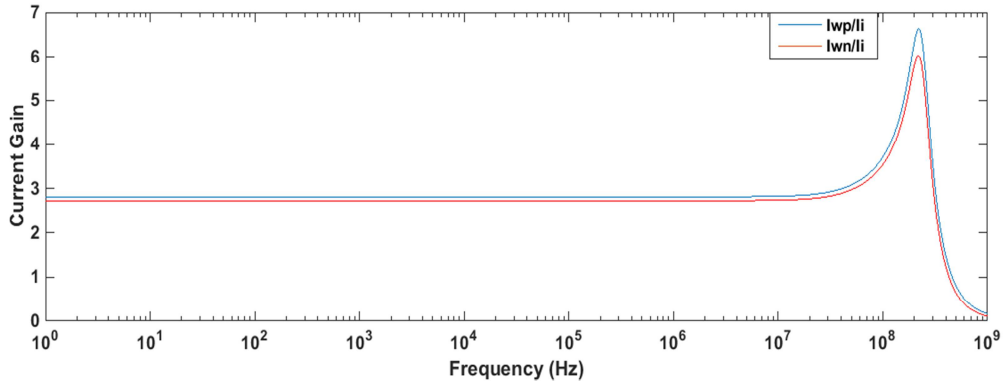


Figure 2.17 Frequency response of current amplifier circuit shown in figure 2.12

2.3.2 Transconductance amplifier and voltage amplifier:

VDCC based transconductance amplifier is shown in figure 2.18. The transconductance gain is the ratio of output current to the input voltage. The transconductance gain is described as follows For non-inverting amplifier –

$$\frac{I_{WP}}{V_i} = \frac{g_m R_1}{R_2} \tag{2.8}$$

For inverting amplifier -

$$\frac{I_{WN}}{V_i} = -\frac{g_m R_1}{R_2} \tag{2.9}$$

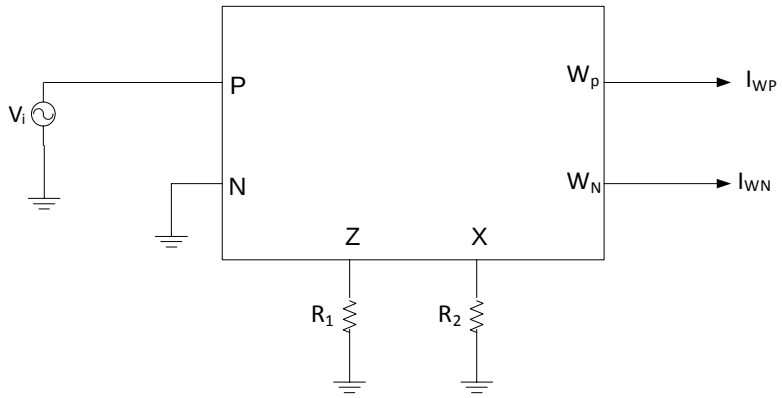


Figure 2.18 VDCC based transconductance amplifier

Voltage gain is the ratio of output voltage to the input voltage. If output is taken at X terminal in terms of voltage then it is called as voltage amplifier. The voltage gain for figure 2.18 is given by

$$\frac{V_X}{V_i} = g_m R_1 \tag{2.10}$$

From figure 2.18, it is clear that we can get two types of amplifiers from single circuit i.e. voltage amplifier and transconductance amplifier. This is also the unique advantage of VDCC.

2.3.2.1 Simulation results:

The amplifier shown in figure 2.18 was simulated in PSPICE. The bias currents are taken as I_{B1} = 50µA (g_m = 273.13µA/V) and I_{B2} = 100µA. The value of resistors are taken as R_1 = 11KΩ, R_2 = 11KΩ in figure 2.18 which indicate voltage gain equals to 3 and transconductance gain is equals to 273.13µA/V. The time and frequency responses of the figure 2.18 as voltage amplifier are shown in figure 2.19 and figure 2.20 respectively. Similarly, time and frequency response of the figure 2.18 as transconductance amplifier is shown in figure 2.21 and figure 2.22.

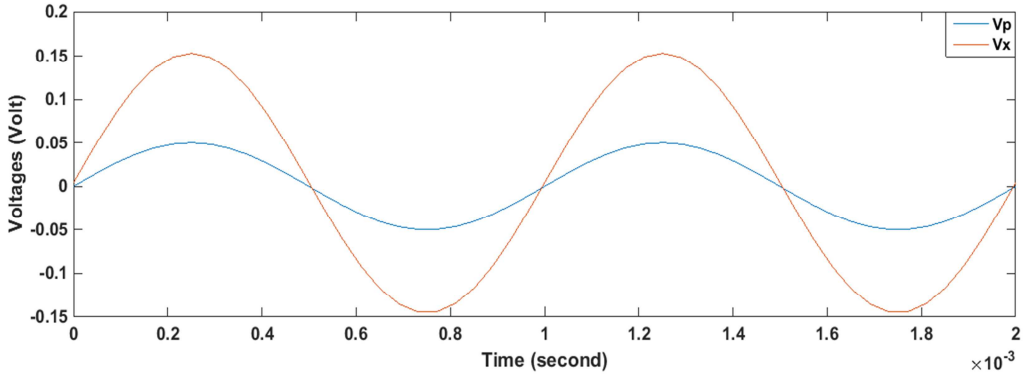


Figure 2.19 Time response of voltage amplifier circuit shown in figure 2.18

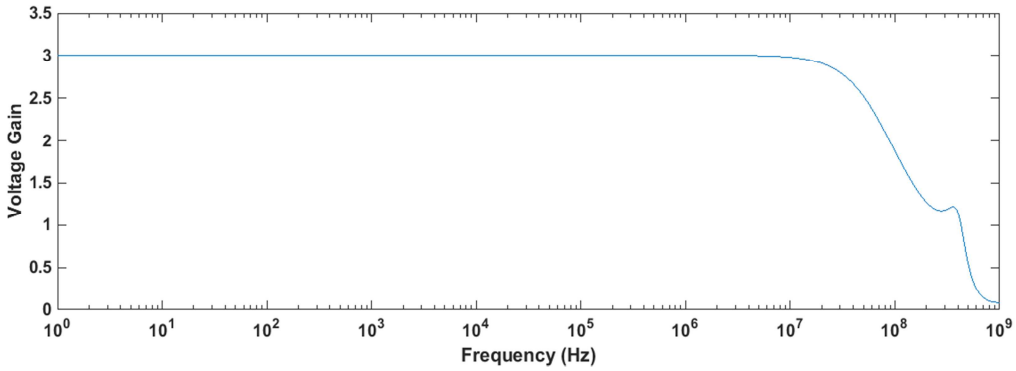


Figure 2.20 Frequency response of the voltage amplifier shown in figure 2.18

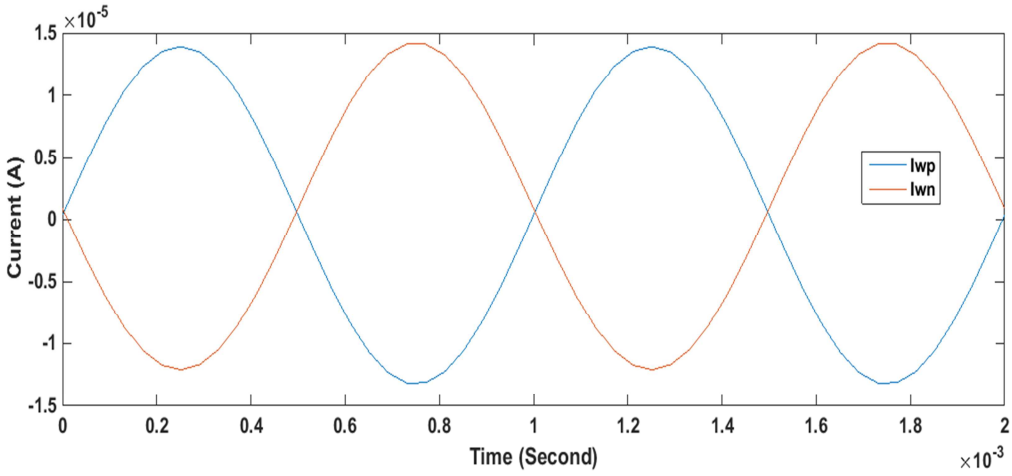


Figure 2.21 Time response of the transconductance amplifier circuit

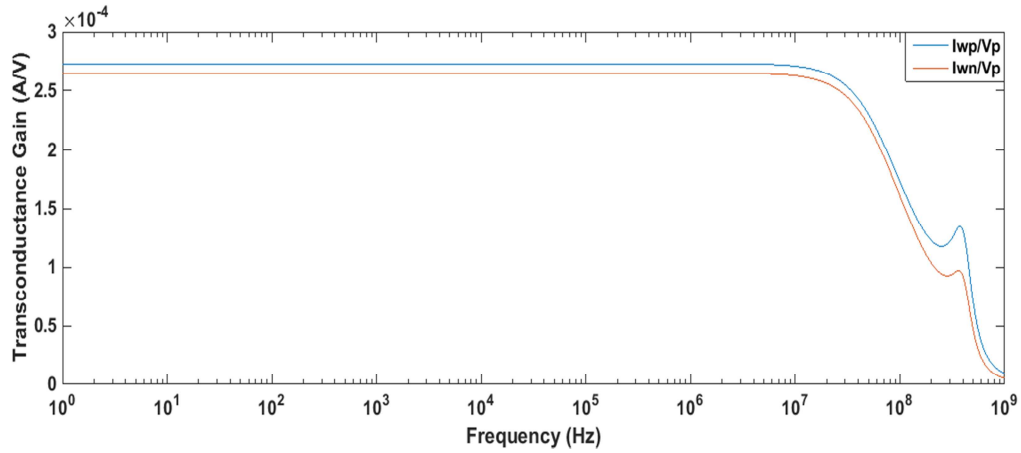


Figure 2.22 Frequency response of the transconductance amplifier circuit

2.4 Applications of VDCC as negative impedance converter (NIC):

A negative impedance converter (NIC) is a suitable building block in synthesis of several biquads, including notch filter [3]. The implementation of NIC using VDCC is shown in figure 2.23.

From figure 2.23, it is clear that the impedance transfer is

$$Z_{in} = -\frac{Z_L}{g_m Z_1} \tag{2.11}$$

If we take $Z_1 = \frac{1}{g_m}$ then the impedance transfer is

$$Z_{in} = -Z_L \tag{2.12}$$

By changing the input and output, we find that NIC is reciprocal**.**

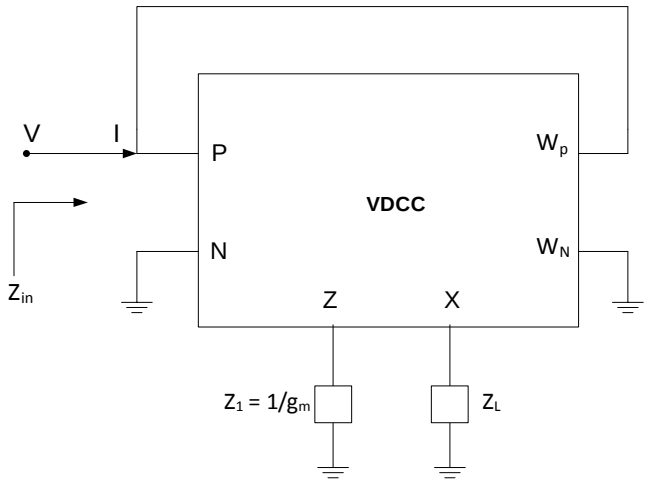


Figure 2.23 Negative impedance converter using VDCC

2.4.1 Simulation results:

The NIC shown in figure 2.23 was simulated in PSPICE. The bias currents are taken as I_{B1} = 50μA (g_m = 273.13μA/V) and I_{B2} = 100μA. The value of impedances are taken as $Z_1 = 1/g_m$ = 3.66KΩ, Z_L = 3KΩ which indicate Z_{in}= -Z_L= -3KΩ. By PSPICE simulation we get the slope of V-I curve equals to 2.91KΩ which is nearly equal to theoretical value. Figure 2.24 shows the voltage current curve for NIC. Figure 2.25 shows the variations of current through input voltage due to bias current I_{B1}.

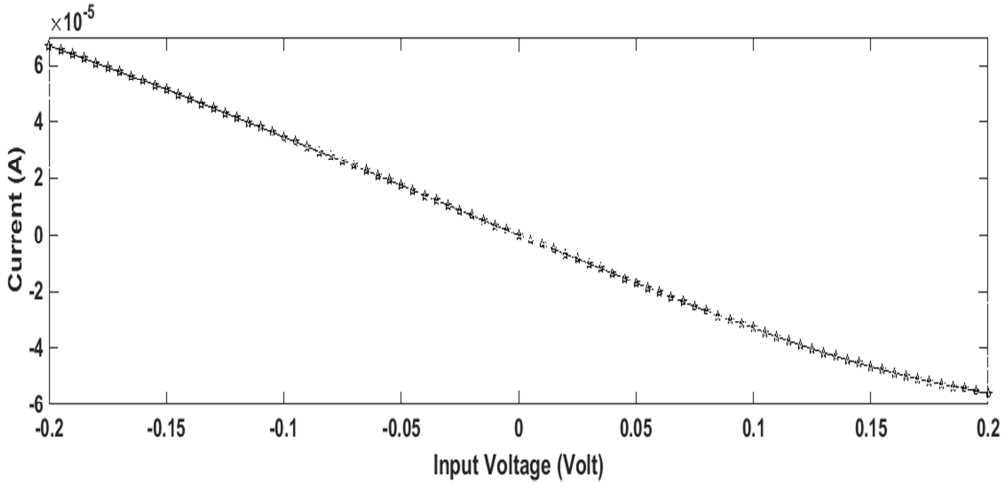


Figure 2.24 V-I curve for NIC

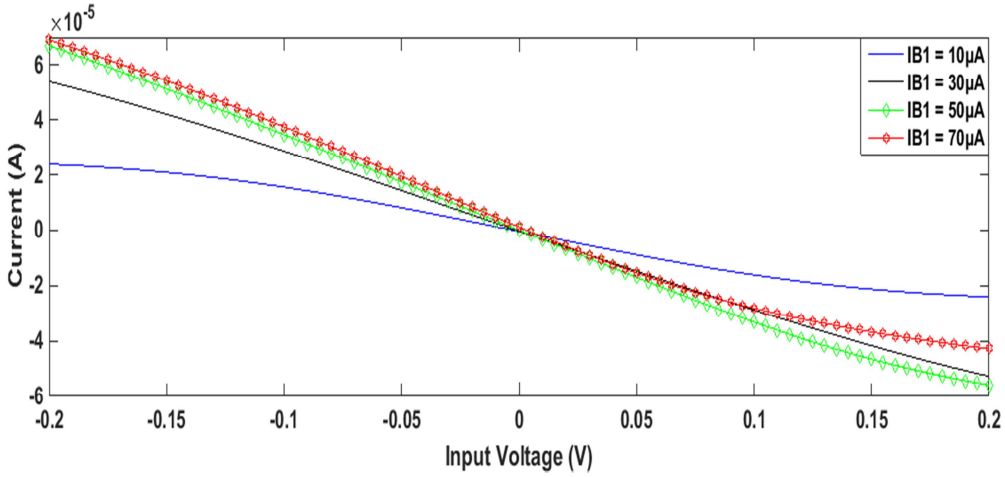


Figure 2.25 Variations of current through input voltage due to bias current I_{B1}

2.5 Conclusion:

A novel active building block namely VDCC has been discussed in detail in this chapter. Its DC and AC characteristics of input-output have been verified using PSPICE simulation. The basic signal processing applications such as amplifiers and negative impedance converter were designed using VDCC and simulated in PSPICE.

2.6 References:

1. Dalibor Biolek, Raj Senani, Viera Biolkova, Zdenek Kolka,"Active elements for analog signal processing : Classification, Review and New Proposals" Radioengineering, Vol. 17, No. 4, December 2008.
2. Firat Kacar, Abdullah Yesil, Shahram Minaei, Hakan Kuntman, "Positive/Negative lossy/lossless grounded inductance simulators employing single VDCC and only two passive elements" Int. J. Electron. Commun. (AEU) 68 (2014) 73-78.
3. Tomas Dostal, Vladimir Axman, "Biquads based on single negative impedance converter implemented by classical current conveyor", Radioengineering, Vol. 16, No. 3, September 2007.
4. Dinesh Prasad, Javed Ahmad, "New electronically-controllable lossless synthetic floating inductance circuit using single VDCC", Scientific Research, Circuits and Systems, 2014, 5, 13-17, January 2014.

Chapter 3
Grounded and floating inductor realization using VDCC and its application as higher order Butterworth filter

3.1 Introduction:

This chapter deals with electronically-controllable lossless grounded inductance (GI) and floating inductance (FI) simulators employing only one voltage differencing current conveyor (VDCC), one grounded capacitor and one grounded resistor.

For signal processing at low to medium frequencies, passive inductors are not preferred for integrated circuit realization. Besides being bulky, their quality factor is also very poor. Thus inductors are simulated rather than integrated on the IC.

Many simulated grounded inductors (GI) and floating inductor (FI) simulator circuits using different active elements such as op-amps, CCs, CCCIIs, CFOAs, FTFNs, OMAs, DVCCs, DDCCs, CDBAs, CFTAs, CDTAs, OTA, combination of CC and OTA and DXCCII have been proposed, but they suffer from following drawbacks [2]:

I. requirement for passive component matching conditions,
II. realizing only lossy or negative inductance simulator,
III. use of excessive number of active components and
IV. use of at least three passive elements.

Recently, several active devices have been introduced in [1], where VDCC is one of them. VDCC provides electronically tunable transconductance gain. It also transfers both voltage and current to its relevant terminals. It is very suitable for the design of several inductor simulators, amplifiers and active filters.

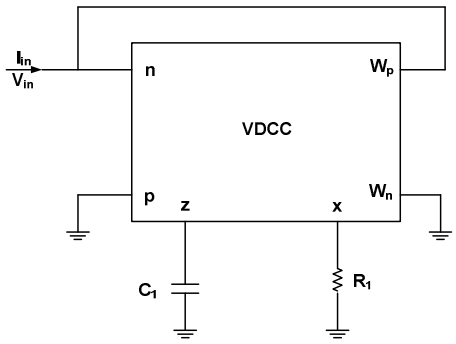
With the help of grounded inductor simulator, a 4^{th} order butterworth HPF circuit has been realized and using floating inductor simulator, a 4^{th} order butterworth LPF circuit and 2^{nd} order BPF circuit have been realized. The validity of these circuits has been verified using PSPICE simulations with TSMC CMOS 0.18μm process parameters [2].

3.2 VDCC based grounded inductor:

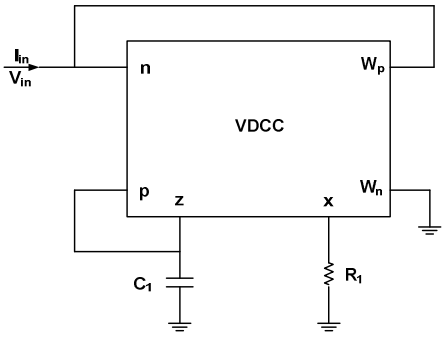
Grounded inductance realization circuits using VDCC are shown in figure 3.1. All these circuits are designed with single VDCC, one grounded capacitor and one grounded resistor. Using routine circuit analysis of all these circuits, the equivalent inductance, equivalent resistance and input impedance can be found which is given in table 3.1, where negative simulated inductor is used for many applications like active filters, impedance matching in microwave circuits, designing of oscillators and analog phase shifter etc. [2].

Table 3.1 Grounded inductance realizable forms [2]

Circuit	Z_{eq} (input impedance)	L_{eq} (equivalent inductance)	R_{eq} (equivalent resistance)	Type
Fig. 3.1(a)	sC_1R_1/g_m	C_1R_1/g_m	-	Pure +L
Fig. 3.1(b)	$-sC_1R_1/g_m$	$-C_1R_1/g_m$	-	Pure –L
Fig. 3.1(c)	$sC_1R_1/g_m + R_1$	C_1R_1/g_m	R_1	+L series with +R
Fig. 3.1(d)	$sC_1R_1/g_m - R_1$	C_1R_1/g_m	$-R_1$	+L series with -R
Fig. 3.1(e)	$-sC_1R_1/g_m + R_1$	$-C_1R_1/g_m$	R_1	-L series with +R
Fig. 3.1(f)	$-sC_1R_1/g_m - R_1$	$-C_1R_1/g_m$	$-R_1$	-L series with -R



(a)



(d)

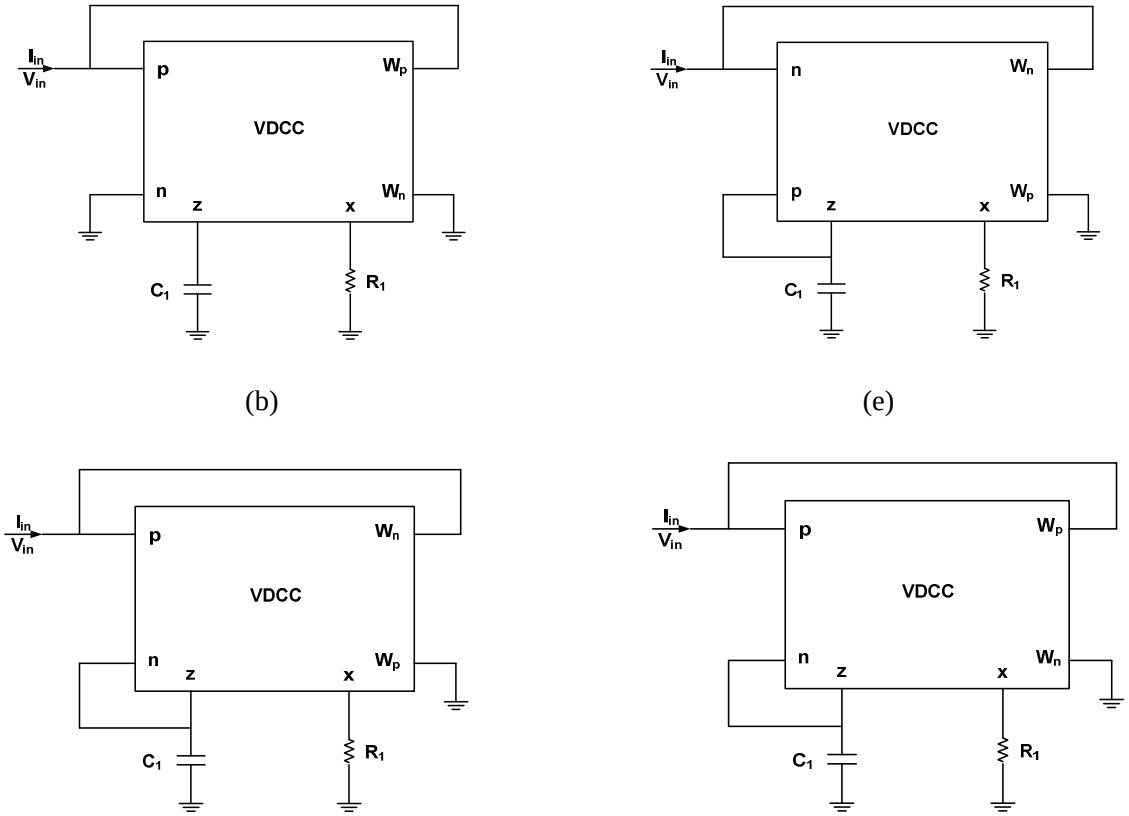


Figure 3.1 Grounded inductance realized using single VDCC [2]

3.2.1 Simulation results for lossless grounded inductor:

The circuit shown in figure 3.1 (a) and (b) were simulated with the following passive elements value: R_1 = 1KΩ and C_1 = 80pF, taking I_{B1}=50µA and I_{B2}=100µA which results in g_m=273.13µS and L_{eq} = ±0.29mH. The simulation results are shown in figure 3.2 and figure 3.3 respectively. It can be seen that simulated value of inductance is constant with frequency and is approximately equal to theoretical value of inductance.

Figure 3.4 exhibits the tuning property of the VDCC based grounded inductance circuit given in figure 3.1(a). Variation of the inductance value by changing I_{B1} as 10µA (L=0.75mH), 30µA (L=0.37mH) and 60µA (L=0.26mH) is shown in figure 3.4. Hence, it is cleared that the tuning of the inductance value can be performed easily via the control current I_{B1}.

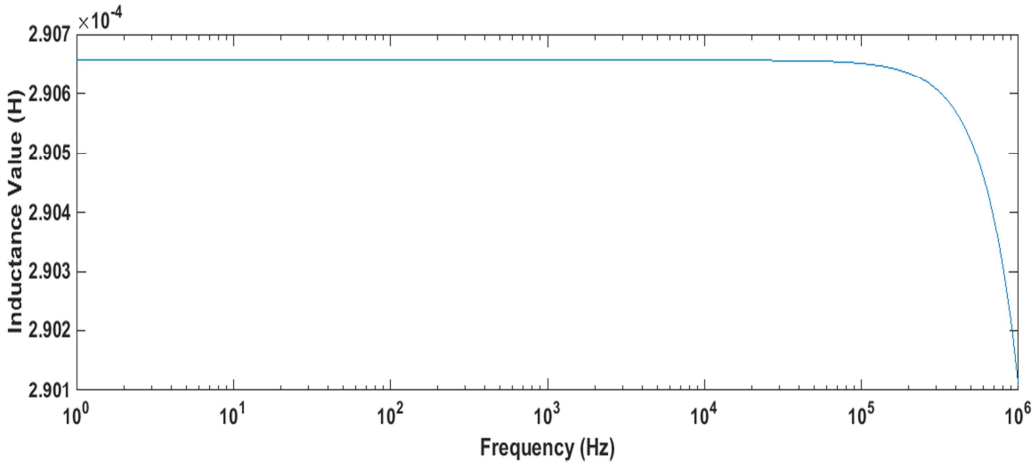


Figure 3.2 Inductor simulation of figure 3.1(a)

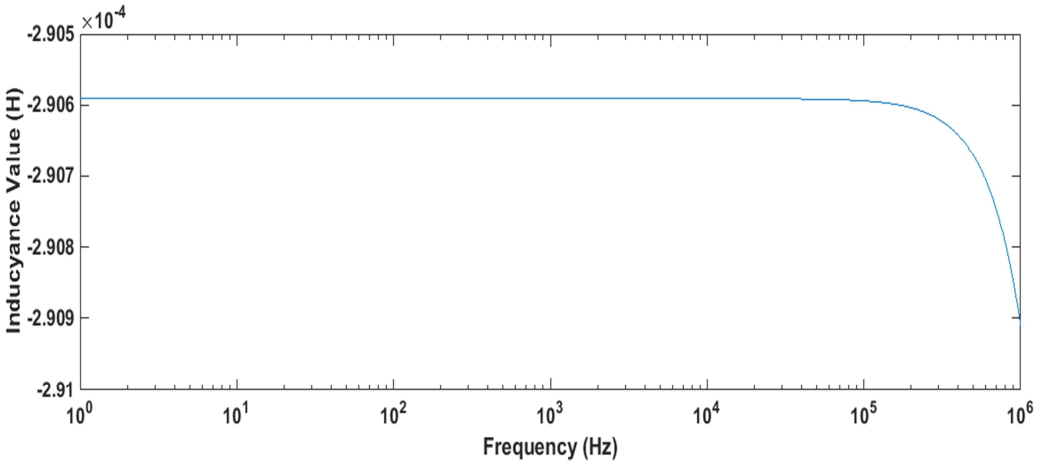


Figure 3.3 Inductor simulation of figure 3.1(b)

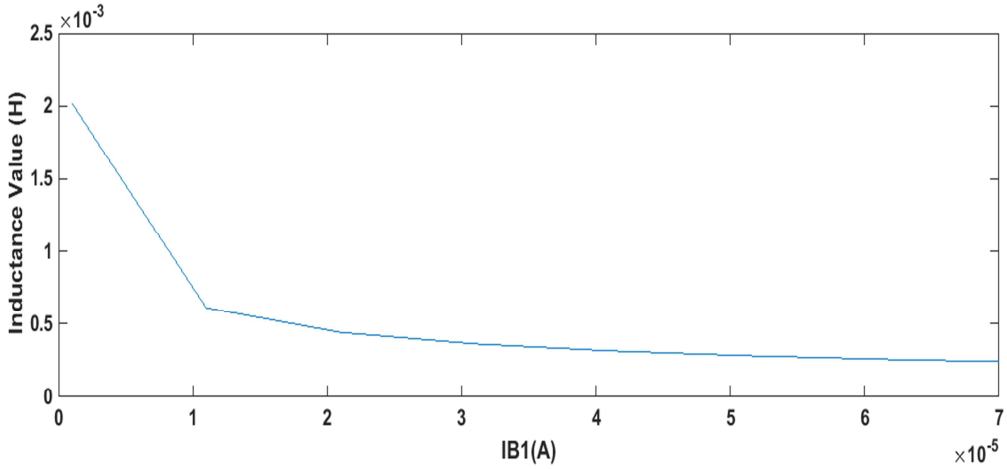


Figure 3.4 Inductance value variation with the bias current I_{B1}

3.3 4th order high pass Butterworth ladder filter:

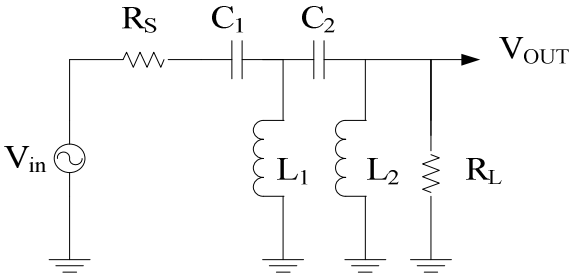
Passive prototype of the 4th order high pass butterworth filter is shown in figure 3.5(a). In this circuit, grounded inductors are used which can be replaced by the simulated inductance. The VDCC based simulated grounded inductance is shown in figure 3.1(a) which is used to design a 4th order HPF as shown in figure 3.5(b).

The transfer function for 4th order high pass butterworth filter is given by

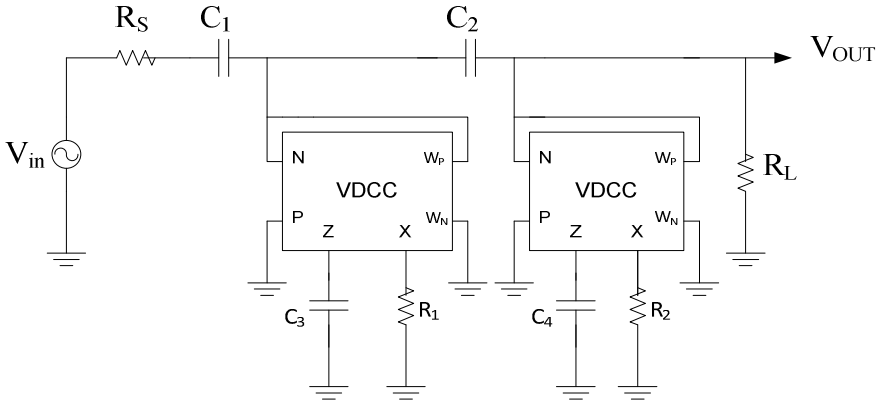
$$\frac{V_{out}}{V_{in}} = \frac{s^4}{s^4\left(1+\frac{R_S}{R_L}\right)+s^3\left(\frac{R_S}{L_1}+\frac{R_S}{L_2}+\frac{1}{R_LC_2}+\frac{1}{R_LC_1}\right)+s^2\left(\frac{1}{L_1C_1}+\frac{1}{L_2C_1}+\frac{1}{L_2C_2}+\frac{R_S}{R_LC_2L_1}\right)+s^1\left(\frac{1}{L_1C_2R_LC_1}+\frac{R_S}{L_2C_2L_1}\right)+\frac{1}{C_1C_2L_1L_2}} \quad (3.1)$$

Where $L_1 = \frac{R_1C_3}{g_{m1}}$ and $L_2 = \frac{R_2C_4}{g_{m2}}$

g_{m1} and g_{m2} are transconductances of two VDCC blocks respectively.



(a)



(b)

Figure 3.5 4th order HP butterworth ladder filter (a) Passive prototype

(b) VDCC based GI simulator based realization circuit

3.3.1 Simulation results:

To design the circuit for a pole frequency of 1MHz with butterworth characteristics, the normalized design (f_0 = 1Hz) was obtained with the following components values -

$R_L = R_S = 1\Omega$, $C_1 = 0.2768F$, $C_2 = 0.0780F$, $L_1 = L_2 = 0.1217H$

The passive elements are selected as $R_L = R_S = 2K\Omega$ and $C_1 = 0.1384nF$, $C_2 = 0.03nF$ and $L_1 = L_2 = 0.2434mH$ (by applying magnitude scaling and frequency scaling in normalized design) which results in pole frequency of 1MHz. The inductance of figure 3.1(a) was used to design a 4^{th} order high-pass butterworth filter. The performance of simulated grounded inductance has been verified by taking $R_1 = 1K\Omega$, $C_1 = 69.65pF$ and $g_m = 283.8\mu A/V$ ($I_{B1} = 65\mu A$, $I_{B2} = 100\mu A$) in figure 3.1(a), which results in $L_1 = L_2 = 0.243mH$. The simulated inductor result is shown in figure 3.6.

The frequency response of 4^{th} order high pass butterworth filter is shown in figure 3.7 which has pole frequency of 995 KHz which is close to 1MHz. The transient analysis is shown in figure 3.8. For the testing of the input dynamic range of the 4^{th} order HPF, sinusoidal signal of f_0 = 1MHz with different amplitudes are applied to the input. The total harmonic distortion of the output signal versus amplitude of the input signal is shown in figure 3.9. The result shows that for input signal with amplitude lower than 300mV peak-to-peak, the THD remains below 3%. By PSPICE simulation, the power dissipation of the filter was calculated as 1.85mW which is acceptable to design an IC implementation.

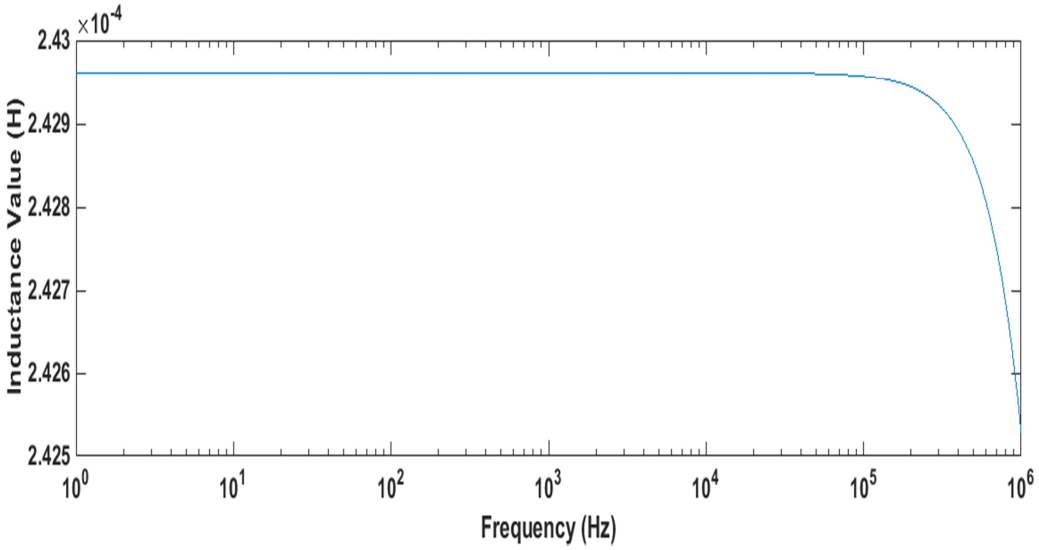


Figure 3.6 Inductor simulation result for 4^{th} order HPF

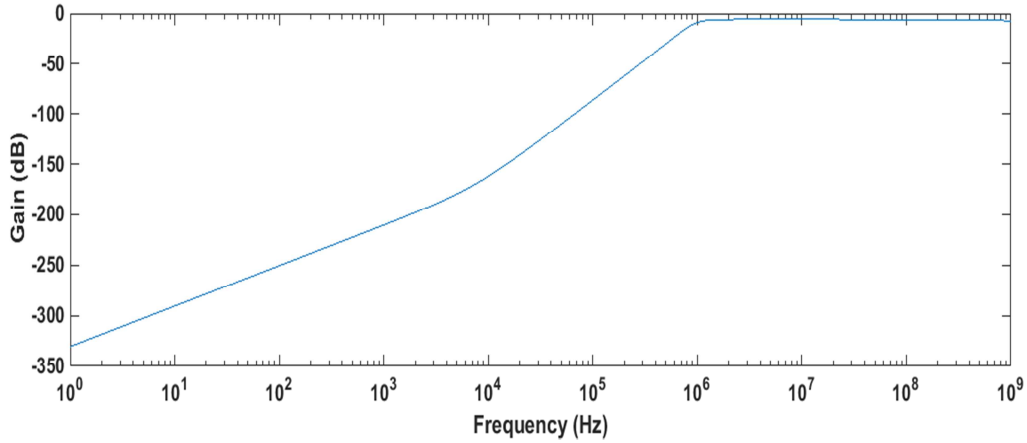


Figure 3.7 Frequency response of 4th order HPF

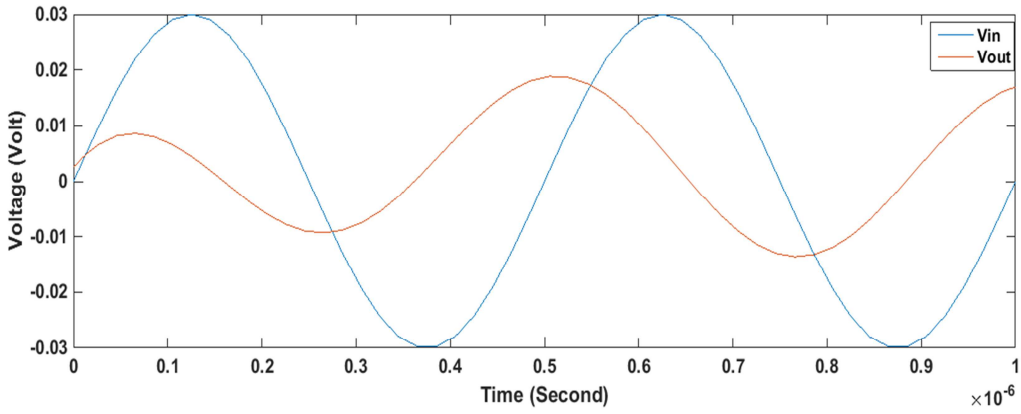


Figure 3.8 Transient analysis of 4th order HPF

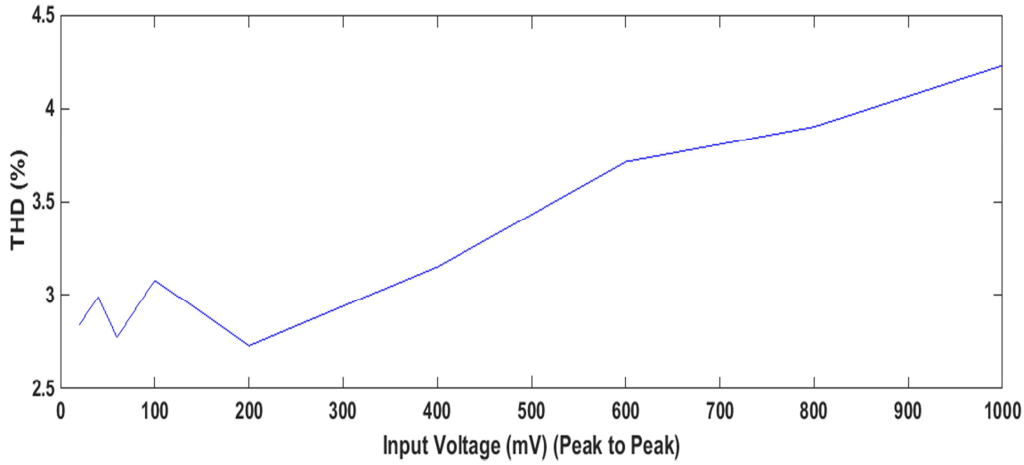


Figure 3.9 Dependence of output voltage THD on input voltage amplitude of 4th order HPF

3.4 VDCC based floating inductor:

The floating inductor (FI) circuit is shown in figure 3.10. The circuit employs one VDCC, one grounded resistor and one grounded capacitor, like grounded inductor circuits, to realize electronically controllable lossless FI circuit [3]. Routine circuit analysis yields

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = (g_m/sCR) \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3.2}$$

The above matrix shows that circuit simulates a lossless floating inductance with the inductance value given by

$$L_{eq} = \frac{RC}{g_m} \tag{3.3}$$

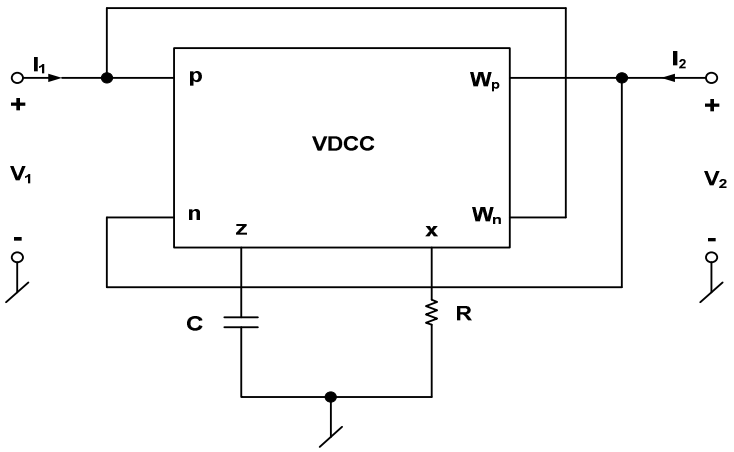


Figure 3.10 Floating inductor circuit [3]

3.4.1 Simulation results:

The circuit shown in figure 3.10 was simulated with the following passive elements value: R = 10KΩ and C = 10pF, taking I_{B1}=50μA and I_{B2}=100μA which results in g_m=273.13μS and L_{eq} = 0.366mH. The simulation result is shown in figure 3.11. It can be seen that simulated value of inductance is constant with frequency upto 10MHz and is approximately equal to theoretical value of inductance.

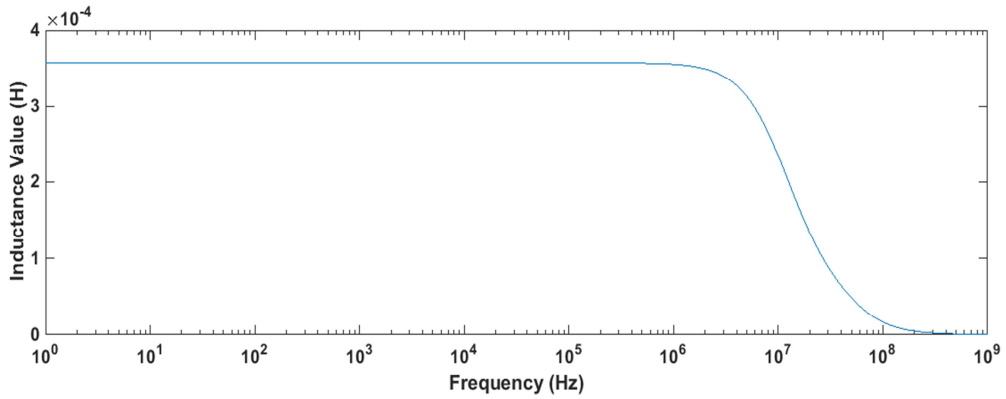


Figure 3.11 Inductor simulation result of figure 3.10

3.5 Second order band pass filter:

The workability of floating inductor (FI) circuit is demonstrated by realizing band pass filter, where floating inductor is used which can be replaced by the simulated floating inductance. The VDCC based simulated floating inductance is shown in figure 3.10 which is used to design a 2nd order BPF as shown in figure 3.12.

The transfer function for 2nd order band pass filter is given by

$$\frac{V_{out}}{V_{in}} = \frac{s(\frac{g_m R_2}{R_1 C_1})}{s^2 + s(\frac{R_2 g_m}{R_1 C_1}) + \frac{g_m}{R_1 C_1 C_2}} \tag{3.4}$$

where pole frequency (ω_0), quality factor (Q) are given by

$$\omega_0 = \sqrt{\frac{g_m}{R_1 C_1 C_2}} \tag{3.5}$$

$$Q = \frac{1}{R_2}\sqrt{\frac{R_1 C_1}{g_m C_2}} \tag{3.6}$$

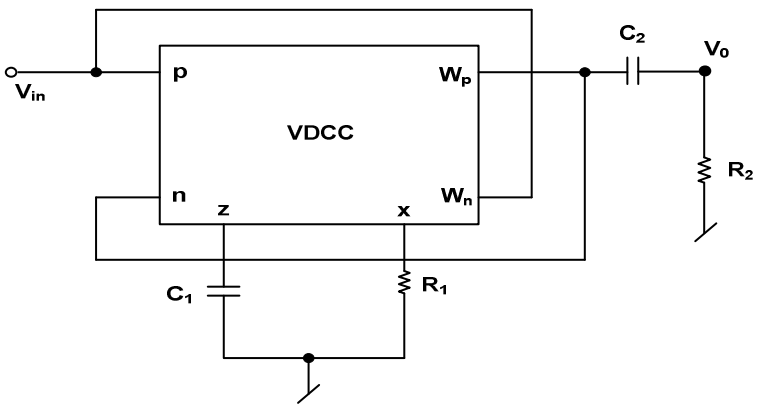


Figure 3.12 2nd order band pass filter realization with VDCC based FI simulator [3].

3.5.1 Simulation results:

To design the circuit for a pole frequency of 1MHz and Q=0.707, the filter was simulated with PSPICE program. The passive elements are selected as R_1 = 70KΩ, R_2 = 22.6KΩ and C_1 = C_2 = 10pF. The bias currents are selected as I_{B1} = 50μA (g_m = 273.13μA/V) and I_{B2} = 100μA. The frequency response is shown in figure 3.13. The simulated pole frequency of BPF was measured as 1.09MHz. By PSPICE simulation, the total power dissipation for this filter was calculated as 0.845 mW which is acceptable to design an IC implementation.

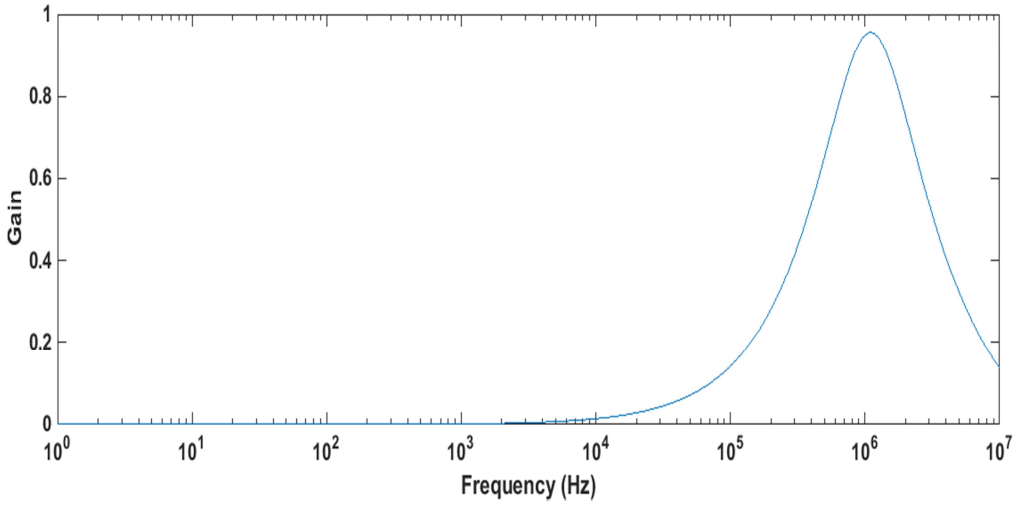


Figure 3.13 Frequency response of 2nd order BPF

3.6 4th order low pass Butterworth ladder filter:

Passive prototype of the fourth order low pass butterworth ladder filter is shown in figure 3.14(a). In this circuit, floating inductor is used which can be replaced by the simulated inductance. The VDCC based simulated floating inductance is shown in figure 3.10 which is used to design a 4th order LPF as shown in figure 3.14(b).

The transfer function for 4th order low pass butterworth filter is given by

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{L_1L_2C_1C_2}}{s^4 + s^3\left(\frac{R_S}{L_1} + \frac{1}{R_LC_4}\right) + s^2\left(\frac{1}{L_1C_3} + \frac{1}{L_2C_3} + \frac{1}{L_2C_4} + \frac{R_S}{R_LC_4L_1}\right) + s^1\left(\frac{1}{L_1C_3R_LC_4} + \frac{R_S}{L_2C_4L_1} + \frac{1}{L_2C_3R_LC_4} + \frac{R_S}{L_2C_3L_1}\right) + \frac{1}{C_1C_2L_1L_2} + \frac{R_S}{L_2C_3R_LC_4L_1}} \quad (3.5)$$

Where $L_1 = \frac{R_1 C_1}{g_{m1}}$ and $L_2 = \frac{R_2 C_2}{g_{m2}}$

g_{m1} and g_{m2} are transconductances of two VDCC blocks respectively.

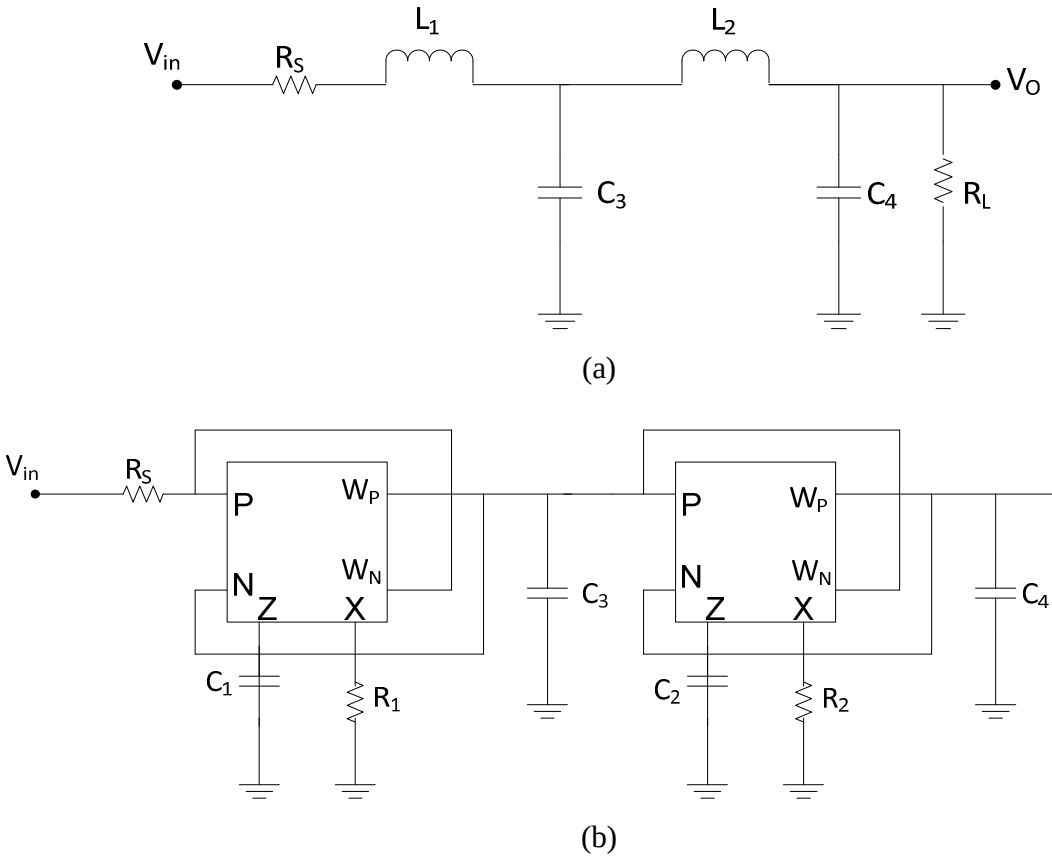


Figure 3.14 4th order LP butterworth filter (a) Passive prototype

(b) VDCC based FI simulator based realization circuit

3.6.1 Simulation results:

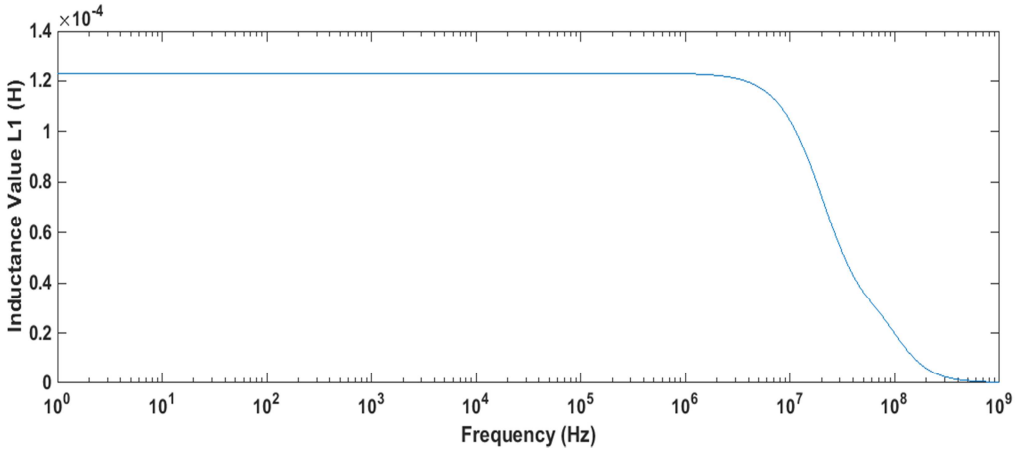
To design the circuit for a pole frequency of 1MHz with Butterworth characteristics, the normalized design (f_0 = 1Hz) was obtained with the following components values -

$R_L = R_S = 1\Omega$, $C_3 = 0.2942F$, $C_4 = 0.12185F$, $L_1 = 0.12185H$ and $L_2 = 0.2942H$

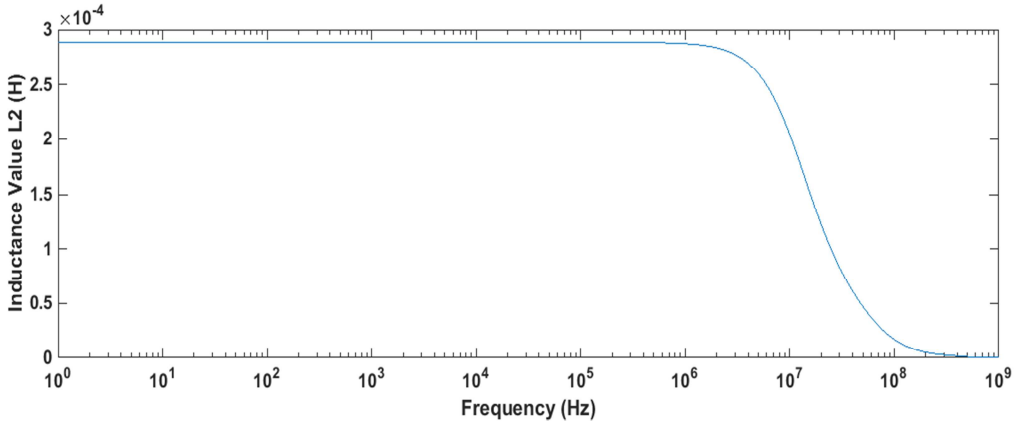
The passive elements are selected as $R_L = R_S = 1K\Omega$, $C_3 = 0.2942nF$, $C_4 = 0.12185nF$, $L_1 = 0.12185mH$ and $L_2 = 0.2942mH$ (by applying magnitude scaling and frequency scaling in normalized design) which results in a pole frequency of 1MHz. The inductance of figure 3.10 was used to design a 4th order low-pass butterworth filter. The performance of simulated floating inductance has been verified by taking $R_1 = 3.32K\Omega$, $C_1 = 0.01nF$, $R_2 = 8K\Omega$, $C_2 = 0.01nF$ and

$g_{m1} = g_{m2} = 273.13\mu A/V$ ($I_{B1} = 50\mu A$, $I_{B2} = 100\mu A$) which results in $L_1 = 0.123mH$ and $L_2 = 0.288mH$. The simulated inductor results are shown in figure 3.15.

The frequency response of 4th order low pass butterworth filter is shown in figure 3.16 which has pole frequency of 1.03MHz which is close to 1MHz. The transient analysis is shown in figure 3.17. For the testing of the input dynamic range of the 4th order LPF, a sinusoidal signal of $f_0 =$ 1MHz with different amplitudes are applied to the input. The total harmonic distortion of the output signal versus amplitude of the input signal is shown in figure 3.18. The result shows that for input signal with amplitude lower than 250mV peak-to-peak, the total harmonic distortion remains below 2%. By PSPICE simulation, the power dissipation of the filter was calculated as 1.70mW which is acceptable to design an IC implementation.



(a)



(b)

Figure 3.15 Inductor simulation result for 4th order LPF

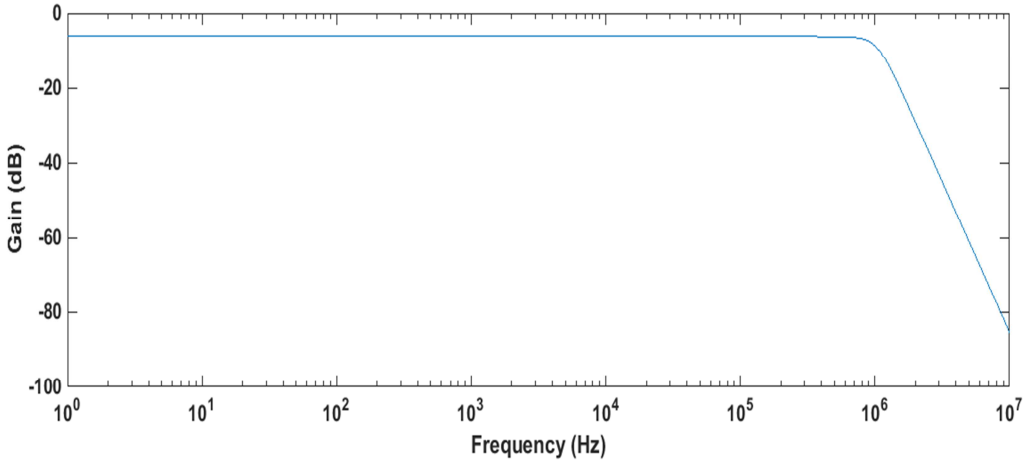


Figure 3.16 Frequency response of 4th order LPF

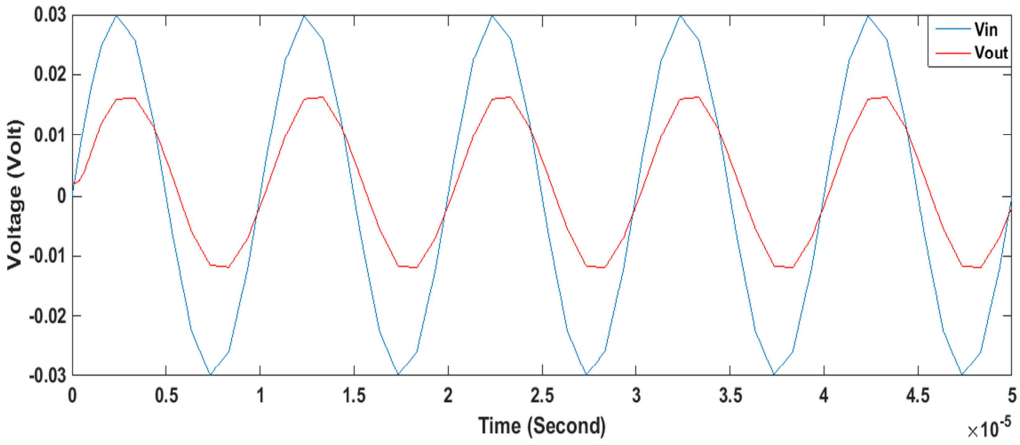


Figure 3.17 Transient analysis of 4th order LPF

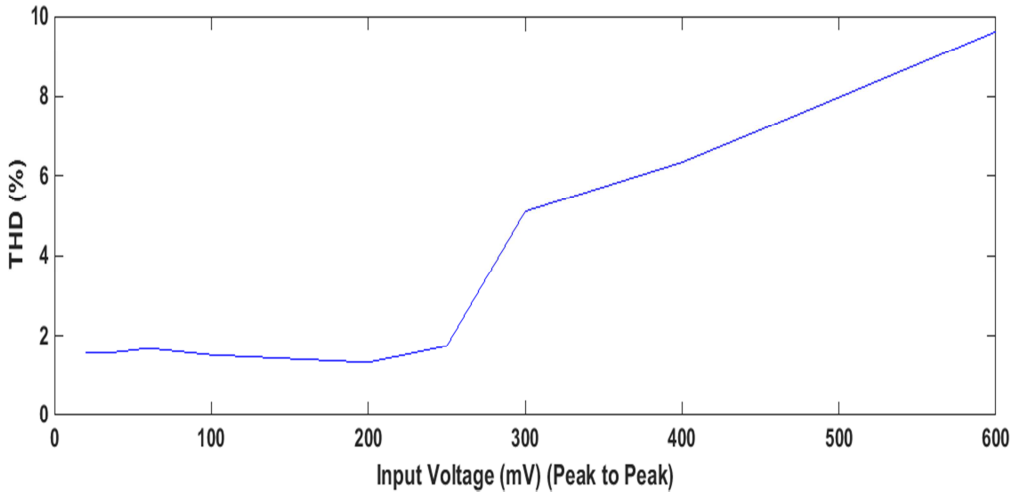


Figure 3.18 Dependence of output voltage THD on input voltage amplitude of 4th order LPF

3.7 Conclusion:

This chapter covers the realization of grounded and floating inductors using single voltage differencing current conveyor and only two passive elements, and its application in realization of higher order butterworth filter. These circuits were simulated which verified the usability of VDCC in the analog signal processing among the novel active building blocks. The grounded and floating inductance simulators yield the following advantages [2]:

(i) They use minimum number of active and passive elements (a single active element, one grounded capacitor and one grounded resistor),
(ii) They have electronically tunability by means of the biasing current I_{B1} and
(iii) They don't require passive component matching.

This chapter introduces VDCC based GI and FI simulators. The workability of these circuits has been confirmed by higher order filter design applications using PSPICE. Table 3.2 shows the comparison between theoretical values and simulated values.

Table 3.2 Comparison between theoretical values and simulated values

Sr. No.	Filter	Theoretically design value of pole frequency	Practical value of pole frequency
1.	4^{th} order high pass butterworth filter	1MHz	995KHz
2.	2^{nd} order band pass filter	1MHz	1.09MHz
3.	4^{th} order low pass butterworth filter	1MHz	1.03MHz

3.8 References:

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Chapter 4

Single VDCC based second order filter realization

4.1 Introduction:

Filter is an electronic circuit that performs a frequency selection function: passing signals whose frequency spectrum lies within a specified range, and stopping signals whose frequency spectrum falls outside this range.

In the present chapter we have dealt with the realization of single VDCC based biquad. Biquad filters are an important class of active filters which can be used for realization of higher order filters.

Biquad filters can be classified in the following categories namely (i) fixed structure type (ii) variable structure type. Another classification may be in terms of number of inputs and outputs viz single / multiple input single / multiple output.

In the following we present a general structure of a single input single output biquad filter in which by appropriately choosing different admittances, different 2nd order filters can be realized.

4.2 General structure of single VDCC biquad:

Let us consider the single VDCC biquad, which is shown in figure 4.1, where the VDCC is connected to five passive elements. By analysis of figure 4.1, we obtain the following transfer function (assuming an ideal VDCC) –

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m Y_1 Y_3}{Y_5}}{Y_1Y_3+Y_1Y_4+Y_2Y_3+Y_2Y_4-\frac{g_m Y_3 Y_4}{Y_5}} \tag{4.1}$$

It can be seen that equation (4.1), expressed in terms of admittances, is able to perform several 2nd order voltage filtering operation, including low pass, high pass and band pass functions.

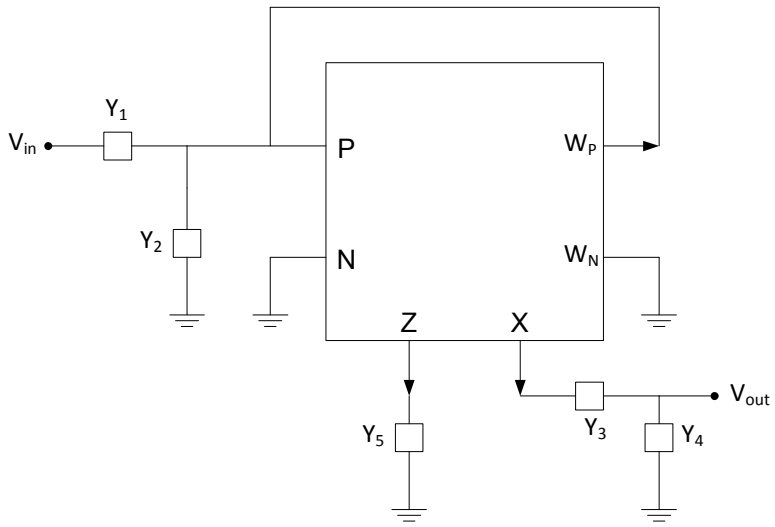

Figure 4.1 Circuit for the synthesis of single VDCC biquads

4.2.1 Low pass filter:

If the value of admittances shown in figure 4.1 is taken as follows –

$Y_1 = 1/R_1$, $Y_2 = sC_1$, $Y_3 = 1/R_2$, $Y_4 = sC_2$, $Y_5 = 1/R_3$ (as shown in figure 4.2), then the transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m R_3}{R_1 R_2 C_1 C_2}}{s^2 + s\left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} - \frac{g_m R_3}{R_2 C_1}\right) + \frac{1}{R_1 R_2 C_1 C_2}} \tag{4.2}$$

which is the transfer function of LPF.

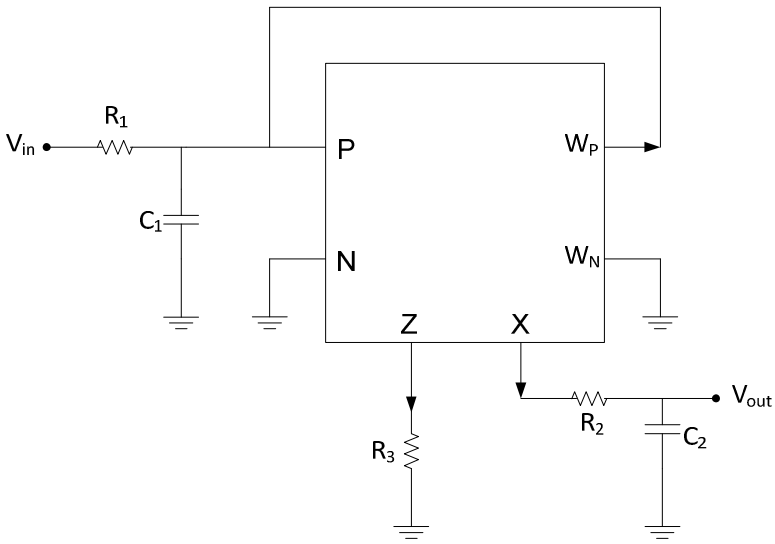

Figure 4.2 Circuit for LPF

The pole frequency (ω_0), quality factor (Q) and DC gain (K) of the circuit are given as

$$\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \tag{4.3}$$

$$Q = \frac{\sqrt{\frac{C_1 C_2}{R_1 R_2}}}{\frac{C_1}{R_2}+\frac{C_2}{R_1}-\frac{g_m R_3 C_2}{R_2}} \tag{4.4}$$

$$K = g_m R_3 \tag{4.5}$$

4.2.2 High pass filter:

If the value of admittances shown in figure 4.1 is taken as follows –

$Y_1 = sC_1$, $Y_2 = 1/R_1$, $Y_3 = sC_2$, $Y_4 = 1/R_2$, $Y_5 = 1/R_3$ (as shown in figure 4.3), then the transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{g_m R_3 s^2}{s^2+s\left(\frac{1}{R_1 C_1}+\frac{1}{R_2 C_2}-\frac{g_m R_3}{R_2 C_1}\right)+\frac{1}{R_1 R_2 C_1 C_2}} \tag{4.6}$$

which is the transfer function of HPF.

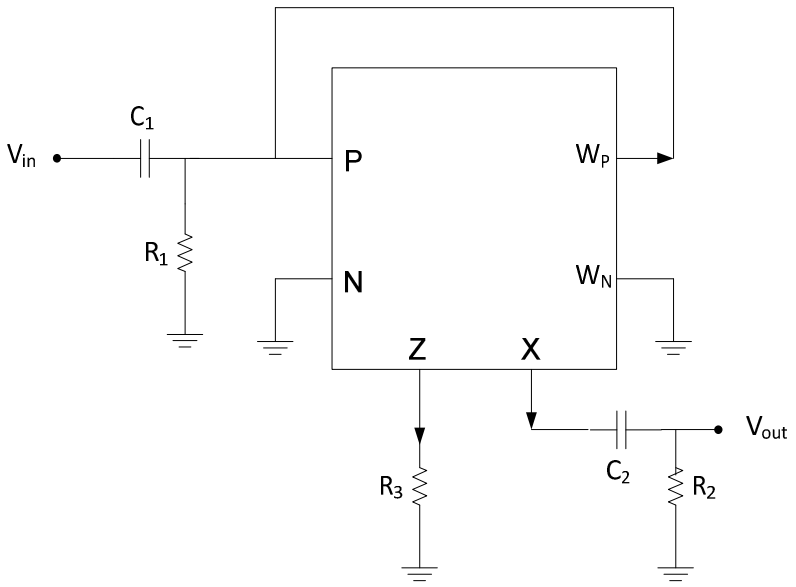

Figure 4.3 Circuit for HPF

The pole frequency (ω_0), quality factor (Q) and high frequency gain (K) of the circuit are given as

$$\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \tag{4.7}$$

$$Q = \frac{\sqrt{\frac{C_1 C_2}{R_1 R_2}}}{\frac{C_1}{R_2} + \frac{C_2}{R_1} - \frac{g_m R_3 C_2}{R_2}} \tag{4.8}$$

$$K = g_m R_3 \tag{4.9}$$

4.2.3 Band pass filter:

If the value of admittances shown in figure 4.1 is taken as follows –

$Y_1 = sC_1$, $Y_2 = R_1$, $Y_3 = 1/R_2$, $Y_4 = sC_2$, $Y_5 = 1/R_3$ (as shown in figure 4.4), then the transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m R_3 s}{R_2 C_2}}{s^2 + s\left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} - \frac{g_m R_3}{R_2 C_1}\right) + \frac{1}{R_1 R_2 C_1 C_2}} \tag{4.10}$$

which is the transfer function of BPF.

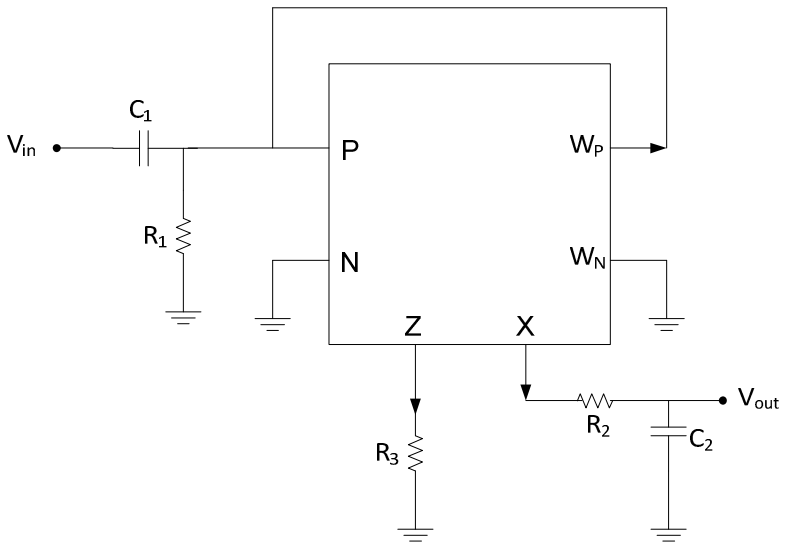

Figure 4.4 First circuit for BPF

Similarly, if we take the value of admittances shown in figure 4.1 is taken as follows –

$Y_1 = 1/R_1$, $Y_2 = sC_1$, $Y_3 = sC_2$, $Y_4 = 1/R_2$, $Y_5 = 1/R_3$ (as shown in figure 4.5), then the transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m R_3 s}{R_1 C_1}}{s^2 + s\left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} - \frac{g_m R_3}{R_2 C_1}\right) + \frac{1}{R_1 R_2 C_1 C_2}} \tag{4.11}$$

which is also the transfer function of BPF.

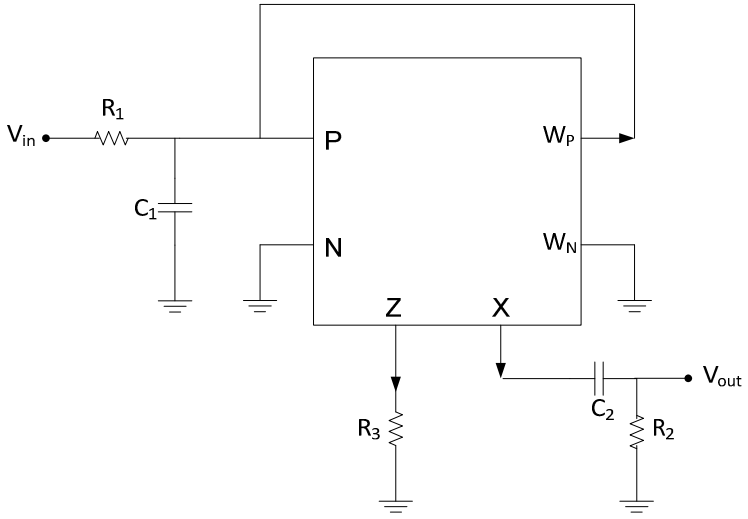

Figure 4.5 Second circuit for BPF

The pole frequency (ω_0), quality factor (Q) and center frequency gain (-KQ) of the circuit are given as follows

$$\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \tag{4.12}$$

$$Q = \frac{\sqrt{\frac{C_1 C_2}{R_1 R_2}}}{\frac{C_1}{R_2} + \frac{C_2}{R_1} - \frac{g_m R_3 C_2}{R_2}} \tag{4.13}$$

$$\text{Center frequency gain (-KQ)} = \frac{\frac{g_m R_3 C_1}{R_2}}{\frac{C_1}{R_2} + \frac{C_2}{R_1} - \frac{g_m R_3 C_2}{R_2}} \tag{4.14}$$

4.3 Simulation results:

To prove the theoretical validity of single VDCC biquad filter of figure 4.2, 4.3 and 4.4 for pole frequency (f_0) = 5MHz and Q=0.707, the filters were simulated with PSPICE program. The passive elements are selected as R_1 = 2.25KΩ, R_2 = 4.5KΩ, R_3 = 3.67KΩ and C_1 = C_2 = 10pF. The bias currents are selected as I_{B1} = 50μA (g_m = 273.13μA/V) and I_{B2} = 100μA. The LPF, HPF

and BPF frequency responses and time responses are shown in figure 4.6 to figure 4.11 respectively. The simulated pole frequency of LPF, HPF and BPF were measured as 5MHz, 4.56MHz and 4.79MHz respectively. The sensitivity of ω_0 is given as follows

$$S^{\omega_0}_{C_1,C_2,R_1,R_2} = -\frac{1}{2} \tag{4.15}$$

For the testing of input dynamic range of the 2nd order filters, a sinusoidal signal of f_0 = 5MHz with different amplitudes are applied to the input. The total harmonic distortion of the output signal versus amplitude of the input signal is shown in figure 4.12. The result shows that for input signal with amplitude lower than 300mV peak-to-peak, the total harmonic distortion remains below 2%. By PSPICE simulation, the total power dissipation of the single VDCC biquad was calculated as 0.845 mW which is acceptable to design an IC implementation. Table 4.1 shows the comparison between theoretical values and simulated values.

Table 4.1 Comparison between theoretical values and simulated values

Sr. No.	Filter	Theoretically design value of pole frequency	Practical value of pole frequency
1.	Low pass filter	5MHz	5MHz
2.	High pass filter	5MHz	4.56MHz
3.	Band pass filter	5MHz	4.79MHz

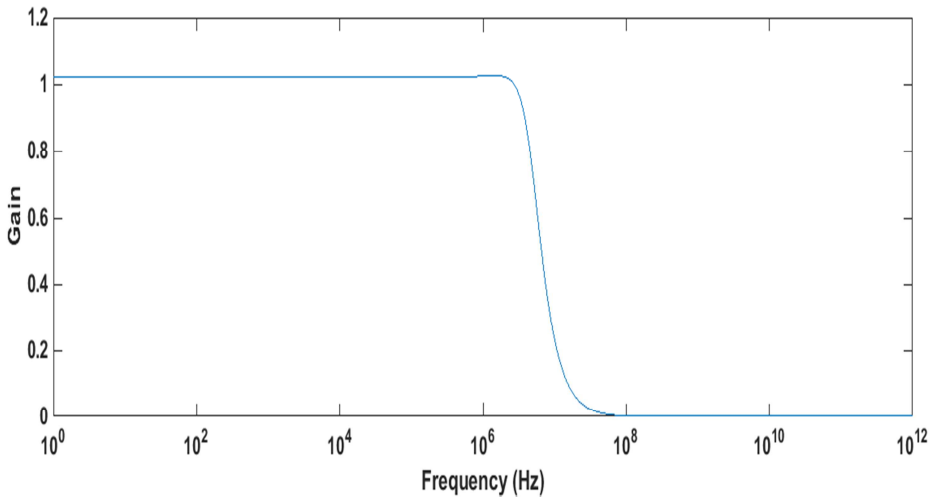

Figure 4.6 Frequency response of low pass filter shown in figure 4.2

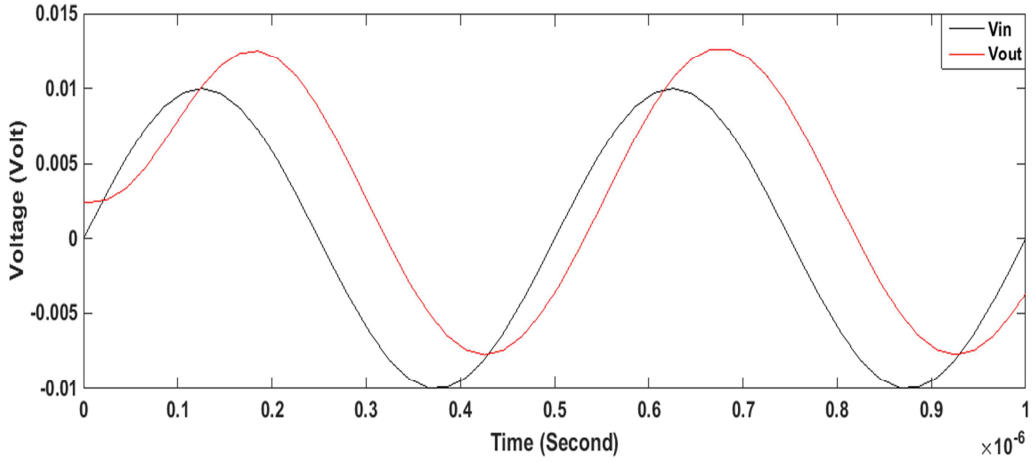

Figure 4.7 Time response of low pass filter shown in figure 4.2

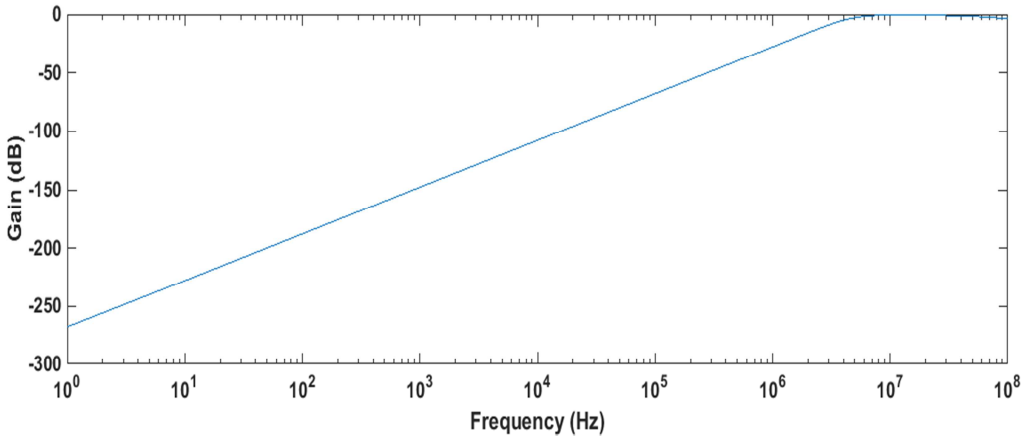

Figure 4.8 Frequency response of high pass filter shown in figure 4.3

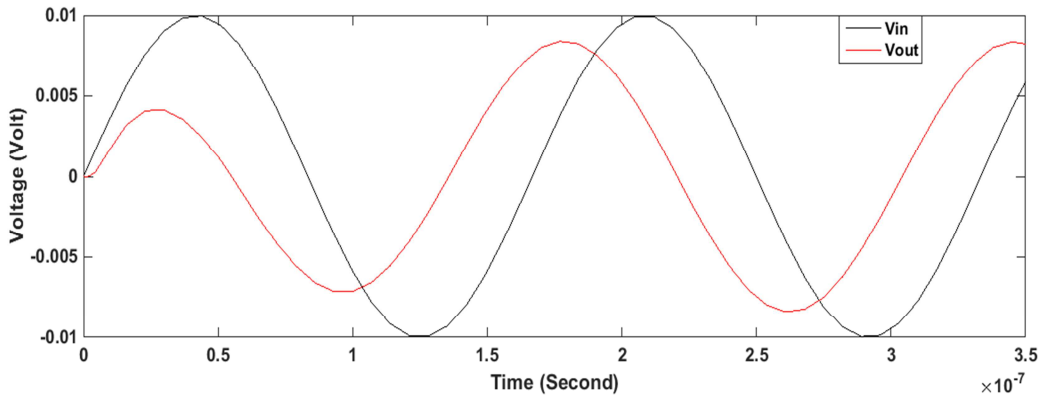

Figure 4.9 Time response of high pass filter shown in figure 4.3

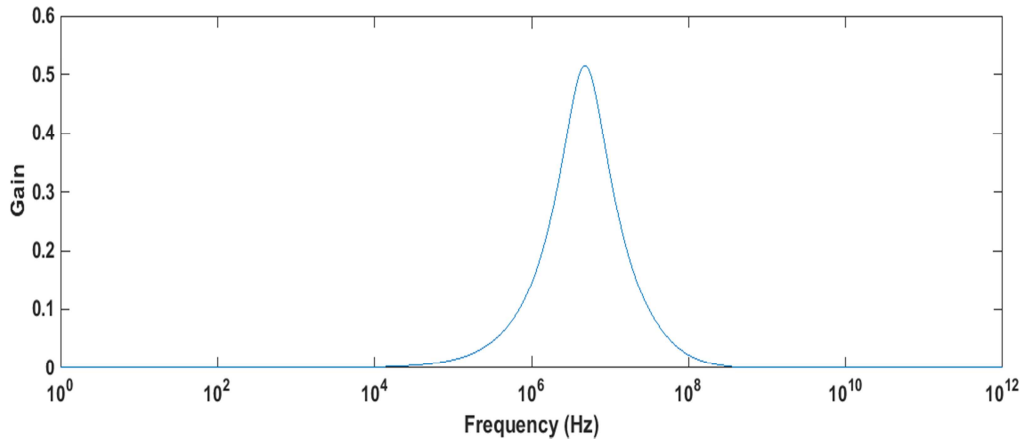

Figure 4.10 Frequency response of band pass filter shown in figure 4.4

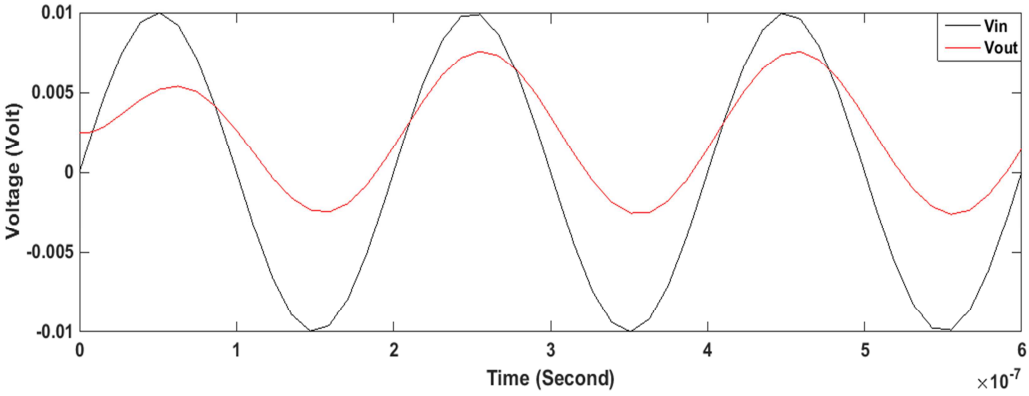

Figure 4.11 Time response of band pass filter shown in figure 4.4

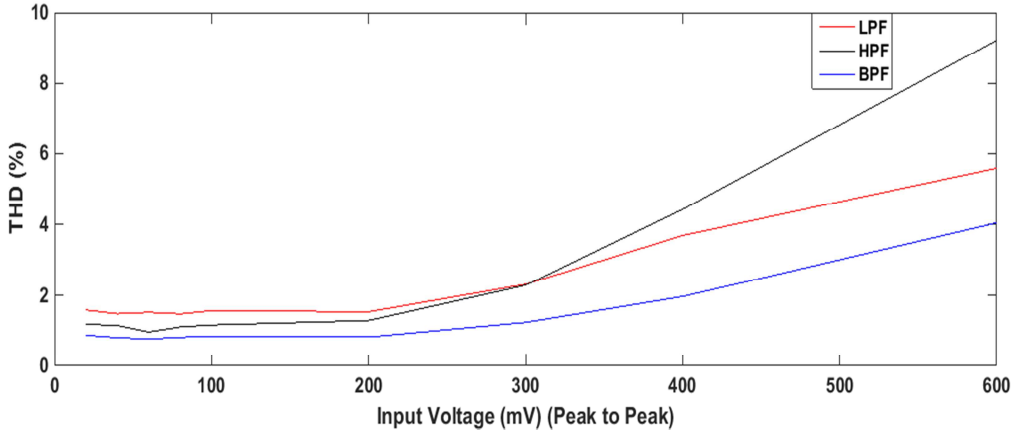

Figure 4.12 Dependence of output voltage THD on input voltage amplitude of low pass, high pass and band pass filter

4.4 Conclusion:

This chapter covers the realization of single VDCC based second order filters such as low pass filter, high pass filter and band pass filter. The single VDCC based voltage mode second order filters have been proposed and simulated which verified the usability of VDCC in the analog signal processing among the novel active building blocks. The time responses and frequency responses for these filters have been shown which was simulated using PSPICE.

4.5 References:

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Chapter 5
Tow-Thomas and KHN biquad filters using VDCC

5.1 Introduction:

In the previous chapters, applications (amplifiers and filters) of VDCC in voltage mode signal processing have been discussed. The VDCC is a versatile active building block similar to other derivatives of current conveyors. A VDCC combines the features of an operational transconductance amplifier and a current conveyor. In this chapter, we discuss in detail about novel application of VDCC in the realization of voltage mode and current mode multifunction filters with the following features.

(i) tunability of bandwidth and

(ii) tunability of central frequency

But before we discuss, it is necessary to have a review of universal / multifunction biquad filters.

Realizations of filters, particularly biquad filters have been a very prominent application of any active building block. Out of different filter configurations implemented from these active building blocks, multifunction / universal filter realizations are preferred because they provide more than one filter functions from the same structure. Apart from their usual application as standard second-order building blocks, multifunction active biquad filters find applications in touch tone telephone systems, crossover networks used in three-way high fidelity loud speakers, phase locked loop and FM stereo demodulators [1].

Multifunctional filter can be made on the basis of the number of inputs and number of outputs present in a particular realization. In single-input single-output (SISO) multifunctional filters, there is only one input and one output response available at a time. In single-input multiple-outputs (SIMO) type multifunctional filters, one input is required and different output responses are simultaneously available at different-different points of the circuit. In multiple-input single-output (MISO) type filters, multiple inputs are required and a single output response is available at a time. Lastly, in multiple-inputs multiple-output (MIMO) class, more than one input is

applied and a particular output response can be obtained by judicious choice of inputs or combinations thereof.

In another classification, multifunctional filters can be of fixed topology type in which the number and nature of the active and passive elements remain fixed and usually at least three out of the five generic filtering functions namely “low pass, high pass, band pass, notch and all pass” are simultaneously available in voltage-mode / current-mode or both. Multifunctional filters can also be of variable topology type in which the nature and number of elements vary for different output responses. A multifunction biquad is said to be ‘universal’ if it is capable of realizing all the five standard filter functions.

In this chapter we have proposed multifunction biquad filters based on the use of two integrators connected in cascade in an overall feedback loop (and are thus known as two integrator loop circuits), proposed by Tow-Thomas and Kerwin-Huelsman-Newcomb. The name biquad stems from the fact that these circuits in its most general form is capable of realizing a biquadratic transfer function, that is, one that is the ratio of two quadratic polynomials.

5.1.1 Kerwin-Huelsman-Newcomb (KHN) biquad filter [2-4]:

The KHN biquad filter is used for multifunction filtering structures. This structure is based on the use of two integrators connected in cascade in an overall feedback loop. The most important feature of this structure is to provide second order high-pass (HP), band-pass (BP) and low-pass (LP) responses simultaneously. KHN-biquad filter is generally used because it provides some advantages like low active and passive sensitivities, low component spread and sufficient stable response [2-4]. There are different active blocks, which are used to design KHN biquad filter. Some of them are operate in voltage mode and others in current mode. The block diagram of KHN-biquad filter in voltage mode is shown in figure 5.1.

Consider a 2nd high-pass filter with transfer function

$$T_{hp}(s) = \frac{V_{hp}}{V_i} = \frac{Ks^2}{s^2+s\frac{\omega_0}{Q}+\omega_0^2} \tag{5.1}$$

where K is the gain at high frequency. By rearranging equation (5.1), it becomes

$$V_{hp} + \frac{1}{Q}\left(\frac{\omega_0}{s}V_{hp}\right) + \left(\frac{\omega_0^2}{s^2}V_{hp}\right) = KV_i \tag{5.2}$$

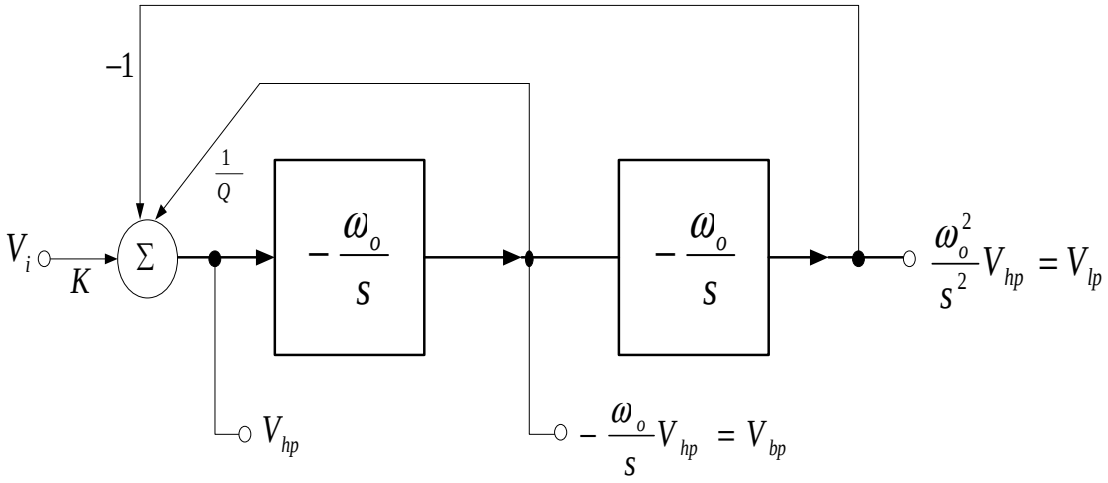


Figure 5.1 Block diagram of KHN biquad filter using two integrators in feedback loop [2-4]

The signal V_{hp} can be derived from eq. (5.2) as follows

$$V_{hp} = KV_i - \frac{1}{Q}\left(\frac{\omega_0}{s}V_{hp}\right) - \left(\frac{\omega_0^2}{s^2}V_{hp}\right) \tag{5.3}$$

The output of first integrator is band pass signal whose transfer function is given as follows

$$T_{bp}(s) = \frac{V_{bp}}{V_i} = \frac{-K\omega_0 s}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{5.4}$$

where the center frequency gain of the band pass filter is equal to –KQ. Similarly, the output of second integrator is low pass signal whose transfer function is given as follows

$$T_{lp}(s) = \frac{V_{lp}}{V_i} = \frac{K\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{5.5}$$

where the DC gain of low pass filter is equal to K.

The two integrator-loop biquad filter realizes three basic second order filter functions high pass, band pass and low pass simultaneously. This circuit is very much popular and it is commonly known as universal active filter (KHN biquad).

5.1.2 Tow–Thomas (TT) biquad filter [5]:

The block diagram of TT biquad filter is shown in figure 5.2. In TT based filters, two outputs can be taken simultaneously such as low-pass (LP) and band pass (BP) responses. Two negative integrator loops are used in which one is ideal integrator and other one is lossy integrator [5]. TT biquad filter has been implemented using Op-amp, OTRA, CCII and DVCC [5]. The block diagram of TT biquad filter in voltage mode is shown in figure 5.2.

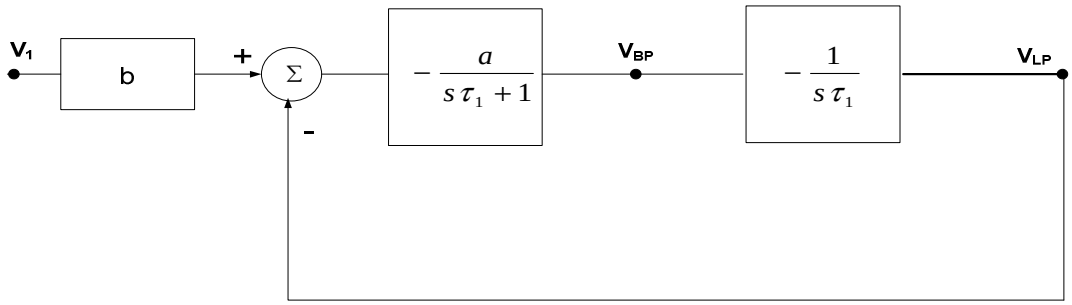


Figure 5.2 Block diagram representation of the Tow-Thomas (TT) biquad filter [5]

5.2 The proposed VDCC based voltage mode Tow-Thomas (TT) biquad filter:

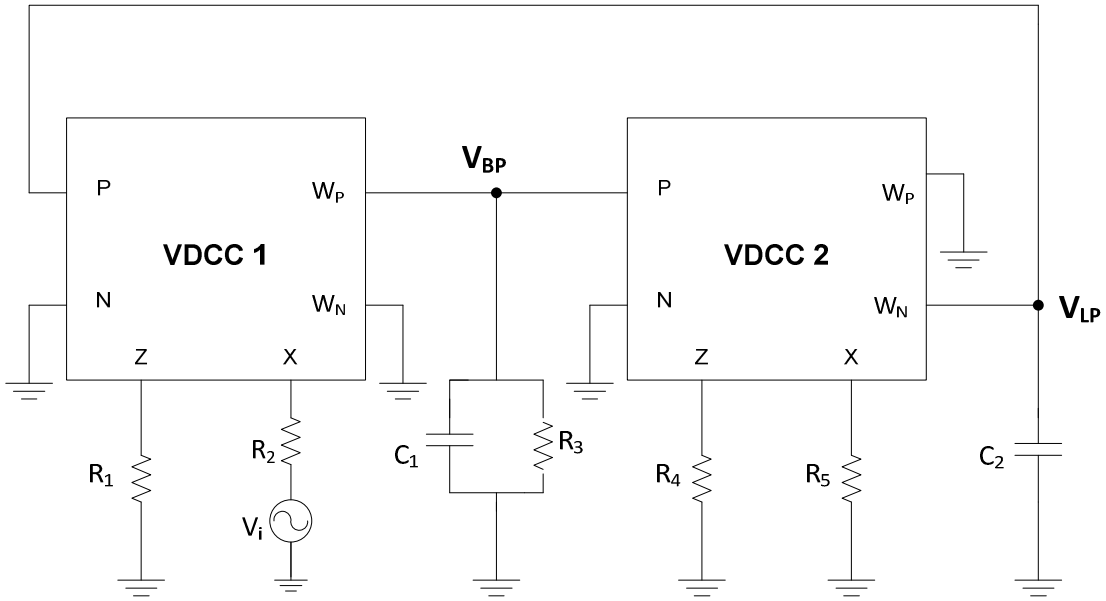


Figure 5.3 Proposed voltage mode multifunctional Tow-Thomas biquad filter using VDCC

The block diagram of voltage mode (VM) multifunction Tow-Thomas (TT) biquad filter is shown in figure 5.2. The proposed VDCC based voltage mode multifunction TT biquad filter is shown in figure 5.3. In this, the important thing is that the passive elements are used as grounded element (except one resistor). So it is easy to fabricate in the form of IC.

From the circuit analysis of the circuit shown in figure 5.3, the transfer function of band pass response is given as follows

$$T_{BP}(s) = \frac{V_{BP}}{V_i} = \frac{-\frac{s}{C_1R_2}}{s^2+\frac{s}{R_3C_1}+\frac{g_{m1}g_{m2}R_1R_4}{C_1C_2R_2R_5}} \tag{5.6}$$

It is clear that this transfer function is resulting in inverting band pass response. Similarly, the transfer function of low pass response is given as follows

$$T_{LP}(s) = \frac{V_{LP}}{V_i} = \frac{\frac{g_{m2}R_4}{C_1C_2R_2R_5}}{s^2+\frac{s}{R_3C_1}+\frac{g_{m1}g_{m2}R_1R_4}{C_1C_2R_2R_5}} \tag{5.7}$$

It is clear that this transfer function is resulting in non-inverting low pass response. By interchanging the above two VDCC blocks resulting in non-inverting band pass response and non-inverting low pass response.

The important parameters of this filter are pole frequency (ω_0), bandwidth (BW) and quality factor (Q) which can be expressed as follows (by comparing equations (5.6) and (5.7) with equations (5.4) and (5.5) respectively)

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}R_1R_4}{C_1C_2R_2R_5}} \tag{5.8}$$

$$\text{BW} = \frac{1}{R_3C_1} \tag{5.9}$$

$$Q = R_3C_1\omega_0 = R_3C_1\sqrt{\frac{g_{m1}g_{m2}R_1R_4}{C_1C_2R_2R_5}} \tag{5.10}$$

For low pass response, the DC gain (K) is given by

$$K = \frac{1}{g_{m1}R_1} \tag{5.11}$$

For band pass response, the center frequency gain (-KQ) is given by

$$-KQ = -\frac{R_3}{R_2} \tag{5.12}$$

where g_{m1} is transconductance of block VDCC 1 and g_{m2} is transconductance of block VDCC 2. The sensitivities of ω_0 and Q of proposed filter are given as follows

$$S^{\omega_0}_{C_1,C_2,R_2,R_5} = -\frac{1}{2} \tag{5.13}$$

$$S^{\omega_0}_{g_{m_1},g_{m_2},R_1,R_4} = +\frac{1}{2} \tag{5.14}$$

$$S^{\omega_0}_{R_3} = 0 \tag{5.15}$$

$$S^{Q}_{g_{m_2},g_{m_1},C_1,R_1,R_4} = +\frac{1}{2} \tag{5.16}$$

$$S^{Q}_{R_2,R_5,C_2} = -\frac{1}{2} \tag{5.17}$$

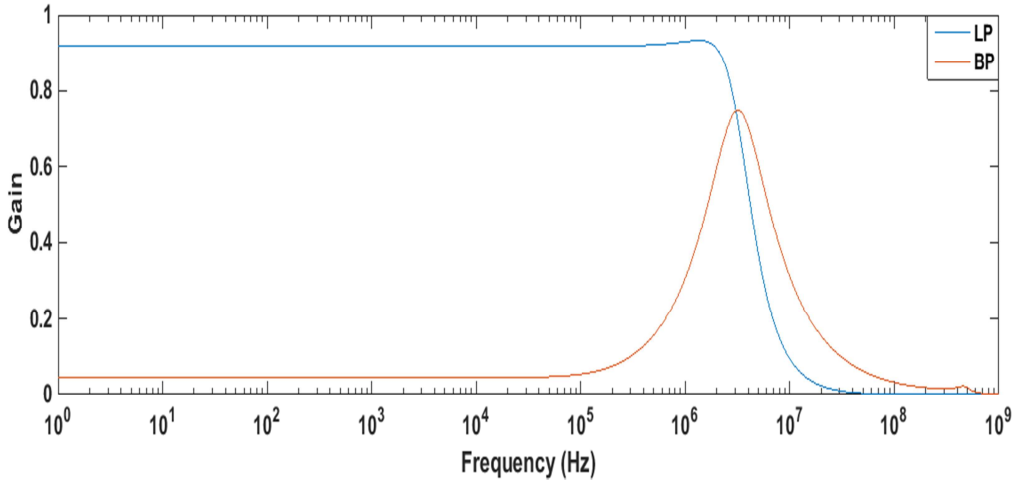
$$S^{Q}_{R_3} = +1 \tag{5.18}$$

It can be remarked that bandwidth (BW) can be adjusted by varying the resistor R_3 without affecting the pole frequency (ω_0). Pole frequency can be controlled by varying R_1, R_2, R_4, R5 and transconductances. Here important feature is that pole frequency and bandwidth can be tuned independently.

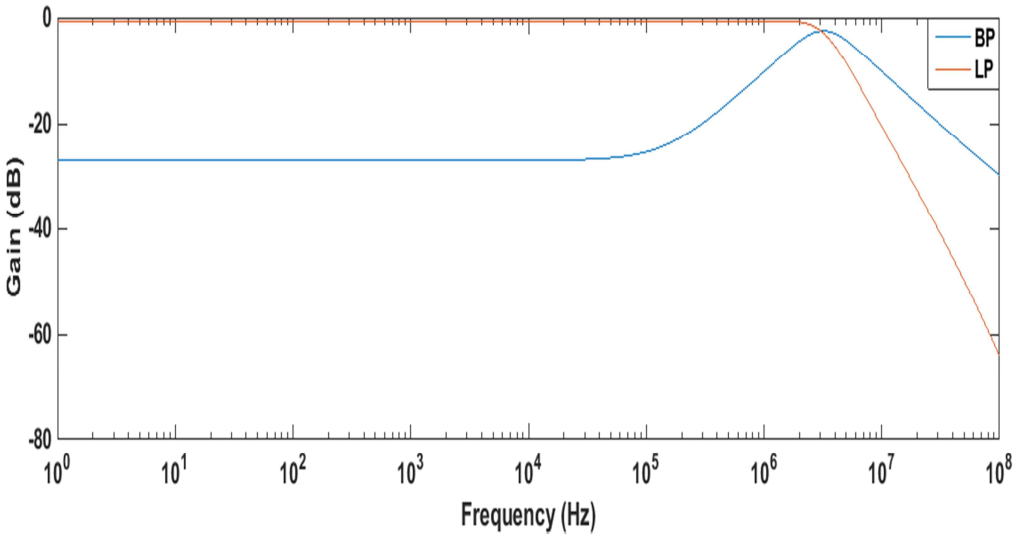
5.2.1 Simulation results:

To prove the theoretical validity of the proposed Tow Thomas (TT) biquad filter of figure 5.3 for pole frequency (f_0) = 3MHz and Q=0.707, the filter has been simulated with PSPICE program. The passive elements are selected as $R_1 = R_4 = 3.5K\Omega$, $R_2 = R_5 = 12.7K\Omega$, $R_3 = 9.4K\Omega$ and $C_1 = C_2 = 4pF$. The bias current are selected as $I_{B1} = 50\mu A$ ($g_m = 273.13\mu A/V$) and $I_{B2} = 100\mu A$. The low pass and band pass frequency responses and time responses are shown in figure 5.4 and figure 5.5 respectively. The simulated pole frequency of band pass response and low pass response were measured as 3.16MHz and 3.43MHz respectively. In the case of band-pass response, center frequency and bandwidth (BW) can be varied independently which are shown in figure 5.6 and figure 5.7 respectively.

For the testing of the input dynamic range of the 2nd order Tow-Thomas (TT) filter, a sinusoidal signal of f_0 = 3 MHz with different amplitudes are applied to the input. The total harmonic distortion of the output signal versus amplitude of the input signal is shown in figure 5.8. The result shows that for input signal with amplitude lower than 400mV peak-to-peak, the THD remains below 2%. By PSPICE simulation, the total power dissipation of the filter was calculated as 1.69 mW which is acceptable to design an IC implementation.



(a)



(b)

Figure 5.4 Frequency Response of proposed multifunctional VM TT biquad filter

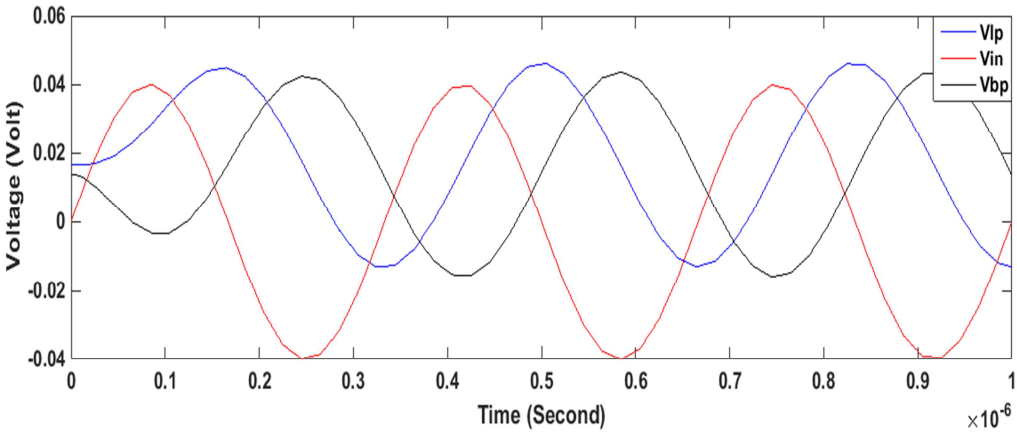


Figure 5.5 Time response of proposed multifunctional VM TT biquad filter

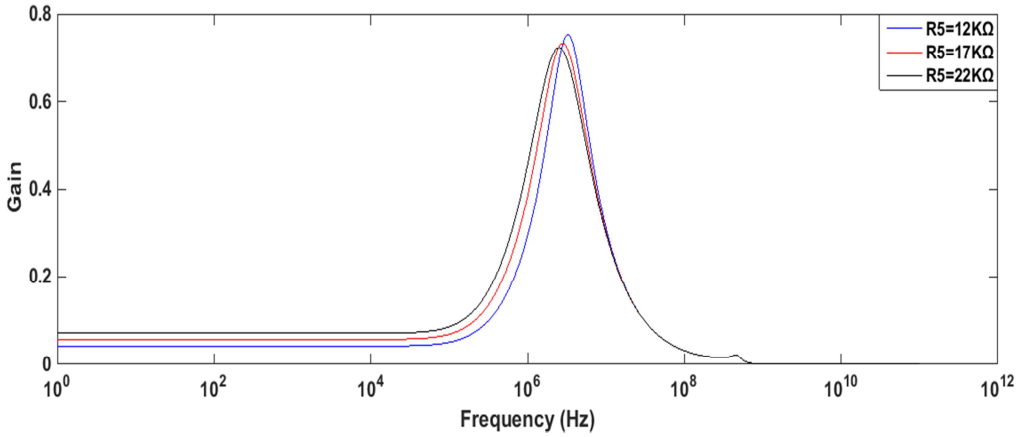


Figure 5.6 Frequency response of TT filter when pole frequency is varied and BW is constant

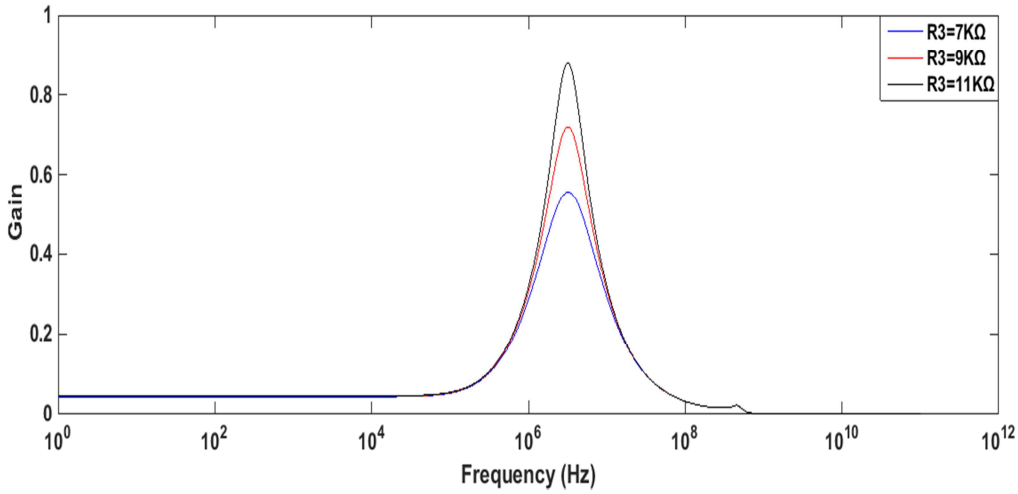


Figure 5.7 Frequency response of VM TT filter when bandwidth (BW) is varied and pole frequency is constant

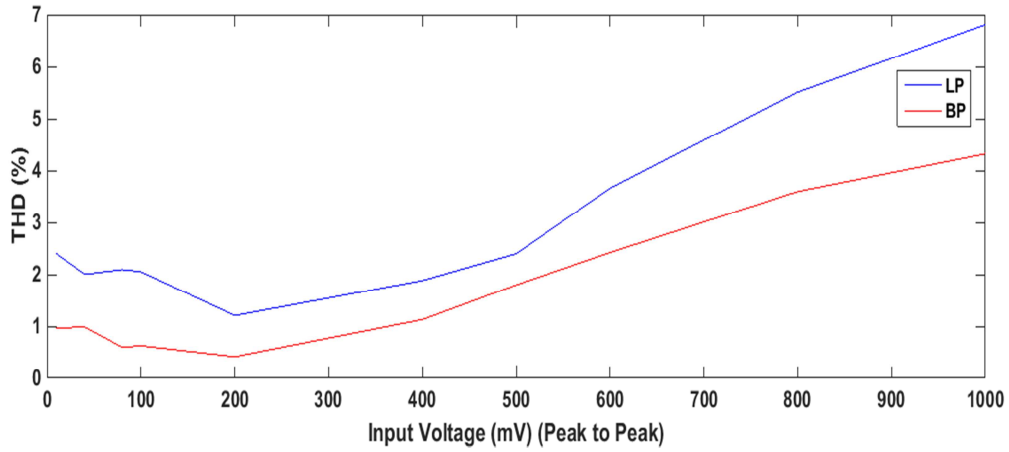


Figure 5.8 Dependence of output voltage THD on input voltage amplitude of VM TTF

5.2.2 Independent tuning of gain, bandwidth and pole frequency:

For the independent tuning of gain, bandwidth and pole frequency, let us assume that

$$R_2 = R_4 = R' \tag{5.19}$$

and

$$R_1 = R_5 = R'' \tag{5.20}$$

Then

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{5.21}$$

$$\text{BW} = \frac{1}{R_3C_1} \tag{5.22}$$

$$Q = R_3C_1\omega_0 = R_3C_1\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{5.23}$$

For low pass response, the DC gain (K) is given by

$$K = \frac{1}{g_{m1}R''} \tag{5.24}$$

For band pass response, the center frequency gain (-KQ) is given by

$$-KQ = -\frac{R_3}{R'} \tag{5.25}$$

The sensitivities of ω_0 and Q are given as follows

$$S_{C_1,C_2}^{\omega_0} = -\frac{1}{2} \tag{5.26}$$

$$S_{g_{m_1},g_{m_2}}^{\omega_0} = +\frac{1}{2} \tag{5.27}$$

$$S_{R_3,R',R''}^{\omega_0} = 0 \tag{5.28}$$

$$S_{g_{m_2},g_{m_1},C_1}^{Q} = +\frac{1}{2} \tag{5.29}$$

$$S_{C_2}^{Q} = -\frac{1}{2} \tag{5.30}$$

$$S_{R_3}^{Q} = +1 \tag{5.31}$$

$$S_{R',R''}^{Q} = 0 \tag{5.32}$$

It is clear for low pass filter from equation (5.21),(5.22) and (5.24) that the pole frequency and DC gain (K) can be varied independently without affecting each other.

Similarly, it is clear for band pass filter from equation (5.21), (5.22) and (5.25) that pole frequency and center frequency gain (-KQ) can be varied independently. For R' = R_3, the bandwidth can be varied without affecting pole frequency and center frequency gain (=1).

To prove the theoretical validity of these assumptions for pole frequency (f_0) = 3MHz and Q=0.707, the filter has been simulated with PSPICE program. The passive elements are selected as R_3 = 2.59KΩ, R' = R_2 = R_4 = 3.66 KΩ, R'' = R_1 = R_5 = 3.66KΩ and C_1 = C_2 = 14.5pF. The bias current are selected as I_{B1} = 50μA (g_m = 273.13μA/V) and I_{B2} = 100μA. The low pass and band pass frequency responses and time responses are shown in figure 5.9 and figure 5.10 respectively. The simulated pole frequency of band pass response and low pass response were measured as 3.02MHz and 3.3MHz respectively. Figure 5.11 to figure 5.14 shows the variation in one parameter without affecting the other parameters.

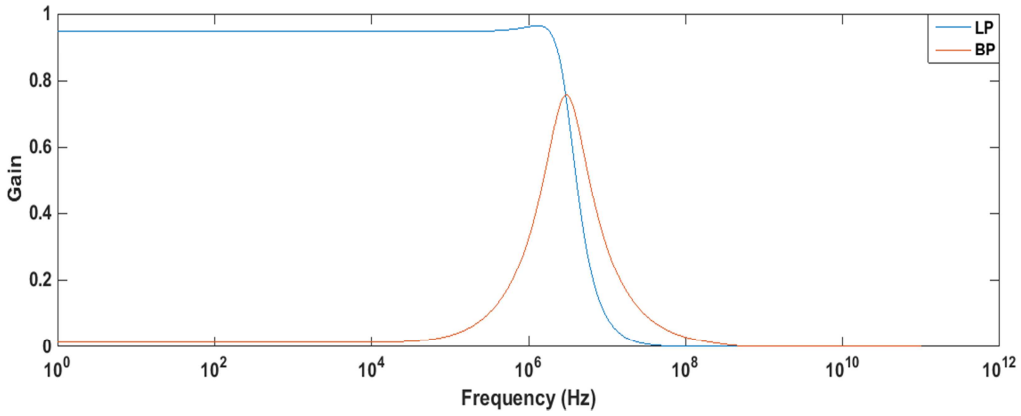


Figure 5.9 Frequency Response of proposed VM TT biquad filter

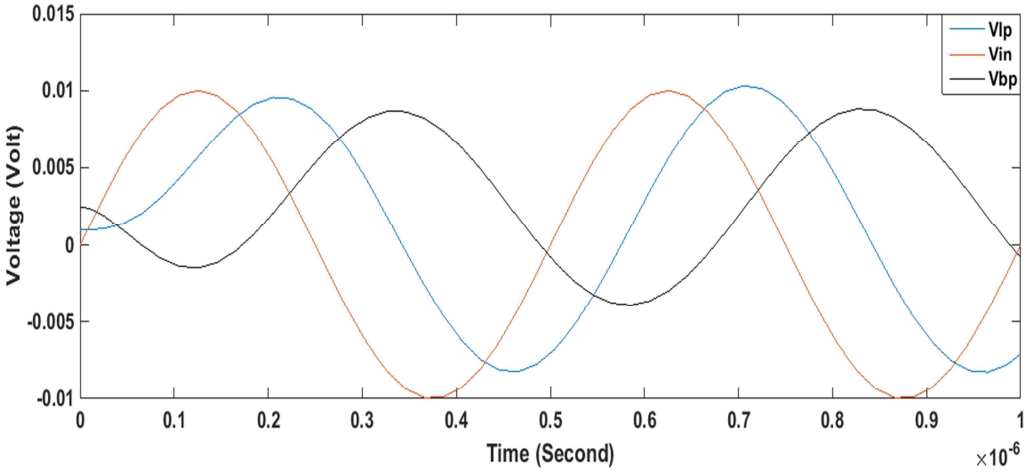


Figure 5.10 Time response of proposed VM TT biquad filter

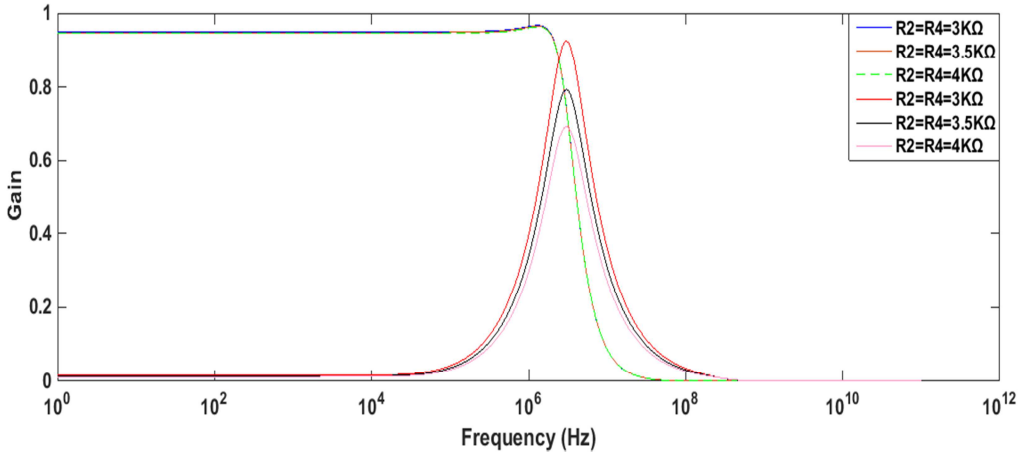


Figure 5.11 Variation in center frequency gain while other parameters are constant

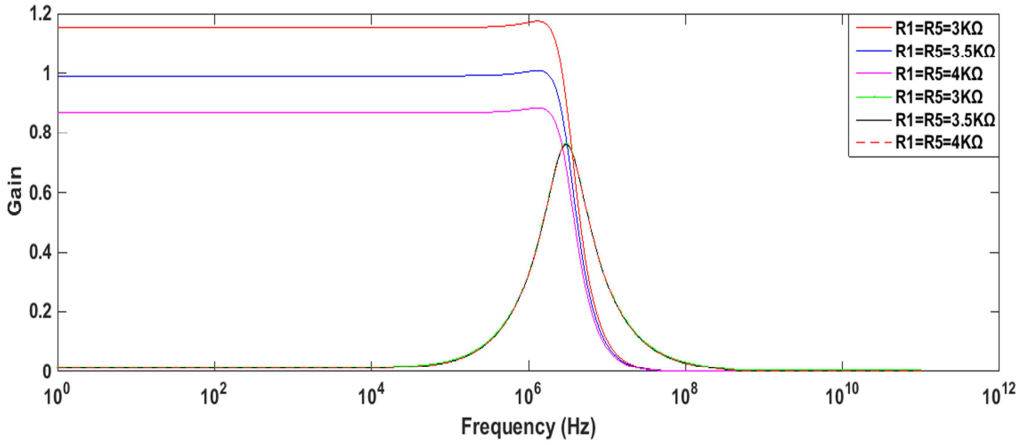


Figure 5.12 Variation in DC gain while other parameters are constant

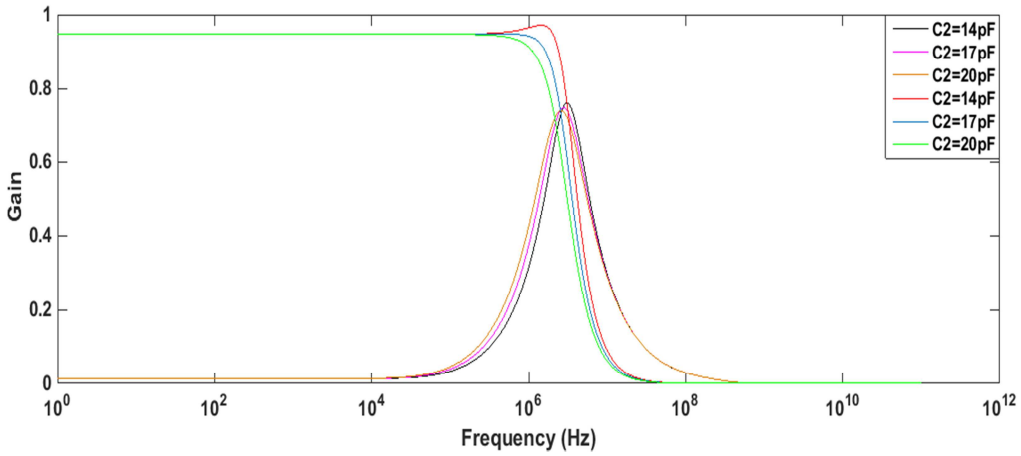


Figure 5.13 Variation in pole frequency while other parameters are constant

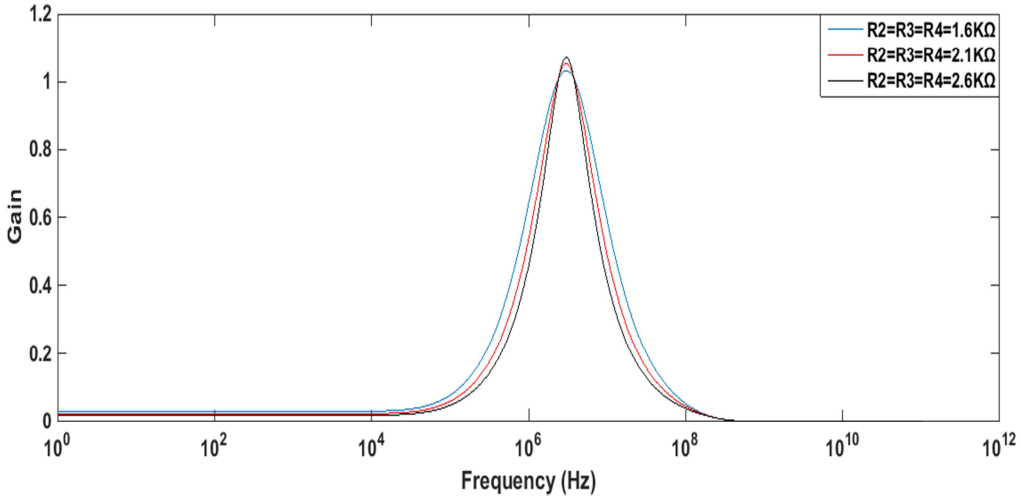


Figure 5.14 Variation in bandwidth while other parameters are constant

5.3 The proposed VDCC based current mode Tow-Thomas biquad filter:

The proposed VDCC based current mode (CM) multifunction Tow-Thomas biquad filter is shown in figure 5.15. In this, the important thing is that the passive elements are used as grounded element. So it is easy to fabricate in the form of IC. From the analysis of the circuit shown in figure 5.15, the transfer function of band pass response is given as follows

$$T_{BP}(s) = \frac{I_{BP}}{I_{IN}} = \frac{s\left(\frac{g_{m1}R_3}{C_1R_1}\right)}{s^2+s\frac{g_{m1}R_3}{R_1C_1}+\frac{g_{m1}g_{m2}R_4R_3}{C_1C_2R_2R_1}} \quad (5.33)$$

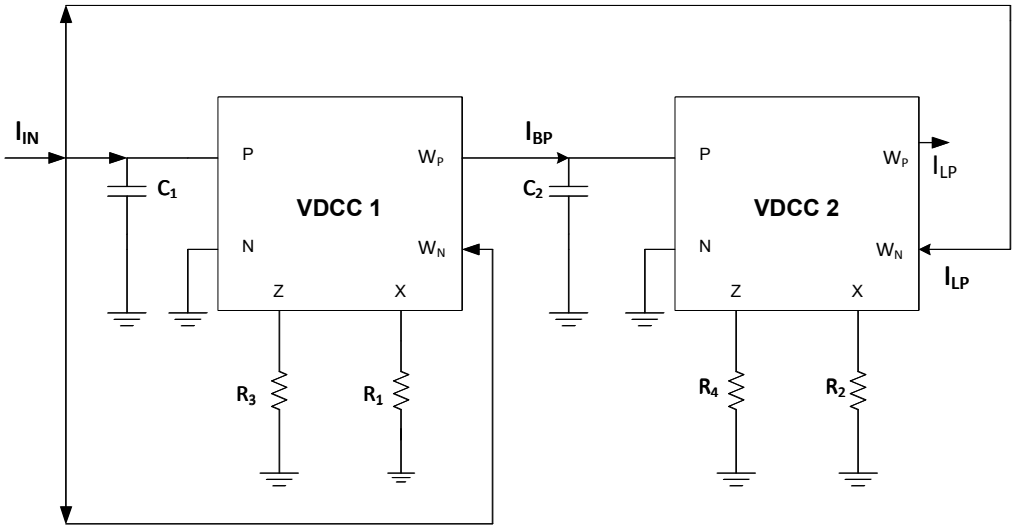


Figure 5.15 Proposed current mode multifunctional Tow-Thomas biquad filter using VDCC

It is clear that this transfer function is resulting in non-inverting band pass response. Similarly, the transfer function of low pass response is given as follows

$$T_{LP}(s) = \frac{I_{LP}}{I_{IN}} = \frac{\frac{g_{m1}g_{m2}R_3R_4}{C_1C_2R_1R_2}}{s^2+s\frac{g_{m1}R_3}{R_1C_1}+\frac{g_{m1}g_{m2}R_4R_3}{C_1C_2R_2R_1}} \quad (5.34)$$

It is clear that this transfer function is resulting in non-inverting low pass response. The important parameters of this filter are pole frequency (ω_0), bandwidth (BW) and quality factor (Q) which can be expressed as follows

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}R_3R_4}{C_1C_2R_1R_2}} \quad (5.35)$$

$$BW = \frac{g_{m1}R_3}{R_1C_1} \quad (5.36)$$

$$Q = \sqrt{\frac{g_{m2}R_1R_4C_1}{g_{m1}R_2R_3C_2}} \quad (5.37)$$

where g_{m1} is transconductance of block VDCC 1 and g_{m2} is transconductance of block VDCC 2. For low pass response, the DC gain is unity and similarly, for band pass response, the center frequency gain is also unity. It can be remarked that pole frequency can be controlled by varying

R_2, R_4, C_2 and g_{m2} without affecting bandwidth. The sensitivities of ω_0 and Q of proposed filter are given as follows

$$S^{\omega_0}_{C_1,C_2,R_2,R_1} = -\frac{1}{2} \tag{5.38}$$

$$S^{\omega_0}_{g_{m_1},g_{m_2},R_4,R_3} = +\frac{1}{2} \tag{5.39}$$

$$S^{Q}_{g_{m_2},C_1,R_1,R_4} = +\frac{1}{2} \tag{5.40}$$

$$S^{Q}_{g_{m_1},C_2,R_2,R_3} = -\frac{1}{2} \tag{5.41}$$

5.3.1 Simulation results:

To prove the theoretical validity of the proposed current mode Tow Thomas biquad filter of figure 5.15 for pole frequency (f_0) = 5MHz and Q=0.707, the filter was simulated with PSPICE program. The passive elements are selected as R_3 = R_4 = 975Ω, R_2 = 6KΩ, R_1 = 3KΩ and C_1 = C_2 = 2pF. The bias current are selected as I_{B1} = 50μA (g_m = 273.13μA/V) and I_{B2} = 100μA. The low pass and band pass frequency responses and time responses are shown in figure 5.16 and figure 5.17 respectively.

The simulated pole frequency of band pass response and low pass response were measured as 5.5MHz and 5.54MHz respectively. In the case of band-pass response, pole frequency can be varied independently (without affecting bandwidth) which are shown in figure 5.18. By PSPICE simulation, the total power dissipation of the filter was calculated as 1.68 mW which is acceptable to design an IC implementation.

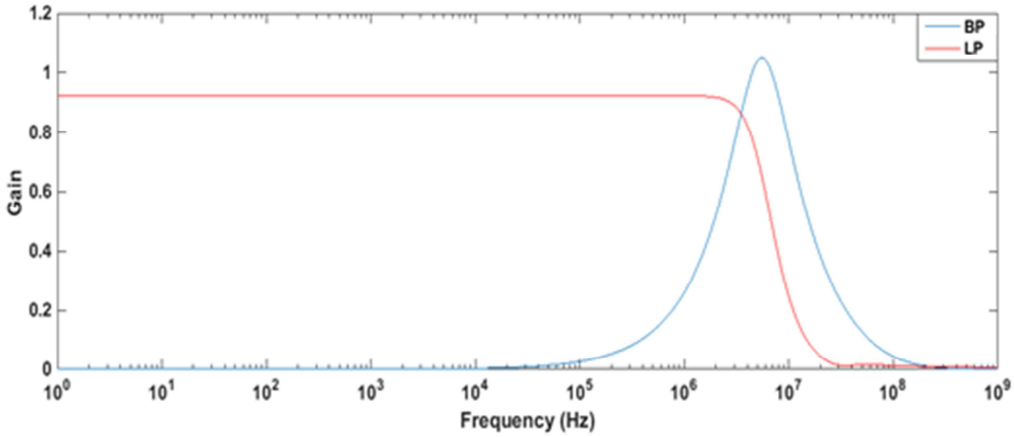


Figure 5.16 Frequency Response of proposed multifunctional CM TT biquad filter

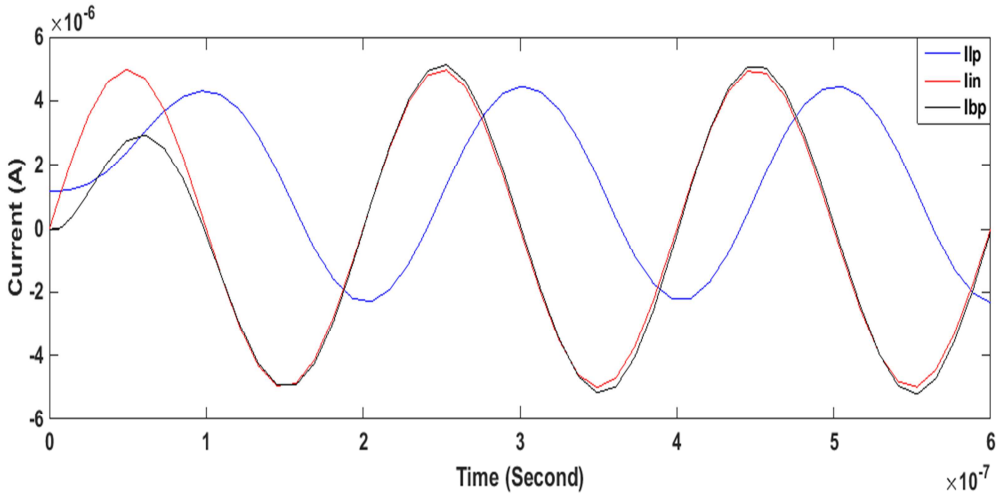


Figure 5.17 Time response of proposed multifunctional CM TT biquad filter

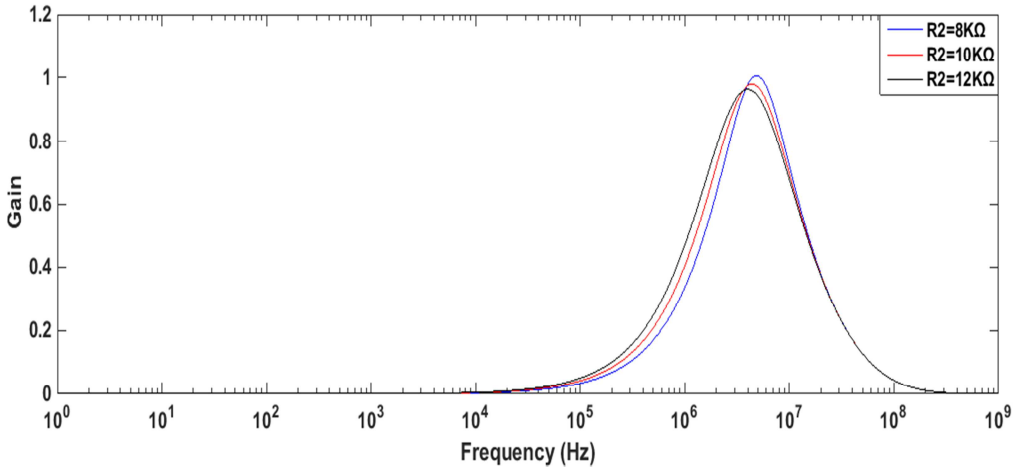


Figure 5.18 Frequency response of TT filter when pole frequency is varied and BW is constant

5.4 The proposed VDCC based voltage mode KHN biquad filter:

The block diagram of voltage mode multifunction KHN biquad filter is shown in figure 5.1. The proposed VDCC based voltage mode (VM) multifunction KHN biquad filter is shown in figure 5.19. In this, the important thing is that the passive elements are used as grounded element (except one resistor). So it is easy to fabricate in the form of IC.

From the analysis of the circuit shown in figure 5.19, the transfer function of band pass response is given as follows

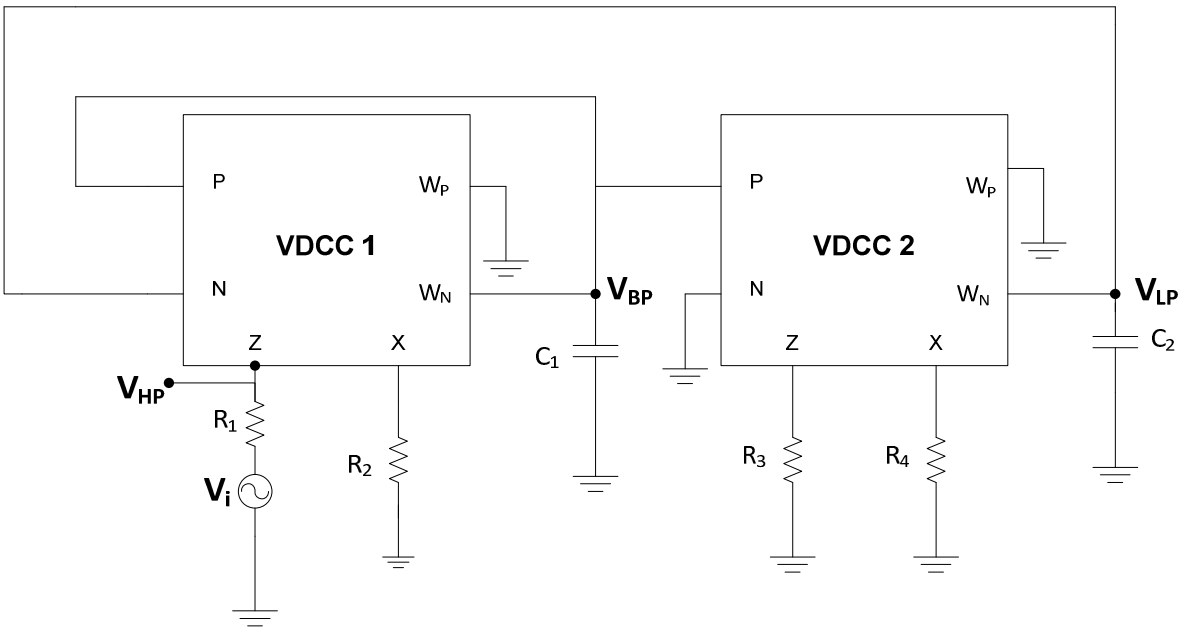


Figure 5.19 Proposed voltage mode multifunctional KHN biquad filter using VDCC

$$T_{BP}(s) = \frac{V_{BP}}{V_i} = \frac{-\frac{s}{C_1 R_2}}{s^2 + s\frac{g_{m1}R_1}{R_2 C_1} + \frac{g_{m1}g_{m2}R_1R_3}{C_1C_2R_2R_4}} \tag{5.42}$$

It is clear that this transfer function is resulting in inverting band pass response. Similarly, the transfer function of low pass response is given as follows

$$T_{LP}(s) = \frac{V_{LP}}{V_i} = \frac{\frac{g_{m2}R_3}{C_1C_2R_2R_4}}{s^2 + s\frac{g_{m1}R_1}{R_2 C_1} + \frac{g_{m1}g_{m2}R_1R_3}{C_1C_2R_2R_4}} \tag{5.43}$$

It is clear that this transfer function is resulting in non-inverting low pass response. Similarly, the transfer function of high pass response is given as follows

$$T_{HP}(s) = \frac{V_{HP}}{V_i} = \frac{s^2}{s^2 + s\frac{g_{m1}R_1}{R_2 C_1} + \frac{g_{m1}g_{m2}R_1R_3}{C_1C_2R_2R_4}} \tag{5.44}$$

The important parameters of this filter are pole frequency (ω_0), bandwidth (BW) and quality factor (Q) which can be expressed as follows

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}R_1R_3}{C_1C_2R_2R_4}} \tag{5.45}$$

$$\text{BW} = \frac{g_{m1}R_1}{R_2C_1} \tag{5.46}$$

$$Q = \sqrt{\frac{g_{m2}R_2R_3C_1}{g_{m1}R_1R_4C_2}} \tag{5.47}$$

For low pass response, the DC gain (K) is given by

$$K = \frac{1}{g_{m1}R_1} \tag{5.48}$$

For band pass response, the center frequency gain (-KQ) is given by

$$-KQ = -\frac{1}{g_{m1}R_1} \tag{5.49}$$

For high pass response, the high frequency gain (K) is equal to unity. Here g_{m1} is transconductance of block VDCC 1 and g_{m2} is transconductance of block VDCC 2. The sensitivities of ω_0 and Q of proposed filter are given as follows

$$S^{\omega_0}_{C_1,C_2,R_2,R_4} = -\frac{1}{2} \tag{5.50}$$

$$S^{\omega_0}_{g_{m_1},g_{m_2},R_1,R_3} = +\frac{1}{2} \tag{5.51}$$

$$S^{Q}_{g_{m_2},C_1,R_2,R_3} = +\frac{1}{2} \tag{5.52}$$

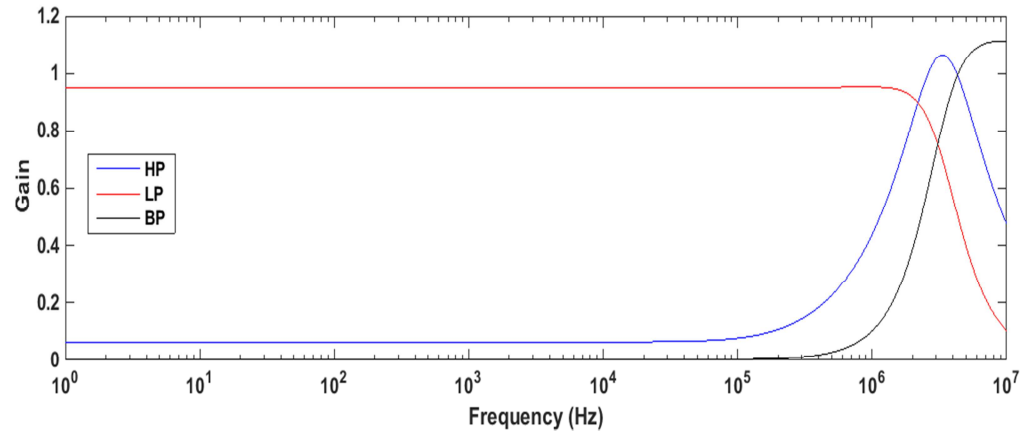
$$S^{Q}_{g_{m_1},C_2,R_1,R_4} = -\frac{1}{2} \tag{5.53}$$

It can be remarked that pole frequency can be controlled by varying R_3, R_4, C_2 and g_{m2} without affecting bandwidth.

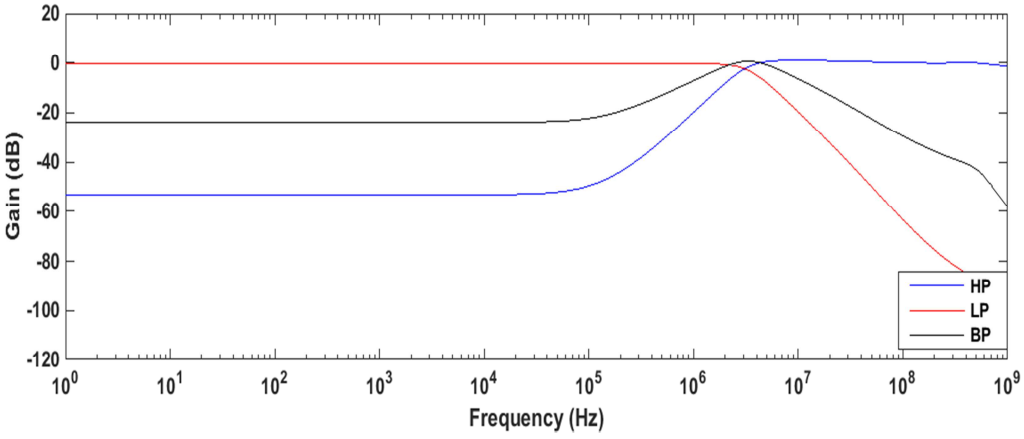
5.4.1 Simulation results:

To prove the theoretical validity of the proposed KHN biquad filter of figure 5.19 for pole frequency (f_0) = 3MHz and Q=0.707, the filter was simulated with PSPICE program. The passive elements are selected as $R_1 = R_3 = 3.5K\Omega$, $R_2 = 9K\Omega$, $R_4 = 18K\Omega$ and $C_1 = C_2 = 4pF$. The bias current are selected as $I_{B1} = 50\mu A$ ($g_m = 273.13\mu A/V$) and $I_{B2} = 100\mu A$. The low pass, high pass and band pass frequency responses and time responses are shown in figure 5.20 and figure 5.21 respectively.

The simulated pole frequency of band pass response, low pass response and high pass response were measured as 3.31MHz, 3.45MHz and 3.13MHz respectively. In the case of band-pass response, center frequency can be varied independently (without affecting bandwidth) which is shown in figure 5.22. For the testing of the input dynamic range of the 2nd order KHN filter, a sinusoidal signal of f_0 = 3 MHz with different amplitudes are applied to the input. The total harmonic distortion of the output signal versus amplitude of the input signal is shown in figure 5.23. The result shows that for input signal with amplitude lower than 200mV peak-to-peak, the THD remains below 2%. By PSPICE simulation, the total power dissipation of the filter was calculated as 1.69 mW which is acceptable to design an IC implementation.



(a)



(b)

Figure 5.20 Frequency Response of proposed multifunctional VM KHN biquad filter

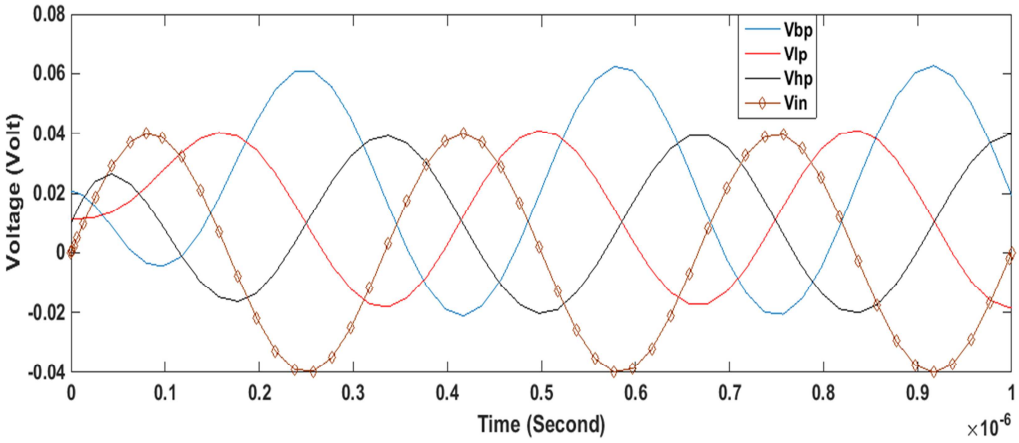


Figure 5.21 Time response of proposed multifunctional VM KHN biquad filter

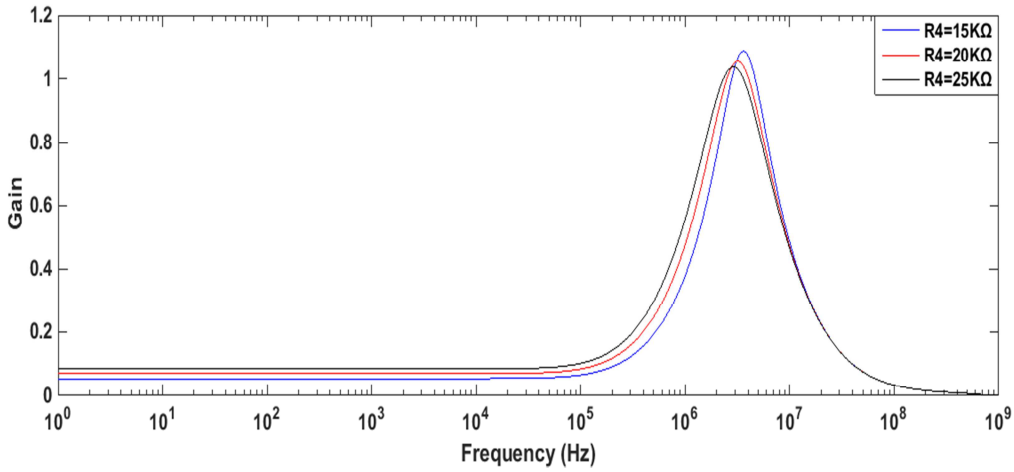


Figure 5.22 Frequency response of KHN filter when pole frequency is varied and BW is constant

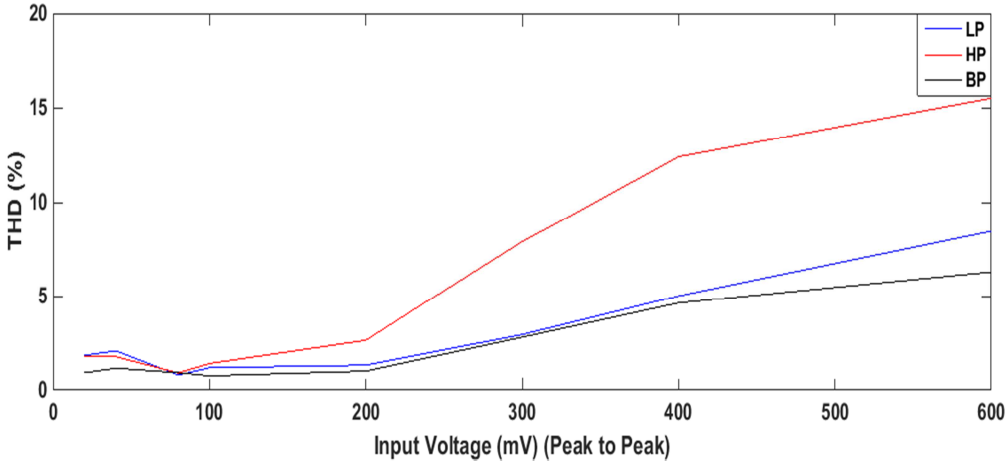


Figure 5.23 Dependence of output voltage THD on input voltage amplitude of VM KHN filter

5.5 Conclusion:

This chapter covers the basic theory of biquad filters and its types such as Tow-Thomas and KHN-biquad. The VDCC based multifunction voltage mode and current mode biquad filters have been proposed and simulated which verified the usability of VDCC in the analog signal processing among the novel active building blocks. Using PSPICE simulation, the results of tunability of central frequency, bandwidth and gain were noticed that they are independent to each other in case of voltage mode Tow-Thomas biquad filter. Table 5.1 shows the comparison between theoretical values and simulated values. Table 5.2 shows the comparison of the different voltage mode Tow-Thomas circuits using different active building blocks which confirm the practical utility of the proposed circuit.

Table 5.1 Comparison between theoretical values and simulated values

Sr. No.	Filter	Theoretical design value of pole frequency	Practical value of pole frequency for		
			Low pass response	High pass response	Band pass response
1.	Voltage mode Tow-Thomas biquad filter	3MHz	3.43MHz		3.16MHz
2.	Current mode Tow-Thomas biquad filter	5MHz	5.54MHz		5.5MHz
3.	Voltage mode KHN biquad filter	3MHz	3.45MHz	3.13MHz	3.31MHz

Table 5.2 Comparison of the different voltage mode Tow-Thomas circuits using different active building block [5]

Active element	Block	Resistor (G=Grounded F=Floating)	Capacitor (G=Grounded F=Floating)	Independent gain control
Op-Amp	3	6F	2F	Yes
OTRA	2	4F	2F	Yes
CCII	3(+)	4F	2F	Yes
CCII	3(+)	1G + 3F	1G + 1F	Yes
CCII	3(+)	2G + 2F	1G + 1F	Yes

CCII	3(+)	2G + 2F	2G	Yes
CCII	3(+)	3G + 1F	2G	Yes
CCII	3(+)	4G	2G	Yes
CCII	1(+) + 1(-)	2G + 1F	2G	No
DVCC	2(+)	3G	2G	No
DVCC	1(+) + 1(-)	3G	2G	No
VDCC (Proposed)	**2**	**4G + 1F**	**2G**	**Yes**

5.6 References:

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Chapter 6
Conclusion and future scope

6.1 Conclusion:

In chapter 2, a novel active building block namely VDCC has been discussed in detail. Its DC and AC characteristics of input-output have been verified using PSPICE simulation. The basic signal processing applications such as amplifiers and negative impedance converter have been designed using VDCC and simulated using PSPICE.

In chapter 3, grounded and floating inductances have been described which uses only single VDCC and two passive elements and has been applied to design a higher order butterworth filters which were simulated using PSPICE.

In chapter 4, realization of single VDCC based second order filters such as low pass filter, high pass filter and band pass filter have been discussed and simulated which verified the usability of VDCC in the analog signal processing among the novel active building blocks.

In chapter 5, a brief introduction of multifunction biquad filters design using the two-integrator in a loop methodology have been discussed. Finally, single input multiple output type voltage mode and current mode multifunction biquad filters using voltage differencing current conveyor have been discussed. The Tow Thomas biquad filter has low pass and band pass outputs. The KHN biquad filter has low pass, high pass and band pass outputs. The pole frequency, bandwidth and gain are independently tunable in case of voltage mode Tow Thomas biquad filter. These filters have been simulated in PSPICE using 0.18 um CMOS technology.

6.2 Scope for future work:

In the present work the application of VDCC as an inductor simulator and biquad filter has been discussed. VDCC is a very versatile block as it combines the features of both operational transconductance amplifier (OTA) as well as current conveyor (CCII). It can be used for realization of oscillators with different properties. Filter circuits with tuning properties in both current mode and voltage mode can also be realized with VDCC. Thus there is enough scope for extension of the work presented in this dissertation.

Appendix

PSPICE model file used for simulation is TSMC CMOS 0.18 µm process which has following model parameters -

.MODEL nmos_transistor **NMOS** (LEVEL=7 VERSION=3.1 TNOM=27 TOX=4.1E-9 XJ=1E-7 +NCH=2.3549E17 VTH0=0.354505 K1=0.5733393 K2=3.177172E-3 K3=27.3563303 +K3B=-10 W0=2.341477E-5 NLX=1.906617E-7 DVT0W=0 DVT1W=0 DVT2W=0 +DVT0=1.6751718 DVT1=0.4282625 DVT2=0.036004 U0=327.3736992 UA=-4.52726E-11 +UB=4.46532E-19 UC=-4.74051E-11 VSAT=8.785346E4 A0=1.6897405 AGS=0.2908676 +B0=-8.224961E-9 B1=-1E-7 KETA=0.021238 A1=8.00349E-4 A2=1 RDSW=105 PRWG=0.5 +PRWB=-0.2 WR=1 WINT=0 LINT=1.351737E-8 XL=-2E-8 XW=-1E-8 DWG=1.610448E-9 +DWB=-5.108595E-9 VOFF=-0.0652968 NFACTOR=2.4901845 CIT=0 CDSC=2.4E-4 +CDSCD=0 CDSCB=0 ETA0=0.0231564 ETAB=-0.058499 DSUB=0.9467118 +PCLM=0.8512348 PDIBLC1=0.0929526 PDIBLC2=0.01 PDIBLCB=-0.1 DROUT=0.5224026 +PSCBE1=7.979323E10 PSCBE2=1.522921E-9 PVAG=0.01 DELTA=0.01 RSH=6.8 +MOBMOD=1 PRT=0 UTE=-1.5 KT1=-0.11 KT1L=0 KT2=0.022 UA1=4.31E-9 UB1=-7.61E-+18 UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1 WWL=0 LL=0 LLN=1 LW=0 +LWN=1 LWL=0 CAPMOD=2 XPART=0.5 CGDO=7.7E-10 CGSO=7.7E-10 CGBO=1E-12 +CJ=1.010083E-3 PB=0.7344298 MJ=0.3565066 CJSW=2.441707E-10 PBSW=0.8005503 +MJSW=0.1327842 CJSWG=3.3E-10 PBSWG=0.8005503 MJSWG=0.1327842 CF=0 +PVTH0=1.307195E-3 PRDSW=-5 PK2=-1.022757E-3 WKETA=-4.466285E-4 +LKETA=9.715157E-3 PU0=12.2704847 PUA=4.421816E-11 PUB=0 PVSAT=1.707461E3 +PETA0=1E-4 PKETA=2.348777E-3)

.MODEL pmos_transistor **PMOS** (LEVEL=7 VERSION=3.1 TNOM=27 TOX=4.1E-9 XJ=1E-7 +NCH=4.1589E17 VTH0=-0.4120614 K1=0.5590154 K2=0.0353896 K3=0 K3B=7.3774572 +W0=1E-6 NLX=1.103367E-7 DVT0W=0 DVT1W=0 DVT2W=0 DVT0=0.4301522 +DVT1=0.2156888 DVT2=0.1 U0=128.7704538 UA=1.908676E-9 UB=1.686179E-21 +UC=-9.31329E-11 VSAT=1.658944E5 A0=1.6076505 AGS=0.3740519 B0=1.711294E-6 +B1=4.946873E-6 KETA=0.0210951 A1=0.0244939 A2=1 RDSW=127.0442882 PRWG=0.5

+PRWB=-0.5 WR=1 WINT=5.428484E-10 LINT=2.468805E-8 XL=-2E-8 XW=-1E-8
+DWG=-2.453074E-8 DWB=6.408778E-9 VOFF=-0.0974174 NFACTOR=1.9740447 CIT=0
+CDSC=2.4E-4 CDSCD=0 CDSCB=0 ETA0=0.1847491 ETAB=-0.2531172 DSUB=1.5
+PCLM=4.8842961 PDIBLC1=0.0156227 PDIBLC2=0.1 PDIBLCB=-1E-3 DROUT=0
+PSCBE1=1.733878E9 PSCBE2=5.002842E-10 PVAG=15 DELTA=0.01 RSH=7.7
+MOBMOD=1 PRT=0 UTE=-1.5 KT1=-0.11 KT1L=0 KT2=0.022 UA1=4.31E-9
+UB1=-7.61E-18 UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1 WWL=0 LL=0
+LLN=1 LW=0 LWN=1 LWL=0 CAPMOD=2 XPART=0.5 CGDO=7.11E-10 CGSO=7.11E-10
+CGBO=1E-12 CJ=1.179334E-3 PB=0.8545261 MJ=0.4117753 CJSW=2.215877E-10
+PBSW=0.6162997 MJSW=0.2678074 CJSWG=4.22E-10 PBSWG=0.6162997
+MJSWG=0.2678074 CF=0 PVTH0=2.283319E-3 PRDSW=5.6431992 PK2=2.813503E-3
+WKETA=2.438158E-3 LKETA=-0.0116078 PU0=-2.2514581 PUA=-7.62392E-11
+PUB=4.502298E-24 PVSAT=-50 +PETA0=1E-4 PKETA=-1.047892E-4)