CURRENT MODE LOGIC WITH ENHANCED PERFORMANCE

by

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(2K9/PhD/EC/02)

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to the

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Candidate's Declaration

I hereby certify that the research work which is being presented in the thesis entitled "**Current Mode Logic with Enhanced Performance**" in fulfillment of requirement of the award of degree of Doctor of Philosophy is an authentic record of my own research work carried under the guidance and supervision of Dr. Neeta Pandey (Delhi Technological University) and Prof. Maneesha Gupta (Netaji Subhas Institute of Technology).

The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for award of any degree.

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Certificate

This is to certify that the thesis titled "**Current Mode Logic with Enhanced Performance**" being submitted by Kirti Gupta to the Department of Electronics and Communication Engineering, Delhi Technological University, New Delhi, for the award of the degree of Doctor of Philosophy, is a record of a bonafide research work carried out by her under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in the thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

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Abstract

The recent advancement in VLSI technology has facilitated the integration of digital and analog circuits on a single chip. This integration has enabled the user to directly take the data from the real world and process it within a digital system. A single chip realization results in improved performance, lower cost and smaller size. It, however, poses critical constraint due to the switching noise in CMOS digital circuits which gets coupled to the analog parts and degrades their accuracy. This problem becomes severe at higher operating frequencies as aggressive technology scaling is often used to improve the chip performance and the integration levels. Therefore noise becomes important along with design matrices such as area, power consumption and speed; and needs attention.

To minimize the effect of noise, research efforts are directed towards (i) minimizing noise coupling (ii) reduction of switching noise generated in CMOS digital circuits. Several techniques are suggested at different levels of abstraction which fundamentally work on limiting the coupling of the noise to analog parts. Emergence of various low noise logic styles is the outcome of the considerable progress in the direction of reducing switching noise generation which is achieved by keeping power supply current nearly constant during the switching event and/or working with smaller voltage swings. These logic styles can be classified in four categories namely current balance logic (CBL) style, current steering logic (CSL) style, folded source-coupled logic (FSCL) style and the MOS current mode logic style. MOS current mode logic (CML) style among these is attractive as it addresses both the issues and is explored in this work.

The work on CML gates ranges from modifying the basic topology, analysis and design, to the applications in communication systems (phase-locked loop and ring

oscillators), optical fiber links (multiplexing and demultiplexing) and microprocessors and signal processors, (adders, multipliers and compressors). The prime concern of these is to provide better performance and enable designer to adopt systematic design methodology.

A CML gate primarily consists of a pull down network (PDN) to implement the logic function, a current source that maintain a constant bias current, and a load to perform the current to voltage conversion. New topologies are developed in this work for reducing the minimum power supply voltage requirement, eliminating the use of CMOS circuit elements, decreasing power consumption, enhancing speed, reducing the gate count in circuit realization. These are achieved by applying modifications in the PDN, load, and the current source sections of the basic CML gate. The proposed topologies are analyzed and suitable design procedure is put forward.

The power supply requirement in a CML gate is decided by the number of source-coupled transistor pair levels in the PDN and can be lowered by reducing this number. The triple-tail cell concept is introduced in the PDN and new topologies are developed. An analytical approach to model their behavior is presented. An important contribution in this topic is the identification of the design cases where the proposed topologies can be advantageously adopted.

The static power consumption of a CML gates is a major hindrance in employing these for portable system design. In this research work, the scheme employing dynamic current source is considered. New improved dynamic CML (D-CML) gates are examined and the techniques to implement multi-stage applications are also discussed. The elimination of the CMOS inverter from the available dynamic current source and a new self-timed buffer are the major contributions in this area.

The speed of the CML gates needs to be improved in order to meet the high data-transmission rate. A new active load without using any passive component is presented. New differential and PFSCL topologies are developed and are examined. A complete mathematical model for the static parameters and the delay is developed and a design procedure is put forward. The improvement in the speed of the CML gates through the capacitive coupling phenomenon in the proposed load is the main contribution.

The conventional NOR based realization of PFSCL circuits consist of multiple gates. An alternate approach that reduces the gates count in PFSCL circuit realization is proposed wherein triple-tail cell concept is applied. The development of a new fundamental cell and its various configurations is the research contribution.

Tri-state circuits find ubiquitous use in Field Programmable Gate Arrays (FPGAs), microprocessors and clock/data recovery systems. Two CML tri-state circuits are available in literature. In an effort to the lower power consumption, a new CML tri-state circuit is proposed.

All the theoretical propositions are verified through extensive SPICE simulations using TSMC 0.18 μm technology parameters and are compared with the existing counterparts to demonstrate their effectiveness.

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International Journal

1. Neeta Pandey, Kirti Gupta, and Maneesha Gupta, "An Efficient Triple-tail Cell based PFSCL D Latch," **Microelectronics Journal, Elsevier**, vol. 45, no. 8, pp. 1001-1007, 2014.

2. Kirti Gupta, Neeta Pandey, and Maneesha Gupta, "Analysis and Design of MOS Current Mode Logic Exclusive-OR Gate using Triple-tail Cells," **Microelectronics Journal, Elsevier**, vol. 44, no. 6, pp. 561-567, 2013.

3. Kirti Gupta, Neeta Pandey, and Maneesha Gupta, "MCML D-Latch Using Triple-Tail Cells: Analysis and Design," **Active and Passive Electronic Component**, vol. 2013, pp. 1-9, 2013.

4. Kirti Gupta, Neeta Pandey, and Maneesha Gupta, "Low-Power Tri-State Buffer in MOS Current Mode Logic," **Analog Integrated Circuits and Signal Processing, Springer**, vol. 75, pp. 157-160, 2013.

5. Kirti Gupta, Neeta Pandey, and Maneesha Gupta, "Low-Voltage MOS Current Mode Logic Multiplexer," **Radioengineering Journal**, vol. 22, no. 1, pp. 259-268, 2013.

6. Kirti Gupta, Neeta Pandey, and Maneesha Gupta, "MOS Current Mode Logic with Capacitive Coupling," **ISRN Electronics**, vol. 2012, Article ID 473257, pp. 1-8, 2012.

International Conferences

1. Kirti Gupta, Neeta Pandey, and Maneesha Gupta, "Performance Improvement of PFSCL gates through Capacitive Coupling," proceedings of **IEEE International**

Conference on Multimedia, Signal Processing and Communication Technologies, Aligarh, pp. 185-188, 2013.

2. Neeta Pandey, Radhika Tanwar, Kirti Gupta, and Maneesha Gupta, "Low Power D-Latch Design using MCML Tri-state Buffers," proceedings of **IEEE International Conference on Signal Processing and Integrated Networks**, Greater Noida, pp. 531-534, 2014.

1.1 BACKGROUND

In last few decades, most of the research efforts are being directed towards moving the signal processing to the digital domain. However in application areas such as digital and mobile communication, microprocessors and sensor design, it is difficult to substitute analog functions with their digital counterpart. Therefore, there is need for combining the high resolution, low power, low voltage analog circuits with high frequency complex digital circuits and placing these on a single die to reduce the cost and improve the reliability of the complete electronic system. This need led towards the development of mixed mode circuit design [1-4]. The accuracy of analog parts in such circuits is degraded due to coupling of noise generated in digital circuits. The problem is alleviated further at higher operating frequencies as aggressive technology scaling is often used to improve chip performance and integration levels. Therefore noise becomes important along with design matrices such as area, power consumption and speed; and needs attention.

The conventional CMOS logic is often employed in digital circuits owing to its ease in designing, high speed capability, high packing density and negligible static power consumption [5, 6]. In spite of these advantageous features, the CMOS logic suffers from large current spikes during the switching which flow through parasitic interconnects, bonding wire and pin to pin inductance. This degrades the resolution of the sensitive analog circuits via supply line and substrate coupling [4, 7]. To overcome this shortcoming, several methods are suggested in literature which works at different levels of abstraction [7-11]. The silicon-on-insulator or a highly doped epitaxial wafer is used at technology level to reduce substrate coupling. It however increases the fabrication cost. At physical level careful floor planning

and skilled layout techniques are used. The analog and digital blocks are placed apart at floor planning level, whereas diffused guard bands are suggested at the layout level. At circuit level, fully differential and substrate referenced analog architectures are preferred due to their intrinsic noise immunity features. Separate power grids, multiple supply pins and bonding wires are suggested at the system level. All these methods are based on reducing the amount of coupled noise. The noise problem can further be addressed by reducing the switching noise in digital circuits. This insight directed researchers to explore new logic styles.

The switching noise can be lowered by reducing the voltage swing and the amount of current that flows during switching event [12]. Variety of logic styles [13-26] are presented in the literature which maintain a nearly constant current during the switching event and therefore are suitable for mixed-signal IC design. These logic styles can be classified in four categories as current balance logic (CBL) [13-16], current steering logic (CSL) [17-19], folded source-coupled logic (FSCL) [11, 20-22] and the MOS current mode logic [23-26]. The CBL is further classified into enhanced current balance logic (E-CBL) [14], complementary output current balance logic(C-CBL) [15], modified current balance logic (M-CBL) [16]. Similarly, the CSL includes folded current steering logic (FCSL) [18], differential current steering logic (D-CSL) [19] whereas the enhanced folded source-coupled logic (EF^2SCL) [21], and enhancement source-coupled logic [22] belongs to FSCL style. The CBL and FSCL based circuits use multiple current sources for logic function realization whereas the CSL circuits work on larger voltage swing. The MOS current mode logic based circuits need a single current source and work on smaller voltage swing; therefore it is a preferred choice for mixed signal IC applications.

1.2 CURRENT MODE LOGIC

A current mode logic gate uses a differential amplifier as the fundamental block. It consists of three main parts namely a pull down network (PDN), a current source, and a load [23-26]. The PDN implements the logic function; the current source generates the constant bias current while the load performs the current to voltage conversion. Depending on the nature of the inputs and outputs, a current mode logic gate can be differential or single-ended [27].

In this work, MOSFET based current mode logic (CML) topologies have been investigated with the objective of

- Lowering the value of minimum power supply voltage,
- Eliminating the use of CMOS circuit elements,
- Reduction in power consumption,
- Speed enhancement,
- Reduction of gate count for logic function realization.

Keeping in view the above objectives, new topologies are developed by modifying the PDN, the load, and the current source sections of the basic CML gates. The analysis of the topologies so developed is carried out and suitable design procedure is put forward.

1.3 AVAILABLE LITERATURE AND SCOPE OF WORK

The existing literature on CML gates is broadly classified under the following three categories

(i) Various CML topologies [28-67]

(ii) Analysis and design [26, 27, 68-84]

(iii) System applications [85-114]

Various CML topologies [28-67]

A variety of CML topologies [28-67] have been reported in literature wherein PDN, load and current source sections are modified in order to improve performance. The modifications are briefly reviewed in the following subsection.

The PDN in a CML gate realizes the functionality and consists of source-coupled transistor pairs [27]. Many design methods to implement the PDN of the conventional CML gate for speed enhancement [28, 29, 34-40] and power reduction [30-33] are reported. The first method [28, 29] employs feedback transistors in the PDN to eliminate the effect of threshold voltage fluctuations during fabrication and results in speed improvement. Analytical formulations for the same are also presented and the concept is verified through IC implementation of a multiplexer and demultiplexer for optical-fiber link. The second method [30, 31] aims at reducing the power consumption by lowering the minimum power supply required by the gate. It uses transistors with different threshold voltage for each level of source-coupled transistor pairs in the PDN. The gates based on this methodology are named as multi-threshold CMOS (MTCMOS) MOS current mode logic gates. An entirely different approach to reduce power consumption is proposed in [32, 33]. It introduces an extra invalid level in addition to the high and low logic levels of a conventional CML gate and is called as triple-rail MOS current mode logic (Tr-MCML) style. The new style is shown to be beneficial for pipeline operations and also supports power-on-demand operations in pipeline architectures. In an effort to improve performance of single-ended CML style, positive-feedback is applied to replace the voltage reference source and resulting topology is termed as positive-feedback source-coupled logic (PFSCL) [34]. This change

provides significant improvement in the speed, power and area. The analysis, modeling and design of the PFSCL gate are presented in [35-40].

In a CML gate, the load is mainly used to perform the current to voltage conversion and determines the voltage swing and speed of the gate. Conventionally, a passive resistor or a PMOS transistor operating in the linear region [27] is used as load. The modifications in the load section are reported to enable adaptation to real time environments [41, 42], improve speed [43-52] and provide high resistor value [53-60]. The conventional load provides a fixed resistance and hence a fixed voltage swing. An adaptable bias and swing controllers are employed in [41, 42] for resistance variations. The controllers set the bias voltages of all the PMOS load transistors according to the desired current and voltage swing thereby making circuits ready for real time adaptation. These are termed as Adaptable MOS current mode logic (AMCML) circuits. Another refinement in load is introduction of shunt peaking [43-52] wherein an inductor is connected in series with conventional resistive load. The CML gates using the passive inductor and the active inductor are presented. The gate with passive inductor provides significant speed improvement but is not preferred due to the restrictions such as large component size and lengthier design process [47]. An active inductor employing an NMOS transistor with its gate connected to separate supply via resistor is suggested as an alternative [51]. The CML gates operating in sub-threshold region (also called as subthreshold source-coupled (STSCL) gates) [53-60] work on very small value of the bias current, therefore a high valued resistance is needed to maintain the desired voltage swing. A bulk-drain connected PMOS transistor is recommended as load for these gates.

A CML gate employs a current source to maintain a constant bias current. The constant bias current is advantageous in lowering the switching noise but results in static power consumption which restricts its usage for low power applications. Many attempts are made towards the reduction of the static power consumption [61-67]. The first attempt replaces the constant current source with a dynamic current source [61, 62]. These gates works on the precharge-evaluate logic and require an additional clock signal to achieve the desired functionality. The gates do not have static power consumption but show small dynamic power due to the small instantaneous current during switching transitions. Such gates are named as dynamic current mode logic (DyCML) gates. The second attempt allows the current source to operate only during the transitions at input, giving rise to a Self-timed MOS current mode logic (ST-MCML) style reported in [63]. It however uses two additional components namely a pulse generator and a sense amplifier. The pulse generator generates the short duration pulses corresponding to the transitions in the inputs. The short duration pulses drive the current source instead of a constant voltage and hence lower the static power consumption. The sense amplifier measures the small changes at the inputs and amplifies it to the desired output levels. The sleep methods are applied as third attempt in order to lower the power consumption in differential MOS current mode logic circuits [64-67] where sleep transistor are placed in series with the power supply. These circuits have two operating modes namely the active mode and the sleep mode. In the active mode, the sleep transistor connects the power supply to the circuit to execute the normal operation. In the sleep mode, the sleep transistor isolates the power supply from the circuit to reduce the power consumption. Different sleep mechanisms to shut down the current source or to simply cut off the current are presented in [66-67].

Analysis and design [26, 27, 68-84]

The behavior of the CML gate is analyzed in terms of static parameters and delay. The former is expressed in terms of parameters such as voltage swing, noise margin and the gain while the propagation delay is representative of the later one. The behavior of CML gates is analyzed in terms of static parameters and basic RC delay in [27, 68-76] using various MOS models such as Sah [68], BSIM [69-74] and alpha power law [75, 76].

The ultimate goal of the design is to determine the aspect ratios of the transistors in the PDN, load and the current source sections for given design specifications and the selection of a bias current to meet design constraints. The available design approaches can be broadly divided into three categories [26, 27, 68-84]. The first approach is simulation based wherein the CML gates are sized according to high speed or low power performance levels [26]. In high speed design, the primary aim is to minimize the delay therefore high bias current is recommended. It results in larger transistor sizes and higher power supply to meet the desired static characteristics. For low power gate, a small bias current may be used that can work with small transistors and power supply values. This approach is time consuming due to the tedious simulation iterations. The second is analytical approach and is termed as the pencil-and-paper approach [27, 68-76]. The aspect ratios of the transistors are expressed as a function of the bias current to meet the noise margin requirements. The bias current is determined according to the power efficient, high speed and low power design criteria. This approach is based on linearization of transistor parameters and therefore is suitable in early design phases. The third one is algorithmic approach [77-84] wherein all the performance parameters are considered simultaneously and optimal design satisfying the performance requirement is derived. Here, the design of CML gates is treated as an optimization problem

with nonlinear design constraints and linear goal function. Various solution algorithms have been suggested and are implemented in different software programs.

System applications [85-114]

CML gates are extensively used in a wide variety of applications due to its high speed and reduced switching noise characteristics. Typical application areas include communication systems, optical fiber links, microprocessors and signal processors.

In communication systems, a phase-locked loop (PLL) is the key element used for frequency synthesis, clock generation, data recovery and synchronization. A typical PLL consists of a mixer/phase detector, low pass filter, voltage controlled oscillator and a frequency divider. The phase detector primarily uses a XOR gate or D latch. Frequency divider realized as a cascade of divide-by-two stages can be classified as regenerative and static type. Various implementations for phase detector [85-89] and frequency divider [90-93] are available in literature. The oscillators also play an important role in modulation and demodulation of the signals. The implementations of the ring oscillators and their design are presented in [94, 95].

Another important application field for CML circuits is the optical-fiber-link system wherein multiplexing and demultiplexing of signals is commonly used for the efficient utilization of the optical fiber channel bandwidth. A multiplexer transfers the data serially across the optical fiber which is then transferred in parallel through a demultiplexer. The realizations of multiplexer and demultiplexer involving D latch are shown in [27-29].

The CML gates are employed in the design of number of circuits often used in the datapaths of microprocessors and signal processors [96-102]. The datapath is the core of the processor and consists of an interconnection of basic combinational functions such as arithmetic

(addition, multiplication, shift and comparison) and logic operators. A variety of complex building blocks such as adders [103-105], compressors [62] and multipliers [106-109] are available. The use of CML circuits to implement pipeline datapath systems is demonstrated in [25, 109-114].

Following are the highlights of the proposed work in the field of current mode logic gates.

- A design methodology for differential CML gates that is beneficial for high speed and low power design cases.
- A dynamic current source which eliminate the CMOS inverter from the available [61] one. A self timed buffer for cascading dynamic CML circuits based on new dynamic current source.
- Introduction of capacitive coupling in the load that result in speed improvement.
- An efficient scheme for complex PFSCL circuit realization which improves both speed and power consumption by reducing the total gate count.
- A differential topology for tri-state CML circuits that consumes low power.

1.4 ORGANIZATION OF THE THESIS

There has been a continuous evolution of electronic system design to suit the needs of the market. Traditionally the digital system designs are aimed at adapting to the continual reduction in feature size, high speed and low power consumption. However there is a renewed interest in finding topologies catering to high frequency mixed signal applications. Although the performance of CMOS technologies improves notably with scaling, conventional static CMOS generates significant switching noise, thus hindering the on-chip integration of analog with digital circuits. Hence, alternate logic styles having the feature of

low noise level generation are explored. The CML style is the most promising style among the ones suggested in literature [13-26], and therefore forms the main subject of the thesis. New topologies by modifying the basic parts of the conventional CML gate are suggested in the work. A brief outline of the research work carried out in the thesis is presented.

Chapter-1 focuses on the noise generated by the digital circuits in mixed-signal environments and briefly presents the available methods to reduce the propagation of the noise to analog blocks. The noise reduction by employing different low noise digital logic families is also addressed and the advantages of MOS current mode logic family over the others are highlighted. A review of the earlier work on MOS current mode logic circuits is presented. This is followed by the outline of the research work presented in this thesis.

Chapter-2 is devoted to the study of the conventional MOS current mode logic gates. A detailed analysis and design procedure of differential CML and single-ended (PFSCL) inverter based on the pencil-and-paper approach are presented. The mathematical expressions are derived using BSIM3v3 transistor model equations and are used in the analysis of the proposed CML circuits in the work. The realization of the basic logic gates in differential CML and the single-ended (PFSCL) styles are also included.

In **Chapter-3** the pull down network of the differential CML gate is modified to lower the power supply requirement. The triple-tail cell concept is introduced for logic function realization to reduce the number of source-coupled transistor pair levels. New triple-tail cell based topologies for differential combinational and sequential CML gates are presented. A design-oriented model for the new topologies is derived with an intention to develop an understanding on the impact of design and process parameters. The performance

of the proposed topologies is illustrated for low power, high speed and power efficient design cases.

A CML gate consumes static power thereby restricting its usage in portable applications. In order to reduce static power consumption, the available modifications in the current source section are briefly reviewed and the scheme employing dynamic current source is chosen. **Chapter-4** presents new improved dynamic CML (D-CML) gates and examines their behavior. The design of multi-stage applications is explored and a novel implementation of the self-timed buffer is put forward. The chapter ends by presenting a performance comparison between the proposed D-CML and the conventional CML gates.

Chapter-5 deals with the speed improvement of the CML gates by modifying its load. The proposed load uses the capacitive coupling phenomenon. A complete mathematical model for static parameters and the delay is developed for differential CML and PFSCL gates. A systematic design procedure to size the bias current and the transistor aspect ratio to meet design goals is also presented.

Efficient realization of a logic function in PFSCL style is the aim of **Chapter-6.** A method to reduce the gate count in comparison to the conventional NOR based logic function realization is proposed. A new fundamental cell developed by applying triple-tail cell concept in PFSCL style is presented and analyzed. The use of fundamental cell in realizing various logic functions is discussed and the overall improvement in terms of gate count, propagation delay and power is compared with the conventional ones.

Tri-state circuits are the essential elements in bus organized and programmable logic devices and are explored in **Chapter-7.** The implementation of tri-state circuits in CML style is worked upon. A brief review of the existing tri-state CML inverter/buffer implementation

is presented. Thereafter, a low power implementation of the tri-state CML inverter/buffer is proposed.

The work is concluded exactly on the roadmap outlined above with a scope of updating as per latest available on the subject in **Chapter-8**.

The functionality of the proposed circuits and the accuracy of the mathematical formulations in the research work are validated through SPICE simulations by using TSMC 0.18 μm CMOS technology parameters.

2.1 INTRODUCTION

In the last few decades, the electronic industry has witnessed a phenomenal growth due to the advancements in the integration technologies. The current trend is towards the high resolution mixed signal integrated circuits. The current mode logic style is preferred in digital circuit design over CMOS logic style due to its low noise characteristics. The current mode logic gates were originally implemented by using bipolar transistor [27] and currently due to the advantages offered by MOS transistors, current mode logic gates employing them are favored.

This chapter presents the basic concepts of the MOS based current mode logic (CML) gate. The operation of the CML gate is described first, followed by the analysis and design of differential and the single-ended CML inverters using pencil-and-paper approach. The realization of basic digital gates in CML style is also discussed.

2.2 BASIC CONCEPTS

The basic architecture of a CML gate consists of a pull down network (PDN), a current source and a load. The PDN implements the logic function, the current source maintains a constant bias current and the load performs the current-to-voltage conversion [23-25]. The schematic of a CML inverter with inputs (v_{in1} and v_{in2}) and outputs (v_{out1} and v_{out2}) is shown in Fig. 2.1. The PDN comprises of source-coupled transistor pair (M2-M3), the current source use an NMOS transistor M1 operating in saturation region whereas the passive resistors R1, R2 act as load for the inverter circuit.

A CML gate works on the principle of current-steering. Assuming transistor pair (M2-M3) to be matched and operating in the saturation region, the drain current of transistor M2

(i_{D2}) and M3 (i_{D3}) can be expressed as a function of differential input voltage ($v_d = v_{in1}$-v_{in2}). The corresponding current equations can be written as

$$i_{D2} = \begin{cases} 0 & v_d < -\sqrt{\frac{2\,I_{SS}}{\mu_n C_{ox}\frac{W_N}{L_N}}}, \\ \frac{I_{SS}}{2} + \frac{v_d}{2}\sqrt{\mu_n C_{ox}\frac{W_N}{L_N}\,I_{SS} - \left(\mu_n C_{ox}\frac{W_N}{L_N}\frac{v_d}{2}\right)^2} & |v_d| \le \sqrt{\frac{2\,I_{SS}}{\mu_n C_{ox}\frac{W_N}{L_N}}}, \\ I_{SS} & v_d > \sqrt{\frac{2\,I_{SS}}{\mu_n C_{ox}\frac{W_N}{L_N}}}, \end{cases} \quad (2.1a)$$

$$i_{D3} = I_{SS} - i_{D2}, \quad (2.1b)$$

where I_{SS} is the constant bias current, C_{ox} is the oxide capacitance per unit area. The parameters μ_n, W_N and L_N are the electron mobility, the effective channel width and length of the NMOS transistors M2, M3 respectively.

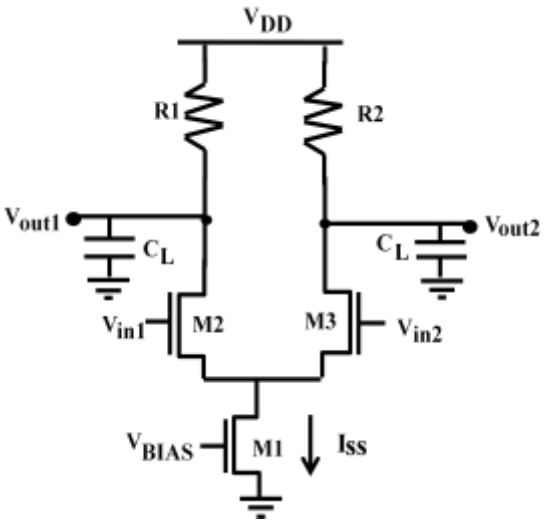


Fig. 2.1 CML inverter

It is clear from eqn. (2.1) that the bias current I_{SS} is completely steered to one of the two output branches for the differential input voltage exceeding the value

($\sqrt{2\,I_{SS}/(\mu_n C_{ox}\frac{W_N}{L_N})}$). The current steered in the inverter is converted into the differential output voltage ($v_{out} = v_{out1} - v_{out2}$), through the passive resistors R1 and R2. The passive resistors require large implementation area, therefore active loads are employed. A PMOS transistor operating in the linear region is commonly used. A CML inverter with PMOS transistors (M4, M5) as load is shown in Fig. 2.2.

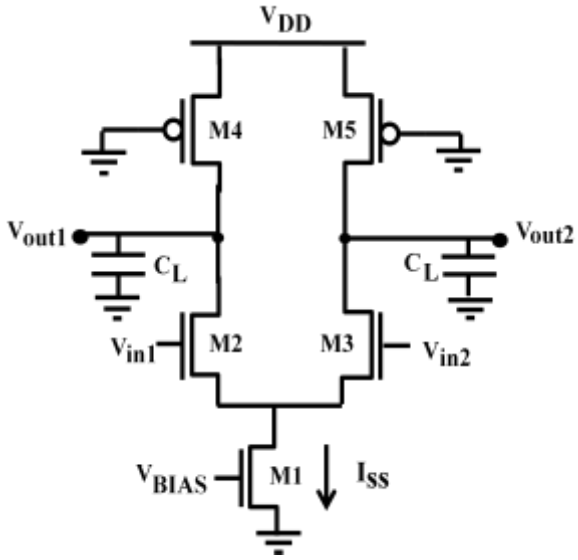


Fig. 2.2 CML inverter with PMOS load

The equivalent linear resistance of the load transistors M4, M5 using the standard BSIM3v3 MOSFET model [115] is computed as

$$R_P = \frac{R_{int}}{1-\frac{(R_{DSW}10^{-6})/W_P}{R_{int}}}, \tag{2.2}$$

where R_{DSW} is the empirical model parameter, W_P is the effective channel width of transistors M4, M5 and the parameter R_{int} is the intrinsic resistance of the transistors in the linear region and is given as

$$R_{int} = \left[\mu_{eff,p} C_{ox}\frac{W_P}{L_P}\left(V_{DD} - |V_{T,P}|\right)\right]^{-1}, \tag{2.3}$$

where the parameters $\mu_{eff,p}$, $V_{T,P}$ and L_P are the effective hole mobility, the threshold voltage, and the effective channel length of the transistors M4, M5 respectively.

It may be noted that the CML inverter (Fig. 2.2) processes a differential input (v_{in1}-v_{in2}) and provides a differential output voltage (v_{out1}-v_{out2}) and is referred to as differential CML inverter. The CML gates, in general, can be differential or single-ended and are investigated in this work. The analysis and design of both the differential and single-ended CML inverters are discussed in the following sections. A general framework for the basic logic gates is also included.

2.3 DIFFERENTIAL CML GATES

The differential CML gates use differential signaling. The schematic of a differential CML inverter is shown in Fig. 2.2. The differential input (v_d) and output (v_{out}) voltages are defined as

$$v_d = v_{in1} - v_{in2}, \tag{2.4a}$$

$$v_{out} = v_{out1} - v_{out2} = R_P(i_{D3} - i_{D2}). \tag{2.4b}$$

2.3.1 Operation of the differential CML inverter

In the differential CML inverter, the bias current I_{SS} flows through the transistor M2 for high value of the differential input v_d, and produces a low differential output voltage ($v_{out} = V_{OL} = -I_{SS} R_P$). Conversely, when the differential input v_d is low, the bias current I_{SS} gets steered to transistor M3 and produces a high differential output voltage ($v_{out} = V_{OH} = I_{SS} R_P$).

2.3.2 Analysis of the differential CML inverter

The analysis of the differential CML inverter based on the pencil-and-paper approach [69, 70] is described here. The behavior is modeled in terms of the static and delay parameters.

2.3.2.1 Static Model

The voltage transfer characteristic (VTC) of the differential CML inverter is plotted in Fig. 2.3 which can be modeled in terms of voltage swing, small-signal voltage gain and noise margin. The characteristic is symmetrical around zero value and hence the logic threshold voltage is specified as $V_{LT} = 0$. The high (V_{OH}) and low (V_{OL}) differential output voltages are

$$V_{OH} = I_{SS} R_P, \tag{2.5a}$$

$$V_{OL} = -I_{SS} R_P. \tag{2.5b}$$

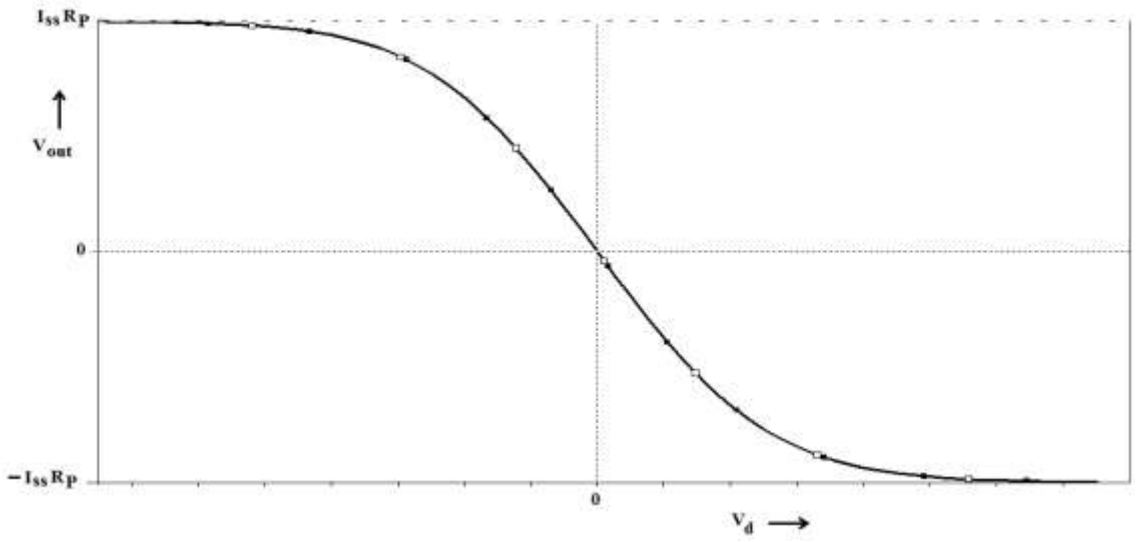


Fig. 2.3 Voltage transfer characteristic of a differential CML inverter

a. Voltage Swing: The voltage swing (V_{SWING}) is defined as the difference in the high and low output voltages. Using eqn. (2.5), V_{SWING} is given as

$$V_{SWING} = V_{OH} - V_{OL} = 2\, I_{SS} R_P. \tag{2.6}$$

b. Small-Signal Voltage Gain: The small-signal voltage gain (A_v) is evaluated around the logic threshold voltage for which the drain currents of transistors M2 and M3 are equal due to symmetry. Using the half circuit concept, A_v around the logic threshold voltage is computed as

$$A_v = g_{m,n} R_P = \frac{V_{SWING}}{2} \sqrt{\mu_{eff,n} C_{ox} \frac{W_N}{L_N} \frac{1}{I_{SS}}}, \tag{2.7}$$

where $g_{m,n}$ is defined as the transconductance and is substituted as $\sqrt{\mu_{eff,n} C_{ox} \frac{W_N}{L_N} I_{SS}}$.

c. Noise Margin: Due to the symmetry of the VTC, the noise margin (NM) for low and high signal value (NM_L and NM_H) are equal [27]. The NM is evaluated as

$$NM = \frac{V_{SWING}}{2}\left(1 - \frac{\sqrt{2}}{A_v}\right). \tag{2.8}$$

It may be noted in eqn. (2.8) that the noise margin is proportional to half the voltage swing, and approximately assumes this value for large values of A_v.

2.3.2.2 Delay Model

The propagation delay of the differential CML inverter is evaluated as the time it takes to charge or discharge the load capacitor C_L. The inverter circuit is linearized around the logic threshold and the half circuit concept is applied, since the circuit is symmetrical and differential input is applied. The equivalent linear half circuit is shown in Fig. 2.4. The

parasitic capacitances namely the drain-bulk junction capacitance (C_{dbi}) and the gate-to-drain capacitance (C_{gdi}) are considered for the (i^{th} = 2, 4) transistors.

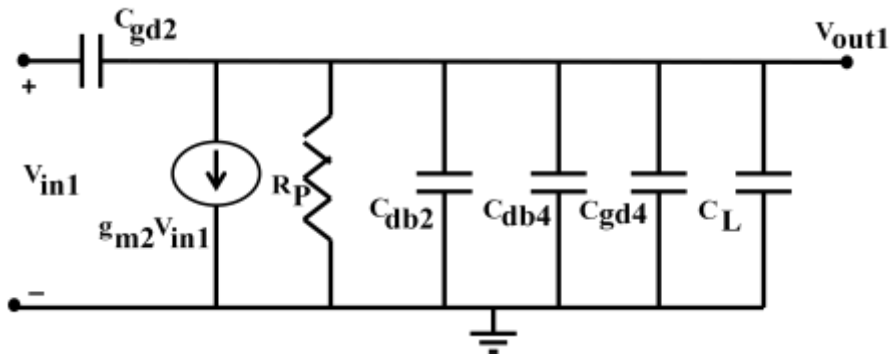


Fig. 2.4 Half circuit of a differential CML inverter

The network in Fig 2.4 is a first-order circuit therefore the open-circuit time constant method is used. For a unit step input waveform, the propagation delay t_{PD} of the inverter is expressed as

$$t_{PD} = 0.69\, R_P \left(C_{gd2} + C_{db2} + C_{db4} + C_{gd4} + C_L\right). \quad (2.9)$$

For the NMOS transistors operating in saturation region, C_{gd} is equal to the overlap capacitance $C_{gdo}W_n$ between the gate and the drain [70]. For the PMOS transistor operating in linear region, C_{gd} is evaluated as the sum of the overlap capacitance and the intrinsic contribution associated with its channel charge [70]. The junction capacitance C_{db} for the transistors are computed as explained in [70].

2.3.3 Design of the differential CML inverter

In this section, an approach to design a differential CML inverter for a given value of the bias current I_{SS} and the noise margin NM is presented [27].

For a specified value of NM, and A_v (>1.4 for differential CML gates [71]), the voltage swing is calculated using eqn. (2.8) as

$$V_{SWING} = \frac{2NM}{1-\frac{\sqrt{2}}{A_v}}. \tag{2.10}$$

The voltage swing obtained from eqn. (2.10) requires sizing of the load transistor with equivalent resistance $R_P \left(= \frac{V_{SWING}}{2I_{SS}}\right)$. To this end, the equivalent resistance, R_{P_MIN}, for the minimum sized PMOS transistor is first computed and then the bias current I_{HIGH} for the required voltage swing is determined as

$$I_{HIGH} = \frac{V_{SWING}}{2R_{P\_MIN}}. \tag{2.11}$$

If the bias current is higher than I_{HIGH}, then R_P should be less than R_{P_MIN} and this is achieved by setting L_P to its minimum value i.e. L_{MIN} and W_P which is calculated by solving eqns. (2.2) and (2.3) as

$$W_P = \frac{2I_{SS}}{V_{SWING}} \frac{L_{MIN}}{\mu_{eff,p}C_{ox}(V_{DD}-|V_{T,P}|)\left\{1-\frac{R_{DSW}10^{-6}}{L_{MIN}}\left[\mu_{eff,p}C_{ox}(V_{DD}-|V_{T,P}|)\right]\right\}}. \tag{2.12}$$

Similarly, if the bias current is lower than I_{HIGH}, then R_P should be greater than R_{P_MIN} and this is achieved by setting W_P to its minimum value i.e. W_{MIN} and L_P which is calculated by solving eqns. (2.2) and (2.3) as

$$L_P = W_{MIN}\,\mu_{eff,p}C_{ox}\left(V_{DD} - |V_{T,P}|\right)\left(\frac{V_{SWING}}{2I_{SS}} - \frac{R_{DSW}10^{-6}}{W_{MIN}}\right). \tag{2.13}$$

The A_v given in eqn. (2.7) is used to size transistors M2, M3. Assuming minimum channel length for the said transistors, the width (W_N) is computed as

$$W_N = \frac{4}{\mu_{eff,n} C_{ox}} \left(\frac{A_v}{V_{SWING}}\right)^2 I_{SS} L_{MIN}. \quad (2.14)$$

Sometimes the eqn. (2.14) results in a value of W_N smaller than the minimum channel width therefore, in such cases, W_N is also set to W_{MIN}. This happens when the bias current is lower than the current of the minimum sized NMOS transistor, I_{LOW} . Using eqn. (2.7), I_{LOW} is given as

$$I_{LOW} = \frac{1}{4} \frac{W_{MIN}}{L_{MIN}} \mu_{eff,n} C_{ox} \left(\frac{V_{SWING}}{A_v}\right)^2. \quad (2.15)$$

2.3.4 Realization of the basic gates

The series-gating approach is used to realize differential CML gates [27]. It is a systematic and a general approach wherein an arbitrary logic function F(Y1,….Yn) is implemented as an network of source-coupled transistor pairs having all transistor paths associated with the 2^n possible input combinations and then properly connecting each of the upper drain nodes to the output nodes.

The following rules are generally followed while realizing a logic function.

(i) The source-coupled transistor pairs are not allowed to share their source terminal with other transistor pair.

(ii) The current source must be connected to the source of only one transistor pair.

(iii) Each of the two drain node of the transistor pair is connected to the source of another transistor pair which is stacked to the first one.

By iterating this reasoning, a tree of stacked source-coupled transistor pair is obtained. A generalized two level differential CML gate is shown in Fig. 2.5. The drain terminals of the transistor pairs at the highest level can be connected to the appropriate output nodes according to the logic function. Based on the outlined concept, it is possible to realize basic

combinational gates such as exclusive-OR (XOR) gate, 2:1 multiplexer (MUX) etc. and sequential circuits such as D latch. The corresponding realizations are depicted in Fig. 2.6.

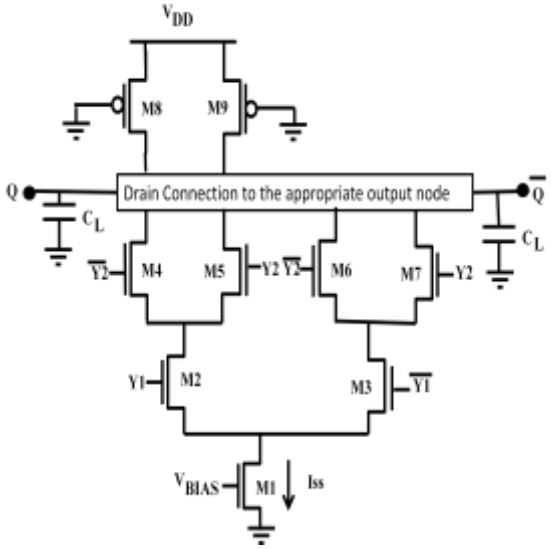
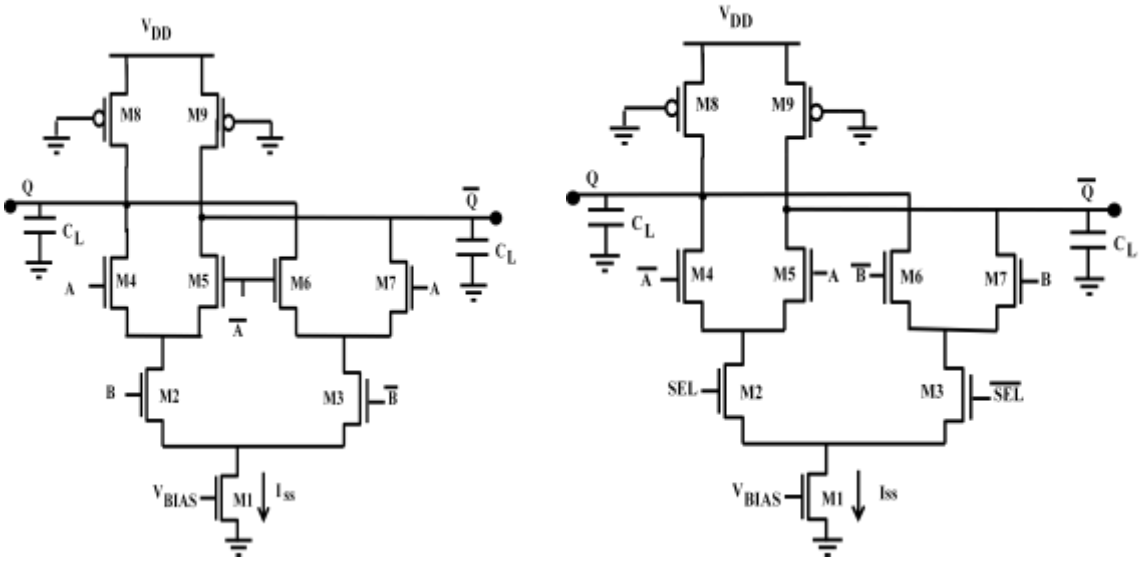
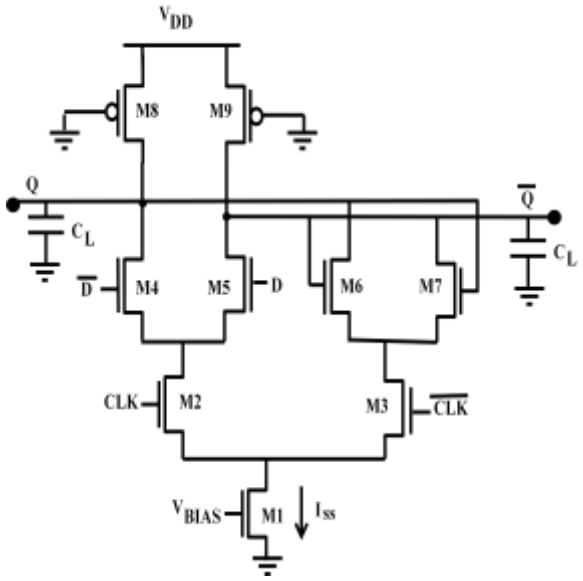


Fig. 2.5 A generalized two level differential CML gate



(a) (b)



(c)

Fig. 2.6 Differential CML gates a) XOR gate b) 2:1 MUX c) D latch

2.4 SINGLE-ENDED CML GATES

The single-ended CML gates use single-ended signalling. The schematic of a single-ended CML inverter [34] is shown in Fig. 2.7. The input (v_{in}) is applied to the gate of only one transistor of the source-coupled pair (say M2) while the gate of the other transistor M3 is connected to a voltage reference source V_{REF} . The circuit provides a single-ended output (v_{out}).

An improved form of single-ended CML style named as positive-feedback source-coupled logic (PFSCL) style is suggested in literature [34]. The circuit of a PFSCL inverter is shown in Fig. 2.8. This logic style uses a positive feedback to replace the reference voltage source of single-ended CML inverter (Fig. 2.7) and is therefore chosen as a representative of single-ended CML gates in this work. The input transistor M2 is source-coupled with a feedback transistor M3 whose gate is connected to the output node. The constant current

source M1 provides the bias current I_{SS} while the PMOS load transistor M4 performs the current to voltage conversion.

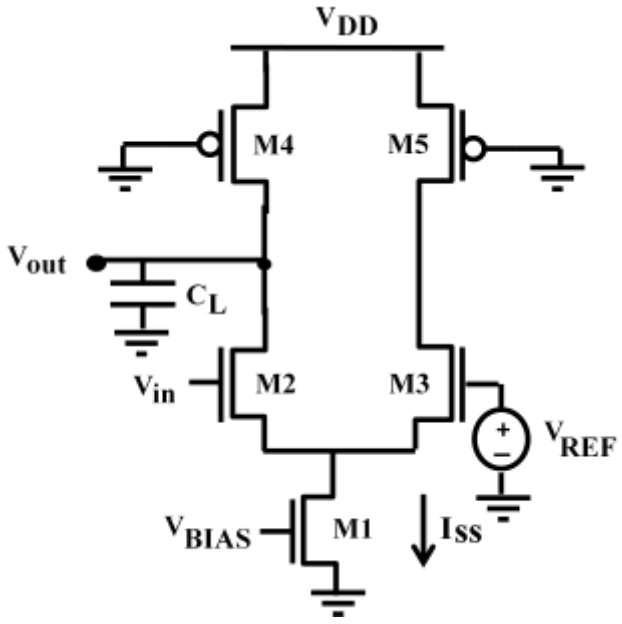


Fig. 2.7 Single-ended CML inverter

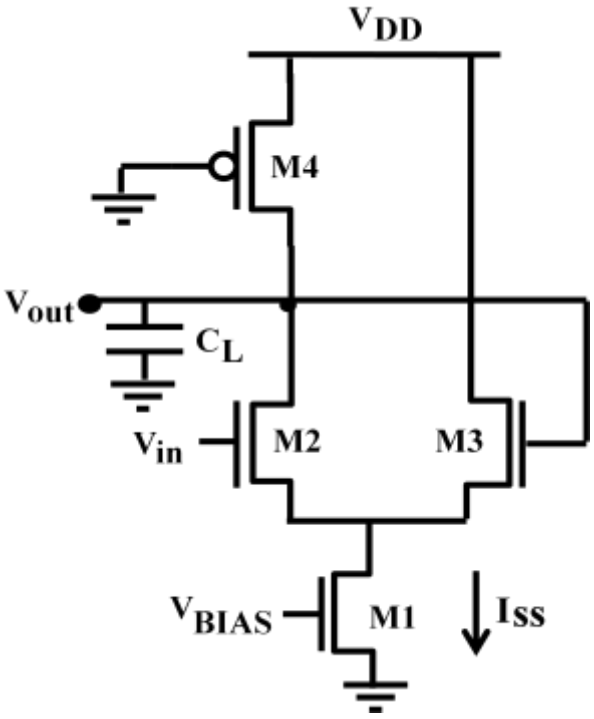


Fig. 2.8 PFSCL inverter

2.4.1 Operation of the PFSCL inverter

For the high value of the input v_{in}, the bias current I_{SS} is steered through transistor M2 and a low voltage ($V_{OL} = V_{DD} – R_P I_{SS}$) is obtained at the output [34]. Similarly, the transistor M2 is turned OFF for low value of input v_{in}, and a high voltage ($V_{OH} = V_{DD}$) is obtained at the output.

2.4.2 Analysis of the PFSCL inverter

The analysis of the PFSCL inverter based on the pencil-and-paper approach is described here [37]. The behavior is modeled in terms of static and delay parameters.

2.4.2.1 Static Model

The static parameters such as voltage swing, small-signal voltage gain and the noise margin are used to model the PFSCL inverter. The voltage transfer characteristics of the PFSCL inverter is plotted in Fig. 2.9 and is found to be symmetrical around the logic threshold voltage $V_{LT} = V_{DD} - R_P I_{SS}/2$. The high (V_{OH}) and low (V_{OL}) output voltages are

$$V_{OH} = V_{DD}, \tag{2.16a}$$

$$V_{OL} = V_{DD} - I_{SS} R_P. \tag{2.16b}$$

a. Voltage Swing: The voltage swing (V_{SWING}) is computed as the difference between the high and low output voltages and is given as

$$V_{SWING} = V_{OH} - V_{OL} = I_{SS} R_P. \tag{2.17}$$

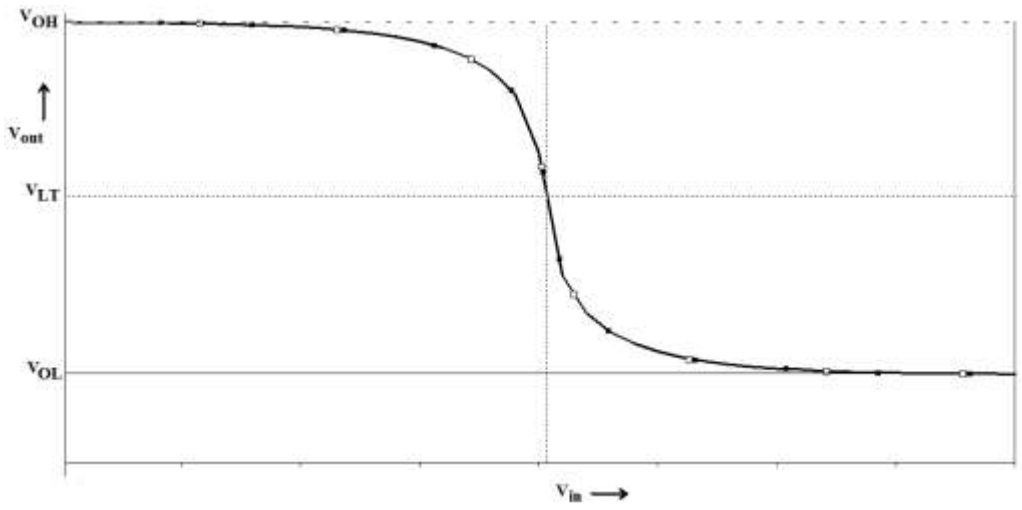


Fig. 2.9 Voltage transfer characteristic of a PFSCL inverter

b. Small-Signal Voltage Gain: The small-signal voltage gain (A_v) is evaluated around the logic threshold voltage. By applying the superposition of the input voltages at the gate of the transistors M2 and M3, the value of A_v around the logic threshold voltage is computed as

$$A_v = \frac{g_{m,n} R_P/2}{1-g_{m,n} R_P/2}, \tag{2.18}$$

where $g_{m,n}$ is the transconductance of the NMOS transistor computed around the logic threshold as $\sqrt{\mu_{eff,n} C_{ox} \frac{W_N}{L_N} I_{SS}}$.

c. Noise Margin: The noise margin (NM) of a PFSCL inverter [37] is evaluated as

$$NM = \frac{V_{SWING}}{2} f\left(g_{m,n} R_P/2\right), \tag{2.19a}$$

where function f is expressed as

$$f(x) = 2\sqrt{\frac{1}{2}(1-1/16x^2)\left(1-\sqrt{1-\frac{1-1/4x^2}{(1-1/16x^2)^2}}\right)}.\left[2\sqrt{1-\frac{1}{2}(1-1/16x^2)\left(1-\sqrt{1-\frac{1-1/4x^2}{(1-1/16x^2)^2}}\right)}-\frac{1}{x}\right].$$

(2.19b)

The function f(x) represented in eqn. (2.19b) can be approximated by the expression

$$f(x) = 1.4\,x - 0.65. \quad (2.19c)$$

The above relation is valid for $x = g_{m,n} R_P/2 < 1$ whereas it exhibits hysteresis for values greater than 1. Alternatively, by using the piecewise-linear approximation of the VTC [34], the NM can also be computed as

$$NM = \frac{V_{SWING}}{2}\left(1-\frac{1}{A_v}\right). \quad (2.19d)$$

2.4.2.2 Delay Model

The delay of a PFSCL inverter can be analytically evaluated by linearizing the circuit around the logic threshold. The presence of feedback, however, makes the analysis complex so an alternate approach [37] is followed. According to the approach, when the input voltage switches abruptly from low logic level to the high logic level, the propagation delay t_{PD} is evaluated as

$$t_{PD} = R_P C_{out} = R_P \left(C_{db2} + C_{gd2} + C_{db,4} + C_{gd,4} + C_{gd,3} + \frac{1}{2} C_{gs,3} + C_L\right). \quad (2.20)$$

The overall capacitance C_{out} at the output node is determined by considering the capacitive effects associated with the transistors and the external load capacitance C_L. The capacitive effects for the NMOS and the PMOS transistor consist of the drain-bulk junction capacitance (C_{db}), the gate-to-source capacitance (C_{gs}) and the gate-to-drain capacitance (C_{gd}). For the NMOS transistors operating in saturation region, C_{gd} is equal to the overlap capacitance

$C_{gdo}W_n$ between the gate and the drain [37]. For the PMOS transistor operating in linear region, C_{gd} is evaluated as the sum of the overlap capacitance and the intrinsic contribution associated with its channel charge [37]. The junction capacitance C_{db} for the transistors are computed as explained in [37]. The capacitance C_{gs} is multiplied with ½ due to the miller effect associated with the gain from the gate-to-source of transistor M3 [37].

2.4.3 Design of the PFSCL inverter

In this section, the design approach of a PFSCL inverter for a given value of the bias current I_{SS} and the noise margin is presented [37].

For a specified value of NM, and by assuming $g_{m,n}\,R_P/2 = 1$, the value of voltage swing for which the NMOS transistors in the PDN remain in saturation is calculated using eqn. (2.19) as

$$V_{SWING} = \frac{2NM}{f(1)} = 2.7\ NM. \tag{2.21}$$

The voltage swing obtained from eqn. (2.21) requires sizing of the load transistor with equivalent resistance R_P $\left(=\frac{V_{SWING}}{I_{SS}}\right)$. To this end, the equivalent resistance, R_{P_MIN}, for the minimum sized PMOS transistor is first determined and then the bias current I_{HIGH} for the required voltage swing is determined as

$$I_{HIGH} = \frac{V_{SWING}}{R_{P\_MIN}}. \tag{2.22}$$

If the bias current is higher than I_{HIGH} , then R_P should be less than R_{P_MIN} and this is achieved by setting L_P to its minimum value i.e. L_{MIN} and W_P which is calculated by solving eqns. (2.2) and (2.3) as

$$W_P = \frac{I_{SS}}{V_{SWING}} \frac{L_{MIN}}{\mu_{eff,p} C_{ox}(V_{DD} - |V_{T,P}|)\left\{1 - \frac{R_{DSW}10^{-6}}{L_{MIN}}\left[\mu_{eff,p} C_{ox}(V_{DD} - |V_{T,P}|)\right]\right\}}. \quad (2.23)$$

Similarly, if the bias current is lower than I_{HIGH}, then R_P should be greater than R_{P_MIN} and this is achieved by setting W_P to its minimum value i.e. W_{MIN} and L_P which is calculated by solving eqns. (2.2) and (2.3) as

$$L_P = W_{MIN}\, \mu_{eff,p} C_{ox}(V_{DD} - |V_{T,P}|) \left(\frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW}10^{-6}}{W_{MIN}}\right). \quad (2.24)$$

The size of the transistors M2, M3 can be computed by expressing $g_{m,n} R_P/2$ in terms of the bias current and voltage swing. By using eqn. (2.17), the term $g_{m,n} R_P/2$ can be expressed as

$$\frac{g_{m,n} R_P}{2} = \frac{V_{SWING}}{2} \sqrt{\mu_{eff,n} C_{ox} \frac{W_N}{L_N} \frac{1}{I_{SS}}}. \quad (2.25)$$

Solving the above equation, with the minimum channel length, the width of the said transistors can be computed as

$$W_N = \frac{4}{\mu_{eff,n} C_{ox}} \frac{I_{SS} L_{MIN}}{V_{SWING}^2}. \quad (2.26)$$

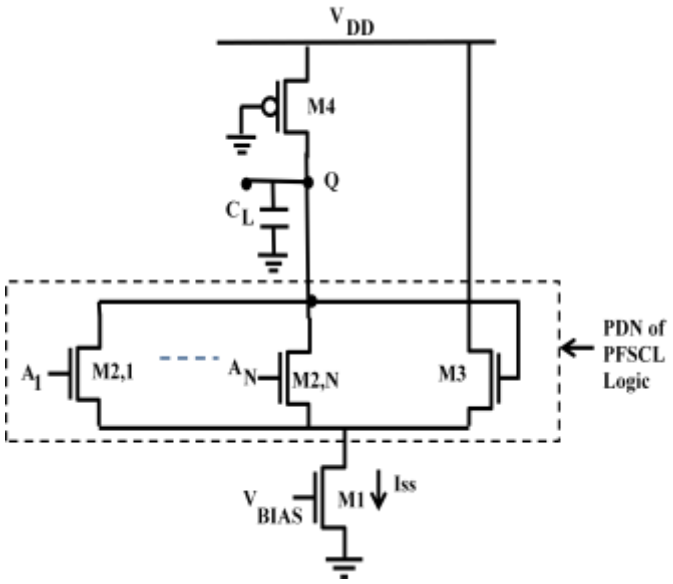
Sometimes the eqn. (2.26) results in a value of W_N smaller than the minimum channel width therefore, in such cases, W_N is also set to W_{MIN}. This happens when the bias current is lower than the current of the minimum sized NMOS transistor, I_{LOW} .Using eqn. (2.26), I_{LOW} is given as

$$I_{LOW} = \frac{1}{4} \frac{W_{MIN}}{L_{MIN}} \mu_{eff,n} C_{ox} V_{SWING}^2. \quad (2.27)$$

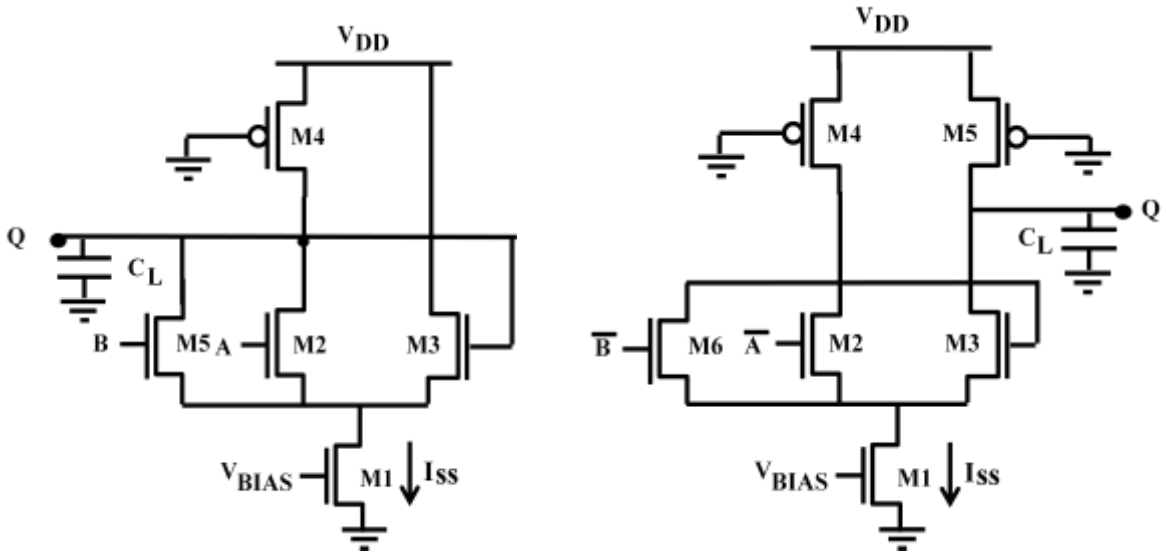
2.4.4 Realization of the basic gates

A generic N-input PFSCL gate (Fig. 2.10a) realizes a N-input NOR function by connecting NMOS transistors in parallel to each other and finally inverting the input. It is suggested that the same topology can be used for N-input NAND gate with help of De Morgan law [34]. The inputs need to be applied in the inverted form, and the output is taken from the other branch. Therefore, PFSCL gates using NAND based realization use cascading of stages instead of the stacking of transistor pairs employed in differential CML gates.

The PFSCL realizations of 2-input NOR gate, 2-input NAND gate are shown in Figs. 2.10b, c. The PFSCL based realization of the XOR gate is shown in Fig. 2.11. It consist of five identical 2-input PFSCL NOR gates that are arranged in three levels. The first level is responsible for generating the complement of the applied inputs whereas the subsequent two levels implement the XOR functionality. Other combinational gates can also be realized in the similar manner.



(a)



(b) (c)

Fig. 2.10 a) A generic PFSCL gate b) 2-input NOR gate c) 2-input NAND gate

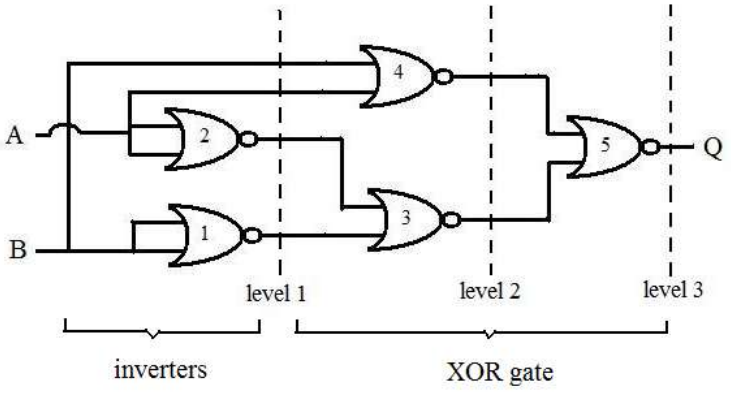


Fig. 2.11 A PFSCL based XOR gate implementation

2.5 CONCLUDING REMARKS

In this chapter, the basic concepts related to the CML gates are presented. The operating principles of the differential and single-ended CML gates are discussed. An improved version of the single-ended CML gate named as positive-feedback source-coupled logic (PFSCL) gate is presented and is worked upon. The behavior modeling of the

differential CML and PFSCL gates based on the pencil-and-paper approach is described. A systematic procedure to design CML gates using BSIM3v3 model parameters is also elaborated. The approach to realize logic function in differential CML as well as in PFSCL styles is discussed and the realization of few common digital logic gates is drawn.

3.1 INTRODUCTION

The logic function realization in differential CML gates is based on series-gating approach that infers a multilevel structure of source-coupled transistor pairs in the PDN. The number of levels decides the minimum supply voltage for the gate. In this chapter, a new approach to realize the logic function in differential CML gates is presented. The PDN is modified to reduce the number of source-coupled transistor pair levels. The triple-tail cell concept, originally suggested using bipolar junction transistor is extended to the differential CML gates. The proposed approach is applied to the combinational and the sequential CML gates and their behavior in terms of static and delay parameters is examined. A design procedure is formulated and is followed by the performance comparison of the proposed topologies with their existing counterparts for different design cases such as high speed, power efficient and low power.

3.2 LITERATURE SURVEY

The PDN of the differential CML gate realizes the functionality and consists of source-coupled transistor pairs arranged in accordance with the series-gating approach [27]. In literature, the PDN is modified to improve speed [28, 29, 34-40] and reduce power consumption [30-33]. The first method [28, 29] employs feedback transistors in the PDN to eliminate the effect of threshold voltage fluctuations during fabrication and results in speed improvement. Analytical formulations are presented and the concept is verified through IC implementation of a multiplexer and a demultiplexer for optical-fiber link. The second method [30, 31] aims at reducing the power consumption by lowering the minimum power supply required by the gate. It uses transistors with different threshold voltage for each level

of source-coupled transistor pairs in the PDN. The gates based on this methodology are named as Multi-Threshold CMOS (MTCMOS) MOS current mode logic gates. An entirely different approach to reduce power consumption is proposed in [32, 33]. It introduces an extra invalid level in addition to the high and low logic levels of a conventional CML gate and is called as Triple-rail MOS current mode logic (Tr-MCML) style. This style is beneficial for pipeline operations and also supports power-on-demand operations in pipeline architectures.

Of all the available PDN modifications, the MTCMOS MCML gates and the Tr-MCML gates are reported to reduce power consumption. The first one use multiple threshold voltage transistors in the PDN to lower the minimum power supply value. But from the IC fabrication viewpoint, this adds additional fabrication steps leading to an increase in the fabrication cost. The second approach introduces an extra logic level. In this chapter, a new approach to reduce the power supply value for differential CML gate is presented. The approach reduces the number of source-coupled transistor pair levels in comparison to the conventional ones by using triple-tail cell concept. The proposed approach therefore avoids the use of multiple threshold voltage transistors in the PDN and does not require any extra logic level. The realization of differential CML style based on the proposed approach is presented and investigated in the next section**.**

3.3 PROPOSED APPROACH

A differential CML gate is a multi-level topology of stacked source-coupled transistor pairs. Conventionally, the series-gating approach is followed for realizing the logic function. The approach has already been discussed in detail in section 2.3.4. For the differential CML

gate, the minimum power supply voltage, $V_{DD\_MIN\_TR}$ is defined as the voltage at which all the transistors in the PDN operates in the saturation region [31]. Thus, the number of transistor pair levels determines the minimum power supply value of the gate. To illustrate this, a generalized structure of a two level CML gate (Fig. 2.5) is considered and is redrawn here. The value of $V_{DD\_MIN\_TR}$ is computed as

$$V_{DD\_MIN\_TR} = V_{DSAT,1} + V_{DSAT,2} + V_{GS,4}\,, \tag{3.1}$$

where $V_{DSAT,1}$, $V_{DSAT,2}$, represent the drain-to-source saturation voltage of the transistors M1, M2, and $V_{GS,4}$ is the gate-to-source voltage of M4. In general, the drain-to-source saturation voltage is expressed as

$$V_{DSAT} = V_{GS} - V_T\,, \tag{3.2}$$

where V_T is the threshold voltage of the transistor.

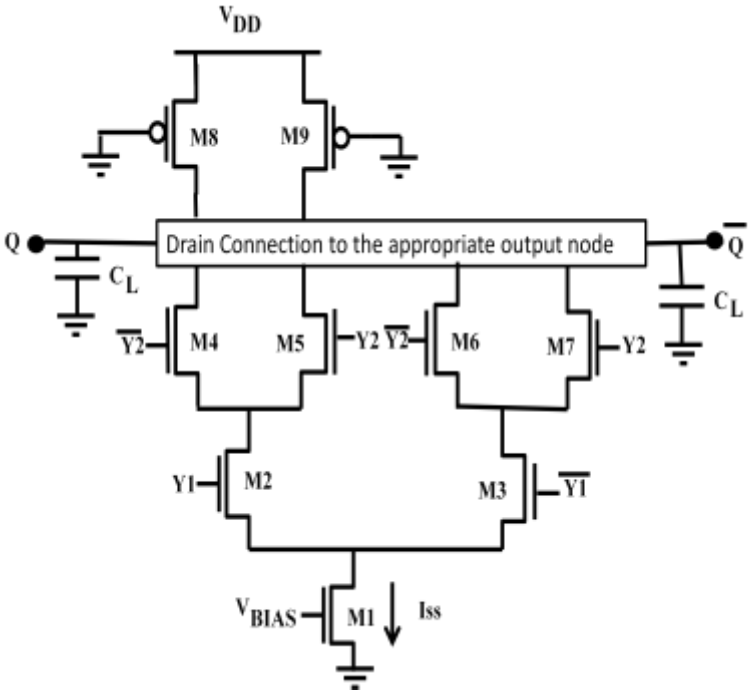


Fig. A generalized two level differential CML gate

Further, the gate-source voltage, V_{GS} in saturation region is expressed as

$$V_{GS} = \sqrt{\frac{I_D}{k}} - V_T , \quad (3.3)$$

where I_D and k is the drain current and the device transconductance of the transistor respectively.

Using eqns. (3.2) and (3.3), the minimum power supply voltage, $V_{DD\_MIN\_TR}$ is calculated as

$$V_{DD\_MIN\_TR} = 3V_{BIAS} - 3V_{T\_TR1} + V_{T\_TR}, \quad (3.4)$$

where V_{T_TR} is the threshold voltage of the transistors M4-M7, V_{T_TR1}, V_{BIAS} are the threshold and the bias voltages of the transistor M1 respectively. For 0.18 µm TSMC CMOS technology, with V_{T_TR}= V_{T_TR1}= 500 mV, and if $V_{BIAS} = 800$ mV, the minimum supply voltage, $V_{DD\_MIN\_TR}$ for a two level CML gate is calculated as 1.4 V.

The proposed approach introduces triple-tail cell concept [116-118] in logic function realization. A triple-tail cell drawn in Fig. 3.1 has three source-coupled transistors (M2, M3, M4). The flow of bias current I_{SS} in the transistor pair (M3-M4) is controlled by the third transistor M2. The transistor pair (M3-M4) draw bias current I_{SS} only when the transistor M2 is OFF otherwise the transistor M2 draws the entire bias current.

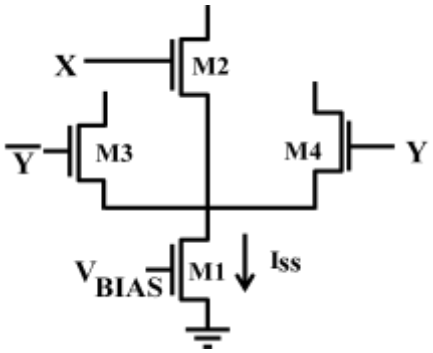


Fig. 3.1 A triple-tail cell

A generalized structure of a two level differential CML gate based on the proposed approach is shown in Fig. 3.2. It uses two triple-tail cells (M3, M4, M7) and (M5, M6, M8)

biased by separate current sources of $I_{SS}/2$ value. The value of the minimum power supply voltage $V_{DD\_MIN\_LV}$ can be computed by using the method followed for conventional CML gates and is computed as

$$V_{DD\_MIN\_LV} = 2V_{BIAS} - 2V_{T\_LV1} + V_{T\_LV}\,, \tag{3.5}$$

where V_{T_LV} is the threshold voltage of transistors M3-M6, V_{T_LV1}, V_{BIAS} are the threshold and the bias voltages of transistor M1. For 0.18 µm TSMC CMOS technology, with $V_{T\_LV} = V_{T\_LV1} = 500$ mV, and if $V_{BIAS} = 800$ mV, the minimum power supply voltage, $V_{DD\_MIN\_LV}$ for the proposed two level CML gate is calculated as 1.1 V.

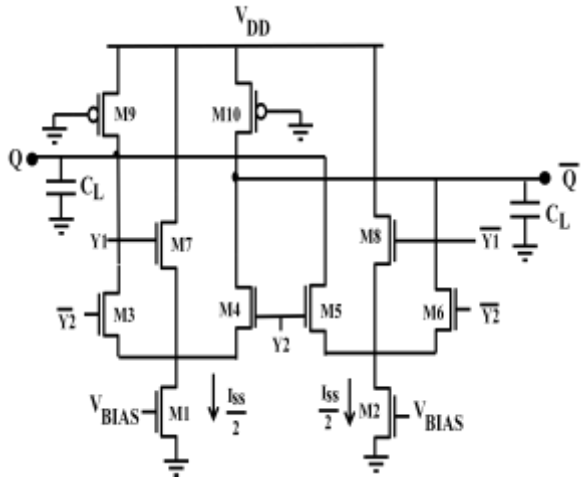


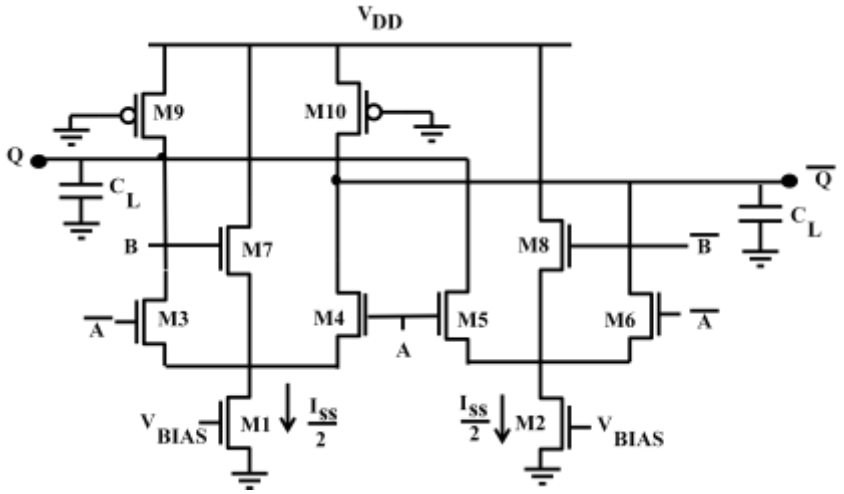
Fig. 3.2 A generalized two level differential CML gate based on the proposed approach

It may be noted from eqns. (3.4) and (3.5) that the minimum power supply voltage is reduced in the proposed approach. The combinational and sequential circuits are developed using the proposed approach and their behavior is examined, analyzed and modeled in the following subsections.

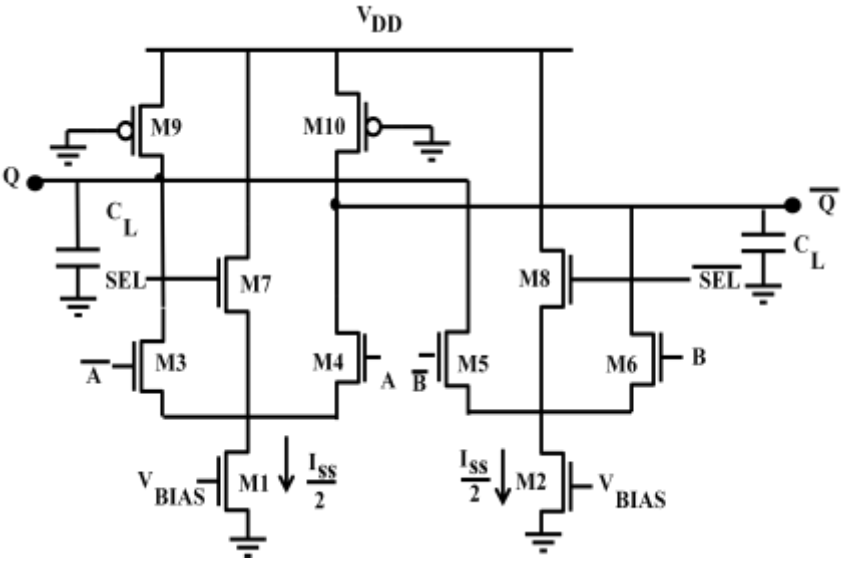
3.4 PROPOSED COMBINATIONAL GATES WITH MODIFIED PDN

The realization of the combinational gates such as an exclusive-OR (XOR) gate, 2:1 multiplexer (MUX) based on the proposed approach is shown in Fig. 3.3. It may be noted

that the topologies of MUX and XOR gate are similar but differs in the manner the inputs are connected to the transistor pairs. Therefore, the XOR gate with differential inputs A and B (Fig. 3.3a) is examined. It consists of two triple-tail cells (M3, M4, M7) and (M5, M6, M8) biased by separate current sources of $I_{SS}/2$ value. The transistors M7 and M8 are driven by the differential input B and are connected between the power supply terminal and the common source terminal of transistor pairs (M3–M4) and (M5 –M6) respectively.



(a)



(b)

Fig. 3.3 Proposed combinational gates a) XOR gate b) 2:1 MUX

3.4.1 Operation of the proposed XOR gate

A high voltage on differential input B turns ON the transistor M7, and deactivates the transistor pair (M3–M4). At the same time, the transistor M8 turns OFF so that the transistor pair (M5–M6) generates the output according to the differential input A. Similarly, the transistor pair (M3-M4) gets activated for low voltage of differential input B and produces the corresponding output.

3.4.2 Analysis of the proposed XOR gate

The behavior of the proposed XOR gate is analyzed in terms of the static and the delay parameters using pencil-and-paper approach. The analysis is simplified by modeling the load transistors M9, M10 with an equivalent linear resistance, R_P expressed in eqn. (2.2).

3.4.2.1 Static Model

The static behavior is modeled in terms of the voltage swing, the small-signal voltage gain and the noise margin. A careful examination of the proposed circuit shows that if equal aspect ratio of all the transistors in the triple-tail cells is considered, then the transistors M7 and M8 will not be able to completely switch OFF the transistor pair (M3–M4) and (M5–M6). To illustrate this behavior, the value of differential input A is chosen such that the transistors M3, M6 are ON while the transistors M4, M5 are OFF. Then, a high differential B voltage turns ON the transistor M7. In this condition the transistors M3 and M7 draws the equal currents as their gate-source voltages are same. Hence the transistor M7 is not able to completely deactivate the transistor pair (M3–M4). Therefore to achieve proper operation, the aspect ratio of transistors M7, M8 is made greater than other transistors' aspect ratio by a

factor N. Thus, for the above case the currents flowing through the transistors M3 and M7 can be written as

$$i_{D,3} = \frac{I_{SS}}{2}\frac{1}{1+N}, \quad (3.6a)$$

$$i_{D,7} = \frac{I_{SS}}{2}\frac{N}{1+N}. \quad (3.6b)$$

The current through M3 can be minimized by increasing factor N. This input condition produces V_{OH} as

$$V_{OH} = V_Q - \overline{V_Q} = R_P\left[\left(i_{D,4} + i_{D,6}\right) - \left(i_{D,3} + i_{D,5}\right)\right] = \frac{R_P I_{SS}}{2}\left(\frac{N}{1+N}\right), \quad (3.7)$$

where $i_{D,3}, i_{D,4}, i_{D,5}, i_{D,6}$ are the currents through transistors M3, M4, M5, and M6 respectively. The differential output voltages for various input combinations are enlisted in Table 3.1.

Table 3.1 Differential output voltages of the proposed XOR gate for various input combinations

Differential inputs		**Currents through the transistors**						**Differential output ($V_Q - \overline{V_Q}$)**	
A	**B**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**	**Level**	$R_P\left[\left(i_{D,4} + i_{D,6}\right) - \left(i_{D,3} + i_{D,5}\right)\right]$
L	L	I_1	0	0	I_3	0	I_2	V_{OL}	$-R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$
L	H	I_3	0	0	I_1	I_2	0	V_{OH}	$R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$
H	L	0	I_1	I_3	0	0	I_2	V_{OH}	$R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$
H	H	0	I_3	I_1	0	I_2	0	V_{OL}	$-R_P\frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$

where L/H= low/high differential input voltage, $I_1 = \frac{I_{SS}}{2}$, $I_2 = \frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$ and $I_3 = \frac{I_{SS}}{2}\left(\frac{1}{1+N}\right)$

Hence, from Table 3.1, the voltage swing of the circuit can be expressed as

$$V_{SWING} = V_{OH} - V_{OL} = R_P I_{SS}\left(\frac{N}{1+N}\right). \quad (3.8)$$

The small-signal voltage gain (A_v) and noise margin (NM) for the proposed XOR gate are computed by the method outlined in section 2.3.2 as

$$A_v = g_{m,n}R_P = \frac{1+N}{N}\frac{V_{SWING}}{2}\sqrt{2\mu_{eff,n}C_{OX}\frac{W_N}{L_N}\frac{1}{I_{SS}}}, \quad (3.9)$$

$$NM = \frac{V_{SWING}}{2}\left[1-\frac{\sqrt{2}}{A_v}\right], \quad (3.10)$$

where $\mu_{eff,n}$, $g_{m,n}$, W_N and L_N are the effective electron mobility, the transconductance, the effective channel width and length of transistors M3-M6 respectively.

3.4.2.2 Delay Model

In this subsection, the delay expression for the proposed XOR gate is formulated. For a high-to-low transition on the differential input B, the output switch by activating (deactivating) the transistor pair M3–M4 (M5–M6), the circuit reduces to a simple differential CML inverter. The equivalent linear half circuit is shown in Fig. 3.4 where C_{gdi} , C_{dbi} represents the gate-drain capacitance and the drain-bulk junction capacitance of the i^{th} (i= 3, 5, 9) transistor as discussed in section 2.3.2.2.

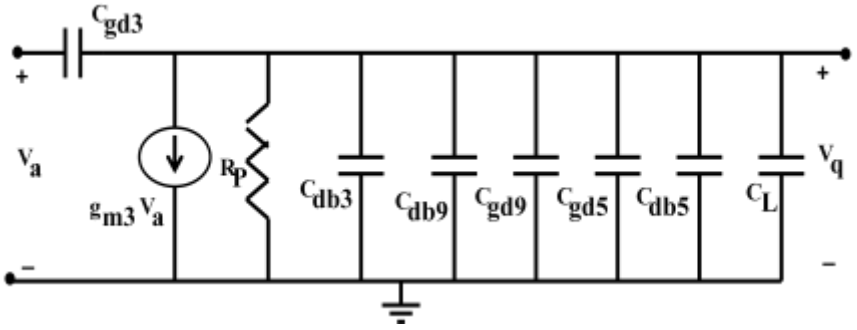


Fig. 3.4 Linear half-circuit (with low value of differential input A)

The delay of the proposed XOR gate can be expressed as

$$t_{PD} = 0.69\, R_P\left(C_{db3} + C_{gd3} + C_{gd9} + C_{db9} + C_{db5} + C_{gd5} + C_L\right), \quad (3.11)$$

with $C_{db3} = C_{db5}$, $C_{gd3} = C_{gd5}$ and, $R_P = \frac{1+N}{N}\frac{V_{SWING}}{I_{SS}}$, eqn. (3.11) can be rewritten as

$$t_{PD} = 0.69\ \frac{1+N}{N}\frac{V_{SWING}}{I_{SS}}\left(2C_{db3} + 2C_{gd3} + C_{gd9} + C_{db9} + C_L\right), \quad (3.12)$$

It can be observed that the delay given in eqn. (3.12) is expressed in terms of the transistors' capacitances, which in turn depend on their aspect ratio. In practical situations, the transistor aspect ratio must be set to meet the design specifications on noise margin, power and delay. Therefore, the dependence of the delay on the aspect ratio should also be determined. To this end, a design procedure to size the transistors is worked out and the delay model is revisited again for the purpose.

3.4.3 Design of the proposed XOR gate

An approach to size the transistors in the proposed XOR gate on the basis of static model is developed. For a specified value of NM, factor N and A_v ($\geq$1.4 for CML [71]), the voltage swing of the proposed XOR gate is calculated using eqn. (3.10) as

$$V_{SWING} = \frac{2NM}{1-\frac{\sqrt{2}}{A_v}}, \quad (3.13)$$

It may be noted that V_{SWING} should be lower than the maximum value of $2V_T$ so as to ensure that transistors M3-M6 operates in saturation region. The voltage swing obtained from eqn. (3.13) requires sizing of the load transistor with equivalent resistance $R_P\left(=\frac{1+N}{N}\frac{V_{SWING}}{I_{SS}}\right)$. To this end, the equivalent resistance, R_{P_MIN}, for the minimum sized PMOS transistor is first determined and then the bias current I_{HIGH} for the required voltage swing is determined as

$$I_{HIGH} = \frac{V_{SWING}}{R_{P\_MIN}}. \quad (3.14)$$

If the bias current is higher than I_{HIGH} , then R_P should be less than R_{P_MIN} and this is achieved by setting L_P to its minimum value i.e. L_{MIN} and W_P which is calculated by solving eqns. (2.2) and (2.3) as

$$W_P = \frac{N}{1+N}\frac{I_{SS}}{V_{SWING}}\frac{L_{MIN}}{\mu_{eff,p}C_{ox}(V_{DD}-|V_{T,P}|)\left\{1-\frac{R_{DSW}10^{-6}}{L_{MIN}}[\mu_{eff,p}C_{ox}(V_{DD}-|V_{T,P}|)]\right\}}. \quad (3.15)$$

Similarly, if the bias current is lower than I_{HIGH}, then R_P should be greater than R_{P_MIN} and this is achieved by setting W_P to its minimum value i.e. W_{MIN} and L_P which is calculated by solving eqns. (2.2) and (2.3) as

$$L_P = W_{MIN}\,\mu_{eff,p}C_{ox}\left(V_{DD} - |V_{T,P}|\right)\left(\frac{1+N}{N}\frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW}10^{-6}}{W_{MIN}}\right). \quad (3.16)$$

The small-signal voltage gain (A_v) given in eqn. (3.9) is used to size transistors M3-M6. Assuming minimum channel length for the said transistors, the width is computed as

$$W_N = \frac{2}{\mu_{eff,n}C_{ox}}\left(\frac{N}{1+N}\right)^2\left(\frac{A_v}{V_{SWING}}\right)^2 I_{SS}\,L_{MIN}. \quad (3.17)$$

Sometimes the eqn. (3.17) results in a value of W_N smaller than the minimum channel width. Therefore, in such cases, W_N is also set to W_{MIN}. This happens when the bias current is lower than the current of the minimum sized NMOS transistor, I_{LOW}. Using eqn. (3.9), I_{LOW} can be computed as

$$I_{LOW} = \frac{1}{2}\left(\frac{1+N}{N}\right)^2\frac{W_{MIN}}{L_{MIN}}\,\mu_{eff,n}C_{ox}\left(\frac{V_{SWING}}{A_v}\right)^2. \quad (3.18)$$

For proper switching, the width of the transistors M7, M8 is made N times the width of the transistors M3-M6.

The design eqns. (3.13)–(3.18) can be used to express the parasitic capacitances in the delay in terms of the bias current and the voltage swing as

$$C_{xy} = \frac{a_{xy}}{(V_{SWING})^2}I_{SS} + b_{xy}\frac{V_{SWING}}{I_{SS}} + c_{xy}, \quad (3.19)$$

where C_{xy} is the capacitance between the terminals x and y and a_{xy}, b_{xy}, c_{xy} are the associated coefficients. Using eqns. (3.16) and (3.17), various capacitances in eqn. (3.12) for I_{SS} ranging from I_{LOW} to I_{HIGH} may be expressed as

$$C_{gd3} = C_{gdo}W_3 = 2A_v^2 C_{gdo}\left(\frac{N}{1+N}\right)^2 \frac{L_{MIN}}{\mu_{eff,n}C_{OX}} \frac{I_{SS}}{(V_{SWING})^2}, \tag{3.20}$$

where C_{gdo} is the drain-gate overlap capacitance per unit transistor width.

$$C_{db3} = W_3\left(K_{jn}C_{jn}L_{dn} + 2K_{jswn}C_{jswn}\right) + 2K_{jswn}C_{jswn}L_{dn}, \tag{3.21}$$

$$= 2A_v^2 \frac{L_{MIN}}{\mu_{eff,n}C_{OX}}\left(\frac{N}{1+N}\right)^2\left(K_{jn}C_{jn}L_{dn} + 2K_{jswn}C_{jswn}\right)\frac{I_{SS}}{(V_{SWING})^2} + 2K_{jswn}C_{jswn}L_{dn}, \tag{3.22}$$

where C_{jn}, C_{jswn} are the zero-bias junction capacitance per unit area and zero-bias sidewall capacitance per unit parameter respectively. The coefficients K_{jn}, K_{jswn} are the voltage equivalence factor for the junction and the sidewall capacitances [27].

$$C_{gd9} = C_{gdo}W_{MIN} + \frac{3}{4}A_{bulk,max}W_{MIN}L_P C_{ox}, \tag{3.23}$$

$$= C_{gdo}W_{MIN} + \frac{3}{4}A_{bulk,max}W_{MIN}C_{ox}\left\{\mu_{eff,p}C_{ox}W_{MIN}\left(V_{DD} - |V_{T,P}|\right)\left[\frac{1+N}{N}\frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW}10^{-6}}{W_{MIN}}\right]\right\}, \tag{3.24}$$

where $A_{bulk,max}$ is a parameter defined in BSIM3v3 model [72].

$$C_{db9} = W_{MIN}\left(K_{jp}C_{jp}L_{dp} + 2K_{jswp}C_{jswp}\right) + 2K_{jswp}C_{jswp}L_{dp}, \tag{3.25}$$

The coefficients a_{xy} , b_{xy} and c_{xy} of all the capacitances in eqn. (3.12) are summarized in Table 3.2.

Table 3.2 Coefficients of the capacitances for the proposed XOR gate

NMOS coefficients	
a_{db3}	$\frac{2A_v^2 L_{MIN}}{\mu_{eff,n} C_{ox}} \left(\frac{N}{1+N}\right)^2 \left(K_{jn} C_{jn} L_{dn} + 2K_{jswn} C_{jswn}\right)$
a_{gd3}	$2A_v^2 C_{gdo} \left(\frac{N}{1+N}\right)^2 \frac{L_{MIN}}{\mu_{eff,n} C_{ox}}$
c_{db3}	$2K_{jswn} C_{jswn} L_{dn}$
$b_{db3}, b_{gd3}, c_{gd3}$	0
PMOS coefficients	
b_{gd9}	$\frac{3}{4}\left(\frac{1+N}{N}\right) A_{bulk,max}\, \mu_{eff,p} C_{ox}^2 W_{MIN}^2 \left(V_{DD} - \lvert V_{T,P}\rvert\right)$
c_{gd9}	$C_{gdo} W_{MIN} - \frac{3}{4} A_{bulk,max}\, \mu_{eff,p} C_{ox}^2 W_{MIN} \left(V_{DD} - \lvert V_{T,P}\rvert\right) R_{DSW} 10^{-6}$
c_{db9}	$K_{jp} C_{jp} L_{dp} W_{MIN} + 2K_{jswp} C_{jswp} \left(L_{dp} + W_{MIN}\right)$
$a_{gd9}, a_{db9}, b_{db9}$	0

where the symbols have their usual meaning.

Using eqns. (3.20) – (3.25), the delay can be written as

$$t_{PD} = 0.69 \frac{1+N}{N} V_{SWING} \left(\frac{a}{V_{SWING}{}^2} + b\frac{V_{SWING}}{I_{SS}^2} + \frac{c + C_L}{I_{SS}}\right), \tag{3.26}$$

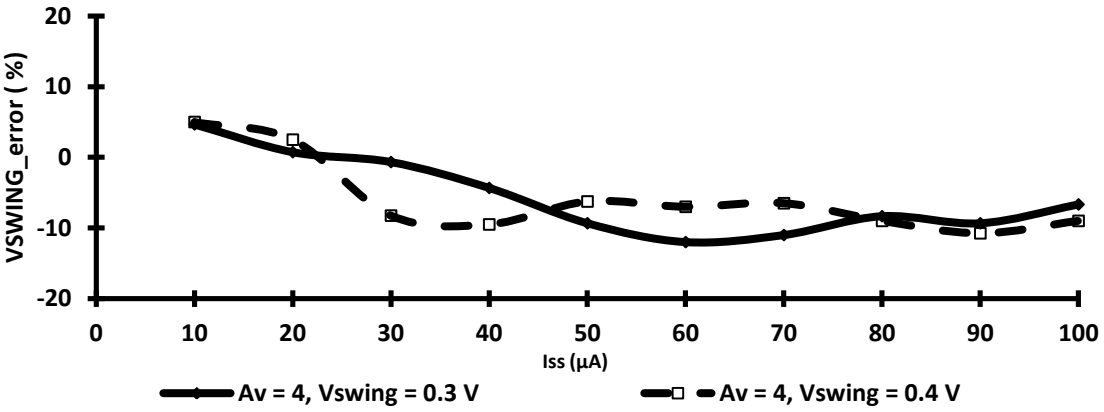
where $a = 2a_{db3} + 2a_{gd3}$, (3.27a)

$b = b_{gd9}$, (3.27b)

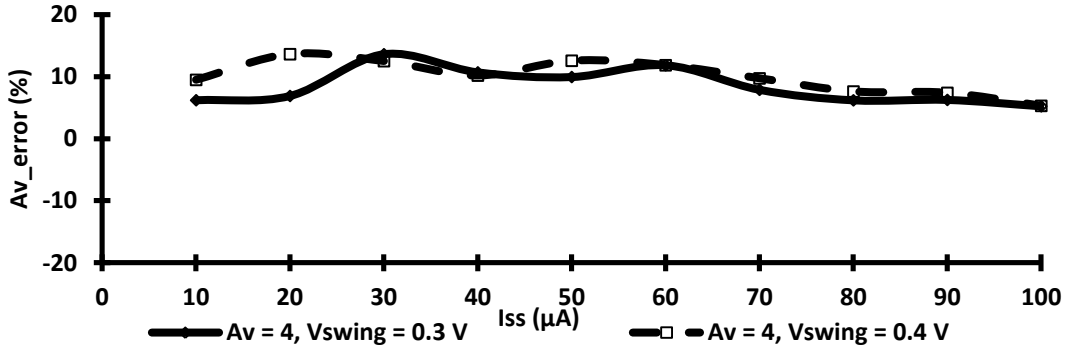
$c = 2c_{db3} + c_{gd9} + c_{db9}$. (3.27c)

The delay model can also be used for I_{SS} value outside the range [I_{LOW}, I_{HIGH}]. This is because for $I_{SS} > I_{HIGH}$, the capacitance coefficients of PMOS transistor in eqn. (3.26) differ as explained in section 3.4.3. As the capacitive contribution of PMOS transistor is negligible for high values of I_{SS}, eqn. (3.26) is used to predict the delay. Similarly, for $I_{SS} < I_{LOW}$, the capacitance coefficients of NMOS transistor in eqn. (3.26) differs. As the delay majorly depends on the capacitances of PMOS transistor for low values of I_{SS}, therefore, eqn. (3.26) is used to estimate the delay.

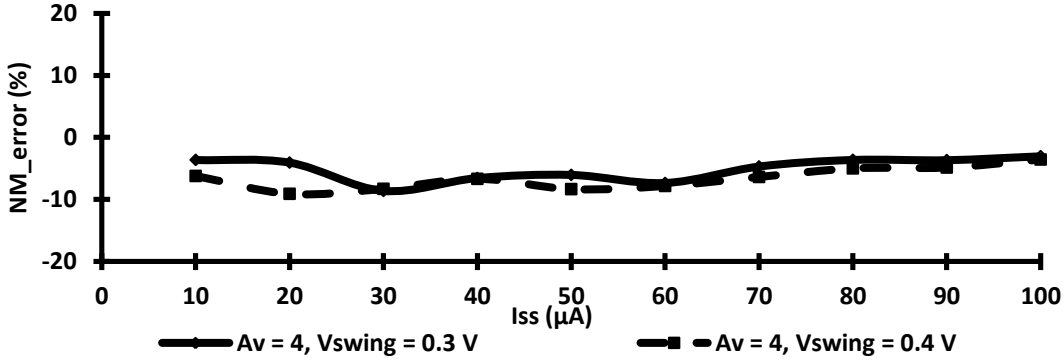
The accuracy of the static model is validated through SPICE simulations. The proposed XOR gate was designed and simulated with a power supply of 1.1 V for wide range of operating conditions:- voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, N =5, and the bias current ranging from 10 µA to 100 µA. The error plots in the simulated values of static parameters with respect to the predicted values in particular for small-signal voltage gain of 4 and voltage swing of 300 mV and 400 mV are shown in Figs. 3.5a-c. It may be noted that maximum error in voltage swing, small-signal voltage gain and noise margin are 11 %, 13 % and 11 % respectively. An error plot of noise margin for small-signal voltage gain of 2 and 4, N = 5 and the voltage swing ranging from 0.2 V to 0.7 V is plotted in Fig. 3.5d. It may be observed that the maximum error in noise margin is 14 %. It is found that there is a close agreement between the simulated and the predicted values of static parameters for all the operating conditions. Using the 3σ variations [71], the Monte Carlo simulations for noise margins is carried out for 300 sample runs and the results for different cases are reported in Table 3.3. It is found that the mean value of noise margin is always larger than the (3σ) variations [68].


VSWING_error (%)
20
10
0
-10
-20
0
10
20
30
40
50
60
70
80
90
100
Iss (µA)
Av = 4, Vswing = 0.3 V
Av = 4, Vswing = 0.4 V

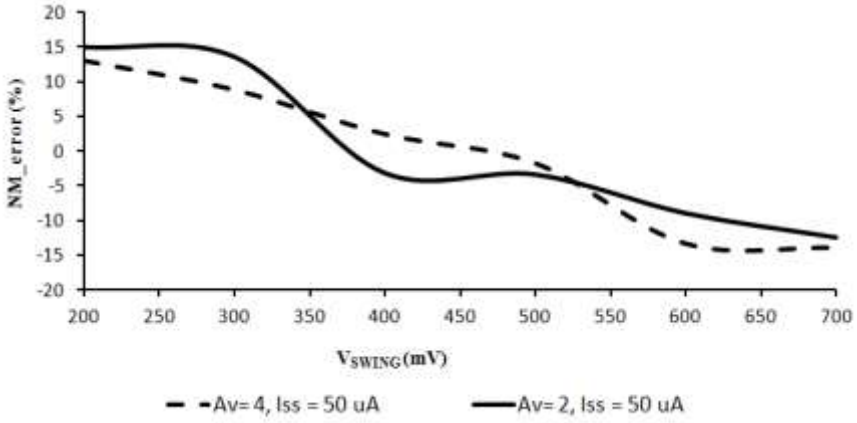
(a)


Av_error (%)
20
10
0
-10
-20
0
10
20
30
40
50
60
70
80
90
100
Iss (µA)
Av = 4, Vswing = 0.3 V
Av = 4, Vswing = 0.4 V

(b)


NM_error (%)
20
10
0
-10
-20
0
10
20
30
40
50
60
70
80
90
100
Iss (µA)
Av = 4, Vswing = 0.3 V
Av = 4, Vswing = 0.4 V

(c)



(d)

Fig. 3.5 Errors in the static parameters of the proposed XOR gate a) voltage swing b) small-signal voltage gain c) noise margin d) noise margin for different voltage swing values

Table 3.3 Results of Monte Carlo simulations (300 sample runs) on noise margin

Operating conditions	**Mean (μ)**	**Sigma (3σ)**
$A_v = 4$, $V_{SWING} = 0.2$ V	61.8 mV	39.6 mV
$A_v = 4$, $V_{SWING} = 0.4$ V	128 mV	46 mV
$A_v = 4$, $V_{SWING} = 0.6$ V	191 mV	66 mV

The delay is plotted as a function of N for $A_v = 4$, NM = 130 mV, $I_{SS} = 50$ μA and $C_L = 50$ fF in Fig. 3.6. It is found out that the delay asymptotically reaches to value of 455 ps. However, a high value of N results in larger transistor sizes of M7, M8 thus increasing the input capacitance seen from input B. Therefore, a good compromise between the two opposing requirements is to set N = 5 as after which improvement in speed is not significant. Similar results are obtained for other operating conditions.

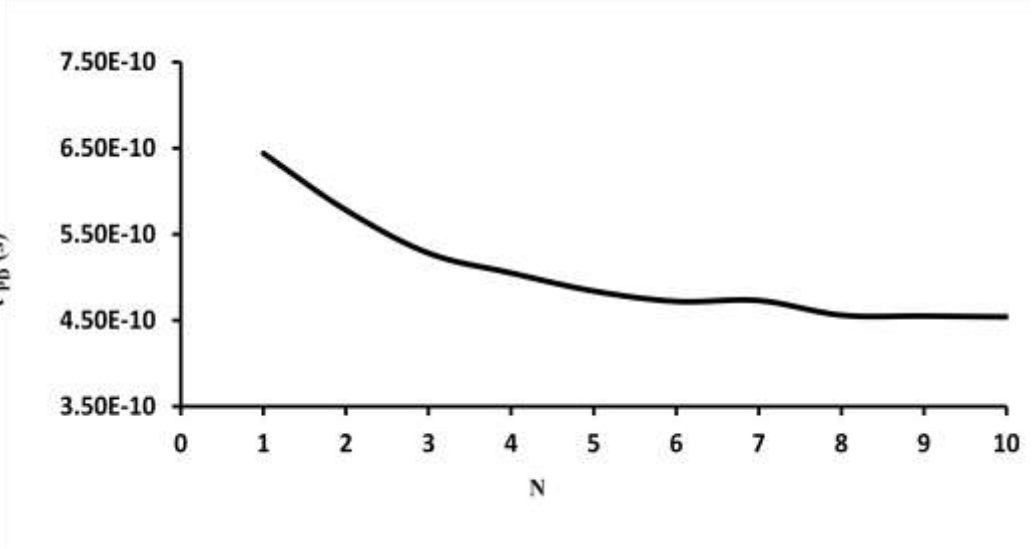
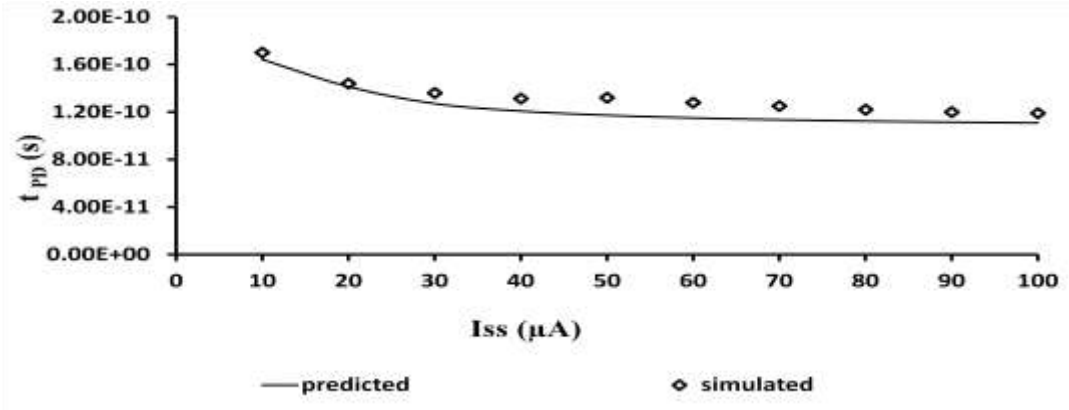
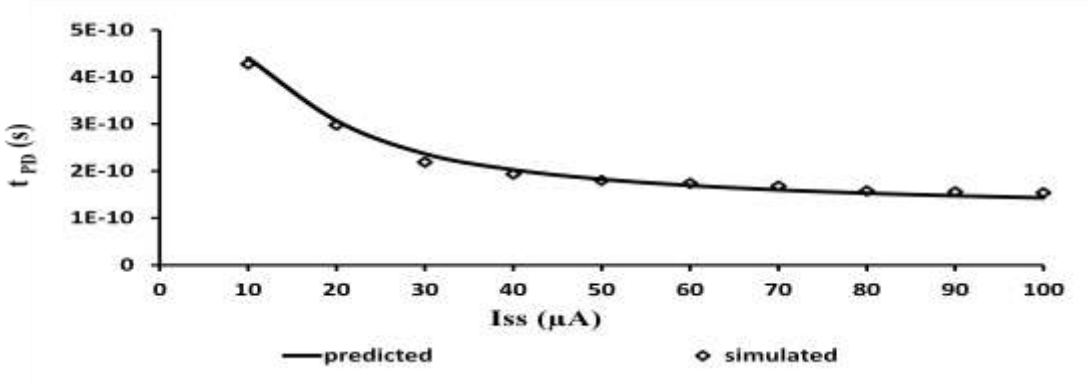


Fig. 3.6 Delay vs. N of the proposed XOR gate

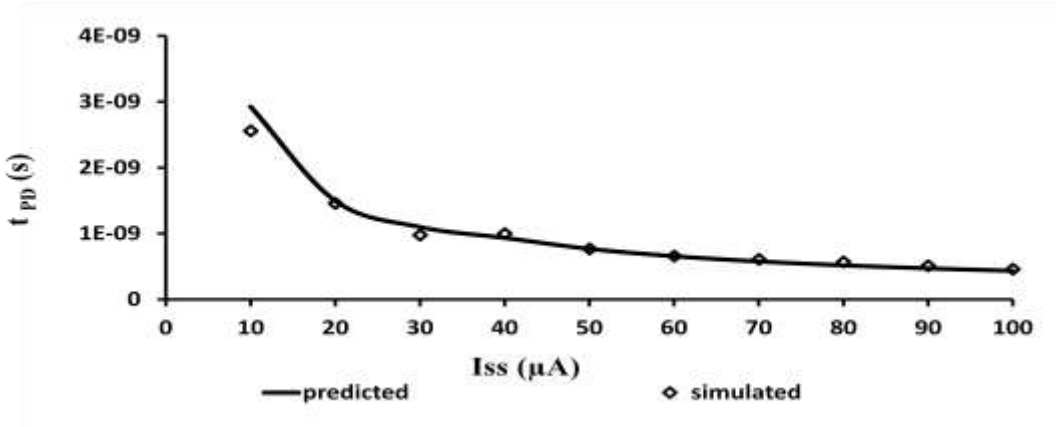
The accuracy of the delay model is validated through SPICE simulations with a power supply of 1.1 V. The proposed XOR gate was designed for wide range of operating conditions:- voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, the bias current ranging from 10 µA to 100 µA, N = 5, and load capacitance of 0 fF, 10 fF, 100 fF, 1 pF and fan out of 4. The simulated and the predicted delay in particular for $A_V = 4$, V_{SWING} = 400 mV, with different load capacitances are plotted in Fig. 3.7. It is found that there is a close agreement between the simulated and the predicted delay for all the operating conditions.



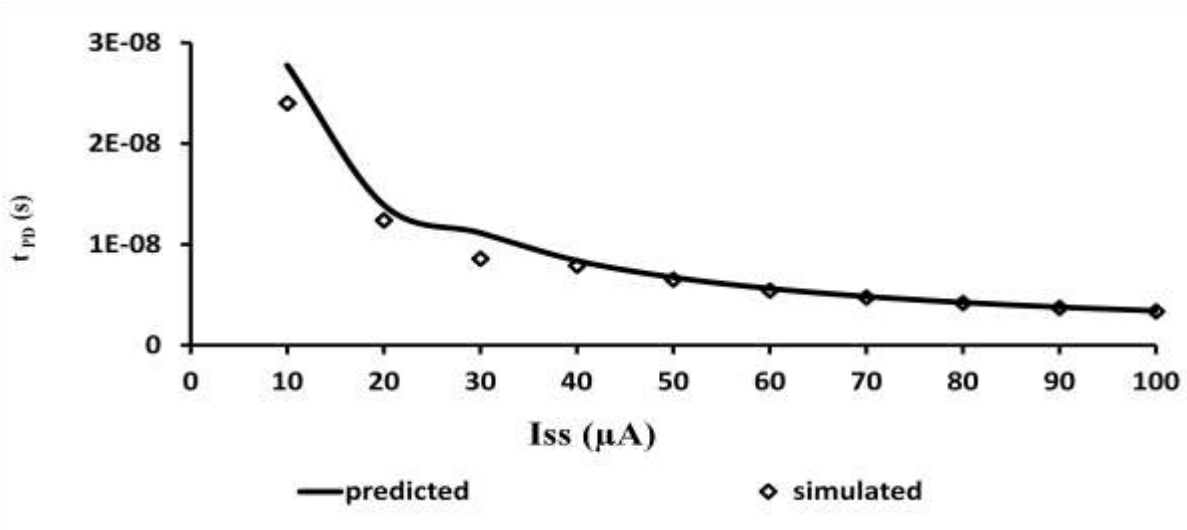
(a)


5E-10
4E-10
3E-10
2E-10
1E-10
0
t_{PD} (s)
0
10
20
30
40
50
60
70
80
90
100
Iss (μA)
predicted
simulated

(b)


4E-09
3E-09
2E-09
1E-09
0
t_{PD} (s)
0
10
20
30
40
50
60
70
80
90
100
Iss (μA)
predicted
simulated

(c)


3E-08
2E-08
1E-08
0
t_{PD} (s)
0
10
20
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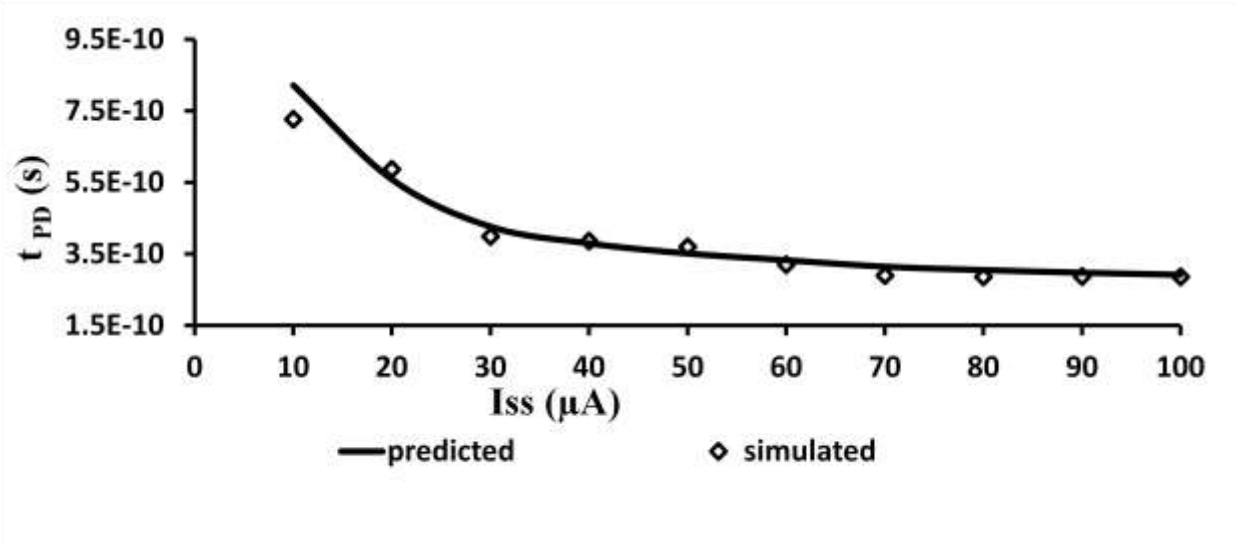
50
60
70
80
90
100
Iss (μA)
predicted
simulated

(d)



(e)

Fig. 3.7 Simulated and predicted delays of the proposed XOR gate vs. Iss with A_v = 4, NM = 130 mV for different C_L values a) 0 fF b) 10 fF c) 100 fF d) 1 pF e) FO4

The impact of parameter variations on the static parameters and the delay of the proposed and conventional XOR gates performance are studied at different design corners. The findings for various operating conditions are summarized in Table 3.4. It is found that the voltage swing, small-signal voltage gain, noise margin and delay of the proposed XOR gate varies by a factor of 1.87, 2.94, 2.28 and 1.89 respectively between the best and the worst cases whereas the corresponding variation for the conventional XOR gate is 1.76, 2.42, 1.8 and 1.85 respectively. Thus, the proposed XOR gate shows slightly higher variations than the conventional topology for different design corners which can be attributed to the smaller aspect ratio of transistors in the proposed XOR gate [71].

To demonstrate the effect of mismatch, the width of NMOS and PMOS transistors of the proposed and the differential CML XOR gates are varied by 10%. The variation in voltage swing, small-signal voltage gain, noise margin and delay are within 8% for both the gates.

Table 3.4 Impact of parameter variations on the static parameters and the delay of the proposed XOR gate

Simulation Condition: $A_v = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 100$ µA						
Parameter \ **NMOS / PMOS**		**T T**	**F F**	**S S**	**F S**	**S F**
V_{SWING} (mV)	Proposed	344	481	260	430	350
	Conventional	366	465	267	378	370
A_V	Proposed	3.1	2.1	5.2	3.1	3.1
	Conventional	3.2	2.1	4.3	3.1	3.1
NM (mV)	Proposed	94.2	78.5	94.6	116.6	95.4
	Conventional	100.6	76.7	90	103.1	101.1
t_{PD} (ps)	Proposed	265	237	448	255	262
	Conventional	553	515	954	527	550
Simulation Condition: $A_v = 4$, $V_{SWING} = 0.4$ V, $C_L = 50$ fF, $I_{SS} = 10$ µA						
V_{SWING} (mV)	Proposed	410	498	265	420	415
	Conventional	342	519	294	443	407
A_V	Proposed	3.8	1.9	5.5	2.9	3.7
	Conventional	2.98	1.81	4.39	2.67	2.81
NM (mV)	Proposed	130.2	63.6	98.9	110.6	129.4
	Conventional	89.8	56.7	99.6	104.2	101.1
t_{PD} (ns)	Proposed	2.4	1.7	3.2	2.1	2.3
	Conventional	3.7	3.2	4.6	3.5	3.6

where different design corners are denoted by T = Typical, F= Fast, S= Slow

3.4.4 Performance Comparison

In the previous subsections, the behavior of the proposed XOR gate is modeled and design parameters are expressed as a function of bias current and voltage swing. To compare the performance of the proposed XOR gate with the conventional one, high speed, power efficient and low power design cases are considered. The proposed and the conventional XOR gates are designed with their respective minimum power supply, NM = 130 mV, $A_v = 4$, N = 5.

3.4.4.1 High Speed Design

A high speed design requires bias current that results in minimum delay. The delay given in eqn. (3.26) decreases with the increasing I_{SS} and tends to an asymptotic minimum value of $0.69\ \frac{1+N}{N}\frac{a}{V_{SWING}}$ for $I_{SS} \to \infty$. A substantial improvement in delay with increasing bias current is achieved if condition

$$\frac{a}{{V_{SWING}}^2} \geq b\frac{V_{SWING}}{I_{SS}^2} + \frac{c+ C_L}{I_{SS}}, \tag{3.28}$$

is satisfied. However, a high value of bias current results in large transistor sizes. Therefore, the bias current should be set to such a value after which the improvement in speed is not significant. If equality sign in eqn. (3.28) is considered then the delay is close to its minimum value and the use of high bias current is avoided. Therefore, this assumption leads to a bias current (I_{SS_HS}) and delay (t_{PD_MIN}) as

$$I_{SS\_HS} = \frac{c+ C_L}{2a}\, V_{SWING}^2 \left(1 + \sqrt{1 + 4\,\frac{ab}{(c+C_L)^2}\frac{1}{V_{SWING}}}\right), \tag{3.29}$$

$$t_{PD\_MIN} = 2 \times 0.69\ \frac{1+N}{N}\frac{a}{V_{SWING}}. \tag{3.30}$$

For a load capacitance of 50 fF, the bias current (I_{SS_HS}) as expressed in eqn. (3.29) is calculated as160 µA. A delay of 194 ps and 211 ps are obtained from eqn. (3.30) and simulations respectively. On the contrary, the conventional XOR gate results in a delay of 528 ps. This indicates that the proposed XOR gate can achieve much higher speed than the conventional one.

3.4.4.2 Power Efficient Design

A power efficient design requires bias current that results in minimum power-delay product (PDP). The power is calculated as the product of V_{DD} and I_{SS}. So, the PDP of the proposed XOR gate may be expressed as

$$PDP = 0.69\, V_{DD} V_{SWING} \frac{1+N}{N}\left(\frac{a}{V_{SWING}{}^2} I_{SS} + b\frac{V_{SWING}}{I_{SS}} + c + C_L\right). \quad (3.31)$$

Therefore, the current I_{SS_PDP} for minimum PDP may be given as

$$I_{SS\_PDP} = \sqrt{\frac{b}{a}}(V_{SWING})^{\frac{3}{2}}. \quad (3.32)$$

Accordingly, the minimum PDP results to

$$PDP = 0.69\, V_{DD} V_{SWING} \frac{1+N}{N}\left(\frac{2\sqrt{ab}}{\sqrt{V_{SWING}}} + c + C_L\right). \quad (3.33)$$

With a load capacitance of 50 fF, the bias current for minimum PDP (I_{SS_PDP}) is 5.8 µA. A PDP value of 32 fJ is obtained for the proposed XOR gate. On the other hand, a conventional XOR gate results in a PDP value of 13 fJ. The result signifies that the proposed XOR gate has higher PDP value than the conventional one.

3.4.4.3 Low Power Design

In low power designs, the bias current I_{SS} is set to low values so that the term $b\frac{V_{SWING}}{I_{SS}^2}$ is dominant in eqn. (3.26). Hence, the delay reduces to

$$t_{PD} = 0.69\, b \left(\frac{1+N}{N}\right)\left(\frac{V_{SWING}}{I_{SS}}\right)^2. \quad (3.34)$$

The proposed XOR gate with the load capacitance of 5 fF, gives I_{SS} as 2 µA and has a power consumption of 2.2 µW while the conventional XOR gate results in power consumption of 2.8 µW.

The performance comparison of the proposed and conventional XOR gates for different design cases is summarized in Table 3.5.

Table 3.5 Summary of the design cases for the proposed and the conventional XOR gates

Design case	Parameter	Proposed	Conventional
High speed	Delay	Low	High
Power efficient	Power delay product	High	Low
Low power	Power	Low	High

3.5 PROPOSED SEQUENTIAL GATES WITH MODIFIED PDN

The proposed approach is used to implement sequential circuits. A D latch is chosen as representative of the sequential circuits. The topology for a D latch with differential inputs D and CLK is shown in Fig. 3.8. It consists of two triple-tail cells (M3, M4, M7) and (M5, M6, M8) biased by separate current sources of $I_{SS}/2$ value. The transistors M7 and M8 are driven by the differential CLK input and are connected between the supply terminal and the common source terminal of transistor pairs M3–M4 and M5–M6 respectively.

3.5.1 Operation of the proposed D latch

A high differential CLK voltage turns ON the transistor M8, and deactivates the transistor pair (M5–M6). At the same time, the transistor M7 turns OFF so that the transistor pair (M3–M4) generates the output according to the differential input D. Thus, the D latch works in the transparent state. Similarly, the transistor pair (M5–M6) gets activated for low differential CLK voltage and preserves the previous output. Therefore, the D latch operates in the hold state for low value of the differential CLK input.

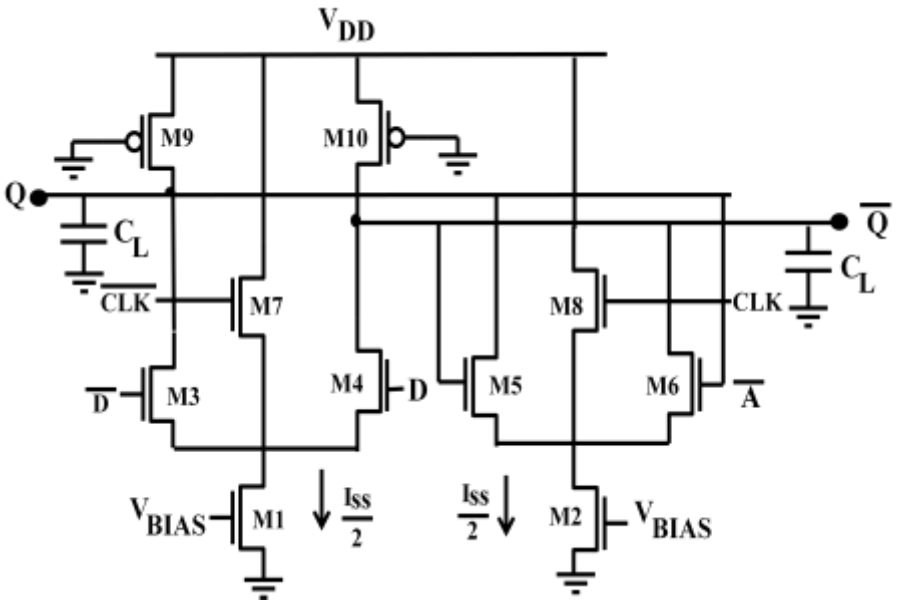


Fig. 3.8 Proposed D latch

3.5.2 Analysis of the proposed D latch

The behavior of the proposed D latch is analyzed in terms of static and delay parameters using pencil-and-paper approach. The analysis is simplified by modeling the load transistors M9, M10 with an equivalent linear resistance, R_P given in eqn. (2.2).

3.5.2.1 Static Model

The static behaviour is modelled in terms of the voltage swing, the small-signal voltage gain and the noise margin. As explained for the proposed XOR gate to achieve proper operation of the triple-tail cells, the aspect ratio of transistors M7, M8 is made greater than other transistors' aspect ratio by a factor N. The differential output voltages for various input combinations of the D latch is obtained by following the procedure as suggested for the proposed XOR gate. The corresponding values are enlisted in Table 3.6. It can be observed that there are two values of maximum output voltage (V_{OH}) and minimum output voltage (V_{OL}). Consequently, the voltage swing, V_{SWING1} when the input D and the present state are same can be expressed as

$$V_{SWING1} = V_{OH1} - V_{OL1} = R_P I_{SS}\left(1 + \frac{1}{1+N}\right), \quad (3.35)$$

where V_{OH1}, V_{OL1} are maximum output voltage and minimum output voltage respectively for the same input D and the present state. The voltage swing, V_{SWING2} for the different value of the input D and the present state can be expressed as

$$V_{SWING2} = V_{OH2} - V_{OL2} = R_P I_{SS}\left(\frac{N}{1+N}\right), \quad (3.36)$$

where V_{OH2}, V_{OL2} are maximum output voltage and minimum output voltage respectively for different input D and the present state.

Table 3.6 Differential output voltages of the proposed D latch for various input combinations

Inputs		**Present State**	**Currents through the transistors**						**Next State** **Differential output ($V_Q - \overline{V_Q}$)**	
CLK	**D**	**Q**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**	**Level**	$R_P[(i_{D,4} + i_{D,6}) - (i_{D,3} + i_{D,5})]$
L	L	L	I_3	0	I_1	0	I_2	0	V_{OL1}	$-R_P\frac{I_{SS}}{2}(1+\frac{1}{1+N})$
L	L	H	I_3	0	0	I_1	I_2	0	V_{OH2}	$R_P\frac{I_{SS}}{2}(\frac{N}{1+N})$
L	H	L	0	I_3	I_1	0	I_2	0	V_{OL2}	$-R_P\frac{I_{SS}}{2}(\frac{N}{1+N})$
L	H	H	0	I_3	0	I_1	I_2	0	V_{OH1}	$R_P\frac{I_{SS}}{2}(1+\frac{N}{1+N})$
H	L	L	I_1	0	I_3	0	0	I_2	V_{OL1}	$-R_P\frac{I_{SS}}{2}(1+\frac{N}{1+N})$
H	L	H	I_1	0	0	I_3	0	I_2	V_{OL2}	$-R_P\frac{I_{SS}}{2}(\frac{N}{1+N})$
H	H	L	0	I_1	I_3	0	0	I_2	V_{OH2}	$R_P\frac{I_{SS}}{2}(\frac{N}{1+N})$
H	H	H	0	I_1	0	I_3	0	I_2	V_{OH1}	$R_P\frac{I_{SS}}{2}(1+\frac{N}{1+N})$

where L/H= low/high differential input voltage, $I_1 = \frac{I_{SS}}{2}$, $I_2 = \frac{I_{SS}}{2}\left(\frac{N}{1+N}\right)$ and $I_3 = \frac{I_{SS}}{2}\left(\frac{1}{1+N}\right)$

As $V_{SWING2} < V_{SWING1}$, V_{SWING2} is considered as the worst case voltage swing

$$V_{SWING} = R_P I_{SS}\left(\frac{N}{1+N}\right). \quad (3.37)$$

The small-signal voltage gain (A_v) and noise margin (NM) for the proposed D latch are computed as

$$A_v = g_{m,n}R_P = \frac{1+N}{N}\frac{V_{SWING}}{2}\sqrt{2\mu_{eff,n}C_{OX}\frac{W_N}{L_N}\frac{1}{I_{SS}}}, \quad (3.38)$$

$$NM = \frac{V_{SWING}}{2}\left[1-\frac{\sqrt{2}}{A_v}\right], \quad (3.39)$$

where $\mu_{eff,n}$, $g_{m,n}$, W_N and L_N are the effective electron mobility, the transconductance, the effective channel width and length of transistors M3-M6 respectively.

3.5.2.2 Delay Model

In this section, a delay model of the proposed D latch is formulated in terms of bias current and the voltage swing. For a low-to-high transition on CLK input the output switches by activating (deactivating) the transistor pair M3–M4 (M5–M6), the circuit reduces to a simple CML inverter. The equivalent linear half circuit is shown in Fig. 3.9 where C_{gdi} , C_{dbi} represents the gate-drain capacitance and the drain-bulk junction capacitance of the i^{th} (i= 3, 9, 5) transistor. The capacitance C_{input} represents the input capacitance of the transistor M5 [27].

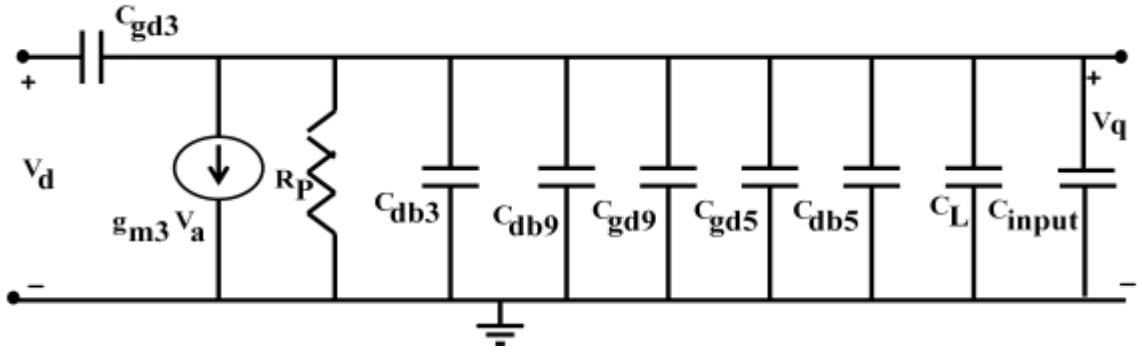


Fig. 3.9 Linear half-circuit (with low-to-high transition on CLK)

The delay of the proposed D latch can be expressed as

$$t_{PD} = 0.69\, R_P\left(C_{db3} + C_{gd3} + C_{gd9} + C_{db9} + C_{db5} + C_{gd5} + C_L + C_{input}\right), \quad (3.40)$$

with $C_{db3} = C_{db5}$, $C_{gd3} = C_{gd5}$ and, $R_P = \frac{1+N}{N}\frac{V_{SWING}}{I_{SS}}$, eqn. (3.40) can be rewritten as

$$t_{PD} = 0.69\ \frac{1+N}{N}\frac{V_{SWING}}{I_{SS}}\left(2C_{db3} + 2C_{gd3} + C_{gd9} + C_{db9} + C_L + C_{input}\right). \quad (3.41)$$

It can be observed that the delay given in eqn. (3.41) is expressed in terms of the transistors' capacitances, which in turn depend on their aspect ratio. In practical situations, the transistor aspect ratio must be set to meet the design specifications on noise margin, power and delay. To this end, a design procedure to size the transistors is worked out and the delay model is revisited again for the purpose.

3.5.3 Design of the proposed D latch

An examination of the static model of the proposed D latch reveals that it is similar to the one developed for combinational circuits in section 3.4.2.1. Therefore, the proposed D latch is designed by following the same procedure outlined for combinational gates in section 3.4.3 on the basis of static model and is not repeated here.

Further, the design eqns. (3.13)–(3.18) can be used to express the parasitic capacitances in the delay in terms of the bias current and the voltage swing as done for the proposed XOR gate. The additional input capacitance C_{input} for the transistor M5 can be expressed as

$$C_{input} = \frac{2}{3}C_{ox}L_{MIN}W_5 = \frac{4}{3\mu_{eff,n}}\left(\frac{N}{1+N}\right)^2\left(\frac{A_v}{V_{SWING}}\right)^2 I_{SS}\,{L_{MIN}}^2. \quad (3.42)$$

The coefficients a_{xy}, b_{xy} and c_{xy} of all the capacitances in eqn. (3.41) are summarized in Table 3.7. The delay of the D latch can be written as

$$t_{PD} = 0.69\ \frac{1+N}{N}V_{SWING}\left(\frac{a}{{V_{SWING}}^2} + b\frac{V_{SWING}}{I_{SS}^2} + \frac{c+C_L}{I_{SS}}\right), \quad (3.43)$$

where $a = 2a_{db3} + 2a_{gd3} + a_{input}$, (3.44a)

$b = b_{gd9}$, (3.44b)

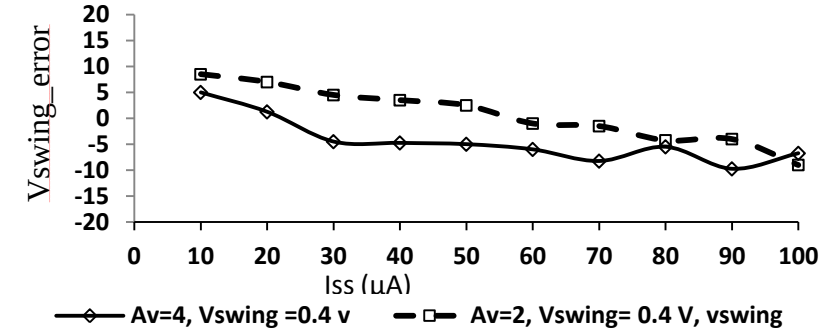
$$c = 2c_{db3} + c_{gd9} + c_{db9}. \quad (3.44c)$$

Table 3.7 Coefficients of the capacitances for the proposed D latch

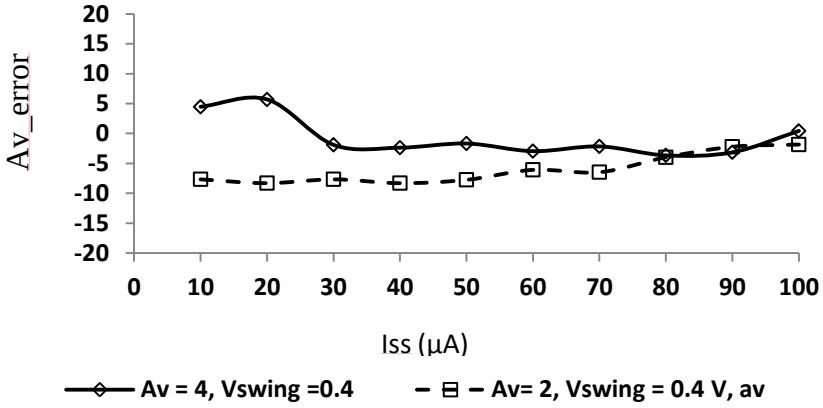
NMOS coefficients	
a_{db3}	$\frac{2A_v^2 L_{MIN}}{\mu_{eff,n} C_{ox}} \left(\frac{N}{1+N}\right)^2 \left(K_{jn} C_{jn} L_{dn} + 2K_{jswn} C_{jswn}\right)$
a_{gd3}	$2A_v^2 C_{gdo} \left(\frac{N}{1+N}\right)^2 \frac{L_{MIN}}{\mu_{eff,n} C_{ox}}$
a_{input}	$\frac{4A_v^2}{3\mu_{eff,n}} \left(\frac{N}{1+N}\right)^2 {L_{MIN}}^2$
c_{db3}	$2K_{jswn} C_{jswn} L_{dn}$
$b_{db3}, b_{gd3}, c_{gd3}$	0
PMOS coefficients	
b_{gd9}	$\frac{3}{4} \left(\frac{1+N}{N}\right) A_{bulk,max}\, \mu_{eff,p} C_{ox}^2 W_{MIN}^2 \left(V_{DD} - \left\|V_{T,P}\right\|\right)$
c_{gd9}	$C_{gdo} W_{MIN} - \frac{3}{4} A_{bulk,max}\, \mu_{eff,p} C_{ox}^2 W_{MIN} \left(V_{DD} - \left\|V_{T,P}\right\|\right) R_{DSW} 10^{-6}$
c_{db9}	$K_{jp} C_{jp} L_{dp} W_{MIN} + 2K_{jswp} C_{jswp} \left(L_{dp} + W_{MIN}\right)$
$a_{gd9}, a_{db9}, b_{db9}$	0

where the symbols have their usual meaning.

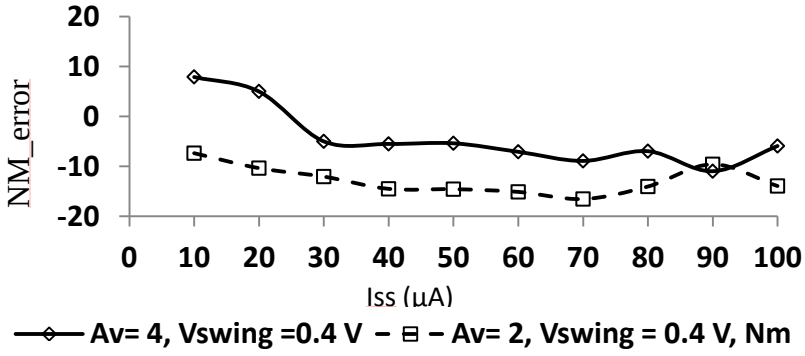
The accuracy of the static model is validated through SPICE simulations. The proposed D latch was designed with a power supply of 1.1 V and simulated for wide range of operating conditions:- voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, N = 5, and the bias current ranging from 10 µA to 100 µA. The error in simulated and theoretical values for voltage swing, small-signal voltage gain and noise margin using eqn. (3.37), eqn. (3.38) and eqn. (3.39) respectively are calculated and are plotted in Fig. 3.10. It may be noted that maximum error in voltage swing, small-signal voltage gain and noise margin are 10 %, 8 % and 14 % respectively.



(a)



(b)



(c)

Fig. 3.10 Errors in the static parameters of the proposed D latch a) voltage swing b) small-signal voltage gain c) noise margin

To verify the accuracy of the delay model, the proposed D latch was designed for wide range of operating conditions:- voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, the bias current ranging from 10 µA to 100 µA, N = 5, and load capacitance of 0 fF, 10 fF, 100 fF, and 1 pF. The simulated and the predicted delay in particular for NM = 130

mV, A_v = 4 and with different load capacitances are plotted in Fig. 3.11. It is found that there is a close agreement between the simulated and the predicted values for all the operating conditions.

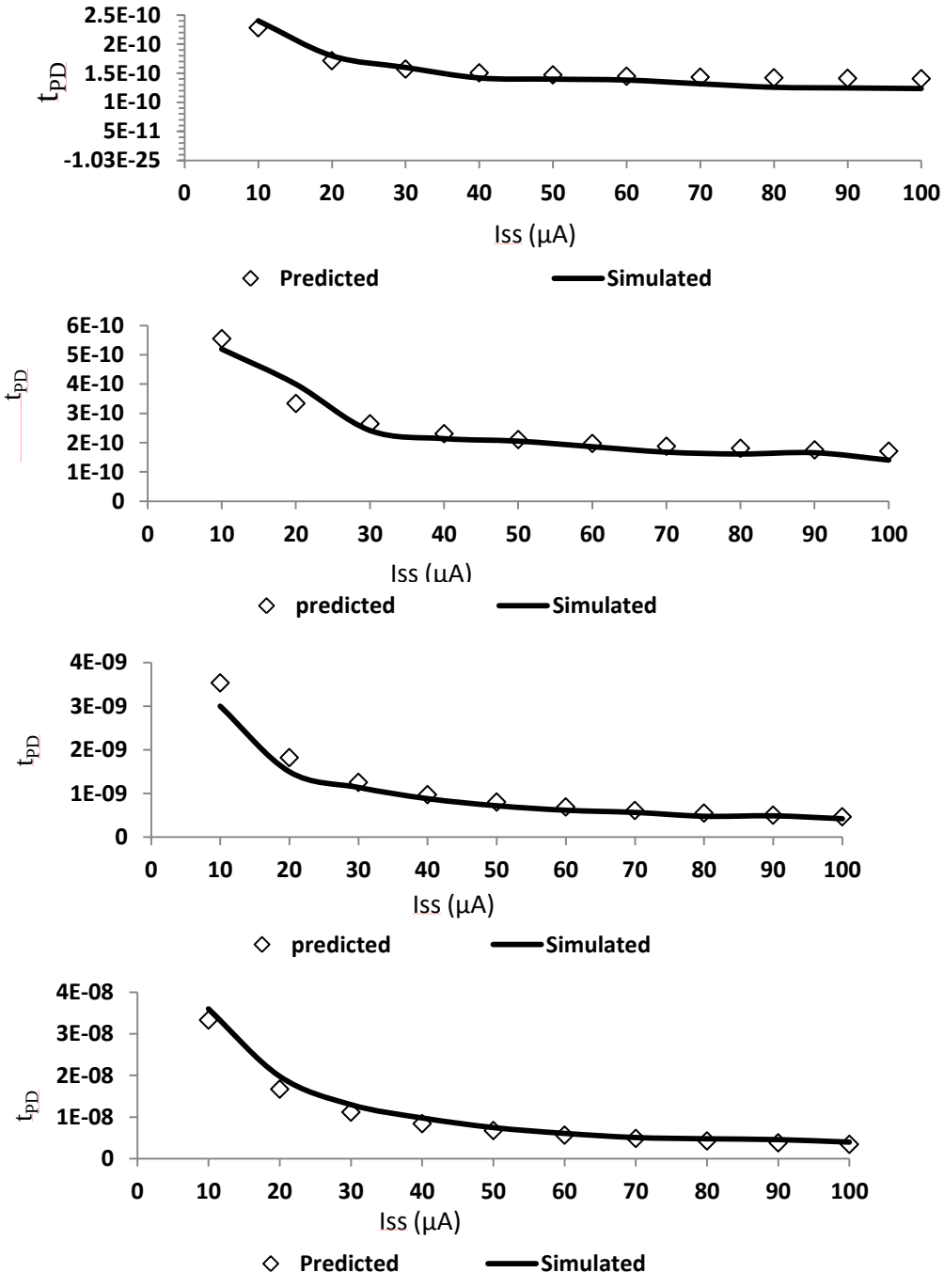


Fig. 3.11 Simulated and predicted delays of the proposed D latch vs. I_{SS} with NM = 130 mV, A_v = 4 for different C_L values a) 0 fF b) 10 fF c) 100 fF d) 1 pF

The impact of parameter variations on the proposed and conventional D latch performance is studied at different design corners. The findings with the operating conditions $A_v = 4$, $V_{SWING} = 0.4$ V, $C_L = 100$ fF, $I_{SS} = 100$ µA are summarized in Table 3.8. It is found that the voltage swing, small-signal voltage gain, and noise margin of the proposed D latch varies by a factor of 1.8, 1.4, and 2.1 respectively between the best and the worst cases whereas the corresponding variation of 1.7, 1.2, and 1.7 respectively is observed for the conventional D latch. In relation to the delay, it is found that the delay varies by a factor of 1.8 and 1.7 between the best and the worst cases for the proposed and the conventional D latch respectively. Thus, the proposed D latch show slightly higher variations than the conventional D latch for different design corners which can be attributed to the smaller aspect ratio of transistors in the proposed D latch [71].

Table 3.8 Impact of parameter variations on the static parameters and the delay of the proposed D latch

Parameter \ **NMOS / PMOS**		**T T**	**F F**	**S S**	**F S**	**S F**
V_{SWING} (mV)	Proposed	427	590	327	447	417
	Conventional	416	508	300	509	457
A_V	Proposed	4.3	5.34	3.9	4.14	4.9
	Conventional	4.34	4.42	4	4.46	5
NM (mV)	Proposed	143	216	104	147	148
	Conventional	139	172	97	173	163
t_{PD} (ps)	Proposed	467	380	580	410	430
	Conventional	589	565	984	587	590

where different design corners are denoted by T = Typical, F= Fast, S= Slow

3.5.4 Performance Comparison

In the previous subsections, the behavior of the proposed D latch is modeled and design parameters are expressed as a function of bias current and voltage swing. To compare the performance of the proposed D latch with the conventional one, design cases such as high speed, and power efficient are considered. The proposed and the conventional gates are designed with their respective minimum a power supply, noise margin of 130 mV, small-signal gain of 4, N = 5.

3.5.4.1 High Speed Design

A high speed design requires bias current that results in minimum delay. The delay expressed in eqn. (3.43) decreases with the increasing I_{SS} and tends to an asymptotic minimum value of $0.69\ \frac{1+N}{N}\frac{a}{V_{SWING}}$ for $I_{SS} \rightarrow \infty$. A substantial improvement in delay with increasing bias current is achieved if condition

$$\frac{a}{{V_{SWING}}^2} \geq b\frac{V_{SWING}}{I_{SS}^2} + \frac{c+ C_L}{I_{SS}}, \tag{3.45}$$

is satisfied. However, high value of bias current results in large transistor sizes. Therefore, the bias current should be set to such a value after which the improvement in speed is not significant. If equality sign in eqn. (3.45) is considered then the delay is close to its minimum value and the use of high bias current is avoided. Therefore, this assumption leads to a bias current (I_{SS_HS}) and delay (t_{PD_MIN}) as

$$I_{SS\_HS} = \frac{c+ C_L}{2a}\, V_{SWING}^2 \left(1 + \sqrt{1 + 4\,\frac{ab}{(c+C_L)^2}\frac{1}{V_{SWING}}}\right), \tag{3.46}$$

$$t_{PD\_MIN} = 2 \times 0.69\ \frac{1+N}{N}\frac{a}{V_{SWING}}. \tag{3.47}$$

The proposed D latch designed for high speed performance with a load capacitance of 50 fF, gives I_{SS_HS} as 254 µA. A delay of 265 ps and 255 ps are obtained from eqn. (3.47) and

simulations respectively. On the contrary, a conventional high speed D latch results in a delay of 598 ps. This indicates that the proposed D latch can achieve much higher speed than the conventional one.

3.5.4.2 Power Efficient Design

A power efficient design requires bias current that results in minimum power-delay product (PDP). The power is calculated as the product of V_{DD} and I_{SS}. So, the PDP of the proposed D latch may be expressed as

$$\mathrm{PDP} = 0.69\, V_{DD} V_{SWING} \frac{1+N}{N}\left(\frac{a}{{V_{SWING}}^2} I_{SS} + b\frac{V_{SWING}}{I_{SS}} + c + C_L\right),. \quad (3.48)$$

Therefore, the current I_{SS_PDP} for minimum PDP may be given as

$$I_{SS\_PDP} = \sqrt{\frac{b}{a}}(V_{SWING})^{\frac{3}{2}}. \quad (3.49)$$

Accordingly, the minimum PDP results to

$$\mathrm{PDP} = 0.69\, V_{DD} V_{SWING} \frac{1+N}{N}\left(\frac{2\sqrt{ab}}{\sqrt{V_{SWING}}} + c + C_L\right). \quad (3.50)$$

The proposed D latch for the power efficient design case, gives I_{SS_PDP} as 5.3 µA for a load capacitance of 100 fF. A PDP value of 38.5 fJ has been obtained for the proposed D latch. On the other hand, a conventional D latch has a PDP value of 24 fJ. The result signifies that the proposed D latch results in higher PDP values than the conventional one.

3.5.4.3 Low Power Design

In low power designs, the bias current I_{SS} is set to low values so that the term $b\frac{V_{SWING}}{I_{SS}^2}$ is dominant in eqn. (3.43). Hence, the delay reduces to

$$t_{PD} = 0.69\, b\left(\frac{1+N}{N}\right)\left(\frac{V_{SWING}}{I_{SS}}\right)^2. \quad (3.51)$$

The proposed D latch with the load capacitance of 5 fF, N = 5 gives I_{SS} as 2 µA and has a power consumption of 2.3 µW while the conventional XOR gate results in power consumption of 2.85 µW.

3.6 CONCLUDING REMARKS

In this chapter, a new approach to realize the logic function is presented. The PDN of the differential CML gate is modified to lower the power supply requirement. The triple-tail cell concept is introduced in differential CML gates such that the number of source-coupled transistor pair levels is reduced in comparison to ones required in series-gating approach. New topologies for combinational and sequential circuits are developed. The behavior of the proposed gates is examined and modeled using pencil-and-paper approach. A design procedure based on the static model of the gates is put forward. The validity of the models is verified by designing and comparing the simulated results with the predicted ones for wide range of operating conditions. A close agreement between the simulated and the predicted values for the static and delay parameters is observed. The impact of parameter variations is also studied on the proposed and existing topologies. It is found that the proposed topologies show slightly higher variations than the existing ones for different design corners which can be attributed to the smaller sizes of the transistors employed in the proposed ones. In the last, the method to design the proposed topologies for different design cases such as high speed, power efficient and low power is described. This is accompanied by the performance comparison with the conventional ones designed for the respective case. The comparison results recommend the use of proposed topologies for high speed and low power design cases.

5.1 INTRODUCTION

The proliferation of efficient telecommunication networks, high speed microprocessors and memories has rekindled interest in electronics devices and systems. High capacity channels and high speed digital transceiver circuits are needed in communication system designs. CML gates, since the early days of digital integrated circuits are used to implement high speed digital circuits. However, to meet the increasing rate of data-transmission speed, it is necessary to improve the speed of the CML gates. The load section in a CML gate plays an important role in determining its speed and therefore is worked upon.

In this chapter, a brief description of available loads for the CML gate is presented. A new active load exhibiting the capacitive coupling phenomenon is put forward and is analyzed. New differential CML and PFSCL gates are developed and their behavior is modeled. The mathematical formulation for the delay of the proposed gates is also put forward. Basic digital logic gates are implemented and their performance is compared with the existing ones.

5.2 AVAILABLE LOADS

In a CML gate, the load determines the delay and hence its speed. Conventionally, a passive resistor as shown in Fig. 5.1a is employed as load but it requires large implementation area, therefore active loads are used. A variety of MOS active loads such as diode-connected transistor, a current source and a transistor operating in the linear region are available [2, 52] and are shown in Figs. 5.1 b,c,d respectively. In digital circuits, the emphasis is on smaller delays therefore the devices biased in saturation region are not used.

A PMOS transistor with its gate connected at the ground is employed as load in CML gate. It operates in linear region for all output range and has a resistance independent of substrate bias effect [52].

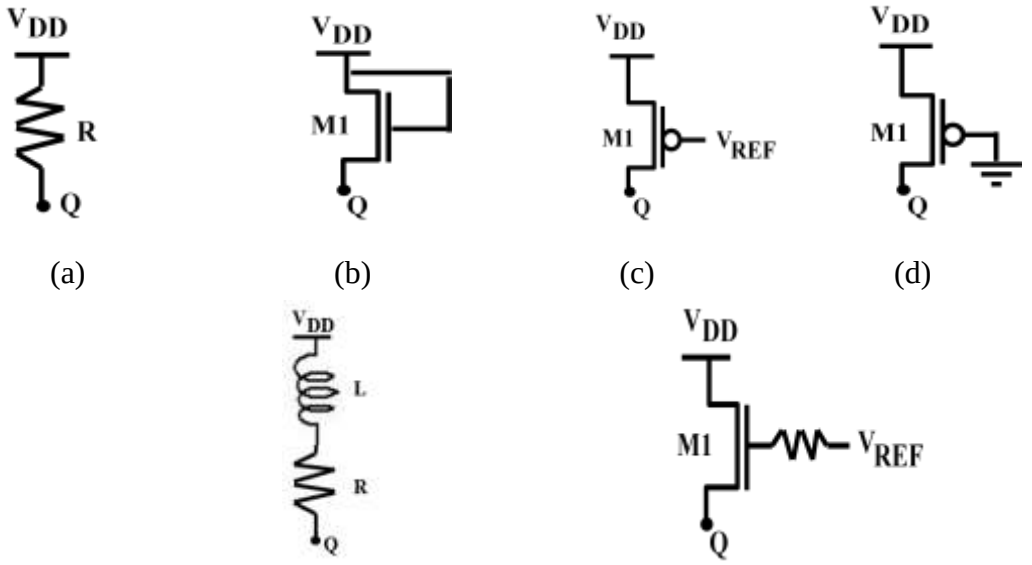


Fig. 5.1 Existing loads for a CML gate a) passive resistor b) diode-connected transistor c) current source d) transistor in linear region e) series connected passive inductor and resistor f) active inductor

The basic building block of a CML gate is a differential amplifier; therefore the techniques developed to improve circuit performance in analog domain can be exploited. In view of this, the shunt-peaking technique is introduced [45] wherein a passive inductor as shown in Fig. 5.1e is placed in series with the resistor to improve the speed of the CML gates. Several restrictions such as large component size and lengthier design process are imposed due to passive inductor hence active inductor (Fig. 5.1f) is recommended. An active inductor employs an NMOS transistor with its gate connected to separate supply via resistor

[43]. Both the arrangement use passive components and hence are not preferred in integrated circuit design. In this work, a new active load employing only transistors is proposed.

5.3 PROPOSED NP-LOAD

The circuit of the proposed load is shown in Fig. 5.2. It uses an NMOS transistor M1 and a PMOS transistor M2 and is referred to as NP-load. The drain and the source terminals of the transistor M1 are connected to the power supply and the output node Q respectively. The gate of transistor M2 is connected to the output node Q whereas its source terminal is connected to a reference voltage source V_{REF}. The load exhibits capacitive coupling during the transition at the output node Q. The detailed analysis of the capacitive coupling phenomenon and the evaluation of the load resistance are discussed.

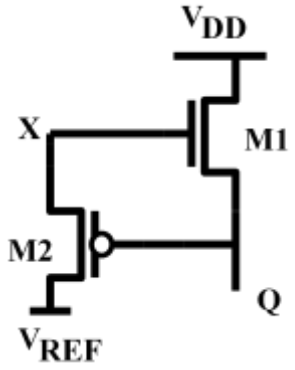


Fig. 5.2 Proposed NP-load

5.3.1 Analysis of the proposed NP-load

To reflect the capacitive coupling behavior of the proposed load, the parasitic capacitances at different nodes are identified and are shown in Fig. 5.3 where C_{gdi}, C_{dbi} and C_{gsi} represents the gate-to-drain capacitance, drain-bulk capacitance and gate-to-source capacitance of the i^{th} (i =1, 2) transistor in the load. The analysis is simplified by representing

the capacitances between the node Q and the intermediate node X as coupling capacitance C_C (C_{gs1} + C_{gd2}) while denoting the capacitances between node X and ground as C_X (C_{gd1}+ C_{db2}).

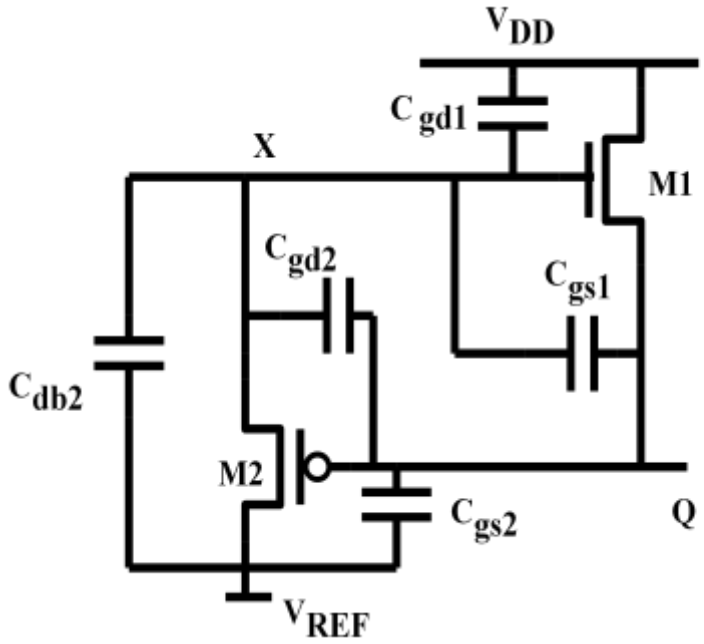


Fig. 5.3 Parasitic capacitances of the transistors M1 and M2

Consider a low-to-high transition at the output node Q, this change in the voltage of node Q gets coupled to node X through the coupling capacitance C_C. Let i_{CC} and i_{CX} be the transient currents flowing through C_C and C_X respectively. By applying the KCL, the current equation at node X can be written as

$$i_{CC} - i_{CX} \approx 0, \tag{5.1}$$

where it is assumed that negligible current flows in transistor M2. Substituting the current values,

$$C_X \frac{dV_X}{dt} \approx C_C \frac{d(V_Q - V_X)}{dt}, \tag{5.2}$$

where V_Q and V_X represents the voltages of the node Q and X respectively. The eqn. (5.2) can be rearranged as

$$\frac{dV_X}{dt} = \frac{C_C}{C_C+C_X}\frac{dV_Q}{dt}. \tag{5.3}$$

It is clear from eqn. (5.3) that voltage of the node X follows the change in the output voltage. The solution of eqn. (5.3) can be found as

$$\int_{V_{REF}}^{V_X(t)} dV_X = \left(\frac{C_C}{C_C+C_X}\right)\int_{V_Q(0)}^{V_Q(t)} dV_Q \; dt\,. \tag{5.4}$$

The evaluation of the integral yields

$$V_X(t) = V_{REF} + m\left[V_Q(t) - V_Q(0)\right], \tag{5.5}$$

where $m = \frac{C_C}{C_C+C_X}$ represents the capacitance ratio and $V_{REF} = V_{DD} + V_{T,N}$.

5.3.2 Resistance of the proposed NP-load

The effect of capacitive coupling phenomenon was investigated in the previous subsection. For further analysis it is necessary to evaluate the resistance of the proposed NP-load. In CML gates, the output node makes a transition from V_{DD} to $V_{DD} - 0.5V_{SWING}$ or $V_{DD} - 0.5V_{SWING}$ to V_{DD} i.e. $V_{DD} > V_Q > V_{DD} - 0.5V_{SWING}$ where $V_{SWING} <= 2V_{T,N}$. The voltage at node X exceeds the power supply voltage atleast by $V_{T,N}$ therefore the transistor M1 operates in the linear region. Thus, the resistance of the proposed NP-load is calculated by using the standard BSIM3v3 MOSFET model parameters as

$$R_{NP} = \frac{R_{int}}{1-\frac{(R_{DSW}10^{-6})/W_N}{R_{int}}}, \tag{5.6}$$

where R_{DSW} is the empirical model parameter, W_N is the effective channel width of the transistor M1 and the parameter R_{int} is the intrinsic resistance of the NMOS transistor in the linear region and is given as

$$R_{int} = \left[\mu_{eff,n} C_{ox} \frac{W_N}{L_N}\left(V_{REF} - V_{DD} + 0.5V_{SWING} - V_{T,N}\right)\right]^{-1}, \quad (5.7)$$

where the parameters $V_{T,N}$ and L_N are the threshold voltage, and the effective channel length of the transistor M1 respectively. The proposed NP-load is used in the differential CML and PFSCL gates and the corresponding gates are referred to as MCML-CC and PFSCL-CC gates. The effect of the proposed NP-load on the performance of the gates is examined in the next section.

5.4 PROPOSED DIFFERENTIAL CML GATES WITH MODIFIED LOAD

The schematic of the proposed MCML-CC inverter is shown in Fig. 5.4. The PDN (M2-M3) and the current source (M1) is the same as in conventional CML inverter. The transistor (M4, M5) and (M6, M7) forms the NP-load. The operation, analysis and design of the MCML-CC inverter are described below.

5.4.1 Operation of the proposed MCML-CC inverter

The proposed NP-load behaves as a resistor as explained in section 5.3.2 therefore the operation of the proposed MCML-CC inverter remains same as that of a conventional CML inverter. However, the benefit of the proposed NP-load is visible during the switching event at the output node. For a low-to-high transition at the output node, the capacitive coupling occurs and a larger gate-to-source voltage is produced at node X than if the gate was

connected to a fixed potential thus verifying eqn. (5.5). This accelerates the charging process and results in the speed improvement.

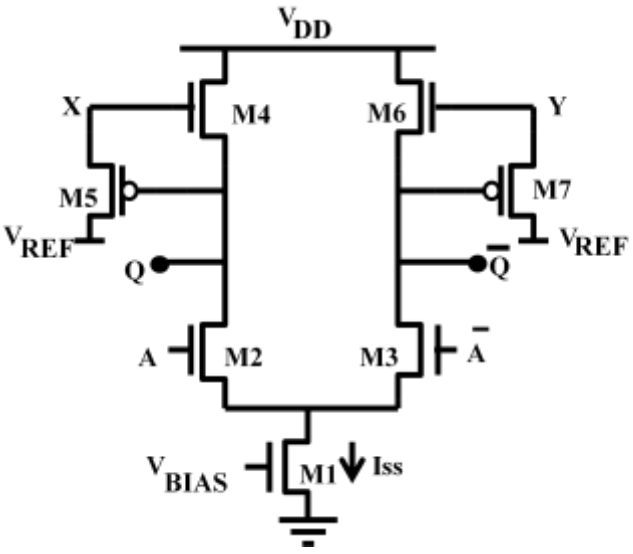


Fig. 5.4 Proposed MCML-CC inverter

5.4.2 Analysis of the proposed MCML-CC inverter

The proposed MCML-CC inverter is analysed in terms of static and delay parameters and are presented below.

5.4.2.1 Static Model

The static behavior is modeled in terms of voltage swing, small-signal voltage gain and the noise margin. The operation of the proposed MCML-CC inverter is similar to the differential CML inverter; therefore the static model can be derived by simply substituting the resistance of the proposed load expressed in eqn. (5.6) in the model detailed in section 2.3.2.1. The corresponding expressions are

- $V_{OH} = R_{NP}$, (5.8)
- $V_{OL} = -I_{SS} R_{NP}$, (5.9)

- $V_{SWING} = 2\, I_{SS} R_{NP}$, (5.10)

- $A_v = g_{m,n}\, R_{NP} = \frac{V_{SWING}}{2} \sqrt{\mu_{eff,n} C_{ox} \frac{W_N}{L_N} \frac{1}{I_{SS}}}$, (5.11)

- $NM = \frac{V_{SWING}}{2}\left(1 - \frac{\sqrt{2}}{A_v}\right)$, (5.12)

where $V_P = I_{SS}\, R_{NP}$ is defined as the potential drop across the load, and the symbols have their usual meaning.

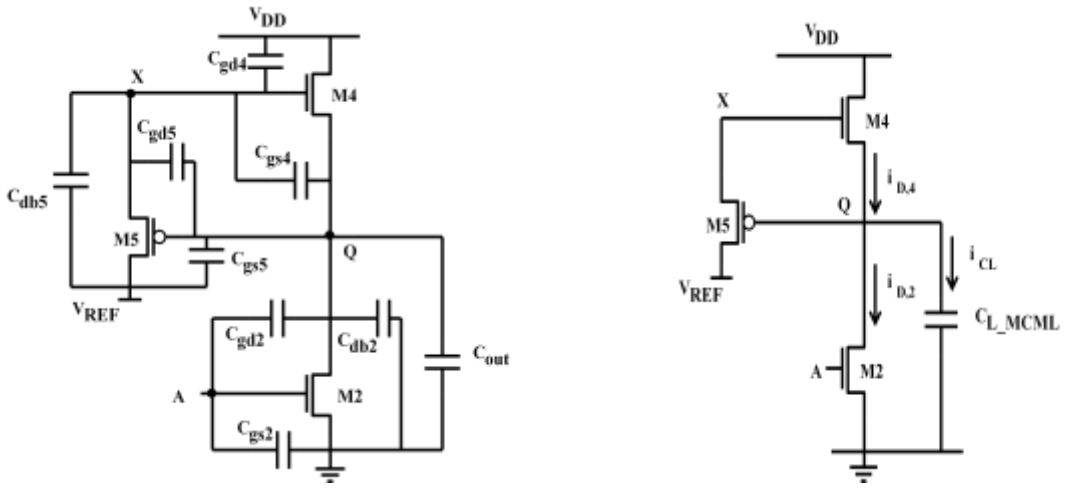
5.4.2.2 Delay Model

The delay of the proposed MCML-CC inverter is computed by solving the state equation of the output node in the time domain [5]. The half circuit of the proposed MCML-CC inverter with the parasitic capacitances of the transistors is shown in Fig. 5.5a where C_{out} represents the output capacitance that includes the interconnect capacitance and the input capacitance of the subsequent stage. The total capacitance at the output node C_{L_MCML} is shown in Fig. 5.5b which is computed as

$$C_{L\_MCML} = C_{gd2} + C_{db2} + C_{gs5} + C_{gd5} + C_{gs4} + C_{out}, \quad (5.13)$$

where C_{gdi}, C_{dbi} and C_{gsi} represents the gate-to-drain capacitance, drain-bulk capacitance and gate-to-source capacitance of the i^{th} (i = 2, 4, 5) transistor. The current through capacitor C_{L_MCML} is computed as the difference of drain currents flowing through the transistors M4 and M2 and may be written as

$$C_{L\_MCML} \frac{dV_Q}{dt} = i_{C_{L\_MCML}} = i_{D,4} - i_{D,2}\,, \quad (5.14)$$



(a) (b)

Fig. 5.5 Half circuit of the proposed MCML-CC inverter a) with different capacitances b) with total capacitance C_{L_MCML}

When the input switches from high to low logic level, the current through the transistor M2 becomes zero such that C_{L_MCML} begins to charge through the transistor M4. Thus, eqn. (5.14) reduces to

$$C_{L\_MCML}\,\frac{dV_Q}{dt} = i_{D,4}\,. \tag{5.15}$$

The rising output voltage initiates the process of capacitive coupling in the load circuit. It is clear from eqn. (5.5) that the gate potential of the transistor M4 remains greater than or equal to V_{REF} during the charging process, hence transistor M4 operates in linear region throughout the switching process. Therefore, the delay t_{PD} may be calculated by solving eqn. (5.15) as

$$t_{PD} = \int_{t_0}^{t_1} dt = C_{L\_MCML} \int_{V_0}^{V_1} \left(\frac{1}{i_{D,4}}\right) dV_Q. \tag{5.16}$$

Substituting $i_{D,4}$ results in

$$t_{PD} = \frac{2\,C_{L\_MCML}}{k_{n,4}} \int_{V_0}^{V_1} \left(\frac{1}{\left[2(V_X - V_Q - V_{T,N})(V_{DD} - V_Q) - (V_{DD} - V_Q)^2\right]} \right) dV_Q \,, \tag{5.17}$$

where $k_{n,4}$ is the transconductance of transistor M4

Substituting V_X from eqn. (5.5), the delay expression becomes

$$t_{PD} = \frac{2\,C_{L\_MCML}}{k_{n,4}} \int_{V_0}^{V_1} \left(\frac{1}{(V_{DD} - V_Q)\left[V_{DD} + (2m-1)V_Q - 2m\,V_Q(0)\right]} \right) dV_Q \,. \tag{5.18}$$

Evaluating the integral yields

$$t_{PD} = \frac{C_{L\_MCML}}{2k_{n,4}} \frac{1}{m(V_{DD} - V_{0)}} \ln \frac{V_{DD} + 2m(V_1 - V_0) - V_1}{V_{DD} - V_1} \,. \tag{5.19}$$

5.4.3 Design of the proposed MCML-CC inverter

The approach to design the proposed MCML-CC inverter for a given value of the bias current I_{SS} and the noise margin NM is presented. For a specified value of NM, and assuming A_v ($\geq$1.4 for differential CML gates [71]), the voltage swing is calculated using eqn. (5.12) as

$$V_{SWING} = \frac{2NM}{1 - \frac{\sqrt{2}}{A_v}} \,. \tag{5.20}$$

The voltage swing obtained from eqn. (5.20) requires sizing of the transistor M4, M6 with equivalent resistance R_{NP} $\left(= \frac{V_{SWING}}{2I_{SS}}\right)$. To this end, the equivalent resistance, R_{NP_MIN}, for the minimum sized NMOS transistor is first determined and then the bias current I_{HIGH} for the required voltage swing is determined as

$$I_{HIGH} = \frac{V_{SWING}}{2R_{NP\_MIN}}. \quad (5.21)$$

If the bias current is higher than I_{HIGH} , then R_{NP} should be less than R_{NP_MIN} and this is achieved by setting L_N to its minimum value i.e. L_{MIN} and W_N which is calculated by solving eqns. (5.6) and (5.7) as

$$W_N = \frac{2I_{SS}}{V_{SWING}} \frac{L_{MIN}}{\mu_{eff,n}C_{ox}(V_{REF}-V_{DD}+0.5V_{SWING}-V_{T,N})\left\{1-\frac{R_{DSW}10^{-6}}{L_{MIN}}[\mu_{eff,n}C_{ox}(V_{REF}-V_{DD}+0.5V_{SWING}-V_{T,N})]\right\}}. \quad (5.22)$$

Similarly, if the bias current is lower than I_{HIGH}, then R_N should be greater than R_{N_MIN} and this is achieved by setting W_N to its minimum value i.e. W_{MIN} and L_N which is calculated by solving eqns. (5.6) and (5.7) as

$$L_N = W_{MIN}\,\mu_{eff,n}C_{ox}\left(V_{REF}-V_{DD}+0.5V_{SWING}-V_{T,N}\right)\left(\frac{V_{SWING}}{2I_{SS}}-\frac{R_{DSW}10^{-6}}{W_{MIN}}\right). \quad (5.23)$$

The dimensions of the transistor M5 is set by following the simulation based approach for the given specification. The small-signal voltage gain (A_v) given in eqn. (5.11) is used to size transistors M2, M3. Assuming minimum channel length for the said transistors, the width is computed as

$$W_N = \frac{4}{\mu_{eff,n}C_{ox}}\left(\frac{A_v}{V_{SWING}}\right)^2 I_{SS}\,L_{MIN}\,. \quad (5.24)$$

Sometimes the eqn. (5.24) results in a value of W_N smaller than the minimum channel width. Therefore, in such cases, W_N is also set to W_{MIN}. This happens when the bias current

is lower than the current of the minimum sized NMOS transistor, I_{LOW} Using eqn. (5.11), I_{LOW} is given as

$$I_{LOW} = \frac{1}{4} \frac{W_{MIN}}{L_{MIN}} \mu_{eff,n} C_{ox} \left(\frac{V_{SWING}}{A_v}\right)^2. \quad (5.25)$$

The theoretical prepositions are validated through SPICE simulations with a power supply of 1.8 V. The proposed MCML-CC inverter is designed for A_v = 2, NM = 130 mV, I_{SS} = 100 µA and C_{L_MCML} = 50 fF. A plot of the simulated delay for various values of m is shown in Fig. 5.6. It is found out that the value of m = 0.6 results in minimum delay and therefore is chosen as the optimum value.

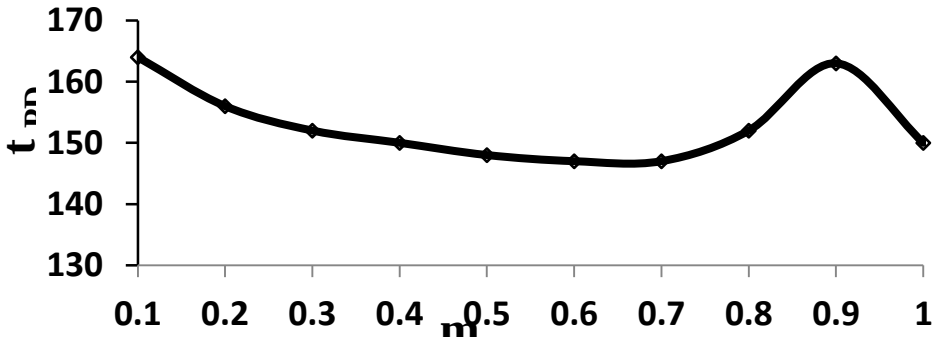


Fig. 5.6 Propagation delay vs. m for the proposed MCML-CC inverter

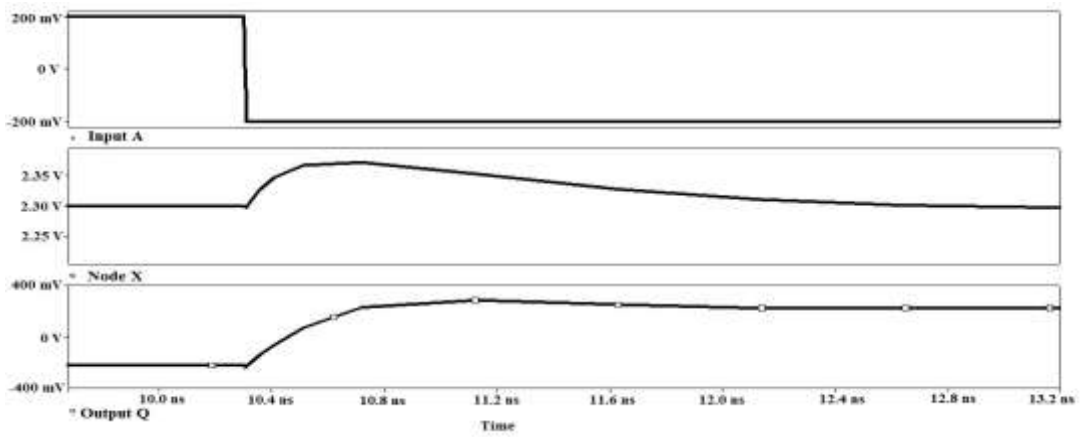
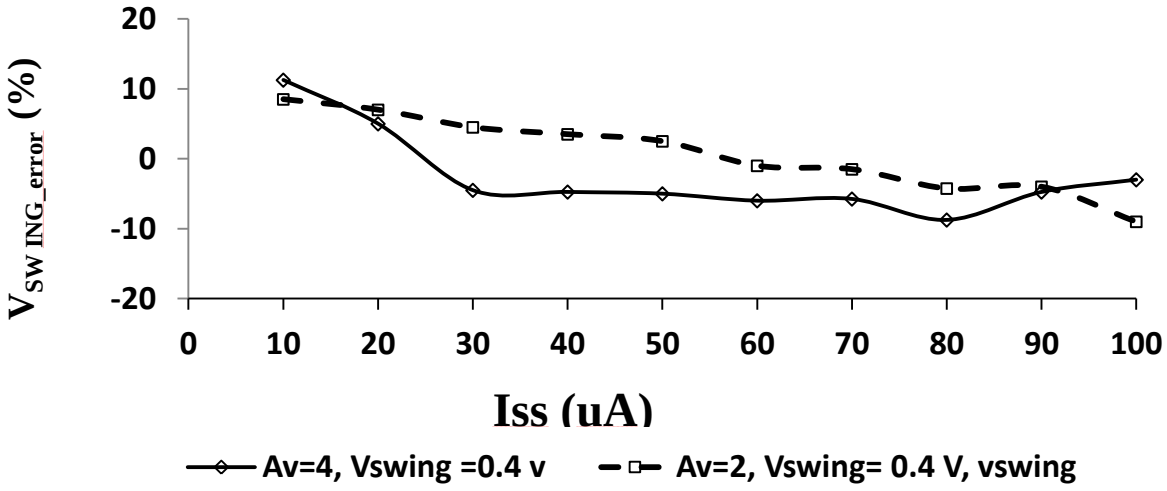


Fig. 5.7 Simulation waveforms of the different nodes in the proposed MCML-CC inverter

The behavior of the proposed MCML-CC inverter during the switching is verified through simulations for the above conditions. The simulated waveforms for the input A, node X, and output Q are shown in Fig. 5.7. It can be observed that a low to high transition at the output node Q subsequently results in an increased voltage of node X. This confirms the relation eqn. (5.5) between voltages at node Q and X.

The accuracy of the analytical model is verified by designing and simulating the inverter for wide range of operating conditions: - voltage swing of 400 mV and 800 mV, small-signal voltage gain of 2 and 4, and the bias current ranging from 10 µA to 100 µA. The error plots in the simulated values of static parameters with respect to the predicted values in particular for small-signal voltage gain of 2 and voltage swing of 400 mV are shown in Figs. 5.8a-c. It may be noted that maximum error in voltage swing, small-signal voltage gain and noise margin are 11 %, 13 % and 13 % respectively. It is found that there is a close agreement between the simulated and the predicted values of static parameters for all the operating conditions.



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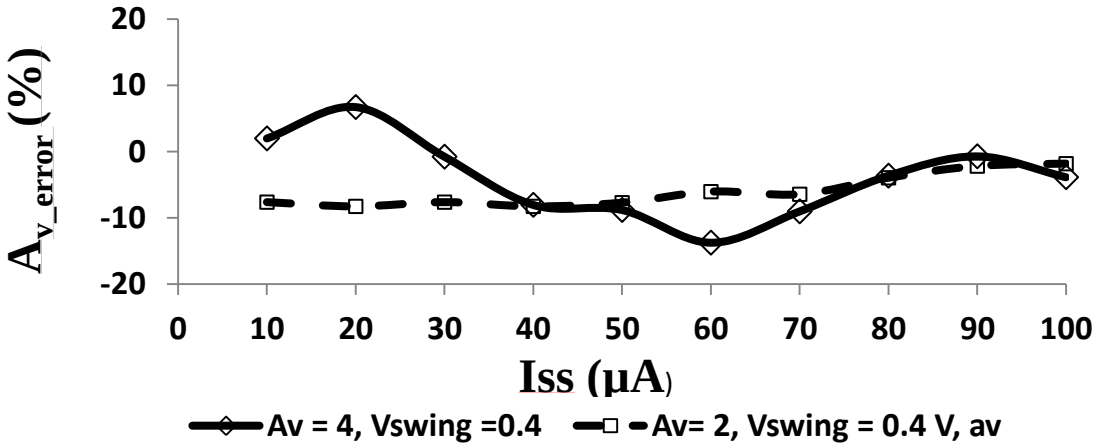

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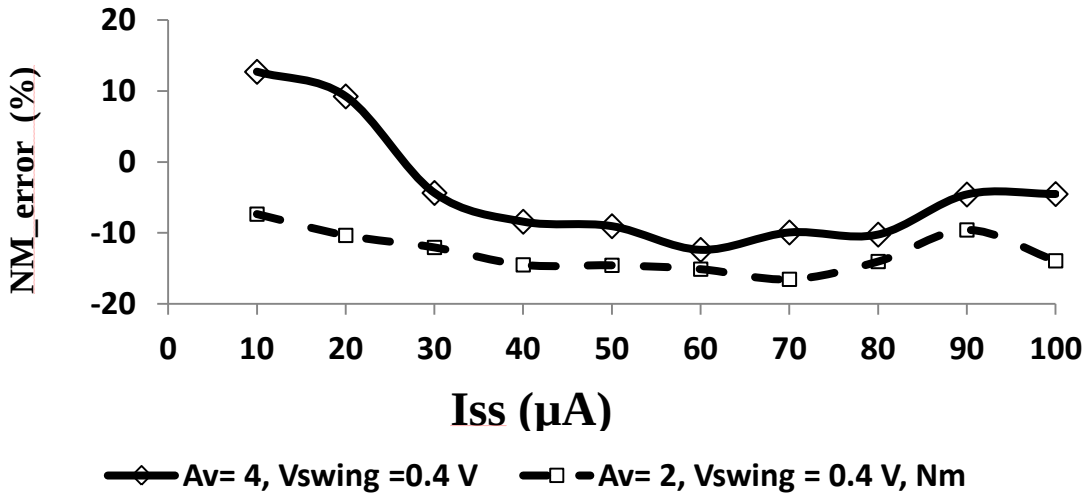
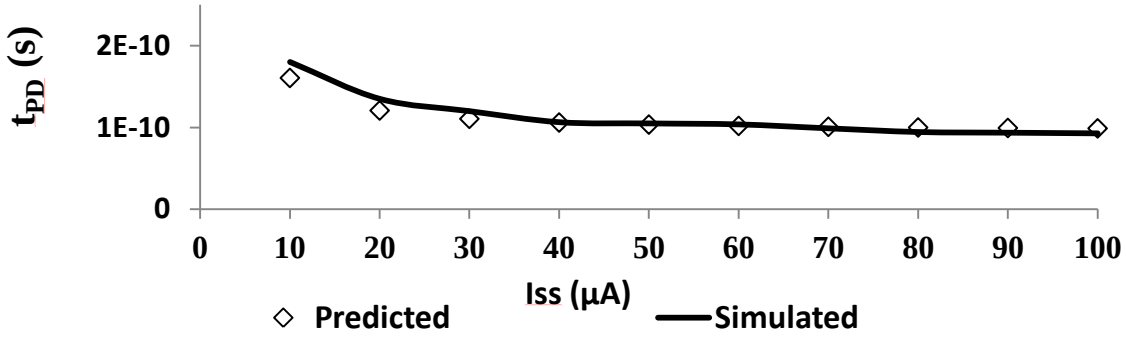


(c)

Fig. 5.8 Errors in the static parameters of the proposed MCML-CC inverter a) voltage swing b) small-signal voltage gain c) noise margin

The accuracy of the delay model for the proposed MCML-CC inverter is validated with load capacitance of 0 fF, 10 fF, 100 fF. The simulated and the predicted delay in particular for NM = 130 mV, A_v = 2 and with different load capacitances are plotted in

Fig. 5.9. There is a close agreement between the simulated and the predicted delay for all the operating conditions.



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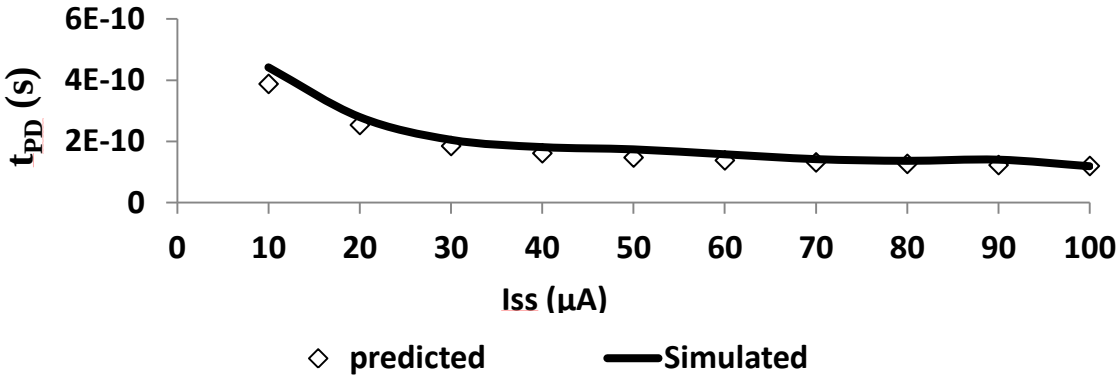

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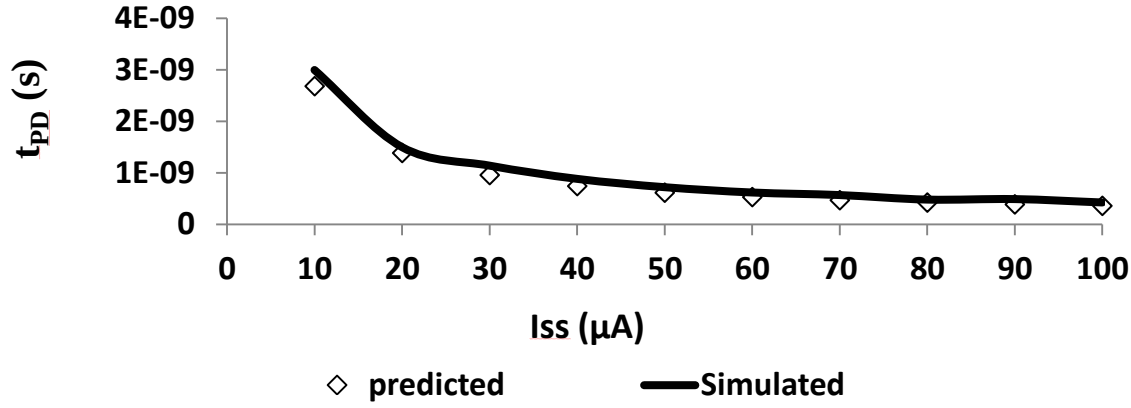


(c)

Fig. 5.9 Simulated and predicted delays of the proposed MCML-CC inverter vs. Iss with NM = 130 mV, $A_v = 2$ for different C_{L_MCML} values a) 0 fF b) 10 fF c) 100 fF

5.4.4 Performance Comparison

Several logic gates such as inverter, two input AND/NAND, 2:1 MUX, full adder and a D latch are implemented in the proposed MCML-CC style and conventional differential CML style with resistor, PMOS and the inductor (passive and the active inductor) as loads. All the gates operate with a power supply, bias current, noise margin and small-signal gain of 1.8 V, 100 µA, 130 mV and 4 respectively. It may be noted that since all the circuits are implemented with the same supply voltage and bias current therefore all of these consume same static power computed as the product of the supply voltage and bias current [27]. The simulated values for the delay are listed in Table 5.1. It can be observed that the passive inductor topology shows the maximum improvement in delay, followed by the proposed topology. The proposed MCML-CC gates show a maximum delay improvement of 21 % with respect to the conventional CML inverter having PMOS load.

Table 5.1 Comparison in propagation delay (ps) of differential CML circuits with different loads

Load / Circuit		Resistor	PMOS	Spiral Inductor	Active Inductor	Proposed NP-load
Inverter		142	148	122	140	135
AND/NAND		150	158	128	145	142
2:1 MUX		175	193	149	169	153
Full Adder	**Sum**	327	367	289	301	295
	Carry	332	381	290	322	301
D Latch		195	225	161	191	181

The impact of parameter variations is studied at different design corners for the inverters. The findings for various operating conditions are given in Table. 5.2. It is found that the propagation delay varies by a factor of 1.28, 1.29, 1.53, 1.41 and 1.31 for the resistive, PMOS, spiral inductor, active inductor and the proposed NP-load respectively between the best and the worst cases.

Table 5.2 Impact of parameter variations on propagation delay (ps) of the inverter with different loads

NMOS / PMOS / Load	**T T**	**F F**	**S S**	**F S**	**S F**
Resistor	142	125	160	149	148
PMOS	148	140	181	152	158
Spiral inductor	122	95	146	115	114
Active inductor	140	108	153	127	128
Proposed NP-load	135	101	140	122	125

5.5 PROPOSED PFSCL GATES WITH MODIFIED LOAD

The schematic of the proposed PFSCL-CC inverter is shown in Fig. 5.10. The PDN (M2-M3) and the current source (M1) are same as in conventional PFSCL inverter. The transistors (M4, M5) form the NP-load. The operation, analysis and design of the proposed PFSCL-CC inverter are discussed below.

5.5.1 Operation of the proposed PFSCL-CC inverter

The proposed NP-load behaves as a resistor as explained in section 5.3.2 so the operation of the proposed PFSCL-CC inverter remains the same as that of a conventional PFSCL inverter. However, the benefit of the proposed NP-load is visible during the switching event at the output node. For a low-to-high transition at the output node, the capacitive coupling occurs and a larger gate-to-source voltage is produced at node X than if the gate was connected to a fixed potential thus confirming the relation depicted in eqn. (5.5). This accelerates the charging process and results in the speed improvement.

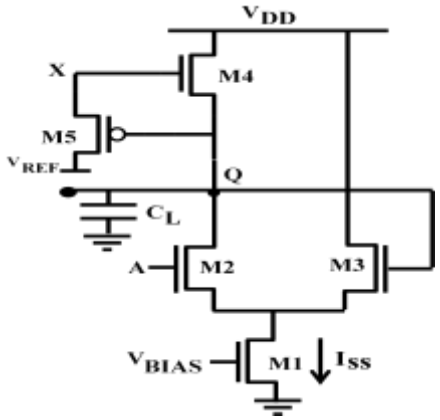


Fig. 5.10 Proposed PFSCL-CC inverter

5.5.2 Analysis of the proposed PFSCL-CC inverter

The proposed PFSCL-CC inverter is analysed in terms of static and delay model and is presented below.

5.5.2.1 Static Model

The static behavior is modeled in terms of voltage swing, small-signal voltage gain and the noise margin. As explained in section 5.5.1, the proposed PFSCL-CC inverter operates similar to the conventional PFSCL inverter consequently; the static model derived

for the conventional inverter can be used wherein the resistance of the proposed load given in eqn. (5.6) is substituted. The concern expressions are as follows

- $V_{OH} = V_{DD}$, (5.26)
- $V_{OL} = V_{DD} - V_P = V_{DD} - I_{SS} R_{NP}$, (5.27)
- $V_{SWING} = V_{OH} - V_{OL} = V_P = I_{SS} R_{NP}$, (5.28)
- $A_v = \frac{g_{m,n} R_{NP}/2}{1 - g_{m,n} R_{NP}/2}$, (5.29)
- $NM = \frac{V_{SWING}}{2} f\left(g_{m,n} R_P/2\right)$, (5.30a)

where function f is expressed as

$$f(x) = 2\sqrt{\frac{1}{2}(1 - 1/16x^2)\left(1 - \sqrt{1 - \frac{1-1/4x^2}{(1-1/16x^2)^2}}\right)}.\left[2\sqrt{1 - \frac{1}{2}(1 - 1/16x^2)\left(1 - \sqrt{1 - \frac{1-1/4x^2}{(1-1/16x^2)^2}}\right)} - \frac{1}{x}\right].$$

(5.30b)

The function f(x) represented in eqn. (5.30b) can be approximated by expression

$$f(x) = 1.4\,.\,x - 0.65\,. \quad (5.30c)$$

The above relation is valid for $x = g_{m,n} R_P/2 < 1$ whereas it exhibits hysteresis for values greater than 1.

5.5.2.2 Delay Model

The delay of the proposed PFSCL-CC inverter is computed by solving the state equation of the output node in the time domain [5]. The total capacitance at the output node C_{L_PFSCL} is shown in Fig. 5.11 and is computed as

$$C_{L\_PFSCL} = C_{gd2} + C_{db2} + C_{gs4} + C_{gd5} + C_{gs5} + C_{gd3} + 0.5C_{gs3} + C_{out}\,, \quad (5.31)$$

where C_{gdi}, C_{dbi} and C_{gsi} represents the gate-to-drain capacitance, drain-bulk capacitance and gate-to-source capacitance of the i^{th} (i = 2, 3, 4, 5) transistor and C_{out} accounts for the interconnect capacitance and the input capacitance of the subsequent stage. By neglecting the gate currents of transistor M3 and M5, the current through capacitor C_{L_PFSCL} may be written as

$$C_{L\_PFSCL}\frac{dV_Q}{dt} = i_{C_{L\_PFSCL}} = i_{D,4} - i_{D,2}\,, \tag{5.32}$$

where i_D represents the drain current of the transistor.

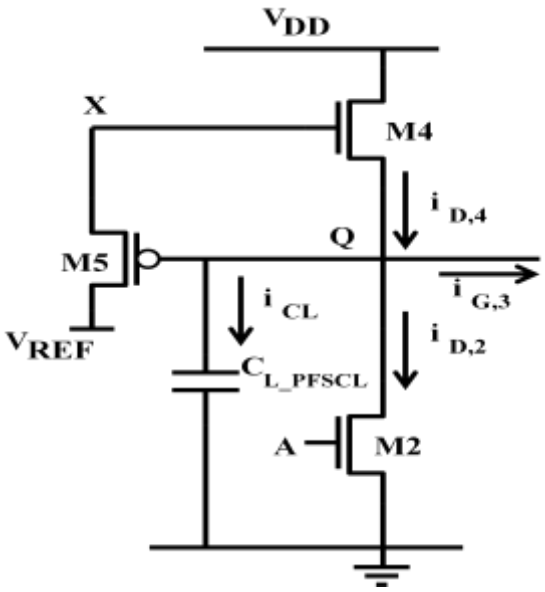


Fig. 5.11 Proposed PFSCL-CC inverter with load capacitance C_{L_PFSCL}

When the input switches from high-to-low logic level, the current through transistor M2 becomes zero such that C_{L_PFSCL} begins to charge through the load transistor M4. Thus, eqn. (5.32) reduces to

$$C_{L\_PFSCL}\frac{dV_Q}{dt} = i_{D,4}. \tag{5.33}$$

The rising output voltage initiates the process of capacitive coupling in the load circuit. It is clear from eqn. (5.5) that the gate potential of M4 remains greater than or equal to V_{REF} during the charging process, hence M4 operates in linear region throughout the switching process. Therefore, the delay t_{PD} may be calculated by solving eqn. (5.33) as

$$t_{PD} = \int_{t_0}^{t_1} dt = C_{L\_PFSCL} \int_{V_0}^{V_1} \left(\frac{1}{i_{D,4}}\right) dV_Q. \tag{5.34}$$

Substituting $i_{D,4}$ results in

$$t_{PD} = \frac{2\,C_{L\_PFSCL}}{k_{n,4}} \int_{V_0}^{V_1} \left(\frac{1}{\left[2(V_X - V_Q - V_T)(V_{DD} - V_Q) - (V_{DD} - V_Q)^2\right]}\right) dV_Q\,, \tag{5.35}$$

where $k_{n,4}$ is the transconductance parameter of transistor M4. Evaluating the integral by substituting V_X from eqn. (5.5) yields

$$t_{PD} = \frac{C_{L\_PFSCL}}{2k_{n,4}} \frac{1}{m(V_{DD} - V_0)} \ln \frac{V_{DD} + 2m(V_1 - V_0) - V_1}{V_1 - V_0}\,. \tag{5.36}$$

5.5.3 Design of the proposed PFSCL-CC inverter

The approach to design the proposed PFSCL-CC inverter for a given value of the bias current I_{SS} and the noise margin NM is presented. For a specified value of NM, and by assuming $g_{m,n} R_{NP}/2 = 1$, the voltage swing is calculated using eqn. (5.30) as

$$V_{SWING} = \frac{2NM}{f(1)} = 2.7\ NM. \tag{5.37}$$

The voltage swing obtained from eqn. (5.37) requires sizing of the load transistor with equivalent resistance R_{NP} $\left(= \frac{V_{SWING}}{I_{SS}}\right)$. To this end, the equivalent resistance, R_{NP_MIN}, for the

minimum sized NMOS transistor is first determined and then the bias current I_{HIGH} for the required voltage swing is determined as

$$I_{HIGH} = \frac{V_{SWING}}{R_{NP\_MIN}}. \tag{5.38}$$

If the bias current is higher than I_{HIGH} , then R_{NP} should be less than R_{NP_MIN} and this is achieved by setting L_N to its minimum value i.e. L_{MIN} and W_N which is calculated by solving eqns. (5.6) and (5.7) as

$$W_N = \frac{I_{SS}}{V_{SWING}} \frac{L_{MIN}}{\mu_{eff,n} C_{ox}(V_{REF}-V_{DD}+0.5V_{SWING} - V_{T,N})\left\{1-\frac{R_{DSW}10^{-6}}{L_{MIN}}[\mu_{eff,n} C_{ox}(V_{REF}-V_{DD}+0.5V_{SWING} - V_{T,N})]\right\}} . \tag{5.39}$$

Similarly, if the bias current is lower than I_{HIGH}, then R_N should be greater than R_{N_MIN} and this is achieved by setting W_N to its minimum value i.e. W_{MIN} and L_N which is calculated by solving eqns. (5.6) and (5.7) as

$$L_N = W_{MIN}\, \mu_{eff,n} C_{ox}\left(V_{REF} - V_{DD} + 0.5V_{SWING} - V_{T,N}\right)\left(\frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW}10^{-6}}{W_{MIN}}\right). \tag{5.40}$$

The small-signal voltage gain (A_v) represented in eqn. (5.29) is used to size transistors M2, M3. Assuming minimum channel length for the said transistors, $g_{m,n} R_{NP}/2 = 1$ and using eqn. (5.28), the width is computed as

$$W_N = \frac{4}{\mu_{eff,n} C_{ox}} \frac{I_{SS} L_{MIN}}{V_{SWING}^2}. \tag{5.41}$$

Sometimes the eqn. (5.41) results in a value of W_N smaller than the minimum channel width. Therefore, in such cases, W_N is also set to W_{MIN}. This happens when the bias current is

lower than the current of the minimum sized NMOS transistor, I_{LOW}. Using eqn. (5.41), I_{LOW} is given as

$$I_{LOW} = \frac{1}{4} \frac{W_{MIN}}{L_{MIN}} \mu_{eff,n} C_{ox} V_{SWING}^{2} . \quad (5.42)$$

The theoretical prepositions are validated through SPICE simulations with a power supply of 1.8 V. The proposed PFSCL-CC inverter is designed for A_v = 0.9, V_{SWING} = 400 mV, I_{SS} = 100 µA and C_L = 50 fF. A plot of the simulated delay for various values of m is shown in Fig. 5.12. It is found out that the value of m = 0.7 results in minimum delay and therefore is chosen as the optimum value.

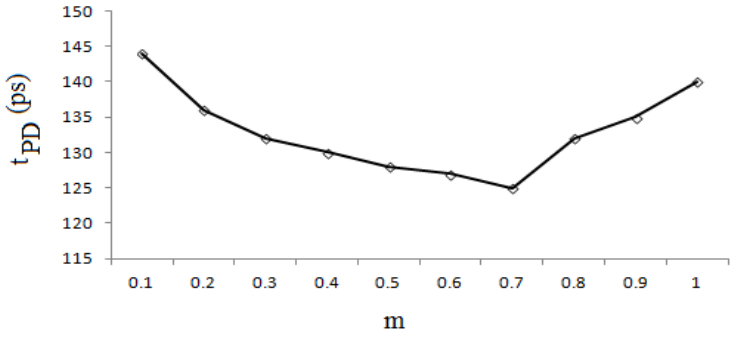


Fig. 5.12 Propagation delay vs. m for the proposed PFSCL-CC inverter

The behavior of the proposed PFSCL-CC inverter during the switching is verified through simulations for the above conditions. The simulated waveforms for the input A, node X, and output Q are shown in Fig. 5.13. It can be observed that the voltage of node X increases for a low-to-high transition at the output node Q thus confirming the relation expressed in eqn. (5.5).

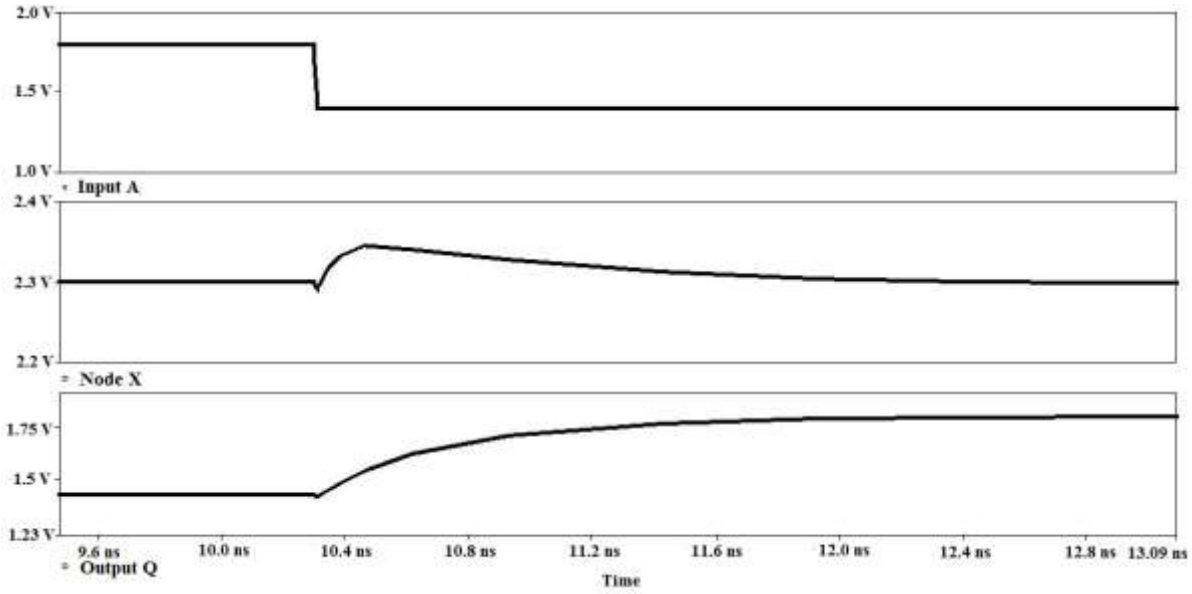
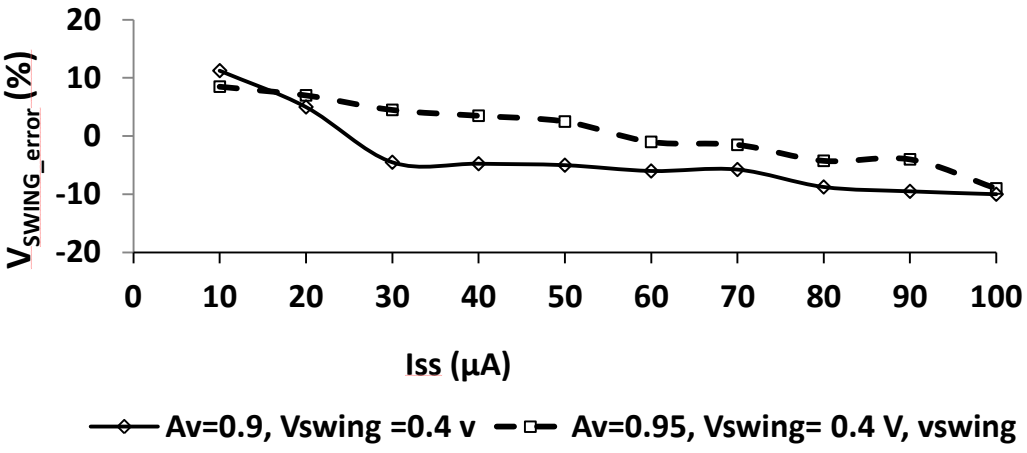
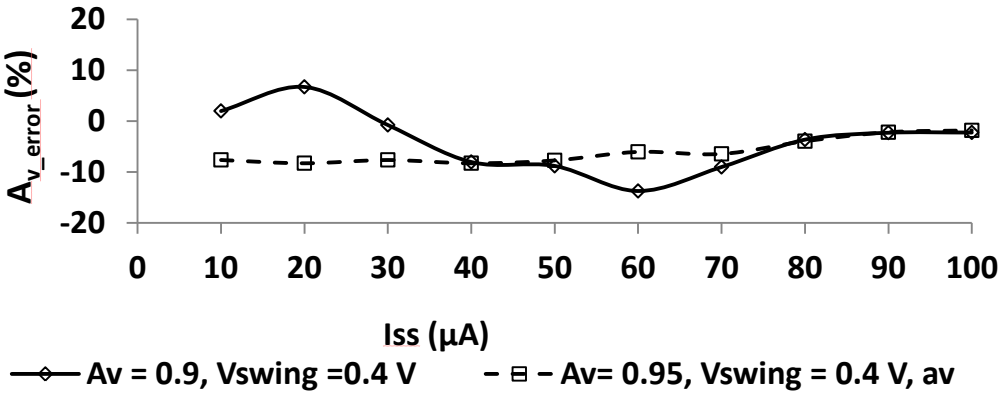


Fig. 5.13 Simulation waveforms of the proposed PFSCL-CC inverter

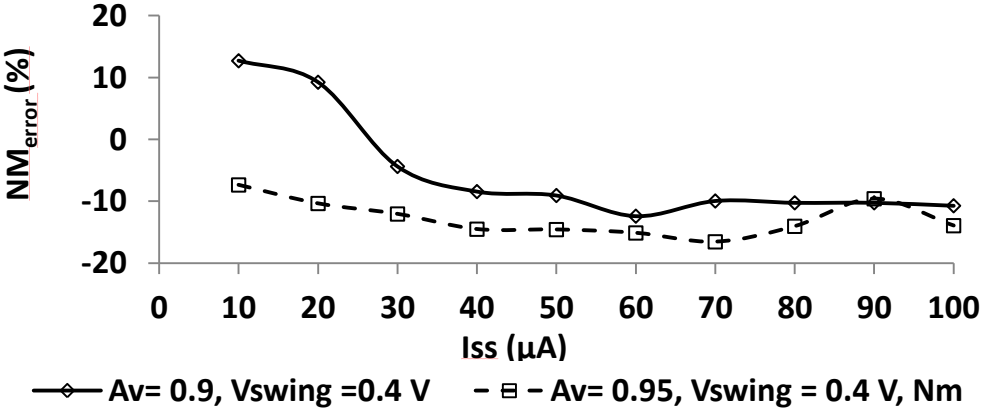
The accuracy of the analytical model is verified by designing and simulating the inverter for wide range of operating conditions: - voltage swing of 300 mV and 400 mV, small-signal voltage gain of 0.9 and 0.95, and the bias current ranging from 10 µA to 100 µA. The error plots in the simulated values of static parameters with respect to the predicted values in particular for small-signal voltage gain of 0.9, 0.95 and voltage swing of 0.4 V are shown in Figs. 5.13a-c. It may be noted that maximum error in voltage swing, small-signal voltage gain and noise margin are 12 %, 14 % and 13 % respectively. It is found that there is a close agreement between the simulated and the predicted values of static parameters for all the operating conditions.



(a)



(b)

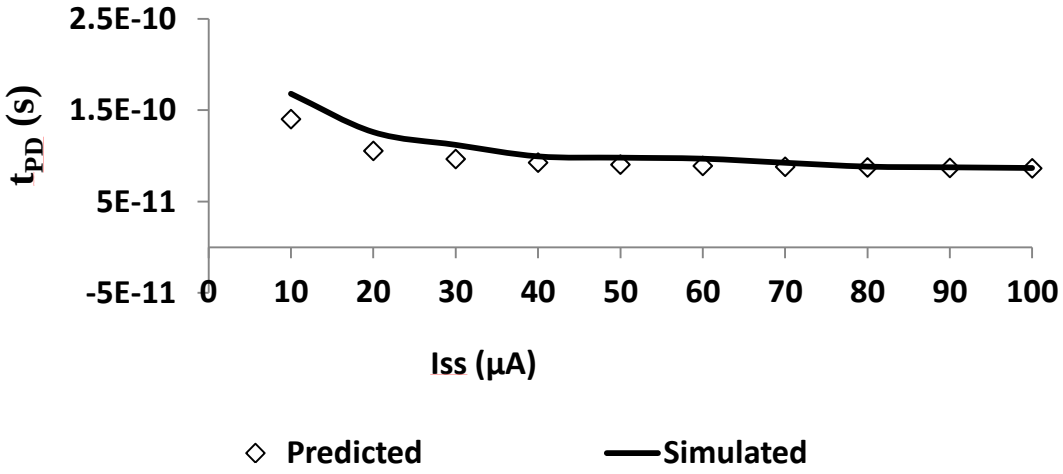


(c)

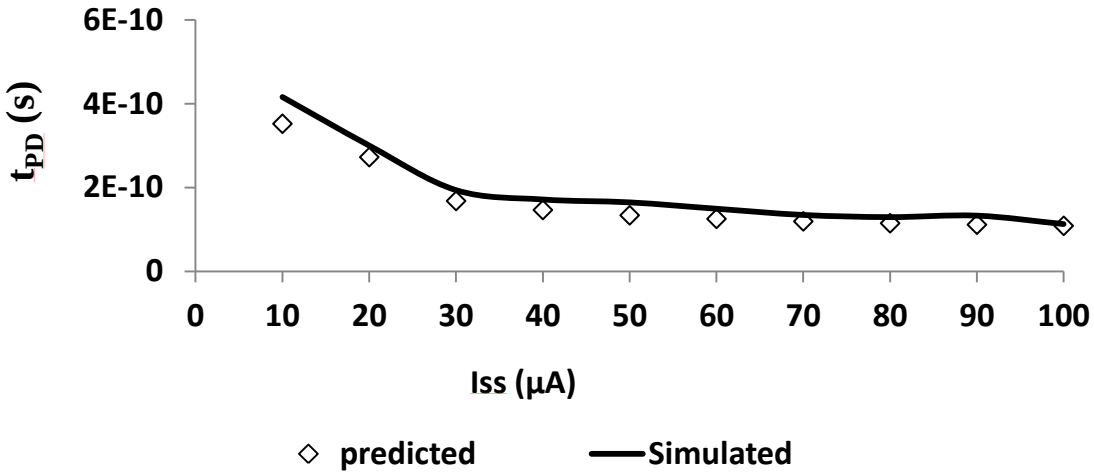
Fig. 5.14 Errors in the static parameters of the proposed PFSCL-CC inverter a) voltage gain b) small-signal voltage gain c) noise margin

The accuracy of the analytical model is verified by designing and simulating the inverter for wide range of operating conditions:- voltage swing of 300 mV and 400 mV, small-signal voltage gain of 0.9 and 0.95, and the bias current ranging from 10 µA to 100 µA. The error plots in the simulated values of static parameters with respect to the predicted values in particular for small-signal voltage gain of 0.9, 0.95 and voltage swing of 0.4 V are shown in Figs. 5.14a-c. It may be noted that maximum error in voltage swing, small-signal voltage gain and noise margin are 12 %, 14 % and 13 % respectively. It is found that there is a close agreement between the simulated and the predicted values of static parameters for all the operating conditions.

The accuracy of the delay model for the proposed PFSCL-CC inverter is validated with load capacitance of 0 fF, 10 fF, 100 fF. The simulated and the predicted delay in particular for NM = 130 mV, Av = 0.95 and with different load capacitances are plotted in Fig. 5.15. It is found that there is a close agreement between the simulated and the predicted delay for all the operating conditions.



(a)



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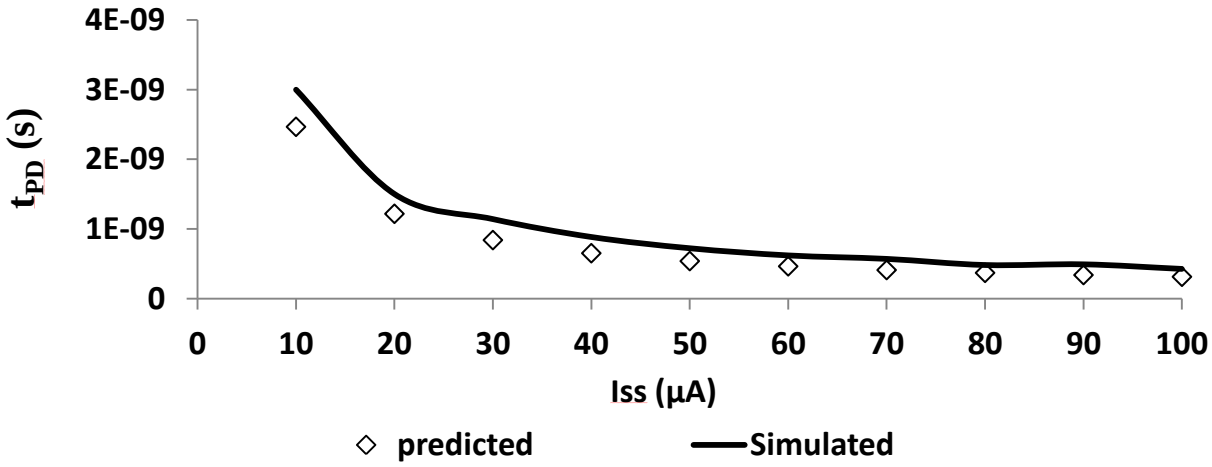


(c)

Fig. 5.15 Simulated and predicted delays of the proposed PFSCL-CC inverter vs. Iss with NM = 130 mV, A_v = 0.95 for different C_{L_PFSCL} values a) 0 fF b) 10 fF c) 100 fF

5.5.4 Performance Comparison

Several logic gates such as inverter, 2-input NOR, 3-input NOR, 2-input XOR, 3-input XOR gates are implemented in the proposed PFSCL-CC style and conventional PFSCL

style with a resistive, PMOS and the inductor (passive and the active inductor) loads. All the gates maintain a bias current of 100 μA and voltage swing of 0.4 V. The supply voltage of 1.8 V and a load capacitance of 50 fF are taken for simulations. It may be noted that since all the circuits are implemented with the same supply voltage and bias current therefore consume equal static power. The simulated delays for various gates with available and proposed load are listed in Table 5.3. It can be observed that the passive inductor topology shows the maximum delay improvement, followed by the proposed topology. A maximum improvement of 25 % with respect to the PMOS load is obtained in delay by using the proposed PFSCL-CC logic style.

The impact of parameter variations is studied at different design corners for the inverters with available and proposed loads. The findings for various operating conditions are given in Table 5.4. It is found that the propagation delay varies by a factor of 1.48, 1.29, 1.53, 1.33 and 1.36 for the resistive, PMOS, passive inductor, active inductor and the proposed load respectively between the best and the worst cases. It can be observed that the inverters employing passive components show slightly greater variation in comparison to ones with active loads.

Table 5.3 Comparison in propagation delay (ps) of PFSCL circuits with different loads

Load / Circuit	**Resistor**	**PMOS**	**Spiral Inductor**	**Active Inductor**	**Proposed NP-load**
Inverter	132	148	102	127	115
2-input NOR	143	158	108	135	122
3-input NOR	149	162	112	140	128

2-input XOR	163	193	139	159	144
3-input XOR	311	367	289	307	300

Table 5.4 Impact of parameter variations on propagation delay (ps) of PFSCL inverter with different loads

NMOS / PMOS / Load	**T / T**	**F / F**	**S / S**	**F / S**	**S / F**
Resistor	132	118	175	149	148
PMOS	148	140	181	152	158
Spiral inductor	102	95	146	115	114
Active inductor	127	115	153	127	128
Proposed NP-load	115	110	150	122	125

5.6 CONCLUDING REMARKS

In this chapter, the speed of the CML gates is improved by modifying its load section. A new active load without using any passive component is proposed. New differential and PFSCL topologies are developed and examined. It is observed that during the switching event at the output node of the developed gates, the capacitive coupling phenomenon occurs in the proposed load that results in the speed improvement. The phenomenon is analyzed in detailed and its effect on the delay of the inverter is modeled. The theoretical propositions are verified by designing and comparing the simulated results with the predicted ones for wide range of

operating conditions. A close agreement between the simulated and the predicted values for the static and delay parameters is observed. The impact of parameter variations is also studied on the proposed and existing topologies. In the last, the performance of the proposed topologies is compared with the existing ones. The comparison results indicate delay improvements in the proposed topologies.

6.1 INTRODUCTION

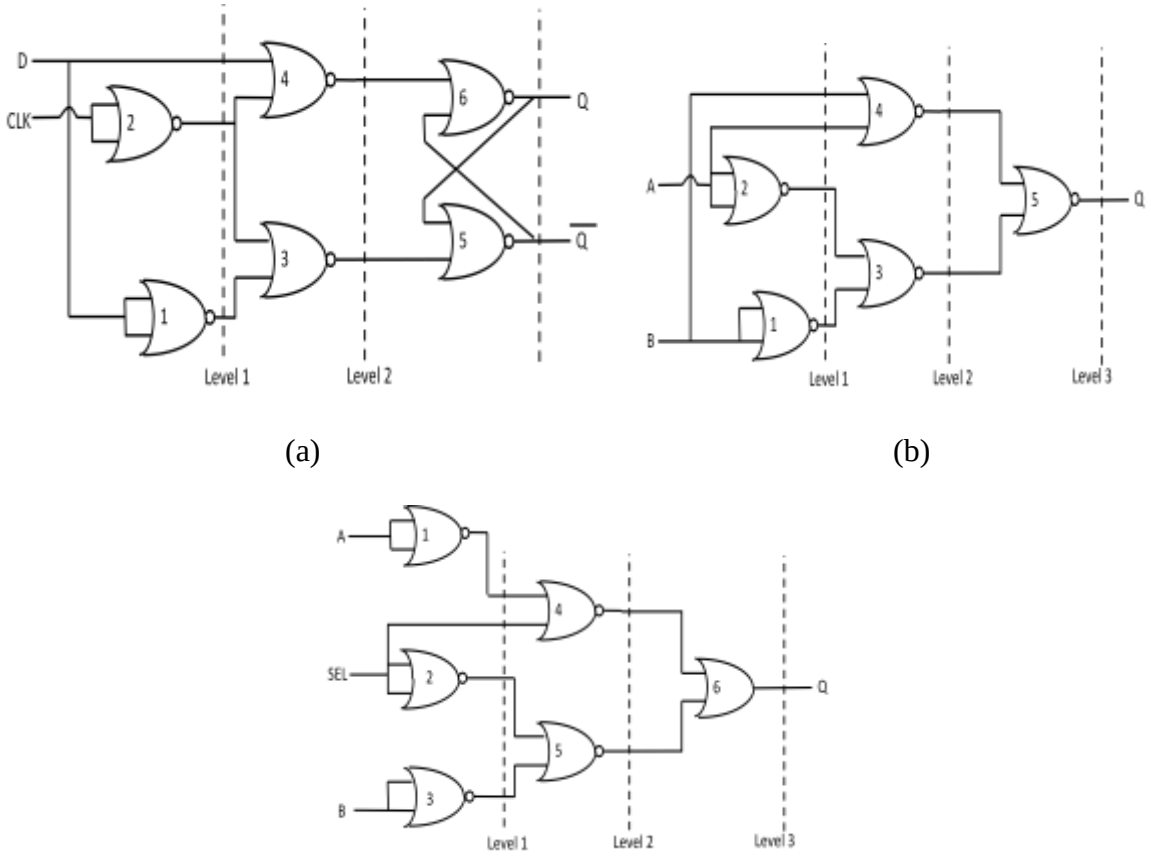
The basic architecture of PFSCL style allows implementation of NOR/OR functions in a single gate so that the stacking of the transistor pairs is not needed [34]. The value of minimum supply voltage in NOR/OR based topology is thus smaller than their stacked counterparts. Therefore, the NOR/OR based realization of PFSCL circuits is preferred and is referred to as conventional method in context of this chapter. The circuits implemented using the conventional method, in general consist of multiple PFSCL NOR/OR gates.

In this chapter, a new method to realize PFSCL circuits with reduced gate count in comparison to the conventional approach is presented. The proposed method introduces triple-tail cell concept in PFSCL style and presents a new fundamental cell. The operation of the fundamental cell is examined and its behavior is investigated. Thereafter, the realizations of PFSCL circuits by configuring the fundamental cell are discussed. The effectiveness of the proposed PFSCL circuit realizations is compared with the existing realizations in terms of the gate count, propagation delay and power consumption.

6.2 EXISTING REALIZATION OF PFSCL CIRCUITS

The conventional method for PFSCL circuit realization infers multiple NOR gates. To illustrate this, the realization of a D latch in PFSCL style is shown in Fig. 6.1a. It use six PFSCL NOR gates arranged in three levels (Level 1, Level 2 and Level 3). The first level (Level 1) generates the complement of the inputs and D latch is implemented in the next two levels (Level 2 and Level 3). The total power consumption of the latch is, therefore five times the power consumed by a single PFSCL NOR gate. Also, the arrangement of the NOR gates in three levels adds to the propagation delay. Similar, observations are made in the realization

of a XOR gate and 2:1 multiplexer (MUX) shown in Figs 6.1b, c. In this work, an alternate method that reduces the gate count in PFSCL circuit realization is proposed.



(a) (b)

(c)

Fig. 6.1 Gate level schematic to implement PFSCL circuits using conventional method a) D latch b) XOR gate c) 2:1 MUX

6.3 PROPOSED REALIZATION OF PFSCL CIRCUITS

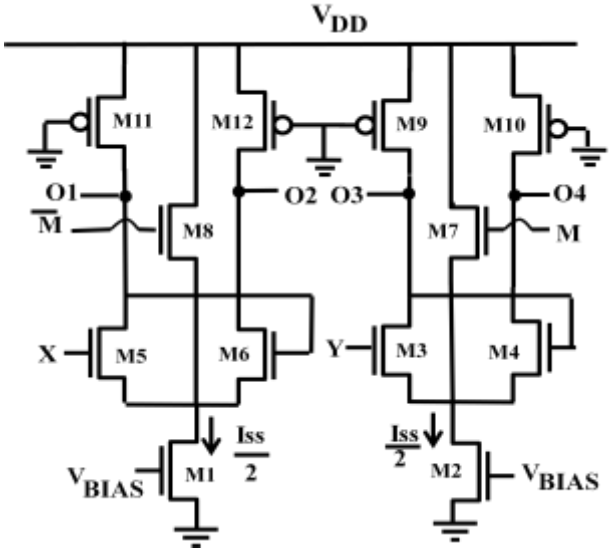
The method proposes the use of PFSCL inverter and a new fundamental cell in circuit realization. The new fundamental cell is examined first in this section, and its use in PFSCL circuits is elaborated later. The performance of the PFSCL circuits based on the proposed and the conventional methods are compared and the results are summarized.

6.3.1 Proposed Fundamental Cell

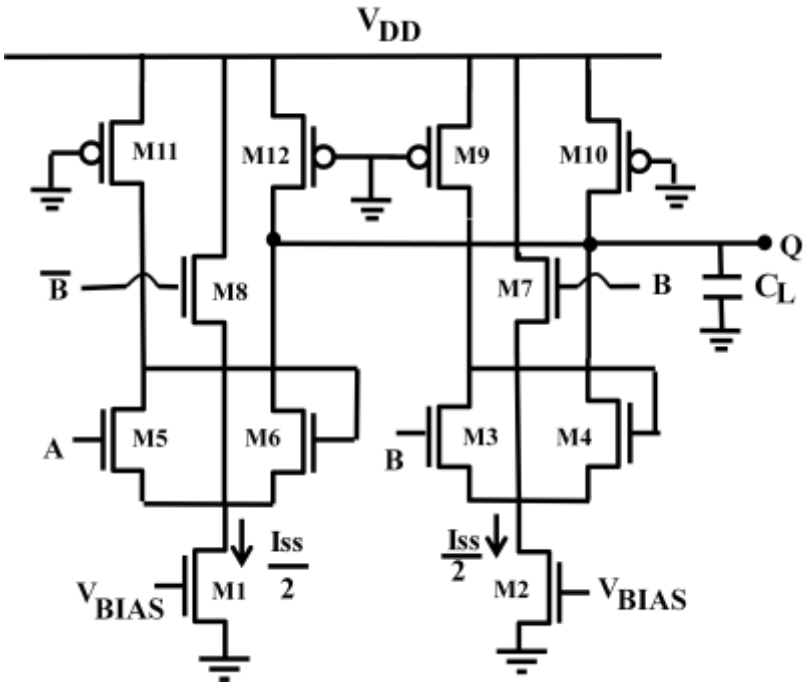
The triple-tail cell concept is introduced in conventional PFSCL style to develop the new fundamental cell. The architecture, operation and the analysis of the fundamental cell is presented by configuring it for AND functionality.

6.3.1.1 Architecture and operation

The proposed fundamental cell with inputs denoted as X, Y, M, and complement of M ($\bar{M}$) is shown in Fig. 6.2a. It employs two triple-tail cells (M3, M4, M7) and (M5, M6, M8) that are biased by separate current sources of $I_{SS}/2$ value such that the cell draws the same current as the basic PFSCL gate. The inputs Y, X, M and, $\bar{M}$ drive the transistors M3, M5, M7 and, M8 respectively. The transistors M7 and M8 are connected between the power supply and the common source terminal of transistor pairs (M3-M4) and (M5-M6) respectively. The output Q of the fundamental cell is formed by combining any one of the two output nodes from each of the two triple-tail cells (O1/O2, O3/O4).



(a)



(b)

Fig. 6.2 a) Proposed fundamental cell b) fundamental cell configured to realize AND functionality

The operation of the fundamental cell is explained by configuring it for AND functionality. The schematic is shown in Fig. 6.2b. The input A is connected to X, the input B is connected to Y and M and $\overline{B}$ is connected to $\overline{M}$. The output Q is taken by connecting nodes O2 and O4 to a load capacitance C_L. When the input B is high, the transistor M7 is ON and the transistor pair (M3-M4) is deactivated. At the same time, the transistor M8 is turned OFF and the input A is reflected at the output through the transistor pair (M5-M6). Similarly, a low voltage on B activates the transistor pair (M3-M4) and the output attains a low voltage level. Thus, the new fundamental cell configured as AND gate conforms to the functionality.

6.3.1.2 Analysis of the fundamental cell

The fundamental cell of Fig. 6.2b is analyzed in terms of voltage swing, small-signal gain and noise margin by using the pencil-and-paper approach.

It may be noted that if equal aspect ratio of all transistors (M3-M8) is assumed, then the transistors M7 and M8 will not be able to completely deactivate the transistor pair (M3-M4) and (M5-M6). To illustrate this point, consider the case when both the inputs are high, the transistors M3, M5 and M7 are ON while M4, M6 and M8 are OFF. A high-to-low transition at B makes the transistor M8 ON. In this condition the transistors M5 and M8 will draw equal currents as their gate-to-source voltages are same. Hence the transistor M8 is not able to completely deactivate the transistor pair (M5–M6). Therefore to achieve proper operation, the aspect ratio of transistors M7, M8 is made greater than other transistors' aspect ratio by a factor N. Thus, for the above case the currents flowing through the transistors M5 and M8 can be written as

$$i_{D,5} = \frac{I_{SS}}{2}\frac{1}{1+N}, \tag{6.1}$$

$$i_{D,8} = \frac{I_{SS}}{2}\frac{N}{1+N}. \tag{6.2}$$

Based on this observation, the output voltage for the different input combinations is derived below

Case 1: Both inputs (A and B) are high

When both the inputs are high, the transistors M3, M5, M7 are ON and the transistors M4, M6

and M8 are OFF. The current through the transistors M3 ($i_{D,3}$), M5 ($i_{D,5}$), M7 ($i_{D,7}$) may be written as

$$i_{D,3} = \frac{I_{SS}}{2}\frac{1}{1+N}, i_{D,5} = \frac{I_{SS}}{2}, i_{D,7} = \frac{I_{SS}}{2}\frac{N}{1+N}. \quad (6.3)$$

This input condition produces the high output voltage V_{OH} as

$$V_{OH} = V_{DD} - R_P\left[\left(i_{D,4} + i_{D,6}\right)\right] = V_{DD}, \quad (6.4)$$

where R_P is the resistance of the load transistors (M9-M12).

Case 2: Both inputs (A and B) are low

When both the inputs are low, the transistors M4, M6, M8 are ON and transistors M3, M5 and M7 are OFF. The current through the transistors M4 ($i_{D,4}$), M6 ($i_{D,6}$), M8 ($i_{D,8}$) may be written as

$$i_{D,4} = \frac{I_{SS}}{2}, i_{D,6} = \frac{1}{1+N}\frac{I_{SS}}{2}, i_{D,8} = \frac{I_{SS}}{2}\frac{N}{1+N}. \quad (6.5)$$

This input condition produces the low output voltage V_{OL1} as

$$V_{OL1} = V_{DD} - R_P\left[\left(i_{D,4} + i_{D,6}\right)\right] = V_{DD} - \frac{R_P I_{SS}}{2}\left(1 + \frac{1}{1+N}\right). \quad (6.6)$$

Case 3: A is high and B is low

For this input condition, the transistors M4, M5, M8 are ON and transistors M3, M6 and M7 are OFF. The current through the transistors M4 ($i_{D,4}$), M5 ($i_{D,5}$), M8 ($i_{D,8}$) may be written as

$$i_{D,4} = \frac{I_{SS}}{2}, i_{D,5} = \frac{1}{1+N}\frac{I_{SS}}{2}, i_{D,8} = \frac{I_{SS}}{2}\frac{N}{1+N}. \quad (6.7)$$

This input condition produces the low output voltage V_{OL2} as

$$V_{OL2} = V_{DD} - R_P\left[\left(i_{D,4} + i_{D,6}\right)\right] = V_{DD} - \frac{R_P I_{SS}}{2}. \quad (6.8)$$

Case 4: A is low and B is high

For this input condition, the transistors M3, M6, M7 are ON while the transistors M4, M5 and M8 are OFF. The current through the transistors M3 ($i_{D,3}$), M6 ($i_{D,6}$), M7 ($i_{D,7}$) may be written as

$$i_{D,3} = \frac{I_{SS}}{2}\frac{1}{1+N}, i_{D,6} = \frac{I_{SS}}{2}, i_{D,7} = \frac{I_{SS}}{2}\frac{N}{1+N}. \quad (6.9)$$

This input condition produces the low output voltage given by eqn. (6.8)

It may be observed that there are two values of low output voltage V_{OL1} given in eqn. (6.6) and V_{OL2} given in eqn. (6.8) resulting in the two values of the voltage swing given as

$$V_{SWING1} = V_{OH} - V_{OL1} = \frac{R_P I_{SS}}{2}\left(1 + \frac{1}{1+N}\right), \quad (6.10)$$

$$V_{SWING2} = V_{OH} - V_{OL2} = \frac{R_P I_{SS}}{2}. \quad (6.11)$$

For large values of N, the voltage swing V_{SWING} can be approximated as

$$V_{SWING} = \frac{R_P I_{SS}}{2}. \quad (6.12)$$

The small-signal voltage gain (A_v) and noise margin (NM) for the new fundamental cell are computed as

$$A_v = \frac{g_{m,n}R_P/2}{1-g_{m,n}R_P/2}, \quad (6.13)$$

$$NM = \frac{V_{SWING}}{2}\left[1 - \frac{1}{A_v}\right], \quad (6.14)$$

where $g_{m,n} = \sqrt{\mu_{eff,n} C_{OX} \frac{W_N}{L_N} \frac{I_{SS}}{2}}$ is the transconductance of the transistors (M3-M6) and W_N , L_N are the effective channel width and length of the said transistors respectively.

The expressions of A_v and NM represented in eqns. (6.13) and (6.14) respectively are valid for $g_{m,n}R_P/2 < 1$, the circuit exhibits hysteresis otherwise. To avoid large sizes of the transistors, the value of $g_{m,n}R_P/2$ values close to unity is recommended for designing of PFSCL circuits [37]. The DC behavior of the proposed fundamental cell is validated through SPICE simulations with a power supply of 1.1 V. The new fundamental gate was implemented and simulated for a voltage swing of 400 mV, N = 10, and the bias current of 100 µA. The voltage transfer characteristic (VTC) of the fundamental cell for $g_{m,n}R_P/2$ = 0.98 and $g_{m,n}R_P/2$ = 3 by varying the two inputs simultaneously are shown in Fig. 6.3 and Fig. 6.4 respectively. The simulation results conform to the theoretical propositions.

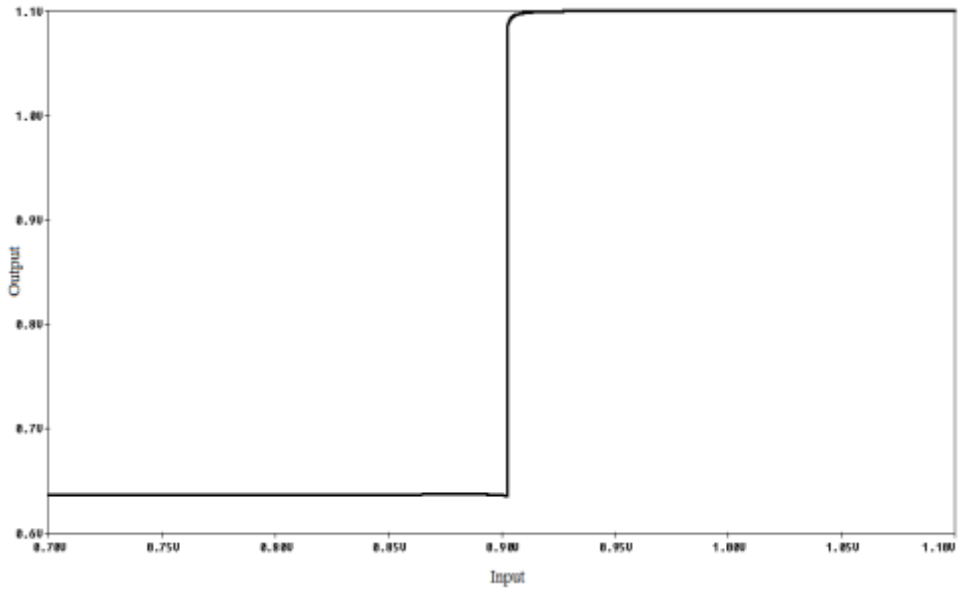


Fig. 6.3 VTC of the fundamental cell configured as AND gate ($g_mR_D/2$ = 0.98)

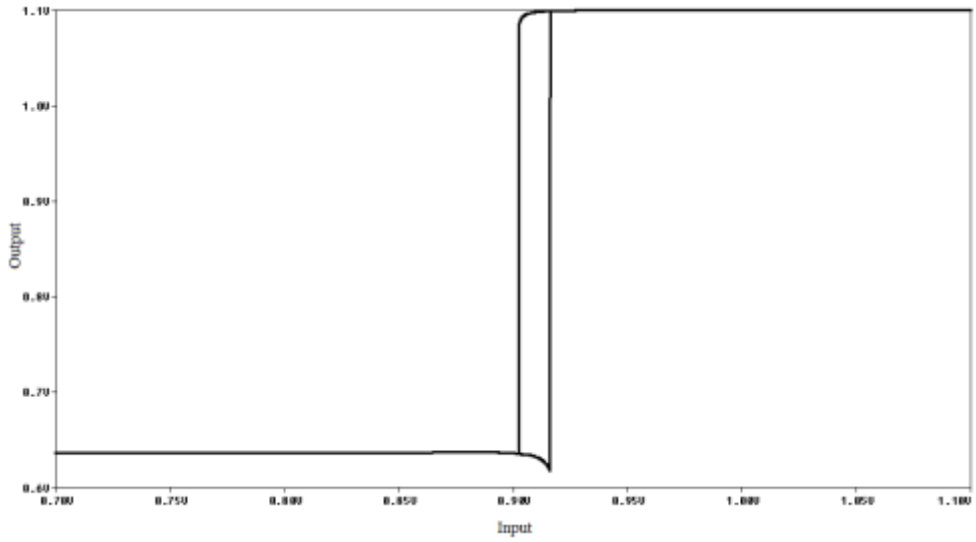


Fig. 6.4 VTC of the fundamental cell configured as AND gate ($g_mR_D/2 = 3$)

6.3.2 Realization of the PFSCL circuits

The operation of the fundamental cell suggests that a PFSCL inverter is required to invert one of the inputs for activation/deactivation of the two triple-tail cells. The proposed method therefore uses a cascade of PFSCL inverter and the fundamental cell for realizing PFSCL circuits. The block diagram illustrating the same is shown in Fig. 6.5.

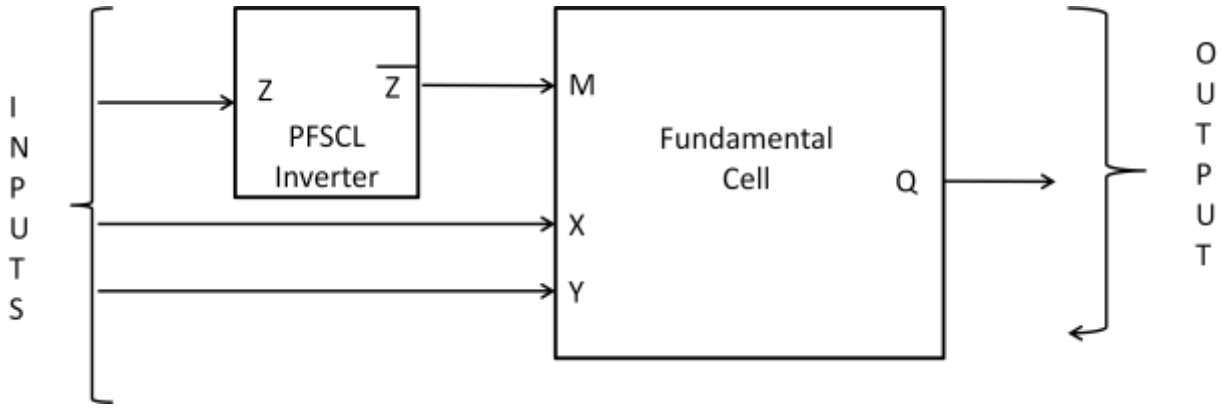


Fig. 6.5 Block diagram for realizing PFSCL circuits using the proposed method

To elaborate the proposed method, an implementation of a D latch as shown in Fig. 6.6 is considered. The PFSCL inverter (M13-M16) generates the complement of CLK which is fed as the input to the fundamental cell (M1-M12). The CLK and its complement $\overline{CLK}$ drives the transistors M7 and M8 connected between the supply terminal and the common source terminal of transistor pairs (M3-M4) and (M5-M6) respectively. A high voltage on CLK turns ON the transistor M7, and deactivates the transistor pair (M3-M4). At the same time, the transistor M8 turns OFF so that the transistor pair (M5-M6) generates the output according to the input D. Similarly, the transistor pair (M3–M4) gets activated for low voltage on CLK and preserves the previous output. Thus the proposed D latch models a positive level sensitive D latch.

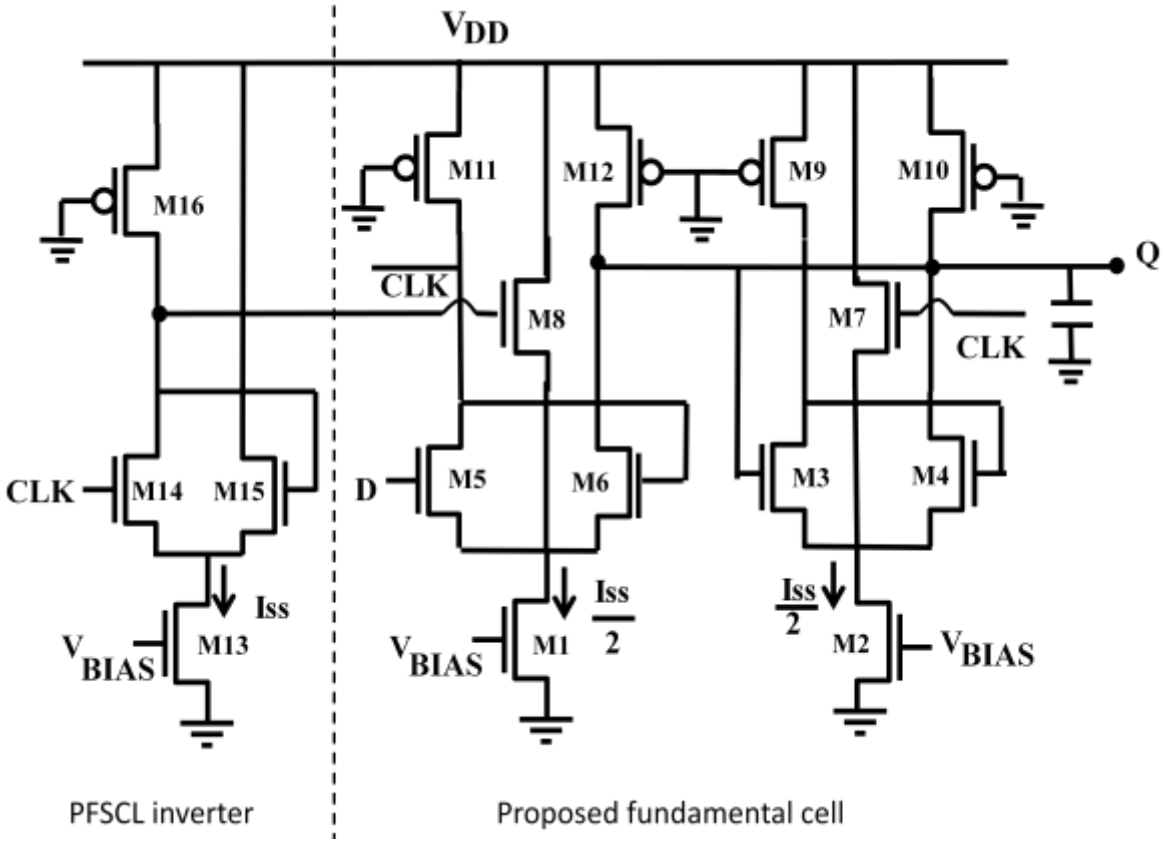


Fig. 6.6 Complete schematic of a PFSCL D latch using the proposed method

The functionality of the D latch is verified through simulations. A voltage swing of 400 mV and a bias current of 100 µA are considered. The simulation waveforms of the inputs (D and CLK), and the output node Q are shown in Fig. 6.7. It can be observed that for high values of the CLK signal, the D latch is in the transparent state whereas it is in the hold state for low values of the CLK signal.

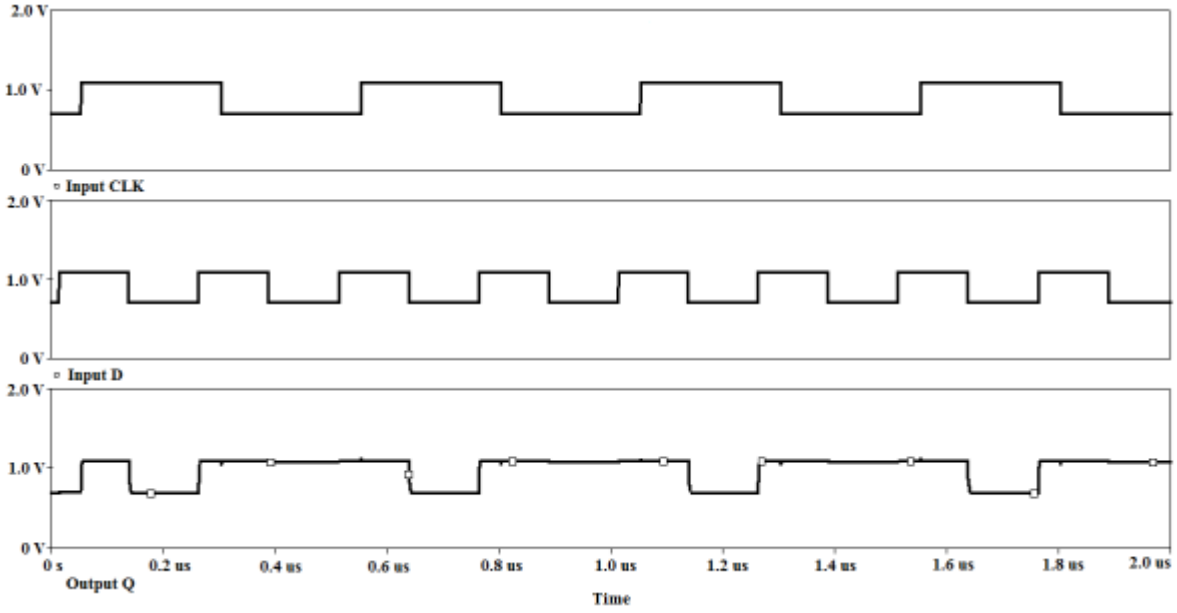


Fig. 6.7 Simulation waveform of a D latch

The PFSCL inverter and the new fundamental cell can be configured to realize different PFSCL circuits. The mapping of the actual circuit inputs to the inputs of the inverter and fundamental cell are listed in Table 6.1. Further, to illustrate the reduction in gate count, different PFSCL circuits are realized using the proposed and the conventional method and the respective gate count is summarized in Table 6.2. It may be noted that the NOR and OR circuits realized using the proposed method require more PFSCL gates in comparison to the conventional one due to the intrinsic nature of the later one. However, the realizations of NAND, AND, XOR, XNOR, 2:1 multiplexer and D latch using the conventional method

require three to six PFCSL gates in contrast to the one inverter and a fundamental cell in the proposed method. Thus, a reduction in the gate count is possible through the proposed method.

Table 6.1 Realization of PFSCL circuits using the proposed method

PFSCL circuit	**Actual Inputs**	**PFSCL inverter input**	**Fundamental cell inputs**			**Output nodes**
		Z	**M**	**X**	**Y**	**Q**
OR	A, B	B	B	A	A	O4, O2
NOR	A, B	B	B	A	A	O1, O3
NAND	A, B	B	B	A	B	O3, O1
AND	A, B	B	B	A	B	O4, O2
XOR	A, B	B	B	A	A	O1, O4
XNOR	A, B	B	B	A	A	O2, O3
2:1 MUX	SEL I_0, I_1	SEL	SEL	I_0	I_1	O2, O4
D-Latch	CLK, D	CLK	CLK	Q	D	O2, O4

Table 6.2 Comparison in the gate count

PFSCL circuit	**Conventional method**	**Proposed method**	**Percentage reduction**
OR	1	2	-50
NOR	1	2	-50
NAND	3	2	33
AND	3	2	33
XOR	5	2	60
XNOR	6	2	66
2:1 MUX	6	2	66
D-Latch	6	2	66

6.3.3. Performance Comparison

The effectiveness of the PFSCL circuits realized using the proposed method over the conventional one is demonstrated through SPICE simulations for a power supply of 1.1 V. A voltage swing of 400 mV and a bias current of 100 µA are considered.

The PFSCL circuits listed in Table 6.1 are simulated with the conditions specified above. The simulation results are summarized in Table 6.3. It is found that the NOR and OR circuits realized using the conventional method exhibits better performance than ones realized using the proposed one. This is can be attributed to the intrinsic nature of the former one. However, the realizations of NAND, AND, XOR, XNOR, 2:1 multiplexer and D latch using the proposed method lowers the power consumption by 64 % and delay by 48 % in comparison to the conventional method ones. Hence, the proposed method can be applied to implement efficient PFSCL circuits.

Table 6.3 Performance comparison of PFSCL circuits

Method	**PFSCL circuit**							
	OR	**NOR**	**AND**	**NAND**	**XOR**	**XNOR**	**2:1 MUX**	**D latch**
Power consumption (µW)								
Conventional	106	108	319	319	539	424	640	640
Proposed	228	228	228	228	228	228	228	228
Propagation delay (ps)								
Conventional	563	648	710	720	1135	1119	1139	1270
Proposed	682	688	615	633	661	653	655	658
Power Saving (%)								
Proposed	-53.5	-52.6	29	29	58	46	64	63
Speed Improvement (%)								
Proposed	-21	-6	13	12	41	41	42	48

The impact of parameter variations on PFSCL D latch realized using the proposed and the conventional methods is also studied and the findings are comprehended in Table 6.4.

It is found that the propagation delay and the power of the proposed D latch vary by a factor of 1.5 and 1.8 respectively between the best and the worst cases whereas a factor of 1.43 and 1.9 respectively are obtained for the conventional PFSCL D latch. Similar results are obtained for other PFSCL circuits and are not included for the sake of brevity.

Table 6.4 Impact of parameter variations on the PFSCL D latch realized using the proposed and the conventional method

Parameter	NMOS / PMOS	T / T	F / F	S / S	F / S	S / F
Propagation delay(ps) (C_L = 100 fF)	**Proposed**	658	628	953	631	640
	conventional	1270	1036	1489	1203	1240
Power (µW)	**Proposed**	228	283	158	261	256
	conventional	633	846	438	642	635

where different design corners are denoted by T = Typical, F = Fast, S = Slow

6.4 CONCLUDING REMARKS

A new method to realize PFSCL circuits is presented in this chapter. The proposed realization has lower gate count in comparison to the existing realizations. It uses a PFSCL inverter and a new fundamental cell. The new fundamental cell introduces the triple-tail cell concept in PFSCL style. A detailed analysis of the fundamental cell configured as AND function is carried out and its use to implement various PFSCL circuits is demonstrated. The performance of the proposed circuit realizations is compared with the existing ones in terms of the gate count, power consumption and the propagation delay. It is found that for single gate NOR/OR functions, the PFSCL circuit based on the conventional method are advantageous. Conversely, the cases where the conventional method requires high gate

count, the proposed realizations shows a reduction of 64 % and 48 % in the power consumption and delay values respectively. Hence it is expected that the proposed method for PFSCL circuit realizations will provide an efficient design option to designers.

7.1 INTRODUCTION

Tri-state circuits are the essential elements in bus organized systems such as high performance processors, asynchronous transfer mode (ATM) crossbar switches, and programmable logic devices [119-122]. These circuits can be easily designed using CMOS logic style [5] but are not favoured at high frequencies due to the large switching noise generation and substantial power consumption. Therefore, tri-state CML circuits are preferred in applications operating at high frequencies. The chapter first reviews the two available tri-state CML circuit implementations [101]. Thereafter, the power issue in the available ones is identified and a new low power tri-state CML circuit is proposed. The performance of the proposed tri-state CML circuit is compared with the available ones and applications are included to demonstrate their practical use.

7.2 LITERATURE SURVEY ON TRI-STATE CML CIRCUITS

A tri-state gate assumes a high-impedance state in addition to high and low logic levels attained by a regular gate. An additional Enable signal is employed to achieve the desired functionality. In literature, two circuits for differential tri-state CML inverter/buffer are presented and are briefly reviewed in following subsections.

7.2.1 Switch based tri-state CML circuit

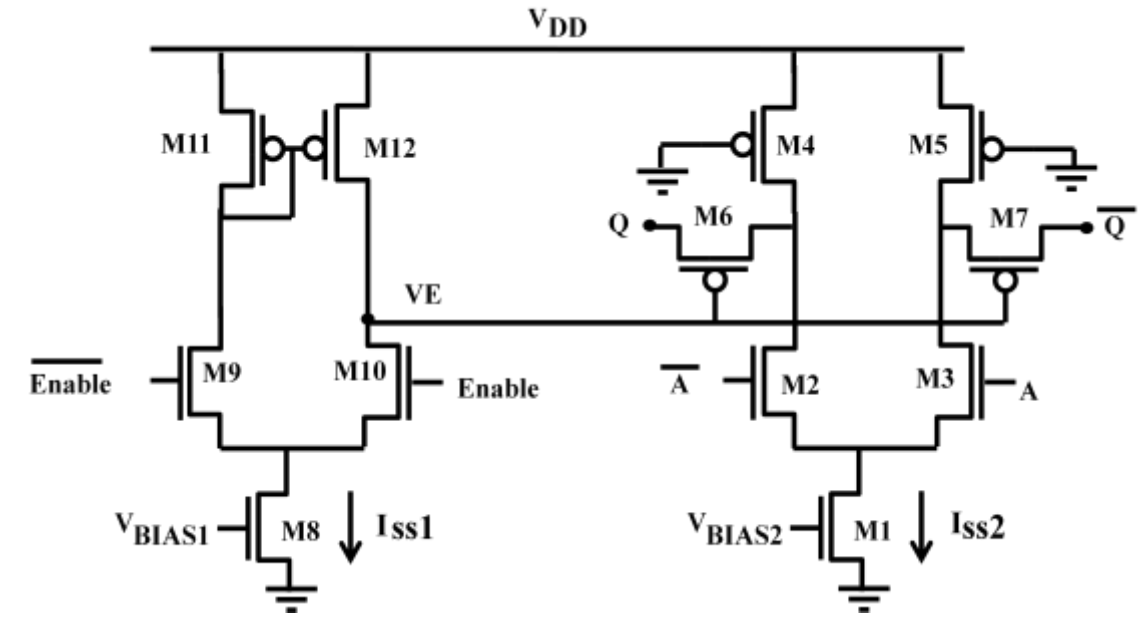
The complete schematic of a switch based tri-state CML inverter/buffer [101] is shown in Fig. 7.1a. The circuit is fully differential in nature and consists of a conventional CML inverter/buffer (M1-M5), two PMOS transistor (M6-M7) and a differential to single

ended converter (M8-M12). The reduced swing differential Enable signal is converted to a full swing VE signal by the converter. For a high value of the Enable signal, the VE signal attains a low voltage such that the PMOS transistors M6, M7 turns ON and the circuit behaves as a regular CML inverter/buffer. Conversely, a low on Enable signal makes VE signal high which turns the PMOS transistors M6, M7 OFF and a high-impedance state is achieved at the output. It may be noted that a constant current is maintained in the circuit during the high-impedance state as both the current sources (M1 and M8) are always ON.

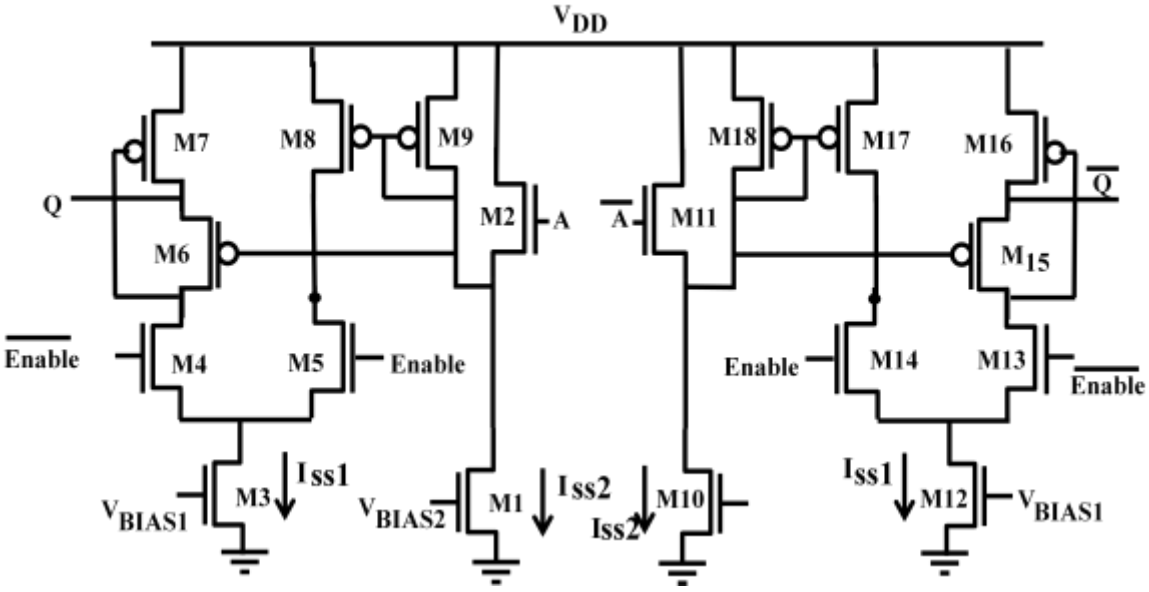
7.2.2 Voltage follower based tri-state CML circuit

The complete schematic of the voltage follower based tri-state CML inverter/buffer [101] is shown in Fig. 7.1b. It is pseudo-differential in nature and consists of cascade of source follower (M1-M2 and M10-M11) and flipped voltage follower (M6-M7 and M15-M16). The circuit behaves as an inverter for low value of differential Enable signal. For high value of Enable, the inverter/buffer is in the high-impedance state as the transistors M4, M7, M13 and M16 are OFF. In this state, the power is consumed due to the fact that the current sources M1, M3, M10 and M12 remain always ON.

It can be observed that all the current sources remain ON irrespective of being in the high-impedance or enabled state in the existing circuits. Therefore, in bus based systems wherein only one inverter/buffer out of many is active at a given instant, the existing circuits will result in significant power consumption. Hence, there is a need for low power tri-state CML circuits.



(a)



(b)

Fig. 7.1 Existing differential tri-state CML inverter/buffer [101] a) switch based b) voltage follower based

7.3 PROPOSED DIFFERENTIAL TRI-STATE CML CIRCUIT

In this section, a new low power differential tri-state CML circuit is proposed. The circuit and its operation are described first and are followed by the performance comparison with the existing ones in the following subsections. Two applications using the proposed tri-state buffer are also developed in the section.

7.3.1 Operation of the proposed circuit

The complete schematic of the proposed differential tri-state CML inverter/buffer is shown in Fig. 7.2. It uses a differential CML inverter/buffer (M1-M7) with Enable controlled load and the current source sections and a differential to single ended converter (M8-M12). The differential Enable signal is applied to the converter which generates a full swing VE signal that enables the load transistors M4, M5 and also controls the operation of current source M1 via transistors M6 and M7.

When VE is low, the transistors M4 and M5 are turned ON and act as load to the inverter/buffer. At the same time, the transistor M6 charges node X to the potential V_{BIAS2} since the transistor M7 is OFF. Thus, the transistor M1 works as a current source and provides the bias current I_{SS2} to the buffer. Therefore, for low value of VE signal, the proposed circuit behaves as a regular differential CML inverter/buffer. For high value of VE signal, the transistors M4, M5 and M6 are turned OFF whereas the transistor M7 conducts and pulls down the node X to the ground potential. Thus the output nodes are disconnected from the power supply as well as ground and a high-impedance is obtained at the output of the inverter/buffer.

It may be noted that during the high-impedance state, the current source M1 is OFF in contrast to the existing tri-state CML inverters/buffers (Fig. 7.1) where all the current sources

remain in ON state. Thus, the proposed circuit has reduced power consumption in comparison to the existing ones.

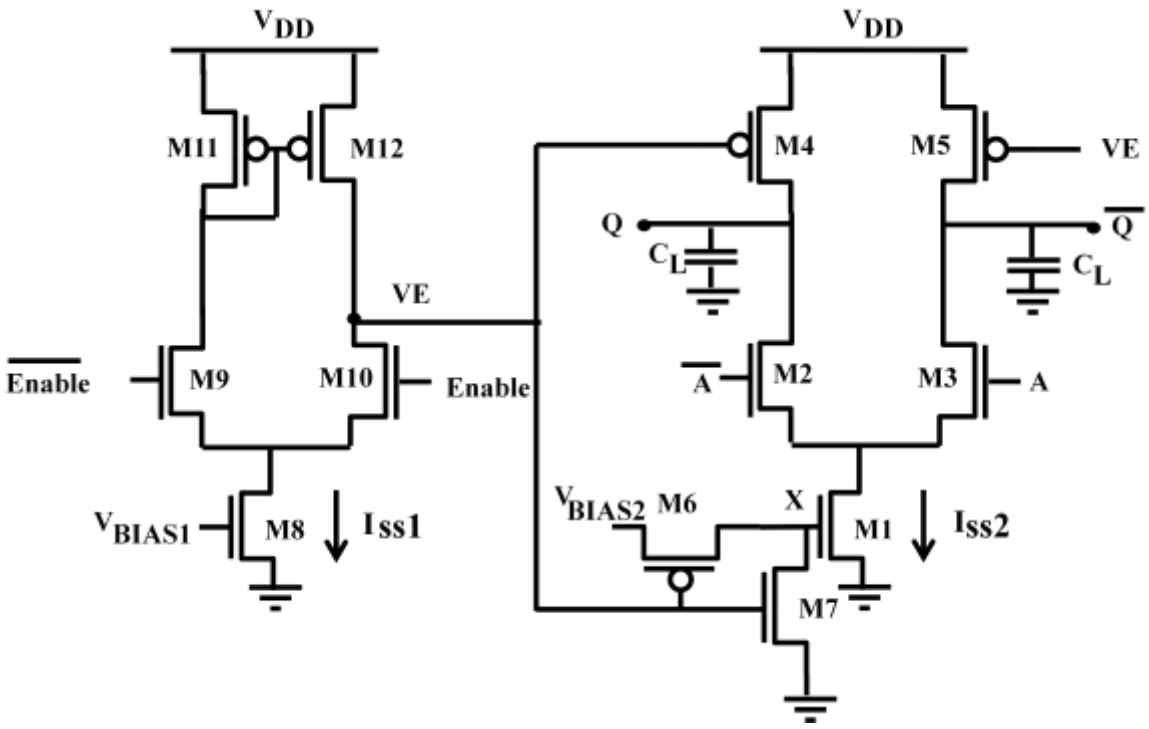


Fig 7.2 Proposed differential tri-state CML inverter/buffer

7.3.2 Performance Comparison

A performance comparison of the proposed tri-state buffer (Fig. 7.2) with existing tri-state buffers (Fig. 7.1) is carried out through SPICE simulations with a power supply of 1.8 V. The buffers maintain a bias current of 100 µA, voltage swing of 400 mV, and a load capacitance of 100 fF is connected at the output. A summary of the simulation results for different timing parameters, power consumption, and PDP is listed in Table 7.1. It may be observed that both the existing differential tri-state CML buffers consume more power than the proposed tri-state buffer. This is due to the fact that in the existing tri-state buffers all the current sources remain ON in the enabled as well as in the high-impedance state whereas in

the proposed circuit some of the current sources are OFF in the high-impedance state. Also, the proposed tri-state buffer has lowest the PDP value, thus making it power efficient than the existing ones.

Table 7.1 Summary of the simulation results for different tri-state CML buffers

Parameter	**Switch based [101]**	**Voltage follower based [101]**	**Proposed**
Power (μW)	435	435	308
Propagation Delay (ps)	481	348	340
Output Enable Time (ps)	1075	1052	1062
Power Delay Product (fJ)	209	151	104

7.3.3 Application Examples

In this section, few applications to demonstrate the practical use of the proposed tri-state CML inverter/buffer are developed.

Application 1: Bus System Implementation

The CML gates are extensively used in the design of complex circuits in microprocessors. Their use can be further extended to implement bus architectures wherein all the modules receive data at the same time, but only one of them transmit the data over the bus at a particular instant of time and the others remain disconnected from the bus. This can be achieved by either multiplexing of the transmitters or by using open-drain or tri-state circuits [101]. The multiplexer based method connects all the transmitters to a multiplexer, and thus requires all transmitters to physically reside on the same location in a chip [101].

The second method of employing open-drain circuits require a pull up network is therefore convenient for point-to-point communication, wherein the receiver implements the pull-up network [101]. The last method using tri-state circuits do not need any particular consideration, except that only one should be enabled at any given time. Therefore, bus system implemented using tri-state buffers are preferred [101].

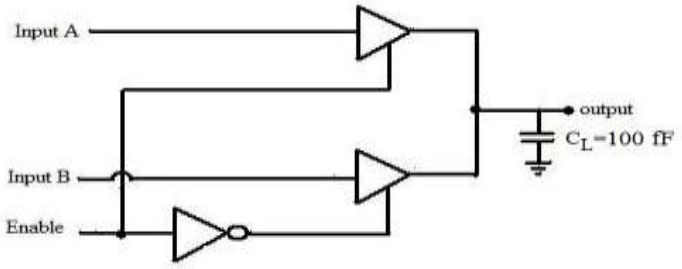


Fig. 7.3 Simulation test bench

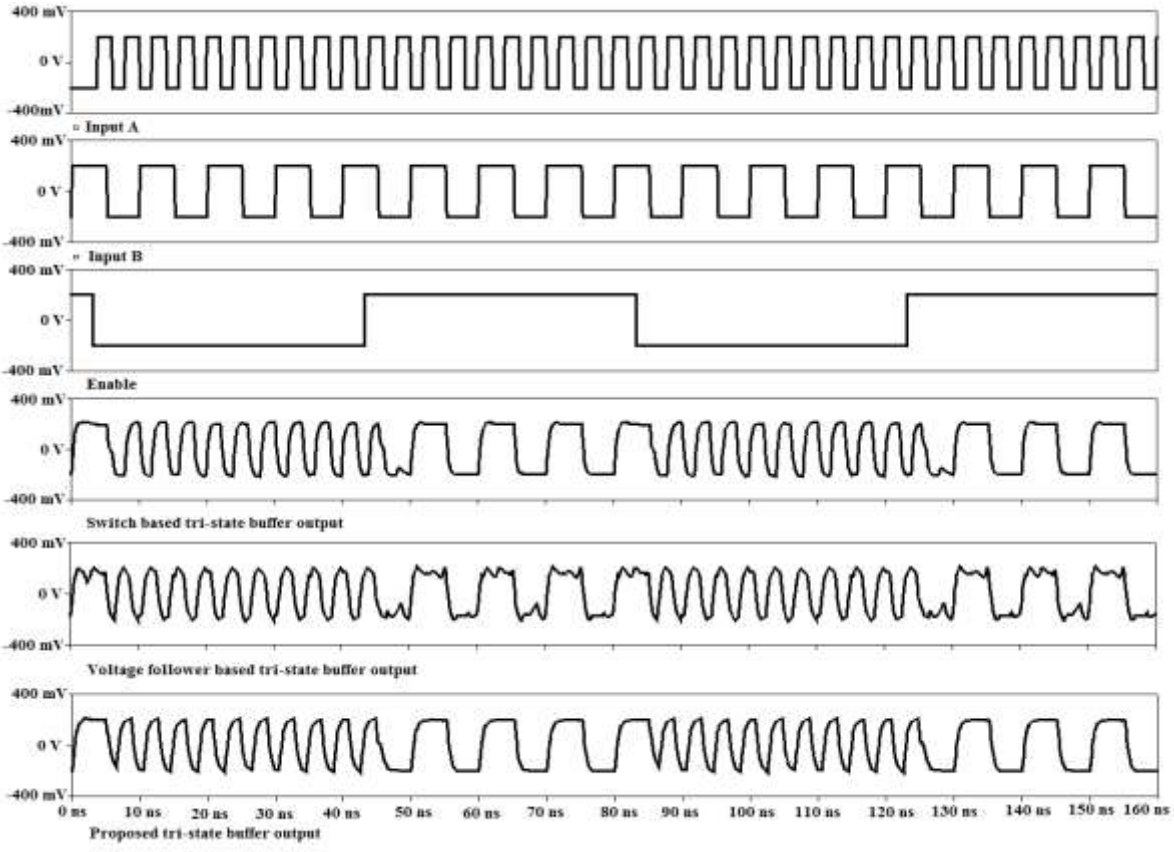


Fig. 7.4 Simulation waveform of the inputs and the outputs of the different tri-state buffers

A simulation test bench to model a typical bus system is shown in Fig. 7.3. It comprises of two differential tri-state CML buffers connected to an output node with load capacitance of 100 fF. The system is simulated by using the existing as well as the proposed tri-state buffers implementations. The waveforms of the applied inputs A, B and Enable and the output of the existing and the proposed tri-state buffers are shown in Fig. 7.4. It can be observed that the proposed tri-state buffer also conforms to the functionality of a bus system.

Application 2: D latch Implementation

The tri-state inverter based implementation of a D latch is given in Fig. 7.5. It uses two tri-state inverters (I1 and I3) and a regular inverter (I2). The clock signal (CLK) controls the operation of I1 and I3. When CLK is high, I3 is in the high-impedance state and I1 is enabled such that the input data (D) gets transferred to the output node (Q) through I1 and I2. Thus, the D latch operates in transparent mode. Alternatively, for low value of the CLK signal, I1 is in high-impedance state and no changes in the input are reflected at the output node Q. At this point I3 is enabled, that makes the feedback loop around I2 and I3 closed therefore the last output value is preserved.

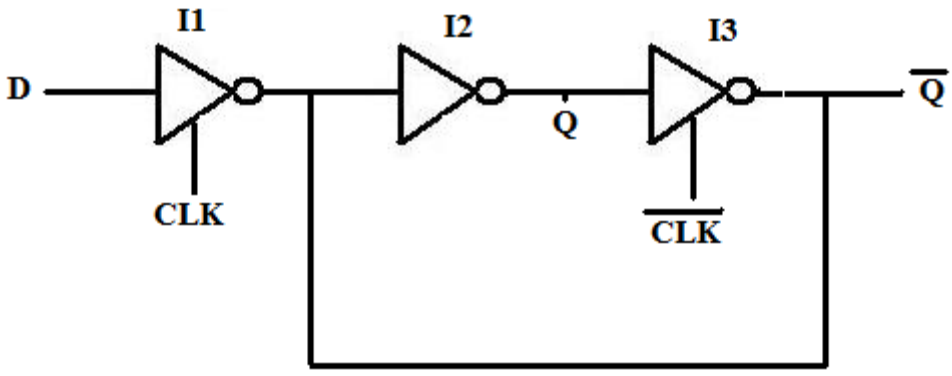


Fig. 7.5 D latch implementation using tri-state inverter

The tri-state inverter based D latch design requires three gates. The functionality of D latch can also be achieved by tri-state buffers as depicted in Fig. 7.6. It consists of two tri-state buffers B1 and B2 controlled by clock signal (CLK) and its complement $\overline{\text{CLK}}$. When CLK is high, the tri-state buffer B1 acts as a regular buffer and the D latch is transparent making the input data (D) available at the output (Q). The tri-state buffer B2 enters high-impedance state and the feedback loop is not closed. Similarly, when CLK is low, the enabled tri-state buffer B2 preserves the last output value and does not reflect any changes at the input to the output node.

The later implementation of D latch is preferable in differential CML style as the functionality of buffer can be obtained by simply interchanging the output nodes.

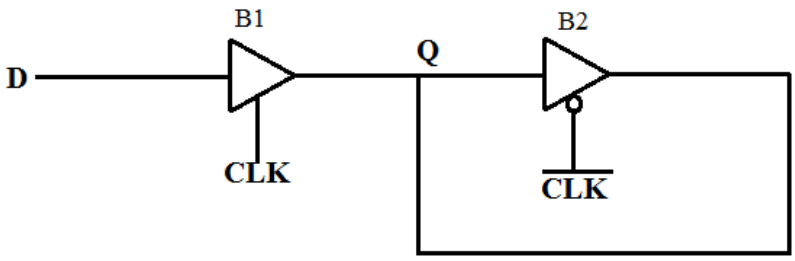


Fig. 7.6 D latch implementation using differential tri-state CML buffers

The D latch is implemented using the proposed and the existing tri-state buffer topologies and is simulated with a clock frequency of 500 MHz. All the buffers maintain a bias current of 50 μA, voltage swing of 400 mV, and a load capacitance of 10 fF. The values of the power consumption and different timing parameters are summarized in Table 7.2. It is observed that the D latch implemented using the proposed tri-state buffer shows the best performance values in comparison to the other existing ones.

Table 7.2 Summary of the D latch simulation results

Circuit	Power (µW)	CLK->Q (ps)		D->Q (ps)	
		L->H	H->L	L->H	H->L
Switch based [101]	180	275.8	271.6	302.9	306.8
Voltage follower based [101]	180	310.3	290.1	290.1	281.4
Proposed	90	320.1	305.1	206.7	201.6

7.4 CONCLUDING REMARKS

In this chapter, the two available circuits to implement tri-state CML inverter/buffer are briefly reviewed. The power issue in the available ones is identified and a new circuit for tri-state CML inverter/buffer is presented. The proposed circuit offers power saving by restricting the current flow in the high-impedance state. The performance of the proposed tri-state buffer is compared with the existing ones through simulations. It is found that the proposed tri-state CML buffer implementation is power efficient. The usefulness of the proposed tri-state CML buffer is demonstrated through two applications.

This thesis presents current mode logic circuits with enhanced performance by modifying the basic parts of a conventional CML gate, used for digital circuit design in mixed-signal environments. In this chapter a summary of the major conclusions of the work reported in various chapters of the thesis are presented.

8.1 MAIN RESULTS OF THE THESIS

The primary investigation deals with the analysis and design of the new CML topologies. In particular, following new CML topologies have been suggested in this work.

1. The triple-tail cell concept is used for logic function realization in the PDN of differential CML gates.
2. Developed a dynamic current source and investigated its usage in dynamic differential CML and PFSCL gates.
3. Proposed a self-timed buffer for cascading multiple stages of dynamic gates.
4. An active load exhibiting capacitive coupling, for improving the speed of the CML gates, is proposed.
5. A new fundamental cell is developed to reduce gate count in PFSCL circuit realization.
6. Proposed a low power tri-state CML inverter/buffer and its usefulness are illustrated through bus implementation and D latch.

Several modifications in the CML topology for performance enhancement have been suggested in this work. The proposed CML topologies may be widely used for various find applications in the area of high speed and low power designs.

A detailed study of the CML gates is presented in chapter-2. The operating principles of the differential and single-ended CML gates are reviewed. An improved version of the single-ended CML gate named as positive-feedback source-coupled logic (PFSCL) is worked upon. The pencil-and-paper approach for analysis and design of differential CML and PFSCL inverters is presented. The mathematical expressions are derived using BSIM3v3 transistor model equations. The method for logic function implementations in differential CML and PFSCL styles are also described and illustrated through few common digital logic gates. Chapters 3 to 7 present the research contribution of this thesis.

The logic function realization in differential CML gates is based on series-gating approach that infers a multilevel structure of source-coupled transistor pairs in the PDN. In chapter-3, the PDN of the differential CML gate is modified to reduce the number of source-coupled transistor pair levels, using triple-tail cell based approach, for logic function realization. It also lowers the minimum power supply requirement. New triple-tail cell based differential CML topologies for XOR gate and D latch are presented. The behavior of the proposed topologies is examined and modeled using pencil-and-paper approach which is followed by static model based design procedure. The theoretical propositions are verified by designing the proposed topologies for wide range of operating conditions and comparing the simulated results with the predicted ones. The maximum error between the simulated and the predicted values for voltage swing, small-signal voltage gain, noise margin and delay is found to be well within 14 % . The impact of parameter variations show slightly higher variations, in the proposed topologies than the existing ones for different design corners which can be attributed to the smaller sizes of the transistors employed, in comparison to existing ones. The effect of transistors mismatch is also studied by varying widths of NMOS and PMOS

transistors by 10 %. The variation in voltage swing, small-signal voltage gain, noise margin and delay are within 8 % for both the topologies. The chapter is concluded by evaluating the performance of the proposed topologies for different design cases such as high speed, power efficient and low power. The comparison results recommend the use of the proposed topologies for high speed and low power design cases.

The current source section of the CML gates is modified in chapter-4 to reduce power consumption. The dynamic current source scheme is investigated in this work. The CML gates employing the dynamic current source are named as Dynamic CML gates and are abbreviated as D-CML gates in this work. The existing dynamic current source implementation employs a CMOS inverter which is not suited in mixed-signal applications. Therefore a new dynamic current source is proposed, which overcomes this problem, and is further used to develop new dynamic differential CML gates, abbreviated as D-MCML-NP gates in this work. The performance of proposed D-MCML-NP gates is compared with the differential CML and the existing dynamic CML gates (abbreviated as D-MCML-NN gates in this work) in terms of power and delay. A maximum power saving of 71 % is achieved in D-MCML-NP gates as compared to the existing ones. Also, the results pertaining to propagation delay indicate lower value for the proposed gates in comparison to the differential CML gates as additional switching in not required for low input. However, the delay of D-MCML-NP gates is higher than the existing D-MCML-NN gates which can be attributed to the larger capacitance used in the former one. New PFSCL gates based on the existing (named as D-PFSCL-NN gates) and the proposed dynamic current source (named as D-PFSCL-NP gates) are also designed. The power consumption analysis of these gates shows data dependency. The proposed dynamic PFSCL gates show significant reduction of

83 % in power consumption with respect to the conventional PFSCL gates. The proposed dynamic PFSCL gates show similar delay variation as observed in differential D-CML gates. The chapter is concluded by addressing use of self-timed buffer in multi-stage applications of D-CML gates. A new self-timed buffer implementation for CML circuits using proposed dynamic current source is presented. It does not require the complement of the clock signal in contrast to its existing counterpart and thus beneficial in mixed-signal applications.

Chapter-5 deals with the speed improvement of the CML gates by modifying its load section. A survey on the available loads for the CML gate is presented. A new load structure using only active components is proposed and used to develop new differential and PFSCL topologies. Speed improvement is observed in the proposed differential and PFSCL topologies due to the capacitive coupling occurring in the proposed load during switching event. The phenomenon is analyzed in detail and its effect on the delay of the inverter is modeled. A systematic design procedure to determine the bias current and the transistor aspect ratios satisfying the given design specifications is also presented. The theoretical propositions are verified by designing the inverter for wide range of operating conditions. The maximum error of 14 % is found in the simulated values of the voltage swing, small-signal voltage gain, noise margin and delay with respect to the predicted values. The performance of the proposed topologies is also compared in terms of delay, with their existing counterparts, which shows a maximum improvement of 25 %.

In chapter-6, a method for reducing gate count in PFSCL circuit implementation is proposed. The triple-tail cell concept is applied in PFSCL style and a new fundamental cell is developed. The cell is analyzed and configured for different circuit realizations. The performance of the new circuit realizations is compared with conventional PFSCL

realizations in terms of the gate count, power consumption and propagation delay. There is significant reduction in gate count (66%) for NAND, AND, XOR, and XNOR gates, 2:1 multiplexer and D latch using the proposed method which leads to improvements in power consumption (64%) and speed (48%). Hence it is expected that the proposed method for PFSCL circuit realizations will provide an efficient design option to designers.

Tri-state circuits are the vital elements in bus organized, and programmable logic devices and are explored in Chapter-7. Available tri-state CML inverter/buffer circuits are briefly reviewed. These circuits consume same power in the enabled and the high impedance states. Therefore a new tri-state CML inverter/buffer circuit is presented which offers power saving by restricting the current flow in the high impedance state. The performance of the proposed tri-state buffer is compared with the existing ones through simulations. It is found that the proposed tri-state CML buffer implementation consume less power than the available circuits. The usefulness of the proposed tri-state CML buffer in bus systems and D latch implementations is demonstrated.

8.2 SUGGESTIONS FOR THE FUTURE WORK

In this work, the PDN, load and current source sections of CML gates are modified for performance enhancement. The work can be extended to develop complex arithmetic blocks such as adders, compressors and multipliers to be used in microprocessors. Also, in the area of communication systems, the modifications in CML topologies can be adopted to implement phase detectors, frequency dividers and oscillators.

The analysis and design of the proposed topologies is based on the pencil-and-paper approach that is useful in early design phase. Alternatively, the algorithmic approach involving the use of software programs can be followed to design proposed CML gates.

All the designs in this thesis are simulated using 0.18 μm TSMC CMOS technology parameters. The proposed modifications can be extended to the lower technology nodes such as 130 nm, 90 nm and 45 nm. The layout can be drawn and post layout simulations can be done for all the proposed circuits in the thesis.

LIST OF FIGURES

REFERENCES

[1] S. Kiaei, D. Allstot, "Low-noise Logic for Mixed-mode VLSI Circuits," Microelectronics Journal, vol. 23, no. 2, pp. 103–114, 1992.

[2] B. Razavi, "Design of Analog CMOS Integrated Circuits," Tata McGraw Hill Edition 2007.

[3] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," Oxford University Press, Second Edition, 2007.

[4] S. Kiaei, S. Chee, and D. Allstot, "CMOS Source-Coupled Logic for Mixed-Mode VLSI," proceedings of IEEE International Symposium on Circuits and Systems, New Orleans, pp. 1608–1611, 1990.

[5] S. M. Kang, Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design," Tata McGraw Hills, Third Edition, 2006.

[6] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits," Pearson Education, Second Edition, 2003.

[7] B. Stanistic, N. Verghese, R. Rutenbar, L. Carley, and D. Allstot, "Addressing Substrate Coupling in Mixed-Mode ICs: Simulation and Power Distribution Synthesis," IEEE Journal of Solid-State Circuits, vol. 29, no. 3, pp. 226–238, 1994.

[8] D. Su, M. Loinaz, S. Masui, and B. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," IEEE Journal of Solid-State Circuits, vol. 28, no. 4, pp. 420–430, 1993.

[9] S. Masui, "Simulation of Substrate Coupling in Mixed-Signal MOS Circuits," proceedings of IEEE Symposium on VLSI Circuits, Seattle, pp. 42–43, 1992.

[10] R. Sàez, M. Kayal, M. Declercq, and M. Schneider, "Digital Circuit Techniques for Mixed Analog/Digital Circuits Applications," proceedings of IEEE International Conference on Electronics, Circuits and System, Rodos, pp. 956-959, 1996.

[11] D. Allstot, S. Chee, S. Kiaei, and M. Shristawa, "Folded Source-Coupled Logic vs. CMOS Static Logic for Low-Noise Mixed-Signal ICs," IEEE Transactions on Circuits and Systems-I, vol. 40, no. 9, pp. 553–563, 1993.

[12] S. Badel, "MOS Current-Mode Logic Standard Cells for High-Speed Low-Noise Applications," thesis no. 4098, 2008.

[13] E. Albuquerque, J. Fernandes, and M. Silva, "NMOS Current-Balanced Logic," Electronics Letters, vol. 32, no. 11, pp. 997-998, 1996.

[14] Li Yang, J. S. Yuan, "Enhanced Techniques for Current Balanced Logic in Mixed-Signal ICs," proceedings of IEEE Computer Society Annual Symposium on VLSI, pp. 1-2, 2003.

[15] E. F. M. Albuquerque, M. M. Silva, "An Experimental Comparison of Substrate Noise Generated by CMOS and by Low-noise Digital Circuit," proceedings of IEEE International Symposium on Circuits and Systems, pp. II-481-II-482, 2004.

[16] P. Saxena, K. M. Sudheer, and V. B. Chandratre, "Design of Novel Current Balanced Voltage Controlled Delay Element," International Journal of VLSI design & Communication Systems, vol. 5, no. 3, pp. 37- 45, 2014.

[17] H. Ng, D. Allstot, "CMOS Current Steering Logic for Low-Voltage Mixed-Signal Integrated Circuits," IEEE Transactions on VLSI Systems, vol. 5, no. 3, pp. 301–308, 1997.

[18] S. Radiom, B. Sheikholeslami, H. Aminzadeh, and R. Lotfi, "Folded-Current-Steering DAC: An Approach to Low-Voltage High-Speed High-Resolution D/A Converters," proceedings of IEEE International Symposium on Circuits and Systems, pp.4783 -4786, 2006.

[19] D.Y. Jeong, S. H. Chai, W. C. Song, and G. H. Cho, "CMOS Current-Controlled Oscillators Using Multiple-Feedback-Loop Ring Architectures," proceedings of IEEE International Solid-state Circuits Conference, pp. 386-491, 1997.

[20] S. Maskai, S. Kiaei, and D. Allstot, "Synthesis Techniques for CMOS Folded Source-Coupled Logic Circuits," IEEE Journal of Solid-State Circuits, vol. 27, no. 8, pp. 1157–1167, 1992.

[21] J. Kundan, S. Hasan, "Enhanced Folded Source-Coupled Logic Technique for Low-Voltage Mixed-Signal Integrated Circuits," IEEE Transactions on Circuits and Systems-II, vol. 47, no. 8, pp. 810–817, 2000.

[22] M. Maleki, S. Kiaei, “Enhancement Source-Coupled Logic for Mixed-Mode VLSI Circuits,” IEEE Transactions on Circuits and Systems-II, vol. 39, no. 7, pp. 399-402, 1992.

[23] M. Yamashina, H. Yamada, “An MOS Current Mode Logic (MCML) Circuit for Low-Power Sub-GHz Processors,” IEICE Transactions on Electronics, vol. E75-C, no. 10, pp. 1181-1187, 1992.

[24] M. Yamashina, M. Mizuno, K. Furuta, H. Igura, M. Nomura, H. Abiko, K.Okabe, A. Ono, and H. Yamad, “A Low-Supply Voltage GHz MOS Integrated Circuit for Mobile Computing Systems,” proceedings of IEEE Symposium on Low Power Electronics, San Diego, pp. 80-81, 1994.

[25] M. Mizuno, M. Yamashina, K. Furuta, H. Igura, H. Abiko, K. Okabe, A. Ono, and H. Yamada, “A GHz MOS Adaptive Pipeline Technique using MOS Current-Mode Logic,” IEEE Journal of Solid-State Circuits, vol. 31, no. 6, pp. 784-791, 1996.

[26] J. M. Musicer, J. Rabaey, “MOS Current Mode Logic for Low Power, Low Noise, CORDIC Computation in Mixed-Signal Environments,” proceedings of International Symposium of Low Power Electronics and Design, pp.102-107, 2000.

[27] M. Alioto, G. Palumbo, “Model and Design of Bipolar and MOS Current-Mode logic (CML, ECL and SCL Digital Circuits),” Kluwer Academic Publications, 2005.

[28] A. Tanabe, M. Umetani, I. Fujiwara, T. Ogura, K. Kataoka, M. Okihara, H. Sakuraba, T. Endoh, and F. Masuoka, “0.18-μm CMOS 10-Gb/s Multiplexer/Demultiplexer ICs using Current Mode Logic with Tolerance to Threshold Voltage Fluctuation,” IEEE Journal of Solid-State Circuits, vol. 36, no. 6, pp. 988–996, 2001.

[29] A. Tanabe, M. Umetani, I. Fujiwara, T. Ogura, K. Kataoka, M. Okihara, H. Sakuraba, T. Endoh, and F. Masuoka, “A 10-Gb/s Multiplexer/Demultiplexer IC in 0.18μm CMOS using Current Mode Logic with Tolerance to Threshold Voltage Fluctuation,” proceedings of IEEE International Conference on Solid-State Circuits, San Francisco, pp. 62-63,2000.

[30] H. Hassan, M. Anis, and M. Elmasry, “Low Power Multi-threshold MCML: Analysis, Design and Variability,” Microelectronics Journal, vol. 37, no. 10, pp. 1097-1104, 2006.

[31] H. Hassan, M. Anis, and M. Elmasry, "Analysis and Design of Low-Power Multi-Threshold MCML," proceedings of the IEEE International Conference on System-on-Chip, pp. 25-29, 2004.

[32] K. Zhou, S. Chen, A. Rucinski, J. F. McDonald, and T. Zhang, "Self-Timed Triple-Rail MOS Current Mode Logic Pipeline for Power-on-Demand Design," proceedings of IEEE International Symposium on Circuits and Systems, pp. 1394-1397, 2005.

[33] K. Zhou, Y. Luo, S. Chen, A. Drake, J. F. McDonald, and T. Zhang, "Triple-rail MOS Current Mode Logic for High-Speed Self-Timed Pipeline Applications," proceedings of IEEE International Symposium on Circuits and Systems, Island of KOS, pp. 3654-3657, 2006.

[34] M. Alioto, L. Pancioni, S. Rocchi, and V. Vignoli, "Modeling and Evaluation of Positive-Feedback Source-Coupled Logic," IEEE Transactions on Circuits and Systems-I, Regular Papers, vol. 51, no. 4, pp. 2345–2355, 2004.

[35] M. Alioto, A. Fort, L. Pancioni, S. Rocchi, and V. Vignoli, "Positive-Feedback Source-Coupled Logic: a Delay Model," proceedings of IEEE Symposium on Circuits and Systems, pp. II/641-644, 2004.

[36] M. Alioto, A. Fort, L. Pancioni, S. Rocchi, and V. Vignoli, "An Approach to the Design of PFSCL gates," proceedings of IEEE Symposium on Circuits and Systems, pp. 2437–2440, 2005.

[37] M. Alioto, L. Pancioni, S. Rocchi, and V. Vignoli, "Power-Delay-Area-Noise Margin Trade-offs in Positive-Feedback Source-Coupled Logic Gates," IEEE Transactions on Circuits and Systems-I, Regular Papers, vol. 54, no. 9, pp. 1916-1928, 2007.

[38] M. Alioto, L. Pancioni, S. Rocchi, and V. Vignoli, "Exploiting Hysteresys in MCML Circuits," IEEE Transactions on Circuits and Systems-II, vol. 53, no. 11, pp. 1170-1174, 2006.

[39] R. Cao, J. Hu, "Near-threshold Computing of Single-rail MOS Current Mode Logic Circuits," Research Journal of Applied Sciences, Engineering and Technology, vol. 5, Article ID: 836019, pp. 2991-2996, 2013.

[40] R. Cao, J. Hu, "Near-Threshold Computing and Minimum Supply Voltage of Single-Rail MCML Circuits," Journal of Electrical and Computer Engineering, vol. 2014, Article ID 836019, 10 pages, 2014.

[41] M. P. Houlgate, D. J. Olszewski, K. Abdelhalim, and L. M. Eachern, "Adaptable Performance MOS Current Mode Logic for use in a 3GHz Programmable Frequency Divider," proceedings of IEEE Conference on Circuits and Systems, pp. 1303-1306, 2003.

[42] M. P. Houlgate, D. J. Olszewski, K. Abdelhalim, and L. M. Eachern, "Adaptable MOS Current Mode Logic for use in a Multi-band RF Prescaler," proceedings of IEEE Conference on Circuits and Systems, pp. 329-332, 2004.

[43] A. Worapishet, M. Thamsirianunt, "An NMOS Inductive Loading Technique for Extended Operating Frequency CMOS Ring Oscillators," proceedings of IEEE Midwest Symposium on Circuits and Systems, pp. 116-119, 2002.

[44] H. T. Bui, Y. Savaria, "10 Ghz PLL using Active Shunt-Peaked MCML Gates and Improved Frequency Acquisition XOR Phase Detector in 0.18 μm CMOS," proceedings of the IEEE International Workshop SOC for Real-Time Applications, pp. 115–118, 2004.

[45] S. S. Mohan, M del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth Extension in CMOS with Optimized On-Chip Inductors," IEEE Journal of Solid-State Circuits, vol. 35, no. 3, pp. 346 – 354, 2000.

[46] H. T. Bui, Y. Savaria, "Shunt-Peaking of MCML Gates using Active Inductors," proceedings of IEEE Northeast Workshop on Circuits and Systems, pp. 361-364, 2004.

[47] F. Yuan, "CMOS Active Inductors and Transformers: Principle, Implementation and Applications," Springer, 2008.

[48] S. Mohan, S. Hershenson, M. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," IEEE Journal of Solid-State Circuits, vol. 34, no. 10, pp. 1419–1424, 1999.

[49] B. Sun, F. Yuan, "A New Inductor Series-Peaking Technique for Bandwidth Enhancement of CMOS Current-Mode Circuits," Analog Integrated Circuits and Signal Processing, vol. 37, pp. 259–264, 2003.

[50] F. Yuan, "CMOS Current-Mode Circuits for Data Communications," Springer, 2007.

[51] H. T. Bui, "Dual-Path and Diode-Tracking Active Inductors for MCML Gates," Canadian Conference on Electrical and Computer Engineering, pp. 1060 – 1063, 2006.

[52] S. M. Masood, "Active Loads in Current-Mode Logic (CML) Topology," Technical University of Denmark, 2006.

[53] A. Tajalli, E. VIttoz, and Y. Leblebici, "Ultra Low Power Subthreshold MOS Current Mode Logic Circuits using a Novel Load Device Concept," proceedings of International Conference on Solid State Circuits, Munich, pp. 304 – 307, 2007.

[54] Cannillo, C. Toumazou, and T. S. Lande, "Bulk-Drain Connected Load for Subthreshold MOS Current Mode Logic," Electronics letter, vol. 43, no. 12, pp. 662-664, 2007.

[55] A. Tajalli, E. VIttoz, Y. Leblebici, and E. J. Brauer, "Ultra-Low Power Subthreshold Current-Mode Logic utilizing PMOS Load Device," Electronics Letter, vol. 43, no. 17, pp. 911-912, 2007.

[56] M. Alioto, Y. Leblebici, "Analysis and Design of Ultra-Low Power Subthreshold MCML Gates," proceedings of IEEE International Symposium on Circuits and System, Taipei, pp. 2557 – 2560, 2009.

[57] E A. Shapiro, E. G. Friedman, "Performance Characteristics of 14 nm Near Threshold MCML Circuits," proceedings of IEEE Unified Conference on SOI-3D-Subthreshold Microelectronics Technology, Monterey, pp.1-2, 2013.

[58] A. Tajalli, Y. Leblebici, "Subthreshold Source-Coupled Logic," Book Chapter in Advanced Circuits for Emerging Technologies (ed K. Iniewski), John Wiley & Sons, Inc., Hoboken, NJ, USA, 2012.

[59] A. Tajalli, E. J. Brauer, Y. Leblebici, and E. Vittoz, "Subthreshold Source-Coupled Logic Circuits for Ultra-Low-Power Applications," IEEE Journal of Solid-State Circuits, vol. 43, no. 7, pp. 1699-1710, 2008.

[60] F. Cannillo, C. Toumazou, and T. S. Lande, "Nanopower Subthreshold MCML in Submicrometer CMOS Technology," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 56, no. 8, pp. 1598 – 1611, 2009.

[61] M.W. Allam, M. I. Elmasry, "Dynamic Current Mode Logic (DyMCML): A New Low-Power High Performance Logic Style," IEEE Journal Solid-State Circuits, vol. 36, no. 3, pp. 550-558, 2001.

[62] G. Caruso, D. Sclafani, "Analysis of Compressor Architectures in MOS Current-Mode Logic," proceedings of IEEE International Conference on Electronics, Circuits, and Systems, Athens, pp. 13 – 16, 2010.

[63] M. H. Anis, M. I. Elmasry, "Self-timed MOS Current Mode Logic for Digital Applications," proceedings of IEEE International Symposium on Circuits and Systems, pp. 113–116, 2002.

[64] J. B. Kim, "Low-Power MCML Circuit with Sleep-Transistor," proceedings of IEEE International Conference on Application-Specific Integrated Circuits, pp. 25-28, 2009.

[65] K. Zou, J. Hu, "A Power-Gating Scheme for MOS Current Mode Logic Circuits," Telkomnika, vol. 11, no. 10, pp. 6111-6119, 2013.

[66] Y. Wu, X. Fan, H. Ni, and J. Hu, "Low-Power Near-threshold MOS Current Mode Logic with Power-Gating Techniques," proceedings of the 2nd International Conference on Computer Science and Electronics Engineering, Changsha, pp. 1694-1697, 2013.

[67] A. Cevrero, F. Regazzoni, M. Schwander, S. Badel, P. Ienne, and Y. Leblebici, "Power-gated MOS Current Mode Logic (PG-MCML): A Power Aware DPA-Resistant Standard Cell Library," proceedings of in IEEE International Conference on Design Automation, New York, pp. 1014 – 1019, 2011.

[68] S. Bruma, "Impact of on-chip Process Variations on MCML Performance," proceedings of IEEE Conference on Systems-on-Chip, pp. 135–140, 2003.

[69] M. Alioto, G. Palumbo, "Design Strategies for Source Coupled Logic Gates," IEEE Transactions on Circuits and Systems- I, vol. 50, no. 5, pp. 640–654, 2003.

[70] M. Alioto, G. Palumbo, and S. Pennisi, "Modelling of Source-Coupled Logic Gates," International Journal of Circuit Theory and Applications, vol. 30, no. 4, pp. 459–477, 2002.

[71] H. Hassan, M. Anis, and M. Elmasry, "MOS Current Mode Circuits: Analysis, Design, and Variability," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 8, pp. 885-898, 2005.

[72] M. Alioto, G. Palumbo, "Power-Delay Optimization of D-latch/MUX Source Coupled Logic Gates," International Journal of Circuit Theory and Applications, vol. 33, no. 1, pp. 65-85, 2005.

[73] M. Alioto, L.Pancioni, S. Rocchi, and V. Vignoli, "Analysis and Design of MCML gates with Hysteresis," proceedings of International Symposium on Circuits and Systems, Island of KOS, pp. 1263-1267, 2006.

[74] M. Alioto, G. Palumbo, "Modelling and design considerations on CML gates under high-current effects," International Journal of Circuit Theory and Applications, vol. 33, pp. 503-518, 2005.

[75] M. Alioto, G. Palumbo, "Nanometer MCML gates: Models and Design Considerations," proceedings of IEEE International Symposium on Circuits and Systems, Marrakech, 2006.

[76] M. Alioto, "Design of Nanometer MOS Current Mode Logic: From Very High-Speed Down to Ultra-Low Power," proceedings of International Conference on Microelectronics, pp. 12-13, 2009.

[77] A. H. Ismail, M. I. Elmasry, "A Low Power Design Approach for MOS Current Mode Logic," proceedings of IEEE Conference on Systems on-Chip, pp.143–146, 2003.

[78] G. Caruso, "Design of MOS Current Mode Logic Gates-Computing the Limits of Voltage Swing and Bias Current," proceedings of IEEE International Symposium on Circuits and Systems, pp. 5637-5640, 2005.

[79] G. Caruso, A. Macchiarella, "Optimum Design of two-level MCML gates," proceedings of IEEE International Conference on Electronics, Circuits and Systems, St. Julien's, pp. 141-144, 2008.

[80] O. Musa, M. Shams, "An Efficient Delay Model for MOS Current-Mode Logic Automated Design and Optimization," IEEE Transactions on Circuits and Systems-I, vol. 57, no. 8, pp. 2041 – 2052, 2010.

[81] U. Seckin, C. K. Yang, "A Comprehensive Delay Model for CMOS CML Circuits," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 55, no. 9, pp. 2608-2618, 2010.

[82] H. Hassan, M. Anis, and M. Elmasry, "Design and Optimization of MOS Current Mode Logic for Parameter Variations," Integration, the VLSI Journal - Special issue: ACM Great Lakes Symposium on VLSI, vol. 38, no. 3, pp. 417-437, 2005.

[83] R. P. Arroyo, P. A. Moya, and H. Wolfgang, "Design of a MCML Gate Library Applying Multiobjective Optimization," proceedings of the IEEE Computer Society Annual Symposium on VLSI, Porto. Alegre, pp. 310–314, 2007.

[84] R. Pereira, P. Alvarado, and H. Krautschneider, "Multi-Objective Optimization of MCML Circuits using a Genetic Algorithm," Workshop on Iberchip In Memorias, pp. 1-4, 2006.

[85] J. K. Shin, T. W. Yoo and M. S. Lee, "Design of Half-Rate Linear Phase Detector using MOS Current Mode Logic Gates for 10-Gb/s Clock and Data Recovery Circuits," proceedings of International Conference on Advanced Communication Technology, Phoenix Park, pp. 205-210, 2005.

[86] P. Heydari, R. Mohavavelu, "Design of Ultra High-speed CMOS CML Buffers and Latches," proceedings of IEEE Conference on Circuits and Systems, pp. 208-211, 2003.

[87] M. Sumanthi, Y. C. Kartheek, "Performance and Analysis of CML Logic Gates and Latches," proceedings of IEEE International Symposium on Microwave, Antenna, Propagation and EMC technologies for Wireless Communications, Hangzhou, pp. 1428-1432, 2007.

[88] P. Heydari, R. Mohavavelu, "Design of Ultra High-Speed CMOS CML Buffers and Latches," proceedings of the International Symposium on Circuits and Systems, pp. II-208 - II-211, 2003.

[89] M. Usama, Tad A. Kwasniewski, "Design and Comparison of CMOS Current Mode Logic Latches," proceedings of IEEE International Symposium on Circuits and Systems, pp. 353-356, 2004.

[90] M. Alioto, R. Mita, and G. Palumbo, "Design of High-Speed Power Efficient MOS Current Mode Logic Frequency Dividers," IEEE Transactions on Circuits and Systems – II: Express Briefs, vol. 53, no. 11, pp. 1165-1169, 2006.

[91] R. Nonis, E. Palumbo, P. Palestri, and L. Selmi, "A Design Methodology for MOS Current-Mode Logic Frequency Dividers," IEEE Transactions on Circuits and Systems – I: Regular Papers, vol. 54, no. 2, pp. 245-254, 2007.

[92] B. Razavi, "A Model to Understand Current Consumption, Maximum Operating Frequency and Scaling Trends Of MCML Frequency Dividers," Rf Microelectronics, Prentice Hall, 1998.

[93] U. Singh, M. M. Green, "High-Frequency CML Clock Dividers in 0.13-m CMOS Operating Up to 38 GHz, IEEE Journal of Solid-State Circuits, vol. 40, no. 8, pp. 1658-1661, 2005.

[94] M. Nocente, D. Fontanelli, P. Palestri, R. Nonis, D. Esseni, and L. Selmi, "A Numerical Model for the Oscillation Frequency, the Amplitude and the Phase-Noise of MOS-Current-Mode-Logic Ring Oscillators," International Journal of Circuit Theory and Applications, vol. 38, no. 6, pp. 591-623, 2009.

[95] A. H. Ismail, M. Sharifkhani, and M I. Elmasry, "On the Design of Low Power MCML Based Ring Oscillators," proceedings of IEEE Canadian Conference on Electrical and Computer Engineering, pp. 2383-2386, 2004.

[96] L. Li, S. Raghavendran, and D. T. Comer, "CMOS Current Mode Logic Gates for High Speed Applications," proceedings of NASA Symposium on VLSI Design, Coeurd' Alene, Idaho, pp. 1-3, 2005.

[97] S. Kabiri, M. Shams, "Implementation of MCML Universal Logic for 10 GHz Range in a 0.13 μm CMOS Technology," proceedings of the International Symposium on Circuits and Systems, pp. 653-656, 2004.

[98] P. Heydari, "Design and Analysis of Low-Voltage Current-Mode Logic Buffers," proceedings of IEEE International Symposium on Quality Electronic Design, pp. 293–298, 2003.

[99] M. Alioto, G. Palumbo, "Power Aware Design of Nanometer MCML Tapered Buffers," IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 55, no. 1, pp. 16-20, 2008.

[100] Y. M. El-Hariry, A. H. Madian, "MOS Current Mode Logic Realization of Digital Arithmetic Circuits," proceedings of International Conference on Microelectronics, Cairo, pp. 128-131, 2010.

[101] S. Badel, Y. Leblebici, "Tri-state Buffer/Bus Driver Circuits in MOS Current-Mode Logic," proceedings of Research in Microelectronics and Electronics Conference, Bordeaux, pp. 237-240, 2007.

[102] N. Haiyan, H. Jianping, "The Layout Implementations of High-Speed Low-Power MCML Cells," proceedings of IEEE International Conference on Electronics, Communication and Control, Zhejiang, pp. 2936 – 2939, 2011.

[103] M. Haghi, J. Draper, "A Single-Event Upset Hardening Technique for High Speed MOS Current Mode Logic," proceedings of IEEE International Symposium on Circuits and Systems, Paris, pp. 4137–4140, 2010.

[104] S. Khabiri, M. Shams, "An MCML Four-Bit Ripple-Carry Adder Design in 1 GHz Range," proceedings of IEEE International Symposium on Circuits and Systems, pp. 1634 – 1637, 2005.

[105] B. Liang, K. Ma, Z. Ding, and X. Fu, "The Structure Design of MOS Current Mode Logic Adder," proceedings of International Conference on millimeter wave Technology, Shenzen, vol. 4, pp. 1-4, 2012.

[106] Y. Delican, T. Yildirim, "High Performance 8-bit MUX based Multiplier Design using MOS Current Mode Logic," proceedings of International Conference on Electrical and Electronics Engineering, Bursa, pp. II-89 - II-93, 2011.

[107] A. Saha, D. Pal, M. Chandra, and M. K. Goswami, "Novel High Speed MCML 8-Bit by 8-Bit Multiplier," proceedings of International Conference on Devices and Communications, Mesra, pp. 1-5, 2011.

[108] V. Srinivasan, S. H. Dong, and J. B. Sulistyo, "Gigahertz-Range MCML Multiplier Architectures," proceedings of the International Symposium on Circuits and Systems, pp.785-788, 2004.

[109] Y. Delcan, A. Morgul, "High Performance 16-bit MCML Multiplier," proceedings of IEEE European Conference on Circuit Theory and Design, Antalya, pp.157-160, 2009.

[110] M. Mizuno, M. Yamashina, K. Furuta, H. Igura, H. Abiko, K. Okabe, A. Ono and H. Yamada, "A GHz MOS Adaptive Pipeline Technique using Variable Delay Circuits," IEEE International Symposium on VLSI circuits, pp. 27-28, 1994.

[111] T. W. Kwan, M. Shams, "Multi-GHz Energy-Efficient Asynchronous Pipelined Circuits in MOS Current Mode Logic," proceedings of IEEE International Symposium on Circuits and Systems, pp. II-645–II-648, 2004.

[112] T. W. Kwan, M. Shams, "Design of Multi-GHz Asynchronous Pipelined Circuits in MOS Current Mode Logic," proceedings of International Conference on VLSI Design, pp. 301-305, 2005.

[113] T. W. Kwan, M. Shams, "Design of Asynchronous Circuit Primitives using MOS Current Mode Logic," proceedings of International Conference on VLSI Design, pp. 170-173, 2004.

[114] T. W. Kwan, M. Shams, "Design of High-Performance Power-Aware Asynchronous Pipelined Circuits in MOS Current Mode Logic," proceedings of IEEE International Symposium on Asynchronous Circuits and Systems, pp. 1-10, 2005.

[115] Y. Cheng, Hu C, "MOSFET Modeling & BSIM3 User's Guide," Kluwer Academic Publishers, Boston, 1999.

[116] K. Kimura, "Circuit Design Techniques for Very Low-Voltage Analog Functional Blocks using Triple-Tail Cells," IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications, vol. 42, no. 11, pp. 873-885, 1995.

[117] F. Matsumoto, Y. Noguchi, "Linear Bipolar OTAs Based on a Triple-Tail Cell Employing Exponential Circuits," IEEE Transactions on Circuits and Systems – II: Express Briefs, vol. 51, no. 12, pp. 670-674, 2004.

[118] M. Alioto, R. Mita, and G. Palumbo, "Performance Evaluation of the Low-voltage CML D latch Topology," INTEGRATION, the VLSI Journal, vol. 36, no. 4, pp. 191-209, 2003.

[119] H. C. Jonathan, C. A. Johnston, and L.S. Smoot, "A Packet Video/Audio System using the Asynchronous Transfer Mode Technique," IEEE Transaction on Consumer Electronics, vol. 35, no. 2, pp. 97-105, 1989.

[120] R. Golshan, B. Haroun, "A Novel Reduced Swing CMOS Bus Interface Circuit for High-Speed Low-Power VLSI Systems," proceedings of the International Symposium on Circuits and System, pp. 351–354, 1994.

[121] M. Akata, S. Karube, T. Sakamoto, T. Saito, S. Yoshida, and T. Maeda, "A 250 Mb/s 32 x 32 CMOS Cross Point LSI for ATM Switching Systems," proceedings of IEEE International Solid-State Circuits Conference, pp. 30-31, 1990.

[122] L. Louis, J. Chroma, and J. Draper, "A Self-sensing Tri-State Pad Driver for Control Signals of Multiple Bus Controller," proceedings of the IEEE International Symposium on Circuits and Systems, pp. 447-450, 1999.

BIO-DATA

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