

REALIZATION OF PULSE TRIGGERED D FLIP FLOP

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I, Ankur Mangla, Roll No. 2K17/VLS/03 student of Master of Technology in VLSI Design and Embedded System, hereby declare that the project titled “Realization of pulse triggered D Flip Flop” which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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ANKUR MANGLA

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ABSTRACT

The evolution of hand held devices and desire to place increased functionality on single chip has led to increased power consumption. This has necessitated to explore methods to lower overall power consumption.

Flip flops are the fundamental storage element and are used for sequential circuit design, the power consumption in these elements need be reduced. The pulse triggered (PT) flip flop are addressed in this work as it has lower power consumption in comparison to master slave flip flop. The PT flip flops are classified as–implicit and explicit. The explicit pulse triggered D flip flop consists of a latch circuitry a pulse generator circuitry which can be reused in different flip flops. The implicit type flip flop, on the other hand, requires separate pulse generator circuitry for every flip flop. So it consumes more power than explicit type. In this project new topologies of explicit pulse triggered D flip flop are presented which use available four transistors based pulse generator and/ or modified the latch circuitry. The PT flip flops are simulated using CMOS 90nm process technology at 1V supply voltage using Cadence Virtuoso. Simulation results shows that the proposed topologies consume less power in comparison to the other PT flip flops and also shows improvement in delay.

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LIST OF ABBREVIATIONS

Abbreviation	Full form
FF	Flip flop
EP-DCO FF	Explicit data close to output
CDFE	Conditionally discharge flip flop
SCDFE	Static conditionally discharge flip flop
SFTFF	Signal feed through flip flop
4 TPG	Four transistors pulse generator

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CHAPTER 1

Introduction

The continuous improvement in VLSI technology has led into downsizing of the device dimensions which has resulted in increased transistor densities [1-5]. Millions of transistors coexist on the chips today, due to which consumption of power is constantly increasing. Though power supply and capacitance are scaled down, still power consumption in VLSI chips is increasing day by day and researchers are looking into methods of combat it [4-5].

Digital circuits employ pipeline techniques wherein many flip flop rich components such as shift registers and register files [6] are used. Flip flops are also used in clock distribution circuitry. Therefore, flip flops are mainly responsible for the functionality and performance. The flip flops consume a major portion, typically 30 to 50 percent, of total power consumption and chip area, hence low power and smaller area flip flops are of prime importance.

1.1 Motivation

Flip flop is the fundamental storage element extensively used in all digital circuits [1-6]. Flip flops are of three types- pulse triggered and master slave and transmission gate flip flops [1-18]. Pulse triggered flip flops are popular than any other type of flip flops like master slave flip flops or transmission gate flip flops due to the single latch structure which is useful in high speed circuit applications. Along with the speed advantage, its circuit is simple due to which the power consumption of clock tree circuitry is reduced.

A pulse triggered flip flop [PT-FF] [2, 4-7, 9-10, 14-18] contains a latch for storage of data and a pulse generator for pulsed clock signal generation. If the pulse after pulse generation is notably narrow then the latch will act like an edge triggered flip flop. Conventional master slave type flip flops contain two latch but PT-FF uses only one latch due to which PT-FF has simple circuitry. Hence PT-FF has high toggle rate in applications of high speed circuitry.

Across boundaries of clock cycle, PT - FF allows time borrowings, due to which have a zero and even negative setup time. But pulse generation also needs a delicate control over pulse width for the variations in signal distribution network. The PT-FF is classified in two categories on the basis of pulse generation, one is explicit type PT-FF and other one is implicit type PT-FF. In implicit type PT-FF, pulse generator and latch are not separate and strobe signals here generated implicitly, due to which these type of flip flops consumes less power. But the disadvantage is the longer discharging path, by which there is deterioration of timing characteristics.

In explicit type PT-FF, the latch and the pulse generator are separate and strobe signals are explicitly generated here. Due to the separation of logic and latch circuitry, this type of PT-FF consumes more power than the implicit PT-FF. But the separation of logic and latch circuitry provides faster speed than implicit PT-FF. But it has disadvantage over implicit type PT-FF, of power consumption, which can be decreased by sharing a number of flip flops to a single pulse generator circuitry. Due to the advantage in terms of power consumption and reduced complexity of the circuit, explicit type PT-FF is preferred [14-18].

1.2 Organisation of thesis

The thesis contains six chapters including this chapter.

In chapter 2 ,there is a discussion about working of PT D flip flops, explicit data close to output flip flop (EP-DCO FF) [14], conditionally discharged flip flop (CDFF) [15], static conditionally discharged flip flop (SCDFF) [16], signal feed through flip flop (SFTT) [17] and about the novel design of low power pulse triggered D flip flop [18].

In chapter 3, the functionality of PT flip flops is examined using four transistor pulse generator. Three new topologies are presented in chapter 4 and used in shift register in chapter 5. In chapters 2 to 5, the simulation results using Cadence Virtuoso are presented to verify the functionality and examine power consumption and delay.

The conclusions are drawn in Chapter 6.

CHAPTER 2

Literature Survey

In this chapter, explicit pulse triggered flip flops namely explicit data close to output flip flop (EP-DCO FF) [14], conditionally discharged flip flop (CDFF)[15], static conditionally discharged flip flop (SCDFF) [16] , signal feed through flip flop (SFTFF) [17] and novel design of low power pulse triggered flip flop[18] are reviewed. The functionality is examined through simulations in Cadence Virtuoso using 90 nm CMOS technology parameters and parameters namely delay and power consumption are calculated.

2.1 Explicit data close to output flip flop (EP-DCO FF) [14]:-

The designing of single edge triggered flip flops is simplest. The sampling of data takes place at only on either rising edge of clock pulse or falling edge of clock pulse. Different types of flip flops of single edge triggered are used; each flip flop is being used for a specific application.

The EP –DCO FF is pulse triggered flip flop and has semi dynamic functionality and is selected for high speed and high performance applications. We get a very small flip flop delay from EP –DCO FF, because of which we place them in most critical paths. Due to the usage of pulse triggered mechanism, allows more space in budgeting of cycle due to feature of negative setup time. Figure 2.1 shows EP –DCO FF circuit diagram. There are two stages in this flip flop because of its semi-dynamic nature, first one is dynamic and other one is static stage.

In Fig.2.1, We use four inverters and a NAND gate in the pulse generator to produce the single edge triggered clock (pulsed clock).

Initially when clock =0, transistor p1 will turn on because of pull up path, node X will get a value '1'. There are two inverters I1 and I2 to store and maintain the value of X.

When the value of X is '1' transistor P2 will turn off because of P transistor and transistor N4 will turn on because of NMOS transistor.

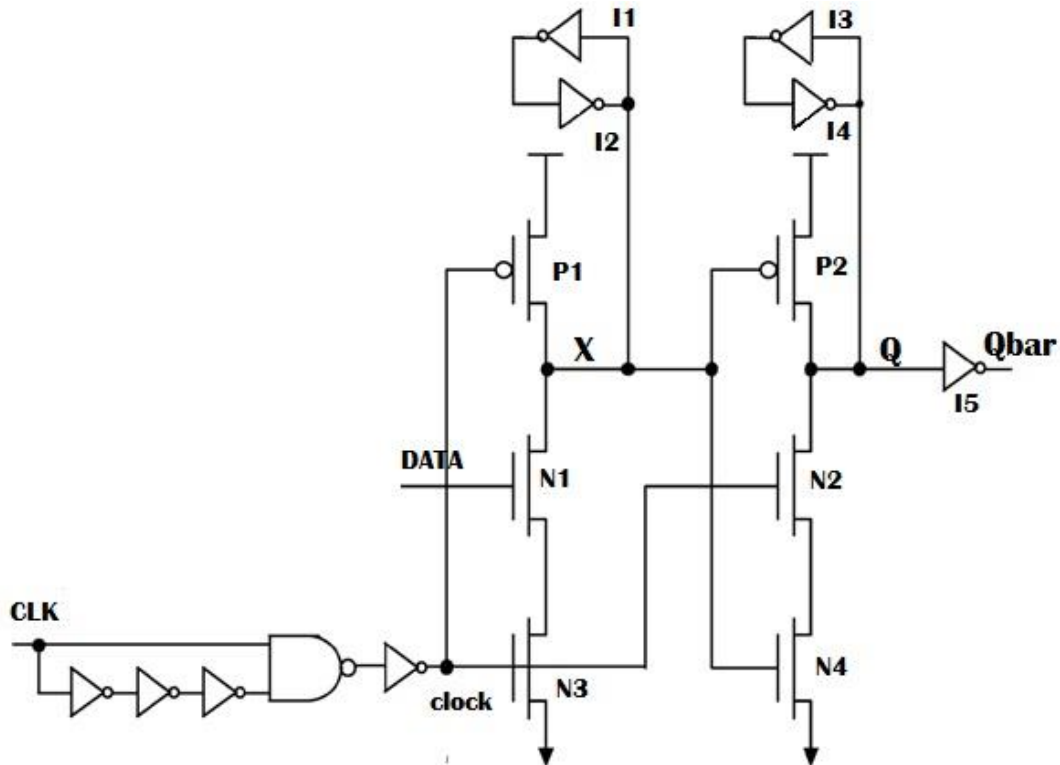


Fig 2.1 Circuit diagram of EP-DCO FF [14]

When Clock=1, for a short period of time transistors N2 and N3 will turn on whose period will be equal to the delay occurred from the pulse generator circuitry. Now, if data at transistor N1 comes with '1' then transistor N1 will turn on and as node X stores the value '1' before the rising edge of the clock, then this node X will discharge through transistors N1 and N2. Hence the value of node X will become '0', which will turn on the transistor P2 and will turn off the transistor N4. Because of pull up path through transistor P2, value at output Q will come as '1'.

When data comes as '0' at transistor N1, it will be turned off because of the NMOS transistor, as node X stores value '1' before the rising edge of the clock, it will turn off the P2 transistor and will turn on the N4 transistor. As both N3 and N4 transistor turn

on , output Q will be connected to ground by pull down network through transistors N3 and N4 and will acquire a value '0'.

In this period, flip flop becomes transparent and data from input will pass to the output. After this period of transparent, when there is no rising edge of clock, these transistors N2 and N3 will turn off from the pull down path. After that any change in the input can't propagate to the output. Keepers I3 and I4 are used to maintain output value.

In the hold mode of the circuit, on careful analysis, we get that due to charging and discharging of the internal node X, there is a consumption of significant amount of energy. When the input is at '1', node x is charged before the rising edge of the clock and when input remains same at '1' after the rising edge of the clock, this node will discharge through transistors N1 and N2.

There is no useful operation of internal activities of these charging and discharging of node. Hence this part of power dissipation does not provide any significance to the circuit operation. When the input is at '1', there is continuous charging and discharging of node X at each clock cycle due to which glitches occurs at the output. At the stage of starting of evaluation period, due to the discharging path of the internal node when it pre-charged at '1', output node will stay on for a small period and due to this path output will lose some charge.

Due to the glitches, pass to driven gates increases power consumption of the circuitry and also causes problems of noise, due to which system can damage.

2.2 Conditional discharge flip flop (CDFF) [15]

Dynamic technique is one of the best techniques to obtain minimum power consumption and is utilised in flip flops for high speed applications. Due to multiple number of internally undesired switching activities because of this dynamic functionality, a large amount of power is wasted, mainly in an environment with low or a moderate activity of data. If we can reduce these activities then we can also reduce the power dissipation.

The circuit diagram of CDFE [15] is depicted in Fig. 2.2. It uses four inverters and a NAND gate in the pulse generator to produce the single edge triggered clock (pulsed clock).

In this design, when input is at high, we control the discharge path due to which there is elimination of extra produced switching activity. Hence it is named as conditionally discharge technique. In this technique there is insertion of N transistor with Qb in the discharge path of high switching activity stage. When input is from '0' to '1', output will be at '1' and Qb at '0'. This breaks off the discharge path when input as at '1'

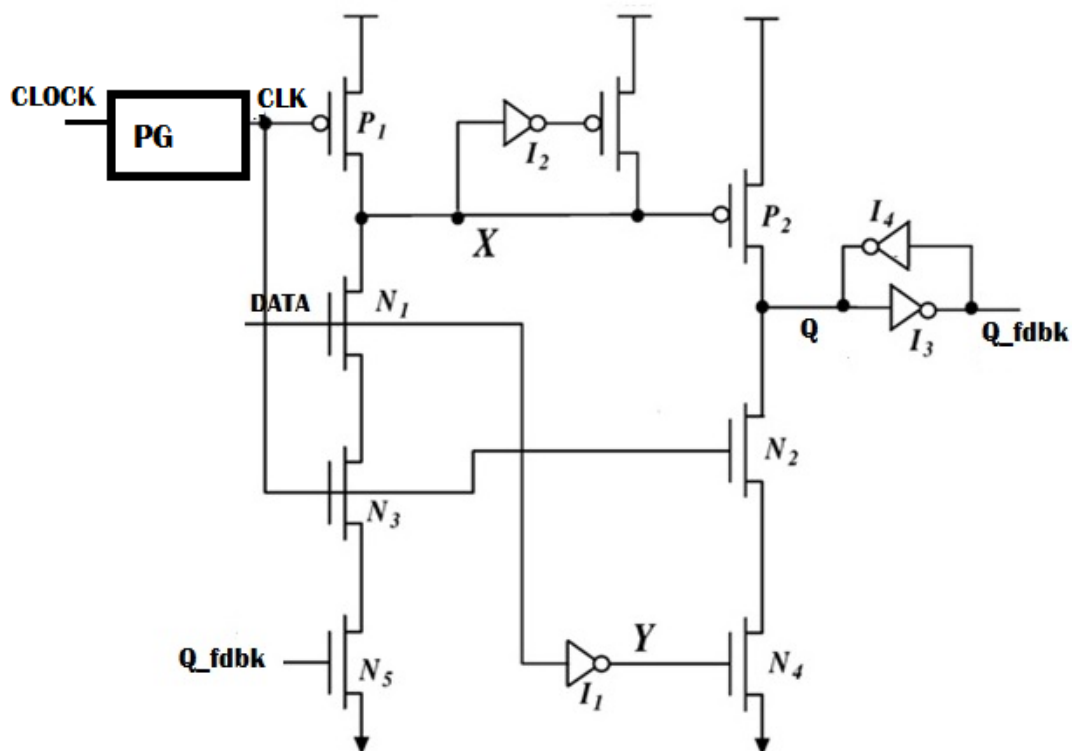


Fig 2.2 Circuit diagram of CDFE [15]

The flip flop has two stages, in stage one there is capturing of '0' to '1' transition and stage 2 has capturing of '1' to '0' transition.

Initially when clock =0, transistor p1 will turn on because of pull up path, node X will get a value '1'. There are one inverter I1 and a P transistor which forms a pull up path, to store and maintain the value of X. When the value of X is '1' transistor P2 will turn off because of PMOS transistor.

When clock=1, for a short period of time transistors N2 will turn on whose period will be equal to the delay occurred from the pulse generator circuitry. Then if data at transistor N1 comes with '1' then transistor N1 will turn on and as node X stores the value '1' before the rising edge of the clock, then this node X will discharge through transistors N1,N3 and N5, because Q b is at '1'. Hence the value of node X will become '0', which will turn on the transistor P2 and N4 will be turned off. Because of pull up path through transistor P2, value at output Q will come as '1'.

When data comes as '0' at transistor N1, it will be turned off because of the N transistor as node X stores value '1' before the rising edge of the clock, it will turn off the P2 transistor and will turn on the N4 transistor. As both N2 and N4 transistor turn on, output Q will be connected to ground by pull down network through transistors N2 and N4 and Q will acquire a value '0'.

In this period, flip flop becomes transparent and data from input will pass to the output. After this period of transparent, when there is no rising edge of clock, these transistors N2 and N3 will turn off. After that any change in the input can't propagate to the output. Keepers I3 and I4 are used to maintain output value.

In the hold mode of the circuit, when we do careful analysis, we get that due to charging and discharging of the internal node X, there is a consumption of significant amount of energy. When the input is at '1', node x is charged before the rising edge of the clock and when input remains same at '1' after the rising edge of the clock, this node will discharge through transistors N1 and N2 in EP-DCO FF [14].

There is no useful operation of internal activities of these charging and discharging of node X, hence this part of power dissipation doesn't provide any significance to the circuit operation. But here is a feedback controlled system with inverted output, due to

which, When the input is at '1', there is no continuous charging and discharging of node X because of the N5 transistor, because N5 transistor will turn off when there is '1' at output (when data is at '1' previously).

Due to the glitches, pass to driven gates increases power consumption of the circuitry and also causes problems of noise, due to which system can damage. Hence glitches are removed here with the help of feedback controlled circuit

2.3 Static conditionally discharged flip flop (SCDFF) [16]:-

For the requirement of critical paths with high speed, we use one of the most semi-dynamic high speed flip flops, explicit pulsed data close to output (EP-DCO FF)[14]. But the power consumption is high in this case because of the continuous charging and discharging (in the precharge and the evaluation phase) when data input was at value '1'. Hence explicit pulsed static flip flops [7] are more useful than the explicit pulsed dynamic flip flops[7] due to their functionality of not precharging the internal nodes which helps in reducing unnecessary transitions at these nodes.

We also know that static circuits are far better than the dynamic circuits when there is small 'fan in' in the circuit because there is reduction of power occupation and glitches are reduced without any optimization with the circuit performance. Hence we need a flip flop which will have a static nature (no precharge phase) and also there is controlled feedback circuitry of inverted output, which is the static conditionally discharged flip flop (SCDFF) [16] (Fig. 2.3). Here, four inverters and a NAND gate are used in the pulse generator to produce the single edge triggered clock(pulsed clock).

Considering Fig2.3, flip flop has two stages, in stage one there is capturing of '0' to '1' transition and stage 2 has capturing of '1' to '0' transition.

Initially when clock =0, transistor MP1 will not turn on here like in CDFF because it is connected to data now, node X will get a value '1'. There are two inverters I2 and I3, to store and maintain the value of X. When the value of X is '1' transistor MP2 will turn off because of PMOS transistor.

When the clock is =1, for a short period of time transistors MN1 and MN4 will turn on ,whose period will be equal to the delay occurred from the pulse generator circuitry. Then if data at transistor MN2 comes with '1' then transistor MN2 will turn on and as node X stores the value '1' before the rising edge of the clock, then this node X will discharge through transistors MN1,MN2 and MN3, because Q b is at '1'. Hence the value of node X will become '0', which will turn on the transistor MP2 and MN5 will be turned off. Because of pull up path through transistor MP2, value at output Q will come as '1'.

When clock=1, for a short period of time transistors MN1 and MN4 will turn on , whose period will be equal to the delay occurred from the pulse generator circuitry. Then if data at transistor MN2 comes with '1' then transistor MN2 will turn on and as node X stores the value '1' before the rising edge of the clock, then this node X will discharge through transistors MN1,MN2 and MN3, because Q b is at '1'. Hence the value of node X will become '0', which will turn on the transistor MP2 and MN5 will be turned off. Because of pull up path through transistor MP2, value at output Q will come as '1'.

2.4 Signal feed through scheme flip flop (SFTFF) [17]:-

All the previous circuits suffer worst case delay from '0' to '1' transition and this delay is improved by signal feed through scheme. This design also adopts a static latch like SCDFE [16] and also a conditional feedback control system to avoid discharging of the internal node X. Three things are different in this design from the previous ones.

In first stage, use of Weak PMOS pull up transistor in which gate is connected to ground .which forms a pseudo NMOS circuitry and used as a charge keeper circuitry. It also reduces the node X load capacitance [24-25].

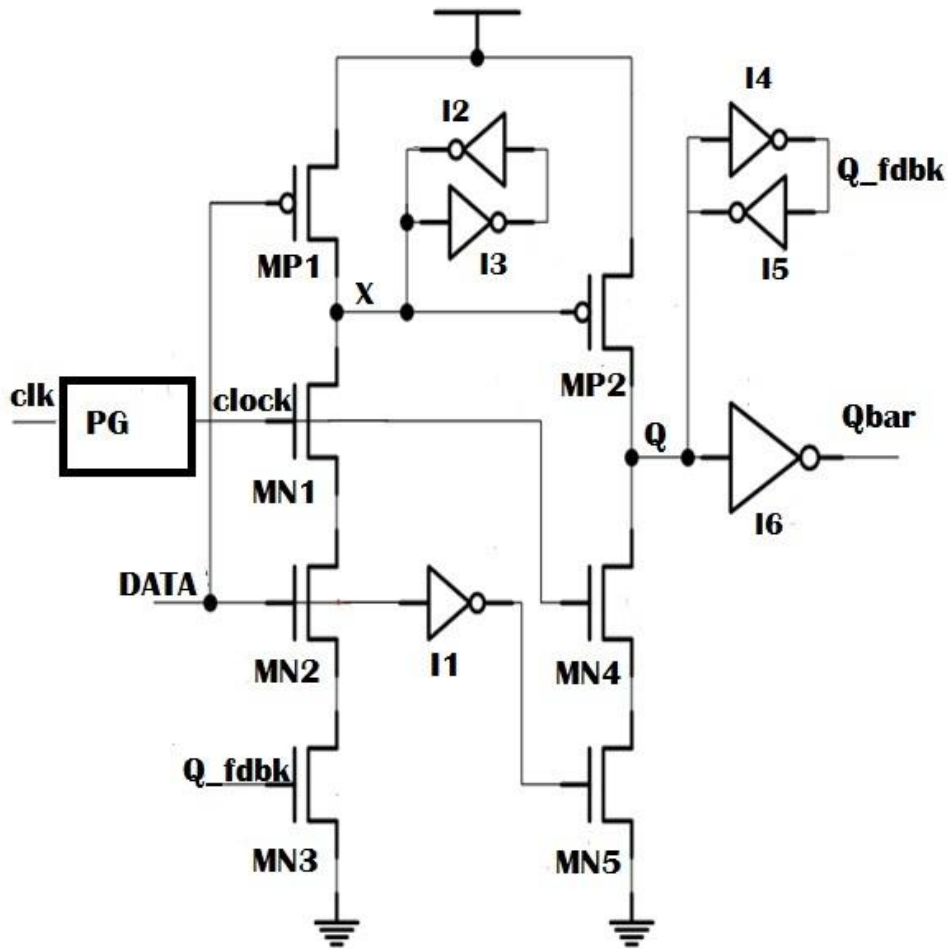


Fig. 2.3 Circuit diagram of SCDF [16]

To derive the output Q directly, there is inclusion of a pass transistor named as MNx which is controlled by the clock pulse, as there is signal driving from the MP2 transistor, MNx also helps in signal driving of input to the output Q. There is complete removal of second stage pull down network and here MNx will provide the path for discharging .

There are two roles played by transistor MNx, provides driving of data to output Q and also discharging of output node Q from '1' to '0' transitions. When we compare this scheme with the previously used flip flop circuitry (SCDF), we save power of two inverters used for keeper circuitry, two NMOS transistors used for pull down network and also the inverter used as a controller.

Considering Fig 2.4, flip flop has two stages, in stage one there is capturing of '0' to '1' transition and stage 2 has capturing of '1' to '0' transition.

We use four inverters and a NAND gate in the pulse generator to produce the single edge triggered clock (pulsed clock).

When clock=1, if there is no transition of data, means output Q and the data at input are at the same level. Then from the MNx transistor, current will pass, due to which it will keep the flip flop's input stage without any effort.

At this time also the inverted output feedback control transistor and the data input will have complementary levels of signals and hence node X pull down path will be off. Hence there will be no switching of signals at the internal nodes.

When clock=1, for a short period of time transistors MNx and MN3 will turn on, whose period will be equal to the delay occurred from the pulse generator circuitry. Then if data at transistor MN2 changes with '1' from '0' then transistor MN1 will turn on and as node X stores the value '1' before the rising edge of the clock, then this node X will discharge through transistors MN1, MN2 and MN3, because Qb is at '1'. Hence the value of node X will become '0', which will turn on the transistor MP2 and also there is direct signal driving of data '1' through transistor MNx. Because of pull up path through transistor MP2, value at output Q will come as '1'. Hence delay will be less than previous flip flops because of this extra driving effort.

When data changes with '0' from '1' at transistor MN1, it will be turned off because of the N transistor, as node X stores value '1' before the rising edge of the clock, it will turn off the MP2 transistor, output Q will be connected to ground by pull down network through transistors MNx and MN5 and Q will acquire a value '0'. Keepers I1 and I2 are used to maintain output value.

2.5 Novel design of low power pulse triggered D flip flop [18]

It uses a four transistor pulse generator (4TPG) against three inverters and a NAND gate in previously described flip flops. The latch circuitry is modified to reduce the power dissipation. Data input is controlled by transmission gate T1 here.

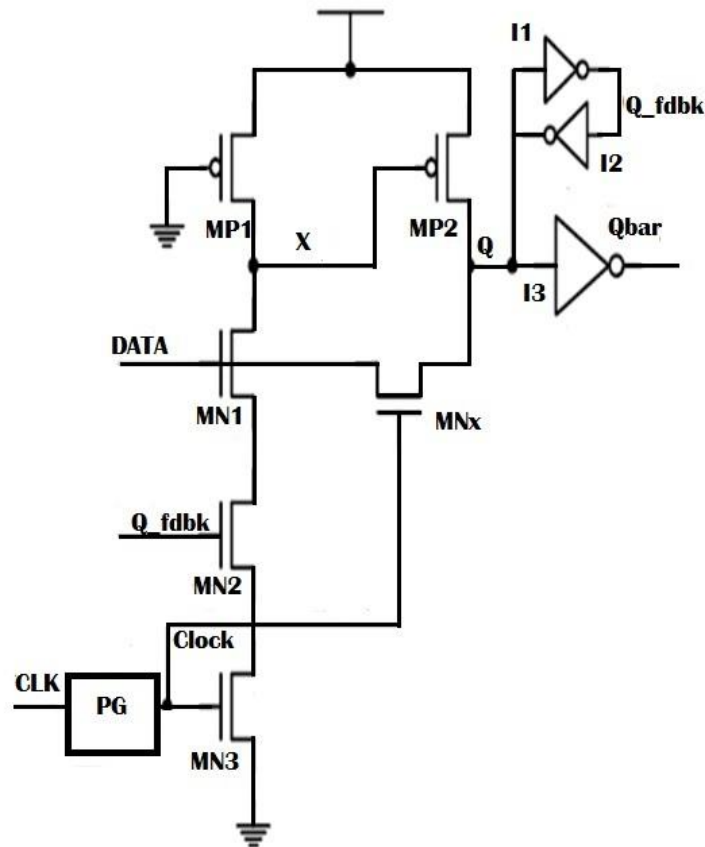


Fig 2.4 Circuit diagram of SFTFF [17]

2.5.1 The 4 TPG architecture [18]

Here modified pulse generator consists only 4 transistors. As the clock circuitry consumes a lot of amount of power, hence this circuitry is best from the previous ones. In previous pulse generators there are multiple numbers of transistors are in use to produce delay but here (as shown in Fig. 3.1) only a single inverter is being used to produce pulse clock.

When CLOCK =0 then because of P transistor only CP0 transistor will be on and other CN2,CN1,CN3 transistors will be off because of the N transistors due to which node Z will acquire a value '1'.

When the CLOCK =1 then CP0 transistor will be off and then instantly transistor CN3 will turn on because the size of the transistor CN3 is large than that of transistors CN1 and CN2. And due to which transistors CN1 and CN2 will also turn on after a small

instant of time after transistor CN3. Hence a small pulse will pass through the transistor CN3 because node Z will be discharged from the transistors CN1 and CN2 and will become zero. And only a small clock pulse will pass through the transistor CN3 (CLK) which will be enough to drive the latch circuitry and a care must be taken of this pulse width because it will be very narrow. We must take care that the size of transistors CN1 and CN2 must be small than the transistor CN3 to produce a clock pulse (CLK) enough to drive the latch circuitry.

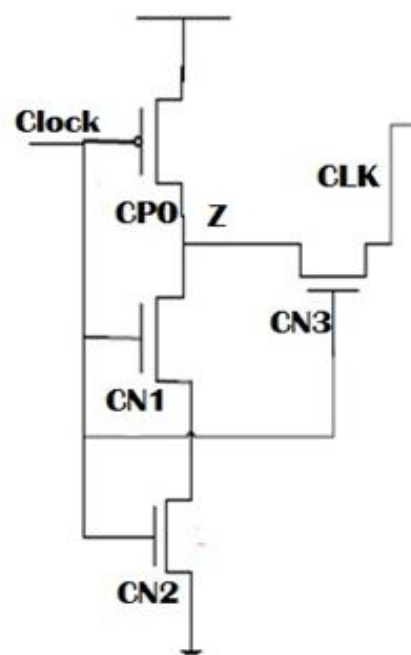


Fig 2.5 Circuit diagram of 4TPG [18]

We use our inverter and a pass transistor in the pulse generator to produce the single edge triggered clock (pulsed clock).

When clock=1, for a short period of time transistors N1 and N4 will turn on whose period will be equal to pulse duration from the pulse generator circuitry. Now if data at transmission gate T1 comes with '0' then transistor P0 will turn on and as transistor N4 will turn on because of clock pulse, data '0' will pass through the transistor N4 because it will work as a pass transistor.

When data comes as '0' at transmission gate T1, it will turn on the P0 transistor, as Q was at '1' previously it will turn off the transmission gate T1, will turn on MNQ transistor and MNQ will be connected to the transistor N2 and N2 will be connected to ground through it and will turn off transistor N2, as node X stores the value '0' before the rising edge of the clock, but it will attain a value '1' because of pull up path formed by transistor P0 and it will not discharge as transistor N2 is off. It will turn off transistor P2 and because of pull up transistor. As both N1 and N4 transistor are turned on because of clock pulse, data '0' will pass through this pass transistor N4. output Q will attain '0' from this path. Keepers I1 and I2 are used to maintain output value.

In the hold mode of the circuit, when we do careful analysis, we get that due to charging and discharging of the internal node X, there is a consumption of significant amount of energy. When the input is at '1', node x is at '1' before the rising edge of the clock and when input remains same at '1' after the rising edge of the clock, this node will discharge through transistors N1 and N2. But there is also a transistor N3 like the previous ones to stop discharging this node and will save power dissipation.

2.6 Functional Verification and Comparison

The operation of PT flip flops described in sections 2.1 to 2.5 is verified through simulations in Cadence Virtuoso environment. The power supply of 1V and 90 nm technology parameters are used throughout simulations.

2.6.1 Simulations results of EP-DCO FF[14]

The EP-DCO FF of Fig. 2.1 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverters and NAND gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 2.1. The schematic of EP-DCO FF is shown in Fig. 2.1.

Table 2.1 Aspect Ratios of Transistors for EP DCO FF

Component		W/L
Inverter	PMOS	1.2
	NMOS	1.2
NAND	PMOS	1.2
	NMOS	10
P1		5
P2		1.2
N1		1.2
N2		1.2
N3		1.2
N4		12

To verify the functionality of EP-DCO FF, the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig. 2.8. The power waveforms are depicted in Fig. 2.9. The delay of 162.54ps was observed and the average power consumption is found to be 44.46 μ W.

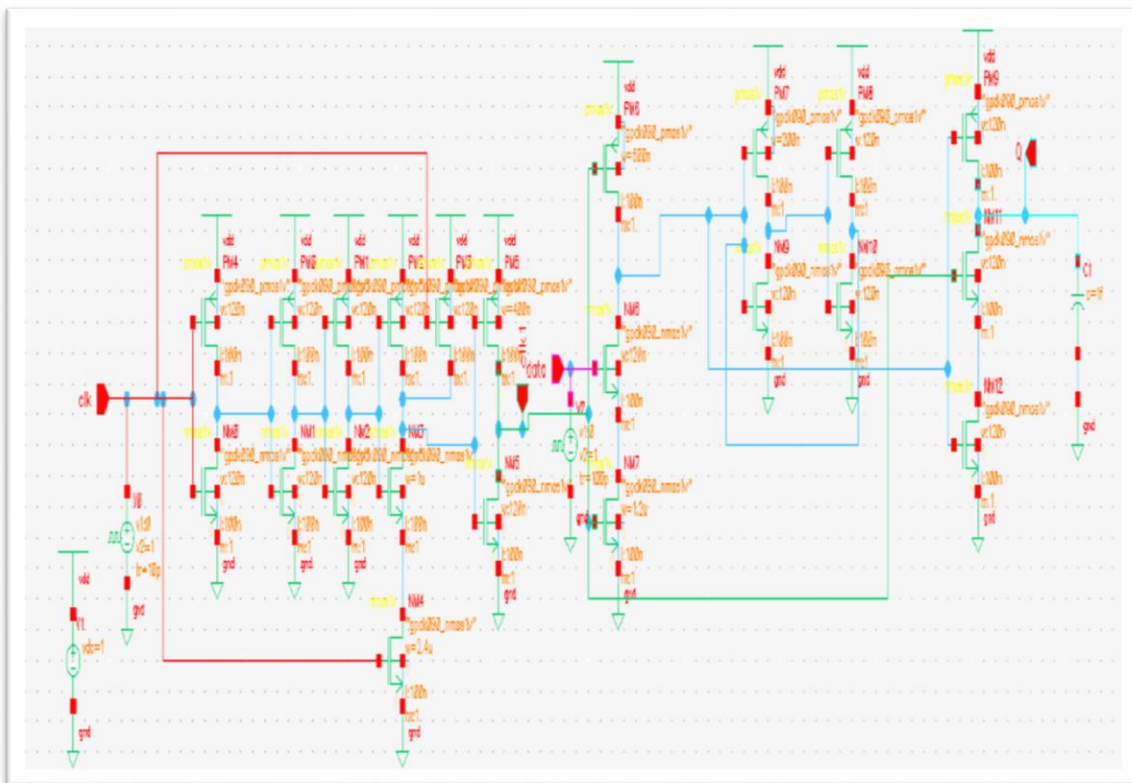


Fig 2.7 Schematic of EP-DCO FF

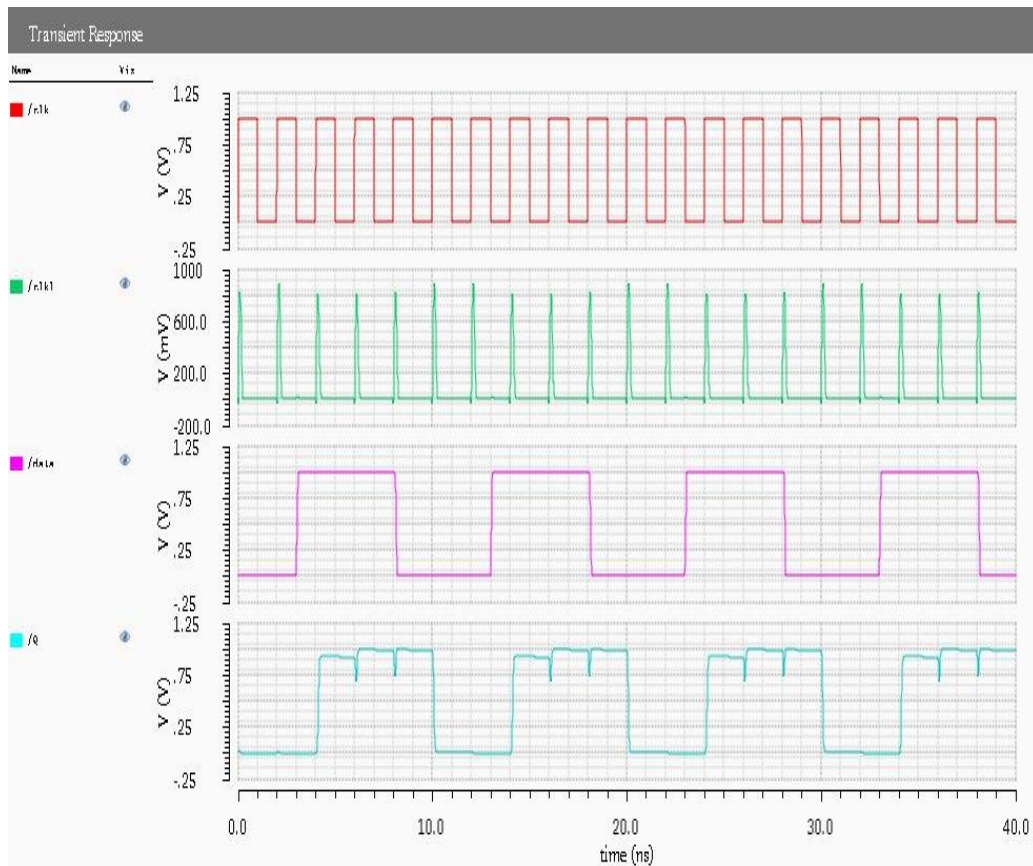


Fig.2.8 Timing waveform of EP-DCO FF schematic

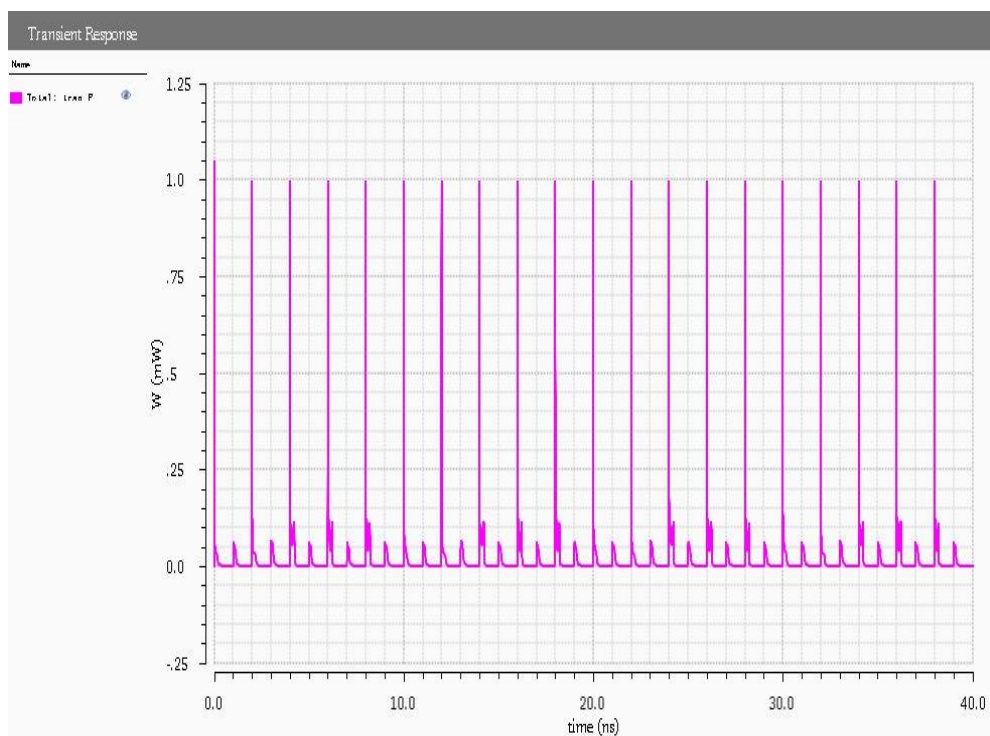


Fig.2.9 Power waveform of EP-DCO FF

2.6.2 Simulations results of CDFF [15]

The CDFF of Fig. 2.2 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverters and NAND gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 2.2. The schematic of CDFF is shown in Fig. 2.10.

Table 2.2 Aspect Ratios of Transistors for CDFF

Component		W/L
Inverter	PMOS	1.2
	NMOS	1.2
NAND	PMOS	1.2
	NMOS	10
P1		5
P2		1.2
N1		1.2
N2		1.2
N3		12
N4		1.2
N5		12

To verify the functionality of CD FF, the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig. 2.11. The power waveforms are depicted in Fig. 2.12. The delay of 180.66ps was observed and the average power consumption is found to be 24.72 μ W.

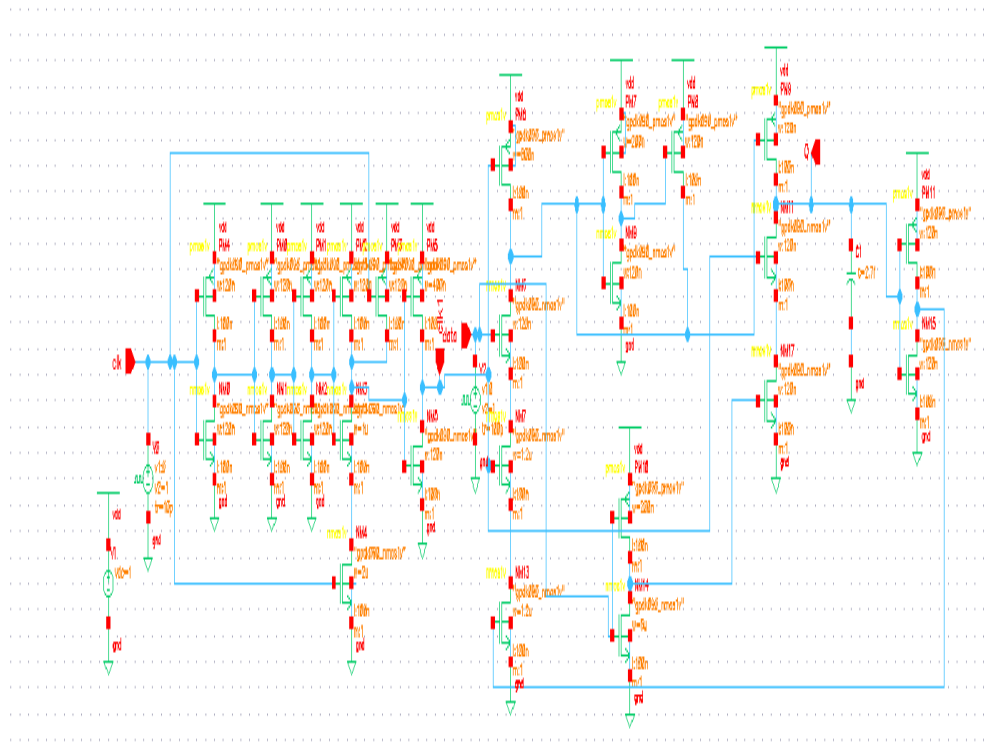


Fig 2.10 Schematic of CDFF

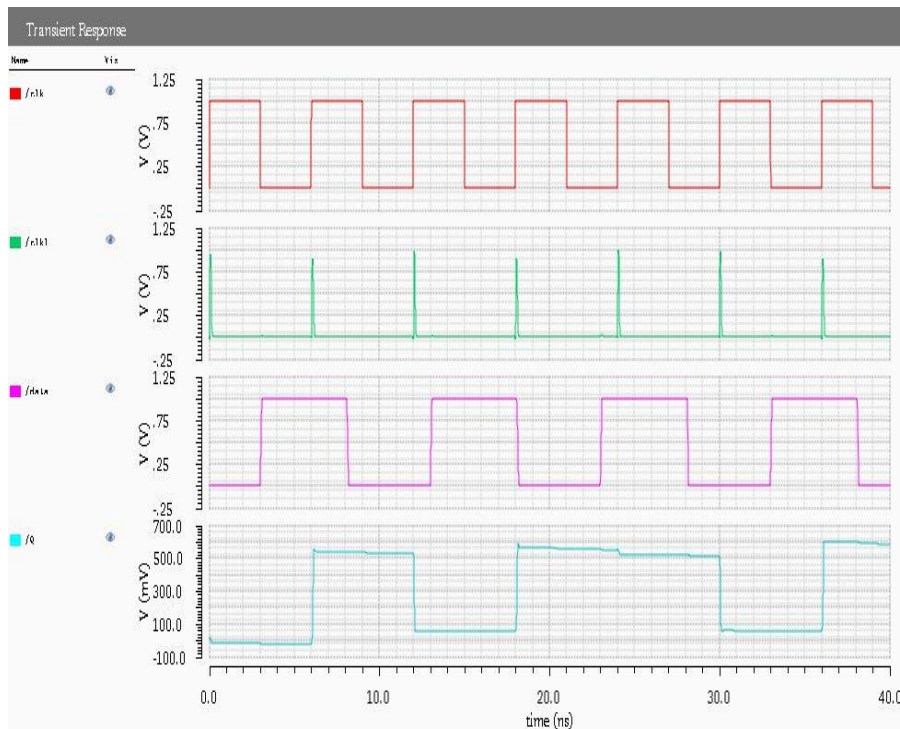


Fig.2.11 Timing waveform of CDFF schematic

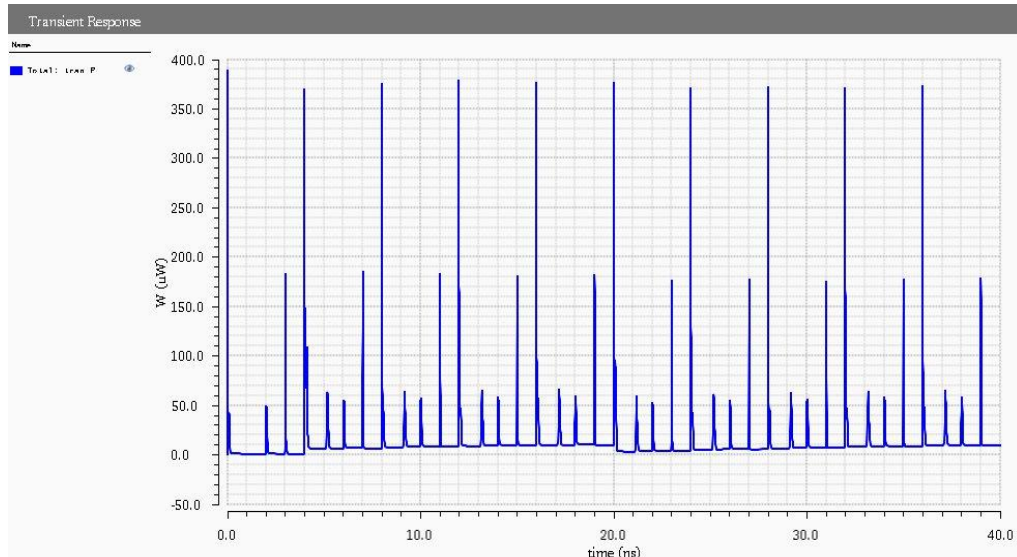


Fig.2.12 Power waveform of CDFFF

2.6.3 Simulations results of SCDFF [16]

The SCDFF of Fig. 2.3 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverters and NAND gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 2.3. The schematic of SCDFF is shown in Fig.2.13.

Table 2.3 Aspect Ratios of Transistors for SCDFF

Component		W/L
Inverter	PMOS	1.2
	NMOS	1.2
NAND	PMOS	1.2
	NMOS	10
P1		5
P2		1.2
N1		1.2
N2		1.2
N3		12
N4		1.2
N5		12

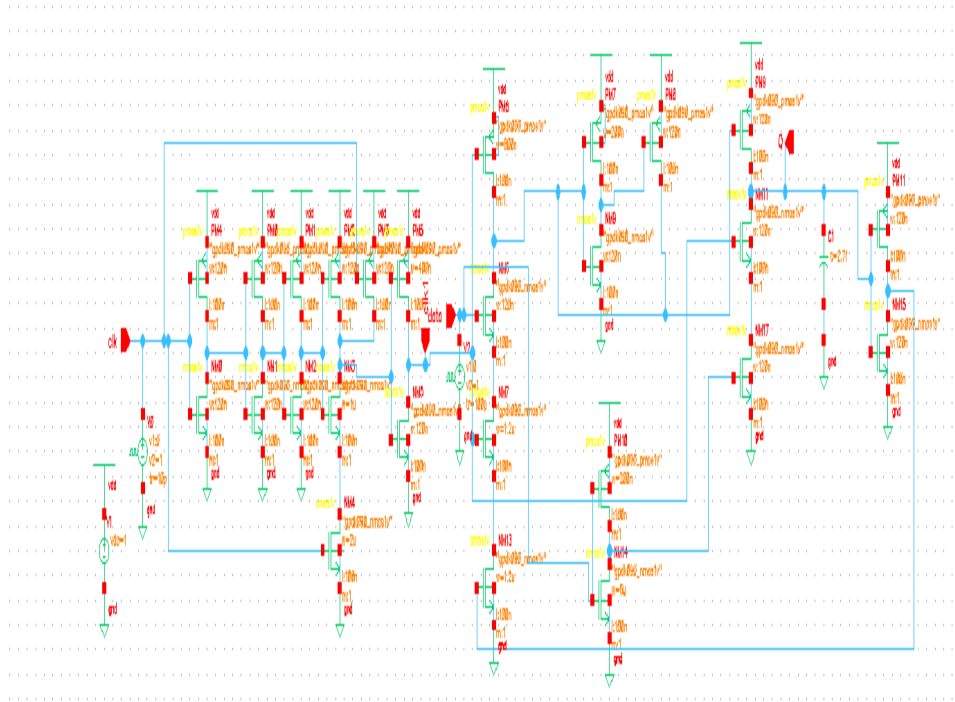


Fig 2.13 Schematic of SCDFF

To verify the functionality of SCDFF, the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig. 2.14. The power waveforms are depicted in Fig. 2.15. The delay of 188.73ps was observed and the average power consumption is found to be 21.26 μ W.

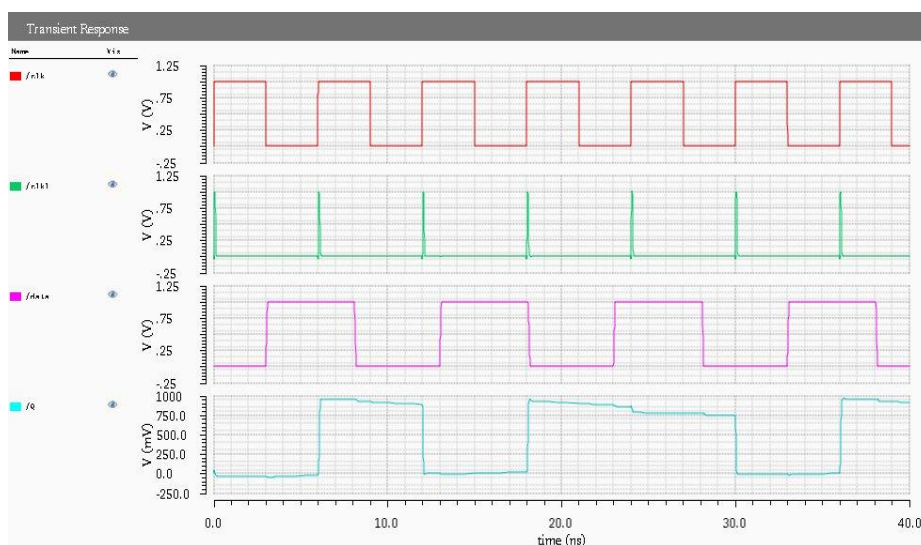


Fig. 2.14 Timing waveform of SCDFF schematic

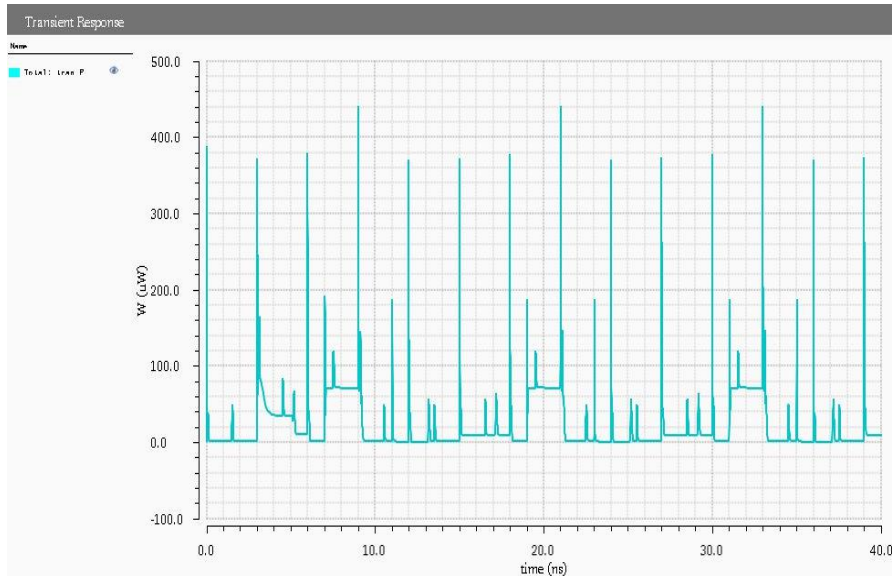


Fig.2.15 Power waveform of SCDF

2.6.4 Simulations results of SFTFF [17]

The SFTFF of Fig. 2.4 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverters and NAND gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 2.4. The schematic of SFTFF is shown in Fig. 2.16.

Table 2.4 Aspects Ratios of Transistors for SFTFF

Component		W/L
Inverter	PMOS	1.2
	NMOS	1.2
NAND	PMOS	1.2
	NMOS	10
MP1		1.2
MP2		8
MN1		1.2
MNx		1.2
MN2		2
MN3		10

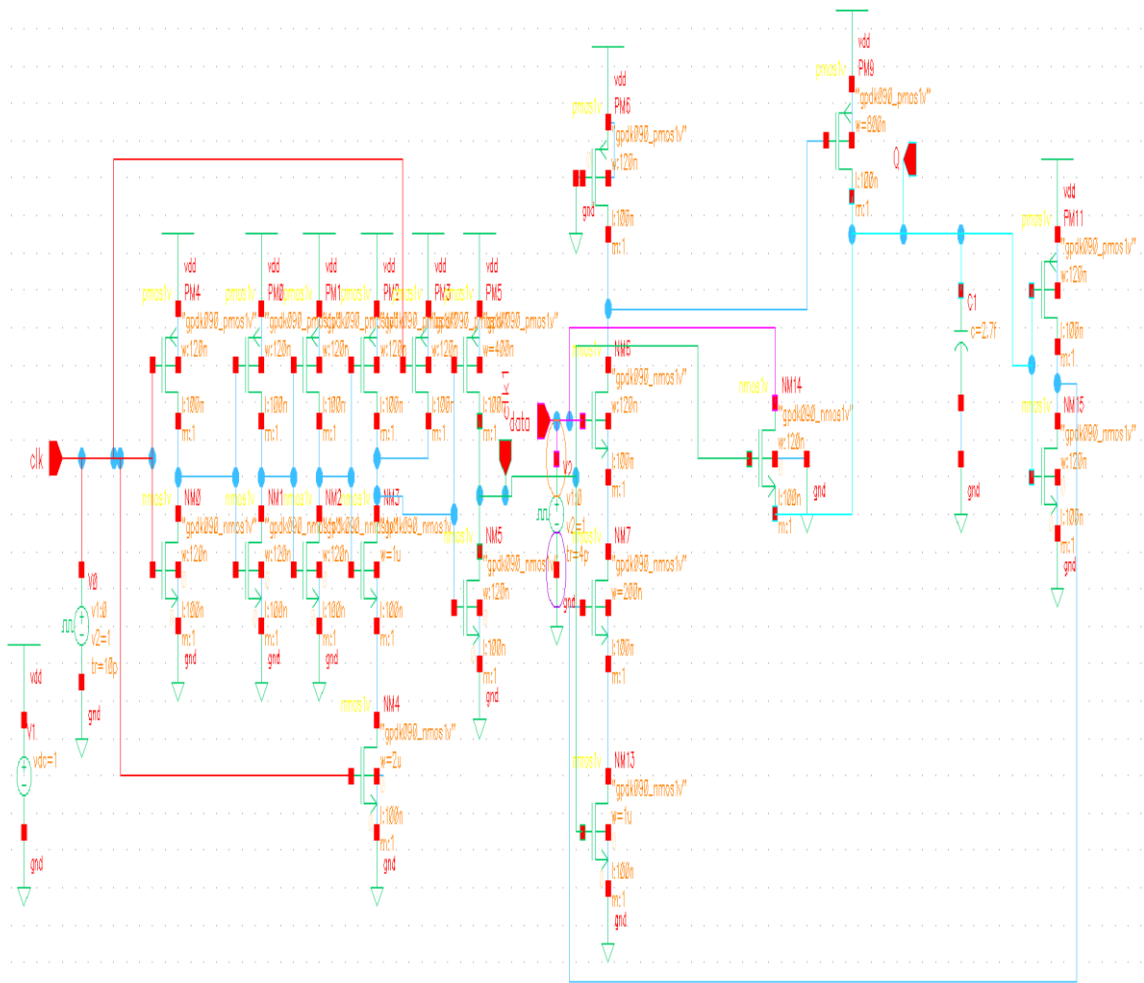


Fig 2.16 Schematic of SFTFF

To verify the functionality of SFTFF, the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig.2.17. The power waveforms are depicted in Fig.2.18. The delay of 149.34ps was observed and the average power consumption is found to be 13.38 μ W.

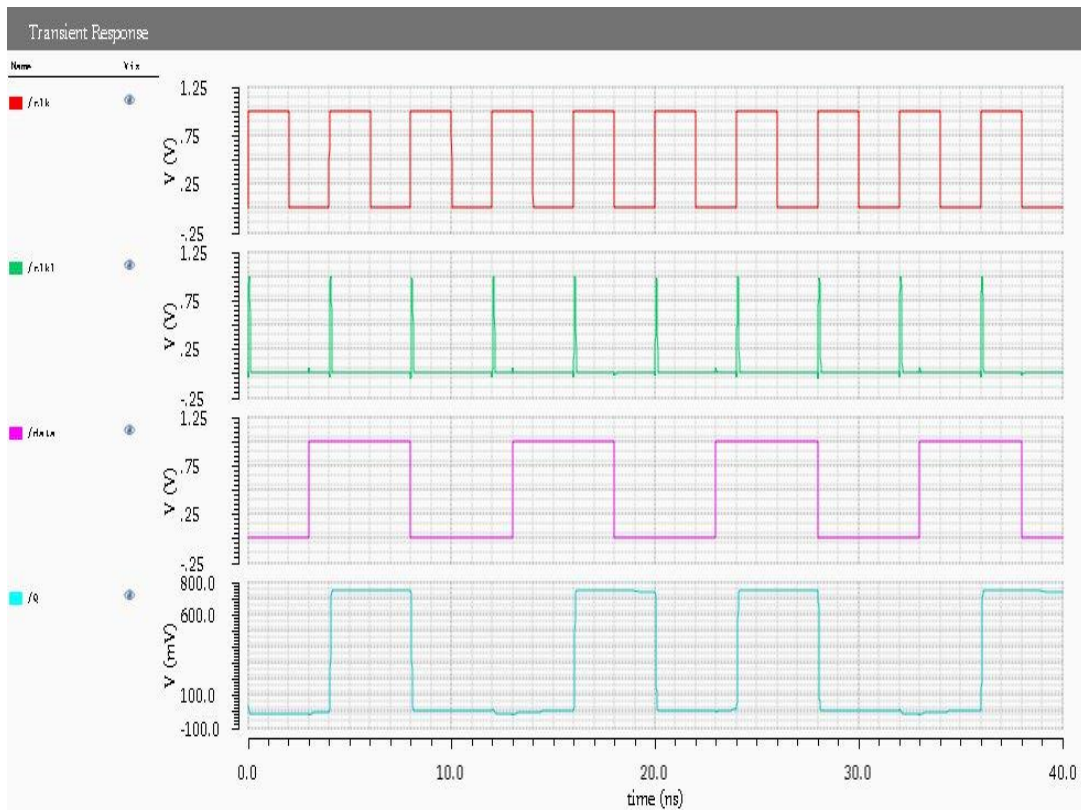


Fig.2.17 Timing waveform of SFTFF schematic

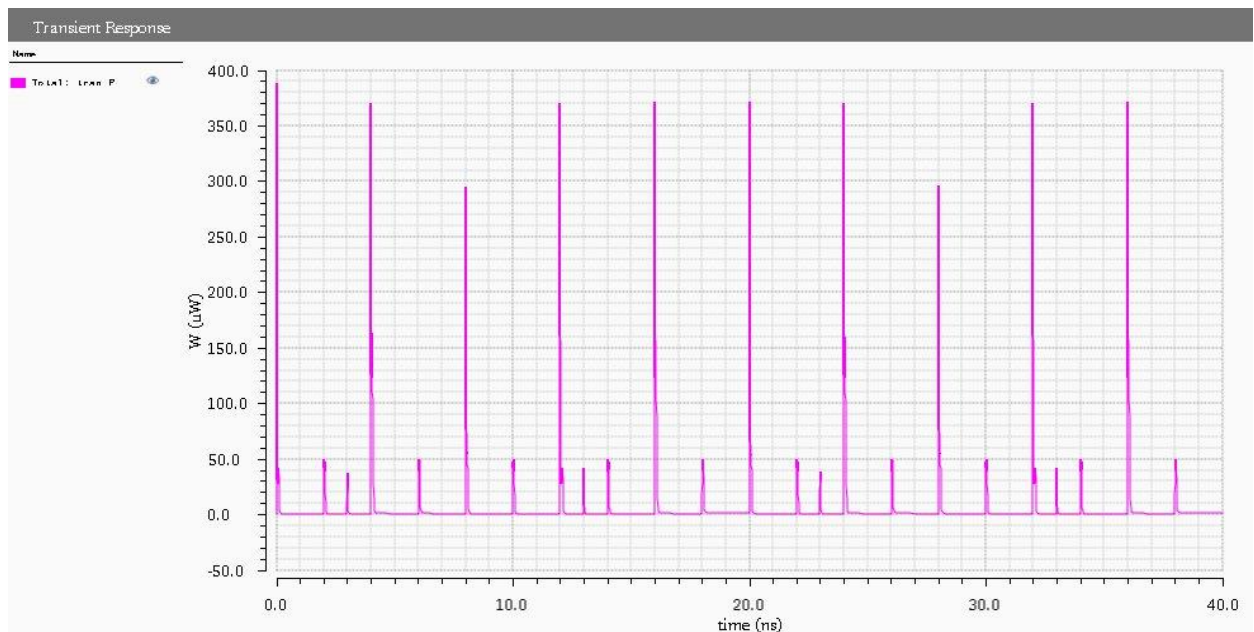


Fig.2.18 Power waveform of SFTFF

2.6.5 Simulations results of Novel design of low power flip flop[18] :-

The novel design of low power flip flop of fig. 2.5 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverter gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 2.5. The schematic of novel design of low power flip flop of is shown in Fig. 2.19

Table 2.5 Aspect Ratios of Transistors for Novel design flip flop

Component		Aspect ratio
CPO		52
CN1		1.2
CN2		1.2
CN3		30
P0		2
P2		7.6
N1		6
N2		6
N3		6
N4		1.2
MNQ		1.2
T1	PMOS	1.2
	NMOS	1.2

To verify the functionality of novel design of low power flip flop, the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig. 2.20. The power waveforms are depicted in Fig. 2.21. The delay of 128.83ps was observed and the average power consumption is found to be 4.32 μ W.

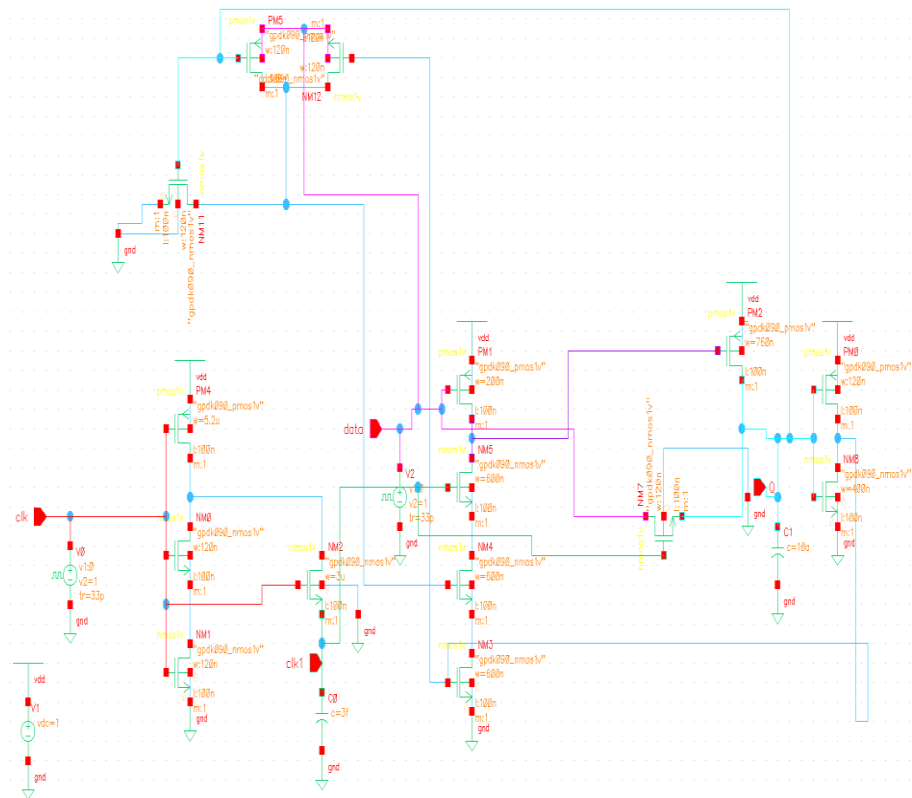


Fig 2.19 Schematic of Novel design of low power flip flop

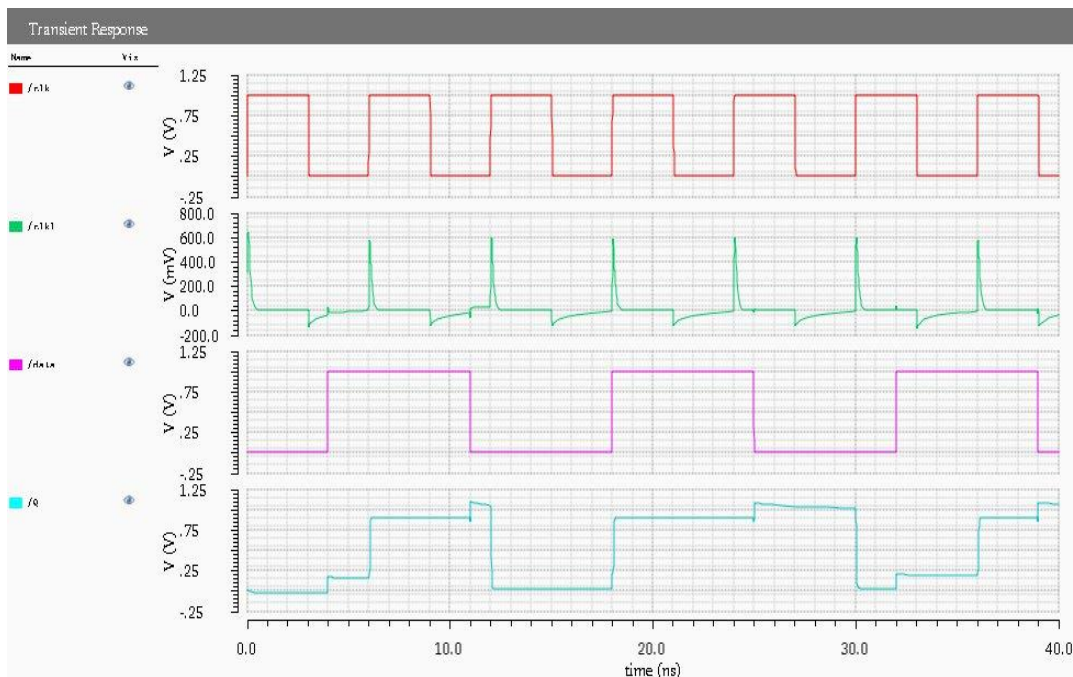


Fig.2.20 Timing waveform of Novel design of low power flip flop schematic

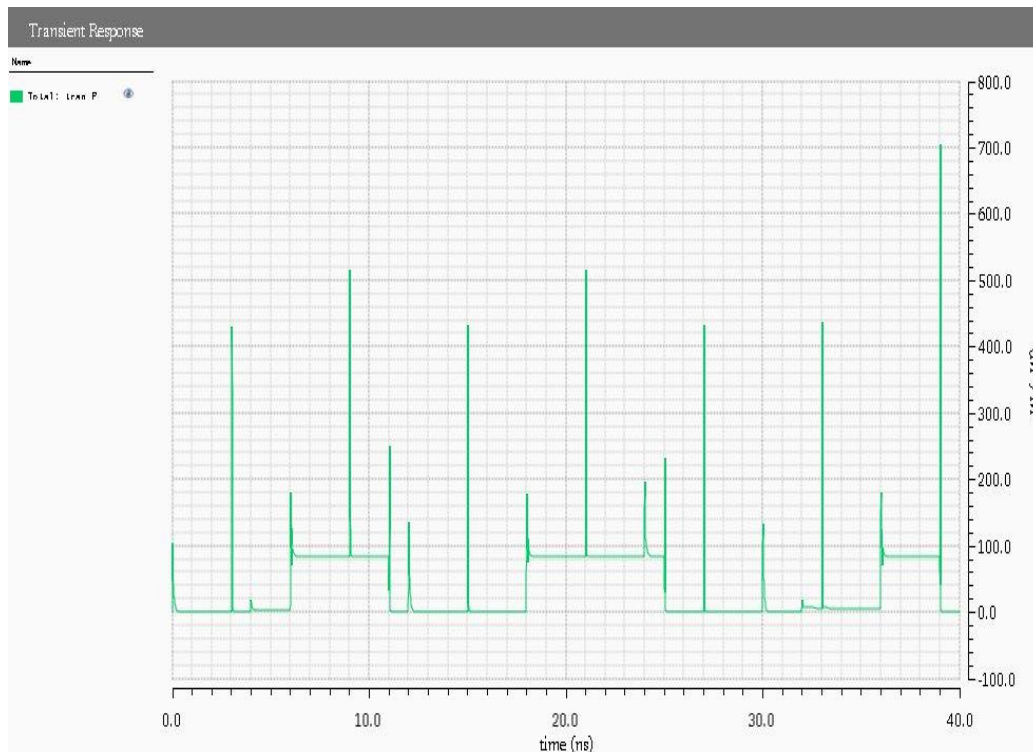


Fig 2.21 Power waveform of novel design of low power flip flop

2.6.6 Comparison

In this section the transistor count, average power consumption and delay of various PT flip flops are compared and the observations are placed in Table 2.6. It may be noted that the transistor count, power consumption and delay for Novel design of low power D flip flop is minimum.

Table 2.6 Comparison Table

Flip flop	No of transistors	Average.power consumption(uW)	Delay (ps)
EP-DCO FF	28	44.46	162.54
CDFP	30	24.72	180.66
SCDFP	31	21.26	188.73
SFTFF	24	13.38	149.34
Novel design of low power D flip flop	17	4.32	128.83

CHAPTER 3

Flip Flops Using Four Transistor Pulse Generator

The PT flip flops described in chapter 2 majorly use pulse generator comprising of three inverters and one NAND gate. The PT of novel design of low power pulse triggered flip flop use only four transistors for pulse generation and is referred as 4TPG in context of the present work. The chapter examines the functionality of EP-DCO FF, CDFE, SCDFE and SFTFE PT flip flops with 4 TPG using simulations in Cadence Virtuoso. The performance is compared with the results presented in Chapter 2.

3.1 EP-DCO FF [14] with 4 TPG

The circuit diagram of EP-DCO FF with 4TPG is shown in Fig. 3.1. The simulations are carried out using the aspect ratios of various transistors given in table 3.1. To verify the functionality of circuit, the clock of frequency 500MHz is applied to 4TPG.

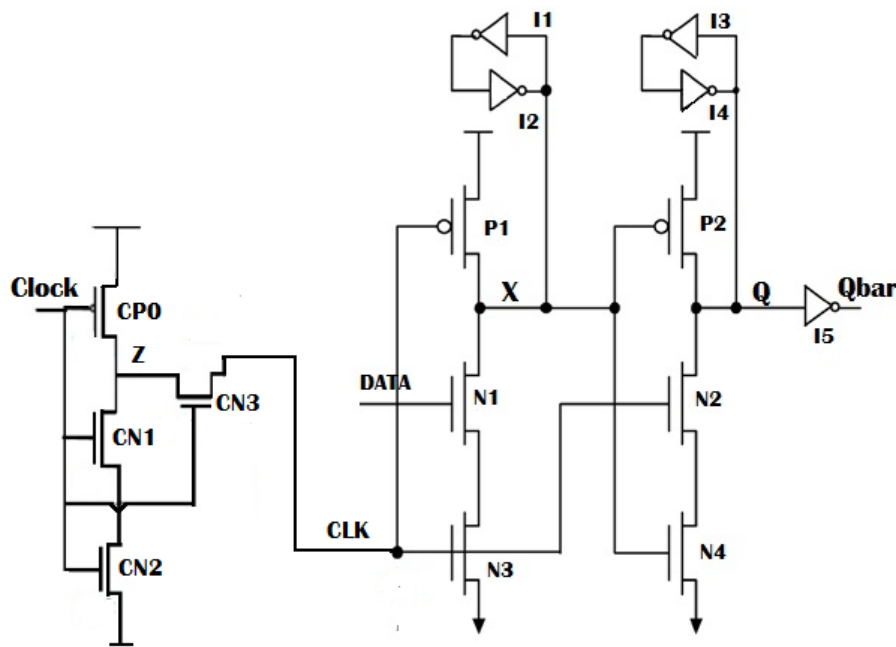


Fig. 3.1 EP-DCO FF with 4 TPG

The aspect ratios of various transistors are placed in Table 3.1. The schematic drawn in Cadence Virtuoso is given in Fig. 3.2.

Table 3.1 Aspect Ratios of Transistors for EP DCO FF with 4 TPG

Component		Aspect ratio
INVERTER	NMOS	1.2
	PMOS	1.2
CPO		52
CN1		1.2
CN2		1.2
CN3		7
P1		1.8
P2		1.2
N1		1.2
N2		1.2
N3		1.2
N4		12

The timing waveforms of applied clock generated pulse, input and output are shown in Fig.3.3. It may be noted that a pulse is generated when the clock makes a low to high transition. The output is changed according to input with according to the pulse and retains the value till next pulse is generated. The delay of 160.23ps is observed. Further, power waveforms are also obtained through simulations and are depicted in Fig.3.4. Simulated average power consumption is found to be 24.43uw.

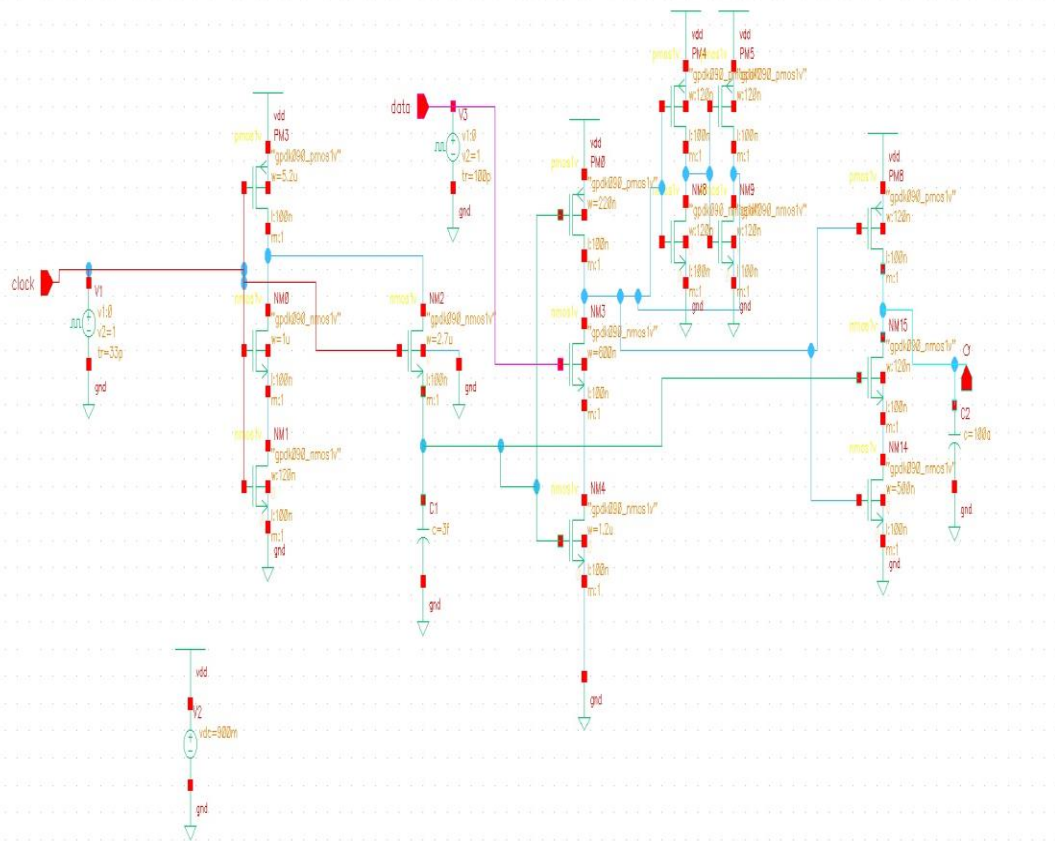


Fig 3.2 Schematic of EP-DCO FF with 4 TPG

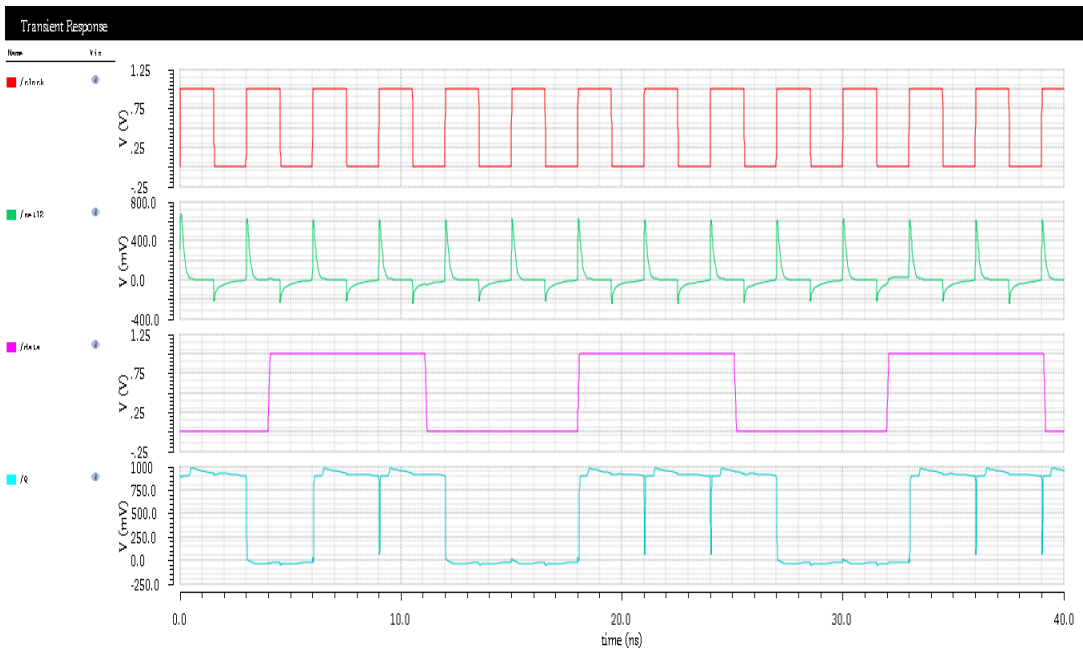


Fig.3.3 Timing waveform of EP-DCO FF with 4 TPG schematic

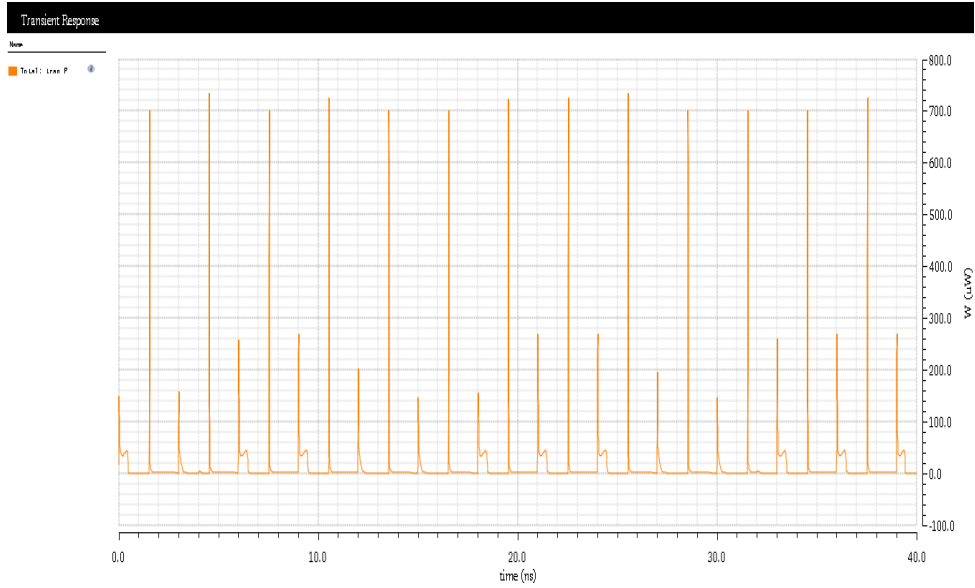


Fig.3.4 Power waveform of EP-DCO FF with 4 TPG

3.2 CDFE [15] with 4 TPG

The circuit diagram of CDFE with 4TPG is shown in Fig.3.5. The simulations are carried out using the aspect ratios of various transistors given in Table 3.2. The schematic drawn in Cadence Virtuoso is given in Fig.3.6. To verify the functionality of circuit, the clock of frequency 500MHz is applied to 4TPG.

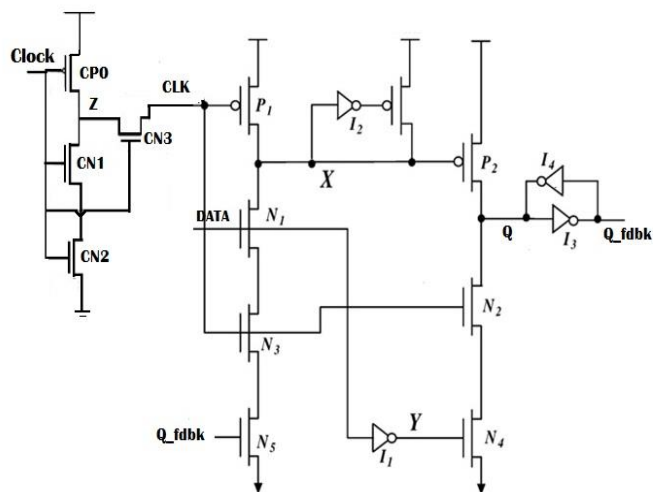


Fig. 3.5 CDFE with 4 TPG

Table 3.2.Aspect Ratios of Transistors for CDFE with 4 TPG

Component		Aspect ratio
INVERTER	NMOS	1.2
	PMOS	1.2
CPO		52
CN1		1.2
CN2		1.2
CN3		27
P1		3.6
P2		1.2
N1		6
N2		20
N3		12
N4		12
N5		1.2

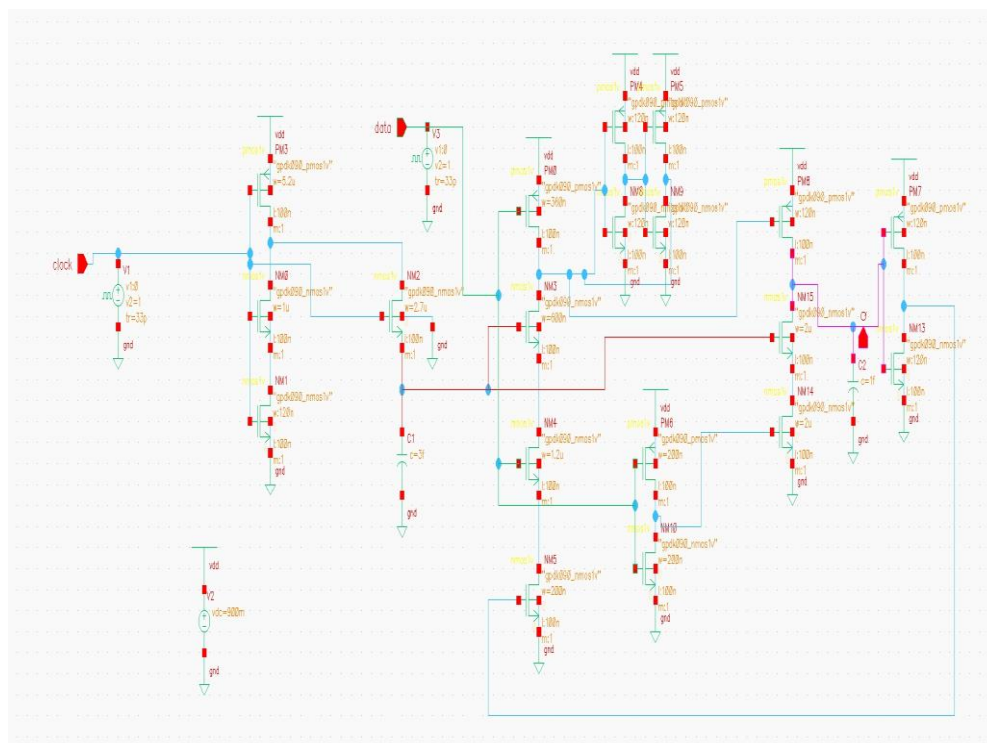


Fig. 3.6 Schematic of CDFE with 4 TPG

The timing waveforms of applied clock generated pulse ,input and output are shown in Fig. 3.7.It may be noted that a pulse is generated when the clock makes a low to high transition. The output is changed according to input with according to the pulse and retains the value till next pulse is generated. The delay of 178.47ps is observed. Further, power waveforms are also obtained through simulations and are depicted in Fig. 3.8. Simulated average power consumption is found to be 13.34 μ w.



Fig.3.7 Timing waveform of CDFD schematic with 4 TPG

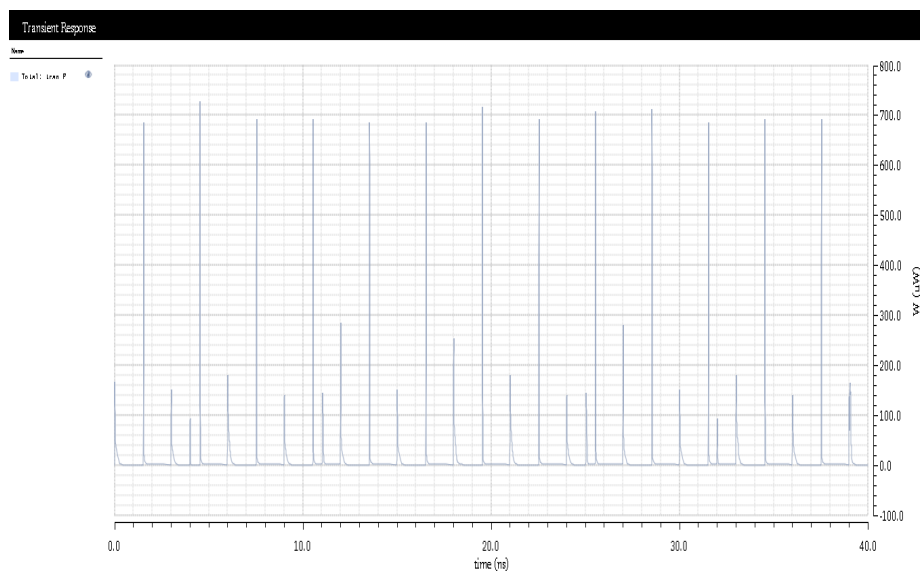


Fig.3.8 Power waveform of CDFD with 4 TPG

3.3 SCDFE [16] with 4 TPG

The circuit diagram of SCDFE with 4TPG is shown in Fig.3.9. The simulations are carried out using the aspect ratios of various transistors given in Table 3.3. The schematic drawn in Cadence Virtuoso is given in Fig. 3.10. To verify the functionality of circuit, the clock of frequency 500MHz is applied to 4TPG.

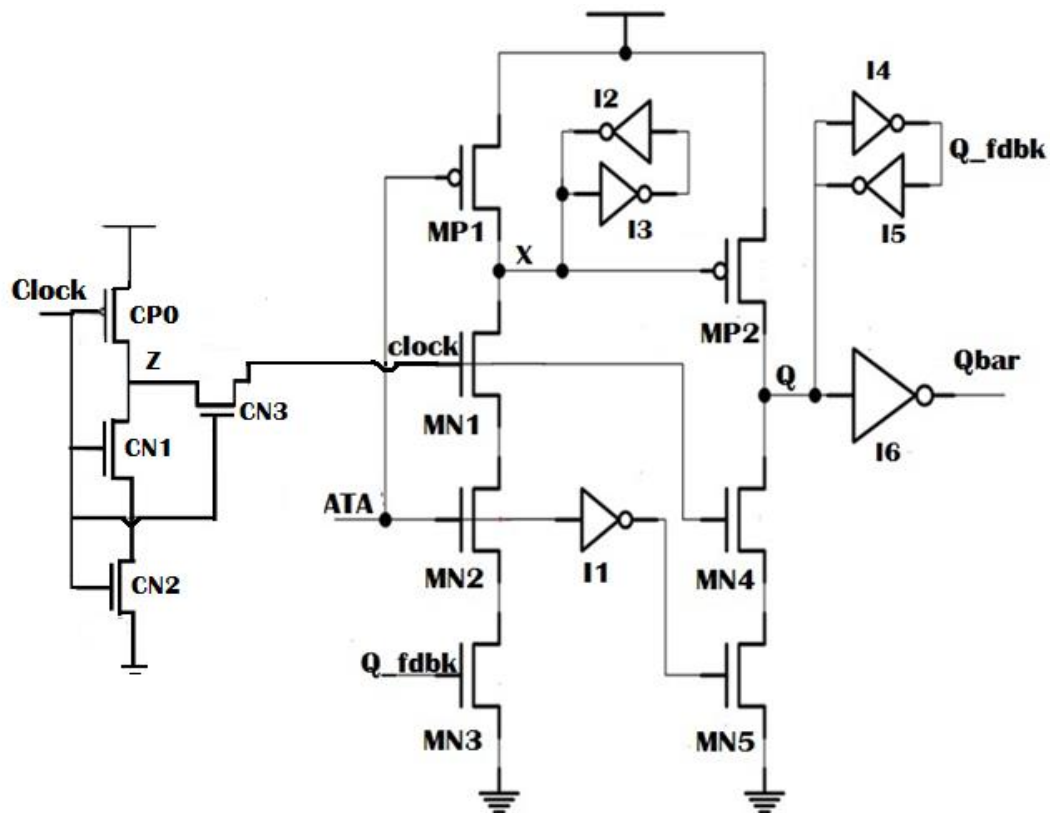


Fig. 3.9 Circuit diagram of SCDFE with 4 TPG

The timing waveforms of applied clock generated pulse, input and output are shown in Fig. 3.11. It may be noted that a pulse is generated when the clock makes a low to high transition. The output is changed according to input with according to the pulse and retains the value till next pulse is generated. A delay of 186.69ps is observed. Further, power waveforms are also obtained through simulations and are depicted in Fig. 3.12. Simulated average power consumption is found to be 12.74 uw.

Table 3.3 Aspect Ratios of Transistors for SCDFE with 4 TPG

Component		Aspect ratio
CPO		52
CN1		1.2
CN2		1.2
CN3		27
MP1		2.2
MP2		1.2
MN1		6
MN2		12
MN3		10
MN4		1.2
MN5		5
INVERTER	NMOS	1.2
	PMOS	1.2

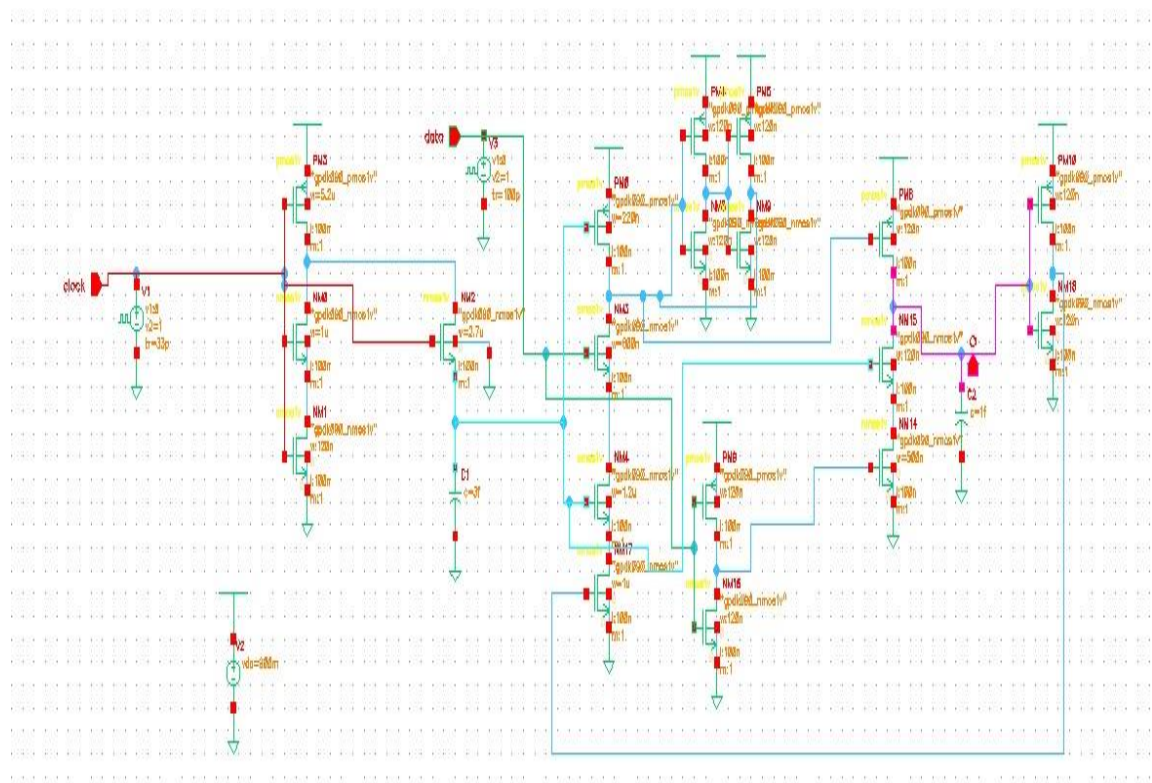


Fig.3.10 Schematic of SCDFE with 4 TPG

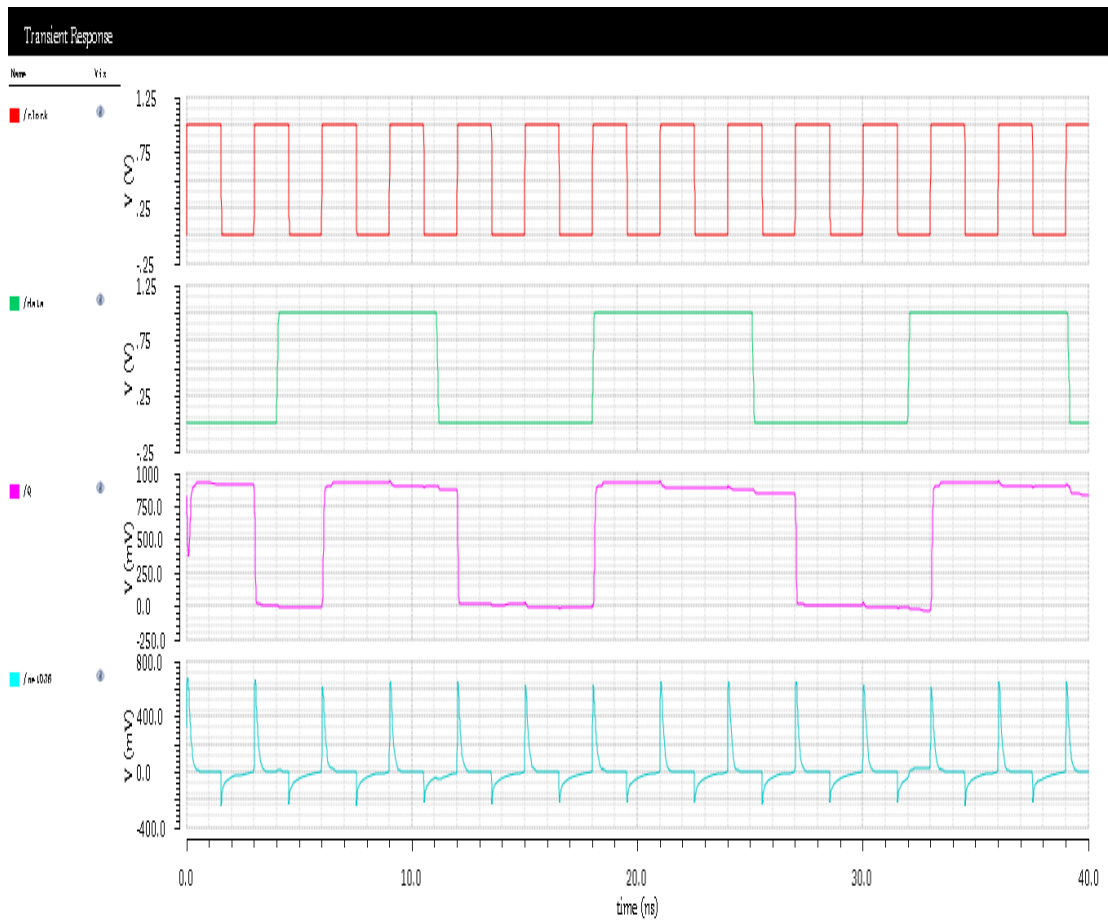


Fig.3.11 Timing waveform of SCDFF schematic with 4 TPG

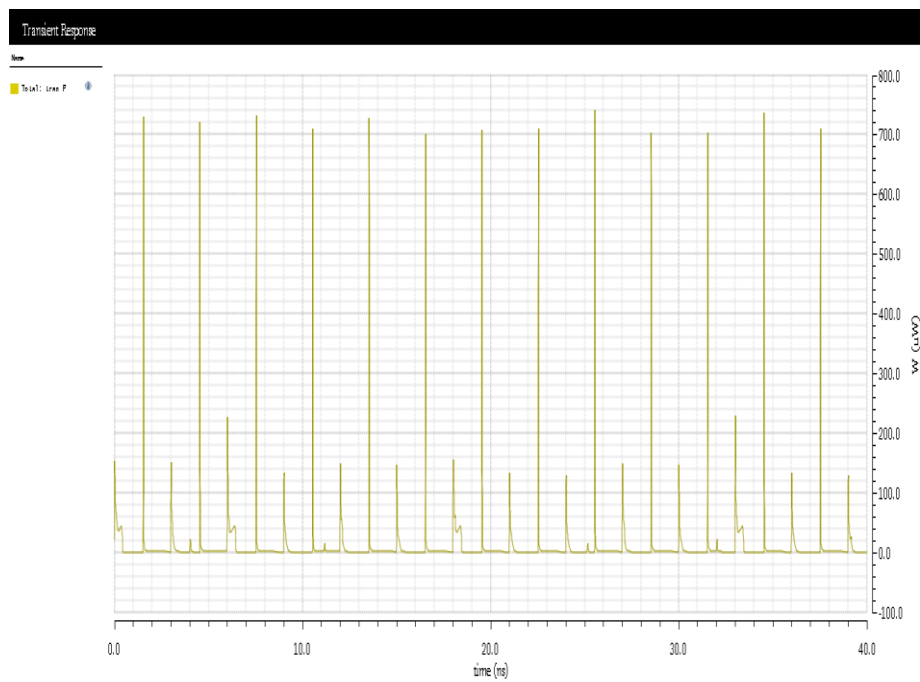


Fig.3.12 Power waveform of SCDFF with 4 TPG

3.4 SFTFF [17] with 4 TPG

The circuit diagram of SFTFF with 4TPG is shown in Fig. 3.13. The simulations are carried out using the aspect ratios of various transistors given in Table 3.4. The schematic drawn in Cadence Virtuoso is given in Fig. 3.14. To verify the functionality of circuit, the clock of frequency 500MHz is applied to 4 TPG.

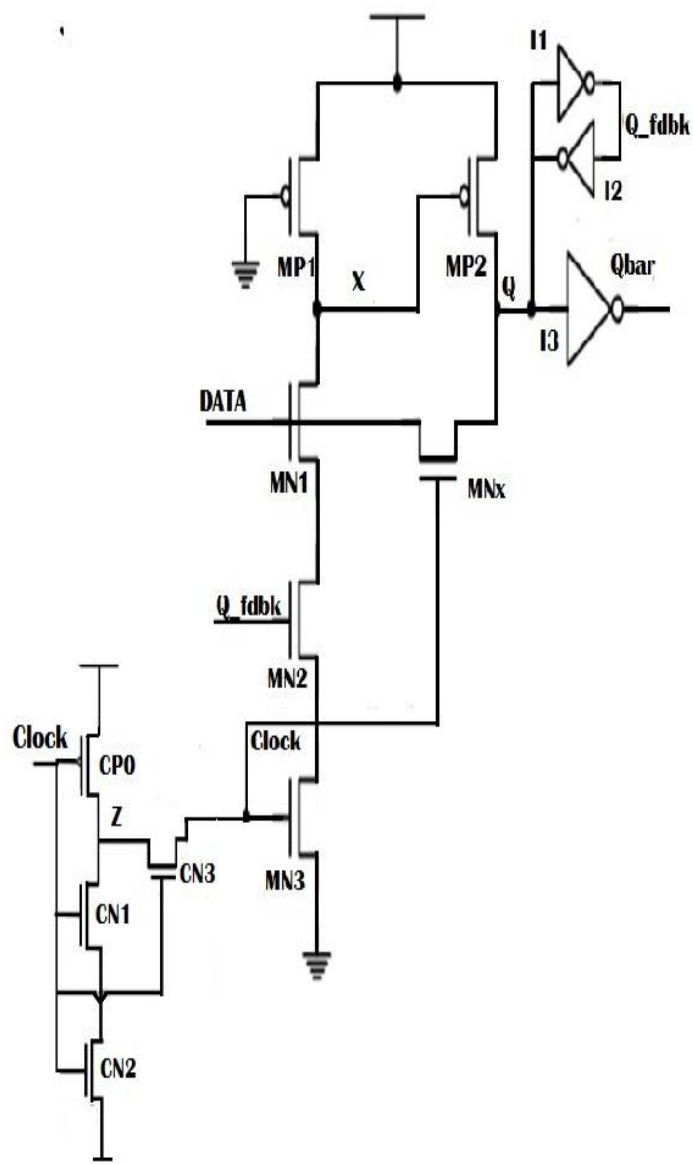


Fig. 3.13 Circuit diagram of SFTFF with 4 TPG

Table 3.4 Aspect Ratios of Transistors for SFTFF with 4 TPG

Component	Aspect ratio
CPO	52
CN1	1.2
CN2	1.2
CN3	27
MP1	1.2
MP2	2
MNx	1.2
MN1	10
MN2	10
MN3	10

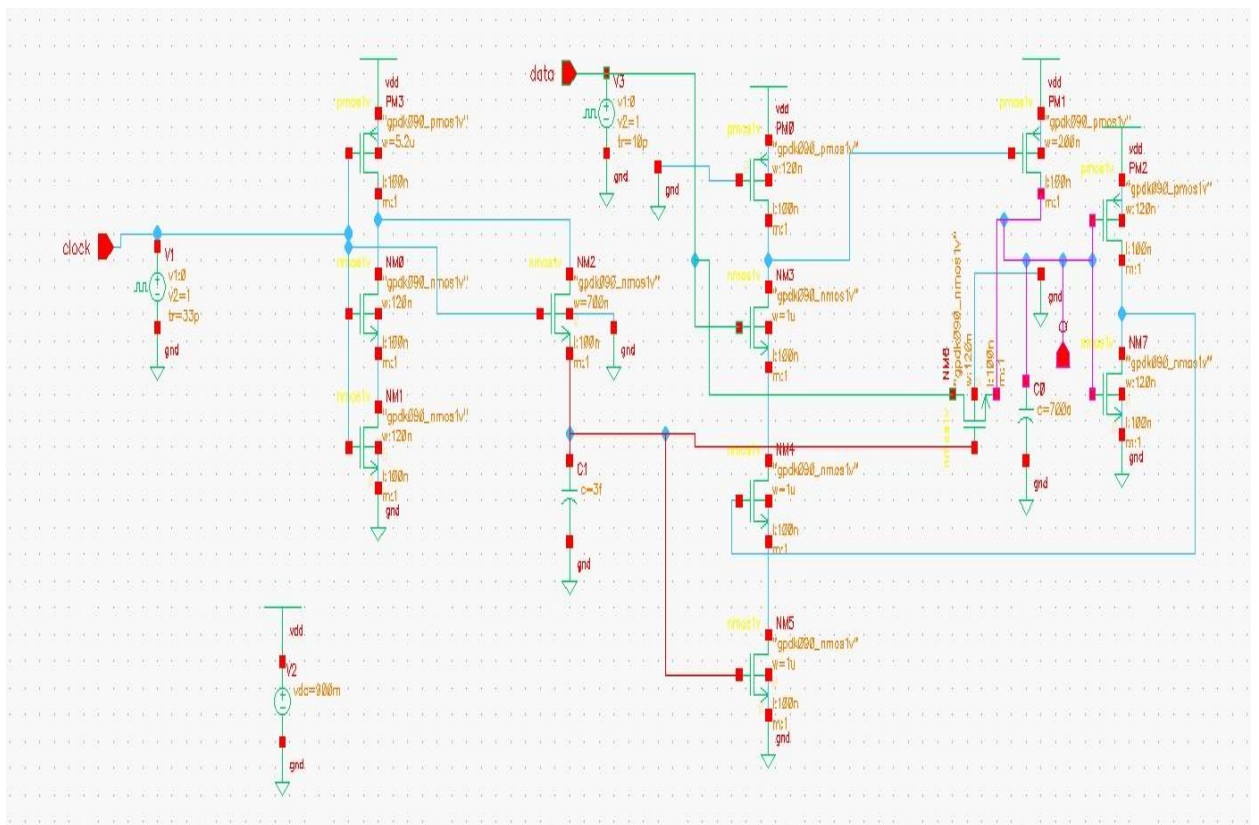


Fig 3.14 Schematic of SFTFF with 4 TPG

The timing waveforms of applied clock generated pulse, input and output are shown in Fig. 3.15. It may be noted that a pulse is generated when the clock makes a low to high transition. The output is changed according to input with according to the pulse and retains the value till next pulse is generated. The delay of 147.41ps is observed. Further, power waveforms are also obtained through simulations and are depicted in Fig. 3.16. Simulated average power consumption is found to be 6.47 uw.

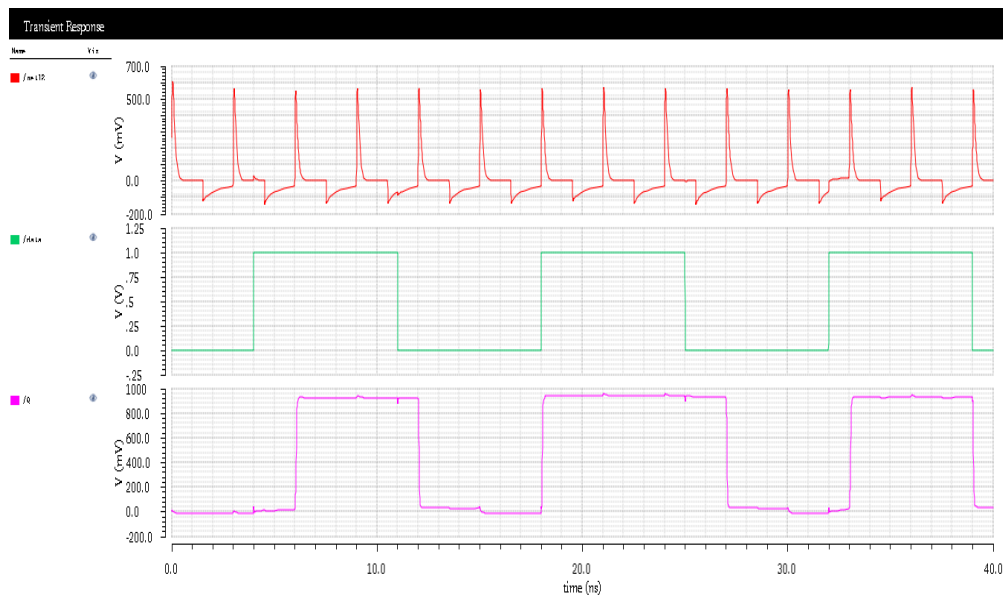


Fig.3.15 Timing waveform of SFTFF schematic with 4 TPG

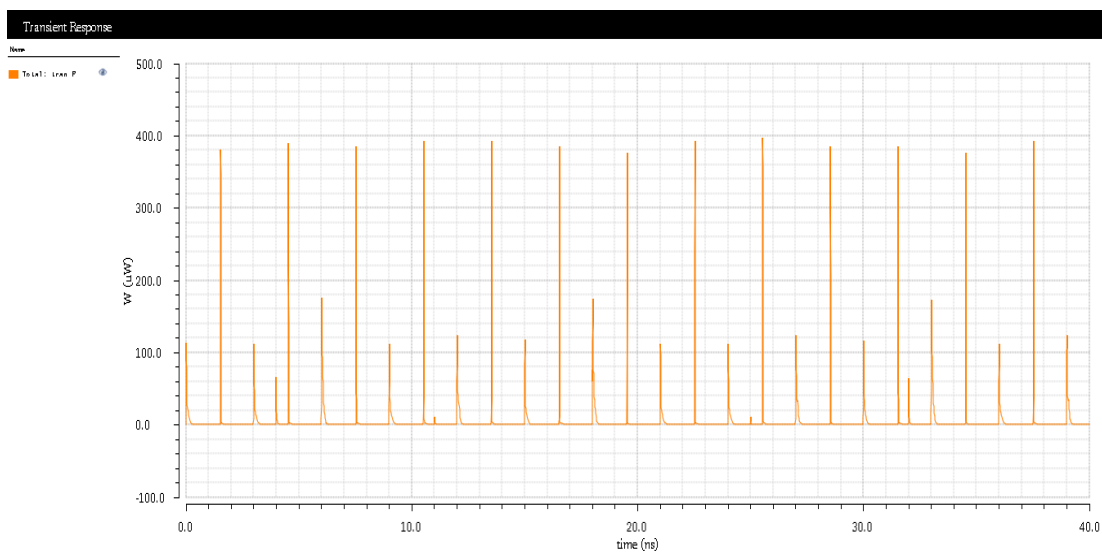


Fig.3.16 Power waveform of SFTFF with 4 TPG

3.5 Comparison

In this section the transistor count, average power consumption and delay of various existing PT flip flop is compared with the 4 TPG flip flops and the observations are placed in Table 3.5.

Table 3.5 Comparison Table

Flip flop		No of transistors	Average power consumption(μ W)	Delay (ps)
EP-DCO FF	Existing[14]	28	44.46	162.54
	4TPG	20	24.43	160.53
CDFF	Existing[15]	30	24.72	180.66
	4TPG	22	13.34	178.47
SCDFF	Existing[16]	31	21.26	188.73
	4TPG	23	12.74	186.69
SFTFF	Existing[17]	24	13.38	149.34
	4TPG	16	6.47	147.41

CHAPTER 4

Proposed Designs

This chapter presents new D flip flop designs wherein the latch circuitry is modified to reduce the power dissipation and use four transistor pulse generator.

4.1 Proposed topology I

The SFTFF flip flop of Fig.3.4 consumes a lot of power because of the P1 transistor connected to ground always. In proposed topology I, the P1 transistor is driven by data instead of ground, is depicted in Fig. 4.1.

When clock=1, for a short period of time transistors MN3 and MNx will turn on whose period will be equal to pulse duration from the pulse generator circuitry. Now, if data comes with '0' then transistor MP1 will turn on and transistor MN1 will turn off because of NMOS transistor (Data is connected to MP1 transistor and MN1 transistor) as MNx connected with clock pulse, data '0' will pass through the transistor MNx because it will work as a pass transistor.

When data comes as '1', it will turn off the MP1 transistor and turn on the transistor MN1, as node X stores the value '1' before the rising edge of the clock, it will be discharge through the MN1, MN2 and MN3 transistor (as Q_fdbk will be at '1' because Q is at '0'). Now node X will become '0'. It will turn on transistor MP2 and because of pull up transistor, Q will become '1'. As both MN3 and MNx transistor are turn on due to clock pulse, data '1' will also pass through this pass transistor MNx. Output Q will attain '1' from this path also.

When data comes as '0', it will turn on the MP1 transistor and will turn off transistor MN1, as node X stores the value '0' before the rising edge of the clock, but it will attain a value '1' because of pull up path formed by transistor MP1 and it will not discharge as transistor MN1 is off. It will turn off transistor MP2 and because of pull up transistor. As both MN3 and MNx transistor are turn on due to clock pulse, data '0' will pass through this pass transistor MNx. Output Q will attain '0' from this path. Keepers I1 and I2 are used to maintain output value.

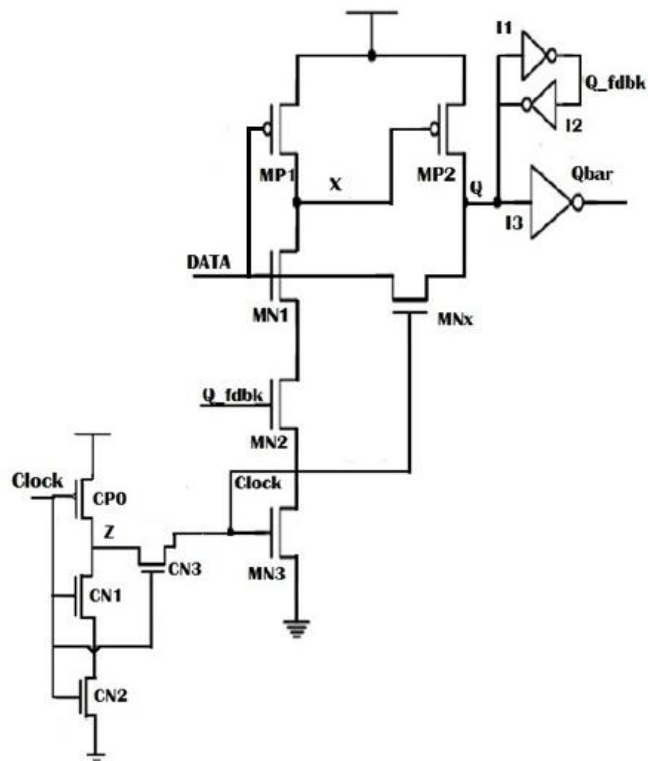


Fig.4.1 Proposed topology I

In the hold mode of the circuit, when we do careful analysis, we get that due to charging and discharging of the internal node X, there is a consumption of significant amount of energy. When the input is at '1', node x is at '1' before the rising edge of the clock and when input remains same at '1' after the rising edge of the clock, this node will discharge through transistors MN2 and MN3. But there is also a transistor MN1 (Q_fdbk) like the previous ones to stop discharging this node and will save power dissipation.

The proposed topology I of Fig.4.1 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverter gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 4.1. The schematic of proposed topology I is shown in Fig. 4.2

Table 4.1 Aspect Ratios of Transistors for Proposed topology I

Component	Aspect ratio
CPO	52
CN1	1.2
CN2	1.2
CN3	7
MP1	1.2
MP2	7.6
MN1	8
MN2	8
MN3	8
MNx	2

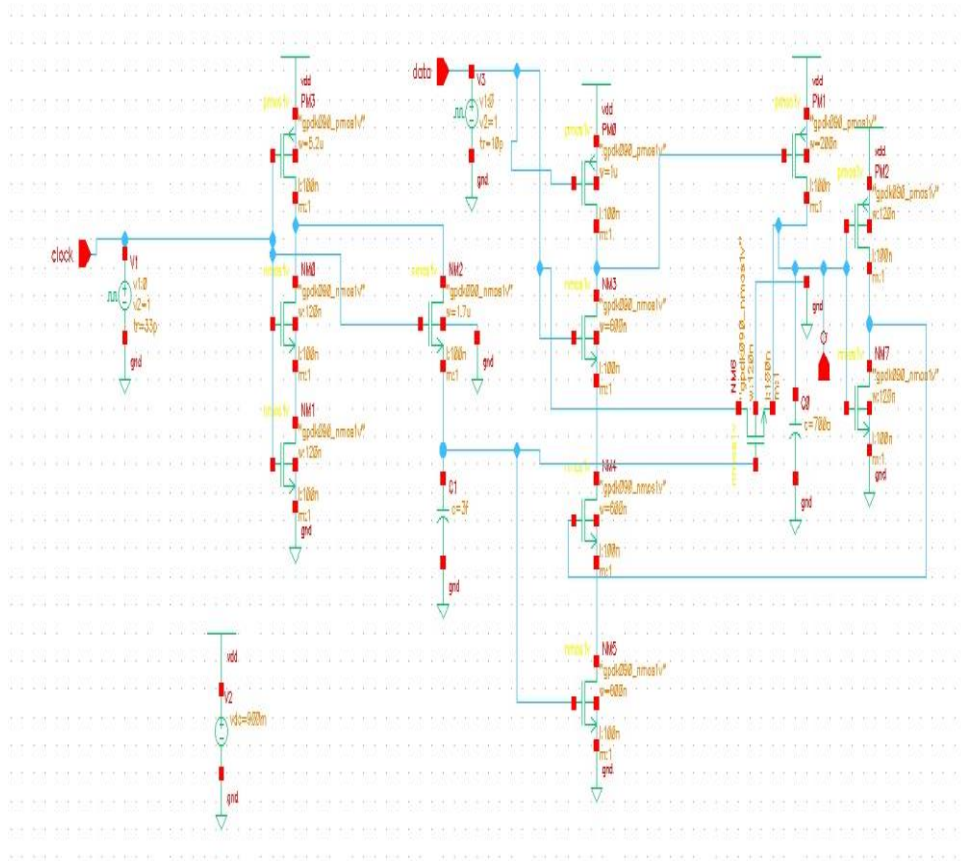


Fig 4.2 Schematic of Proposed topology I

To verify the functionality of Proposed topology I, the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig. 4.11. The power waveforms are depicted in Fig. 4.12. The delay of 123.41ps was observed and the average power consumption is found to be 2.12 μ W.

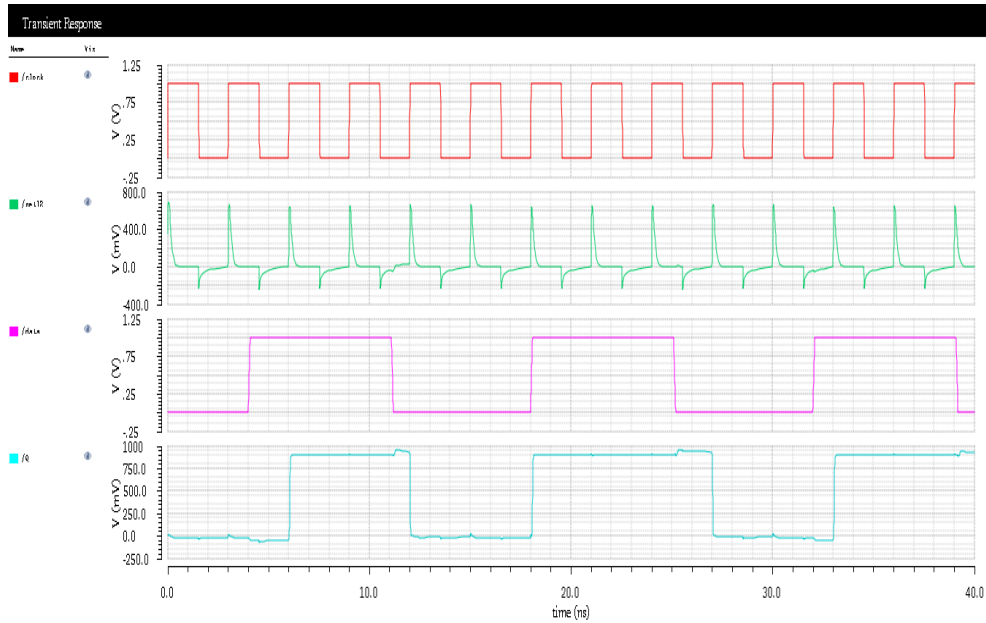


Fig.4.3 Timing waveform of proposed topology I

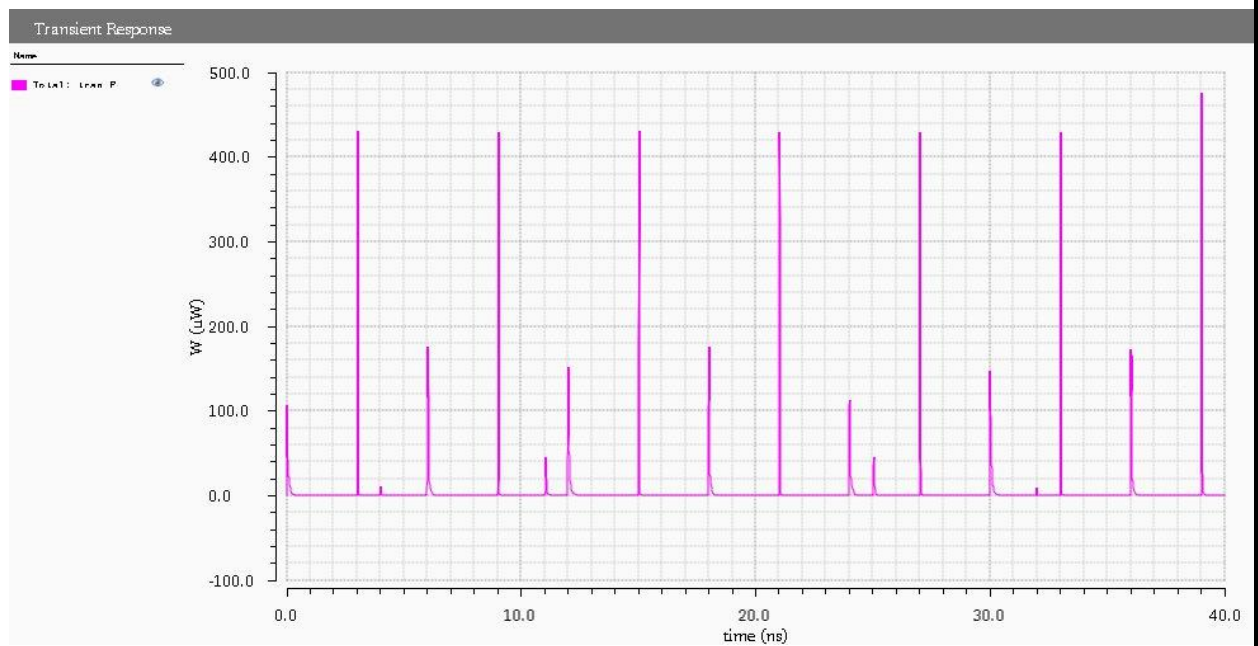


Fig.4.4 Power waveform of Proposed topology I

When data comes as '1', it will turn off the P1 transistor and turn on the transistor N2, as node X stores the value '1' before the rising edge of the clock, it will be discharge through the N1, N2 and N3 transistor (as Q_fdbk will be at '1' because Q is at '0'). Now node X will become '0'. It will turn on transistor P2 and because of pull up transistor, Q will become '1'. As both N3 and N4 transistor are turn on due to clock pulse, data '1' will also pass through this pass transistor N4. Output Q will attain '1' from this path also.

When data comes as '0', it will turn on the P1 transistor and will turn off transistor N2, as node X stores the value '0' before the rising edge of the clock, but it will attain a value '1' because of pull up path formed by transistor P1 and it will not discharge as transistor N2 is off. It will turn off transistor P2 and because of pull up transistor. As both N3 and N4 transistor are turn on due to clock pulse, data '0' will pass through this pass transistor N4. Output Q will attain '0' from this path. Keepers I1 and I2 are used to maintain output value.

In the hold mode of the circuit, when we do careful analysis, we get that due to charging and discharging of the internal node X, there is a consumption of significant amount of energy. When the input is at '1', node x is at '1' before the rising edge of the clock and when input remains same at '1' after the rising edge of the clock, this node will discharge through transistors N2 and N3. But there is also a transistor N1 (Q_fdbk) like the previous ones to stop discharging this node and will save power dissipation.

The proposed topology II of Fig.4.5 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverter gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 4.2. The schematic of proposed topology II is shown in Fig.4.6.

Table 4.2 Aspect Ratios of Transistors for proposed topology II

Component	Aspect ratio
CPO	52
CN1	1.2
CN2	1.2
CN3	7
MP1	1.2
MP2	7.6
MN1	8
MN2	8
MN3	8
MN4	2

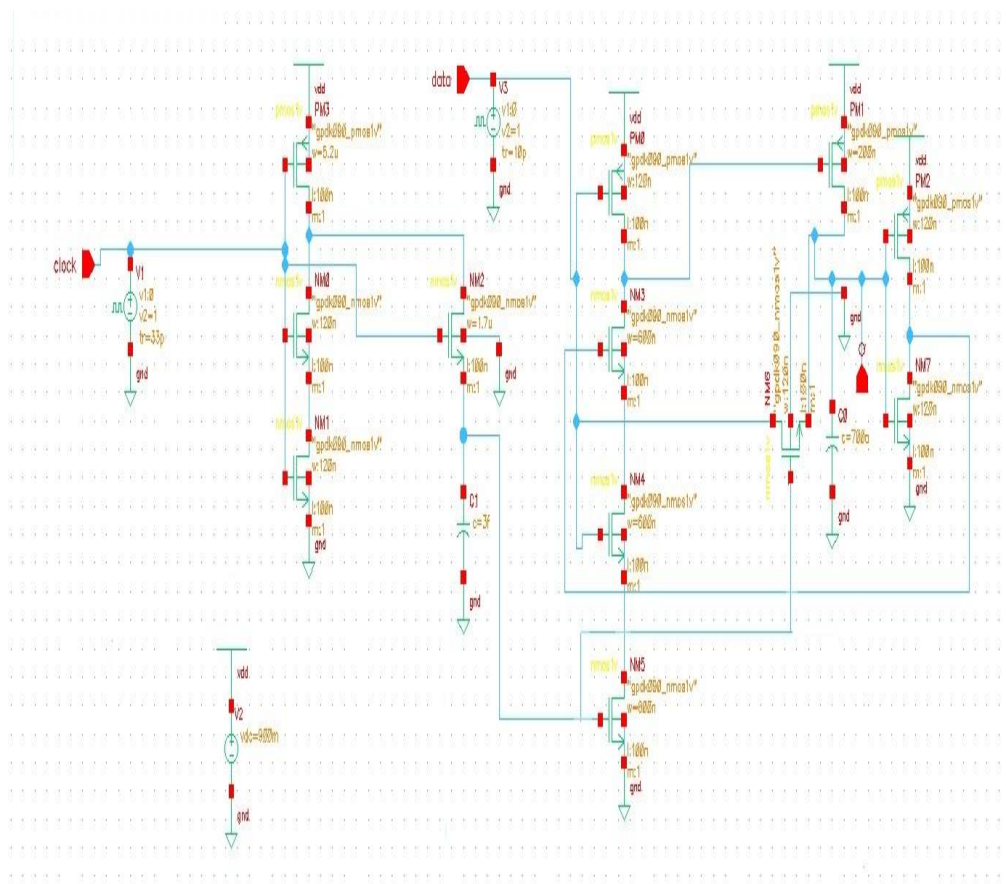


Fig 4.6 Schematic of Proposed topology II

To verify the functionality of proposed topology II the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig. 4.7. The power waveforms are depicted in Fig. 4.8. The delay of 123.36ps was observed and the average power consumption is found to be 2.06 μ W.

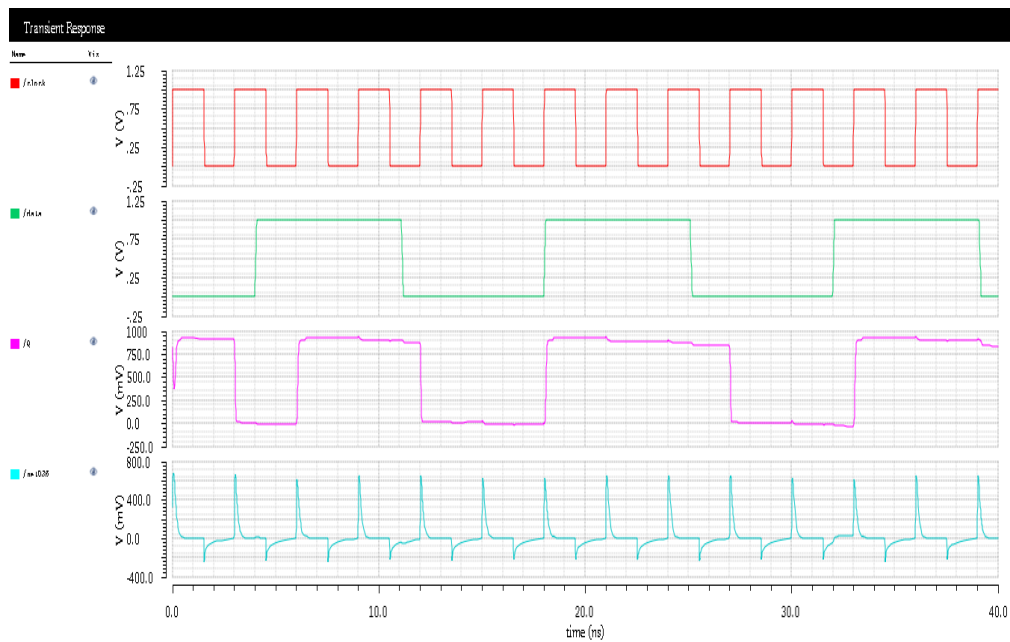


Fig.4.7 Timing waveform of proposed topology II

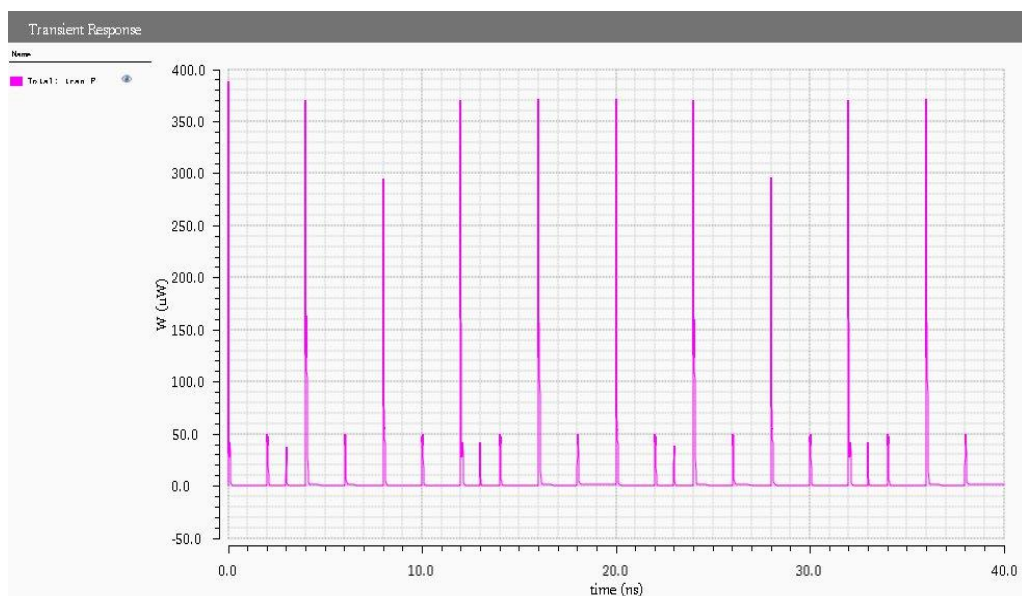


Fig.4.8 Power waveform of proposed topology II

4.3 Proposed topology III

The novel design of low power PT flip flop of Fig.2.6 contains a transmission gate T1 and a pass transistor MNQ connected to data input. Here we design a new topology which can perform the desired output without the use of that transmission gate T1 and pass transistor MNQ. This topology is also based on the same functionality of direct feed through of data signal. Here data input will control the P1 transistor and the transistor N1 unlike previous circuitry [15-16, 18]. Pulse generator is derived from the novel design low power pulse triggered flip flop.

The proposed topology III is depicted in Fig.4.9. In this proposed design, circuit performs the desired result without the use of the transmission gate T1 and of the pass transistor MNQ for the D flip flop circuit [18]. Thus, the complexity of the circuit and also decreases the numbers of transistor count.

When clock=1, for a short period of time transistors N1 and N4 will turn on whose period will be equal to pulse duration from the pulse generator circuitry. Now, if data comes with '0' then transistor P1 will turn on and transistor N1 will turn off because of NMOS transistor (Data is connected to P1 transistor and N2 transistor) as N4 connected with clock pulse, data '0' will pass through the transistor N4 because it will work as a pass transistor.

When data comes as '1', it will turn off the P1 transistor and turn on the transistor N2, as node X stores the value '1' before the rising edge of the clock, it will be discharged through the N1, N2 and N3 transistor (as Q_{fdbk} will be at '1' because Q is at '0'). Now node X will become '0'. It will turn on transistor P2 and because of pull up transistor, Q will become '1'. As both N1 and N4 transistor are turned on due to clock pulse, data '1' will also pass through this pass transistor N4. Output Q will attain '1' from this path also. There will be less delay compared to previous flip flop, in transition of data from '0' to '1' because there is no transmission gate.

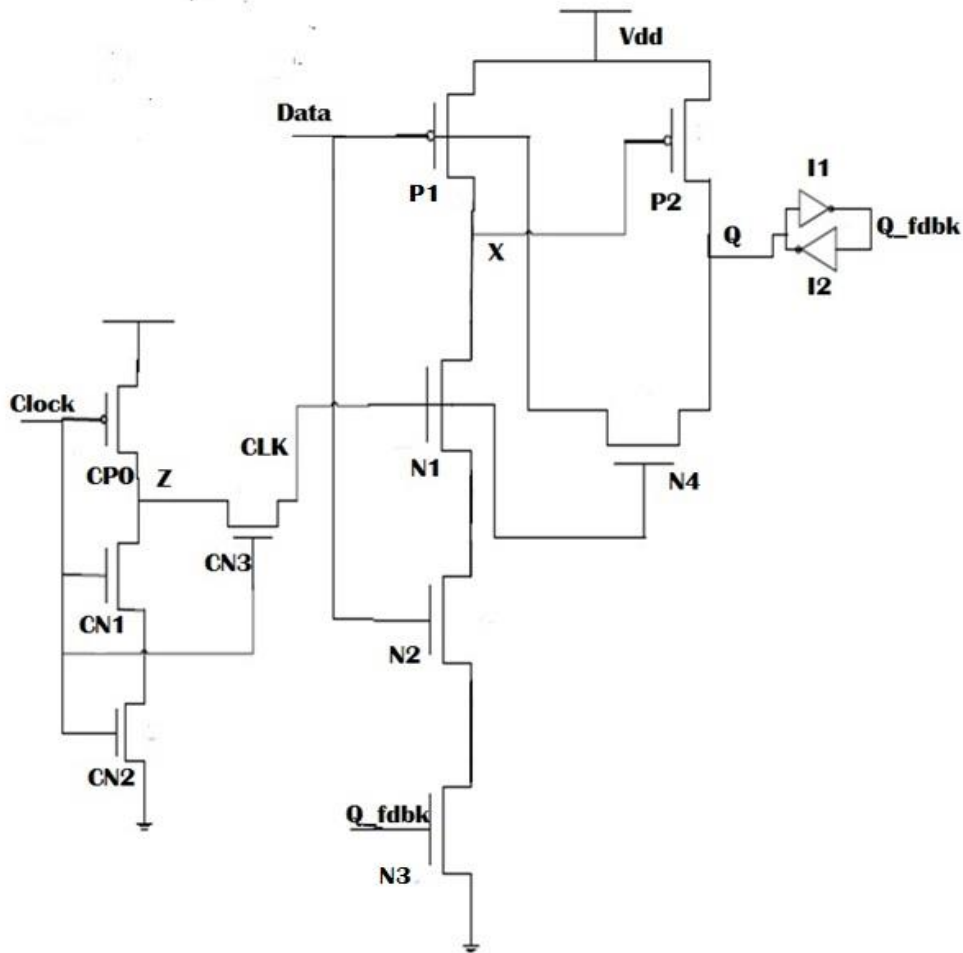


Fig. 4.9 Proposed topology III

When data comes as '0', it will turn on the P1 transistor and also N2 is connected to ground through it and will turn off transistor N2, as node X stores the value '0' before the rising edge of the clock, but it will attain a value '1' because of pull up path formed by transistor P1 and it will not discharge as transistor N2 is off. It will turn off transistor P2 and because of pull up transistor. As both N1 and N4 transistor are turn on due to clock pulse, data '0' will pass through this pass transistor N4. Output Q will attain '0' from this path. Keepers I1 and I2 are used to maintain output value.

In the hold mode of the circuit, when we do careful analysis, we get that due to charging and discharging of the internal node X, there is a consumption of significant amount of energy. When the input is at '1', node x is at '1' before the rising edge of the

clock and when input remains same at '1' after the rising edge of the clock, this node will discharge through transistors N1 and N2. But there is also a transistor N3 (Q_fdbk) like the previous ones to stop discharging this node and will save power dissipation.

The proposed topology III of Fig. 4.9 is simulated on Cadence Virtuoso using CMOS 90nm technology parameters. The inverter gates are realized using static CMOS. The aspect ratios of various transistors are placed in Table 4.3. The schematic of proposed topology III is shown in Fig. 4.10

Table 4.3 Aspect Ratios of Transistors for proposed topology III

Component	Aspect ratio
CPO	52
CN1	1.2
CN2	1.2
CN3	7
MP1	1.2
MP2	7.6
MN1	8
MN2	8
MN3	8
MN4	2

To verify the functionality of proposed topology III the clock frequency of 500 MHz is applied. The applied clock, generated pulse, input and output waveforms are shown in Fig. 4.11. The power waveforms are depicted in Fig. 4.12. The delay of 123.33ps was observed and the average power consumption is found to be 2.04 μ W.

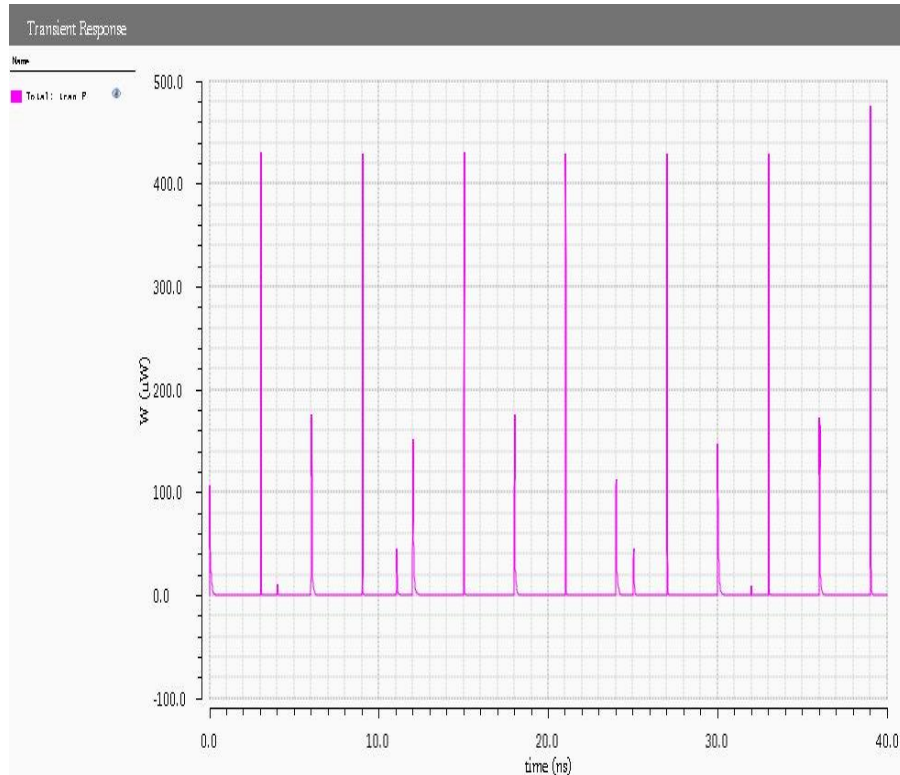


Fig.4.12 Power waveform of Proposed topology III

4.4 Comparison

In this section the transistor count, average power consumption and delay of various proposed topologies are compared and the observations are placed in Table 4.4. It may be noted that the power consumption and delay for proposed topology III is minimum.

Table 4.4 Comparison Table

Flip flop	No of transistors	Average power consumption(uW)	Delay (ps)
Proposed topology I	14	2.12	123.41
Proposed topology II	14	2.06	123.36
Proposed topology III	14	2.04	123.33

It may be noted that:-

- 1) The proposed topology I is better than PT flip flop of Fig. 3.14 in terms of average power consumption by 67.23% and delay by 16.28%.
- 2) The proposed topology II is better than novel design flip flop of Fig. 2.6 in terms of transistor count by 17.64%, average power consumption by 52.31% and delay by 4.25%.
- 3) The proposed topology III is better than novel design flip flop of Fig. 2.6 in terms of transistor count by 17.64%, average power consumption by 52.77% and delay by 4.27%.

CHAPTER 5

Shift Registers Based On Proposed Flip Flops

In this chapter, the flip flops proposed in Chapter 4 are cascaded to achieve the functionality of shift register. The shift register, in particular is used due to its wide applications in various applications such as counters, serial to parallel conversion and vice versa, multiplication etc. The functionality is verified via simulations in Cadence Virtuoso.

5.1 Shift Registers

Shift register is formed by series connection of D flip flops which are driven by common clock. A serial input is applied to the first flip flop of shift registers which is shifted by one position with each transition of the clock input. The schematic of 4-bit shift register is depicted in Fig. 5.1.

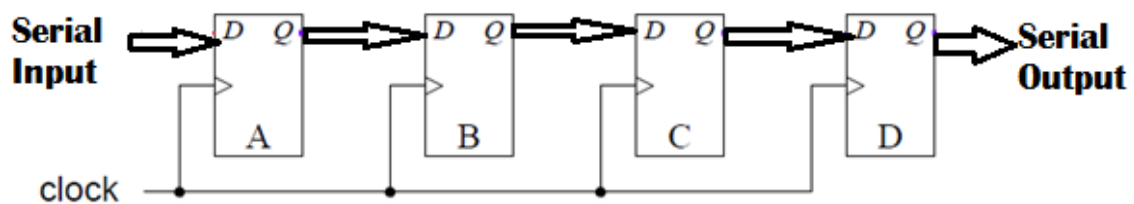


Fig.5.1 Shift Register

5.2 Shift Register using proposed topology I

The proposed topology I of Fig. 4.1 is used to build a three bit shift register. The circuit schematic is depicted in Fig. 5.2. It may be noted that a single pulse generator is used for all the three flip flops. The serial input is applied to 1st flip flop and output of it is processed by 2nd flip flop and so on.

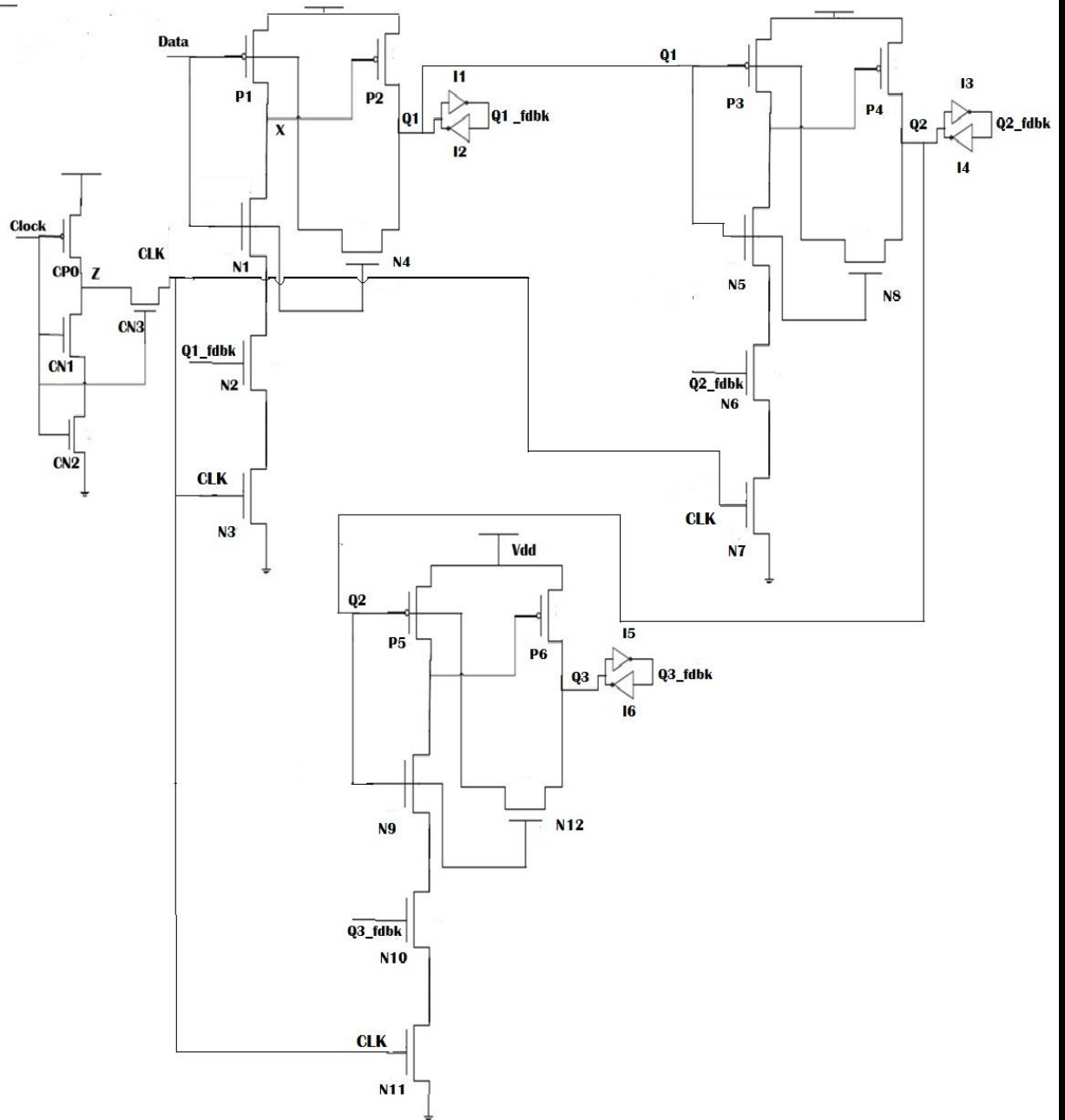


Fig. 5.2 Shift register using proposed topology I

The 3 bit shift register of Fig. 5.2 is simulated in Cadence Virtuoso using CMOS 90nm technology parameters. The aspect ratios of various transistor are same as those given in Table 4.1 The schematic drawn in Cadence Virtuoso is given in Fig. 5.3.

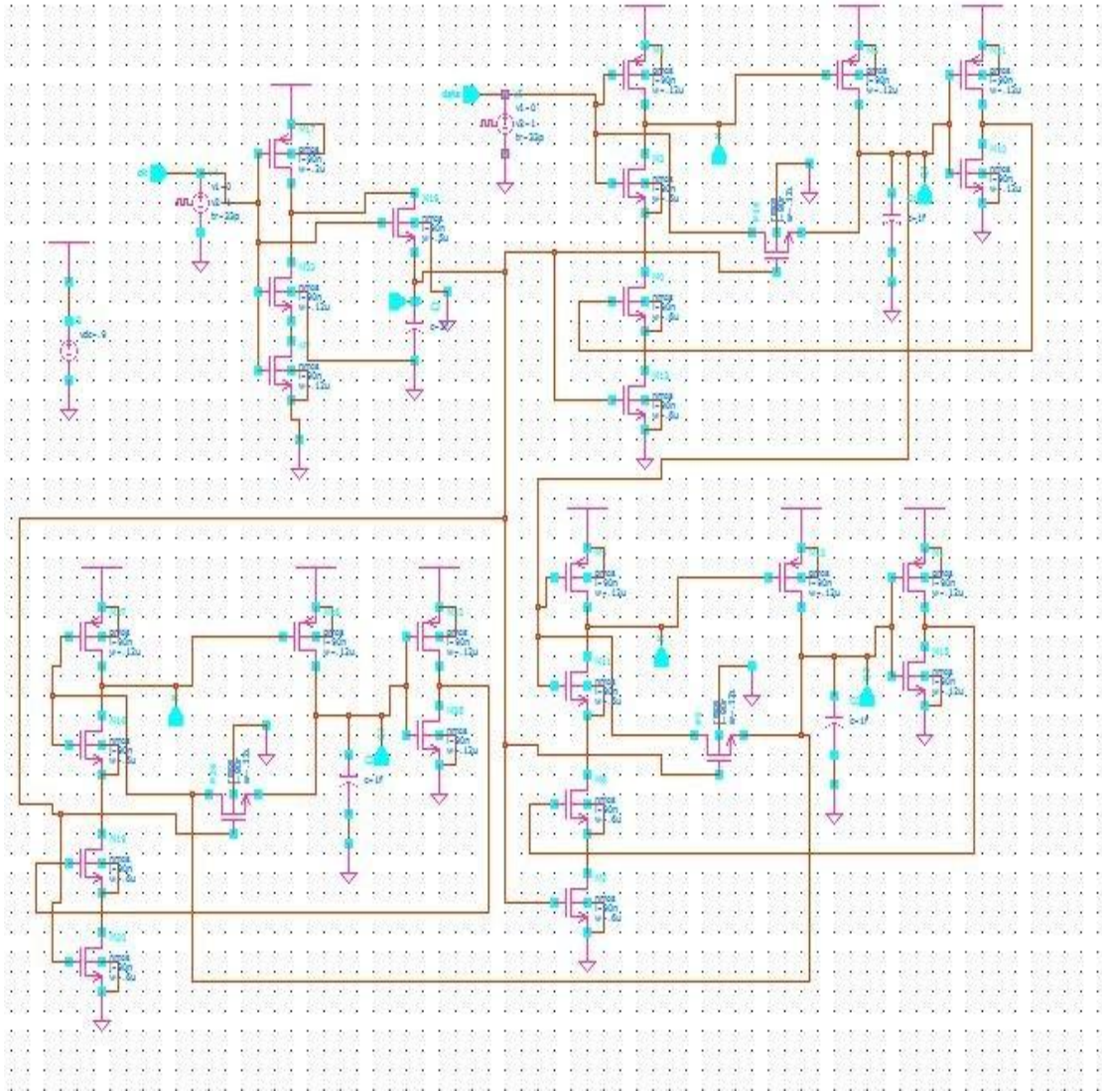


Fig 5.3 Schematic of 3 bit shift register using proposed topology I

To verify the functionality of 3 bit shift register of Fig 5.3, the clock frequency of 500 MHz is used. The applied clock, generated pulse, input and output waveforms are shown in Fig. 5.4. It may be noted that with each clock transition data is shifted by one bit position. The power waveforms are depicted in Fig. 5.5. The delay from serial input to serial output is 323.71ps and the average power consumption is found to be 5.32 μ W.

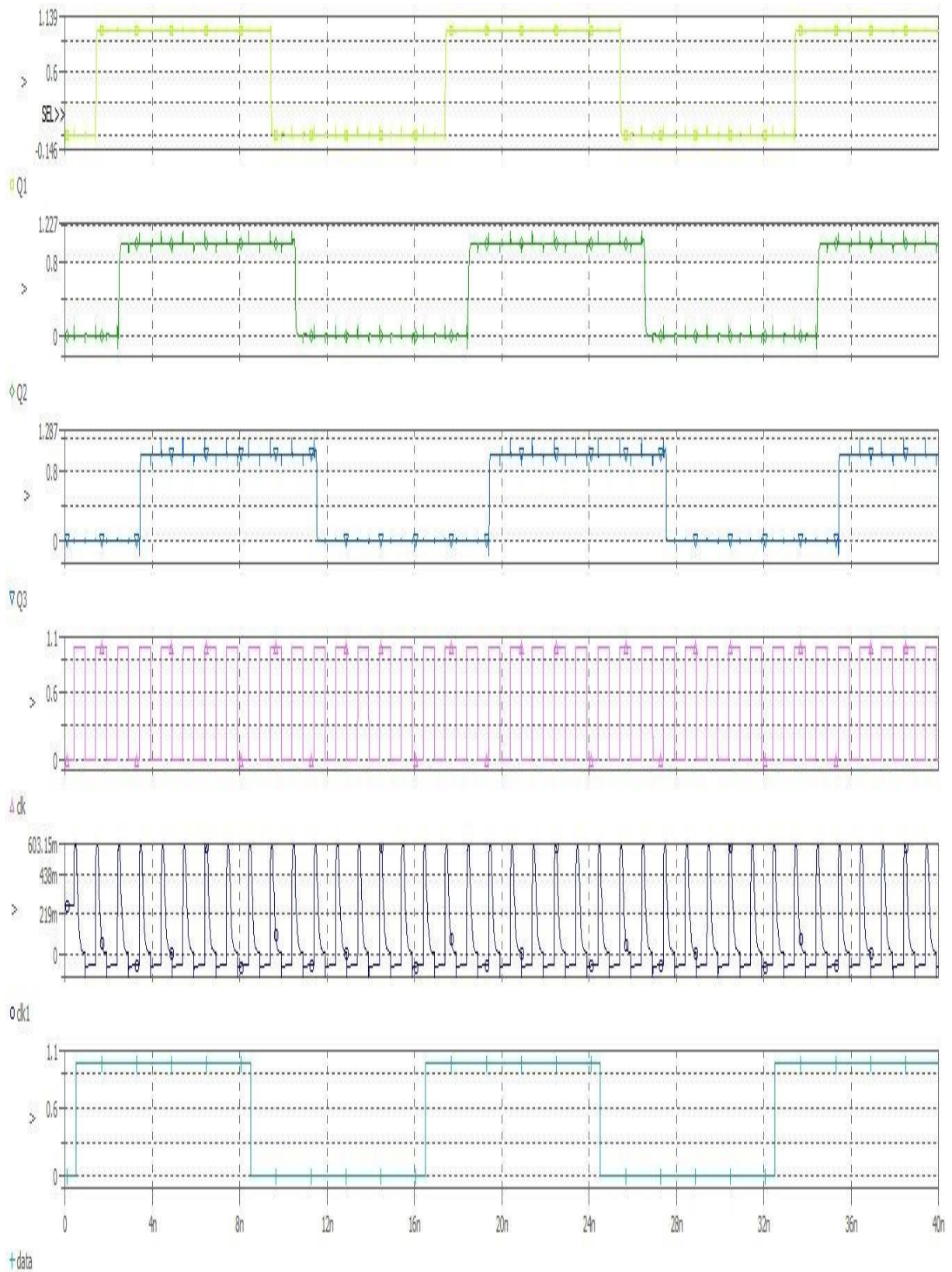


Fig.5.4 Timing waveform of 3 bit shift register using proposed topology I

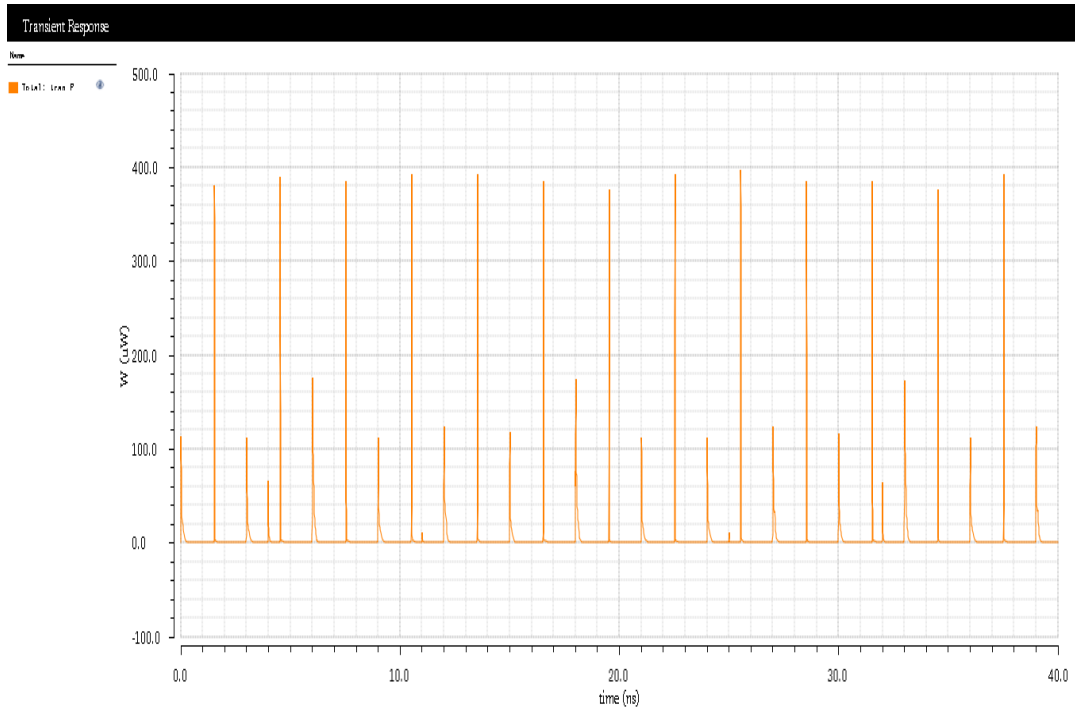


Fig.5.5 Power waveform of 3 bit shift register using proposed topology I

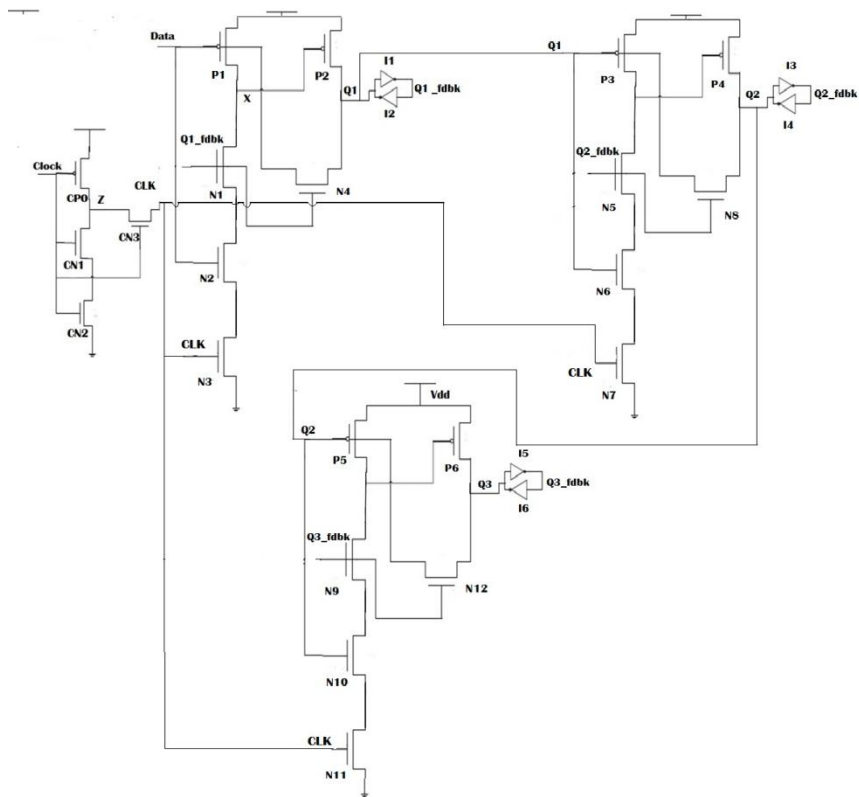


Fig 5.6 Shift register using proposed topology II

5.3 Shift Register using proposed topology II

The proposed topology II of Fig. 4.5 is used to build a three bit shift register. The circuit schematic is depicted in Fig. 5.6. It may be noted that a single pulse generator is used for all the three flip flops. The serial input is applied to 1st flip flop and output of it is processed by 2nd flip flop and so on.

The 3 bit shift register of Fig. 5.6 is simulated in Cadence Virtuoso using CMOS 90 nm technology parameters. The aspect ratios of various transistors are same as those given in Table 4.2. The schematic drawn in Cadence Virtuoso is given in Fig. 5.7.

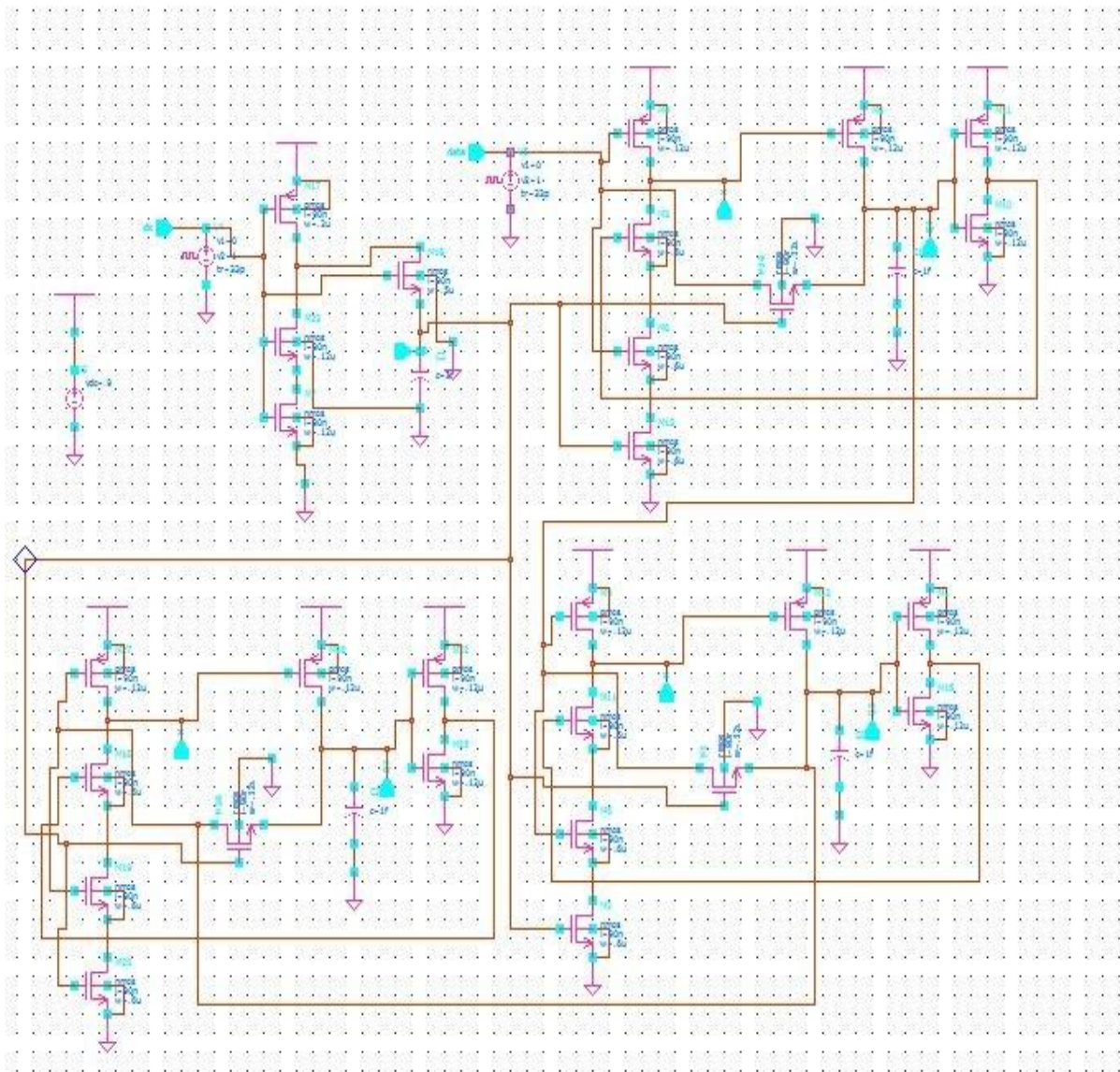


Fig 5.7 Schematic of 3 bit shift register using proposed topology II

To verify the functionality of 3 bit shift register of Fig 5.7, the clock frequency of 500 MHz is used. The applied clock, generated pulse, input and output waveforms are shown in Fig. 5.8. It may be noted that with each clock transition data is shifted by one bit position. The power waveforms are depicted in Fig. 5.9. The delay of delay from serial input to serial output is 323.12ps and the average power consumption is found to be 5.26 μ W.

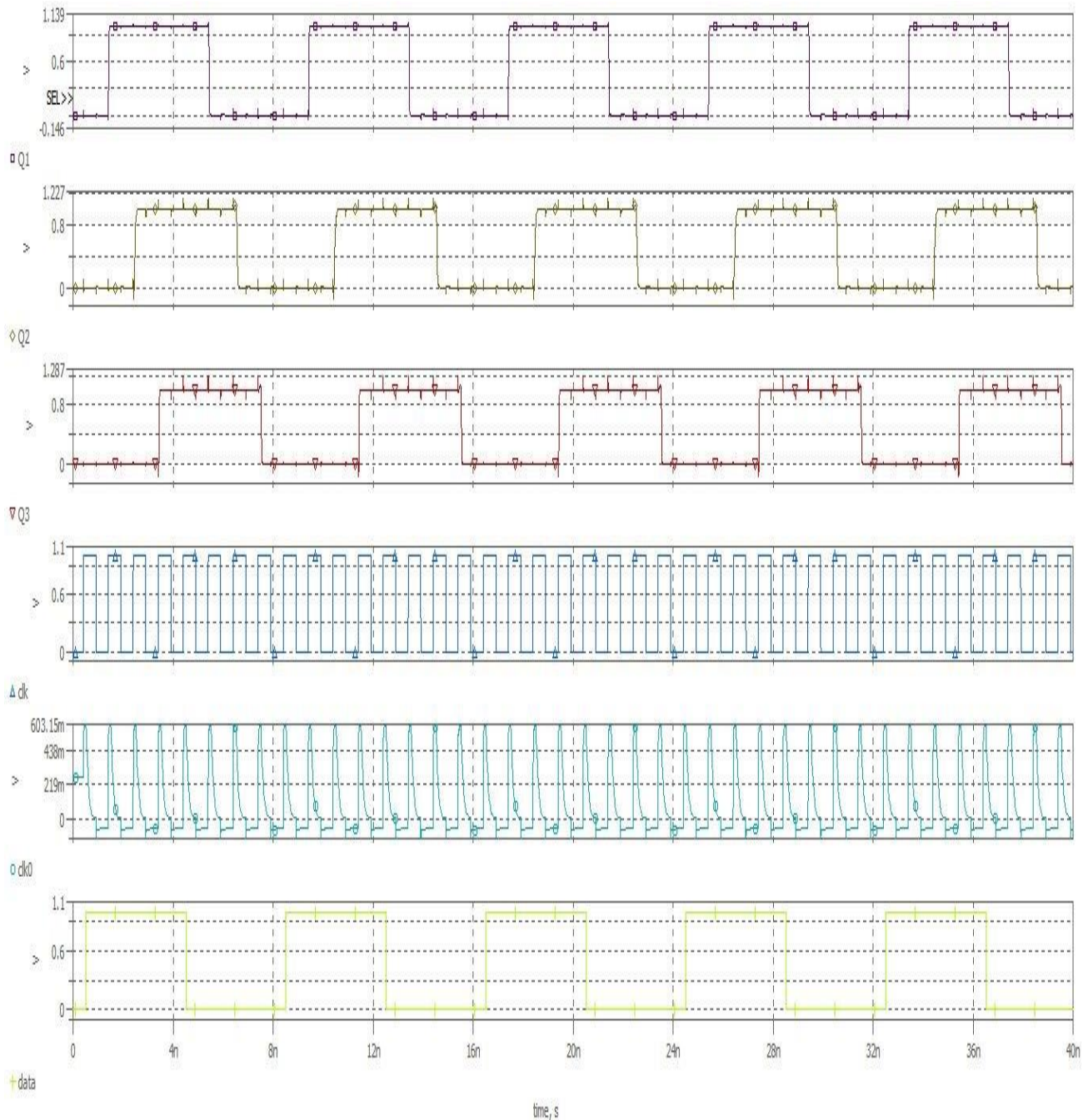


Fig.5.8 Timing waveform of 3 bit shift register using proposed topology II

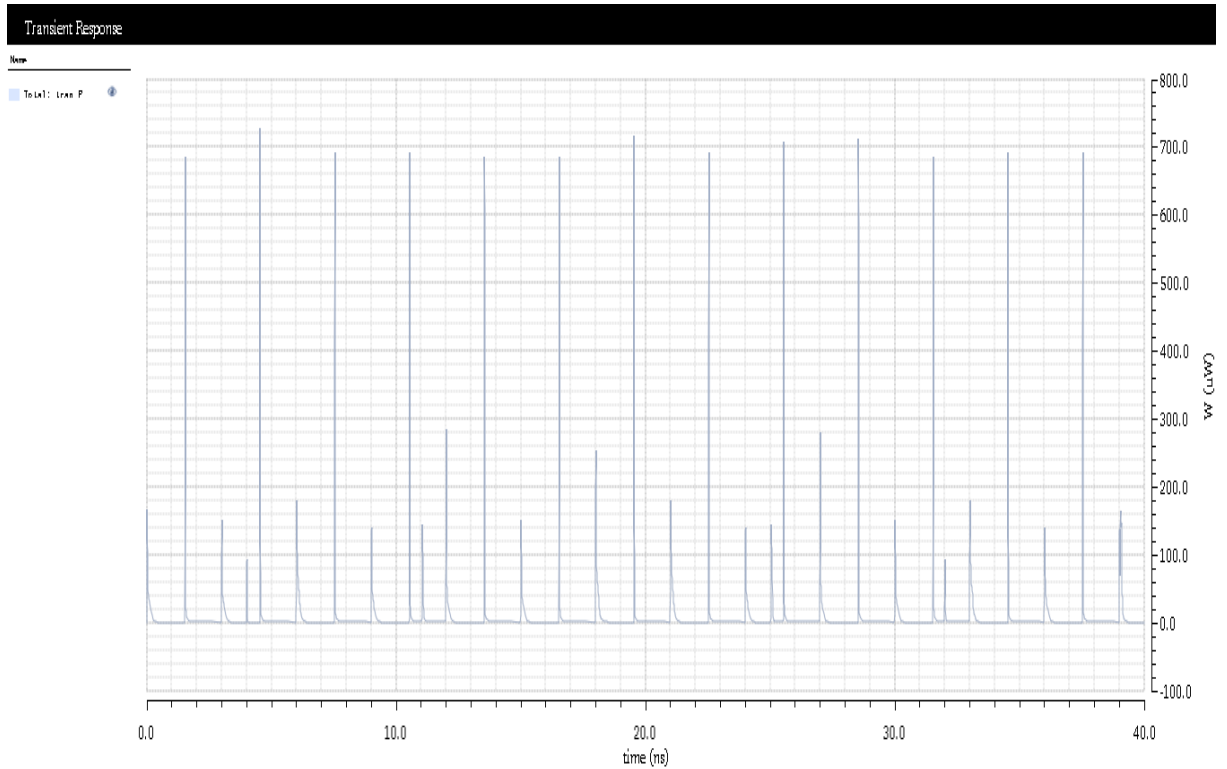


Fig.5.9 Power waveform of 3 bit shift register using proposed topology II

5.4 Shift Register using proposed topology III

The proposed topology III of Fig. 4.8 is used to build a three bit shift register. The circuit schematic is depicted in Fig. 5.10. It may be noted that a single pulse generator is used for all the three flip flops. The serial input is applied to 1st flip flop and output of it is processed by 2nd flip flop and so on.

The 3 bit shift register of Fig. 5.6 is simulated in Cadence Virtuoso using CMOS 90 nm technology parameters. The aspect ratios of various transistors are same as those given in Table 4.3. The schematic drawn in Cadence Virtuoso is given in Fig. 5.11.

To verify the functionality of 3 bit shift register of Fig 5.11, the clock frequency of 500 MHz is used. The applied clock, generated pulse, input and output waveforms are shown in Fig. 5.12. It may be noted that with each clock transition data is shifted by one bit position. The power waveforms are depicted in Fig. 5.13. The delay of delay from serial input to serial output is 321.26ps and the average power consumption is found to be 5.17 μ W.

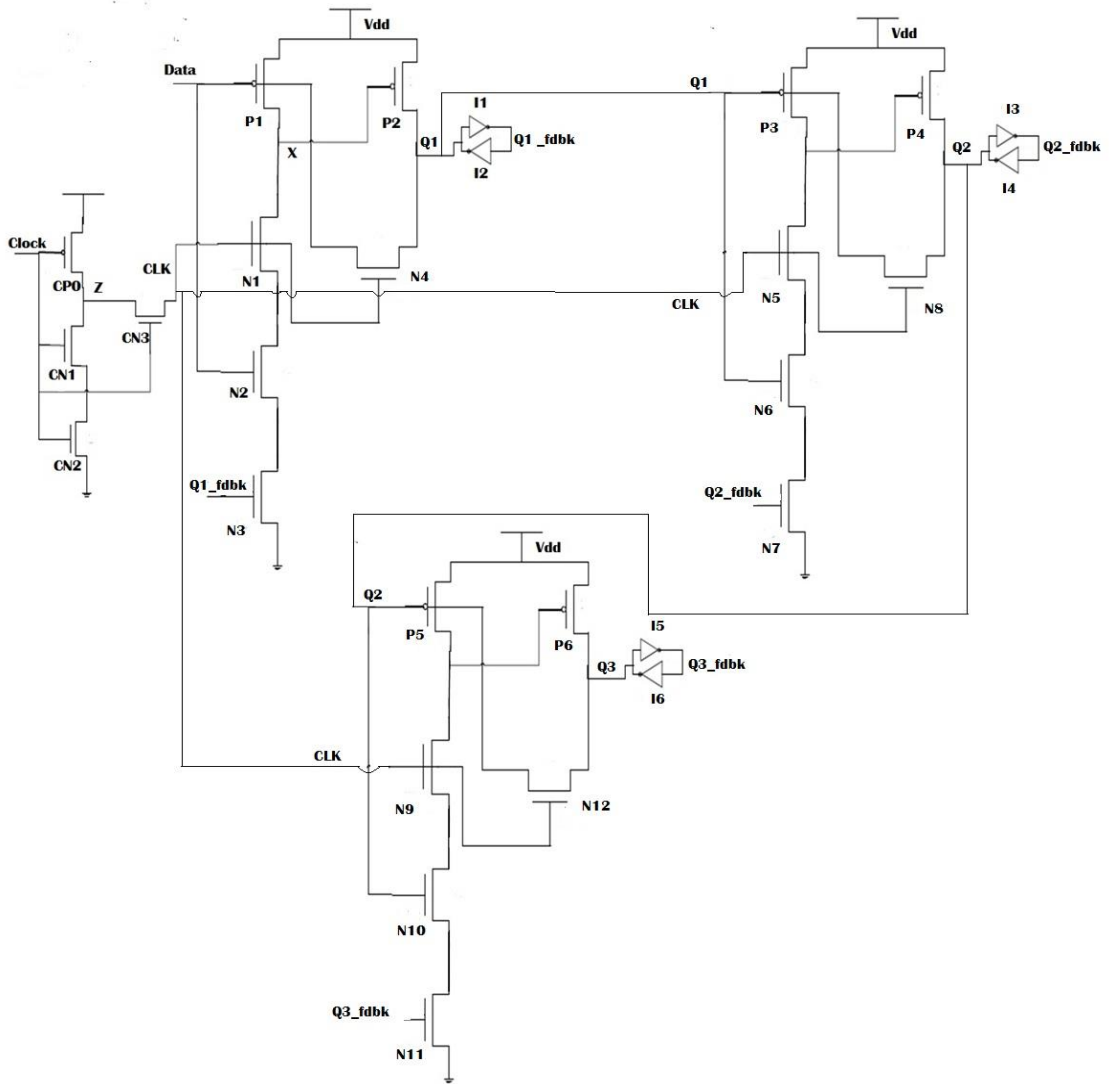


Fig. 5.10 Shift register using proposed topology III

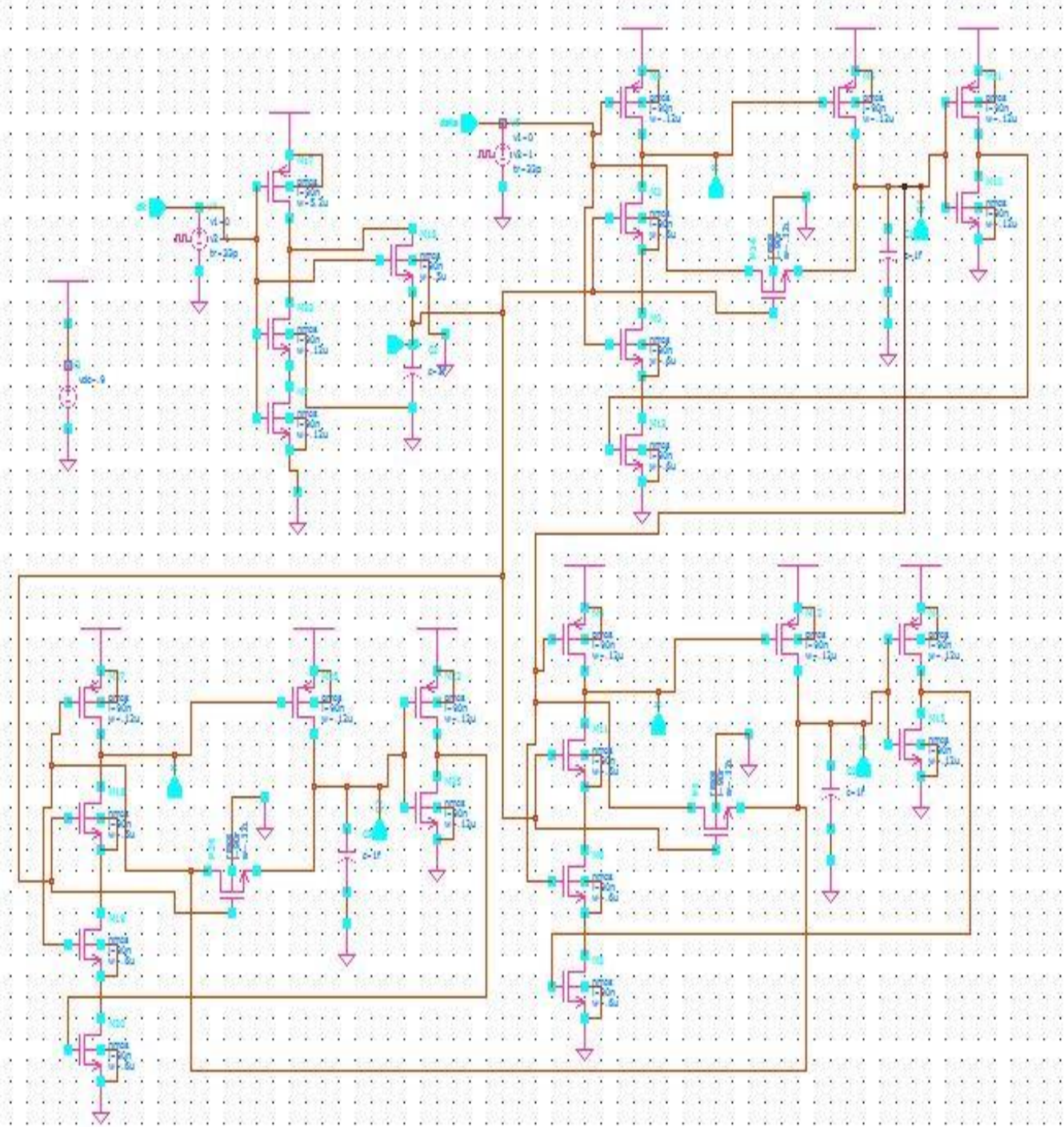


Fig 5.11 Schematic of 3 bit shift register using proposed topology III

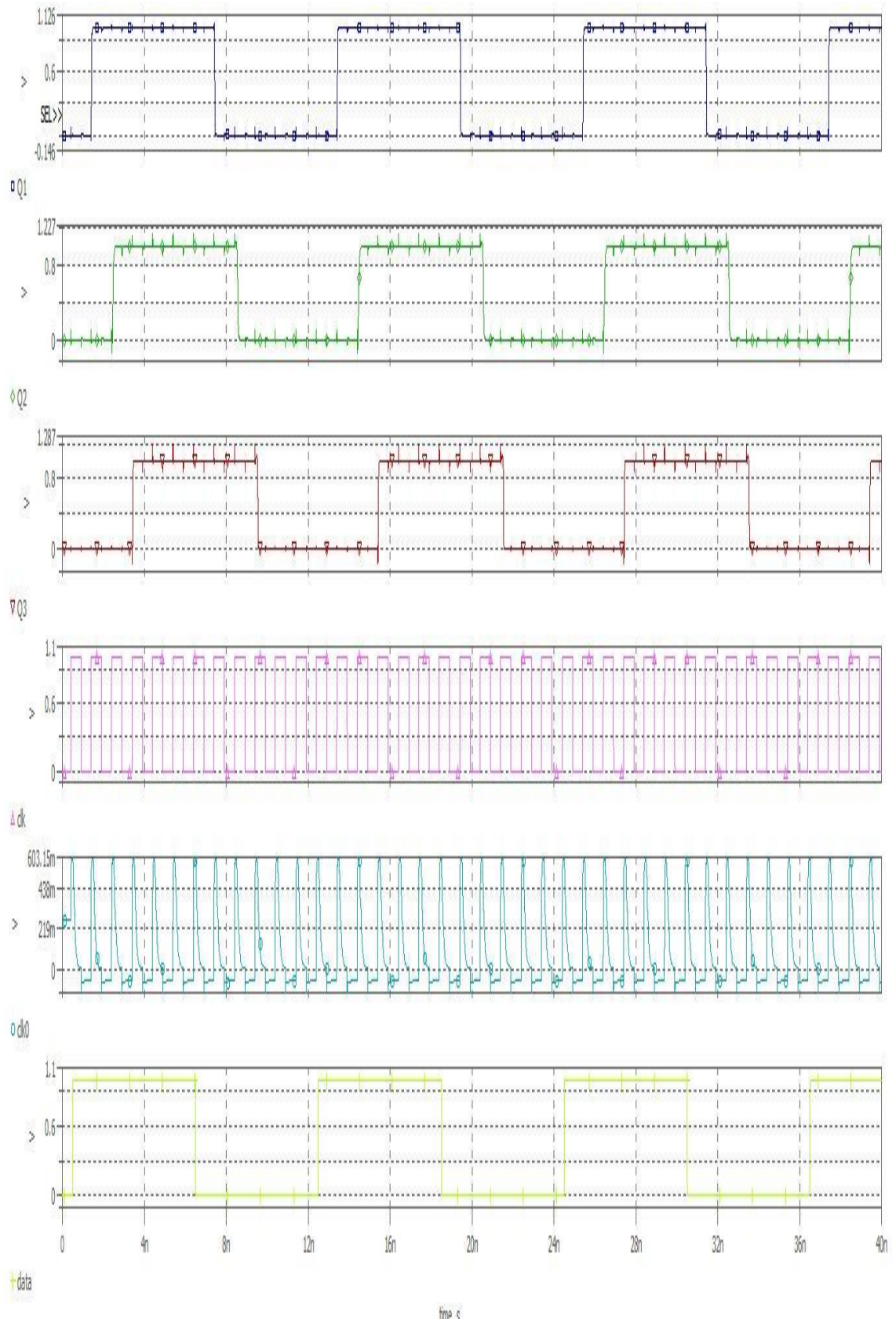


Fig.5.12 Timing waveform of 3 bit shift register using proposed topology III

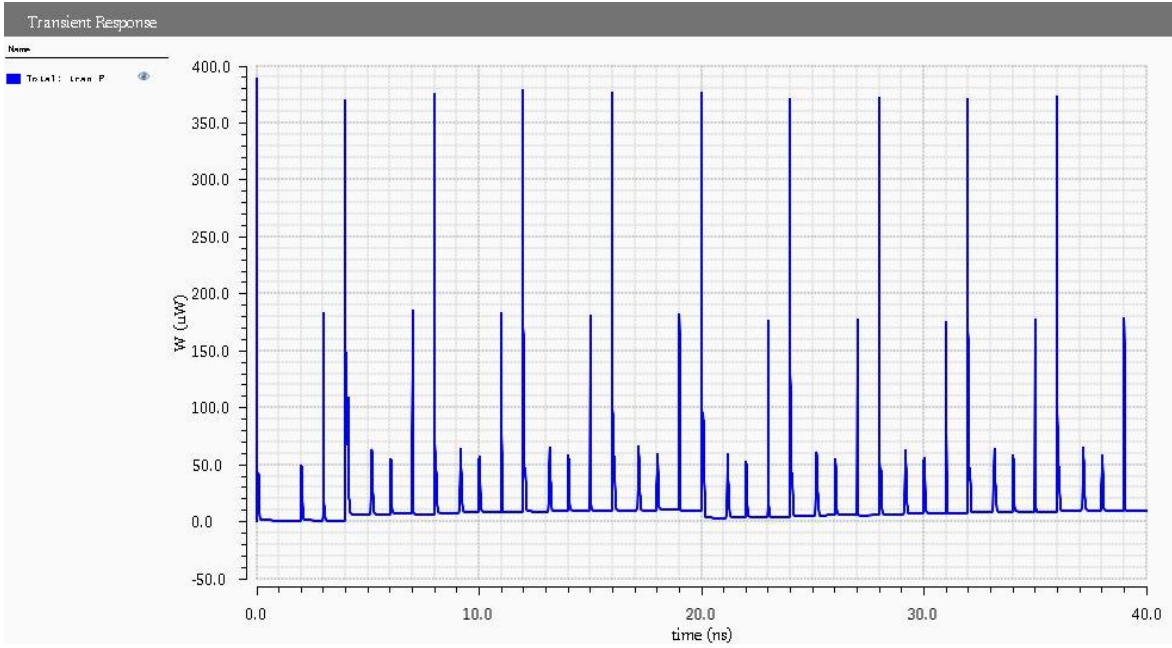


Fig.5.13 Power waveform of 3 bit shift register using proposed topology III

5.5 Comparison

In this section the transistor count and average power consumption of various 3 bit shift registers of various PT flip flop is compared and the observations are placed in Table 5.1. It may be noted that the power consumption for shift register with proposed topology III is minimum.

Table 5.1 Comparison Table

3 bit Shift register Based on proposed topology	Transistor count	Average power consumption(μ W)
I	34	5.32
II	34	5.26
III	34	5.17

Conclusion

As flip flop is the fundamental storage element of the digital circuits, these are used extensively. Flip flops also plays a significant role in the synchronous type of systems. In this project, we designed a new pulse triggered D flip flop with reduced power consumption from the previous flip flops and also with lesser delay of data to output Q.

The new topologies use 4TPG and/or modified latch circuit. These circuits are simulated using CMOS90 nm process technology and 1Vsupply voltage in Cadence Virtuoso. A 3fF capacitor at the output of the pulse generator and .1fF capacitor at the output of the latch circuit are used throughout simulations. Table 6.1 gives a summary of the proposed circuits. It may be noted that the proposed topologies used 14 transistors, which is least among the examined topologies. The overall power consumption is minimum for proposed topology III.

Table 6.1 Summary of the flip flops

Flip flop		No of transistors	Average power consumption(μ W)	Delay (ps)
EP-DCO FF	Existing[14]	28	44.46	162.54
	4TPG	20	24.43	160.53
CDFF	Existing[15]	30	24.72	180.66
	4TPG	22	13.34	178.47
SCDFF	Existing[16]	31	21.26	188.73
	4TPG	23	12.74	186.69
SFTFF	Existing[17]	24	13.38	149.34
	4TPG	16	6.47	147.41
Proposed topology I		14	2.12	123.41
Proposed topology II		14	2.06	123.36
Proposed topology III		14	2.04	123.33