OTRA based Signal Generators and their Performance Analysis

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by

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CERTIFICATE

This is to certify that the thesis entitled "**OTRA based Signal Generators and their Performance Analysis**" submitted by **Komanapalli Gurumurthy** (2K14/PHD/EC/06) to the Department of Electronics and Communication Engineering, Delhi Technological University for the award of the degree of Doctor of Philosophy is based on the original research work carried out by him under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. It is further certified that the work presented in this thesis is not submitted to any other university or institution for the award of any degree or diploma.

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CANDIDATE'S DECLARATION

I hereby certify that the research work, which is being presented in the thesis, titled, "**OTRA based Signal Generators and their Performance Analysis"** in fulfillment of requirements of the award of the degree of Doctor of Philosophy is an authentic record of my research work carried under the supervision of Prof. Rajeshwari Pandey and Prof. Neeta Pandey. The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for the award of any degree.

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ABSTRACT

The reduction of the minimum feature size of MOS transistor for digital very-large-scale integration (VLSI) circuits has been ongoing for the past few decades. As the channel length is scaled down into deep sub-micrometer dimensions, the lower power supply voltage is required to ensure the device reliability. To be compatible with digital VLSI technologies, analog integrated circuits, which can operate at low supply voltages, also, received significant attention. The current mode signal processing emerged as low voltage design technique for analog circuits which was manifested in proposition of numerous current mode analog building blocks for the realization of various signal processing and generation circuits. The Operational transresistance amplifier (OTRA), a current-controlled voltage source, is one among those. Due to its inherent pros like bandwidth independent of closed loop gain, high slew rate and simplicity in assimilating the effect of parasitic capacitances at the input ports OTRA is being used widely for signal processing and generating applications.

Sinusoidal oscillators are extensively used in the field of communication, instrumentation, testing and measurements. Versatility of oscillators in electronic applications coupled with advantages of OTRA and availability of limited literature has led the author of the thesis to explore the area of OTRA based signal generation. In this work several OTRA based sinusoidal oscillators that provide additional features not available in previously known OTRA oscillators have been presented.

It is useful to minimize the number of active blocks and passive elements in the oscillator topologies from power consumption optimization, reduction in parasitic

effects and area efficient design viewpoint. Therefore, sinusoidal oscillator design with single OTRA is given due consideration and three second order oscillators are presented. Additionally, the viability of oscillators providing low frequencies oscillations is also examined. Another significant contribution is development of single OTRA based third order SO having smaller component spread in condition of oscillation compared to available topologies, which is a desirable feature from IC fabrication viewpoint.

Quadrature oscillators find widespread applications in the field of communication. In this work, five new structures (one second order and four third order designs) are presented. Out of these five circuits, three third order topologies are derived from a generic structure. The second order design also qualifies for low frequency operations.

Further, four new oscillators are presented that are capable of generating a wide range of frequencies from very low to high. All the topologies provide electronic tuning, independent control of frequency of oscillations without disturbing the condition of oscillation. One of the configurations provides linear tuning, which is suitable for measurement and instrument applications.

Finally, a new OTRA based Wein bridge oscillator with wider tuning range is proposed in this work. A detailed mathematical formulation of harmonic distortion analysis is also presented to ascertain the linearity of the proposed design.

The non-ideal behavior of all proposed configurations is studied by considering nonidealities of OTRA and various performance analyses such as sensitivity, frequency stability, harmonic and phase noise analysis as applicable are carried out. Functionality of all propositions is verified through simulations using SPICE/Cadence Virtuoso spectre ADE tool using 0.18 μm CMOS process parameters. Further, few circuits are verified experimentally also and post layout simulation results are included for rest.

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ABBREVATIONS

ABB	Analog building block
ADE	Analog design Environment
CCII	Second generation current conveyor
CCCII	Second generation current controlled conveyor
CCVS	Current controlled voltage source
CCCDTA	Current controlled current difference transconductance amplifier
CDTA	Current difference transconductance amplifier
CCCCTA	Current controlled current conveyor transconductance amplifier
CDBA	Current differencing buffered amplifier
CFOA	Current feedback amplifier
CM	Current-mode
CO	Condition of oscillation
DAC	Digital-to-analog convertor
DDCC	Differential difference current conveyor
DRC	Design Rule Check
DVCC	Voltage current conveyor
DVCCTA	Differential voltage current conveyor transconductance amplifier
FFT	Fast Fourier transform
FO	Frequency of oscillation

HD	Harmonic distortion
IF	Inverse filter
IBP	Inverse bandpass filter
ILP	Inverse lowpass
IHP	Inverse Highpass
LFSOs	Low frequency sinusoidal oscillators
LVS	Layout vs. Schematic check
MCCCFTA	Modified current controlled current follower transconductance amplifier
MDCC	Modified differential current conveyor
OTA	Operational transconductance amplifier
OTRA	Operational Transresistance Amplifier
pFTFN	Positive four terminals floating nullor
QO	Quadrature oscillators
SO	Sinusoidal oscillator
THD	Total harmonic distortion
TOSO	Third order sinusoidal oscillators
UVC	Universal voltage conveyor
VLF	Very low frequency
VM	Voltage mode
VDTA	Voltage difference transconductance amplifier

CHAPTER 1
INTRODUCTION

1.1 Background

Tremendous advancement in analog circuit design has occurred over the last few decades, mainly due to rapid growth in very large scale integration (VLSI) technology. One of the main driving forces that ensured this continuous growth and interest in analog circuit design is the grown need for fully integrated systems, which are compatible with CMOS technology encompassing a larger number of digital as well as analog circuits on a single chip. Analog circuits such as continuous time filters, oscillators, current and voltage amplifiers, voltage comparators, rectifiers, digital to analog and analog to digital converters, disk drive electronics, etc. are inevitable analog circuits, which cannot be accomplished by digital techniques. Moreover, new applications continue to appear where high performance and low power requirements are being treated with equal importance.

Voltage mode (VM) operational amplifier has been in the mainstay for decades and considered to be the most prominent and dominant analog building block (ABB) in the area of analog signal processing. The limitations imposed by opamp based topologies in their high-frequency operations due to lower slew rate and constant gain-bandwidth product made analog designers and researchers to search for the alternative approach.

More recently, current-mode (CM) signal processing is widely considered to be the viable design technique to overcome the limitations imposed by VM counterparts [1]-[6]. In contrast to the conventional VM, current-mode signal representing the information being processed is in the form of electric current. These circuits are low impedance node networks, hence result in a low time constant, thereby improving system performance in terms of speed and slew rate.

Thus, the CM technique has resulted in the emergence of numerous CM ABBs. The literature has thus addressed voluminous blocks, which may run into an equally voluminous bibliography, which is beyond the scope of the present work and hence limited to some important selected works.

The CM building blocks, such as first-generation current conveyor (CCI) [7], second-generation CCII [8], third-generation CCIII [9], have drawn significant attention of the circuit designers and researchers. The CC based structures were being proposed in abundance since 1970 onwards, with different alterations in the basic CC structure, a number of newer elements have been introduced for better utilization [10]-[23]. To encompass both electronic tunability and for CMOS integration, the operational transconductance amplifier (OTA)-C [24] configurations were also significantly inspected beyond 1985. The topologies using current feedback operational amplifier (CFOA) [25] and its variants such as current controlled current feedback amplifier (CC-CFA) [26] differential voltage current feedback amplifier (DVCFA) [27] and differential difference complementary current feedback amplifier (DDCCFA) [28] came in prominence around 1990 onwards to maintain compatibility with the existing voltage mode topologies. The need for the floating output in some applications led to the design four terminal floating nullor (FTFN) [29] and its variants, fully balanced four-terminal floating nullor (FBFTFN) and operational floating amplifier (OFA) are presented in [30] and [31] respectively.

The operational transresistance amplifier (OTRA) [32]-[35] implements a current control voltage source and its generalization is current differencing buffered amplifier (CDBA) [36]. Another interesting, current mode ABB, which is well suited for on-chip implementation, is current differencing transconductance amplifier (CDTA) [37]. Differential voltage current conveyor (DVCC) [38] and its variants such as differential

voltage current conveyor transconductance amplifier (DVCCTA), current controlled current conveyor transconductance amplifier (CCCCTA) are reported in [39] and [40] respectively. Current controlled current follower transconductance amplifier (CFTA) [3] and its variant modified current MC-CFTA [41] provides parasitic resistance R_f that can be controlled by the bias current. Differential-difference current conveyor (DDCC) [42], differential voltage controlled current source (DVCCS) [43], differential difference amplifier (DDA) [44], differential difference OFA (DDOFA) [45], universal voltage conveyor (UVC) [46] are some other ABBs available in the literature. These active blocks are used for the realization of various signal processing and generation circuits.

Signal generators can be divided into two categories; function generators and arbitrary waveform generators (AWGs). Function generators are designed to generate periodic waveforms at precise frequencies, whereas AWGs, is designed to generate large and often complex waveforms. The function generators can broadly be classified as (i) linear generators (ii) nonlinear generators. A linear generator can generate oscillations which are sinusoidal and periodic, whereas nonlinear generators provide pulses, ramp and sawtooth waveform, etc. Unlike function generators, AWGs can generate any arbitrarily defined waveshape as their output.

Sinusoidal oscillators (SOs) find numerous applications in various fields such as applications in communication such as signal generators, spectrum analyzers, A/D converters, etc., measurement and instrumentation systems [47]-[49]. This electronic function provides standard test and carrier signals for communication and instrumentation circuits and also acts as the starting signal for the generation of several other types of test signals. Therefore, these topologies acquired ample attention among various researchers and inspired to develop new topologies, with better performance than earlier known circuits, that are most suited for these applications. These new SO

topologies have been realized employing a variety of ABBs such as op-amps [47], [50]-[56], CCII [57]-[65], OTA [57], [66]-[67], CCCII [68]-[70]. The designs proposed in [59], [71]-[80] use CFOA. The structures proposed in [38], [81]-[82] use DVCC, whereas the design of [83] utilizes DVCCTA. The CDTA based SOs are available in [84]-[85], while CCCCTA based oscillator is presented in [86]. The VDTA and MCCCFTA based oscillators are discussed in [87]-[88] and [41], [89]respectively. The structure of [90] is designed using OTA and CCCCTA, whereas [42] uses OTA and DDCC. Combination of OTA and current controlled current difference transconductance amplifier (CCCDTA) is reported in [91]. Reference [92] proposes DDCC and VDTA based SO and the oscillator presented in [93] is based on CCII and UVC.

The OTRA [32] is a high gain current input, voltage output amplifier and has gained much consideration from several researchers, due to its inherent pros like bandwidth independent of closed-loop gain, higher slew rate and simplicity in assimilating the effect of parasitic capacitances at the input ports. The parasitic impedances at input and output terminals of OTRA are low and have a negligible effect on circuits. As the output of OTRA can be used without a buffering device so these circuits can easily be cascaded. Therefore, OTRA has been explored in the recent past to develop various applications [94] such as immitance simulators [95]-[103], filters [35], [104]-[139], inverse filters [140], analog multipliers and dividers [141]-[142], relaxation oscillators and multivibrators [143]-[148] and various other applications such as instrumentation amplifier [149], proportional derivative controller [150], pulse width modulator [151], digital-to-analog converter (DAC) [152], field-programmable analog array (FPAA) [153], PID controller [154], semi-Gaussian shaper [155] , time marker generator [156], voltage transfer characteristics generator [157], and linear signal generation circuits (SOs) etc.

In this work, OTRA is chosen for the development of sinusoidal oscillators.

1.2 Related Literature and Scope of Work

The available literature on SO designed using OTRA can be categorized based on 1) number of OTRAs used in the topology 2) a number of output phases 3) order of the circuit 4) tuning law of the oscillation frequency.

The available literature on SO designed using OTRA can be classified into four categories as detailed below:

1) Category I- on the basis of number of OTRAs used in the topology.

2) Category II- on the basis of number of output phases.

3) Category III- on the basis of the order of the circuit.

4) Category IV- on the basis of tuning law of the oscillation frequency.

Category I

On the basis of the number of OTRAs used the literature is further classified as (i) single OTRA based oscillators [158]-[170], (ii) two OTRA based SOs [35], [166]-[167], [170]-[181] and (iii) SOs using three OTRAs [182]-[183]. A further delving revealed that most of the single OTRA based SOs are second order structures [158]-[159], [161]-[166] and only single topology [160] is a third order SO (TOSO). It is worth noticing that in the TOSO of [160], the capacitive component spread in oscillation condition is large, which is not favorable for IC implementation. It may, therefore, be concluded that there is a lean presence of single ABB based TOSO in literature, which led authors to present a single ABB based TOSO structure.

Category II

On the basis of number of output phases the SOs can be divided in (i) single-phase oscillators [158]–[165], [167]-[170], [178]-[180] (ii) quadrature oscillators (QO) [35], [166]-[167], [171]-[178], [181]-[183] and (iii) multiphase sinusoidal oscillators (MSO) [184]–[186]. Among several kinds of oscillators, QO (sinusoidal signals with 90^o phase difference) has acquired ample attention by circuit designers because of its wide range of applications in telecommunications, measurements, etc. Therefore, many QO topologies based on OTRA are designed and readily found in the literature [166]-[167], [171]-[178], [182]-[183]. Among these topologies, no OTRA based QO qualifies for generating low frequency (LF) quadrature outputs. In this work, a new OTRA based electronically tunable low frequency quadrature oscillator (LFQO) is presented. To the best of the author's knowledge, this is the first OTRA based LFQO.

Further, from a literature survey, it reveals that several third order QO designs [171]-[173], [182]-[183] are also available. These QOs are in general based on forming closed loop using lossy and lossless integrators and can be classified in particular as those using (i) two lossy and one lossless integrators [183], (ii) one lossy and two lossless integrators [183] (iii) a second order low pass filter followed by an integrator [172] (iv) three lowpass filters and gained feedback around the loop (v) High pass filter and differentiator [171]. The structures of [173], [182] are based on intuitive design methods. However, for controlling the FO, the topology [172] suffers from the tracking problems inherent in dual-element control and topology in [173] has capacitive FO control, which is not suitable IC integration viewpoint. The SOs discussed in [183] (Figure 2) lack independent tuning. New realizations of third order QOs are designed in this work that adds to the present repertoire of OTRA based QOs.

Category III

Based on order of the SO topologies they can be divided in to second order [35], [158]-[159], [161]–[170], [174]–[181] and third order oscillators [160], [171]-[173], [182]-[183].

Category IV

Based on the tuning expression OTRA based SOs can be divided into oscillators having tuning expression in the form of 1/2πRC [35], [158]-[165], [167]-[187] and SOs are having tuning law of the form $\frac{\sqrt{|1-k|}}{2\pi RC}$ where *K* is resistor ratio [166]. On the other hand, the structures presented in [35], [158]-[187] are suitable for achieving medium to high frequencies. The topology in [166] uses two OTRAs having tuning law of the form $\frac{\sqrt{|1-k|}}{2\pi RC}$. This type of tuning law used to generate LF oscillations by employing less passive component spread, which ultimately reduces significant area overhead in IC implementation. Further, most of the second order SOs [158]-[159], [161]-[165] have an expression for the frequency of oscillation (FO) of form 1/2πRC, which is suitable for generating frequencies ranging from medium frequencies (MF) to high frequencies (HF).

However, to ensure a wide range of frequencies (very low frequencies (VLF) to high frequencies) with less sensitivity to passive component variations at all frequencies, FO should be of the form $\sqrt{k}/2\pi$RC where *k* is resistive gain. This has motivated the development of SOs having an oscillation frequency of the form $\sqrt{k}/2\pi$RC. An extensive literature survey suggests that although numerous OTRA based SOs have been advanced, the evaluation of non-linearity and harmonic distortion (HD) factors of SOs have not been carried out. To fill this void OTRA based mathematical formulation HD analysis is carried out in this work by proposing Weinbridge SO topology.

1.3 Objectives

This work presents several OTRA based SO topologies which provide additional features and advantages not available in previously known OTRA oscillator circuits. Based on the literature survey and identified research gaps following objectives are set:

i. To design new single OTRA based second order SOs
ii. To develop a single OTRA based TOSO topology with the reduced component spread in the condition of oscillation (CO).
iii. To design oscillator topologies with a wide frequency range.
iv. To develop OTRA based QOs having independent CO, FO tuning feature
v. To design OTRA based Wien bridge oscillator and to carry out its harmonic analysis

1.4 Organization of the Dissertation

The following section presents the sequencing of chapters in the thesis:

Chapter 1:

This chapter takes a detailed look at the significance of signal generation circuits and presents a review of existing literature available on OTRA based sinusoidal oscillators.

Chapter 2:

Characterization of OTRA realizations using (i) commercially available AD844 (CFOA) ICs and (ii) CMOS based integrated circuit implementation is presented in this chapter to set the groundwork for the material that follows. Functional verification of CMOS OTRA circuit has been carried out through simulations using Cadence Virtuoso analog design Environment (ADE) spectre tool at 0.18μm CMOS technology node. The schematic driven and post layout simulation results have been presented in this chapter.

Chapter 3:

This chapter is devoted to the design of single OTRA based sinusoidal oscillators. Two new second order SOs and one TOSO each employing one OTRA and few passive components have been presented in this chapter. The functionality of all proposed structures is verified through simulations as well as experimentation using CFOA based realization of OTRA.

Chapter 4:

This chapter of the thesis extends into the designing of quadrature oscillators and in all five QO topologies have been proposed. The first one is a second order structure and it qualifies for low frequency operations as well without having large component spread. One of the third order quadrature oscillator (TOQO) topology adapts the scheme of using second order high pass filter and a differentiator in a feedback loop whereas the other three topologies are derived from an inverse filter based generalized structure.

Chapter 5:

This chapter presents four new electronically tunable sinusoidal oscillators. Each of the proposed SO consists of forward path derived from a generic structure along with one/two OTRA based resistive gain stages or integrator in its feedback path. All the proposed SOs enjoy independent tuning of the FO through resistors without affecting the CO. One of the structures also provides a quadrature output. The proposed SOs have been successfully implemented and verified in 0.18µm CMOS technology node using Cadence Virtuoso ADE spectre tool. Both schematic driven and post-layout simulation results have been included.

Chapter 6:

This chapter presents an OTRA based Wien bridge oscillator. The mathematical formulation of harmonic analysis is presented to characterize the linear performance of

the proposed oscillator. The workability of the proposed Wien bridge oscillator is verified through SPICE simulations followed by experimental results.

Chapter 7:

This chapter presents a summary of the work presented in the thesis and future scope.

CHAPTER 2
OPERATIONAL TRANSRESISTANCE AMPLIFIER (OTRA)

2.1 Introduction

The CM signal processing has grown rapidly in the past few decades and demonstrated to be a viable design technique to provide efficient solutions to circuit design problems. This evolution has resulted in the emergence of numerous CM analog building blocks [3], [5].

The OTRA [32], [34], [188] is one among these blocks and has gained much consideration from several researchers, due to its inherent pros like bandwidth independent of closed-loop gain, higher slew rate and simplicity in assimilating the effect of parasitic capacitances at the input ports. As a result, OTRA is being used widely for signal processing and generating applications [94] and the references cited therein.

It is interesting to note that topologies developed employing OTRA as ABB has an advantage from the current processing capabilities at the input terminals and can directly drive the existing VM signal processing circuits, thus eliminating the requirement of additional circuitry and associated power consumption, at the output.

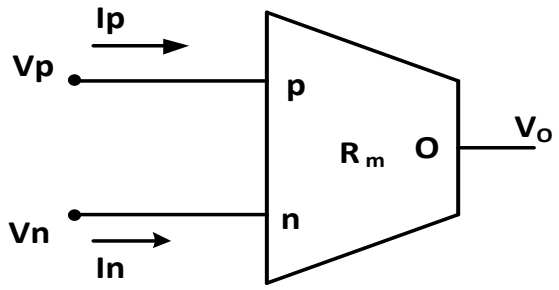
In this chapter, OTRA characterization, using CFOA and CMOS, has discussed in detail, followed by nonideal analysis using a single pole and active resistor realization in OTRA based Circuits.

2.2 Basics of OTRA

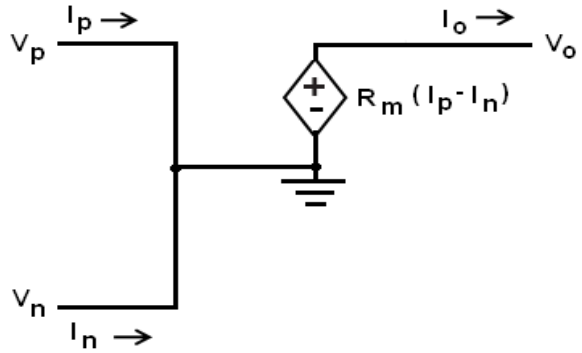
OTRA is a high gain current input voltage output analog building block [32]. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances and hence is a suitable choice for high-frequency applications. The circuit symbol of OTRA is shown in Figure 2.1 (a) and the port characteristics are given by (2.1), which signifies the output voltage (V_o) is equal to

the product of the difference of input currents (I_p, I_n) and transresistance gain R_m. For ideal operations, the R_m of OTRA approaches infinity and forces the input currents to be equal.

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix} \tag{2.1}$$



(a)



(b)

Figure 2.1. (a) Schematic symbol representation of OTRA (b) Equivalent of OTRA

An equivalent circuit model of OTRA is illustrated in Figure 2.1(b). The equivalent circuit model of a practical OTRA is depicted in Figure 2.2, where R_p and R_n characterize the terminal resistances of p and n ports, respectively.

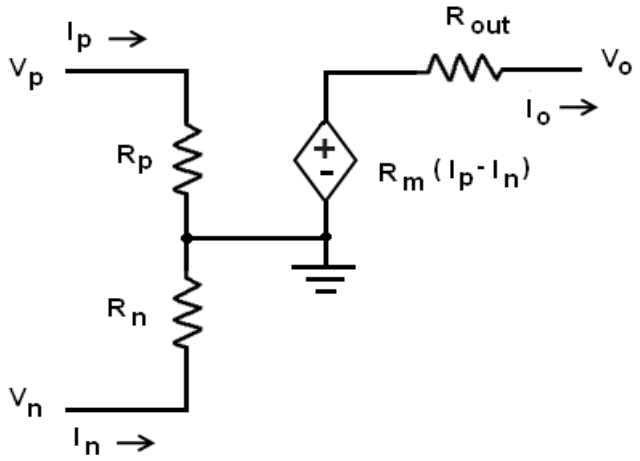


Figure 2.2. Equivalent circuit model of a practical OTRA

2.3 Nonideal Analysis

Nonideal analysis of OTRA using a single-pole is presented in this section, which will come handy to analyze the behavior of proposed circuits in this work in the presence of OTRA nonidealities.

The performance of the proposed OTRA designs may deviate from the original results because of the OTRA nonidealities. As already discussed, because of internally grounded input terminals, most of the parasitics affecting the performance of OTRA can be ignored. Ideally, R_m is assumed to approach infinity. However, practically, its value is frequency-dependent.

Considering a single-pole model, R_m can be expressed as

$$R_m(s) = \left(\frac{R_o}{1 + \frac{s}{\omega_o}} \right) \tag{2.2}$$

Where R_o represents the dc transresistance gain. For high-frequency applications, the $R_m(s)$ reduces to

$$R_m(s) = \frac{1}{sC_p} \tag{2.3}$$

where C_p in (2.3) designates the parasitic capacitance of OTRA ; $C_p = \frac{1}{R_O \omega_O}$

2.4 OTRA Implementation

In this section, OTRA implementations that are used in the proposed work are presented. These implementations are based on:

(i) Using commercially available AD844 (CFOA) ICs [189].

(ii) Using integrated circuit implementations [27], [36]-[40].

2.4.1 CFOA based Implementation and its Characterization

The symbol of the CFOA is shown in Figure 2.3. An OTRA can be realized using two AD844 ICs [189] connected, as depicted in Figure 2.4.

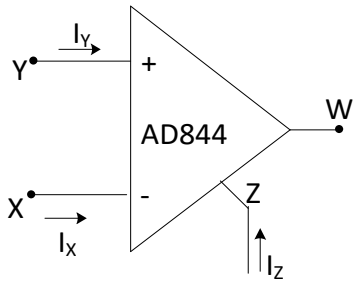


Figure 2.3. Symbol of IC AD 844

By using terminal equations of CFOA $V_X = V_Y; I_Y = 0; I_Z = I_X; V_W = V_Z$, Figure 2.4 may be analyzed to verify the terminal characteristics of OTRA, as given below. The voltages at different ports can be written as

$$V_p = V_{X1} = V_{Y1} = 0 \tag{2.4}$$

$$V_n = V_{X2} = V_{Y2} = 0 \tag{2.5}$$

$$V_{o1} = V_{Z1} = V_{2n} = V_{2p} = 0 \tag{2.6}$$

From Figure 2.4 the currents can be evaluated as

$$I_{Z1} = I_{X1} = I_p \tag{2.7}$$

$$I_{Z2} = I_{X2} = I_n - I_{Z1} = I_n - I_p \tag{2.8}$$

From above-quoted equations, the output port voltage (V_o) can be yielded as

$$V_o = V_{Z2} = -I_{Z2}.R_Z = -R_Z\left(I_n - I_p\right) \tag{2.9}$$

$$V_o = R_Z\left(I_n - I_p\right) \tag{2.10}$$

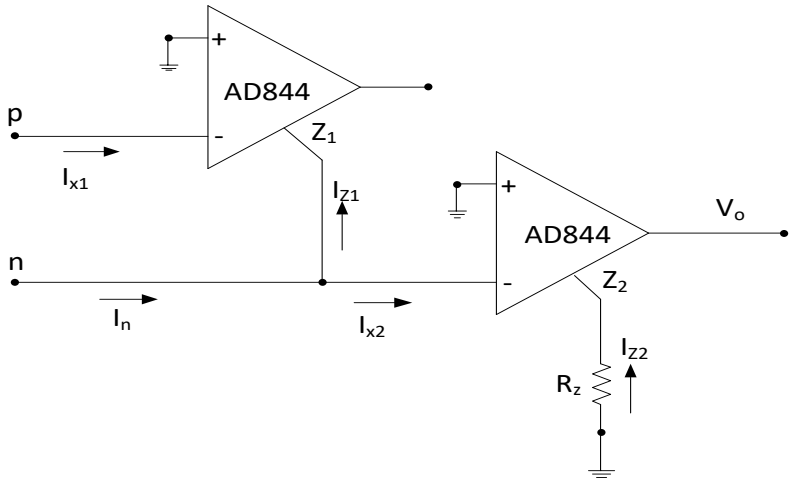


Figure 2.4. IC AD 844 based OTRA [189]

It may be observed that (2.10) is similar to (2.1) provided that the value of R_Z be very high. To have large resistance gain, the resistance R_Z at Z terminal of the second AD844 is kept high.

The functionality of the OTRA has been verified through SPICE simulations, where the OTRA is realized using commercially available IC AD844N. The supply voltages are chosen as ± 8.5V.

The DC characteristics of CFOA based OTRA are plotted in Figures 2.5. The offset current is obtained as 0.1 µA. The magnitude and phase responses are depicted in Figures 2.6 (a) and (b), respectively. The DC open loop transresistance gain (R_o) for OTRA is obtained as 136 dBΩ.

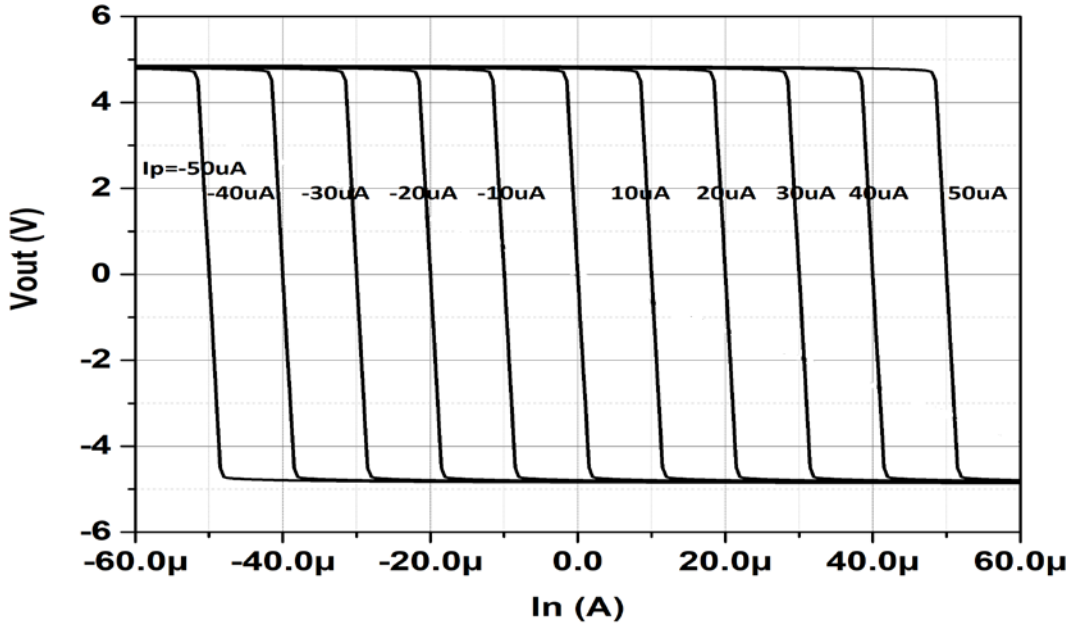
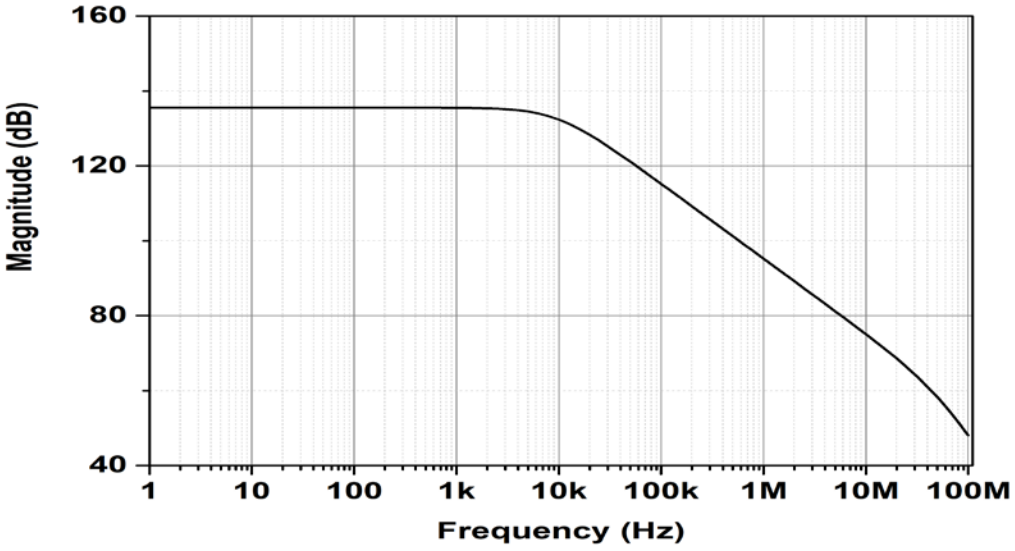
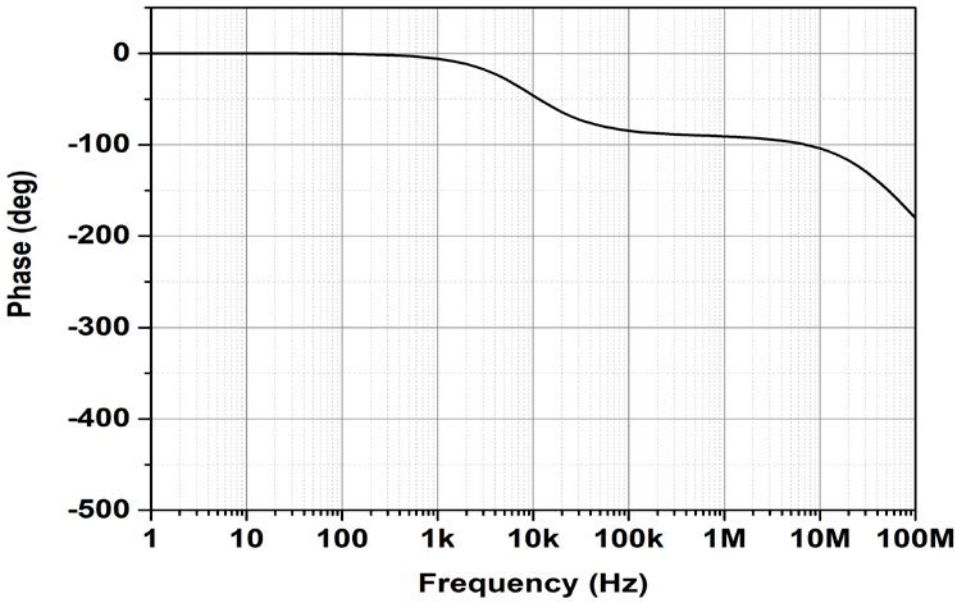


Figure 2.5. DC characteristics of CFOA based OTRA



(a)



(b)

Figure 2.6. Frequency response of CMOS based OTRA (a) Magnitude (b) Phase

The input resistance is plotted in Figure 2.7 and its value is observed to be 50 Ω.

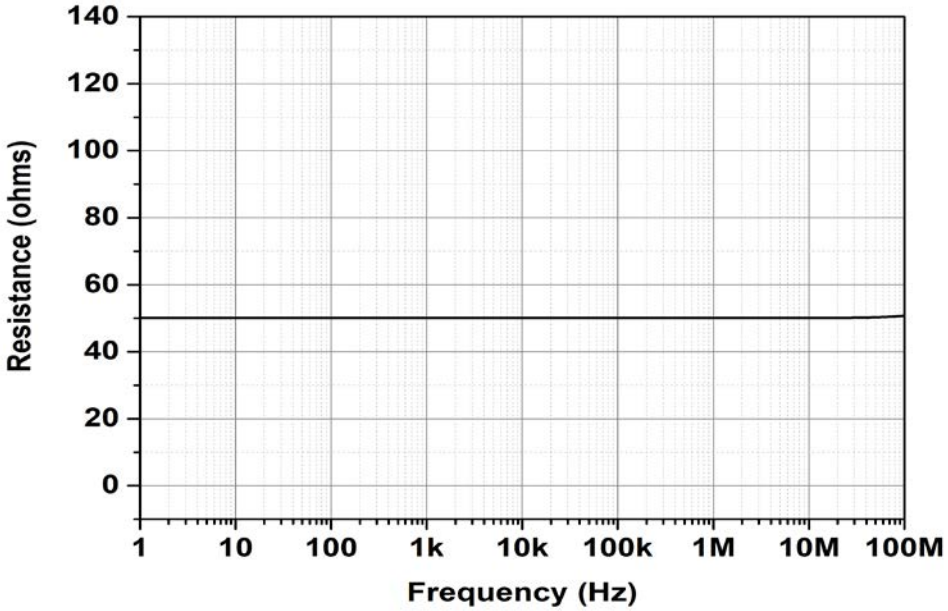


Figure 2.7. The input resistance of CFOA based OTRA

2.4.2 CMOS based Implementation and its Characterization

The CMOS realization of OTRA [32] is shown in Figure 2.8. It is based on the cascaded connection of the modified differential current conveyor (MDCC) and a common source amplifier.

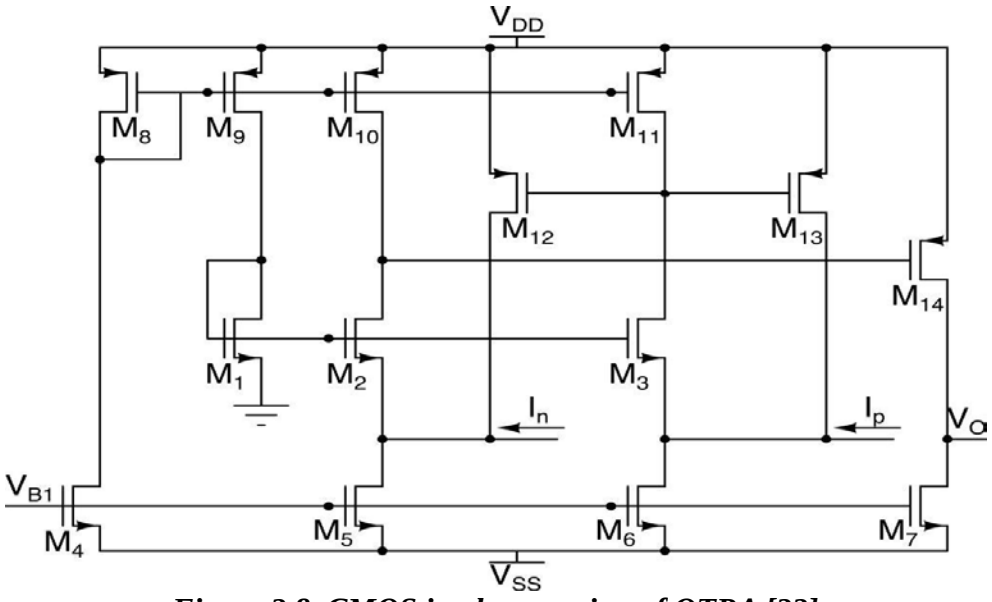


Figure 2.8. CMOS implementation of OTRA [32]

Assuming that all transistors operate in saturation region and each of the groups of the transistors (M_1-M_3), (M_5 and M_6), (M_8-M_{11}) and (M_{12} and M_{13}) are matched, the circuit operation can be explained as follows. The current mirrors formed by (M_8-M_{11}) force equal currents (I_B) in the transistors M_1, M_2 and M_3. This operation drives the gate to source voltages of M_1, M_2 and M_3 to be equal and in turn, forces the two input terminals to be virtually grounded.

The current mirrors formed by the transistor pairs (M_{10} and M_{11}) and (M_{12} and M_{13}) provide the current differencing operation, whereas the common source amplifier (M7, M_{14}) serves as high gain stage.

Table 2.1. Aspect Ratios of Transistors

Transistor	W(µm)/L(µm)
M1–M3	36/0.9
M4	3.6/0.9
M5, M6	10.8/0.9
M7	3.6/0.9
M8-M11	18/0.9
M12,M13	36/0.9
M14	18/0.18

The functionality of CMOS OTRA [32] is verified through the Cadence Virtuoso ADE spectre tool using 0.18µm parameters. Supply voltages are taken as ±1 V and bias voltage as -0.3 V. The aspect ratios of transistors are given in Table 2.1. The Complete layout of CMOS OTRA is shown in Figure 2.9 and the total die area is about 1753.4433 μm^2 (29.19µmx 60.07µm).

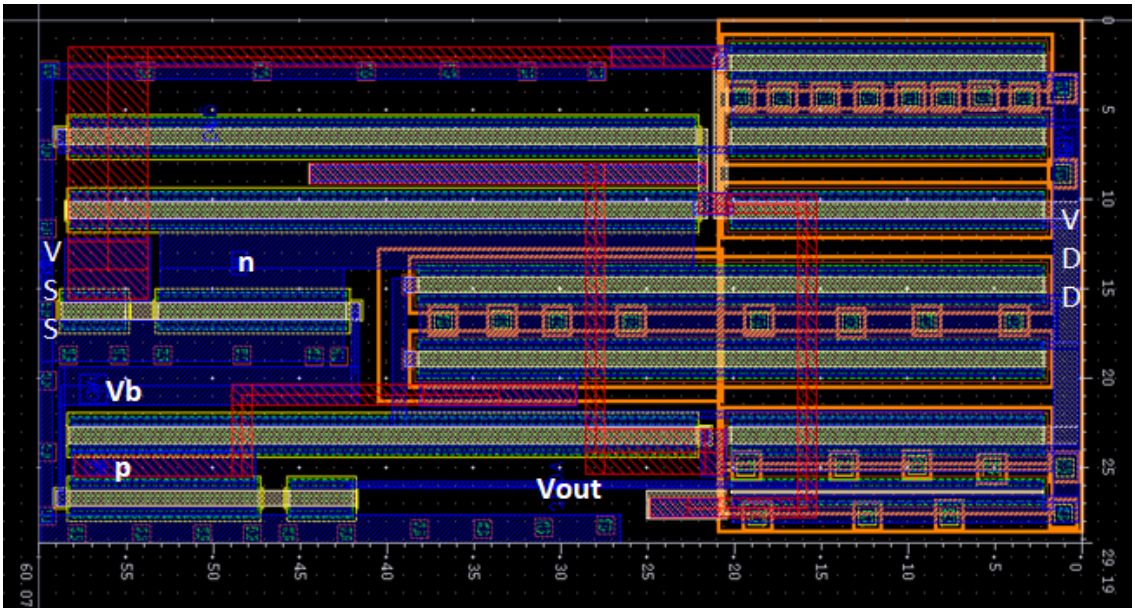


Figure 2.9. The complete physical layout of OTRA

The DC characteristics of the simulated OTRA are shown in Figure 2.10, which shows that the input differential current range is -25µA to 25µA. The pre and post-layout magnitude and phase responses are depicted in Figures 2.11 (a) and (b), respectively.

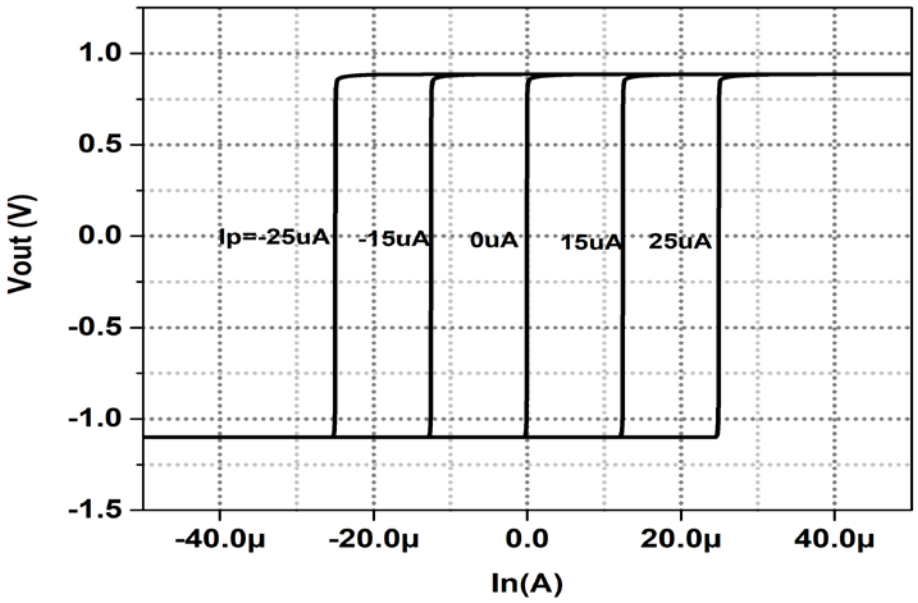
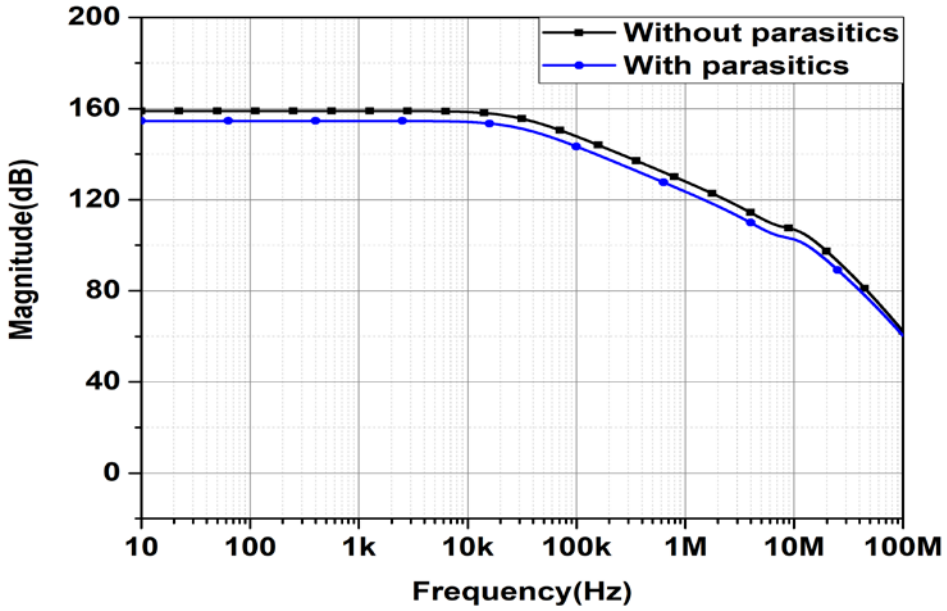
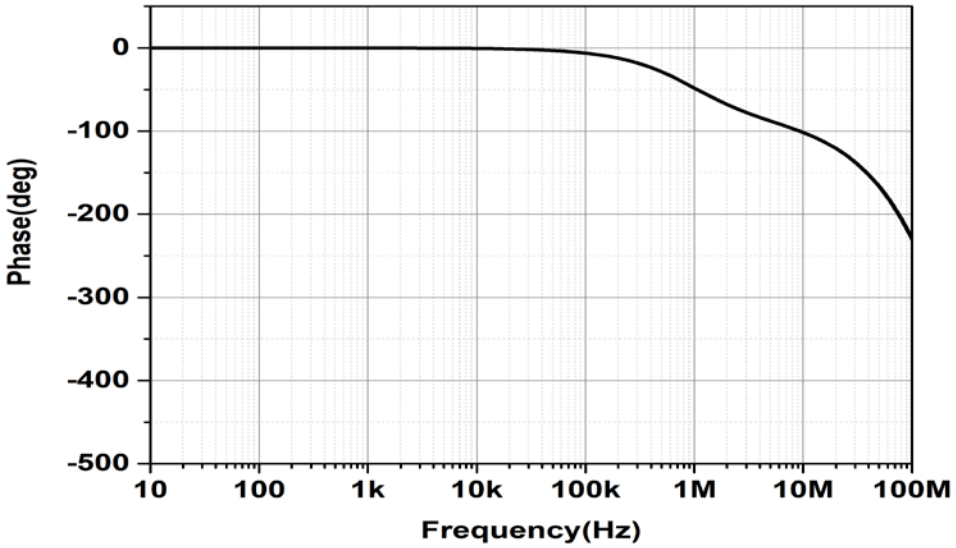


Figure 2.10. DC characteristics of CMOS based OTRA



(a)



(b)

Figure 2.11. Frequency response of CMOS based OTRA (a) Magnitude (b) Phase

The layout implemented is verified by physical verification checks [190] such as Design Rule Check (DRC), Layout vs. Schematic check (LVS) and RC parasitic extraction. Due to the inclusion of parasitics, the post layout simulated magnitude response is slightly in deviation from one obtained from schematic driven simulation.

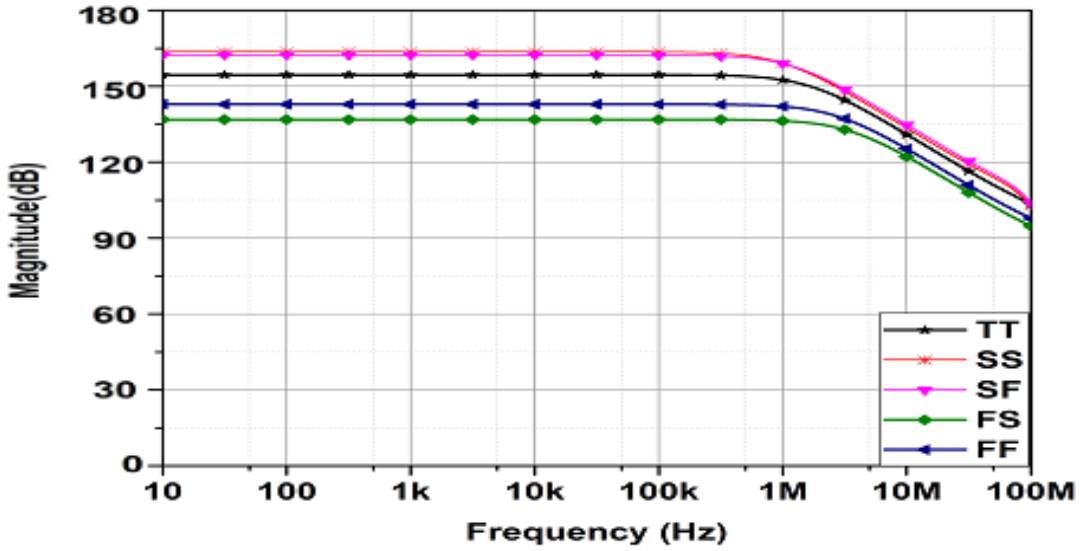


Figure 2.12. Frequency response of CMOS based OTRA at different corner parameters

The postlayout DC transresistance gain is observed to 157 dBΩ as against 160 dBΩ prelayout value. Figure 2.12 shows the effect of different process corners (SS, SF, TT, FS, FF) on the output waveform. The input resistance is plotted in Figure 2.13 and its value is observed to be 3.8 Ω till 2 MHz.

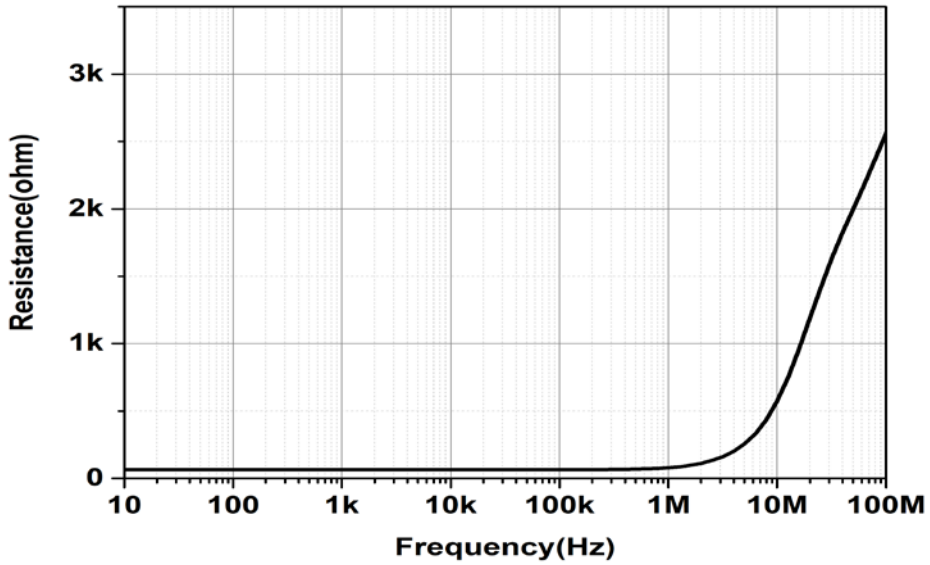


Figure 2.13. Input impedance of OTRA

The gain-bandwidth product, parasitic capacitance and power dissipation are obtained as 440 GHz.Ω, 5.03 fF and 226.26 µW respectively. These results are summarized in Table 2.2.

Table 2.2. Parameters of CMOS OTRA circuit

Technology	0.18µm CMOS
DC open loop transresistance gain	157 dBΩ
Gain bandwidth product	440 GHzΩ
Power dissipation	226.26 µW
Parasitic capacitance	5.03fF
Input resistance	3.8Ω
Offset current	71.2nA

2.5 Active Resistor Realization in OTRA based Circuits

The current differencing property of the OTRA makes it feasible to realize the resistors connected to the input terminals of OTRA, using MOSFETs with complete nonlinearity cancellation [35]. Each resistor implementation requires two matched NMOS transistors, as shown in Figure 2.14.

Essentially, both the transistors should operate in the ohmic region. Figure 2.15 shows a typical MOS based implementation of resistance connected at the inverting terminal of OTRA, where nodes X and Y need to be connected to inverting and non-inverting terminals of the OTRA, respectively. The currents flowing into the two transistors can be specified as

$$I_x = k_n(V_a - V_T)V_{DS1} + x_1 V_{DS1}^2 + x_2 V_{DS1}^3 + ...$$

$$= k_n(V_a - V_T)(V_1 - V_2) + x_1(V_1 - V_2)^2 + x_2(V_1 - V_2)^3 + ... \quad (2.11)$$

$$I_y = k_n(V_b - V_T)V_{DS2} + x_1 V_{DS2}^2 + x_2 V_{DS2}^3 + ...$$

$$= k_n(V_b - V_T)(V_1 - V_2) + x_1(V_b - V_2)^2 + x_2(V_b - V_2)^3 + ... \quad (2.12)$$

Since the transistors M_1 and M_2 are perfectly matched and have the same drain to source voltages, the difference of the currents flowing into the two transistors can be computed as

$$(I_x - I_y) = k_n(V_a - V_b)(V_1 - V_2)$$

$$= \frac{1}{R}.(V_1 - V_2) \quad (2.13)$$

The resistance value can thus be expressed as

$$R = \frac{1}{\mu_n C_{ox}(W/L)(V_a - V_b)} \tag{2.14}$$

where μ_n = electron Mobility; C_{ox} = Oxide capacitance per unit area; W/L = Effective channel width/ Effective channel length and V_a, V_b are the gate voltages.

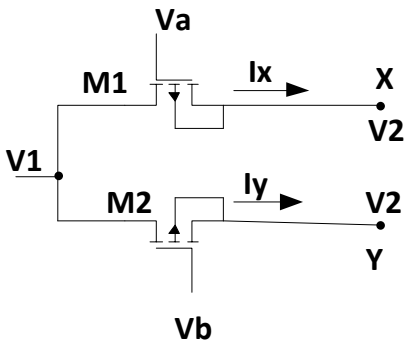


Figure 2.14. MOS implementation of resistance [35]

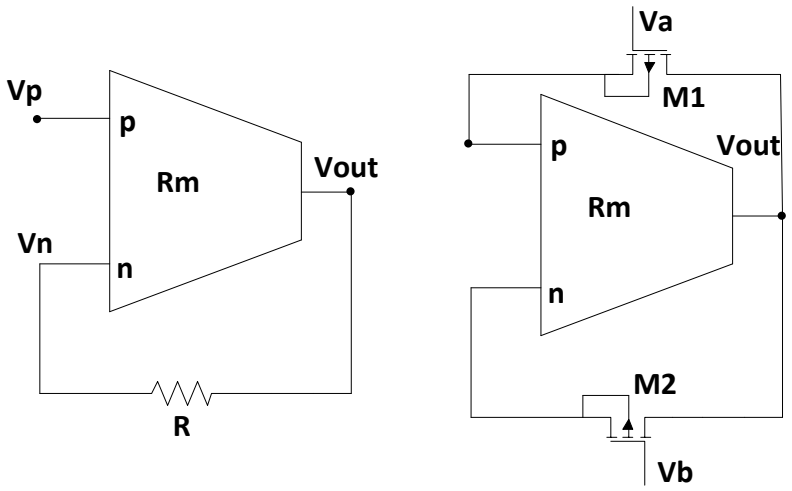


Figure 2.15. MOS implementation of a linear resistance connected between negative and output terminals of OTRA

Further, different values of resistors have been realized using MOSFETs by setting W/L as 1 µm/2.5 µm. Table 2.3 lists the difference of gate controlling voltages required for implementing different resistor values. It also shows the current flowing through corresponding resistors.

Table 2.3. Gate controlling voltages for different resistor values implementation

R(kΩ)	(V_a-V_b) (V)	$I_R(\mu A)$
10.1	0.963	95.3
10.2	0.953	93.4
10.3	0.944	91.6
11	0.875	79.5
12	0.802	66.8
13	0.741	57
14	0.688	49.1
15	0.642	42.8
16	0.602	37.6
17	0.566	33.29
18	0.535	29.7

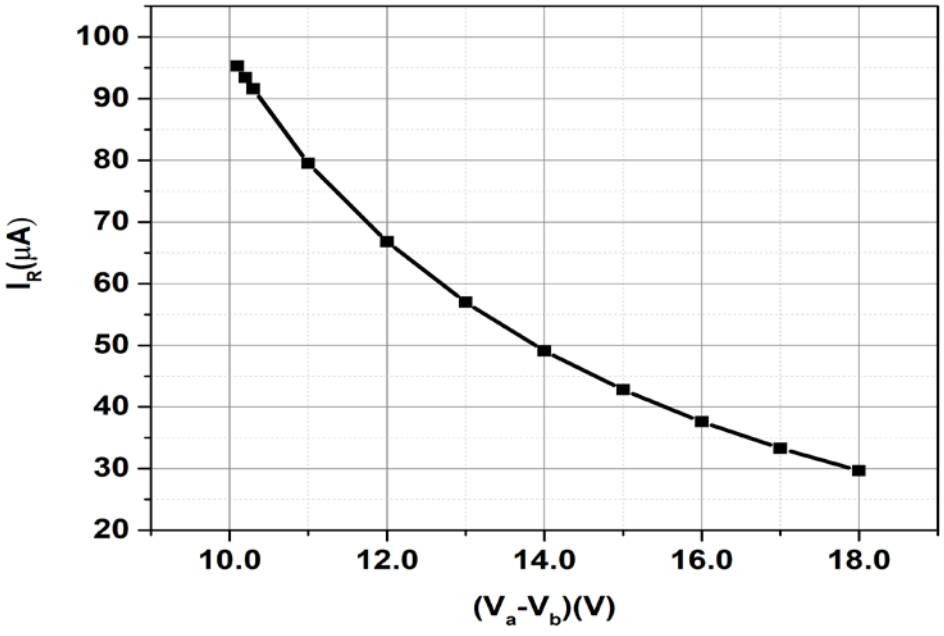


Figure 2.16. Differential gate controlling voltage versus transistor current

The graph between gate controlling voltages and its current is depicted in Figure 2.16.

2.6 Concluding Remarks

In this chapter, CFOA and CMOS based OTRAs are characterized. Nonidealities of practically realized OTRA are also discussed, which would be helpful in performance evaluation of any OTRA based circuit. The active resistor realization in OTRA based circuits is also presented in this chapter.

CHAPTER 3
SINGLE OTRA BASED SINUSOIDAL OSCILLATORS

The content and results of the following papers have been reported in this chapter

[1] K. Gurumurthy, R. Pandey and N. Pandey, “Minimum component count Low frequency sinusoidal oscillator based on Single OTRA,” *IJCTA*, vol. 9, pp. 181–7, 2016. **(SCOPUS)**

[2] K. Gurumurthy, N. Pandey and R. Pandey, “Single OTRA Based Low frequency Sinusoidal Oscillator Realization,” *IOP: Materials Science and Engineering*; vol. 225, 2017. **(SCOPUS)**

[3] K. Gurumurthy, N. Pandey and R. Pandey, “New realization of third order sinusoidal oscillator using single OTRA,” *Int J Electron Commun (AEÜ)*, vol. 93, pp. 182–90, 2018. **(SCI) (IF: 2.82)**

3.1 Introduction

Sinusoidal oscillators (SOs) play a vital role in control, power electronics, instrumentation, measurement, standard test and carrier signals for communications and other electronic systems [47]–[49]. These oscillators may generate signals of various frequencies ranging from very low to very high.

Low frequency (LF) oscillators are a specific class of oscillators, which produce periodic waveforms at a very low frequency generally in (0-20 Hz) range. These are very commonly used for music and speech synthesis and also find applications in various other fields such as testing of various servomechanisms, geophysical systems, biological and biomedical fields [53], [76], [191]. The oscillators, which can produce medium to high frequencies, can be easily designed by implementing tuning expression of the form 1/RC, whereas, designing of LF oscillators with lower passive component spread needs a special tuning function of the form $\frac{\sqrt{|1-n|}}{2\pi RC}$.

The SOs are most commonly designed using a forward active network of single/multiple ABBs based amplifiers/filters and passive networks placed in the feedback loop. The oscillator topologies with a reduced number of ABBs and passive components lead to power and area efficient designs wherein the parasitic effects are also reduced. Therefore, this chapter is devoted to the design of single OTRA based SOs. It is pertinent to mention here that with reference to harmonic distortion performance, the TOSOs are always preferred over second order oscillators. This led us to present a third order SO (TOSO) also in this chapter.

3.2 Single OTRA based Second Order SOs

This section elaborates on the proposed second order SO topologies. Each topology is described first, which is followed by its MOS resistor based realization. The effect of nonidealities of OTRA on these structures is analyzed in the subsequent section.

3.2.1 Proposed Topology I

The proposed topology I is shown in Figure 3.1, using routine analysis the characteristic equation (CE) of the SO can be expressed as

$$s^2 C_1 C_2 + s\left(\frac{C_2}{R} - \frac{C_1}{R_1}\right) - \frac{1}{R_1 R} + \frac{1}{R^2} = 0 \tag{3.1}$$

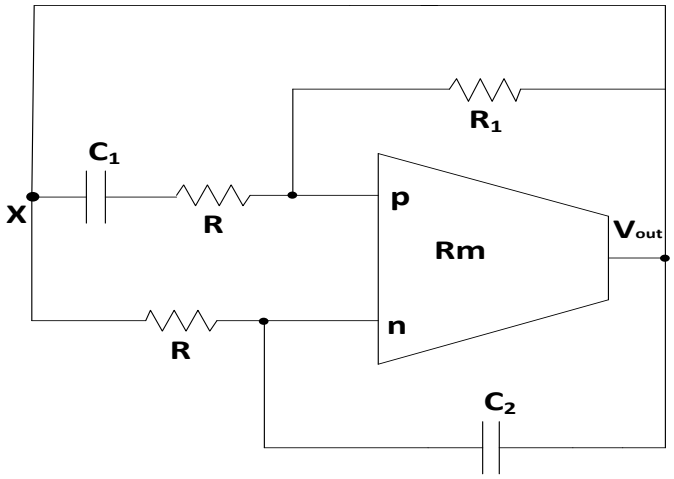


Figure 3.1. Proposed single OTRA SO topology I

The CO and FO (f_o) for topology I from CE are given as

$$\left.\begin{aligned} &\text{CO}: C_2 R_1 = C_1 R \\ &\text{FO}: f_o = \frac{1}{2\pi R\sqrt{C_1 C_2}}\left[1-n\right]^{\frac{1}{2}}; \text{where } n = \frac{R}{R_1} \end{aligned}\right\} \tag{3.2}$$

By choosing the appropriate value of *n*, the proposed oscillator can provide low to medium frequencies.

3.2.2 Proposed Topology II

The proposed topology II is depicted in Figure 3.2 and its CE is expressed as

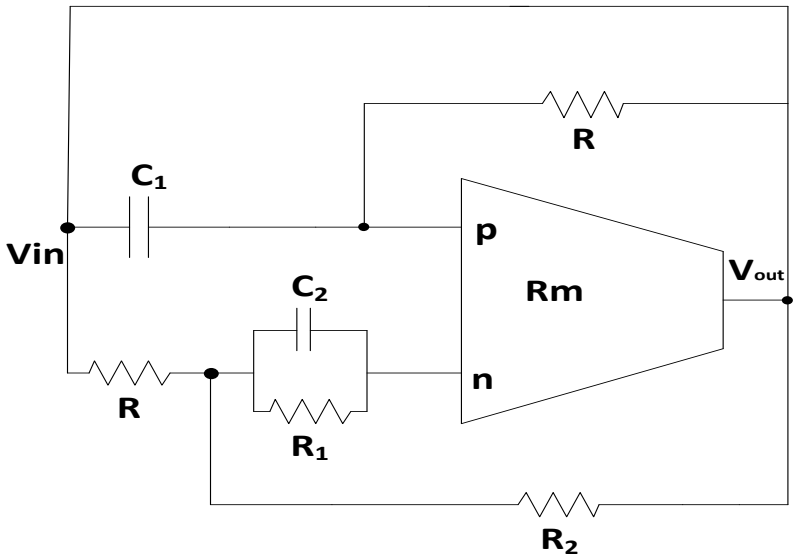


Figure 3.2. Proposed single OTRA SO topology II

$$\begin{cases} s^2C_1C_2R^2R_1R_2 + s\left[C_1R_1R_2R + C_1R^2(R_1+R_2) - C_2R^2R_1\right] \\ +R_1R_2 - R^2 + RR_1 = 0 \end{cases} \tag{3.3}$$

The CO and FO may be obtained as

$$\left.\begin{aligned} &\text{CO}: C_1R_2(R+R_1) = RR_1(C_2 - C_1) \\ &\text{FO}: f_o = \frac{1}{2\pi R\sqrt{C_1C_2}}\left[1+\left(\frac{R}{R_2} - \frac{R^2}{R_1R_2}\right)\right]^{\frac{1}{2}} \end{aligned}\right\} \tag{3.4}$$

The FO can further be written as

$$f_o = \frac{1}{2\pi R\sqrt{C_1C_2}}[K]^{\frac{1}{2}} \tag{3.5}$$

Where K =1+n and n denotes the resistor ratio $\left(\frac{R}{R_2} - \frac{R^2}{R_1R_2}\right)$.

The multiplication factor *K* can be selected to be greater than or less than unity by choosing the appropriate values of *R*, R_1, R_2. By making $\frac{R}{R_1}<1$ the *K* value may be chosen to be greater than unity, whereas if $\frac{R}{R_1}>1$ the *K* value is set to be less than one. Thus, the proposed oscillator can provide frequencies ranging from LF to MF by simply adjusting *K*.

3.2.3 Proposed Topology III

The proposed topology III is presented in Figure 3.3 and the CE is given by (3.6).

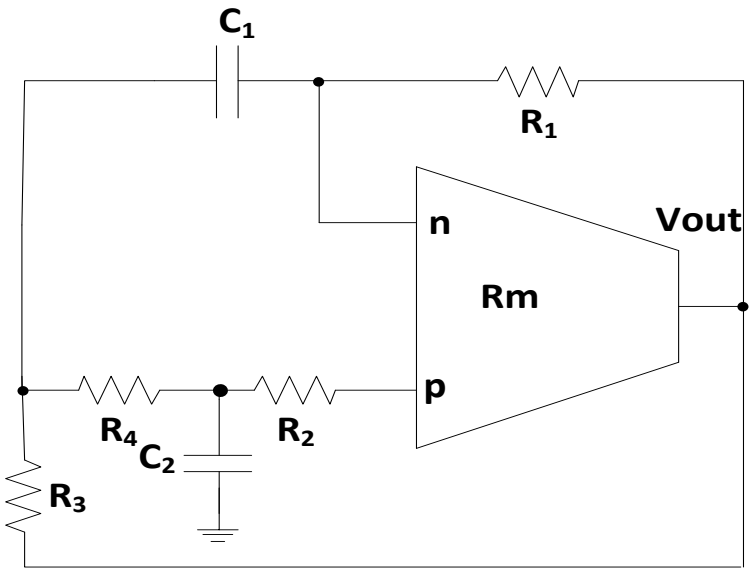


Figure 3.3. Proposed single OTRA SO topology III

$$\begin{cases} s^2+\dfrac{s}{C_1C_2}\left(C_2\left(\dfrac{1}{R_3}+\dfrac{1}{R_4}\right)+\dfrac{C_1}{R_2}+\dfrac{C_1(1-K)}{R_4}\right)+\dfrac{1}{C_1C_2}\left(\dfrac{1}{R_3R_4}+\dfrac{1}{R_2R_4}+\dfrac{1}{R_2R_3}\right) \\ -\dfrac{K}{R_3R_4C_1C_2}=0 \end{cases} \quad (3.6)$$

where $K=\frac{R_1}{R_2}$; by considering equal capacitances, the FO and CO are computed as

$$\text{FO}: f_o = \frac{1}{2\pi C}\sqrt{\frac{1}{R_2R_4}+\frac{1}{R_2R_3}-\frac{2}{R_3R_4}} \tag{3.7}$$

$$\text{CO}: \frac{1}{R_2}+\frac{1}{R_3}=\frac{1}{R_4}; K=3 \tag{3.8}$$

3.2.4 MOS-C implementation of Proposed Topology-I

The current differencing property of the OTRA makes it feasible to realize the resistors connected to the input terminals of OTRA, using MOSFETs with complete nonlinearity cancellation [35], as explained in chapter 2.

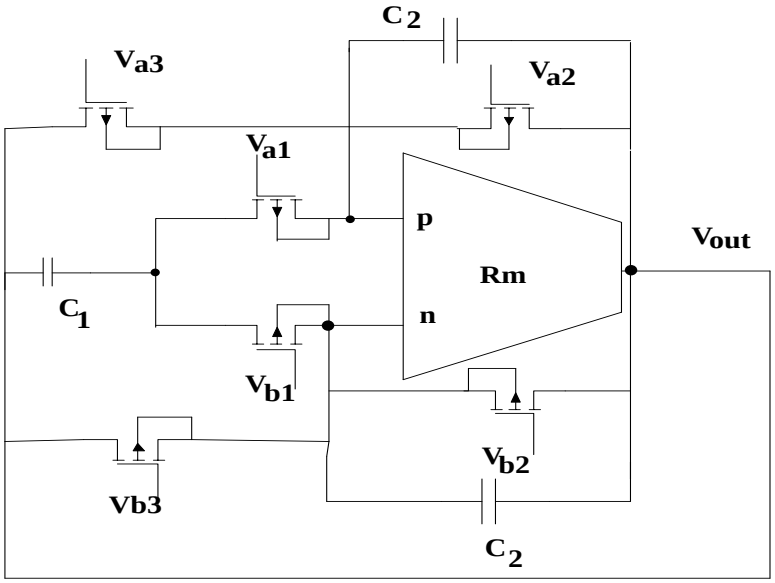


Figure 3.4. MOS-C implementation of proposed topology-I

A thorough inspection of proposed topology-I suggests that all the resistors of Figure 3.1 are MOS realizable and the resulting structure is shown in Figure 3.4. The resistance values can be tuned with the help of gate voltages and thus, the FO can be tuned electronically.

3.2.5 Nonideal Analysis

The performance of the proposed oscillators may deviate from the ideal results because of the OTRA nonidealities. Ideally, R_m is assumed to approach infinity. However, practically, its value is frequency-dependent.

Considering a single-pole model single-pole mode of OTRA in Figure 3.1, the CE of (3.1) modifies to

$$s^2C_1(C_2+C_p)R^2+s[(C_2+C_p)R-C_1\frac{R^2}{R_1}]-\frac{R}{R_1}+1=0 \tag{3.9}$$

The modified CO and FO are computed as

$$\text{CO: } R_1(C_2+C_p)=C_1R$$

$$\text{FO: } \hat{f}_o=\frac{1}{2\pi(C_2+C_p)\sqrt{RR_1}}\left[1-n\right]^{\frac{1}{2}} \tag{3.10}$$

For, Figure 3.2, the CE of (3.2) changes to (3.11) by considering the nonidealities.

$$\begin{aligned} &s^2(C_1+C_p)C_2R^2R_1R_2+s\begin{bmatrix}(C_1+C_p)R_1R_2R+(C_1+C_p)R^2(R_1+R_2)\\-C_2R^2R_1\end{bmatrix} \\ &-R^2+R_1R_2+RR_1=0 \end{aligned} \tag{3.11}$$

The altered CO and FO are computed as

$$\text{CO}:(C_1+C_p)R_2(R+R_1)=RR_1(C_2-(C_1+C_p))$$

$$\text{FO}: \quad \hat{f}_o=\frac{1}{2\pi R\sqrt{(C_1+C_p)C_2}}\left[1+\left(\frac{R}{R_2}-\frac{R^2}{R_1R_2}\right)\right]^{\frac{1}{2}} \tag{3.12}$$

From (3.10) and (3.12), it is observed that there is a slight deviation in FO in the presence of nonidealities. The effect of parasitic capacitances C_p can be eliminated by preadjusting C_1 and C_2, thus achieving self-compensation.

Considering the nonidealities of OTRA, the CE of Figure 3.3 changes to

$$X_1 s^2 + Y_1 s + Z_1 = 0 \tag{3.13}$$

where coefficients X_1, Y_1 and Z_1 are represented respectively as

$$X_1 = C_1 C_2 \left(1 + sC_p R_1 + \frac{C_p}{C_1} R_1 \left(\frac{1}{R_3} + \frac{1}{R_4}\right) + \frac{C_p}{C_2} R_1 \left(\frac{1}{R_2} + \frac{1}{R_4}\right)\right) \tag{3.14}$$

$$Y_1 = C_1 C_2 \left(\frac{1}{C_1}\left(\frac{1}{R_3} + \frac{1}{R_4}\right) + \frac{1}{R_2 C_2} + \frac{(1-K)}{R_4 C_2} + \frac{C_p R_1}{C_1 C_2}\left(\frac{1}{R_2 R_4} + \frac{1}{R_2 R_3} + \frac{1}{R_3 R_4}\right)\right) \tag{3.15}$$

$$Z_1 = \left(\frac{1}{R_2 R_4} + \frac{1}{R_2 R_3} + \frac{1}{R_3 R_4}\right) - \frac{K}{R_3 R_4} \tag{3.16}$$

It is clear that the CE modifies in the presence of nonidealities. However, the effect may practically be ignored by choosing oscillator frequency much below $1/C_p R_1$ and selecting external capacitors of value much higher than C_p. In such a situation, the coefficients X_1, Y_1 and Z_1 modify to

$$X_1 \approx C_1 C_2 ; \tag{3.17}$$

$$Y_1 \approx C_1 C_2 \left(C_2\left(\frac{1}{R_3} + \frac{1}{R_4}\right) + \frac{C_1}{R_2} + \frac{C_1}{R_4}(1-K)\right) \tag{3.18}$$

$$Z_1 = \left(\frac{1}{R_2 R_4} + \frac{1}{R_2 R_3} + \frac{1}{R_3 R_4}\right) - \frac{K}{R_3 R_4} \tag{3.19}$$

By substituting (3.17), (3.18) and (3.19) in (3.13), the CE given by (3.13) reduces to (3.6) and FO, CO are given by (3.7) and (3.8) respectively.

3.2.6 Sensitivity Analysis

The sensitivity is an important performance criterion for any circuit, which enables analog IC designers to choose which elements should be carefully designed to maintain high circuit performance. The sensitivity of FO is calculated with respect to all passive components [48] may be calculated as

$$S_X^{f_o} = \frac{X}{f}.\frac{\partial f_o}{\partial X} \tag{3.20}$$

where X refers to various elements used.

The sensitivity of f_o for Figure 3.1 with respect to circuit components is computed as

$$\left|S_{C_1}^{f_o}\right| = \left|S_{C_2}^{f_o}\right| = \frac{1}{2}; \left|S_{R_1}^{f_o}\right| = \frac{R}{2\left(R_1 - R\right)}; \left|S_R^{f_o}\right| = \frac{2R_1 + R}{2\left(1 - \frac{R}{R_1}\right)} \tag{3.21}$$

The sensitivities of f_o for Figure 3.2 with respect to C_1, C_2, R_2, R_1, R are

$$\begin{cases} \left|S_{C_1}^{f_o}\right| = \left|S_{C_2}^{f_o}\right| = \frac{1}{2}; \left|S_{R_2}^{f_o}\right| = \frac{R(R - R_1)}{2\left[R_1(R + R_2) - R^2\right]}; \\ \left|S_{R_1}^{f_o}\right| = \frac{R^2}{2\left[R_1(R + R_2) - R^2\right]}; \left|S_R^{f_o}\right| = \frac{R_1(2R_2 + R)}{2\left[R_1(R + R_2) - R^2\right]} \end{cases} \tag{3.22}$$

The sensitivities of f_o for Figure 3.3 with respect to C, R_2, R_3, R_4 are

$$\begin{cases} \left|S_C^{f_o}\right| = 1; \left|S_{R_3}^{f_o}\right| = \frac{1}{2\left[1 + R_3/(R_4 - 2R_2)\right]}; \left|S_{R_4}^{f_o}\right| = \frac{1}{2\left[1 + R_4/(R_3 - 2R_2)\right]} \\ \left|S_{R_2}^{f_o}\right| = \frac{1}{2\left[1 - 2R_2/(R_3 + R_4)\right]}; \end{cases} \tag{3.23}$$

From (3.21) to (3.23), it can be seen that all the sensitivities with respect to passive components and parasitic capacitances are less than unity in magnitude.

3.2.7 Simulation Results

The workability of the proposed structures is tested using SPICE simulations and the CMOS implementation [32] of OTRA is used. The process parameters are taken as 0.18 µm provided by MOSIS (AGILENT) for the transistors used in OTRA. Supply voltages V_{SS} and V_{DD} used are ± 1.5V.

For topology in Figure 3.1 simulations are carried out for f = 45 Hz by selecting R_1= 11 kΩ, R= 10 kΩ, C_1= 110 nF, C_2= 100 nF. The corresponding timing waveform and its frequency spectrums are depicted in Figure 3.5 and Figure 3.6, respectively. The Total harmonic distortion (THD) is observed to be 2.24%. Figure 3.7 shows the variation of frequency with resistor ratio '*n*'. At n = 0.8 the frequency is 1 Hz.

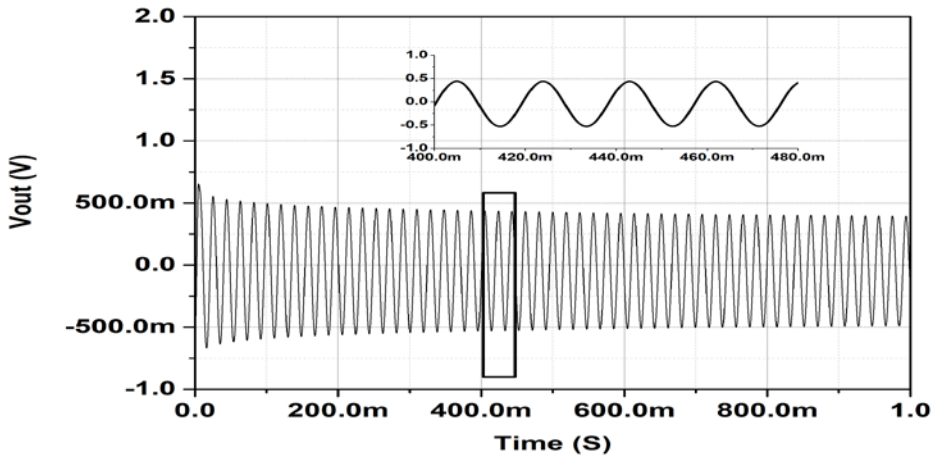


Figure 3.5. Timing waveform of proposed topology I

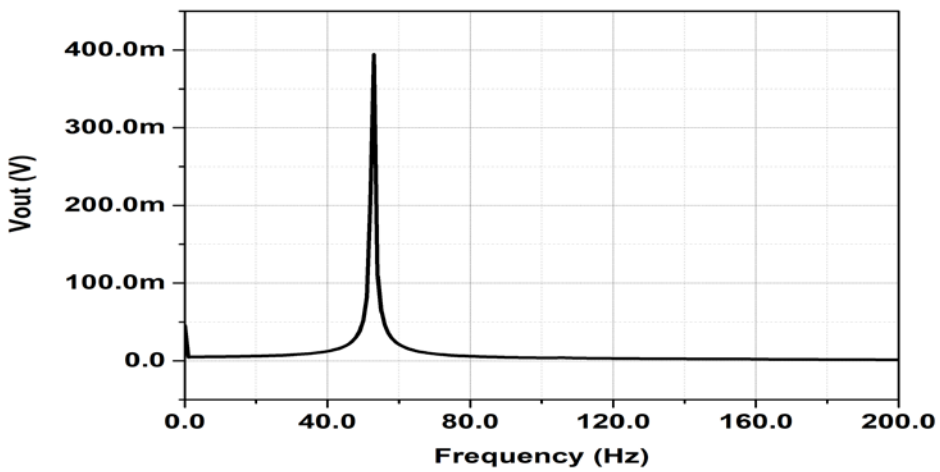


Figure 3.6. Frequency spectrum of proposed SO topology-I

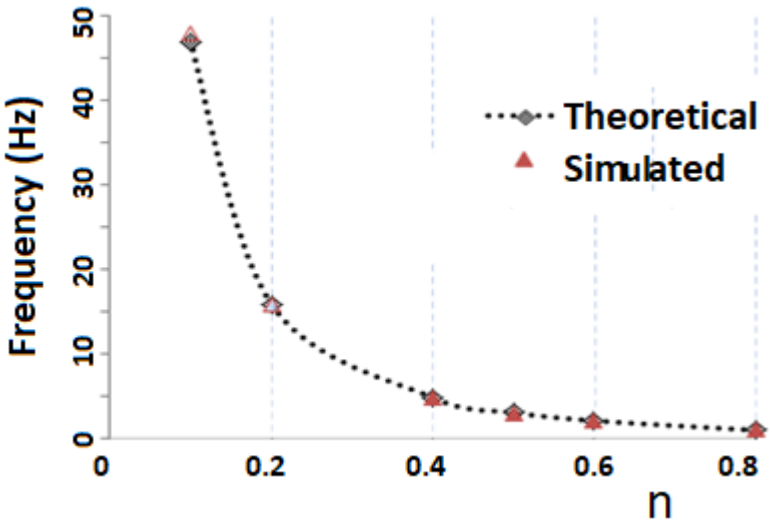


Figure 3.7. Variation of frequency with respect to n

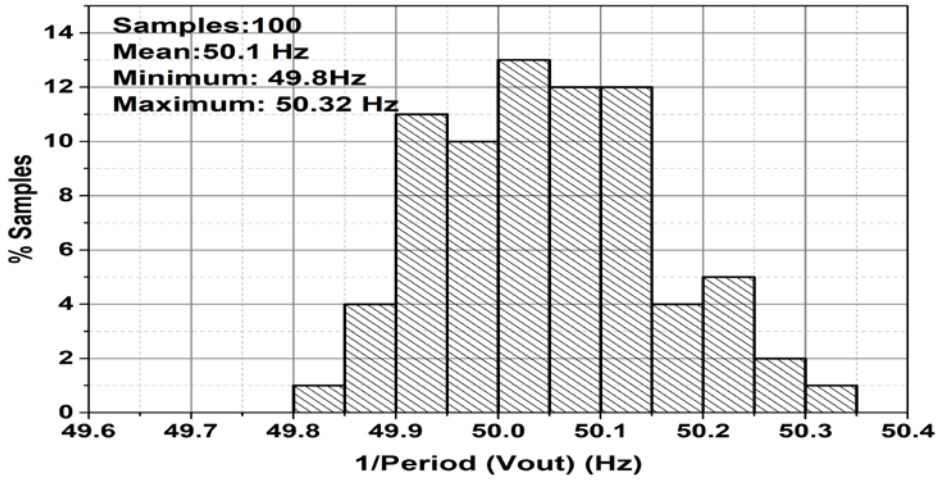
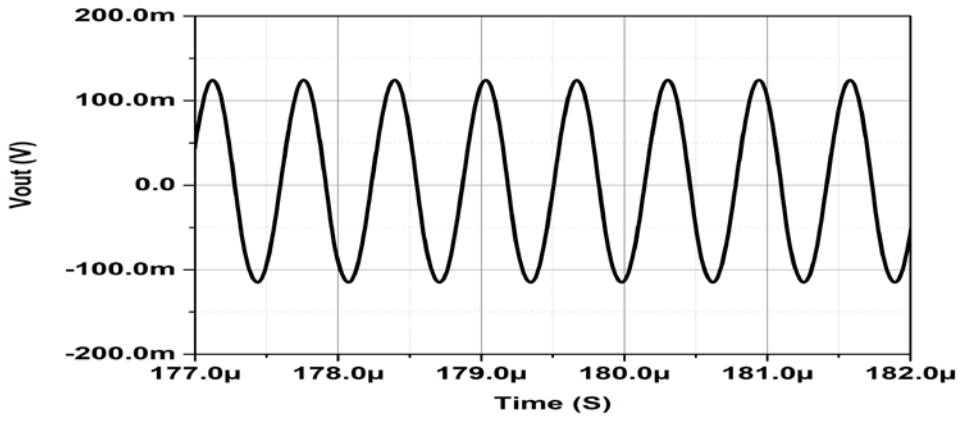
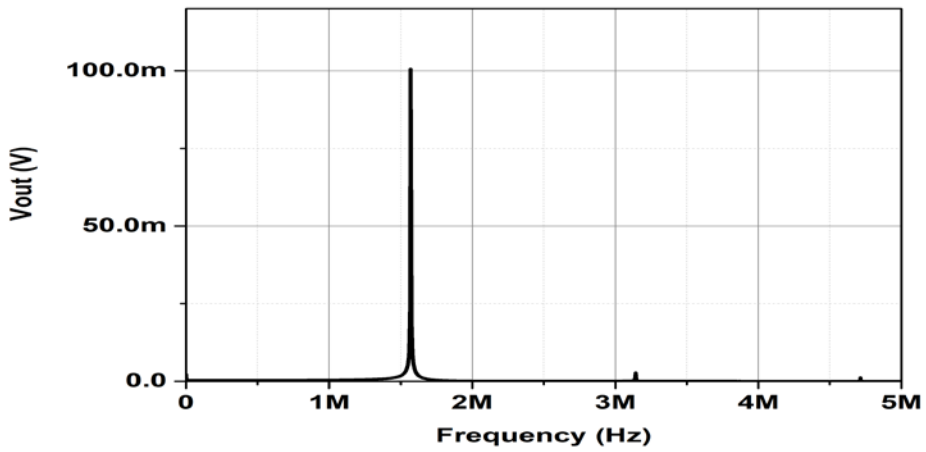


Figure 3.8. Histogram of Proposed SO-I after Monte Carlo simulation

The robustness of the proposed circuit is examined through Monte Carlo simulations by considering hundred samples with 5% variations in all passive components. Figure 3.8 shows the histogram in which the value of FO remains close to its theoretical value of 45 Hz. The proposed topology in Figure 3.1 also provides oscillations at higher frequencies. To illustrate this point, the oscillator was designed for a FO of 1.59 MHz by selecting component values as R= 1 kΩ, R_1= 2 kΩ, C_1= 100 pF, C_2= 50 pF. The simulated timing waveform and its frequency spectrum are plotted in Figure 3.9 (a) and (b), respectively. The THD is observed as 0.47% at FO of 1.59 MHz.



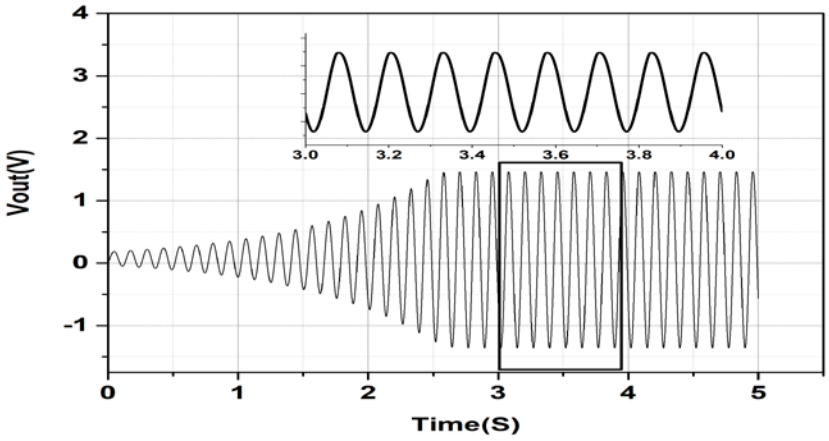
(a)



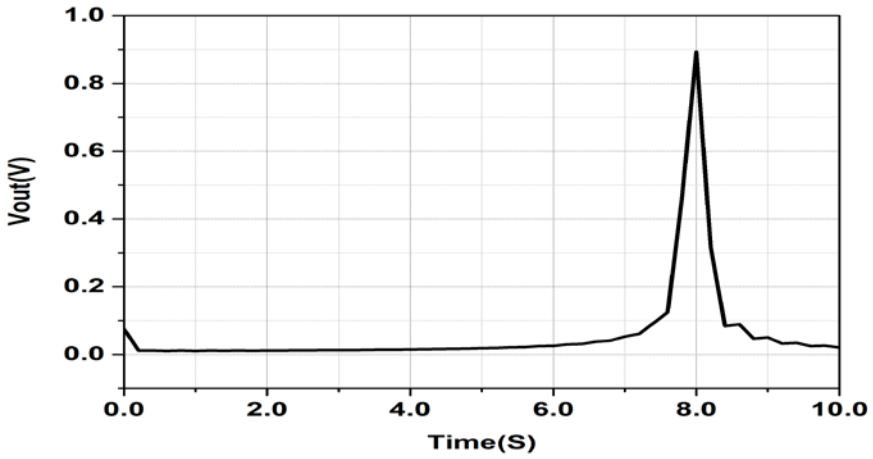
(b)

Figure 3.9. (a) Timing waveform and (b) frequency spectrum of proposed SO topology I

Simulations are performed for oscillator topology in Figure 3.2 at FO of 7.96 Hz by selecting R= 50 kΩ, R_1= R_2= 100 kΩ, C_1= 100 nF, C_2= 400 nF. The simulated transient response and its corresponding frequency spectrum are shown in Figure 3.10 (a) and (b), respectively. The robustness of the proposed SO topology II is examined through Monte Carlo simulations by considering hundred samples with 5% variations in all passive components.



(a)



(b)

Figure 3.10. (a) Transient waveform and (b) frequency spectrum of proposed SO-II

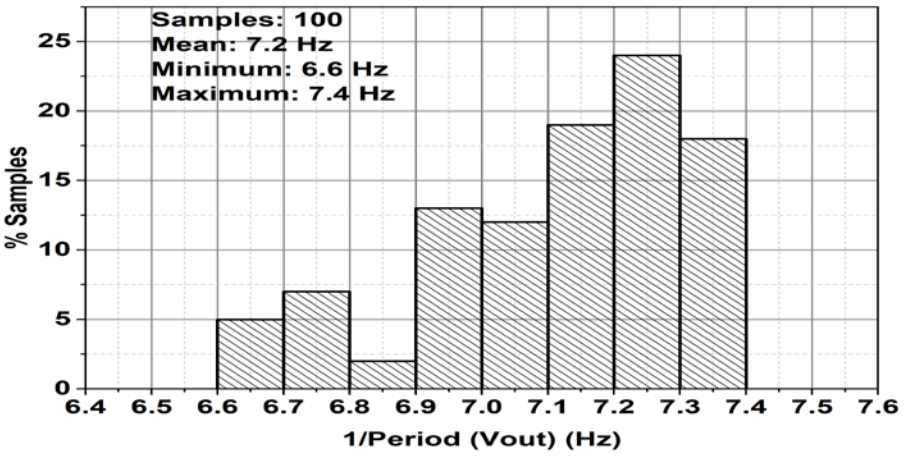
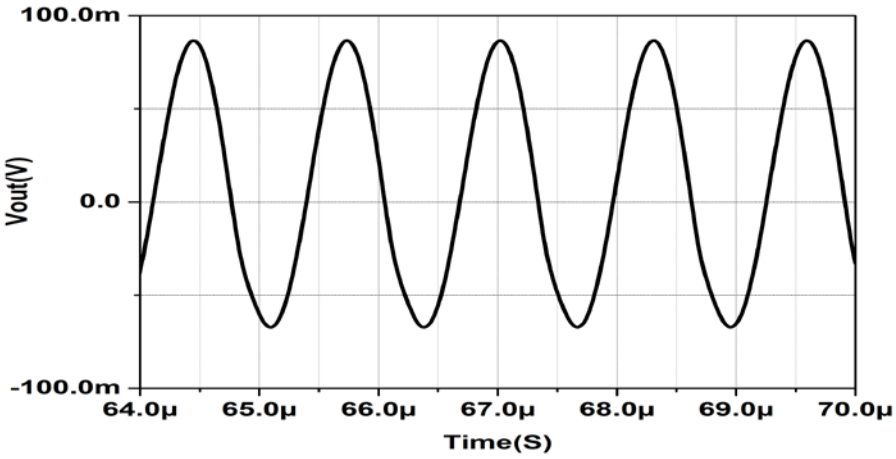
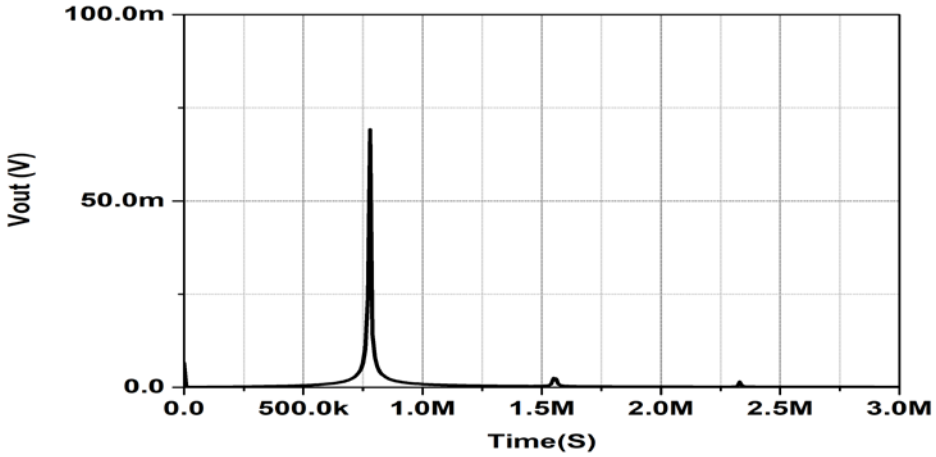


Figure 3.11. Histogram of proposed SO-II after Monte Carlo simulation

Figure 3.11 shows the histogram in which the value of FO remains close to its standard value of 7.9 Hz. By adjusting the multiplication factor *K* in (3.5), the proposed structure can provide higher frequency oscillations. To verify this fact, the oscillator was tested at 796 KHz by choosing component values as R= 0.5 kΩ, R_1= R_2= 1 kΩ, C_1= 100 pF, C_2= 400 pF.



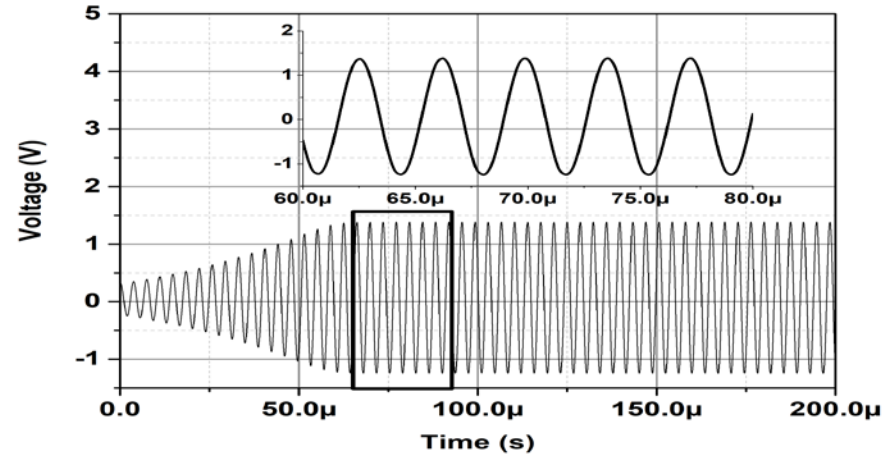
(a)



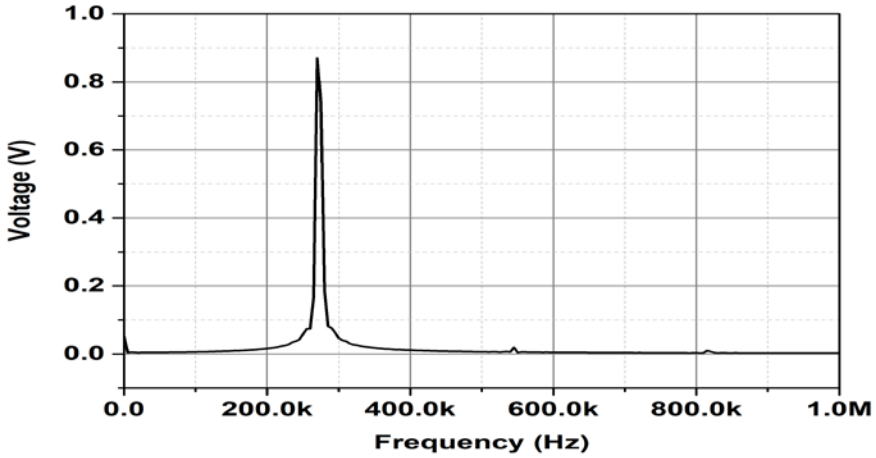
(b)

Figure 3.12. (a) Transient waveform and (b) frequency spectrum of proposed SO-II

The simulated transient response and corresponding frequency spectrum are plotted in Figure 3.12 (a) and (b), respectively. The THD is observed as 2.14% for 7.96 Hz oscillation and 0.6% at 796 KHz.



(a)



(b)

Figure 3.13. (a) Transient waveform and (b) frequency spectrum of proposed SO-III

For simulation of circuit of Figure 3.3, the component values are chosen as R_1= 5.4 kΩ, R_2= 1.8 kΩ, R_3= 7.2 kΩ, R_4= 1.44 kΩ and capacitor values are taken as 300 pF. The simulated transient response and corresponding frequency spectrum are shown in Figure 3.13 (a) and (b), respectively. The simulated FO is obtained to be 273 KHz and THD is observed to be 3.27%.

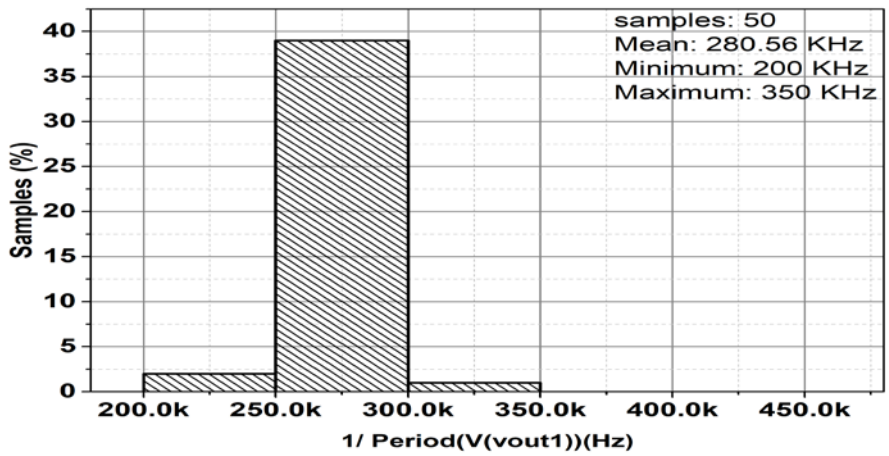
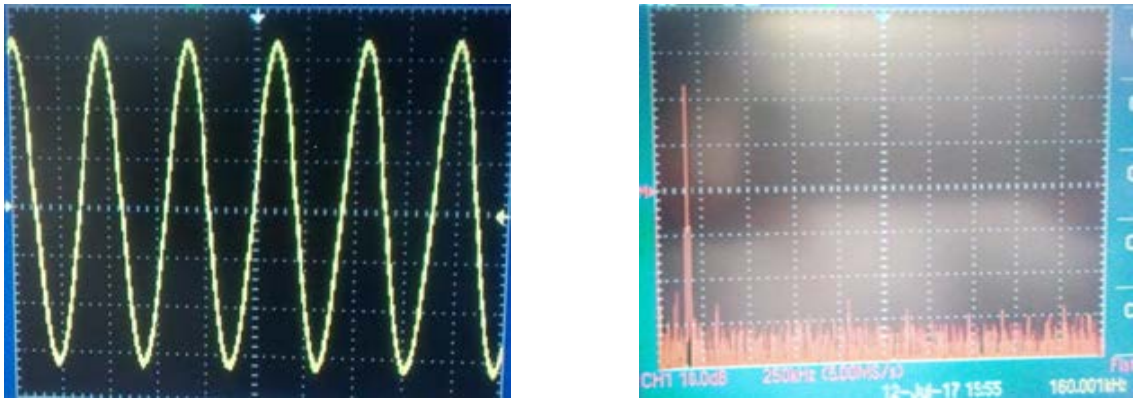


Figure 3.14. Histogram of Proposed SO-III after Monte Carlo simulation.

The robustness of the proposed SO topology III is examined through Monte Carlo simulations by considering fifty samples with 5% variations in all passive components. Figure 3.14 shows the histogram in which the value of FO remains close to its standard value of 273 KHz.

3.2.8 Experimental Results

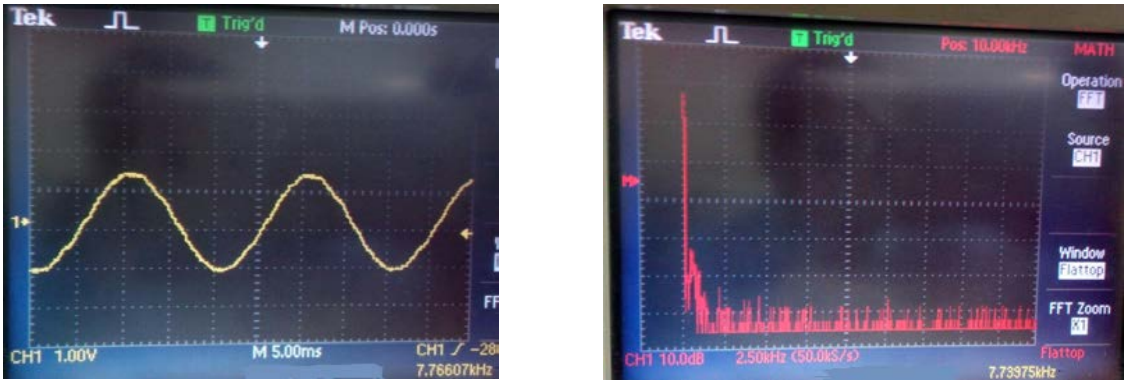
The proposed SOs are also verified experimentally by breadboarding AD844IC based implementation of OTRA [181] and supply voltages of ± 8V are used.



(a) (b)

Figure 3.15. Experimental results of Figure 3.1

(a) steady-state output and it's (b) frequency spectrum

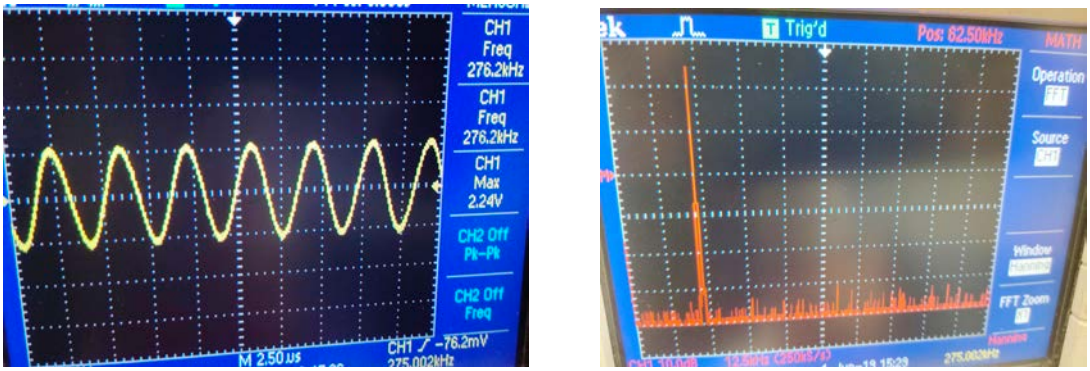


(a) (b)

Figure 3.16. Measured outputs of SO-II

(a) steady-state output and it's (b) frequency spectrum

The resistor and capacitor values taken are R_1= 10.1 kΩ, R= 10 kΩ, C_1= 10 pF, C_2= 10.1 pF. Figures 3.15 (a) and (b) show the observed oscillations and FFT spectrums at 160 KHz for topology in Figure 3.1. Figure 3.2 is designed at 7 KHz (R_1= 10 kΩ, R_2= 1.2 kΩ, R= 11 kΩ; C_2= 100 pF, C_1= 436 pF) and the corresponding steady-state response and FFT spectrum are depicted in Figure 3.16 (a) and (b), respectively.



(a) (b)

Figure 3.17. Measured outputs of SO-III

(a) steady-state output and it's (b) frequency spectrum

Figure 3.3 is modeled at 275 KHz (R_1= 5.4 kΩ, R_2= 1.8 kΩ, R_3= 7.2 kΩ, R_4= 1.44 kΩ). Its steady-state response and corresponding frequency spectrum are depicted in Figure 3.17 (a) and (b), respectively.

3.3 Proposed TOSO Configuration

The literature review, as presented in chapter 1, suggested that only a single topology [160] of TOSO using single OTRA is available. It is worth noting that in the TOSO of [160], the capacitive component spread in the oscillation condition is large, which is not favorable for IC implementation.

The proposed TOSO is shown in Figure 3.18. It uses a single OTRA and six passive components. The CE is obtained by performing routine analysis, assuming ideal OTRA and is given by

$$\begin{cases} s^3 C_1 C_2 C_3 R_1 R_2 R_3 + s^2 \begin{bmatrix} C_1 C_2 R_1 R_2 + C_2 C_3 R_1 R_3 + \\ C_2 C_3 R_2 R_3 - C_1 C_3 R_1 R_2 \end{bmatrix} + \\ s\left[C_2 R_1 + C_2 R_2 + C_3 R_3 - C_3 R_1 - C_3 R_2\right] + 1 = 0 \end{cases} \tag{3.24}$$

Assuming $C_1 = C_2 = C_3 = C$, $R_1 = R_2 = R$ the CE (3.24) reduces to

$$s^3 C^3 R^2 R_3 + 2s^2 C^2 R R_3 + sCR_3 + 1 = 0 \tag{3.25}$$

Therefore FO and CO are given by

$$\text{FO: } f_o = \frac{1}{2\pi RC}$$

$$\text{CO: } 2R_3 = R \tag{3.26}$$

From (3.26), it is clear that FO can be tuned using C without affecting CO. Similarly, CO can be adjusted using R_3. In practice, frequency tuning via capacitor variation is difficult. However, the capacitors may be replaced by a capacitor bank formed by a parallel connection of a capacitor and a series switch. The value of capacitance may be varied by appropriate switch settings.

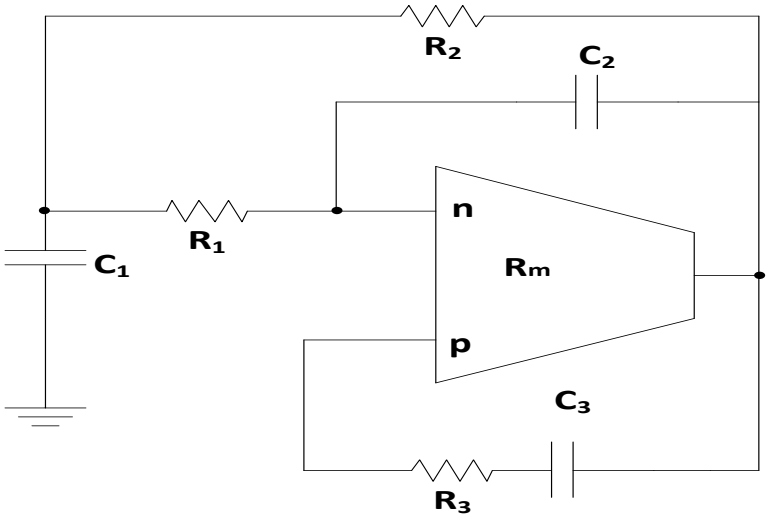


Figure 3.18. Proposed TOSO circuit

3.3.1 MOS resistor based Implementation

A thorough inspection of Figure 3.18 reveals that all the resistors except R_2 can be realized using MOSFETs. The MOS resistor based implementation of proposed TOSO is shown in Figure 3.19.

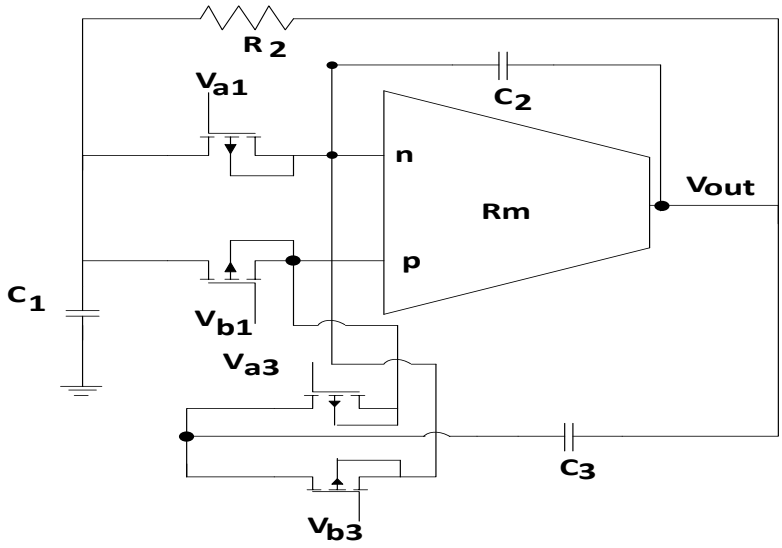


Figure 3.19. MOS resistor implementation of proposed TOSO

3.3.2 Nonideal Analysis

Using a single-pole model for R_m the CE given in (3.24) modifies to

$$s^3C_1C_3R_1R_2R_3(C_2+C_p)+s^2\left[(C_2+C_p)\left(C_3R_3(R_1+R_2)+C_1R_1R_2\right)-C_1C_3R_1R_2\right]+ s\left[(R_1+R_2)(C_2+C_p)-C_3\left(R_1+R_2-R_3\right)\right]+1=0 \quad (3.27)$$

and the FO and CO change to

$$\text{FO: } \overset{\Lambda}{f_o}=\frac{1}{2\pi}\sqrt{\frac{(R_1+R_2)(C_2+C_p)-C_3\left(R_1+R_2-R_3\right)}{C_1C_3R_1R_2R_3(C_2+C_p)}} \quad (3.28)$$

$$\text{CO: } \begin{cases}\left[\dfrac{(R_1+R_2)(C_2+C_p)-C_3\left(R_1+R_2-R_3\right)}{C_1C_3R_1R_2R_3(C_2+C_p)}\right]= \\ \dfrac{1}{(C_2+C_p)\left(C_3R_3(R_1+R_2)+C_1R_1R_2\right)-C_1C_3R_1R_2}\end{cases} \quad (3.29)$$

The effect of C_p can be eliminated by pre-adjusting the value of capacitor C_2, thus achieving self-compensation. By choosing equal capacitance and resistor values except for R_3, the FO and CO are reduced to (3.26).

3.3.3 Sensitivity Analysis

The sensitivity of FO (f_o) for the circuit of Figure 3.18 with respect to R and C are given as

$$\left|S_C^{f_o}\right|=\left|S_R^{f_o}\right|=1;\ \left|S_{R_3}^{f_o}\right|=0 \quad (3.30)$$

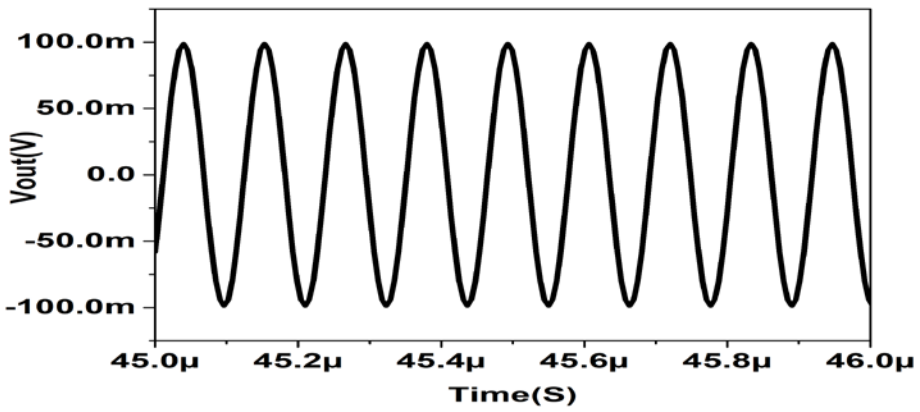
From (3.31), it is observed that all passive sensitivities are less than or equal to unity in magnitude. Therefore, it ensures that the sensitivity performance is satisfactory. Sensitivities of the proposed TOSO structure by considering nonidealities and component setting of $C_1= C_2 = C_3= C$, $R_1= R_2= R$ are given by

$$\begin{cases} \left|S_R^{\hat{f}_o}\right| = \dfrac{RC_p + R_3C}{2RC_p + R_3C}; \left|S_{R_3}^{\hat{f}_o}\right| = \dfrac{2RC_p}{2RC_p + R_3C}; \\ \left|S_C^{\hat{f}_o}\right| = \dfrac{R_3C(C + C_p) - \left(2RC_p + R_3C\right)(3C + 2C_p)}{2\left(2RC_p + R_3C\right)(C + C_p)}; \\ \left|S_{C_p}^{\hat{f}_o}\right| = \dfrac{RC_p(C + C_p) - \left(2RC_p + R_3C\right)C_p}{\left(2RC_p + R_3C\right)(C + C_p)} \end{cases} \tag{3.31}$$

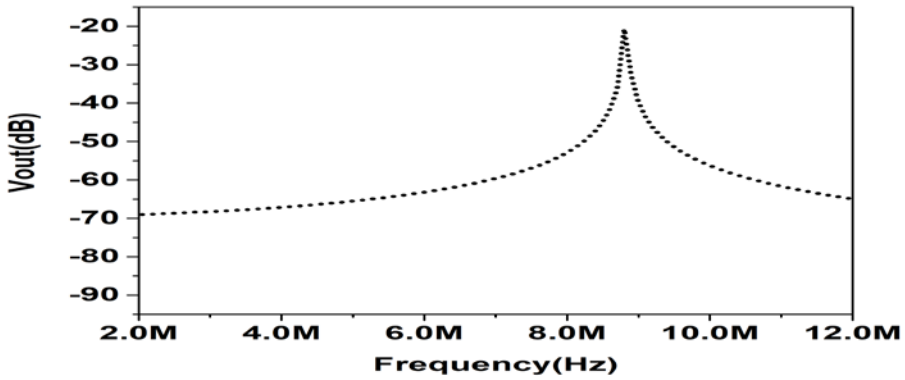
It is found that with $C_p \rightarrow 0$ the above passive sensitivities reduce to as given in (3.31)

3.3.4 Simulation and Layout Results

The proposed TOSO circuit is verified through simulations using the Cadence Virtuoso ADE spectre tool at 0.18µm CMOS technology node. The simulated FO for the component values $C_1 = C_2 = C_3 = C = 1.8$ pF and $R_1 = R_2 = 10$ kΩ, $R_3 = 5$ kΩ was observed to be 8.82 MHz against the calculated value of 8.84 MHz. The corresponding transient output and the FFT spectrum are shown in Figure 3.20 (a) and (b), respectively. It may be noted that the simulated and theoretical values of FO are in close agreement.



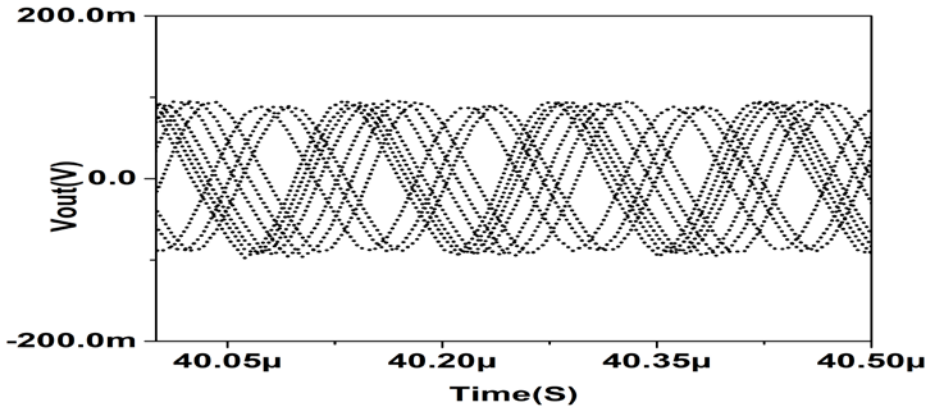
(a)



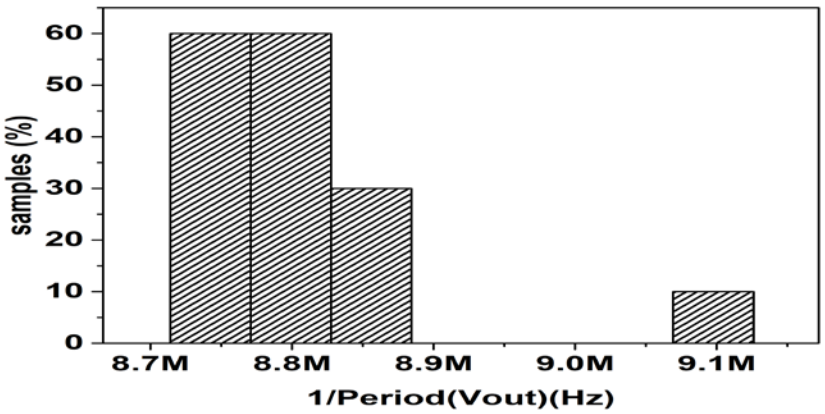
(b)

Figure 3.20. (a) Transient Output and (b) frequency spectrum of proposed TOSO

The robustness of the proposed TOSO is examined through Monte Carlo simulations by considering ten samples with 3% variations in R_3 and the results are shown in Figure 3.21. Figures 3.21 (a) and (b) shows that circuit performance is well acceptable with 3% variation of R_3. Further, the histogram of frequency is depicted in Figure 3.21 (b) which indicates that FO remains close to the theoretical value of 8.84 MHz. The FO variation with respect to R and C are shown in Figure 3.22 (a) and (b), respectively. In Figure 3.22 (a) capacitor value is fixed at 100 pF and R is varied from 0.5 kΩ to 25 kΩ.



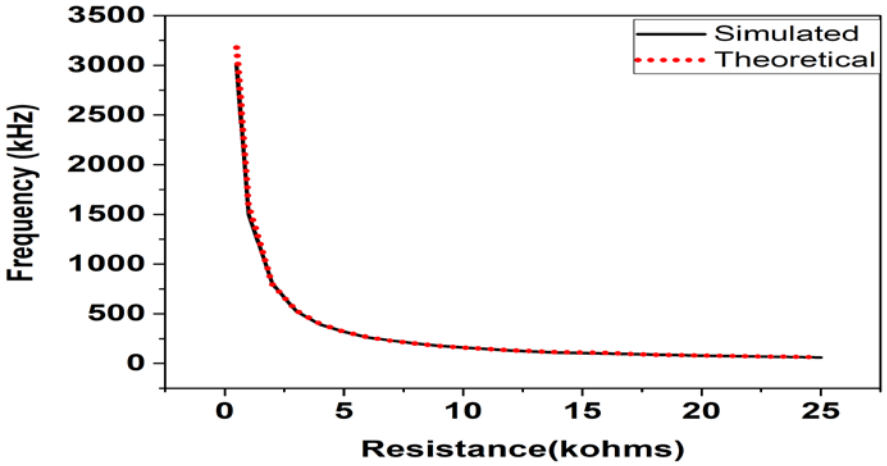
(a)



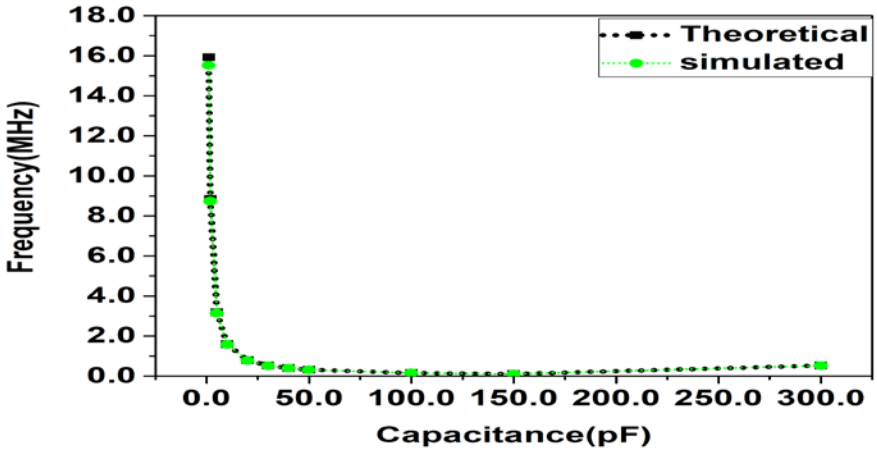
(b)

Figure 3.21. Monte Carlo simulation (a) Transient output (b) Histogram of FO

For Figure 3.22 (b), resister value is set at 10 kΩ and the capacitor is varied from 1 pF to 10 nF. The highest frequency measured is 15.92 MHz and the lowest frequency is 1.59 KHz.



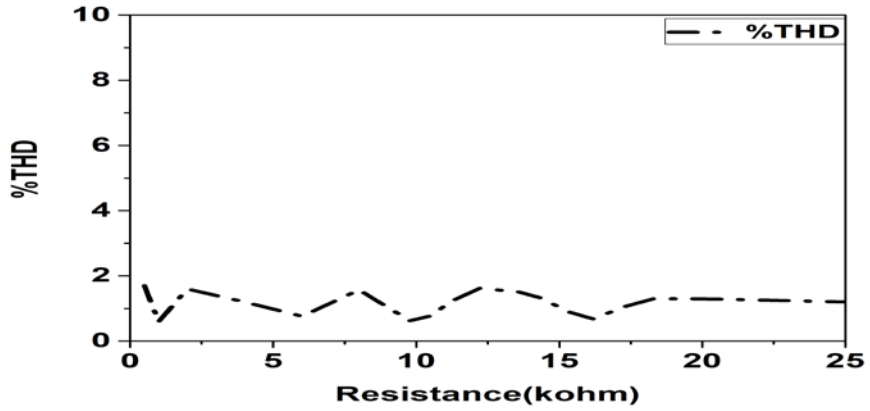
(a)



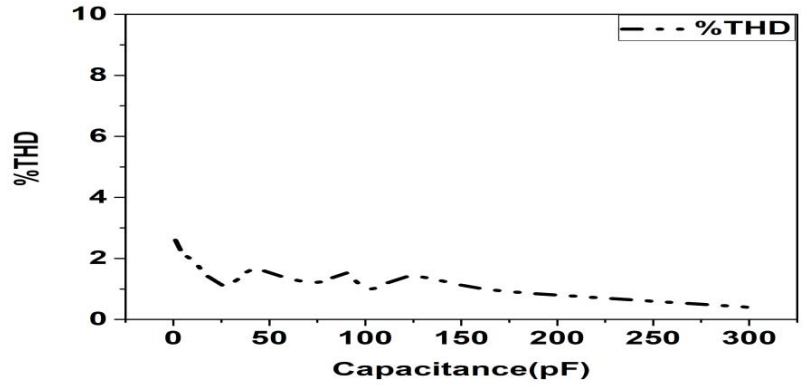
(b)

Figure 3.22. (a) Frequency Tuning with (a) Resistance (b) with Capacitance for proposed TOSO

The THD variation with respect to R and C are shown in Figure 3.23 (a) and (b) respectively. It is observed that simulated THD does not exceed 2.6%. The proposed TOSO is also laid out and verified through post-layout simulations. The typical values of the passive components are considered as R_1= R_2= 10 kΩ, R_3= 5 kΩ and C_1= C_2= C_3= C= 1.8 pF. The resultant theoretical FO is found to be 8.84 MHz. The complete layout of the proposed TOSO is shown in Figure 3.24.



(a)



(b)

Figure 3.23.* The *% THD variation with (a) Resistance (b) Capacitance

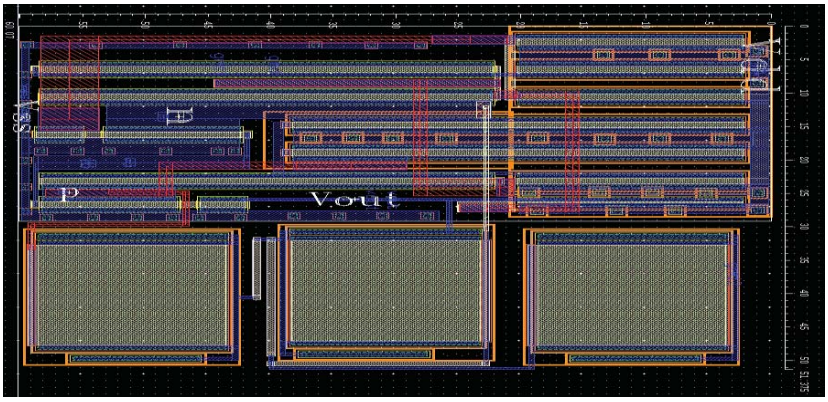
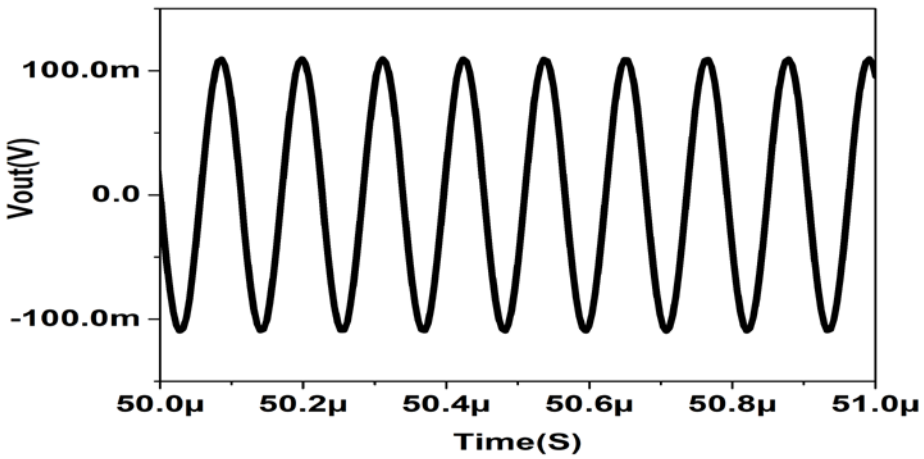
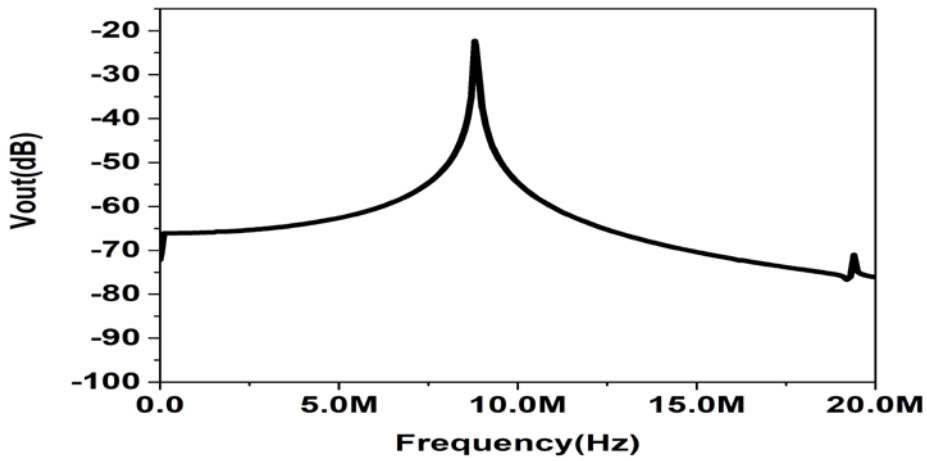


Figure 3.24. The complete physical layout of proposed TOSO

The physical verification checks such as DRC, LVS, RC parasitic extraction authenticate the layout implemented. The total active die area occupied by the oscillator is 3085.7959 μm^2 (51.37µm x 60.07µm). The post-layout simulated waveform and frequency spectrum are shown in Figure 3.25 (a) and (b), respectively. The simulated FO is obtained as 8.79 MHz, which accords well with the theoretical value.



(a)



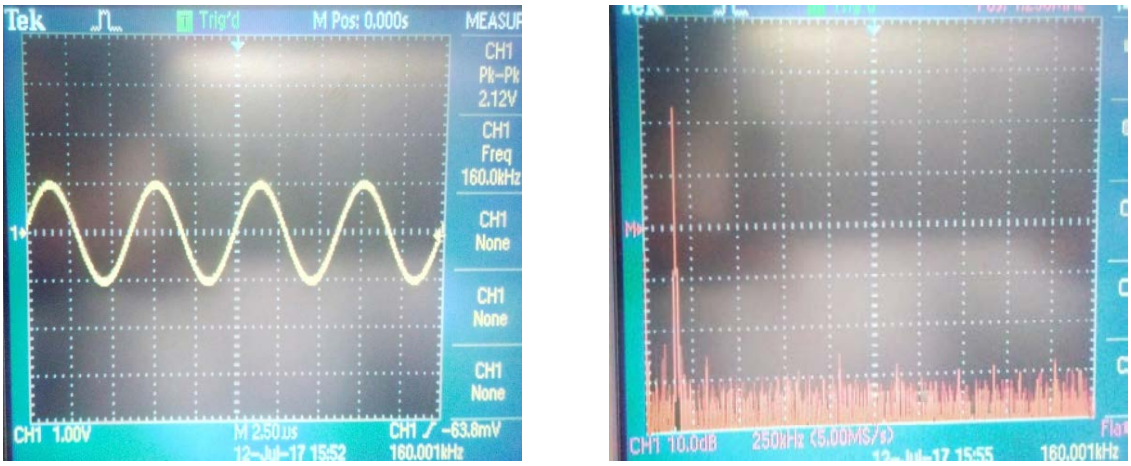
(b)

Figure 3.25. (a) Simulated Output waveform and (b) frequency spectrum of proposed TOSO

3.3.5 Experimental Results

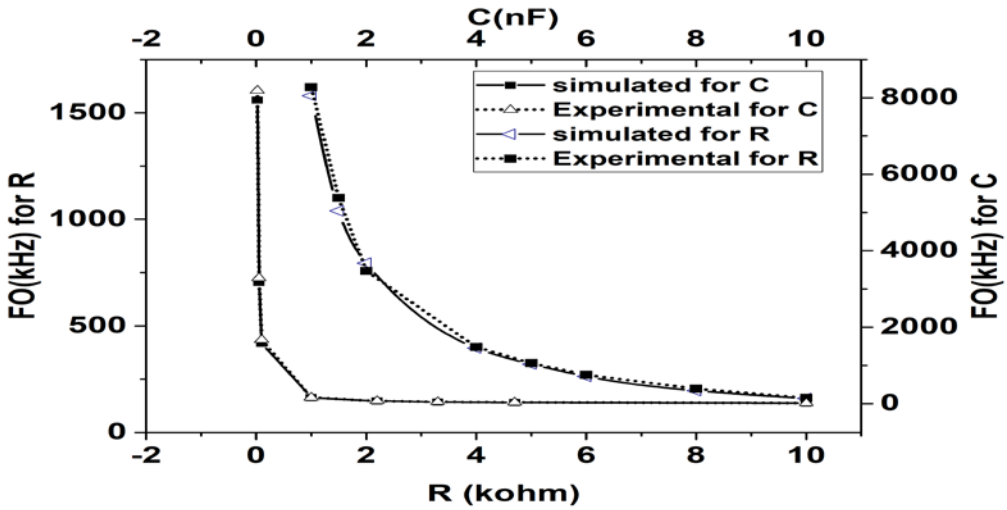
The proposed TOSO is modeled with resistor values R_1= R_2= 10 kΩ, R_3= 5 kΩ and capacitor values C_1= C_2= C_3= C= 100 pF for which the calculated FO is 159.2 KHz. The experimental steady-state response, FFT spectrums are shown in Figure 3.26 (a) and (b), respectively and the practical FO is found to be 160 KHz.

The proposed TOSO has also been simulated in SPICE in which OTRA has been realized using IC AD 844. Figures 3.27 (a) and (b) show the simulated and experimental results for FO and THD variation of FO by varying R from 1 kΩ to 10 kΩ while keeping C= 100 pF and by changing C from 20 pF to 10 nF with R fixed at R= 1 kΩ respectively. The FOs obtained through simulation and experiment are in close agreement. It is observed that the highest experimental THD obtained is 3%, which is considered to be low.

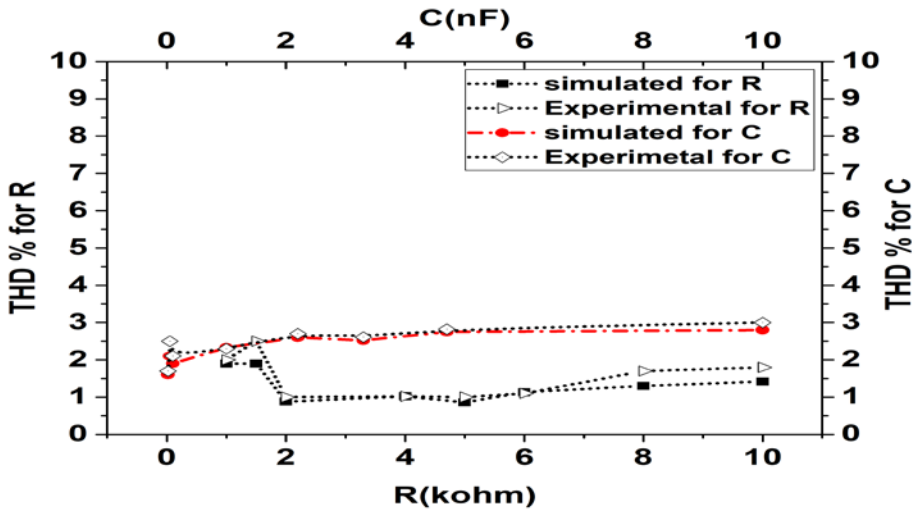


(a) (b)

Figure 3.26. Experimental (a) steady-state output and it's (b) frequency spectrum



(a)



(b)

Figure 3.27. (a) Frequency Tuning with R and C (b) %THD variation with R and C

3.4 Conclusion

New realizations of single OTRA based oscillators are presented in this chapter. The functionality of proposed structures is verified through PSPICE/Cadence Virtuoso ADE spectre tool using 0.18 µm technology parameters. Moreover, the layout of the proposed TOSO structure is also presented. The simulation and experimental results are found to be in close agreement with theoretical propositions.

The proposed circuits are analyzed considering nonidealities of OTRA and it is observed that the effect of nonidealities can be mitigated using self-compensation. The sensitivity of oscillation frequency with respect to passive components is also examined and values found out to be less than or equal to unity in magnitude. All topologies are further tested experimentally wherein the OTRA is realized using off the shelf CFOA IC AD844. Experimental results corroborate the theoretical propositions.

CHAPTER 4
QUADRATURE OSCILLATOR REALIZATIONS

The content and results of the following papers have been reported in this chapter

1. K. Gurumurthy, N. Pandey and R. Pandey, “New realization of quadrature oscillator using OTRA,” *Int J Electr Comput Eng (IJECE)*, vol. 7, no. 4, pp. 1815-1823, 2017. **(SCOPUS)**
2. Realization of Third order Inverse filters and its Applications **(Communicated** Proceedings of the National Academy of Sciences, India, Springer**)**
3. K. Gurumurthy, R. Pandey and N. Pandey, “New Electronically tunable Low-frequency Quadrature Oscillator using Operational Transresistance Amplifier,” *IETE Journal of Research*, Taylor and Fransis**.(SCIE) (IF:0.829)** (Accepted)

4.1 Introduction

Sinusoidal oscillators providing two outputs with 90^o phase difference are termed as quadrature oscillators (QOs). The QOs find wide applications in the field of communication, power electronics and instrumentation such as in single-sideband modulators, quadrature mixers, vector generators or selective voltmeters, etc. [166], [178]. Therefore, there is a consistent research effort towards QO designs.

The design of single-phase oscillators was discussed in chapter 3. This chapter is devoted to the realization of QOs and three new topologies are proposed. The first topology is a second order QO, which also qualifies for low frequency operations, whereas the other two are third order QOs.

4.2 Proposed Second Order QO Topology

From the literature review, it is observed that only a few second order OTRA based QOs [166]-[167], [174]-[178] are available. A detailed study of these topologies divulges that these structures have the FO of form $1/2\pi RC$ and are thus suitable for generating oscillations ranging from medium to high frequencies. These topologies need a large RC component spread in attaining lower frequencies, which is not desirable for functional accuracy, performance and IC chip area viewpoint. Further, among these topologies, no SO qualifies for generating low frequency quadrature sinusoid waveforms. Therefore, in this work, a second order QO capable of producing low frequency signals is presented. The proposed second order low frequency QO (LFQO) structure is depicted in Figure 4.1. It consists of a forward path having all-pass type of transmission characteristics followed by a feedback path comprising of an inverting differentiator. Using the terminal characteristics of OTRA and performing routine analysis, the CE of the proposed circuit is computed as

$$s^2 C_1 C_3 R_1 R_4 + s\{C_2 R_1 - C_3 R_4\} + \frac{R_1}{R_2} - \frac{R_1}{R_3} = 0 \tag{4.1}$$

The FO and CO may be computed as

$$\text{FO: } f_o = \frac{\sqrt{1-k}}{2\pi\sqrt{C_1 C_3 R_2 R_4}}; \text{ where } k = \frac{R_2}{R_3} \tag{4.2}$$

$$\text{CO: } C_2 R_1 = C_3 R_4 \tag{4.3}$$

The straightforward analysis gives the relationship between $Vout_1$ and $Vout_2$ as

$$\frac{Vout_2}{Vout_1} = -sC_3 R_4 = \omega_o C_3 R_4 e^{-j90^o} \tag{4.4}$$

It implies that $Vout_2$ lags $Vout_1$ by a phase of 90^o, which verifies the relationship between these outputs.

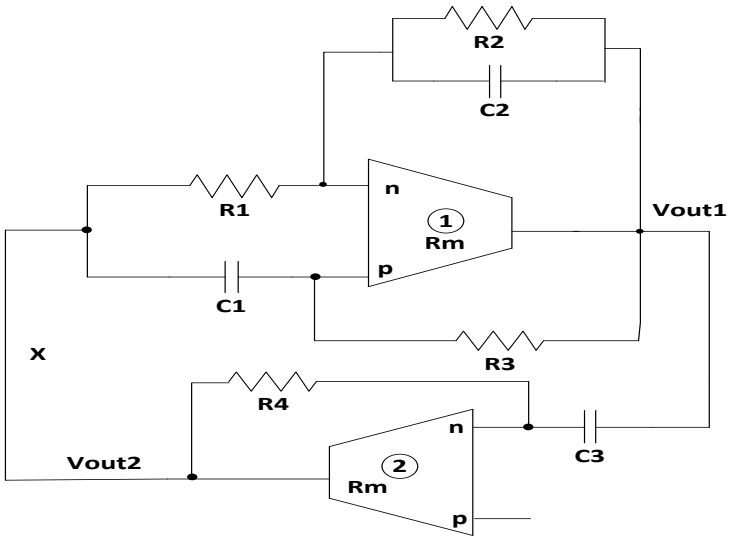


Figure 4.1. Proposed second order LFQO

Inspection of (4.2) and (4.3) indicates that FO can be adjusted using R_2 or R_3 without affecting and similarly, the CO can be adjusted through R_1 without altering FO. Further,

by selecting R_2 slightly less than R_3 lower values of f_o (LF oscillations) are attainable with low component spread.

4.2.1 MOS-C Realization

As all the resistors in proposed topologies are connected between input and output terminals, therefore a complete MOS-C realization is possible. Implementing resistors through MOSFETs gives the topology of Figure 4.2. The CO and FO of Figure 4.2 can be tuned electronically as resistor values may be varied by changing gate control voltages V_{ai}, V_{bi} for i = 1to 4.

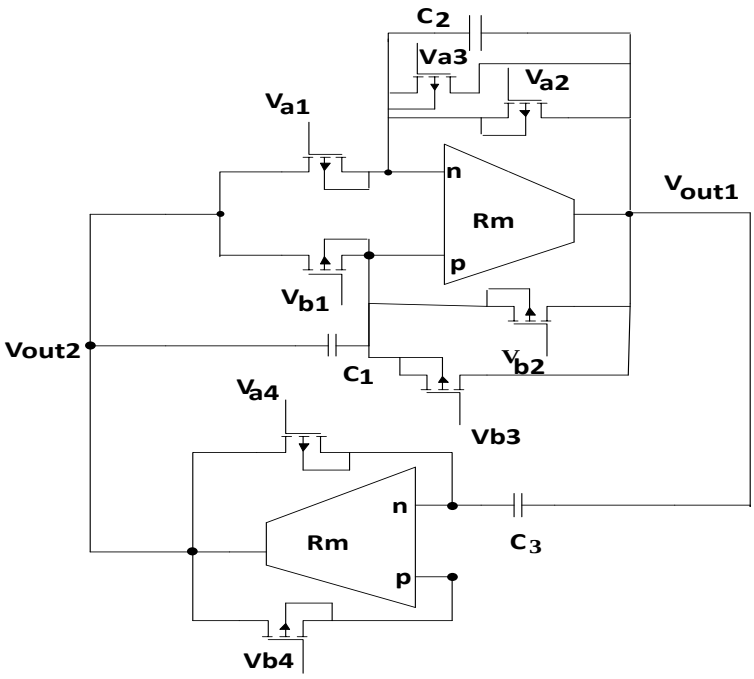


Figure 4.2. Complete MOS-C implementation of proposed second order LFQO

4.2.2 Nonideal Analysis

Taking the nonidealities into account, the CE of (4.1) modifies to

$$s^2 C_1(C_3+C_p)R_1R_4 + s\left\{C_2R_1-(C_3+C_p)R_4\right\} + \frac{R_1}{R_2} - \frac{R_1}{R_3} = 0 \qquad (4.5)$$

the modified CO and FO are given by (4.6) and (4.7) respectively

$$\hat{f_o} = \frac{\sqrt{1-k}}{2\pi\sqrt{C_1(C_3+C_p)kR_2R_4}} \text{ where } k = \frac{R_2}{R_3} \tag{4.6}$$

$$\text{CO}: (C_2+C_p)R_1 = (C_3+C_p)R_4 \tag{4.7}$$

It may be noted that the effect of C_p can be eliminated by pre-adjusting the value of capacitors C_2 and C_3, thus achieving self-compensation.

4.2.3 Sensitivity Analysis

The sensitivities of f_o with respect to various circuit parameters are

$$\begin{cases} S_{C_2}^{f_o} = 0; S_{C_1}^{f_o} = S_{C_3}^{f_o} = S_{R_4}^{f_o} = -\frac{1}{2}; \\ S_{C_3}^{\hat{f_o}} = -\frac{C_3}{2\left(C_3+C_p\right)}; S_{C_p}^{\hat{f_o}} = -\frac{C_p}{2\left(C_3+C_p\right)}; S_k^{\hat{f_o}} = \frac{k-2}{2(1-k)} \end{cases} \tag{4.8}$$

It may be noted from (4.8), that all the sensitivities for proposed QO are less than or equal to 1/2 except sensitivity with respect to *k*. Therefore, it confirms that the sensitivity performance of the proposed QO is satisfactory.

4.2.4 Frequency Stability

The frequency stability (S^F) is yet another significant performance measure for sinusoidal oscillators [3]. The S^F is defined as

$$S^F = d\varphi(\alpha)/d\alpha\big|_{\alpha=1} \tag{4.9}$$

where $\alpha = \omega/\omega_o$ is the normalized frequency and $\varphi(\alpha)$ characterizes the phase function of the open loop transfer function of the oscillator.

The open loop transfer function *H(s)* of the oscillator circuit is

$$H(s)=\frac{s^2C_1C_3R_1R_2R_3R_4-sC_3R_4R_2R_3}{R_1\left(R_2-R_3\right)-sC_2R_1R_2R_3} \tag{4.10}$$

The frequency stability factor with condition setting as $C_1= C_2= C_3= C$ and $R_1= R_3= R_4= R$, $R_2= R/n$ is given by

$$S^F=-\frac{2\sqrt{n-1}}{n}\approx-\frac{2}{\sqrt{n}} \text{ for n>>1.} \tag{4.11}$$

Inspection of (4.11) suggests that the frequency stability of proposed QO decreases with increasing *n*.

4.2.5 Phase Noise Analysis

The random frequency fluctuations in a phase of a signal can be treated as phase noise. To calculate the phase noise, a procedure discussed in [83], [192] is adopted.

By breaking the feedback loop at X in the proposed oscillator and assuming equal capacitances and resistances except for R_3, the open loop transfer function H(s) is computed as

$$H(s)=\frac{s^2C^2R^3R_3-sCR^2R_3}{R^2-(1+sCR)RR_3} \tag{4.12}$$

The phase noise spectral density is shaped by

$$\frac{Y}{X}\left[j\left(\omega_o+\Delta\omega\right)\right]^2=\frac{1}{\Delta\omega^2\left|dH/d\omega\right|^2} \tag{4.13}$$

where ω_o is the FO and $\omega=\left(\omega_o+\Delta\omega\right)$ is frequency close to the carrier frequency.

The H(s) given by (4.12) can also be expressed in terms of magnitude and phase as

$$H(j\omega)=A(\omega).e^{j\varphi(\omega)} \tag{4.14}$$

Differentiation of (4.14) with respect to ω gives

$$\frac{dH}{d\omega} = \left(\frac{dA}{d\omega} + jA\frac{d\phi}{d\omega}\right)\exp(j\phi) \tag{4.15}$$

Using (4.13), (4.15) can be rewritten as

$$\frac{Y}{X}\left[j(\omega_o + \Delta\omega)\right]^2 = \frac{1}{\Delta\omega^2\left[\left|\frac{dA}{d\omega}\right|^2 + \left|\frac{d\phi}{d\omega}\right|^2\right]} \tag{4.16}$$

For $\omega \approx \omega_o, A \approx 1,$ (4.13) to (4.15) are used to compute phase noise.

Substituting the CO and FO in (4.12) the magnitude A(ω) can be written as

$$\left|A(\omega)\right| = \sqrt{\frac{\left(\frac{\omega}{\omega_o}\right)^4 (R_3 - R) + \left(\frac{\omega}{\omega_o}\right)^2 (R_3 - R)R_3}{\left(\frac{\omega}{\omega_o}\right)^2 (R_3 - R)R_3 + (R_3 - R)^2}} \tag{4.17}$$

Differentiation of (4.17) with respect to ω gives

$$\left|\frac{dA}{d\omega}\right| = \frac{2}{\omega_o}.\frac{(R_3 - R)}{(2R_3 - R)} \tag{4.18}$$

the phase $H(j\omega)$ can be written as

$$\angle H(j\omega) = \varphi = tan^{-1}\left(\left(\frac{\omega}{\omega_o}\right)^{-1}.\sqrt{\frac{R_3}{R_3 - R}}\right) - tan^{-1}\left(\left(\frac{\omega}{\omega_o}\right).\sqrt{\frac{R_3}{R_3 - R}}\right) \tag{4.19}$$

determining $\left|\frac{d\varphi}{d\omega}\right|$ from (4.18) results in

$$\left|\frac{d\varphi}{d\omega}\right| = \frac{2R_3}{(2R_3 - R)}.RC \tag{4.20}$$

The inspection of (4.18) and (4.20) reveals that the frequency stability at lower frequencies can be stated high either by keeping product RC high or choosing R close to $2R_3$.

The notable properties of the proposed oscillator are: 1) independent controllability of FO through resistors without affecting the CO 2) possibility of complete MOS-C implementation, thereby making FO electronically tunable 3) low passive sensitivities 4) good frequency stability properties.

By considering the above-listed benefits, the proposed circuit adds to the present repertoire of OTRA based oscillators and serves to be the first OTRA based LFSO with the capability of delivering quadrature outputs.

4.2.6 Simulation and Layout Results

The functionality of the proposed oscillator is verified through post-layout simulations. The Cadence Virtuoso ADE spectre tool with 0.18µm GPDK CMOS parameters is used for simulations. The layout is implemented by physical verification checks such as DRC and LVS. The layout drawn for component setting R_1= R_2= R_4=10 kΩ, R_3= 10.1 kΩ and C_1= C_2= C_3= 5 pF is shown in Figure 4.3. The total layout die area is about 6876.145µm^2 (120.995µm x 56.83µm). Using RC parasitic extraction, the C_p value is obtained as 5.03 fF.

The transient output for $V_{out1,}$ V_{out2} and corresponding frequency spectrums are obtained through post-layout simulations, shown in Figures 4.4 (a) and (b), respectively. The X-Y plot for V_{out1} versus V_{out2} is depicted in Figure 4.4 (c), which verifies the quadrature relations between these voltage outputs. The simulated FO is observed as 316.32 KHz against the calculated value of 316.89 KHz. The slight variation between simulated and theoretical FO may be attributed to the parasitic capacitance of OTRA.

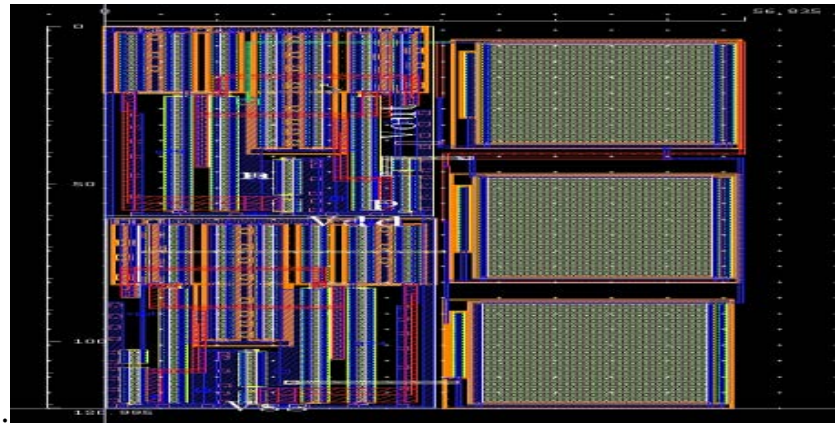
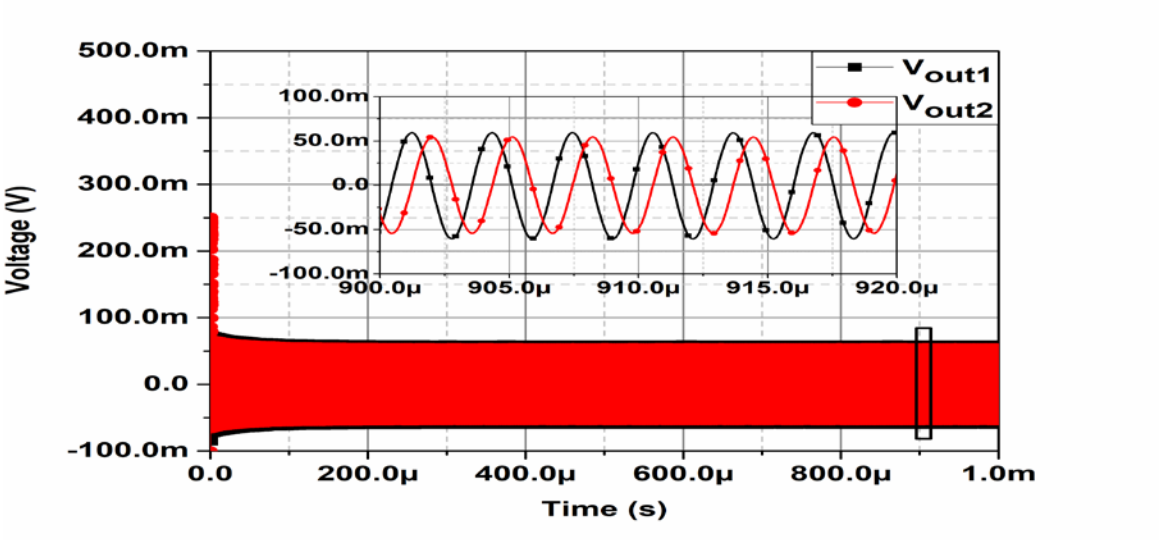
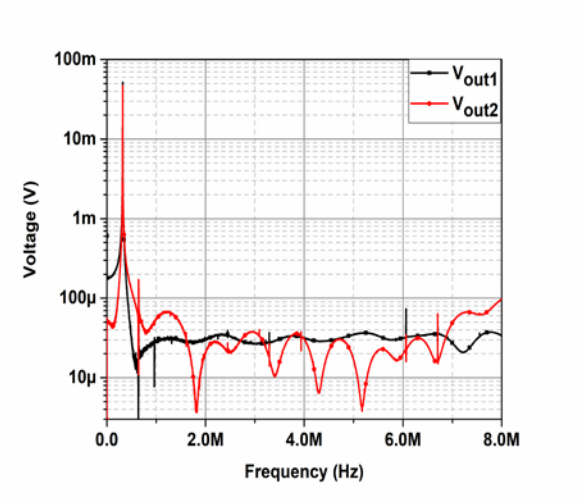


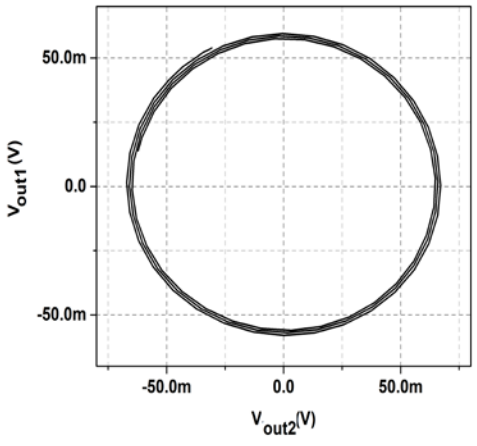
Figure 4.3. The complete physical layout of proposed LFQO



(a)



(b)



(c)

Figure 4.4. Post layout results of proposed LFQO (a) simulated transient Response (b) FFT spectrum (c) Vout1 versus Vout2

The robustness of the proposed circuit is tested through Monte Carlo simulations by considering Gaussian distribution with 5% variations in all the passive components. Figure 4.5 presents the histogram of the Monte Carlo runs and it signifies that the circuit operates well within 2% variation around theoretical FO.

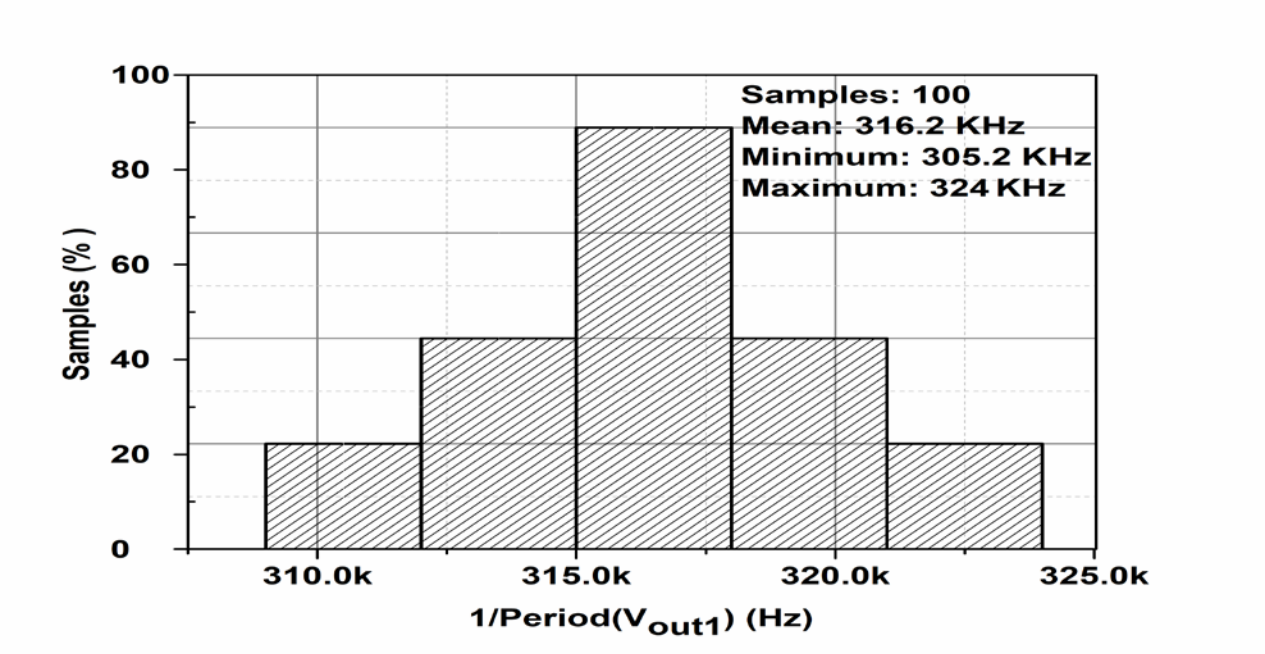


Figure 4.5. Histogram of proposed LFQO

Further, the FO variation with respect to resistance R_3 is shown in Figure 4.6. The other component settings are chosen as R_1= R_2= R_4= 10 kΩ and C_1= C_2= C_3= 10 pF while R_3 is varied from 10.1 kΩ to 20 kΩ. Similarly, the phase error plots between V_{out1} and V_{out2} with respect to R_3 is examined for similar simulation settings and observations are plotted as shown in Figure 4.7. The highest phase error is found to be 3.6^o.

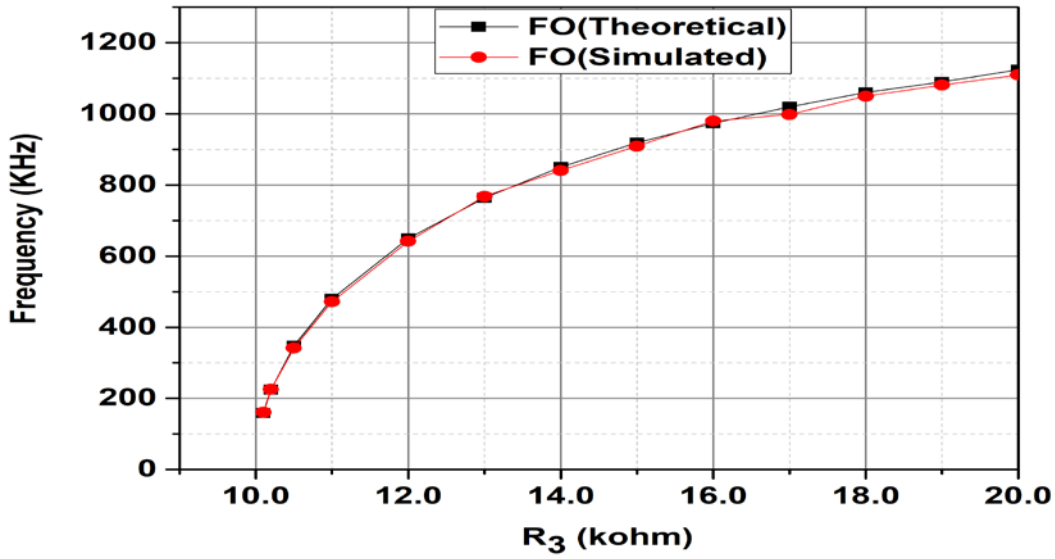


Figure 4.6. Variation of FO with Resistance R3

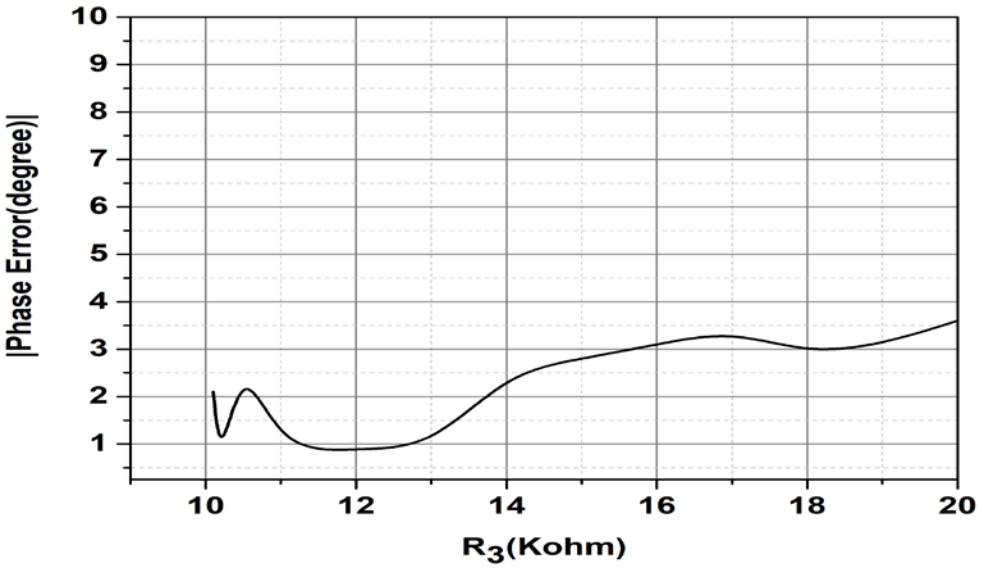


Figure 4.7. Variation of phase error between Vout1 and Vout2 with Resistance R3

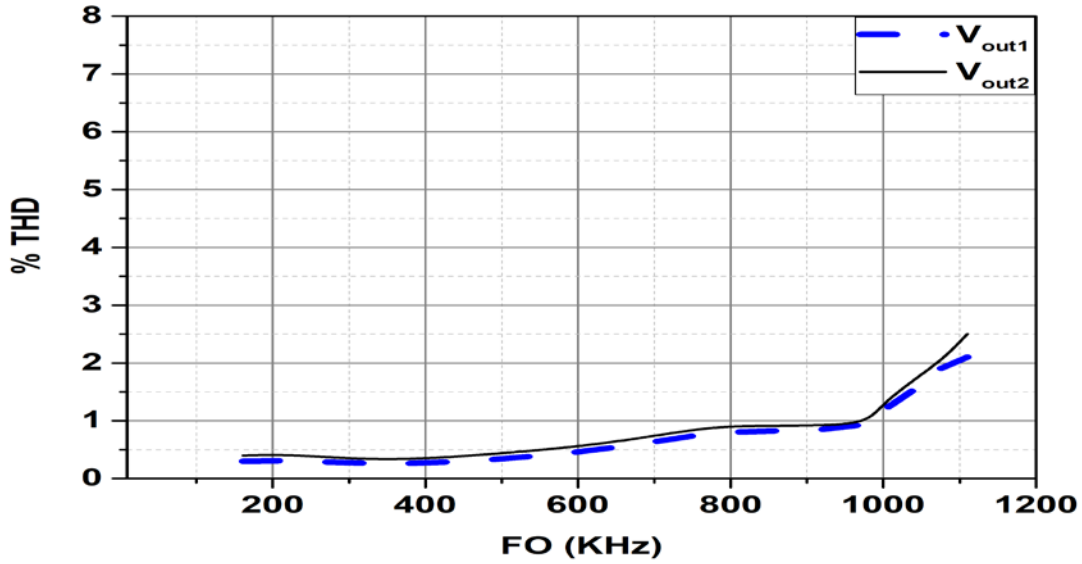


Figure 4.8. Variation of %THD with Resistance R3

Total harmonic distortion is also observed for various frequencies using simulation setting used for studying FO variation with R_3. The findings are plotted in Figure 4.8, which show THD up to 3% till FO of 1 MHz.

Further to demonstrate the electronic tunability of the proposed QO, the drawn channel width (W_{drawn}) and channel length (L_{drawn}) are considered as 1µm and 2.5 µm respectively for all MOSFETs used for resistor realization.

To realize resistors of value 10 kΩ, 10.1 kΩ, the gate controlling voltages V_{ai}, V_{bi} (where i= 1, 2, 3, 4) are adjusted so that (V_{ai} -V_{bi}) is equal to 0.963 V, 0.953 V, respectively. The electronic tuning of FO by MOS based resistor R_3 (by altering gate controlling voltages Va_3 and Vb_3) is shown in Figure 4.9.

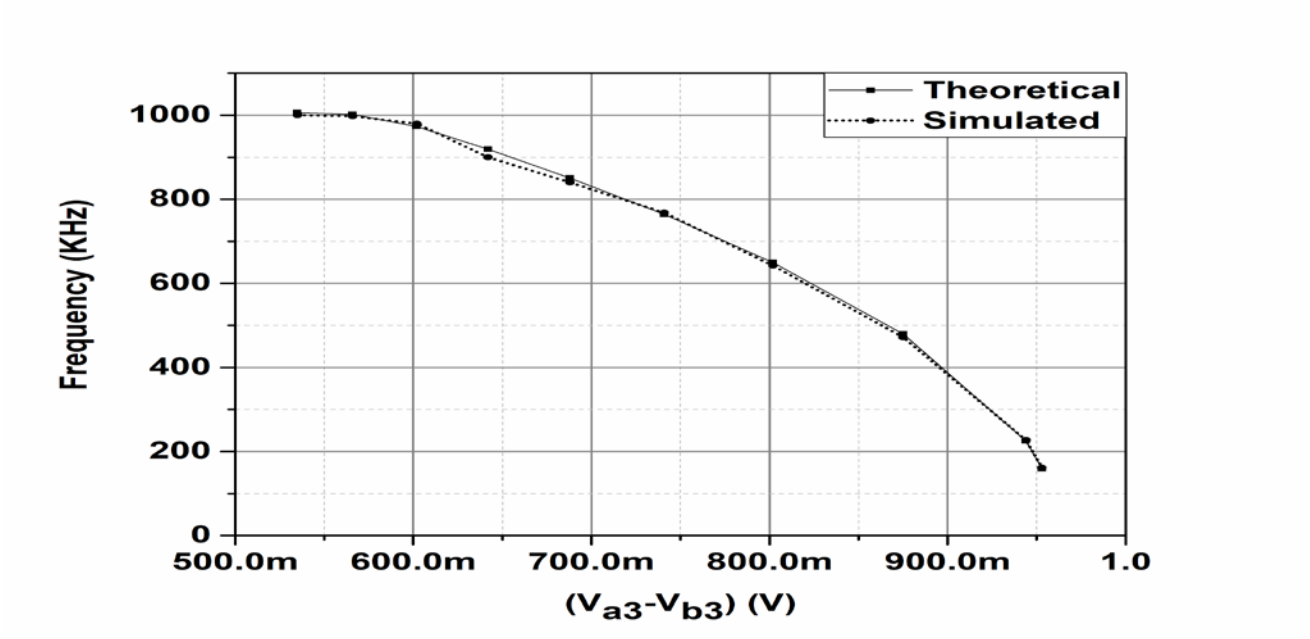
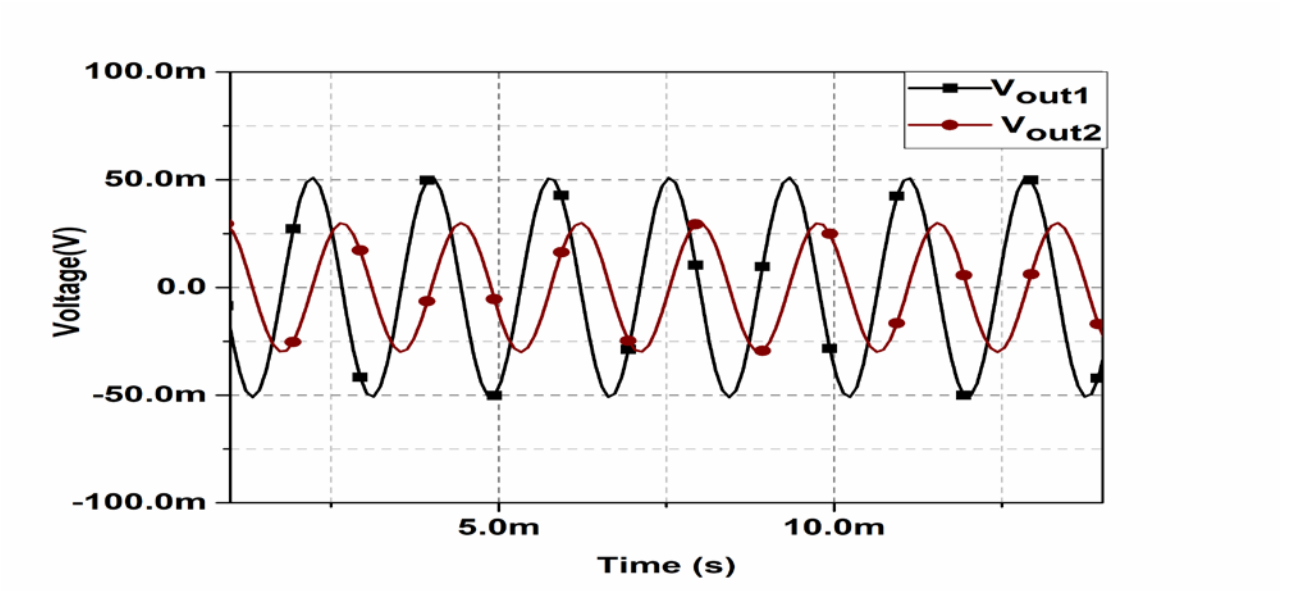
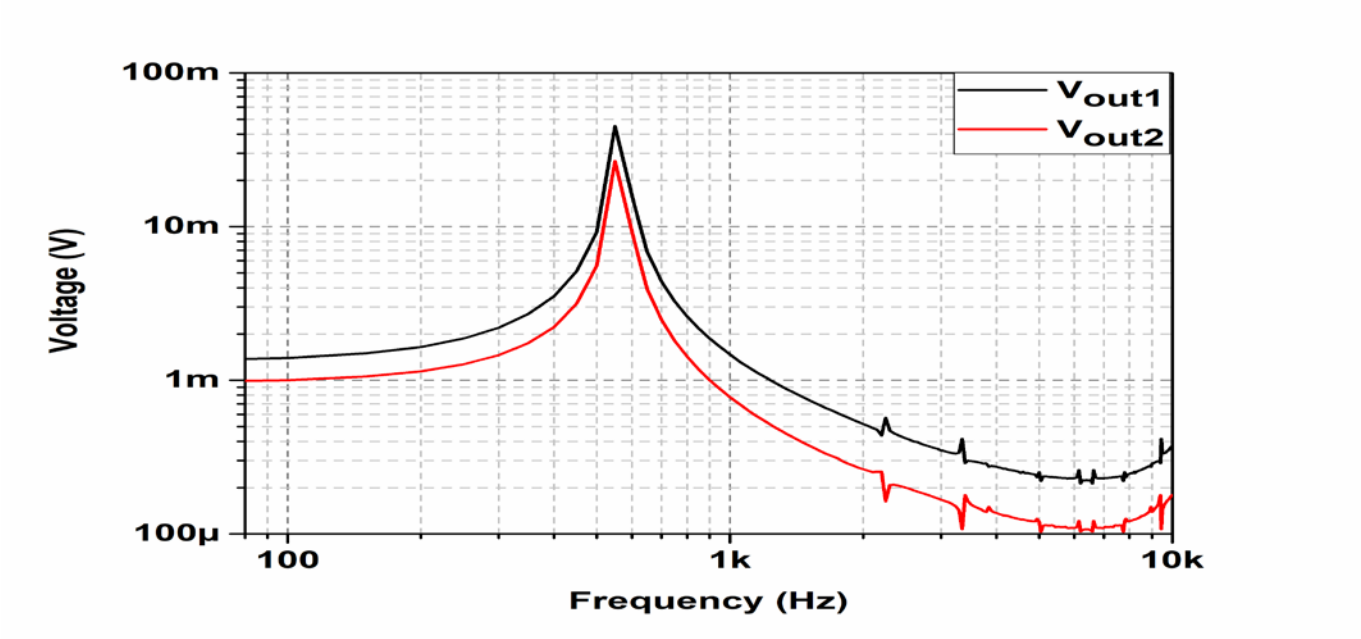


Figure 4.9. Variation of FO with resistance R_3 by changing (Va3 – Vb3)

The proposed QO is also tested for LF operation by setting R_1= R_2= R_4= 20 kΩ, R_3= 20.1 kΩ and by selecting capacitance values as C_1= C_2= C_3= 1 nF. The frequency of the generated waveform is 0.559 KHz as against the theoretical value of 0.561 KHz. The resultant schematic driven transient response and frequency spectrum are shown in Figure 4.10 (a) and (b), respectively. The THD is found to be l.82%.



(a)



(b)

Figure 4.10. Schematic driven simulated results of proposed LFQO-I (Figure 4.1) (a) transient response (b) FFT spectrum

4.3 Realization of Third order QOs

Few TOQO designs are already available [171]–[173], [182]-[183] in the literature. These reported TOQOs are designed using (i) two lossy and one lossless integrators [183], (ii) one lossy and two lossless integrators [183] (iii) a second order low pass filter followed by an integrator [172] (iv) three low pass filters and gained feedback around the loop (v) high pass filter and differentiator [171] (vi) intuitive method [173], [182].

In this section, two OTRA based TOQOs are proposed. The first structure is designed using second order high pass filter and a differentiator in a feedback loop. The other topology is derived from the inverse filter configuration.

4.3.1 Proposed TOQO Topology-I

The proposed TOQO topology-I is shown in Figure 4.11. It uses an OTRA based second order high pass filter [171] (C_1= C_3) and an inverting differentiator in the feedback forming a closed loop

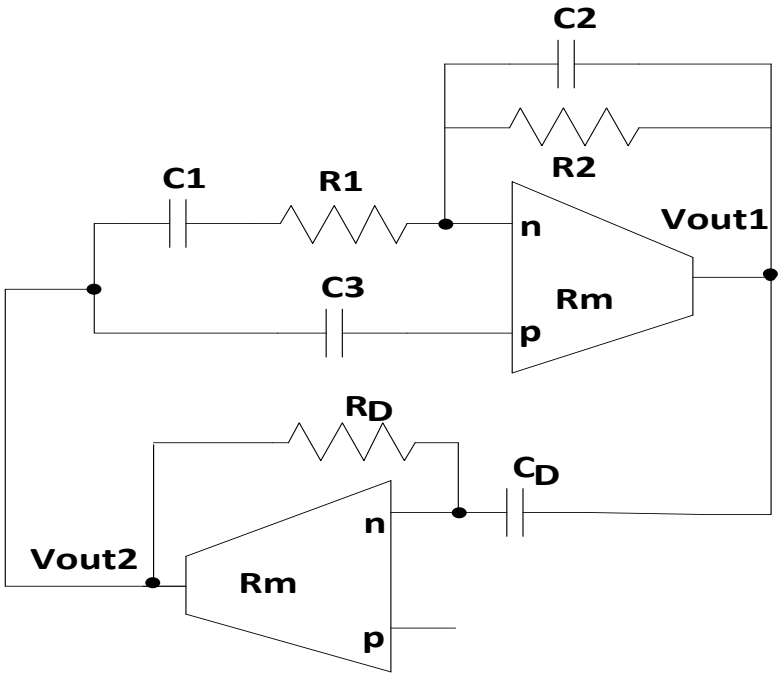


Figure 4.11. Proposed TOQO-I

Routine analysis of proposed topology gives the CE as

$$s^3C_1C_3R_DC_D + s^2C_1C_2 + s\left(\frac{C_1}{R_2}+\frac{C_2}{R_1}\right)+\frac{1}{R_1R_2}=0 \tag{4.21}$$

The FO and CO are computed as

$$\text{FO: } f=\frac{\sqrt{C_1R_1+C_2R_2}}{2\pi\sqrt{C_1C_3R_1R_2R_DC_D}} \tag{4.22}$$

$$\text{CO: } (C_1R_1+C_2R_2)C_2=C_3R_DC_D \tag{4.23}$$

4.3.2 MOS -C Implementation of TOQO Topology-I

The MOS-C implementation of the proposed TOQO topology-I is shown in Figure 4.12 The resistance value may be adjusted by appropriate choice of gate controlling voltages (V_{ai}, V_{bi}; (i=1,2,3)) thereby making FO electronically tunable.

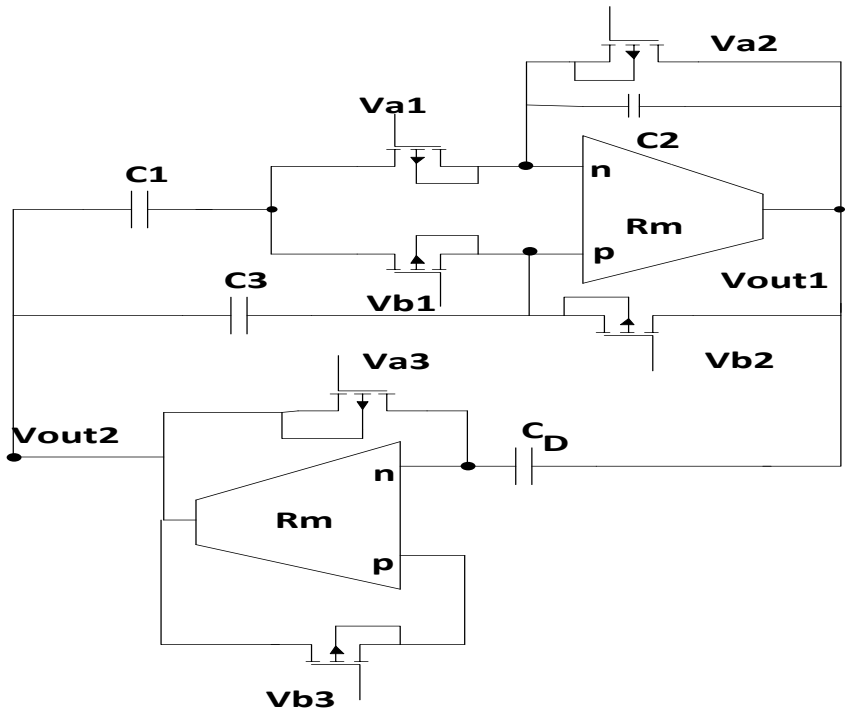


Figure 4.12. The MOS resistor based implementation of proposed TOQO-I

4.3.3 Nonideal Analysis

Taking the nonideal behavior of OTRA into account, the CE given by (4.21) modifies to

$$Ws^3 + Xs^2 + Ys + Z = 0 \tag{4.24}$$

where the coefficients W, X, Y and Z can respectively be expressed as

$$W = CC_2C_PR_D + C_P^2CR_D + C^2C_DR_D;$$

$$X = CC_2 + CC_P + CC_P\frac{R_D}{R_2} + C_PC_2\frac{R_D}{R_1} + C_P^2C\frac{R_D}{R_1};$$

$$Y = \frac{C}{R_2} + \frac{(C_2 + C_P)}{R_1} + \frac{R_DC_P}{R_1R_2}; Z = \frac{1}{R_1R_2}$$

The modified FO and CO due to nonidealities are given by

$$\text{FO: } \hat{f}_o = \frac{1}{2\pi}\sqrt{\frac{\frac{R_D C_p}{R_1+R_2}+\frac{C}{R_2}+\frac{C_2+C_p}{R_1}}{C^2 C_D R_D + C R_D (C_2+C_p)}} \tag{4.25}$$

$$\text{CO}: (C_2+C_p)R_2 + CR_1 + C_p R_D = \frac{R_1 R_2 R_D \{C(C_2+C_p)+C^2 C_D\}}{R_2(C+C_p)\left(R_1 C + R_D C_p\right) + R_1 R_D C_p C} \tag{4.26}$$

As the parasitic capacitance of the OTRA is very small, using approximation $(C_2+C_p)\approx C$ the coefficients W, X, Y and Z can be simplified as

$$\begin{cases} W = CC_2C_pR_D + C_p^2CR_D + C^2C_DR_D \\ \quad = CR_D\left(C_p(C_2+C_p)+CC_D\right) \\ \quad \approx CR_D\left(C_pC+CC_D\right) \\ \quad \approx C^2R_D\left(C_p+C_D\right) \\ \quad \approx C^2R_DC_D \end{cases} \tag{4.27}$$

$$\begin{cases} X = CC_2 + CC_p + CC_p\frac{R_D}{R_2} + C_pC_2\frac{R_D}{R_1} + C_p^2C\frac{R_D}{R_1} \\ \quad = C(C_2+C_p) + C_p(C_2+C_p)\frac{R_D}{R_1} + \frac{R_D}{R_2}C_pC \\ \quad \approx C^2 + CC_p\left(\frac{R_D}{R_1}+\frac{R_D}{R_2}\right) \\ \quad \approx C^2 \text{ as } CC_P << C^2 \end{cases} \tag{4.28}$$

$$\begin{cases} Y = \frac{C}{R_2} + \frac{(C_2+C_p)}{R_1} + \frac{R_DC_p}{R_1R_2} \\ \quad \approx \frac{C}{R_2} + \frac{C}{R_1} + \frac{R_DC_p}{R_1R_2} \; as \; C_p << C \text{ as } C_p << C \\ \quad \approx \frac{C}{R_2} + \frac{C}{R_1} \end{cases} \tag{4.29}$$

$$Z = \frac{1}{R_1 R_2} \tag{4.30}$$

By substituting W, X, Y, Z (4.27) to (4.30) in (4.24), the CE becomes same as (4.21) and FO and CO of (4.25) and (4.26) reduce to (4.22) and (4.23) respectively.

4.3.4 Sensitivity Analysis

The sensitivity of FO (f_o) with respect to R_1, R_2, C and C_D are given as

$$\left|S_{C_D}^{f_o}\right| = \left|S_{C}^{f_o}\right| = \frac{1}{2}; \left|S_{R_1}^{f_o}\right| = \frac{R_2}{2(R_1+R_2)}; \left|S_{R_2}^{f_o}\right| = \frac{R_1}{2(R_1+R_2)} \tag{4.31}$$

It may be noted that all sensitivities are well within unity.

4.3.5 Frequency Stability

The open loop transfer function *H(s)* of Figure 4.11 is computed as

$$H(s) = \frac{-s^3 C_1 C_3 C_D R_D R_1 R_2}{(1+sC_1R_1)(1+sC_2R_2)} \tag{4.32}$$

The frequency stability factor (S^F) with condition setting as C_1= C_3= C, C_2= C_D= nCand R_1= R_2= R/2, R_D= R, is given by

$$S^F = -\sqrt{n} \text{ for n>>1.} \tag{4.33}$$

Inspection of (4.33) suggests that high S^F values can be achieved by selecting a larger value of *n*. Therefore, the proposed QO offers excellent frequency stability.

4.3.6 Phase Noise Analysis

The open loop transfer function H(s) of the proposed circuit by assuming equal capacitances except C_D is given as

$$H(s) = \frac{-s^3 C^2 C_D R_D R_1 R_2}{(1+sCR_1)(1+sCR_2)} \tag{4.34}$$

For $\omega \approx \omega_o, A \approx 1,$ the H(s) given by (4.34) can be expressed in terms of magnitude and phase as

$$H(j\omega) = A(\omega).e^{j\varphi(\omega)} \tag{4.35}$$

Substituting the CO and FO of the proposed oscillator in (4.34) the magnitude A(ω) can be written as

$$|A(\omega)| = \frac{\left(\frac{\omega}{\omega_o}\right)^2 \omega}{\sqrt{\left(-\frac{1}{C_D R_D}\left(\frac{\omega}{\omega_o}\right)^2 + \frac{1}{C(R_1+R_2)}\right)^2 + \omega^2}} \tag{4.36}$$

determining $\left|\frac{dA}{d\omega}\right|$ from (4.36) results in

$$\left|\frac{dA}{d\omega}\right| = \frac{2}{\omega_o} \tag{4.37}$$

the phase $\angle H(\omega)$ can be evaluated as

$$\angle H(\omega) = \varphi = -tan^{-1}\left(\frac{\frac{1}{\omega C_D R_D} - \frac{1}{C\omega\left(\frac{\omega}{\omega_o}\right)^2 (R_1+R_2)}}{\left(\frac{\omega}{\omega_o}\right)^{-2}}\right) \tag{4.38}$$

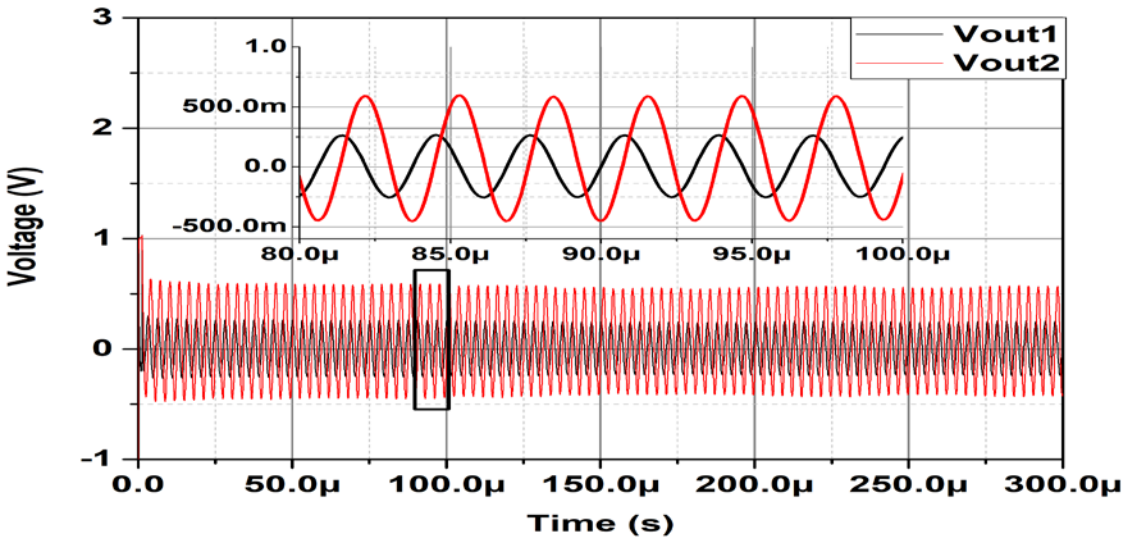
determining $\left|\frac{d\varphi}{d\omega}\right|$ from (4.38) results

$$\left|\frac{d\varphi}{d\omega}\right| = \frac{2}{\omega_o^2 C_D R_D} \tag{4.39}$$

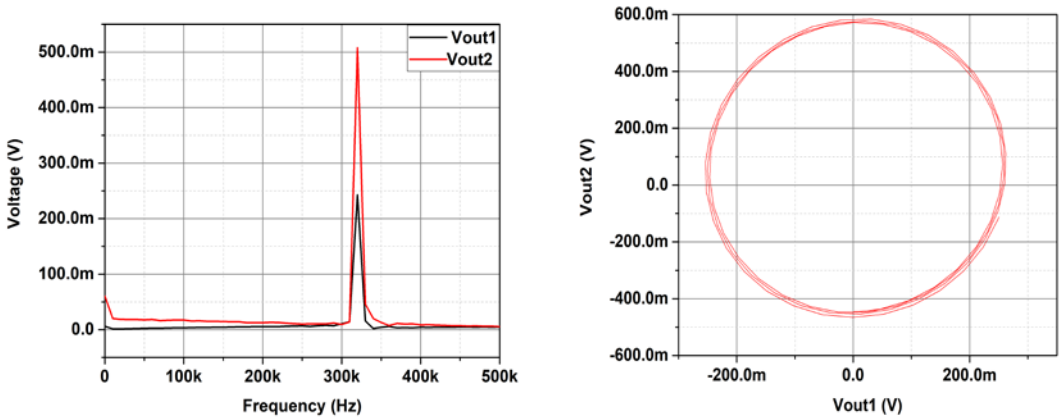
From (4.39), it is clear that the frequency stability of proposed TOQO topology-I decreases with the increase of ω_o due to phase noise.

4.3.7 Simulation Results

The workability of the proposed circuit is tested through SPICE simulations. Component values are chosen as C_1= C_2= C_3= C_D= 100 pF and R_1= R_2= 5 kΩ, R_D= 10 kΩ. The simulated transient output, corresponding frequency spectrum and plot of $Vout_1$ vs. $Vout_2$ are shown in Figure 4.13 (a), (b) and (c), respectively. The simulated FO was observed to be 320 KHz as against the calculated value of 318.47 KHz. The quadrature phase relationship between Vout1 and Vout2 is also verified through Figure 4.13 (c).



(a)



(b) (c)

Figure 4.13. (a) Transient output (b) frequency spectrum and (c) plot of Vout1 vs. Vout2 of proposed TOQO topology-I

The robustness of the proposed circuit is tested through Monte Carlo simulations by considering Gaussian distribution with 5% variations in all the passive components used. Figure 4.15 presents the histogram of the Monte Carlo runs it is observed, that the circuit operates well within 2% variation around theoretical FO.

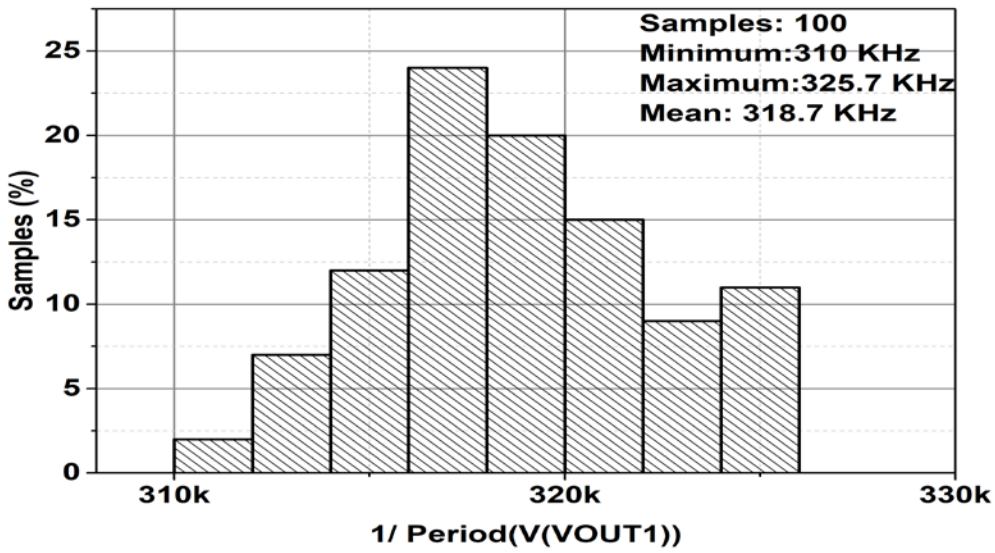
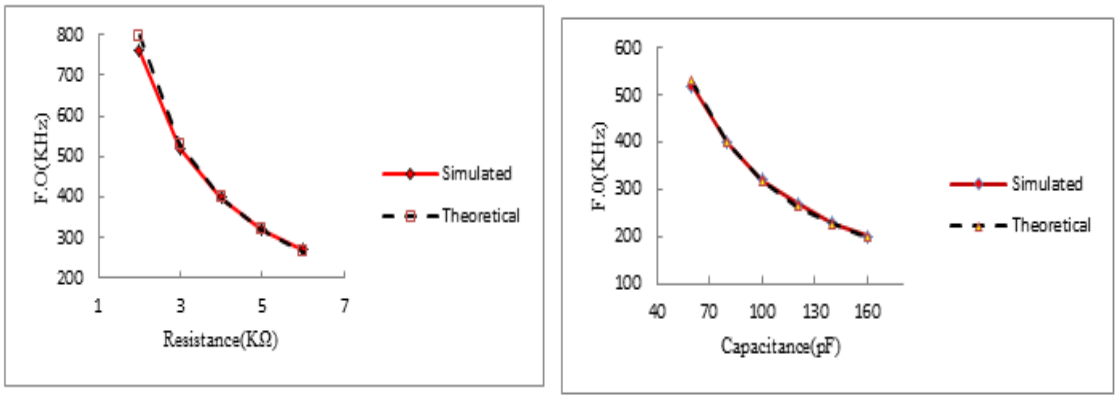


Figure 4.14. Histogram of proposed third order QO-I

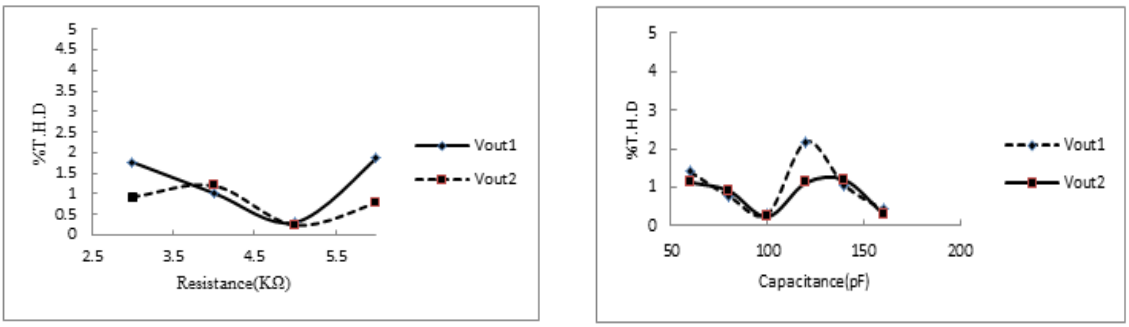
The FO of the proposed QO can be tuned by varying R, as suggested by (4.22). The FO tuning with R (varied from 3 kΩ to 6 kΩ) while keeping C fixed (100 pF) is shown in Figure 4.15 (a) whereas tuning with C (varied from 60 pF to 140 pF) with R fixed at 5 kΩ is depicted in Figure 4.15 (b). It may be observed that the simulated and theoretical values of FO are in close agreement



(a) (b)

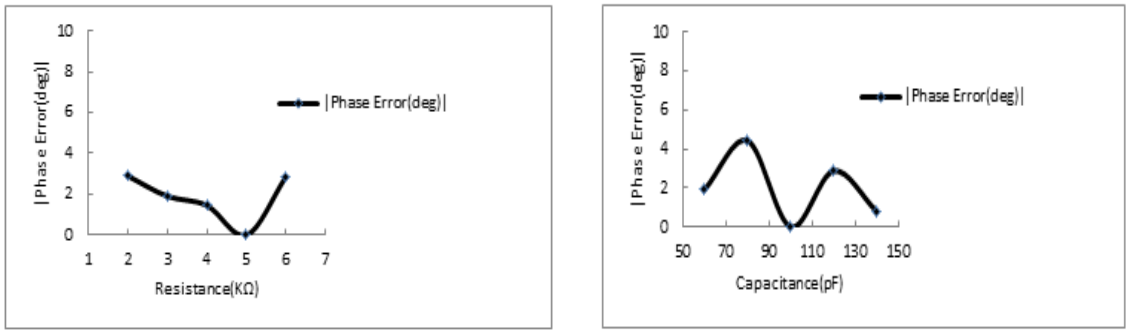
Figure 4.15. Frequency tuning of proposed QO (Figure 4.12) with (a) Resistance (b) Capacitance

The % THD variation with R and C is also studied and is depicted in Figure 4.16. The % THD variation with R (C= 100 pF) for both quadrature outputs is recorded in Figure 4.16 (a) and the largest value observed is 1.87%. Similarly, Figure 4.16 (b) shows % THD variation with C (R= 5 kΩ), wherein the maximum observed value is well within 2.5%.



(a) (b)

Figure 4.16. The % THD variation with (a) Resistance (b) Capacitance



(a) (b)

Figure 4.17. Phase error between Vout1 and Vout2

with (a) Resistance (b) Capacitance

The phase error plots between V_{out1} and V_{out2} are also examined by varying R and keeping C constant and vice versa. Variation of phase error with resistance and capacitance are depicted in Figure 4.17 (a) and (b), respectively. The largest value of error is observed to be 5^{o}.

4.3.8 Experimental Results

The proposed TOQO topology-I is also tested experimentally by breadboarding the circuit of Figure 4.12. The passive component values are chosen same as simulated driven output. Figure 4.18 depicts the transient output obtained on CRO at 320 KHz.

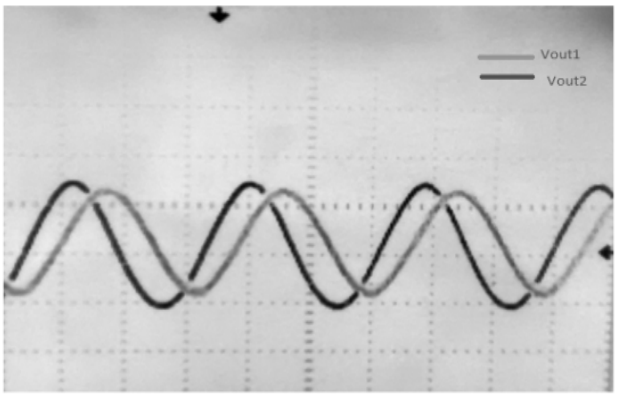


Figure 4.18. Transient Response of Proposed TOQO-I on CRO

4.3.9 Proposed TOQO Topology-II

This section presents three TOQO topologies, derived from a generic third order inverse filter (IF). The IFs are used to reverse the distortions of the signal incurred due to signal processing and transmission. For the signal correction, the IF should have a frequency response reciprocal to the frequency response of the system causing distortion [193]-[211]. It is observed that few first order [202] and second order [193]-[201], [203]-[207], [209]-[211] IF topologies are reported in literature. However, no third order IF topology is available in the open literature. In this work, a generic third order IF structure based on the OTRA is developed, which is configured to provide inverse low-pass (ILP), inverse High-pass (IHP) and Inverse band-pass (IBP) filter responses through component selections. The proposed generic IF is then used to derive a generalized third order SO structure, which leads to the design of three different SOs with appropriate component selection.

Proposed Generic IF

The proposed generic third order IF is shown in Figure 4.19. It uses three OTRAs and nine passive components. The transfer function for the proposed configuration is obtained as

$$\frac{Vout}{Vin} = \frac{Y_1Y_3Y_5 + Y_2Y_4Y_6}{Y_2Y_4Y_7} \tag{4.40}$$

where Y_i (i= 1to7) represents some admittance. The component selection, corresponding transfer functions and filter parameters are listed in Table 4.1.

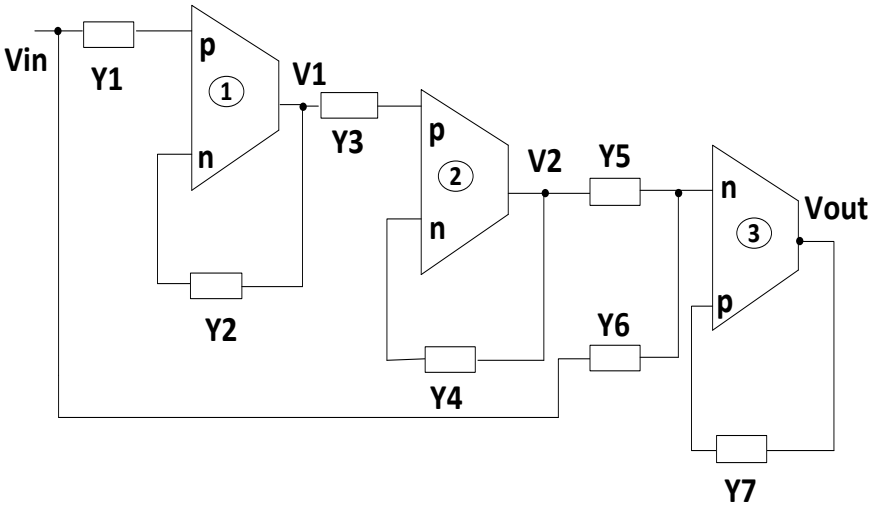


Figure 4.19. Proposed generalized third order IF

In literature, active filters have been used to design sinusoidal oscillators by creating a unity feedback loop around the filters. This concept is adapted here with proposed IFs for the first time to develop the new oscillator topologies. By placing unity feedback around ILP, IHP and IBP filters, CEs of (4.41)-(4.43) are obtained and corresponding oscillators are termed as ILP_SO, IHP_SO and IBP_SO.

$$s^3C_1C_2C_4R_1R_2R_3 + \frac{s^2C_1C_2R_1R_2R_3}{R_4} + sC_3R_3 + \left(1 - \frac{R_3}{R_5}\right) = 0 \tag{4.41}$$

Table 4.1. Proposed IF transfer functions and their parameters

IF Type	***Component selection***	***Transfer function***	***IF parameters***
ILP	$Y_1=sC_1, Y_2=\frac{1}{R_1}, Y_3=sC_2, Y_4=\frac{1}{R_2},$ $Y_5=\frac{1}{R_4}+sC_4,\ Y_6=\frac{1}{R_3}+sC_3,\ Y_7=\frac{1}{R_5}$	$\frac{Vout}{Vin}=\frac{\frac{1}{C_1C_2C_4R_1R_2R_3}\left(\frac{R_3}{R_5}\right)}{s^3+\frac{s^2}{C_4R_4}+\frac{sC_3}{C_1C_2C_4R_1R_2}+\frac{1}{C_1C_2C_4R_1R_2R_3}}$	$\omega_{oILP}^3=\frac{1}{C_1C_2C_4R_1R_2R_3};$ $Q_{ILP}=\frac{C_4R_4}{\sqrt[3]{C_1C_2C_4R_1R_2R_3}-C_4R_4};(H_o)_{ILP}=\frac{R_3}{R_5}$
IHP	$Y_1=\frac{1}{R_1},\ Y_2=sC_1,\ Y_3=\frac{1}{R_2},\ Y_4=sC_2,$ $Y_5=\frac{1}{R_4}+sC_4,\ Y_6=\frac{1}{R_3}+sC_3,\ Y_7=sC_5;$	$\frac{Vout}{Vin}=\frac{s^3\left(\frac{C_5}{C_3}\right)}{s^3+\frac{s^2}{C_3R_3}+\frac{sC_4}{C_1C_2C_3R_1R_2}+\frac{1}{C_1C_2C_3R_1R_2R_4}}$	$\omega_{oIHP}^3=\frac{1}{C_1C_2C_3R_1R_2R_4};$ $Q_{IHP}=\frac{C_3R_3}{\sqrt[3]{C_1C_2C_4R_1R_2R_3}-C_3R_3};(H_o)_{IHP}=1;$ $for\ C_3=C_5$
IBP	$Y_1=\frac{1}{R_1},\ Y_2=sC_1,\ Y_3=\frac{1}{R_2}\ \ Y_4=sC_2,$ $Y_5=\frac{1}{R_4}+sC_4,\ Y_6=\frac{1}{R_3}+sC_3,\ Y_7=\frac{1}{R_5}$	$\frac{Vout}{Vin}=\frac{\frac{s^2}{C_3R_3}\left(\frac{R_3}{R_5}\right)}{s^3+\frac{s^2}{C_3R_3}+\frac{sC_4}{C_1C_2C_3R_1R_2}+\frac{1}{C_1C_2C_3R_1R_2R_4}}$	$\omega_{oIBP}^3=\frac{1}{C_1C_2C_3R_1R_2R_4};$ $Q_{IBP}=\frac{C_3R_3}{\sqrt[3]{C_1C_2C_4R_1R_2R_3}-C_3R_3};(H_o)_{IBP}=\left(\frac{R_3}{R_5}\right)$

$$s^3C_1C_2C_3R_1R_2R_4\left(1-\left(\frac{C_5}{C_3}\right)\right)+\frac{s^2C_1C_2R_1R_2R_4}{R_3}+sC_4R_4+1=0 \tag{4.42}$$

$$s^3C_1C_2C_3R_1R_2R_4+\frac{s^2C_1C_2R_1R_2R_4}{R_3}\left(1-\left(\frac{R_3}{R_5}\right)\right)+sC_4R_4+1=0 \tag{4.43}$$

Table 4.2 enlists the FO and CO of the proposed ILP_SO, IHP_SO and IBP_SO computed from CEs of (4.41) to (4.43). It is worth mentioning that the FO for all proposed SO topologies can be tuned independently using resistors without affecting CO. Similarly, CO can be altered with the help of resistors without affecting FO, thereby manifesting independent tuning.

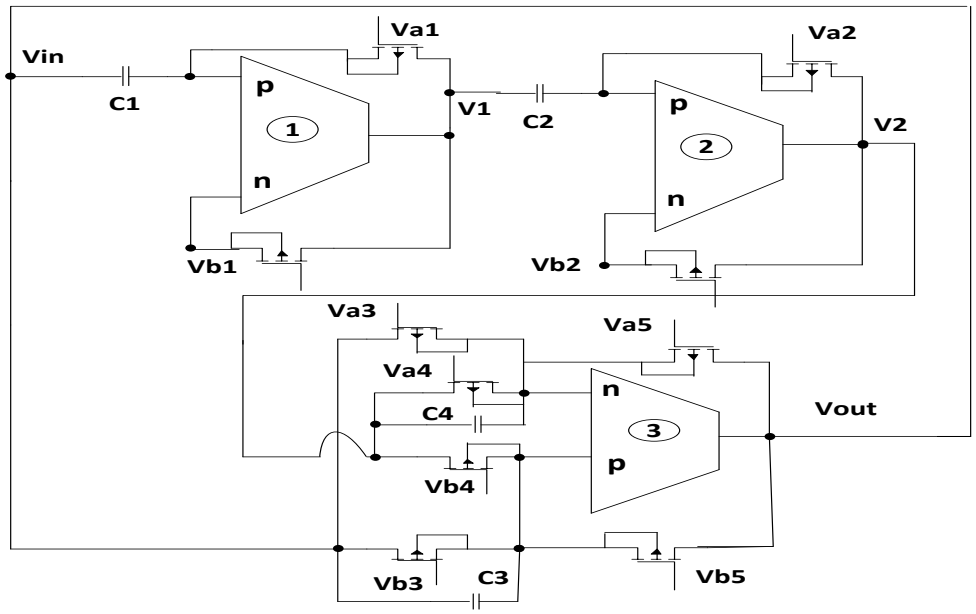
Table 4.2. Frequency of oscillation and condition of oscillation of proposed QO topologies

Circuit	Frequency of oscillaton (f_o)	Condition of oscillation	Independent Tuning
ILP_SO	$\frac{\sqrt{C_3}}{2\pi\sqrt{C_1C_2C_4R_1R_2}}$	$\frac{C_3}{C_4}=\left(1-\frac{R_3}{R_5}\right)\frac{R_4}{R_3}$	R_1, R_2
IHP_SO	$\frac{\sqrt{C_4}}{2\pi\sqrt{C_1C_2C_3R_1R_2(1-C_5/C_3)}}$	$\frac{R_3}{R_4}=\frac{C_4}{C_3(1-C_5/C_3)}$	R_1, R_2
IBP_SO	$\frac{\sqrt{C_4}}{2\pi\sqrt{C_1C_2C_3R_1R_2}}$	$\frac{C_4}{C_3}=\frac{R_3}{R_4\left(1-R_3/R_5\right)}$	R_1, R_2

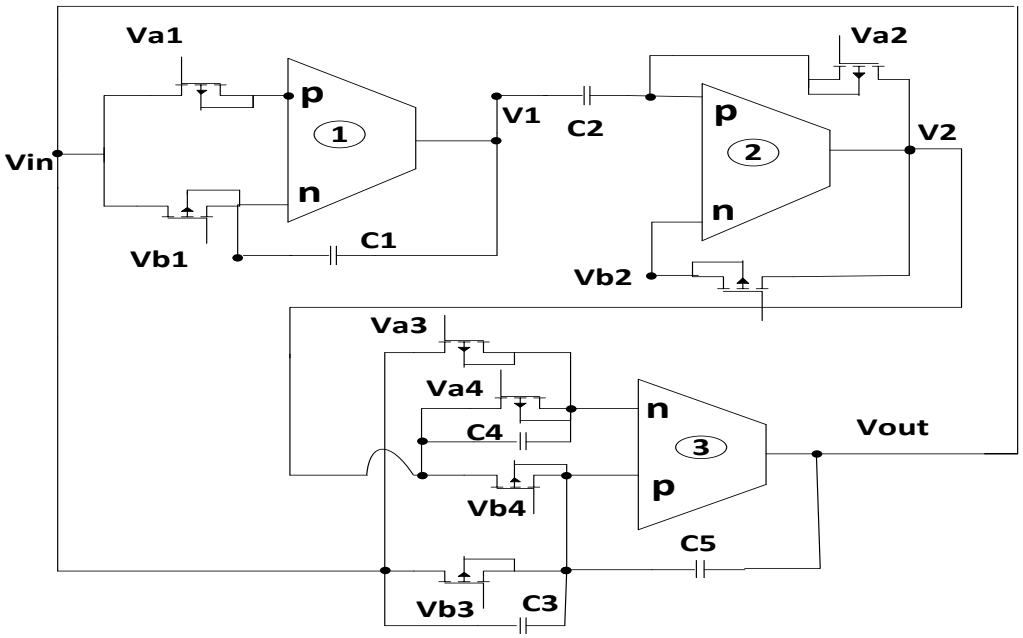
Further, a close observation on the component selection in Table 4.1 shows that ILP, IHP and IBP filters use either lossless integrator or lossless differentiator. Therefore, all three SOs provide quadrature response.

4.3.9.1 MOS -C Implementations

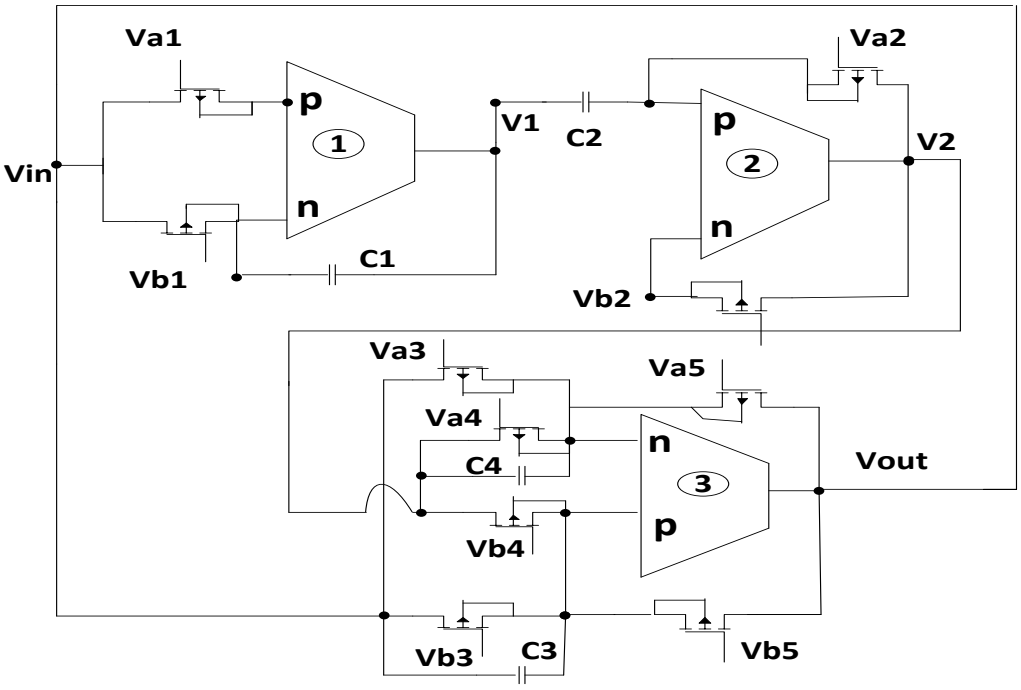
All the proposed IF based TOQOs are completely MOS-C realizable, which facilitates electronic tuning. The complete MOS-C implementations are shown in Figure 4.20.



(a)



(b)



(c)

Figure 4.20. Complete MOS-C implementations of proposed IF based TOQOs (a) ILP_SO (b) IHP_SO (c) IBP_SO

4.3.9.2 Nonideal Analysis

This subsection presents the effect of OTRA nonidealities on proposed QOs. The CE of ILP_SO, in presence of nonidealities, is expressed as

$$\begin{cases} s^3 C_1 C_2 C_4 R_1 R_2 R_3 \varepsilon_1(s)\ \varepsilon_2(s) + \dfrac{s^2 C_1 C_2 R_1 R_2 R_3}{R_4} \varepsilon_1(s)\ \varepsilon_2(s) + sC_3 R_3 + \\ \left(1 - \dfrac{R_3}{R_5} \varepsilon_3(s)\right) = 0 \end{cases} \tag{4.44}$$

where error functions are given as

$$\varepsilon_1(s) = 1/\left(1 + sC_p R_1\right); \varepsilon_2(s) = 1/\left(1 + sC_p R_2\right); \varepsilon_3(s) = 1/\left(1 - sC_p R_5\right)$$

The altered CE of (4.41) results in modification of FO and CO. Therefore, the compensation method must be applied for high-frequency applications to account for

deviations introduced in FOs. A complete passive compensation may be achieved by simply connecting a capacitor C_x between V_i and *p* terminal of i^{th} OTRA (i=1, 2) and V_{out} and *p* terminal of third OTRA. The CE of (4.41) with C_x, modifies to

$$\begin{cases} s^3C_1C_2C_4R_1R_2R_3+\dfrac{s^2C_1C_2R_1R_2R_3}{R_4}+\left(sC_3R_3+\left(1-\dfrac{R_3}{R_5}\left(1+s\left(C_p-C_X\right)R_5\right)\right)\right) \\ \left\{\left(1+s\left(C_p-C_X\right)R_1\right)\left(1+s\left(C_p-C_X\right)R_2\right)\right\}=0 \end{cases} \quad (4.45)$$

It may be noted that the effect of C_p can be eliminated by choosing $C_x = C_p$.

The CE of the IHP_SO in the presence of nonidealities is computed as

$$\begin{cases} s^3\left(C_p+C_1\right)\left(C_p+C_2\right)C_3R_1R_2R_4\left(1-\left(\dfrac{C_5-C_p}{C_3}\right)\right)+ \\ \dfrac{s^2\left(C_p+C_1\right)\left(C_p+C_2\right)R_1R_2R_4}{R_3}+sC_4R_4+1=0 \end{cases} \quad (4.46)$$

The effect of C_p can be eliminated by pre-adjusting the value of capacitors C_1, C_2 and C_5, thus achieving self-compensation.

The CE of the IBP_SO in the presence of nonidealities is obtained as

$$\begin{cases} s^3\left(C_p+C_1\right)\left(C_p+C_2\right)C_3R_1R_2R_4+s^2\left(C_p+C_1\right)\left(C_p+C_2\right)R_1R_2R_4 \\ \left(\dfrac{1}{R_3}-\dfrac{1}{R_5}\varepsilon_1(s)\right)+sC_4R_4+1=0 \end{cases} \quad (4.47)$$

where $\varepsilon_1(s)=1\Big/\left(1-sC_pR_5\right)$

The effect of C_p may be eliminated by pre-adjusting the value of capacitors C_1 and C_2 and placing capacitor of value C_x between V_{out} and *p* terminal of third OTRA

The nonideal FO and CO of all three topologies, along with the passive compensated error functions (wherever applicable), are listed in Table. 4.3

Table 4.3. Nonideal FO and CO of proposed IF based QO topologies

Circuit	Nonideal FO ($\hat{f}_o$)	Nonideal CO	Passive compensated error functions
ILP_SO	$\frac{f_0}{\sqrt{\varepsilon_1(s)\,\varepsilon_2(s)}}$	$\frac{C_3}{C_4}=\left(1-\frac{R_3}{R_5}\varepsilon_3(s)\right)\frac{R_4}{R_3}$	$\in_1(s)=1\Big/\left(1+s\left(C_p-C_X\right)R_1\right)$ $\in_2(s)=1\Big/\left(1+s\left(C_p-C_X\right)R_2\right)$ $\in_3(s)=1\Big/\left(1-s\left(C_p-C_X\right)R_5\right)$
IHP_SO	$\frac{f_0\sqrt{\left(1-\left(C_5-C_p\right)\Big/C_3\right)}}{\sqrt{\left(1+C_p/C_1\right)\left(1+C_p/C_2\right)\left(1-\left(C_5-C_p\right)\Big/C_3\right)}}$	$\frac{R_3}{R_4}=\frac{C_4}{C_3\left(1-\left(C_5-C_p\right)\Big/C_3\right)}$	-
IBP_SO	$\frac{f_0}{\sqrt{\left(1+C_p/C_1\right)\left(1+C_p/C_2\right)}}$	$\frac{C_4}{C_3}=\frac{R_3}{R_4\left(1-\varepsilon_1(s)(R_3/R_5)\right)}$	$\in_3(s)=1\Big/\left(1-s\left(C_p-C_X\right)R_5\right)$

Table 4.4. Sensitivity calculations for proposed IF based TOQOs

Circuit	$S_Y^{f_o}$
ILP_SO	$\left\|S_{R_3}^{f_o}\right\| = \left\|S_{R_4}^{f_o}\right\| = \left\|S_{R_5}^{f_o}\right\| = 0; \left\|S_{C_1}^{f_o}\right\| = \left\|S_{C_2}^{f_o}\right\| = \left\|S_{C_3}^{f_o}\right\| = \left\|S_{C_4}^{f_o}\right\| = \left\|S_{R_1}^{f_o}\right\| = \left\|S_{R_2}^{f_o}\right\| = \frac{1}{2}$
IHP_SO	$\left\|S_{R_3}^{f_o}\right\| = \left\|S_{R_4}^{f_o}\right\| = 0; \left\|S_{C_1}^{f_o}\right\| = \left\|S_{C_2}^{f_o}\right\| = \left\|S_{C_4}^{f_o}\right\| = \left\|S_{R_1}^{f_o}\right\| = \left\|S_{R_2}^{f_o}\right\| = \frac{1}{2}; \left\|S_{C_3}^{f_o}\right\| = \frac{1}{2(1-C_5/C_3)}; \left\|S_{C_5}^{f_o}\right\| = \frac{C_5}{2(1-C_5/C_3)}; \left\|S_{C_1}^{\Lambda f_o}\right\| = \frac{C_1}{2(C_1+C_p)}; \left\|S_{C_1}^{\Lambda f_o}\right\| = \frac{C_2}{2(C_2+C_p)}; \left\|S_{C_3}^{\Lambda f_o}\right\| = \frac{1}{2\left(1-\left(C_5-C_p\right)/C_3\right)}$ $\left\|S_{C_5}^{\Lambda f_o}\right\| = \frac{C_5}{2\left(1-\left(C_5-C_p\right)/C_3\right)}; \left\|S_{C_p}^{\Lambda f_o}\right\| = \frac{C_p\left(2C_p(C_1+C_2+C_3-C_5)\right)+3C_p^2+C_1(C_2+C_3-C_5-C_2C_5/C_1+C_2C_3/C_1)}{2C_3\left(1-\left(C_5-C_p\right)/C_3\right)\left(C_1+C_p\right)\left(C_2+C_p\right)}$
IBP_SO	$\left\|S_{R_3}^{f_o}\right\| = \left\|S_{R_4}^{f_o}\right\| = \left\|S_{R_5}^{f_o}\right\| = 0; \left\|S_{C_1}^{f_o}\right\| = \left\|S_{C_2}^{f_o}\right\| = \left\|S_{C_3}^{f_o}\right\| = \left\|S_{C_4}^{f_o}\right\| = \left\|S_{R_1}^{f_o}\right\| = \left\|S_{R_2}^{f_o}\right\| = \frac{1}{2}; \left\|S_{C_1}^{\Lambda f_o}\right\| = \frac{C_1}{2(C_1+C_p)}; \left\|S_{C_2}^{\Lambda f_o}\right\| = \frac{C_2}{2(C_2+C_p)}; \left\|S_{C_p}^{\Lambda f_o}\right\| = \frac{C_p(C_1+C_2+2C_p)}{2(C_2+C_p)(C_1+C_p)}$

4.3.9.3 Sensitivity Analysis

The sensitivity of f_o with respect to circuit component and parasitics for proposed IF based TOQOs is listed in Table 4.4. From Table 4.4, it is evident that all the passive sensitivities of proposed IF based TOQOs are low. It is found that with $C_p \rightarrow 0$, the above-quoted passive sensitivities reduces to less than or equal half in magnitude.

4.3.9.4 Frequency Stability

The frequency stability expressions for all the proposed TOQOs are derived and are presented in Table 4.5.

Table 4.5. Frequency stability factors for proposed topologies

Circuit	Condition	S^F
ILP_SO	$C_1=C_2=C_3=C_4=C$ and $R_2=R_4=R_5=$ R, $R_3=R/2, R_1=$ R/n	$-2\sqrt{n}$
IHP_SO	$C_1=C_2=C_3=C_4=C, C_5=C/2$ and $R_2=R_3=$ R, $R_4=R/2, R_1=$ R/n	$\frac{-2\sqrt{2}}{\sqrt{n}}$
IBP_SO	$C_1=C_2=C_3=C_4=C$ and $R_2=R_4=R_5=$ R, $R_3=R/2, R_1=$ R/n	$-2\sqrt{n}$

It may be observed that the S^F can be made high by keeping n larger than unity for ILP_SO and IBP_SO. The S^F for IHP_SO can be made high by keeping n small. Therefore, all proposed oscillators enjoy good frequency stability by selecting n appropriately.

4.3.9.5 Phase Noise Analysis

The open loop transfer function for ILP_SO ($H_1(s)$) and IBP_SO ($H_2(s)$), by assuming equal capacitances and resistances except R_3 is given by

$$\begin{cases} H_1(s) = \dfrac{s^3C^3R^2R_3 + s^2C^2RR_3 + sCR_3 + 1}{\left(R_3 / R\right)} \\ H_2(s) = \dfrac{s^3C^3R^3 + s^2C^2R^3/R_3 + sRC + 1}{s^2C^2R^2} \end{cases} \quad (4.48)$$

Similarly, the open loop transfer function for IHP_SO ($H_3(s)$) by assuming equal resistances and capacitances except for C_3 is given by

$$H_3(s) = \frac{s^3C^2C_3R^3 + s^2C^2R^2 + sRC + 1}{s^3C^3R^3} \quad (4.49)$$

Let $H_i(j\omega) = A_i(\omega)\exp(j\varphi_i(\omega))$ for i = 1,2,3 then

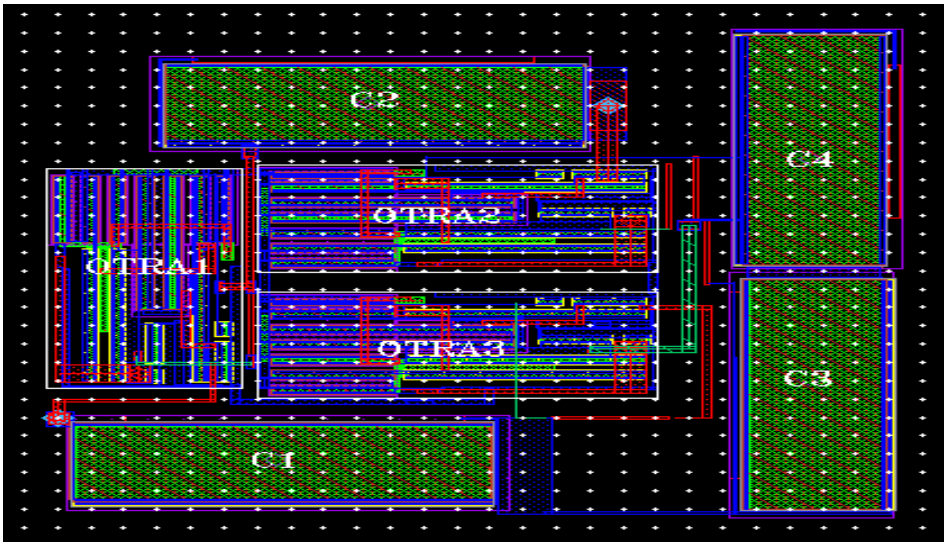
$$\left|\frac{dA_i}{d\omega}\right| = \frac{2}{\omega_o} \quad (4.50)$$

$$\left|\frac{d\varphi_1}{d\omega}\right| = \frac{2}{\omega_o}; \left|\frac{d\varphi_2}{d\omega}\right| \approx \frac{0.02}{\omega_o}; \left|\frac{d\varphi_3}{d\omega}\right| = \frac{3}{\omega_o} \quad (4.51)$$

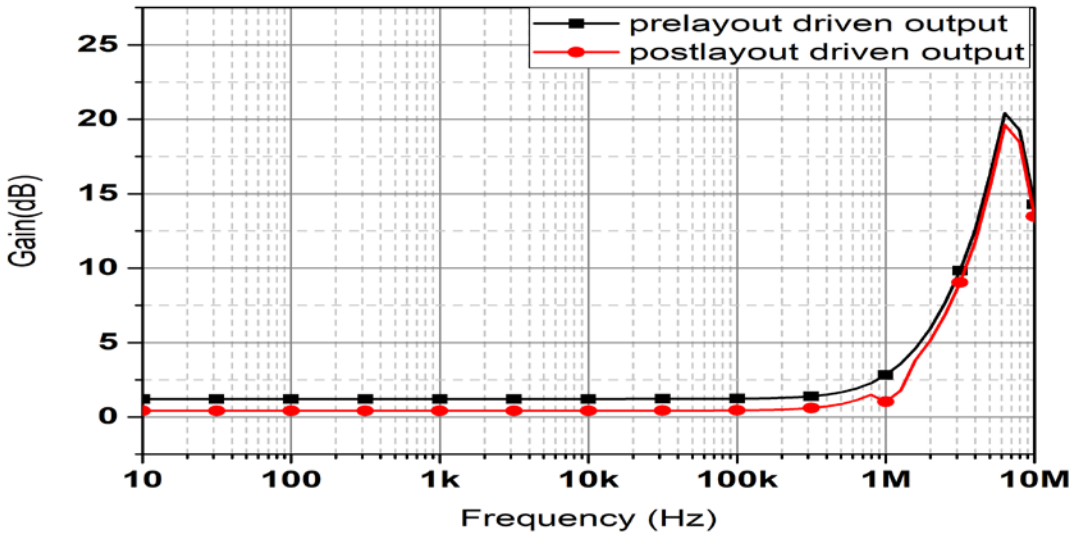
Inspection of (4.51) indicates that at higher frequencies, the frequency stability of all topologies decreases due to phase noise.

4.3.9.6 Functional Verification

The performances of the proposed IF configurations are tested both pre and post layout simulations in Cadence Virtuoso ADE spectre tool. The frequency responses of proposed IFs are examined for pole frequency of 1.59 MHz. All capacitors and resistors are chosen as 10 pF and 10 kΩ respectively. The complete physical layouts, pre and post-layout frequency responses for ILPF, IHPF and IBPF are shown in Figures 4.21, 4.22 and 4.23, respectively. The total die area taken by these IFs is 15693.5655µm^2 (24.05µmx126.51µm)(ILPF), 21267.2187µm^2(157.43µmx135.09µm)(IHPF), 16815.488 µm^2 (132.395µm x 127.01µm) (IBPF).

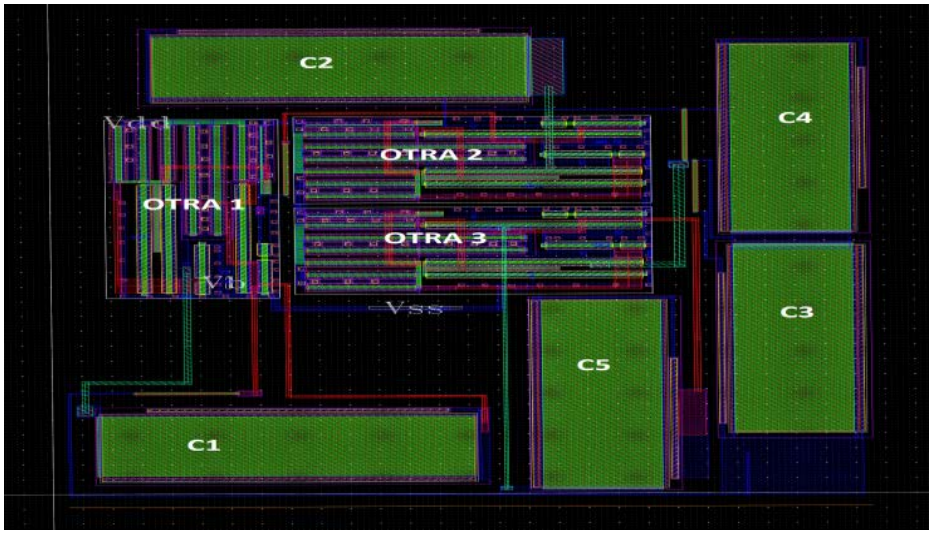


(a)

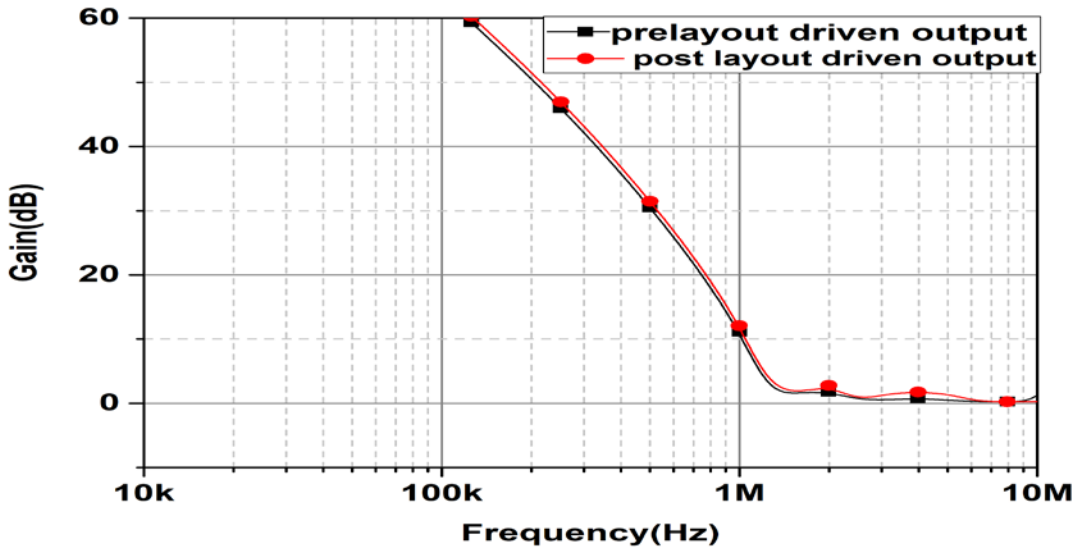


(b)

Figure 4.21. (a) Complete physical layout of ILPF and its (b) frequency response

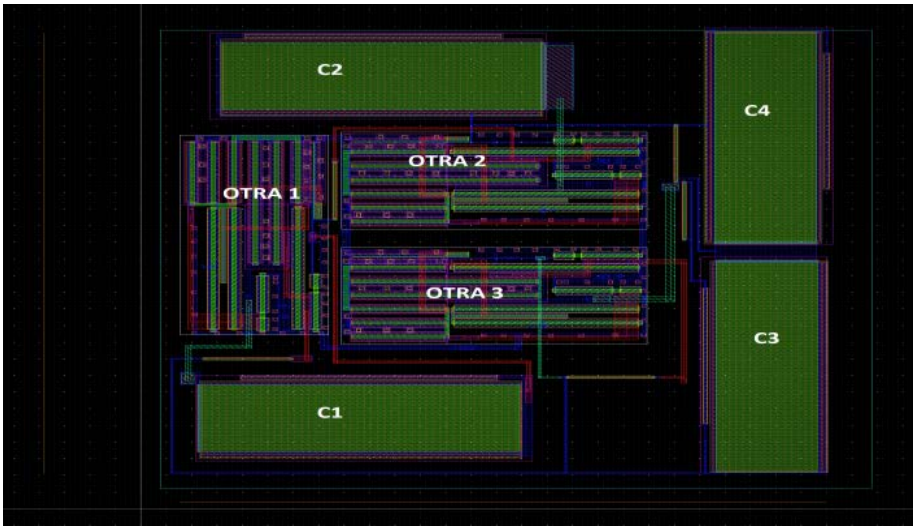


(a)

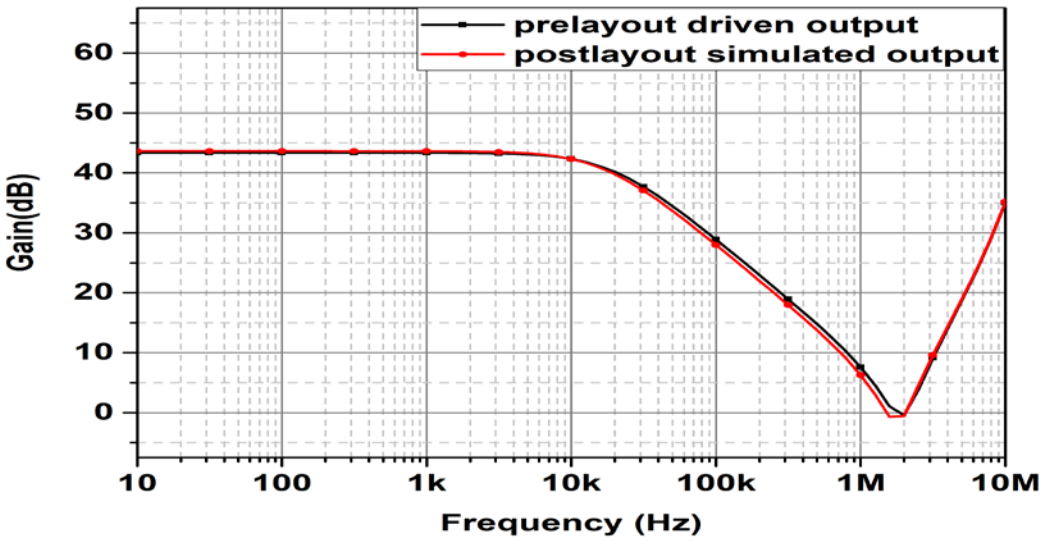


(b)

Figure 4.22. (a) Complete physical layout out IHPF and its (b) frequency response



(a)



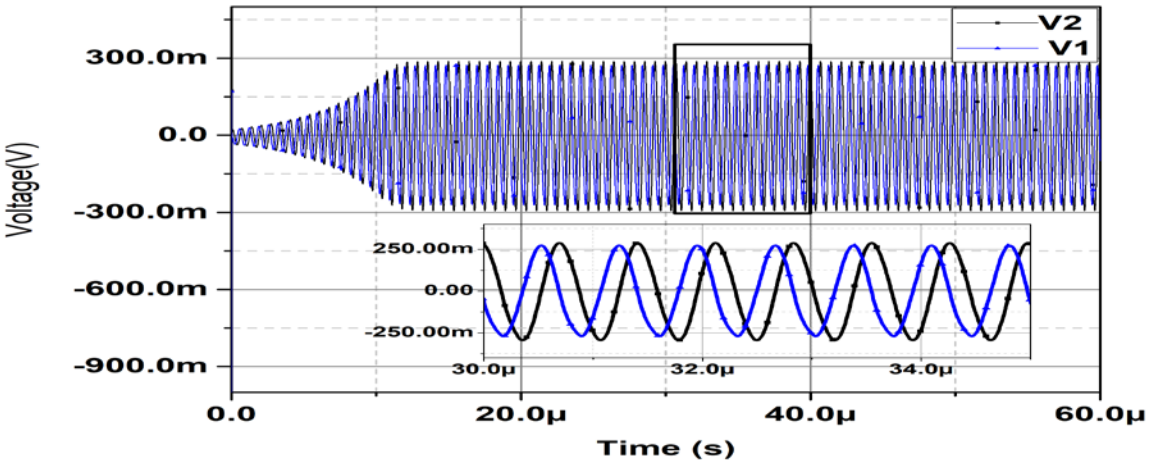
(b)

Figure 4.23. (a) Complete physical layout out IBPF and its (b) frequency response

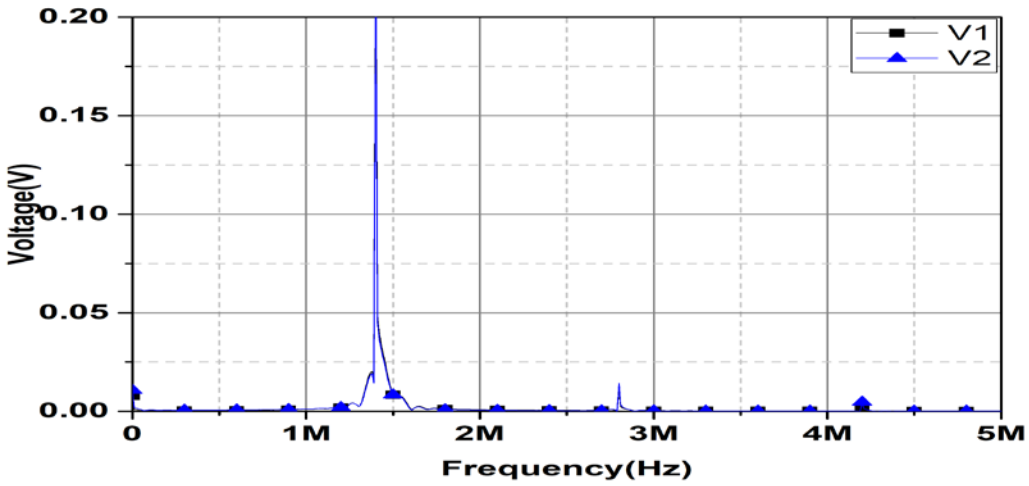
The maximum deviation between pre and post-layout results 6% for all IFs. Therefore, all the structures have been found to work in corroboration with theoretical propositions. The workability of the proposed SOs is verified through simulations. The component values are taken as : ILP_SO (R_1= R_2= R_4= R_5= 10 kΩ, R_3= 5 kΩ, C_1= C_2= 10 pF, C_3= C_4= 5 pF), IBP_SO (R_1= R_2=R_4= 10 kΩ, R_3= 5 kΩ, C_1= C_2= C_3= 10 pF, C_4= C_5= 5

pF) and IHP_SO (R_1= R_2= R_4= R_5= 10 kΩ, R_3=5 kΩ, C_1= C_2= 10 pF, C_3= C_4= 5 pF) which result in FO of 1.59 MHz.

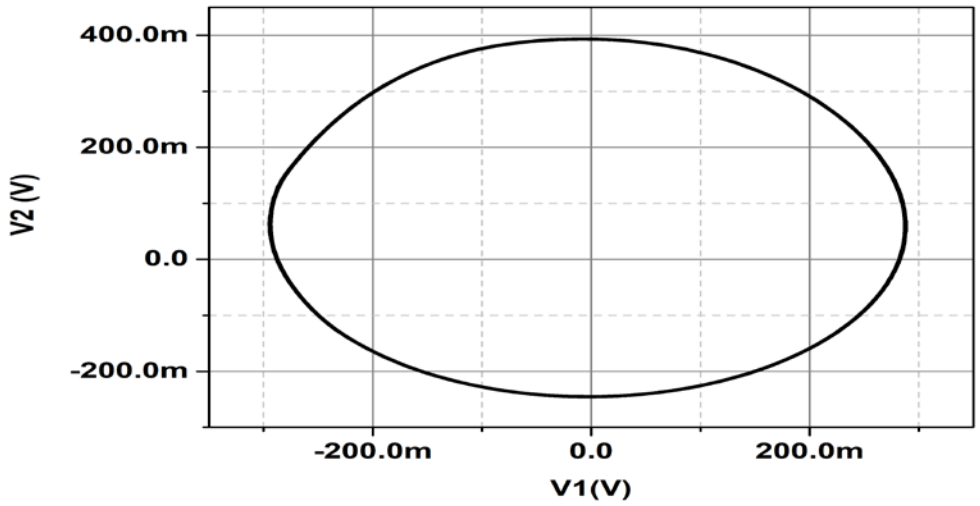
The simulated transient response and corresponding FFT responses and V_1 versus V_2 plot for proposed oscillators are depicted in Figures 4.24, 4.25 and 4.26, respectively. The % error in FO between simulated and theoretical values is obtained within 5.5%. The simulated FOs are found to be in well accordance with the theoretical values. The THDs for all TOQOs are found to be less than 2.3 %.



(a)

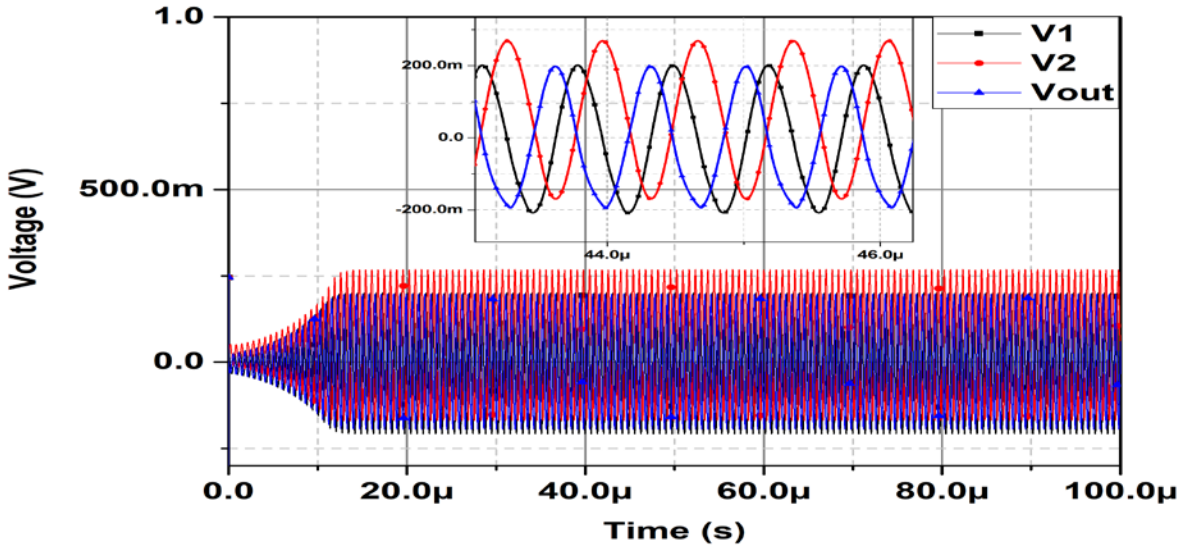


(b)

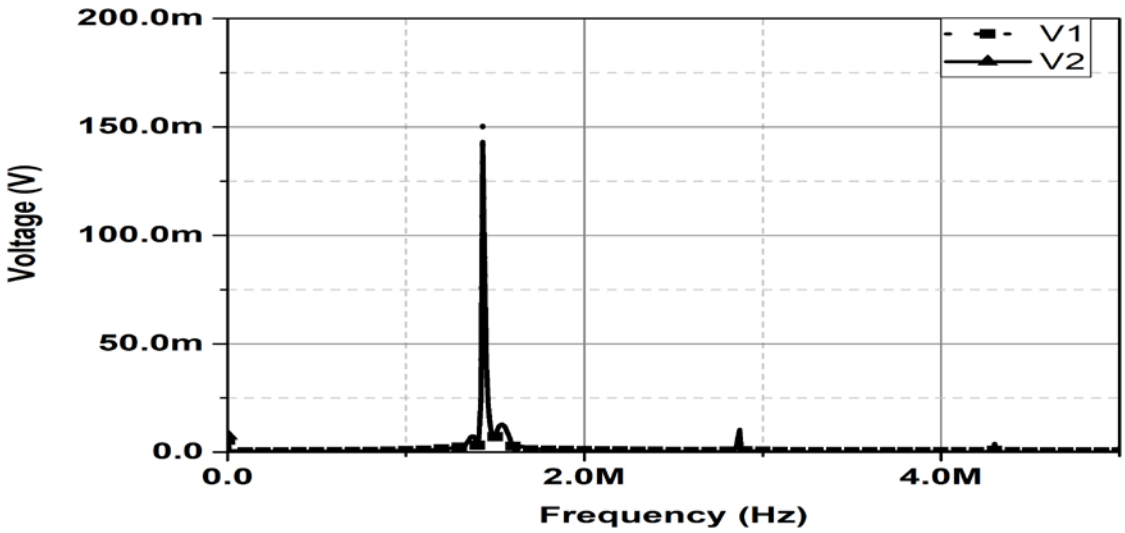


(c)

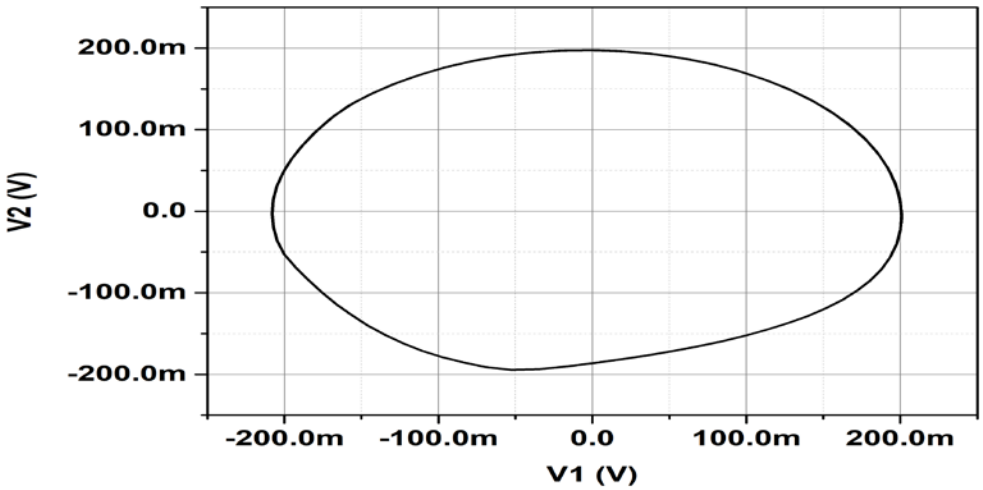
Figure 4.24. (a) Transient / steady-state response (b) FFT and (c) V1 versus V2 graphs for proposed ILP_SO



(a)

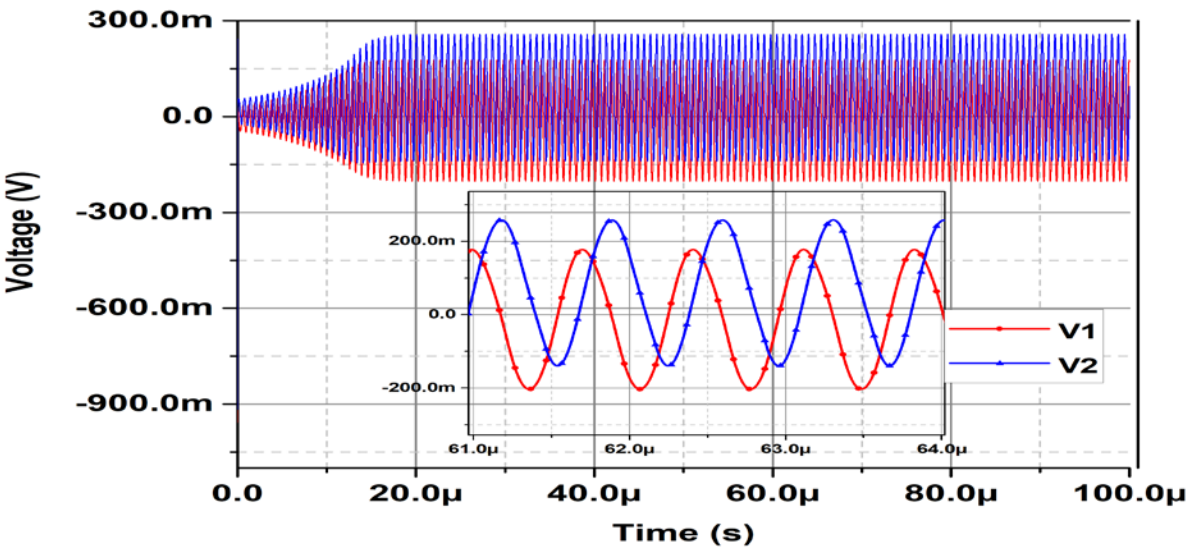


(b)

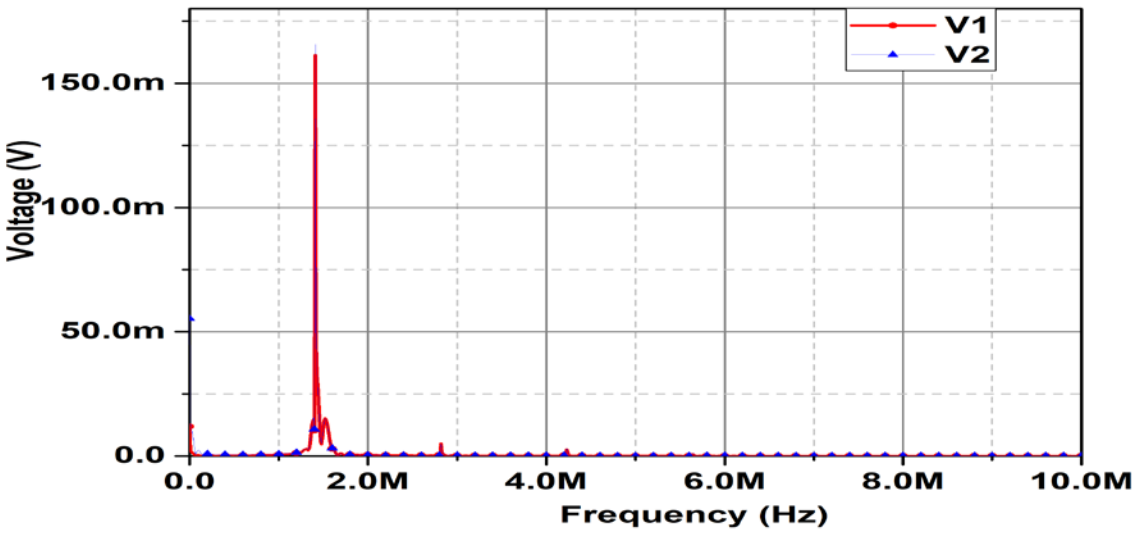


(c)

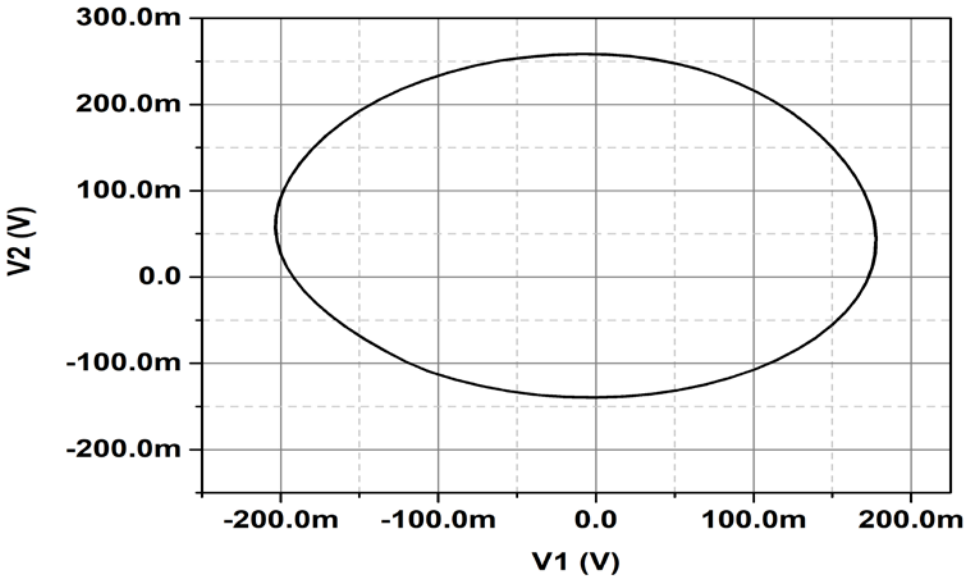
Figure 4.25. (a) Transient / steady-state response (b) FFT and (c) V1 versus V2 graphs for proposed IHP_SO


300.0m
0.0
-300.0m
-600.0m
-900.0m
Voltage (V)
0.0
20.0µ
40.0µ
60.0µ
80.0µ
100.0µ
Time (s)
200.0m
0.0
-200.0m
61.0µ
62.0µ
63.0µ
64.0µ
V1
V2

(a)


150.0m
100.0m
50.0m
0.0
Voltage (V)
0.0
2.0M
4.0M
6.0M
8.0M
10.0M
Frequency (Hz)
V1
V2

(b)



(c)

Figure 4.26. (a) Transient / steady-state response (b) FFT and (c) V1 versus V2 graphs for proposed IBP_SO

4.4 Conclusion

New topologies of OTRA based QOs are presented in this chapter. A new realization of second order OTRA based low frequency sinusoidal oscillator is proposed first followed by a third order quadrature oscillator using a high pass filter and a differentiator. Further, a new approach has been presented to design third order QOs employing a third order inverse filter (IF). Three different structures are proposed using the IF based approach. The functionality of the proposed structures is verified through Cadence Virtuoso ADE spectre tool using 0.18 µm technology parameters. Moreover, the layouts of the proposed IFs, second order QO are also presented. The pre, post-layout simulation results are found to be in close agreement with theoretical propositions.

The QO designed using a high pass filter and a differentiator is verified through SPICE simulations using a 0.18µm technology parameter. This topology is further tested experimentally wherein the OTRA is realized using off the shelf CFOA IC AD844.

The effect of nonidealities of OTRA has been analyzed by considering a single-pole model, which suggests that for high-frequency applications, self-compensation can be used. The sensitivity of f_o with respect to passive components is also examined and values found out to be less than or equal to half in magnitude. The simulated value of THD for all proposed QOs is observed to be quite low.

CHAPTER 5
GENERIC OSCILLATOR STRUCTURE FOR WIDE FREQUENCY TUNING

The content and results of the following papers have been reported in this chapter

1. K. Gurumurthy, R. Pandey and N. Pandey, “New sinusoidal oscillator configurations using operational transresistance amplifier,” Int J Circ Theor Appl. vol. 47, no. 5, pp. 666-685, 2019. **(SCI) (IF:1.5)**

5.1 Introduction

Sinusoidal Oscillators with wide frequency tuning have many advantages in the field of communication, measurement and instrumentation systems. In chapter 3, single OTRA based single-phase SOs capable of generating LF without using high values of passive components were presented. However, these topologies suffer high FO sensitivity to passive component variations and lack independent tuning.

The objective of this chapter is to design SOs having wide frequency tuning range with low FO passive sensitivities. This chapter introduces four new structures with following features: 1) less RC component spread for wide range of frequency tuning 2) minimal FO sensitivity to component variations 3) electronic tunability 4) independent FO tuning 5) excellent frequency stability and 6) less complex design constraints/equations.

5.2 Proposed Oscillators

The proposed oscillators consist of a generic forward path with varied structures in the feedback loop, thereby resulting in different topologies. The generalized representation of forward-path used in the proposed configurations is shown in Figure 5.1.

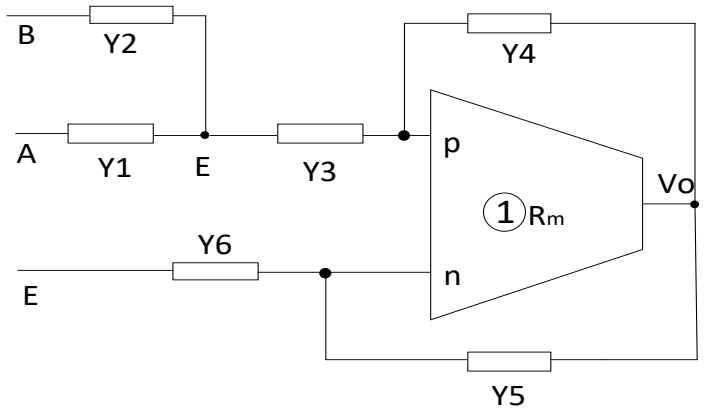


Figure 5.1. Generalized representation of forward path

Considering the node potentials of A, B, D and E to be V_1, V_2, V_3 and V_x respectively and performing routine analysis, the following equations are derived.

$$V_X Y_3 + V_o Y_4 = V_3 Y_6 + V_o Y_5 \tag{5.1}$$

$$V_1 Y_1 Y_3 + V_2 Y_2 Y_3 + V_o Y_4 \left(Y_1 + Y_2 + Y_3\right) = \left(V_3 Y_6 + V_o Y_5\right)\left(Y_1 + Y_2 + Y_3\right) \tag{5.2}$$

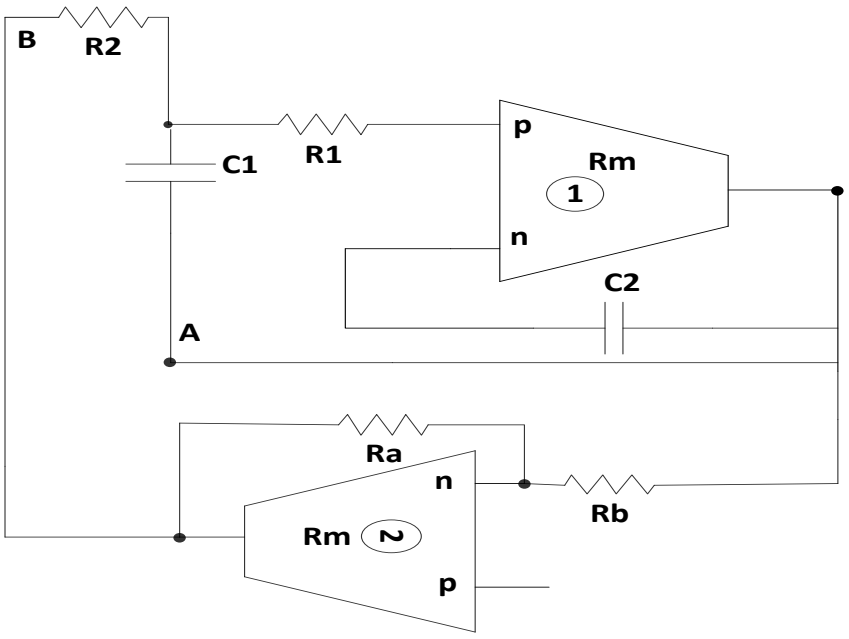
where Y_i represents the admittance. Suitable choice of admittances, results in the following cases:

Case. I. Considering $Y_4 = Y_6 = 0$, $Y_1 = sC_1$, $Y_2 = \frac{1}{R_2}$, $Y_3 = \frac{1}{R_1}$, $Y_5 = sC_2$; $V_1 = V_o$; (5.2)

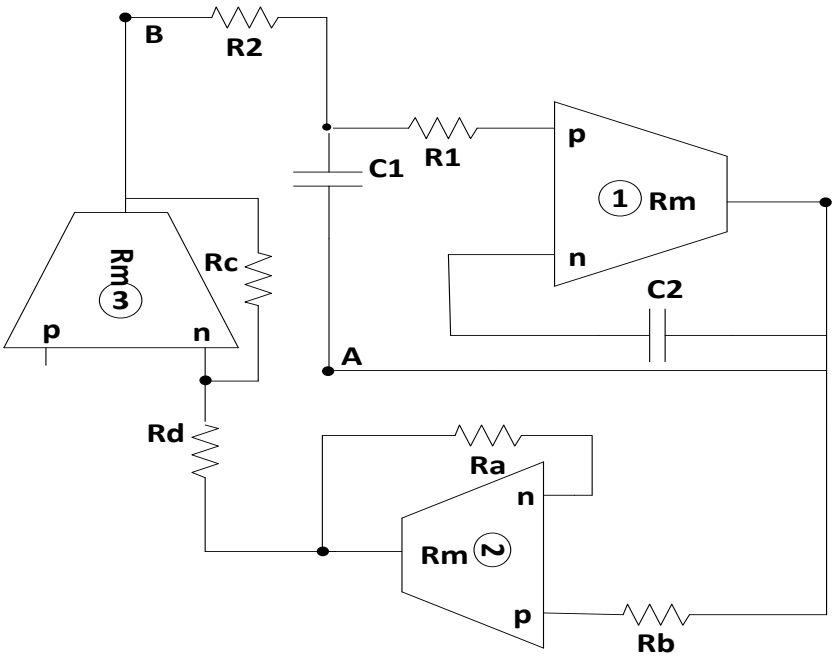
simplifies to

$$V_o\left(s^2 C_1 C_2 R_1 R_2 + s\{C_2\left[R_1 + R_2\right] - C_1 R_2\}\right) - V_2 = 0 \tag{5.3}$$

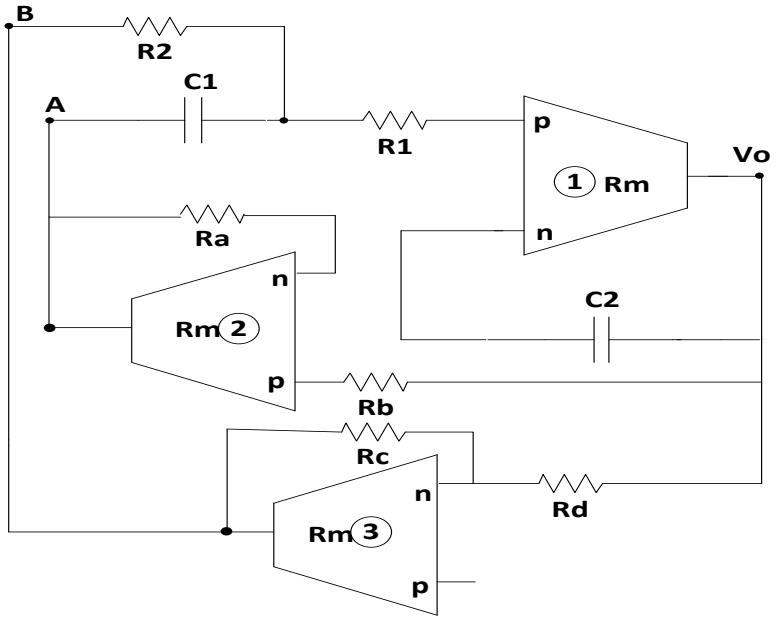
Examining (5.3), it is seen that by connecting an OTRA based inverting resistive gain stage characterized by $\left(-\frac{R_a}{R_b}\right)$ between output of OTRA1 and node B results in new SO



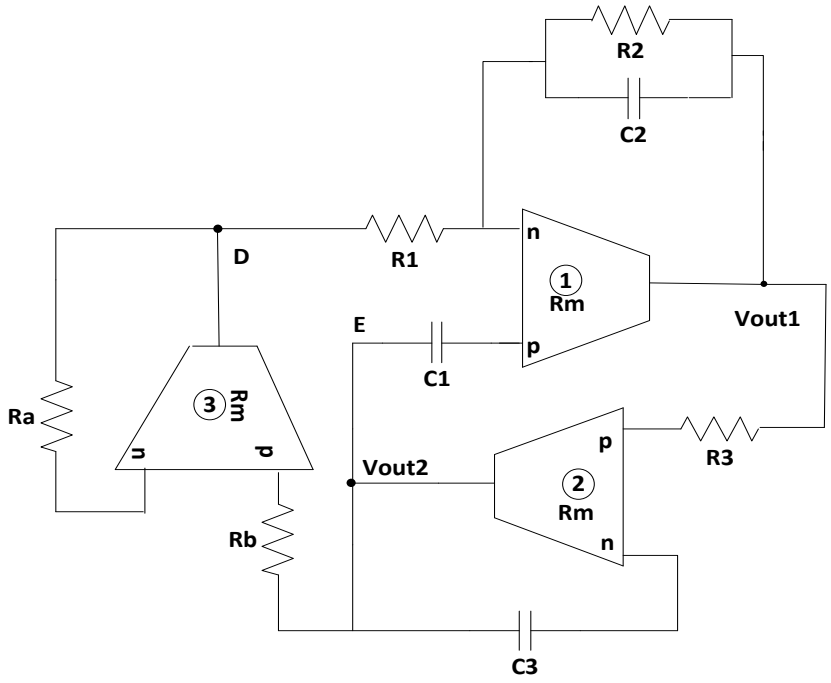
(a)


B
R2
C1
R1
p
1
Rm
n
C2
Rm
3
Rc
p
n
A
Rd
Ra
n
Rm
2
p
Rb

(b)


B
R2
C1
A
R1
p
1
Rm
Vo
n
Ra
n
C2
Rm
2
p
Rb
Rc
n
Rd
Rm
3
p

(c)



(d)

Figure 5.2. Proposed sinusoidal configurations

depicted in Figure 5.2 (a). Its CE may be expressed as

$$s^2 C_1 C_2 R_1 R_2 + s\{C_2[R_1 + R_2] - C_1 R_2\} + \frac{R_a}{R_b} = 0 \tag{5.4}$$

The corresponding FO and CO are given by

$$\text{FO:} \quad f_o = \frac{\sqrt{k}}{2\pi\sqrt{C_1 C_2 R_1 R_2}}; \text{ where } k = \frac{R_a}{R_b} \tag{5.5}$$

$$\text{CO:} C_2[R_1 + R_2] = C_1 R_2 \tag{5.6}$$

Case. II. With component and node settings similar to the case I and introducing a cascade connection of inverting and non-inverting resistive gain stages (characterized by $-\frac{R_c}{R_d}$, $\frac{R_a}{R_b}$ respectively) in feedback as shown in Figure 5.2 (b) a new SO topology may be obtained and its CE is given as

$$\left(s^2 C_1 C_2 R_1 R_2 + s\left\{C_2[R_1 + R_2] - C_1 R_2\right\}\right) + \frac{R_a}{R_b}\frac{R_c}{R_d} = 0 \tag{5.7}$$

The FO and CO are obtained as

$$\text{FO:}\quad f_o = \frac{\sqrt{k}}{2\pi\sqrt{C_1C_2R_1R_2}};\ \text{where}\ k = \frac{R_a}{R_b}\frac{R_c}{R_d} \tag{5.8}$$

$$\text{CO: } C_2\left[R_1 + R_2\right] = C_1R_2 \tag{5.9}$$

by taking R_a and R_c equal, the proposed SO provides linear FO tunability.

Case. III. Using component and node settings similar to the case I and connecting OTRA based inverting and non-inverting resistive gain stages in feedback as shown in Figure 5.2 (c), a new SO topology can be obtained and its CE is expressed as

$$s^2C_1C_2R_1R_2 + sC_2\left[R_1 + R_2\right] - sC_1R_2\frac{R_a}{R_b} + \frac{R_c}{R_d} = 0 \tag{5.10}$$

The FO and CO are obtained as

$$\text{FO:}\quad f_o = \frac{\sqrt{k}}{2\pi\sqrt{C_1C_2R_1R_2}};\ \text{where}\ k = \frac{R_c}{R_d} \tag{5.11}$$

$$\text{CO: } C_2\left[R_1 + R_2\right] = C_1R_2\frac{R_a}{R_b} \tag{5.12}$$

From (5.11) and (5.12), it may be observed that the topology of Figure 5.2 (c) enjoys completely uncoupled tuning between FO and CO.

Case. IV. With $Y_1 = Y_2 = Y_4 = 0$, $Y_3 = sC_1$, $Y_4 = \frac{1}{R_3}$, $Y_5 = \frac{1}{R_2} + sC_2$, $Y_6 = \frac{1}{R_1}$; (5.1) minimizes to

$$V_oR_1\left(1 + sC_2R_2\right) + V_3R_2 - V_3\left(sC_1R_1R_2\right) = 0 \tag{5.13}$$

New SO, can be obtained by connecting OTRA based noninverting integrator and noninverting gain stages (characterized by $\frac{1}{sC_3R_3}, \frac{R_a}{R_b}$ respectively) as shown in Figure 5.2 (d) and its CE is given by

$$s^2 C_2 C_3 R_2 R_3 + s\{C_3 R_3 - C_1 R_2\} + \frac{R_a}{R_b}\frac{R_2}{R_1} = 0 \tag{5.14}$$

The FO and CO are obtained as

$$\text{FO: } f_o = \frac{\sqrt{k}}{2\pi\sqrt{C_2 C_3 R_1 R_3}};\ \text{where } k = \frac{R_a}{R_b} \tag{5.15}$$

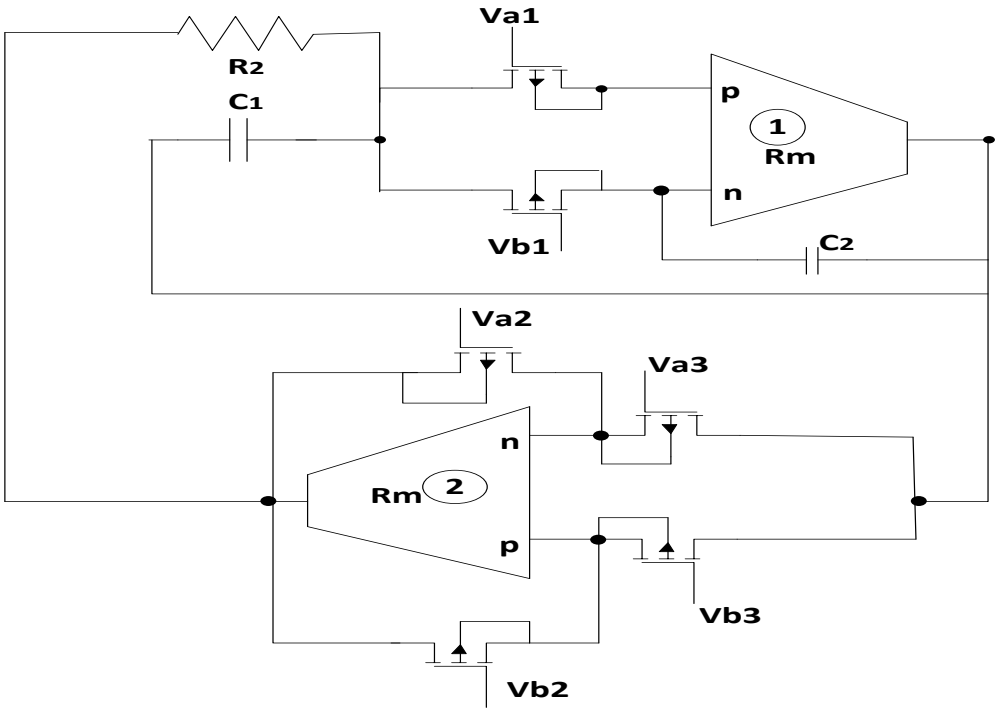
$$\text{CO: } C_3 R_3 = C_1 R_2 \tag{5.16}$$

This structure also provides quadrature outputs.

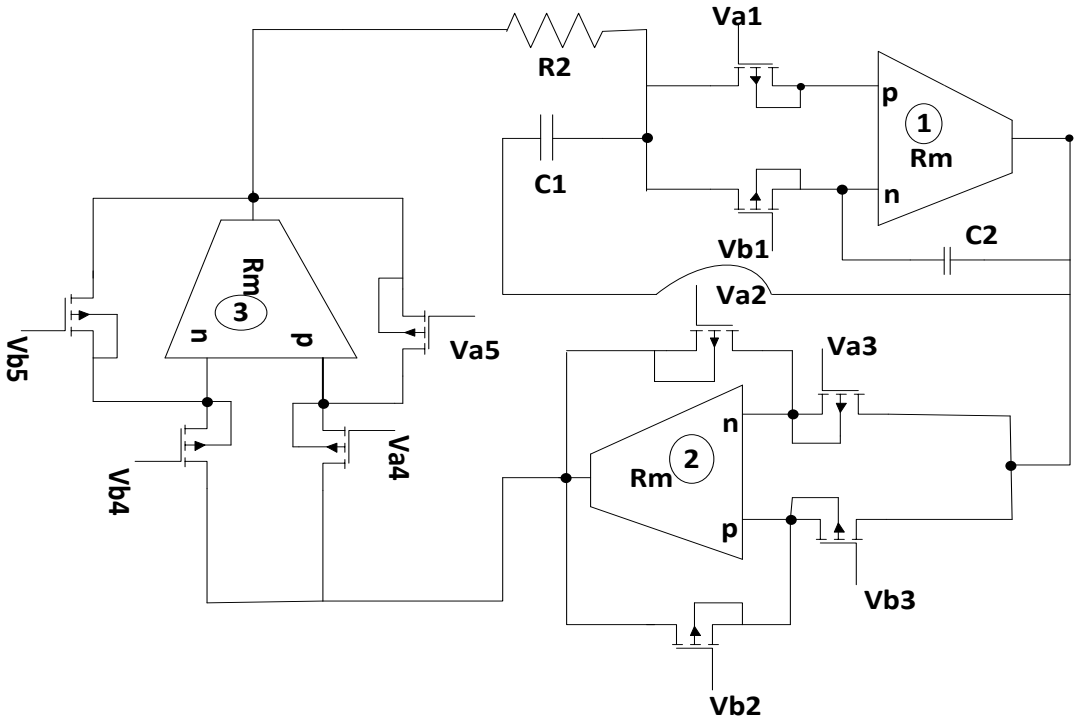
From FO and CO expressions of all the proposed topologies, it is clear that all the circuits provide independent tuning of FO by distinct resistors without affecting CO. Therefore all the circuits enjoy orthogonal tuning. Further, Figure 5.2 (c) enjoys completely independent tuning between FO and CO without affecting each other. Furthermore, it is interesting to note that the scaling factors in the numerator of FO of proposed circuits are not part of CO, unlike topologies in [76], [78], [166], [212]-[214] thereby making frequency scaling simpler.

5.2.1 MOS Resistor based Implementation

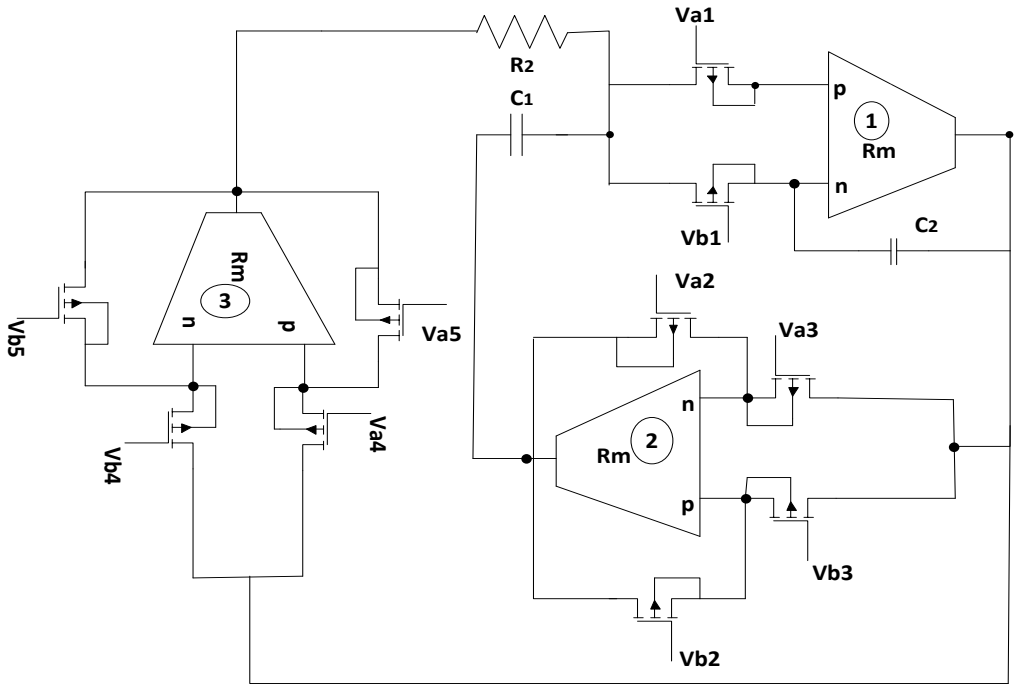
A thorough inspection of the circuits of Figure 5.2 reveals that all the resistances which are involved in the tuning of FO and CO can be realized using MOSFETS, thereby making topologies electronically tunable. The proposed circuits with MOS based resistor realization are depicted in Figure 5.3. It is worth notify that the SO of Figure 5.2 (d) is completely MOS-C realizable.


Va1
R2
C1
p
1
Rm
n
Vb1
C2
Va2
Va3
n
Rm
2
p
Vb3
Vb2

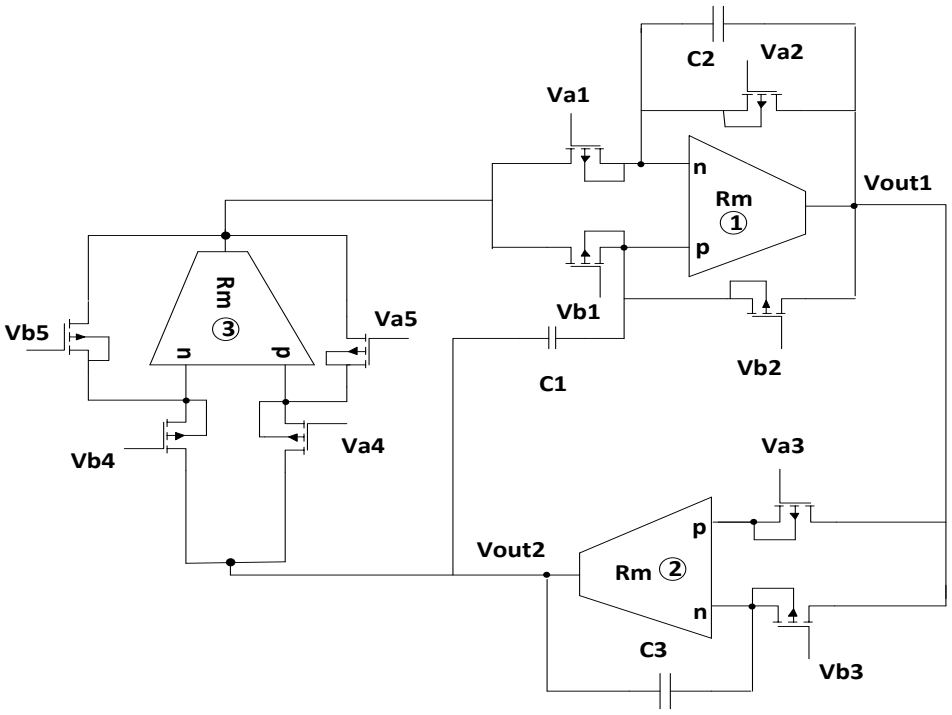
(a)


Va1
R2
p
1
Rm
C1
n
C2
Vb1
Va2
Rm
3
n
p
Va5
Va3
Vb5
n
2
Rm
Va4
p
Vb4
Vb3
Vb2

(b)



(c)



(d)

Figure 5.3. (a)-(d) Electronically tunable realizations of proposed SOs

5.2.2 Nonideal Analysis

Considering the nonidealities of OTRA, the proposed circuits are reanalyzed and the modified CE for Figure 5.2 (a) may be expressed as

$$s^2C_1(C_2+C_p)R_1R_2+s\left\{(C_2+C_p)\left[R_1+R_2\right]-C_1R_2\right\}+\frac{R_a}{R_b}\varepsilon_1(s)=0 \tag{5.17}$$

where $\varepsilon_1(s)=\dfrac{1}{\left\{1+sC_pR_a\right\}}$

Resulting FO and CO respectively are represented as

$$\text{FO: } \hat{f}_o=\frac{\sqrt{k_n}}{2\pi\sqrt{C_1(C_2+C_p)R_1R_2}};\text{where } k_n=\frac{R_a}{R_b}\varepsilon_1(s) \tag{5.18}$$

$$\text{CO: } (C_2+C_p)\left[R_1+R_2\right]=C_1R_2 \tag{5.19}$$

The modified CE for Figure 5.2 (b) may be expressed as

$$s^2C_1(C_2+C_p)R_1R_2+s\left\{(C_2+C_p)\left[R_1+R_2\right]-C_1R_2\right\}+\frac{R_c}{R_d}\frac{R_a}{R_b}\varepsilon_1(s)\ \varepsilon_2(s)=0 \tag{5.20}$$

where $\varepsilon_1(s)=\dfrac{1}{\left\{1+sC_pR_c\right\}}$, $\varepsilon_2(s)=\dfrac{1}{\left\{1+sC_pR_a\right\}}$

Resulting FO and CO respectively are given by

$$\text{FO: } \hat{f}_o=\frac{\sqrt{|k_n|}}{2\pi\sqrt{C_1(C_2+C_p)R_1R_2}};\ \text{where } k_n=\frac{R_a}{R_b}\frac{R_c}{R_d}\varepsilon_1(s)\varepsilon_2(s) \tag{5.21}$$

$$\text{CO: } (C_2+C_p)\left[R_1+R_2\right]=C_1R_2 \tag{5.22}$$

The modified CE for Figure 5.2 (c) may be expressed as

$$s^2C_1(C_2+C_p)R_1R_2+s\left\{(C_2+C_p)(R_1+R_2)-C_1R_2\frac{R_a}{R_b}\varepsilon_2(s)\right\}+\frac{R_c}{R_d}\varepsilon_1(s)=0 \tag{5.23}$$

where $\varepsilon_1(s)=\dfrac{1}{\left\{1+sC_pR_c\right\}}$, $\varepsilon_2(s)=\dfrac{1}{\left\{1+sC_pR_a\right\}}$

From (5.23) the FO and CO are given respectively as

$$\text{FO: } \hat{f}_o = \frac{\sqrt{k_n}}{2\pi\sqrt{C_1(C_2+C_p)R_1R_2}};\ \text{ where } k_n = \frac{R_c}{R_d}\varepsilon_1(s) \tag{5.24}$$

$$\text{CO: } (C_2+C_p)\left[R_1+R_2\right] = C_1R_2\frac{R_a}{R_b}\varepsilon_2(s) \tag{5.25}$$

The modified CE for Figure 5.2 (d) may be expressed as

$$s^2(C_2+C_p)(C_3+C_p)R_2R_3 + s\left\{(C_3+C_p)R_3 - C_1R_2\right\} + \frac{R_a}{R_b}\frac{R_2}{R_1}\varepsilon_1(s) = 0 \tag{5.26}$$

where $\varepsilon_1(s) = \dfrac{1}{\left\{1+sC_pR_a\right\}}$

The modified FO and CO are expressed as

$$\text{FO: } \hat{f}_o = \frac{\sqrt{k_n}}{2\pi\sqrt{(C_2+C_p)(C_3+C_p)R_1R_3}};\ \text{where } k_n = \frac{R_a}{R_b}\varepsilon_1(s) \tag{5.27}$$

$$\text{CO: } (C_3+C_p)R_3 = C_1R_2 \tag{5.28}$$

It is clear from the above quoted analysis that FO and CO are altered in the presence of nonidealities. Therefore, the compensation method must be applied for high-frequency applications to account for the errors $\varepsilon_1(s), \varepsilon_2(s)$ introduced in FOs. Additionally, the COs for all four topologies also get modified.

The complete passive compensation for the topology of Figure 5.3 (a) may be achieved by connecting single capacitor C_x between *p* terminal and output of OTRA-2 as shown in Figure 5.4(a). For the topologies of Figure 5.3 (b) and (c) C_x should be connected between *p* terminal and output of OTRA-3 and *p* terminal and output of OTRA-2 as shown in Figure 5.4 (b) and (c) respectively. For the SO shown in Figure 5.3 (d) passive

compensation may be achieved by connecting single capacitor C_x between *p* terminal and output of OTRA-2 as depicted in Figure 5.4 (d).

The CE of Figure 5.4 (a) may then be written as

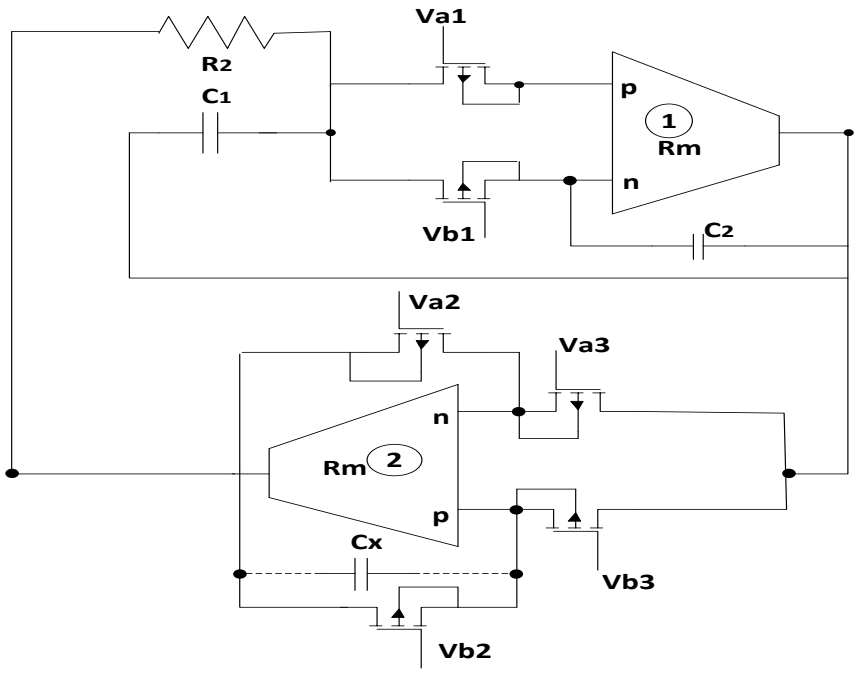
$$s^2C_1(C_2+C_p)R_1R_2+s\left\{(C_2+C_p)\left[R_1+R_2\right]-C_1R_2\right\}+\frac{R_a}{R_b}\varepsilon_{1n}(s)=0 \tag{5.29}$$

where $\varepsilon_{1n}(s)=\dfrac{1}{\left\{1+s(C_p-C_X)R_a\right\}}$,

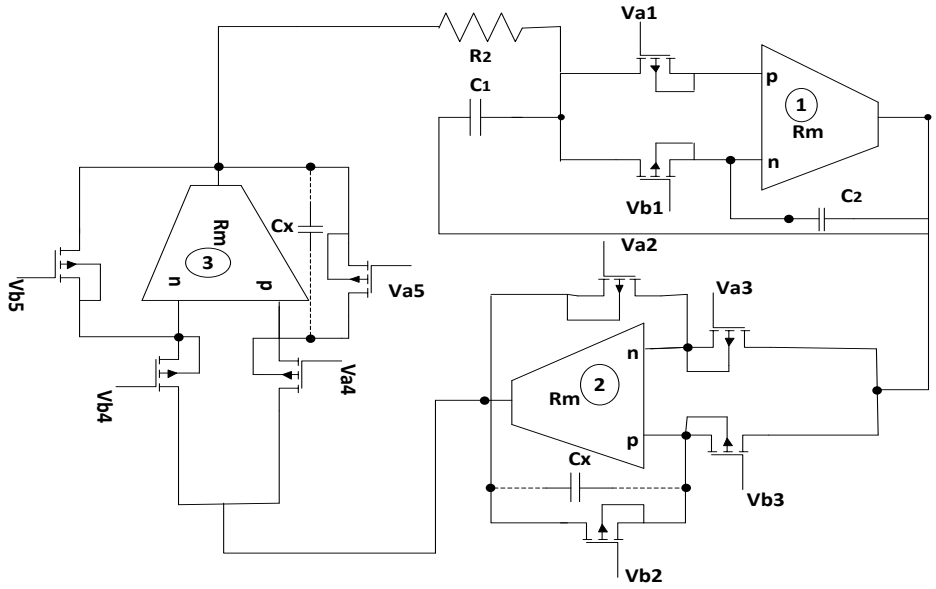
The CE of Figure 5.4 (b) may then be written as

$$s^2C_1(C_2+C_p)R_1R_2+s\left\{(C_2+C_p)\left[R_1+R_2\right]-C_1R_2\right\}+\frac{R_c}{R_d}\frac{R_a}{R_b}\varepsilon_{1n}(s)\ \varepsilon_{2n}(s)=0 \tag{5.30}$$

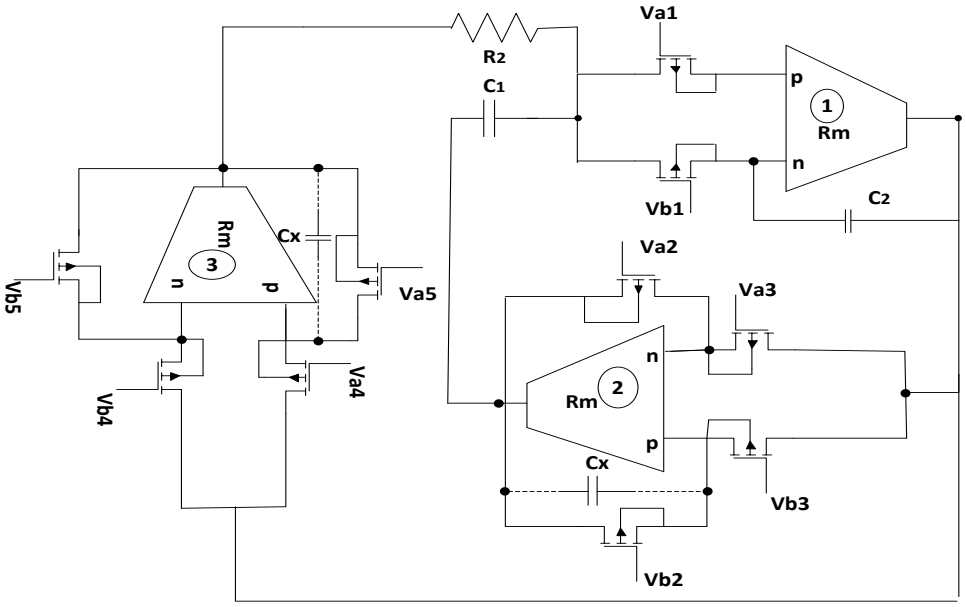
where $\varepsilon_{1n}(s)=\dfrac{1}{\left\{1+s(C_p-C_X)R_a\right\}}$, $\varepsilon_{2n}(s)=\dfrac{1}{\left\{1+s(C_p-C_X)R_c\right\}}$



(a)


Va1
R2
C1
p
1
Rm
n
Vb1
C2
Va2
Va3
Rm
3
n
p
Cx
Va5
Vb5
Va4
Vb4
n
Rm
2
p
Cx
Vb3
Vb2

(b)


Va1
R2
C1
p
1
Rm
n
Vb1
C2
Va2
Va3
Rm
3
n
p
Cx
Va5
Vb5
Va4
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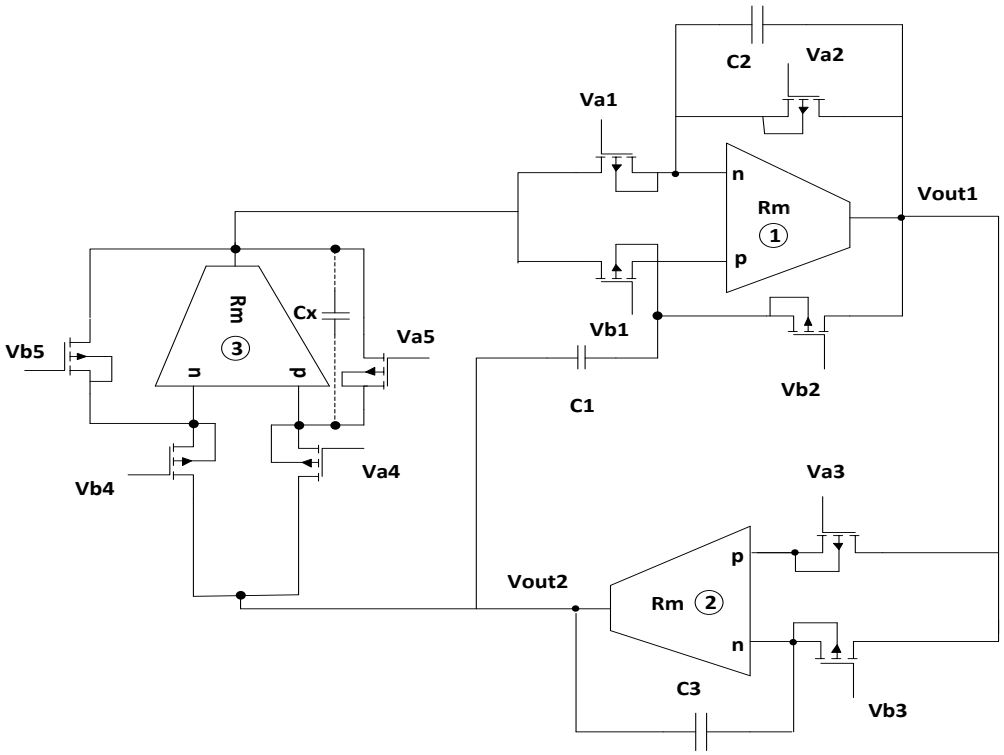
Rm
2
p
Cx
Vb3
Vb2

(c)



(d)

Figure 5.4. (a)-(d) Passive compensated proposed SOs

Figure 5.4 (c) represents the passive compensated topology of Figure 5.3 (c) and the CE for the same is given by

$$s^2C_1(C_2+C_p)R_1R_2+s\left\{(C_2+C_p)\left[R_1+R_2\right]-C_1R_2\frac{R_a}{R_b}\varepsilon_{2n}(s)\right\}+\frac{R_c}{R_d}\varepsilon_{1n}(s)=0 \tag{5.31}$$

where $\varepsilon_{1n}(s)=\dfrac{1}{\left\{1+s(C_p-C_X)R_c\right\}}$, $\varepsilon_{2n}(s)=\dfrac{1}{\left\{1+s(C_p-C_X)R_a\right\}}$

The passive compensation of Figure 5.3 (d) is depicted in Figure 5.4 (d) which leads to a CE of

$$s^2(C_2+C_p)(C_3+C_p)R_1R_3+s\left\{(C_3+C_p)R_3-C_1R_2\right\}+\frac{R_a}{R_b}\frac{R_2}{R_1}\varepsilon_{1n}(s)=0 \tag{5.32}$$

where $\varepsilon_{1n}(s) = \dfrac{1}{\{1 + s(C_p - C_X)R_a\}}$

Equations (5.29) to (5.32) signify that by choosing the capacitor C_x equal to parasitic capacitance C_p, the error terms vanish, thereby nullifying the effect of C_p. Further, the effect of C_p appearing in other terms can be eliminated by pre adjusting the value of capacitor C_2 in (5.29)-(5.32) and C_3 in (5.32) thus achieving self-compensation.

5.2.3 Sensitivity Analysis

The sensitivity analysis for the proposed oscillators is carried out and sensitivities of f_o for all configurations with respect to various circuit parameters are listed in Table 5.1.

Table 5.1. Sensitivity calculations for proposed circuits

Ckt.No	$S_Y^{f_o}$
Figure 5.2 (a)	$\left\|S_{R_1}^{f_o}\right\| = \left\|S_{R_2}^{f_o}\right\| = \left\|S_{C_1}^{f_o}\right\| = \left\|S_{C_2}^{f_o}\right\| = \left\|S_k^{f_o}\right\| = \frac{1}{2};\ \left\|\hat{S}_{C_p}^{f_o}\right\| = \frac{C_p}{2(C_2 + C_p)}$
Figure 5.2 (b)	$\left\|S_{R_1}^{f_o}\right\| = \left\|S_{R_2}^{f_o}\right\| = \left\|S_{C_1}^{f_o}\right\| = \left\|S_{C_2}^{f_o}\right\| = \left\|S_k^{f_o}\right\| = \frac{1}{2};\ \left\|\hat{S}_{C_p}^{f_o}\right\| = \frac{C_p}{2(C_2 + C_p)}$
Figure 5.2 (c)	$\left\|S_{R_1}^{f_o}\right\| = \left\|S_{R_2}^{f_o}\right\| = \left\|S_{C_1}^{f_o}\right\| = \left\|S_{C_2}^{f_o}\right\| = \left\|S_k^{f_o}\right\| = \frac{1}{2};\ \left\|\hat{S}_{C_p}^{f_o}\right\| = \frac{C_p}{2(C_2 + C_p)}$
Figure 5.2 (d)	$S_{R_1}^{f_o} = S_{R_3}^{f_o} = S_k^{f_o} = \left\|S_{C_2}^{f_o}\right\| = \left\|S_{C_3}^{f_o}\right\| = \frac{1}{2};\ S_{R_2}^{f_o} = S_{C_1}^{f_o} = 0;\ \left\|\hat{S}_{C_p}^{f_o}\right\| = \frac{C_p}{2(C_2 + C_p)(C_3 + C_p)}$

The frequency f_o and sensitivity ($S_k^{f_0}$) variation with respect to k for all proposed topologies has been depicted in Figure 5.5. The sensitivity $\left|S_k^{f_0}\right|$ is fixed and is equal to 1/2, for the entire frequency range for all configurations.

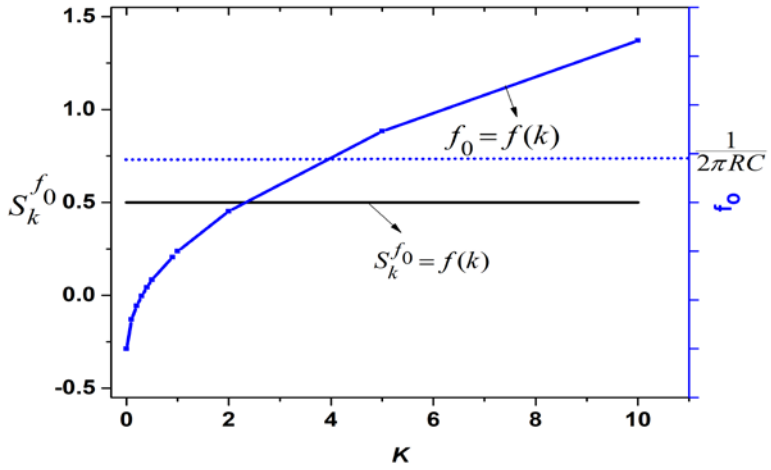


Figure 5.5. f_0 and $S_k^{f_0}$ as a function of k for proposed topologies

5.2.4 Frequency Stability

The frequency stability factors are derived for all proposed topologies for the chosen condition setting, as shown in Table 5.2. Inspection of Table 5.2 suggests that the high S^F values can be achieved by selecting larger value of scaling factor (n) for all the circuits. Therefore, proposed oscillators offer excellent frequency stability.

Table 5.2. Frequency stability factors for proposed topologies

Circuit	Condition	S^F
Figure 5.2 (a)	C_1=2C, C_2=C and R_1=R_2=R_a= R, R_b= R/n	$-\sqrt{2n}$
Figure 5.2 (b)	C_1=2C, C_2=C and R_1=R_2=R_b=R_c=R_a=R, R_d= R/n	$-\sqrt{2n}$
Figure 5.2 (c)	C_1=C_2=C and R_1=R_2= R_b=R_c=R, R_a=2R,R_d= R/n	$-\sqrt{n}$
Figure 5.2 (d)	C_1=C_2=C_3=C and R_1=R_2=R_3=R_a =R, R_b= R/n	$-2\sqrt{n}$

5.2.5 Phase Noise Analysis

The open loop transfer function $H_1(s)$ and $H_2(s)$ of the oscillator circuits of Figure 5.2 (a) and (b) respectively are given as

$$H_1(s) = \frac{sC_1R_2}{s^2C_1C_2R_1R_2 + sC_2(R_1+R_2) + \frac{R_a}{R_b}} \tag{5.33}$$

$$H_2(s) = \frac{sC_1R_2}{s^2C_1C_2R_1R_2 + sC_2(R_1+R_2) + \frac{R_aR_c}{R_bR_d}} \tag{5.34}$$

For $\omega \approx \omega_o, A \approx 1,$ the $H_1(s)$ and $H_2(s)$ given by (5.33) and (5.34) can be expressed in terms of magnitude and phase as

$$H_i(\omega) = A_i(\omega).e^{j(\varphi_i\omega)} \tag{5.35}$$

Substituting CO and FO of the corresponding circuits in (5.33) and (5.34) the magnitude $A_i(\omega)$ can be written as

$$\left|A_1(\omega)\right| = \frac{\left(\frac{\omega}{\omega_o}\right)\sqrt{\frac{C_1R_2R_b}{C_2R_1R_a}}}{\sqrt{\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + \left(\frac{\omega}{\omega_o}\right)^2\frac{C_1R_2R_b}{C_2R_1R_a}}} \tag{5.36}$$

$$\left|A_2(\omega)\right| = \frac{\left(\frac{\omega}{\omega_o}\right)\sqrt{\frac{C_1R_2}{C_2R_1}\frac{R_aR_c}{R_bR_d}}}{\sqrt{\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + \left(\frac{\omega}{\omega_o}\right)^2\frac{C_1R_2}{C_2R_1}\frac{R_aR_c}{R_bR_d}}} \tag{5.37}$$

The $\left|\frac{dA_i}{d\omega}\right|$ for i= 1, 2 may be obtained as

$$\left|\frac{dA_i}{d\omega}\right| = C_2R_1 \tag{5.38}$$

The phase of $H_i(j\omega)$ can be written as

$$\angle H_1(j\omega) = \varphi_1 = -tan^{-1}\left(\sqrt{\frac{C_1R_2R_b}{C_2R_1R_a}}\left\{\left(\frac{\omega}{\omega_o}\right)-\left(\frac{\omega}{\omega_o}\right)^{-1}\right\}\right) \tag{5.39}$$

$$\angle H_2(j\omega) = \varphi_2 = -tan^{-1}\left(\sqrt{\frac{C_1R_2}{C_2R_1}\frac{R_aR_c}{R_bR_d}}\left\{\left(\frac{\omega}{\omega_o}\right)-\left(\frac{\omega}{\omega_o}\right)^{-1}\right\}\right) \tag{5.40}$$

Now the $\left|\frac{d\varphi_i}{d\omega}\right|$ for i= 1, 2 can be expressed as

$$\left|\frac{d\varphi_i}{d\omega}\right| = 2C_2R_1 \tag{5.41}$$

The openloop transfer function $H_3(s)$ of the oscillator circuit in Figure 5.2 (c) is given as

$$H_3(s) = \frac{sC_1R_2\frac{R_a}{R_b}}{s^2C_1C_2R_1R_2 + sC_2\left(R_1+R_2\right)+\frac{R_c}{R_d}} \tag{5.42}$$

Substituting the CO and FO in (5.42) the magnitude of $A_3(\omega)$ can be written as

$$\left|A_3(\omega)\right| = \frac{\left(\frac{\omega}{\omega_o}\right)\frac{1}{\omega_o}\frac{R_a}{C_2R_1R_b}}{\sqrt{\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2+\left(\left(\frac{\omega}{\omega_o}\right)\frac{1}{\omega_o}\frac{R_a}{C_2R_1R_b}\right)^2}} \tag{5.43}$$

Further $\left|\frac{dA_3}{d\omega}\right|$ is computed as

$$\left|\frac{dA_3}{d\omega}\right| = \frac{R_a}{C_2R_1R_b}\frac{1}{\omega_o^2} \tag{5.44}$$

the phase of $H(j\omega)$ can be written as

$$\angle H_3(j\omega) = \varphi_3 = -tan^{-1}\left(\left(\frac{\omega}{\omega_o}\right)\frac{\omega_o R_b}{R_a}C_2R_1 - \left(\frac{\omega}{\omega_o}\right)^{-1}\frac{\omega_o R_b}{R_a}C_2R_1\right) \tag{5.45}$$

Differentiation of (5.45) results in

$$\left|\frac{d\varphi_4}{d\omega}\right| = \frac{R_b}{R_a}C_2R_1 \tag{5.46}$$

The openloop transfer function $H_4(s)$ of the oscillator circuit in Figure 5.2 (d) is given as

$$H_4(s) = \frac{sC_1R_2 - \dfrac{R_2R_a}{R_1R_b}}{s^2C_3C_2R_2R_3 + sC_3R_3} \tag{5.47}$$

Substituting the CO and FO in (5.47) the magnitude of $A_4(\omega)$ can be written as

$$\left|A_4(\omega)\right| = \sqrt{\frac{\left(\frac{R_a}{R_b}\right)^2 + \left(\frac{\omega}{\omega_o}\right)^2\left(\frac{R_a}{R_b}\right)}{\left(\frac{\omega}{\omega_o}\right)^2\left(\frac{R_a}{R_b}\right) + \left(\frac{\omega}{\omega_o}\right)^4\left(\frac{R_a}{R_b}\right)^2}} \tag{5.48}$$

The $\left|\frac{dA_4}{d\omega}\right|$ can be expressed as

$$\left|\frac{dA_4}{d\omega}\right| = \frac{2}{\omega_o\left(1+\frac{R_b}{R_a}\right)} \tag{5.49}$$

The phase of $H(j\omega)$ can be written as

$$\angle H_4(j\omega) = \varphi_4 = -tan^{-1}\left(\left(\frac{\omega}{\omega_o}\right)^{-1}\sqrt{\frac{R_b}{R_a}}\right) - Tan^{-1}\left(\left(\frac{\omega}{\omega_o}\right)\sqrt{\frac{R_b}{R_a}}\right) \tag{5.50}$$

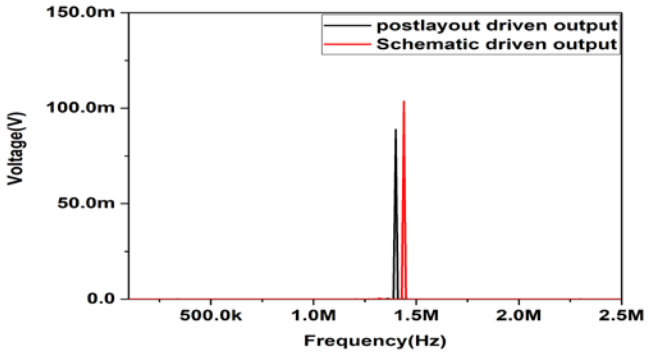
From (5.50) $\left|\frac{d\varphi_4}{d\omega}\right|$ results in

$$\left|\frac{d\varphi_4}{d\omega}\right| = \frac{2}{\omega_o}\frac{\sqrt{\frac{R_b}{R_a}}}{\left(1+\frac{R_b}{R_a}\right)} \tag{5.51}$$

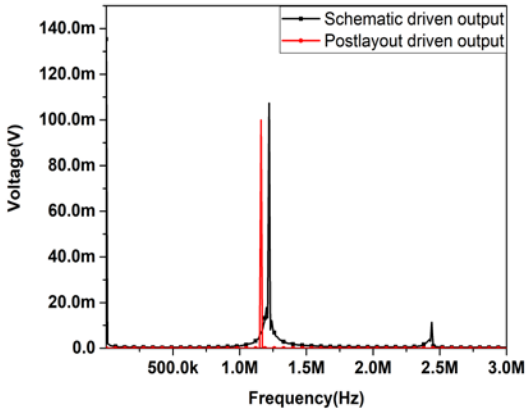
The inspection of the above-quoted equations indicates that proposed topologies of Figure 5.2 (a), (b) and (c) are independent of the frequency of oscillation (ω_o). Hence the frequency stability of these topologies can be mentioned high by keeping product RC high. On the other hand, the frequency stability of topology presented in Figure 5.2 (d) decreases at higher frequencies with an increase in ω_o due to phase noise.

5.3 Simulation Results

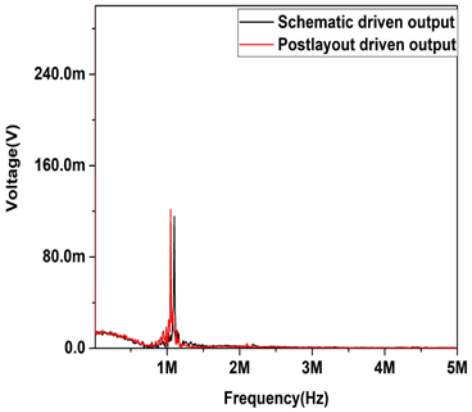
To validate the theoretical propositions schematic and post lay out driven simulations are carried out using the Cadence Virtuoso ADE spectre tool. For proposed topologies, the layouts and corresponding pre, post-layout transient outputs for chosen passive component values are shown in Table 5.3. The layout implemented is verified by physical verification checks [190], [215] such as DRC, LVS and RC parasitic extraction. Due to the inclusion of parasitics, the post layout simulated frequencies are slightly decreased compared to simulated frequencies. The discrepancies between pre and post layout simulation frequencies are found to be less than 5% for all oscillators. Therefore, all the topologies have been found to work in corroboration with theoretical propositions. The THDs of proposed configurations are observed to be less than 3.5%. The frequency spectrums of configurations of Figures 5.2 (a)-(d) are shown in Figure 5.6 (a)-(d), respectively. The graph between V_{out1} versus V_{out2} for proposed QO (Figure 5.2 (d)) is shown in Figure 5.6 (e), respectively.



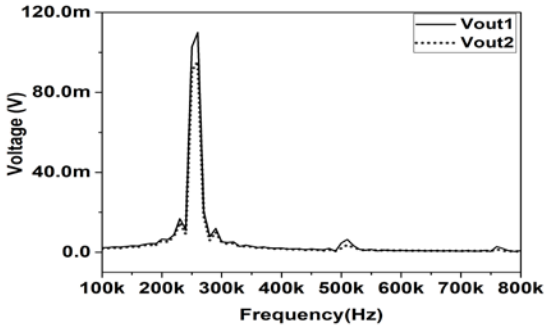
(a)



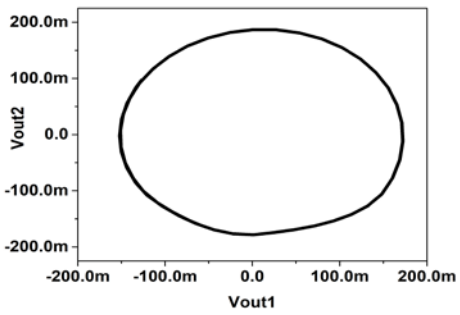
(b)



(c)



(d)



(e)

Figure 5.6. (a)-(d) FFT spectrums of Figure 5.2 (a)-(d) and (e) Vout1 versus Vout2 graph for proposed QO (Figure 5.2 (d))

Table 5.3. Pre and Post layout results

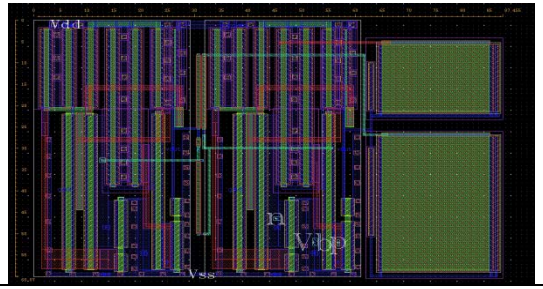
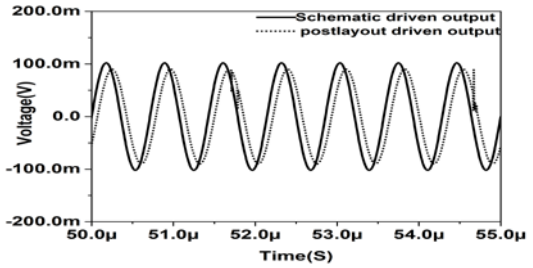
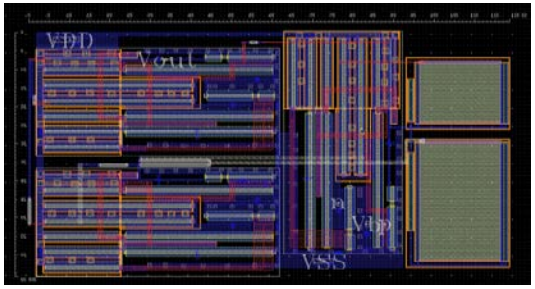
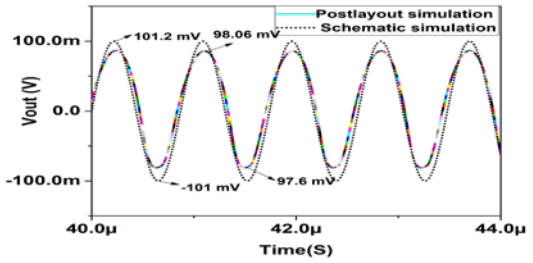
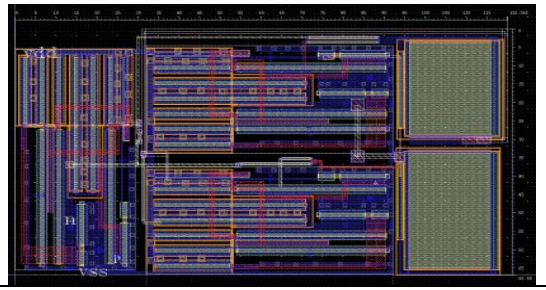
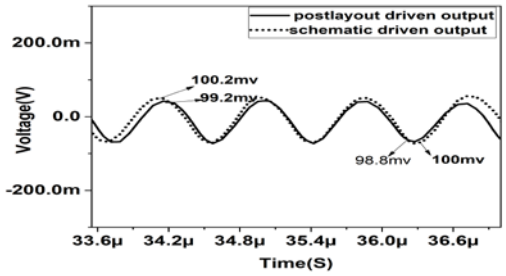
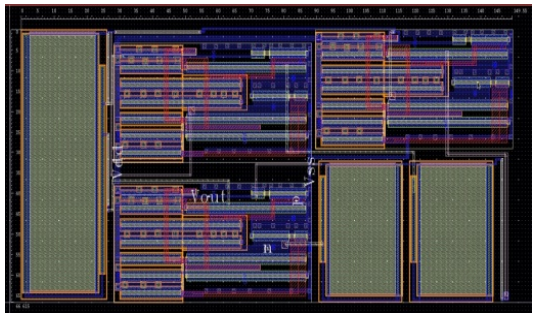
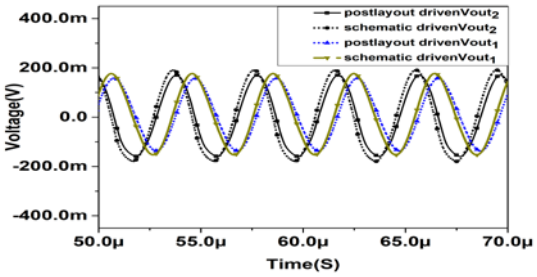
Figure 5.2 (a)	$R_1=R_2=R_b=10k\Omega, R_a=1k\Omega, C_1$ = 5pF, C_2=2.5pF/ FO:1.42MHz	5253.4218 μm^2 (87.45µmx 60.07µm). 	
Figure 5.2 (b)	$R_1=R_2=10k\Omega, R_a=R_c=1k\Omega, R_b=R_d=4k\Omega, C_1=5pF, C_2=2.5pF$/ FO:1.12 MHz.	7805.7891 μm^2 (118.62µmx 65.805µm) 	
Figure 5.2 (c)	$C_1=5pF, C_2=4pF, R_1=R_2=10k\Omega, R_c=1k\Omega, R_d=10k\Omega$/ FO:1.12 MHz	8029.9472 μm^2 (120.06µmx 66.88µm) 	

Figure 5.2 (d)	$C_1=C_3=5pF, C_1=10pF, R_1=15k\Omega, R_3=10k\Omega R_a=20k\Omega, R_b=0.4k\Omega$/ FO:260 KHz	9962.2732 μm^2 (149.55µmx 66.615µm) 	

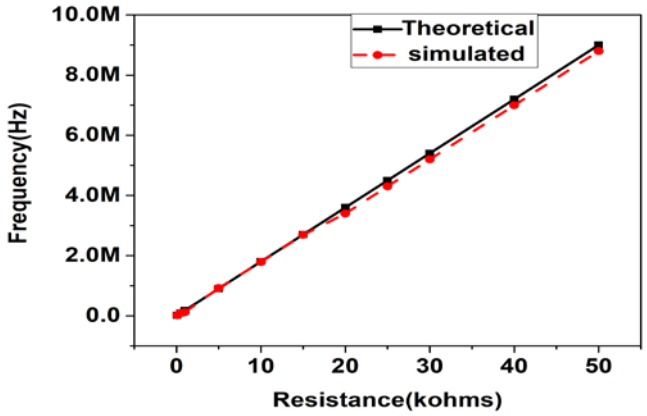
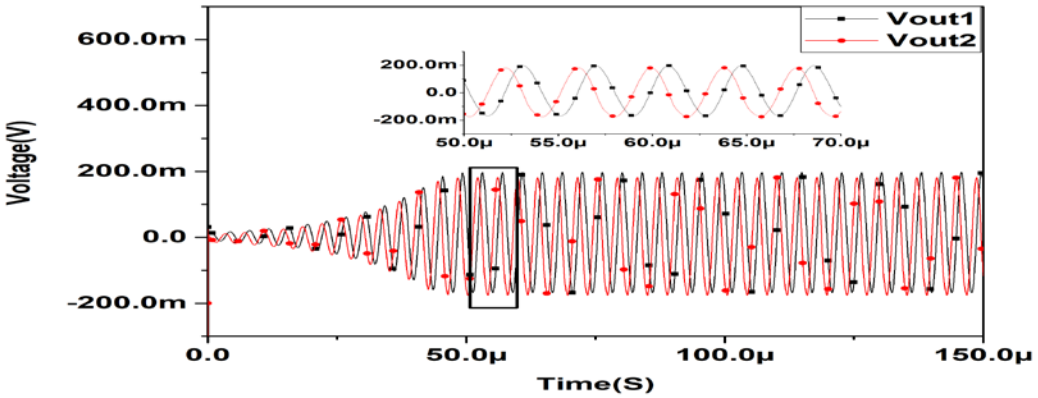


Figure 5.7. Variation of FO with R for SO of Figure 5.2 (b)

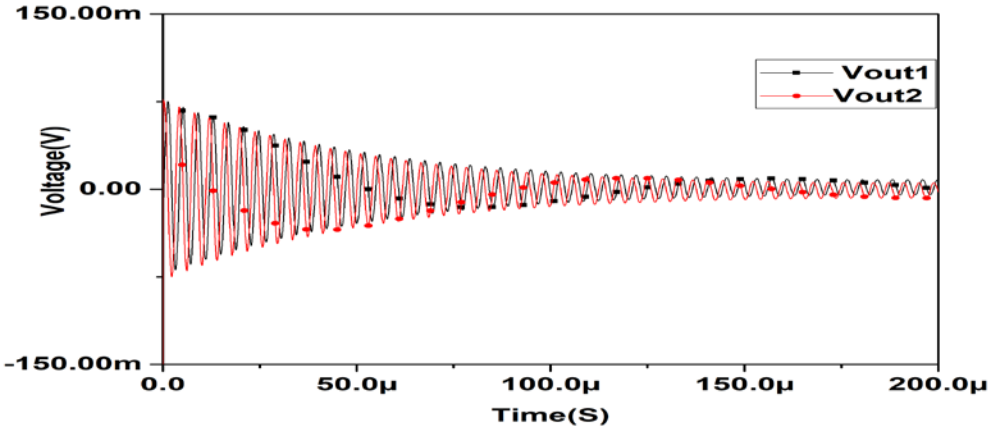
To validate the linear variability of FO with R_a= R_c= R (say) for Figure 5.2 (b), R is varied from 0.1 kΩ to 50 kΩ while remaining resistance and capacitance values are chosen as R_1= R_2= 10 kΩ, R_a= R_c= R, R_b= R_d= 25 kΩ and C_1= 5 pF, C_2= 2.5 pF. The corresponding graph is depicted in Figure 5.7, which confirms the linear relation between FO and R. The maximum THD was observed to be 2.4%.

Further, to demonstrate the electronic tunability of the proposed SOs, the topology of Figure 5.3 (d) was chosen wherein the resistors R_a, R_b, R_c and R_d are realized using MOS transistors. According to the technology node used for simulation, the parameter values are: μ_n = 327.37 Cm^2/ V.s.; gate oxide thickness T_{ox}= 4 x 10^{-9} m, channel width offset (WINT) and channel length offset (LINT) = 0.01µm. Therefore, C_{ox} is calculated as 8.65 x 10^{-3} F/m^2. In simulations, we assumed W_{drawn} as 3.6 µm and L_{drawn} as 0.72 µm. To realize R ≈ 10 kΩ, (≈ 1 kΩ), the gate controlling voltages V_{ai}, V_{bi} (where i= 1, 2) are adjusted, so that (V_{ai} -V_{bi}) is equal to 0.073 V, (0.73 V).

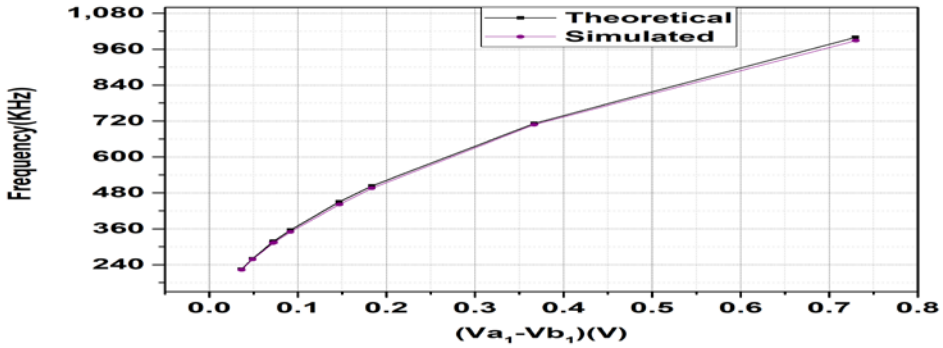
The growth and sustained oscillations of Figure 5.3 (d) at 260 KHz are illustrated in Figure 5.8 (a) and the decaying oscillations are depicted in Figure 5.8 (b). Further, Figure 5.8 (c) depicts the tuning of FO by varying resistor R_1 by altering gate controlling voltages V_{a1} and V_{b1}.



(a)



(b)



(c)

Figure 5.8. Simulated output waveforms at 260 KHz for proposed SO (Figure 5.3 (d)) (a) growing oscillations (b) decay of oscillations (c) variation of FO with R_1 by changing (V_{a1}-V_{b1}).

To assess the oscillator post-fabrication performances, PVT is carried out for all the topologies. For brevity, only the results obtained for Figure 5.2 (b) are shown. Figure 5.9 (a) shows the effect of different process corners (SS, SF, TT, FS, FF) on the output waveform, whereas, Figure 5.9 (b) and (c) represent output sinusoidal waveforms in the presence of supply voltage variations (±2.5%, ±5%), temperature variations (-20^{o} C to 100^{o} C), respectively. It may be seen from Figure 5.9 that no abrupt change in the output in the presence of PVT variations is observed. Similar PVT analysis is accomplished for remaining topologies also and good quality of sine waves have been obtained.

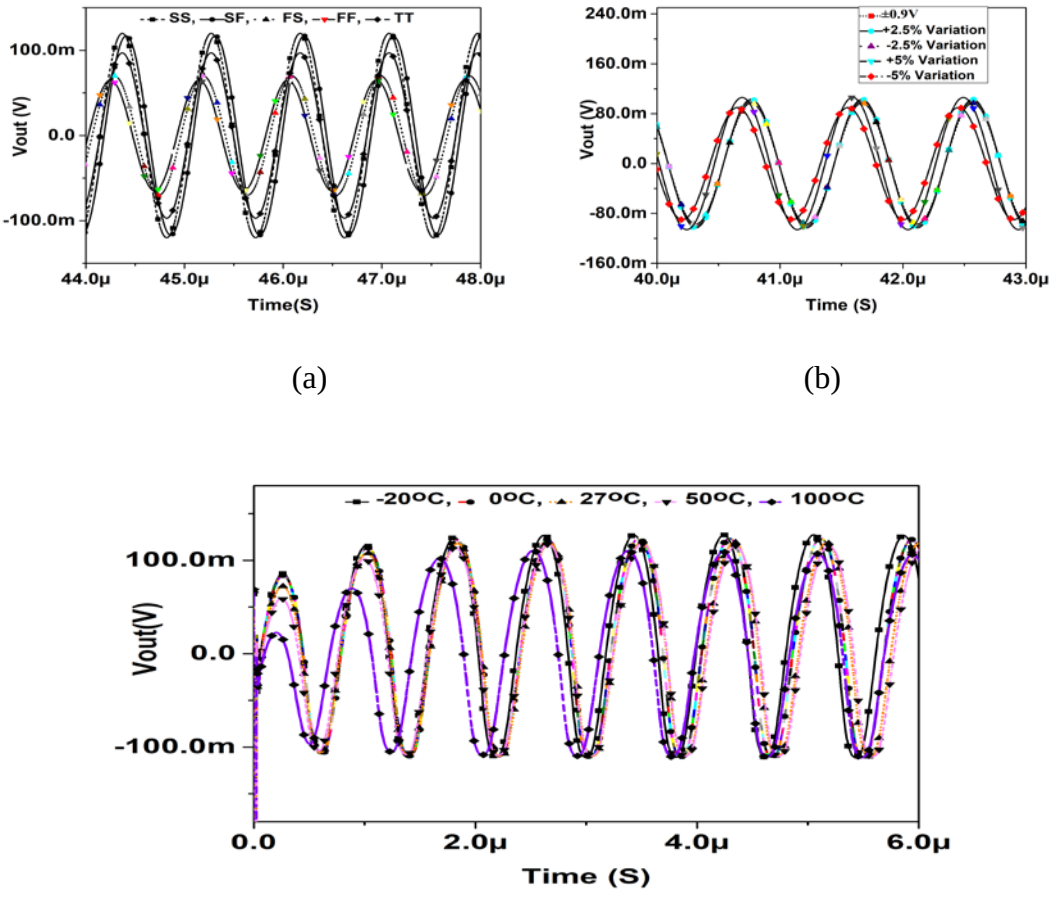
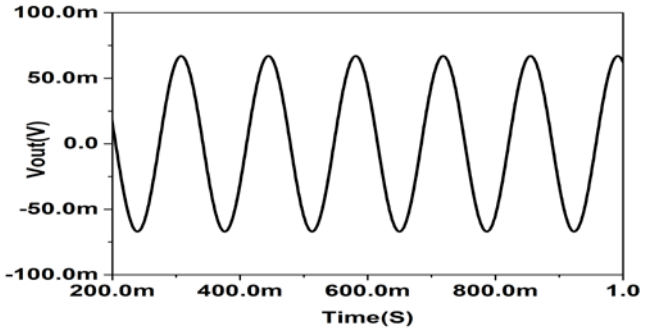
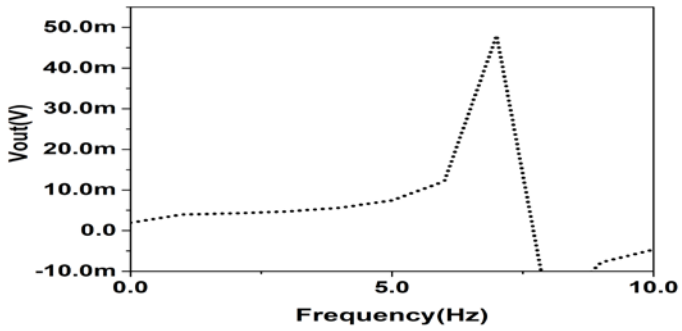


Figure 5.9. Output waveforms of PVT analysis corresponding to (a) process variations (b) supply voltage Variations, (c) variations in temperature.

To operate the proposed circuit (Figure 5.2 (b)) in VLF mode the passive component values are chosen as C_1= 300 pF, C_2= 150 pF and R_1= R_2= R_b= R_d= 100 kΩ, R_a= R_c= 0.1 kΩ. The frequency of the generated waveform is 7.31 Hz as against the calculated value of 7.5Hz. The resultant transient response and frequency spectrum are shown in Figure 5.10 (a) and (b), respectively. The THD is found to be less than 2.5%.



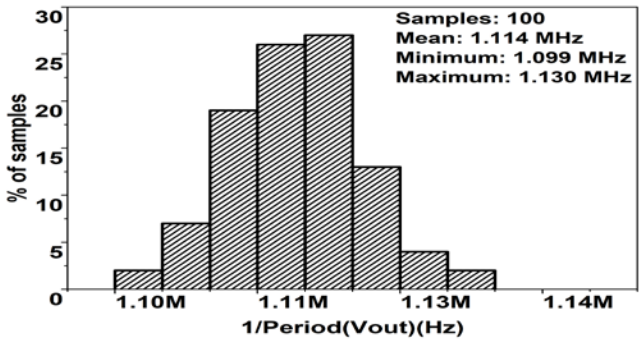
(a)



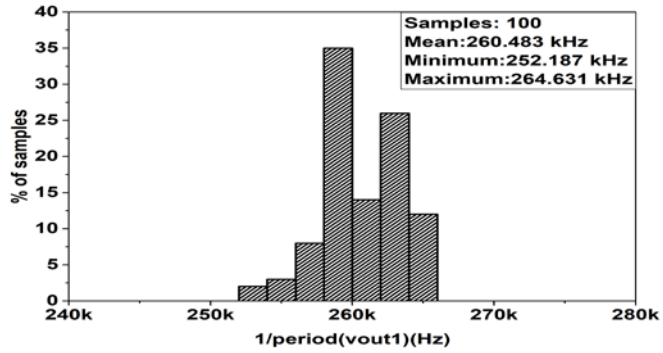
(b)

Figure 5.10. (a) Simulated transient waveform, (b) FFT spectrum

The robustness of the proposed circuits is tested by performing Monte Carlo simulations by considering Gaussian distribution for a hundred runs. For brevity results corresponding to (Figure 5.2 (c), (d)) only are shown. The runs are carried out with a nominal tolerance of 3% in R_1 and R_a/R_b, respectively. The FO for Figure 5.2 (c) is set at 1.12 MHz and that for Figure 5.2 (d) is considered as 260 KHz. Figure 5.11 shows the histogram of the Monte Carlo runs and it signifies that the circuits generate stable output in all iterations despite a change introduced in CO.



(a)



(b)

Figure 5.11. Histogram of the proposed circuits

for (a) Figure 5.2 (c); (b) Figure 5.2 (d)

5.4 Conclusion

This chapter introduces four new structures of electronically tunable SOs. Each of the proposed SO consists of forward path derived from a generic structure along with one/two OTRA based resistive gain stages or integrator in its feedback path. All the proposed SOs enjoy independent tuning of FO through resistors without affecting the CO. Further, all topologies are found to exhibit low f_o sensitivities at all frequencies with respect to circuit parameters. One of the topologies is capable of achieving VLF using less RC component spread and provides linear tuning too. One configuration provides quadrature outputs also. The schematic driven and post layout simulations, layout

designs are carried by the Cadence Virtuoso ADE spectre tool are included for verification of functionality of proposed structures. The PVT and Monte Carlo analyses are presented to estimate the mismatch after the fabrication process. Thus, the proposed circuits add to the present repertoire of OTRA based oscillators.

CHAPTER 6
OTRA BASED WIEN BRIDGE OSCILLATOR AND ITS HARMONIC ANALYSIS

The content and results of the following papers have been reported in this chapter

1. K. Gurumurthy, R. Pandey and N. Pandey, “Operational transresistance amplifier based Wien bridge oscillator and its Harmonic Analysis,” *Wireless personal communications*, vol. 108, no.1, 2019. Springer. **(SCI E) (IF: 1.2)**

6.1 Introduction

A wide variety of sinusoidal oscillators are available in the literature and Wien bridge oscillator is one among those which provides sinusoids with high linearity [215]. Traditionally, operational amplifiers are used to realize Wien bridge oscillator [51], [55]; however, their high-frequency operations are limited due to constant gain-bandwidth product and low slew rate [3]. A new OTRA based Wein bridge SO with wider tuning range is proposed in this chapter. A detailed harmonic distortion analysis is presented to ascertain the linearity of the proposed design.

6.2 Proposed Oscillator

The proposed circuit is shown in Figure 6.1, which is derived from traditional Wien bridge oscillator by replacing the opamp with OTRA based voltage controlled voltage source (VCVS). As the OTRA is a current-controlled voltage source, the combination of buffer and OTRA is used as a VCVS, which forms a forward path of gain K given by

$$K = \frac{R_4}{R_3} \tag{6.1}$$

The feedback factor H(*s*) involving two RC sections is expressed by

$$H(s) = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{6.2}$$

where $Z_1(s) = R_1 + \frac{1}{sC_1}$ and $Z_2(s) = R_2 \| \frac{1}{sC_2}$; Substituting the values of Z_1 and Z_2 in (6.2) the H(*s*) can be expressed as

$$\mathrm{H}(s) = \frac{sC_1R_2}{s^2C_1C_2R_1R_2 + s\left[C_1R_1 + C_2R_2 + C_1R_2\right] + 1} \tag{6.3}$$

The well-known Barkhausen criterion [48] for sustained oscillations can also be expressed in terms of the CE of the system as given

$$1 - KH(s) = 0 \tag{6.4}$$

Substituting (6.1) and (6.3) in (6.4) the CE of the circuit of Figure 6.1 may be obtained as

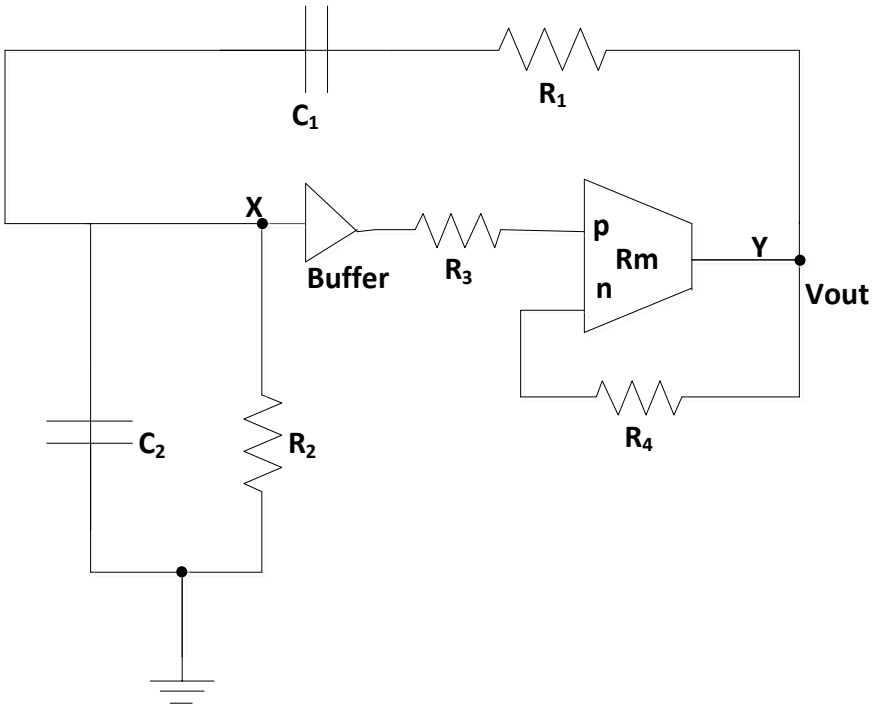


Figure 6.1. OTRA based Wien bridge Oscillator

$$s^2 C_1 C_2 R_1 R_2 + s\left[C_1 R_1 + C_2 R_2 + C_1 R_2 - \frac{C_1 R_2 R_4}{R_3} \right] + 1 = 0 \tag{6.5}$$

Considering $C_1 = C_2 = C$ and equating real and imaginary parts of (6.5) the CO and FO can be determined as

$$\text{CO: } \frac{R_2 R_4}{R_3} = \left(R_1 + 2R_2 \right); \text{ FO : } f_o = \frac{1}{2\pi C\sqrt{R_1 R_2}} \tag{6.6}$$

It is observed from (6.6) that both CO and FO can be adjusted independently, i.e. the FO can be tuned using C, whereas the CO can be adjusted through R_3 and R_4.

In this chapter, the OTRA and buffer are implemented using CFOA (AD844). The realization of OTRA using AD844 ICs has already been presented in section 2.4. The buffer can be realized, using CFOA as shown in Figure 6.2.

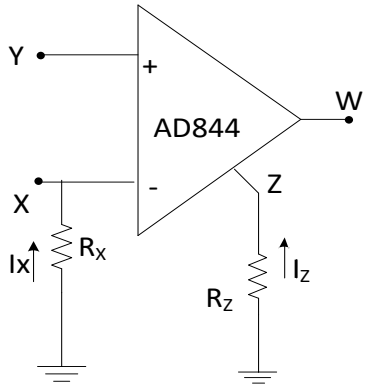


Figure 6.2. IC AD 844 based Buffer implementation

Using terminal characteristics of CFOA the I_x and I_z can be expressed as

$$I_X = -\frac{V_X}{R_X} = -\frac{V_Y}{R_X}; I_Z = -\frac{V_Z}{R_Z} \tag{6.7}$$

Therefore, $$\frac{V_Z}{R_Z} = \frac{V_Y}{R_X} \tag{6.8}$$

With $R_Z = R_X$, a combination of (6.7) and (6.8) gives

$$V_Z = V_Y \text{ and } V_W = V_Y \tag{6.9}$$

The voltage of V_Y, a high impedance terminal, is now available at a low impedance terminal W. Thus, the circuit of Figure 6.2 implements a buffer.

6.2.1 Nonideal Analysis

In the analysis of the proposed oscillator presented in section 6.2, the CFOA characteristics are considered to be ideal. However, in practice, the output of the oscillator may deviate due to the nonideal behaviour of CFOA. For analysing the nonideal behaviour the nonideal model of CFOA [206] is considered, which includes a

finite input resistance at X terminal, parasitic impedances $\left(R_y \| C_y\right)$ and $\left(R_z \| C_z\right)$ at Y and Z terminals, respectively.

The parasitic impedance at Y terminals of all CFOAs can be neglected as the Y terminal is grounded. Considering the nonidealities outlined above (6.5) modifies to (6.10).

$$\frac{sC_1R_2}{s^2C_1C_2R_1R_2+s\left[C_1R_1+C_2R_2+C_1R_2\right]+1}\frac{\left(R_X+R_{X3}\right)\left(1+sC_{Z3}R_{eq}\right)}{R_{eq}}\cdot \frac{R_{Z1}R_{Z2}R_4}{\left(R_3+R_{X2}\right)\left[R_{Z1}R_{Z2}-R_{X3}R_4\left(1+sC_{Z1}R_{Z1}\right)\left(1+sC_{Z2}R_{Z2}\right)+R_{Z1}R_{X3}\left(1+sC_{Z2}R_{Z2}\right)\right]}=1 \quad (6.10)$$

Where R_{Xi}, (R_{Zi}, C_{Zi}) represents X and Z terminal parasitic impedances of i^{th} CFOA.

$$R_{eq}=\frac{R_{Z3}R_Z}{R_{Z3}+R_Z}\approx R_Z \text{ as } R_{Z3}>>R_Z \quad (6.11)$$

$$\text{As } R_3>>R_{X2};\left(R_3+R_{X2}\right)\approx R_3 \text{ and } R_X>>R_{X3};R_X+R_{X3}\approx R_{X3}; \quad (6.12)$$

The proposed structure can be redrawn, as shown in Figure 6.3, with CFOA parasitic impedances.

Using approximations of (6.11) and (6.12) the (6.10) can be rewritten as

$$\frac{sC_1R_2}{s^2C_1C_2R_1R_2+s\left[C_1R_1+C_2R_2+C_1R_2\right]+1}\cdot\frac{R_X\left(1+sC_ZR_{eq}\right)}{R_X} \frac{R_{Z1}R_{Z2}R_4}{R_3\left[R_{Z1}R_{Z2}-R_{X3}R_4\left(1+sC_{Z1}R_{Z1}\right)\left(1+sC_{Z2}R_{Z2}\right)+R_{Z1}R_{X3}\left(1+sC_{Z2}R_{Z2}\right)\right]}=1 \quad (6.13)$$

Selecting the FO to be much smaller than $\frac{1}{C_{Z1}R_{Z1}}$ and $\frac{1}{C_{Z2}R_{Z2}}$ (6.13) reduces to (6.5) and therefore, expressions for FO and CO remain unaffected.

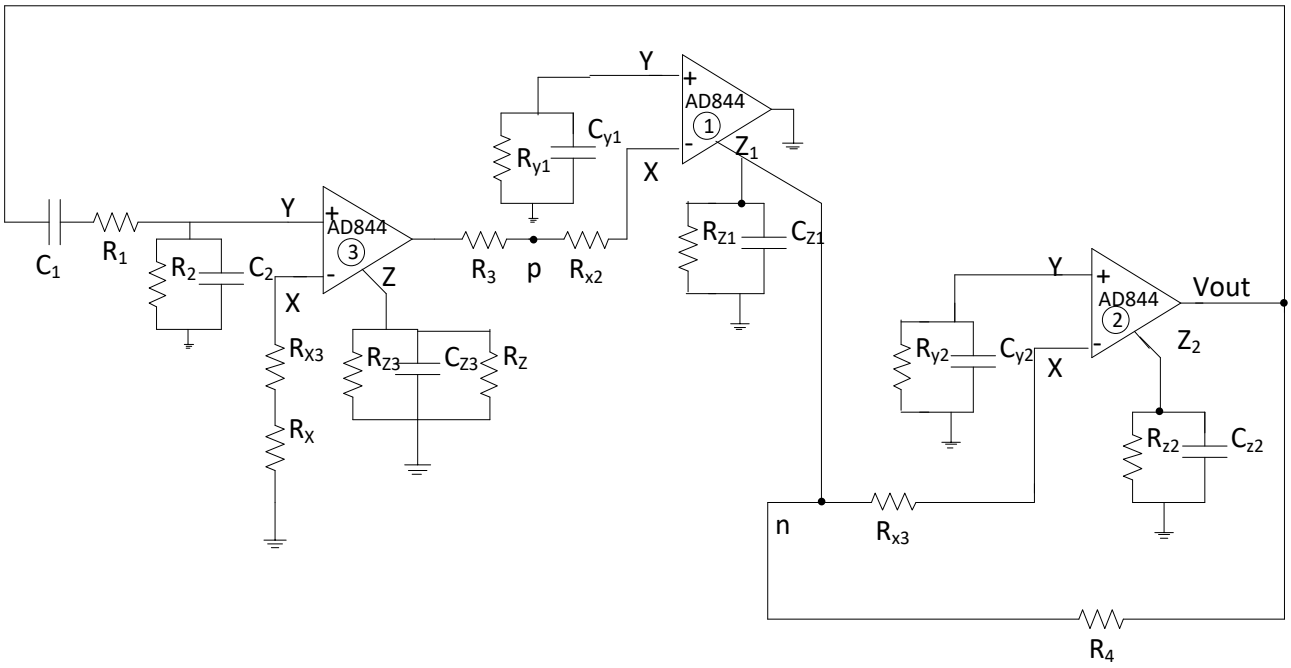


Figure 6.3. Proposed oscillator including Nonidealities

6.3 Harmonic Distortion Analysis

Harmonic distortion analysis is usually carried out to characterize the linearity performance of a circuit [216]. The low value of THD is always necessary to avoid the harmful effects such as the heating effect of electronic equipment etc. There are different methods and models discussed in the literature [215]-[222] to study the nonlinear behavior of the oscillator.

The HD analysis method given in [215] is based on separating the nonlinear function from the frequency-dependent linear transfer function for the computing of THD and the same has been adapted for the proposed circuit also. Being the most significant components, the second and third harmonics only are considered and the respective distortion factors, namely HD_2 and HD_3, are computed.

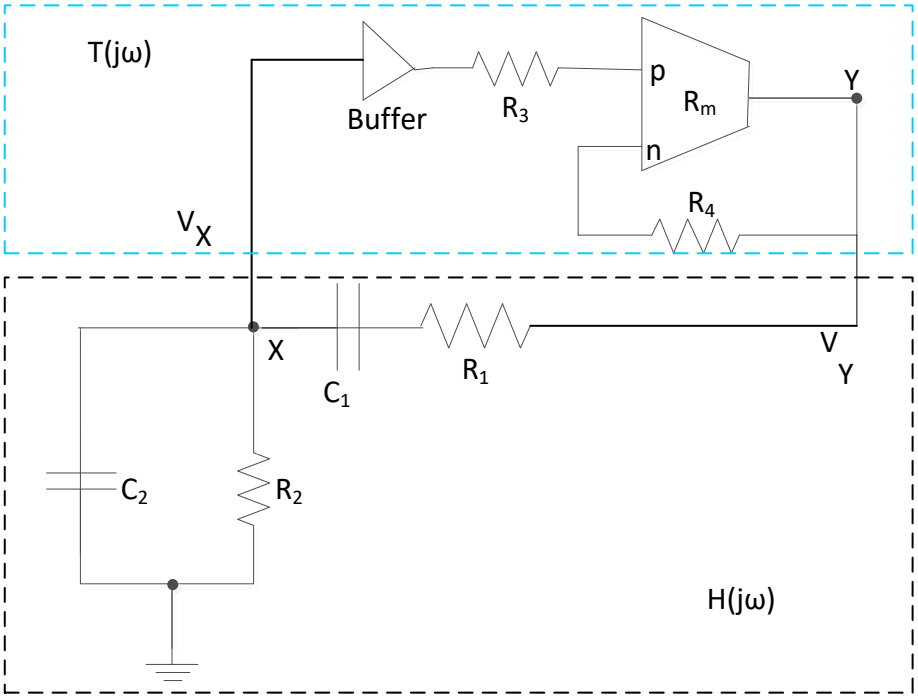


Figure 6.4. Generic block diagram representation of proposed circuit

The proposed circuit is redrawn in Figure 6.4 with the OTRA based VCVS in forward-path (transfer function T(jω)) and the passive network represented by H(jω) in the feedback path.

Considering only the first three harmonics the voltage at node X may be represented in phasor notation as

$$V_X(t) = \mathrm{Re}\left[V_{X1}e^{j\omega_o t} + V_{X2}e^{j2\omega_o t} + V_{X3}e^{j3\omega_o t}\right] \tag{6.14}$$

where

ω_o - oscillation frequency and

V_{Xi} - complex quantity with a magnitude as $|V_{Xi}|$ and phase as $\angle V_{Xi}$ with (i=1, 2, 3).

Assuming the fundamental component as the real number, the phase of second and third harmonics are computed with respect to fundamental. Taking nonlinearity of OTRA into account, the output at node Y is modeled as

$$V_Y = a_1(\omega_o)V_X + a_2(\omega_o)V_X^2 + a_3(\omega_o)V_X^3 \tag{6.15}$$

The coefficients a_i (i=1,2,3) can be frequency independent and their values are obtained by analyzing Fourier components of voltage V_Y. The corresponding calculations are presented below.

Considering the circuit of buffer and OTRA separating Z_1 and Z_2 from Figure 6.1(highlighted in blue dotted box) and assuming the input V_X as pure sinusoidal voltage with amplitude V_{X1} and frequency ω_o as given by

$$V_X = V_{X1}\cos(\omega_o t) \tag{6.16}$$

Then the output voltage V_Y of the circuit given by (6.15) can be rewritten as

$$V_Y = a_1(\omega_o)V_X + a_2(\omega_o)V_X^2 + a_3(\omega_o)V_X^3 \tag{6.17}$$

Substituting the expression of V_X into (6.17), we get

$$V_Y = \begin{cases} a_1(\omega_o)V_{X1}\cos(\omega_o t) + a_2(\omega_o)V_{X1}^2\left(\dfrac{1+\cos(2\omega_o t)}{2}\right) \\ +a_3(\omega_o)V_{X1}^3\left(\dfrac{\cos(3\omega_o t)+3\cos(\omega_o t)}{4}\right) \end{cases} \tag{6.18}$$

By neglecting the DC term [222] in (6.18) and considering frequency dependent terms V_{Y1}, V_{Y2} and V_{Y3} we get

$$\left.\begin{aligned} V_{Y1} &= a_1(\omega_o)V_{X1} + \frac{3}{4}a_3(\omega_o)V_{X1}^3 \\ V_{Y2} &= a_2(\omega_o)\frac{V_{X1}^2}{2} \\ V_{Y3} &= \frac{1}{4}a_3(\omega_o)V_{X1}^3 \end{aligned}\right\} \tag{6.19}$$

Equation (6.19) relates coefficients a_1, a_2 and a_3 to the magnitude of the harmonics of V_{Y1}, V_{Y2} and V_{Y3} as given by

$$a_1 = \frac{V_{Y1} - 3V_{Y3}}{V_{X1}}; a_2 = -\frac{V_{Y2}}{V_{X1}^2}; a_3 = 4\,\frac{V_{Y3}}{V_{X1}^3} \tag{6.20}$$

The components V_{Y1}, V_{Y2} and V_{Y3} are derived using the Fourier integral as given in (6.21).

$$V_{Yk} = \frac{1}{\pi}\int_0^{2\pi} V_Y(t) e^{jk\omega_o t} d(\omega_o t)\text{; where } k = 1, 2, 3; \tag{6.21}$$

Assuming signal distortion is due to the output voltage saturation mechanism, the Fourier integral is evaluated in three different regions, namely when $V_Y(t) < -V_{sat}$; $V_Y(t) \le -V_{sat}$ and $V_Y(t) > -V_{sat}$. The value of V_Y for these three different regions are $-V_{sat}$, $\left(\frac{R_4}{R_3} V_{X1}\cos(\omega_o t)\right)$ and V_{sat} respectively.

The values of a_1, a_2 and a_3 are computed as

$$a_1 = \frac{R_4}{R_3}\left[1 - \frac{2}{\pi}\arccos\frac{V_{sat}R_3}{V_{X1}R_4} + \frac{2}{\pi}\frac{V_{sat}R_3}{V_{X1}R_4}\left(3 - 2\left(\frac{V_{sat}R_3}{V_{X1}R_4}\right)^2\right)\sqrt{1 - \left(\frac{V_{sat}R_3}{V_{X1}R_4}\right)^2}\right] \tag{6.22}$$

$$a_2 = -\frac{4}{3\pi}\frac{R_4}{R_3}.\frac{2\frac{V_{sat}R_3}{V_{X1}R_4}.\left[1 - \left(\frac{V_{sat}R_3}{V_{X1}R_4}\right)^2\right]\sqrt{1 - \left(\frac{V_{sat}R_3}{V_{X1}R_4}\right)^2}}{V_{X1}} \tag{6.23}$$

$$a_3 = -\frac{16}{3\pi}\frac{R_4}{R_3}.\frac{\frac{V_{sat}R_3}{V_{X1}R_4}.\left[1 - \left(\frac{V_{sat}R_3}{V_{X1}R_4}\right)^2\right]\sqrt{1 - \left(\frac{V_{sat}R_3}{V_{X1}R_4}\right)^2}}{V_{X1}^2} \tag{6.24}$$

The voltage $V_Y(t)$ and $V_X(t)$ are related by

$$V_Y = V_X * H(j\omega) \tag{6.25}$$

where the operator * is used to compute the output of the forward block and the value of the function $H(j\omega)$ is to be computed at input signal frequency [218]-[219]. Substituting (6.14) into (6.15) for evaluation of product terms between the real part of the sum of phasors yields

$$V_Y(t) = \mathrm{Re}\left[V_{Y1} e^{j\omega_o t} + V_{Y2} e^{j2\omega_o t} + V_{Y3} e^{j3\omega_o t} \right] \tag{6.26}$$

where the terms up to third harmonics are retained and dc component and higher terms are neglected [219] The values of V_{Y1}, V_{Y2}, V_{Y3} are computed as

$$V_{Y1} = a_1(\omega_o)V_{X1} + \frac{3}{4}a_3(\omega_o)V_{X1}^3 \tag{6.27}$$

$$V_{Y2} = a_1(2\omega_o)V_{X2} + \frac{1}{2}a_2(\omega_o)V_{X1}^2 + \frac{3}{2}a_3(\omega_o)V_{X1}^2 V_{X2} \tag{6.28}$$

$$V_{Y3} = a_1(3\omega_o)V_{X3} + a_2(\omega_o)V_{X1}V_{X3} + \frac{1}{4}a_3(\omega_o)V_{X1}^3 \tag{6.29}$$

The voltage V_X of the linear section may be obtained by retracing feedback path and its value is given by

$$V_X(t) = \mathrm{Re}\left[V_{Y1} e^{j\omega_o t} H(j\omega_o) + V_{Y2} e^{j2\omega_o t} H(2j\omega_o) + V_{Y3} e^{j3\omega_o t} H(3j\omega_o) \right] \tag{6.30}$$

The, V_{X1}, V_{X2} and V_{X3} may be evaluated by substituting (6.27)-(6.29) in (6.30) and comparing the resulting expression with (6.14). Thus, V_{X1} is given as

$$V_{X1} = \left[a_1(\omega_o)V_{X1} + \frac{3}{4}a_3(\omega_o)V_{X1}^3 \right] H(j\omega_o) \tag{6.31}$$

$$= \left[V_{X1} + \frac{3}{4}\frac{a_3}{a_1} V_{X1}^3 \right] a_1 H(j\omega_o)$$

where $a_1 H(j\omega_o)$ is the loop gain of the linearized system at $\omega = \omega_o$. Simplification of (6.31) gives

$$V_{X1} = 2\sqrt{\frac{\frac{1}{H(j\omega_o)} - a_1}{3a_3}} \tag{6.32}$$

Substituting $s = j\omega$ in (6.3), the value of $H(j\omega)$ at $\omega = \omega_o$ maybe expressed as

$$H(j\omega)\Big|_{\omega = \omega_o} = \frac{1}{1+u+v} \quad \text{where } u = \frac{R_1}{R_2};\ v = \frac{C_1}{C_2}$$

Similarly V_{X2} is obtained as

$$V_{X2} = \left[a_1(2\omega_o) V_{X2} + \frac{1}{2} a_2(\omega_o) V_{X1}^2 + \frac{3}{2} a_3(\omega_o) V_{X1}^2 V_{X2} \right] H(j2\omega_o) \tag{6.33}$$

Solving (6.33) yield

$$V_{X2} = \frac{1}{2}\frac{a_2}{a_1} \frac{a_1 H(j2\omega_o)}{1 - \left(1 + \frac{3}{2}\frac{a_3}{a_1} V_{X1}^2\right) a_1 H(j2\omega_o)} V_{X1}^2 \tag{6.34}$$

where
$$H(2j\omega_o) = \frac{1}{-3 + j\sqrt{\frac{v}{u}}(1+u+1/v)} \tag{6.35}$$

Finally, V_{X3} is computed as

$$V_{X3} = \left[a_1(3\omega_o) V_{X3} + a_2(\omega_o) V_{X1} V_{X3} + \frac{1}{4} a_3(\omega_o) V_{X1}^3 \right] H(j3\omega_o) \tag{6.36}$$

$$\text{or } V_{X3} = \frac{1}{4}\frac{a_3}{a_1} \frac{a_1 H(j3\omega_o)}{1 - a_1 H(j3\omega_o)} \left[1 + \frac{2a_2^2}{a_1 a_3} \frac{a_1 H(j2\omega_o)}{1 - \left(1 + \frac{3}{2}\frac{a_3}{a_1} V_{X1}^2\right) a_1 H(j2\omega_o)} \right] V_{X1}^3 \tag{6.37}$$

The term $\frac{a_1 H(j3\omega_o)}{1-a_1 H(j3\omega_o)}$ can be evaluated and is given by

$$\frac{a_1 H(j3\omega_o)}{1-a_1 H(j3\omega_o)} = \frac{j3a_1\sqrt{\frac{v}{u}}}{-8+j3\sqrt{\frac{v}{u}}\left(1+u+\frac{1}{v}a_1\right)} \tag{6.38}$$

By considering (6.32), (6.34) and (6.37), HD_2 and HD_3 are evaluated as

$$HD_2 = 20\log\left|\frac{V_{X2}}{V_{X1}}\right| = 20\log\frac{|a_2|V_{X1}}{\sqrt{9u\left(\frac{3}{4}a_3V_{X1}^2+a_1-1-u\right)+\left(\frac{-9}{4}a_3V_{X1}^2-9a_1\right)^2}} \tag{6.39}$$

$$HD_3 = \begin{cases} \left|\frac{V_{X3}}{V_{X1}}\right| = 20\log\frac{\frac{3}{4}|a_3|V_{X1}^2}{\sqrt{64u\left(\frac{3}{4}a_3V_{X1}^2+a_1-1-u\right)+\frac{81}{16}a_3^2V_{X1}^4}}. \\ \sqrt{\frac{9u\left(\frac{3}{4}a_3V_{X1}^2+a_1-1-u\right)+\left(\frac{-9}{4}a_3V_{X1}^2-9a_1+\frac{a_2^2}{a_3}\right)^2}{9u\left(\frac{3}{4}a_3V_{X1}^2+a_1-1-u\right)+\left(\frac{-9}{4}a_3V_{X1}^2-a_1\right)^2}} \end{cases} \tag{6.40}$$

The minimum values of HD_2 and HD_3 can be obtained by choosing optimum u value, which may be determined by differentiating (6.39) and (6.40) with respect to u. The optimal value of u is computed as

$$u_{opt} = \frac{3}{8}a_3V_{X1}^2 + \frac{1}{2}(a_1-1) \tag{6.41}$$

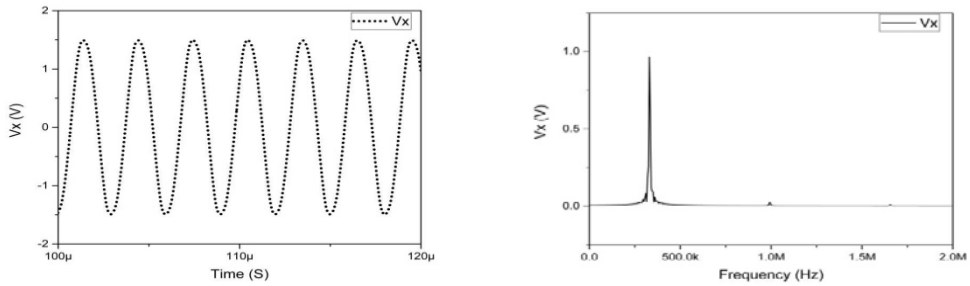
The values of HD_2 and HD_3 depend on V_{X1}(amplitude); coefficients a_1, a_2, a_3 and on the parameter u. Further, the coefficients a_1, a_2, a_3 will depend on $\frac{R_4}{R_3}, V_{X1}$ and the saturation voltage of OTRA (V_{sat}). In order to allow amplitude stabilization mechanism, the values of $\frac{R_4}{R_3}$ and V_{X1} must be chosen to satisfy the condition of

$$\frac{R_4}{R_3} >> \frac{V_{sat}}{V_{X1}} \tag{6.42}$$

6.4 Simulation Results

The functionality of the proposed Wien bridge oscillator has been verified through SPICE simulations where the OTRA and the buffer are realized using commercially available IC AD844N as shown in Figure 2.4 (chapter 2) and 6.3 respectively. The supply voltages are chosen as ± 8.5 V. The proposed oscillator is designed for a FO of 300 KHz for which the components are computed as R_1= 9 kΩ, R_2= 3 kΩ, R_3= 1 kΩ, R4 = 5.1 kΩ and C= 104 pF. Simulated transient output and the corresponding frequency spectrum obtained through simulation are depicted in Figure 6.5. The simulated value of THD is observed as 0.8%.

Next, the simulations are carried out to examine the harmonic distortion of the oscillator for the chosen supply voltages, V_{SAT} of 5 V is obtained for OTRA from SPICE simulation. To examine the impact of R_4/R_3 on HD_2 and HD_3, for FO of 300 KHz different peak amplitudes of 0.5 V, 1 V and 1.65 V are considered. The corresponding R, C values and u_{opt} for these peak voltages are shown in Table 6.1. The simulated waveforms of V_X and V_Y for settings at serial number 1, 2 and 3 of Table 6.1 are depicted in Figures 6.6 (a), 6.7 (a) and 6.8 (a), respectively. It has been discussed in section 6.3 that signal distortion occurs mainly due to active element saturation mechanism [216]. To validate this point, R_4/R_3 is changed from settings given in Table 6.1 and corresponding waveforms are placed as Figures 6.6 (b), 6.7 (b) and 6.8 (b) which are slightly distorted waveform thus confirming the mentioned fact.



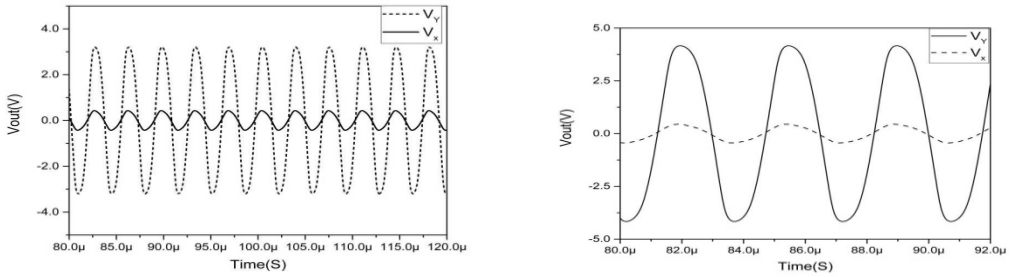
(a) (b)

Figure 6.5. (a) Transient output (b) Frequency spectrum

Table 6.2 enlists simulated and theoretical values of HD_2 and HD_3 for the three cases discussed above. There is close agreement between the two. The THD for the three cases is within 1%.

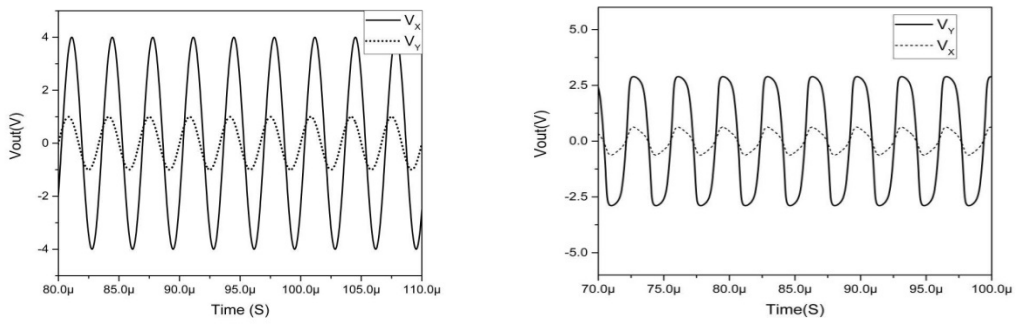
Table 6.1. Example design parameters

S.No.	V_{X1}	Resistance (kΩ)	C(pF)	u_{opt}
1	0.5V	R_1=16,R_2=2,R_3=1,R_4=10.1	94	4.5
2	1V	R_1=9,R_2=3, R_3=1,R_4=5.1	102	2.5
3	1.65V	R_1=R_2=5.2, R_3=1,R_4=3.1	102	1.5



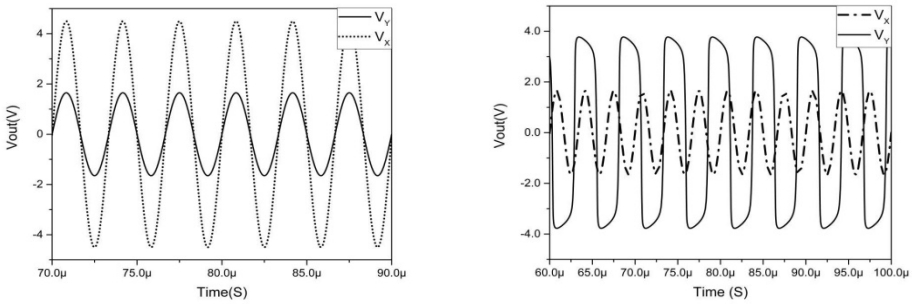
(a) (b)

Figure 6.6. Simulated waveforms for V_X and V_Y (Settings of S. No. 1 of Table 6.1) with (a) R4/R3 = 10.1 (b) R4/R3= 11



(a) (b)

Figure 6.7. Simulated waveforms for V_X and V_Y (Settings of S. No. 2 of Table 6.1) with (a) R4/R3 = 5.1 (b) R4/R3 = 6



(a) (b)

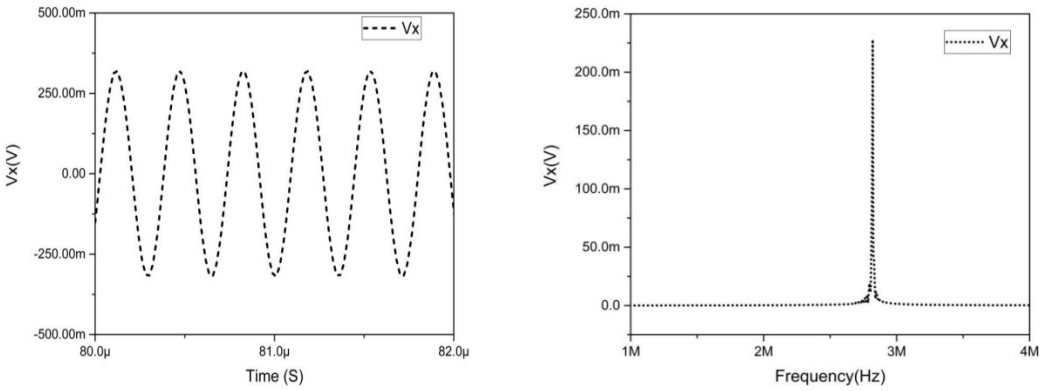
Figure 6.8. Simulated waveforms for V_X and V_Y (Settings of S. No. 3 of Table 6.1) with (a) R4/R3 = 3.1 (b) R4/R3 = 4

Table 6.2. Theoretical and Simulated values of HD2 and HD3.

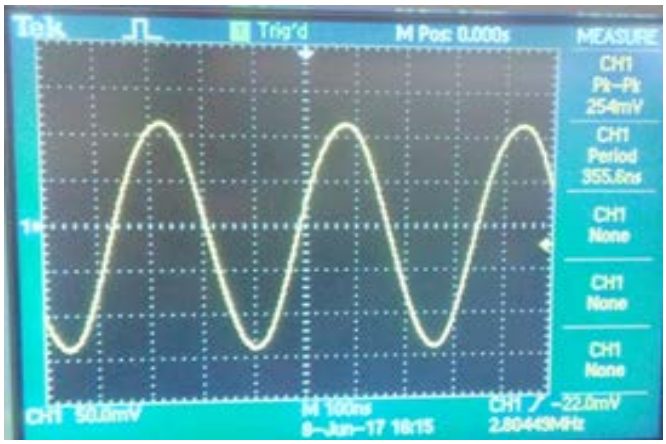
S.No	**V_{X1}**	**Theoretical**		**Simulated**	
		HD_2(dB)	HD_3(dB)	HD_2(dB)	HD_3(dB)
1	0.5V (R_4/R_3)=10	-46.71	-54.65	-48.80	-52.34
2	1V (R_4/R_3)=5	-45.52	-48.40	-46.65	-48.89
3	1.65mV (R_4/R_3)=3	-45.51	-46.64	-42.27	-41.68

6.4.1 Experimental Results

The functionality of the proposed Wien bridge oscillator is also verified experimentally for which the circuit is breadboarded using AD844 ICs. The passive components are chosen as R_1= 16 kΩ, R_2= 2 kΩ, R_3= 1 kΩ, R_4 = 10.1 kΩ and C= 10 pF corresponding to FO of 2.82 MHz.



(a) (b)



(c)

Figure 6.9. (a) Simulated transient output waveform and (b) its frequency spectrum (c) Experimental output waveform

The simulated transient output waveform and its frequency spectrum are shown in Figures 6.9 (a) and (b), respectively. Simulated THD value at FO of 2.82 MHz is found to be 0.7%. The experimental output is depicted in Figure 6.9 (c). The observed values of FO (2.80 MHz) closely match with the theoretical values.

6.5 Conclusion

The OTRA based Wien bridge oscillator has been presented in this chapter, which is a suitable choice for high-frequency applications. The FO and the CO for the proposed structure are derived and the structure is also analyzed in the presence of device nonidealities. The detailed harmonic analysis is carried out to characterize the linear performance of the proposed oscillator. The workability of the proposed oscillator is presented through SPICE simulations and experimental prototyping. The THD for the proposed design is found to be less than 1%.

Chapter 7
CONCLUSION AND FUTURE SCOPE

This thesis presents the signal generating circuits and their performance analysis using OTRA, a current mode analog building block of relatively recent origin. In this chapter, a summary of the major conclusions of the work reported in various chapters of the thesis is presented.

7.1 Summary of Work done in this Thesis

The introduction chapter presents a brief overview of various current mode analog building blocks. Further, it takes a detailed look at the significance of signal generation circuits and this is followed by literature review on OTRA based SOs.

In chapter 2, the CMOS based and off the shelf ICs (CFOA-AD844 IC) based realizations of OTRA are studied and characterized. The characterization of the CMOS OTRA circuit is done through Cadence Virtuoso ADE spectre tool at 0.18 μm CMOS technology node. The schematic driven and post-layout simulation results have been included. The CFOA IC-based realization is characterized using SPICE. These simulated structures set the groundwork for the material that follows as these are used for validation of all proposed designs. Nonideal behavior of OTRA is also studied so that its effect on proposed circuits can be analyzed.

Chapter 3 deals with single OTRA based SOs. Three, second order SOs are proposed in this chapter, out of which two SOs can be used to achieve low frequencies without a large component spread. Further, a third order oscillator is also presented.

Chapter 4 of this thesis extends into the designing of quadrature oscillators and in all five QO topologies have been proposed. The first one is a second order structure and it qualifies for low frequency operations as well without having large component spread. One of the TOQO topologies adapts the scheme of using second order high pass filter and a differentiator in a feedback loop, whereas the other three topologies are derived from an inverse filter based generalized structure.

In chapter 5, four new structures of electronically tunable SOs are presented. Each of the proposed SO consists of forward path derived from a generic structure along with one/two OTRA based resistive gain stages or differentiator in its feedback path. All the proposed SOs enjoy independent tuning of the FO through resistors without affecting the CO. Further, all topologies are found to exhibit low sensitivities to circuit parameters at all frequencies. One of the proposed structures is capable of providing frequencies in the VLF range with low RC component spread and provides linear tuning too, whereas one of those provides quadrature outputs.

Chapter 6 of this thesis presents Wien bridge oscillator, which uses an OTRA, two RC sections and a buffer. Further, harmonic analysis is carried out to characterize the linear performance of the proposed oscillator.

Effect of nonidealities of OTRA is studied on the proposed structure and various performance analyses such as sensitivity, stability, harmonic and phase noise analysis as applicable are carried out. Functionality of all propositions is verified through simulations using SPICE/Cadence Virtuoso spectre ADE tool using 0.18 µm CMOS process parameters. Further, few circuits are verified experimentally also and post layout simulation results are included for rest.

It is significant to state here that all the proposed designs in this work has some floating passive components. The grounded capacitors are preferred from fabrication viewpoint, using top-quality IC technology of today, they can be implemented using advance techniques such as metal–insulator–metal (MIM) or metal–oxide–metal (MOM), double poly (poly1–poly2) capacitor processes.

The salient features of all proposed structures have been summarized in Table 7.1.

Table 7.1. Salient features of proposed structures

Chapter	Name of Structure	No.of OTRA	Order	Analysis	O/p phase	Complete MOS-C based realization	Electronic Tuning	Independent Tuning	Layout	Experimental
1	*Introduction and Background of Analog Building Blocks and Literature Review*									
2	*Basic OTRA and its Characteristics*									
3 Single OTRA based Oscillators	Topology-I	1	2	Sensitivity, Monte Carlo	S	Yes	No	No	No	Yes
	Topology-II	1	2			No	No	No	No	Yes
	Topology-III	1	2			No	No	Yes	No	Yes
	TOSO	1	3			No	No	Yes	Yes	Yes
4 Quadrature Oscillators	QO-I	2	2	Frequency Stability, Sensitivity, Phase Noise, Monte Carlo	Q	Yes	Yes	Yes	Yes	No
	TOQO-I	2	3		Q	Yes	No	Yes	No	Yes
	Topology-I	3	3		Q	Yes	Yes	Yes	Yes	No
	Topology-II	3	3		Q	Yes	Yes	Yes	Yes	No
	Topology-III	3	3		Q	Yes	Yes	Yes	Yes	No
5	Topology-I	2	2	Frequency Stability,	S	No	Yes	Yes	Yes	No

Wide Range tuning Oscillators	Topology-II	3	2	Sensitivity, Phase Noise, Monte Carlo, PVT	S	No	Yes	Yes	Yes	No
	Topology-III	3	2		S	No	Yes	Yes	Yes	No
	Topology-IV	3	2		Q	Yes	Yes	Yes	Yes	No
6	Wein bridge Oscillator	1+ Buffer	2	Harmonic analysis	S	No	No	Yes	No	Yes

7.2 Future Scope

Signal generator is the extensively used general instrument in the modern test area. The signal source is needed in production, testing and maintenance of equipment. In the modern field of electronic systems, wave generator can be used as stand-alone signal sources or may be integrated in sensing system for providing excitation and control.

Versatility of oscillators in electronic applications coupled with advantages of OTRA and availability of limited literature has led the author of the thesis to explore the area of OTRA based signal generation.

Tuning of amplitude and frequency and their independent control adds extra flexibility to the system. Therefore, the SO topologies may be designed with inbuilt amplitude control feature, which was not undertaken in this work. Further, in this era of miniaturization, low voltage low power SO topologies may be investigated.

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