MITIGATION OF T.H.D OF MICROCONTROLLER BASED THREE PHASE VOLTAGE SOURCE INVERTER

THESIS

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
POWER SYSTEMS

Submitted by:

Hemant Kumar

2K17/PSY/06

Under the supervision of

Prof. Uma Nangia

DEPARTMENT OF ELECTRICAL ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

M.Tech (Power Systems) **Hemant Kumar** **2019**

DEPARTMENT OF ELECTRICAL ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, **Hemant Kumar**, Roll No, **2K17/PSY/06** student of M. Tech (PSY), hereby declare that the thesis titled "**Mitigation of THD of Microcontroller based Three Phase Voltage Source Inverter**" which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology ,is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

Place: Delhi **HEMANT KUMAR**

Date:

DEPARTMENT OF ELECTRICAL ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I, **Hemant Kumar**, Roll No. **2K17/PSY/06** student of **M. Tech. (Power Systems),** hereby declare that the dissertation/project titled "**Mitigation of THD of Microcontroller based Three Phase Voltage Source Inverter**" under the supervision of **Prof. Uma Nangia** of Electrical Engineering Department Delhi Technological University in partial fulfillment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any Degree.

Place: Delhi **HEMANT KUMAR**

Prof. Uma Nangia
HoD,Electrical Engineering Department

ACKNOWLEDGEMENT

On the submission of my thesis entitled "**Mitigation of THD of Microcontroller based Three phase Voltage Source Inverter**", as a M.Tech thesis, I would like to extend my appreciation & my sincere thanks to my project supervisor, a very generous guide in fact, **Prof. Uma Nangia**, Department of Electrical Engineering for her ceaseless encouragement and support during the course of my work. I verily appreciate and value her prestigious guidance and motivation from the beginning to the end of this work. Her knowledge and support at the time of crisis will be remembered lifelong. She has been great source of inspiration to me and I thank her from the bottom of our hearts.

I would also like to thank the staff of Electrical engineering department for constant support and providing place to work during project period.

Hemant Kumar

M.Tech (Power Systems)

ABSTRACT

The use of power electronic devices plays a crucial role in control and transformation of electrical power.These devices are non-linear which takes enough space in all the regions of Power electronic converters. Inverter plays important role in industrial and domestic-applications for converting the direct current(DC) power into an alternating current(AC) power.

Use of these controlled switches in inverters is gives a smooth and precise control for the transformation of electric power. But on the other hand, usage of these controlled switches results in the high level of Total Harmonic Distortion (THD) which has poor effects on the converter's performance. This thesis aims at the mitigation of THD for three-phase voltage source inverter using low pass filter. This method is analyzed using fourier spectrum of the output phase voltages and the total harmonic distortion (THD). With addition to this, this thesis also discusses three phase inverter with 180 and 120 degrees conduction mode. RLC low pass filter is designed to reduce the lower order dominating harmonics and to lowers the total harmonic distortion (THD). The models for boost converter, gate driver circuit three phase inverter with 180 and 120 degrees conduction mode (with and without filter) have been simulated using proteus (simulator) and 8051 microcontroller is programmed using uKeil (programming software) to control the switching pattern of MOSFET's.

CONTENTS

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

List of Tables

Chapter 1

Chapter 5

CHAPTER 1

INTRODUCTION

In present days, an electric power converter plays a important role in industries and power sector. Power converters like, Rectifiers are used for transformation of AC power into DC power; Inverters are used for transformation of DC power into AC power; AC voltage controllers/ Cycloconverters are used for transformation of fixed AC into variable AC with variation in both magnitude/frequency; Choppers are used for transforming fixed DC into variable DC. Among these converters, this thesis shows focus towards inverters which finds an very important application in industries and domestic purposes. Usually, an inverter gives a square waveform for given DC input. To make the output sinusoidal, passive filter (Low Pass Filter) has been implemented in this thesis. Inverters can be designed either uncontrolled switches like diodes or controlled switches like SCRs, IGBT's and MOSFET's etc. But to get a AC output, it is necessary to use these controlled switches in inverters. Since these devices are nonlinear, it includes disturbances called harmonics in the sinusoidal waveform. Harmonics are multiple of fundamental frequency [1]. For example, if fundamental frequency is 50Hz, then the second harmonic will be (2*50) 100Hz; third harmonic will be (3*50) 150Hz and so on. These harmonics will cause several disadvantages in power system like increase of current, high losses, torque pulsations and heating of the equipments etc. Therefore the reduction of harmonics is important to run the electrical systems smoothly. These harmonics are cumulatively leads to a distortion called as Total Harmonic Distortion or THD. The Total Harmonic Distortion or THD of a signal is the ratio of the square root of sum of the squares of all individual harmonic voltage components to the power of the]voltage fundamental frequency component.

THD is used to assess the power quality of power electronic converters. Less the THD, the waveform will be free of harmonics and more the sinusoidal. Mitigation of THD in inverters can be done by eliminating lower order harmonics using Low Pass Filter.

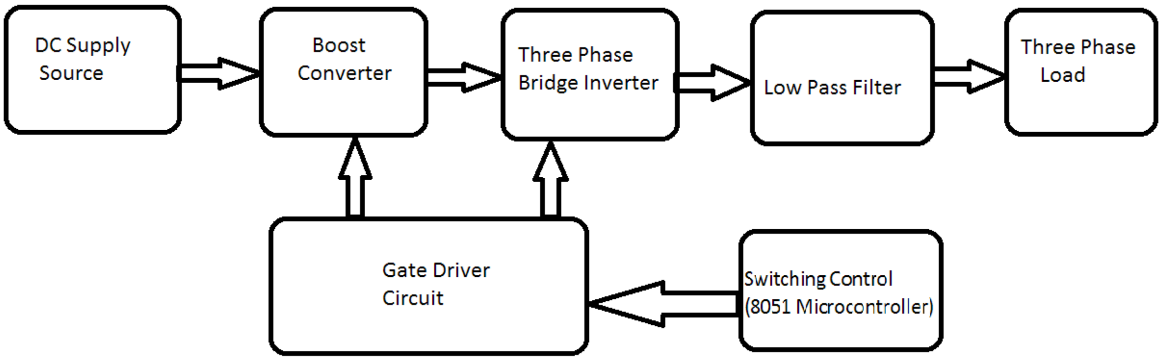


Figure 1.1 *Block diagram of the design of the inverter*

The design of inverter has a DC supply whose voltage is stepped up by a DC-DC step up converter or Boost Converter, the output of the boost converter acts as an input DC source for the three phase bridge inverter. The output of the bridge inverter is square waveform, which has harmonics. In order to convert the square wave out into sinusoidal wave form, we need to reduce to the harmonic component of different order. In square wave output of the inverter,the lower order harmonics of 150Hz,200Hz,250Hz. are more dominating as compared to the higher order harmonics. In other words, peak voltage levels of lower order harmonic component is greater than the peak voltage level of the higher order harmonic component. The lower order harmonics are the main reason of undesirable Total Harmonic Distortion(THD). In order to eliminate these harmonics, lower pass filter of cutoff frequency less than that of is required dominating frequency is required.The low pass filter reduces the peak voltage level of the dominating harmonics and gives an approximate sinusoidal wave which is low in THD.

The switching control unit is a 8051 microcontroller which is programmed to control switching duration and pattern of switching of MOSFETs of boost converter and inverter. The pin output voltage of microcontroller is 5V, which is less than the required gate voltage to trigger a MOSFET.

To overcome this problem a gate driver is interfaced with microcontroller and it amplifies the low pin voltage (5V) to high voltage(14.75V).

CHAPTER 2

LITERATURE REVIEW

A three-phase output can be obtained from a configuration of six MOSFETs as shown in Figure 2.1.

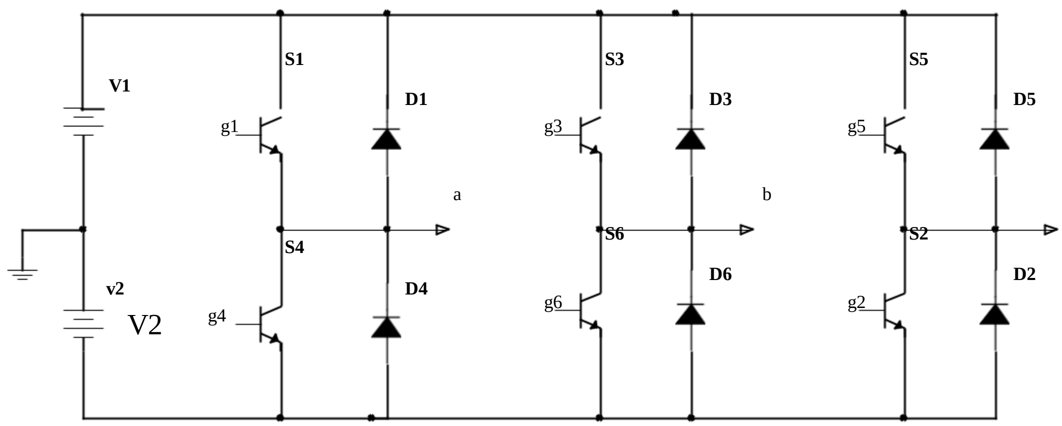


Figure 2.1 *Three Phase Bridge Inverter Circuit Diagram*

Two types of control signals can be applied to the MOSFET:

- 180˚ conduction mode
- 120˚ conduction mode

180˚ conduction mode

Each MOSFET conducts for 180˚. Three MOSFETs remain on at any instant of time. When MOSFET S1 is turned ON, terminal ‘a’ of Figure 2.1 is connected to the positive terminal of the DC source. When MOSFET S4 is turned ON, terminal ‘a’ is connected to the negative terminal of the DC source. There are six modes of operation in a cycle and the duration of each mode is 60˚. The switching pulses are as shown in Figure 2.2. The MOSFETs are numbered in the sequence of gating the MOSFETs. That is S1 S2 S3, S2 S3 S4, S3 S4 S5, S4 S5 S6, S5 S6 S1, and S6 S1 S2.

The signals are shifted from each other by an angle of 60˚ to obtain balanced three phase voltages.

The load may be in form of star or delta connected. For delta connected load, the phase currents can be calculated from line to line voltages. Line currents are calculated from phase currents.

Table 2.1 *Switching Sequence in 180˚ conduction mode*

180° Degree Conduction Mode

Mode	S_1	S_2	S_3	S_4	S_5	S_6
1st	ON	OFF	OFF	OFF	ON	ON
2nd	ON	ON	OFF	OFF	OFF	ON
3rd	ON	ON	ON	OFF	OFF	OFF
4th	OFF	ON	ON	ON	OFF	OFF
5th	OFF	OFF	ON	ON	ON	OFF
6th	OFF	OFF	OFF	ON	ON	ON

For star connected load, the phase voltages must be calculated to determine the line currents.

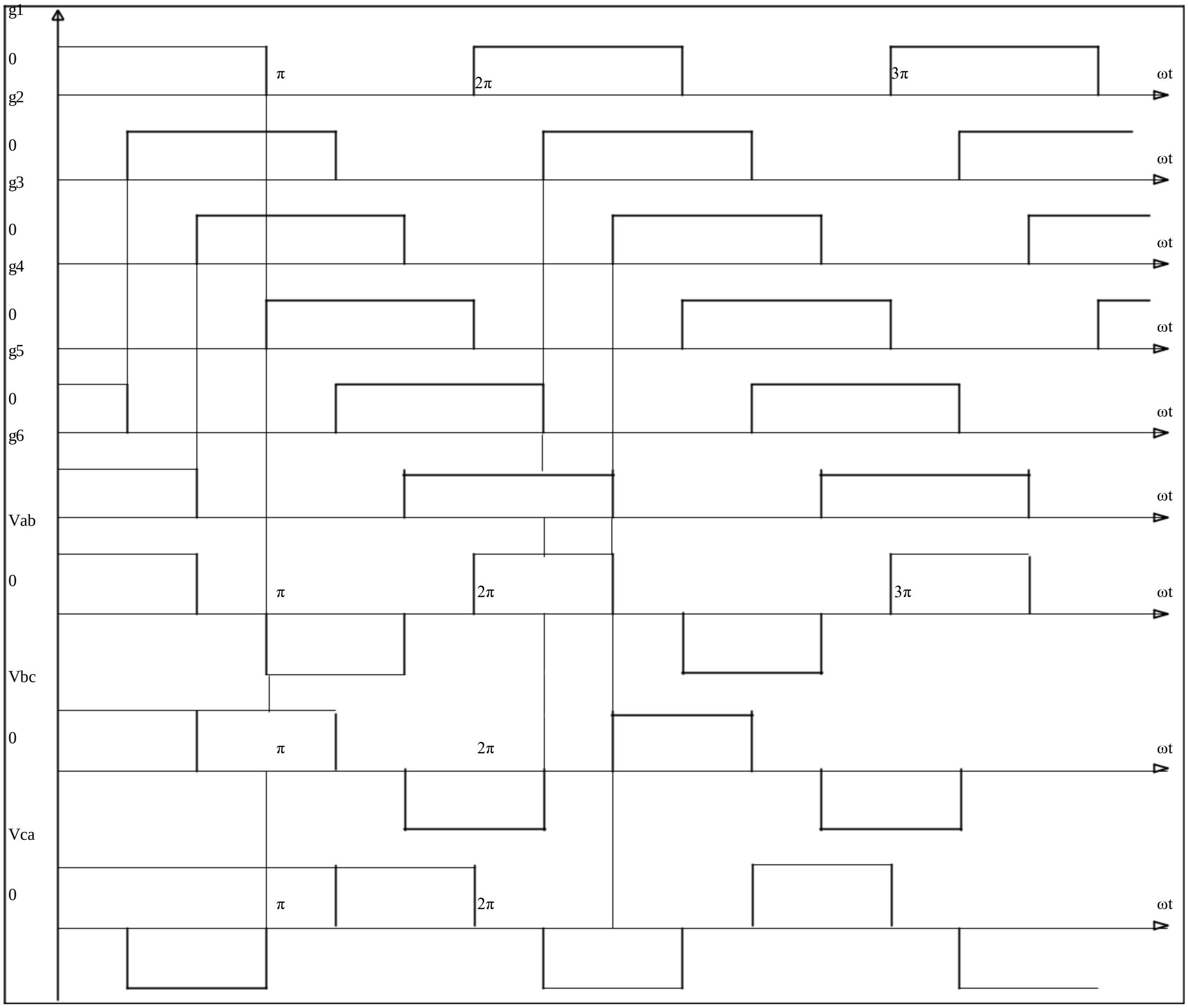


Figure 2.2 *Switching pulse Waveforms for and 180˚ conduction mode*

120˚ conduction mode

In 120˚ conduction mode , each MOSFET conducts for 120˚ duration . Only 2 MOSFETs remain ON at any instant of time. The switching pulses are as shown in Figure 2.3. The conduction sequence of the MOSFETs is S6 S1, S1 S2, S2 S3, S3 S4,S4 S5, S5 6 and S6 S1.

***Table 2.2** Switching Sequence in 120˚ conduction mode*

120° Degree Conduction Mode

Mode	S1	S2	S3	S4	S5	S6
1st	ON	OFF	OFF	OFF	OFF	ON
2nd	ON	ON	OFF	OFF	OFF	OFF
3rd	OFF	ON	ON	OFF	OFF	OFF
4th	OFF	OFF	ON	ON	OFF	OFF
5th	OFF	OFF	OFF	ON	ON	OFF
6th	OFF	OFF	OFF	OFF	ON	ON

.

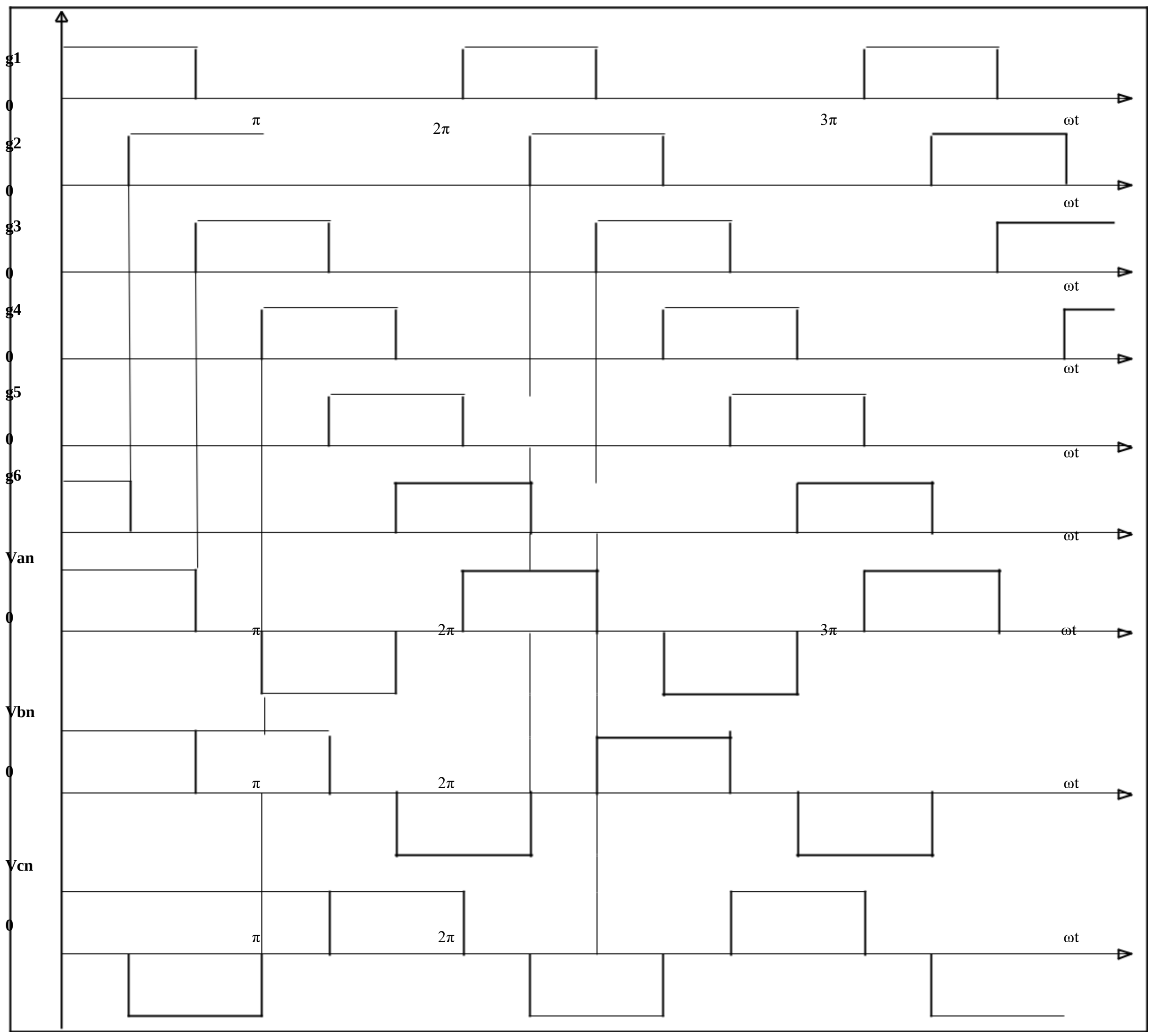


Figure 2.3 *Switching pulse for 120˚ conduction mode*

2.1 Control of inverter output voltage

There are many applications in which it is important to control the output voltage of the inverter. Two of these applications are a stabilized AC or DC voltage source from a supply whose voltage changes rapidly during discharge, and an AC motor control system, in which a constant/fixed voltage-to-frequency ratio has to be maintained to avoid saturation of motor. In both cases, control of inverter voltage is required [1].

The output voltage of the single-phase inverter is square wave with magnitude nearly equal to the input DC supply voltage. Therefore the output is proportional to the input supply voltage.

Three methods of output control are:

- Control of DC input supply t voltage
- Controlling AC output voltage
- And by Pulse width modulation (PWM)

If inverter is supplied from an AC supply by a rectifier, the input to the inverter can be controlled by an induction regulator ,variac controlled rectifier[2].

If the supply is DC, it can be controlled by series or shunt ,chopper or regulator or using time-ratio control method.

Reduction of harmonics in the inverter

The inverter output waveform varies depending on the load and the circuit used. In most cases load requires sinusoidal wave output but most of the inverter produces square voltage output. Therefore methods are required to convert the waveforms of the inverter output to a sinusoidal waveform.[1] Harmonic reduction/mitigation can be done by the following methods:

- Resonating of load
- Low pass LC filter
- pulse width modulation
- Polyphase inverters.

2.2 Three phase inverter conduction modes

180˚ conduction mode

There are six modes of operation in a complete cycle and the equivalent circuits of three mode are shown in Figure 2.4. The output waveforms for the voltages of each phase are shown in Figure 2.5

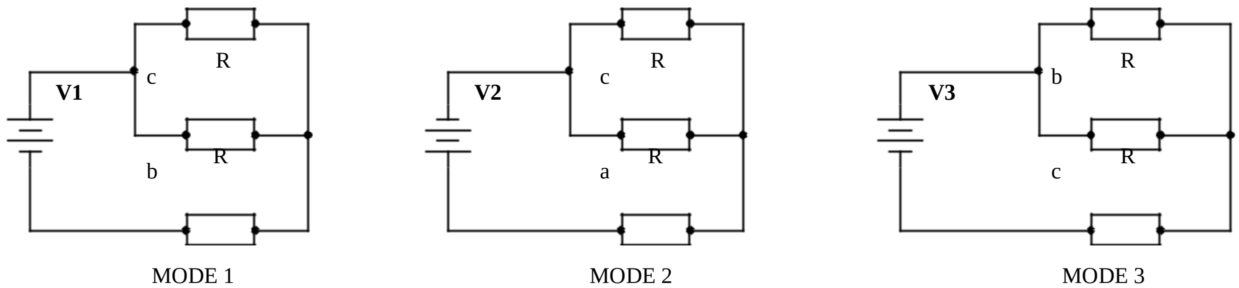


Figure 2.4 *Equivalent circuit diagrams for different modes of operation*

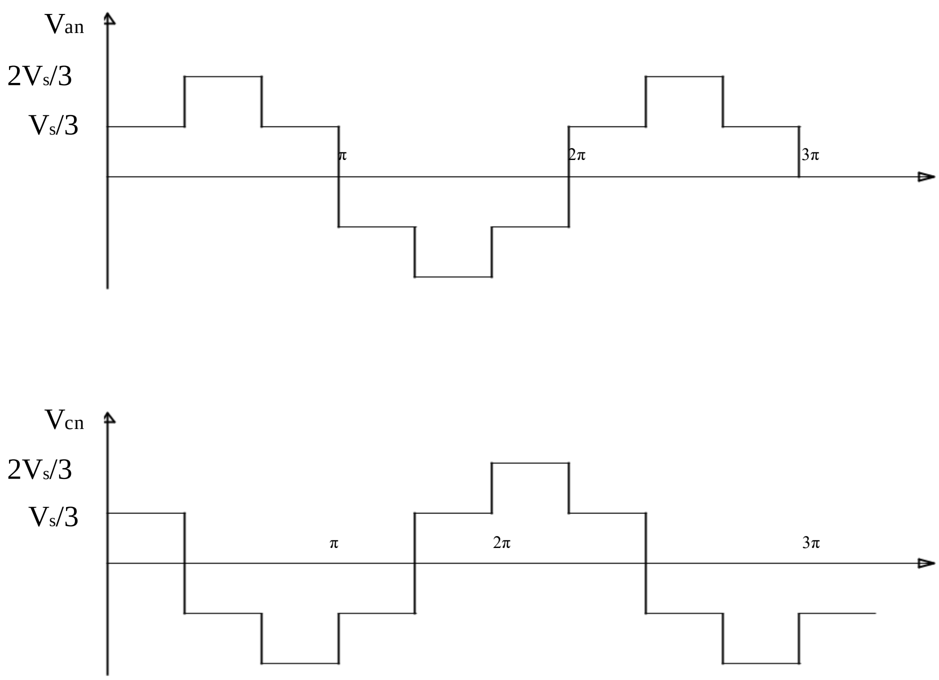


Figure 2.5 *Phase voltage for 180˚ conduction mode*

(a) During mode 1 of operation , for 0 ≤ ωt ≤ π/3

MOSSFETs S5,S6 and S1 conducts, the equivalent resistance as seen from input source Vs is,

R_{eq} =R +R/2= 3R/2

i_1= Vs/ R_{eq} =2V_s/3R

v_{an}= v_{cn} = i_1Req /2 =Vs/3

$v_{bn} = -i_1 \frac{R}{2}$ = -2Vs/3

(b) During mode 2 of operation, for π/3 ≤ ωt ≤2π/3

MOSSFETs S2,S6 and S1 conducts, the equivalent resistance as seen from input source Vs is,

R_{eq} =R +R/2= 3R/2

i_2= Vs/ R_{eq} =2V_s/3R

$v_{an} = i_2 \frac{R}{2}$ = 2Vs/3

v_{cn}= v_{bn} =$-$ i_2Req /2 =-V_s/3

(c) During mode 3 of operation, for,2π/3 ≤ ωt ≤ π

MOSSFETs S1,S2 and S3 conducts, the equivalent resistance as seen from input source Vs is,

R_{eq} = R +R/2= 3R/2

i_3 = 2Vs/3R

$v_{cn} = -i_3 \frac{R}{2}$ = -2Vs/3

v_{an}= v_{bn} = i_3Req /2 =Vs/3

The instantaneous line current voltage, v_{ab}, in Figure 2.2 can be expressed in a Fourier series, knowing that v_{ab} is shifted by 30 °and the even harmonics are absent .

$$v_{ab} = \sum_{n=1,3,5\ldots}^{\infty} \left(\frac{4\mathrm{V_S}}{\mathrm{n\pi}}.\cos\frac{n\pi}{6}.\sin \mathrm{n}(\omega\mathrm{t}+\frac{\pi}{6})\right) \quad (2.1)$$

V_{bc} and V_{ca} can be determined by phase shifting V_{ab} by 120° and 240° respectively.

$$v_{bc} = \sum_{n=1,3,5\ldots}^{\infty} \left(\frac{4\mathrm{V_S}}{\mathrm{n\pi}}.\cos\frac{n\pi}{6}.\sin \mathrm{n}(\omega\mathrm{t}-\frac{\pi}{2})\right) \quad (2.2)$$

$$v_{ca} = \sum_{n=1,3,5\ldots}^{\infty} \left(\frac{4\mathrm{V_S}}{\mathrm{n\pi}}.\cos\frac{n\pi}{6}.\sin \mathrm{n}(\omega\mathrm{t}+\frac{5\pi}{6})\right) \quad (2.3)$$

From equations (2.1), (2.2) and (2.3) it can be noticed that the triplhen harmonics i.e, n=3, 6, 9........ would be zero valued in the line voltages.

The line RMS voltages can be found from,

0. $$v_{ln} = \sqrt{\frac{2}{2\pi}\int_0^{\frac{2\pi}{3}} v_s^2 \; d(\omega t)} \quad (2.4)$$

$$= 0.816 \text{ Vs}$$

From equation (2.4) the RMS nth component of the line voltage is

$$v_{ln} = \frac{4\mathrm{V_s}}{\mathrm{n\pi}\sqrt{2}}\cos\left(\frac{n\pi}{6}\right) \quad (2.5)$$

Which for n=1, gives the fundamental line to line voltage.

v_{ab}= 0.78 Vs

The RMS value of the phase voltages can be determined from the line voltage

v_{ph}= 0.4717 Vs

$$v_{an} = \sum_{n=6k\pm1}^{\infty} \left(\frac{2\mathrm{V_s}}{\mathrm{n\pi}}\sin \mathrm{n\omega t}\right) \quad (2.6)$$

With resistive load, the diodes across the MOSFETs have no role. If the load's nature is inductive/capacitive, the current in each leg of the inverter would be delayed to its voltage.

The MOSFETs must be continuously triggered since the conduction time of MOSFETs and diodes depends on the load power factor.

For a star connected load, the phase voltage is Van =0.8523Vab with a delay angle of 30˚.

The line current i_a for an R-L load is given by[2]

$$\mathrm{ia} = \sum_{n=1,3,5\ldots}^{\infty}\left(\frac{4\mathrm{V_s}}{\sqrt{\mathrm{R}^2+(\mathrm{n}\omega\mathrm{L})^2}.\mathrm{n}\pi\sqrt{3}}.\cos\left(\frac{n\pi}{6}\right)\right).(\sin(\mathrm{n}\omega\mathrm{t}-\theta_\mathrm{n})) \qquad (2.7)$$

where $\theta_n = \tan^{-1}\frac{\omega L}{R}$

120˚ conduction mode.

There are three modes of operation in half cycle and the equivalent circuits are star connected loads.

During mode1 of operation, for $0 \leq \omega t \leq \pi/3$,MOSFETs S1 and S6 conduct,

$v_{an} = V_s/2 \quad v_{bn} = -Vs/2 \quad v_{cn} = 0$

During mode 2 of operation, for $\pi/3 \leq \omega t \leq 2\pi/3$, MOSFETs S1 and S2 conduct,

$v_{an} = Vs/2 \quad v_{bn} = 0, v_{cn} = -Vs/2$

During mode 3 of operation for, $2\pi/3 \leq \omega t \leq \pi$, MOSFETs S2 and S3 conduct

$v_{an} = 0, v_{bn} = V_S/2 \ , v_{cn} = -V_S/2$

The phase voltages can be expressed in Fourier series as

$$v_{an} = \sum_{n=1,3,5\ldots}^{\infty}\left(\frac{2\mathrm{V_S}}{\mathrm{n}\pi}.\cos\frac{n\pi}{6}.\sin\mathrm{n}(\omega\mathrm{t}+\frac{\pi}{6})\right) \qquad (2.8)$$

$$v_{bn} = \sum_{n=1,3,5\ldots}^{\infty}\left(\frac{2\mathrm{V_S}}{\mathrm{n}\pi}.\cos\frac{n\pi}{6}.\sin\mathrm{n}(\omega\mathrm{t}-\frac{\pi}{2})\right) \qquad (2.9)$$

$$v_{cn} = \sum_{n=1,3,5\ldots}^{\infty}\left(\frac{2\mathrm{V_S}}{\mathrm{n}\pi}.\cos\frac{n\pi}{6}.\sin\mathrm{n}(\omega\mathrm{t}+\frac{5\pi}{6})\right) \qquad (2.10)$$

The line voltage between phase ‘a’ and ‘b’ is V_{ab}=1.732 V_{an} with a phase angle of 30 degree . There is a delay of 30˚ angle between turning off MOSFET S1 and turning on MOSFET S4. Such that no short circuit of the dc supply occurs.

At any time there, two load terminals are connected to the dc supply and the third one remains open. Since the MOSFET conducts for 120˚ duration the MOSFETs are less utilized as compared to that of the 180˚ conduction mode for the same connected load[9].

An inverter circuit is used to transform the DC power to AC power. This transformation can be done by MOSFETs or by SCRs switches. For low and medium power output, common MOSFETs and BJTs but MOSFETs are suitable but for high power outputs and high power MOSFETs such as IGBT are used.[3] For low power self oscillating, MOSFETized inverters are suitable but for high power output applications, driven inverter are more common than self oscillating ones [1]. Moreover for multiphase ac output, driven inverters must be used.

The driven inverters have higher frequency stability because a separate microcontroller is used for the purpose. For inverter applications, MOSFET has following advantages over SCR [1]

- Higher switching speed(fast operation)
- Simple gate driver circuit(IR2101 MOSFET driver is used)
- Higher efficiency and more reliability(low switching losses)

This is mainly due to the fact that SCR inverters require separate circuit to turn off SCRs, moreover another additional complex logic circuits is also needed to prevent unwanted triggering and to provide proper commutation timing.

2.3 Performance Parameters of Inverter

The output voltage of a practical inverter always have harmonics content of different orders therefore, the quality of an inverter is usually assessed by performance parameters given below[3]

2.3.1 Harmonic factor of nth harmonic (HF_n)

This is the measure of individual harmonic contribution and is expressed

as:

$$HFn = \frac{V_n}{V_1}$$

where V_1 is the RMS value of the fundamental component and V_n is the

RMS value of the n^{th} order harmonic component present.

2.3.2 Total harmonic distortion, THD

This is the measure of closeness or exactness in shape between a waveform and its fundamental components.[3]

It is expressed as:

$$TDH = \frac{1}{V_1}\left(\sum_{n=2,3\ldots}^{\infty} V^2\right)^{1/2}$$

2.3.1 Distortion factor, DF

It is a measure of effectiveness in reducing undesirable harmonics content without specifying the values of a second order filter. DF shows the amount of harmonic distortion that remains in a waveform after the harmonic content of that waveform have been subjected to a second order filter.[3]

$$DF = \frac{1}{V_1}\left[\sum_{n=2,3\ldots}^{\infty}\left(\frac{V_n}{n^2}\right)^2\right]^{1/2}$$

The distortion of an individual (or nth) harmonic component is written as:

$$DF = \frac{V_n}{V_1 n^2}$$

2.3.4 Lower-order harmonic, LOH

This is that harmonic content whose frequency is nearest to the fundamental frequency, and its magnitude is more than or equal to three percent of the fundamental component[3]

2.4 Types of load

2.4.1 Resistive load

The resistive load gives no problem to inverter. The voltage waveform is a square wave and since current and voltage are in phase its waveform is also square in nature. This is shown in the Figure 2.6..

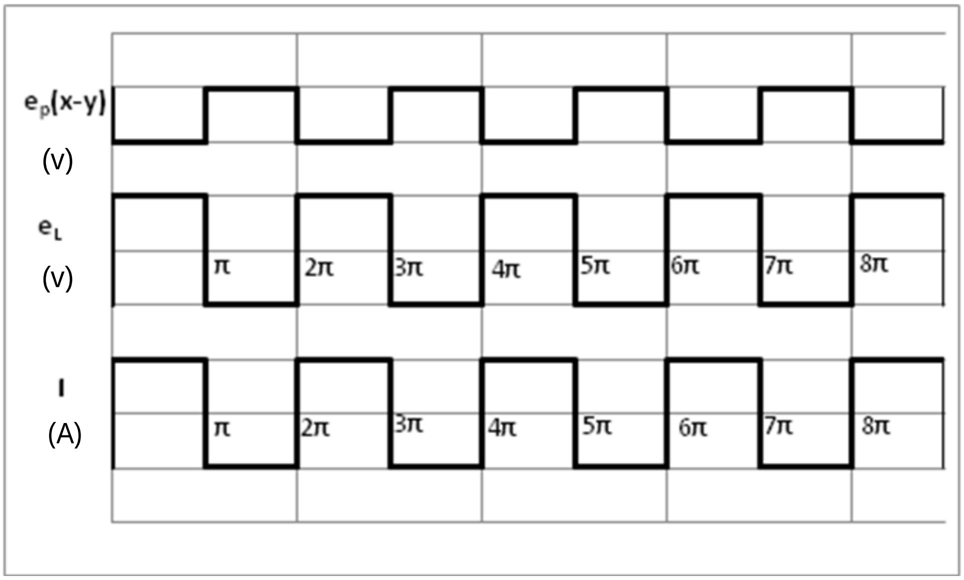


Figure 2.6 *Voltage and current waveforms for resistive load*

Every MOSFET conducts for 180° and the magnitude for current depends on the load value. The power delivered by MOSFET is $\int VIdt$ and current's waveform is also a square-wave whose area is proportional to the power absorbed by load.

2.4.2 Inductive load

AC source while supplying a load having lagging (or leading) power factor load delivers power to load in first half-cycle and receives power from load in the remaining half-cycle. In static inverter the power source is DC in nature and if it has to supply a lagging power factor load, it must be able to deliver power in half-cycle of the inverter and receiving power in the other half-cycle.[8] In voltage source inverter, the transformed voltage is always a square wave in nature because bit works in accordance with the driver circuit and hence current must shift phase [4]. Therefore in first half cycle of the voltage, power is delivered to the load (or given by the source) and the inverter must be able to receive power and deliver it to the DC source in the other cycle of the voltage--waveform, or this power should be dissipated on the load connected to the inverter. The voltage and current waveform for an inductive (purely) load are shown in Figure 2.6. below

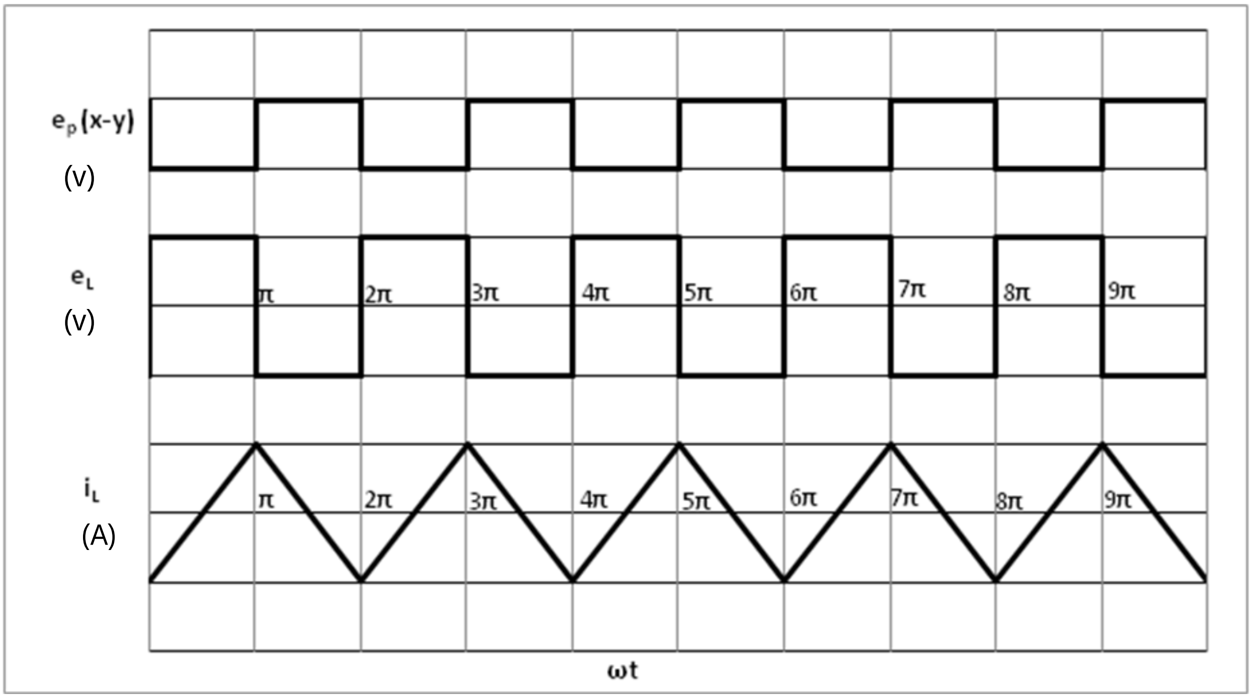


Figure 2.7 .*Voltage and current waveforms across a purely inductive load*

When load voltage and current are in same phase, source delivers power and absorbed by the load. But when the load voltage and current are in opposite phase, load delivers powers to source .In a voltage source inverter (VSI), the MOSFETs should pass current(conduct) as soon as they are turned ON, that is switch S_1 should start to conduct in the normal direction as the voltage crosses zero, but because of the inductive type load, the current doesn't change its direction immediately and continues to flow in opposite(reverse) direction. This means that the inductive property of the load tries to force a reverse current through the MOSFETs switches. However, the semiconductor devices are unidirectional in nature and blocks reverse current interruption takes place when the load current is at its maximum/peak value. This sudden blockage of current causes a reverse voltage spike to develop on the transformer primary[2]. The reverse voltage is of infinite value(high dv/dt) which can damage the devices. Switch S_2 would also face the same when it tries to conduct at an angle of π. This problem can be dealt by providing a freewheeling path for the load current to flow during the device switching duration. There are two ways:

- Preloading the inverter (resistance in parallel with non resistive loads)
- Use of feedback diode.

- **Preloading the inverter**

Inverter preloading involves connecting a resistance in parallel with the non resistive loads. This provides a freewheeling path for the stored energy in the inductor to dissipate itself and improves the overall load power factor. This method increases losses and reduces the efficiency of the inverter and because of large power dissipated (heat) across the resistor, the inverter size (KVA rating) has to be increased.[3]

- **Using feedback/freewheeling diodes**

This method provides a freewheeling path for the current across the BJT.

This is done by connecting diodes across the semiconductor switches as sown in Figure 2.8

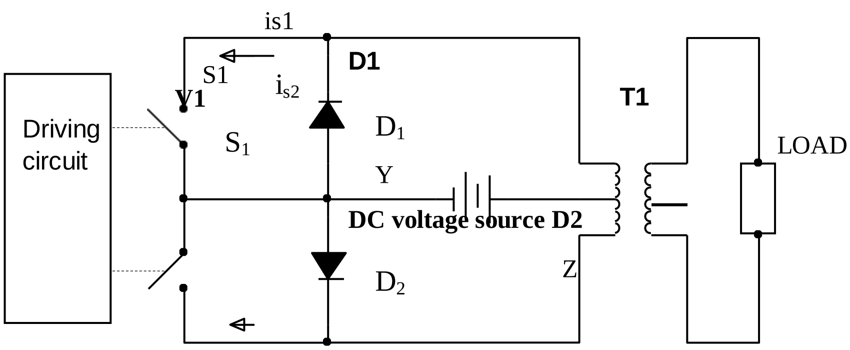


Figure 2.8 *Circuit of voltage source inverter (VSI) with purely inductive load and feedback diodes*

These diodes are referred to as feedback/ freewheeling diodes. When seen from the direction of the load the feedback/freewheeling diodes operate as rectifiers permitting reverse energy to flow from the load to the source.

Consider the instance when switch S_2 is closed and S_1 switch is open, as S_2 switch is opened and S_1 switch is closed, the current through S_2 becomes zero suddenly and unexpectedly but the energy in the inductive load tries to force

current in the same direction. This creates a surge voltage due to di/dt if no path is available for the current to flow. To avoid this situation, D_1 and D_2 diodes are connected across the switches S_1 and S_2 respectively, the transformer acts as a source and excess voltage more than the supply source forces current through the voltage source V_1 and through the diodes D_1. This continues till the transformer voltage becomes equal to or less than the supply voltage. So long as D_1 diode is conducting S_1 switch is reverse biased by the voltage drop of D_1 diode and cannot conduct. As soon as current flowing through D_1 diode becomes zero, S_1 switch starts to conduct if it is still closed. The same phenomenon occurs in the reverse cycle when switch S_1 is opened and S_2 switch is closed.

The average current(in a complete cycle) through the supply source is always zero in this case because no active power is drawn by pure inductive load.

2.4.3 Capacitive load

A capacitive load creates a similar problem as an inductive load for the voltage source inverter (VSI). The voltage becomes a square wave while the current waveform changes considerably due to capacitive loading[7. The voltage and current waveforms of the transformer primary for purely capacitive load are shown in figure 2.8

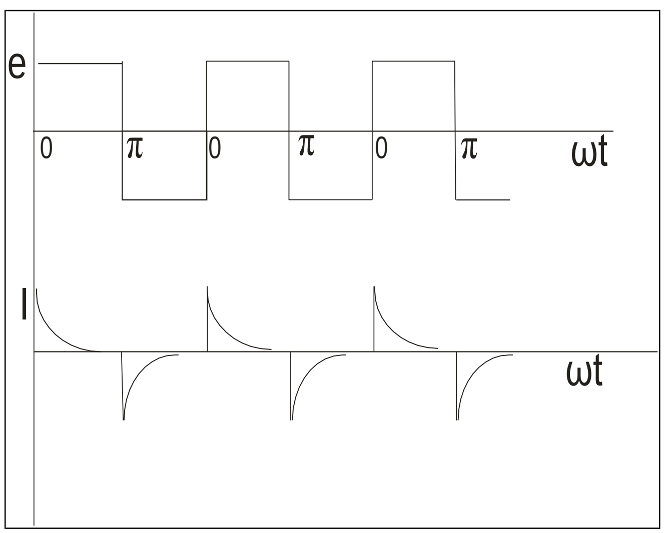


Figure 2.9 *Voltage and current wave form of capacitive load*

Each time the semiconductor switch starts to conduct, current spikes appear in the transformer primary because the square wave voltage of the transformer secondary supplies power to reverse-charges the capacitor through the very low impedance(in milli ohm) presented by the transformer windings and the reflected saturation resistance of the semiconductor switches. This current continues to flow till the charge across the capacitor build up sufficiently. Due to these large current peaks, the heat losses of the inverter rises to a greater value lowering its efficiency. Moreover the high value of di/dt exceeds the safe limit value of the semiconductor devices and permanently damages them. This problem is overcomed by some resistance in the circuit to limit the peak/maximum current but this increases the size of the inverter.

2.4.4 Motor load

The voltage source inverter (VSI) does not operate satisfactorily on motor loads. At the time of start, power/current requirements of a motor may be several times greater than required in the normal operation. This extreme transient condition may continue for many seconds depending on the speed of the motor's rotor. The power factor of the motor at this condition becomes extremely poor and i.e, the order 0.3 lagging. Even with a power factor improvement condenser connected across the motor, the low transient power factor during start- up can't be compensated. To deal with this transients, the current rating of the semiconductor devices/switches and the KVA rating transformer should be accordingly increased and devices should be properly protected by snubber circuit. Alternatively the motor inrush current could be lowered to a minimum value by inserting a current-limiting series resistor.

The loop response should be compatible with the motor, otherwise this will cause hunting in motors. That is sudden application/removal of motor load may generate high oscillations which may continue indefinitely if a proper damping arrangement is not included.

CHAPTER 3

DESIGN OF CONVERTERS

A microcontroller based three phase inverter was simulated using power MOSFET. IRF540 power MOSFETs is used in the simulation of the VSI inverter. IRF540 power MOSFETs were used because of the following reasons;

- They have feedback/freewheeling diodes internally connected between their drain and source
- Low ON state voltage
- High current carrying capability
- Low ON state resistance

  Design of Gate driver, boost converter, three phase inverter and low pass RLC filter is discussed in this chapter.

3.1 Gate Driver Circuit

Gate driver circuit is circuit integral part of power electronics converters which is used to drive power semiconductor devices like BJT’s, IGBT’s and MOSFETs. Output of DC-DC converters mainly depend on behavior of gate driver circuits. If gate driver circuit doesn’t drive the gate of MOSFET switch properly, designed DC- DC converter output will not be according to the requirement. Therefore design of the gate driver circuit is very important in designing of the power electronics converters.

In order to amplify the low voltage level (5V) from the microcontroller’s pin, boost strap IR2101 IC based gate driver circuit is always required. This circuit amplifies 5V of switching pulse to 14.75V. With a voltage amplitude of 14.75 V the IR540 N-MOSFET can be easily triggered.

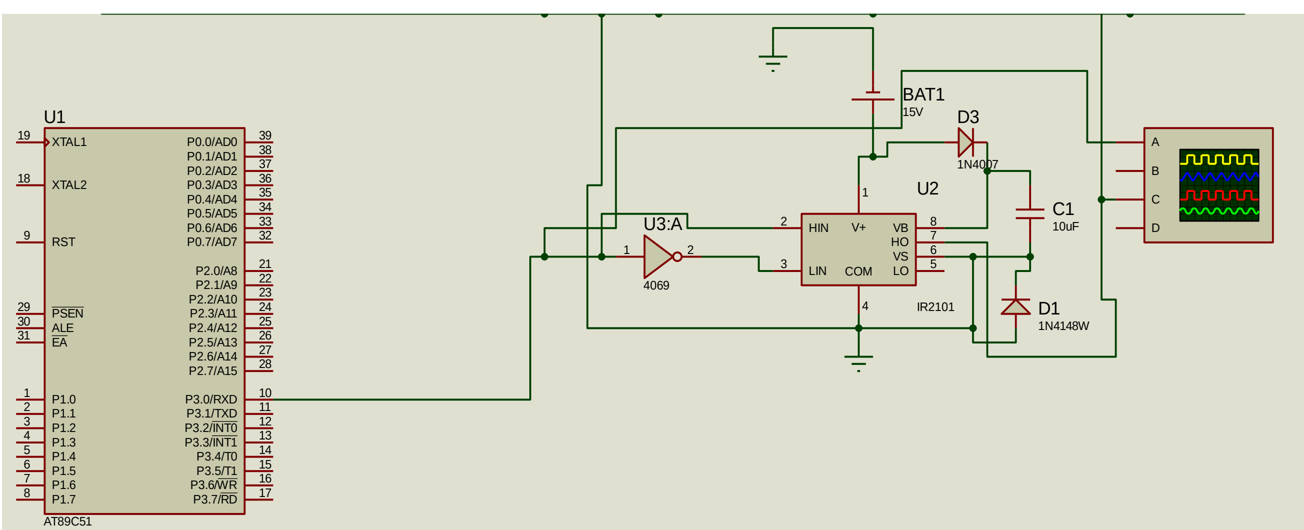


Figure 3.1 *circuit diagram IR2101 boost strap gate driver*

3.2 Boost Converter

The voltage output from solar panel is very low in magnitude, hence we need a converter which can step up this voltage. In order to raise the voltage magnitude, power electronic DC to DC step up converter called boost converter is needed.

3.2.1 General configuaration of Boost Converter

In a boost converter, the output voltage is greater than the input supply voltage – hence the word "boost" is used. A boost converter having a MOSFET as a switch is shown in figure below.

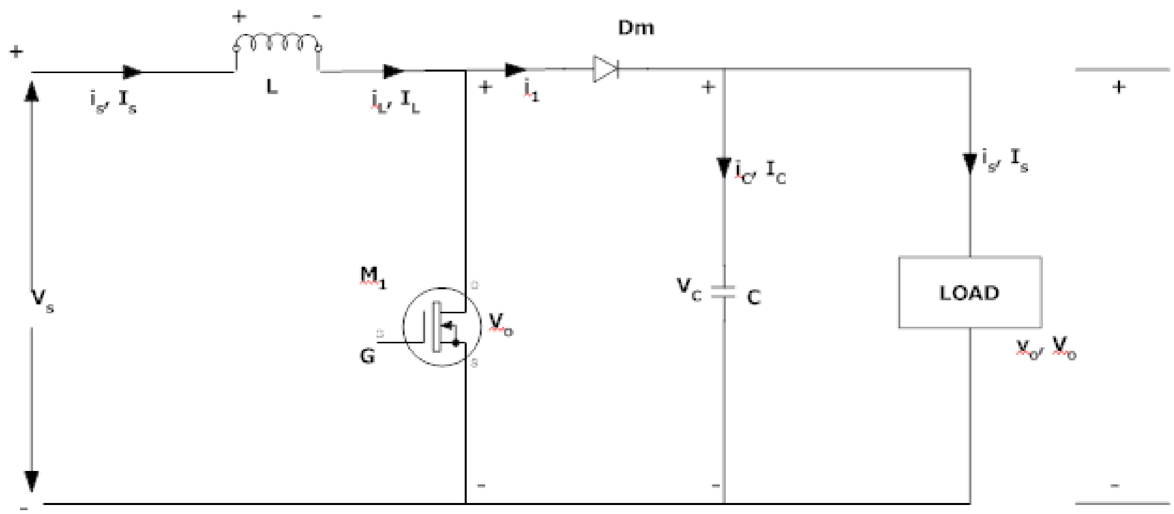
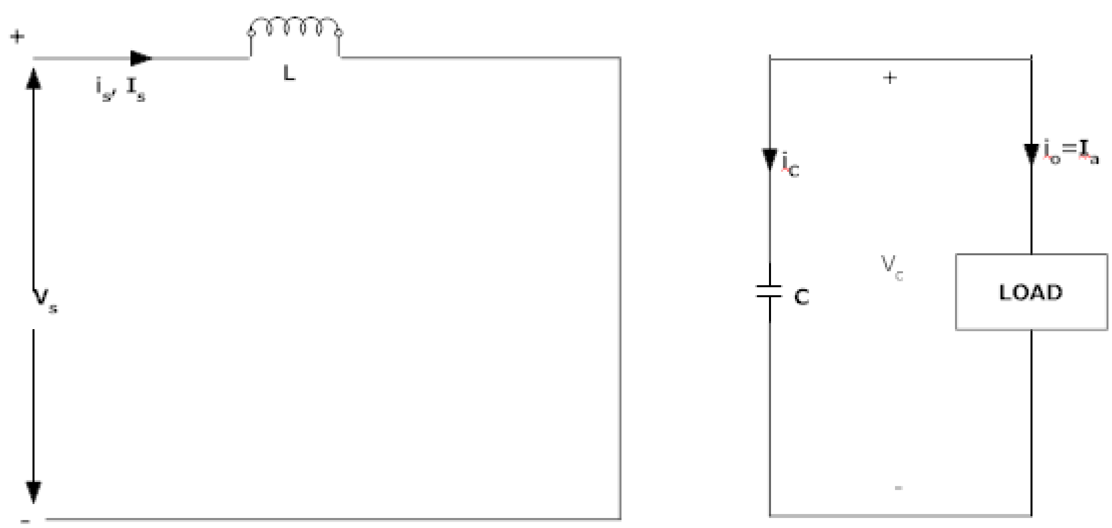


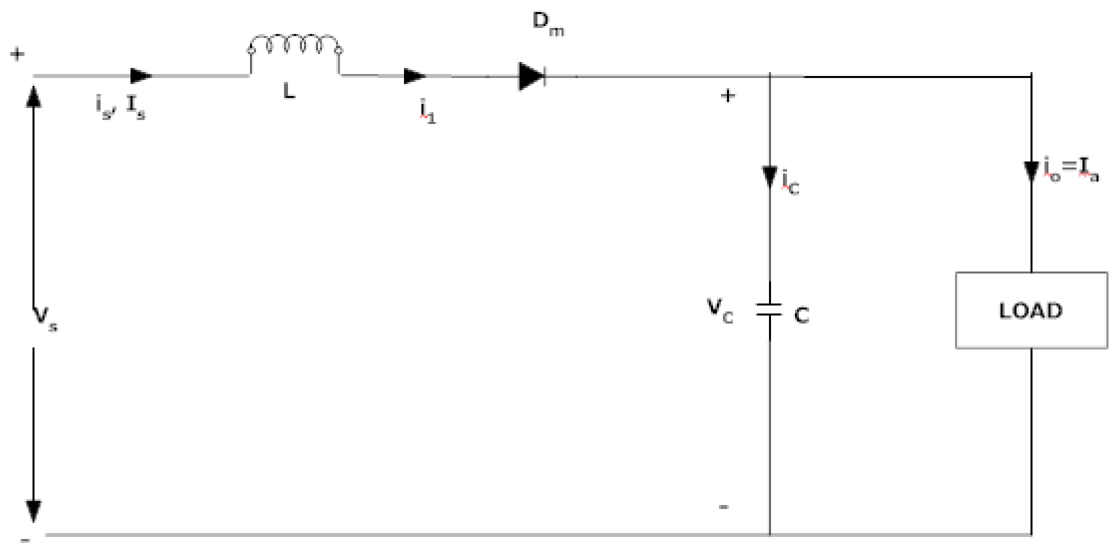
***Figure 3.2** Circuit diagram of Boost Converter.*

The function of boost converter can be dealt in two modes, Mode 1 & Mode 2. **Mode 1** starts MOSFET is turned on at time t=0. The input current rises and flows through inductor L and MOSFET M 1.

Mode 2 starts when MOSFET M_1 is turned off at time t = t_1. The input current now flows through inductor L, capacitor C, load, and diode D. The inductor current falls until the next cycle. The energy stored in inductor L flows through the load



(a)



(b) ***Figure 3.3*** *(a) & (b) Circuits for the two modes of operation*

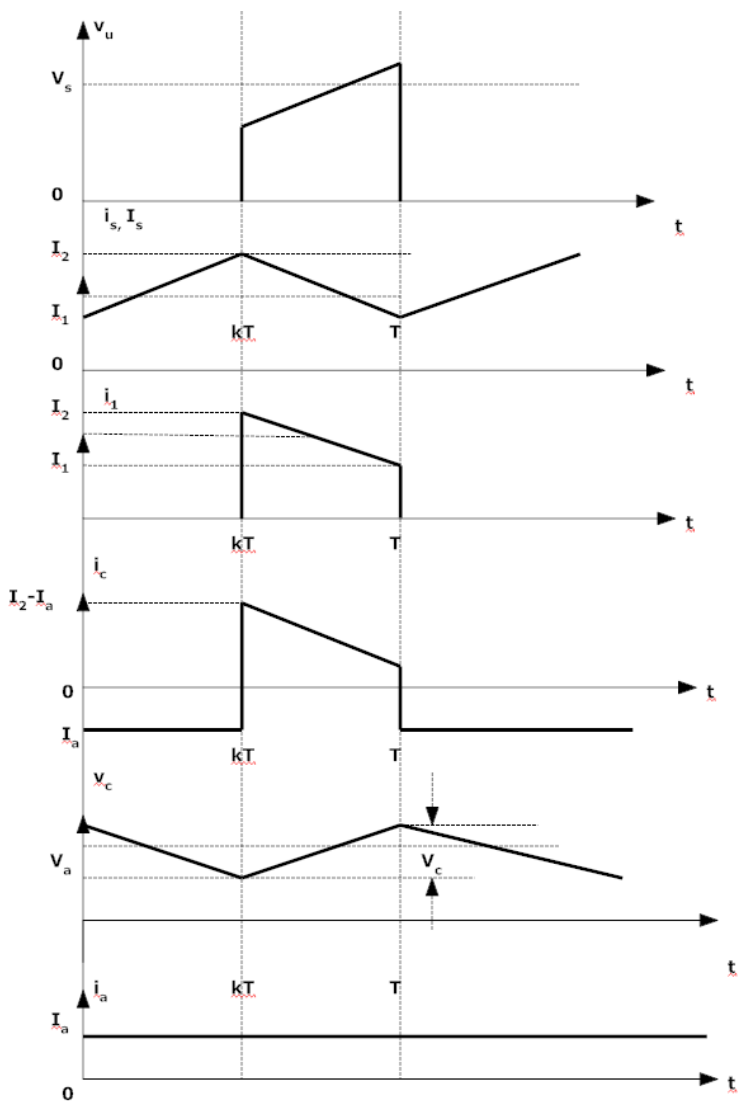


Figure 3.4 *Waveforms of the voltages and currents*

3.2.3 Calculations of Boost Converter

Input Voltage (v_s) = 150 V

Input Resistance (r) = 1.5 Ohms

Output Voltage (v_o) = 200 V

Output Current (i_o) = 5 A

Ripple in input current (m) = 10% of output current = 5*0.1= 0.5A

Ripple in output voltage (n) = 3% =0.03*200= 6 V

Duty Cycle (D) = $1 - \frac{v_s}{vo}$ = 1-(150/200) = 0.25

Input Current (i_i) = 6.66 A

Load Resistance (r_o) = v_o/i_o = 200/5= 40 Ohms

MOSFET ON state resistance(r_m) = 0.3 Ohms

Critical Inductance(L_c) = (D*v_s)/($f * m$) = (0.25*150)/(20000*0.5) = 5mH

Critical Capacitor (C_c) = (D*i_o)/($f * n$) = (0.25*5)/(20000*6)= 150uF

LOSSES

MOSFET loss = (v_m*v_m* D)/ r_m) =4*4*0.25/6 = 13.33 W

Input losses = (i_i *i_i)*r =1.5*1.5*6.66 = 2.25*6.67= 15 W

Diode Losses = (1- D)*(v_d*i_i + i_i *i_i *r_d)= (1-0.25)*(2*6.66 + 6.66*6.66*0.5)= 26.62 W

Losses = 26.62+15+13.33 =55 W

EFFICIENCY

Efficiency = 1-(losses/input power) = 1-(55/(150*6.66)= 94.49%

3.3 Design of Inverter

3.3.1 180° conduction Mode

Input Voltage (v_i) = 200 V

MOSFET ON state resistance(r_m) = 0.28 Ohms

Per phase resistance (Y connected load, r) = 10 Ohms

Source Current (i_s) = 12.8 A

Voltage per phase v_o (RMS) = 91.4 V

Line or Phase current =v_o/r = 94.266/10 =9.14 A

Switch current (RMS) (i_{sw}) = $v_s/3r$ =6.56A

MOSFET Voltage Drop(v_m) = 1.84 V

Input power = 200*12.8= 2560 W

Output Power = 3*v_o *v_o / r = 3*91.4*91.4/10 =2506.8 W =2.5068 kW

Losses

Input power –output power =2560-2506.8 =53.8W, $g = \frac{v_1}{v_{or}} = \frac{3}{\pi}$ THD = $\sqrt{\frac{1}{g^2} - 1}$

THD = 31.08%

3.3.2 120° conduction Mode

Input Voltage (v_i) = 200 V

MOSFET ON state resistance(r_m) = 0.28 Ohms

Per phase resistance (Y connected load,r) = 10 Ohms

Source Current(i_s) = 9.63 A

Voltage per phase v_o (RMS) = 78 V

Line or Phase current =v_o/r = 78/10 =7.8 A

Switch current (RMS) (i_{sw}) = $v_s/3r$ =5.55A

MOSFET Voltage Drop (v_m) = 1.56V

Input power = 200*9.63= 1926 W

Output Power = 3*v_o *v_o / r = 3*78*78/10 =1825.2 W =1.825 kW

Losses

Input power –output power =1926-1825.2 =100.2W, $g = \frac{v_1}{v_{or}} = \frac{3}{\pi}$, THD = $\sqrt{\frac{1}{g^2} - 1}$

which gives THD = 31.08%

3.4. Design of Low Pass Filter

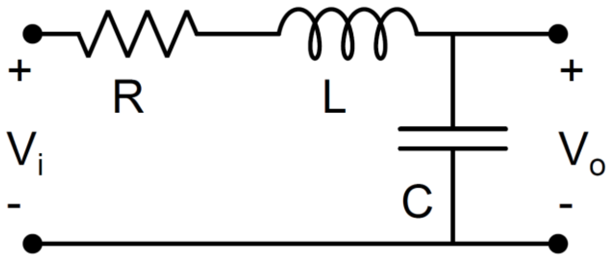


Figure 3.5 *Second Order Low Pass Filter*

Transfer Function is given

$$\frac{vo}{vi} = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \qquad (3.1)$$

3.4.1 Filter for 180° conduction mode

Cut off frequency

$$fc = \frac{1}{2\pi\sqrt{LC}} \qquad (3.2)$$

Cut-off and required frequency of oscillation = 50Hz

ω =2*3.14*50 = 314 radian per second

Taking Quality factor = Q = 3.2 and C = 100uF

and the quality factor Q

$$Q = \frac{1}{\omega_0 CR} = \sqrt{\frac{L}{C}}\frac{1}{R} \qquad (3.3)$$

Q = ω L/R (3.4)

3.2 = 1/ (314*100*R)

R = 9.8 Ohms

From Equation

3.2 = (314*L)/9.8

L= 100 mH

From equation (3.1)

Transfer Function:

$$G(s) = \frac{100000}{s^2 + 98s + 100000}$$

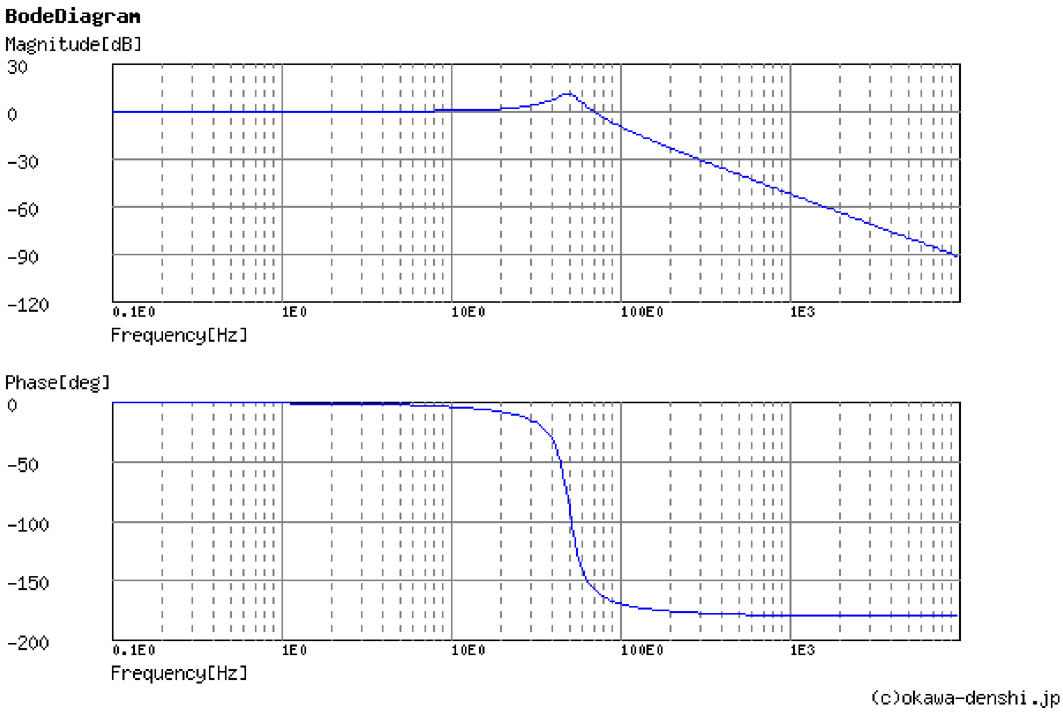


***Figure 3.6** Gain and Phase characteristics of filter (Bode Diagram)*

Damping ratio

$Q = 1/2\,\zeta$, $3.2 = 1/2\,\zeta$ (3.5)

Which gives

$\zeta = 0.155$

3.4.2 Filter Design for 120° conduction mode

Cut off frequency

$$fc = \frac{1}{2\pi\sqrt{LC}}$$

Cut-off and required frequency of oscillation = 50Hz

ω =2*3.14*50 = 314 radian per second

Taking Quality factor = Q =4 and C = 100uF and the quality factor Q

$$Q = \frac{1}{\omega_0 CR} = \sqrt{\frac{L}{C}}\frac{1}{R}$$

$Q = \omega L/R$

4 = 1/(314*100*R)

R = 7.8 Ohms

From Equation

4 = (314*L)/7.8

L=100mH

Transfer Function:

$$G(s)=\frac{100000}{s^2+78s+100000}$$

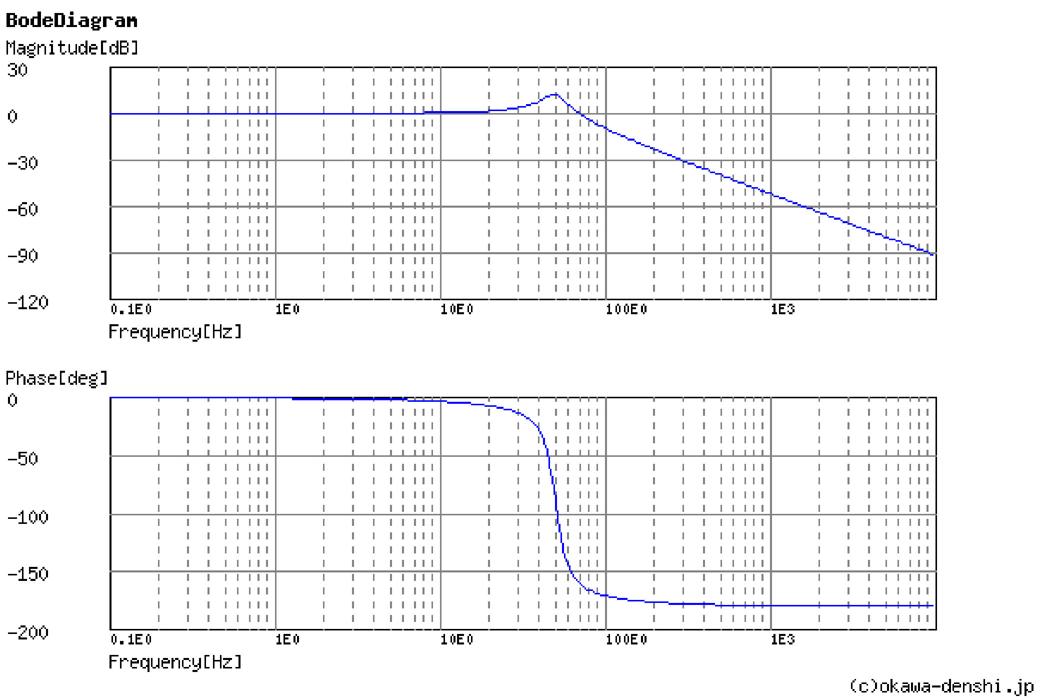


Figure 3.7 *Gain and Phase characteristics of filter (Bode Diagram)*

Damping ratio

$Q = 1/2\ \zeta$, which gives, $4=1/2\ \zeta$, $\zeta = 0.123$

3.4.3 Gain Calculation of the Filter using Transfer Function

The cutoff frequency of both the filters used is 50Hz,which means that it will pass only the first harmonic component of the inverter output i.e, the filter will pass only the fundamental component.
Transfer Function is given by

$$\frac{vo}{vi} = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$$

Where Vo is the inverter output voltage and Vi is the fundamental component of unfiltered square output voltage .

$$\frac{v_0}{v_i} = \frac{\omega^2}{\frac{1}{L^2C^2} - \omega^2 + j\omega\frac{R}{L}}$$

Gain is given by

$$\left|\frac{v_0}{v_i}\right| = \frac{\omega^2}{\sqrt{\left(\frac{1}{L^2C^2} - \omega^2\right)^2 + \omega^2\frac{R^2}{L^2}}}$$

For **180° conduction mode's filter**

R=9.8 ohms , L=100 mH C=100uF,

$$\left|\frac{v_0}{v_i}\right| = \frac{100000^2}{\sqrt{(100000^2 - 314^2)^2 + (98^2.314^2)}}$$

$$\left|\frac{v_0}{v_i}\right| = 3.58$$

$v_i = 90.3$ V (RMS of fundamental calculated from equation (2.6))

For **120° conduction mode's filter**

R=7.8 ohms , L=100 mH C=100uF,

$$\left|\frac{v_0}{v_i}\right| = \frac{100000^2}{\sqrt{(100000^2 - 314^2)^2 + (78^2.314^2)}}$$

$$\left|\frac{v_0}{v_i}\right| = 4.076$$

$v_i = 77.9$ V (RMS of fundamental calculated from equation (2.8)

CHAPTER 4

CIRCUIT AND WAVEFORMS

4.1 Circuits

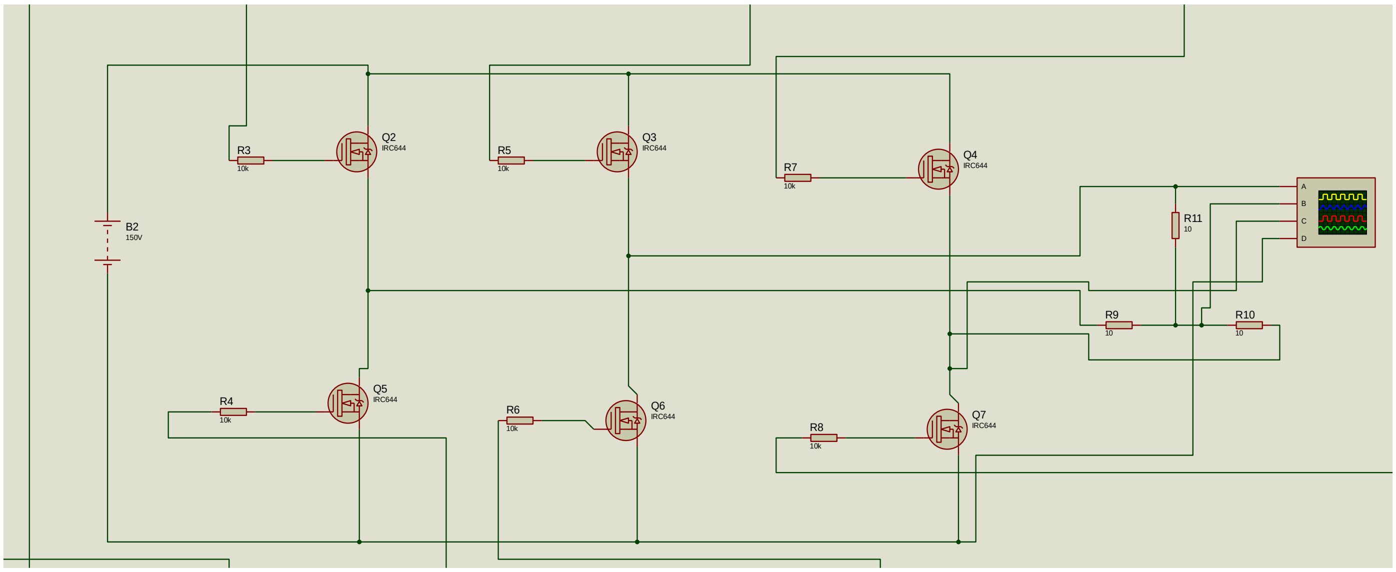


Figure 4.1 *Circuit of Bridge Inverter*

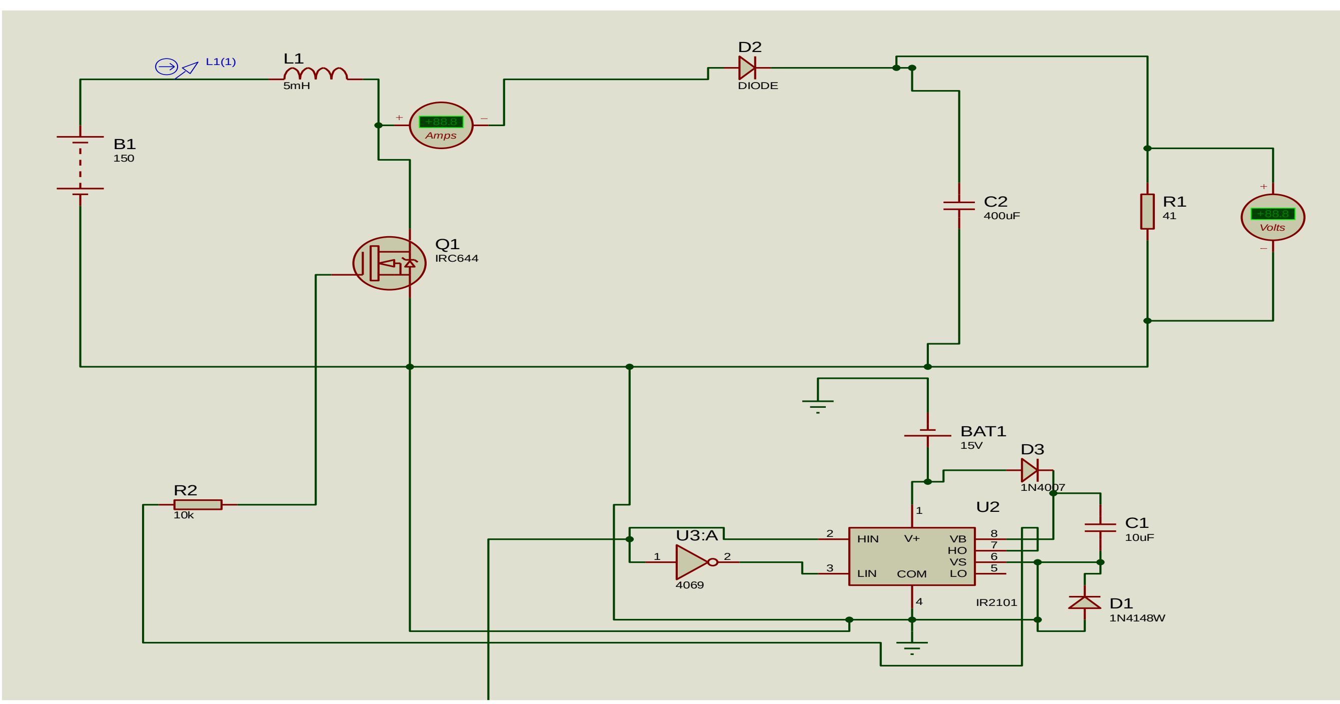


Figure 4.2 *Circuit of Boost Converter*

4.2 Inverter Waveforms

4.2.1 Phase and Line Voltages(Without RLC filter)

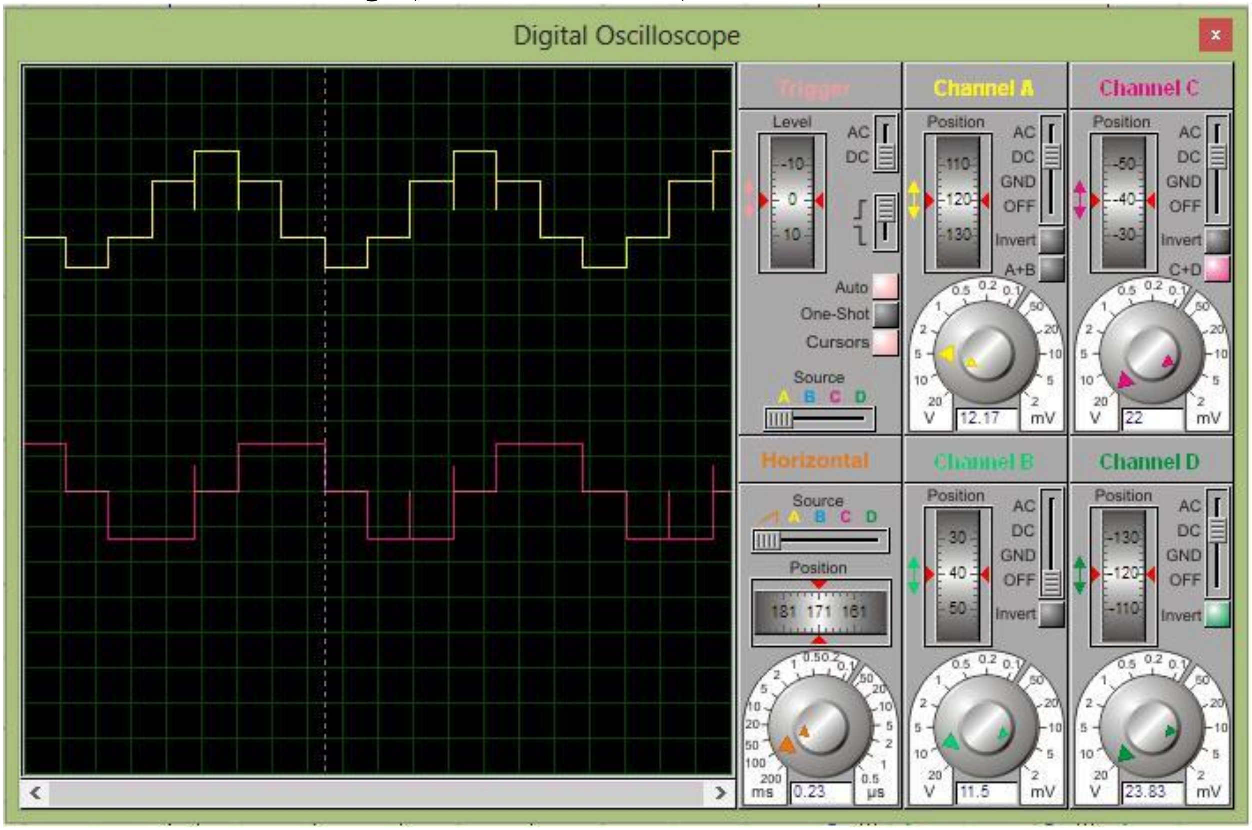


Figure 4.3 *Phase and Line Voltages (180˚ conduction mode)*

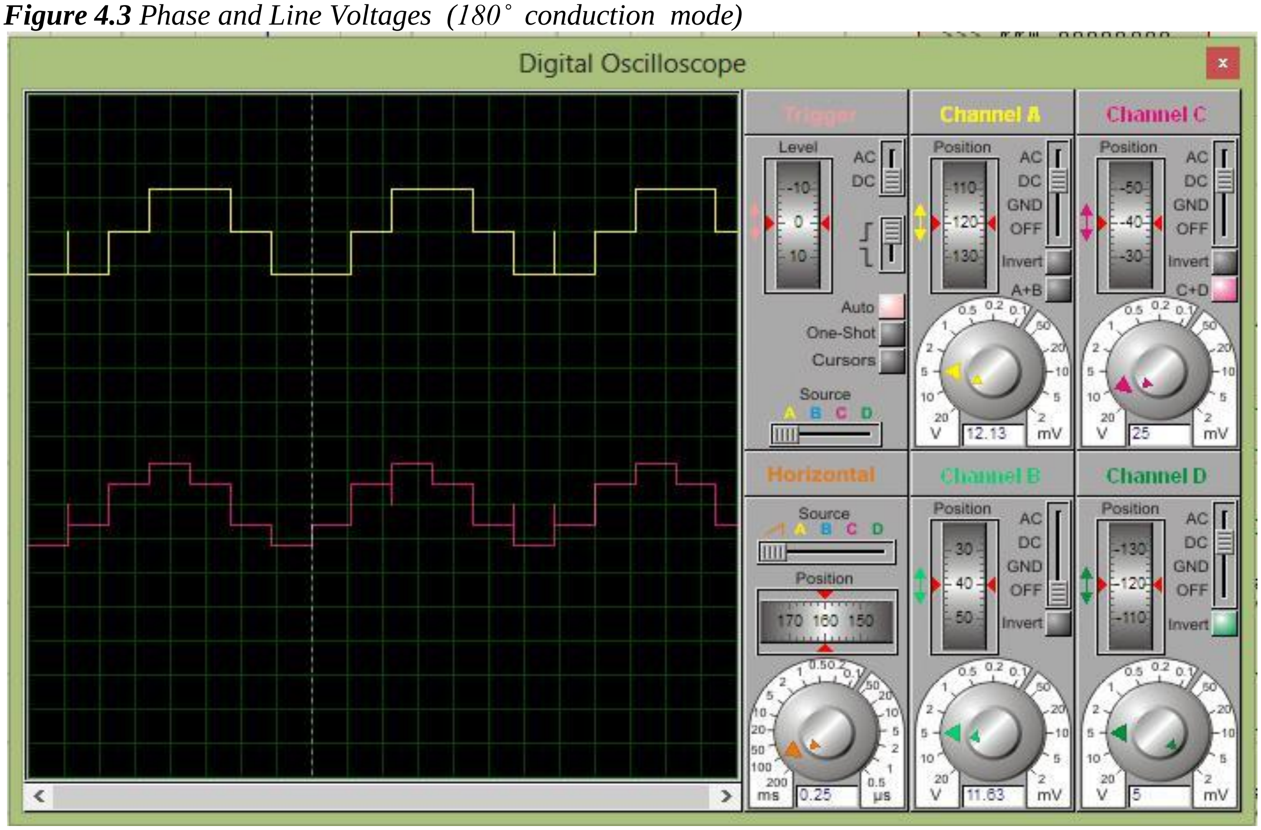


Figure 4.4 *Phase and Line (120˚ conduction mode)*

4.2.2 Phase and Line Voltages (With RLC filter)

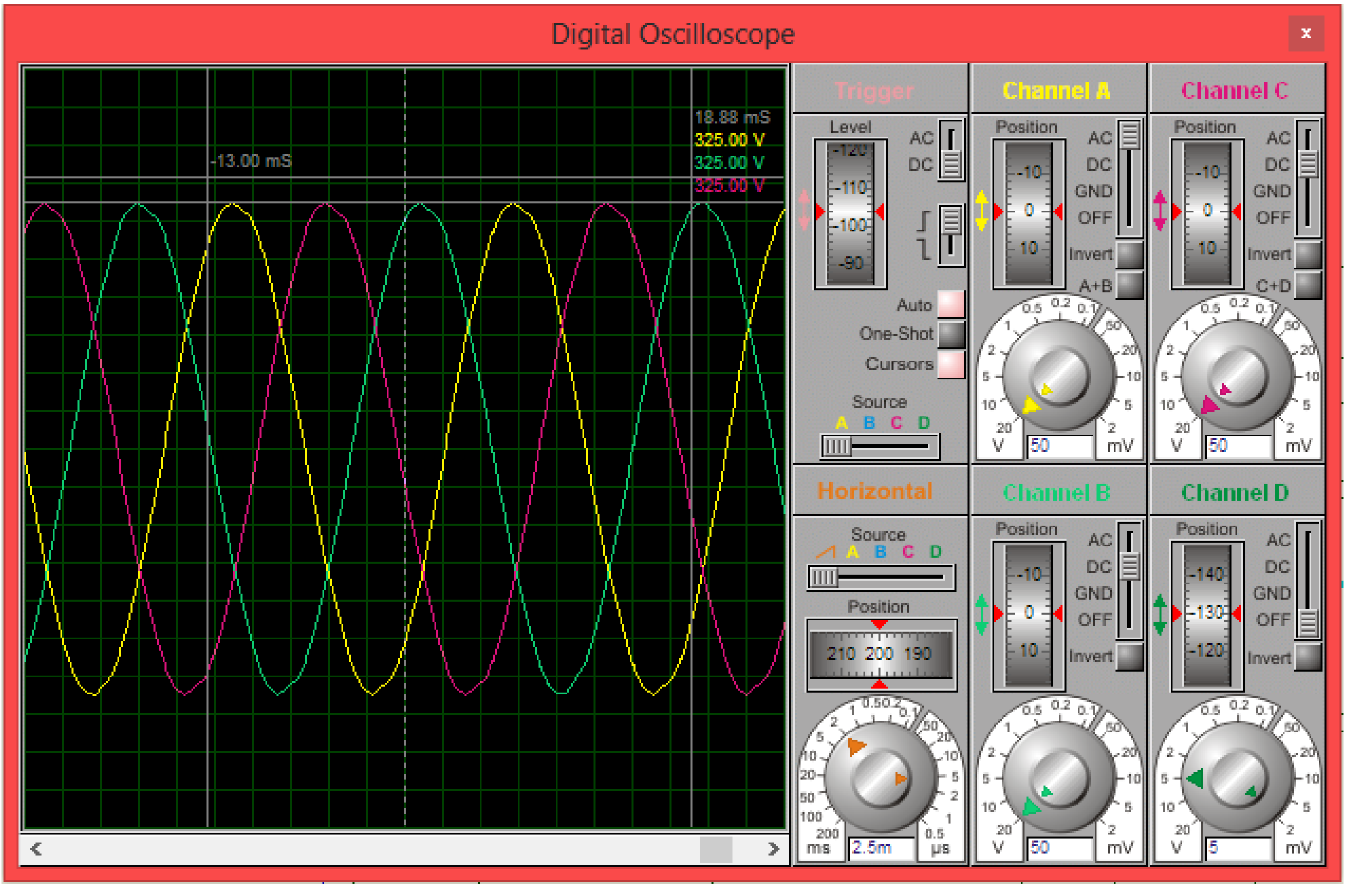


Figure 4.5 *Three phase voltages of Inverter (180˚ conduction mode)*

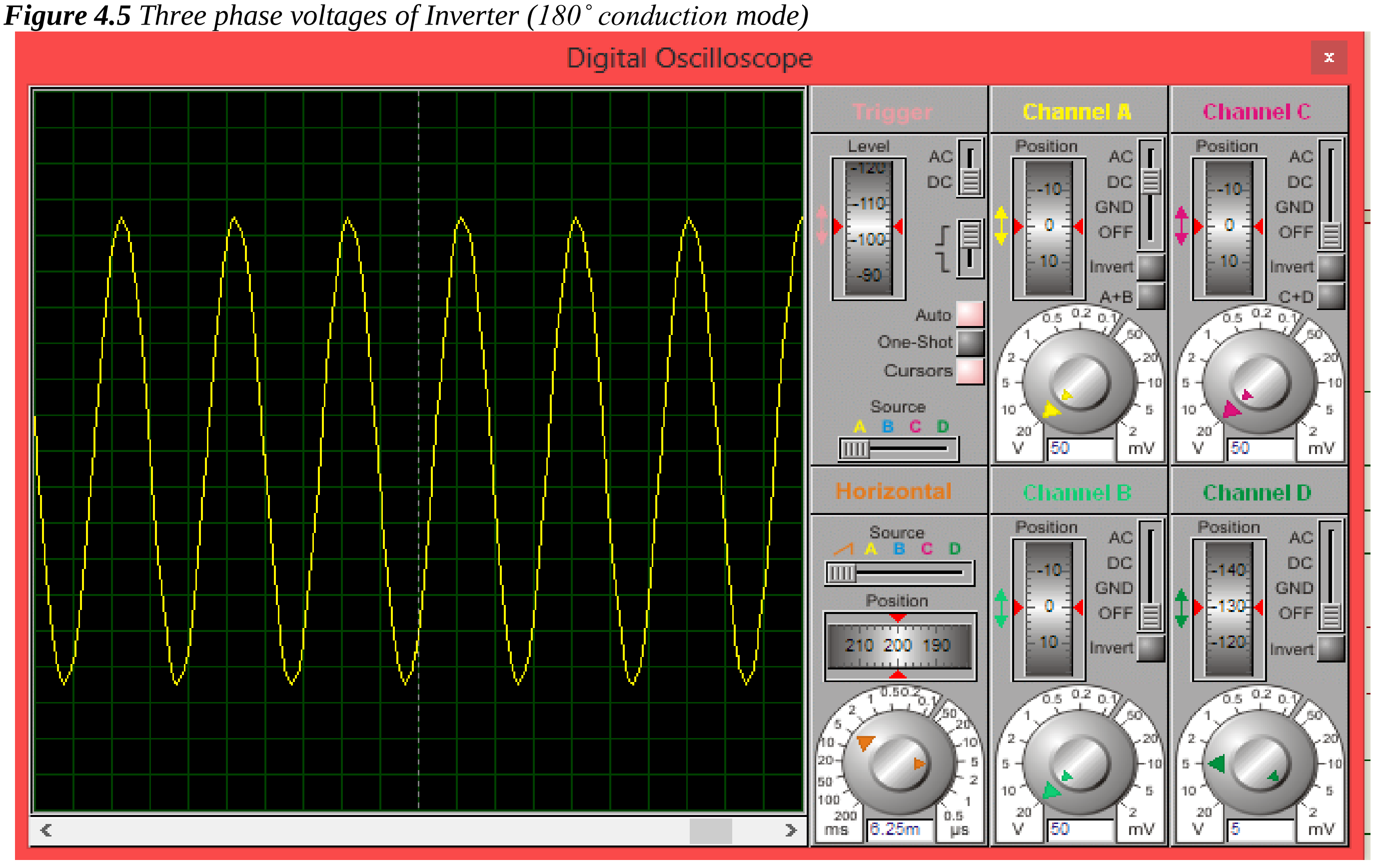


Figure 4.6 *Line voltage of Inverter (180˚ conduction mode)*

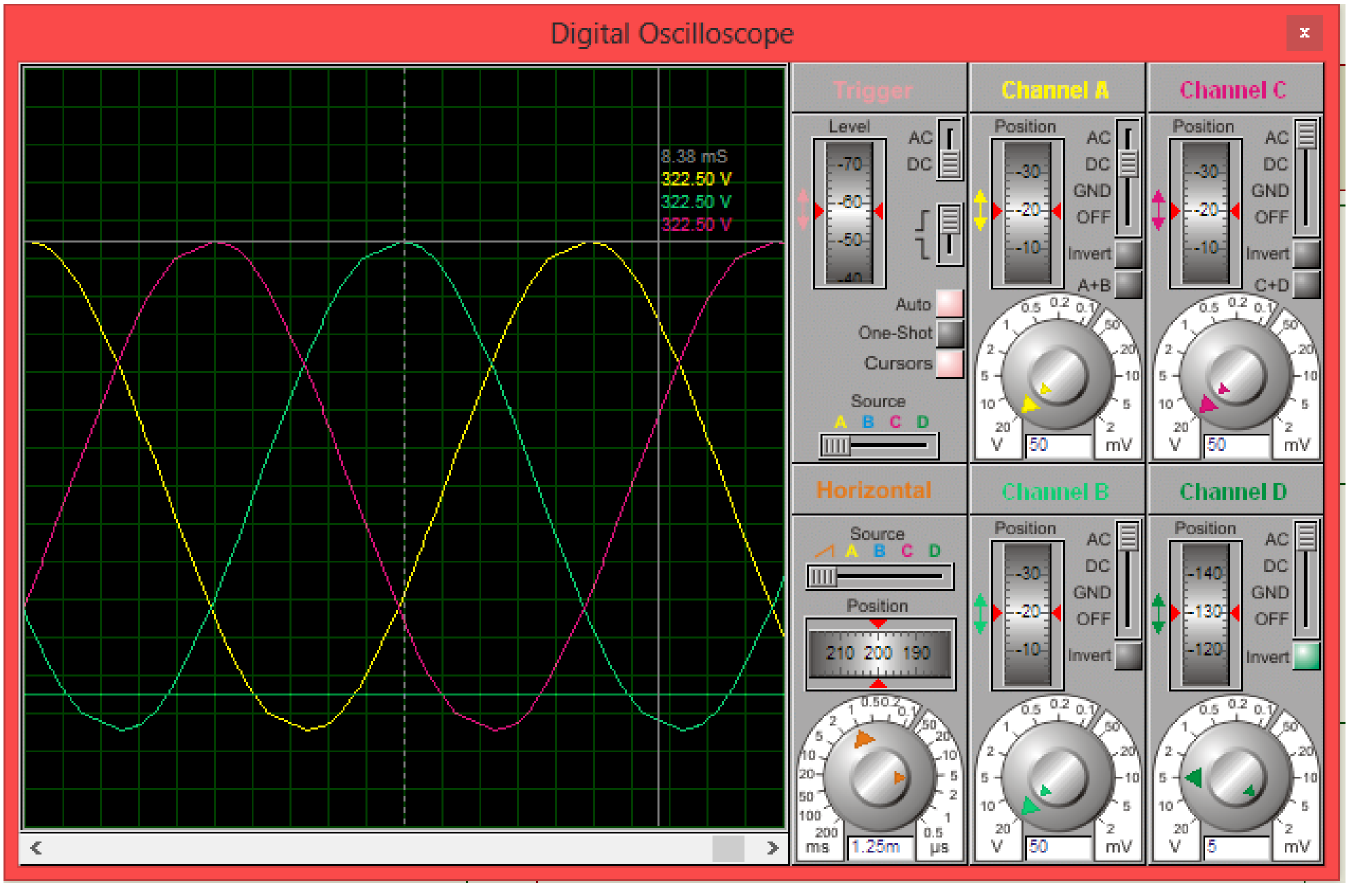


Figure 4.7 *Three phase voltages of Inverter (120˚ conduction mode)*

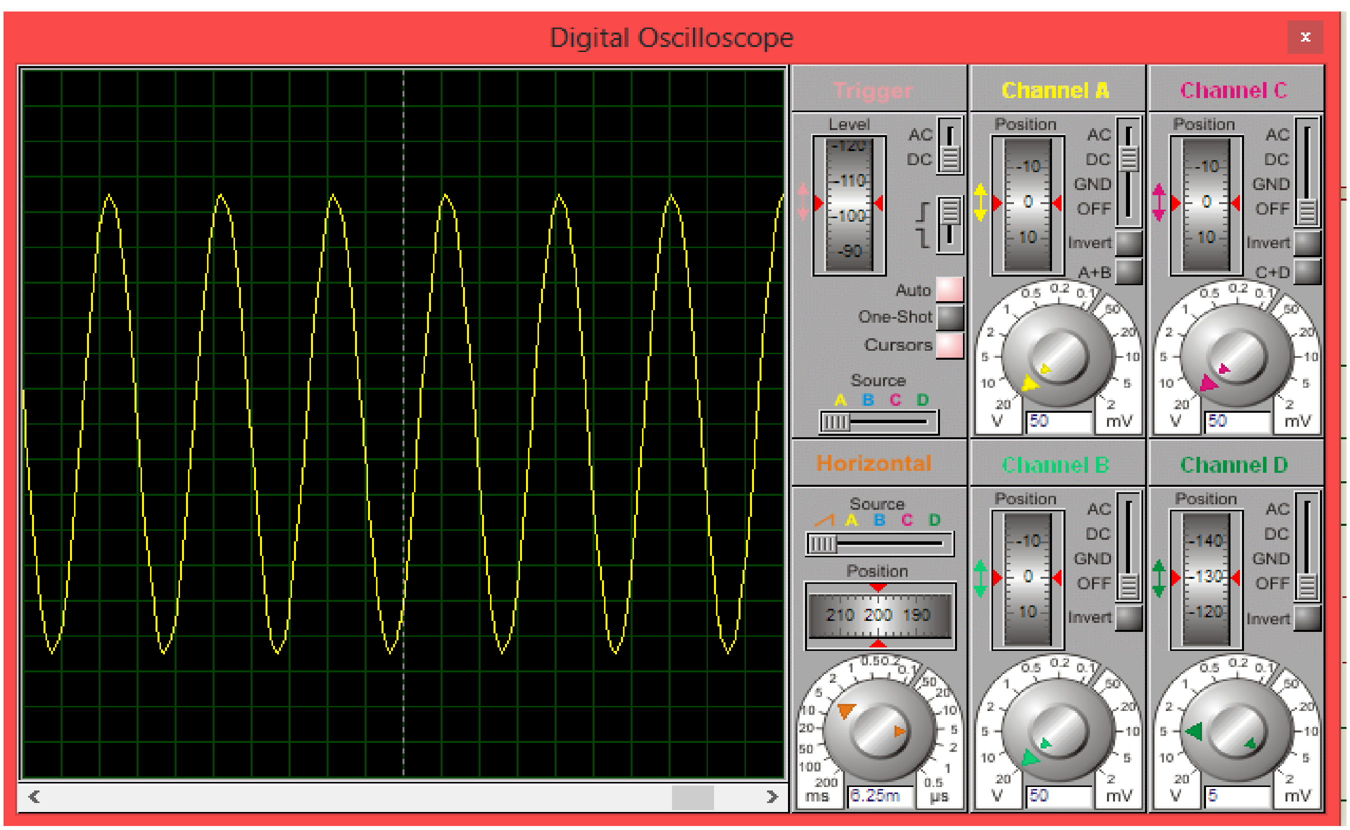


Figure 4.7 *Three phase voltages of Inverter (120˚ conduction mode)*

4.3.1 Boost Converter's Waveforms (Voltage)

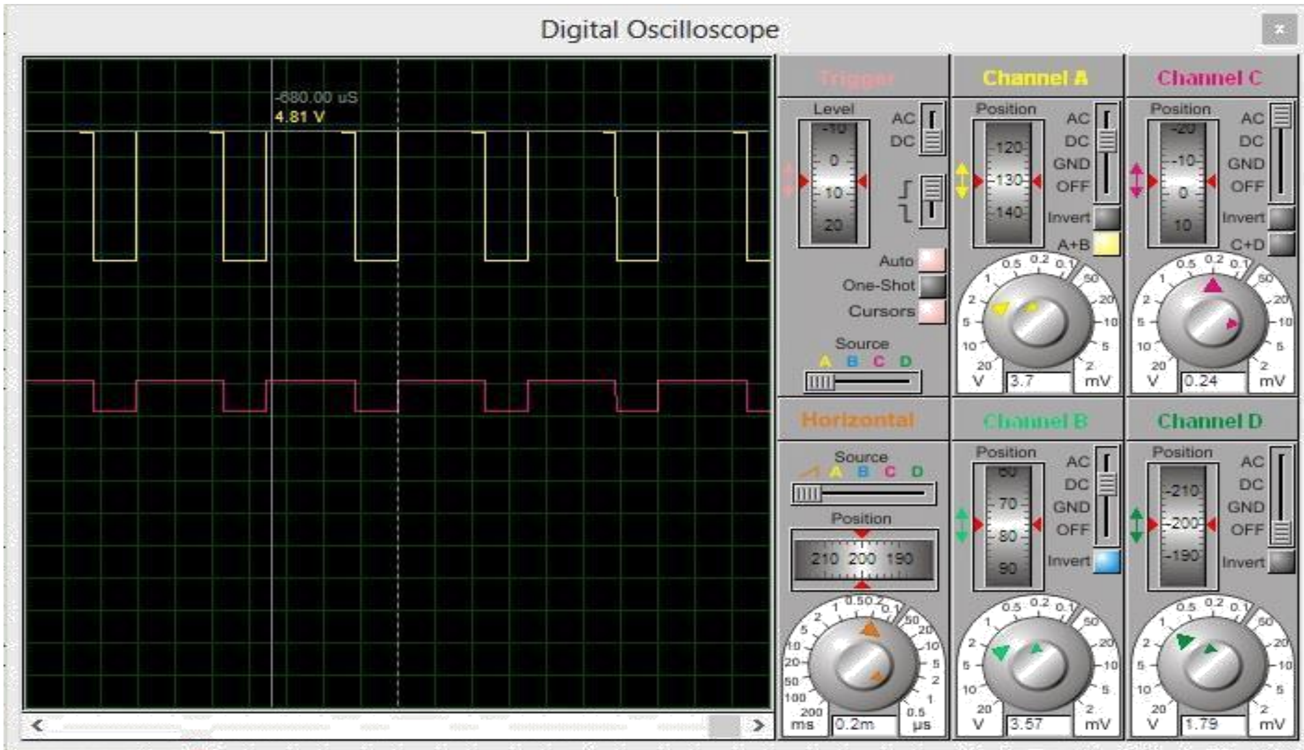


***Figure 4.9** Inductor Voltage and Switching Pulse Voltage*

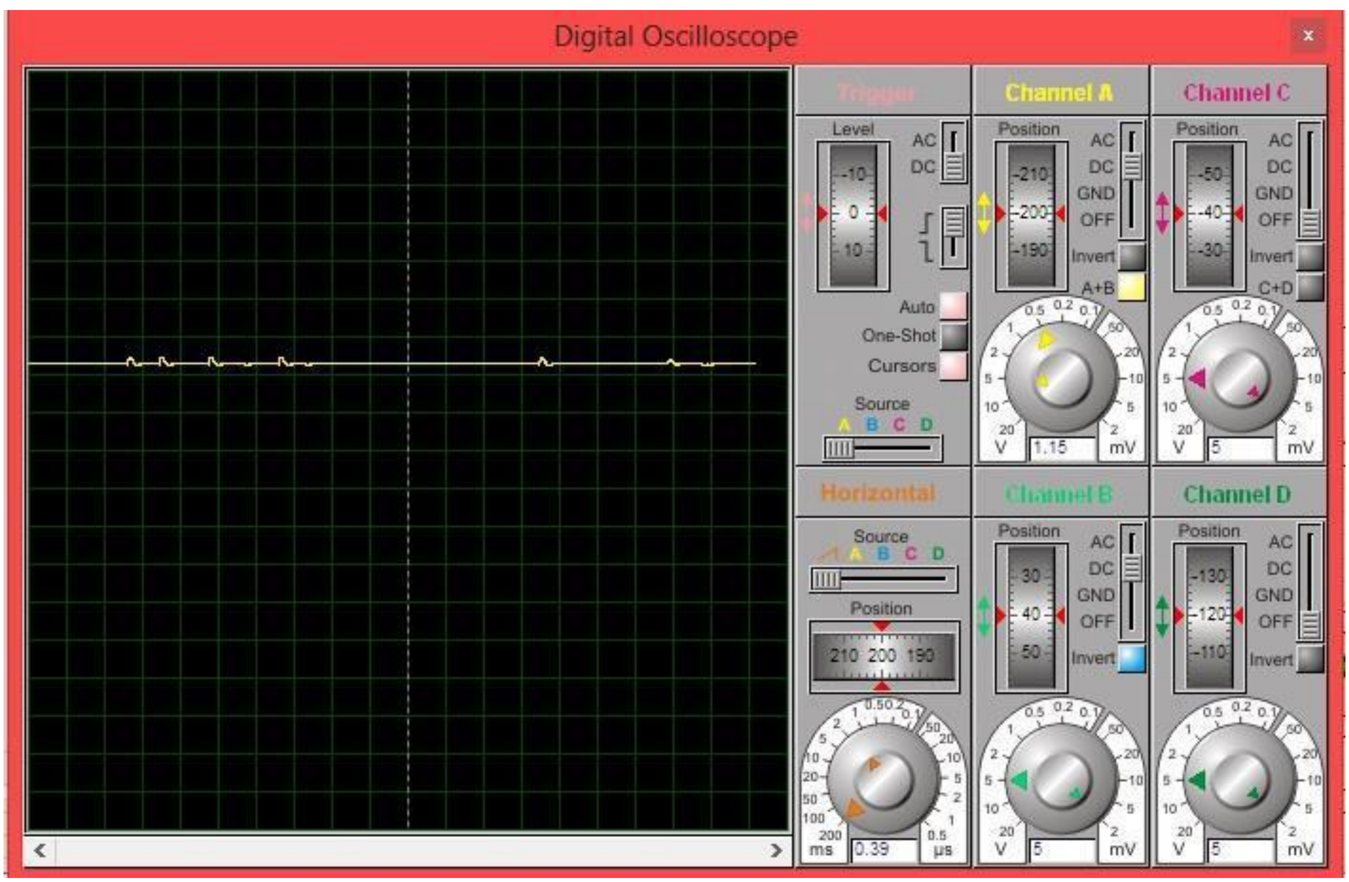


***Figure 4.10** (VOUT (output voltage) vs Time)*

4.3.2 Boost Converter's Waveforms (Current)

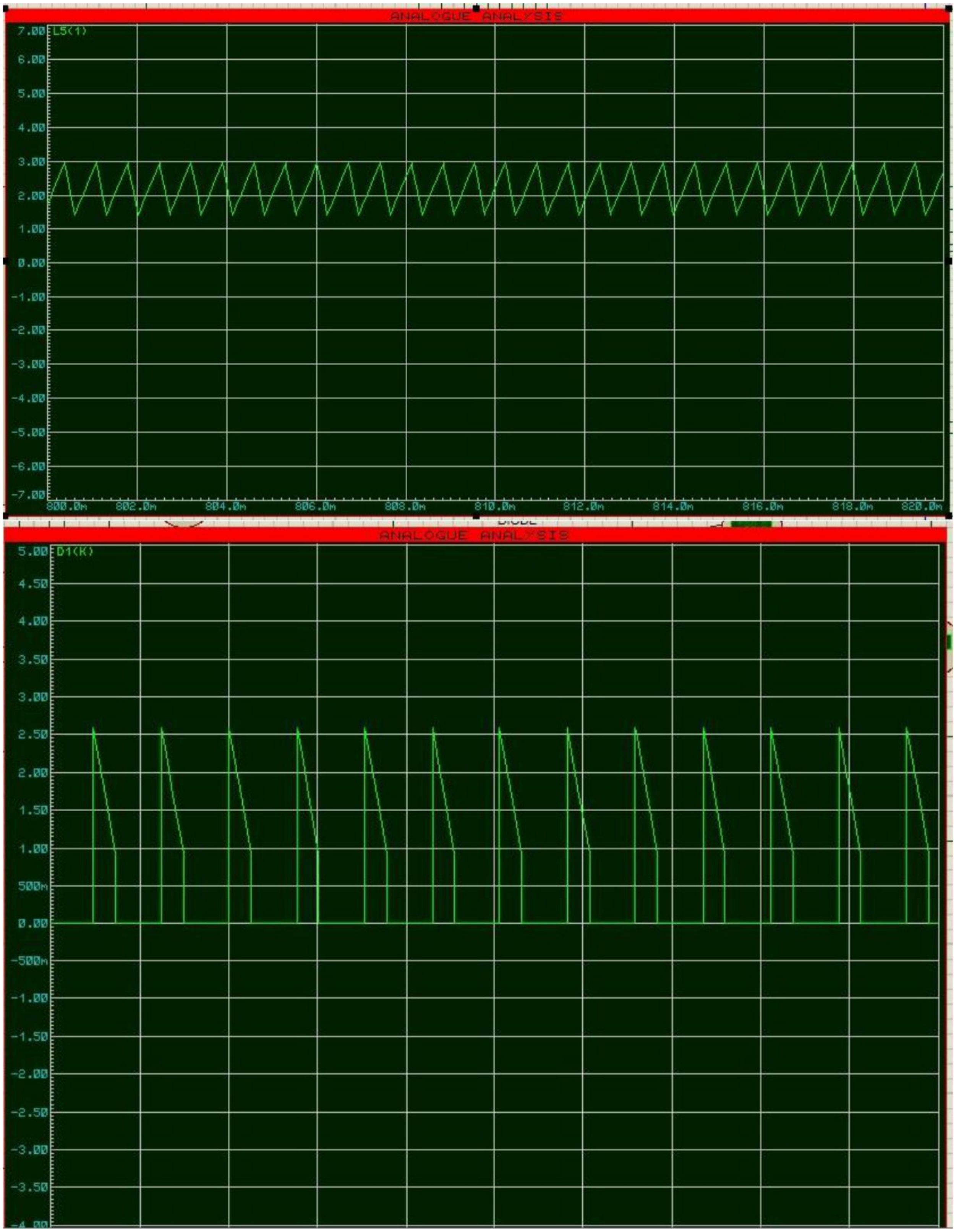


Figure 4.11 (a) *Inductor and* ***(b)*** *Diode Current.*

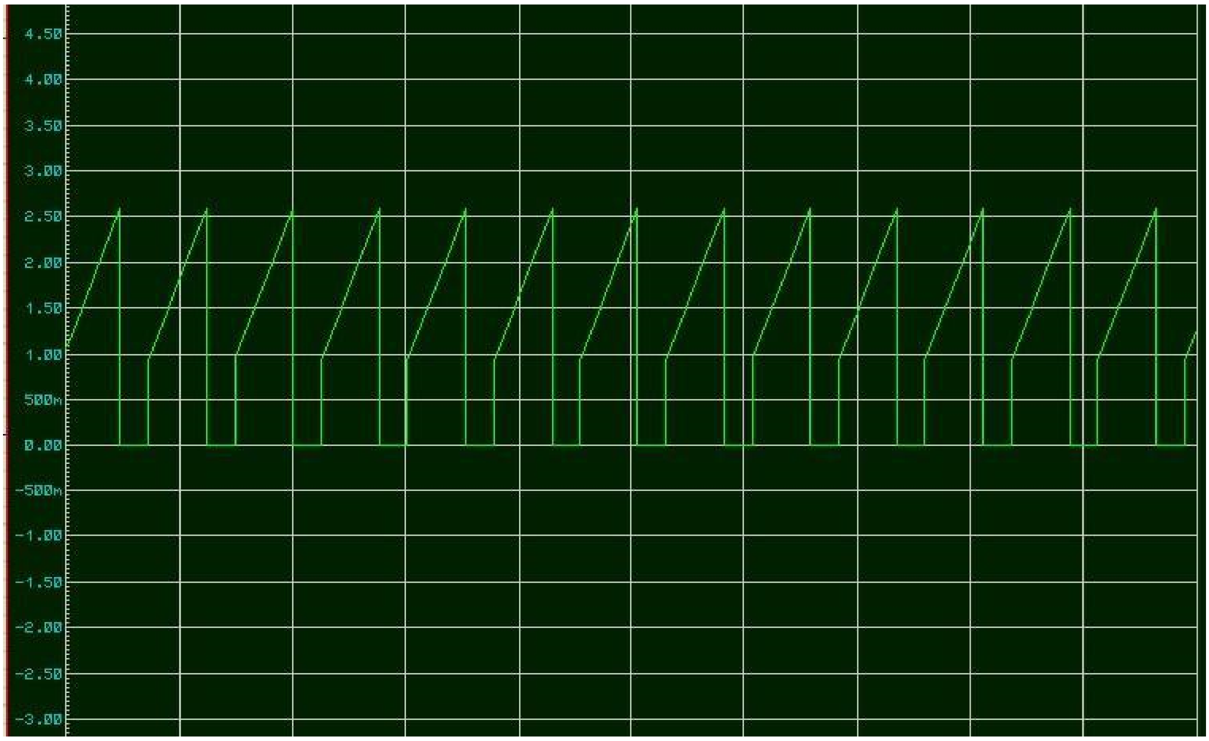


__Figure 4.12__ Switch Current vs Time.

4.4 Switching Pulses

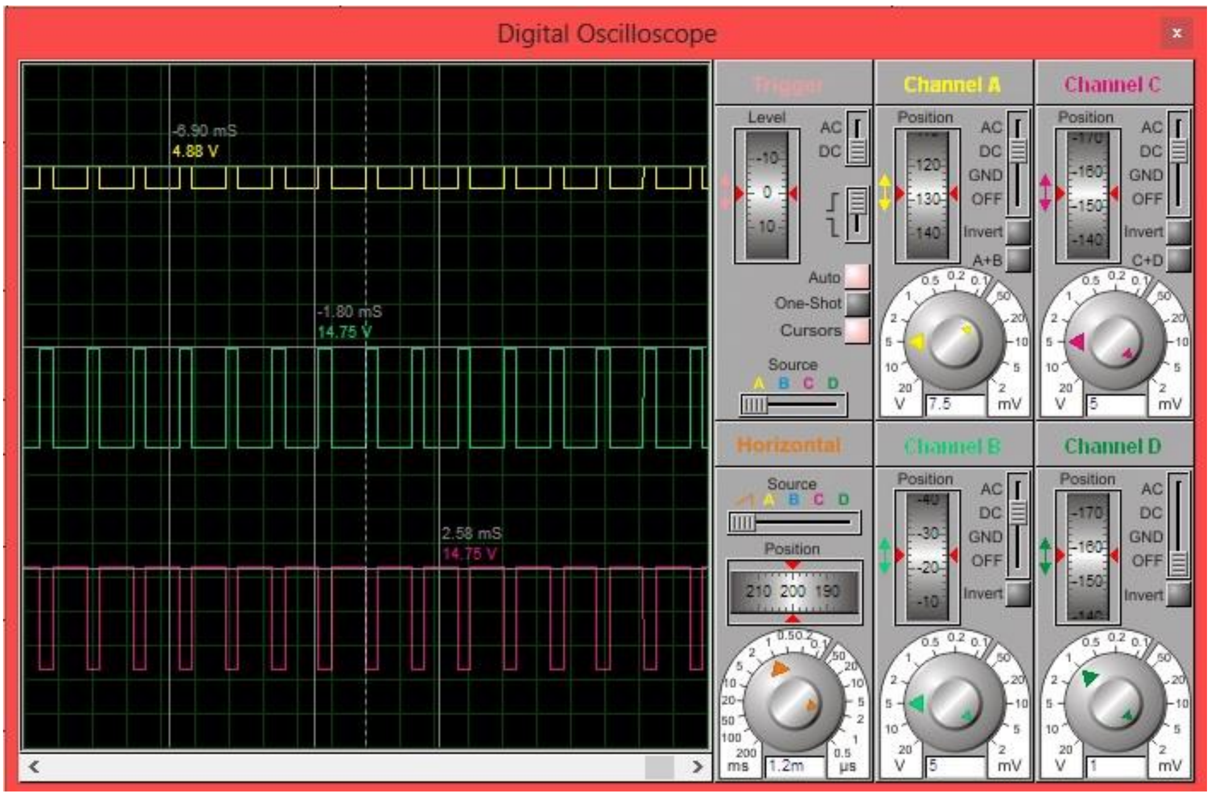


__Figure 4.13__ Microcontroller's and gate driver's output switching pulse waveform

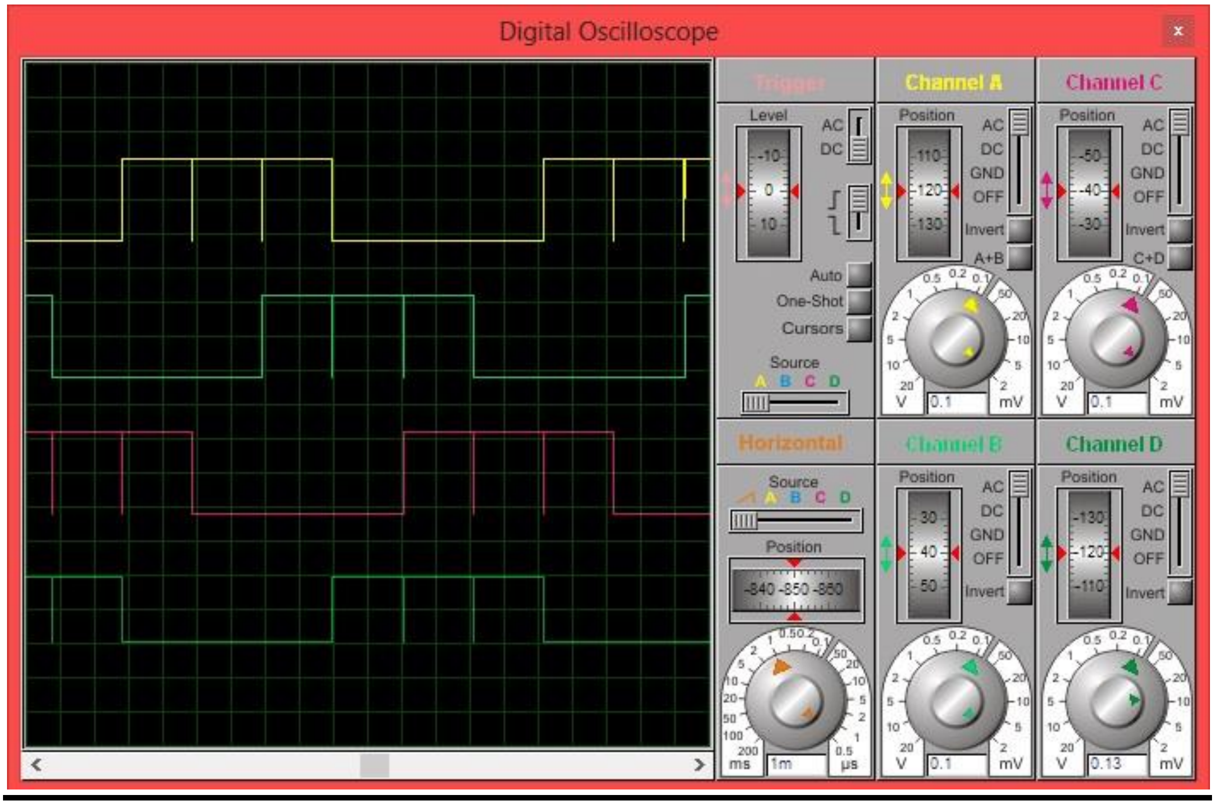


Figure 4.14 *Switching pulses waveform 180˚ conduction*

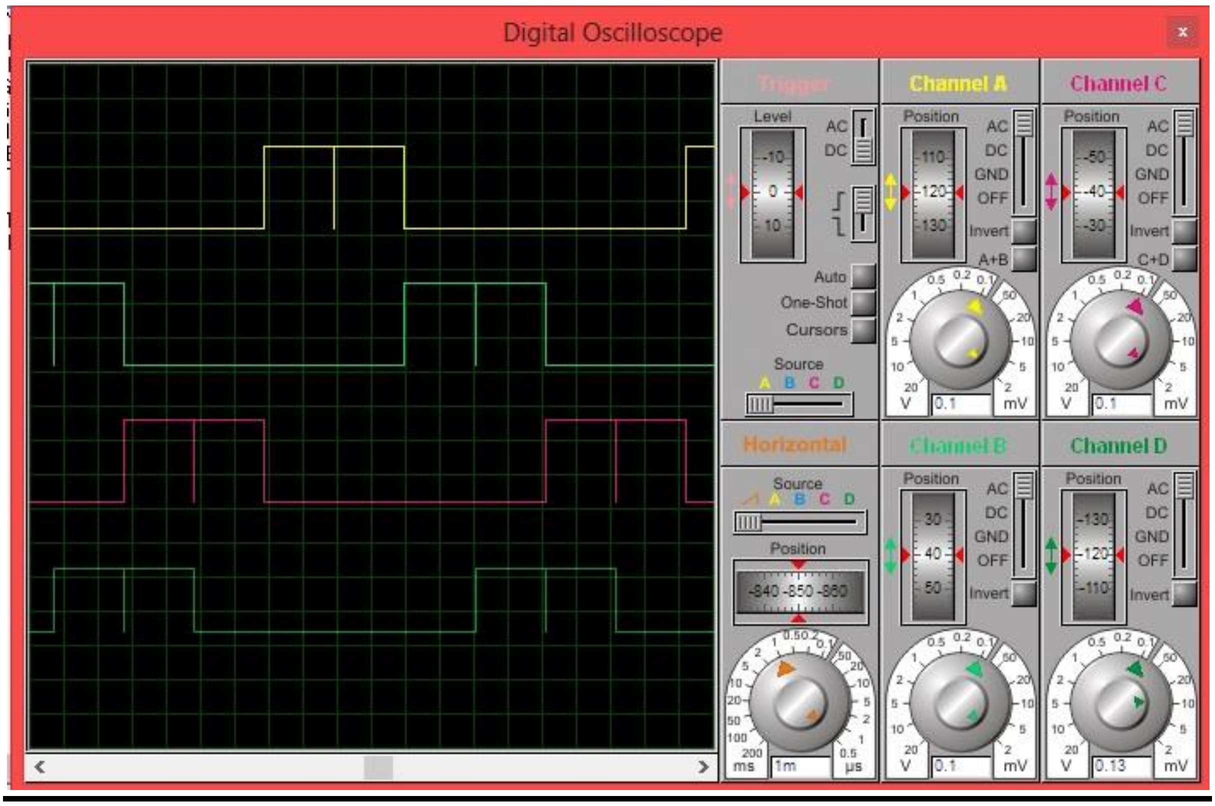


Figure 4.15 *Switching pulses waveform 120˚ conduction*

CHAPTER 5

FOURIER ANALYSIS

To calculate the Total Harmonic Distortion of the inverter's output voltage, Voltage vs Frequency graph is plotted. This plot is known as Fourier spectrum. One can observe the peak values of the voltages at different frequencies or we can say that peak voltage of different order of harmonics can seen from the fourier spectrum.

$$v_{ao} = \sum_{n=6k\pm1}^{\infty} \left(\frac{2V_s}{n\pi} \sin n\omega t\right) \quad \text{and} \quad v_{ao} = \sum_{n=1,3,5\ldots}^{\infty} \left(\frac{2V_S}{n\pi} . \cos\frac{n\pi}{6} . \sin n(\omega t + \frac{\pi}{6})\right)$$

Are the equation of phase voltages of inverter in 120 and 180° of conduction mode, phase voltage of inverter output in 120° conduction has harmonics of order n=6k±1(k=0,1,2...) whereas phase voltage in 180° conduction has only odd harmonics.

5.1 Fourier Spectrum of Inverter (120° conduction Mode)

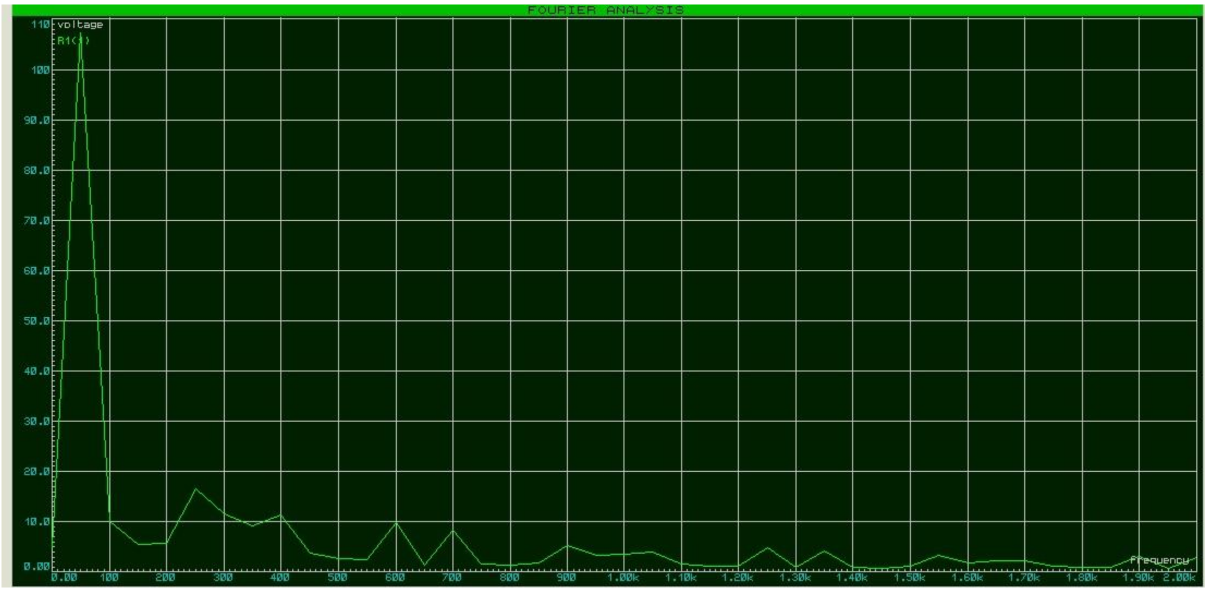


***Figure 5.1** Fourier Spectrum of Inverter in 120° conduction mode (without filter)*

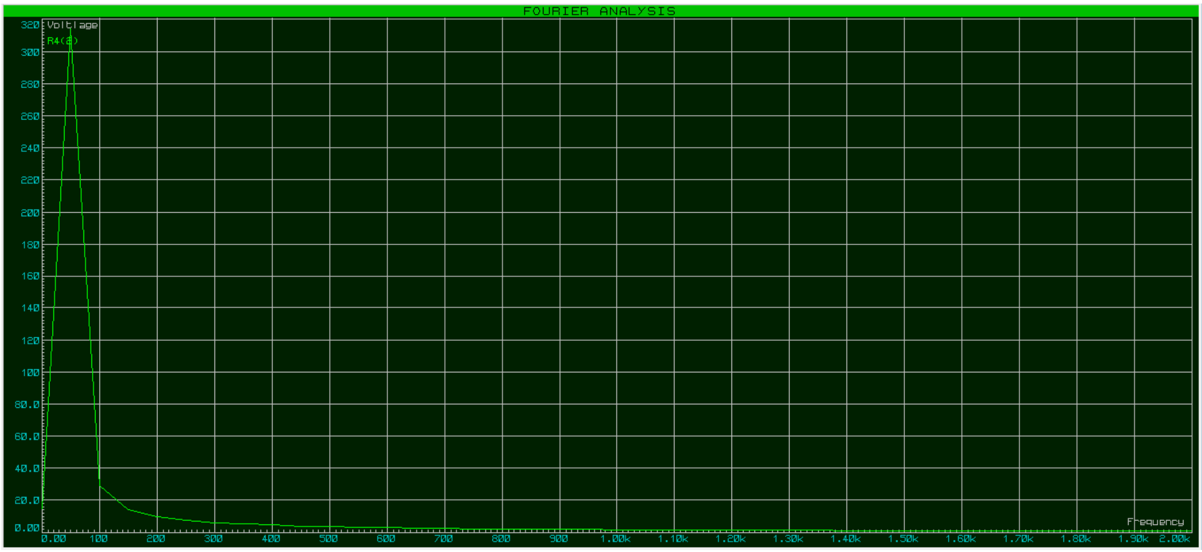


Figure 5.2 *Fourier Spectrum of Inverter in 120˚ conduction mode (with filter)*

From Fig 5.1 and 5.3, it can be observed that at lower frequencies there are peaky voltages and with increase in frequency the peak of the voltages reduces gradually, the voltage peaks at lower frequencies shows the dominant nature of lower order harmonics in inverter without a filter.

When a low pass filter of cut off frequency of 50Hz at each phase of inverter is applied, it reduces the peaks of voltages at lower frequency or it filters out the dominating lower order harmonics.

5.2 Fourier Spectrum of Inverter (180˚ conduction Mode)

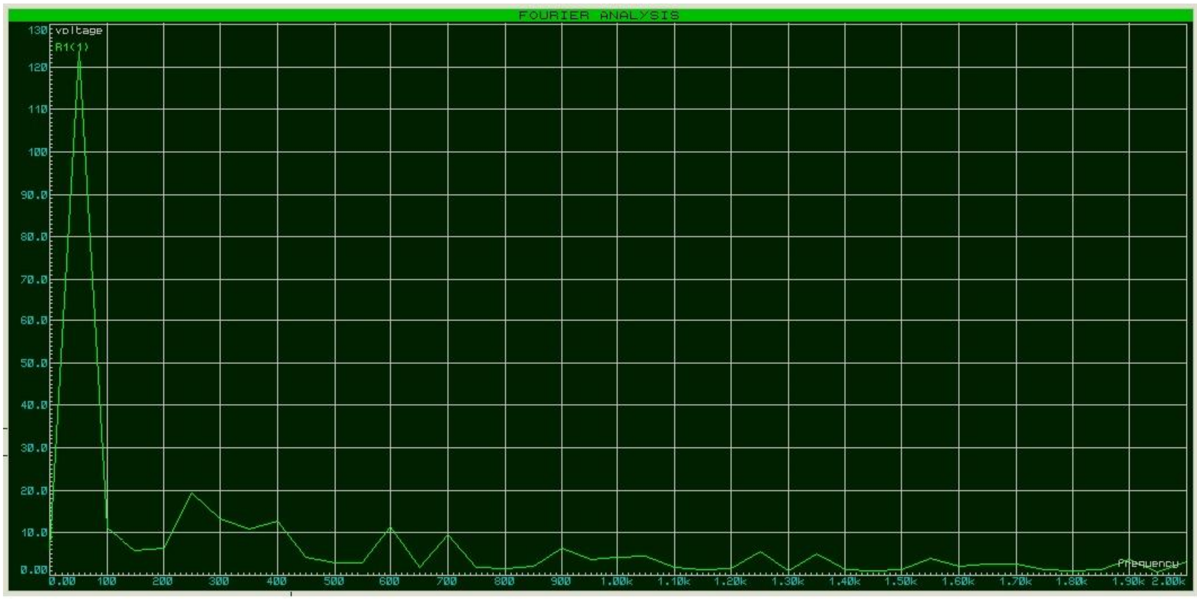


Figure 5.3 *Fourier Spectrum of Inverter in 180˚ conduction mode (without filter)*

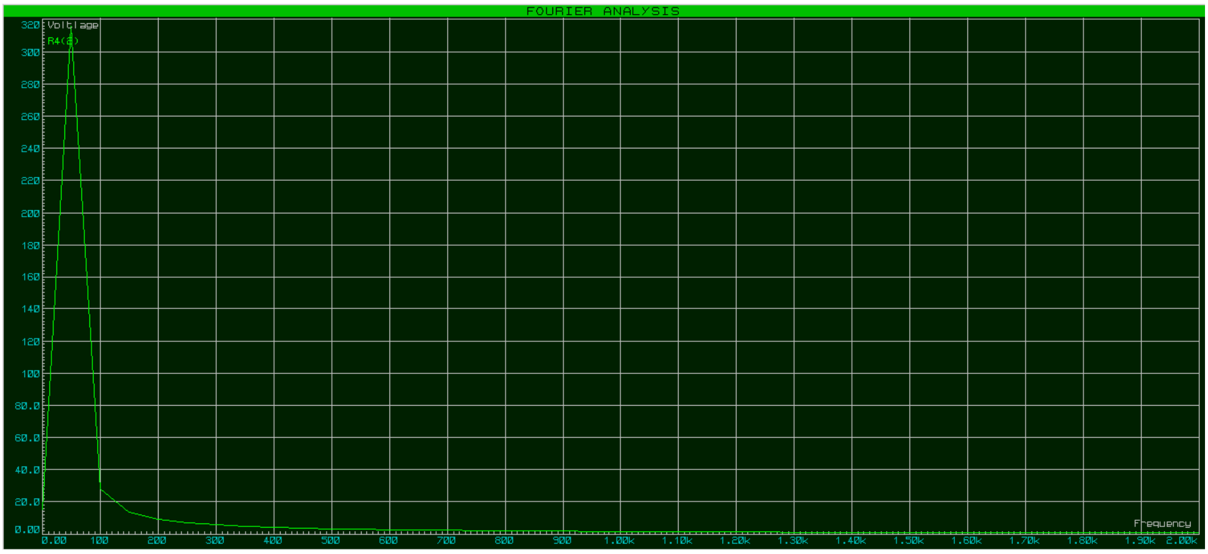


Figure 5.4 *Fourier Spectrum of Inverter in 180˚ conduction mode (without filter)*

It can be observed from Fig 5.2 and 5.4, unlike Fig 5.1 and 5.3 the fourier spectrum doesn't have peaky voltages levels at lower frequencies, this indicates the dominant harmonics has been filtered out upto a certain extent and THD of the inverter is reduced and performance is improved.

5.3 THD Calculation of 120° conduction Mode & 180° conduction Mode

Order of Harmonic	Frequency(Hertz)	Peak Voltage Magnitude Vn (Volts)	RMS Voltage Magnitude Vn =Vpn/1.414 (Volts)
1	50	314	222.03
2	100	28	19.8
3	150	15	10.6
4	200	9.9	7
5	250	9.6	6.78
6	300	8	5.65
7	350	5	3.53
8	400	4.7	3.35
9	450	4.5	3.18
10	500	4.2	2.96
11	550	3.9	2.75
12	600	3.2	2.26
13	650	2	1.41
14	700	1.2	0.85
15	750	1	0.707

Table 5.1 *Harmonic Analysis of Filtered phase voltage of inverter (120° conduction mode)*

$V_n = Individual\ harmonic\ voltage\ distortion\ values\ in\ volts, per\ unit\ volts, or\ kV.$

$V_1 = Fundamental\ voltage\ distortion\ values\ in\ volts, per\ unit\ volts, or\ kV.$

$V_2 = 2nd\ harmonic\ voltage\ distortion\ values\ in\ volts, per\ unit\ volts, or\ kV.$

$$V_{RMS} = \sqrt{V_1^2 + V_2^2 + V_3^2 \ldots + V_n^2} \qquad (5.1)$$

= 223.5V

$$CF = Crest\ Factor = \frac{|V_{Peak}|}{V_{RMS}} \qquad (5.2)$$

= 322.50/223.5 = 1.44

$$THD = Total\ Harmonic\ Distortion = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_n^2}}{V_1}\ x\ 100\% \qquad (5.3)$$

= (26.26/2220.03) *100

= 11.827%

Order of Harmonic	Frequency(Hertz)	Peak Voltage Magnitude Vpn (Volts)	RMS Voltage Magnitude Vn =Vpn/1.414 (Volts)
1	50	318	224.86
2	100	28	19.8
3	150	13.5	9.54
4	200	9	6.36
5	250	8.5	6.01
6	300	6	4.24
7	350	5.5	3.89
8	400	4.5	3.53
9	450	3.8	2.68
10	500	3.6	2.54
11	550	3.5	2.47
12	600	2.8	1.97
13	650	2.5	1.76
14	700	1.2	0.84
15	750	1.1	0.77

Table 5.2 *Harmonic Analysis of Filtered phase voltage of inverter (180° conduction mode)*

V_n = *Individual harmonic voltage distortion values in volts, per unit volts, or kV.*
V_1 = *Fundamental voltage distortion values in volts, per unit volts, or kV.*
V_2 = *2nd harmonic voltage distortion values in volts, per unit volts, or kV.*

$$V_{RMS} = \sqrt{V_1^2 + V_2^2 + V_3^2 \ldots + V_n^2} \quad = 226.263V$$

$$CF = Crest\ Factor = \frac{|V_{Peak}|}{V_{RMS}}$$

= 325.5/1.44 = 1.44

$$THD = Total\ Harmonic\ Distortion = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_n^2}}{V_1}\ x\ 100\%$$

= (25.16/224.86) *100 = 11.908%

RESULT

Table 5.3 *THD and Output Voltage analysis with increasing value of Quality factor*

S.No	Resistance of Filter (Ohms)	Quality Factor	RMS Ouput Voltage(180 Deg. Conduction mode) Volts	RMS Ouput Voltage(120 Deg. Conduction mode) Volts	THD(%)
1	21.08	1.5	121	102	23.45%
2	12.65	2.5	192	160	16.87%
3	9.03	3.5	246	208	10.7%
4	7.02	4.5	294	248	7.79%
5	5.75	5.5	328	282	5.68%
6	4.86	6.5	355	311	4.81%
7	4.21	7.5	378	332	2.79%

It can be observed from the above analysis that as the value of ‘R’ in the filter decreases the quality factor ‘Q’ of the filter increases, With increasing value of ‘Q’ the voltage output of the inverter also increases and the value of THD decreases and hence the performance of improves with increasing value of the Quality Factor.

There is a limitation that as the value of the ‘Q’ increases the current drawn from the DC input of the inverter also increases,this increased value of current also increases the switching losses and moreover if very high amount of current is drawn from the source then the input DC voltage will sag down ,therefore practically the quality factor of the filter cannot be increased above a permissible limit.

REFERENCES

[1] A. Iqbal, E. Levi, M. Jones and S. N.Vukosavic, "Generalized sinusoidal PWM with harmonic injection for multi-phaseVSIs," in Proc. IEEE Power Elec. Spec.Conf. PESC, Jeju, Korea, 2006, pp. 2871-2877.

[2] "Analysis of a modulation technique applied to FC inverter for THD reduction" Davi R.Joca, Allan U. Barbosa2, Demercil S.OLIveira jr3, Paulo P. Praca$, Luiz H.S.C.barreto Department of electrical engineering, N.A.L. Silva department of electrical engineering federal university ofpiauiteresina.

[3] "Comparative analysis of two control schemes for reduction of the THD in voltage applied to a single phase inverter with nonlinear loads" Escuela Superior de computo – instituto Politecnico Nacional, Av. Juan de Dios Batiz SIN, D. F, 07738,Mexico. 2Departamento de IngenieriaElectronica – UPV, Camino de Vera SIN, 7F, Valencia, 46022, Espana.

[4] Text book "POWER ELECTRONICS Converters, Applications, and Design" 3rd edition by NED MOHAN, Dept., of electrical engineering, University of Minnesota, Minneapolis, Minnesota &WILLIAM P.ROBBINS, , Dept., of electrical engineering, University of Minnesota, Minneapolis, Minnesota &TORE M.UNDELAND, Faculty of electricalengineering& computer science, NorwegianInstitute of Technology, Trondheim, Norway.

[5] Text book "POWER ELECTRONICS", KHANNA PUBLISHERS By Dr. P. S. Bimbhra, Ph. D., M.E. (Hons.0, F.I.E.(India), M.I.S.T.E. Ex-dean, Ex-Prof. And Head of Electrical & Electronics Engg. Dept.Thapar Institute of Engineering and Technology PATIALA-147004.

[6] Text book "POWER ELECTRONICS CIRCUITS , DEVICES AND APPLICATIONS" third edition by MUMAMMAD H. RASHID, dept of electrical and computer engineering, university of west florida.

[7] Paper on NON-LINEAR LOADS by MIRUS International Inc.

[8] SIEMENS Whitepaper Harmonics in power systems Causes, effects and control usa.siemens.com/lv-drives.

[9] International Journal of Computer Applications (0975 – 8887) Volume 92 –No.10, April 2014 Harmonics Analysis of Power Electronics Loads Srijan Saha, Suman Das M.Tech. Final Year Student Dept. of Electrical Engineering,TripuraUniversity. Champa Nandi, Assistant Professor Dept. Of Electrical Engineering Tripura University.

APPENDIX A

SOURCE CODE

There are two microcontrollers used for the designing purpose of the inverter. The first microcontroller controls the switching sequence and duration of the inverter in both 180 and 120 degree conduction mode and the the second microcontroller is used to control the switching of the boost converter.Both the microcontroller are programmed in ‘C’ language using a programming software called Keil uVision4.

A.1 Boost Converter’s Switching Code

```
#include<reg51.h>
sbit rel=P3^0;
void delay7()   //1 uS timer
{TMOD=0X01;
TL0=0xfe;
TH0=0xff;
TR0=1;
while(TF0==0);
TR0=0;
TF0=0;
}
void main()
{int i;
        rel=0;
for (;;)
        {
for (i=1;i<=50;i++)
{


        if(i<=13) //D=0.25
        {rel=1;;delay7();}
  else
         {rel=0;delay7();}


}}
```

A.2 Three Phase Inverter's Switching Code

```
#include<reg51.h>
#include<math.h>
sbit s1=P1^0;
sbit s2=P1^1;
sbit s3=P1^2;
sbit s4=P1^3;
sbit s5=P1^4;
sbit s6=P1^5;
sbit s7=P1^6;

sbit rs=P3^0;
sbit sw1=P3^1;
sbit sw2=P3^2;
sbit sw3=P3^3;
sbit sw4=P3^4;
sbit sw5=P3^5;
sbit sw6=P3^6;
sbit en=P3^7;
sbit reset=P0^1;
sbit rel=P1^7;

int i,j,m=0,n=20/6,q[8],c=0,k=0;

char a2[]="MODE OF OPRTN:";
void delay7()   //1 uS timer
{TMOD=0X01;
TL0=0xfe;
TH0=0xff;
TR0=1;
while(TF0==0);
TR0=0;
TF0=0;
}
```

```
void delay(unsigned int s) //delay for lcd
{while(s)
s++;}
void delay2()   //1 millisecond timer..
{TMOD=0X01;
TL0=0x18;
TH0=0xfc;
TR0=1;
while(TF0==0);
TR0=0;
TF0=0;
}
void delay1() //50 msec
{TMOD=0X01;
TL0=0xfd;
TH0=0x4b;
TR0=1;
while(TF0==0);
TR0=0;
TF0=0;
}
void lcd_cmd(char d)
{
P2=d;
rs=0;

en=1;
delay(1);
en=0;
}
void lcd_data(char e)
{P2=e;
rs=1;

en=1;
```

```
delay(1);
en=0;
}
void lcd_cmds()
{ lcd_cmd(0x01);
lcd_cmd(0x80);
lcd_cmd(0x38);
lcd_cmd(0x0e);
}


void main()
{P3=0x00;
	lb3:




lb4:
	lcd_cmds();
for (i=0;i<=12;++i)
lcd_data(a2[i]);
lcd_cmd(0xc0);
lcd_data('1');lcd_data('.');lcd_data('1');lcd_data('2');lcd_data('0');//1.120
lcd_data(' ');//space
lcd_data('2');lcd_data('.');lcd_data('1');lcd_data('8');lcd_data('0');//2.180*/
lb:

for (i=1;i<=21;i++)
{

	if(i<=14)
	{rel=1;;delay7();}
  else
	 {rel=0;delay7();}

}
```

```
goto lb;

if(s1==0) //120
{
lb2:

P3=0x00;
for (i=0;i<n;++i)
{sw6=sw1=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw2=sw1=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw3=sw2=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw3=sw4=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw5=sw4=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw6=sw5=1;
delay2();
}
```

```
if(s3==0)
goto lb4;

goto lb2;}
if(s2==0) //180

{
        lb:
P3=0x00;
for (i=0;i<n;++i)
{sw6=sw5=sw1=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw6=sw2=sw1=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw3=sw2=sw1=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw2=sw3=sw4=1;
delay2();
}
P3=0x00;
for (i=0;i<n;++i)
{sw3=sw5=sw4=1;
delay2();
}
```

```
P3=0x00;
for (i=0;i<n;++i)
{sw6=sw5=sw4=1;
delay2();
}
if(s1==0)
        goto lb2;
if(s3==0)
        goto lb4;

goto lb;}

if(s3==0)
goto lb4;
getch();
}
```

APPENDIX B

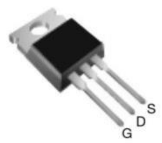
DATA SHEET OF ICs

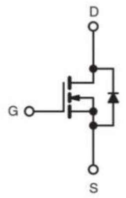
IRF540, SiHF540
Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.077
Q_g (Max.) (nC)	72	
Q_{gs} (nC)	11	
Q_{gd} (nC)	32	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF540PbF
	SiHF540-E3
SnPb	IRF540
	SiHF540

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	28	A
		T_C = 100 °C		20	
Pulsed Drain Current[a]			I_{DM}	110	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	230	mJ
Repetitive Avalanche Current[a]			I_{AR}	28	A
Repetitive Avalanche Energy[a]			E_{AR}	15	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	150	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

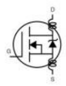
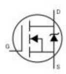
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 440 μH, R_g = 25 Ω, I_{AS} = 28 A (see fig. 12).
c. $I_{SD} \le$ 28 A, dI/dt $\le$ 170 A/μs, $V_{DD} \le V_{DS}$, $T_J \le$ 175 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

Document Number: 91021
S11-0510-Rev. B, 21-Mar-11

www.vishay.com
1

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 17 A[b]	-	-	0.077	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 17 A[b]	8.7	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V,	-	1700	-	pF
Output Capacitance	C_{oss}	V_{DS} = 25 V,	-	560	-	
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz, see fig. 5	-	120	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 17 A, V_{DS} = 80 V, see fig. 6 and 13[b]	-	-	72	nC
Gate-Source Charge	Q_{gs}		-	-	11	
Gate-Drain Charge	Q_{gd}		-	-	32	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 17 A	-	11	-	ns
Rise Time	t_r	R_g = 9.1 Ω, R_D = 2.9 Ω, see fig. 10[b]	-	44	-	
Turn-Off Delay Time	$t_{d(off)}$		-	53	-	
Fall Time	t_f		-	43	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	28	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	110	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 28 A, V_{GS} = 0 V[b]	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 17 A, dI/dt = 100 A/µs[b]	-	180	360	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.3	2.8	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

International
IOR Rectifier

Data Sheet No. PD-6.043C

IR2101

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

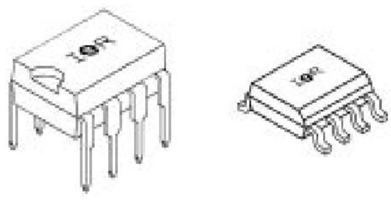
Product Summary

V_{OFFSET}	600V max.
I_O+/-	100 mA / 210 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	130 & 90 ns
Delay Matching	30 ns

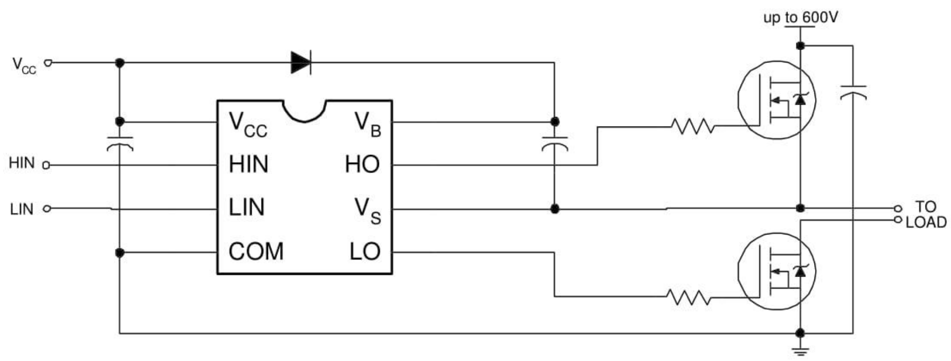
Description

The IR2101 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter Definition		Value Min.	Value Max.	Units
V_B	High Side Floating Supply Voltage		-0.3	625	V
V_S	High Side Floating Supply Offset Voltage		V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage		-0.3	25	
V_{LO}	Low Side Output Voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN & LIN)		-0.3	V_{CC} + 0.3	
dV_s/dt	Allowable Offset Supply Voltage Transient		—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$	(8 Lead DIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(8 Lead DIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T_J	Junction Temperature		—	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Value Min.	Value Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage (HIN & LIN)	0	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low-voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.