CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION ON INVERTER

As a continuous growth of electrical energy demand throughout the world, we need additional source of energy with less harmful effect on environment like renewable energy so we need some power electronic devices that convert renewable energy into useful electrical energy like MPPTs, inverters, cyclo-converters electrochemical processes, heating and lighting control, welding, reactive power compensation, flexible AC transmission systems, active filters, energy storage, motor drives, and for emergency condition we always need backups like batteries, ultra-capacitor etc. which is DC power in the conversion of DC to AC power, inverters are most widely employed in the modern set-up of electric power generation, transmission, distribution, utilization, and protection[32-35].

1.2 TYPES OF INVERTER

The different types of inverter are

1.2.1 Two level square wave inverter,

1.2.1 Three level square wave inverter (simple PWM inverter),

1.2.2 Sine wave PWM inverter,

1.2.3 Multi-level inverter.

As increasing the efficiency of the inverter from '1.2.1' to '1.2.4' the complexity and cost is also increase as the power circuit (H-bridge inverter) is almost is common in two level square wave, three levels square wave, and Sine wave PWM inverter but the difference in the controlling method make the overall system different as two level square wave inverter are the simplest one in the inverter family but it can produce approximately 48.3% THD which reduce efficiency[38-40], the life of the equipment and produce buzzing noise as compare to the Three level square wave inverter which reduce THD up to 30% but complexity of controlling circuit is much more than the two level square wave inverter but sine wave PWM inverter use high frequency switches much more complex controlling system but THD reduce to 20% with inductive filter and need high dV/dt protection as frequency is increase. In the above topologies filters is always required, the size

of filter is directly proportional to value of THD generate in output voltage or current. Passive filter are two types Inductor, capacitor for low pass filter capacitor should be connected in parallel to output voltage and inductor should connected in series of current output because capacitor shows higher impedance for low frequencies harmonics and bypass the high frequencies harmonics as $XC \propto 1/f$, while the inductor shows higher impedance to high frequencies and low impedance to low frequencies as $XL \propto f$. But the multi-level inverter is completely different from above inverter as their power circuit as well as control circuit are completely different and more complex than above inverter, it required smaller value of filter or some time only load impedance is sufficient[41].

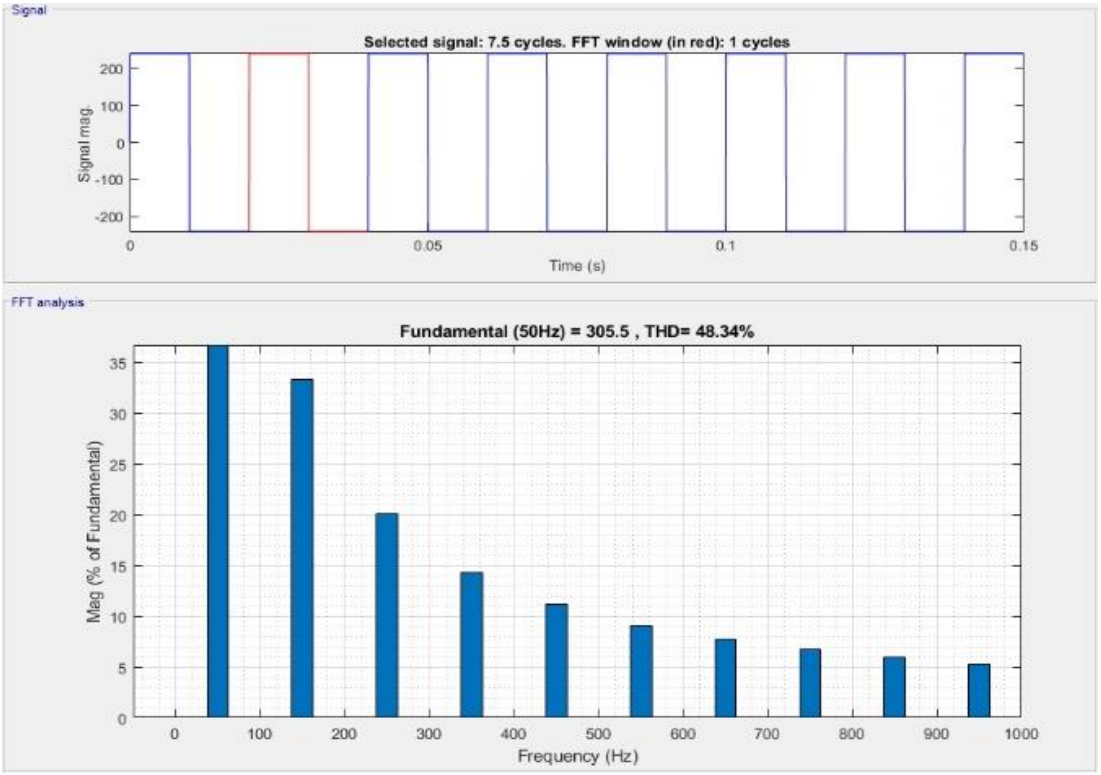

Fig. 1.1- Two Level square wave output THD

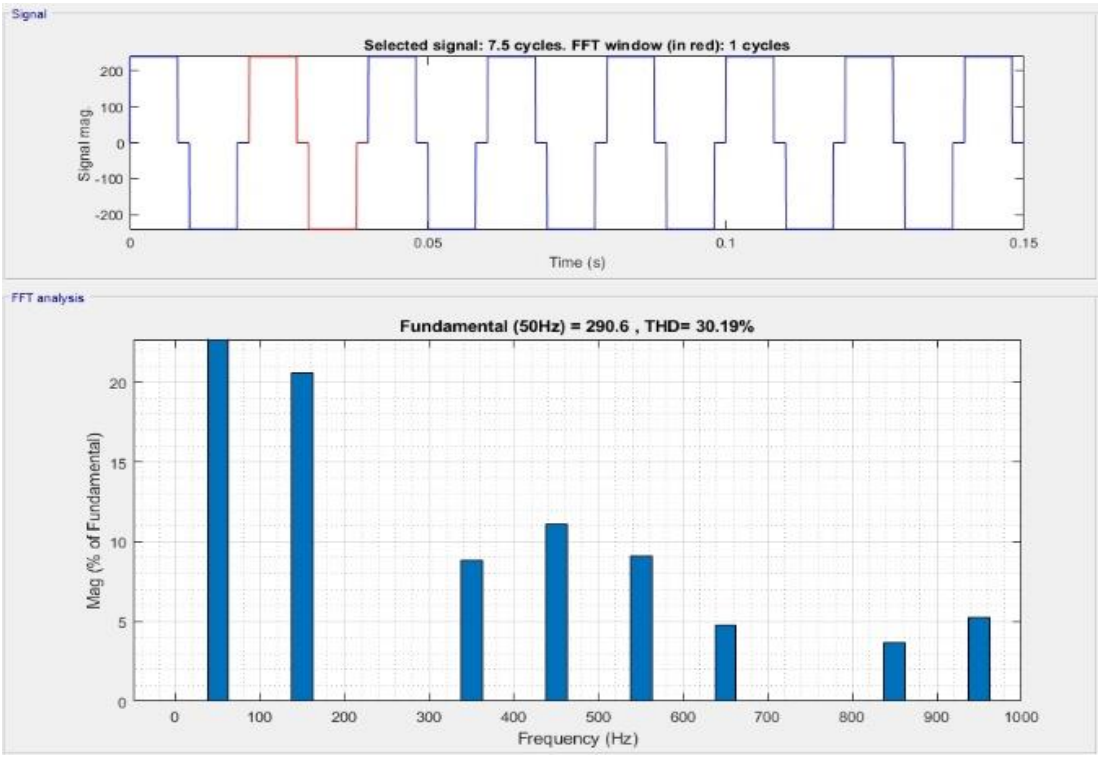

Fig. 1.2- Three Level square wave output THD

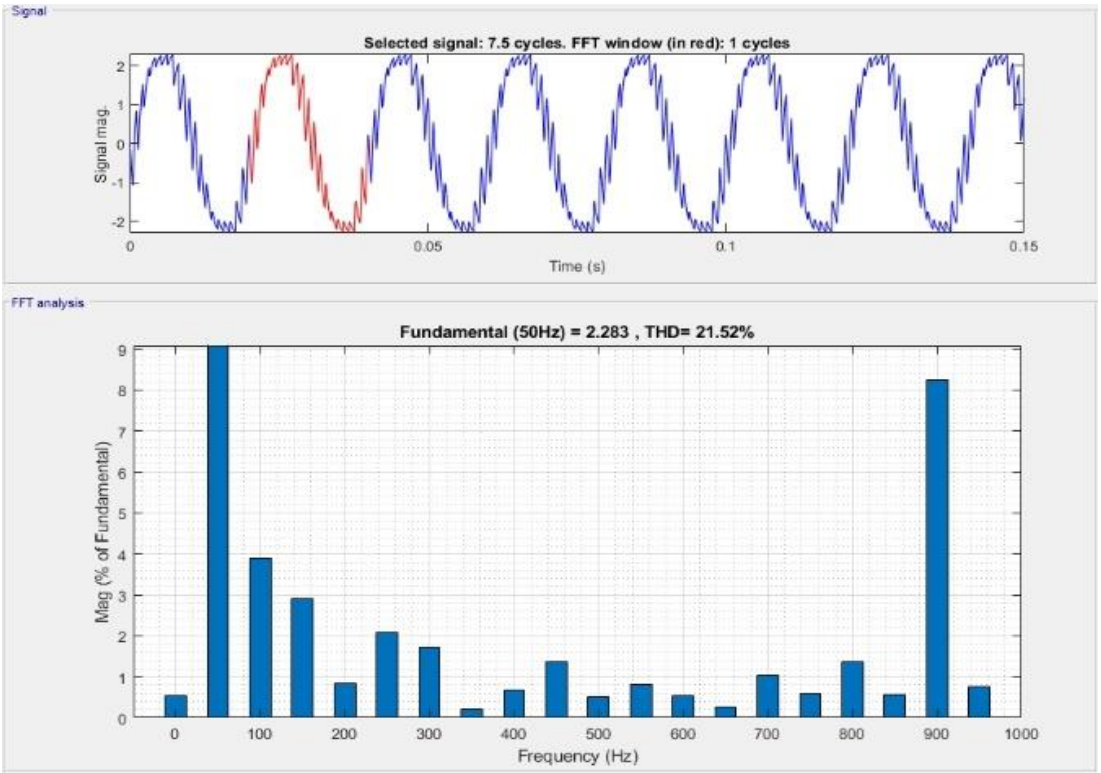

Fig. 1.3- Sine Wave PWM output current THD

1.3 INTRODUCTION ON MULTI-LEVEL INVERTER

Recently expansions in the power electronic devices provide possibility of designing and implementing of novel power electronic converters. Voltage Source Multilevel Inverter (MLI) is very suitable topology in high voltage range applications such as power distribution, motor drive systems, power quality and power conditioning applications.

Motivated by the impetus to reduce the use of electrical energy produced from fossil fuel resources and the continued increased in electric powered equipment, has led to the increased deployment of alternative energy resources. A power converter is often required to ensure its energy is supplied to the load in the most efficient manner. A MLI is able to produce output waveforms featuring a much lower harmonic distortion compared to the typical 2 level converter. In a MLI lower distortion is achieved by reducing the voltage step-size that occurs during a commutation event, some advantages of multilevel inverters as compare to the three-level voltage inverter can be listed as follow: Smaller output voltage steps, harmonic components are lower, operating the MLI atBhigh frequency, enables the reduction of filter size, nevertheless, thisBleads to higher switching losses reducing overall converter efficiency, electromagnetic compatibility are better in multilevel inverters. Also, by increasing the number of levels in the converter, the output voltage has more steps generating a staircase waveform which reduce the Total harmonic distortion. Some disadvantages of multilevel converters are: number of power electronic switches is increased, control scheme is complex, and tend to reduce the overall reliability and stability[10].

1.4 TYPES OF MULTI-LEVEL INVERTER

1.4.1 Diode-clamped multilevel inverter (DCMLI),

1.4.2 Flying capacitor-clamped multilevel inverter (FCMLI), and

1.4.3 Cascaded H-bridge multilevel inverter (CHB).

These are the main fundamental multilevel topologies. There are some certain differences between single-DC-source and multiple-DC source MLI topologies which limit the application of multiple-DC-source ones in power systems. Such limitations are discussed based on the topology and associated controller approach, separately. Saying from topology point of view, multiple-DC-source inverters need more than one isolated DC supplies. Therefore, they will not be cost-effective and

small size because an isolated DC supply is made up of a transformer and a diode bridge, or it could be a battery or PV panel. Consequently, multiple-DC-source topologies have at least one more supply than a single-DC source one, which means undesired additional size and cost. The most popular MLI with multiple-DC-source is the CHB, which is used in very high-power motor drives currently. The main advantages of CHB are the modularity and identical voltage rating of switches due to using equal DC sources. Many other multiple-DC-source topologies have been published but they suffer from unequal voltage rating of DC supplies and switches which is the main reason of not getting attraction from industries. A fair comparison between CHB and all those multiple-DC-source MLIs considering equal voltage rating of components reveals the fact that CHB is still the best one with optimum number of components due to its identical voltage rating in each cell and modularity. A major concern with multiple-DC-source configurations is the power sharing among feeders. An unbalanced power sharing causes undesirable power losses and malfunctioning. Considering the control algorithms, a cascaded control consisting of a current and a voltage loop is required for most of the power converters applications. Focusing on grid-connected ones, such as PV systems, the DC bus should be also regulated by injecting the voltage error into the current reference. Such scheme as shown in Fig. 3, requires numerous voltage loops and consequently voltage PI regulators for multiple-DC-source topologies. Moreover, implementing a power balancing unit is inevitable to share the appropriate amount of power between sources. As well, injecting all voltage errors into only one single current reference cannot ensure proper distributing of the active power among DC links to keep the capacitors voltages fixed. This issue also exists in single-DC-source inverters in which there is no redundant switching states to balance the auxiliary capacitors voltages. For instance, the two DC capacitors in Neutral-Point Clamped (NPC) can be controlled by redundant switching states only in 3-phase configuration; otherwise, they have to use external controllers for single phase applications. The same concern exists for Active Neutral-Point Clamped (ANPC) and Flying Capacitors (FC) inverters except their auxiliary capacitors[11-17].

As a conclusion, a single-DC-source inverter is desired in which the auxiliary capacitors are controlled through switching states without adding extra linear/nonlinear regulators and complexity to the system. Such topology can be installed in all power system applications where the 2-level ones are already

operating. Therefore, the input DC side and output AC side do not require to be modified. Moreover, the controller remains the same since only a single DC link should be regulated and the error signal goes into the reference current. However, the modulation block should be replaced by a multilevel switching technique with integrated voltage balancing using redundant switching states[18].

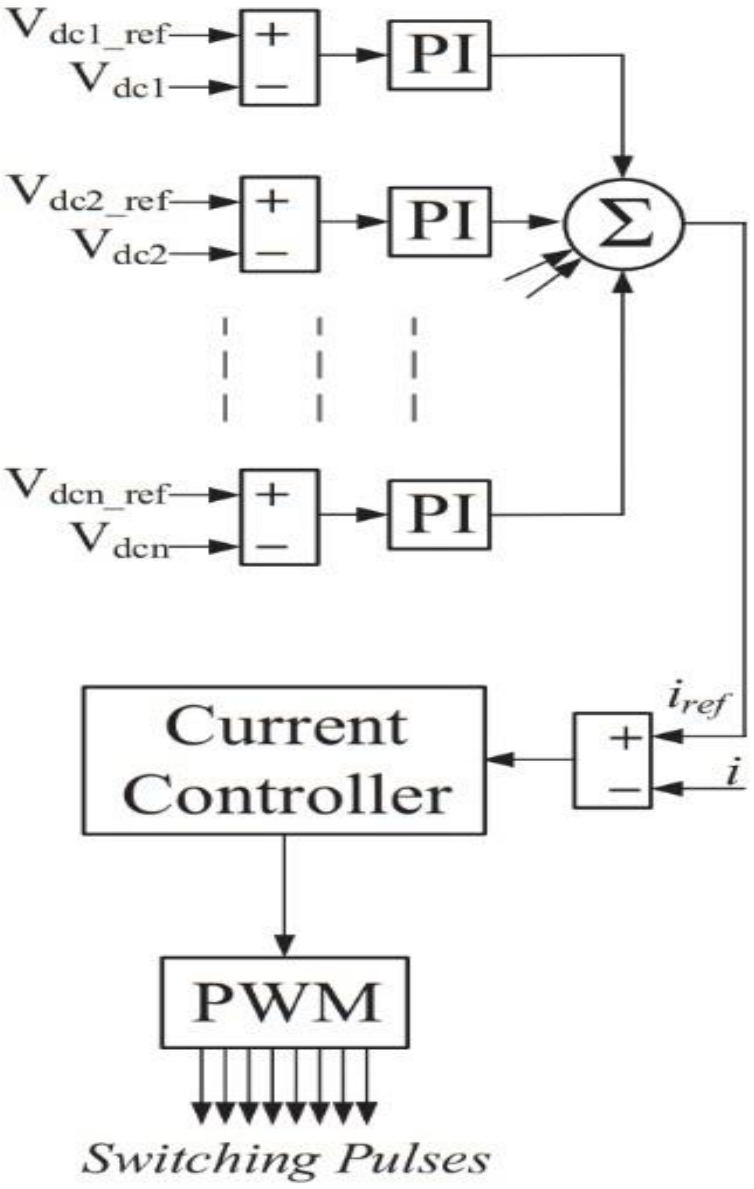

Fig. 1.4- Controlling Scheme for n DC buses

1.4.1 DIODE CLAMPED MULTI-LEVEL INVERTER

This is also known as Neutral Point clamped (NPC) inverter, in 1981 Nabae, Takahashi, and Akagi proposed neutral-point converter asBa three-level diode-clamped inverter. In later years, further developments several research articles published with experimental results for five, and higher level diode-clamped inverters, in particular applicable towards SVC for variable speed motor drives, and high-voltage system interconnections it consists of two parallel pair of series connected four switches (i.e. series connected two pair of switches leg) in parallel with two capacitor connected in series for dividing DC voltage into two equal part, the diodes are connected in such a way that the charge across the capacitors should be maintained, as shown in Fig.1.5. The midpoint of the capacitors take as zero potential (ground reference) than upper capacitor charge with $+\frac{1}{2}V_{dc}$ and lower one with $-\frac{1}{2}V_{dc}$. Therefore, levels in output voltage is $-V_{dc}$, $-\frac{1}{2}V_{dc}$, 0, $+\frac{1}{2}V_{dc}$, and $+V_{dc}$, It is difficult to control, real power flow in case of single inverter because it requires a very precise monitoring and control for intermediate DC levels, which tends to over charges or discharge. Practically, multilevel diode-clamped inverter found application as an interface between high-voltage dc transmission line and ac transmission line number of clamping diodes required. Capacitors requirement is minimized, since all the phases shares the same dc source. For this reasons diode-clamped multilevel converters used as a back-to-back converter and practically applicable to high-voltage back-to-back inter-connection and adjustable speed drives, efficiency is high with fundamental frequency switching but it is difficult to control, real power flow in case of single inverter because it requires a very precise monitoring and control for intermediate dc levels, which tends to over charges or discharge, fundamental frequency switching will cause an increment on voltage and current THD, while increased number of clamping diode makes the configuration bulky[19].

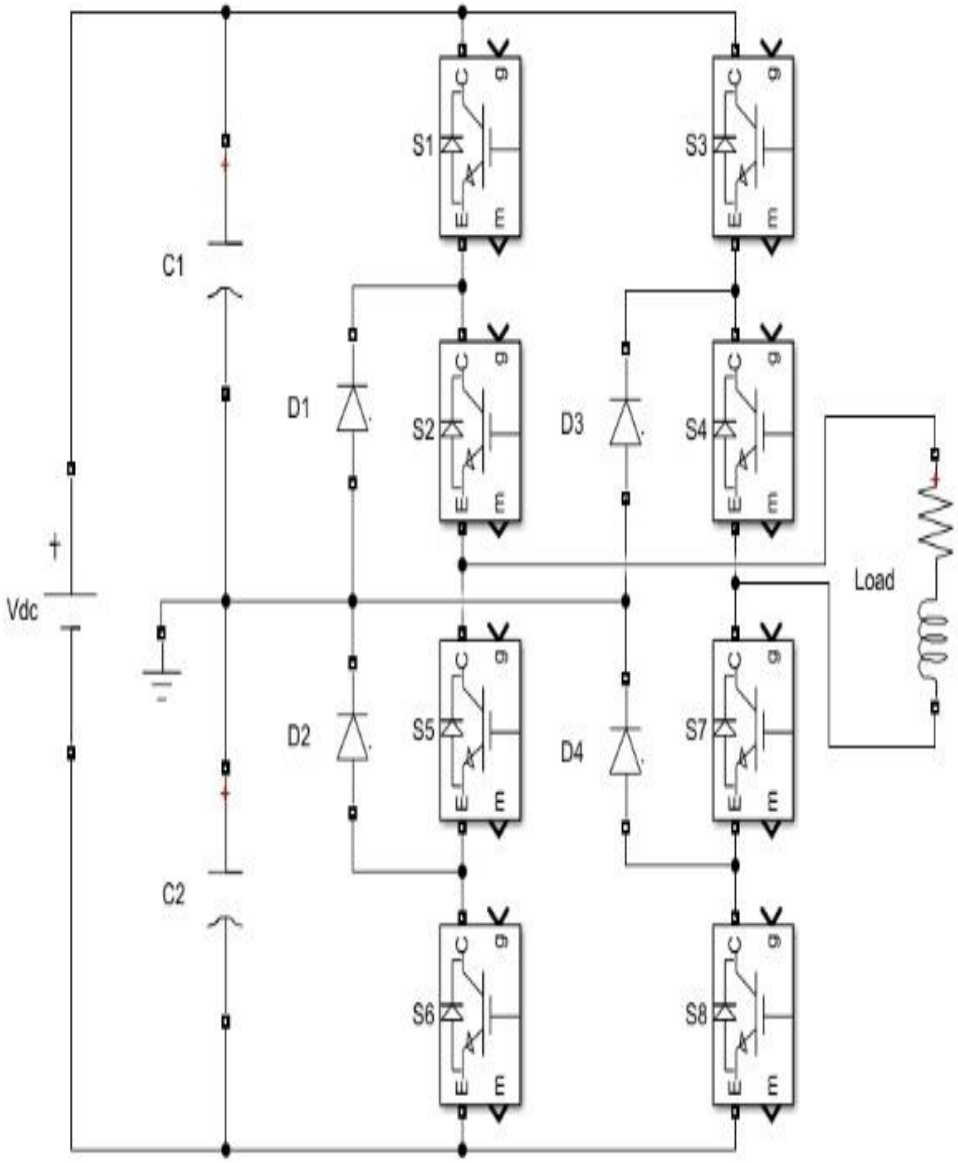

Fig. 1.5- Diode Clamped Five-Level Inverter

1.4.2 FLYING CAPACITOR-CLAMPED MULTILEVEL INVERTER

In 1992 Meynard, and Foch, proposed a multilevel inverter structure which is similar to diode-clamped multilevel inverter, differences instead of using clamping diodes, replaced by capacitors. This topology has a stepping stool structure of DC side capacitors. The voltage on every capacitor varies from that of the following capacitor. The voltage increase between two nearby capacitor legs gives the measure of the voltage ventures in the yield waveform. One favorable position of the flying capacitor based inverter is that it has redundancies for inward voltage levels. Not at all like the diode braced inverter, the flying capacitor inverter does not require the greater part of the switches that are ON (leading) in a continuous arrangement. In addition, the flying capacitor inverter has stage redundancies, though the diode cinched inverter has just line-line redundancies. These redundancies permit a decision of charging and releasing particular capacitors and can be fused in the control framework for adjusting the voltages over the different levels. Similar to neutral point clamped inverter, the capacitor clamped inverter requires a large number of bulk capacitors of voltage clamping as shown in Fig.1.6. The voltage rating of each capacitor used will be the same as that of the main power switch, therefore, an N-level converter will require a total of (N - 1)(N - 2) /2 clamping capacitors per phase leg in addition to (N - 1) main DC-bus capacitors. The mail feature is to provide switch combination redundancy for balancing different voltage levels. Real and reactive power flow can be controlled. The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags, but control is complicated to track the voltage levels of all the capacitors, pre-charging of all the capacitors to the same voltage level and startup are complex, switching utilization and efficiency are poor for real power transmission, and the large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode clamped converters[20].

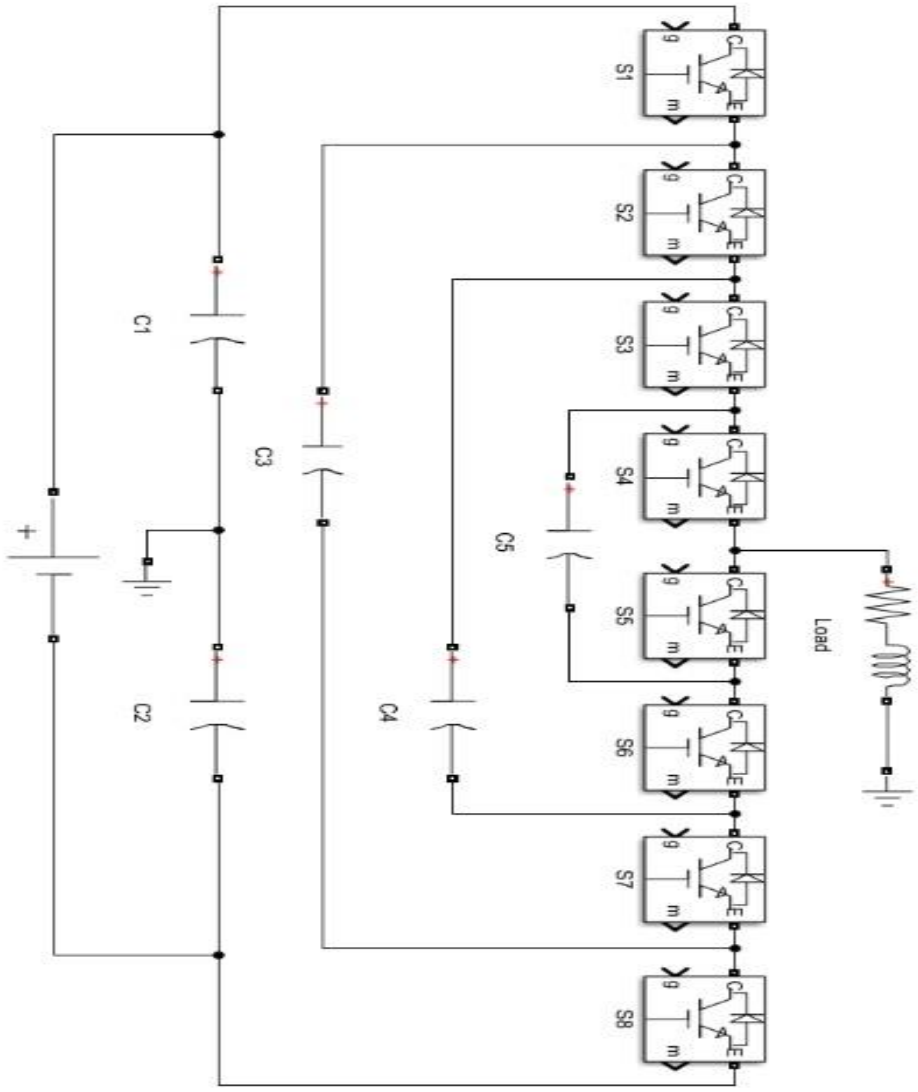

Fig. 1.6- Flying Capacitor-Clamped Five level Inverter

1.4.3 CASCADED H-BRIDGE MULTILEVEL INVERTER

To synthesize a multilevel waveform, the AC output of each of the different level H-bridge cells are connected in series. The cascaded voltage waveform is the sum of the inverter outputs. A single-phase configuration of a *5*-level H-bridge cascaded inverter is depicted in Fig. 5. Each separate dc source is connected to a single-phase full-bridge/or H-bridge, inverter. Each inverter can generate three different voltage level outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, *S1*, *S2*, *S3*, and *S4*. To obtain voltage level $+V_{dc}$, switches *S11, S21* and *S14* turned on, whereas for voltage level $-V_{dc}$ switches *S12, S22* and *S13* turned on. Similarly, for $+2V_{dc}$, switches *S11* and *S24* turned on, whereas for voltage level $-2V_{dc}$ switches *S12* and *S23* turned on. Zero level voltage can obtained by turning on switches *S1* and *S2* or *S3*, and *S4*. AC outputs of each synthesized different full-bridge inverter levels are connected in series for summing up to generate multilevel voltage waveform. The number of output single phase voltage *n*-levels in a cascade inverter defined by $n = 2 * s + 1$, where $'s'$ is the number of separate dc sources. As example phase voltage waveform for n-level cascaded H-bridge inverter with (n-1)/2 separate dc sources and (n-1)/2 full bridges. As mentioned in high voltage applications the cascaded H-bridge (CHB) topology is a good choice because this converter is the modular and the control of it is easy. But number of required separated voltage sources to supply each cell is high [21-25].

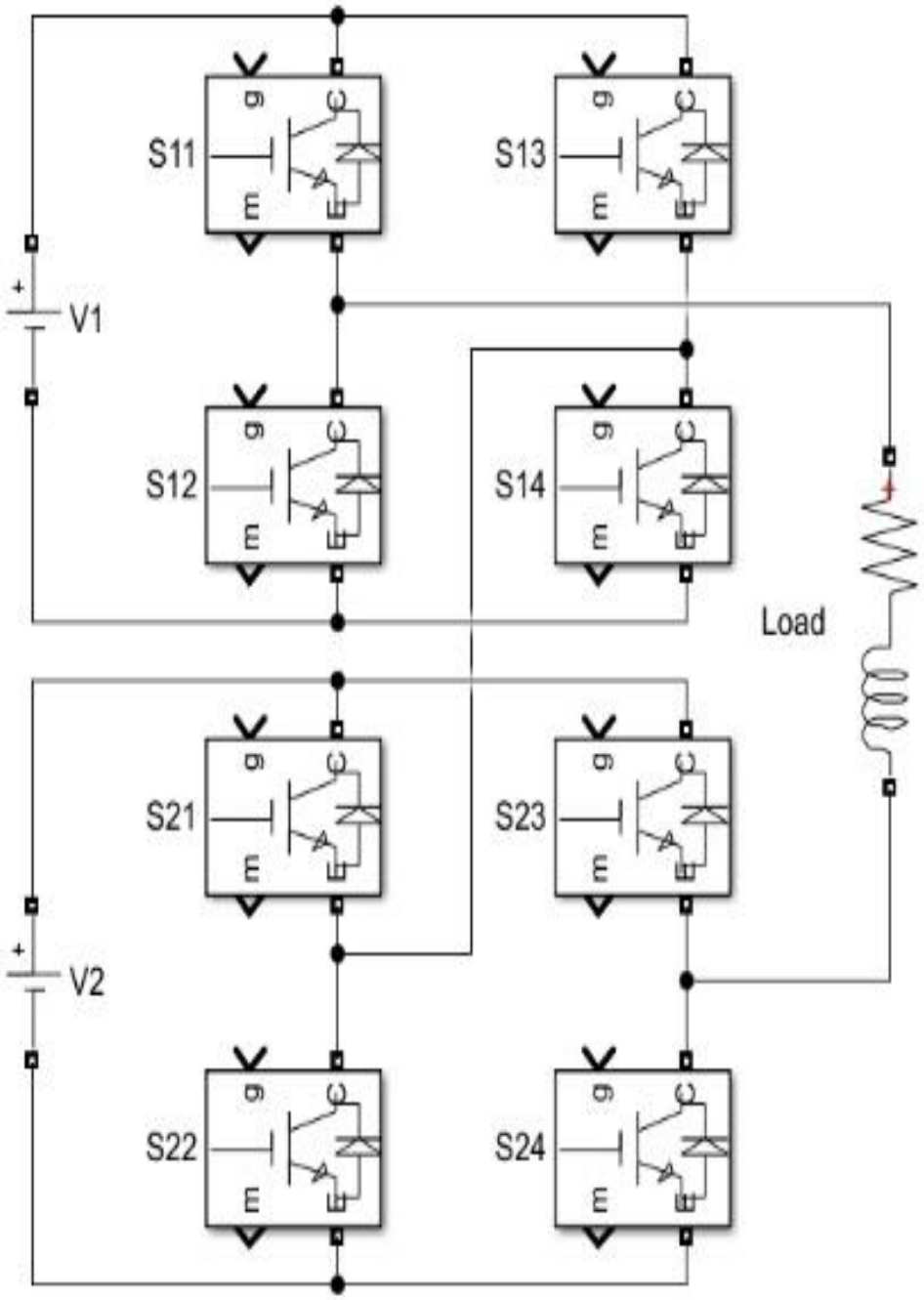

Fig. 1.7- Five Level Cascaded H-Bridge Inverter

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION ON NEW MLI TOPOLOGIES

As discussed previously, with the emergence of MLIs, the so-called classical topologies attracted maximum attention both from academia and industry. Still, no specific topology can be said to be absolutely advantageous, because multilevel solutions are heavily dependent on application and cost considerations. A given topology can be very well adapted in some cases and totally unsuitable in others. Therefore, the optimal solution is often recommended on a case-by-case basis. Hence, along with the classical topologies, researchers continued (and still continue) to evolve newer topologies with an application-oriented approach. Some of these contributions are briefly summarized below. The aim is to enable the reader to appreciate that topological innovations are taking place in numerous ways and continue to be a hot trend.

Agelidis-et-al. [37] presented a single-phase voltage-source MLI topology for photovoltaic applications, which utilizes a combination of unidirectional and bidirectional switches of different ratings along with the use of a phase opposition carrier disposition multicarrier pulse-width modulation (PWM) switching technique.

A hybrid MLI based on CHB topology is presented for a 500-HP, 4.5-kV induction motor drive with investigations into design optimization, capacitor voltage balancing, and harmonic profile of the output waveform by Manjrekar and Lipo [38].

Xiaoming and Barbi [39] presented a modified diode-clamped topology to solve the problem of series-connected diodes in a classical diode-clamped inverter. In this structure, apart from the clamping of the main switches with clamping diodes, there is mutual clamping amongst the clamping diodes.

A generalized MLI was proposed by F.Z. Peng [40] with the primary objective of self-voltage-balancing, a capability which the classical inverters do not have. Although this topology needs many clamping switches, diodes, and capacitors, it presents a large number of redundant states and new topologies that can be further derived from it.

Cheng and Crow [41] have employed an additional circuitry integrated with the diode-clamped topology for implementing a static compensator with a battery energy storage system (STATCOM/BESS). This additional circuitry helps in effective balancing of the DC link capacitors.

A topology is proposed by Mariethoz and Rufer [42] by series combination of a three-phase six-switch voltage source inverter with single-phase Hbridges resulting in better waveform resolution and improved efficiency. This approach reduces the number of DC—DC converters supplying the cells of reversible multilevel converters.

A topology is proposed by Veenstra and Rufer [43] in which a three phase three-level integrated gate-commutated thyristors inverter (as the main inverter) is connected in series with a two-level IGBT H-bridge (as the sub inverter). Asymmetric source configuration is used to obtain a nine-level waveform for medium-voltage drive applications.

To obtain a multilevel voltage waveform in the event of partial failure(s) in the power circuit, a fault-tolerant topology was proposed by Chen et al. [44], which maintains the number of levels in the output voltage waveform with post-fault modification in the control signal, along with redundancy offered by multi switching states.

Chen and He [45] have proposed a concept of using a mix of clamping diodes, power switches, and capacitors for a multilevel topology with self-voltage-balancing of the DC link capacitors for real and reactive power delivery.

To reduce the number of capacitors for a given number of levels, an approach using partial charging of capacitors was presented by Chan and Chau [46] by means of a new topology which also enables voltage boosting.

For the grid connection of two isolated photovoltaic generators with medium and high power ranges, a topology was proposed by Grandi et al. [47] using a dual two-level voltage source inverter so as to obtain a multilevel waveform. The approach reduces grid current harmonics.

Lezana et al. [48] have proposed an enhancement in the classical CHB topology with an active front end with the objective of a better regenerative mode of operation for loads which demand regenerative capability (such as laminators and downhill conveyors). This work demonstrates effective control of the input current and output voltage waveforms.

For standalone applications requiring a few kilowatts of power with a single battery storage, a topological solution has been presented by Daher et al. [49] with an MLI which uses a multi-winding transformer with appropriate turn ratios and an array of bidirectional power switches.

A diode-clamped based structure with a lower number of active devices was proposed by Gonzalez et al. [50] to eliminate the transformer from grid connected photovoltaic power generation. Very interestingly, this topology simultaneously addresses consequent issues such as galvanic isolation safety requirements, leakage currents, and injection of DC into the grid.

For a transformer less multilevel structure, a topology was presented by Wang et al. [51], with floating capacitors forming series-connected independent cells with a large number of redundant states so as to achieve active voltage balancing without any auxiliary circuits.

Du-et-al. [52] have shown implementation of a cascaded multilevel boost inverter for electric vehicle and hybrid electric vehicle applications without the use of inductors.

Ewanchuk-et-al. [53] have proposed incorporation of coupled reactors in each leg of the NPC topology, for low-voltage high-speed motor applications, offering an increased number of output voltage levels, higher frequency waveforms, reduced dead-time effects, and a significant reduction in harmonics.

On the basis of the above glimpse into the evolution of topologies, it can be seen that, apart from exclusive and extensive studies into various aspects of the classical topologies, researchers continue to contribute towards new multilevel structures for different applications. Moreover, with the growing realization of the advantages and viability of MLIs, they are also being employed in low-power applications [54—57]. Hence, MLIs are receiving much more and wider attention, both in terms of topologies and control schemes. As discussed previously, multilevel topologies have an important limitation: they need a large number of power semiconductor switches, which increases the cost and control complexity and tends to reduce their overall reliability and efficiency. Although low-voltage-rated switches can be utilized in a multilevel converter, each switch requires a gate driver and protection circuit. This makes the overall system more expensive and complex. Consequently, for the last few years, efforts have been directed to reducing the device count in MLIs [58-76]. The focus of this chapter is on multilevel topologies with a reduction in the number

of semiconductor devices. In the next section, a review of topologies is presented, introduced by their respective authors, with the sole objective of reducing the component count.

2.2 MLI TOPOLOGIES WITH REDUCED DEVICE COUNT

For the past few years, many researchers have been working on MLI topologies with a significant reduction in component count as compared to the classical topologies. Judging a topology without the consideration of the specific application is not only difficult, but also futile and unjustified. Often it can be seen that, while a topology is near-perfect for one application, it is useless for another. Still, in the context of this book, the general criteria for an overall assessment of a topology include:

1. The number of power switches used;
2. The total blocking voltage of the converter (which depends on the number of power switches and their respective voltage ratings);
3. The optimal controllability of the topology (in terms of possibility of charge balance control and switching of the differently rated switches); and
4. Possibility of employing asymmetric sources/capacitor voltage ratios.

While Parameters (1) and (2) directly influence the reliability of the inverter, efficiency is influenced by Parameters (1), (2), and (3) and application, performance and control complexity are governed by Parameter (3). The number of redundant states and consequently the programmability of fault-tolerant operation is directly influenced by (1) and (4). Based on these parameters, topologies with reduced component counts are discussed in this section.

2.3.1 CASCADED HALF-BRIDGE-BASED MULTILEVEL DC LINK INVERTER

Gui-Jia [12-15] introduced a new class of MLIs based on a multilevel DC link (MLDCL) and a bridge inverter to reduce the device count. An MLDCL, as shown in Fig. 2.1, has cascaded half-bridge cells with each cell having its own DC source. A multilevel voltage-source inverter can be formed by connecting one of the MLDCLs with a single-phase bridge inverter. The MLDCL, which is comprised of sources $V_{DC,J}$ {j = 1-3} and power switches Sj {j = 1-6}, generates a stepped waveform with one polarity, with or without PWM, to the bridge inverter, comprised of switches Qj {j = 1-4}, which in turn alternates the polarity to produce an alternating voltage. For an increased number of levels at the output, the MLDCL inverter can significantly reduce the switch count as well as the number of gate drivers as compared to the CHB topology [58]. It can be observed that, to obtain a given level, three switches conduct simultaneously in the MLDCL part and two switches conduct in the H-bridge part (Switches Q_1 and Q_4 for the positive half cycle, Q_2 and Q_3 for the negative half cycle, and Q_1 and Q_3 or Q_2 and Q_4 for zero level). It can be observed from the topology that each power switch of the H-bridge part must have a minimum voltage-blocking capability equal to the sum of the input voltage values. Thus, these switches are rated higher compared to the switches in the MLDCL part. However, since the zero level can be synthesized using switches of the MLDCL part, the higher-rated switches Q_j {j = 1—4} can be operated at fundamental switching frequency.

For a symmetric source configuration with $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC}$, it can be seen that the switches Sj {j = 1-6} need to block a voltage of V_{DC} and need to conduct a current equal to the load current. Switches Q_j {j = 1-4} need to block a voltage equal to $3V_{DC}$ and conduct a current equal to the load current. Voltage levels V_{DC}, $2V_{DC}$, and $3V_{DC}$ can be synthesized combining all the input sources in groups of one, two, and three, respectively, equal load sharing amongst them is possible. These redundancies also provide flexibility in voltage balancing when capacitors are used.

Regarding asymmetric source configurations in MLDCL topology, no analysis is offered in References [18,19]. Since subtractive combinations of the input DC levels cannot be synthesized, the trinary source configuration (i.e., $V_{DC,j} = 3^{j-1} * V_{DC}$) cannot be employed for this topology. A binary combination with $V_{DC,1} = V_{DC}$, $V_{DC,2} = 2V_{DC}$ and $V_{DC,3} = 4V_{DC}$ is possible since the voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$, $5V_{DC}$, $6V_{DC}$, and $7V_{DC}$ can be synthesized.

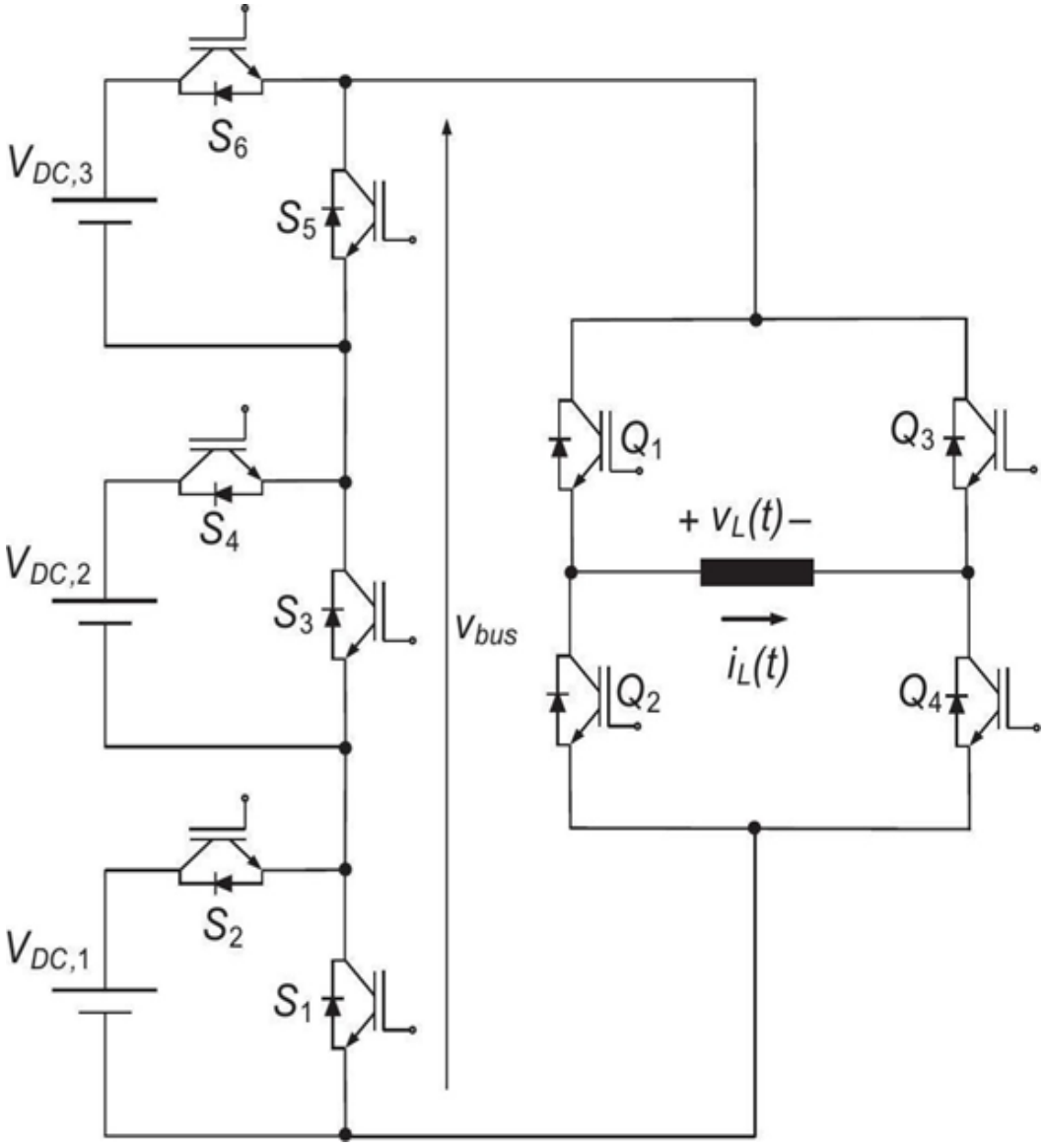

Fig. 2.1- Multi Level DC link Inverter

2.3.2 T-TYPE INVERTER

Gerardo Ceglia et al. [20,22] have presented a new MLI topology, named the T-type inverter, comprising an H-bridge output stage and bidirectional auxiliary switches. It offers a significant reduction in the number of power devices as compared to conventional topologies. A single-phase structure with four input voltage sources, namely, $V_{DC,1}$, $V_{DC,2}$, $V_{DC,3}$, and $V_{DC,4}$, as shown in Fig. 2.2. It comprises three switches Sj{j=1-3} which are bidirectional-blocking-bidirectional-conducting, while four switches Q_j{j=1-4} are unidirectional-blocking-bidirectional-conducting.

Thus, this topology inadvertently requires a mix of unidirectional and bidirectional power switches. It can be seen that the input DC values are required to be symmetric, i.e., $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$. This is because not all combinations of input voltage levels can be synthesized at the load terminals. In most cases, either a positive or negative combination can be synthesized, but not both.

For example, while a voltage level $-V_{DC,4}$ can be synthesized at the load terminals, the level $+ V_{DC,4}$ cannot be synthesized. Thus, it is essential that the input sources are symmetric. Also, lack of sufficient redundancies goes against effective voltage balancing. It can be also observed that equal load sharing amongst the input voltage sources is not possible as the number of valid states is very limited. For a given state, only two switches conduct simultaneously. The bidirectional switches are voltage rated at different values. While S3 should be minimally rated at $3V_{DC}$, S_2 and S_l should be rated at $2V_{DC}$ each. The H-bridge switches must each have minimum blocking capability of $4V_{DC}$. These higher voltage switches, however, can be operated with fundamental switching frequency.

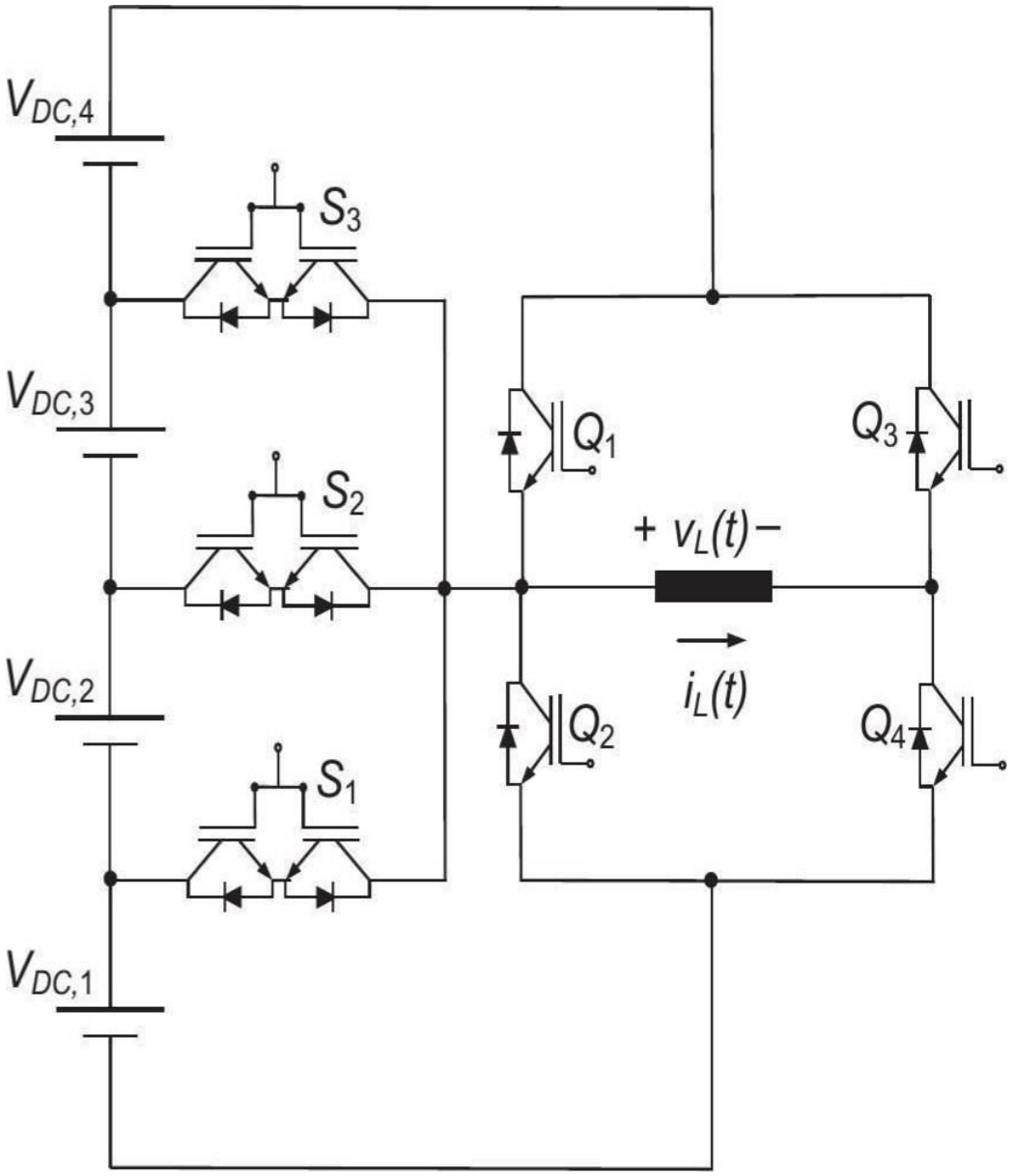

Fig. 2.2- A T-Type inverter with four input sources

2.3.2 SWITCHED SERIES/PARALLEL SOURCES—BASED MLI

Hinago and Koizumi [23,24] have proposed an MLI topology consisting of an H-bridge and DC sources which can be switched in series and in parallel. The topology reduces the number of gate driver circuits, thereby reducing the size and power consumption. The topology synthesizes the same number of output levels with a lower number of power switches as compared to a CHB topology. An important suggested application is for electric vehicular applications where a single battery composed of a number of series connected battery cells is available, which can be rearranged using the switched sources topology, hence reducing the requirement for switching devices. More importantly, the possibility of combining two or more sources in series and parallel gives enough flexibility for meeting voltage/power requirements in the vehicle drive system.

A Switched Series-Parallel Sources MLI with three input DC sources is shown in Fig. 2.3. It consists of two parts: the switched sources part which synthesizes a bus voltage V_{bus} (t) and the H-bridge part which synthesizes positive and negative cycles of voltage (t) to feed an AC load. Three sources, namely, $V_{DC,1}$, $V_{DC,2}$, and $V_{DC,3}$ and power switches $S_j\{j = 1\text{-}6\}$ constitute the switched sources part. Power switches $Q_j\{j = 1\text{-}4\}$ constitute the H-bridge part. For a symmetric source configuration, i.e., $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC}$, that voltage levels V_{DC} and $2V_{DC}$ can be synthesize with three states each, while one state is available for voltage level $3V_{DC}$. Moreover, the voltage stress experienced by the switches S_j {j = 1-6} would each be equal to VDC. An important limitation of this topology is that the switches $Q_j\{j = 1\text{-}4\}$ need to have a minimum blocking capability of summation of voltages of all voltage sources. Thus, for the symmetric source configuration with three sources, the H-bridge switches should possess a voltage-blocking capability of $3V_{DC}$. Another important limitation is that these switches with higher blocking capability cannot be operated at fundamental switching frequencies because the zero voltage level is not synthesized by the switched sources part. It can also be inferred from the table that, with input sources of equal voltages, equal load sharing amongst them is possible as the sources can be combined in all additive configurations. Various combinations can be

utilized in different cycles so as to equate the average current from each source, thereby equalizing the average power amongst the sources.

Although the topology enables the synthesis of all additive combinations of the input sources, subtractive combinations are not possible. Hence, trinary source configuration is not possible for this topology. Binary source configuration is, however, possible so as to maximize the number of levels in the output waveform. For example, in Fig. 2.3 for $V_{DC,1} = V_{DC}$, $V_{DC,2} = 2V_{DC}$, and $V_{DC,3} = 4V_{DC}$, all possible combinations, namely, V_{DC}, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$, $5V_{DC}$, $6V_{DC}$, and $7V_{DC}$ are obtained as $V_{bus}(t)$ by using States 1, 2, 4, 3, 6, 5, and 7, so that the load voltage waveform has 15 levels in equal steps of V_{DC}. Thus, binary, but not trinary, source configuration can be implemented using this topology.

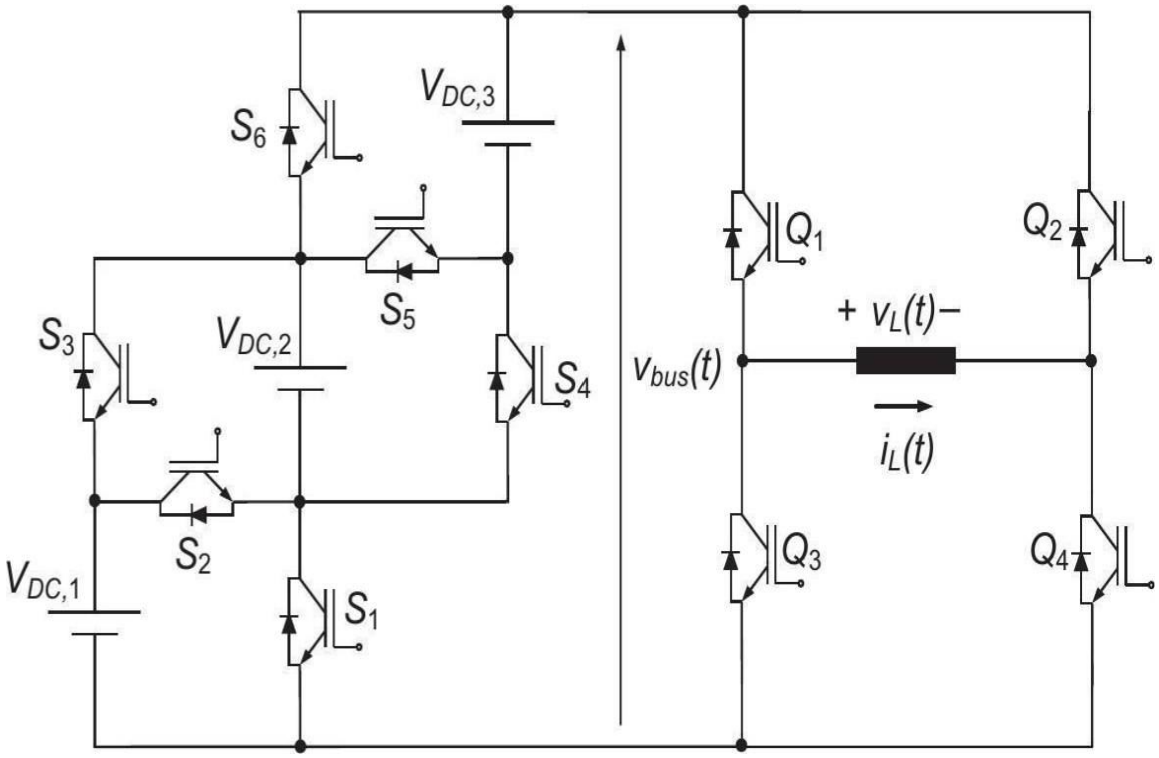

Fig. 2.3- A Switched Series / Parallel Source MLI

2.4 CONCLUSION

Form all the above discuss topology required either multiple DC source or single high voltage DC source coupled with series connected DC link capacitors for dividing the DC voltage into smaller one for generation of steps in output voltage. The complexity of the power circuit and their controller is very high. The number of floating ground connected switches is much higher than convention circuit therefore isolated DC supply requirement is high which increase the cost of the multi-level inverter. For generation of 5 level output minimum eight switches required.

CHAPTER 3

PROPOSED TOPOLOGY

3.1 INTRODUCTION

In this proposed work, a novel topology for multilevel inverter has been presented through which higher number of levels in output voltage may be achieved using multi-tapping transformer with single low voltage DC source and reduce switch counts respect to conventional multilevel inverters. In the suggested inverter only two switches will be turn on in each interval and so the conduction losses of converter will decrease. The selective harmonic elimination (SHE) method is used to generate gate pulses. Hence the loss of the converter includes switching losses and the operation of the loss decreases, and therefore the efficiency of the inverter increases. Design process of transformer turn ratio has been presented. Recommended topology is proposed as a suitable alternative to low voltage sources such as applications like Fuel Cell, PV, etc. In this topology we use transformer having 'N' number of tapping, single low voltage DC source and '$N + 4$' number of unidirectional switches to generate '$2 * N + 3$' levels in output voltage as shown in Fig. 1. Presented simulations results show the validity and effectiveness of the proposed topology. Fig. 1 presents a schematic illustration of an inverter circuit according to the present invention. The inverter circuit is coupled to an external single level of low voltage DC source. This circuit contain $N + 4$ switches for generation of $2 * N + 3$ levels in output voltage as shown in Fig. 3.1. It is unidirectional single stage converter which convert low voltage DC to required voltage AC.

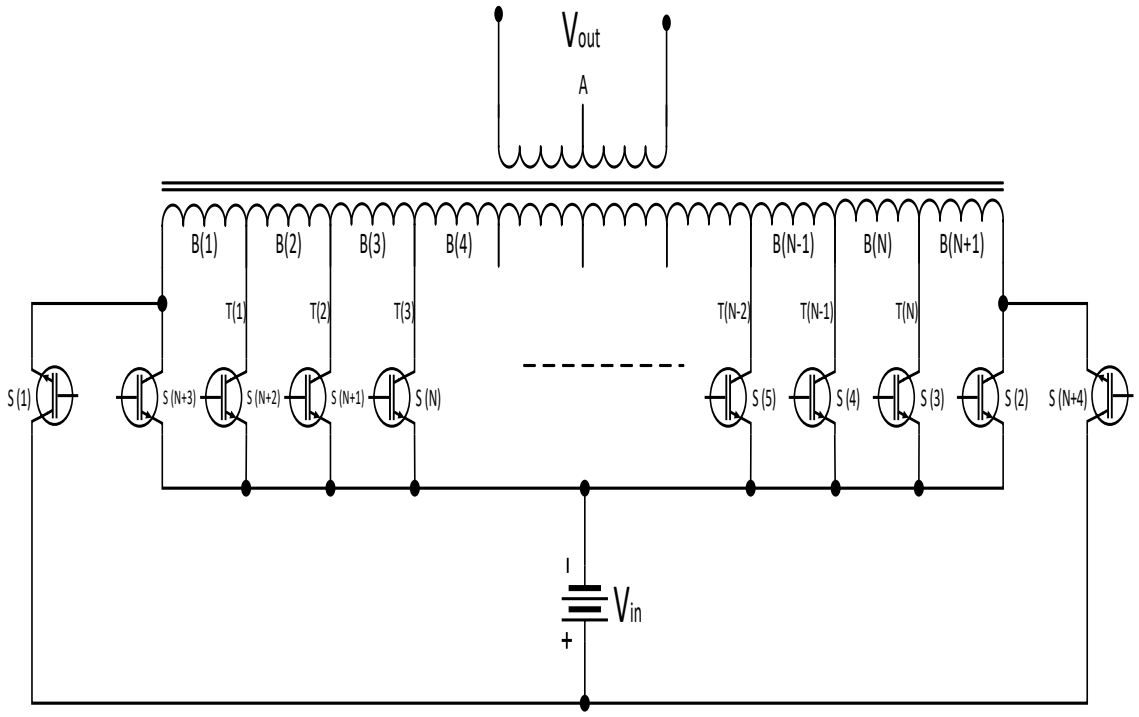

Fig. 3.1- Proposed Topology

Where,

N is number of primary winding tapping($T[i]$) with different number of turns per tapped winding ($B[i]$) in the transformer will be energized different primary tapped winding using unidirectional switches ($S[i]$) and single DC input voltage source(Vin). The output voltage ($Vout$) is directly proportional to DC voltage magnitude Vin and the ratio of number of secondary turns (A) and number of energized primary turns $\sum B(i)$ i.e.

$$Vout = Vin\frac{A}{\sum B(i)}$$

3.2 Level Generation

3.2.1 **Generate Positive level 1** For generation of level 1 in positive half cycle, need to energize all the primary turns falling between $B(1)\ to\ B(N+1)$ by turning on switches $S(1)\ \&\ S(2)$ and remaining switches are turned off. This configuration help to flow the current in a particular direction (let say forward direction) energized $\sum_{i=1}^{N+1} B(i)$ numbers of turns as shown in Fig. 3.2, therefore output voltage will be,

$$Vout = Vin\frac{A}{\sum_{i=1}^{N+1} B(i)} \quad \cdots p(1)$$

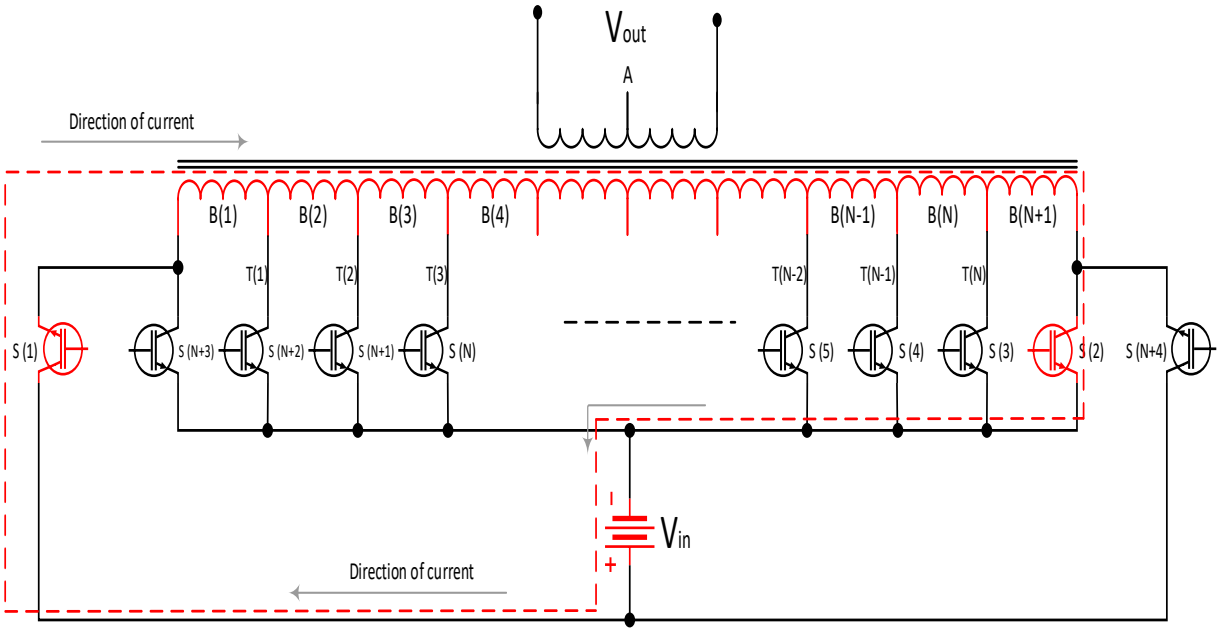

Fig. 3.2- Generate Positive Level 1

3.2.2 **Generate Negative Level 1** For generation of level 1 in negative half cycle, need to energize all the primary turns falling between $B(N+1)\ to\ B(1)$ by turning on switches $S(N+4)$ & $S(N+3)$ and remaining switches are turned off. This configuration help to flow the current in the opposite direction energized $\sum_{i=1}^{N+1} B(i)$ numbers of turns as shown in Fig. 3.3, therefore output voltage will be

$$Vout = Vin\frac{-A}{\sum_{i=1}^{N+1} B(i)} \quad \cdots n(1)$$

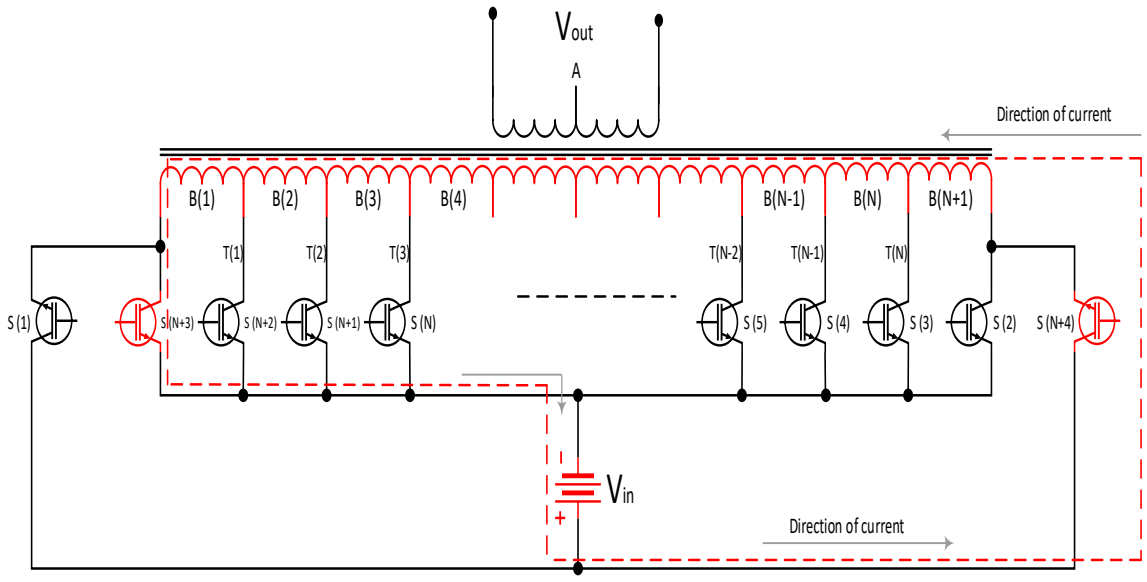

Fig. 3.3- Generate Negative Level 1

3.2.3 **Generate Positive level 2** For generation of level 2 in positive half cycle, need to energize all the primary turns falling between $B(1)\ to\ B(N)$ by turning on switches $S(1)\ \&\ S(3)$ and remaining switches are turned off. This configuration help to flow the current in the forward direction energized $\sum_{i=1}^{N} B(i)$ numbers of turns as shown in Fig. 3.4, therefore output voltage will be,

$$Vout = Vin\frac{A}{\sum_{i=1}^{N} B(i)} \quad \cdots p(2)$$

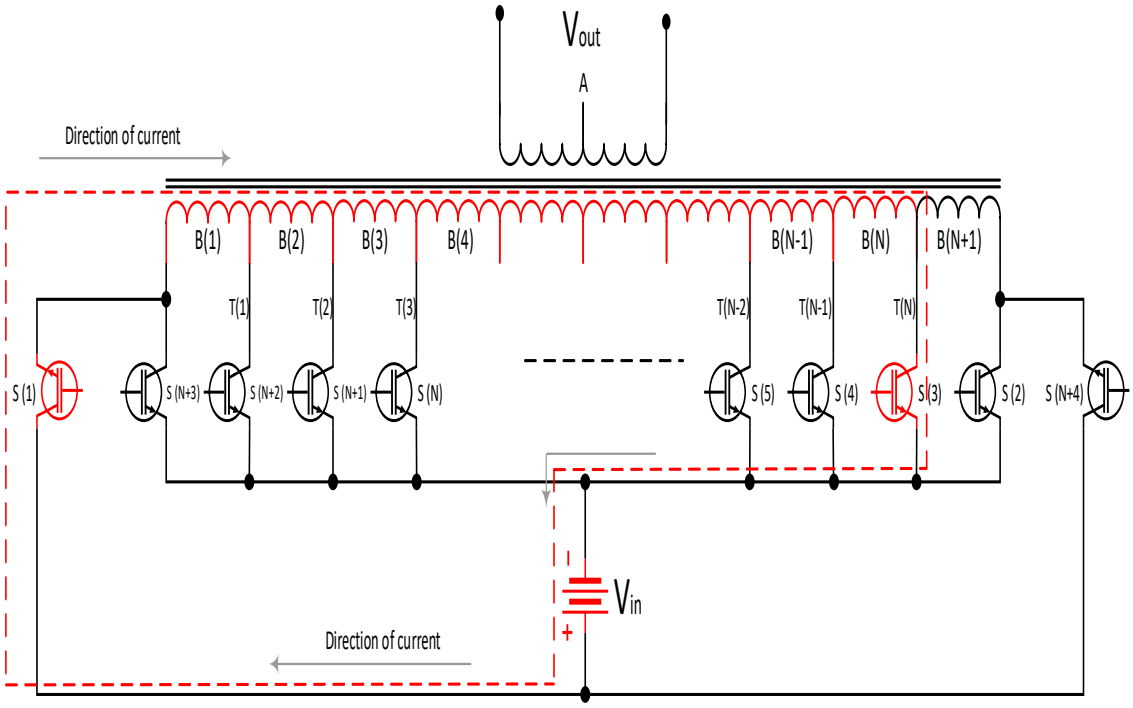

Fig. 3.4- Generate Positive Level 2

3.2.4 **Generate Negative Level 2** For generation of level 2 in negative half cycle, need to energize all the primary turns falling between $B(N+1)\ to\ B(2)$ by turning on switches $S(N+4)$ & $S(N+2)$ and remaining switches are turned off. This configuration help to flow the current in the opposite direction energized $\sum_{i=2}^{N+1} B(i)$ numbers of turns as shown in Fig. 3.5, therefore output voltage will be,

$$Vout = Vin \frac{-A}{\sum_{i=2}^{N+1} B(i)} \quad \cdots n(2)$$

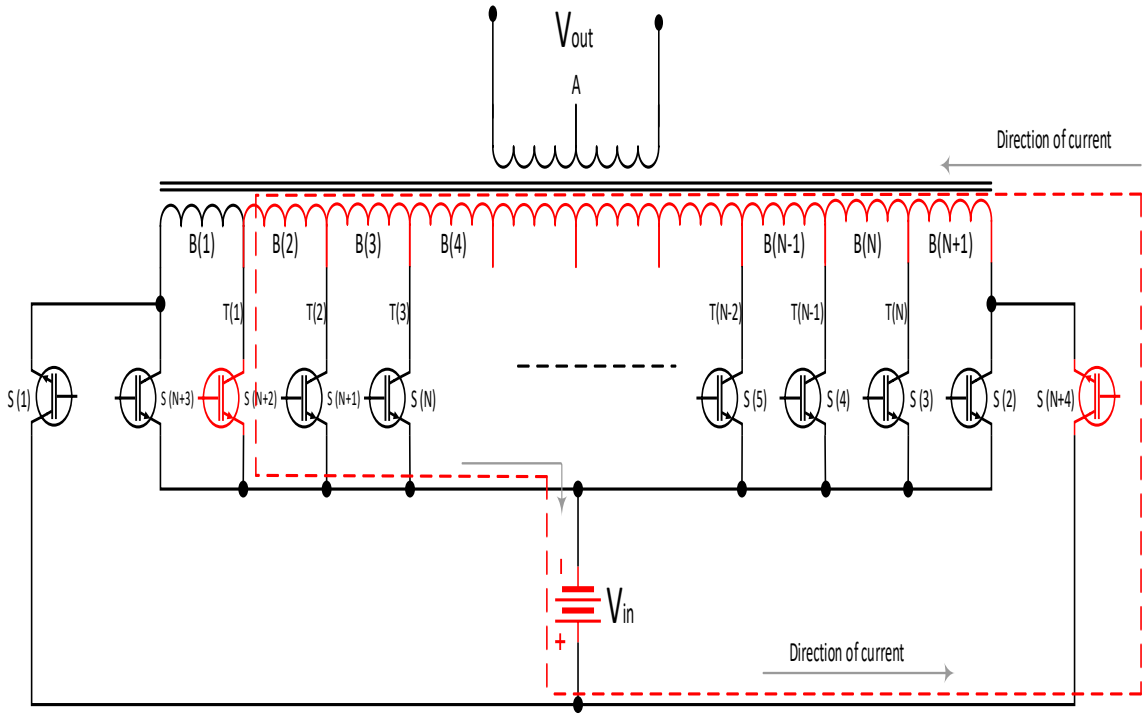

Fig. 3.5- Generate Negative Level 2

3.2.5 **Generate Positive level 3** For generation of level 3 in positive half cycle, need to energize all the primary turns falling between $B(1)\ to\ B(N-1)$ by turning on switches $S(1)\ \&\ S(4)$ and remaining switches are turned off. This configuration help to flow the current in the forward direction energized $\sum_{i=1}^{N-1} B(i)$ numbers of turns as shown in Fig. 3.6, therefore output voltage will be,

$$Vout = Vin\frac{A}{\sum_{i=1}^{N-1} B(i)} \quad \cdots p(3)$$

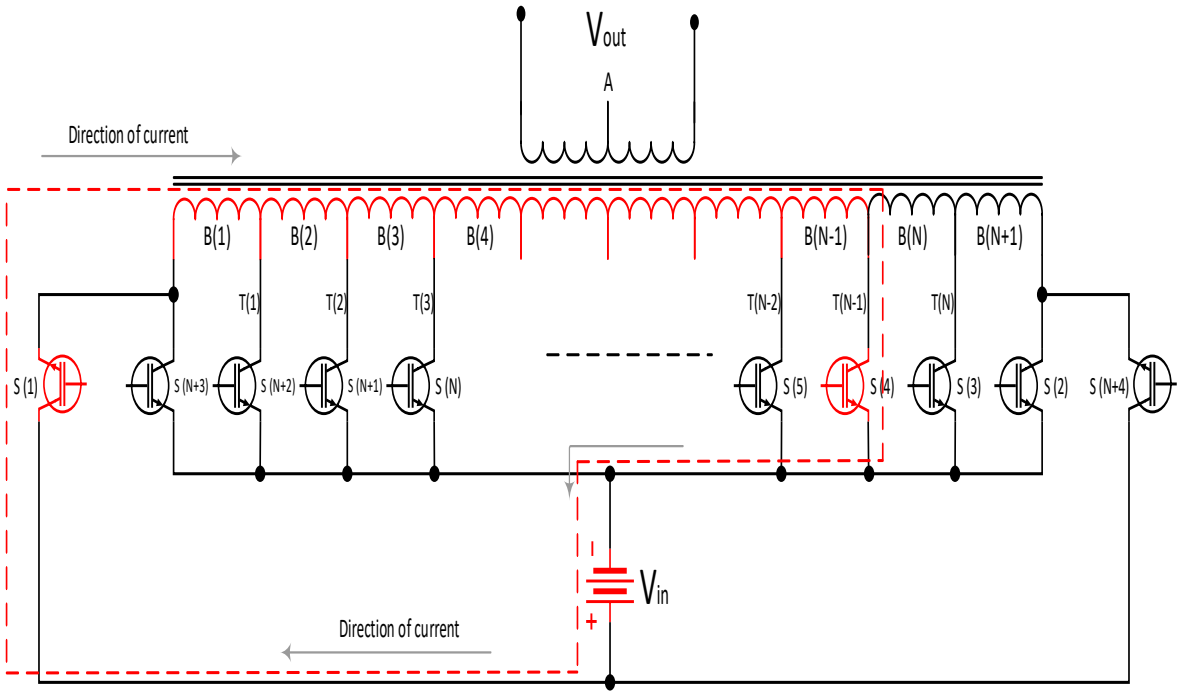

Fig. 3.6- Generate Positive Level 3

3.2.6 **Generate Negative Level 3** For generation of level 3 in negative half cycle, need to energize all the primary turns falling between $B(N+1)\ to\ B(3)$ by turning on switches $S(N+4)$ & $S(N+1)$ and remaining switches are turned off. This configuration help to flow the current in the opposite direction energized $\sum_{i=3}^{N+1} B(i)$ numbers of turns as shown in Fig. 3.7, therefore output voltage will be,

$$Vout = Vin \frac{-A}{\sum_{i=3}^{N+1} B(i)} \quad \cdots n(3)$$

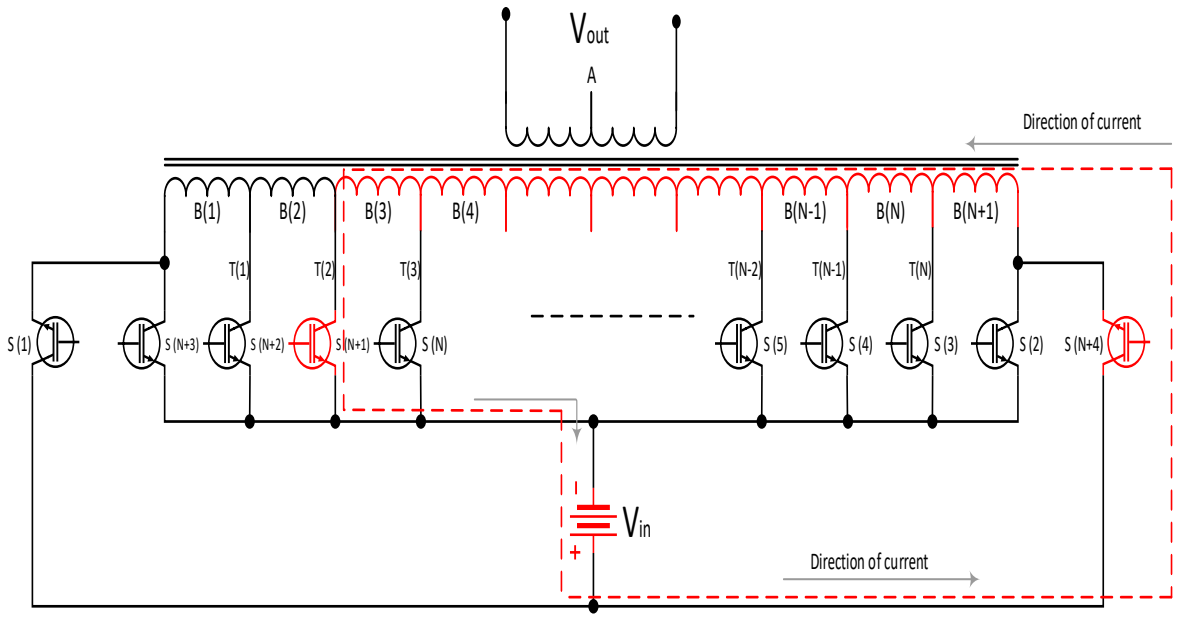

Fig. 3.7- Generate Negative Level 3

3.2.7 **Generate Positive level 4** For generation of level 4 in positive half cycle, need to energize all the primary turns falling between $B(1)\ to\ B(N-2)$ by turning on switches $S(1)\ \&\ S(5)$ and remaining switches are turned off. This configuration help to flow the current in the forward direction energized $\sum_{i=1}^{N-2} B(i)$ numbers of turns as shown in Fig. 3.8, therefore output voltage will be,

$$Vout = Vin\frac{A}{\sum_{i=1}^{N-2} B(i)} \quad \cdots p(4)$$

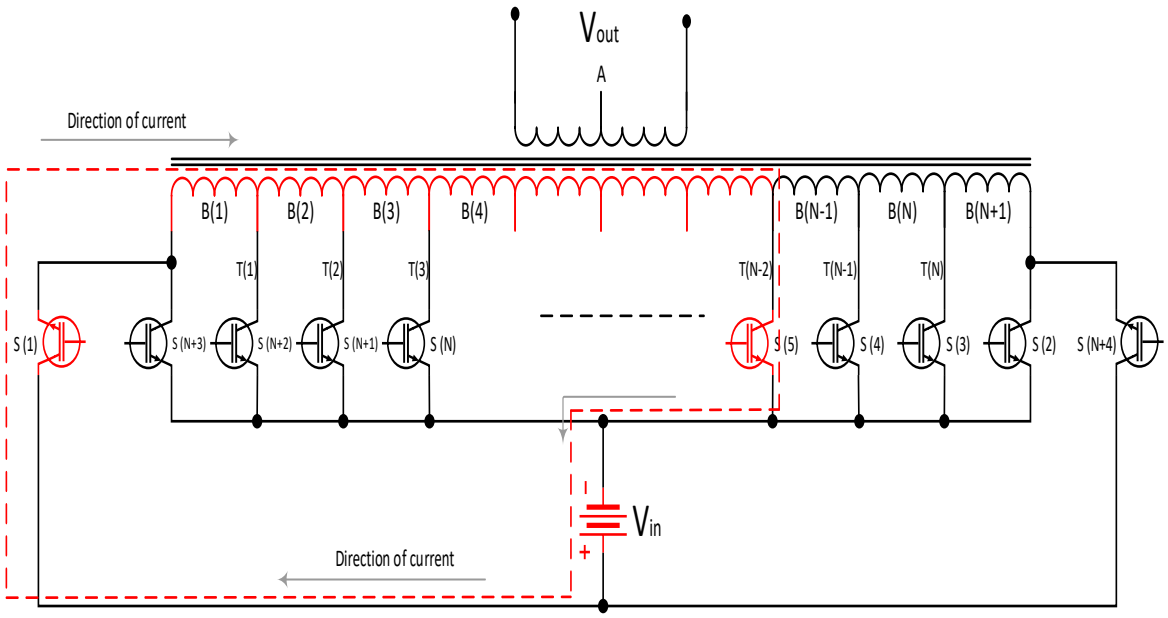

Fig. 3.8- Generate Positive Level 4

3.2.8 **Generate Negative Level 4** For generation of level 4 in negative half cycle, need to energize all the primary turns falling between $B(N+1)\ to\ B(3)$ by turning on switches $S(N+4)$ & $S(N+1)$ and remaining switches are turned off. This configuration help to flow the current in the opposite direction energized $\sum_{i=3}^{N+1} B(i)$ numbers of turns as shown in Fig. 3.9, therefore output voltage will be,

$$Vout = Vin\frac{-A}{\sum_{i=3}^{N+1} B(i)} \quad \cdots n(4)$$

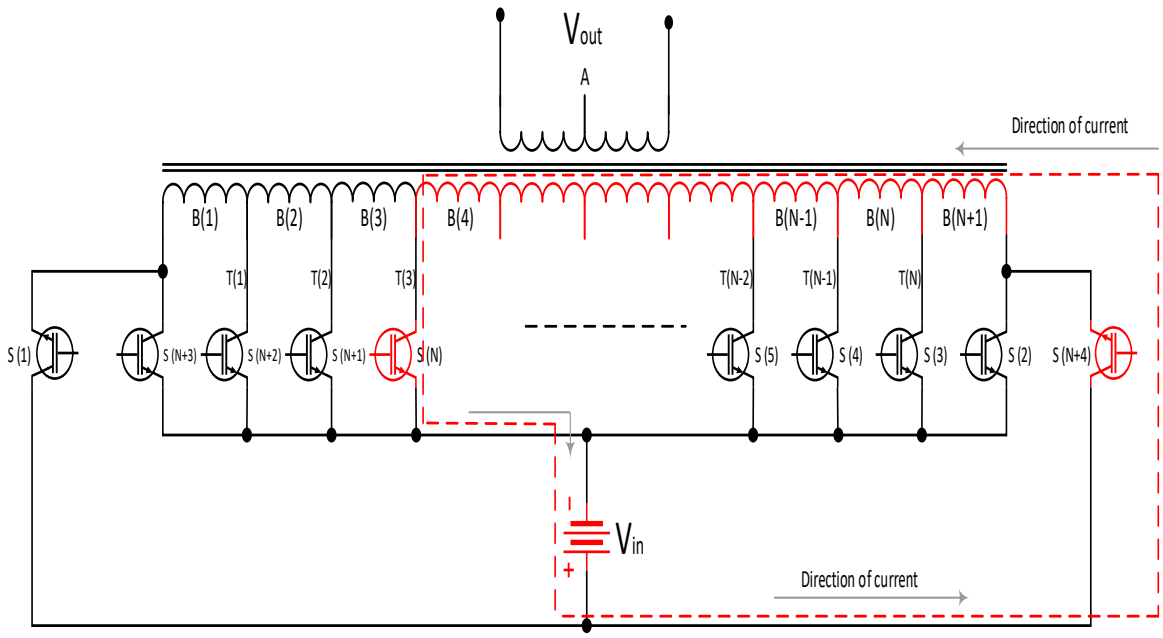

Fig. 3.9- Generate Negative Level 4

3.2.9 **Generate Positive level N-1** For generation of level $N-1$ in positive half cycle, need to energize all the primary turns falling between $B(1)\ to\ B(3)$ by turning on switches $S(1)$ & $S(N)$ and remaining switches are turned off. This configuration help to flow the current in the forward direction energized $\sum_{i=1}^{3} B(i)$ numbers of turns as shown in Fig. 3.10, therefore output voltage will be,

$$Vout = Vin\frac{A}{B(1)+B(2)+B(3)} \quad \cdots p(N-1)$$

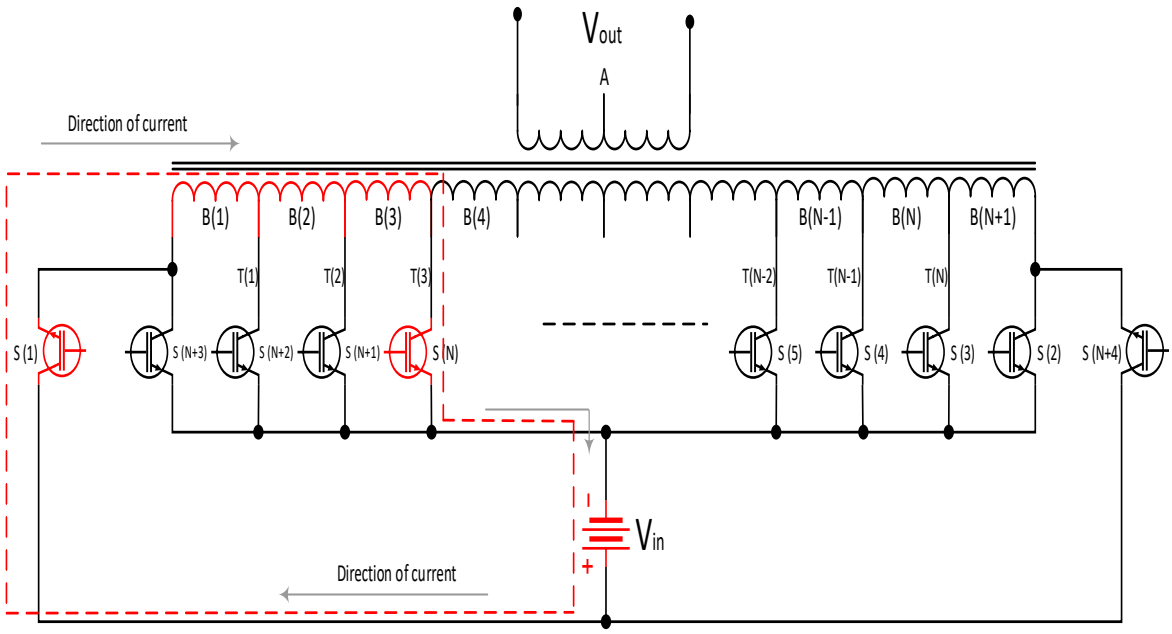

Fig. 3.10- Generate Positive Level N-1

3.2.10 **Generate Negative Level N-1** For generation of level $N-1$ in negative half cycle, need to energize all the primary turns falling between $B(N+1)\ to\ B(N-1)$ by turning on switches $S(N+4)\ \&\ S(5)$ and remaining switches are turned off. This configuration help to flow the current in the opposite direction energized $\sum_{i=N-1}^{N+1} B(i)$ numbers of turns as shown in Fig. 3.11, therefore output voltage will be,

$$Vout = Vin\frac{-A}{B(N+1)+B(N)+B(N-1)} \quad \cdots n(N-1)$$

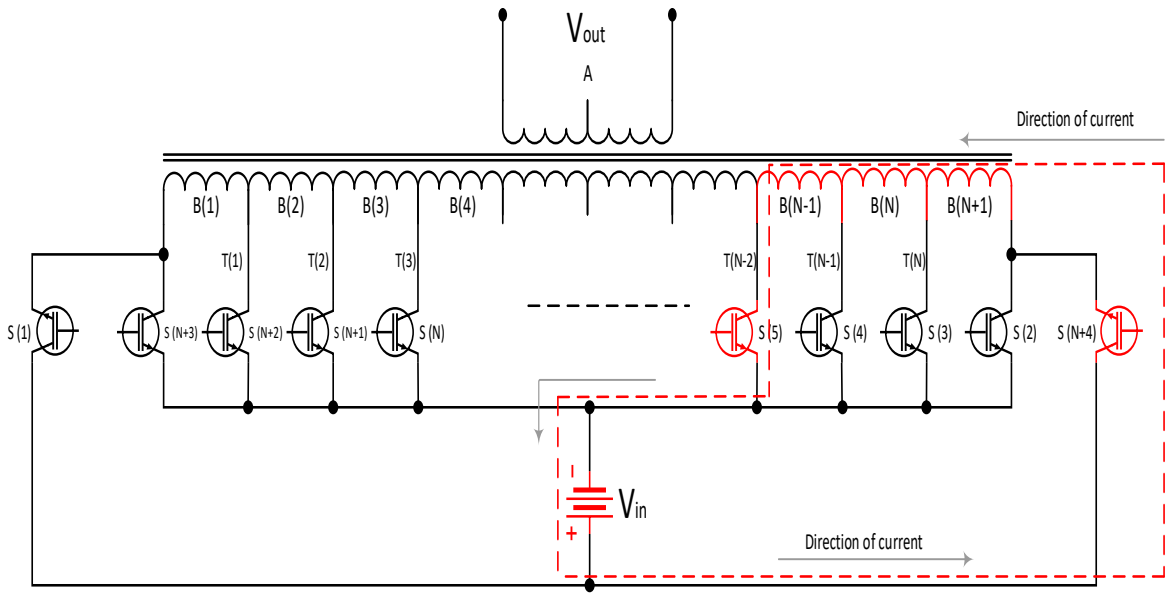

Fig. 3.11- Generate Negative Level N-1

3.2.11 **Generate Positive level N** For generation of level N in positive half cycle, need to energize all the primary turns of $B(1)$ & $B(2)$ by turning on switches $S(1)$ & $S(N+1)$ and remaining switches are turned off. This configuration help to flow the current in the forward direction energized $\sum_{i=1}^{2} B(i)$ numbers of turns as shown in Fig. 3.12, therefore output voltage will be,

$$Vout = Vin \frac{A}{B(1) + B(2)} \quad \cdots p(N)$$

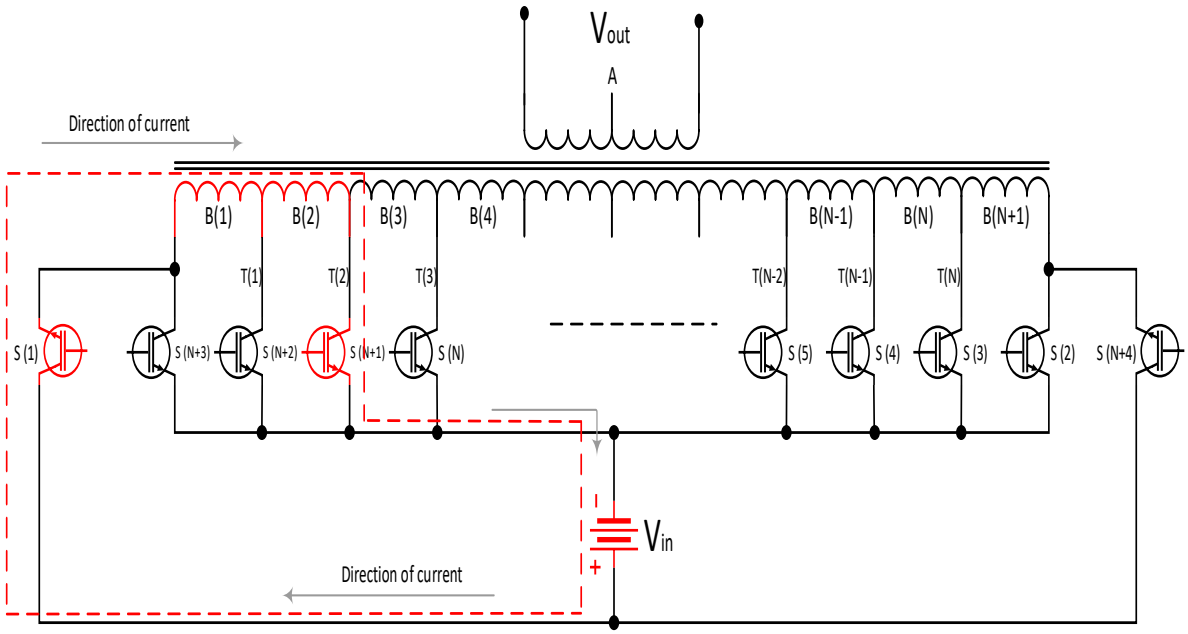

Fig. 3.12- Generate Positive Level N

3.2.12 **Generate Negative Level N** For generation of level N in negative half cycle, need to energize all the primary turns of $B(N+1)$ & $B(N)$ by turning on switches $S(N+4)$ & $S(4)$ and remaining switches are turned off. This configuration help to flow the current in the opposite direction energized $\sum_{i=N}^{N+1} B(i)$ numbers of turns as shown in Fig. 3.13, therefore output voltage will be,

$$Vout = Vin\frac{-A}{B(N+1)+B(N)} \quad \cdots n(N)$$

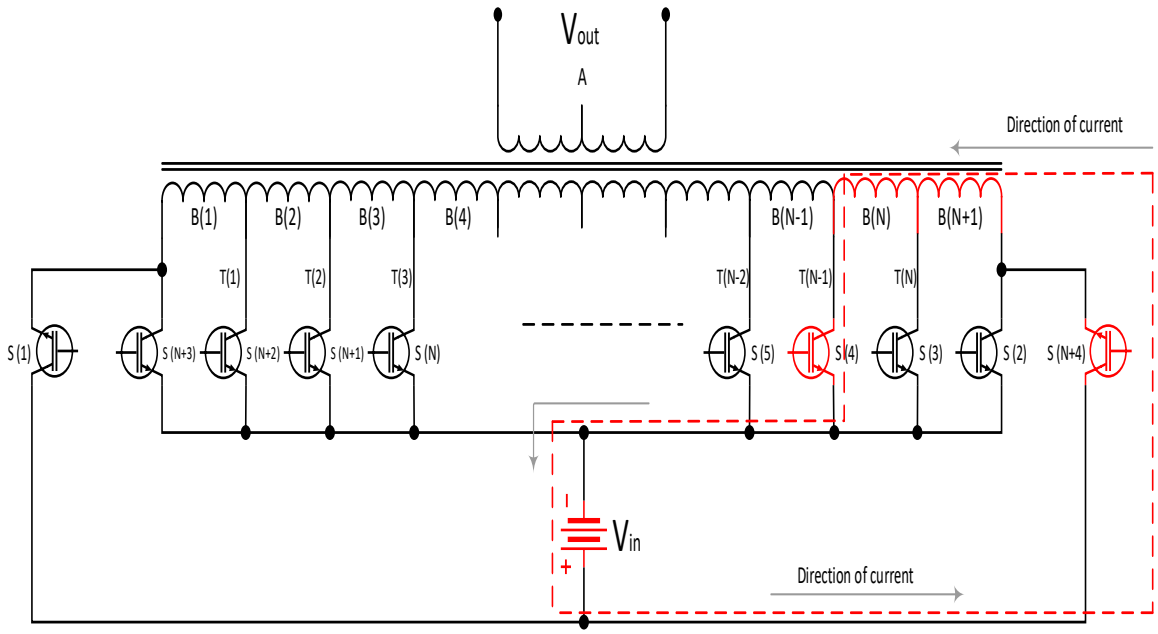

Fig. 3.13- Generate Negative Level N

3.2.13 **Generate Positive level N+1** For generation of level $N+1$ in positive half cycle, need to energize all the primary turns of $B(1)$ by turning on switches $S(1)$ & $S(N+2)$ and remaining switches are turned off. This configuration help to flow the current in the forward direction energized $B(1)$ numbers of turns as shown in Fig. 3.14, therefore output voltage will be,

$$Vout = Vin\frac{A}{B(1)} \quad \cdots p(N+1)$$

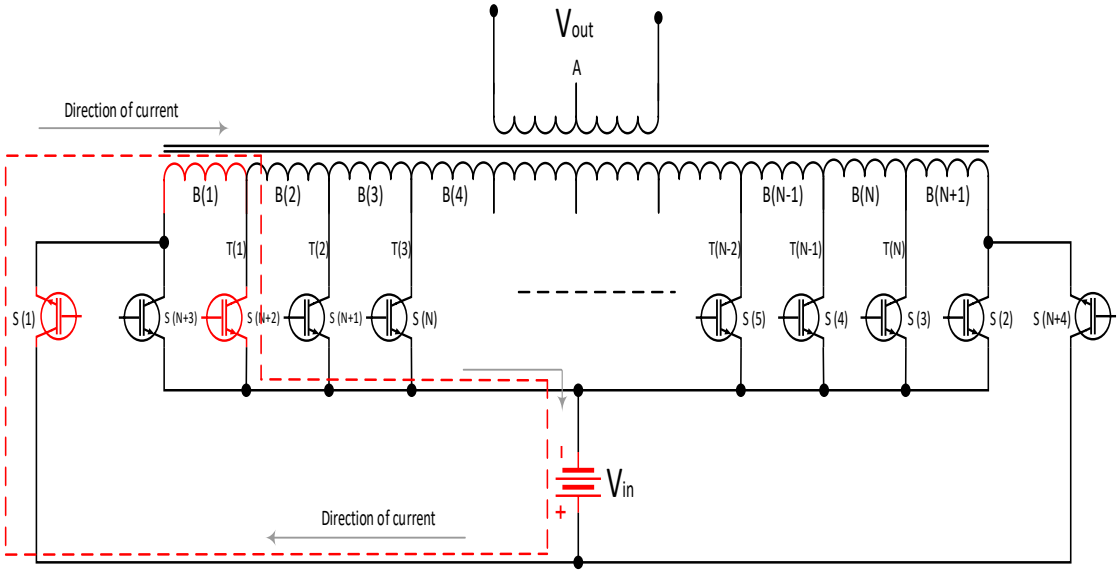

Fig. 3.14- Generate Positive Level N+1

3.2.14 **Generate Negative Level N+1** For generation of level N in negative half cycle, need to energize all the primary turns of $B(N+1)$ by turning on switches $S(N+4)$ & $S(3)$ and remaining switches are turned off. This configuration help to flow the current in the opposite direction energized $B(N+1)$ numbers of turns as shown in Fig. 3.15, therefore output voltage will be,

$$Vout = Vin\frac{-A}{B(N+1)} \quad \cdots n(N+1)$$

4

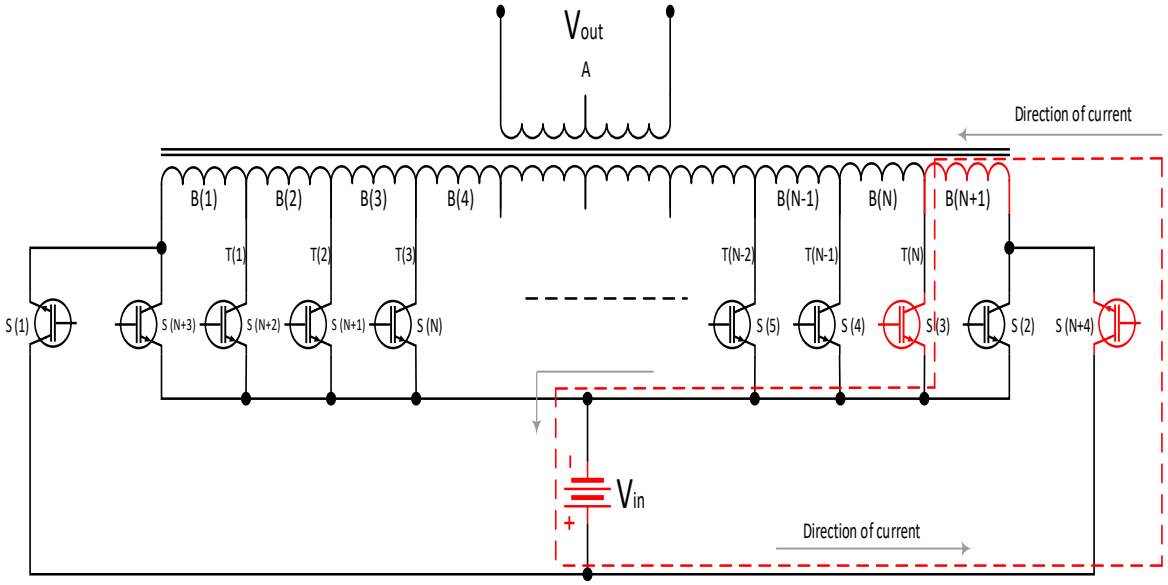

Fig. 3.15- Generate Negative Level N+1

3.3 WORKING

For reduction in THD the power electronic switches should be turned on and off in particular pattern.

3.3.1 **INCREASING POSITIVE HALF WAVE** for starting of positive half wave the switches S(1) & S(2) must be turned on and after particular time S(1) & S(3) and so on up to switches S(1) & S(N+2) are turned on. This make an increasing stair like structure with different voltage level according to equations $p(1)\ to\ p(N+1)$ as shown in Fig.3.16 for $N = 9$. From the equation $p(1)$, V_{out} is minimum because number of energized primary turn are maximum, while from equation $p(N+1)$ V_{out} is maximum because energized primary turn are minimum.

3.3.2 **DECREASING POSITIVE HALF WAVE** for reaching ground the reverse path must follow i.e. S(1) & S(N+2) after particular time S(N+2) must switch of and S(N+1) turn on up to S(2), so that decreasing stair like structure with different voltage level according to equations $p(N+1)\ to\ p(1)$ as shown in Fig.3.16 for $N = 9$ but similar to increasing positive half wave for the symmetry of wave.

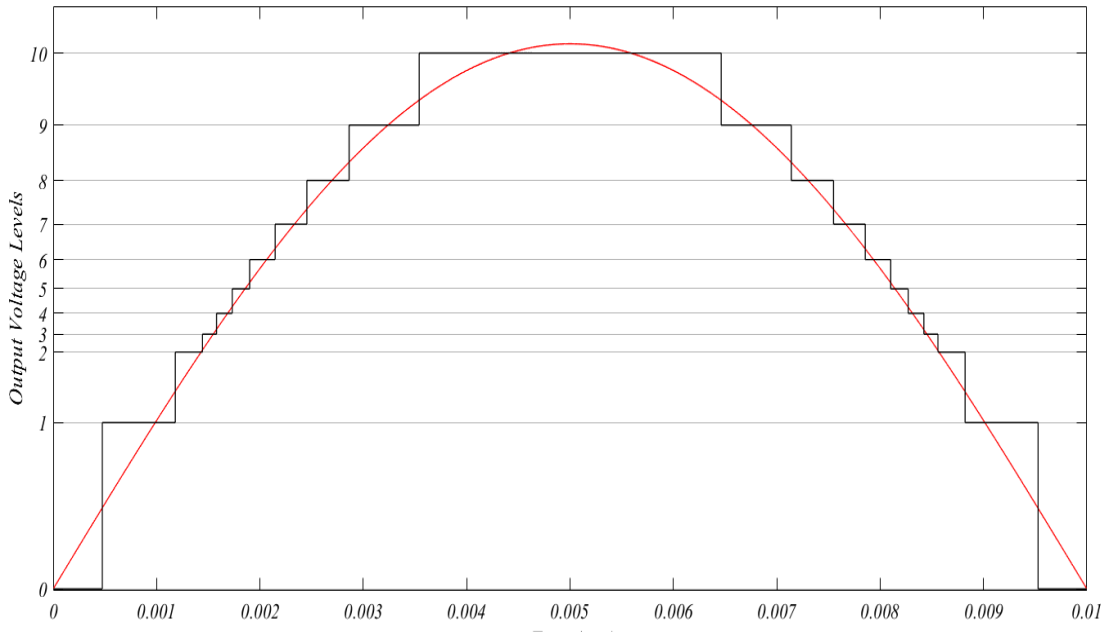

Fig 3.16 Positive half wave for N = 9

3.3.3 **INCREASING NEGATIVE HALF WAVE** similar to increasing positive half wave but switches S(N+4) & S(N+3) to S(3) must turn on and off according to particular pattern time to mate the output voltage like decreasing stair like structure according to equations $n(1)\ to\ n(N+1)$ as shown in Fig.3.17 for $N = 9$.

3.3.4 **DECREASING NEGATIVE HALF WAVE** again reaching to ground the reverse path of increasing negative half wave must follow i.e. S(N+4) & S(3) to S(N+3) must turn on and off according to particular pattern time to mate the output voltage like decreasing stair like structure according to equations $n(N+1)\ to\ n(1)$ as shown in Fig.3.17 for $N = 9$.

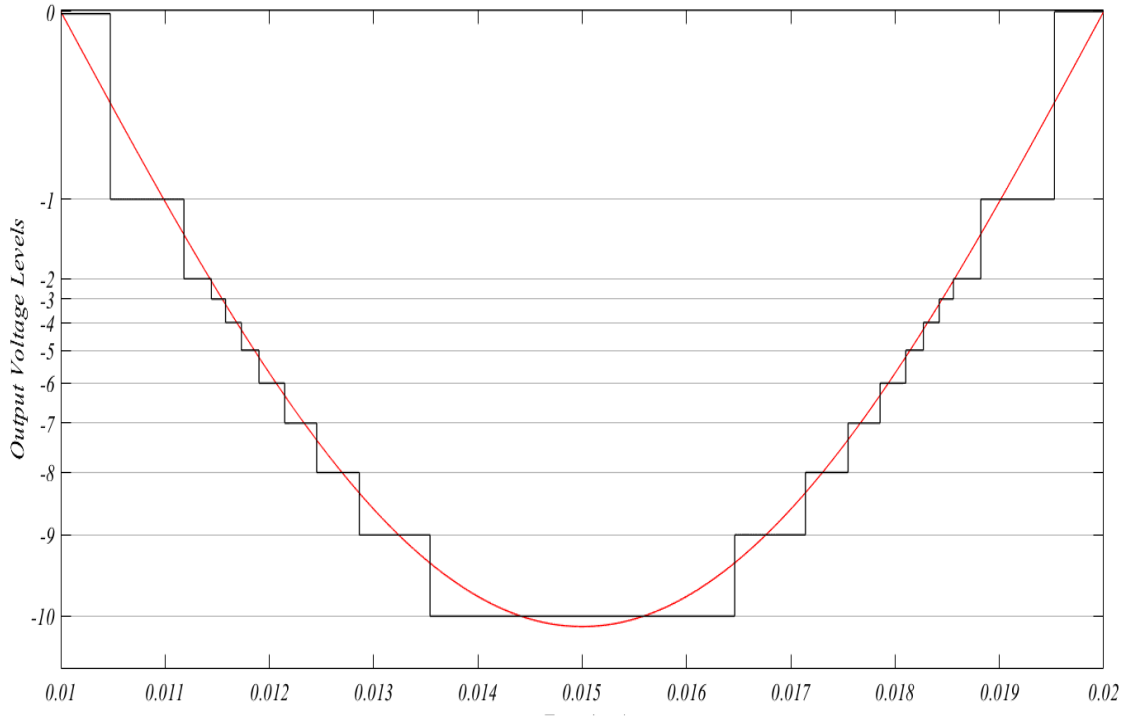

Fig. 3.17 Negative half wave for N = 9

The difference in voltage level is due to difference in number of energized primary turns, and the output voltage is inversely proportional to percentage of energized primary winding and the direction of current in primary winding.

3.4 **SIMULATION & RESULT**

The simulation is done for both $N = 1$ and $N = 9$, as single phase and three phase inverter without any filter, where N is number tapping in primary winding of the transformer.

3.4.1 FOR $N = 1$ SINGLE PHASE INVERTER

The number of switches used is $N + 4 = 5$,

The number of levels in output voltage is $2 * N + 3 = 5$,

The simulated model is shown in Fig 3.18. The voltage waveform of pure resistive is shown in Fig 3.19. And the output voltage THD is shown in Fig. 3.20.

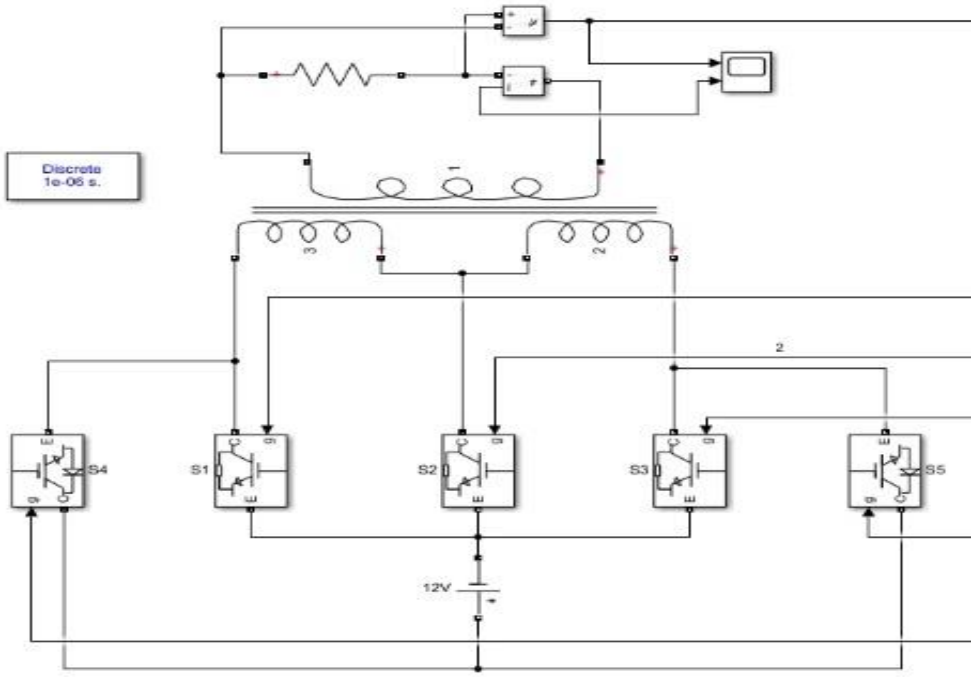

Fig. 3.18 Simulated Model for N=1 single phase inverter

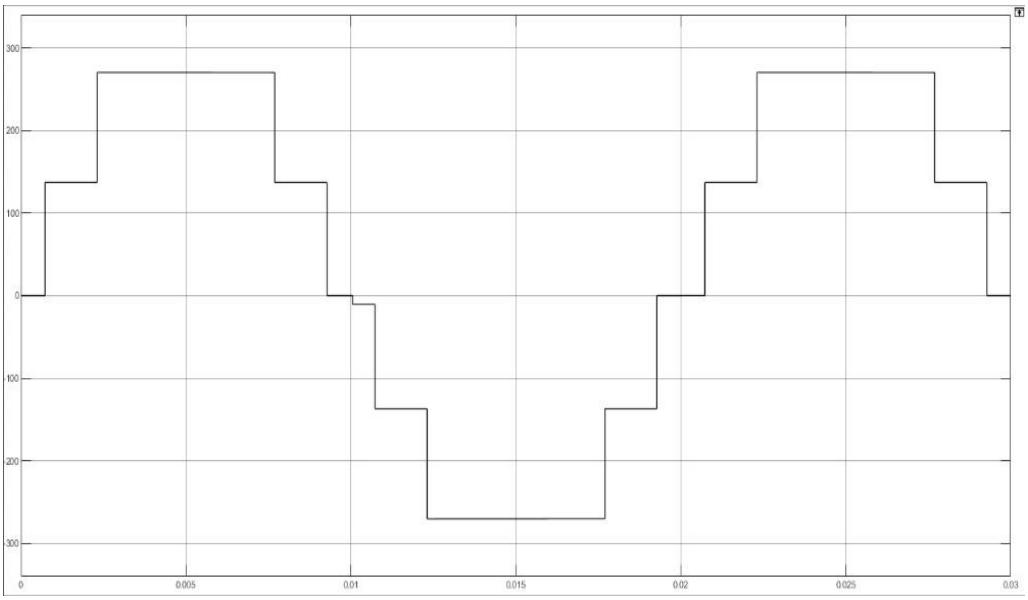

Fig. 3.19 Voltage Waveform for N=1 single phase inverter

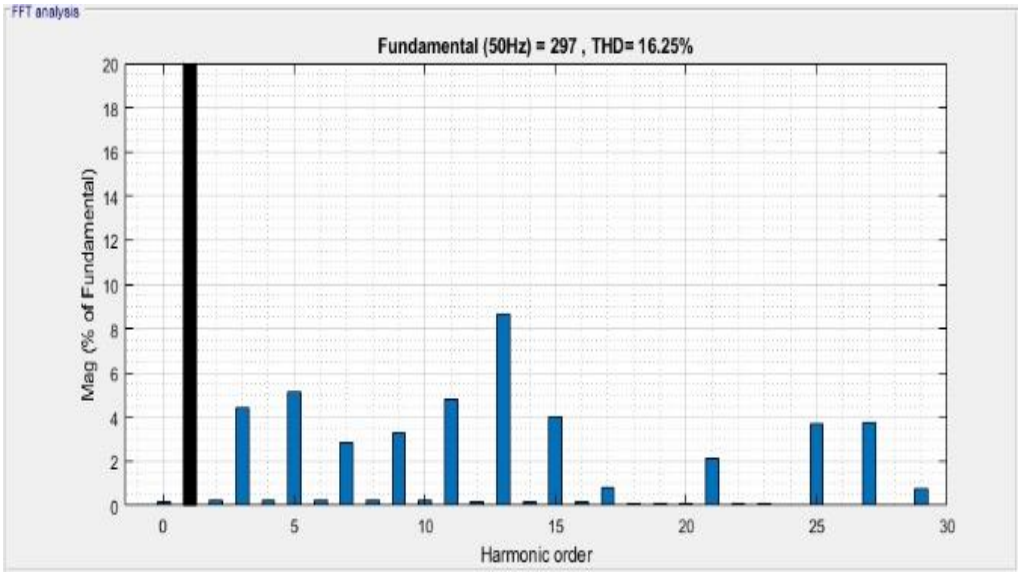

Fig. 3.20 THD in Voltage for N=1 single phase inverter

3.4.2 FOR $N = 1$ THREE PHASE STAR CONNECTED INVERTER

The number of switches used is $3 * (N + 4) = 15$,

The number of levels in output voltage is $4 * N + 3 = 7$,

The simulated model is shown in Fig 3.21. The voltage waveform of pure resistive is shown in Fig 3.22. And the output voltage THD is shown in Fig. 3.23.

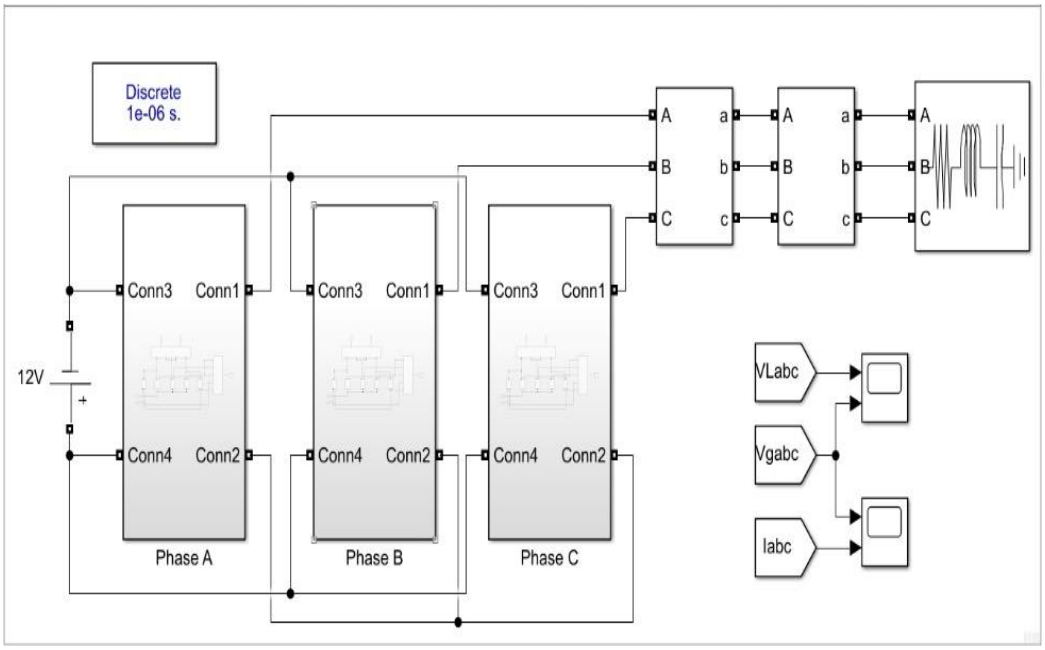

Fig. 3.21 Simulated Model for N=1 Three phase inverter

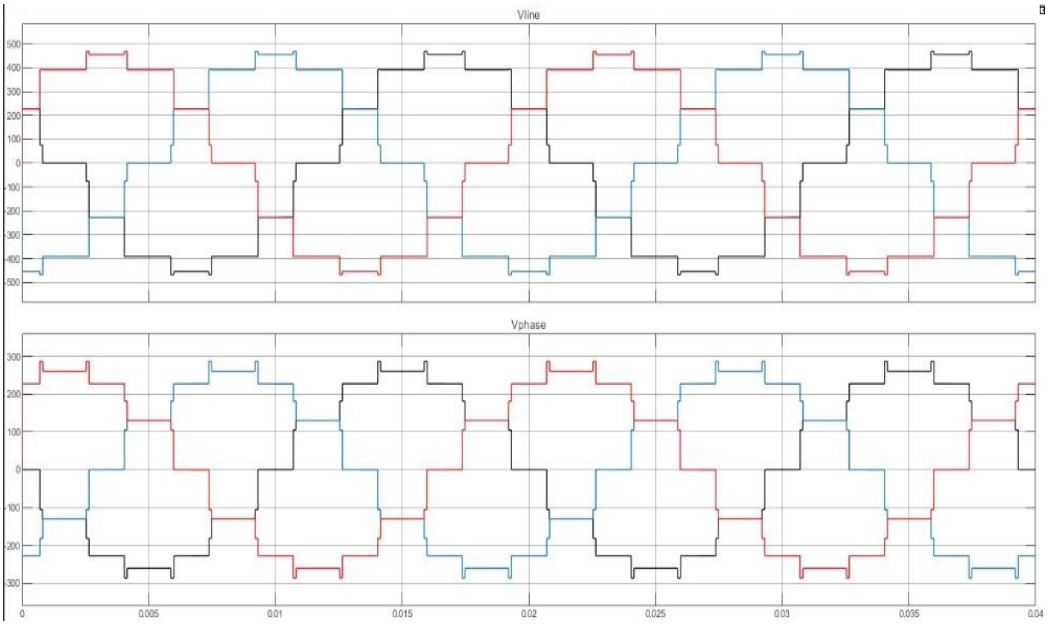

Fig. 3.22 Voltage Waveform for N=1 Three phase inverter

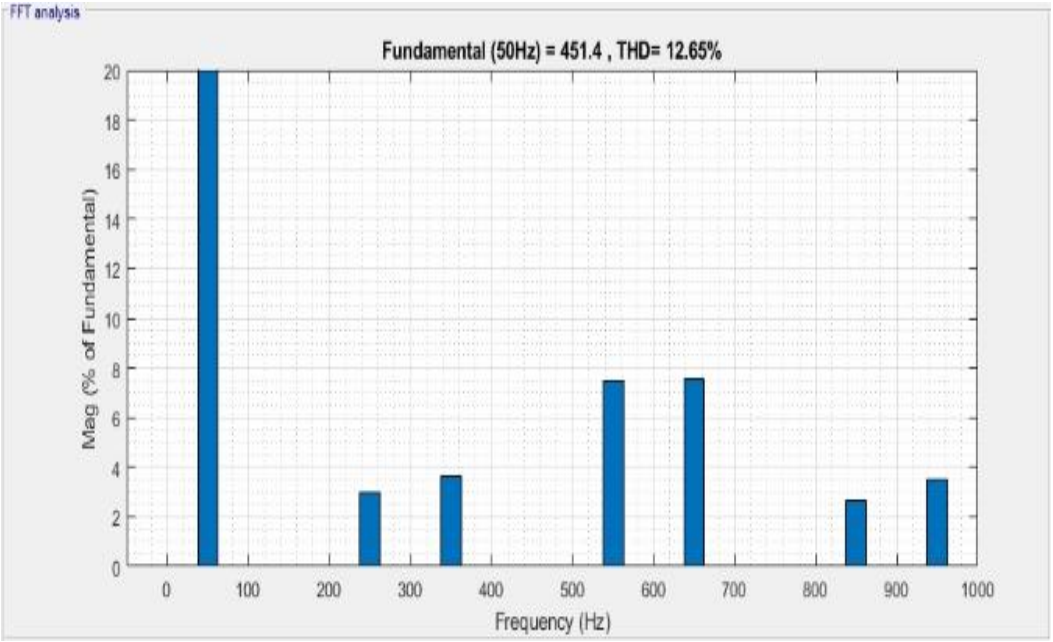

Fig. 3.23 THD in Voltage for N=1 Three phase inverter

3.4.3 FOR $N = 9$ SINGLE PHASE INVERTER

The number of switches used is $N + 4 = 13$,

The number of levels in output voltage is $2 * N + 3 = 21$,

The simulated model is shown in Fig 3.24. The voltage waveform of pure resistive is shown in Fig 3.25. And the output voltage THD is shown in Fig. 3.26.

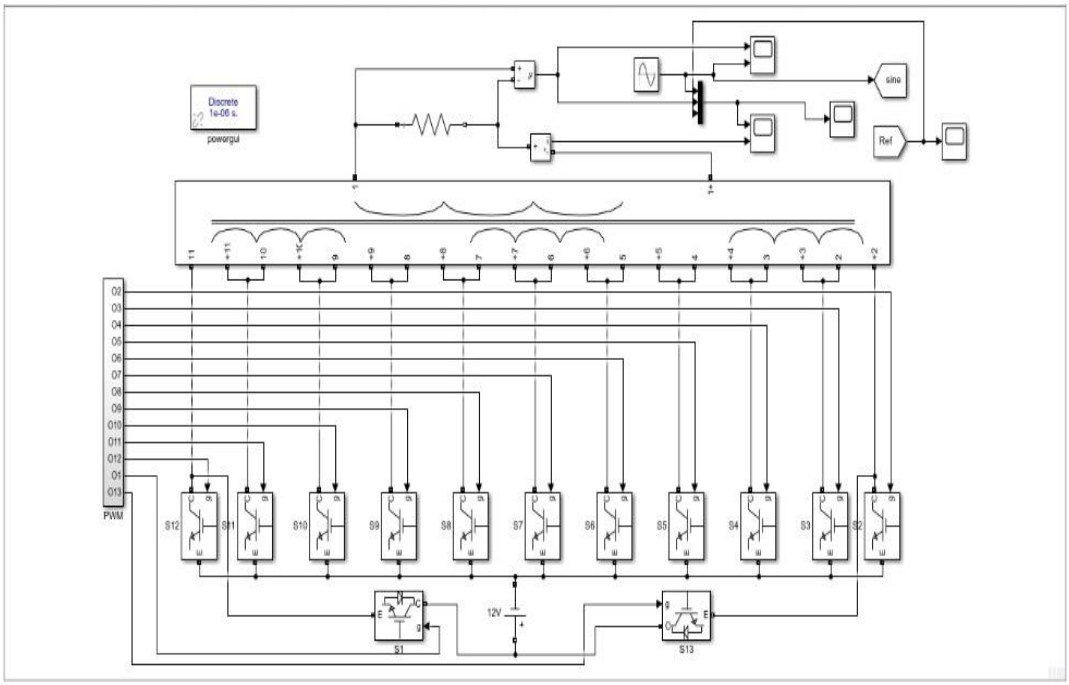

Fig. 3.24 Simulated Model for N=9 single phase inverter

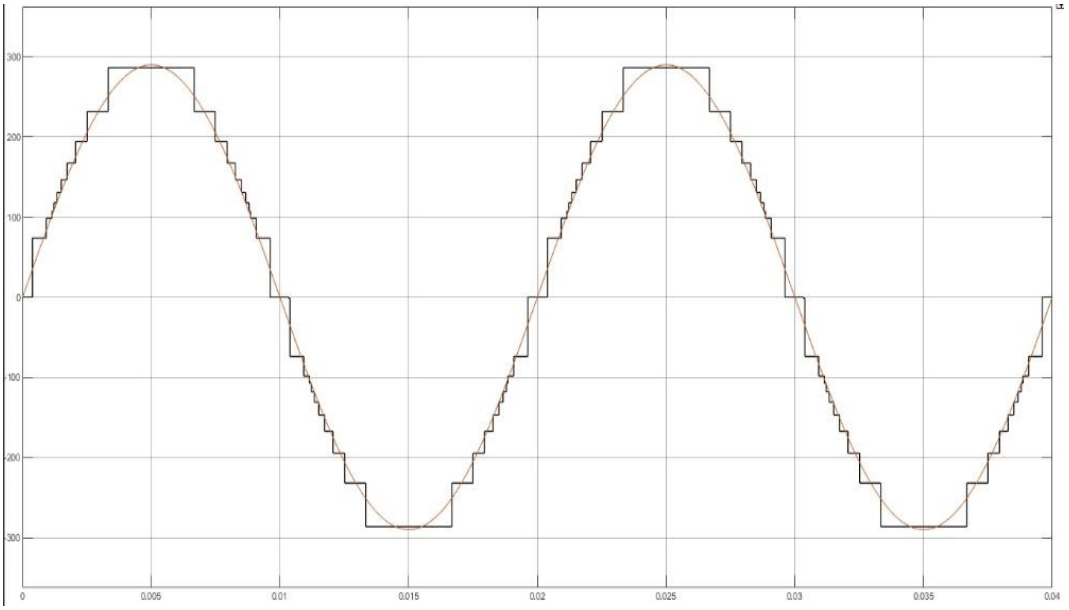

Fig. 3.25 Voltage Waveform for N=9 single phase inverter

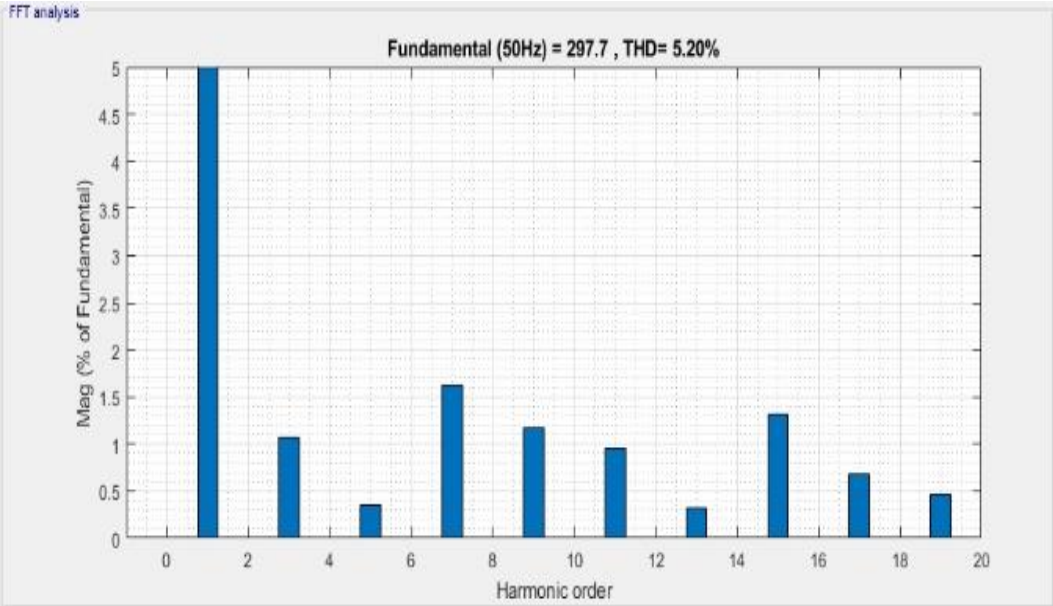

Fig. 3.26 THD in Voltage for N=9 single phase inverter

3.4.4 FOR $N = 9$ THREE PHASE STAR CONNECTED INVERTER

The number of switches used is $3 * (N + 4) = 39$,

The number of levels in output voltage is $4 * N + 3 = 39$,

The simulated model is shown in Fig 3.29. The voltage waveform of pure resistive is shown in Fig 3.28. And the output voltage THD is shown in Fig. 3.29.

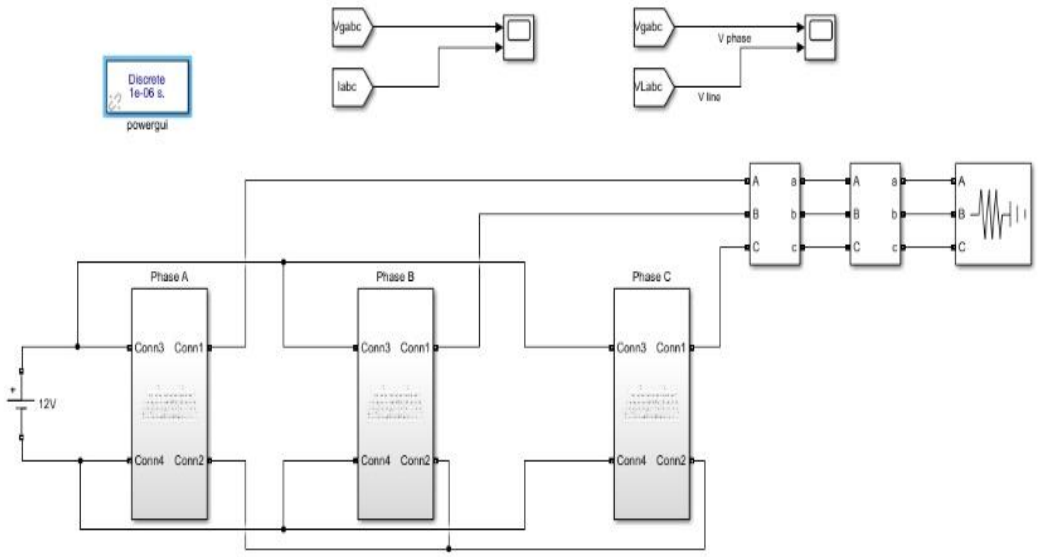

Fig. 3.27 Simulated Model for N=9 Three phase inverter

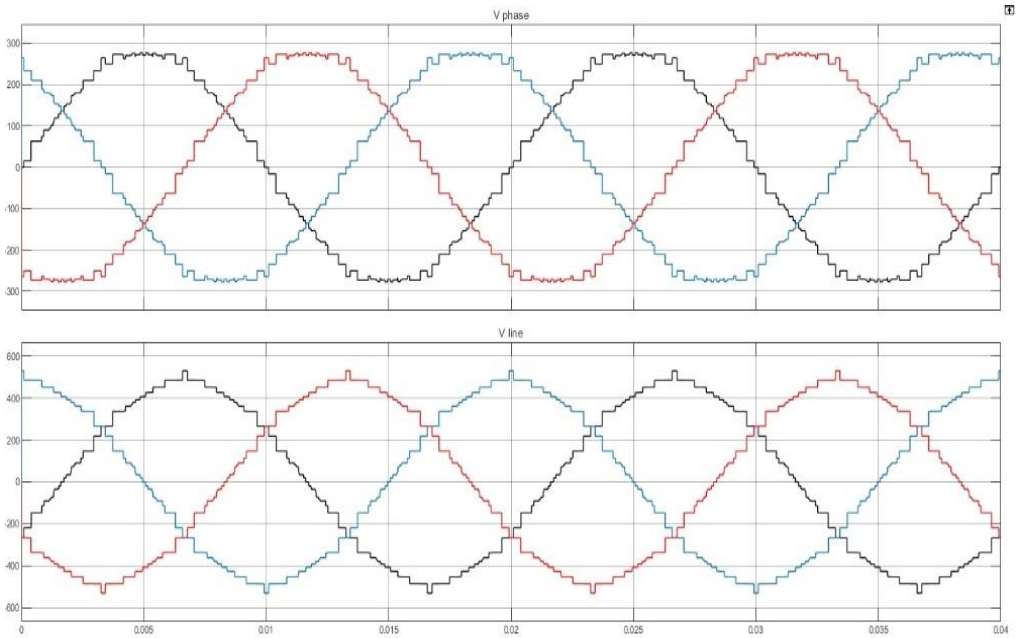

Fig. 3.28 Voltage Waveform for N=9 Three phase inverter

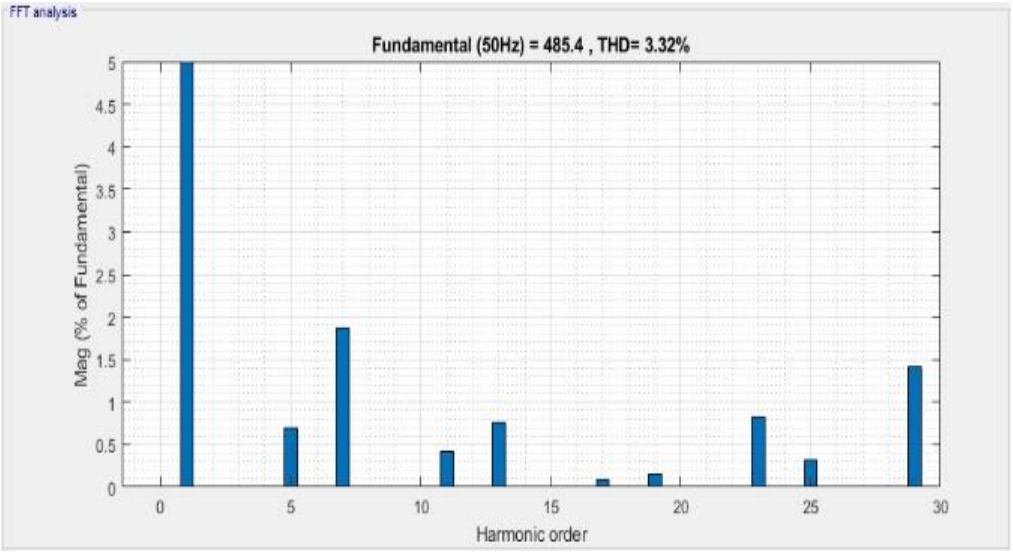

Fig. 3.29 THD in Voltage for N=9 Three phase inverter

3.5 HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

Hardware implementation of single phase inverter for N=1 as shown in fig. 3.24 & fig. 3.25.

12 V single DC supply, one 12-0-12 transformer, Five IGBTs, four power diodes, one microcontroller AtMega-328p and some basic components are used to fabricate the hardware of 5 level single phase inverter. AtMega-328p microcontroller is used to control switching time period of the IGBTs. The output AC voltage waveform is shown in Fig. 3.26 and 3.27 while the output AC current waveform is shown in Fig. 3.29. The THD in output voltage is 15.8% as shown in Fig. 3.28 while the output power THD is 2.5% of fundamental as shown in Fig. 3.30.

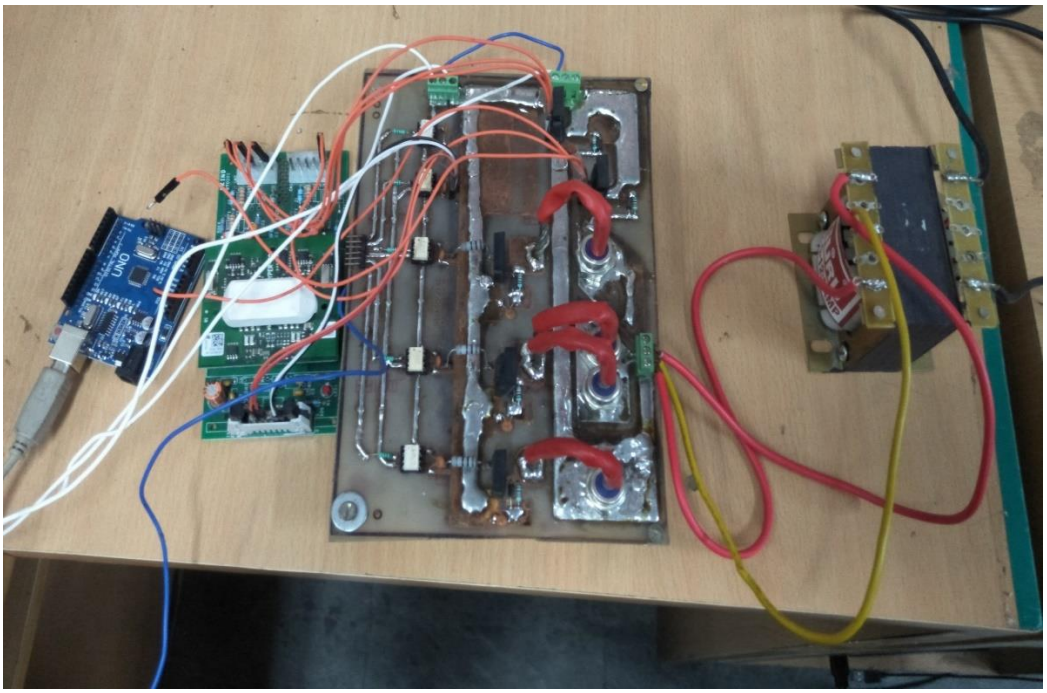

Fig. 3.30 Top View of 5 Level Single Phase Inverter

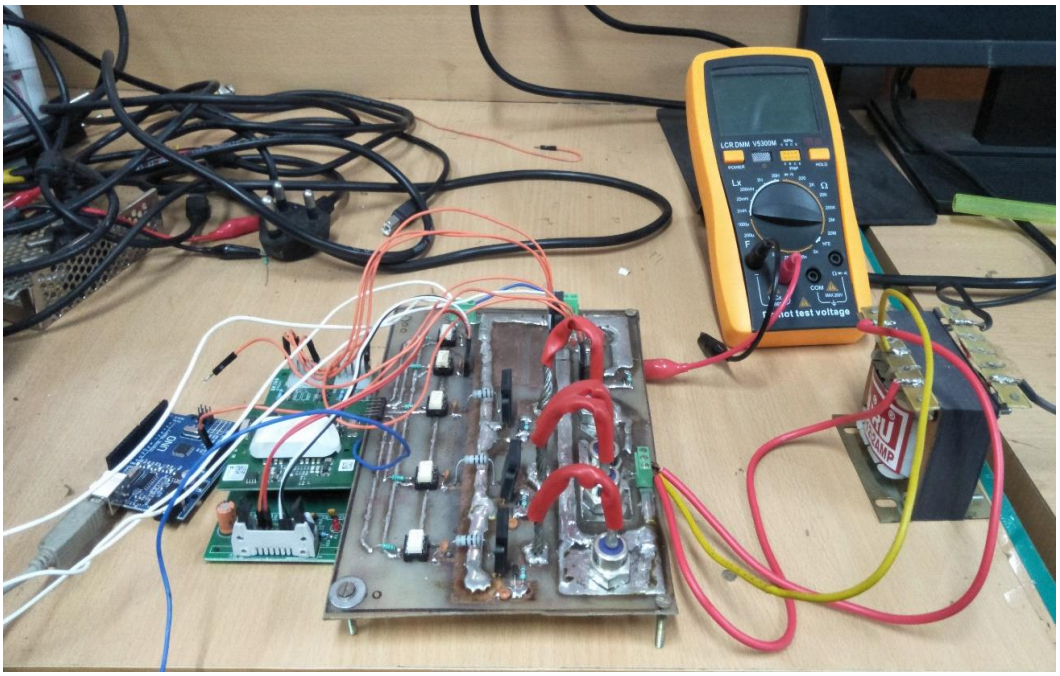

Fig. 3.31 Lateral View of 5 Level Single Phase Inverter

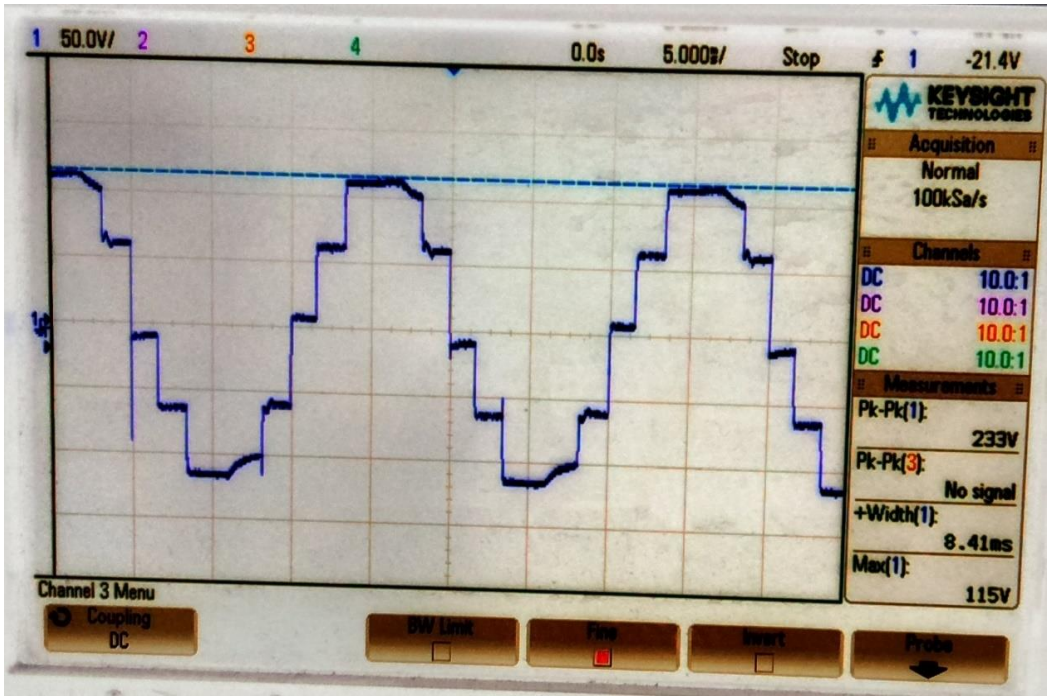

Fig. 3.32 Output Voltage Waveform in Oscilloscope

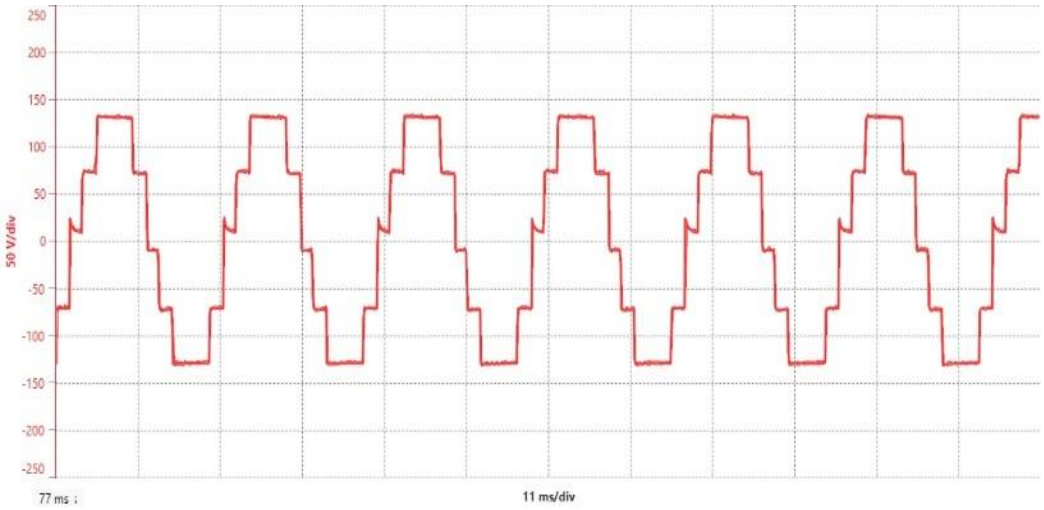

Fig. 3.33 Output Voltage Waveform in Fluke Scope meter

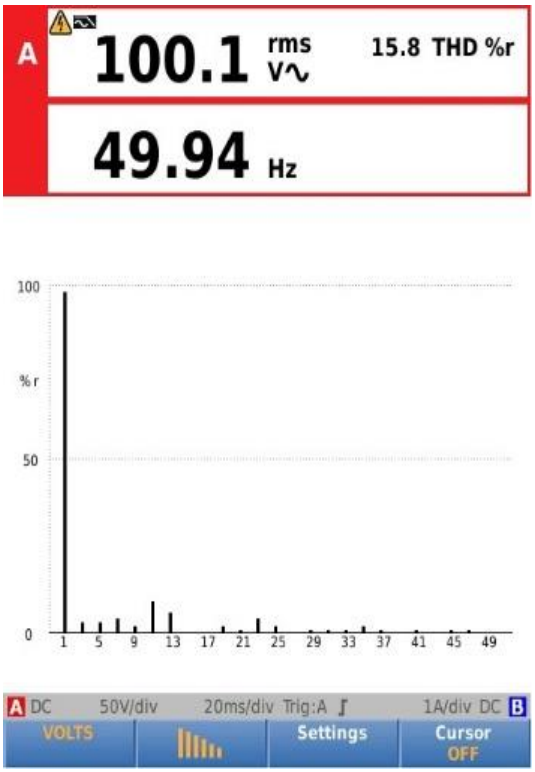

Fig. 3.34 Output Voltage THD in Fluke Scope meter

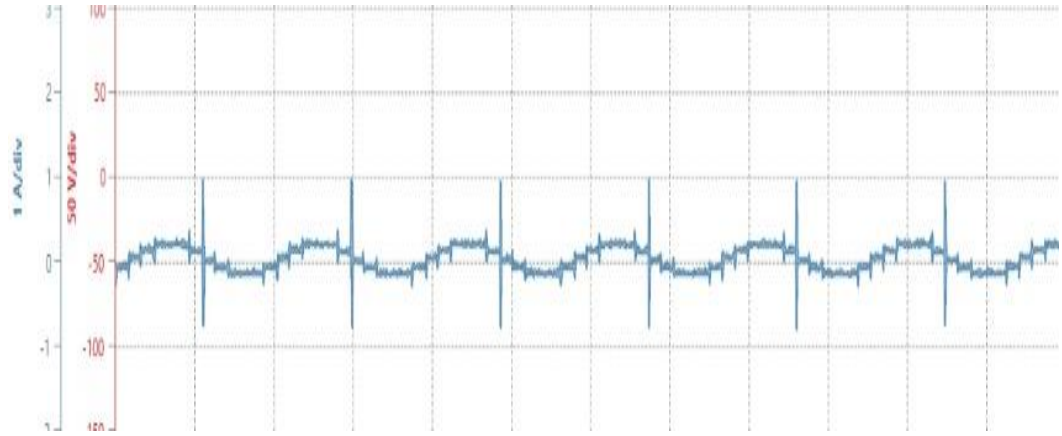

Fig. 3.35 Output Current waveform in Fluke Scope meter

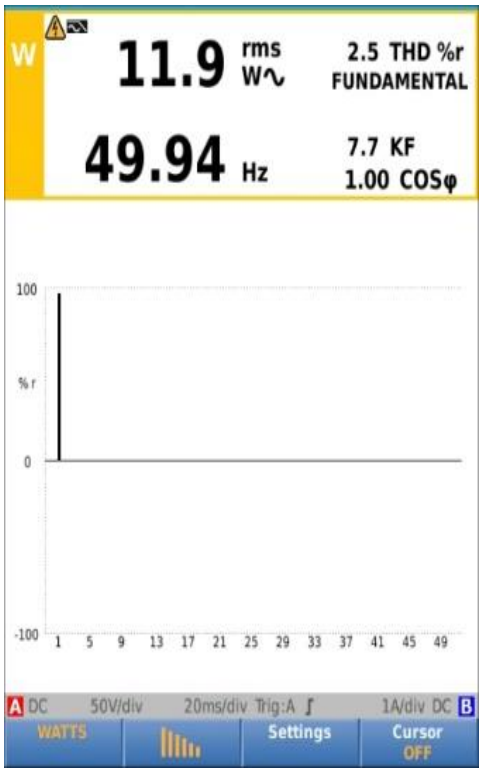

Fig. 3.36 Output power THD in Fluke Scope meter

REFRENCES

[1] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," IEEE Trans. Power Electronics, vol. 31, no. 1, pp. 135–151, Jan. 2016

[2] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-type) module: Asymmetric multilevel inverters with reduced components," IEEE Trans. Ind. Electron., vol. 63, no. 11,pp. 7148–7156, Nov. 2016.

[3] H. Akagi, "Multilevel converters: Fundamental circuits and systems," Proc. IEEE, vol. 105, no. 11, pp. 2048–2065, Nov. 2017

[4] B.K. Bose, Global energy scenario and impact of power electronics in 21st century, IEEE Trans. Ind. Electron. 60 (7) (2013) 2638-2651.

[5] E. Samadaei, A. Sheikholeslami, S.-A. Gholamian, and J. Adabi, "A square T-type (ST-type) module for asymmetrical multilevel inverters," IEEE Trans. Power Electron., vol. 33, no. 2, pp. 987–996, Feb. 2018.

[6] J. Liu, J. Wu, J. Zeng, and H. Guo, "A novel nine-level inverter employing one voltage source and reduced components as high-frequency ac power source," IEEE Trans. Power Electron., vol. 32, no. 4, pp. 2939–2947,Apr. 2017

[7] A. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," IEEE Trans. Ind. Electron., vol. 64, no. 3, pp. 2072–2080, Mar. 2017.

[8] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimization assessment of a new extended multilevel converter topology," IEEE Trans. Ind. Electron., vol. 64, no. 6, pp. 4530–4538, Jun. 2017.

[9] J.D. van Wyk, F.C. Lee, on a future for power electronics, IEEE J. Emerg. Sel. Top. Power Electron 1 (2) (2013) 59—72.

[10] M.A.J. Sathik, S.H.E.A. Aleem, R. Kannan, A.F. Zobaa, A new switched DC-Iink capacitor-based multi-level converter (SDC2MLC), Electr. Power Compon. Syst. 45 (9) (2017) 1001-1015

[11] A. Nabae, I. Takahashi, H. Akagi, A neutral-point-clamped PWM inverter, in: Conference Record IEEE IAS Annual Meeting, Cincinnati, OH, vol. 3, pp. 761—766, September 28-October 3, 1980.

[12] Y. Shi and H. Li, "Isolated modular multilevel DC–DC converter with DC fault current control capability based on current-fed dual active bridge for MVDC application," IEEE Trans. Power Electron., vol. 33, no. 3,pp. 2145–2161, Mar. 2018

[13] J.A. Barrena, L. Marroyo, M.A.R. Vidal, J.R.T Apraiz, Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM, IEEE Trans. Industrial Electron. 55 (1) (2008) 21-29.

[14] D. Thong, L.M. Tolbert, B. Ozpineci, J.N. Chiasson, Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter, IEEE Trans. Pow. Electron. 24 (1) (2009) 25-33.

[15] R. Teodorescu, F. Blaabjerg, J.K. Pedersen, E. Cengelci, P.N. Enjeti, Multilevel inverter by cascading industrial VSI, IEEE Trans. Industrial Electron. 49 (4) (2002) 832—838.
[16] M.A. Perez, P. Cortes, J. Rodriguez, Predictive control algorithm technique for multilevel asymmetric cascaded H-bridge inverters, IEEE Trans. Industrial Electron. 55 (12) (2008) 4354-4361.
[17] A.K. Gupta, A.M. Khambadkone, A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters, IEEE Trans. POW. Electron. 22 (5) (2007) 1672-1681.
[18] S. Vazquez, J.I. Leon, J.M. Carrasco, L.G. Franquelo, E. Galvan, M. Reyes, J.A. Sanchez, E. Dominguez, Analysis of the power balance in the cells of a multilevel cascaded Hbridge converter, IEEE Trans. Industrial Electron. 57 (7) (2010) 2287-2296.
[19] P. Barriuso, J. Dixon, P. Flores, L. Moran, Fault-tolerant reconfiguration system for asymmetric multilevel converters using bidirectional power switches, IEEE Trans. Industrial Electron. 56 (4) (2009) 1300-1306.
[20] Y. Li, B. Wu, A novel DC voltage detection technique in the CHB inverter-based STATCOM, IEEE Trans. Pow. Deliv. 23 (3) (2008) 1613-1619.
[21] P. Samuel, R. Gupta, D. Chandra, Grid interface of wind power with large split-winding alternator using cascaded multilevel inverter, IEEE Trans. Energy Conv. 26 (1) (2011) 299-309.
[22] M.M. Renge, H.M. Suryawanshi, Five- level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives, IEEE Trans. Pow. Electron. 23 1598—1607.
[23] J. Pereda, J. Dixon, High- frequency link: a solution for using only one DC source in asymmetric cascaded multilevel inverters, IEEE Trans. Industrial Electron. 58 (9) (2011) 3884-3892.
[24] R. Rabinovici, D. Baimel, J. Tomasik, A. Zuckerberger, Series space vector modulation for multi-level cascaded H-bridge inverters, IET Power Electron. 3 (6) (2010) 843—857.
[25] J. Kumar, B. Das, P. Agarwal, Optimized switching scheme of a cascade multi-level Inverter, Electr. POW. Compo. Sys. 38 (4) (2010) 445—464.
[26] M. Marchesoni, P. Tenca, Diode-clamped multilevel converters: a practicable way to balance DC-Iink voltages, IEEE Trans. Industrial Electron. 49 (4) (2002) 752-765.
[27] J. Kumar, P. Agarwal, Implementation of cascade multilevel inverter-based STATCOM, IETE J. Res. 56 (2) (2010) 119—128.
[28] J. Pou, R. Pindado, D. Boroyevich, Voltage-balance limits in four-level diode-clamped converters with passive front ends, IEEE Trans. Industrial Electron. 52 (l) (2005) 190-196.
[29] A. Yazdani, R. Iravani, A neutral-point clamped converter system for direct-drive variable-speed wind power unit, IEEE Trans. Energy Conv. 21 (2) (2006) 596—607.
[30] P. Zhiguo, F.Z. Peng, K.A. Corzine, V.R. Stefanovic, J.M. Leuthen, S. Gataric, Voltage balancing control of diode-clamped multilevel rectifier/inverter systems, IEEE Trans. Industrial Electron. 41 (6) (2005) 1698-1706.

[31] B.R. Andersen, L. Xu, P.J. Horton, P. Cartwright, Topologies for VSC transmission, Power Eng. J. 16 (3) (2002) 142-150.
[32] H. Akagi, T. Hatada, Voltage balancing control for a three-level diode-clamped converter in a medium-voltage transformerless hybrid active filter, IEEE Trans. POW. Electron. 24 (3) (2009) 571-579.
[33] A. Yazdani, R. Iravani, Dynamic model and control of the NPC-based back-to-back HVDC system, IEEE Trans. Pow. Deliv. 21 (1) (2006) 414-424.
[34] P. Chaturvedi, S. Jain, P. Agarwal, Carrier based neutral point potential regulator with reduced switching losses for three-level diode clamped inverter, IEEE Trans. Industrial Electron. 61 (2) (2014) 613-624.
[35] A. Bendre, S. Krstic, J. Vander Meer, G. Venkataramanan, Comparative evaluation of modulation algorithms for neutral-point-clamped converters, IEEE Trans. Industry Appl. 41 (2) (2005) 634-643.
[36] M.M. Renge, H.M. Suryawanshi, Three-dimensional space-vector modulation to reduce common-mode voltage for multilevel inverter, IEEE Trans. Industrial Electron. 57 (7) (2010) 2324-2331.
[37] N. Jayaram, P. Agarwal, S. Das, A three phase five level cascaded H-Bridge rectifier with zero current injection scheme, in: Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on, pp. 1-7, 2012.
[38] K. Xiaomin, K.A. Corzine, Y.L. Familiant, A unique fault-tolerant design for flying capacitor multilevel inverter, IEEE Trans. POW. Electron. 19 (4) (2004) 979—987.
[39] C. Feng, J. Liang, V.G. Agelidis, Modified phase-shifted PWM control for flying capacitor multilevel converters, IEEE Trans. POW. Electron. 22 (1) (2007) 178—185.
[40] P. Lezana, R. Aguilera, DE. Quevedo, Model predictive control of an asymmetric flying capacitor converter, IEEE Trans. Industrial Electron. 56 (6) (2009) 1839—1846.
[41] A. Shukla, A. Ghosh, A. Joshi, Improved multilevel hysteresis current regulation and capacitor voltage balancing schemes for flying capacitor multilevel inverter, IEEE Trans. Pow. Electron. 23 518-529.
[42] J. Huang, K.A. Corzine, Extended operation of flying capacitor multilevel inverters, IEEE Trans. Pow. Electron. 21 (1) (2006) 140-147.
[43] M. Khazraei, H. Sepahvand, K.A. Corzine, M. Ferdowsi, Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters, IEEE Trans. Industrial Electron. 59 (2) (2012) 769-778.
[44] V.G. Agelidis, D.M. Baker, W.B. Lawrance, C.V. Nayar, A multilevel PWM inverter topology for photovoltaic applications, in: Industrial Electronics, 1997. ISIE '97. Proceedings of the IEEE International Symposium on, vol.2, no., pp. 589—594, July 7—11, 1997.
[45] M.D. Manjrekar, T.A. Lipo, A hybrid multilevel inverter topology for drive applications, in: Applied Power Electronics Conference and Exposition, 1998. Thirteenth Annual, vol. 2, no., pp. 523-529, February 15-19, 1998.
[46] Y. Xiaoming, I. Barbi, Fundamentals of a new diode clamping multilevel inverter, IEEE Trans. Pow. Electron. 15 (4) (2000) 711—718. [40] F.Z. Peng,

A generalized multilevel inverter topology with self voltage balancing, IEEE Trans. Industry Appl. 37 (2) (2001) 611-618.
[47] Y. Cheng, ML. Crow, A diode-clamped multi-level inverter for the StatCom/BESS, in: Power Engineering Society Winter Meeting, 2002. IEEE, vol. 1, pp. 470—475, 2002.
[48] S. Mariethoz, A. Rufer, New configurations for the three-phase asymmetrical multilevel inverter, in: Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE, vol. 2, pp. 828—835, October 3—7, 2004.
[49] M. Veenstra, A. Rufer, Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives, IEEE Trans. Industry Appl. 41 (2) (March—April 2005) 655-664.
[50] A. Chen, L. Hu, L. Chen, Y. Deng, X. He, A multilevel converter topology with faulttolerant ability, IEEE Trans. Pow. Electron. 20 (2) (2005) 405-415.
[51] A. Chen, X. He, Research on hybrid-clamped multilevel-inverter topologies, IEEE Trans. Industrial Electron. 53 (6) (2006) 1898-1907.
[52] M.S. W. Chan, K. T. Chau, A new switched-capacitor boost-multilevel inverter using partial charging, IEEE Trans. Circuits Syst Il: Express Briefs 54 (12) (2007) 1145—1149.
[53] G. Grandi, D. Ostojic, C. Rossi, A. Lega, Control strategy for a multilevel inverter in grid-connected photovoltaic applications, in: Electrical Machines and Power Electronics, 2007. ACEMP '07. International Aegean Conference on, pp. 156—161, September 10-12, 2007.
[54] P. Lezana, J. Rodriguez, D.A. Oyarzun, Cascaded multilevel inverter with regeneration capability and reduced number of switches, IEEE Trans. Industrial Electron. 55 (3) (2008) 1059-1066.
[55] S. Daher, J. Schmid, F.L.M. Antunes, Multilevel inverter topologies for stand-alone PV systems, IEEE Trans. Industrial Electron. 55 (7) (2008) 2703-2712.
[56] R. Gonzalez, E. Gubia, J. Lopez, L. Marroyo, Transformerless single-phase multilevelbased photovoltaic inverter, IEEE Trans. Industrial Electron. 55 (7) (2008) 2694—2702.
[57] K. Wang, Y. Li, Z. Zheng, A new transformerless cascaded multilevel converter topology, in: Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE, pp. 3124-3129, September 20-24, 2009.
[58] Z. Du, B. Ozpineci, L.M. Tolbert, J.N. Chiasson, DC—AC cascaded H- bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications, IEEE Trans. Industry Appl. 45 963-970.
[59] J. Ewanchuk, J. Salmon, A.M. Knight, Performance of a high-speed motor drive system using a novel multilevel inverter topology, IEEE Trans. Industry Appl. 45 (5) (2009) 1706—1714.
[60] Y. Liu, EL. Luo, Multilevel inverter with the ability of self-voltage balancing, Electr. Pow. Appl. IEE Proc. 153 (1) (2006) 105—115.
[61] S. De, D. Banerjee, K. Siva Kumar, K. Gopakumar, R. Ramchand, C. Patel, Multilevel inverters for low-power application, IET POW. Electr. 4 (4) (2011) 384—392.
[62] C.-C. Hua, C.-W. Wu, C.-W. Chuang, A novel DC voltage charge balance control for cascaded inverters, IET Pow. Electr. 2 (2) (2009) 147—155.

[63] A.R. Beig, A. Dekka, Experimental verification of multilevel inverter-based standalone power supply for low-voltage and low-power applications, IET POW. Electr. 5 (6) (2012) 635-643.
[64] S. Gui-Jia, Multilevel DC-Iink inverter, IEEE Trans. Industry Appl. 41 (3) (2005) 848-854.
[65] S. Gui-Jia, Multilevel DC link inverter, in: Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE, vol. 2, pp. 806—812, October 3-7, 2004
[66] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, M.I. Gimenez, A new simplified multilevel inverter topology for DC-AC conversion, IEEE Trans. POW. Electron. 21 (5) (2006) 1311-1319.
[67] N.A. Rahim, K. Chaniago, J. Selvaraj, Single-phase seven-level grid-connected inverter for photovoltaic system, IEEE Trans. Industrial Electron. 58 (6) (2011) 2435—2444.
[68] G.M. Martins, J.A. Pomilio, S. Buso, G. Spiazzi, Three-phase low-frequency commutation inverter for renewable energy systems, IEEE Trans. Industrial Electron. 53 (5) (2006) 1522—1528.
[69] Y. Hinago, H. Koizumi, A single phase multilevel inverter using switched series/parallel DC voltage sources, in: Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE, pp. 1962-1967, September 20-24, 2009.
[70] Y. Hinago, H. Koizumi, A single-phase multilevel inverter using switched series/parallel DC voltage sources, IEEE Trans. Industrial Electron. 57 (8) (2010) 2643—2650