LOW POWER MULTI-VALUED AIRTHMETIC LOGICAL UNIT DESIGN USING CNFETS

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ABSTRACT

Binary logic and MOS devices have been in use since inception of the design era, but now due to advancement in VLSI industry binary logic has become tedious and complicated. To overcome this challenge Multi-valued logic (MVL) such as ternary and Quaternary Logic (QTL) can be used .MVL designs has an advantage over binary logic deigns with respect to area and interconnects complexity. In this report, we present the design and performance of QTL Full Adder (QFA), Quaternary Multiplier (QM) and QTL Arithmetic and Logical Unit (QTL ALU) using CNFET. For design purpose we have used the Stanford Virtual-Source Carbon Nanotube Field Effect Transistor Model version 1.01 with sub 10nm CNFET technology. The design tool used for simulation is Cadence Virtuoso. This work presents novel multiplexer based approach to design QFA, QM and QTL ALU using CNFET. The proposed QTL ALU design has been compared against the existing CNFET based QTL designs and it is found that proposed ALU design is 90–99% better in terms of power, delay, PDP and EDP.

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LIST OF SYMBOLS

V_{th}	Threshold Voltage
V_{sat}	Saturation Velocity
Ch	Chiral Vector
T	Tube axis
n, m	Chirality parameter
a_1,a_2	CNT vectors
d	CNT diameter
a	bond length between two carbon atoms
φ	Chiral angle
E_x	Transverse electric field
E_y	Longitudinal electric field
D	Range
n	number of digits
R	Radix
k	Constatnt
C	Complexity
E_g	Band gap energy
e	Unit electron charge
ε_0	Permitivity
V_{dd}	Power supply voltage
Tp	PCNFET
Tn	NCNFET

V	Volt
s	second
µm	micrometer
nm	nanometer
Å	Angstrom
~	approximately
S	Source
D	Drain
G	Gate
pF	picofarad
fF	femtofarad
eV	electronvolt
t	Time
Js	Joule sec
C_{load}	Load capacitor

LIST OF ABBREVIATIONS

CMOS	Complementary metal–oxide–semiconductor
VLSI	Very Large Scale Integration
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CNFET	Carbon Nanotube Field Effect Transistor
ITRS	International Technology Roadmap for Semiconductor
SCE	Short Channel Effect
DIBL	Drain Induced Barrier Lowering
TFET	Tunnel Field Effect Transistor
DGFET	Double Gate Field-Effect Transistor
FinFET	Fin Field Effect Effect Transistor
SWCNT	Single Wall Carbon Nano Tube
MWCNT	Multi-Wall Carbon Nano Tube
CNT	Carbon Nanotube
FET	Field Effect Transistor
SB-CNFET	Schottky Barrier CNTFET
PG-CNFET	Partially Gates CNTFET
S/D	Source/Drain
C-CNFET	Conventional CNFET
MVL	Multi-Valued Logic
ALU	Arithmetic Logic Unit
QTL	Quaternary Logic
QNAND	Quaternary NAND
QNOR	Quaternary NOR

mux	Multiplexer
EDP	Energy Delay Product
PDP	Power Delay Product
ITRS	International Technology Roadmap for Semiconductor
et.al	and others
I-V	Current Voltage
C-V	Capacitor Voltage
VS-CNTFET	Virtual Source CNTFET
TNOR	Ternary NOR
TNAND	Ternary NAND
W/L	Width/Length
IC	Integrated Circuit
SB	Schottky Barrier
CNFET_L1	CNFET level 1
CNFET_L2	CNFET level 2
CNFET_L3	CNFET level 3
w.r.t.	With respect to
NCNFET	N type CNFET
PCNFET	P type CNFET
NQI	Negative Quaternary Inverter
IQI	Intermediate Quaternary Inverter
PQI	Positive Quaternary Inverter
SyQI	Symmetrical Quaternary Inverter
QFA	Quaternary full adder
QM	Quaternary Multiplier
APC	Average Power Consumption
PD	Propagation Delay

CHAPTER 1

Introduction

Over the last few decades, silicon has been the building block for the electronics industry and with 0.35μm node, the MOSFET gate length has entered into the submicron region. From 2006, the 65nm technology became mainstream, and around 2007, 45nm technology node has also been reported. As MOSFET continues to extend into the nanoscale regime, various problems have been introduced which affect parameters like gate-oxide, threshold voltage (V_{th}) and saturation velocity (V_{sat}). Due to this Short Channel Effects (SCE) like hot electron effect, minimization of Drain Induced Barrier Lowering (DIBL), impact-ionization and surface scattering are introduced. The ITRS [1] projected that SCE increases as technology advances. Therefore, the necessity of new devices such as Double Gate Field-Effect Transistors (DGFET), Fin Field Effect Transistor (FinFET), Tunnel Field-Effect Transistor (TFET) and Carbon Nanotube Field-Effect Transistors (CNFET) arises [2].

1.1 Carbon Nanotube Field-Effect Transistors

Over the last decade, CNFET devices have shown a tremendous amount of improvement in the nanoscale regime. CNFET devices are capable of avoiding most of the limitations of traditional silicon devices like MOSFETs. These devices are fabricated using graphene layers curled into cylindrical form in which the carbon atoms are bonded in such a manner that each and every atom is associated with other atoms in sp^2 hybridization. It ensures that on a stationary atom there is no unsatisfied valency. This characteristic permits the integration of these devices with high-K dielectric materials. The next section summarizes the basic properties of CNFET.

The CNFET has many potential advancements over the traditional MOSFET devices in terms of intrinsic attributes and its unequalled one-dimensional band structure. Which prevents backscattering and also provides the near ballistic operation [4]. Overall we can conclude that the CNFET is the most promising device in the field of nanotechnology. CNFET device offers faster operation with low power consumption in contradiction to MOSFET technology and is more satisfactory for low-voltage and high-frequency operations. Further, Unlike MOSFET devices (p-type and n-type) that have different size and mobility which results in different current driving capabilities, CNFET devices (p-type and n-type) have the same size and mobility which results in same current driving capabilities.

1.1.1 Carbon Nanotube

Carbon Nanotube (CNT) is used as the semiconducting channel in CNFET device. CNT is hexagonally organized carbon atom sheet to form a graphene layer that is shaped into a tube-like structure with a diameter of few nanometers, this structure is well known as honeycomb structure [3]. In 1991, S. Iijima first perceived that the CNT establishes a macromolecule class that has distinct mechanical, electrical and thermal properties. Few of these properties are the result of the close relationship between carbon nanotube and graphite structure as they both comprise of hexagonal layout and some properties are due to its one-dimensional structure. The lattice of graphene that is shaped in the tube is shown in Figure 1.1.

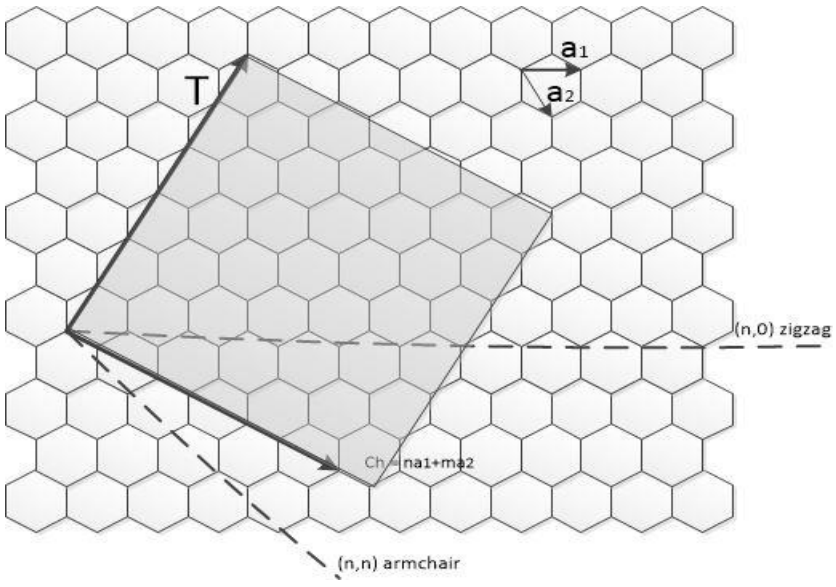


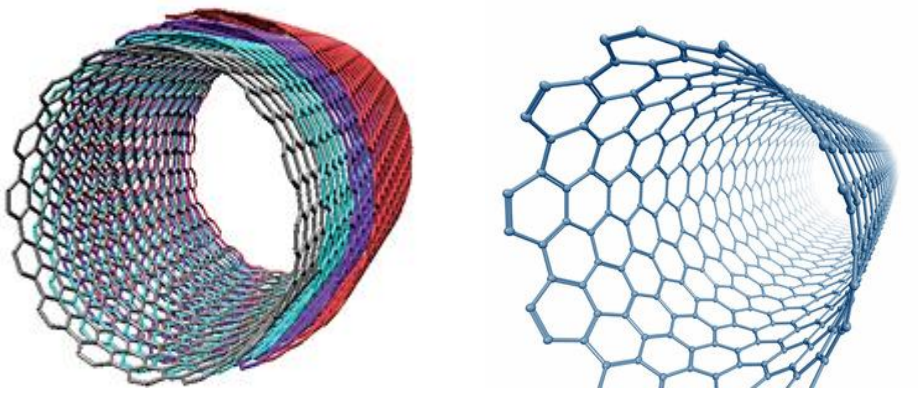
Figure 1.1: Graphene Lattice [3]

Figure 1.1 presents the lattice of the graphene sheet, where carbon atoms are located at each corner of hexagon and sides of hexagon represent the chemical bonds with sp^2 –orbitals. Where *Ch* and *T* represent chiral vector and Tube axis respectively [4]. Chirality vector *Ch* is given as the vector vertical to carbon Nano-tube axis *T*. Equation 1.1 gives the mathematical formula for *Ch*, where pair of integers are given by *n* and *m*, and the lattice vectors $\overline{a_1}$ and $\overline{a_2}$ are given in equation 1.2, where inter-atomic distance between adjacent carbon atoms is given by $a_0 = 1.42$ *Å*.

$$C_h = n\overline{a_1} + m\overline{a_2} \tag{1.1}$$

$$\overline{a_1} = \left(\frac{\sqrt{3}}{2}a_0 , \frac{3a_0}{2}\right) \quad \overline{a_2} = \left(-\frac{\sqrt{3}}{2}a_0 , \frac{3a_0}{2}\right) \tag{1.2}$$

CNT is characterized in two categories based on the number of the cylinders presents as Single Wall Carbon Nanotube (SWCNT) with more than one cylinder and Multi-Wall Carbon Nanotube (MWCNT) which comprises of multiple SWCNT nested inside one another, Figure 1.2 depicts the same[4].



(a) (b)

Figure 1.2: Structure of (a) MWCNT and (b) SWCNT [4]

CNT can behave either as semiconductor or metallic material depending upon C_h. For metallic behaviour integer *n* and *m* must be equal $(n = m)$ or the difference of n and m is equivalent to three times of any positive integer $(n - m = 3i)$ $(i \in N)$ and behaves as semiconductor property for all other conditions. The diameter of the CNT is another important parameter which can be given as:

$$d = \left|\frac{C_h}{\pi}\right| = \frac{a_0}{\pi}\sqrt{n^2 + m^2 + nm} \tag{1.3}$$

CNTs can also be specified in further two categories based on the geometry of carbon bond and the value of *n*, *m*, and φ as:

i. Armchair type for which *n* and *m* must be equal ($n = m$) and chiral angle must be zero ($\varphi = 0^o$)
ii. Zig-Zag type for which integer *m* must be zero ($m = 0$)and have a chiral angle of 30^o ($\varphi = 30^o$)
iii. For chiral angle ranging from 0^o to 30^o ($0^o < \varphi < 30^o$) CNT is known as chiral.

1.1.2 CNFETs

CNT is used to form CNFET which is analogous to MOSFET structure [4] and its operations are also very much similar to the traditional MOSFET. Like MOSFET, CNFET is also a four-terminal device in which the CNT behaves as a channel extending from source to the drain terminal.

CNFET can also be characterized in three categories based on its structure and the materials used for source and drain. The classification is as follows:

i. Schottky-Barrier CNFET (SB-CNFET)
ii. Partially-Gated CNFET (PG-CNFET)
iii. MOS-like CNFET (also known as doped S/D CNFET or C-CNFET)

Figure 1.3(a) shows the SB-CNFET in which the channel used is CNT and source and drain are metallic. It facilitates the direct tunnelling of the current through the source-channel junction (Schottky-barrier). The Schottky barrier across the source-channel junction can be controlled by the difference in the work function of metal and the CNT [5]. The gate voltage is used to control the barrier width and it further controls the transconductance of the device. At low gate potential, the barrier width is wide due to which small current flows through the device. As we increase the gate potential of SB-CNFET, the barrier width decreases which reduces the transconductance causing the increase in current flow. The main disadvantage of this device is that while manufacturing we must be very careful about the alignment of Schottky barrier and gate electrode [6]. Figure 1.3(b) shows the PG-CNFET in which we uniformly dope the CNT and connect ohmic contacts to create the source and drain. These devices can be of either n-type or p-type based on the doping profile of CNT at the source and drain. The fundamental

working of these devices is based on the phenomenon of charge carrier depletion in CNT channel through the gate, making it p-type (n-type) device with positive (negative) threshold voltage [7]. Another type of CNFET is given in Figure 1.3(c) known as C-CNFET or MOS-like CNFET. As the name suggests the structure of this type of CNFET is similar to MOSFET. In this type of CNFET source and drain terminals are heavily doped semiconductors of either p-type or n-type. Due to the similarity to conventional device this type of device is also known as conventional CNFET (C-CNFET). When the positive voltage ($V_{ds} > 0$) is applied across the device constant current will flow through CNT due to ballistic effect [10]. C-CNFET is preferred over SB-CNFET due to the following reasons [8][9].

i. C-CNFET operates faster due to its unipolar nature.
ii. Low leakage (off-state) current, due to the absence of schottky barrier junction.
iii. Significantly higher ON-state current.

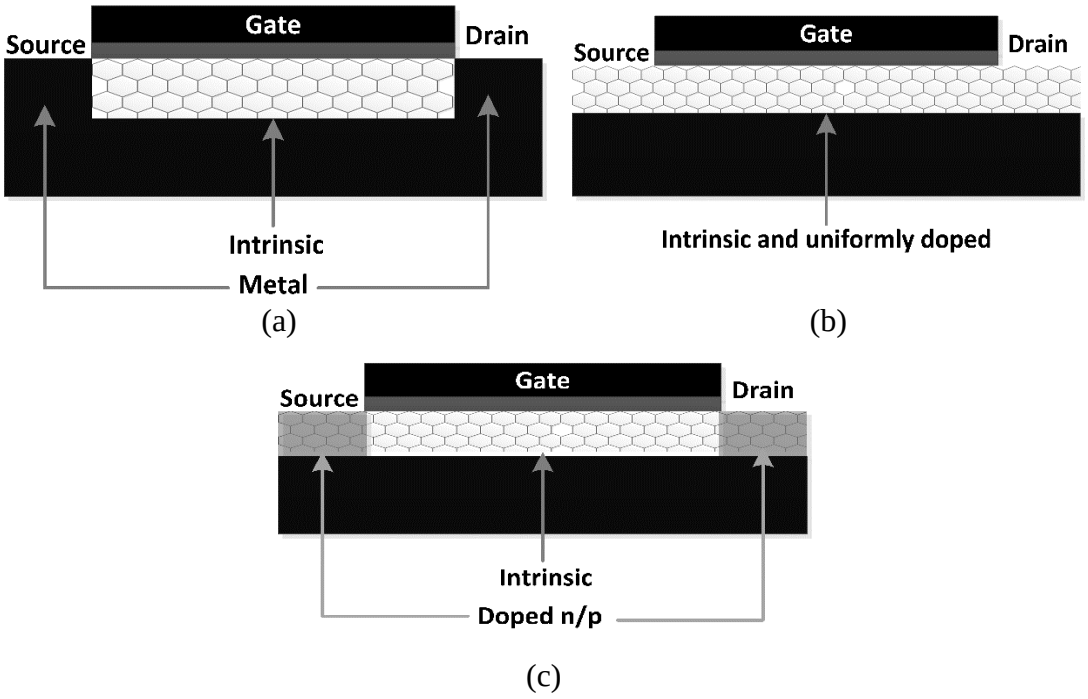


Figure 1.3: CNFET Structures (a) SB-CNFET, (b) PG-CNFET and (c) doped S/D CNFET

1.2 Overview to Multi-Valued Logic

Another complexity arises due to scaling down of the technology as it results in an increase in the number of interconnections. As the technology node decreases the number of transistors increase, which causes the problem in routing of interconnects over the chip [11].

The problem can be solved if we use the multi-valued logic (MVL) instead of binary logic. Using MVL reduces the chip area by reducing the interconnections and functional units in the VLSI design. In MVL the basic principle is to send a large amount of data over a single wire, for example, we need two wires to transmit the binary logic *(00, 01, 10, 11)* whereas in MVL *(0,1,2,3)* we can transmit it over a single wire thus reducing the interconnection complexity. Other than interconnection complexity, usage of MVL also reduces the interconnection delay, dynamic power dissipation and crosstalk [12]. Some advantages of MVL over binary logic are listed below:

i. Reduction in chip area: MVL can transmit more information over the same number of wire as compared to the binary logic.
ii. Complexity of the circuit: Usage of MVL over binary logic will reduce the number of interconnections thus reducing the complexity of the circuit.
iii. Increase in serial transmission speed: Transmitted information per unit time increases.
iv. Less Computational Stages: More than two logic levels are now used to perform a logical and arithmetic operation.

There are several advantages of MVL, but implementing MVL is still a complicated issue because of low noise margin and as we scale down the technology noise margin further reduces. Therefore, we need a technology other than conventional MOSFET through which we can implement MVL more effectively in terms of power dissipation, delay, and noise margin.

1.3 Problem Statement

Over the last few decades, gradual advancement in the VLSI industry has lead to the operations in the nanoscale regime and further reduction in the technology node of conventional FET devices is not possible. Therefore, we need new technologies like FinFET, CNFET, DGFET, TFET among several others [2]. Along with new technologies we also need to develop the new logics like MVL in order to keep up with Moore's law. In MVL we can implement the same logic with less area and less complexity in comparison to the conventional binary logic. The aim of this thesis is to analyse and develop an effective way to reduce the complexity, area and power dissipation of arithmetic and logical unit (ALU) using CNFET with the help of MVL.

1.4 Organization of work

The thesis is divided into 5 chapters. Each chapter is further divided into subparts starting with a brief introduction of the topic covered in chapter followed by the objective and work done. At last the conclusion or brief summary about the chapter is presented. The chapters covered are listed as follows:

Chapter 1: Introduction: Presents the brief overview to CNFET and MVL followed by the discussion about current problems in the VLSI domain. At last, we discuss the organization of the thesis.

Chapter 2: Literature Review: Presents the past work done in the field of Nano-electronics (CNFET) and MVL. Later in this chapter, we also discuss the motivation behind the proposed work followed by a summary of the chapter.

Chapter 3: Overview to QTL and CNFET technology: Chapter starts with a discussion about the need for new technology like CNFET and its merits over traditional FET devices. Later in the chapter, setup and simulation for CNFET are discussed including model hierarchy, model parameter range, and default parameter set. In the later section, the basic setup for MVL, in our case QTL, including CNFET diameter is discussed. At last, basic QTL gates like inverters, QNAND and QNOR are implemented and verified through their transient response.

Chapter 4: Proposed QTL Arithmetic logic unit: In this chapter, we present the proposed design block for ALU. The QTL logic design has been used to implement the following basic circuits:

i. 4:1 multiplexer (mux)
ii. 2:1 mux
iii. incrementor and decrementor circuits

Later these blocks are used to implement QTL full adder, QTL multiplier and at last QTL ALU.

Chapter 5: Metric performance Analysis: Chapter presents the Performance analysis of proposed design based on their Average power consumption, propagation delay, PDP and EDP for two load conditions. This Chapter also contains a comparison of the proposed work with the existing technology.

Chapter 6: Conclusion and Future Scope: This chapter gives the findings of the work done and its advantages over the existing technologies in terms of power consumption, propagation delay, PDP and EDP. It also discusses the applications and areas in which this technology can be utilized in the near future.

CHAPTER 2

Literature Review

2.1 Introduction

Over the past few decades, CNFET and MVL have become a hot topic for low power, high speed, and area-efficient circuits. The CNFET devices have great potential in the VLSI industry due to its distinguished characteristics such as its unique 1-D band structure, high-speed ballistic transport technique and low subthreshold (OFF-state) current. MVL, on the other hand, is capable of attaining operating speed twice as fast as possible for the existing binary logic designs along with the lower power-delay product. Therefore, the combination of CNFET and MVL makes it an interesting field to explore.

This chapter is categorized into four sections, including current introductory section 2.1. Section 2.2 compiles the work that has already been carried out in the field of CNFET and MVL. The motivation behind the proposed work is discussed in section 2.3. The summary of the chapter is given in section 2.4.

2.2 Background

In 1991, S. Iijima was the first to synthesize the C60 and other fullerenes molecular structure and simulate the graphene sheets through theses structure. Later, he also obtained the electron diffraction pattern for the graphene tubes in which the carbon atoms are arranged in the helical pattern [3]. By using this concept in 1998 Tang et al. demonstrated CNFET switching behavior and succeeded in modulating the conductivity of CNFET device by more than 5 times than that of traditional devices by applying the electrical field to the CNT [23]. Forro et al. later introduced the CNFET device which

showed a reduction in the gate threshold while increasing its transconductance significantly. It was achieved by introducing the Al_2O_3 layer on top of the patterned Al gate [25]. Later in 2003 Avouri et al. developed the top gated CNFET using both SWCNT and MWCNT. He also demonstrated the potential of CNFET device by fabricating the CMOS-like voltage inverter and also verified its electrical properties [24]. This concept was further carried out by Choi et al. in 2004 by developing the latest vertical CNFET device in which source and drain were arranged on top of each other which allowed it to have higher packing density [26].

In 2002 Schottky barrier CNFET devices were introduced by Heinze et al. which work on the principle of direct tunneling through the source and drain junctions decreasing the leakage current and hence increasing the performance of these devices [5]. The scaling issues were investigated by Jing Guo et al. in 2004 which included the important properties of CNFET device known as ambipolar conduction using atomic scale and self-consistent simulations [6]. Later in 2004, A. Raychowdhury et al. developed a ballistic compact model of CNFET compatible with SPICE and also efficiently obtained I-V and C-V characteristics [18]. C. Dwyer et al. further developed this SPICE model in the same year to evaluate the potential of CNFET device w.r.t. switching time and energy-delay product for inverter, NAND, FA and SR-Latch circuit [17]. T. Dang et al. in 2006 demonstrated the CNFET basic characteristics by simulation of different models. He also explained the significance of CNT diameter in controlling CNFET current and threshold voltage [7].

R. Marani et al. in 2011 carried out the quantum mechanical simulations by varying the CNT diameter and oxide junction capacitance of the CNFET device. The model used analytical approximations to perform the simulations [10]. The model presented by R. Marani et al. had a limited range of chirality and diameter. This issue was addressed by J. Deng et al. in 2007 by developing the compact model for CNFET device. The model had a wide range of chirality and diameter which included non-idealities as well as multiple CNTs. The model also described the improvement in CNFET device over traditional MOS device [19]. In 2007 A. Hazeghi et al. discussed other limiting parameters of CNFET devices i.e., tunneling current due to band-to-band conduction and ambipolar conduction. He developed spice and Verilog-A SB-CNFET models at Stanford University to treat the above limitations. This model was further enhanced by C. S. Lee et al. in (2013) by presenting the latest VS-CNFET model. In this model different parasitic

effects were modeled and more calibrated metal to CNT contact resistances were presented. This model also included fringe capacitance and coupling capacitance.

The concept of MVL was first introduced by Lukasiewicz in 1920 by developing the first three-valued propositional calculus using non-classical logical calculus [29]. Later in 1930 Tarski et al. published another paper describing Lukasiewicz's n-valued systems of propositional calculi [29]. In 1965 Miller et al. developed the algebra and computation theory for three value system and published a book "Switching Theory, Vol. 1" [30]. Yoeli et al. further developed this logic design based on three value system called ternary switching automata. He used two algebraic methods and a map method to simplify and implement ternary functions using diodes and triodes [31]. Later Review of MVL is presented by Epstein et al. in 1974 and its application in modern VLSI industry with area-efficient implementation is presented in [32]. The concept of ternary logic was further developed by Mukaidono et al. in 1986 by introducing a special ternary function group called regular ternary logic functions. These functions are used in many fields of electronics and computers such as switching theory, the theory of algorithm and many programming languages [33].

First MOS based ternary logic circuit for TNOR, TNAND, and ternary inverter was presented by Balla et al. in 1984 and was used to implement ternary memory and ternary arithmetic circuits. For reducing the interconnection and development of area-efficient design, Mou et al. in 1986 presented a new improved clocking scheme for scan design based on ternary algebra called ternary clocking scheme [35]. Seger et al. in 1988 proposed a method to detect and solve timing problems including critical races and hazards in the digital circuit. Later in 1988 Wang et al. proposed a new scheme to attain low power dissipation and high-speed goal for ternary logic designs known as dynamic ternary logic. These designs are capable of attaining operating speed twice as fast as possible for previous design with the low power-delay product. The proposed approach used Yoeli-Rosenfield algebra to implement logic circuits [36]. Srivastava et al. in 2000 developed a new scheme to implement ternary inverter by simply adjusting the W/L of MOS devices and using transmission gate at the output. The proposed designs used back gate bias as an additional parameter for designing of CMOS ternary logic circuit [37].

A software named ELOmv was developed by Nascimento et al. in (2001) for analysis and design of MVL circuits capable of predicting ternary and quaternary truth tables. ELOmv is used in future work to implement the MVL using CNFET [38]. A novel

method for implementation of MVL using CNFET was presented by Ray chowdhary et al. in 2005 and simulated using HSPICE to obtain DC characteristics [39]. In 2011, Sheng et al. presented a new technique to implement ternary logic using CNFET. In this approach, a conventional binary logic approach is used in conjunction with ternary logic to attain 90% better power delay product than the previous technique [40]. Later Vudadha et al. in 2012 proposed a novel approach to design ternary logic using a multiplexer to attain low power and high speed as compared to previous designs. He also developed a 1-bit comparator and half adder to show the significant improvement in terms of delay and power. Later, Roosta et al. in 2019 developed a novel design of quaternary 4:1 and 2:1 multiplexer with CNFET. The proposed approach showed approximately 68% improvement in terms of PDP.

2.4 Motivation

The work presented in the report is based on MVL using CNFET. Many novel designs are proposed throughout the literature as discussed in the previous section. As concluded from the previous section CNFET is the best option to implement MVL logic due to its properties like the flexibility to vary threshold voltage based on CNT diameter and lower channel length. We also observed that there is a need for new logics like MVL which can help us attain low power dissipation and less delay in logic circuits. So, we have implemented QTL full adder, QTL multiplier and QTL ALU circuit to verify the above properties.

2.6 Summary

In this chapter, we have discussed several approaches that has been presented in the last few decades focusing on the development of CNFET devices and their applications. Later, the advancement in MVL and techniques that has been developed to implement the MVL logic using diode, triode, CMOS and CNFET are discussed.

CHAPTER 3

Overview of Quaternary Logic and CNFET Technology

3.1 Introduction

VLSI industry has been on the boom since 1965 satisfying Moore's law. The demand for high speed and low power circuits has led to the introduction of beyond CMOS devices and alternative logics like reversible logic [13] and multi-valued logic. Over several decades, research has been done in this field and several techniques have been introduced by combining the beyond CMOS and the alternative logic. One of the alternatives can be to combine CNFET (technology) and Quaternary Logic (logic).

This chapter comprises the brief introduction to CNFET and QTL and is divided into five sections including the present introduction section 3.1. Thereafter, section 3.2 focuses on the objective of the chapter. In section 3.3 we discussed the need for CNFET technology. Overview of CNFET and its parameters is given in Section 3.4. Then Section 3.5 summarizes the brief introduction of QTL logic and basic QTL gates implementation. At last brief summary given in section 3.6.

3.2 Objective

The primary objective of the chapter is summarized as follows:

1. Study of Effect of Scaling of Traditional silicon technology
2. A brief study of CNFET and its performance analysis.
3. Brief Study of Quaternary Logic
4. Simulation and setup of quaternary logic Gates using Cadence Virtuoso.

3.3 Scaling of traditional silicon technology

In chapter 1 we studied about the future potential of CNFET technology but before moving further to the new technology CNFET, we must study the need for advancement. In this section, we study the effect of scaling in MOSFETs. There are several methods for scaling, initially in 1974 scaling of IC design process rules were introduced by Robert Dennard [14]. In this type of scaling, for each new generation of logic devices circuit density has approximately doubled and performance has increased by more than 40%.

3.3.2 Limitation of Scaling

In traditional silicon MOSFET devices, scaling down in nanoscale regime presents many scaling limitations. Some of these effects are illustrated below:

3.3.2.1 Short Channel Effect

During scaling as channel length is reduced, several leakage currents are introduced which are classified as Short Channel Effects (SCE). Effects of decreasing the channel length are as follows:

i. As channel length becomes comparable to source and drain width, the potential distribution across the channel depends on the transverse and longitudinal field given as E_x and E_y.
ii. Due to dependence on E_x and E_y, the mobility of the device degrades w.r.t effective electric field.
iii. Some electrons are introduced into the channel before strong inversion is achieved, due to which a current flows through the device called subthreshold current.
iv. As channel length decreases, source and drain also contribute to charge accumulation in the depletion layer, which causes the threshold voltage to decrease. This phenomenon is known as the charge sharing effect.
v. The short channel also introduces DIBL which occurs due to charge sharing effect. In DIBL when the drain depletion region continues to increase it reaches source-channel junction causing a reduction in junction barrier. This contributes

to the decrease of gate terminal controllability causing the device to deviate from ideal characteristics.

vi. Small geometry causes the electric field to increase, which leads to the injection of the electron in the oxide layer known as the hot-electron effect.

Leakage currents introduced due to SCE are shown in figure 3.1. Here reverse-bias leakage current due to p-n junction formed is denoted by I_1. Weak inversion current I_2 and I_3 is the current due to DIBL. Current through gate-induced drain leakage is given by I_4, current introduced due to punch-through is denoted by I_5, current due to narrow-width effect is represented by I_6, gate oxide tunnelling current is denoted by I_7, and hot carrier injection current is represented by I_8 [15].

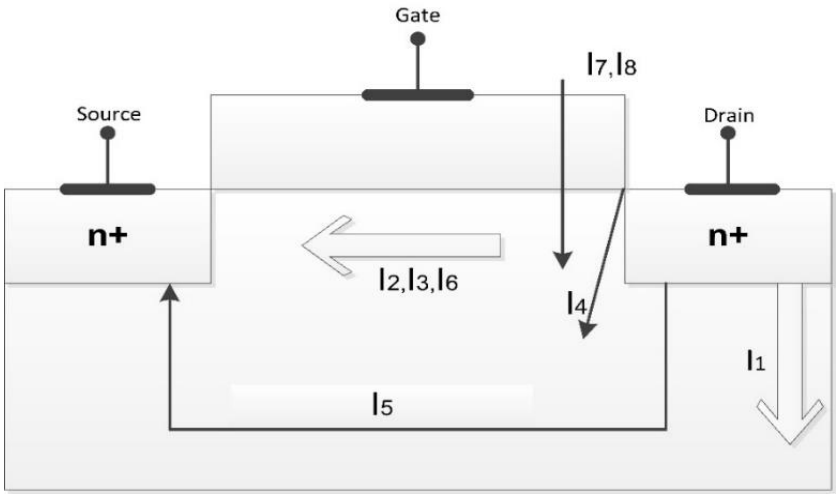


Fig 3.1. SCE leakage currents

3.3.2.2 Oxide Thickness

In MOSFET, we try to maintain the oxide as thick as possible w.r.t. the channel length in order to employ effective channel control. This condition also ensures avoidance of SCE. Based on the sizing of Gate Oxide thickness two drawbacks arise:

i. Leakage current due to quantum effect tunneling in MOSFET. For thin oxide layer, the leakage current is high but as we increase the oxide thickness this current become negligible as compared to the “on state” current.

ii. Inversion charge loss occurs due to the thick oxide layer.

For last several decades, polysilicon is considered as an effective gate oxide material, but as we move forward with scaling substantial challenges such as increase in

resistivity and polysilicon depletion effect are introduced. Therefore, the need for new advancement arises such as increasing doping of polysilicon to decrease the resistivity of gate electrode and to avoid polysilicon depletion effects. However, this methodology is subject to dopant solubility [16].

3.3.2.3 Threshold Voltage

Another limitation of scaling MOSFET is a nonlinear variation of threshold voltage w.r.t transistor scaling. For MOSFET devices, with channel length between 0.1µm-1µm, the threshold voltage is almost constant but for channel length below 0.1µm, it shows exponential decay and inverse proportionality w.r.t thermal energy. The decrease in threshold voltage also causes an increase in subthreshold (off state) current.

3.4 CNFET Overview

The fundamental operation of CNFET is similar to MOSFET, as the current originates at drain terminal and terminates at source terminal. The intensity of current through CNT channel is controlled by the gate terminal of CNFET and no current will flow if the gate voltage is zero. Although several new technologies like DGFET, FinFET, and TFET have been proposed, their complex structure is still a disadvantage in comparison to the simple 1-D structure of CNFET. CNFET also has an advantage in terms of flexibility in the variation of threshold voltage, by varying chirality and diameter of the CNT, which makes it suitable of MVL.

Several attempts have been made for modeling CNFET devices [17][18] for digital and analog applications. In this work, we have used the CNFET Verilog-A model designed by Stanford University [19][20]. It comprises Schottky barrier (SB) resistance, channel scattering, the doped source/drain (S/D) region, several CNTs per device and other device non-idealities.

3.4.1 Device Hierarchy

Stanford CNFET Model is divided into three levels given by level 1, level 2 and level 3. At each hierarchical level device parameters, which basically refer to the non-idealities, are introduced. Figure 3.2 shows the basic representation at each level. CNFET level 1 is symbolized by CNFET_L1, demonstrating the intrinsic behaviour of C-CNFET.

Level 1 model of CNFET is similar to device-level models. The device non-idealities are modelled in level 2, symbolized by CNFET_L2. This level includes non-idealities like:

i. Resistance due to doped S/D CNT region and S/D contacts
ii. Capacitance due to S/D region of CNT.

The top level of the CNFET model is represented by CNFET_L3. The previous two levels of the considered CNFET model comprise of single CNT as the channel, whereas CNFET_L3 deals with multiple CNTs. It also includes parasitic capacitances at the gate and interconnects.

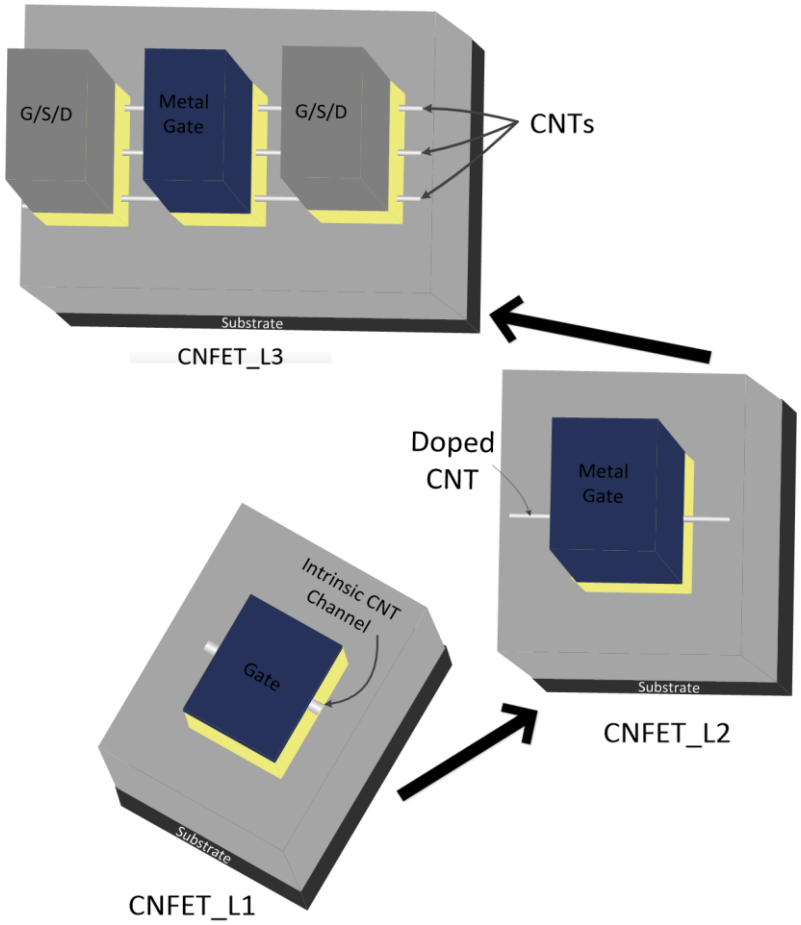


Fig 3.2. CNFET Model Hierarchy

3.4.2 Device parameters

The CNFET model used has some limiting value for parameters like channel length, channel width, the number of CNT tubes and several others, as tabulated in Table 3.1. Moreover, Table 3.2.tabulates different parameters and values used in this work.

Table 3.1: Min and Max value for CNFET Model

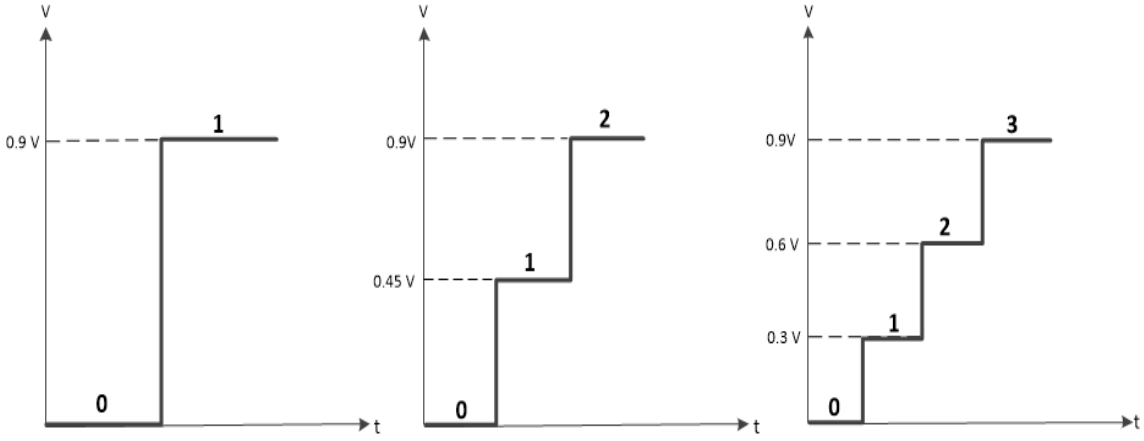
Device Types	n-type/p-type CNFET
Device Dimensions:	
Channel Length (min)	~10 nm
Channel Length (max)	unlimited
Channel Width (min)	4 nm
Channel Width (max)	unlimited
Number of CNTs per Device	1
Number of CNTs per Device	unlimited
Non-idealists/Additional Practical Effect	
Schottky Barrier Effects	Yes: CNT S/D degenerate doping required
Parasitics	S/D/G resistances & capacitances, CNT
Metal Chirality	No

Table 3.2: Parameters description and there values

Global Parameters	Descriptions	Value
L_Channel	physical channel length	15 nm
Lceff	mean value of free intrinsic CNT	200 nm
L_sd	doped S/D extension region length	15 nm
Efo	Fermi level above conduction band for doped S/D region	0.6 eV
Kox	Oxide Dielectric constant	16
Ccsd	channel-source and channel-drain region coupling capacitance	0.0 pF/m
CNTPos	CNT position in channel: 0: CNT is present in the middle 1: CNT is present at the edge	1
(n1,n2)	CNT Chirality	Depend on Vth
Wgate	Metal gate width	6.4 nm
Pitch	Distance between centres of CNT within the device	20 nm
Csub	Channel-Substrate coupling capacitance	20 pF/m

3.5 Introduction to QTL and its implementation

As discussed in chapter 1, MVL can be used to reduce interconnects and achieve cost-effectiveness. In MVL, two types of logic systems radix-3 (ternary) and radix-4 (quaternary), with three and four voltage levels, respectively, have been widely discussed in the literature [39]. The radix-3 number systems can have two logic systems, first balanced ternary logic with levels *-1, 0, 1* and second simple/normal ternary logic with levels *0,1,2*. Radix-4 number system has only one logic system, represented by logic levels *0,1,2,3.* Figure 3.3 shows the logic levels for binary, ternary and quaternary logic for the supply voltage of 0.9 v.



(a) (b) (c)

Figure 3.3. Logic level representation of (a) binary, (b) ternary and (c) quaternary logic

For any number system, the relation between radix of the number system (*R*), number of digits required to represent a value (*n*) and the range of value (*D*) is given by equation 3.1. We can conclude from equation 3.1 that higher the radix, higher shall be the range of value being represented.

$$D = R^n \tag{3.1}$$

Complexity or cost-effectiveness for MVL given by *C* is proportional to *D* and n, as given in equation 3.2 with *k* as a constant.

$$C = k(D \times n) \tag{3.2}$$

The minimum value of *C* given by equation 3.3 is determined by differentiating equation 3.2 w.r.t. *R*.

$$C = k[R \log D / \log R] \quad (3.3)$$

MVL can be implemented in voltage mode and current mode. In this work, we have implemented voltage mode circuit. The next section shows the implementation of basic QTL gate using CNFET.

3.5.1 Fundamentals for QTL Implementation using CNFET

As discussed in the previous section QTL is a radix-4 logic system which uses four voltage level as given in table 3.3.

Table 3.3. QTL logic level

Logic Level	Voltage
0	0 V
1	0.2 V
2	0.4 V
3	0.6 V

The relation between the threshold voltage and CNT diameter is given by equation 3.4.

$$V_{th} \cong \frac{E_g}{2e} \cong \frac{0.436}{d} \quad (3.4)$$

In this work, we have used four chirality values to implement QTL, that is tabulated in Table 3.4, along with the diameter and threshold voltage for CNFET.

Table 3.4. Summary of CNFET parameters
(Chirality, CNT diameter, and threshold voltage)

Chirality	CNT diameter	Threshold Voltage	
		N-CNFET	P-CNFET
(8,0)	0.634 nm	0.687 V	- 0.687 V
(13,0)	1.03 nm	0.423 V	-0.423 V
(19,0)	1.506 nm	0.289 V	-0.289 V
(29,0)	2.298 nm	0.189 V	-0.189 V

3.5.2 QTL Logic Gates

In QTL there are four types of inverters whose logic definitions are given by equations 3.5, 3.6, 3.7 and 3.8. Table 3.5 tabulates the truth table for same.

$$NQI = \begin{cases} 0 \; if \; x \neq 0 \\ 3 \; if \; x = 0 \end{cases} \tag{3.5}$$

$$IQI = \begin{cases} 0 \; if \; x = 0,1 \\ 3 \; if \; x = 2,3 \end{cases} \tag{3.6}$$

$$PQI = \begin{cases} 3 \; if \; x \neq 3 \\ 0 \; if \; x = 3 \end{cases} \tag{3.7}$$

$$SQI = 3 - x \tag{3.8}$$

Table 3.5. Truth table for QTL inverter

Input (x)	Output			
	NQI	IQI	PQI	SQI
0	3	3	3	3
1	0	3	3	2
2	0	0	3	1
3	0	0	0	0

The equation 3.5 represents Negative QTL inverter (NQI) function. CNFET implementation for NQI is shown in figure 3.4 (a), where PCNFET Tp_1 is implemented using CNT (8,0) and NCNFET Tn_1 is implemented using CNT (29,0). In NQI when input *x* is at logic *0*, Tp_1 switches *ON* and Tn_1 switches *OFF* resulting in output at logic *3*. For input *x* at logic *1*, *2* and *3* Tp_1 switches off and Tn_1 switches *ON* resulting in logic *0* at output node.

Intermediate QTL inverter (IQI) also known as Symmetrical QTL inverter (SyQI) function is given in equation 3.6. CNFET implementation for NQI is shown in figure 3.4 (b), where both PCNFET Tp_1 and NCNFET Tn_1 is implemented using CNT (13,0). In IQI when input *x* is at logic *0* and *1*, Tp_1 switches *ON* and Tn_1 switches *OFF* resulting in output at logic *3*. For input *x* at logic *2* and *3* Tp_1 switches *OFF* and Tn_1 switches *ON* resulting in logic *0* at output node.

Positive QTL inverter (PQI) function is given by equation 3.7. CNFET implementation for PQI is shown in figure 3.4 (c), where PCNFET Tp_1 is implemented using CNT (29,0) and NCNFET Tn_1 is implemented using CNT (13,0). In PQI when input *x* is at logic *0, 1* and *2*, Tp_1 switches *ON* and Tn_1 switches *OFF* resulting in output at logic *3*. For input *x* at logic *3* Tp_1 switches *OFF* and Tn_1 switches *ON* resulting in logic *0* at output node.

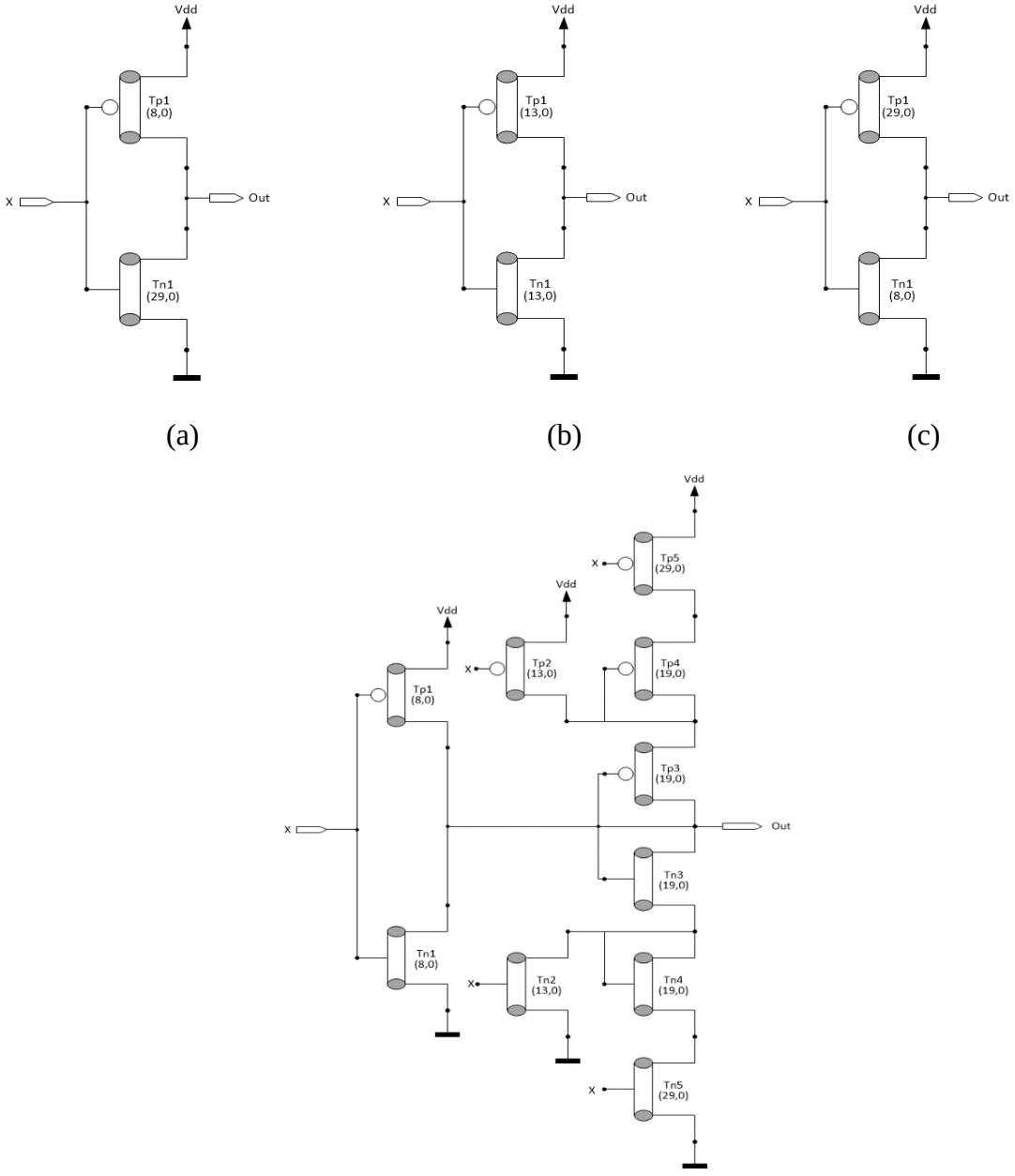


Figure 3.4 CNFET implementation of (a) NQI, (b) IQI, (c) PQI and (d) SQI

Equation 3.8 represents Standard QTL inverter (SQI) function where input and output both have 4 logic levels. Its CNFET implementation is shown in figure 3.4 (d)

where 5 CNFETs of each type (PCNFET and NCNFET) are used. Transistors Tn3, Tn4, Tp3, and Tp4 are used as resistances to obtain different voltage levels. The voltage drop across each of these transistors is Vdd/3. Implementation of Tp_1 has been done using CNT (8,0). Tp_1 switches *ON* at logic *0* while switching *OFF* transistors Tp_2 and Tp_5. For implementing Tp_2 CNT (13,0) has been used. It switches *ON* at $2V_{dd}/3$ while switching *OFF* Tp_1 resulting in logic *2* at output node. Similarly, at logic *2* Tp_5 switches *ON* while switching *OFF* Tp_1 and Tp_2 resulting in logic *1* at output node. Transient response for inverters discussed above is shown in figure 3.5 below.

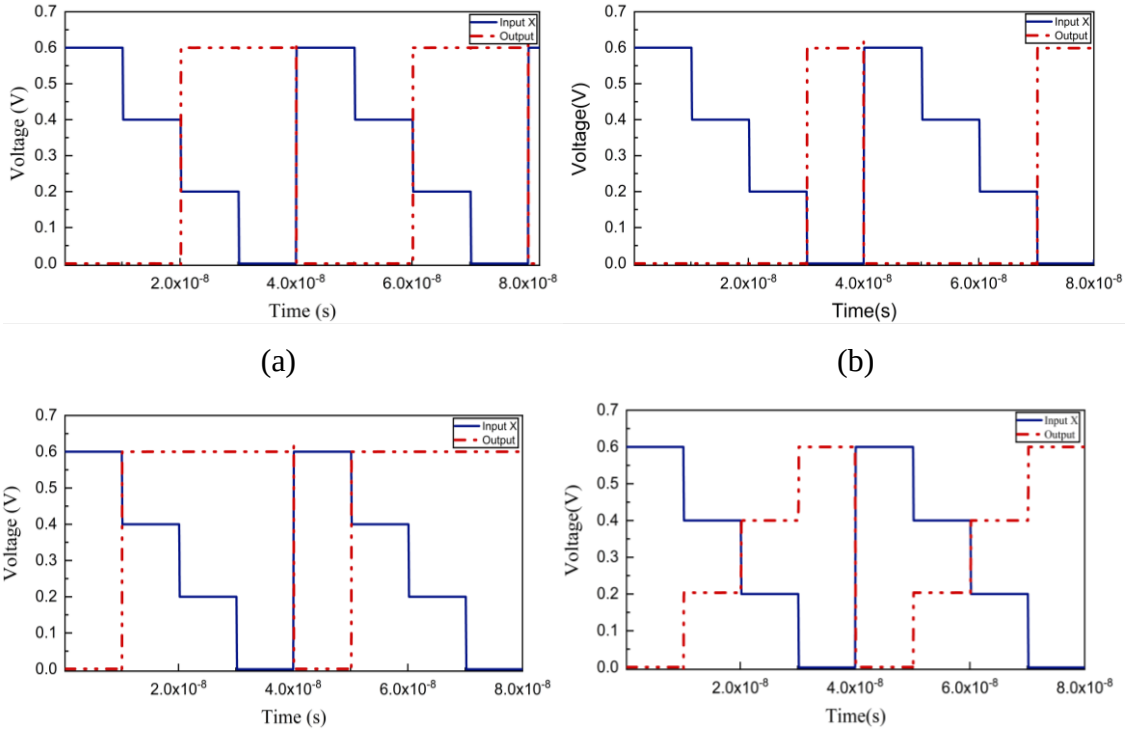


Figure 3.5 Transient Response of (a) IQI, (b) NQI, (c) PQI and (d) SQI

NAND and NOR have also been implemented using QTL called QTL NAND (QNAND) and QTL NOR (QNOR) gates. The logic operations for these gates are given by equation 3.9 and 3.10.

$$QNAND(x_1, x_2, \dots, x_n) = 3 - min(x_1, x_2, \dots, x_n) \quad 3.9$$

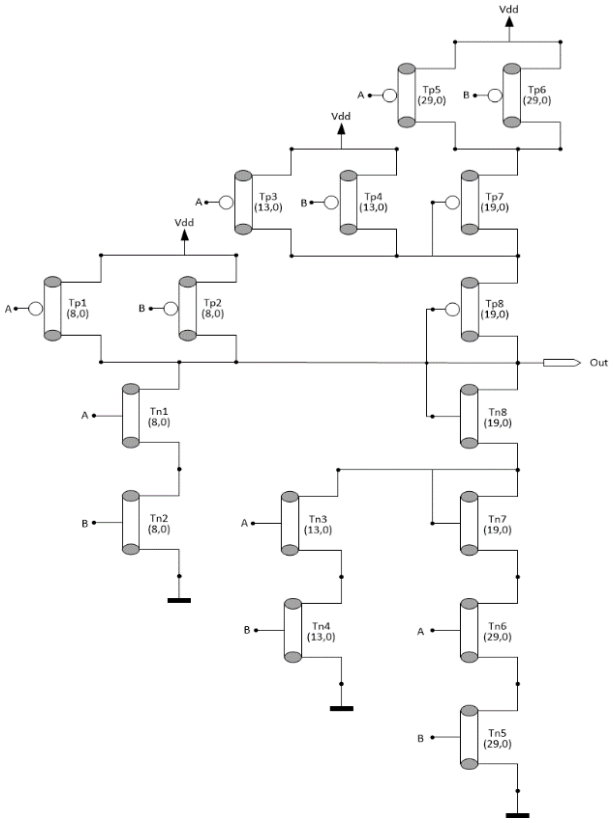
$$\mathrm{QNOR}(x_1, x_2, \dots, x_n) = 3 - max(x_1, x_2, \dots, x_n) \quad 3.10$$

where $x_1, x_2, \dots, and\ x_n$ are the inputs to the gates. Table 3.6 shows the truth table for two input QNAND and QNOR gates.

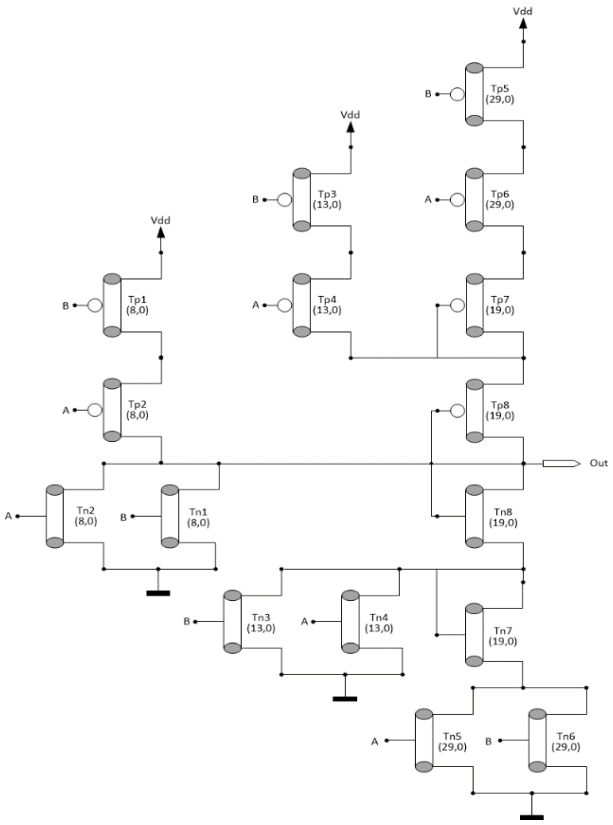
Table 3.6. Truth table for QNAND and QNOR

Input(s)		Output(s)	
A	B	QNAND	QNOR
0	0	3	3
0	1	3	2
0	2	3	1
0	3	3	0
1	0	3	2
1	1	2	2
1	2	2	1
1	3	2	0
2	0	3	1
2	1	2	1
2	2	1	1
2	3	1	0
3	0	3	0
3	1	2	0
3	2	1	0
3	3	0	0

Figure 3.6 (a) shows the QNAND implementation in which Tp_1 and Tp_2 conduct when input A, as well as input B, is at logic *3* resulting in the output of V_{dd}. Output $2V_{dd}/3$ is obtained when Tp_3 and Tp_4 conducts. When Tp_5 and Tp_6 conduct, the output becomes $V_{dd}/3$. Similarly, the implementation of QNOR is given in figure 3.6(b). In this circuit when any one of the inputs is V_{dd}, either Tn_1 or Tn_2, or both, conduct making the direct path between output and ground terminal to obtain logic *0*. When the input is logic *1* then Tn_5, Tn_6, Tp_3, and Tp_4 conduct. Tn_3, Tn_4, Tp_5, and Tp_6 conduct when input is logic *2*. Transient response for QNAND and QNOR gates are also given in figure 3.7.

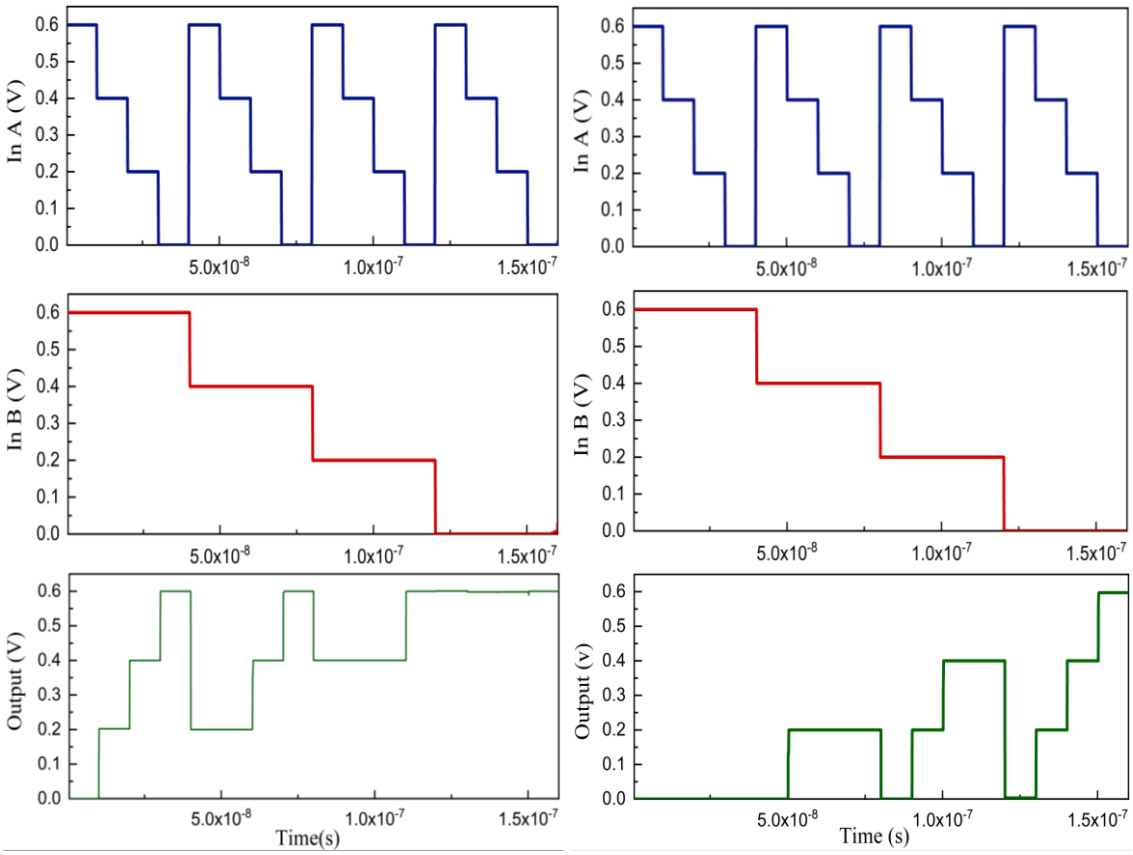

Vdd
Tp5 (29,0)
Tp6 (29,0)
Tp3 (13,0)
Tp4 (13,0)
Tp7 (19,0)
Tp1 (8,0)
Tp2 (8,0)
Tp8 (19,0)
Out
Tn1 (8,0)
Tn8 (19,0)
Tn2 (8,0)
Tn3 (13,0)
Tn7 (19,0)
Tn4 (13,0)
Tn6 (29,0)
Tn5 (29,0)
A
B

(a)


Vdd
Tp5 (29,0)
Tp6 (29,0)
Tp3 (13,0)
Tp4 (13,0)
Tp7 (19,0)
Tp1 (8,0)
Tp2 (8,0)
Tp8 (19,0)
Out
Tn2 (8,0)
Tn1 (8,0)
Tn8 (19,0)
Tn3 (13,0)
Tn4 (13,0)
Tn7 (19,0)
Tn5 (29,0)
Tn6 (29,0)
A
B

(b)

Figure 3.6. CNFET implementation of (a) QNAND and (b) QNOR



(a) (b)

Figure 3.7. Transient Response of (a) QNAND and (b) QNOR

3.6 Summary

In this chapter the complete Stanford CNFET model has been discussed, and for QTL implementation default parameter set is presented. The simulation results for QTL logic gates are obtained and also compared against the truth table to verify the functionality of each circuit.

CHAPTER 4

Proposed QTL Arithmetic Logic unit

4.1 Introduction

In this chapter, efficient QTA full adder (QFA), QTL multiplier (QM) and QTL ALU designs are proposed. Full adder is the most basic element for designing any processing unit. So, power, delay, and area-efficient design for full adder is a necessity. Here we have used efficient QTL multiplexer to design QFA, QM and QTL ALU.

This chapter is portioned into 6 sections starting with section 4.1 about introduction followed by objectives of the chapter in section 4.2. Thereafter section 4.3 and 4.4 focuses on QTL logic designs and proposed adder circuits designs respectively followed by section 4.5 on proposed QTL multiplier. Section 4.6 introduces power and delay efficient QTL ALU design. At last Brief summary given in section 4.7.

4.2 Objective

The primary objectives of this chapter are as follows:

1. To present the power, area and delay efficient designs to implement QTL Logic.
2. QFA, QM and QTL ALU designs using the QTL multiplexer.
3. Operational Analysis of proposed designs.

4.3 QTL Logic Design

In this section, we have designed multiplexer [21], incrementor, level II incrementor and decrementor.

4.3.1 QTL 4:1 Multiplexer

QTL 4:1 multiplexer (mux) design is shown in figure 4.1. It consists of 6 inverters NQI, PQI, IQI, and 3 SQIs in order to obtain the signals $NQI,\ PQI,\ IQI,\ \overline{NQI},$

$\overline{PQI}$ *and* $\overline{IQI}$. These 6 signals are used to control 6 Transmission gates T_1 to T_6 which consist of NCNFET and PCNFET using CNT (29,0). The operation of the multiplexer is given as follows:

- When $S = 0$, signals NQI, PQI and IQI are at logic *3* and $\overline{NQI}, \overline{PQI}$ and $\overline{IQI}$ are at logic *0* due to which transmission gates T_1, T_2 and T_4 act as closed switches and T_3, T_5 and T_6 act as open switches; transferring input I_0 to the output terminal.

- When $S = 1$, signals IQI, $\overline{NQI}$ and PQI are at logic *3* and NQI, $\overline{PQI}$ and $\overline{IQI}$ are at logic *0* due to which transmission gate T_2, T_3 and T_4 act as closed switches and T_1, T_5, and T_6 act as open switches transferring input I_1 to output terminal.

- When $S = 1$, signals $\overline{IQI}$, $\overline{NQI}$ and PQI at logic *3* and NQI, IQI and $\overline{PQI}$ are at logic *0* due to which transmission gate T_3, T_4, and T_5 act as closed switches and T_1, T_2, and T_6 act as open switches transferring input I_2 to output terminal.

- When $S = 1$, signals $\overline{NQI}, \overline{PQI}, and\ \overline{IQI}$ are at logic *3* and NQI, PQI and IQI are at logic *0* due to which transmission gate T_3, T_5 and T_6 act as closed switches and T_1, T_2 and T_4 act as open switches transferring input I_2 to output terminal.

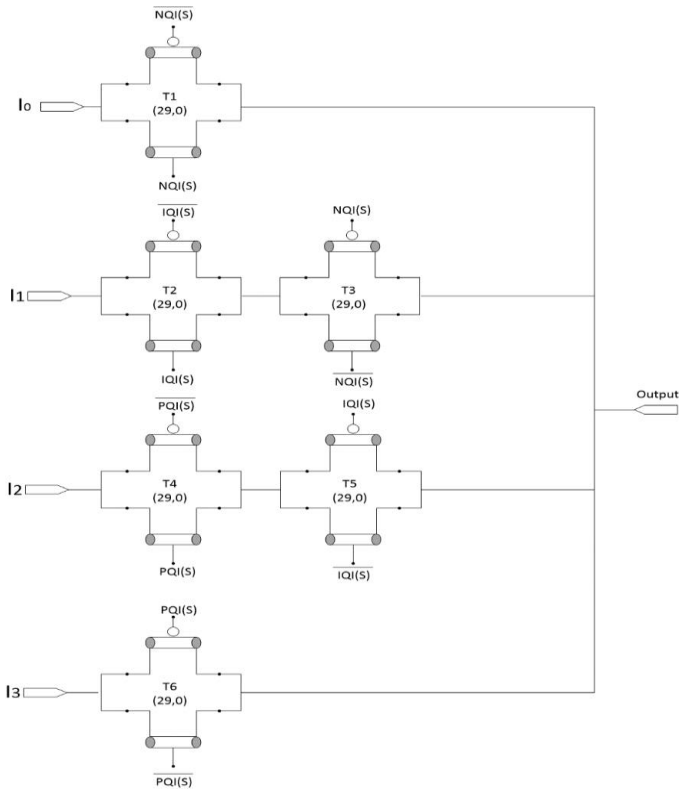


Figure 4.1. CNFET implementation of 4:1 Multiplexer

4.3.2 Positive 2:1 QTL Multiplexer

Positive QTL 2:1 Multiplexer design is shown in figure 4.2 [21]. It consists of inverter NQI and transmission gate T_1 and T_2. The operation of positive 2:1 multiplexer is given as follows:

- When *S = 0*, output of NQI is at logic at *3* due to which transmission gates T_1 act as closed switches and T_2 act as open switches transferring input I_0 to the output terminal.

- For other value of S (*1*,*2* and *3*), output of NQI is at logic *0* due to which transmission gates T_2 act as closed switches and T_1 act as open switches transferring input I_1 to the output terminal.

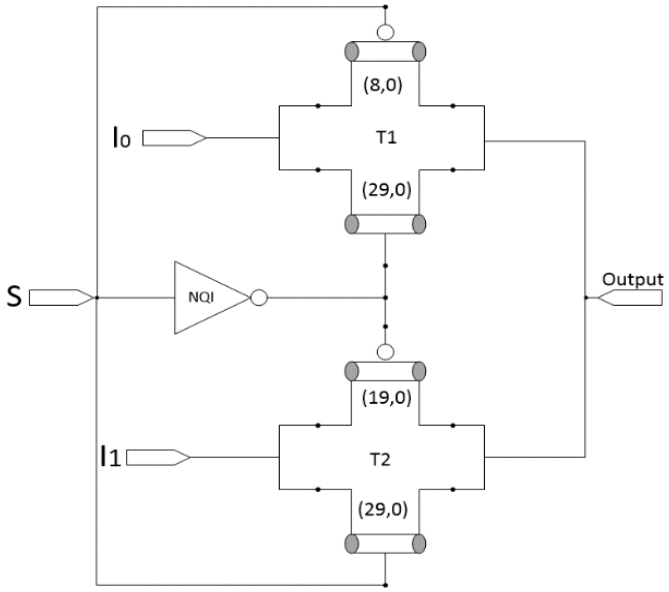


Figure 4.2. CNFET implementation of Positive 2:1 Multiplexer

4.3.3 Incrementor

Modified 4:1 multiplexer is used to implement incrementor that is used in designing the proposed QFA and QM designs. In this implementation, we have only used either P-CNFET or N-CNFET instead of transmission gate based on the value of the input. Figure 4.3 shows CNFET implementation for incrementor where transistor Tp_1, Tp_2, and Tp_3 are used to implement the voltage divider circuit for obtaining logic *1* and logic *2* voltage levels. Table 4.1 shows the truth table for incrementor, Level-II incrementor, and decrementor.

Table 4.1. Truth table for incrementor, Level-II incrementor, and decrementor

Input (x)	Output		
	Incrementor	Level II Incrementor	Decrementor
0	1	2	3
1	2	3	0
2	3	0	1
3	0	1	2

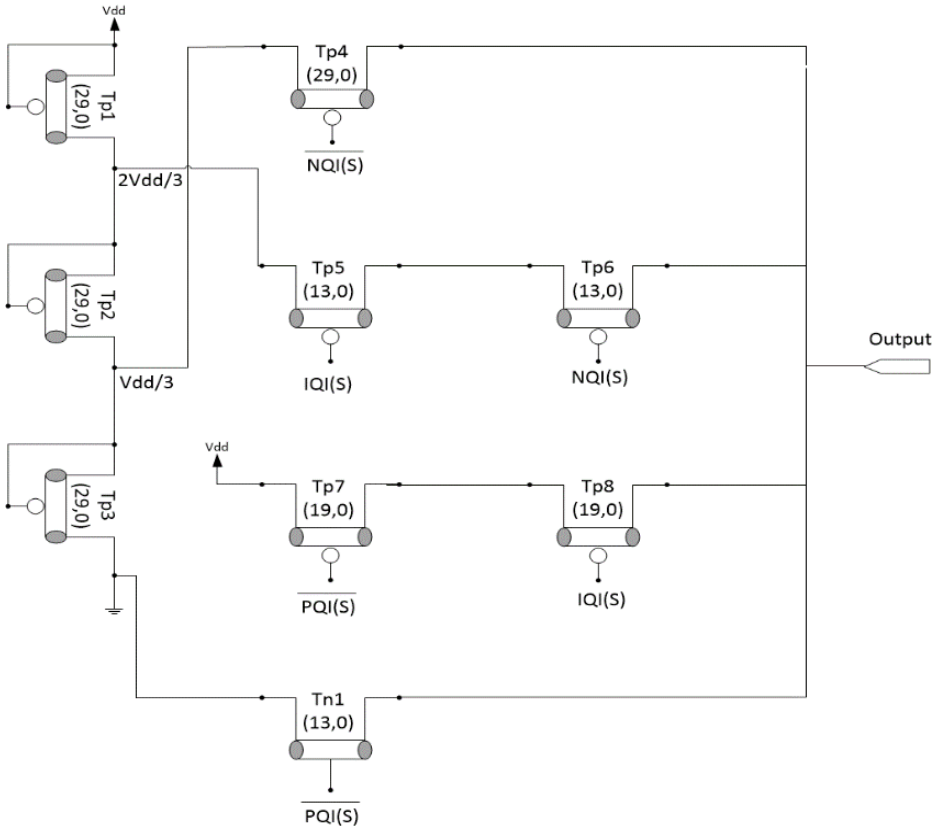


Figure 4.3. CNFET implementation of Incrementor

The operation of incrementor is given as follows:

- When input S is at logic *0*, Tp_4, Tp_5, and Tp_7 are ON while Tp_6, Tp_8 and Tn_1 are OFF; due to this $V_{dd}/3$ voltage node is connected to the output node generating logic *1*.
- When input S is at logic *1*, Tp_5, Tp_6 and Tp_7 are ON while Tp_4, Tp_8 and Tn_1 are OFF; due to this $2V_{dd}/3$ voltage node is connected to the output node generating logic *2*.

- When input S is at logic *2*, Tp_6, Tp_7, and Tp_8 are ON while Tp_4, Tp_5, and Tn_1 are OFF; due to this V_{dd} voltage node is connected to the output node generating logic *3*.
- When input S is at logic 3, Tn_1, Tp_6 and Tp_8 are ON while Tp_4, Tp_5, and Tp_7 are OFF; due to this ground node is connected to the output node generating logic *0*.

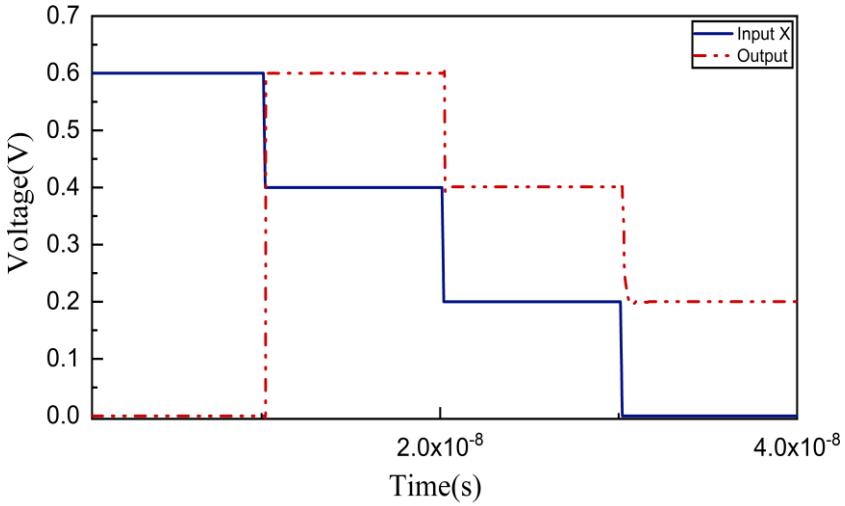


Figure 4.4. Transient Response of Incrementor

4.3.4 Level II Incrementor

In level II incrementor the input voltage is increased by 2. CNFET Implementation and transient response for which shown in figure 4.5 and figure 4.6 respectively. Operation of level II incrementor is as follows:

- When input S is at logic *0*, Tp_4, Tp_5 and Tp_7 are ON while Tp_6, Tn_1 and Tn_2 are OFF; due to this $2V_{dd}/3$ voltage node is connected to the output node generating logic *2*.
- When input S is at logic *1*, Tp_5, Tp_6 and Tn_2 are ON while Tn_1, Tp_4 and Tp_7 are OFF; due to this V_{dd} voltage node is connected to the output node generating logic *3*.
- When input S is at logic *2*, Tp_6, Tn_1, and Tn_2 are ON while Tp_4, Tp_5 and Tp_7 are OFF; due to this ground node is connected to the output node generating logic *0*.
- When input S is at logic *3*, Tp_6, Tp_7, and Tn_1 are ON while Tp_4, Tp_5 and Tn_2 are OFF; due to this $V_{dd}/3$ voltage node is connected to the output node generating logic *1*.

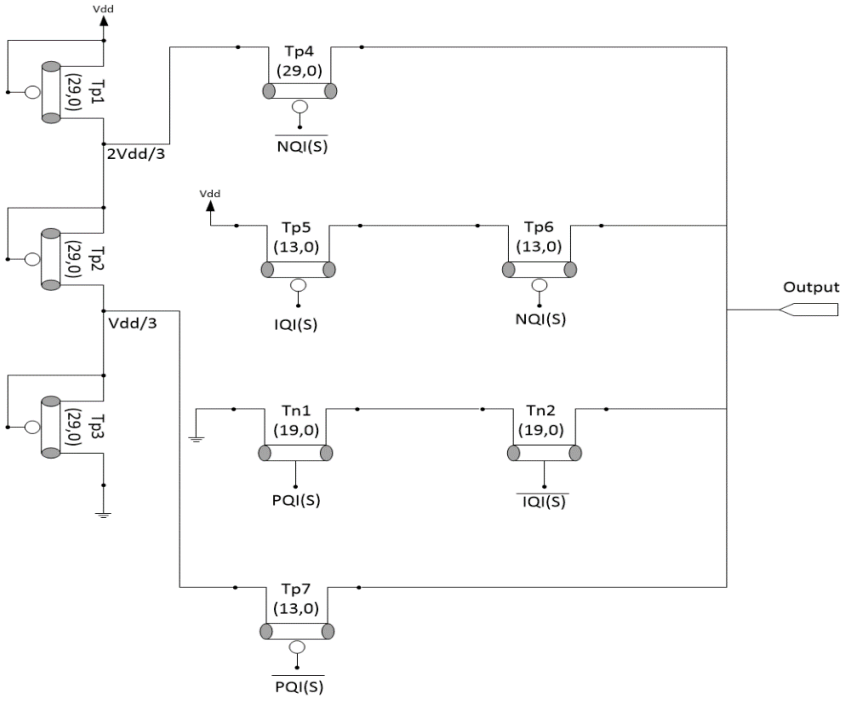


Figure 4.5. CNFET implementation of Level II Incrementor

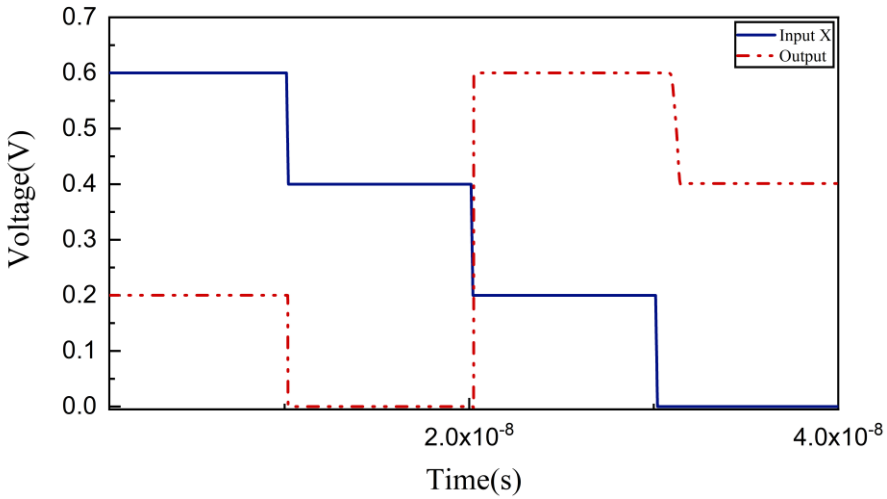


Figure 4.6. Transient response of Level II Incrementor

4.3.4 Decrementor

In decrementor the input voltage is decreased by 1. CNFET Implementation and transient response for which shown in figure 4.7 and figure 4.8 respectively. Operation of decrementor is as follows:

- When input S is at logic *0*, Tp_4, Tp_5 and Tn_1 are ON while Tp_6, Tp_7 and Tn_2 are OFF; due to this V_{dd} voltage node is connected to the output node generating logic *3*.

- When input S is at logic *1*, Tp_5, Tn_1 and Tn_2 are ON while Tp_4, Tp_6 and Tn_7 are OFF; due to this ground node is connected to the output node generating logic *0.*
- When input S is at logic *2*, Tp_5, Tp_6 and Tn_2 are ON while Tp_4, Tp_6 and Tp_7 are OFF; due to this $V_{dd}/3$ voltage node is connected to the output node generating logic *1*.
- When input S is at logic *3*, Tp_6, Tp_7 and Tn_2 are ON while Tp_4, Tp_5 and Tn_1 are OFF; due to this $2V_{dd}/3$ voltage node is connected to the output node generating logic *2*.

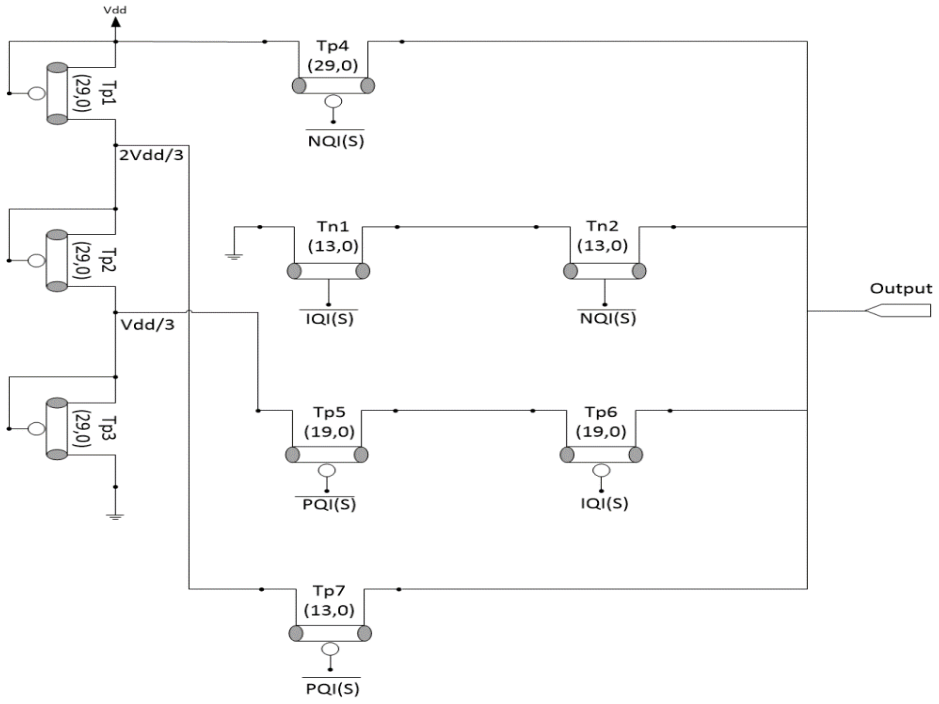


Figure 4.7. CNFET implementation of Decrementor

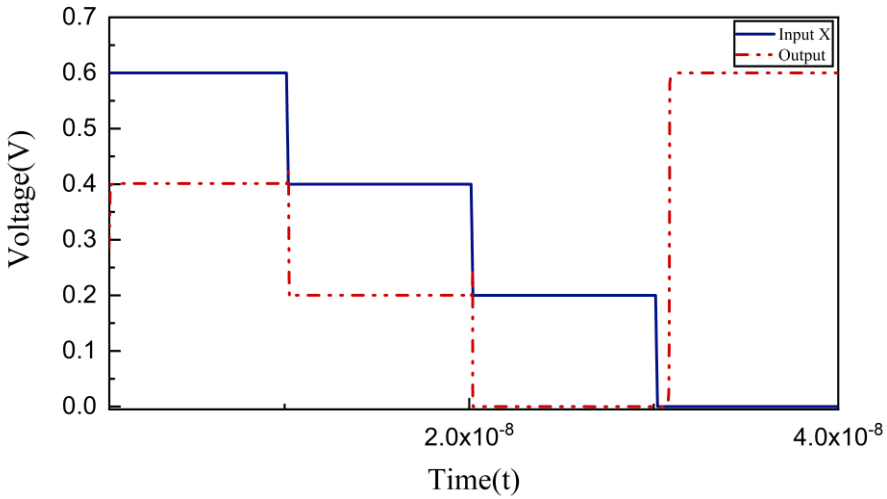


Figure 4.8. Transient response of Decrementor

4.4 Proposed QTL Full Adder

Table 4.2 tabulates the truth table for QFA with inputs A, B and C_{in} and outputs sum and C_{out}

Table 4.2: QFA Truth Table

Input(s)			Output(s)	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	2	0
0	2	0	2	0
0	2	1	3	0
0	3	0	3	0
0	3	1	0	1
1	0	0	1	0
1	0	1	2	0
1	1	0	2	0
1	1	1	3	0
1	2	0	3	0
1	2	1	0	1
1	3	0	0	1
1	3	1	1	1
2	0	0	2	0
2	0	1	3	0
2	1	0	3	0
2	1	1	0	1
2	2	0	0	1
2	2	1	1	1
2	3	0	1	1
2	3	1	2	1
3	0	0	3	0
3	0	1	0	1
3	1	0	0	1
3	1	1	1	1
3	2	0	1	1
3	2	1	2	1
3	3	0	2	1
3	3	1	3	1

Figure 4.9 shows the implementation of the proposed QFA sum circuit which contains one 4:1 multiplexer (M5) with 48 CNFETs, four 2:1 multiplexers (M1, M2, M3 and M4) with 6 CNFETs each, along with incrementor, Level II incrementor and decrementor consisting of 45 CNFETs each. Therefore, we require 207 CNFETs for implementing QFA.

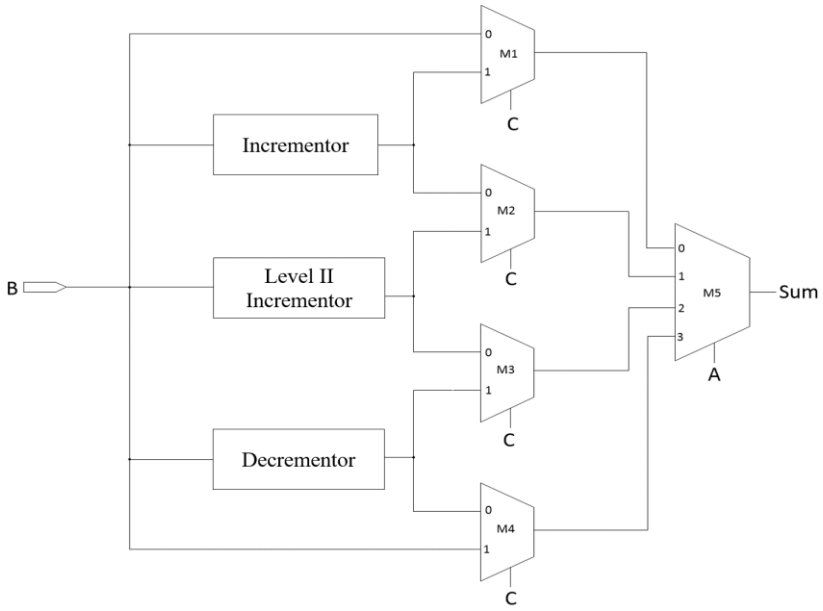


Figure 4.9. Implementation of sum generator circuit

Operation of QFA is as follows:

- When Input *A* is at logic *0*, mux M_5 selects input *0* which is obtained from the output of mux M_1. Input *C* is used to switch between inputs of mux M_1. If *C* is at logic *0*, then we obtain the sum same as input B and when *C* is logic 1 then we obtain the sum after incrementing the input B.
- When Input *A* is at logic *1*, mux M_5 selects input *1* which is obtained from the output of mux M_2. Input *C* is used to switch between inputs of mux M_2. If *C* is at logic *0*, then we obtain the sum after incrementing the input *B* and when *C* is logic *1* then we obtain the sum after incrementing the input *B* by 2.
- When Input *A* is at logic *2*, mux M_5 selects input *2* which is obtained from the output of mux M_3. Input *C* used to switch between inputs of mux M_3. If *C* is at logic *0*, then we obtain the sum after incrementing the input *B* by 2 and when *C* is at logic *1* then we obtain the sum after decrementing the input *B*.
- When Input *A* is at logic *3*, mux M_5 selects input *3* which is obtained from the output of mux M_4. Input *C* is used to switch between inputs of mux M_4. If *C* is at

logic *0*, then we obtain the sum after decrementing the input *B* and when *C* is at logic *1* then we obtain the sum same as input B.

The carry function (C_out) is implemented as given in figure 4.10. For its implementation, we have used 80 CNFETs (one 4:1 multiplexer (M5) with 48 CNFETs, two 2:1 multiplexers (M_1, M_2, M_3 and M_4) with 6 CNFETs each, two NQIs with 6 CNFETs each and single PQI and IQI with 6 CNFETs).

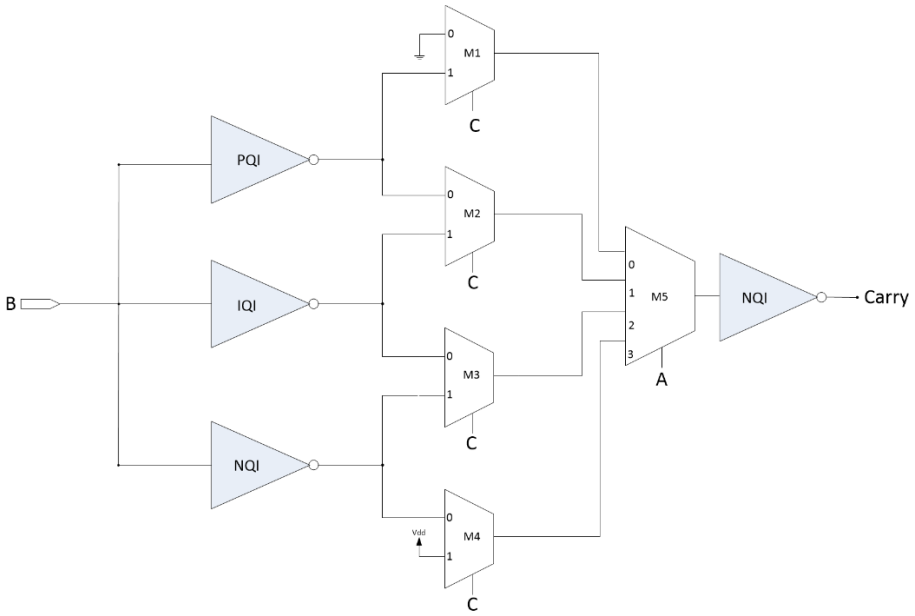


Figure 4.10. CNFET implementation of carry generator circuit

Operation of the QFA carry generator circuit is as follows:

- When Input *A* is logic *0*, mux M_5 selects input *0* which is obtained from the output of mux M_1. Input *C* used to switch between inputs of mux M_1. If *C* is logic *0*, then we obtain the $\overline{C\_out}$ = 1 and when *C* is logic 1 then we obtain the $\overline{C\_out}$ after passing input B through PQI.
- When Input *A* is logic *1*, mux M_5 selects input *1* which is obtained from the output of mux M_2. Input *C* used to switch between inputs of mux M_2. If *C* is logic *0*, then we obtain the $\overline{C\_out}$ after passing input B through PQI and when *C* is logic 1, then we obtain the $\overline{C\_out}$ after passing input B through IQI.
- When Input *A* is logic *2*, mux M_5 selects input *2* which is obtained from the output of mux M_3. Input *C* used to switch between inputs of mux M_3. If *C* is logic *0*, then we obtain the $\overline{C\_out}$ after passing input B through IQI and when *C* is logic 1, then we obtain the $\overline{C\_out}$ after passing input B through NQI.

- When Input *A* is logic *3*, mux M_5 selects input *3* which is obtained from the output of mux M_4. Input *C* used to switch between inputs of mux M_4. If *C* is logic *0*, then we obtain the $\overline{C\_out}$ after passing input B through NQI and when *C* is logic 1, then we obtain the $\overline{C\_out}$ =1.

Operation explained above can be verified with QFA truth table given in table 4.2 with transient response displayed in figure 4.11. Where *In A*, *In B* and *In C_in* represent input *A*, input *B* and input *carry* respectively, while output sum and carry out are represented using Sum and Carry.

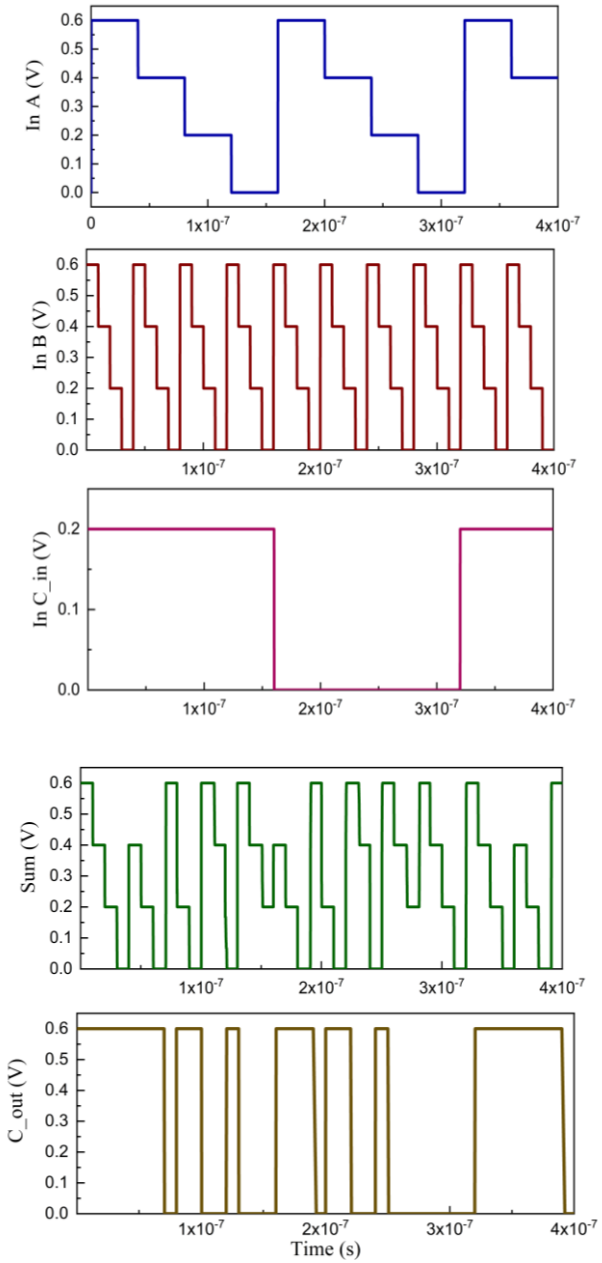


Figure 4.11: Transient response of QFA

4.5 Proposed 1 bit QTL Multiplier

In this section, we will discuss the QTL 1-bit multiplier. Similar to the QFA, QM is also implemented in two parts namely, product generator and carry generator circuits as shown in figure 4.12 and figure 4.13, respectively. Table 4.3 shows the truth table of the QM.

Table 4.3: QM Truth Table

Input(s)			Output(s)	
A	B	C_in	Product	C_out
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	0	0
0	1	1	1	0
0	1	2	2	0
0	2	0	0	0
0	2	1	1	0
0	2	2	2	0
0	3	0	0	0
0	3	1	1	0
0	3	2	2	0
1	0	0	0	0
1	0	1	1	0
1	0	2	2	0
1	1	0	1	0
1	1	1	2	0
1	1	2	3	0
1	2	0	2	0
1	2	1	3	0
1	2	2	0	1

Continue

Continue

Input(s)			Output(s)	
A	B	C_in	Product	C_out
1	3	0	3	0
1	3	1	0	1
1	3	2	1	1
2	0	0	0	0
2	0	1	1	0
2	0	2	2	0
2	1	0	2	0
2	1	1	3	0
2	1	2	0	1
2	2	0	0	1
2	2	1	1	1
2	2	2	2	1
2	3	0	2	1
2	3	1	3	1
2	3	2	0	2
3	0	0	0	0
3	0	1	1	0
3	0	2	2	0
3	1	0	3	0
3	1	1	0	1
3	1	2	1	1
3	2	0	2	1
3	2	1	3	1
3	2	2	0	2
3	3	0	1	2
3	3	1	2	2
3	3	2	3	2

Operation of QM product generator circuit shown in figure 4.12 consists of four 4:1 multiplexer (M_1, M_2, M_3, and M_4) with 48 CNFET transistors each along with incrementor, Level II incrementor and decrementor having 45 transistors each.

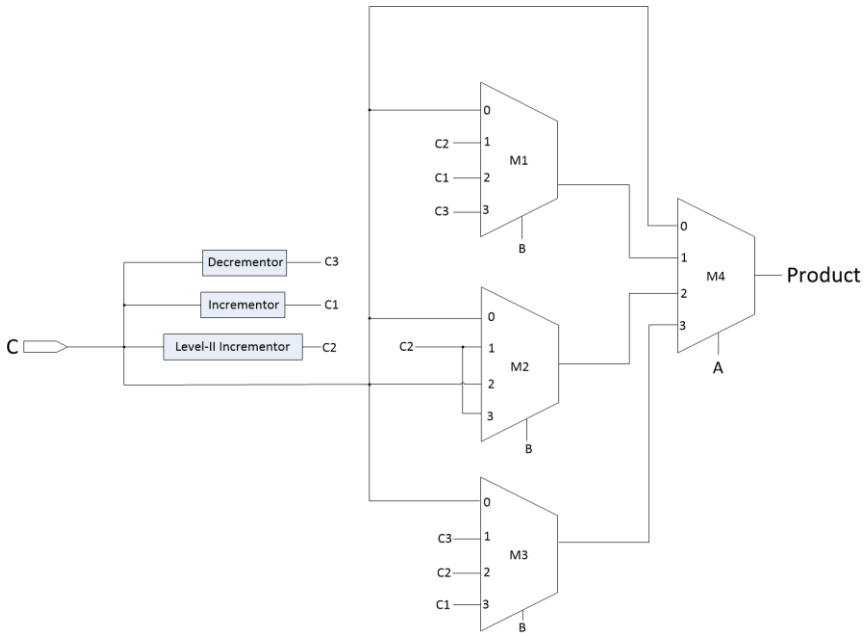


Figure 4.12. CNFET implementation of QM Product generator circuit

In this circuit, incrementor, Level II incrementor and decrementor are used with input *C* (*0, 1, 2* and *3*) to generate the signal C_1 (*1, 2, 3* and *0*), C_2 (*2, 3, 0* and *1*) and C_3 (*3, 0, 1* and *2*). Input *A* is used as a select line in multiplexer M_4 while for multiplexer M_1, M_2, and M_3 input *B* is used as the select line. Operation of this circuit is as follows:

- When Input A is logic *0*, mux M_4 selects input *0* which is connected to input *C*.
- When Input *A* is logic *1*, mux M_4 selects input *1* which is obtained from the mux M_1. In mux M_1 inputs are *C*, C_1, C_2, and C_3 respectively.
- When Input *A* is logic *2*, mux M_4 selects input *2* which is obtained from the mux M_2. In mux M_2 inputs are *C*, C_2, *C*, and C_2 respectively.
- When Input *A* is logic *3*, mux M_4 selects input *1* which is obtained from the mux M_3. In mux M_3 inputs are C, C_3, C_2, and C_1 respectively.

Figure 4.13 shows the implementation of the proposed QM carry generator circuit which contains four 4:1 multiplexers (M_1, M_2, M_3, and M_4) with 48 CNFETs each, NQI with 2 CNFETs, two IQI with 2 CNFETs each, along with incrementor, Level II incrementor and decrementor consisting 45 CNFETs each. Operation of the QM carry generator circuit is as follows:

- Function F_1 is implemented using the combination of IQI and incrementor. The output *0, 0, 1* is obtained for input *C* with value *0, 1* and *2*.
- Function F_2 is implemented using the combination of NQI and incrementor. The output *0, 1, 1* is obtained for input *C* with value *0, 1* and *2*.
- Function F_3 is implemented using the combination of IQI and level-II incrementor. The output *1, 1, 0* is obtained for input C with value *0, 1* and *2*.
- Function F_4 is implemented using the decrementor with *A*.

- When Input A is logic *0*, mux M_4 selects input *0* which is connected to *ground*.
- When Input *A* is logic *1*, mux M_4 selects input *1* which is obtained from the mux M_1. In mux M_1 inputs are *ground, ground,* F_1, and F_2 respectively.
- When Input *A* is logic *2*, mux M_4 selects input *2* which is obtained from the mux M_2. In mux M_2 inputs are *ground,* F_1, F_4, and F_3 respectively.
- When Input *A* is logic *3*, mux M_4 selects input *1* which is obtained from the mux M_3. In mux M_3 inputs are *ground,* F_2, F_4, and F_3 respectively.

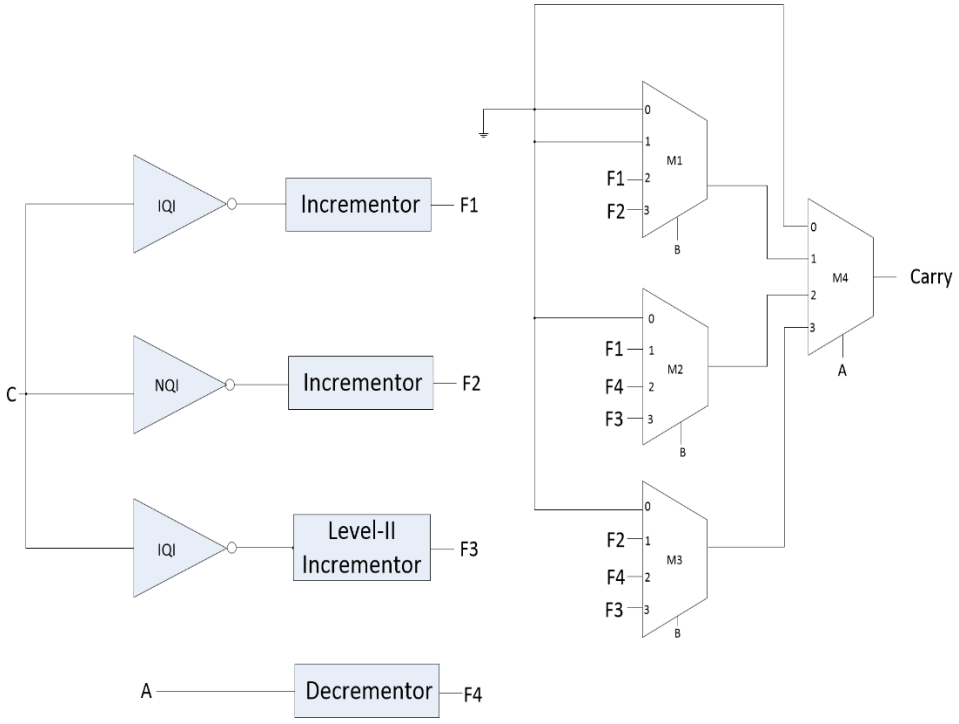


Figure 4.13. CNFET implementation of QM Carry generator circuit

QM Operations explained above can be verified with QFA truth table given in table 4.3 with transient response displayed in figure 4.14. Where In A, In B and In C_in represent input A, input B and input carry respectively, while output product and carry out are represented using Product and C_out.

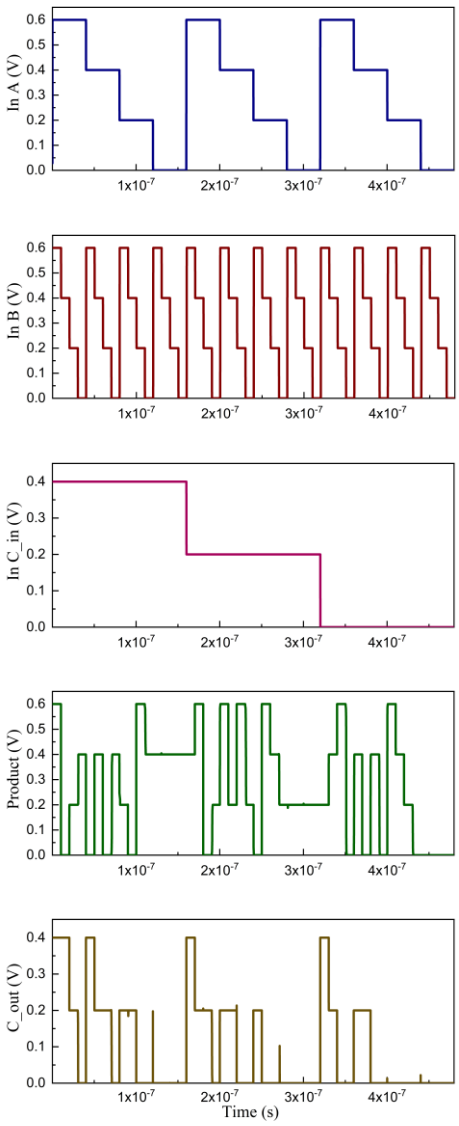


Figure 4.14: Transient response of QM

4.6 Proposed QTL Arithmetic Logic Unit

Figure 4.15 shows the block diagram of QTL ALU. It consists of four 4:1 mux along with QFA and QM. Table 4.4 shows the truth table of the QTL ALU. Proposed QTL ALU implement 17 functions including QFA, QM and QTL logic gates. Input S_2 is used as the select line for mux M_4. The operation of ALU is as follows:

- When S_2 is at logic *0*, the ALU is used as multiplier;
- When S_2 is at logic *1*, the ALU is used to implement QTL inverter function (NQI, IQI, PQI and SQI) based on the value of S_1;
- When S_2 is at logic *2*, the ALU is used to implement QNAND, QNOR, QOR and QNAND based on the value of S_1;

- When S_2 is at logic *3*, the ALU performs addition, subtraction and some special function based on the value of S_1.

Table 4.4: QTL ALU Truth Table

Input(s)			Function
S_2	S_1	C_in	
0	0	X	Multiply the inputs
1	0	X	SQI(A)
1	1	X	NQI(A)
1	2	X	PQI(A)
1	3	X	IQI(A)
2	0	X	QNAND(A,B)
2	1	X	QNOR(A,B)
2	2	X	QOR(A,B) (maximum)
2	3	X	QAND(A,B)(minimum)
3	0	0	Addition of inputs without carry
3	0	1	Addition of inputs with carry
3	1	0	Subtraction of inputs with borrow
3	1	1	Subtraction of inputs without borrow
3	2	0	transfer input A
3	2	1	1 bit Increment Input A (A + 1)
3	3	0	2 bit Increment Input A (A + 2)
3	3	1	3 bit Increment Input A (A + 3)

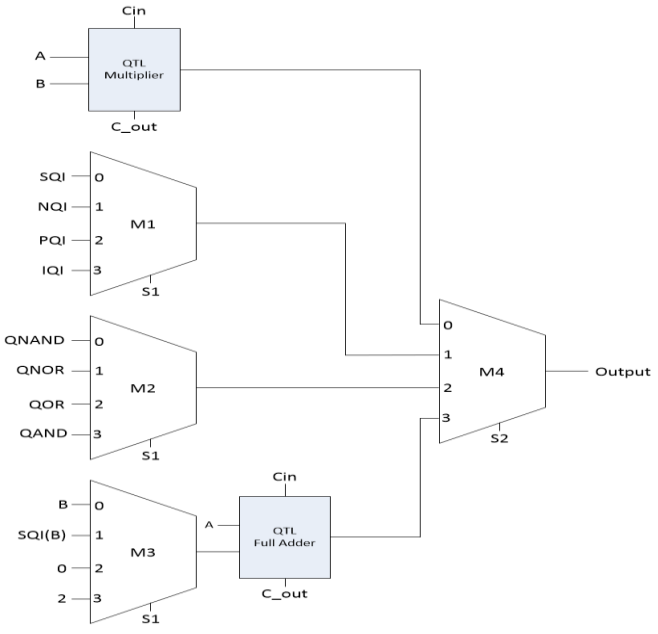


Figure 4.15: Proposed QTL ALU

4.7 Summary

In this chapter, we first implemented the 4:1 and 2:1 mux designs which are further used to implement effective QFA, QM and QTL ALU circuits. The simulation results obtained are compared against the truth table to verify the functionality of each circuit. So this chapter shows a different approach to implement the QTL ALU.

CHAPTER 5

Performance Analysis

5.1 Introduction

In the previous chapter, we proposed different arithmetic and logical blocks for QTL ALU. The implementation and functionality of these blocks were verified by their truth tables and transient responses. The simulations were done using 10nm CNFET model developed by Stanford University on cadence virtuoso. But, only function verification is not enough to conclude that the proposed design is better. So, in this chapter, we have done a performance analysis of the proposed blocks and compared them with the previous works present in the literature.

This chapter is organized in 4 sections out of which section 5.1 gives an introduction followed by section 5.2 in which we have discussed the objectives. In section 5.3 performance analysis for the proposed QFA, QM and QTL ALU design is carried out. Section 5.4 presents a summary of the chapter.

5.2 Objectives

The main objectives of the chapter are as follows:

1. To present the performance analysis for the proposed designs.
2. To compare the proposed designs with existing designs.

5.3 Performance analysis of proposed work

In this report, we have analyzed the proposed QFA, QM and QTL ALU block on the basis of performance parameters namely propagation delay (PD), average power consumption (APC), power delay product (PDP) and energy-delay product (EDP). For calculation of PDP and EDP equation 5.1 and 5.2 respectively are used.

$$PDP = power \times delay \tag{5.1}$$

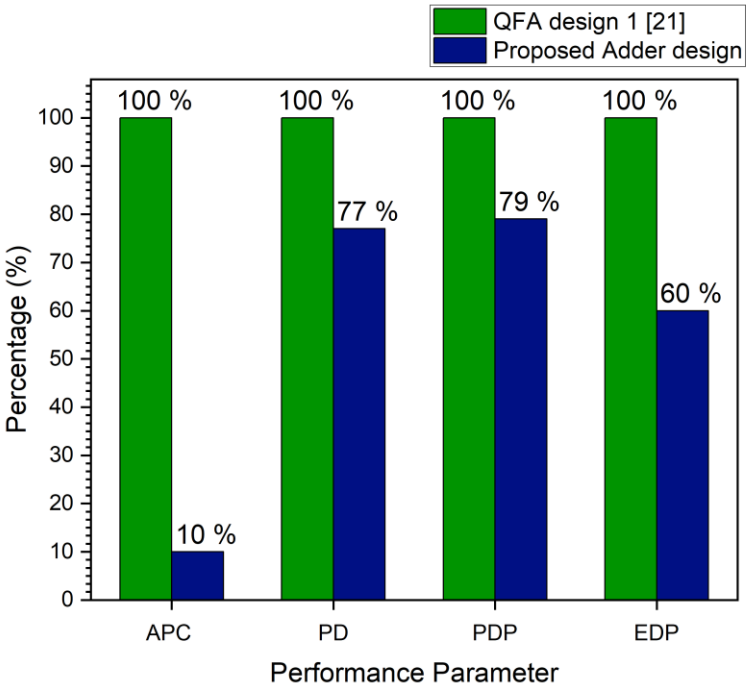
$$EDP = power \times (delay)^2 = PDP \times delay \tag{5.2}$$

Table 5.1 tabulates the performance parameters of the proposed adder blocks and exiting designs [21].

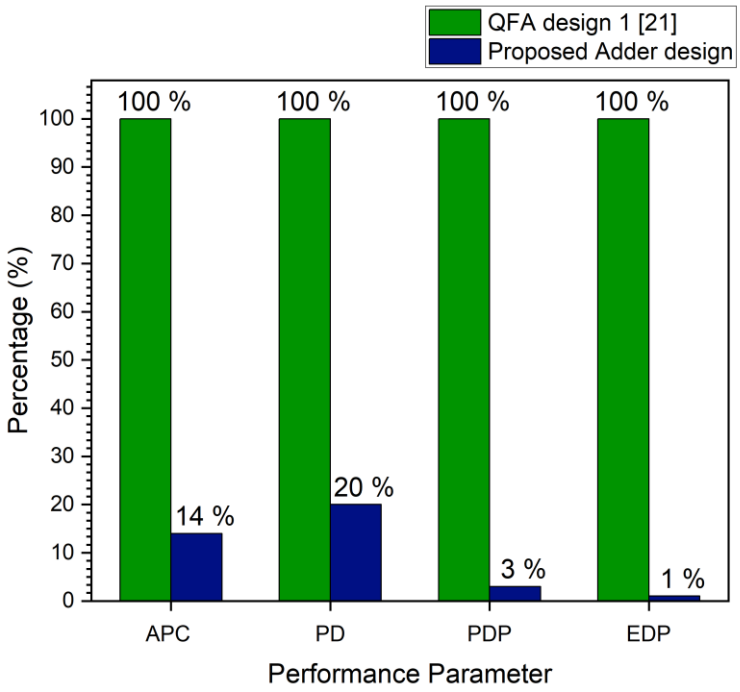
Table 5.1. Performance Analysis for QFA.

Parameter	C-load	Proposed Adder design	QFA design 1 [21]
Average Power Consumption (APC) (uW)	0e-15f	0.0217 (10%)	0.212 (100%)
	2e-15f	0.0589 (14%)	0.453 (100%)
Propagation delay (PD) (ps)	0e-15f	8.458 (77%)	10.92 (100%)
	2e-15f	54.626 (20%)	277.6 (100%)
PDP (e-16 J)	0e-15f	0.001801 (79%)	0.00231 (100%)
	2e-15f	0.03217 (3%)	1.2575 (100%)
EDP (e-28Js)	0e-15f	0.01523286 (60%)	0.02523 (100%)
	2e-15f	1.7573184 (1%)	349.082 (100%)
Power supply Count		1	3

From table 5.1 we can conclude that the proposed QFA design is better than the existing design [21]. Performance parameters (power, delay, PDP and EDP) for proposed QFA design are calculated for two type load conditions C_{load} = 1 fF and C_{load} = 2 fF. The proposed design is ~90% better in terms of power and ~22% (C_{load}= 1fF) & ~80% (C_{load}= 2fF) better in terms of propagation delay than QFA design 1 [21]. Similarly, in the case of PDP and EDP the proposed design is approximately 99% effective than the existing design. Figure 5.1 (a) and (b) depict the comparison between the performance parameters of the proposed QFA with QFA design 1 [21] for C-load 1fF and 2fF (in %).



(a)



(b)

Figure 5.1. Comparison of performance parameters for Proposed QTL Adder with QFA design 1 [21] for C-load (a) 1fF and (b) 2fF (in %)

Table 5.2 tabulates the performance parameters of the proposed QM design for C-load 1fF and 2fF. Figure 5.2 shows the comparison between the performance parameters of the proposed QTL multiplier for C-load 1fF and 2fF.

Table 5.2. Performance Analysis for QM.

Parameter	Proposed multiplier design	
	C-Load = 1fF	C-Load = 2fF
Average Power Consumption (APC) (uW)	0.0664 (70%)	0.0961 (100 %)
Propagation delay (PD) (ps)	10.56 (29%)	36.22 (100 %)
PDP (e-16 J)	0.7011 (21%)	3.4807 (100 %)
EDP (e-28Js)	7.404 (6%)	126.07 (100 %)

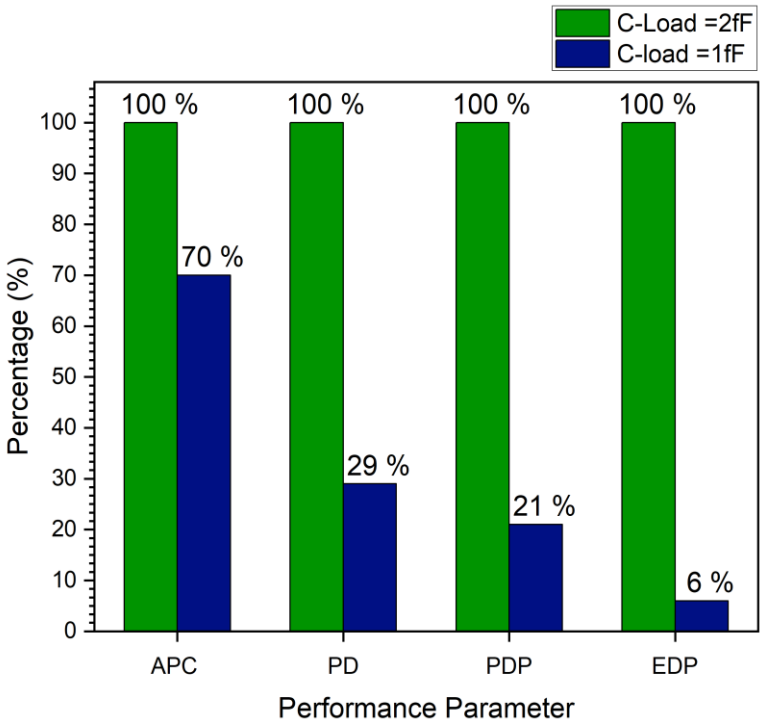


Figure 5.2. Comparison of performance parameters for proposed QTL multiplier for C-load 1fF and 2fF (in %)

Table 5.3 tabulates comparison of the proposed ALU design with the design presented in Sharifi [45]. As given in the table our proposed ALU implements 17 functions which comprise of multiplication, addition, QNAND, QNOR, QOR, QAND, and all four inversion functions. The proposed design is ~99% better in terms of power

and ~91% better in terms of propagation delay than design 1 [45].Similarly, In terms of PDP and EDP the proposed QTL ALU is more than ~99% effective than the existing design. Figure 5.3 depicts the Comparison of performance parameters in percentage of proposed QTL ALU and Design 1 [45] (in %).

Table 5.3. Performance Analysis for QTL ALU

Parameter	Proposed ALU design	Design 1 [45]
Average Power Consumption (APC) (uW)	1.4774 (1%)	164.9 (100%)
Propagation delay (PD) (ps)	35.96 (9%)	435.5 (100%)
PDP (e-16 J)	0.5312 (0.1%)	718.13 (100%)
EDP (e-28Js)	0.00191 (0.01%)	31.27 (100%)
Functions implemented	17	11

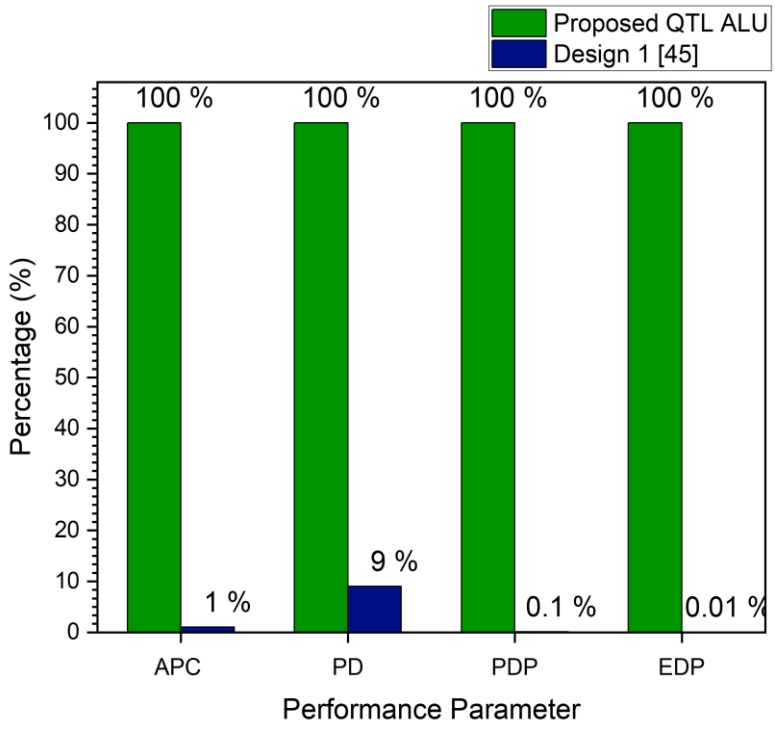


Figure 5.3. Comparison of performance parameters in percentage for proposed QTL ALU and Design 1 [45]

5.4 Summary

In this chapter, We have shown that proposed QTL Adder, QTL multiplier and QTL ALU are 80% - 90% more efficient than the existing designs [21][45] in terms of APC, PD, PDP, and EDP.

CHAPTER 5

Conclusion

The high capacity of CNFET over traditional MOS devices has been advantageous to implement MVL logic. In this thesis, we primarily proposed a design for incrementor, level II incrementor and decrementor using CNFET. Later, the above-mentioned design is used to implement QFA, QM and QTL ALU.

Performance parameters calculated for C-load 1fF & 2fF indicate that the proposed designs of QFA are 90% & 94% efficient in terms of APC, 23 % & 80% better in terms of PD than previous designs respectively. PDP value for the proposed adder design is approximately 21% & 97% less than the previous design. Also, the EDP of the proposed full adder is 40% & 99% better. Moreover, number of power supply required are reduced from 3 to 1. Similarly, the proposed ALU design is ~99% efficient in terms of APC, ~91% efficient in terms of PD along with greater than 99% improvement in PDP and EDP. In addition to this, the number of functions implemented has increased from 11 to 17.

Evaluating the performance parameters under different load conditions suggested that the proposed designs are more than capable to implement arithmetic and logical circuits using QTL.

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