IMPLEMENTATION OF ANALOG SIGNAL PROCESSING CIRCUITS USING DXCCII

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Submitted by:

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2019

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I, (Puneet Singh), Roll No. 2K16/VLS/15 student of M.Tech (VLSI& Embedded systems), hereby declare that the project Dissertation titled "Implementation of Analog Signal Processing circuits using DXCCII" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition

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CERTIFICATE

I hereby certify that the Project Dissertation titled "Implementation of Analog Signal Processing circuits using DXCCII" which is submitted by Puneet Singh, 2k16/vls/15, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Analog signal processing (ASP) is any type of signal processing conducted on continuous analog signals by some analog means as set of continuous values as opposed to the discrete digital Signal Processing (DSP) where the signal processing is carried out by a digital process). DSP suffers of fundamental drawbacks, such as high cost analog-digital conversion, high power consumption and poor performance at high frequencies. To overcome these drawbacks, ASP is preferred.

Current-mode (CM) blocks offer advantages over voltage-mode (VM) blocks, such as performance improvement, low power consumption, controlled gain without feedback components, better linearity and improved bandwidth. This gives the motivation to use CM block to implement various ASP applications and to review already existing literatures available using CM blocks. Current conveyor is used as it is a high-performance active element and it ensures high accuracy, wide bandwidth and exceptionally high slew rates combined with low voltage and low power implementations under small or large signal conditions. As compared to op-amp based circuits, the conveyor-based circuits offer a higher gain-bandwidth product, which makes it an ideal choice for modern applications in analog signal processing. Dual-X second-generation current conveyor (DXCCII) is one of the new emerging CM block. In the process, a DXCCII is used which is a modified second-generation current conveyor that provides an extra input terminal. The block DXCCII and its applications have been verified.

The new topology Current amplifier, Voltage amplifier, Trans-resistance amplifier, Trans-conductance Amplifier, Voltage-mode digitally controlled variable gain amplifier (VGA) and current-mode digitally controlled variable gain amplifier (VGA) are proposed and analyzed. To achieve the required gain control range and step, two VGA stages are cascaded. The first stage is coarse gain control while the second stage is fine gain control. The variable gain amplifier (VGA) circuit is thus operating in a coarse and fine arrangement.

The novice DXCCII based Programmable Gain Amplifier are proposed and analyzed. It operates in trans-impedance mode i.e. it receives current signal as input and provides voltage as output. It uses four blocks – a current amplifier, digitally controlled trans-impedance amplifier, digitally controlled R-2R ladder network and a voltage buffer. First block amplifies input signals. Second and third blocks of proposed PGA provide control over coarse gain and fine gain through bits ($B_5 - B_0$) and a total of 60 different gain values are possible through the arrangement. The last block provides output at low impedance.

Another application as a Current-mode all-pass filter using a single dual-X second-generation current conveyor (DXCCII) is proposed. The proposed circuit has grounded capacitors and resistors, which is good for IC implementation. The functionality of the proposed circuits is analyzed through SPICE simulation using 0.18μm TSMC technology parameters.

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LIST OF ABBREVIATIONS AND SYMBOLS

ASP	:	Analog Signal Processing
DSP	:	Digital Signal Processing
CM	:	Current Mode
VM	:	Voltage Mode
CC	:	Current Conveyor
CCI	:	First generation current conveyor
CCII	:	Second generation current conveyor
CCIII	:	Third generation current conveyor
DXCCII	:	Dual-X second-generation current conveyor
EXCCII	:	Extra-X second generation current conveyor
VGA	:	Variable gain amplifier
OTA	:	Operational trans-conductance amplifier
CMOS	:	Complementary MOSFET
PGA	:	Programmable gain amplifier
AGC	:	Automatic gain amplifier

CHAPTER 1

1.1 Introduction

The present work manages dual-X second-generation current conveyor (DXCCII) and its application in signal processing. There had been a few noteworthy advancements in the region of analog circuits and signal processing which have occurred during the previous four decades. There is a main part of material accessible about the different dynamic blocks created post Current Conveyors. In this thesis, an endeavor has been made to feature some of the essential circuits and double X current conveyor-II based applications in analog signal processing.

Presentation of Current Conveyor was essential as a result of constraints presented by the conventional Operational amplifier, which is an exceptionally adaptable component [1]. With operation amps numerous circuits, both straight and non-direct, can be acknowledged effectively. Broad research had been done from mid-sixties to mid-eighties on the plan of different direct and non-straight simple circuits utilizing coordinated circuit (IC) operation amps. Since operation amp based circuits utilize RC components, their solid IC usage was troublesome on the grounds that exact tuning of the time consistent RC was hard to execute. Additionally, their constrained exhibition because of less data transmission, slew rate and so on constrained the simple originators to search for other dynamic squares [2]. Exchanged capacitor circuits were one arrangement where the resistor was supplanted by an intermittently exchanged capacitor however it again presented issues like associating and clock feed through [3].

In the eighties, Operational Trans-admittance Amplifiers (OTA) was presented. The OTA-C circuits utilize just trans-conductors and capacitors to manufacture different utilitarian circuits and in this way, don't require any resistors; in addition, there inside structure is likewise resistor-less, accordingly adding furthering its potential benefit list. In OTA circuits the trans-conductance can be controlled electronically through an outside DC predisposition voltage/current making its increase variable (programmable).

The improvements in digital circuit structure especially, CMOS digital circuits have impacted the advancements in analog circuits especially in those situations where both digital and analog parts are to be incorporated in a similar chip utilizing a similar innovation (CMOS). Despite the fact that the digital frameworks have numerous preferences over the analog sort the last can't, in any case, be stayed away from, as the regular world is analog. The different advancements in the field of integrated circuit (IC) innovation, once more, presented different difficulties to analog architects to coordinate the analog framework with their quickly developing computerized partners. It is such prerequisites that have brought about proceeded with research on proficient simple circuit plans particularly ebb and current mode (CM) methods and circuits for advancement of rich and effective answers for some contemporary issues in blended mode circuit structure issues. The present mode way to deal with signal processing is frequently considered to have at least one of the accompanying preferences: higher recurrence scope of activity, lower control utilization, higher slew rates, improved linearity and better precision. Before depicting the advancements in analog signal processing and circuit plans we will initially examine a portion of the fundamentals of signal processing.

1.2 Analog and Digital signal processing

Signal processing finds numerous applications in correspondence frameworks, biomedical designing, instrumentation, control frameworks, and so on can be executed in two unique ways:

1. Continuous (analog) strategy.

2. Discrete (digital) strategy.

The analog strategy to signal processing was overseeing for a long time. This uses simple circuit components, for instance, capacitors, resistors, diodes, transistors, and so on. Analog signal processing (ASP) depends on the normal capacity of analog frameworks to comprehend the differential conditions that characterize a physical framework; the arrangements are acquired progressively. Conversely, digital signal processing (DSP) relies

upon numerical counts, this could possibly influence progressively. DSP experiences huge disadvantages, for example, mind-boggling expense A/D (analog/digital) change, terrible showing at high frequencies and high power utilization. To conquer these disadvantages, ASP is liked.

The current conveyor is utilized, as it is a superior dynamic component and it guarantees high precision, surprisingly high slew rates aggregate with low power and low voltage executions under little or enormous sign conditions and wide transmission capacity. As identified with operation amp based circuits, the transport based circuits offer a higher addition transmission capacity item which settles on it a perfect decision for current applications in analog signal processing (ASP).

1.3 Current–mode and Voltage–mode

Voltage-mode (VM) can be characterized as when signals, portrays the data being handled, are as electric voltages. Rather than current mode (CM), which utilizes electric flows. In VM circuits the exhibition can be assessed as far as voltage levels at a few hubs including input and output hubs. The real downsides in the circuits which use VM are increased subordinate transfer speed, an expansion in the estimation of parasitic capacitances at the output hubs subsequently making a predominant post at low recurrence which impacts generally speaking circuit execution and slew rate. In this manner, it isn't reasonable for ASP applications where higher output swings, less power utilization, wide transmission capacity and speed of the circuit are fundamental for predominant circuit exhibitions. In this way, there is a need for an elective system to beat these weaknesses.

As of late, CM procedure has set off the analyst's consideration because of its ascribed highlights like effortlessness in absorbing in parasitic capacitances, less power utilization, higher output swings, basic plan/condition requirements, more extensive transmission capacity, better linearity and higher increase free of data transmission [4-6]. Because of current signal processing CM topologies to have low impedance hubs subsequently by accomplishing low time constants, which improve by and large framework execution with

respect to speed and slew rate. Besides, in current enhancers the transistors can be misused nearly up to their solidarity gain data transfer capacity, so bringing about a more extensive transmission capacity. Moreover, in CM circuits different activities, for example, expansion and subtraction can be gotten by basically associating the terminals at a solitary point bringing about uncomplicated design when contrasted with VM circuits. This outcome in a decrease in power utilization and generally speaking chip region, which is appropriate for present-day IC usage.

This gives the inspiration to utilize CM block to actualize different ASP applications. Writing overview recommends that there are various CM hinders that are as of now accessible. The subtleties of some CM block are recorded beneath.

The current conveyor (CC) [8], a voltage and current hybrid circuit, is the most broadly investigated block. The original of CC (CCI) [7], second-generation CC (CCII) [7], and third era CC (CCIII) [9] are diverse as far as port qualities and were displayed in 1968, 1970 and 1995 individually. And furthermore current criticism speaker (CFA) [10], four Terminal floating nullor (FTFN) [11], and so forth. The assortment of adjustments in the fundamental conveyor structure, for progressively compelling activity, prompted the presentation of different CC based fresher components [12] – [26]. As of late, the second-generation current conveyor was additionally stretched out to the Dual-X current conveyor-II (DXCCII) [26]. The usefulness of the proposed circuits is examined through SPICE simulation utilizing 0.18μm TSMC innovation parameters. Section 2 depicts the device characteristics of DXCCII.

CHAPTER 2

2.1 Dual-X Current Conveyor-II (DXCCII)

The DXCCII is a blend of ordinary CCII and ICCII. Like other current modes active device, the DXCCII has favorable circumstances, for example, higher usable gain, increasingly diminished voltage trip at its delicate hubs, more noteworthy linearity, less power dissipation, wider bandwidth, better accuracy and bigger dynamic range over its voltage mode counterpart [26].

2.2 CMOS implementation of DXCCII

The DXCCII is a five-port building block, which is defined by the following matrix equation:

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (2.1)$$

Where,

V_Y = Voltage at Y port

V_{X+} = Voltage at X+ port

V_{X-} = Voltage at X- port

I_Y = Current at Y port

I_{Z+} = Current at Z+ port

I_{Z-} = Current at Z- port

I_{X+} = Current at X+ port

I_{X-} = Current at X- port

The symbol of DXCCII is shown in Fig.2.1 show that the DXCCII has several ports as follows:

- One high input impedances Voltage input port Y
- Two low impedance current input ports X+, X-
- Two high impedance current output ports Z+, Z-

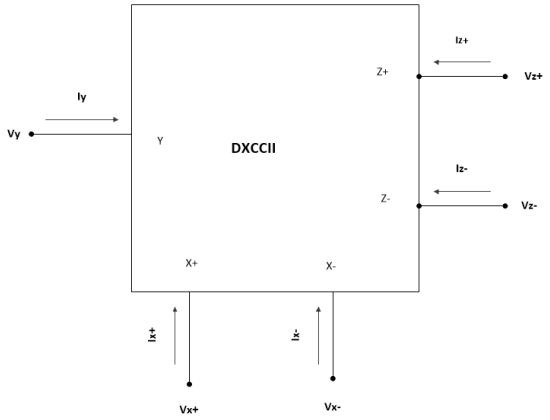

Fig. 2.1 Symbol of DXCCII

CMOS implementation of DXCCII is shown in Fig. 2.2

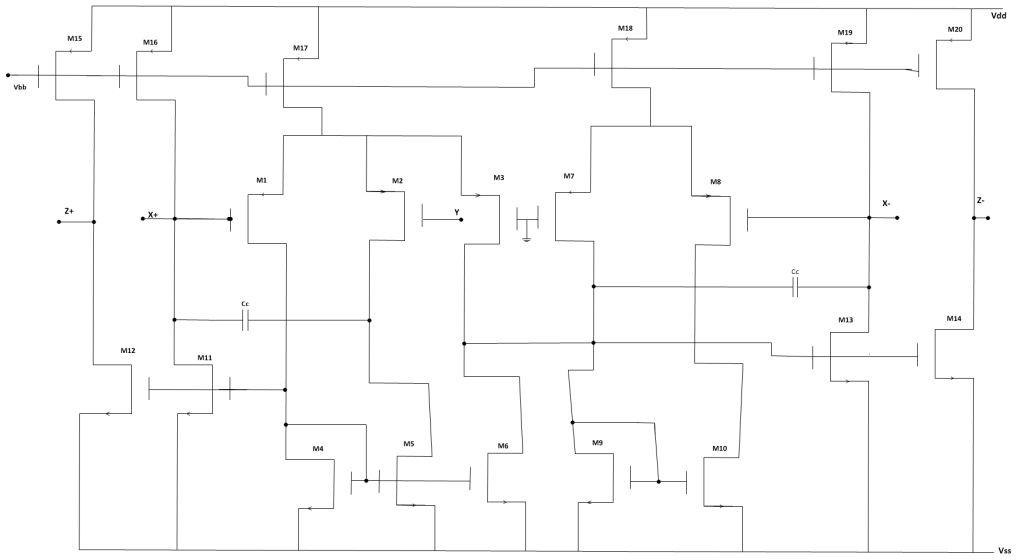

Fig. 2.2 CMOS implementation of DXCCII [26]

The differential pairs M1-M2 and M7-M8, together with transistors M11 and M13 construct active feedback loops, which provide low input impedance at ports X+ and X-, respectively. Since the differential pairs are biased with the drain currents of the PMOS transistors M17 and M18 (controlled with bias voltage V_{BB}), one can increase the bias currents (by decreasing V_{BB}) to improve the linearity of the DXCCII. However, this results in more power consumption. The transistor M3 together with M7, M8, and M13 are involved in a voltage inverting mechanism which inverts the voltage of port Y to port X-. Further, the transistor M12 and M14 are employed to transfer the X+ and X- port currents to Z+ and Z- ports, respectively.

2.3 Non-ideal analysis

Consider the non-idealities effects of the DXCCII, the link of the port voltages and currents of the DXCCII can be written as

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_{k1} & 0 & 0 \\ 0 & 0 & -\beta_{k2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_{k1} & 0 & 0 & 0 & 0 \\ 0 & \alpha_{k2} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{2.2}$$

Where, β_{k1}(s) and β_{k2}(s) represent the frequency transfers of the internal voltage followers and α_{k1}(s) and α_{k2}(s) represent the frequency transfers of the internal current followers of the K_{th}-DXCCII, respectively. If DXCCII is working at frequencies much less than the corner frequencies of β_{k1}(s), β_{k2}(s), α_{k1}(s) and α_{k2}(s), namely, then β_{k1}(s) = β_{k1}=1-ε_{kv1} where, ε_{kv1}($|\varepsilon_{kv1}|$ <<1) is the voltage tracking error from the Y terminal to the X+ terminal of the K_{th}-DXCCII; β_{k2}(s) = β_{k2}=1-ε_{kv2} where, ε_{kv2}($|\varepsilon_{kv2}|$ <<1) is the voltage tracking error from the Y terminal to the X- terminal of the K_{th}-DXCCII; then α_{k1}(s) = α_{k1}=1-ε_{ki1} where, ε_{ki1}($|\varepsilon_{ki1}|$ <<1) denotes the current tracking error from the X+ terminal to the Z+ terminal and α_{k2}(s) = α_{k2}=1-ε_{ki2} where, ε_{ki2}($|\varepsilon_{ki2}|$ <<1) is the current tracking error from the X- terminal to the Z- terminal of the K_{th}-DXCCII.

2.4 Parasitic effects

The parasitic model of DXCCII is shown in fig. 2.3. It is shown that the real DXCCII has parasitic resistors and capacitor at port Z in the form of $R_Z||C_Z$, at port Y in the form of $R_y||C_y$ and at port X parasitic are in form of series combination of resistance R_X and capacitor C_X. Ideally, the DXCCII is used at frequencies much lower than the corner frequencies of α_i (i=1,2) and β_i (i=1,2). For typical applications built around DXCCII, the external resistors (R) are much smaller than the parasitic resistors at the Y and Z terminals of DXCCII, i.e. R<<R_Y or R_Z and the external resistors are much greater than the parasitic resistors at the X terminals of DXCCII, i.e. R_X<<R.

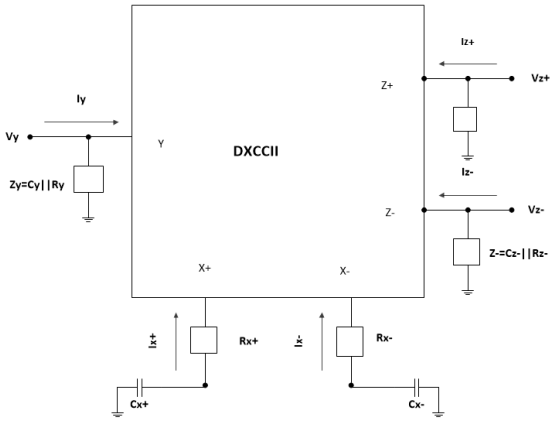

Fig. 2.3 Parasitic model of DXCCII

2.5 Simulation results

The usefulness of the proposed circuits is examined through SPICE simulation utilizing 0.18µm TSMC innovation parameters**.** The MOS transistors are simulated utilizing 0.18μm TSMC innovation parameter. The supply voltages and biasing voltage are given by V_{DD} = $-V_{SS}$ = 2.5V and V_{BB} = -1.6V, respectively and C_C = 0.06pF.

Table 2.1 Size of MOS (Metal oxide semiconductor) transistors used for simulation

Transistors	Width(μm) / Length(μm)
M1, M2, M4, M5, M15-20	1.44 / 0.18
M3, M6-10	2.88 / 0.18
M11-14	11.51 / 0.18

2.6 DC analysis

DC analysis has been done to validate the current and voltage links separately. Fig. 2.4 to fig. 2.7 shows the DC characteristic of DXCCII. Fig. 2.4 shows that when 20mV is applied at input terminal Y then DC voltage 20mV is available at terminal X+ and DC voltage of -10mV is available at X-. In this way, the relationship of voltage equation (2.1) is verified.

Fig. 2.5 shows the difference at X+ terminal (V_{X+}) and X- terminal (V_{X-}) against the input voltage at Y terminal (V_Y). Fig. 2.5 proves that equation (2.1) is correct. It is obtained by varying V_Y from - 1V to +1V and is shown in Fig. 2.5 shows linearity range of voltages at X+ terminal (V_{X+}) and X- terminal (V_{X-}) against the input voltage (V_Y).

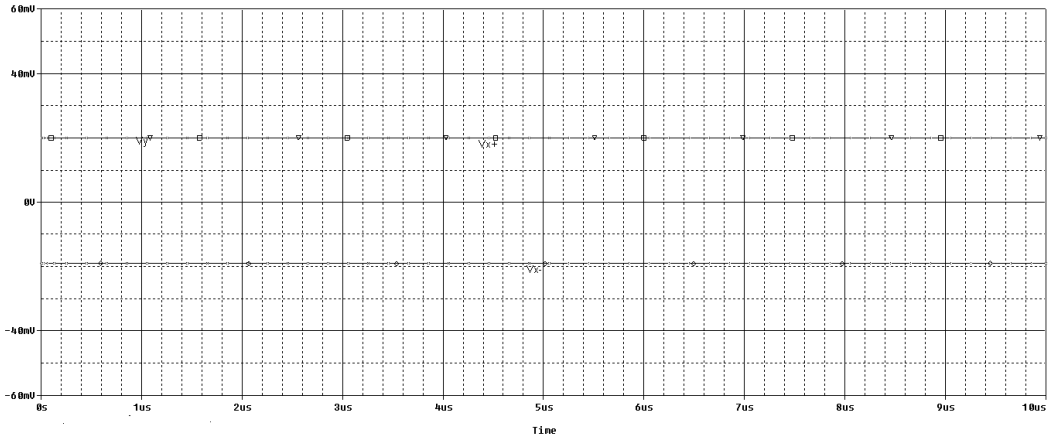

Fig. 2.4 Verification of input voltages (V_{X+}=$+V_Y$ and V_{X+}=$-V_Y$)

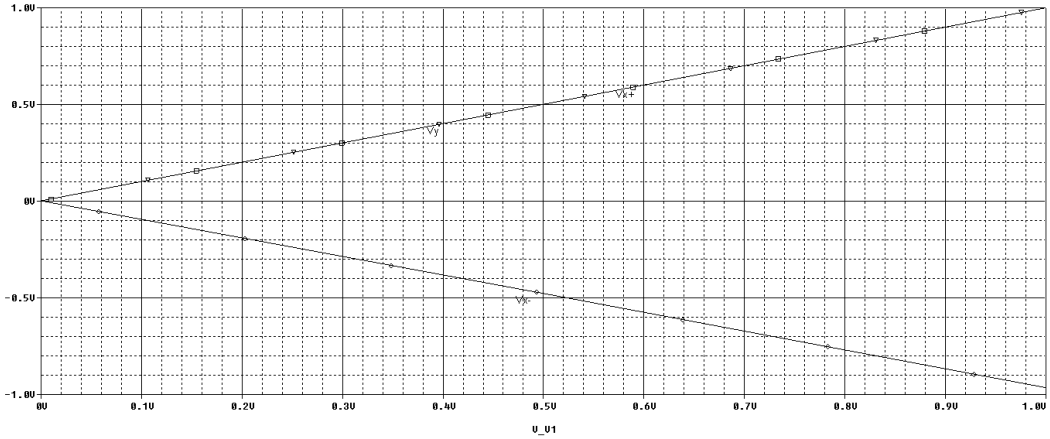

Fig. 2.5 Verification of X+ and X- port voltages (V_{X+} and V_{X-}) against input voltage V_Y)

Fig. 2.6 and Fig. 2.7 show the variations in output current at terminal Z+ (I_{Z+}) and output current at terminal Z- (I_{Z-}) with respect to the current at X terminal (I_X), respectively. These responses of output currents show good linearity. Fig. 2.6 and Fig. 2.7 also verify the current relationships of equation (2.1).

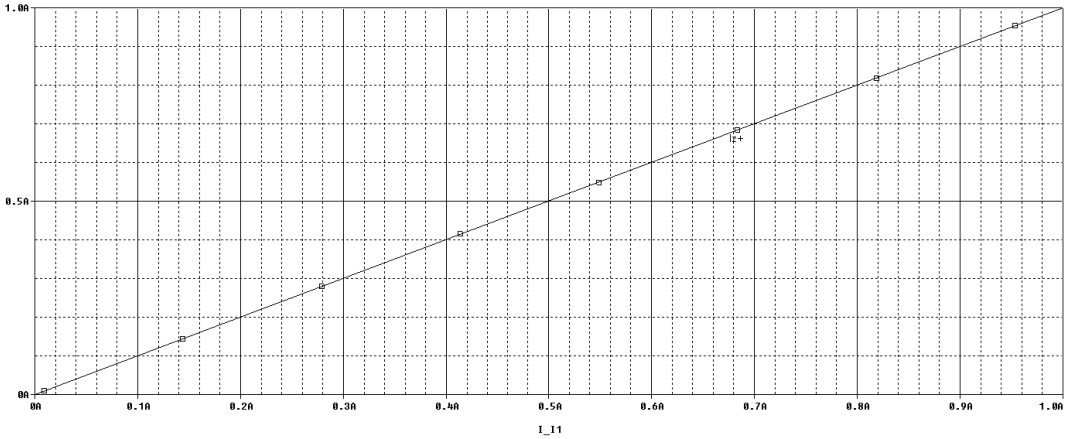

Fig. 2.6 Verification of output current at Z+ port (I_{Z+}) against input current at X+ port (I_{X+})

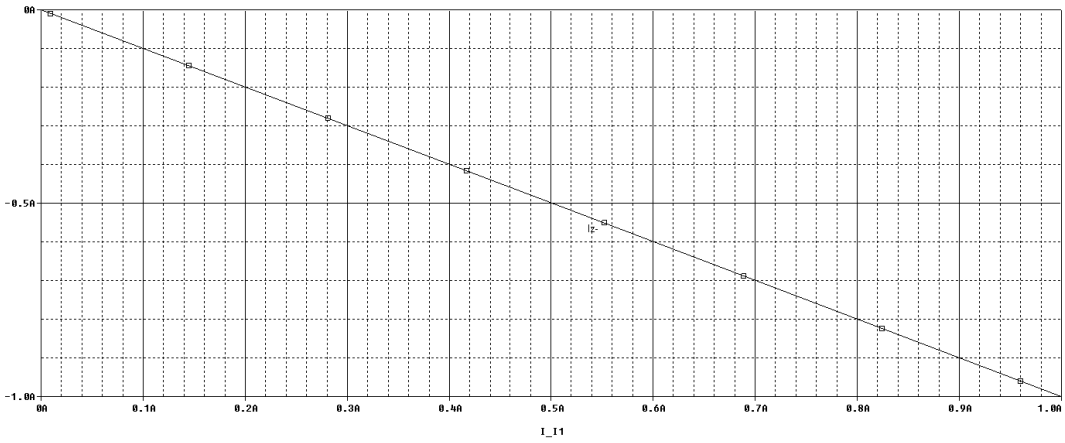

Fig. 2.7 Verification of output current at Z- port (I_{Z-}) against input current at X- port (I_{X-})

2.7 AC analysis

AC analysis also done by applying AC input signal at the input terminal of DXCCII. Frequency responses are shown in Figure 2.8 to Figure 2.10. Fig. 2.8 verifies the voltage relationships of equation (2.1) in frequency domain. Fig. 2.9 and Fig. 2.10 verify the current relationships of equation (2.1) in frequency domain. These responses also show the range of frequency suitable for operation. Fig. 2.8 to Fig. 2.10 clearly indicates that voltage and current relationships are accurate up to 10MHz.

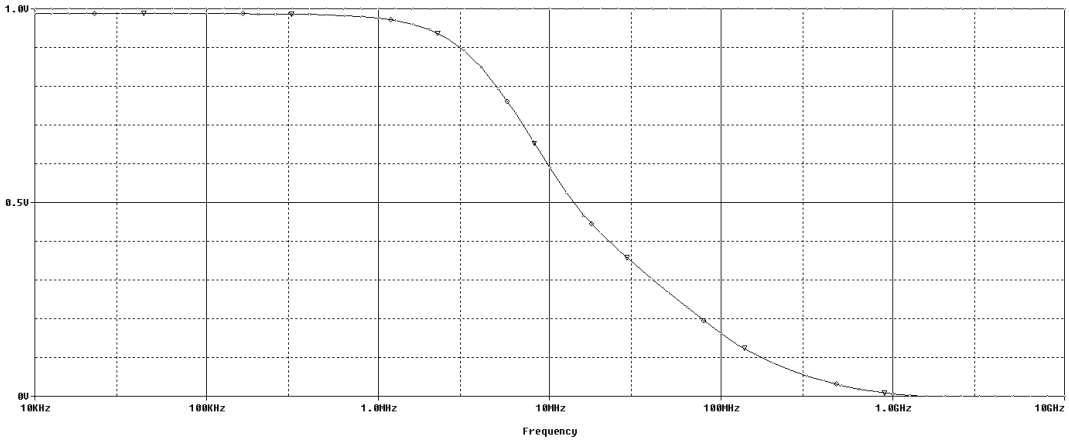

Fig. 2.8 Verification of Voltages in frequency domain

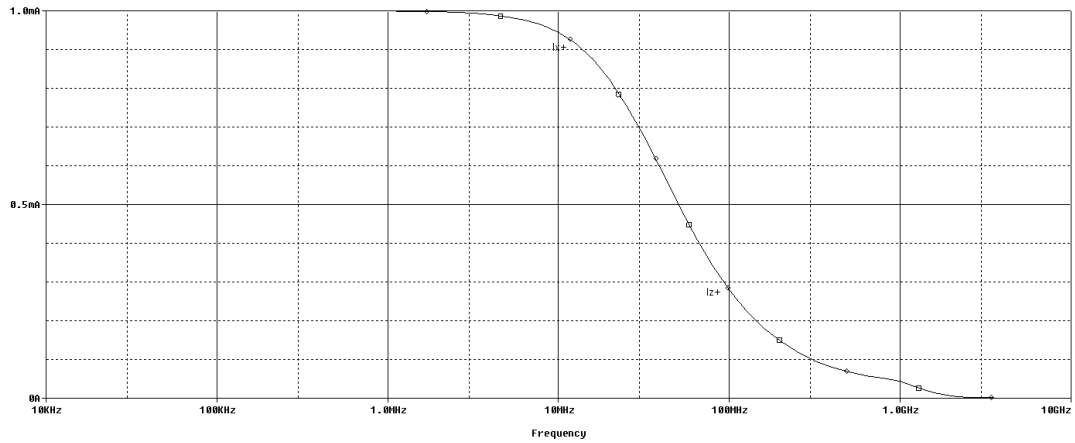

Fig. 2.9 Verification of Currents (I_{Z+} and I_{X+}) in frequency domain

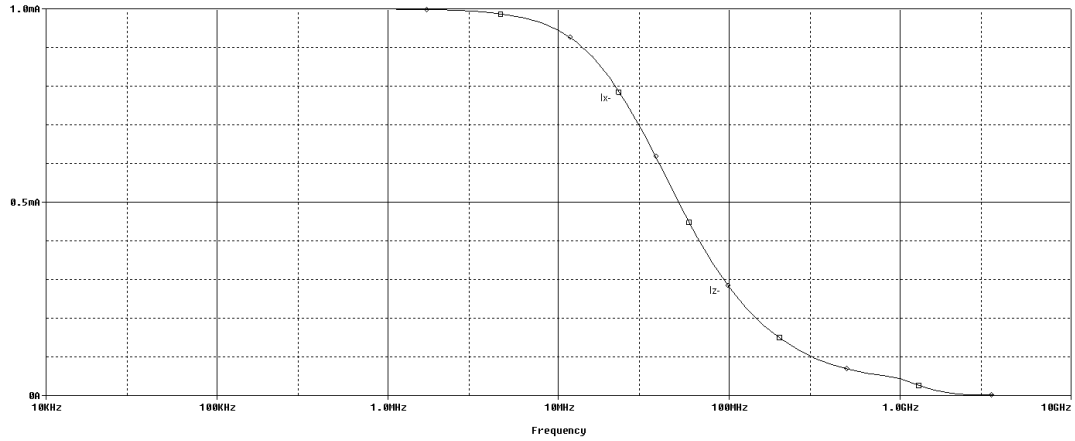

Fig. 2.10 Verification of Currents (I_{Z-} and I_{X-}) in frequency domain

Fig. 2.11 and Fig. 2.12 show the voltage gain in dB. These responses of voltage gain also show that the bandwidth of DXCCII is around 100MHz.

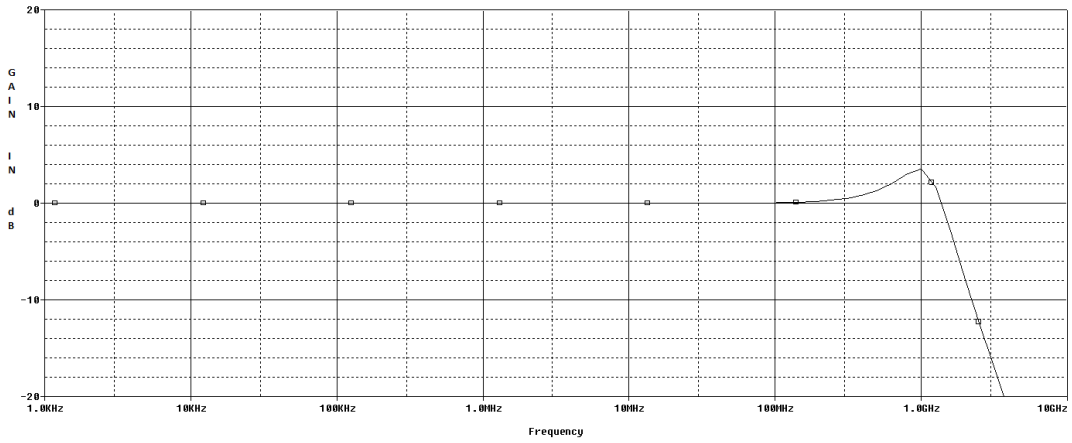

Fig. 2.11 Verification of Voltage gain (V_{X+} / V_Y) IN dB

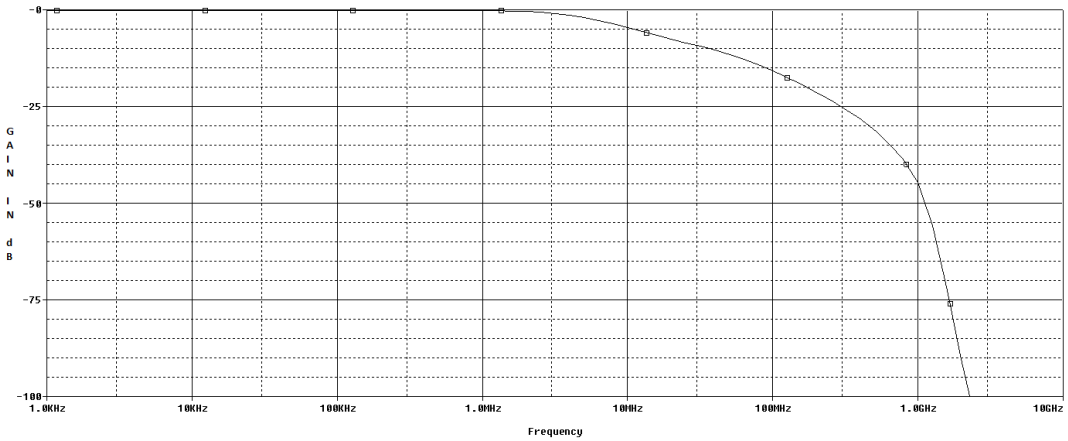

Fig. 2.12 Verification of Voltage gain (V_{X-} / V_Y) in dB

Fig. 2.13 and Fig. 2.14 show the positive current gain and negative current gain in dB, respectively. These responses show the good bandwidth range of DXCCII.

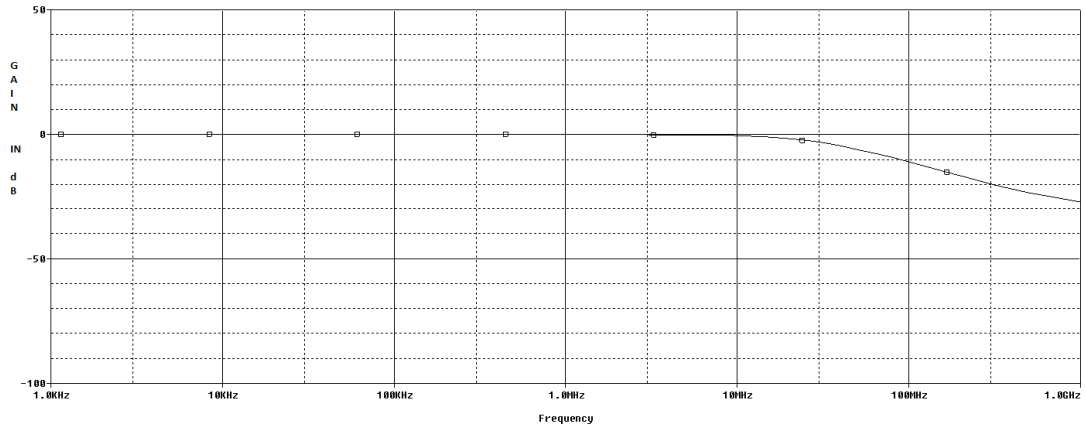

Fig. 2.13 Validation of Current gain (I_{Z+} / I_{X+}) in dB

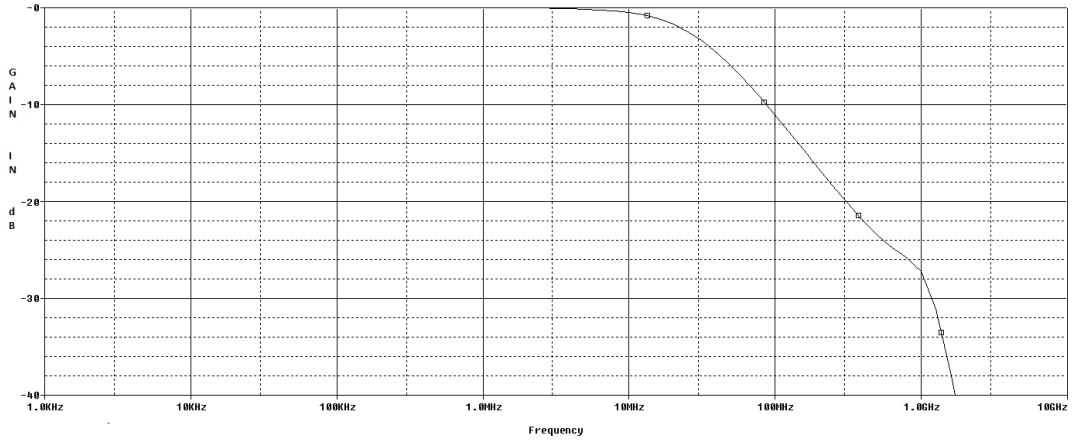

Fig. 2.14 Validation Current gain (I_{Z-} / I_{X-}) in dB

2.8 Transient analysis

PSPICE simulation is also carried out for sinusoidal input. These results also give a good agreement between expected and simulated results. These results also verify the basic equations for DXCCII in time domain and are shown in Fig. 2.15 to Fig. 2.17.

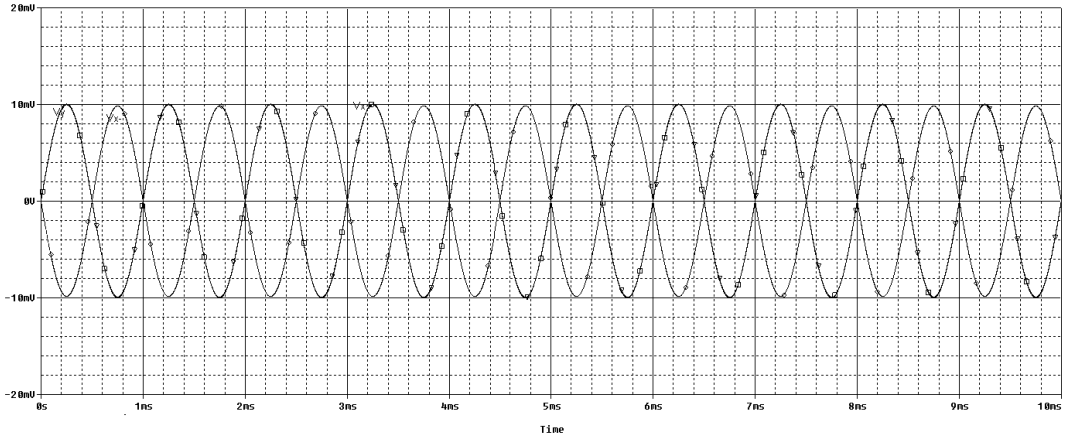

Fig. 2.15 Verification Input/output voltages at Y, X+, X- ports

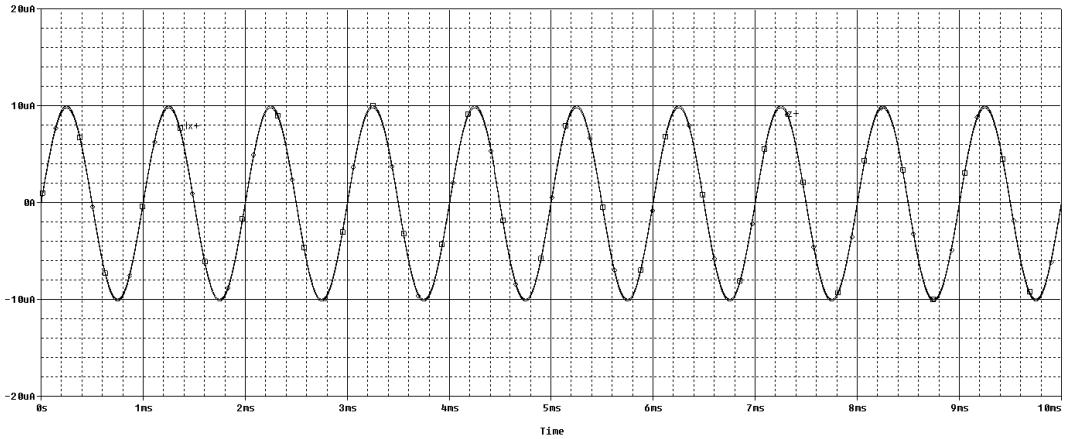

Fig. 2.16 Verification of Input/output current at X+ and Z+ ports

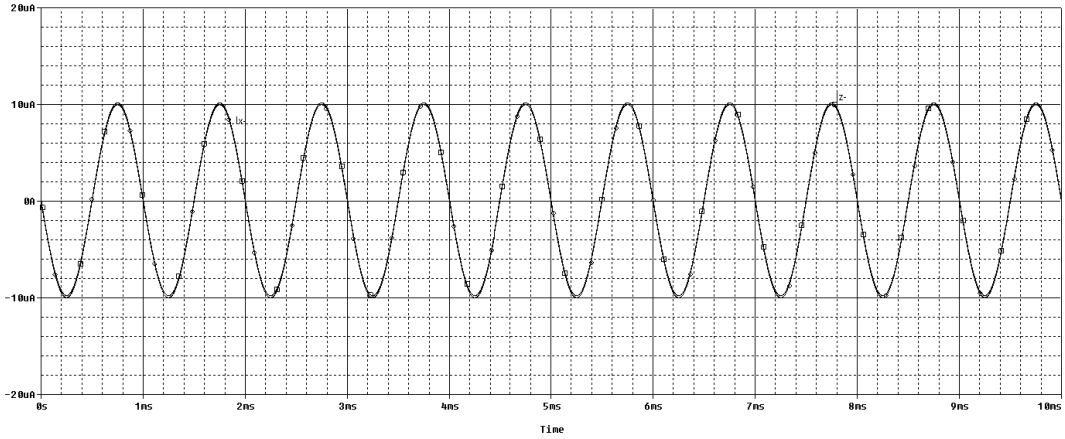

Fig. 2.17 Verification of Input/output current at X- and Z- ports

CHAPTER 3

3.1 Amplifiers

An amplifier, electronic amplifier or (casually) amp is an electronic device that can build the intensity of a signal (a period shifting voltage or current). It is a two-port electronic circuit that utilizations electric power from a power supply to build the adequacy of a signal connected to its information terminals, creating a relatively more prominent sufficiency signal at its output. The measure of enhancement given by an amplifier is estimated by its increase: the proportion of output voltage, current, or capacity to include. A amplifier is a circuit that has a power increase more noteworthy than one.

An amplifier can either be a different bit of hardware or an electrical circuit contained inside another device. Amplifier is crucial to present-day devices, and enhancers are generally utilized in practically all-electronic gear. Enhancers can be classified in various ways. One is by the recurrence of the electronic signal is enhanced. The principal useful electrical device, which could intensify, was the triode vacuum tube, developed in 1906 by Lee De woods, which prompted the main enhancers around 1912. Today most amplifier use transistors.

In this chapter novice voltage amplifier, current amplifier, trans-impedance amplifier, trans-admittance amplifier utilizing single DXCCII is proposed which utilized less number of detached segments (resistors).

3.2 Proposed current amplifier

A current amplifier is an electronic circuit that builds the extent of current of information signals by a fixed various, and nourishes it to the succeeding circuit. This procedure is named as current enhancement of an info signal.

The gain of a current amplifier is the proportion between the sizes of current coursing through its output terminals, to the extent of a current of the information signal. It is signified by the symbol Ai.

Current gain $(A_i) = \frac{Output\ Current}{Input\ current}$

The proposed current amplifier configuration is shown in Figure 3.1

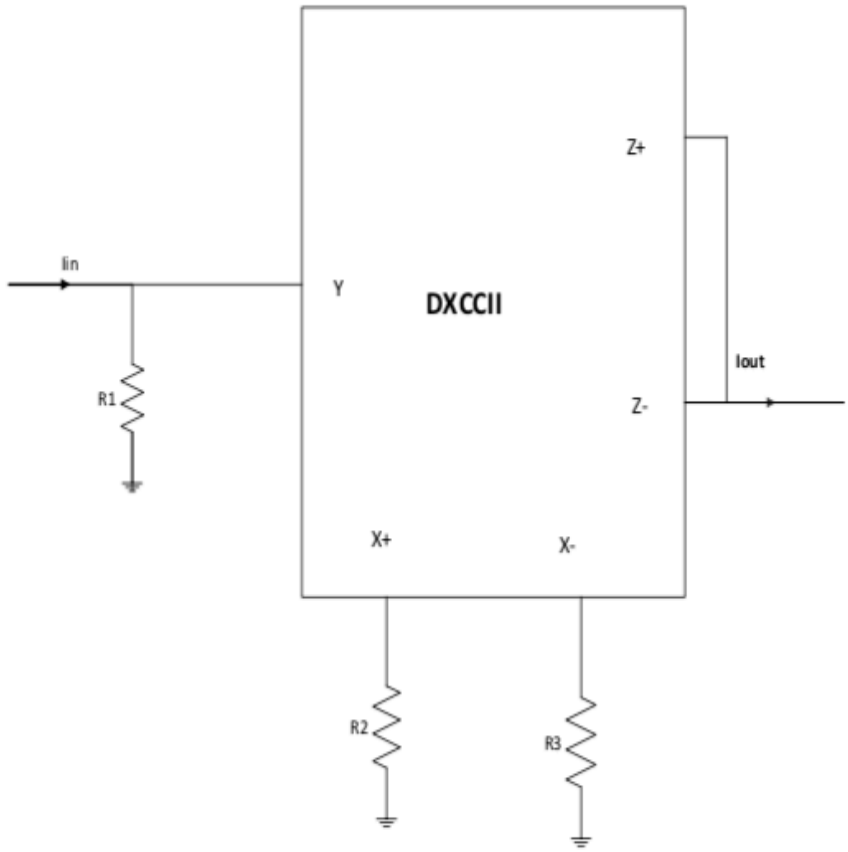

Fig. 3.1 Current amplifier configuration using DXCCII

From the port matrix of DXCCII, we get

$V_Y = V_{X+} = -V_{X-}$

$I_Y = 0$

$I_{X+} = I_{Z+}$

$I_{X-} = I_{Z-}$ 3.1

From circuit analysis, the following Current-mode Transfer function is obtained:

$$I_{out} = R_1 I_{in} \left(\frac{1}{R_2} - \frac{1}{R_3}\right) \quad 3.2$$

$$\frac{I_{out}}{I_{in}} = \frac{R_1(R_3 - R_2)}{R_2.R_3} \quad 3.3$$

The current gain can be acquired as:

$$Current\ gain\ (A_I) = \frac{R_1(R_3 - R_2)}{R_2.R_3} \quad 3.4$$

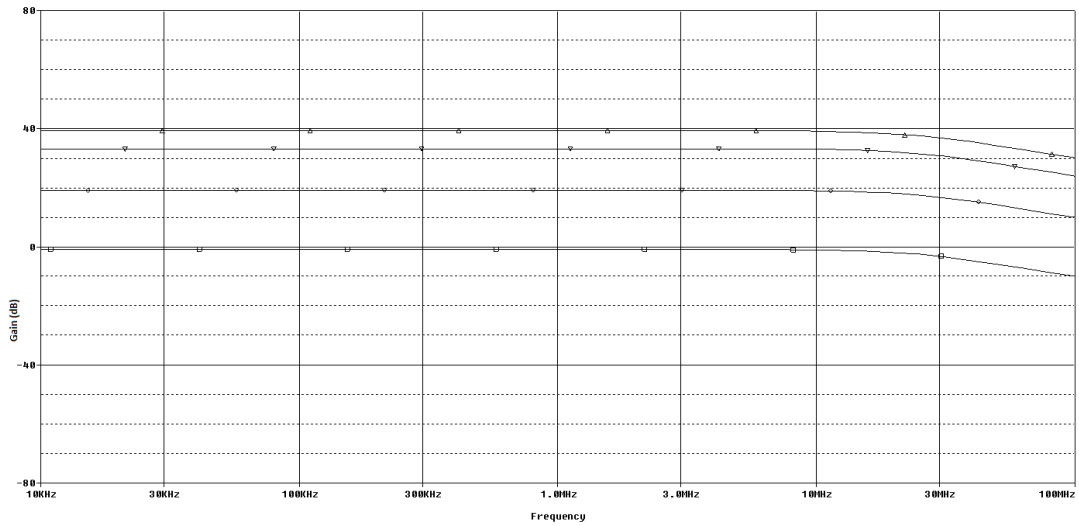

Fig. 3.2 Frequency characteristics of the current gain of the current amplifier configuration as shown in Fig. 3.1

The proposed circuit is simulated utilizing $R_2 = 0.5k\Omega$, $R_3 = 1k\Omega$, $R_1 = 1k\Omega, 10k\Omega, 50k\Omega, 100k\Omega$. The different gains of current amplifier are shown in figure 3.2.

3.3 Proposed Voltage amplifier

A voltage amplifier is an electronic circuit that builds the extent of a voltage of an information signal by a fixed different and nourishes it to the succeeding circuit. This procedure is named as a voltage amplification of an input signal.

The gain of a voltage amplifier is the proportion between the sizes of voltage coursing through its output terminals, to the greatness of voltage of the information signal. It is meant by the symbol Av.

Voltage gain $(A_v) = \frac{Output\ Voltage}{Input\ Voltage}$

The proposed voltage amplifier configuration is shown in Fig. 3.3

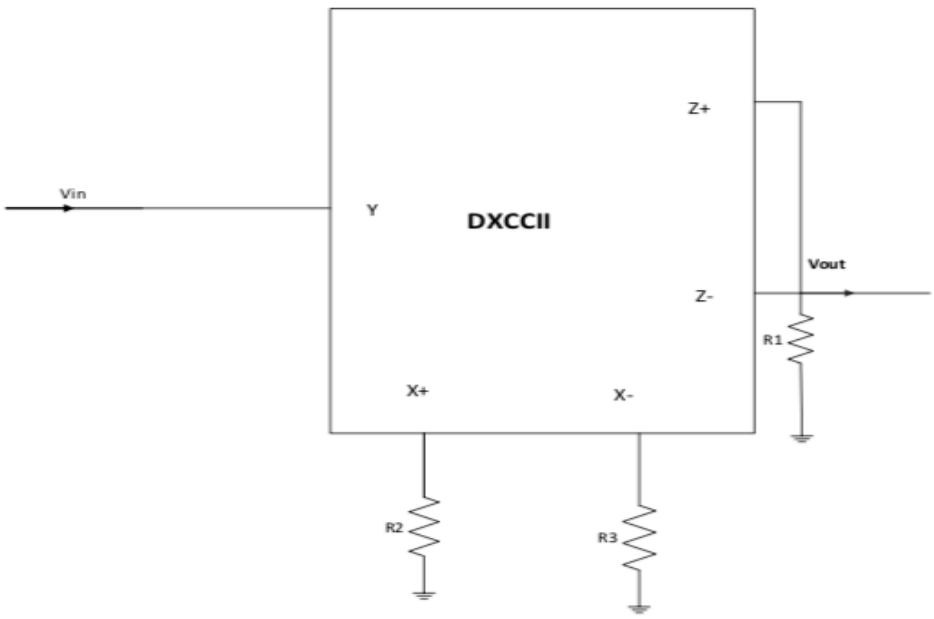

Fig. 3.3 Voltage amplifier configuration using DXCCII

From the port matrix of DXCCII, we get

$V_Y = V_{X+} = -V_{X-}$

$I_Y = 0$

$I_{X+} = I_{Z+}$

$I_{X-} = I_{Z-}$ 3.4

From circuit analysis, the following Voltage-mode Transfer function is obtained:

$$V_{out} = R_1 V_{in} \left(\frac{1}{R_2} - \frac{1}{R_3}\right) \quad 3.5$$

$$\frac{V_{out}}{V_{in}} = \frac{R_1(R_3 - R_2)}{R_2.R_3} \quad 3.6$$

The voltage gain can be acquired as:

$$Voltage\ gain\ (A_V) = \frac{R_1(R_3 - R_2)}{R_2.R_3} \quad 3.7$$

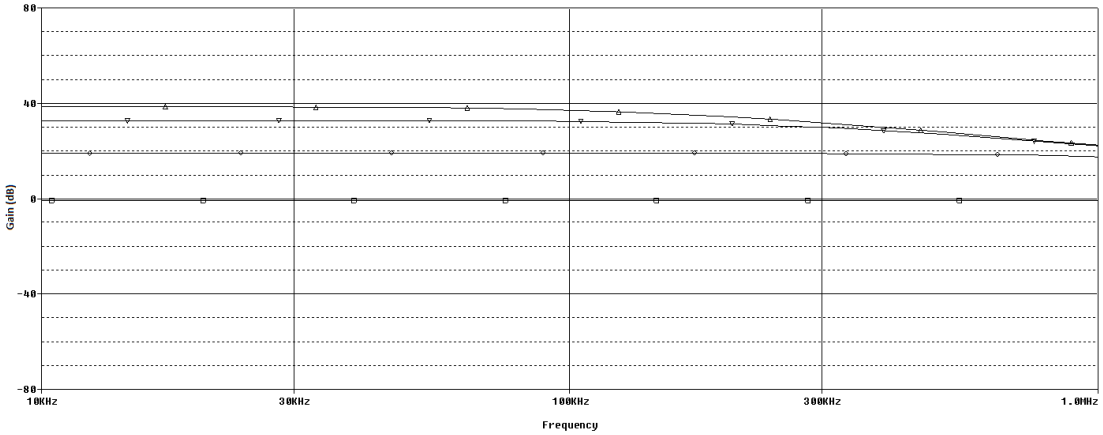

Fig. 3.4 Frequency characteristics of the voltage gain of the voltage amplifier configuration as shown in Fig. 3.3

The proposed circuit is simulated utilizing $R_2 = 0.5k\Omega$, $R_3 = 1k\Omega$, $R_1 = 1k\Omega, 10k\Omega, 50k\Omega, 100k\Omega$. The different gains of voltage amplifier as shown in figure 3.4.

3.4 Proposed Trans-impedance Amplifier

A trans-impedance amplifier converts an input of current to an output of voltage. It is also called a voltage to current converter or V to I converter. It is called trans-impedance because the efficiency of the amplifier is measured in units of resistance.

Trans-impedance gain = $\frac{Output\ Voltage}{Input\ current}$

The proposed trans-impedance amplifier configuration is shown in Figure 3.3

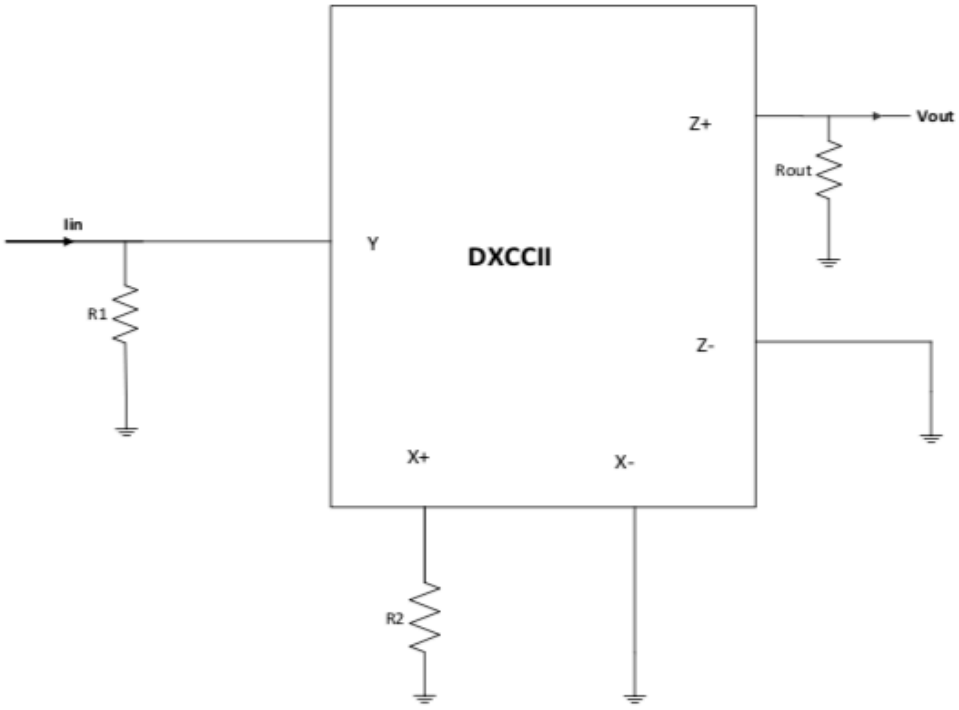

Fig. 3.5 Trans-impedance amplifier configuration using DXCCII

From the port matrix of DXCCII, we get

$V_Y = V_{X+} = -V_{X-}$

$I_Y = 0$

$I_{X+} = I_{Z+}$

$I_{X-} = I_{Z-}$ 3.8

From circuit analysis, the following Trans-impedance Transfer function is obtained:

$$V_{out} = I_{in} \left(R_1 / R_2\right) R_{out} \quad 3.9$$

$$\frac{V_{out}}{I_{in}} = \left(R_1 / R_2\right) R_{out} \quad 3.10$$

The Trans-impedance gain can be acquired as:

Trans-impedance gain = $\left(R_1 / R_2\right) R_{out}$ 3.11

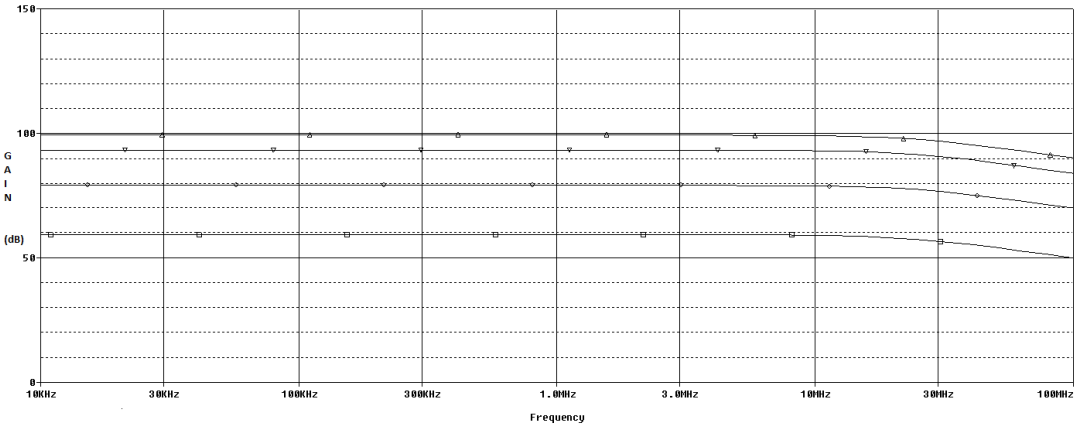

Fig. 3.6 Frequency characteristics of the trans-impedance gain of the trans-impedance amplifier configuration as shown in Fig. 3.5

The proposed circuit is simulated utilizing $R_2 = 1k\Omega$, $R_{out} = 1k\Omega$, $R_1 = 1k\Omega, 10k\Omega, 50k\Omega, 100k\Omega$. The different gains of trans-impedance amplifier is shown in figure 3.6.

3.5 Proposed Trans-admittance Amplifier

A trans-admittance amplifier converts an input of voltage to an output of current. It is also called a current to voltage converter or I to V converter. It is called trans-admittance.

Trans-admittance gain = $\frac{Output\ Current}{Input\ Voltage}$

The proposed trans-admittance amplifier configuration is shown in Figure 3.7

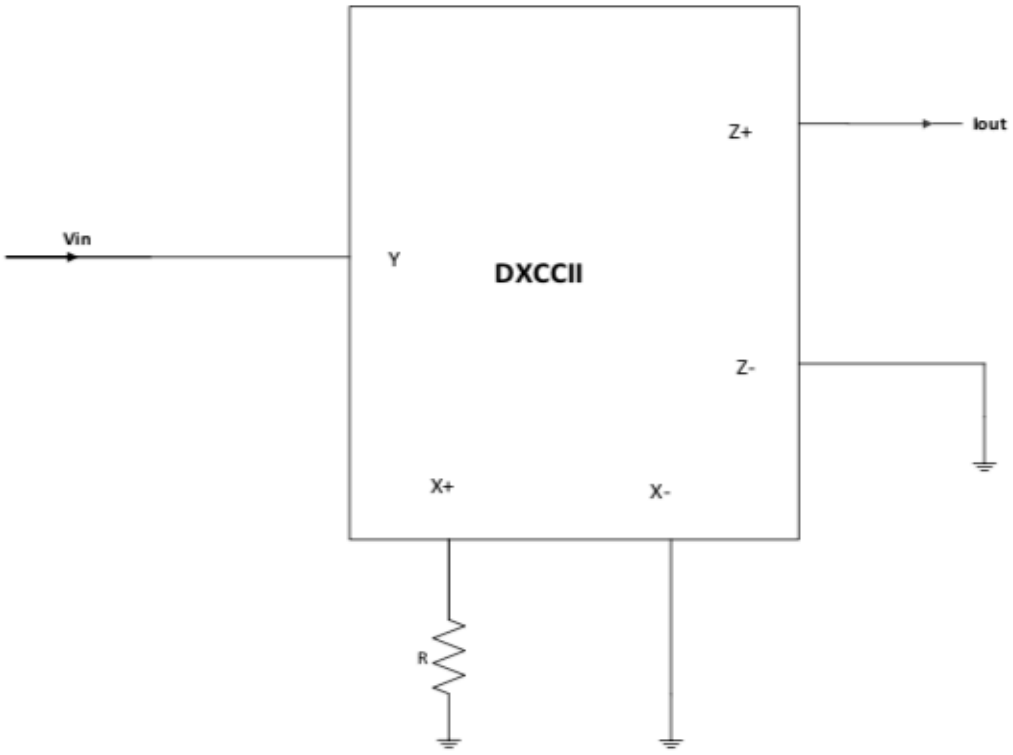

Fig. 3.7 Trans-admittance amplifier configuration using DXCCII

From the port matrix of DXCCII, we get

$V_Y = V_{X+} = -V_{X-}$

$I_Y = 0$

$I_{X+} = I_{Z+}$

$I_{X-} = I_{Z-}$

From proposed circuit analysis, Trans-admittance Transfer function is obtained:

$$I_{out} = -\frac{V_{in}}{R} \qquad 3.12$$

$$\frac{I_{out}}{V_{in}} = -\frac{1}{R} \qquad 3.13$$

The Trans-admittance gain can be acquired as:

$$\text{Trans-admittance gain} = -\frac{1}{R} \qquad 3.14$$

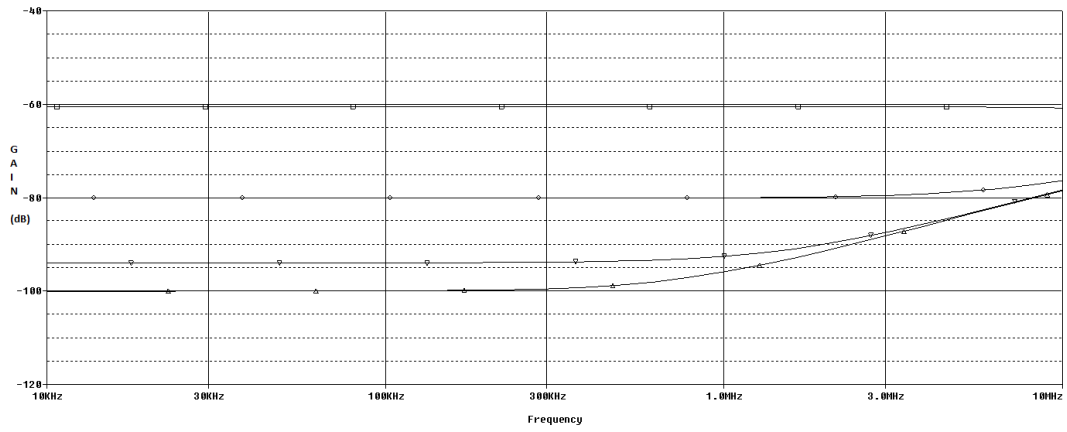

Fig. 3.8 Frequency characteristics of the trans-admittance gain of the trans-admittance amplifier configuration as shown in Fig. 3.7

The proposed circuit is simulated utilizing $R = 1k\Omega, 10k\Omega, 50k\Omega, 100k\Omega$. The different gains of trans-conductance amplifier are shown in figure 3.8.

3.6 Simulation Result

The performance of the proposed current amplifier, voltage amplifier, trans-impedance amplifier, and trans-admittance amplifier is confirmed using the SPICE simulation program. The MOS transistors are simulated utilizing 0.18μm TSMC innovation parameters. The supply voltages and biasing voltage are given by $V_{DD} = -V_{SS} =$ 2.5V and $V_{BB} =$ -1.6V, respectively and $C_C =$ 0.06pF.

3.7 Conclusion

This chapter presents novice current amplifier, voltage amplifier, trans-impedance amplifier, and trans-admittance amplifier using single DXCCII and less passive component (resistors). Simulation results are presented and discussed.

CHAPTER 4

4.1 Digitally controlled Variable gain amplifier (VGA)

Variable gain amplifiers (VGAs) are utilized in numerous applications so as to expand the dynamic scope of the general framework. Listening devices, [27] circle drives, [28-29] and remote interchanges are instances of such frameworks. In a remote correspondence framework, the convertibility of the terminal suggests that the got signal has an extremely wide power range. This requires the utilization of an automatic gain control (AGC) circuit. Its capacity is to naturally modify the increase of the get way with the goal that the signal prepared by the baseband segment hardware seems, by all accounts, to be at a consistent level paying little heed to the real signal quality got at the radio wire. The AGC contains for the most part two hinders, a variable gain amplifier (VGA) and a signal quality finder, which feeds back the control signal used to change the addition of the VGA. In current remote frameworks, the majority of the baseband signal handling is executed carefully by a digital signal processing (DSP). A VGA constrained by a simple signal will require digital to analog converter (DAC) in the AGC circle, expanding both multifaceted nature and postponement. Henceforth, a basic prerequisite of the VGA is to be carefully controlled. The addition of the VGA should increment straightly on the decibel scale so as to accomplish a wide gain control. Albeit customary VGA topologies dependent on high open circle gain operation amps give great outcomes, they experience the ill effects of limited increase data transfer capacity item. The third era remote correspondence frameworks use wideband code division multiple access (WCDMA) strategies [30]. Thus, the transmitted signal is to be spread over a more extensive scope of transfer speed. It is along these lines important to explore new CMOS amplifier based VGA structures that can give huge transfer speed free of the gain. This should be possible by utilizing the DXCCII based voltage-mode digitally controlled variable gain amplifier (VGA) and current-mode digitally controlled variable gain amplifier (VGA).

4.2 Proposed CM digitally controlled variable gain amplifier (VGA)

Proposed CM digitally controlled VGA circuit is shown in Fig. 4.1. It relies on the current amplifier circuit shown in Fig. 3.1. The current gain of the first stage is given by:

$$Current\ gain\ (A_{I1}) = \frac{I_{o1}}{I_{in}} = \frac{R_{f1}}{R_1} \qquad 4.1$$

From Eq. (4.1) that the gain of the principal arranges amplifier can be fluctuated freely of the data transfer capacity by changing the resistance R_1. Additionally, from Eq. (4.2), the gain of the second stage amplifier can be shifted autonomously of the data transmission by changing the resistance R_2. To accomplish the required increase control range and step, two VGA stages are cascaded. The primary stage works in coarse gain control while the second VGA stage gives fine gain control. The VGA circuit is in this way working in a coarse and fine course of action.

The current gain of the second stage is given by:

$$Current\ gain\ (A_{I2}) = \frac{I_{out}}{I_{o1}} = \frac{R_{f2}}{R_2} \qquad 4.2$$

The digital control structure of the resistors R_1 and R_2 is shown in Figs. 4.2 and 4.3, respectively. The resistance R_1 is given by:

$$R_1 = D_0{\times}R + D_1{\times}2R + D_2{\times}4R + D_3{\times}6R + D_4{\times}8R + D_5{\times}10R \qquad 4.3$$

Where R is resistors and $D_0 - D_5$ are the digital inputs that control the value R_1 of. Table 4.1 shows the values of these resistors. The digital inputs and the corresponding gains are shown in Table 4.2. Similarly, the resistance R_2 is given by:

$$R_2 = D_0{\times}R + D_1{\times}2R + D_2{\times}4R + D_3{\times}6R \qquad 4.4$$

Where R is resistors and $D_0 - D_3$ are the digital inputs that control the value of R2. Table 4.3 shows the values of these resistors. The digital inputs and the corresponding gains are shown in Table 4.4.

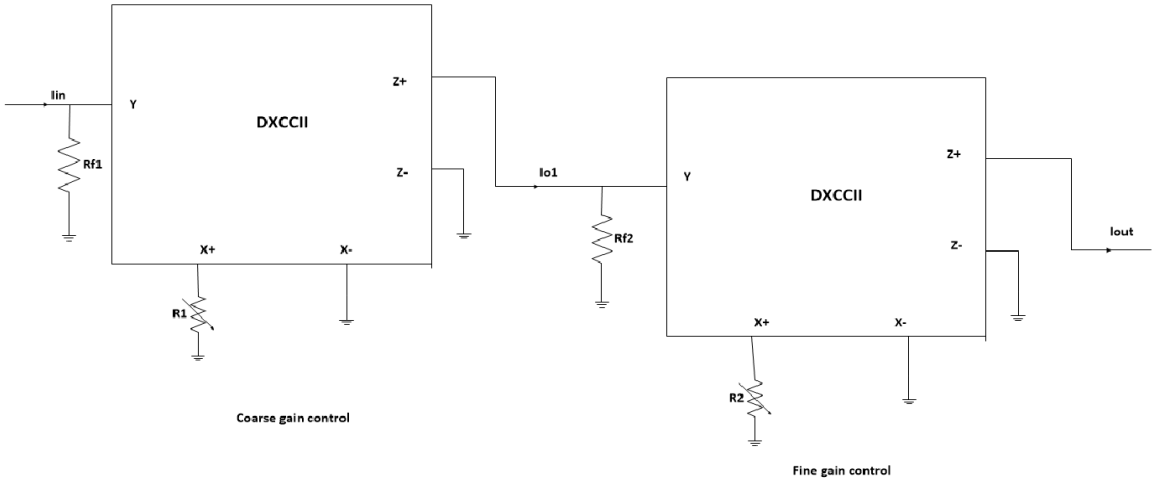

Fig. 4.1 The CM digitally controlled VGA using DXCCII

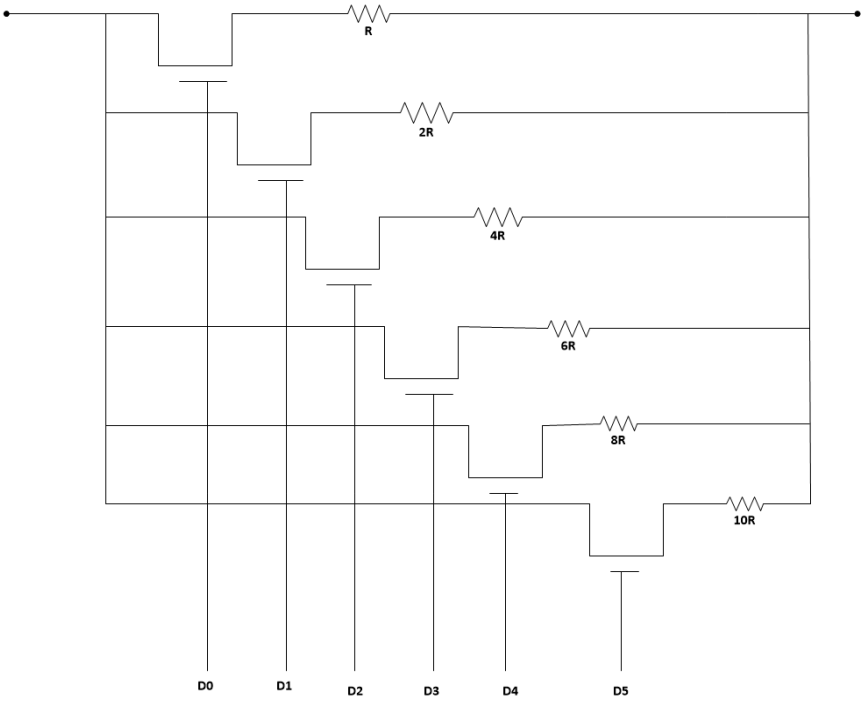

Fig. 4.2 The digitally controlled resistance R_1

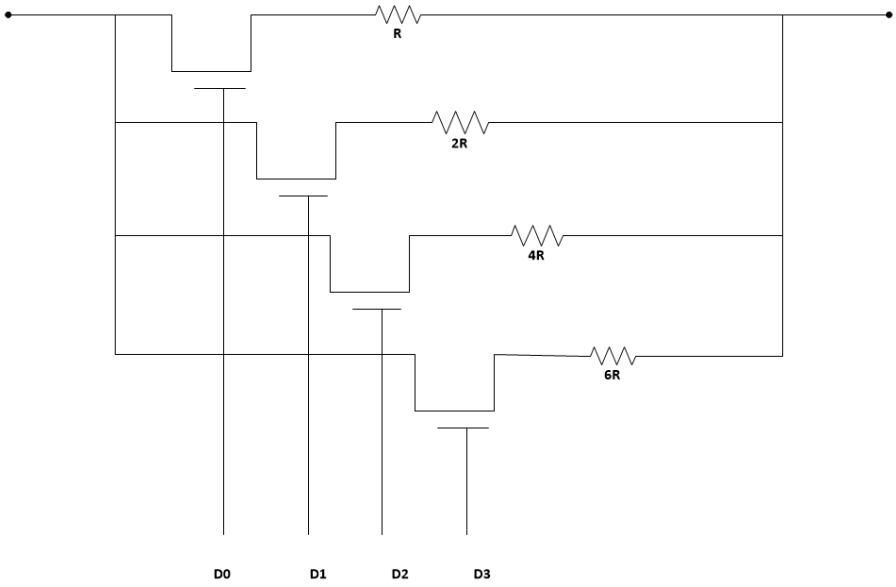

Fig. 4.3 The digitally controlled resistance R_2

Table 4.1: The values of the resistors used to control the resistance R_1 of the first stage of the current-mode digitally controlled VGA as shown in Fig. 4.1.

Resistor	Value (kΩ)
R	1
2R	2
4R	4
6R	6
8R	8
10R	10

Table 4.2: The digital input and the corresponding gain of the first stage of the current-mode digitally controlled variable gain amplifier (VGA) shown in Fig. 4.1.

Gain (dB)	D_0	D_1	D_2	D_3	D_4	D_5
0	1	0	0	0	0	0
29.82	1	1	1	1	1	1

Table 4.3: The values of the resistors used to control the resistance R_2 of the second stage of the current-mode digitally controlled VGA as shown in Fig. 4.1.

Resistor	Value (kΩ)
R	1
2R	2
4R	4
6R	6

Table 4.4: The digital input and the corresponding gain of the second stage of the current-mode digitally controlled variable gain amplifier (VGA) shown in Fig. 4.1.

Gain (dB)	D_0	D_1	D_2	D_3
0	1	0	0	0
6.02	0	1	0	0
12.04	0	0	1	0
18.06	0	1	0	1
22.27	1	1	1	1

The frequency response of the proposed VGA under most extreme coarse gain setting for example $D_0 - D_5$ (Digitally controlled R_1) = 111111 for all the combinations of $D_0 - D_3$ (Digitally controlled R_2) are found out to be -29.02 dB, -35.04 dB, -40.05 dB, -46.32 dB, -51.29 dB and are exhibited in Fig. 4.4. Similarly, the gain variation under least coarse gain setting for example $D_0 - D_5$ (Digitally controlled R_1) = 000001 are found as 0 dB, -6.02 dB, -12.04 dB, -18.06 dB, -22.27 dB for all combinations of $D_0 - D_3$ (Digitally controlled R_2) are displayed in Fig. 4.5 with a gain range of 6.0 dB (approximately).

The variation in gain setting (dB) with respect to the control word inputs ($D_0 - D_5$ (Digitally controlled R_1) and $D_0 - D_3$ (Digitally controlled R_2)) of the proposed VGA as shown in Fig. 4.4 and Fig. 4.5. It may be noted that wide variety of gains can be achieved with the amplifier using appropriate control bits tuning thus verifying overall performance of the proposed VGA while preserving the dB-linear characteristic of the amplifier.

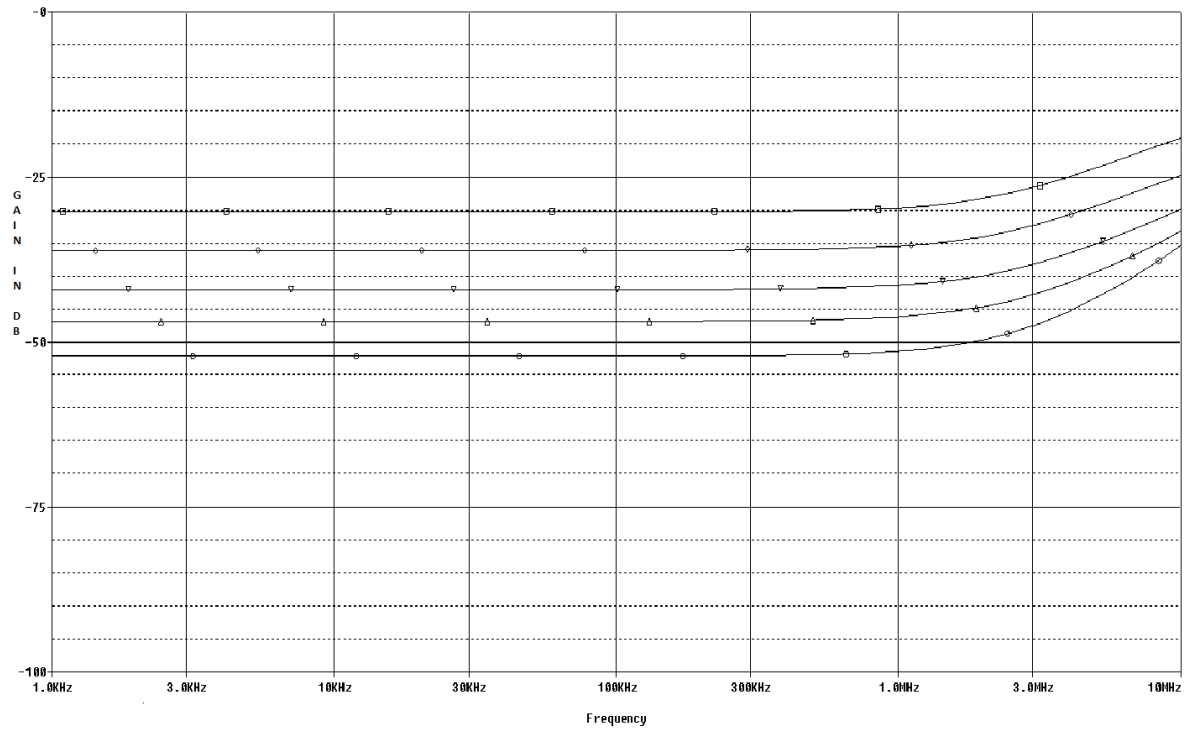

Fig. 4.4 Frequency characteristics of the current-mode digitally controlled VGA. Coarse gain setting for maximum gain values

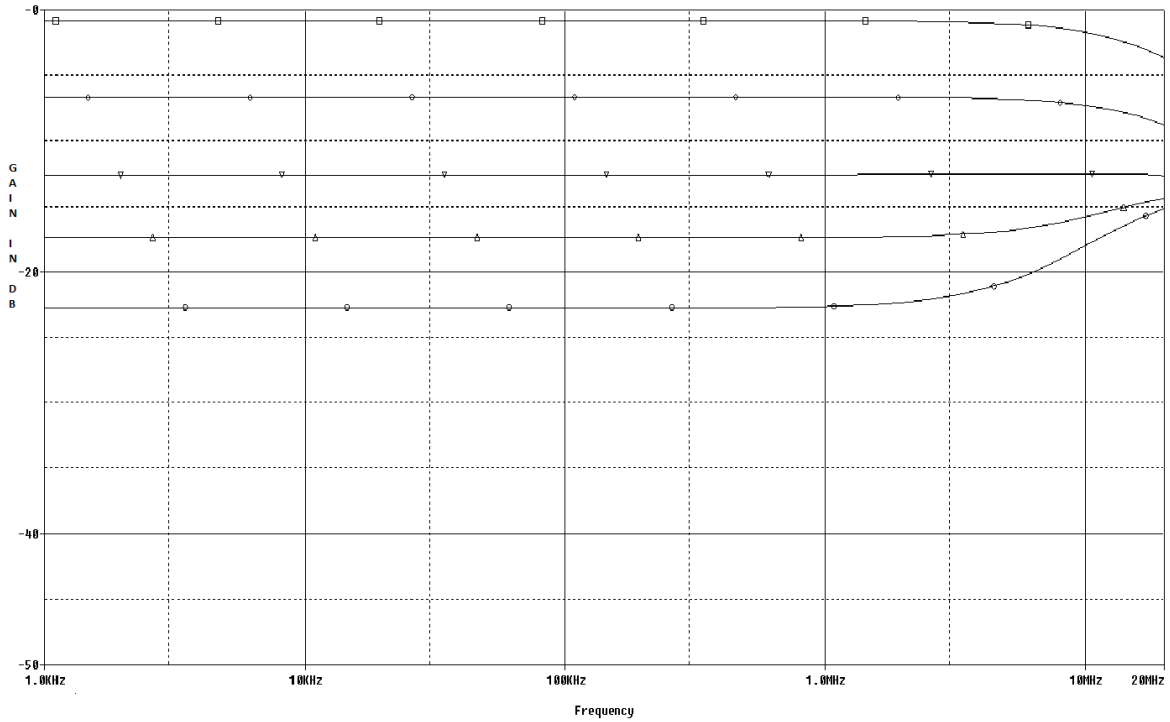

Fig. 4.5 Frequency characteristics of the current-mode digitally controlled VGA. Coarse gain setting for minimum gain values

4.2.1 Simulation Results

The performance of proposed CM digitally controlled VGA is confirmed using the SPICE simulation program. The MOS transistors are simulated using 0.18μm TSMC innovation parameters. The supply voltages and biasing voltage are given by $V_{DD} = -V_{SS}$ = 2.5V and V_{BB} = -1.6V, respectively and C_C = 0.06pF. The resistance is $R_{f1} = R_{f2} = 1k\Omega$. Fig. 4.4 and Fig. 4.5 shows the different gains of the overall VGA circuit with a 6 dB (approximately) gain step. It is clear that the bandwidth is about 1 MHz for the maximum gain of -51.29 dB and the average bandwidth is about 2 MHz at a gain of -40.05 dB. The average gain error is about 0.80 dB.

4.3 Proposed VM digitally controlled VGA

Proposed VM digitally controlled VGA circuit is shown in Fig. 4.6. It relies on the voltage amplifier circuit shown in Fig. 3.3. The voltage gain of the first stage is given by:

$$Voltage\ gain\ (A_{v1}) = \frac{V_{o1}}{V_{in}} = \frac{R_{f1}}{R_1} \qquad 4.5$$

From Eq. (4.5) that the gain of the principal arranges amplifier can be fluctuated freely of the data transfer capacity by changing the resistance R_1. Additionally, from Eq. (4.6), the gain of the second stage amplifier can be shifted autonomously of the data transmission by changing the resistance R_2. To accomplish the required increase control range and step, two VGA stages are cascaded. The primary stage works in coarse gain control while the second VGA stage gives fine gain control. The VGA circuit is in this way working in a coarse and fine course of action.

The voltage gain of the second stage is given by:

$$Voltage\ gain\ (A_{v2}) = \frac{V_{out}}{V_{o1}} = \frac{R_{f2}}{R_2} \qquad 4.6$$

The digital control structure of the resistors R_1 and R_2 is shown in Figs. 4.7 and 4.8, respectively. The resistance R_1 is given by:

$$R_1 = D_0{\times}R + D_1{\times}2R + D_2{\times}4R + D_3{\times}6R + D_4{\times}8R + D_5{\times}10R \qquad 4.7$$

Where R is resistors and $D_0 - D_5$ are the digital inputs that control the value R_1 of. Table 4.5 shows the values of these resistors. The digital inputs and the corresponding gains are shown in Table 4.6. Similarly, the resistance R_2 is given by:

$$R_2 = D_0{\times}R + D_1{\times}2R + D_2{\times}4R + D_3{\times}6R \qquad 4.8$$

Where R is resistors and $D_0 - D_3$ are the digital inputs that control the value of R2. Table 4.7 shows the values of these resistors. The digital inputs and the corresponding gains are shown in Table 4.8.

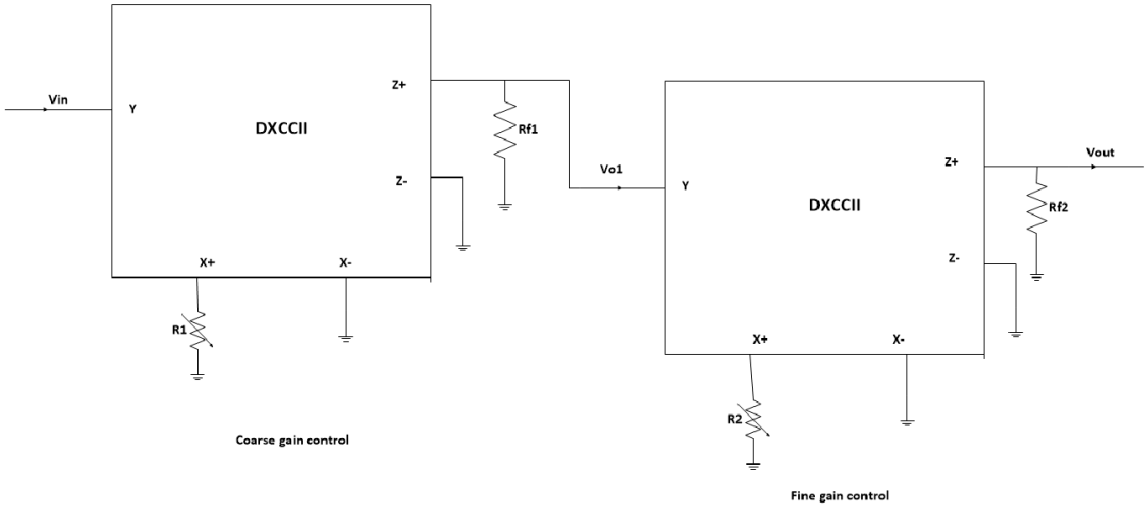

Fig. 4.6 The VM digitally controlled VGA using DXCCII

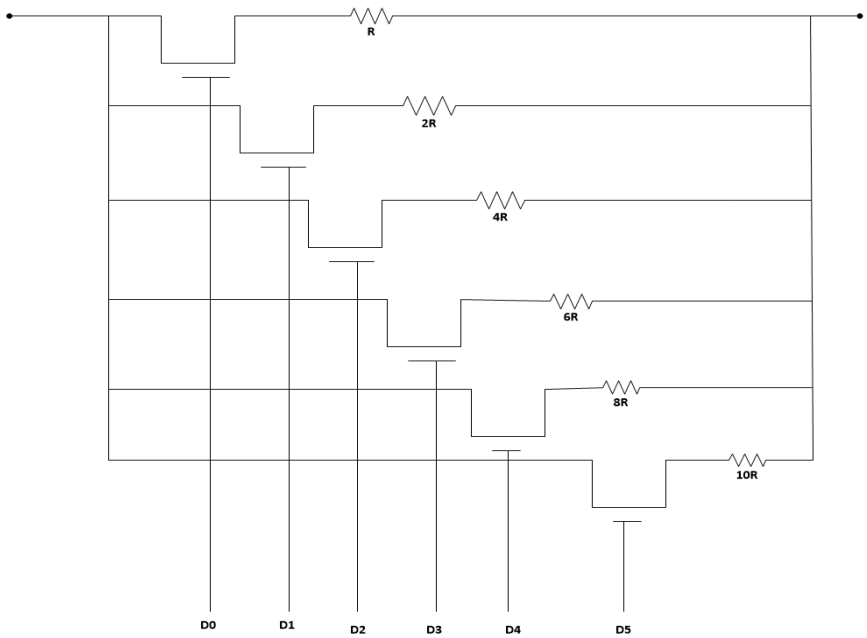

Fig. 4.7 The digitally controlled resistance R_1

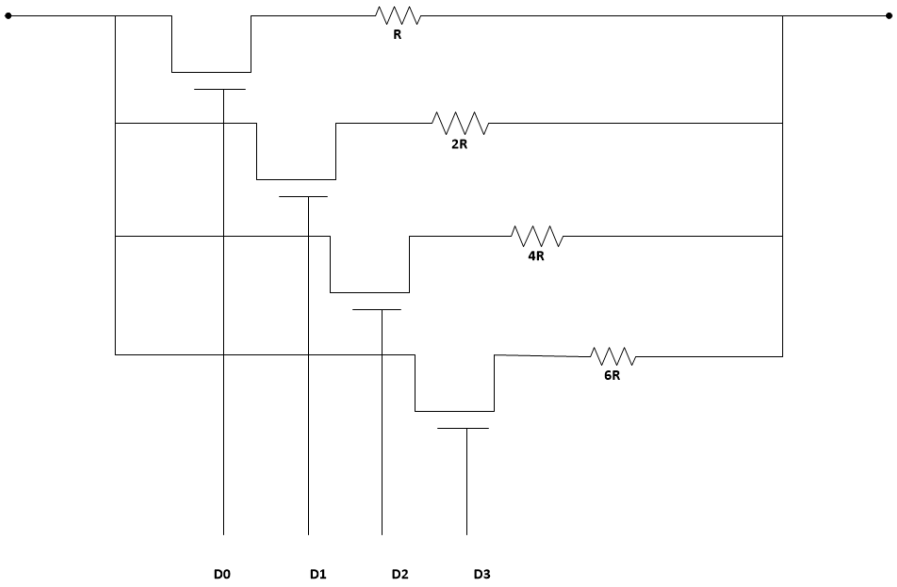

Fig. 4.8 The digitally controlled resistance R_2

Table 4.5: The values of the resistors used to control the resistance R_1 of the first stage of the voltage-mode digitally controlled VGA as shown in Fig. 4.6

Resistor	Value (kΩ)
R	1
2R	2
4R	4
6R	6
8R	8
10R	10

Table 4.6: The digital input and the corresponding gain of the first stage of the voltage-mode digitally controlled variable gain amplifier (VGA) shown in Fig. 4.6.

Gain (dB)	D_0	D_1	D_2	D_3	D_4	D_5
0	1	0	0	0	0	0
29.82	1	1	1	1	1	1

Table 4.7: The values of the resistors used to control the resistance R_2 of the second stage of the voltage-mode digitally controlled VGA as shown in Fig. 4.6.

Resistor	Value (kΩ)
R	1
2R	2
4R	4
6R	6

Table 4.8 The digital input and the corresponding gain of the second stage of the voltage-mode digitally controlled variable gain amplifier (VGA) shown in Fig. 4.6.

Gain (dB)	D_0	D_1	D_2	D_3
0	1	0	0	0
6.02	0	1	0	0
12.04	0	0	1	0
18.06	0	1	0	1

22.27	1	1	1	1

The frequency response of the proposed VGA under most extreme coarse gain setting i.e. $D_0 - D_5$ (Digitally controlled R_1) = 111111 for all the combinations of $D_0 - D_3$ (Digitally controlled R_2) are found out to be -28.93 dB, -34.95 dB, -40.96 dB, -46.97 dB, -51.17 dB and are displayed in Fig. 4.9. Similarly, the gain variation under least coarse gain setting i.e. $D_0 - D_5$ (Digitally controlled R_1) = 000001 are found as 0 dB, -6.02 dB, -12.04 dB, -18.06 dB, -22.27 dB for all combinations of $D_0 - D_3$ (Digitally controlled R_2) are presented in Fig. 4.10 with a gain range of 6.0 dB (approximately).

The variation in gain setting (dB) with respect to the control word inputs $D_0 - D_5$ (Digitally controlled R_1) and $D_0 - D_3$ (Digitally controlled R_2)) of the proposed VGA as shown in Fig. 4.9 and Fig. 4.10. It may be noted that wide variety of gains can be achieved with the amplifier using appropriate control bits tuning thus verifying overall performance of the proposed VGA while preserving the dB-linear characteristic of the amplifier.

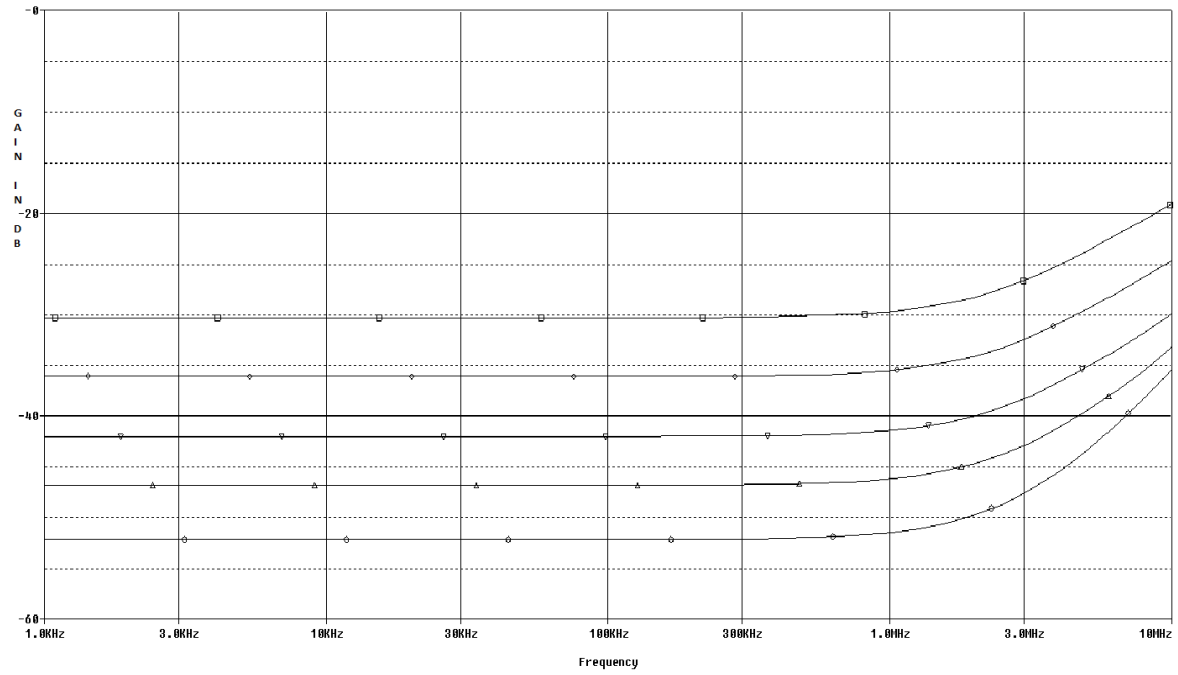

Fig. 4.9 Frequency characteristics of the voltage-mode digitally controlled VGA. Coarse gain setting for maximum gain values

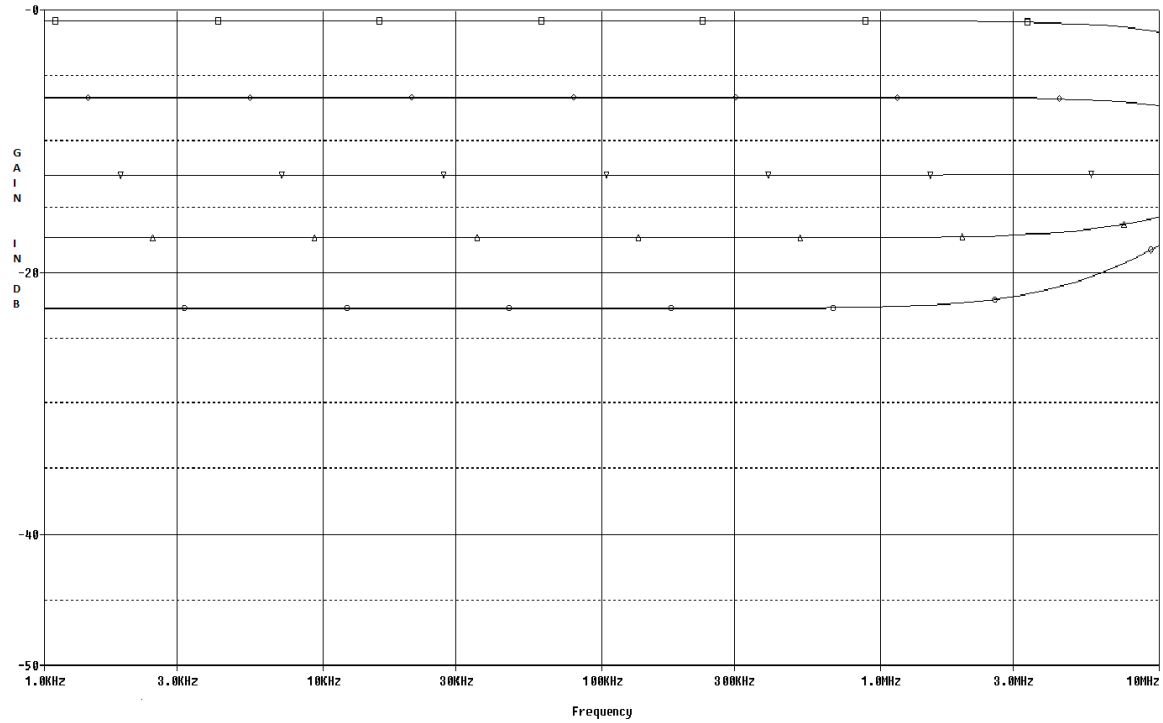

Fig. 4.10 Frequency characteristics of the voltage-mode digitally controlled VGA. Coarse gain setting for minimum gain values

4.3.1 Simulation Results

The performance of proposed voltage-mode digitally controlled variable gain amplifier (VGA) is verified using the SPICE simulation program. The MOS transistors are simulated using 0.18μm TSMC process parameters and are given in Table 2.1. The supply voltages and biasing voltage are given by $V_{DD} = -V_{SS}$ = 2.5V and V_{BB} = -1.6V, respectively and C_C = 0.06pF. The resistance is $R_{f1} = R_{f2} = 1k\Omega$. Fig. 4.9 and Fig. 4.10 shows the different gains of the overall VGA circuit with a 6 dB (approximately) gain step. It is clear that the bandwidth is about 470 KHz for the maximum gain of -51.17 dB and the average bandwidth is about 1.2 MHz at a gain of -40.96 dB. The average gain error is about 0.80 dB.

4.4 Programmable Gain Amplifier (PGA)

Amplifiers, a specifically programmable gain amplifier, discover applications in instrumentation, photodiode circuits, ultrasound preamplifiers, sonar, wide unique range sensors, driving ADCs (some ADCs have on-chip PGAs), automatic gain control (AGC) loops [31, 32]. Fig 4.11 [32] delineates a normal utilization of PGA in the data acquisition system wherein it is set between a sensor and analogue to digital converter (ADC). Extra sign handling hardware, according to request of utilization might be put previously or after the PGA. Previous area is, be that as it may, favored as it permits molding a bigger sign. Regularly, operational enhancer is utilized in planning PGAs. Be that as it may, the benefit of momentum mode sign handling [33, 34] has roused scientists to investigate the PGA plans dependent on current mode building blocks. The highlights of accessible PGAs [35-58] are condensed based on the kind of information being prepared and yield made accessible, dynamic block utilized, input/output impedance and gain controlling component.

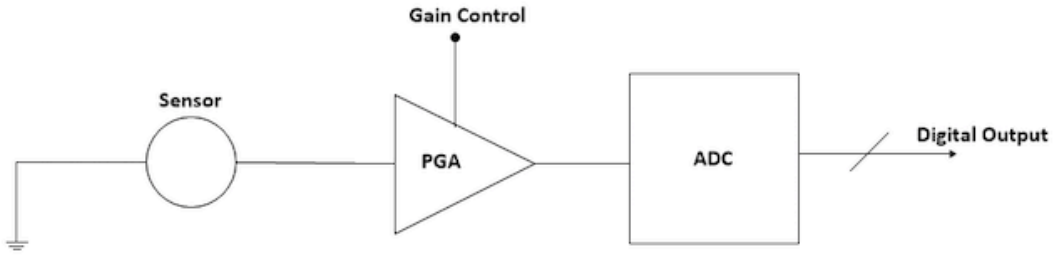

Fig. 4.11 PGAs in data acquisition systems [32]

Following perception are made:

• The PGA plans [35-58] give voltage output and procedure information from the voltage sensor. A current to voltage converter is required if the information is detected from the current sensor.

- The PGA plan [35] forms information detected from the current sensor and gives current output. A current to voltage converter required on the off chance that there is a need of interfacing it with a circuit having a contribution as voltage.

- Different dynamic squares, for example, second era current conveyor (CCII) [37, 39] and its variations, for example, Digitally Programmable CCII (DPCCII) [35], Digitally controlled Fully Differential CCII (DCFDCCII) [36] and Fully Differential CCII (FDCCII) [50]; Current Feedback Amplifier topologies (CFAs) [38] and its variations, for example, Fully Differential Current Feedback Op-amp (FDCFOA) [39]; Operational Floating current transport (OFCC) is utilized in [40]; the topologies [42, 46, 47, 51, 54] utilize differential enhancer; CMOS based basic, single finished and completely differential entryway driven variable gain amplifier (VGA) with programmable increase is likewise revealed in [52, 53]; a couple of topologies with Operational trans-conductance amplifier (OTA) is accounted for in [55, 56]; though [57] utilizes operation amp for PGA plan.

- The input and output impedance are appropriate in [38, 40, 41, 43, 44, 47, 52-54, 57, 58] while extra dynamic block is required in [35, 36, 37. 39, 42, 45, 46, 48-51, 55, 56] to fulfill impedance condition.

- Gain tuning is accomplished through current divisions network (CDN) [36, 37, 48], weighted transistor arrays [35, 47], potentiometer [38, 39, 46, 50] or switches [40, 41-43, 45]; carefully controlled exponential capacity [44] or current mirrors [49]; 4-bit Digitally controlled look up table and pre-adjustment technique [51]; DAC addition control (dB linear/digital) [22]; 4-bit and 5-bit digitally programmable VGA [53]; source deteriorated capacitor array [54]; two stacked transistors [55]; exchanged capacitor array [56]; and resistor array with MOS switches [57, 58].

- Explicit component for fine and coarse addition tuning is connected in [37, 40] and [57].

It is obvious from the above discussion that no PGA configuration is accessible that works in trans-impedance mode (with the exception of OFCC based PGA) for example form information that is accessible from current sensor and gives voltage output. To connect this

hole, another DXCCII based PGA topology, working in a trans-impedance mode, is advanced in this chapter. The proposition has increased control by means of both coarse addition and fine addition bits. The activity of the circuit is checked through SPICE simulation. The substance of present work is organized in four segments including the early on one. The working of DXCCII is quickly explored in section 4.5 alongside a detailed explanation of the proposed PGA. The practical confirmation of the proposition enveloping reenactment is put in section 4.6. Conclusion are attracted Section 4.7.

4.5 Proposed DXCCII based PGA

The block chart of proposed DXCCII based PGA is delineated in Fig. 4.12. The acknowledgement of a constituent block has appeared in Fig. 4.13 (a) – Fig. 4.13 (d). The primary block (Fig. 4.13 (a)) of the proposed PGA is a current gain block. It utilizes DXCCII based current amplifier and its gain is given by (4.9):

$$Io1 = -I_{in}\left(\frac{R_1}{R_G}\right) \qquad 4.9$$

The second and third blocks of proposed PGA provide control over coarse and fine gain through bits $(B_5 - B_4)$ and $(B_3 - B_0)$. The output of first block is applied to second block (Fig. 4.13 (b)) along with coarse gain control bits $(B_5 - B_4)$. A 2 to 4 decoder is used to convert bits $(B_5 - B_4)$ to bits $(D_3 - D_0)$, which enable one out of the four switches connected at X+ port of DXCCII 2 of second block, thus resulting in coarse gain variation of proposed PGA. The current input (Io1) is converted into voltage (Vo1) and its value is given as

$$Vo1 = -Io1\left(\frac{R_2}{R_3}\right)R_4 = I_{in}\left(\frac{R_1}{R_G}\right)\left(\frac{R_2}{R_3}\right)R_4 \qquad 4.10$$

Where R_3 is given by (4.11)

$$R_3 = D_0 \times R + D_1 \times 2R + D_2 \times 4R + D_3 \times 6R \qquad 4.11$$

The third block (Fig. 4.13 (c)) is digitally controlled R-2R ladder network. It adds fine gain control through multiplexers whose operation is controlled by bits $(B_3 - B_0)$. The bits $(B_3 - B_0)$ can vary from 0001 to 1111 therefore fifteen possible gain combinations exist. Taking the coarse gain and fine gain variations into account; the proposed PGA can be tuned 60 possible gain values.

The output of the third block is given as

$$Vout = Vo1\left(\frac{B_0}{16} + \frac{B_1}{8} + \frac{B_2}{4} + \frac{B_3}{2}\right) \qquad 4.12$$

The output of the third block is not at low output impedance terminal, a DXCCII based buffer is used as the fourth block (Fig. 4.13 (d)). The proposed circuit level diagram is shown in Fig. 4.14.

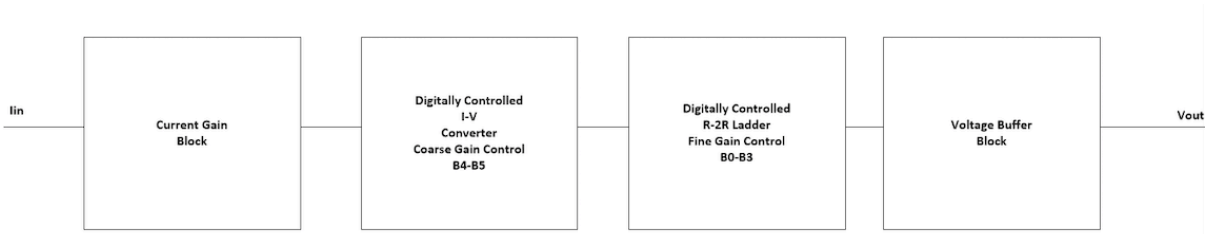

Fig. 4.12 Block diagram of the proposed Programmable Gain Amplifier (PGA)

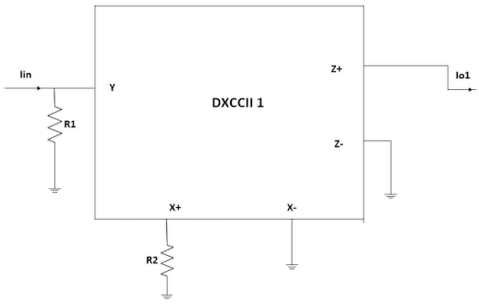

Fig. 4.13 (a) Current Gain Block

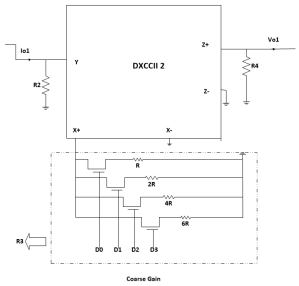

Fig. 4.13 (b) Digitally controlled I-V converter

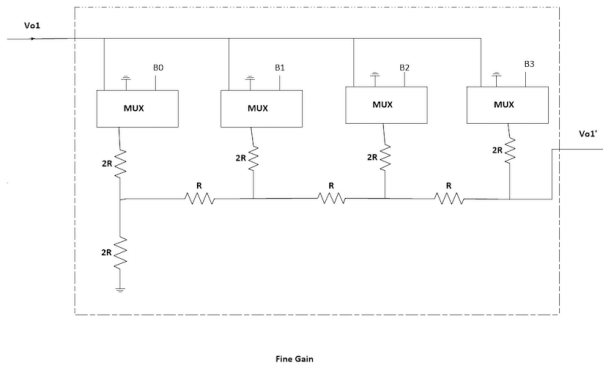

Fig. 4.13 (c) R-2R ladder Network

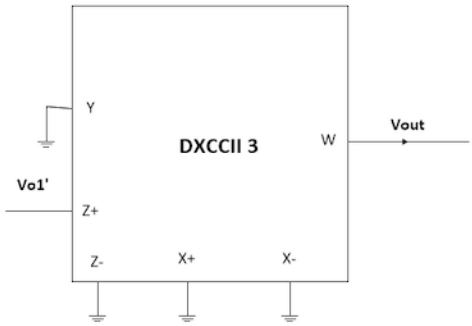

Fig. 4.13 (d) Voltage Buffer

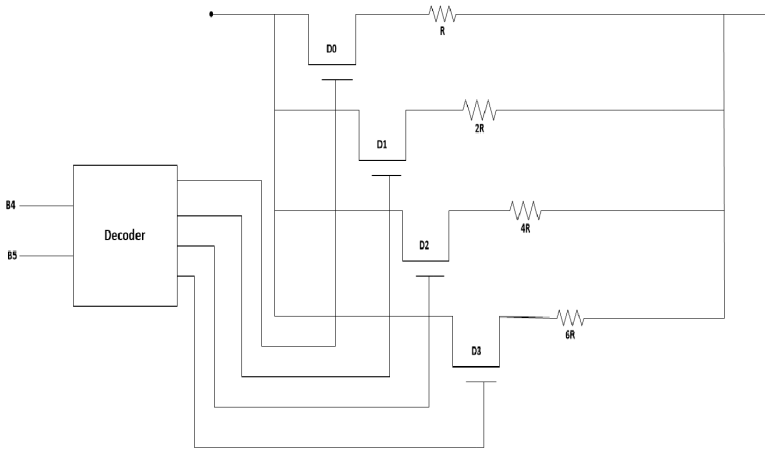

Fig. 4.13 (e) 2 to 4 decoder is used to convert bits ($B_5 - B_4$) to bits ($D_3 - D_0$)

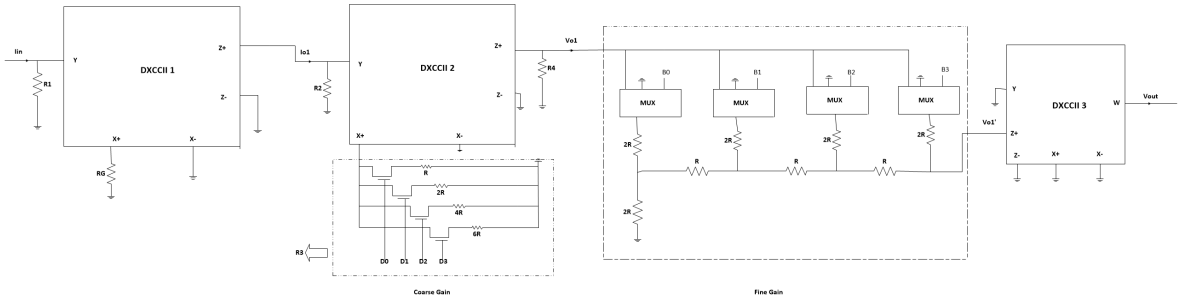

Fig. 4.14 The circuit level diagram of proposed Programmable Gain Amplifier (PGA)

The multiplexer and decoder are shown in Fig. 4.13 (c) and Fig. 4.13 (e) are realized utilizing transmission gate and static CMOS as shown in Fig. 4.15 (a) and Fig. 4.15 (b). Their corresponding functionality is listed in Table 4.9 and Table 4.10.

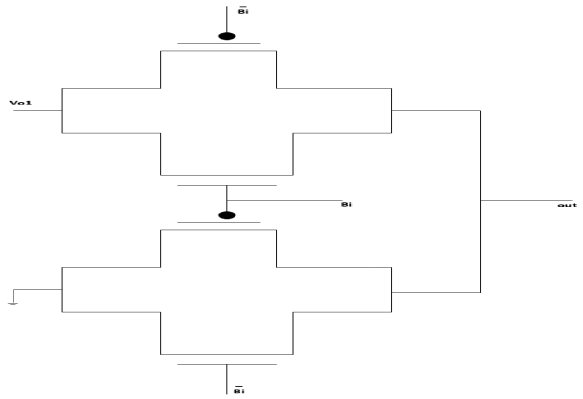

Fig. 4.15 (a) Schematic of 2×1 Multiplexer using Transmission Gates

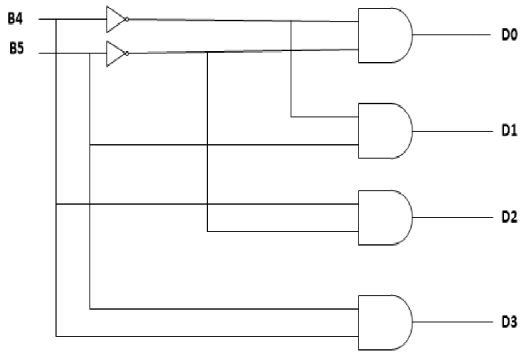

Fig. 4.15 (b) 2×4 Decoder

Table 4.9: Truth Table for 2×1 Multiplexer in Fig. 4.15 (a)

B_i	Out
0	0
1	Vo1

Table 4.10: Truth Table for 2 to 4 Decoder of Fig. 4.13 (e)

B_5	B_4	D_0	D_1	D_2	D_3	Equivalent Resistance at the block, R_3(kΩ
0	0	1	0	0	0	1
0	1	0	1	0	0	2
1	0	0	0	1	0	4
1	1	0	0	0	1	6

4.6 Simulation Results

The performance is verified using the SPICE simulation program. The MOS transistors are simulated using 0.18μm TSMC process parameters and are given in Table 2.1. The supply voltages and biasing voltage are given by $V_{DD} = -V_{SS} =$ 2.5V and $V_{BB} =$ -1.6V, respectively and C_C = 0.06pF. The resistance R_1 and R_G in current gain block Fig. 4.13 (a) are taken as 31 kΩ and 1 kΩ. The value of R_2 and R_4 in second block are taken as 1 kΩ. The values of R in second and third block of proposed PGA are taken as 1 kΩ.

The frequency response of the proposed PGA under maximum coarse gain setting i.e. $B_3 - B_0$ = 1111 for all the combination of B_4 *and* B_5 are found to be 85.97 dB, 80.15 dB, 74.24 dB and 70.56 dB and are shown in Fig. 4.16 (a). Similarly, the gain variation under minimum coarse gain setting i.e. $B_3 - B_0$ = 0001 are found as 81.13 dB, 75.32 dB, 69.40 dB, 65.92 dB for all combination of B_4 *and* B_5 are presented in Fig. 4.16 (b) with a gain range of 20 dB with a bandwidth of approximately 10 MHz.

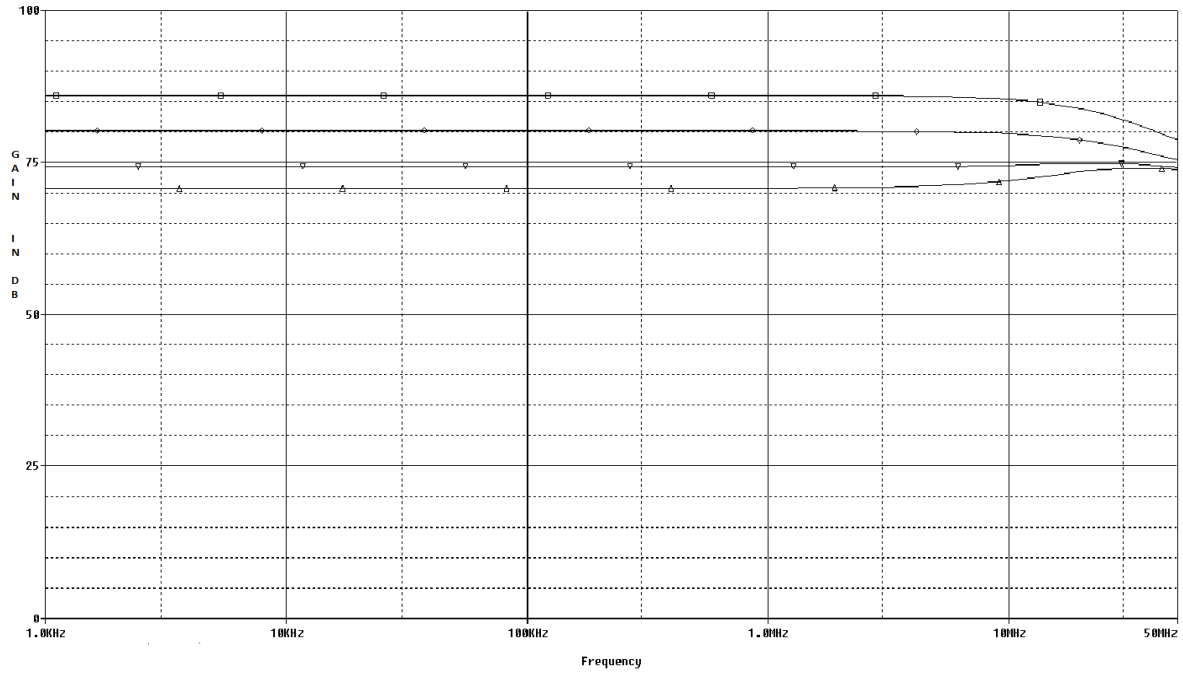

Fig. 4.16 (a) Frequency characteristics of proposed circuit in coarse gain setting for maximum gain values

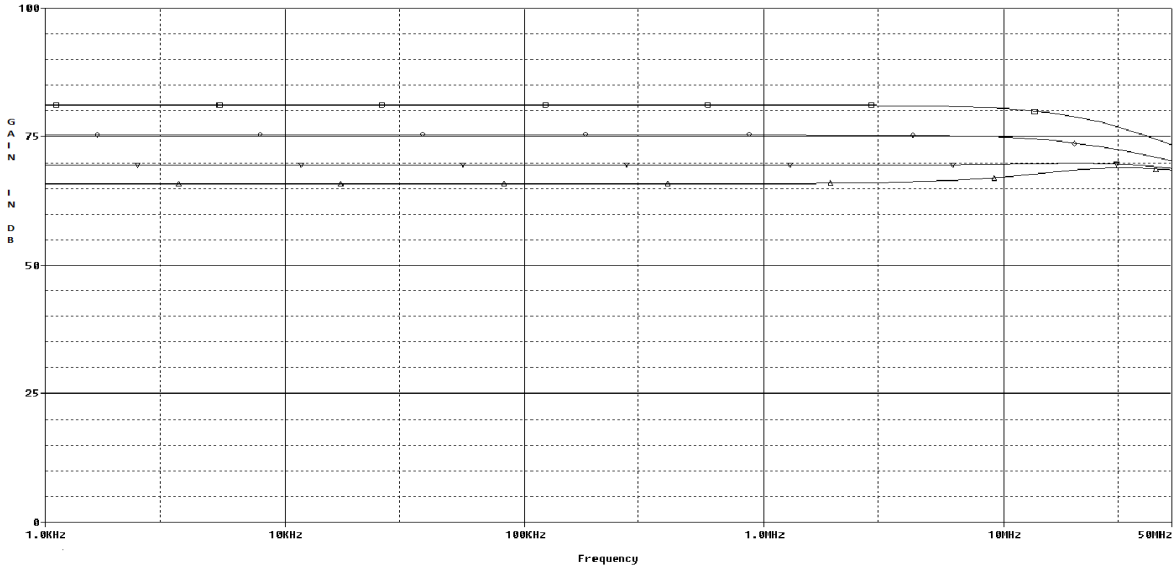

Fig. 4.16 (b) Frequency characteristics of proposed circuit in coarse gain setting for minimum gain values

4.7 Conclusion

This chapter presented VM digitally controlled variable gain amplifier (VGA) and CM digitally controlled variable gain amplifier (VGA) utilizing a DXCCII. To accomplish the required increase control range and step, two VGA stages are cascaded. The main stage is coarse gain control while the subsequent stage is fine gain control. The VGA circuit is in this way working in a coarse and fine course of action are proposed and broke down.

A novice programmable gain amplifier configuration working in trans-impedance mode has been proposed. The structure utilizes variable increase stage utilizing DXCCII pursued by R-2R ladder network to accomplish coarse and fine gain tuning of the amplifier. Due to nuanced mixed signal processing utilized in this structure, a wide scope of gains can be accomplished utilizing the control words with a high level of exactness.

4.5 Future scope

Since the bandwidth of the proposed circuit is low, the bandwidth can be improved in the future by using bandwidth enhancement techniques.

CHAPTER 5

5.1 First Order All-pass filter

The principal request electronic capacity, which finds a wide scope of utilizations in simple signal processing, and a signal generation is a system grouped under filters. It is an all pass filter, which is likewise called a phase shifter, for its plentifulness protecting component (previous name) and recurrence ward stage attributes (later name). The two highlights together make it amazing electronic capacity with broad applications. These range from a basic stage equalizer or phase shifter to increasingly complex ones like signal generation with quadrature or multiphase output. Besides, higher request sifting capacities can be additionally acknowledged with the assistance of this straightforward electronic capacity.

When realized using high performance active element like current conveyor, the first order all pass filters becomes a natural building block for modern communication and instrumentation systems. High accuracy, wide, bandwidth and exceptionally high slew rates combined with low voltage and low power implementations of current conveyors makes it an ideal choice for modern applications in analog signal processing.

5.2 Literature Survey

The dual-X current conveyor-II (DXCCII) is an adaptable dynamic component, which can be utilized for actualizing either voltage-mode or current-mode capacities [26, 60]. A few uses of the DXCCII, for example, Voltage-mode and Current-mode second-order multifunction filters, oscillator and whirligig have been exhibited in [26, 60-62]. It is notable that a topology comprising of just grounded aloof (resistors and capacitors) components are profitable from incorporated circuit (IC) acknowledgement perspective [63-65].

Albeit operational amplifier (operation amp) and passive (resistors and capacitors) components can be utilized to build all-pass filter [66,67], they experience the ill effects of the restricted increase transfer speed result of operation amp. Luckily, acknowledgement of the principal request all-pass filter utilizing current conveyors (CCs) has gotten extensive

consideration in the writing [68-91]. The points of interest and disadvantages of these first-order all-pass filters can be outlined as pursues.

The displayed Voltage-mode circuits in [68] utilize single, positive-type second-age current conveyor (CCII+) and three to five passive (resistors and capacitors) components however they don't ensure high output impedance. Higashimura and Fukui proposed Voltage-mode and Current-mode all-pass filter, separately, in [69] and [70], utilizing single, negative-type, second-age current conveyor (CCII-). In spite of the fact that the exhibited filter in [69] and [70] offer high input and output impedances, individually, they experience the ill effects of utilizing coasting capacitors just as resistor coordinating prerequisite and solidarity gain. In [71] new Current-mode/Voltage-mode all-pass channel utilizing CCII+/CCII-, four resistors and single grounded capacitor were displayed. These channels have high information and yield impedances in Voltage-mode/Current-mode activities, yet they experience the ill effects of a steady addition of 0.5. The CC-based Voltage-mode channels exhibited in [72-75] utilize a gliding capacitor and have recurrence ward input impedances. The first order all-pass filter given in [76] which utilizes a third-generation current conveyor (CCIII) works in trans-admittance mode (TAM) (for example input as voltage and output as current) and does not offer high information impedance. Likewise, basic Voltage-mode first-order all-pass filters utilizing one differential distinction current conveyor (DDCC), one grounded capacitor and one skimming resistor were displayed in [77] and [78], yet their input impedances rely upon the estimations of the utilized latent components. Also, a solitary DDCC-based all-pass channel with a coasting capacitor and grounded resistor was displayed in [79]. In any case, the information impedance of this circuit is additionally recurrence subordinate. As of late, two new Voltage-mode all-pass filter utilizing single double output current conveyors (DO-CCIIs) and single adjusted negative sort current conveyor (MCCII-) were exhibited in [80] and [81], separately. These circuits give high input impedance and utilize one grounded capacitor yet two gliding resistors. The Current-mode and Voltage-mode all-pass filters in [82] and [83] utilize two CCIIs and four grounded passive components. The Voltage-mode filter in [84-87] utilize just grounded aloof components yet require two differential voltage current conveyor (DVCC), and the Current-mode circuit in [88] requires two CCIIs and utilizes a drifting capacitor. The Current-mode all-pass filter in [89] utilize single DVCC together with three latent components however they don't give addition and utilize at any rate

one coasting aloof component. The Current-mode all-pass circuit with high output impedance detailed in [90, 22] utilizes single dynamic component yet requires two indistinguishable info flows. In this manner, an extra dynamic component ought to be utilized to give these indistinguishable info flows. Another Current-mode all-pass channel exhibited in [96] gives low-info and high-yield impedances and uses just grounded latent components, yet requires two DO-CCIIs as dynamic components. At long last, another Current-mode all-pass filter dependent on a functioning component, in particular, Z-copy current inverter trans-conductance amplifier (ZC-CITA), and just one grounded capacitor was introduced in [91]. The ZC-CITA is made out of a double output operational trans-conductance amplifier (OTA), a present mirror and a present inverter circuit.

In this chapter novice Current-mode first-order all-pass filters utilizing a single DXCCII and less number of passive components, (grounded capacitors and grounded resisters), are proposed. Non-ideal gain and parasitic impedance effects of the DXCCII on the transfer function of the proposed filters are investigated.

5.3 Proposed Current-mode first order all-pass filter

The proposed Current-mode first order all-pass filter is shown in figure 5.1. The DXCCII discussed in in Figure 2.2 is used in the realization of Current-mode first order all-pass filter. The proposed circuit uses two grounded capacitors and two grounded resistors and single active component.

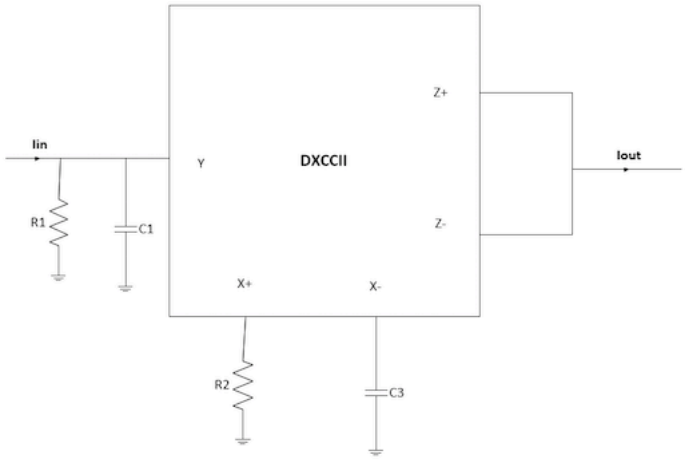

Fig. 5.1 Proposed Current-mode first order all-pass filter

From the port matrix of DXCCII, we get

$V_Y = V_{X+} = -V_{X-}$

$I_Y = 0$

$I_{X+} = I_{Z+}$

$I_{X-} = I_{Z-}$ 5.1

From the circuit analysis, the following Current-mode Transfer function is obtained:

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} \cdot \frac{1-sC_3R_2}{1+sC_1R_1} \quad 5.2$$

If $C_1 = C_3 = C$, $R_1 = R_2 = R$, we get

$$\frac{I_{out}}{I_{in}} = \cdot \frac{1-sCR}{1+sCR} \quad 5.3$$

Filter has pole frequency ω as:

$$\omega_{\circ} = \frac{1}{RC} \quad 5.4$$

Phase response in frequency domain acquired as:

$$\varphi(\omega) = 180^{\circ} - 2\tan^{-1}(\omega CR) \quad 5.5$$

5.4 Non-idealities

The response of the proposed circuit deviates from the conventional one due to non-idealities of the active elements. The non-ideal DXCCII is described by the following relationship:

$$V_{X+} = \beta_1 V_Y, \quad V_{X-} = -\beta_2 V_Y, \quad I_Y = 0, \; I_{Z+} = \alpha_1 I_{X+}, \quad I_{Z-} = \alpha_2 I_{X-} \quad 5.6$$

Where ideally β_1=β_2=1, α_1=α_2=1 and they represent the voltage or current transfer ratios of the DXCCII.

Where, β_1(s) and β_2(s) represent the frequency transfers of the internal voltage followers and α_1(s) and α_2(s) represent the frequency transfers of the internal current followers of the DXCCII, respectively. If DXCCII is working at frequencies much less than the corner frequencies of β_1(s), β_2(s), α_1(s) and α_2(s), namely, then β_1(s) = β_1=1-ε_{v1} where, ε_{v1}($|\varepsilon_{v1}|$ <<1) is the voltage tracking error from the Y terminal to the X+ terminal of the DXCCII; β_2(s) = β_2=1-ε_{v2} where, ε_{v2}($|\varepsilon_{v2}|$ <<1) is the voltage tracking error from the Y terminal to the X- terminal of the kth-DXCCII; then α_1(s) = α_1=1-ε_{i1} where, ε_{i1}($|\varepsilon_{i1}|$ <<1) is the current tracking error from the X+ terminal to the Z+ terminal and α_2(s) = α_2=1-ε_{i2} where, ε_{i2}($|\varepsilon_{i2}|$ <<1) denotes the current tracking error from the X- terminal to the Z- terminal of the kth-DXCCII.

From circuit analysis, following transfer function is realized:

$$\frac{I_{out}}{I_{in}} = \frac{\alpha_1(s)\beta_1(s) - sCR\alpha_2(s)\beta_2(s)}{1+sCR} \quad 5.7$$

5.5 Parasitic effects

The proposed circuit performance is affected by the presence of various parasitic at the terminal of the device. The various parasitic are resistors and capacitor at port Z in the form of $R_Z \| C_Z$, at port Y in the form of $R_y \| C_y$ and at port X parasitic are in form of series combination of resistance R_X and capacitor C_X. Ideally, the DXCCII is used at frequencies much lower than the corner frequencies of α_i (i=1,2) and β_i (i=1,2). For typical applications built around DXCCII, the external resistors (R) are much smaller than the parasitic resistors at the Y and Z terminals of DXCCII, i.e. R<<R_Y or R_Z and the external resistors are much greater than the parasitic resistors at the X terminals of DXCCII, i.e. R_X<<R.

From the circuit analysis, the following transfer function is realized:

$$\frac{I_{out}}{I_{in}} = \frac{R_1 \alpha_1(s)\beta_1(s)}{R_2} \frac{1 - sC_3R_2\frac{\alpha_2(s)\beta_2(s)}{\alpha_1(s)\beta_1(s)}}{1 + sC_1R_1} \qquad 5.8$$

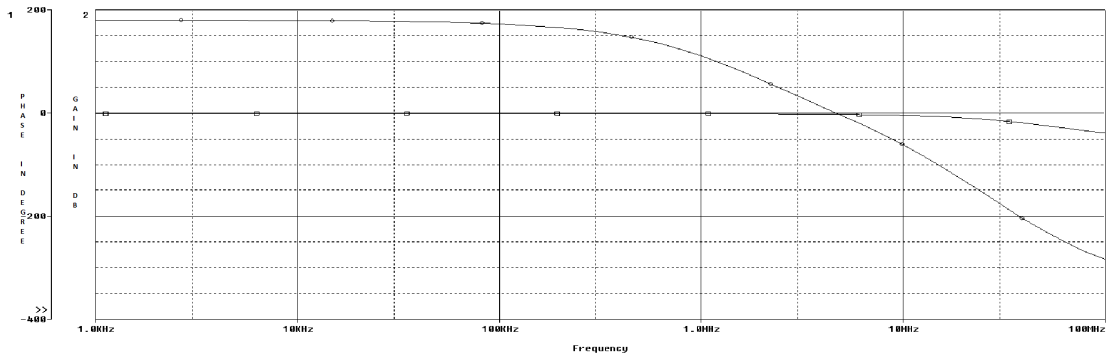

Fig. 5.2 Simulation phase and gain responses of presented Current-mode first order all-pass filter

5.6 Simulation Results

The performance of the proposed current-mode all-pass filter is verified using the SPICE simulation program. The MOS transistors are simulated using 0.18μm TSMC process parameters and are given in Table 2.1. The supply voltages and biasing voltage are given by $V_{DD} = -V_{SS}$ = 2.5V and V_{BB} = -1.6V, respectively and C_C = 0.06pF. The current-mode all-pass filter has a pole frequency of $f_0 = 1.59MHz$ and constant gain are obtained by selecting R=1kΩ and C=0.1nF.

5.7 Conclusion

In this chapter novice Current-mode first-order all-pass filters using a single DXCCII and four passive components, (grounded capacitors and grounded resisters), are proposed. The proposed all-pass filters have attractive features such as single active component and use of only grounded capacitors and resistors. Thus, they are suitable for IC implementation. The presented current-mode filter has high input impedance and high output impedance. Non-ideal gain and parasitic impedance effects of the DXCCII on the transfer function of the proposed filters are investigated. The simulation result are presented and analyzed which is enough close to theoretical.

CHAPTER 6

In the structure of this Thesis, unmistakably the fundamental targets and goals set out at the start of this Thesis have been accomplished. This part abridges the work did inside this Thesis by giving an outline of the commitments made in every individual Chapter. Conceivable future parts of research are called attention to towards the finish of this Chapter.

6.1 Conclusion

The objective of this Thesis was got the commitment to the field of elite widespread dynamic components for the simple sign preparing circuits worked in current-mode, voltage-mode and blended mode. In the most recent decade, current conveyor and its variations got an incredible significance for acknowledging analog signal processing circuits. It is demonstrated that current conveyor can possibly fulfill the prerequisites set out in analog signal processing. The popularity of current conveyor is attributed to their simple circuitry, wider bandwidth and linearity. In chapter 1, Analog signal processing, a brief history of current conveyor alongside a prologue to its variations is introduced. Voltage-mode and current-mode are likewise introduced.

In chapter 2, the definition and execution of superior all inclusive dynamic component for example DXCCII in CMOS innovation are exhibited. What's more, useful confirmation of DXCCII for example DC analysis, AC analysis and Transient analysis to check the general execution of the circuit are exhibited.

In chapter 3, DXCCII based four fundamental amplifiers for example current, voltage, trans-impedance, trans-admittance are proposed and analyzed. Which uses less number of passive component and works precisely.

In chapter 4, DXCCII based Variable gain amplifier and programmable gain amplifier are proposed. Current-mode digitally controlled variable gain amplifier (VGA), voltage-mode digitally controlled variable gain amplifier (VGA) utilizing DXCCII. To accomplish the required gain control range and step, two VGA stages are cascaded. The principal stage works in coarse gain control while the second VGA stage gives fine gain control. The VGA

circuit is along these lines working in a coarse and fine plan. Reenactment results are displayed and talked about. A novice programmable gain amplifier configuration working in trans-impedance mode has been proposed. The plan utilizes variable gain stage utilizing DXCCII pursued by R-2R ladder network to accomplish coarse and fine gain tuning of the amplifier. Due to nuanced mixed-signal processing utilized in this structure, a wide scope of increases can be accomplished utilizing the control words with a high level of exactness.

In chapter 5, Novice Current-mode first-order all-pass filter utilizing a single DXCCII and four passive components, (grounded capacitors and grounded resisters), are proposed. The proposed all-pass filter has appealing highlights, for example, a single dynamic segment and utilization of just grounded capacitors and resistors. Subsequently, they are reasonable for IC implementation. The exhibited current-mode filter has high information impedance and high output impedance. Non-ideal gain and parasitic impedance impacts of the DXCCII on the exchange capacity of the proposed filter are researched. The simulation result is introduced and examined which is sufficient near theoretical.

6.2 Future Scope

The IC execution of the displayed circuits is most characteristic future issue.

The device exhibited in this Thesis depended on at least 0.18 μm CMOS innovation. The device may further be updated utilizing nanometer CMOS innovation. This would make the dynamic components dependent on these plans reasonable for use in portable communication applications in this way limitlessly expanding their adaptability and acknowledgement.

The bandwidth of the proposed circuit is low; the bandwidth can be improved later on by utilizing bandwidth upgrade methods.

To whole up, there is still a great deal of degrees in analog signal processing region to exploit the upsides of superior universal active elements in the forthcoming advancements for further research.

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