# ENHANCED EMIR FLOW DEVELOPMENT FOR ADVANCED TECHNOLOGY NODES

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OF

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IN
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I, **RASHMI SINGH**, **2K17/VLS/17** student of M.Tech (VLSI), hereby declare that the M.Tech Thesis titled "**Enhanced EMIR flow development for advanced technology nodes**" which is submitted by me to the Department of Electronics and Communication, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma, Associateship, Fellowship or other similar title or recognition.

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# CERTIFICATE

I hereby certify that the M.Tech Thesis titled "**Enhanced EMIR flow development for advanced technology nodes**" which is submitted by **RASHMI SINGH**, **2K17/VLS/17** ECE Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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**RASHMI SINGH**

# ABSTRACT

Electromigration and IR drop effects have been a reliability concern in IC design. Electromigration damages in interconnects is a well-known bottleneck of integrated circuits, as it is responsible for performance degradation, affecting parameters like delay, power and frequency. EMIR analysis is performed on two advanced technologies, BiCMOS technology and 3D Integrated technology. Main features of these technologies are discussed for better understanding. Testcases are made for EMIR analysis on these technologies. Schematic and testbench of testcases are made using Cadence Virtuoso. Simulations for EMIR are done on the layout of the testcase. EMIR analysis has been performed using three EDA tools, Synopsys Customsim-RA, Cadence VoltusFi and Ansys Totem. Concise EMIR results are presented for Cadence VoltusFi. Development of EMIR flow is done using QA Machine. Testcases for both the technologies are uploaded on QA Machine for automated testing of the EMIR flow. QA Machine test report is also presented.

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| CMOS | Complementary Metal Oxide Semiconductor |
| CAD | Computer Aided Design |
| EDA | Electronics Design Automation |
| VIA | Vertical Interconnect Access |
| EM | Electromigration |
| ESD | Electrostatic Discharge |
| CDM | Charged Device Model |
| RA | Reliability Analysis |
| LDD | Lightly Doped Drain |
| EMIR | Electromigration and IR drop |
| STI | Shallow Trench Isolation |
| DGO | Double Gate Oxide |
| DRC | Design Rule Check |
| LVS | Layout Vs Schematic |
| DRM | Design Rule Manual |
| DSPF | Detailed Standard Parasitic Format |
| P&R | Placement and Routing |
| PDK | Process Design Kit |
| DSP | Digital Signal Processing |
| RAM | Random Access Memory |
| PVT | Process Voltage Temperature |
| ASIC | Application Specific Integrated Circuit |

# CHAPTER 1

# INTRODUCTION

During the last few years, Complementary Metal Oxide Semiconductor (CMOS) technology has been increasingly important in the world of integrated circuit industry. In its initial phase, the technology of making both polarity devices on the same substrate was used for very low power devices such as watches. As the processing technology used in the fabrication of CMOS circuits was applied to general system designs in limited quantities.

The electronics industry has made an exceptional growth over the last few years, majorly due to the rapid development in integration technologies and large-scale system design. The utility of integrated circuits in high–performance computational design, communication systems and consumer electronics is increasing at a very fast rate. The driving force for fast development of this field is the growing need for high computational and information processing power.

CMOS integrated circuits are majorly used to develop random access memory (RAM) chips, digital signal processor (DSP) chips, microprocessor chips, and application-specific integrated circuits (ASIC) chips. In this mobile computing generation with increased System on Chip (SoC) complexity, consumers expect smaller, higher performing devices with increased battery life. The chips that are used to make these products must be functionally rich and power efficient. These changes imply applying advanced power tradeoff which enables a designer to meet system power requirements by analyzing, reducing, and tracking down power through the entire design cycle dealing with tighter design rules (such as sub-1V power supplies). On the other side, for design engineers ,the time-to-market requirement

continues to be competitive, which makes the end-of-design cycle's power signoff step as difficult as ever for a successful tape-out.

The presence of fast and accurate models at every stage of a design is extremely important if SoC designers want to succeed in designing chips having embedded memories. Hence, embedded memory characterization is one of the important concern for design engineers. The switch to new process geometries is exacerbating the challenge – the number of memory instances used in a single chip grows significantly at advanced technology nodes. The parasitics are also increasing at advanced process geometries which start effecting the timing performance of the device. In order to improve the full range of process, voltage, and temperature corners (PVTs) and to meet the sensitivity of process variations, designers need to perform more and more memory characterization runs.

Computer aided design (CAD) tools provided by Electronic Design Automation (EDA) vendors are used for design optimization and automation. Computer simulation is an essential part of the design process, both for performance validation and for fine-tuning of circuit design. The semiconductor market has accepted the fact that the architecture of the memory structure has a considerable effect on the performance of the system and any performance loss of memory IP cause the failure of the entire chip.

Reliability Analysis plays an important role at lower technology nodes. Since, metal interconnect width is decreasing exponentially, thus overall interconnect area is shrinking. Because of the increase in integration density of the chip, there are more wires on the chip that are susceptible to electromigration effect. Chemical diffusion, material migration, antenna effect, hot carrier effect comes into picture as we go below 28nm. This causes reliability issues.

## 1.1 MOTIVATION

As the reliability concerns is increasing, electromigration is an important phenomenon to consider for short channel devices. As we are moving towards lower technology nodes, electromigration and IR drop plays an important role in defining the reliability of a design

chip. EMIR analysis needs to be performed post layout simulations to take into account possible damage caused to the design by electromigration. The flow for the verification of EMIR needs to be defined and developed to improve the methodology for design flow of the chip.

## 1.2 OBJECTIVE

To study Electromigration and IR drop, delve into the electronic design automated tools and techniques used for their analysis and to improve the flow for electromigration and IR drop verification at advanced technology nodes.

## 1.3 METHODOLOGY

Electromigration and IR drop analysis is necessary for reliability analysis of the design. The following methodology is followed for the development of EMIR flow:

1. Creation of schematic, testbench and layout for the testcase for the particular technology node (BiCMOS and 3D integrated technology) on Cadence Virtuoso.
2. Post layout simulations performed on the layout of the testcase using ST PLSkit
3. Electromigration and IR drop analysis on the extracted netlist using Emir tools which are Synopsys CustomSim-RA, Cadence VoltusFi and Ansys Totem. Analysis of the reports generated by the EMIR tool.
4. Uploading of the testcase on ST QA Machine for automatic verification of the flow.
5. Checking the reports generated by the QA Machine.

## 1.4 THESIS ORGANISATION

This thesis is organized into five chapters, of which the introduction covers the first chapter. The rest of the thesis is organized as follows:

**Chapter 2** describes the effect of electromigration and need for its analysis. It describes the role of EMIR in reliability analysis of the chip.

**Chapter 3** presents the BiCMOS and 3D integrated technologies on which the EMIR analysis is performed.

**Chapter 4** discusses the EMIR tools used for analysis. They are CustomSimRA, VoltusFi and Totem.

**Chapter 5** describes the QA Machine and its working, which is a automatic testing machine.

# CHAPTER 2
# LITERATURE OVERVIEW

Advancement in process technology nodes and design styles are increasing the effects of electromigration (EM) and IR-drop phenomenon on the reliability and performance of analog, RF Designs, mixed-signal, memory and custom digital IP blocks. Extensive IR drop may result in timing violations and/or functional failures. Electromigration mechanisms are more complicated than IR drop and induce an irreversible failure of electrical discontinuities (open circuits) or short circuits due to ion migration.

This chapter describes the phenomenon of electromigration and IR drop and reports how the chip damage is caused by them. It explains the need to do EMIR analysis. It also discusses the experiment done by I.A.Blech to define blech length.

## 2.1 ELECTROMIGRATION

When current is passing through a conductor, the electrons move from one end to the other end. They transfer some of their momentum to the metal atoms and gradually the metal atoms also move. This is called electromigration. This phenomenon is not of much importance when the current densities are low. In IC chip the current densities are very high and electromigration can cause failure of a circuit due to ion migration.

Electromigration (EM) is the gradual displacement of metal atoms; it occurs when the current density is high enough to cause the drift of metal ions in the direction of the electron flow. This creates void when the outgoing ion flux is more than the incoming ion flux, resulting in

an open circuit. And creating a hillock when the incoming ion flux is more than the outgoing ion flux, resulting in a short circuit.

EM is the transport of material in a conductor under the influence of an applied electric field. Transport happens due to the momentum transfer from collisions between conducting electrons and diffusing metal atoms. The net force exerted on a single metal ion in a conductor has two opposing contributions which are Direct Force and Wind Force.

Direct Force is the electrostatic pull being exerted on the metal ion core due to application of an electric field. The direction and magnitude of the electrostatic pull depend on the charge on the ion core. When the overall electron drift velocity is established, the force exerting on the ions due to electron scattering is in the direction of the electron flow is known as the wind force. In good conductors such as Al and Cu Wind force is the dominant force felt by the metal ions resulting in atomic migration towards the anode.

Net force is the summation of wind force and direct force. It is mathematically described using the following Equation (2.1). Fig 2.1 [2] shows the forces acting on the metal ion in a conductor.

$$F_{net} = F_{wind} + F_{direct} = ( Z_w + Z_d )\, e j \rho = Z^* e j \rho \qquad (2.1)$$

Where,

$F_{direct}$ is the Electrostatic interaction with the field ,
$F_{wind}$ is the Momentum transfer from the carriers ($e^-$) ,

$Z_w$ is the wind valence ,

$Z_d$ is the direct valence ,

$Z^*$ is the effective charge number ,

$e$ is the elementary charge ,

$j$ is the current density ,

$\rho$ is the metal resistivity ,

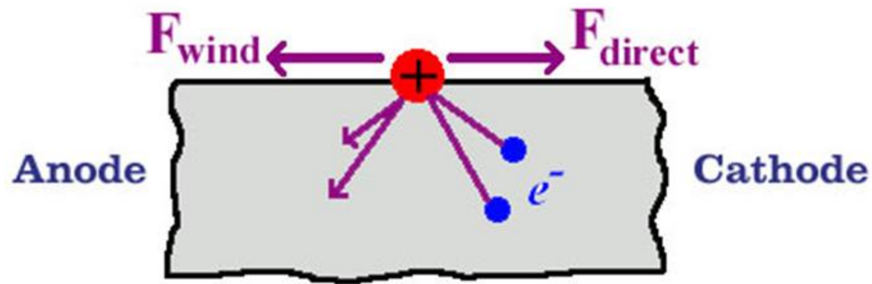


Fig 2.1 Forces acting on a metal ion [12]

### 2.1.1 DAMAGE CAUSED BY ELECTROMIGRATION

Elecrtromigration is of two types, Uniform and non-uniform electromigration. Uniform electromigration within the metallization lines, if it is maintained, would not cause damage. In steady-state, no damage should be observed other than at the beginning and end of the metallization line. This is because, along the metallization line, the number of atoms coming in a given local volume is equal to the number of atoms going out of the volume as shown in Fig 2.2 [2]

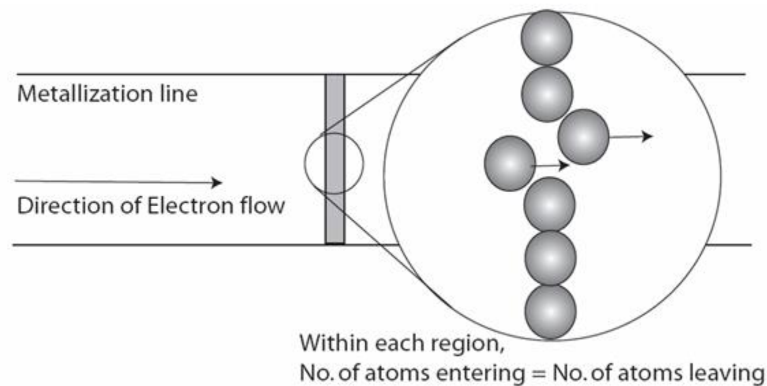


Fig 2.2 Uniform Electromigration [12]

In non-uniform electromigration, the amounts of matter leaving and entering a given volume are unequal, the resulted accumulation or loss of material creates reliability issues. Divergences in atomic flux causes damage to the metallization lines as shown in Fig 2.3 [8].

A Hillock or a whisker is created when the atomic flux entering into a region is more than the atomic flux leaving it. The matter gets accumulated in the region. A Void is created if the flux leaving the region is more than the flux entering. The depletion of matter ultimately creates a void. Regions of void formation are generally associated with neighboring regions of material accumulation, as metal atoms are replaced from one region to the other.

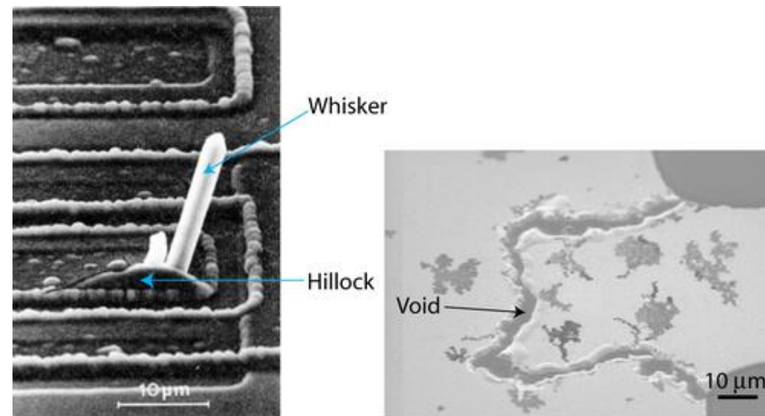


Fig 2.3 Effect of non-uniform Electromigration [12]

Source of images: (left) Microelectronic Materials by CRM Grovenor, IOP Publishing Ltd, Bristol (UK); (right) Dr Lo Veng Cheong

### 2.1.2 BLECH LENGTH

The possibility of electromigration damage depends not only on current density, but it also depends on the absolute length of the conducting segments. Electromigration damage can be prevented if the product of the current density, j, and the line length, l, is below a critical value.

I.A.Blech designed an experiment in which conductor islands were deposited on a titanium nitride (TiN) film and it was stressed at a high current density. Since the conductor resistivity was very less as compared to the TiN layer, the conductor stripe carried most part of the current. The resulting movement of the ends of the stripe was measured. By this experiment, the electromigration induced drift velocity is determined by the following equation.

$$vd = \frac{D_a|Z^*|epj}{kT} \tag{2.2}$$

Where,

Da is atomic diffusivity

k is Boltzmann's constant ,

T is temperature ,

Blech observed that only the upstream end (in relation to the electron flow) of the line moved according to the above equation, and that the upstream end stopped moving, when the stripe was reduced to a certain length, which is known as the blech length. He also observed that no drift was detected below a threshold current density.

Electromigration of atoms, usually results in a buildup of stress within the metallization line. Regions of compressive and tensile stresses develop, resulting in a variation of stress (stress gradient) along the line. This stress gradient contributes to the gradient in the chemical potential, and thereby effects the mass flux, J. Equation (2.3) shows that a gradient of mechanical stress acts as driving force against electromigration.

$$J = \frac{DC}{kT}\left(Z^*epj - \Omega\frac{\Delta\sigma}{\Delta x}\right) \tag{2.3}$$

$$\frac{\Delta\sigma}{l} = \frac{Z^*epj}{\Omega} \tag{2.4}$$

$$(jl)_c = \frac{\Delta\sigma\Omega}{Z^*e\rho} \tag{2.5}$$

Where,

D is vacancy diffusivity ,

C is the vacancy concentration ,

Ω is the atomic volume ,

σ is the hydrostatic stress ,

There is no electromigration damage below (jl)c which is the blech length . An estimation can therefore be made for the longest conductor, which would have “infinite” life.

### 2.1.3 EFFECT OF ELECTROMIGRATION ON METALS

**CONTACTS**

Electromigration causes damage to the metal contacts between the aluminum layer and source/drain. EM creates accumulation and depletion of the aluminum at the point of contact as shown in the Fig. 2.4.

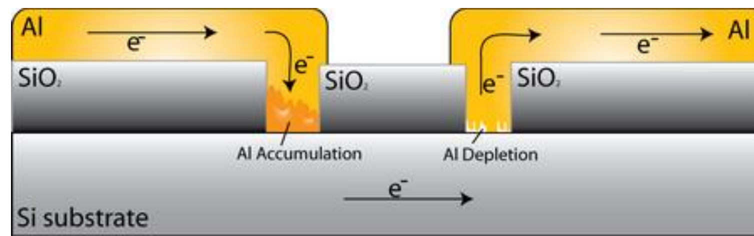


Fig. 2.4 Effect of Electromigration on metal contact [11]

**VIAS**

VIA (Vertical Interconnect Access) is an electrical contact to connect two metal layers in a physical electroic circuit. Due to increased current density, EM causes depletion of the Via and creates void. As shown in Fig 2.5, Via is connecting two metal layers and depletion of electrons is creating void in the connection.

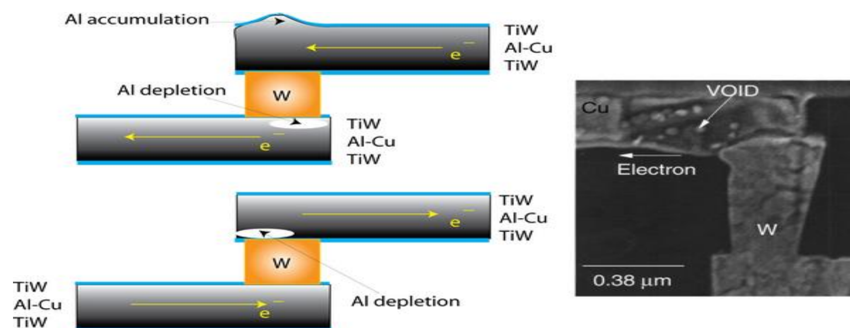


Fig 2.5 Effect of Electromigration on Vias [11]

## 2.2 IR DROP

IR-drop refers to the amount of decrease (increase) in the power (ground) rail voltage due to the resistance of the devices between the rail and a node of interest in the circuit under test. During the initial design phase of the circuit, it is a general practice to define maximum per-rail static voltage drop tolerable. The greater this value, the worse the speed performance of the circuit. This degradation in performance intensifies with increase in test frequency. In a similar way, lower the supply voltage, poorer the performance. The precise physics behind the failure may differ. In some situations, it is proposed that a large delay between the last shift event and the first capture cycle may allow the power supplies to settle "too much", so that they are unable to respond with enough dynamic range to supply a clean clock pulse to the clock trees and scan flip-flops under test.

There are two ways to characterize the IR-drop in a design, statically and dynamically, in the same way as that of power consumption. In the case of static IR-drop, the analysis tool extracts the parasitic resistances of the power/ground networks, connects current sources at cells to represent average power consumption, and solves this DC network to obtain the average IR-drop at each node. In this case, the IR-drop is a static quantity and a function which depends only on the amount of logic between the node and the rail.

Quantification of dynamic IR-drop is a more difficult and costlier as compared to static IR-drop. The amount of effective resistance generated by a transistor varies with change in its input conditions. This is specifically true if the resistor is modeled in a non-ideal way, for e. g., a non-rail voltage on the gate of the transistor. These variations will definitely be affected by the state of the circuit. Measuring dynamic IR-drop requires a simulation-based technique where circuit state values are maintained and then the impedance/capacitance seen by the node is calculated for that particular circuit state. This technique, while possible, is fairly computationally restrictive. It may become mandatory if the level of integration continues to increase at the present rate.

## 2.3 NEED FOR EMIR ANALYSIS

There are various reasons to do EMIR analysis after post layout simulations. In order to take into account the damage caused to the chip by EMIR. As the technology is scaling and number of devices integrated on the chip is increasing day by day, there is increase in temperature and current density which causes EM in the chip. Increase in the length of interconnections makes wires and VIAs more susceptible to EM effects. It is difficult to estimate the potential effects of reliability problems manually. Therefore, we need to perform EMIR analysis using EMIR tools.

EMIR analysis forecast issues due to EM effect before going to silicon production. EMIR tools use optimization of signal nets, power wires and VIAs to reduce overall numbers of incremental fixes.

# CHAPTER 3
# TECHNOLOGY USED

In this chapter, features of BiCMOS technology and 3D Integrated technology is defined. These technologies are used to create testcases for EMIR analysis which is explained in the next chapter. These technologies are chosen for analysis as they are the advanced technology nodes in VLSI industry. BiCMOS technology provides speed-density-power performance by combining BJT and CMOS technology. 3D Integrated technology provides improved performance and functionality by stacking silicon wafers and interconnecting them vertically using through silicon VIAs , so that they behave as a single device.

## 3.1 BICMOS TECHNOLOGY

BiCMOS is an advanced semiconductor technology which integrates two different semiconductor technologies, the bipolar junction transistor and the CMOS transistor, in a single integrated circuit device. Bipolar junction transistors offers excellent properties for high-frequency analog amplifiers such as high speed, high gain, and low output resistance, whereas CMOS technology offers excellent properties for constructing simple, low-power logic gates with high input resistance. The BiCMOS Heterojunction Bipolar Transistor (HBT) allows a much higher cut-off frequency as compared to bulk CMOS, at a given technology node. In order to have similar frequency characteristics, bulk CMOS designs have to use much smaller process technology nodes, which forces compromises on the design. In most of the cases this leads to higher cost and lower overall performance. Fig. 3.1 shows the circuit for an inverter made using BiCMOS technology.

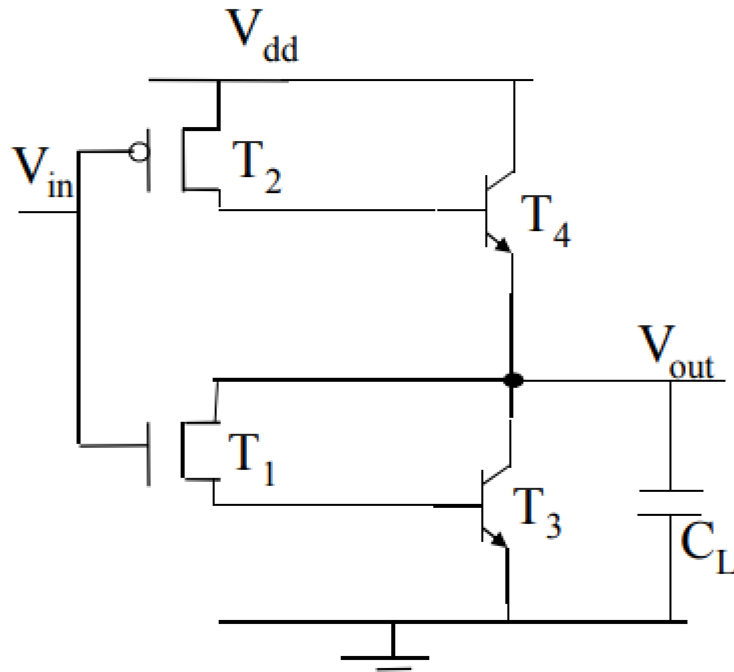


Fig. 3.1 BiCMOS Inverter [9]

**3.1.1 Technology Features**

BiCMOS is a130nm process technology used for analog applications.

**3.1.1.1 Key Features**

Starting material is 200 mm (8 inch) P-type, <100> orientation silicon wafer with resistivity between 10 Ohmscm and 20 Ohms-cm. In order to reduce Active pitch, Shallow Trench Isolation (STI) is used for Active isolation. Deep Trench Isolation is used for EPI substrate in bipolar modules. Retrograde Twin Wells allows getting a lower well sheet resistance and enhancement of latch-up behavior, compared to conventionally diffused wells. An additional advantage is a very good control of short parasitic field transistors. Triple Well (NISO) allows isolating PWELL from the substrate. Dual Gate Oxide is used in this technology. It has N+/P+ poly gate which allows symmetrical design of N-Channel and P-Channel devices. SiGe-C Selective Epitaxial Base Growth is used in bipolar transistors to achieve very high electrical performances. It has poly and active resistors. Silicide protection is used to prevent

silicide formation over active areas, for ESD protection. This process is also used to fabricate poly resistors. Chemical Mechanical Polishing is done for improved planarization (on DTI, STI, Contacts, Metals and VIAs). Dual Damascene copper Interconnects are used for metal 2 to 4**.** Double single damascene copper interconnect for metal 5T**.** This technology is designed to operate in the temperature range -40°C to +150°C.

#### 3.1.1.2 Power supply

CMOS devices with 2.0 nm of gate oxide thickness (GO1) are designed for 1.2V (1.32V max) applications. CMOS devices with 8.5 nm of gate oxide thickness (GO2) are designed for 4.6V (4.8V max) applications. NPN and PNP SiGe Heterojunction Bipolar Transistors (HBT) are designed for Low Voltage (LV) and High Voltage (HV) applications. The 2.0nm thin oxide MOS devices are targeted for nominal power supply voltages of 1.2V. Accounting for a 10% tolerance, the process/devices are qualified for a max power supply of 1.32V. The 8.5nm thick oxide MOS devices are targeted for nominal power supply voltage of 4.6V. The process/device is qualified for a max power supply of 4.8V.

#### 3.1.1.3 Front-end main features

N+/P+ buried layers are formed before a N-epitaxial layer growth on P-type substrate to reduce the collector access resistance. For CMOS core process, Shallow trench isolation (STI), twin-tub, triple well (NISO), and single poly are used. Double poly architecture and SiGe-C epitaxial base growth are used to reach very high electrical performances in NPN and PNP bipolar transistors. The core process features a double gate oxide (DGO): 2.0nm for digital and 8.5 nm for analog and high voltage devices, cobalt silicide on junctions and polysilicon gates and lines, and resistors on active and interconnect N+ or P+ poly.

#### 3.1.1.4 Back-end main features

Back-end has 5 metal levels. The metallization variant is 5M_2X_1B_1T_AP. It has five metal levels out of which three are thin, one is medium, one is thick and one Alucap where

mM-xX-bB-tT refers to a process with a total of m metals out of which x are fine pitch, b are intermediate pitch and t are thick metals. The product designs contains markers to identify the metallization choice.

Damascene Copper is used for metal 1 to last metal. Metal 1 to metal 3 are thin metal layers. Metal 4 and 5 are thick metal layers. Metal4B is thicker than metal3, metal 5T is thicker than metal4B. Fluorinated $SiO_2$ inter metal dielectrics up to metal3 and undoped $SiO_2$ inter metal dielectrics from metal4B to metal5T. Aluminium layer (ALUCAP) on top of last Copper level is mainly used on Pads. It is also used for routing if necessary.

### 3.1.2 ROBUST DESIGN RULES

In today deep-submicron technologies, more and more plasma enhanced process steps are used. Plasma steps are subjected to non-uniformity throughout a wafer. This can cause local non-equilibrium between electron flux and ion flux, creating either positive or negative charges to be abnormally generated on the wafer surface. When collected by conducting wires directly connected to gate of MOS devices, these charges can have several impacts of different gravity. They are as follows:

- Vt shift between Metal1 test and Metal 5T test, particularly on thick oxide.
- Oxide degradation, gate leakage increase.
- Time to Dielectric Breakdown and Hot Carrier performance degradation.

Charging can occur during the process at several steps. The data extracted from dedicated tests structures, and the failure mode analysis have indicated that the main contributors can be over etch part of the poly etch, after the poly lines have been separated; Resist removal; Over etch part of the metal lines and VIAs etch into the inter metal dielectric; Sputter etch before metal deposition; very beginning of metal deposition, until the seed layer is continuous.

Dielectric deposition is well admitted that most of the charging is occurring during the first 1000A deposition. It is important to understand that when the metal is deposited and not yet

patterned, it shorts all the nodes, and in particular it connects the gates to the substrate, ensuring the full protection against charging.

#### 3.1.2.1 Latch-Up Protection

It is important to note that as minimum dimensions are decreasing, resistance of minimum straps is increasing; so rails should be preferred to minimize size straps. A diode in forward mode can generate many carrier pairs. It is an emitter and as such it can easily trigger a Latch-Up event. Its usage is therefore strongly discouraged. If it is used, extreme care must be taken regarding Latch-Up containment

#### 3.1.2.2 ESD Protection

In generation processes, contact to poly space in output buffers was increased to avoid metal melting in the contacts during an ESD event. This would also reduce current crowding. Some major design related parameters are critical for ESD performance. In BICMOS salicided active areas make current crowding more critical, so ESD performance is increased by preventing salicide formation. The rule is process related, it does not guarantee ESD performance. A larger value, in particular on the drain side of the transistor, is necessary to achieve the ESD performance required for each product.

Gate length of the transistor is minimum. It has been observed in other processes that the optimum ESD performance occurs for the minimum channel length, due to the better activation offered by the parasitic NPN transistor. This is the reason why it is advised to use the minimum gate length for ESD protection devices in IO's. Large Width of the transistor, due to current density considerations, it is advised to use large transistors. N-MOS transistor has been proved to be efficient as a clamping device without LDD structure. So LDD structure is suppressed. A complete I/O solution will be characterized on silicon realized during the process development, for more information see the documents provided with the I/O library

### 3.1.3 RELIABILITY DESIGN RULES

The transistor and interconnect reliability rules presented in the following sections include several assumptions about device application requirements, including expected use time, junction temperature and acceptable cumulative percent failure at the end of product life. In particular, target applications are assumed to specify a cumulative failure of 0.1% product failure after 10 years cumulative operating period at junction temperatures of 150°C.

#### 3.1.3.1 Electromigration Design Rules

Current rules limits in metallization wiring are generated to ensure reliable operations over a prescribed time period without significant electromigration (EM) damage. The proposed current limits are generated by considering 0.1% failure over 10years at 150°C.

**Terminology and symbol definitions**

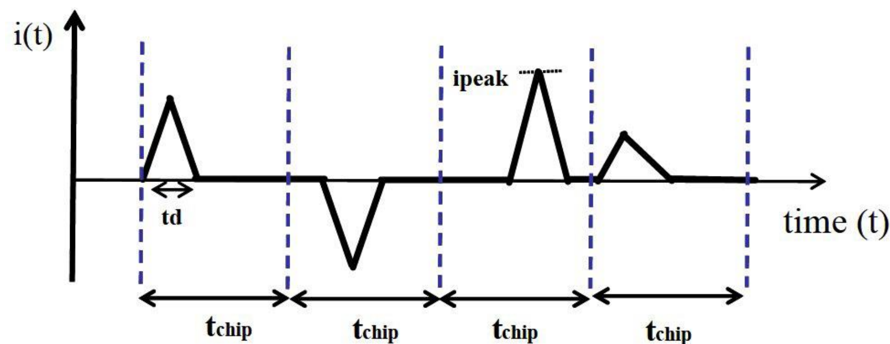


Fig. 3.2 Terminologies and symbols used in EM [11]

Where,

Tchip is the minimum time between successive current switching operations,

Fchip is the Operating chip frequency (tchip=1/Fchip) ,

td is Pulse duration which is the duration of current flow (based on average current during non-zero current flow),

idc is Average DC current,

irms is RMS current ,

ipeak is Peak current ,

#### 3.1.3.2 EM fail types

Rules are defined to protect against three types of current-induced fails: standard EM, local heating enhanced EM and local melting. For each one, a maximum current rule is defined: Idc, Irms and Ipeak respectively. For any current signal i(t), ALL conditions (idc < Idc, irms < Irms, ipeak < Ipeak) have to be fulfilled to prevent any type of failure.

Corresponding rule is defined for each type of failure.
For Standard EM, idc < Idc
For EM enhanced by heating, irms < Irms
For Local melting , ipeak < Ipeak

## 3.2 3D INTEGRATED TECHNOLOGY

Three-dimensional (3D) integration is a promising technology to overcome some physical, technological, and economic limits encountered in planar integrated circuits. It can stack different materials, technologies, and functional components vertically. It extends Moore's Law by enabling "More than Moore" applications. Single layer 3D ICs begin with a base wafer onto which additional layers of crystallized silicon, metalized layers and active as well as passive circuitry are added using traditional fabrication equipment, instead of stacking wafers or die to create 3D ICs. The vertical interconnects are formed between layers rather than chips, using VIAs in the nanometer range.

### 3.2.1 TECHNOLOGY FEATURES

The qualification of the technology is performed in the temperature range -40°C to +125°C. 3D Integration is targeted for Low Power to serve battery operated and wireless applications. It is a single IO oxide with single core oxide dual-Vt process. It gives access to standard Vt transistors (SVT), low Vt transistors (LVT), low leakage (high density) SRAM using LP core oxide, and IO transistors (2.5 V) using IO oxide. It uses Copper metallization with 7 metal levels (5 thin and 2 thick) and ultralow-K dielectrics. 3D integration consists of stacking 2

chips, a top tire and a bottom tire, together through hybrid bonding techniques with HBMetal and HBVia. CMOS chips are used as the bottom tire.

Only one metallization is supported which is7M-4X-0Y-2Z. There are seven metal levels out of which 4 are thin and 2 are thick (standard process) where mM-xX-yY-zZ refers to a process with a total of m metal layers out of which x are fine pitch, y are intermediate pitch and z are thick metals. The product designs contain markers to identify the metallization choice.

#### 3.2.1.1 Key Features

3D Integration (3DI) corresponds to the stacking of 2 chips via hybrid bonding using HBMetal and HBVia. Shallow Trench Isolation (STI) is used for active isolation to reduce active pitch (OD pitch). Retrograde Twin Wells allow getting a low well sheet resistance and enhancement of latch-up behavior compared to conventionally diffused wells, and a very good control of short parasitic field transistors. Triple Well (Deep N-Well) allows isolation of the p well from the substrate. Thick Gate Oxide is used for IO compatibility. N+/P+ Poly Gate allows symmetrical design of N-Channel and P-Channel devices. Chemical Mechanical Polishing is used for improved planarization (on STI, Contacts, Metals and VIAs). It has dual damascene copper interconnects.

#### 3.2.1.2 Power Supply

3D Integration is designed for 1.1 V applications with 2.5 V capable IO's. The 1.7nm thin oxide MOS devices are targeted for nominal power supply voltages of 1.1V. Accounting for a 5% tolerance and 1.2V overdrive supply voltage, the process/devices is qualified for a maximum power supply of 1.26V.

The 5.0nm thick oxide MOS devices (2.5V IO) are targeted for nominal power supply voltages of 2.5V. Accounting for a 10% tolerance and 3.3V overdrive supply voltage, the process/devices is qualified for a maximum power supply of 3.63V.

#### 3.2.1.3 Front-End main features

Shallow trench isolation is used for isolated P-Well (DNW) twin-tub, single poly CMOS process using a type (100) P-substrate in <100> orientation 45° rotated EPI 6um. Nickel silicide is used on junctions and polysilicon gates and lines, and for resistors on active and interconnect N+ or P+ poly. It has Dual Vt transistors. IO’s using 50 Å gate oxide for 2.5 V.

#### 3.2.1.4 Back-End main features

Back-End has 7 metal levels. Damascene Copper is used for metal 1 to last metal. Thick metal layer are used for power, clock, busses and major interconnect signal distribution. Tight pitch levels are used for routing on thin copper for the other metal levels underneath. Ultra-low K (<2.6) inter-metal dielectrics is used for thin metal layers.

# CHAPTER 4
# EMIR ANALYSIS

Since the cost of failure after the chip fabrication is enormous, detailed analysis and validations are done using EDA tools to ensure minimum silicon failure. This chapter is devoted to the understanding of the flow used for EMIR analysis. Analog Design flow is described to provide knowledge of various chip designing steps from schematic to different checks performed on the design. Different EMIR tools and their analysis techniques are also discussed in this chapter.

## 4.1 ANALOG DESIGN FLOW

A Design Flow in VLSI is the sequence of processes/steps involved in the making of an integrated circuit. The design flow for a digital IC and an analog IC is completely different. In analog design flow, we start from schematic of the design and go up to different checks performed on the design. All the steps involved in the analog design flow are described in 4.1.1 for detailed understanding of the flow.

### 4.1.1 STEPS FOR ANALOG FLOW

In Fig. 4.1, the steps of analog flow, followed for integrated chip designing are shown in the order.

Step 1: Migration
The first step is to migrate the design to the technology node for which we want to do the analysis. The specification of the design usually has information about the detailed functional

requirements, the minimum operating speed, the maximum power, area and other robustness and reliability requirements. The detailed specifications for each of the sub-blocks are also derived. The specifications which are same for the new as well as previous technology node remains same, rest are varied according to the present technology node. Migration helps in reducing the time spent on the design flow.

Step 2: Schematic Capture

After we have specifications for the technology node, schematic of the designed circuit is generated. It is created with the help of a schematic capture tool. Cadence Virtuoso is used for creating schematic.

Step3: Simulation

Simulations ae done on the schematic to check the functionality of the design. These simulations are done by using Analog Design Environment (ADE) integrated in Virtuoso. Spectre simulator helps in detecting and reporting circuit problems. Complete corners and Monte Carlo simulations can be done for fixing variation problems. Aging and Variability analysis are also performed in this step.

Step 4: IP level Simulation

Analog IP level simulations are done by using SPICE or equivalent circuit simulator. These simulations play a major role in designing the IP into the SOC. Analog IP means providing analog circuitry in a form which can be plugged in without analysis.

Step 5: Characterization

In order to have accurate modeling of instance specific voltage variation or temperature gradients, it is necessary to characterize each library at multiple voltages and multiple temperatures, increasing number of corners. At advanced technology nodes, higher yield is required at the cost of area and performance of the IC. Thus optimization of the circuit is required. Characterization and optimization delivers greater throughput with accuracy required for advanced technology node library.

Step 6: Analog P&R

At first, Floor Planning is done to specify the area in the chip where the designing needs to be done. Then the power planning is done to route power nets and ground nets to the design. Now, we place the actual instances from synthesized design in the core area. Routing is performed to make connection of the input/output pins as per the design to perform the required functionality. Routing is done in such a way that the clock reaches every flipflop or instance without any skew i.e, at the same instant.

Step 7: Post layout Simulation

After layout designing, various simulation runs are performed multiple times to meet the timing constraints of the design under test. PLS are explained in detail in section 4.3.

Step 8: EMIR Analysis

Electromigration and IR drop analysis is performed after the layout generation using various EDA tools. Reports are generated by the EMIR tools. These reports are studied to check for EMIR violations in the design and necessary changes are made.

Step 9: ESD/CDM checks

After the EMIR Analysis, layout is verified for Electrostatic Discharge and Charged device model checks. Once the chips are manufactured, each of the chips is again tested for presence or absence of any possible faults during the fabrication process.

Step 10: Current Checks

Current densities are checked in different metal layers to keep them within the limits defined by the process design kit (PDK).

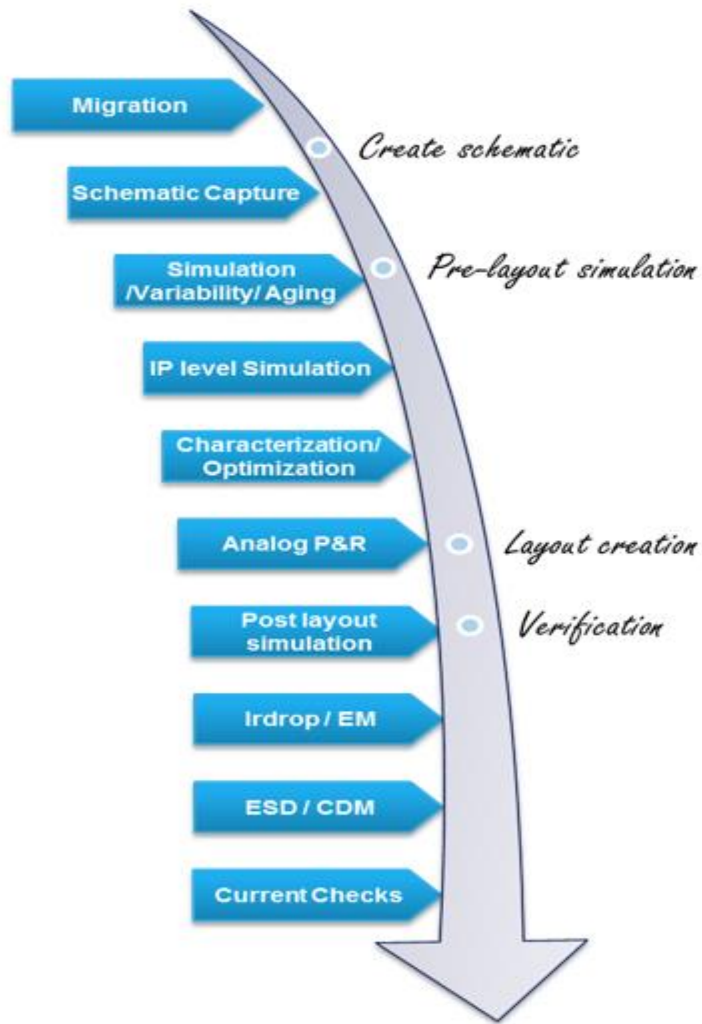


Fig. 4.1 Analog Flow for chip designing

### 4.1.2 ST TOOLS USED IN ANALOG FLOW

The following tools by ST Microelectronics are used in the analog flow at various stages to perform the function defined for them. These tools are integrated in Cadence Virtuoso for smooth working of the flow.

STECCK (Static Electrical Checks): This tool allow us to perform electrical checks at transistor level and detect electrical weaknesses to ensure reliable products and target first silicon success.

ESDCheckKit (Electrostatic Discharge Charge device model Checker): This tool helps in detecting ESD-CDM reliability issues at circuit top level or IP level to ensure first silicon success and avoid re-spin due to ESD-CDM weaknesses for high voltage circuits. It addresses most advanced process nodes, 65nm and below.

VDIKit (Virtuoso Digital Interface Kit) : This kit help us to get the final layout of a small analog block with fully automatic setup, no timing constraints and full floorplan control in CADENCE virtuoso. The final layout is DRC and LVS correct, all these steps are performed at higher speed using VDIKit.

EMIRKit (Electro Migration and IR drop Kit) : This tool allows to build robust power grids during design stage. It verifies if the supply voltage is correct at transistor level. It checks all electromigration DRM rules with all technology node files for electromigration and IR drop flows.

ADOC (Advanced Design Opened Checks) : allow to validate mixed and analog IPs on a given technology node, to guarantee that all necessary rules (DRC, LVS, ERC, ESD and DFM rules) are checked. A final report is made available to compile to all checks results and status. It is also possible to submit DFM reports in LYS (Library Yield System) for visibility & traceability at SoC level.

ArtistKit : It provides many features to the Cadence Virtuoso Simulation Environment such as Models Management methodology and interface for Setup Corners from ADE-L and ADE-XL, Monte-Carlo statistical simulations, Advanced Variability flows, Reliability Analysis for Mentor’s ELDO and Spectre. It also provides Import netlist capability, simulation level management, default view and stop list in analog artist and hierarchy editor.

SAEKIT (Simulation Analog Environment Kit) : It provides the models management methodology and interface for Setup Corners from Synopsys Custom Compiler SAE tool.

PLSKIT (Post Layout Simulation Kit) : It supports the ST Post-Layout Parasitic extraction flow based on Calibre LVS tool from Mentor Graphics and StarRC or Rapid3D interconnect parasitic extraction tools from Synopsys. It uses design kit technology files, either in stand-alone or integrated inside Cadence Virtuoso design platform.

## 4.2 SCHEMATIC AND LAYOUT

Cadence Virtuoso Schematic Editor was used to create schematic for the testcase. The test case has two nmos device, two power supply vdd1 and vdd2 as shown in Fig. 4.2. Testbench is created after the schematic, shown in Fig. 4.3. Layout of the schematic is made in such a way that while routing it has all the metal layers of different lengths so that EMIR analysis for the process technology node, used for the designing, is done properly. Fig. 4.4 and Fig. 4.5 shows the layout of the testcase.

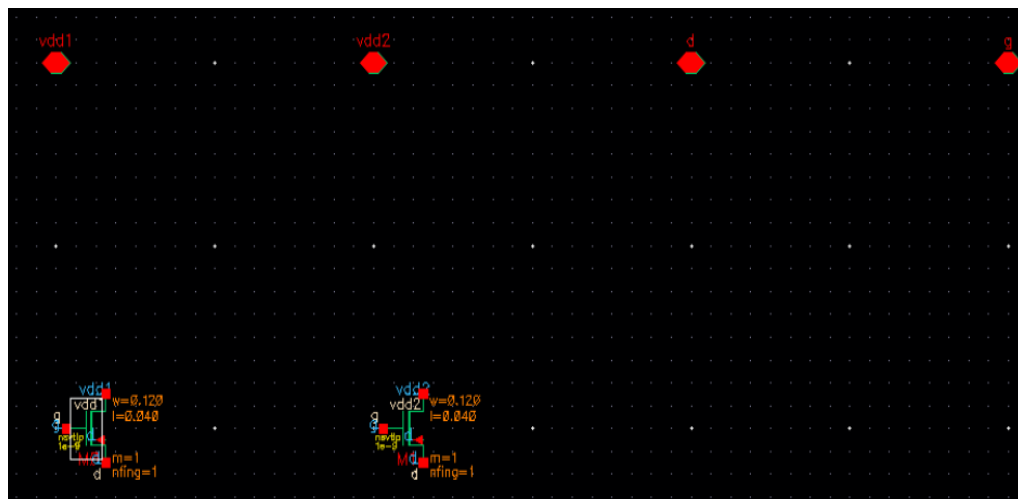


Fig. 4.2 Schematic for testcase

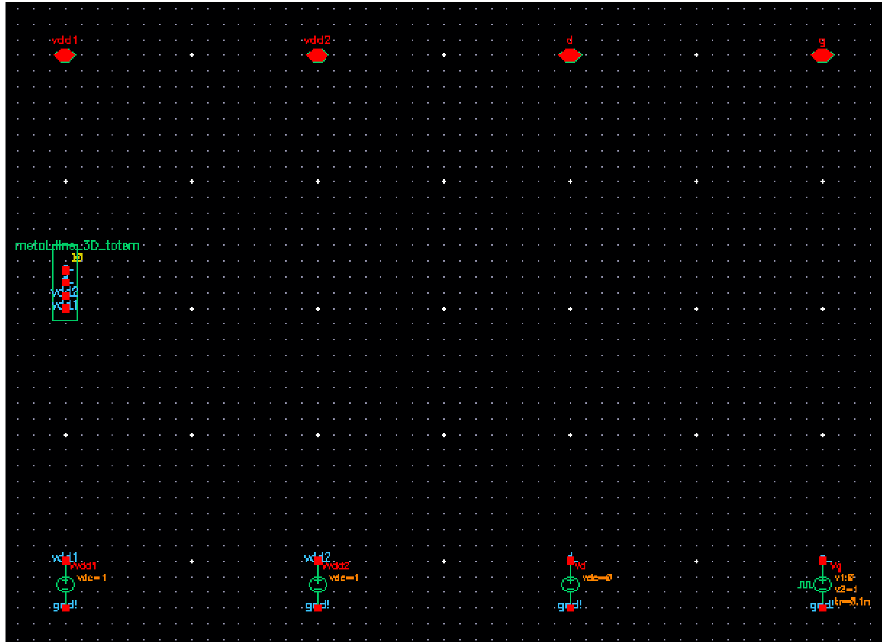


Fig 4.3 Testbench for the testcase

Fig 4.4 Layout for the testcase

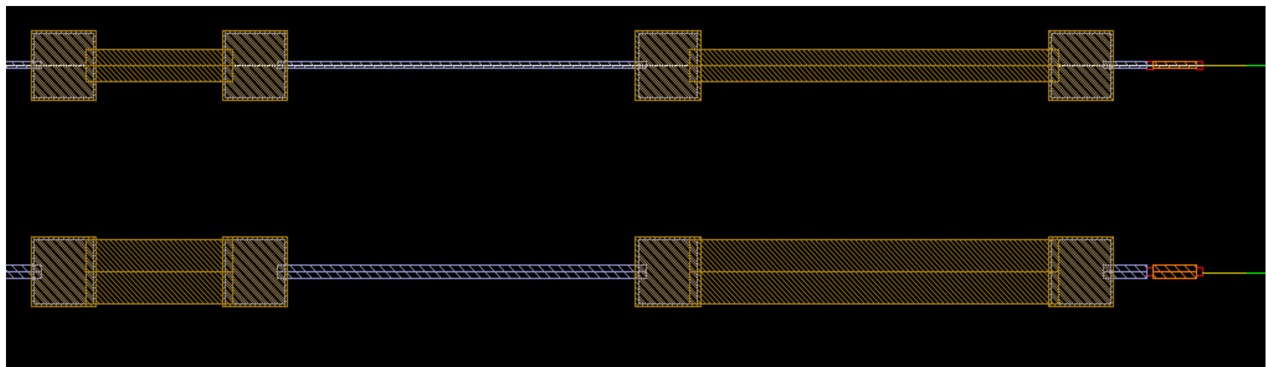

Fig 4.5 Zoomed in picture of Layout

### 4.2.1 INSTANCE INFORMATION

Characteristics Information about the NMOS used in the testcase. It is used from the library cmos045. It has width of 120 nm and length of 40 nm. Its drain area is 1.32e-02 um^2 and source area is 1.32e-02 um^2. It has drain perimeter of 3.40e-01 um and source perimeter of 3.40e-01 um. Other specifications for the NMOS are shown in Fig. 4.6.

Fig. 4.6 Specifications of NMOS

### 4.3 POST LAYOUT SIMULATION

Post Layout simulations are performed on the layout using the ST's PLSKIT. The window for Post layout simulation looks like Fig. 4.7. Post layout simulations gives us the extracted netlist which is required to perform EMIR analysis. The parasitic capacitances are extracted according to the layout design. This is similar to performing simulations for schematic.

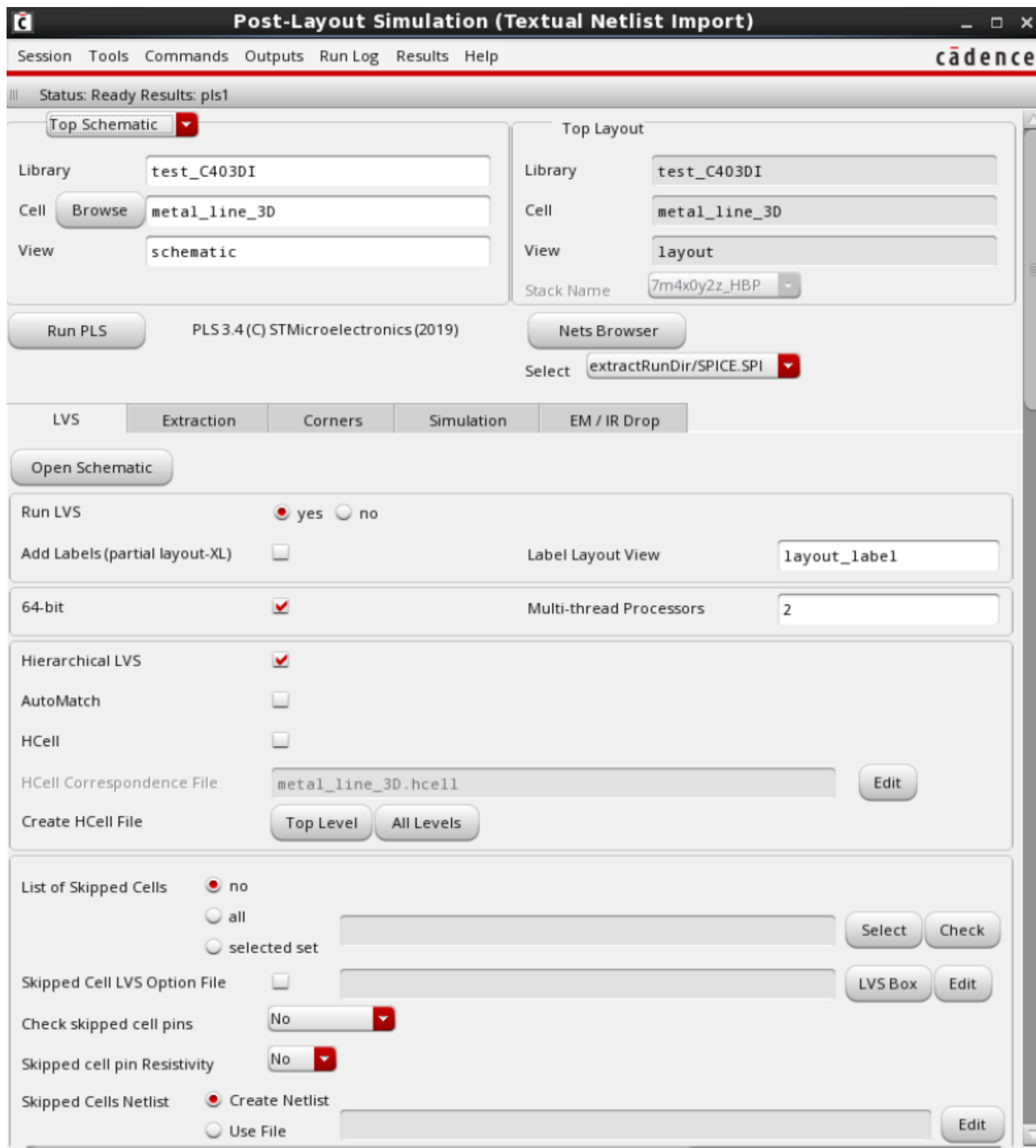


Fig 4.7 Post layout simulation window

### 4.4 EMIR TOOLS USED

IR Drop and Electro Migration analyses are mandatory to ensure design reliability over time. Several solutions in terms of EMIR tools are available at transistor level. Such as:

- Synopsys CustomSim-RA
- Ansys Totem based on Eldo or Spectre or Customsim simulators
- Cadence VoltusFI based on Spectre-aps or on Ams-designer

Several interconnect RC extractors available are Ansys Totem for power/ground supplies, Synopsys StarRC for signal nets and Cadence QRC for all nets. ST's PLSKIT product runs Synopsys StarRC extractor and can run all the EMIR tools (Totem or VoltusFI or CustomSimRA)

EMIR analysis on the testcase is done using three different tools. They are Synopsys CustomsimRA, Ansys Totem and Cadence VoltusFi. In order to do EMIR verification, some steps are followed, which are shown in Fig. 4.8.

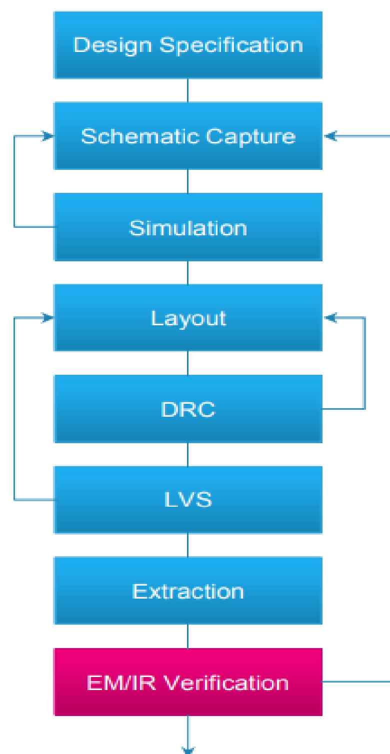


Fig 4.8 EMIR Verification Flow

### 4.4.1 EMIR ANALYSIS USING CUSTOMSIM-RA

CustomSim-RA tool needs to be sourced on the terminal for performing EMIR analysis. Customdesigner is useful to display IR drop and EM maps after simulation. Calibre-RVE can also be used to display display IR drop and EM maps. PLSKit generates the extracted netlists required by CustomSim-RA. Fig 4.9 shows the GUI of CustomSim-RA. Testbench netlist is given as the input to perform the analysis.

Fig. 4.9 CustomsimRA Batch mode window

When selecting EM/IR analysis on either signal nets or power nets, the extraction is performed without reduction and with geometrical information. The following files are generated after the EMIR analysis on CustomSim RA:

• IDEAL.SPI which is SPICE netlist containing devices

• DSPFsignal.SPF is the DSPF with interconnect parasitics of signals nets

• DSPFpower.SPF is the DSPF with interconnect parasitics or power nets

### 4.4.2 EMIR ANALYSIS USING TOTEM

Ansys's Totem is a transistor–level product for analyzing and verifying the design integrity of power/ground structure, substrate, power and signal electromigration, static and dynamic power performance, and electrostatic discharge. The Totem product suite consists of two core applications, Totem-Power Integrity and Totem-Signal EM. Totem-Power Integrity supports early stage power and ground weakness detection, static IR, power EM and dynamic voltage drop analyses. Dynamic voltage drop analyses includes on-chip, as well as package parasitic for accurate modeling of the design and predicting worst-case voltage drop due to issues such as simultaneous switching, insufficient strapping, and inadequate decoupling capacitance.

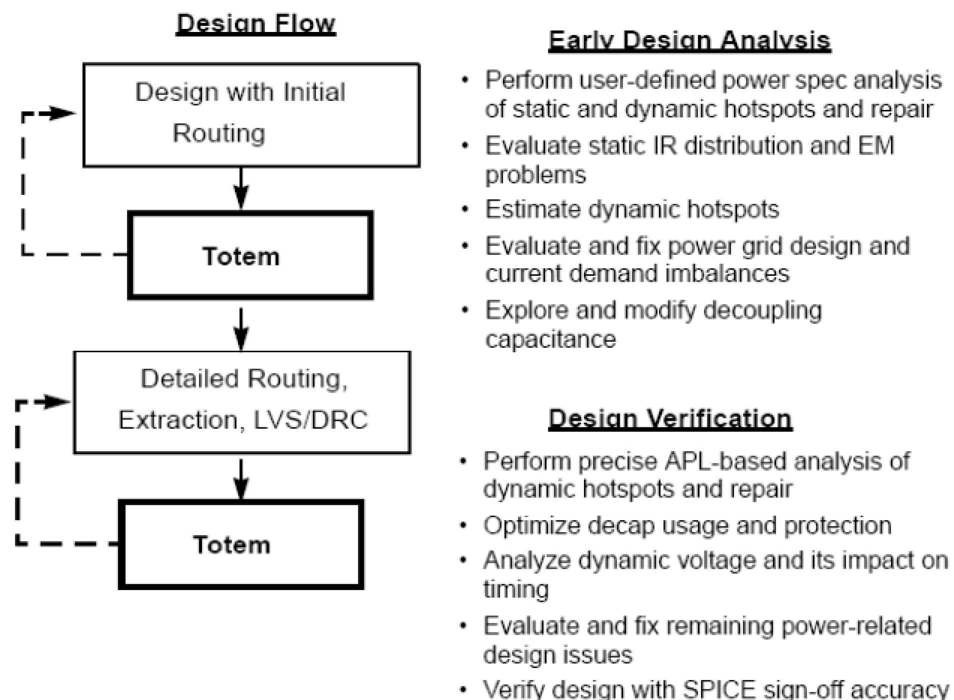


Fig 4.10 Totem flow for Design Verification

Totem's design flow for design verification is shown in Fig. 4.10. One of the underlying technologies is Totem's vectorless dynamic statistical analysis engine, which computes realistic worst-case switching scenarios without requiring functional vectors for standard cells, inside digital P & R blocks. For full custom digital and analog designs, Totem uses the current profiles generated from the functional simulations. During dynamic simulation, it back annotates the current drawn by the transistors to the physical location in layout. It has an internal extraction engine that can extract RC values, as well as inductance, for the power and ground network, so there is no need to rely on external extraction engines for power grid parasitics.

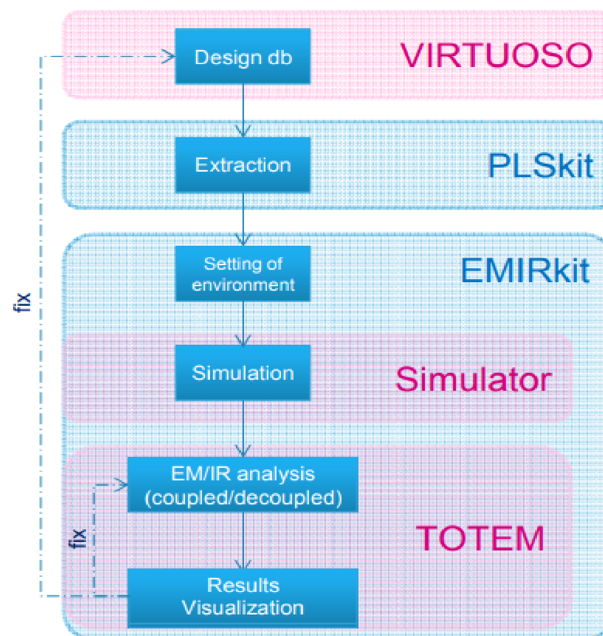


Fig. 4.11 EMIRKit driven Dynamic flow

Totem makes use of ST's EMIRKit and PLSKit to perform EMIR analysis as shown in Fig. 4.11. The Simulator shown in the dynamic flow can be ELDO, Spectre or HSPICE. Schematic and Layout are made in Virtuoso, PLSKit performs post layout simulations on the layout and generates netlist. EMIRKit provides the setup and checks all the DRM rules as per the technology node. The netlist is given to totem to perform EMIR analysis.

Fig 4.12 and 4.13 shows the window for Totem while running it in batchmode. It needs DSPF file, corner file and DSPF file as input for doing the EMIR analysis.

Edit EMIR_Totem parameters

FLOW:

| | |
|---|---|
| Select EMIR mode: | EXPERT |
| Select EMIR flow: | PWRGND |
| Select Apache tool: | TOTEM |
| Early analysis?: | NO |

STEPS:

| | |
|---|---|
| Do all, Electrical modeling only or Totem Analysis only?: | ALL |
| Perform run after initialization?: | YES |
| Analysis in batch Mode instead of GUI?: | NO |

CORNERS CHOICE:

| | |
|---|---|
| "BEOL_STACK" extraction stack choice: | 7m4x0y2z |
| Select corner for powergrid extraction: | typical |
| Select temperature corner: | 125 |

EXTRACTION:

| | |
|---|---|
| Activate high accuracy features?: | YES |
| Split arrays of vias for accuracy purpose?: | YES |
| Length min [um] to split arrays of vias: | 0.001 |
| Extract metal fillers or dummies?: | NO |

ANALYSIS TYPE:

| | |
|---|---|
| Select Electromigration checks: | ALL |
| Need to use a specific mission profile ?: | NO |

INPUTS:

| | |
|---|---|
| Which parasitic extractor has been used?: | StarRCXT |
| Design GDSII File: | |
| Topcell name: | |
| Signal parasitics DSPF file with instances: | |
| Design placement info file: | |

Fig 4.12 Totem Batch mode window (a)

**Edit EMIR_Totem parameters**

| | |
|---|---|
| Design placement info file: | |
| SUPPLIES: | |
| Give same amount in positive and ground: treated as a couple | |
| Positive supply(ies) name: | vdd vdd1 |
| Ground supply(ies) name: | gnd gnd |
| Give same amount of values than supplies by order: | |
| Positive supply(ies) value(s) [V]: | 1.1 1.8 |
| Ground supply(ies) value(s) [V]: | 0 0 |
| SIMULATION: | |
| Select design macro type: | rf |
| Select simulator: | ELDO |
| Number of threads?: | 1 |
| Simulation database reduction ?: | NO |
| Testbench netlist file: | |
| Corners file: | |
| Simulation step [s]: | 1e-12 |
| APL decreasing voltage factor for accuracy: | |
| Number of APL voltages coeffs: | 4 |
| APL voltages offset (0<offset<0.1): | 0.1 |
| ANALYSIS: | |
| Select dynamic pre-simulation mode: | NO |
| How many analysis window(s)?: | 1 |
| Window1 t_start [s]: | 5e-9 |
| Window1 t_stop [s]: | 10e-9 |
| OPTIONAL INCLUDES: | |
| Additional options file for aplmmx file: | |
| Additional options file for gsr file: | |
| Additional options file for totem.cmd file: | |

Reset | Cancel | Ok

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Fig 4.13 Totem Batch mode window (b)

### 4.4.3 EMIR ANALYSIS USING VOLTUSFI

VoltusFi is an EMIR tool by Cadence which is used for EMIR analysis of analog design or custom transistor level digital design. It is integrated into the Virtuoso flow with extraction, simulation and EMIR analysis as shown in Fig 4.14. VoltusFi can generate power grid view for use in the digital implementation flow. It debugs and fixes the error.

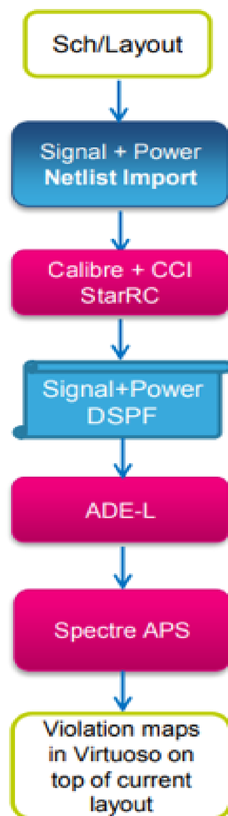


Fig 4.14 VoltusFi flow in Virtuoso

Fig 4.15 shows how PLSKit is integrated in the EMIR flow of VoltusFi. PLSkit generates the netlist and DSPF file which is given as the input to the simulator. Output of simulator is given to the VoltusFi which run the EMIR analysis and generates results.

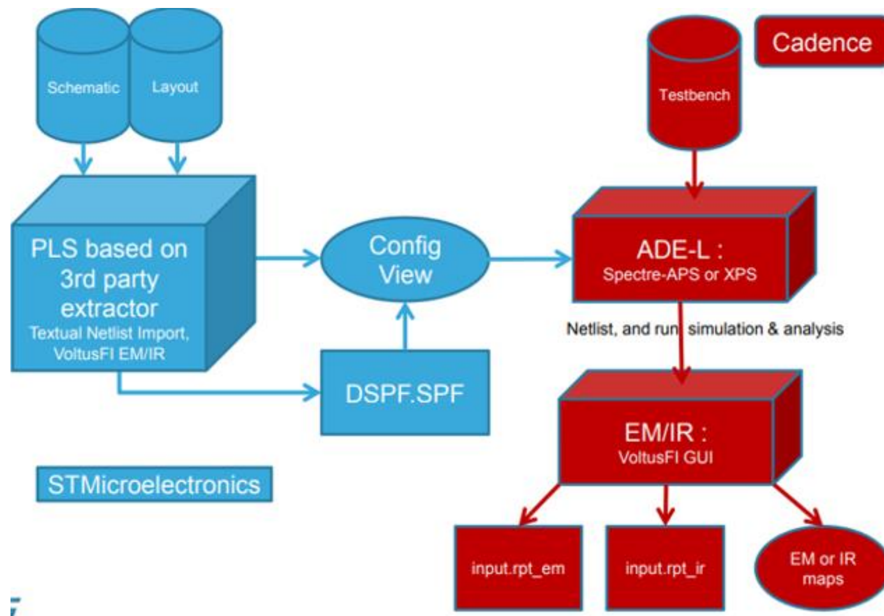


Fig 4.15 PLSKIT-VoltusFi Flow

While running VoltusFi in Batch mode, a popup window appears as shown in Fig 4.16, testbench netlist file is given as the input to the voltusFi to run EMIR analysis. Unix command for batch mode run is EMIR_VOLTUS_FI.

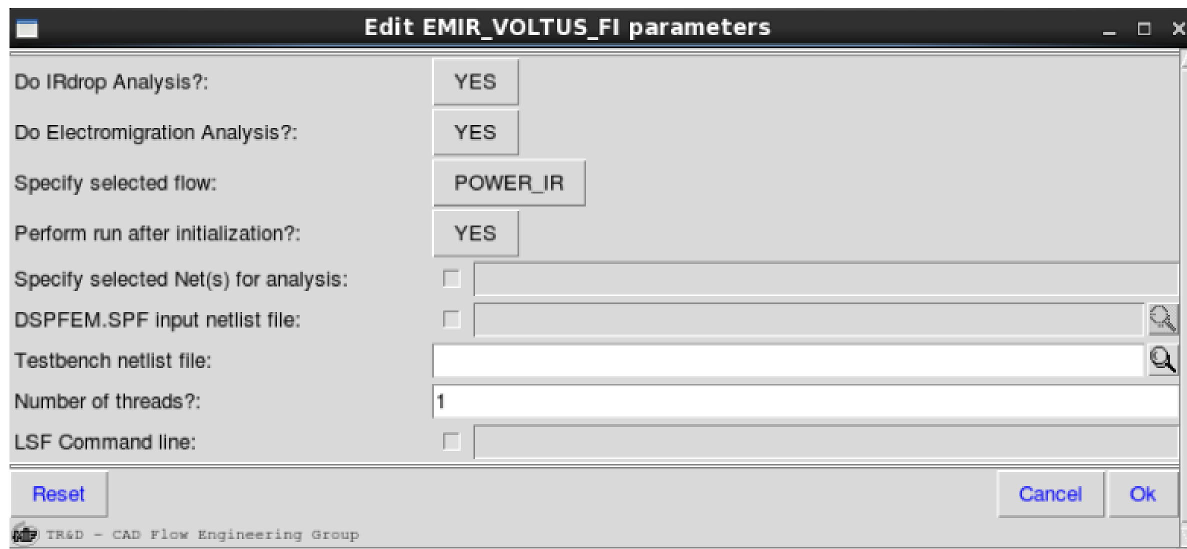


Fig 4.16 VoltusFi Batch mode window

There are various files that are generated by VoltusFi after EMIR analysis. The results for electromigration and IR drop analysis is stored in the output directory as testbench_mod.emirtap.rpt_em and testbench_mod.emirtap.rpt_ir files as shown in Fig 4.17. The file testbench_mod.emirtap.rpt_em has results for electromigration and file testbench_mod.emirtap.rpt_ir has results for IR drop.

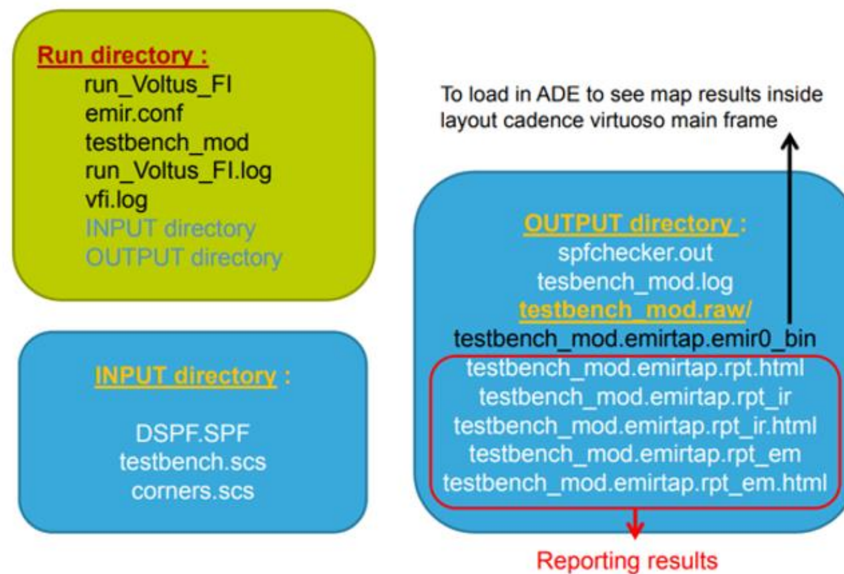


Fig 4.17 Data generated by VoltusFi

The EMIR result file testbench_mod.emirtap.rpt_em has the current values for irms, iavg and imax for Vdd1, Vdd2 and ground. For each resistance value at different metal levels, the file has information about its current, coordinates, width, area, length, and EM length. Some part of the file is shown below.

After reading this file, changes can be made in the design to keep the current within specified limits. Since we have the coordinates of the resistive node, we can know the position and the metal layer where current is exceeding the limit, accordingly we can make changes in our layout.

**vdd1 irms**

**Processing net: vdd1**

| Resistor | I,current (uA) | I,threshold (uA) | I/Imax | Layer | X (um) | Y (um) | Width (um) | Area (um*um) | Length (um) | EM Length (um) |
|---|---|---|---|---|---|---|---|---|---|---|
| r2_199 | 0.00035548 | 0 | 0.000 | ndifsi_final | 315.94500 | -0.00500 | 0.12 | 0.12 um | 0.055 | 0 |
| r2_200 | 34.1041 | 0 | 0.000 | ndifsi_final | 316.00000 | -0.00500 | 0.12 | 0.12 um | 0.068 | 0 |
| r2_201 | 34.104 | 0 | 0.000 | lilsali_final | 316.00000 | -0.00500 | 0.06 | 0.0036 um*um | 0 | |
| r2_203 | 0 | 1173.32 | 0.000 | m1_final | 0.03500 | 0.00000 | 0.07 | 0.07 um | 0.035 | 10.035 |
| r2_204 | 34.0618 | 1173.32 | 0.029 | m1_final | 0.03500 | 0.00000 | 0.07 | 0.07 um | 9.965 | 10.035 |
| r2_205 | 8.84283 | 0 | 0.000 | hbvia_bot | 293.98000 | -1.32000 | 0.36 | 0.1296 um*um | 0 | 3.2 |
| r2_206 | 0 | 0 | 0.000 | hbpad_bot_final | 293.98000 | 0.00000 | 4.4 | 4.4 um | 0.72 | 0 |
| r2_207 | 8.84283 | 0 | 0.000 | hbpad_bot_final | 293.98000 | 0.00000 | 4.4 | 4.4 um | 0.7 | 0 |

**vdd1 imax**
**Processing net: vdd1**

| Resistor | I,current (uA) | I,threshold (uA) | I/Imax | Layer | X (um) | Y (um) | Width (um) | Area (um*um) | Length (um) | Time (ns) | EM Length (um) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| r2_199 | 0.000808574 | 0 | 0.000 | ndifsi_final | 315.94500 | -0.00500 | 0.12 | 0.12 um | 0.055 | 81.000ns | 0 |
| r2_200 | 48.932 | 0 | 0.000 | ndifsi_final | 316.00000 | -0.00500 | 0.12 | 0.12 um | 0.068 | 82.000ns | 0 |
| r2_201 | -48.932 | 0 | 0.000 | lilsali_final | 316.00000 | -0.00500 | 0.06 | 0.0036 um*um | 0 | 3.000ns | 3.035 |
| r2_203 | 0 | 11900 | 0.000 | m1_final | 0.03500 | 0.00000 | 0.07 | 0.07 um | 0.035 | 0.000ns | 10.035 |
| r2_204 | 48.932 | 11900 | 0.004 | m1_final | 0.03500 | 0.00000 | 0.07 | 0.07 um | 9.965 | 95.000ns | 10.035 |
| r2_205 | 12.6892 | 0 | 0.000 | hbvia_bot | 293.98000 | -1.32000 | 0.36 | 0.1296 um*um | 0 | 95.000ns | 3.2 |
| r2_206 | 0 | 0 | 0.000 | hbpad_bot_final | 293.98000 | 0.00000 | 4.4 | 4.4 um | 0.72 | 0.000ns | 0 |
| r2_207 | -12.6892 | 0 | 0.000 | hbpad_bot_final | 293.28000 | 0.00000 | 4.4 | 4.4 um | 0.7 | 95.000ns | 0 |

These result files generated by the EMIR Tools will be used as a golden file while uploading test on QA Machine. This is explained in the next chapter.

# CHAPTER 5
# EMIR VERIFICATION ON QA MACHINE

QA Machine is a ST tool used for automatic testing of analog flows. This chapter describes the overview of QA Machine. It shows the need of QA Machine for automation of verification flow. It also gives insight to how a test is uploaded on QA Machine and explains the report generated by it.

## 5.1 OVERVIEW AND STRATEGY

In order to increase automation, tools need to be developed which can perform the testing of flow for updated versions of the software used in the flow. QA checks list is often launched manually. It requires heavy effort in a very short period of time before release. All test suites should be replayed whenever an issue is raised during QA and some of them are skipped to save time. QA machine (ST) is an automatic testing regression machine for reliable and robust testing of analog kits.

QA Machine Overview is shown in Fig. 5.1. It shows the steps involved in uploading a test on QA Machine. First the test is prepared, after successful validation it is uploaded on the server. QA Machine runs the test and generates report. The report is sent to the designer, if the status of the test is fail or mismatch, necessary changes are made in the test to make its status as pass.

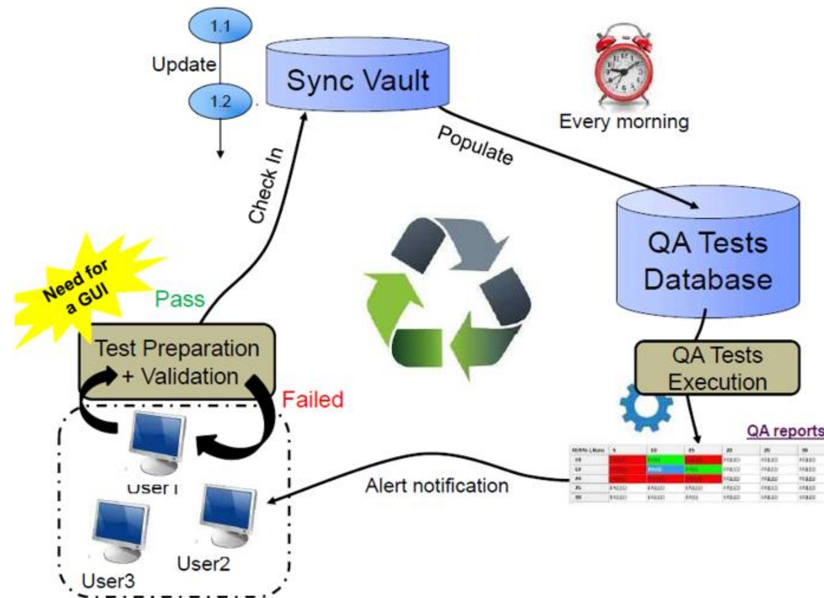


Fig. 5.1 QA Machine Overview

### 5.1.1 PURPOSE OF QA MACHINE

QA Machine's purpose is to help kit developer prepare a new consistent and self-contained test with step by step approach. It requires mandatory dry run to validate the test before submission on repository. It has data integrity, valid batch command, reliable filters, etc. It is developed in python 3.5 on top of python anaconda package. Its main features are agility at work, agile dashboards (Codex), python inheritance as much as possible (modular approach), easy code sharing and maintenance and kraken python framework is used.

### 5.1.2 MAIN FEATURES OF QA MACHINE

QA GUI is available to create consistent and clean constructed tests. Local execution of test under execution with pass/failed report generation. Test is submitted to the server only when test is OK. Automatic execution of QA tests of interest every morning. Automatic notification of failed tests to the owner of the test. Agile development of QA Machine in Kraken framework. Easy code sharing with GIT/Codex.

## 5.2 TEST STRUCTURE

A test in QA Machine needs various files to run the test. Fig.5.2 shows the structure of the test and various files which are required for uploading a test on QA Machine. Inputs include files such as netlist, GDS, DSPF, corners etc. which is the extracted information from the layout of the testcase. The run file contains the shell script for running the desired test. Golden files are the results generated by the EMIR Tool, which are given to QA Machine for comparison to its output file after the dry run is performed**.** Output files are generated by QA Machine after the successful run of the test. Filters are used in order to avoid comparison of some part of the golden file with the output file.

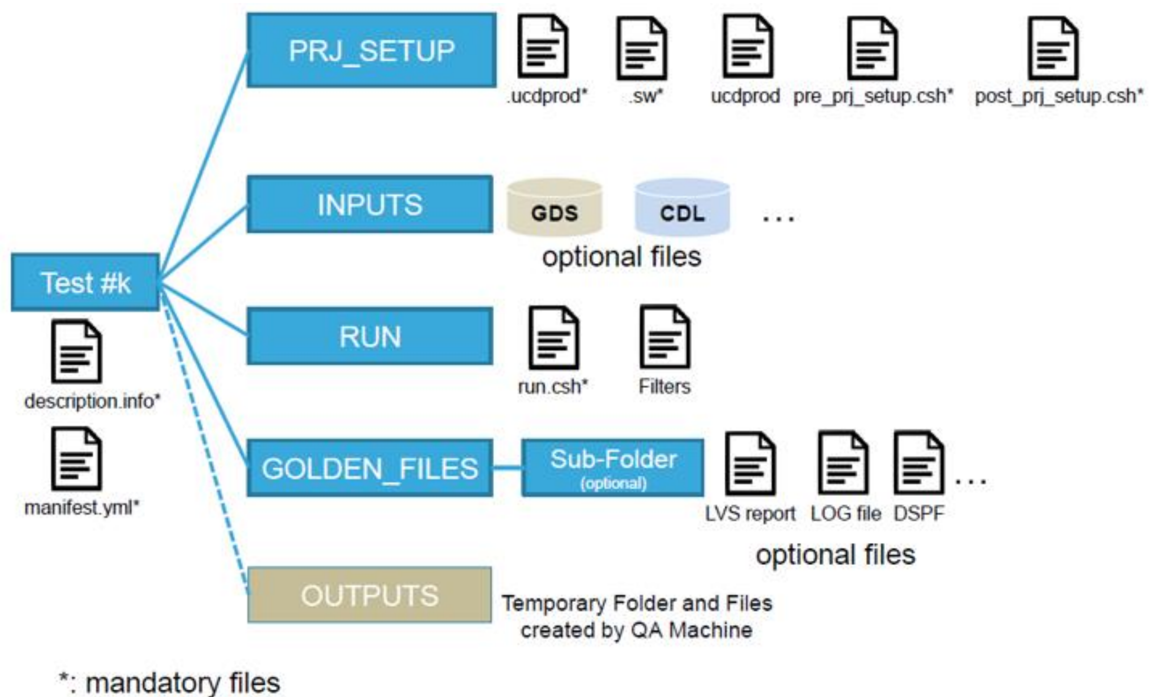


Fig. 5.2 Test Structure

### 5.3 TEST REPORT

Test reports are generated by QA Machine every morning. It run the flow with the latest available version of the tools used in the flow and generates results. It compares the result generated with the golden files which are the result generated by the EMIR tool while running the flow on virtuoso. It will then give the status of the test depending on the comparison.

QA Machine will give PASS status if the output files generated by QA Machine are same as the golden files. It will generate MISMATCH status if there is any difference in the output files and golden files. It will generate MISSING status if the files specified in the golden files are not generated in the output while running the flow. It will generate FAIL status if the test run is unsuccessful because of some error in the Run file or some missing input file.

# Test Report :

## Date: Monday 17 June 2019

### *EMIR*

| Name | Status | Link |
|---|---|---|
| EMIR_VoltusFi-2 | [ Pass ] | View Details |
| EMIR_XARA_B9A | [ Pass ] | View Details |
| EMIR_Totem_B9A_ML | [ Mismatch ] | View Details |
| EMIR_Totem | [ Mismatch ] | View Details |
| EMIR_XARA_B9A_ML | [ Pass ] | View Details |
| EMIR_VoltusFi | [ Pass ] | View Details |
| EMIR_VoltusFi_B9A_ML | [ Pass ] | View Details |

Fig. 5.3 Test Report

Test Report is shown in Fig. 5.3 for all the testcase uploaded on QA Machine. All these testcases are uploaded for EMIR Kit. The status of two of the testcases is mismatch because the version of the process design kit used while uploading the test is different from the version used by QA Machine for running the test. The nomenclature for metal level is different in these different versions of PDK. In one it is represented as metal1, metal2 and in the other as m1, m2.

# CONCLUSION

Electromigration and IR drop is an important reliability concern for IC designers. EMIR analysis was performed for two technologies, BiCMOS Technology and 3D Integrated Technology. Three EMIR analysis tools from different EDA vendors were used for verification, CustomSim-RA from Synopsys, VoltusFi from Cadence and Totem from Ansys. All the reports generated from these tools for each technology were uploaded on QA Machine for automation of EMIR flow verification. QA Machine run the flow with the updated version of tools used and generates results. Reports are generated by QA Machine to give the status of uploaded tests. This helps in the automatic testing of the EMIR flow for the given technologies.

Different technologies has different current limits and number of metal levels. Thus, Future scope includes EMIR analysis for other technologies. Other testcases with different layout structure can be used for EMIR analysis. Work can also be done on correcting the EM violations in the design.

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