DESIGN AND IMPLEMENTATION OF CMOS LNA FOR BLUETOOTH AND BLE APPLICATIONS

A Dissertation

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Candidate's Declaration

I, Diksha Singh, 2K17MOC/04, student of M.Tech(Microwave and Optical Communication Engineering), hereby declare that the project Dissertation entitled " Design and Implementation of CMOS LNA for Bluetooth and BLE applications", which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirements for the award of the degree of Master of Technology in Microwave and Optical Communication Engineering is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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Certificate

I hereby certify that the Project Dissertation entitled "Design and Implementation of CMOS LNA for Bluetooth and BLE Applications" which is submitted by Diksha Singh (2K17/MOC/04), Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirements for the award of the degree of Master of Technology(Microwave and Optical Communication Engineering), is a bonafide record of the project work carried out by her under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Abstract

Low Noise Amplifier (LNA) is an important component of transceivers and is also widely used in wireless applications. LNA is the first active element in the receiving chain. Its NF and gain play a significant role in the overall performance of the receiver.With the increasing need for the Internet of things (IoT), Bluetooth low energy (BLE) technology has become a popular solution for wireless devices. When compared to classic bluetooth, BLE has an advantage of low power consumption. Hence it will be apt for IoT based applications. BLE may replace Bluetooth as it is ought to have a low power consumption which gives BLE an upper edge over Bluetooth. We will study the different topologies used to implement LNA for BLE applications and analyze their performance parameters. Our aim is to design an LNA which is able to provides better performance in terms of all parameters and is apt to be used in Bluetooth and BLE applications. We perform all the simulations in Advanced Design System(ADS).

List of Published Papers

1. **Malti Bansal, Diksha Singh, " Low Noise Amplifier for Neural Applications ", International Journal of Computer & Mathematical Sciences IJCMS ISSN 2347 – 8527 Volume 6, pp -74-81, Issue 11, November 2017**
2. **Malti Bansal, Diksha Singh, "Low Noise Amplifier In Bluetooth And Bluetooth Low Energy (Ble) Applications", In Proceedings Of National Conference On Emerging Trends in Electronics and Communication-2019,pp.110-113**
3. **Malti Bansal, Diksha Singh, "Design and Implementation of Low Noise Amplifier in Neural Signal Analysis", in proceedings of International Conference on Information, Communication and Computing Technology ICCICT 2019,pp. 1-11**
4. **Malti Bansal, Diksha Singh, "Cascode Common Source LNA With Inductive Degeneration Topology Utilizing Different Output Matching Circuits In 45nm CMOS Technology ", in proceedings of International Conference in Communications and Electronics Systems(ICCES 2019), pp. 594-598**
5. **Malti Bansal, Diksha Singh, "Different Input Impedance Matching Circuits For Cascode Common Source LNA With Inductive Degeneration Topology In 45nm CMOS Technology", in proceedings of International Conference in Communications and Electronics Systems(ICCES 2019), 589-593**

List of Contents

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

IoT	Internet of Things
BLE	Bluetooth Low Energy
VLSI	Very Large Scale Integration
CMOS	Complimentary Metal Oxide Semiconductor
RF	Radio Frequency
LNA	Low Noise Amplifier
IIP3	Input Third Order Intercept
IEEE	Institute of Electrical and Electronics Engineers
GFSK	Gaussian Frequency Shift Keying
ECG	Electrocardiogram
NILM	Non-Intrusive Load Monitoring
SNR	Signal to Noise Ratio
NF	Noise Figure
CAD	Computer Aided Design
ADS	Advanced Design Systems
PSD	Power Spectral Density
CS	Common-Source
CG	Common-Gate
IMD	Inter-modulation Distortion
SoC	System on Chip

CHAPTER-1

INTRODUCTION

Wireless communication has become an important necessity of today's world. Demand of technologies that are compatible with changing trends in technology is increasing and end-users desire that their devices should be versatile enough and support new technologies i.e. WiMax, 3G, 4G and so on. Household devices may not be connected to wireless devices at this time but in coming future this will also become possible as Internet of Things (IoT) is the hottest topic of research today. This increases the necessity of designing RF circuits that can be implemented for wireless communications meeting the present standards. This increases the cost of the devices as well as maximises the circuit complexity i.e. integrating a large no of elements on a single chip. All these challenges when considered in designing a circuit can contribute to bright future of RF circuits.

With advancements in technologies, devices which provide better efficiency at a lower cost have been in demand nowadays. Internet of Things (IoT) has also created a tremendous scope for research in many fields which includes wireless networks, sensors, low power operating devices, energy-efficient devices. The next generation devices which intend to turn IoT into a reality require operating on ultra low –power and working for several years. Integration of the elements on-chip is also a critical challenge that needs to be overcome by researchers.

If we restrict to wireless communication, the operating frequency gets fixed to 2.4 GHz because it is the only available frequency which does not require a license. Bluetooth technology also works on the same frequency. When compared to classic Bluetooth, BLE has an advantage of low power consumption. As a consequence of extensive research in the area of Internet of Things (IoT), Bluetooth low energy (BLE) technology seems to provide an apt solution for wireless devices. Hence it will be appropriate for IoT based applications in the coming future.

Designing of RF circuits requires a good understanding of many disciplines that include understanding of RF and microwave theory, VLSI and other basic concepts of RF circuits. RF circuits have created a tremendous scope of research and this comes due to advancements in semiconductor technologies which makes system level integration more flexible. These have also gained popularity due to its low cost which makes it

most attractive technology to work on. CMOS technology advancements have proved to be beneficial for both analog and digital circuits. However redesign of digital circuits for a newer technology is an uncomplicated process it is not so in case of redesigning analog circuit for a newer technology. It is a challenge to redesign analog circuits for newer technologies. [1] With brisk increase in communication technology, additional burden of larger integration also follows up. Better performance delivering Integrated Circuits are in demand with spectacular improvements in technology. CMOS scaling technologies are also improving day by day which is able to provide better performance at a lower cost and lower chip area. These developments in CMOS process technologies have made realizing a System on Chip feasible, for use in almost all domains of life. [2]

Ability to communicate by the means of wireless medium is the most important feature required in the systems nowadays. For this we require a receiver which should be capable of providing an optimum performance when implemented in real-time systems. Transceiver is one of the basic components of RF circuits required in wireless communications. The transceiver is responsible for transmitting as well as receiving information at the same point of time i.e. it performs the work of a transmitter as well as a receiver. Designing a receiver for different applications that should support different range of frequencies is a tedious task. At the receiver end generally the first important functional block is a Low Noise Amplifier (LNA) that is specifically designed to provide a better noise performance than the other amplifiers.

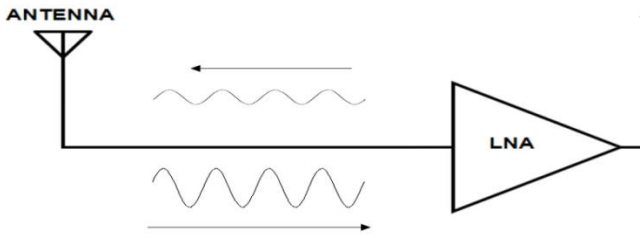

Fig.1.1 Parts of a receiver system

Designing an LNA which is best in terms of performance parameters increases the efficiency of the receivers system. However with expeditious growth in wireless communication industry, manufacturers aim to design a circuit which is able to deliver best results among the already available hardware at present. In case of LNA performance, target is to achieve a low noise figure, high gain, low loss, high Input Third Order

Intercept (IIP3).[3]

We try to analyze the pervious works in the field of LNA design and try to design a new LNA with features that would be compatible with the devices designed keeping new advancements in concern.

LNA'S are being widely used in designing receivers for Bluetooth as well as BLE. However the basic difference lies in the fact that the power consumption is drastically low in BLE applications.BLE has an advantage of low power consumption which makes it suitable for device to device communication. BLE devices can last for years once placed in machine and makes it suitable for IoT devices. Higher speed may not be obtained but longer battery life is a surely obtained. BLE is discussed in detail un the next section.

1.1 BLUETOOTH AND BLE

Many wireless technologies are available for use in healthcare applications which include ANT, ZigBee, and Bluetooth. Out of these available technologies Bluetooth is considered to be the most versatile technology as far as compatibility is concerned. However in the era of IoT low power consuming devices are in demand which limits its applications nowadays.

Bluetooth is also a form of wireless communication which is more prevalent and everybody is more familiar with this form of wireless communication. For Bluetooth communication also we need a transmitter and receiver and the receiver end utilises an LNA as the first block of the system. LNA for this particular application will have different characteristics than the LNA for other forms of communication as LNA parameters depend on the application for which they are being designed. More specifically a LNA for Bluetooth applications should provide a higher gain and consume less power than others. To cope up with the requirements on new generation wireless technologies, Bluetooth was modified and a newer version of Bluetooth is more prevalent in devices now. Bluetooth v4.0 is specially designed to consume less power than the pre-existing Bluetooth version. This version named as Bluetooth Low Energy (BLE) was announced in 2010 and since then it is chosen over other wireless technologies as it overcomes the disadvantages of other wireless technologies. Bluetooth Low Energy (BLE) focuses on reducing the power consumption of the circuit and is apt for IoT applications. BLE devices can work for longer hours as they consume less power.

Bluetooth Low Energy is also known as Bluetooth Smart and was in the specification IEEE 802.15.1. It is apt for applications requiring low power consumption, ability to connect more no of users on a single network, reduced cost and simple implementation. BLE modules are available that can be used in many applications and the users do not have to design the system for BLE implementation by themselves. Being a promising candidate in all aspects, BLE has become a part of many systems that are being utilised in smart phones, wireless sensor networks , medical applications, industrial equipments.[4]

Bluetooth is widely used for short range communications. Bluetooth is known to work at a frequency of 2.4 GHz and provides us with data connectivity upto a range of 50m. Maximum data rate that is achieved in bluetooth is upto 440 Kbps. Bluetooth connections setup should adhere to specifications which are already listed Bluetooth specifications . These specification provide with the allowable range of carrier frequency, modulation, transmitted power etc. Bluetooth standard states that the modulation scheme used should be GFSK with index prescribed in the specifications.[5][6]

Though BLE devices have a lower power requirement they are not capable of transmitting data at very high rates. However BLE devices are not required to have large data transfer rates so lower data rates do not effect its performance . For example, if we wish to control air-conditioner or other home appliances, we do not desire higher data rates. We only need to signal it to switch it on/off or control the settings of the appliance which does not involve large data It simply needs to send the data conveying the required message to turn on/off or vay the temperature to the device and vice-versa to the transmitter.. On the contrary , if the consumer uses a smartphone to run a live video pr television through a wireless connection, it will not be a small amount of data conveying a single task ; instead, it will be a large data that must be smoothly transmitted between the device and the transmitter and that must be smoothly achieved. Otherwise, the user will never replace the wired connection with wireless.

Depending on the application requirement Bluetooth emerged to have different modes of operations. If devices need to operate for longer time we cannot achieve higher data rates and if higher data rates are desired power consumption will increase. A trade-off always exists in higher data rates and power consumption of the circuit.

When we intend to use BLE in our systems we must follow the specifications stated by IEEE for BLE. Operating frequency of BLE is fixed at 2.4 GHz which is standard for most of the wireless technologies as well. For transmission of data BLE uses GFSK (Gaussian Frequency Shift Keying) technique of modulation. It consists of a total 40 channels which were 79 in Classic Bluetooth, resulting in a reduced interference from adjacent channels. The channels are 2 MHz wide and out of the available 40 channels 3 are dedicated to send and receive short messages broadcast. Other remaining channels are dedicated to transfer data packets. [7]

LNA in BLE puts a constraint on power consumption of the circuit and it is a difficult task to adhere to power consumption specifications as well as fulfil other system specifications.[8]

1.2 APPLICATIONS

Bluetooth as well as BLE because of its specifications has opened a plethora of applications in almost every domain. It includes healthcare, smart homes, smart driving, security systems etc. Systems operating on this technology are being reported everyday which aim to provide better efficiency than the previously reported ones.

1.2.1 BIOMEDICAL APPLICATION

With improvements in technologies and everything moving towards automation physical activities of humans have reduced which makes it necessary to keep a record of one's health regularly and people have begun to pay attention to their health . Most important measure of one's health can be predicted by measuring blood pressure and it proves to be an important step in self-health management. Smart-phones are also being used in healthcare and this has further increased the versatility of smart-phones in human life. [9] Keeping a record of a patient blood pressure values assists the doctors also to provide proper treatment to the patient.[10] Further with improvement in wireless technology, application of wireless communication in monitoring health has become an important topic of research and many systems based on wireless monitoring of signals have been proposed.

BLE based electrocardiogram (ECG) monitoring system was also reported in [11]. BLE based blood pressure monitoring systems was also reported after the announcement of BLE.[12] This device was designed to detect the blood pressure signals and convert

them into equivalent BP readings using standard algorithms and then transmit the readings to smart phone using BLE.

With BLE announcements a tremendous increase has been observed in devices utilising this wireless technology specifically in wearable fitness devices. BLE is apt for these devices as its low energy allows it to be compact in size and it can be implemented using a coin size battery only. Moreover BLE works on a simple protocol that can be easily implemented and is suitable for adoption in smart phones. [13]

Conventionally wired electrodes are used to acquire signals and then monitor them which restrict their mobility. Using wireless technology in monitoring these signals has a lot of advantages over conventional methods. Wireless sensors can be implanted very easily as compared to wired ones and these do not create discomfort to the patient and signal can be monitored in any environment. Doctors can easily access these and provide medical assistance to those in need.

1.2.2 LOAD MONITORING SYSTEMS

Energy consumption of households have shoot up because of increase in no of electrical appliances in houses. These results in overload and it can be reduced by judicious use of appliances. This can be monitored using smart sensors which can assist in achieving an increase in energy efficiency. If there is no person in room smart sensors will detect the situation and appliances will be turned off. [14] Information about a user's energy consumption may assist the user in improving energy consumption habits of the family. To improve energy usage by the appliance Non-Intrusive Load Monitoring (NILM) algorithm can be applied which segregates the energy consumed by different appliances. [15][16]

1.2.3 SMART SECURITY SYSTEM

BLE is also used in implementing smart security system A smart security system was reported which allowed the user to control the appliances un home via a webpage even if the user is not physically present at home.[17]

1.2.4 OTHER APPLICATIONS

BLE was also implemented in smart farming i.e. data related to soil was transmitted to the cloud and required operations were performed on the data and again it was

transmitted to the microcontroller. In this process BLE was used to transfer data to the microcontroller. [18]

Other researcher reported using BLE in VANET applications, which was used for smart driving and this was achieved by using a smart phone equipped with BLE radio. This smart phone was used to transmit information between vehicles. [19]

1.3 **LOW NOISE AMPLIFIER**

In wireless communication message signal is transmitted via free space i.e. the transmitter directs the desired signal in free space and the signal then passes through free space and is received by the intended receiver antenna. When this signal is received at the antenna a lot of noise gets added to the signal which reduces the Signal-to-Noise ratio of the signal. This signal received at the antenna needs to be processed further which includes filtering out the undesired frequencies, amplifying the signal, conversion from analog to digital domain if required. As the signal passes through these blocks additional noise gets added to them which further degrades the SNR of the desired signal. Hence we need devices which do not degrade the SNR of the signal and reduce the effect of noise on the signal. Low Noise Amplifier (LNA) serves this purpose perfectly i.e. it amplifies the signal up-to a sufficient level and the noise added by the components of the amplifier is very low.

$$OUTPUT\ SNR = \frac{INPUT\ SIGNAL\ * GAIN}{(INPUT\ NOISE * GAIN) + \ SYSTEM\ NOISE}$$

LNA is designed such that the system noise added by it is very less which provides a better value of SNR than provided by other amplifiers. There are many sources of noise in a device which will be discussed later. LNA is designed to provide better noise performance and is generally placed at the first stage of the receiver system. After LNA other blocks are also present in the receiver system which is connected in cascade for further signal processing. Placing LNA at the first stage improves the noise performance of the complete receiver system because the noise performance of a system with many blocks connected in cascade is given by the formula:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_{n-1}} \quad (1)$$

From the above formula it can be seen that the Noise Figure (NF) of the first stage dominates the NF of the completer receiver system. Therefore placing LNA the initial stages of the receiver reduces the overall cascaded effect of noise on the receiver system and the NF of the LNA determines the performance of the transceiver.

Wireless communication is generally limited to short distances as compared to other forms of communication. Designing a LNA for short distance communication (up-to 10m) is a smooth process in comparison to design a LNA for long distance communication (more than 10 m). LNA for long distance communication where the distance between the transmitter and receiver is more than the specified range requires high sensitivity which in turn leads to increase in complex design process. LNA for short distance communication where the distance between the transmitter and receiver module is less than 10 m drives the next block into compression because of the signal at the input being strong in amplitude. This signal needs leads to a output signal which is distorted. In this scenario we need a LNA that can overcome this problem by suppressing the input signal to prevent this condition.[20]

LNA with all parameters perfectly within the limit cannot be designed as trade-off always exists between the different parameters of a circuit. Based on our application area we need to focus on the parameter to be optimised and accordingly the LNA design procedure is carried out further.

Most of the LNA's are generally single band LNA i.e. they are designed to operate at a single frequency. However multiple band LNA's are also being introduced i.e. they are capable of operation at more than one frequency. Operating a single LNA over multiple frequencies increases the complexity of the circuit but it also makes it versatile for multi-standard applications. However LNA's are reported that operate at two frequencies i.e. they are dual band LNA's. Multiple band LNA's are less common as achieving optimum performance at multiple frequencies increase the overhead of increase in cost of the LNA. Moreover it also results in increase in power requirements of the circuit as well as increase in the chip area occupied by the circuit.[21]

If we wish to design a broadband LNA we generally use a single transistor which is being used in common-source configuration. [22] Darlington amplifier is used in case of

broadband applications i.e. optimum performance over a larger bandwidth.[23]
Application of LNA also decides the components that can be utilised in the circuit design. If we require a system on chip we should avoid components which occupy larger chip area. If we wish to have a higher gain again we can contain connect multiple stages in cascade with each other, they will provide an optimised gain with reduced performance in terms of other parameters. If we wish to optimise chip area occupied by the amplifier we should use a single stage amplifier because increasing the number of stages increases the chip area that is being occupied. We should also avoid using bulk elements i.e. the elements which occupy larger chip area. If we wish to have lower power consumption we should avoid using multiple stages in our amplifier. The parameter that is to be optimised plays important role in design specification and the amplifier is to be designed accordingly.

1.4 LNA APPLICATIONS

LNA finds applications in many domains which include biomedical domain, neural applications, wireless communications etc.

1.4.1 NEURAL APPLICATION

Brain activities are also studied by analyzing the neural signals produced in our brain. These neural signals produced are very weak signals and noise gets added as they are passed through various components which are used in their analysis. Noise degrades the signal to noise ratio of these neural signals and as a consequence of addition of noise, it becomes difficult to study brain activity pertaining to these signals. To analyze these signals in an appropriate manner, they need to be amplified up to a certain threshold level without much noise being added to them. Low Noise Amplifiers are best suited to analyze these weak signals and achieve this function. LNA amplifies the signal received at the input; and very less noise is added due to its components to the received signal. Hence, the SNR of the signal is maintained at an appropriate level which is suitable for analysis of neural signals. LNA can be utilized for neural signal analysis with different design techniques to improve the performance of LNA.

Detailed examination of neural signals produced in our brain helps us to understand the brain activities. Detailed analysis also provides a better understanding of disorders related to brain i.e. Parkinson’s disease, Alzheimer’s disease and various

others.[24][25]. Electrodes are used for interfacing these with the tissues present in the brain[26] .Multiple sites can also be observed at the same point of tine i.e. activities in different parts of brain can be studied by using multichannel neural amplifiers. Multichannel LNA are capable of observing multiple neuron activities at the same instance but the area occupied by these amplifiers is increased because multiple amplifiers are to be fabricated on a single chip. However, many multi-channel amplifiers reported so far were also found to use a very small chip area.

Neural signals lie in the range of few millivolts and are therefore considered as very weak signals and they may get degraded if more noise gets added to them. LNA is suitable for analysis of these signals because the noise added by this type of amplifier is very less and does not degrade the SNR of the signal. Power consumption is a very crucial factor in case of neural amplifiers as high power may result in increase of temperature and this may damage the brain tissues. An important requirement for the use of LNA for neural applications is that they should be designed in such a way that power consumed by them for operation is very low.

Neurons may generate a rhythmic pattern of action potentials or spikes and if they generate action potentials in sync, this gives rise to local field potentials. Neural signal can also be considered as superimposition of action potentials or spikes on low frequency local field potentials. Frequency range for these signals is different .Action potentials lie in higher frequency range (300-6000 Hz) in comparison to local field potentials (1-200 Hz)[27]. LNA's are specially designed to study these signals separately in their respective frequency band. Some configurations focus on action potential analysis and some on local field potential analysis; because of the different frequency range .However some amplifiers used filters which filtered out the desired frequencies to handle Action potentials as well as local field potential simultaneously. In any circumstances ,the gain of the LNA should be high because the signals associated are always weak signals.

Design phase of LNA should be properly executed because before fabrication LNA needs to be designed for certain specifications which are solely dependent on the application it is being designed for. Conventionally LNA design are carried out by trial and error process or using simulation tools which increase the chances of error in design as it requires human intervention. CAD(Computer Aided Design) tools have made the work easier and error free nowadays and are being utilised in LNA design. [28]

1.5 LNA DESIGN PROCESS

LNA is used in a wide range of applications including biomedical domain as well. Designing an LNA is specifically dependent on the application for which it is being designed. Application domain of the device determines the factors that should be considered while designing a circuit and the parameters that are to be enhanced. The parameters to be enhanced play a high-priority role in the design process of LNA. However the basic steps remain the same inattentive of the application it is being designed for. Basic steps involved in design of LNA can be divided into five parts:

- Transistor Selection
- Biasing network
- Matching networks
- Topology
- Stability

Designing a circuit meeting the required standards involves proper investigation of these design steps and then proceeding with the design of the circuit and analysis of the results obtained.

1.5.1 TRANSISTOR SELECTION

Initial step in LNA design is choosing a proper transistor that would be apt for operation at high frequency. Transistor should be chosen such that it is able to work properly at microwave and higher frequencies and keeping in mind the trade-offs regarding the device operation. Choice of transistor may not affect the performance of the circuit in simulating environment to great extent but it affects the real-time performance of the circuit by a significant amount. Hence we need to be cautious while making the choice of transistor to be used in our circuit. A wide variety of transistor choices are available nowadays. Pseudomorphic High Electron Mobility Transistor (PHEMT) was being used while designing a wideband LNA that is capable of providing a high gain over a wide range of frequencies. These transistor types are also suitable for designing microwave monolithic circuits and also for circuits intended for operation at higher frequencies. Amplification property of the MOS transistor is determined by the value of transconductance denoted by g_m. Appropriate value of g_m should be availed and it depends on many parameters. Bias current plays an important role in determining

the value of transconductance and the width and length of the transistor also determine the value of the transconductance. The size of the transistor is also crucial in LNA's design process. Transit frequency of the transistor being used is a major parameter that affects the values of other parameters of the circuit as well. The transit frequency f_T helps to identify the value of inductance required to achieve input matching.

1.5.2 BIASING NETWORK

Once your circuit design is complete you also need to provide proper biasing to your circuit to give it a stable bias point of operation. Biasing can be provided using many different techniques which have their own benefits as well as negative aspects. Choice needs to be made between biasing network to be chosen for a particular circuit. However the technique should be chosen so as to be suitable for the application of LNA. Few techniques that are being used for providing biasing include voltage divider biasing, transistor biasing, current mirror biasing etc. Out of the entire techniques available current mirror biasing is the most widely used biasing in circuits. Voltage divider resistive biasing was used in some LNA circuits which were intended to be used as wide-band LNA i.e. for a wider range of frequencies. Using current mirror biasing has an advantage of providing a reduced chip area when the device is fabricated for practical applications.

1.5.3 MATCHING NETWORKS

LNA is implemented as a part of a larger receiver system that consists of other blocks as well. These blocks are connected in cascade which together forms the receiver system. When devices are connected in cascade maximum power transfer does not take place from one stage to another due to loading effect. Loading effect tends to decrease gain of the device because of impedance mismatch at the input or output stage. Accordingly we need to employ matching circuits at the input and output terminals of the circuit to achieve maximum power transfer to the subsequent stages and minimise the loading effect to a large extent.

In the receiver block, LNA is generally placed after the antenna which denotes an impedance of 50Ω. For maximum power transfer between two stages the output impedance of the first stage should be matched with the input impedance of the second stage. If impedance mismatch occurs between the two stages maximum power transfer

will not take place and reflections are ought to occur. Hence LNA's input impedance needs to be matched with antenna's impedance to achieve complete power transfer. This can be achieved by using an input matching network that performs this task of matching the input impedance and it is very crucial for LNA's performance. Matching networks also have different topology and numerous components are available that can provide matching between two stages. However choosing a proper matching network that enhances the performance of the circuit is a tedious task to be done properly. A change in matching network affects the circuit performance and hence a comparison can be done to find which matching network is best for our circuit design.

Similar to the input stage, output matching also needs to be accomplished in order to transfer maximum power to the next stage after the LNA in the receiver block. Different output matching circuits also affect circuit performance

1.5.4 TOPOLOGY

LNA's utilise configurations that are being used traditionally to design amplifiers. Other than configuration additional steps are to be taken to achieve the desired performance. It can be obtained by introducing a change in the biasing network or it can be through a change in matching networks being used. Most common LNA topologies are common-gate, common-source, cascode etc. Each of the above topology has its own advantages and disadvantages. In-spite of their own merits and demerits the cascode configuration in the most common configuration used in implementing LNA. Topology to be used to design LNA is decided by the applications it is being designed for. Parameters that are to be optimised are application dependent and hence topology must be properly chosen so as to obtain better results.

1.5.5 STABILITY

A device is of no practical use if it is not stable at the required operating frequencies and other conditions which include temperature as well. An amplifier is considered as stable if it is able to resist conditions which may destroy the system. A system should be designed such that is able to overcome conditions which cause hindrance to proper operations of the circuit. LNA may become unstable due to ground and other parasitic capacitances and inductances which arise during fabrication and packaging of the circuit. For example if a large series inductance appears across gate terminal of a

transistor operating in common-gate topology it may create a sufficient amount of feedback in the circuit which may result in instability of the circuit.

1.6 LNA DESIGN PARAMETERS

LNA's performance is characterised by the values of LNA parameters obtained after completion of our design. These values can be obtained by performing simulations using tools which are used for studying behaviour of our circuit at higher frequencies. Before fabrication of our device we need to analyze our design using simulations to get an idea f how the design will perform in real-time environment.

1.6.1 S PARAMETERS

When we move towards analysing circuits at higher frequencies that are in the rage of microwave frequencies port parameters such as Z-parameters, ABCD parameters cannot be evaluated. At higher frequencies these port parameters cannot be obtained because of the following reasons:

(i) Open circuit and short circuit conditions are difficult to achieve at these frequencies

(ii) Sophisticated equipments are not available at higher frequencies to correctly measure the voltage and current in the ports

(iii) When dealing with wave propagation open circuit and short circuit conditions introduce reflections which may damage the device under test

At higher frequencies we define parameters called scattering parameters or S-parameters which act as a tool which makes the analysis of the circuit possible at higher frequencies without creating damage to the device under test. S parameters help us in studying the input-output relations between the different ports of a device in terms of power incident or reflected. S-parameters are usually displayed in a matrix format, with the number of rows and columns equal to the number of ports. For the S-parameter S_{ij} the j subscript stands for the port that is excited (the input port), and the "i" subscript is for the output port.

Sij= Power reflected from port j / Power incident at port i

Thus S_{11} refers to the ratio of the amplitude of the signal that reflects from port one to the amplitude of the signal incident on port one.

$$\begin{Bmatrix} b_1 \\ b_2 \end{Bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{Bmatrix} a_1 \\ a_2 \end{Bmatrix}$$

Fig.1.2 Scattering Matrix

The matrix [S] is called scattering matrix, where [S_{11}] is the input reflection coefficient, [S_{12}] the reverse transmission coefficient, [S_{21}] is the forward transmission coefficient, and [S_{22}] is the output reflection coefficient. The S parameters can be calculated individually by using given expressions:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a2=0} = \frac{reflected\ power\ wave\ at\ port1}{incident\ power\ wave\ at\ port1}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a2=0} = \frac{transmitted\ power\ wave\ at\ port2}{incident\ power\ wave\ at\ port1}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a1=0} = \frac{reflected\ power\ wave\ at\ port2}{incident\ power\ wave\ at\ port2}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a1=0} = \frac{transmitted\ power\ wave\ at\ port1}{incident\ power\ wave\ at\ port2}$$

Fig. 1.3 S-Parameters

1.6.2 NOISE FIGURE

Noise figure of an LNA directly affects the performance of the receiver; however other components of the receiver also affect the performance because we really design an LNA in isolation from other blocks of the receiver. The low noise figure requirement of an LNA generally restricts the circuit topologies that can be used for designing a LNA because as we increase the number of circuit elements the noise contribution also increases. Hence we have to limit our circuit design to a less no of transistors. This is done so that there are a few elements which are a dominant contributor to noise figure. Few configurations provide a higher noise figure which is not desirable.

Typical Noise Figure offered by an LNA is around 2-3 dB. Noise Figure of the LNA affects the performance of the receiver system directly.

1.6.3 GAIN

Gain offered by the LNA should be high enough to overcome the effect of noise from subsequent stages of the receiver system.

Gain of the LNA is desired to be high because LNA is placed at the front end of the receiver and it should provide a gain which is sufficient enough to suppress the noise contribution of the subsequent stages. However a higher gain makes the circuit non-linear. There is a trade-off between higher gain and a high linearity which should be kept in mind.

1.6.4 INPUT RETURN LOSS

LNA is placed at the initial stages of the receiver but before LNA receiver system also consists of antenna and a filter placed before the LNA. Interfacing LNA with the antenna requires analysis of many factors which should be incorporated in the design.

If we consider LNA as a voltage amplifier we would prefer the input impedance of the antenna to be very high whereas if we want to obtain better noise performance we will have to precede the LNA with a transformation network. To transfer maximum power we would wish to provide conjugate matching between the LNA and the antenna. However we will have to make choice between these factors which should minimise reflection in the system.

(1) If a filter is placed before the LNA it should be properly matched with the input impedance of the LNA. Generally a filter is designed with a 50Ω termination and if the input impedance of the antenna deviates from the standard 50Ω impedance the filter may exhibit ripples in the pass band and will not produce required response.
(2) Even if filter is not used, antenna is also designed with certain load impedance which should be kept in mind while designing LNA and interface of LNA with antenna can be managed to provide conjugate matching between the two stages.
(3) In practical circuit implementation, the signal after being received from the antenna should travel a certain distance on the circuit board before reaching the receiver block. If proper matching is not provided it leads to attenuation and losses in the signal. This matching is significant at only the LNA antenna interface. Design of other components of the receiver need not focus on this parameter. They should focus on maximising output swings rather than power transfer.
Input return loss is a measure of input match and is expressed in dB.

1.6.5 LINEARITY

One important parameter at high frequency is the linearity of the circuit. When we

operate in small signal range we approximate the circuit by small signal models of its circuit elements. However non-linearity is also a factor of circuit performance and it may lead to certain interesting phenomena. If we apply a sinusoidal signal to a non-linear system, the output consists of harmonics of the input frequency. The harmonics generated may dominate the fundamental harmonic due to which the desired signal may get suppressed. We need to reduce the non-linearity i.e. we need to reduce the effect of harmonics on the fundamental frequency component.

A measure of non-linearity of an amplifier can be estimated by calculating IIP3 i.e. Input Third Order Intercept. A circuit with higher value of IIP3 is said to be more linear as compared to a circuit with lower value of IIP3. However a better IIP3 value is achieved at the cost of reduced gain.We need to make a choice between a highly linear circuit and a circuit with the high gain, we can only optimise one of these parameters. IIP3 can be depicted graphically as:

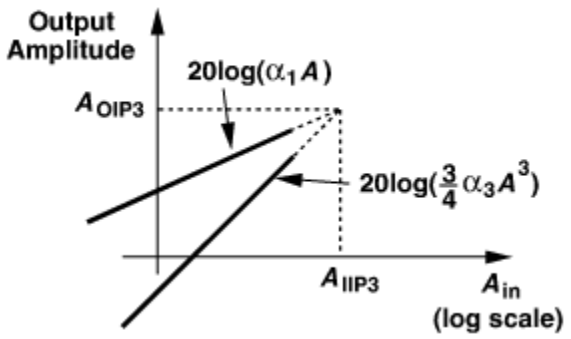

Fig.1.4 Input Third Order Intercept Point (IIP3)

To calculate the value of IIP3 for any circuit amplifier we use two tone tests in Advanced Design System(ADS). However we can also carry out theoretical calculations for IIP3 using relevant formulae. The result obtained during theoretical calculation is an approximate value of IIP3 as it assumes that only third order nonlinearity exists and it ignores the higher harmonics. When we consider the non-linear behaviour of the elements we observe that the gain decreases as we increase the input power level. Here we observe a new parameter i.e. 1dB compression point. It is defined as that input level which decreases the output gain by 1dB. Its graphical representation is given below:

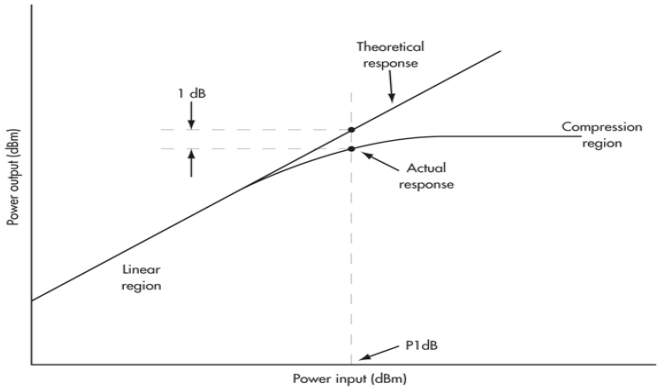

Fig.1.5 1 dB Compression Point

In most of the cases LNA does not limit the linearity of the receiver.

1.6.8 BANDWIDTH

Bandwidth of an LNA defines the frequency range over which the LNA provides desired performance. It may not necessarily be at a single frequency rather it can be a range of frequencies depending on the application domain. LNA must provide a flat response in the frequency range of interest and the gain variation should not be more than 1 dB. We intend to provide a larger 3 dB bandwidth than the actual band required to constraint the gain variation within 1 dB. Instead of referring to 3-dB bandwidth we refer to a circuit's fractional bandwidth.

$$'fractional\ bandwidth' = \frac{3\ dB\ bandwidth}{center\ frequency\ of\ the\ band}$$

For example IEEE 802.11g LNA should have a fractional bandwidth greater than 0.0328. LNA application which needs larger fractional bandwidth can employ a technique which can change the centre frequency of operation which in turn will improve the fractional bandwidth of the circuit.

1.6.9 POWER DISSIPATION

There is a trade-off between noise figure, linearity and the power dissipation of a circuit. However LNA consumes only a small portion of total receiver power. Hence we can improve the noise performance of the LNA as it is more critical for receiver performance. So we do not need to be more specific about the power consumption of the circuit. However for applications in IoT power consumption of the circuit is the most important factor that should be optimised to make it compatible with the newer technologies.

Demand for devices consuming less power is increasing and Bluetooth communication itself requires less power consuming devices which can facilitate longer working hours. Recent research topic IoT and other low power applications have increased the utility of BLE devices as well which are designed to consume less power and are capable of operating on low cost batteries. Power consumption of LNA becomes a crucial factor in determining the application of LNA. LNA designed for application in Bluetooth and BLE should have low power design if it is to be made suitable for practical implementation.

1.7 NOISE CONSIDERATIONS

Noise affects the performance of the RF systems. If noise was absent receiver sensitivity would be very high i.e. receiver will be able to detect very weak signals as well. Noise analysis of a circuit is necessary and it can be done using time domain techniques as well as frequency domain techniques. Time domain analysis of noise is capable of providing limited information about the effect on noise i.e. noise power. However analysis in frequency domain provides a deeper insight into the effect of noise. Power Spectral Density needs to be defined for easier analysis of noise produced in a circuit. Choosing PSD for noise analysis helps us to apply operations that can be applied on random signals as noise is random in nature. If PSD at the input of a system is known PSD at the output can be determined easily if the system's response in known beforehand. Noise is random in nature i.e. its instantaneous value cannot be predicted

In order to analyze noise performance of circuits, we need to create a model which represents all the elements connected in the circuit by modelling noise of these constituent elements. We should know the equivalent noise model of all the elements being used in our circuit.

1.7.1 THERMAL NOISE

Thermal noise is caused by random agitation of electrons in a conducting material. This agitation is caused by heat or temperature.

1.7.1.1 THERMAL NOISE IN RESISTORS

Resistors are employed in almost every circuit and they are a source of thermal noise as well. Charge carrier exhibit random motion with increase in temperature. Due to

ambient temperature also the charge carriers in resistors get agitated and they follow a random path. Because of random nature we study noise in terms of its Power Spectral Density (PSD). Noise in a resistor can be modelled by a voltage source with PSD of $4KTR_1$. Norton equivalent can also be used for modelling which will be represented by a current source in parallel with PSD of $4KT/R_1$.

If we can model a circuit in terms of resistance we can represent the noise of the circuit by the equivalent formula by replacing the resistance by the equivalent resistance. This model is not only applicable to lumped elements but it can be applied to antenna as well

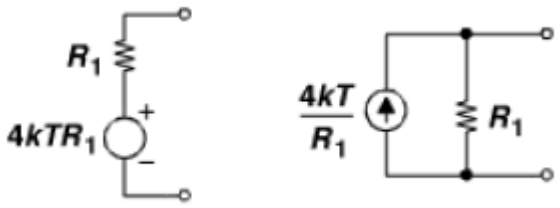

Fig.1.6 Thevnin and Norton model of resistor thermal noise

where the resistance denotes the radiation resistance of the antenna. PSD of the antenna will be given by:

$$(V_{n,\,ant})^2 = 4KTR_{Rad}$$

Where R_{Rad} is the radiation resistance of the antenna.

1.7.1.2 THERMAL NOISE IN MOSFETS

Mostly we operate mosfet in saturation region in our circuit. In saturation region noise in mosfet can be modelled by a current source connected between the source and drain terminals of the device.

$$I_n^2 = 4KT\gamma g_m$$

Where γ is the excess noise coefficient and g_m is the transconductance of the MOS. Value of γ is determined by many factors. It depends on the channel length of the MOS being used and also depends on CMOS technology being used. γ takes vale 2/3 for long channel devices and takes higher values for devices with shorter channel. It may take value 2 for short channel devices. Another component of thermal noise is also present in

MOS that arises from gate and it increases with decrease in gate length. Gate resistance is given by:

$$R = \frac{W}{L} * R'$$

Where W is the width and L is the length. R' denotes the sheet resistance of the polysilicon used in fabrication of the device. This gate resistance is distributed over the entire width of the transistor which makes analysis of noise contribution from this resistance difficult. It can be made easier by representing it by a lumped model which has a gate resistance of $R_G/3$. [30] PSD of noise due to gate resistance can then be given by the formula:

$$V_n^2 = 4KT * \frac{R_G}{3}$$

A device is preferred if the noise added by it is always less than the channel noise. RF circuits are intended to work at higher frequencies which in turn affect the noise in the device. Thermal noise current at higher frequencies becomes the source of an additional noise component which is known as 'gate induced noise current'. [31] However this current is generally ignored in simulations and practical calculations as well because it is no significant to the device performance.

1.7.2 FLICKER NOISE

Flicker noise is also observed in MOS devices. As thermal noise can be modelled flicker noise can also be modelled in a MOS by placing a voltage source in series in with the gate terminal on the MOS. PSD of this noise is given by:

$$V_n^2 = \frac{K}{WLC_{ox}} \frac{1}{f}$$

Where K is process-dependent constant and it is lower for PMOS devices and has a higher value for NMOS devices. Value of K is lower in PMOS because it carries charge carriers well below the surface and hence has a less no dangling bonds.[32] This noise component is larger for noise components which vary slowly because of 1/f dependence. PSD of flicker noise may intercept PSD of thermal noise of a device at some frequency which is termed as corner frequency. Flicker noise has 1/f dependency which reduces its significance at higher frequencies.

1.8 LNA TOPOLOGIES

Parameters which should be kept in mind while designing an LNA provides an important lead so as to which topology should be chosen to design an LNA circuit. LNA determines the receiver performance, designing a LNA with consideration of all parameters within specified limits presents a demanding situation for all the researchers .Out of all the available topologies we have to analyze which topology is better in terms of these design parameters. LNA's utilise configurations that are being used traditionally to design amplifiers. Other than configuration additional steps are to be taken to achieve the desired performance. It can be obtained by introducing a change in the biasing network or it can be through a change in matching networks being used.

Most common LNA topologies are common-gate, common-source, cascode etc. Each of the above topology has its own advantages and disadvantages. In-spite of their own merits and demerits the cascode configuration in the most common configuration used in implementing LNA.

1.8.1 COMMON-SOURCE STAGE WITH RESISTIVE LOAD

This configuration is rarely used in practical applications. This configuration is not adequate to be used in practical applications as it is not able provide proper matching which is the most important factor in the design of LNA. Improper matching gives rise to reflections and most of the power is reflected back if the matching is not proper. This reflected power creates a hindrance to the proper operation of the other circuit components as well. Moreover LNA's are designed to be implemented at high frequencies and this design is not desirable for operation at high frequencies which further restricts its practical applications.

Gain offered by this topology is dependent on the supply voltage being used in the circuit. If we reduce the supply voltage the gain offered by this configuration will be reduced. In the latest CMOS technology this circuit provides a very poor performance as the supply voltage gets reduced with the CMOS technology.

$$|A_V| = g_{m.}R_D$$

Where,

A_V is the voltage gain

$$|A_V| = \frac{2.V_{RD}}{V_{GS}-V_{TH}}$$

Where,

g_m is the transconductance, V_{RD} is the voltage drop across the resistor

For new technologies we work on lower voltages and hence the gain further reduces if we use resistance in our circuit. This dependency is observed if we consider the channel length modulation to be negligible and do not include it in our calculations. If the channel length modulation is also taken into account the gain is further lowered

1.8.2 COMMON SOURCE STAGE WITH INDUCTIVE LOAD

In order to evade the disadvantages of the configuration using Resistance as load we employ an inductor as a load in the configuration. Using an inductor as a load also felicitates the high frequency operation of the circuit. This topology offers provision of operating the circuit at lower supply voltage and high frequency. Operation at lower supply voltage is possible because inductor sustains a lower voltage drop than a resistor. Inductor as a load helps to achieve impedance matching as well as it resonates with the capacitor placed at the output terminal of the circuit.

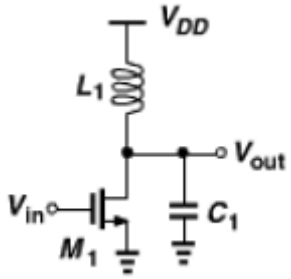

Fig.1.7 Inductively loaded Common Source stage

Along-with output matching we also need to analyze the input matching provided by this configuration. C_F is the capacitor that denotes the gate-drain overlap capacitance of the MOS. Other overlap capacitances are ignored as they are insignificant. On the basis of below circuit we can analyze the circuit for input matching.

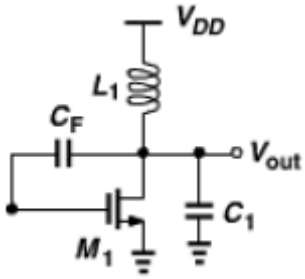

Fig.1.8 Inductively loaded Common Source stage – Input Impedance

On replacing the MOS by its equivalent circuit the circuit can be studied and we can

obtain the value of the input impedance. Impedance obtained has a real part and a imaginary part. Component values can be chosen accordingly and the real part can be made equal to 50 Ω and the imaginary can be equated to 0 to obtain the desired component values. When we try to achieve impedance matching at a frequency we end up having negative resistance at other frequency. If this frequency falls in region of interest it affects the functioning of the circuit and cause instability to the circuit as well.

To achieve optimum performance the effect of the capacitance C_F can be nullified by placing an inductor in parallel with it. Placing an inductor in parallel with this capacitance attains parallel resonance and neutralizes the effect of capacitance. However the capacitance C_F is small we need to place an inductor with large value in parallel with it to satisfy condition of resonance. Use of large inductors introduces parasitic capacitances at the input and output nodes which degrade the performance of the circuit significantly. Hence this configuration is not suitable for use in practical applications.

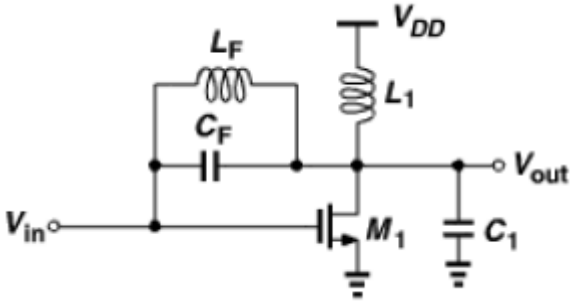

Fig.1.9 Inductor L_F to neutralise the effect of C_F

1.8.3 COMMON SOURCE STAGE WITH RESISTIVE FEEDBACK

Circuit design process gets altered if the frequency of operation gets changes. If the frequency of operation of circuit is a magnitude lower than transit frequency (f_T) of the transistor. Common Source with resistive feedback can be considered for implementing LNA in such scenario.

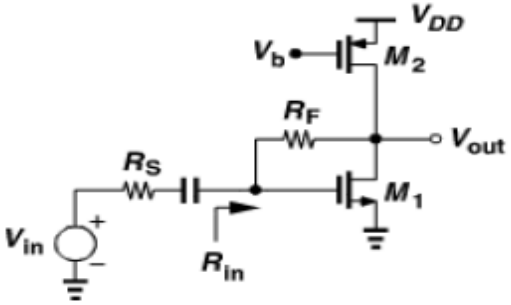

Fig.1.10 CS Stage with resistive feedback

In above configuration MOS M2 operates as a current source. Feedback resistor R_F provides feedback from the output to the input of the circuit. It senses the voltage at the output of the circuit and then sends a current signal in response to the voltage sensed. On simplifications gain of the above circuit comes out to be:

$$|A_V| = \frac{-R_F}{R_S}$$

Where R_F is the feedback resistor, R_S is input resistance.

As indicated by the above formula gain of this configuration is not dependent on the supply voltage. Hence this configuration evades the disadvantage of resistively loaded CS stage. Noise figure of this configuration is observed to be a bit higher. Noise figure of this configuration is given by:

$$NF = 1 + \frac{4R_S}{R_F} + \gamma + \gamma g_{m2} R_S$$

Where symbols have their usual meanings.

Even if we consider $\gamma = 1$, Noise Figure if this configuration will exceed 3 dB which is relatively large value of NF.

1.8.4 COMMON GATE STAGE

Apart from Common Source configuration, Common Gate configuration is also a possible candidate for implementing LNA. This configuration is striking for LNA design owing to low input impedance of Common Gate stage. In this configuration resistance is not preferred as load the reason being the same as discussed earlier. Inductively loaded Common Gate configuration is used and the inductor at the load resonates with the capacitance connected the output terminals. MOS is used in Common Gate configuration and the parameters of MOS are chosen such that it is able to provide an input impedance of $50\ \Omega$.

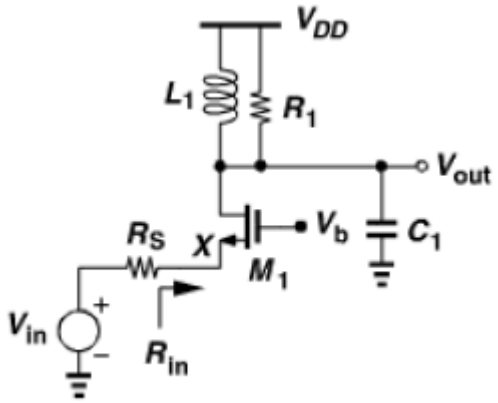

Fig.1.11 Common Gate Stage

In above calculations we neglect the channel length modulation of the MOS. As stated before the input impedance of CG stage is low but this happens only when we assume the channel length modulation to absent. If we consider the channel length modulation, input impedance of this configuration is very high which is a drastic change in the circuit parameter . Techniques have been proposed which tend to deal with this condition as well. One such technique is to use a cascode Common Gate stage to lower the input impedance of the above configuration which came into existence because of the channel length modulation.

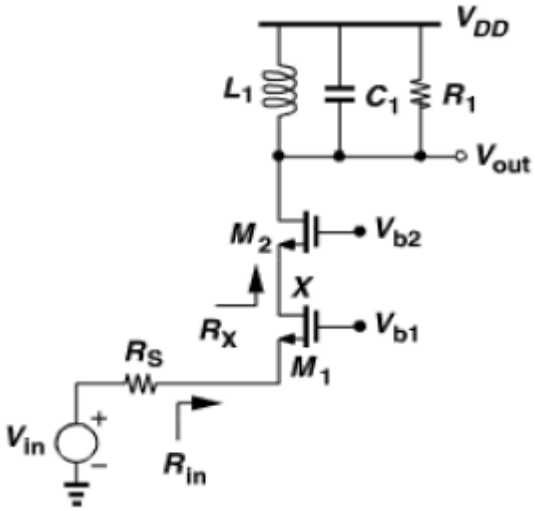

Fig.1.12 Cascode common gate stage

In order to account for noise inefficiency CG configuration generally employ an inductor in their bias networks. Introducing an inductor also helps to neutralize the input capacitance of the circuit. Because of addition of a new circuit component an inductor additional noise gets added to the circuit, Additional noise can be removed by using a proper biasing network for the circuit. This biasing should be provided such that is removes the effect of noise added by the inductor as well as resolves the problem of input matching. Moreover in new technologies inductors can be easily fabricated on chip which makes the implementation of circuits with inductors trouble free.

1.8.5 CASCODE STAGE WITH INDUCTIVE DEGENERATION

We observed that using a capacitor to achieve input matching creates a problem of negative resistance at certain frequencies. We require a configuration that should be able to address this issue and provide a reliable solution to this. We need a configuration that

should provide isolation between the input and output which helps to remove the effect due to feedback and an alternate method of achieving input impedance other than the gate-drain overlap capacitance which is the root of all these problems.

To achieve input matching we prefer a circuit with active devices rather than using passive devices to reduce the noise contribution from circuit components. This configuration is one of the methods to do so. The input impedance of the configuration can be given by the expression:

$$Z_{in} = \frac{1}{s.C_{GS1}} + L_{1.}s + \frac{g_m L_1}{C_{GS1}}$$

The input impedance of the configuration contains a frequency dependent part and a frequency independent part. The frequency independent part can be made equal to 50Ω by choosing appropriate values of the components. Typically the value of inductor used comes in the range of pH. To realise 50Ω input impedance, inductor with value in pH need to be implemented. Inductors are implemented using bond wires because they need to included in design and cannot be realised off-chip. Degeneration inductor cannot be placed off-chip under any circumstances as it is a part of the circuit. Using bond wires realising an inductor within pH range is very tedious task. Even after using technique to obtain minimum inductance, we achieve an inductance value in nH which is much larger than required value. If we realise inductor using bond wires and input impedance greater than 50Ω is achieved which disturbs the input impedance match.

To obtain an input impedance of 50Ω as well as realise it using bond-wire inductors we need to reduce the transit frequency of the mosfet. It can be done by increasing the channel length of the transistor or placing a capacitor in parallel with the $C_{GS.}$ We calculate the above impedance values by neglecting C_{GD} and $C_{SB.}$

If we include the effect of C_{GD} in our calculations we observe that the input impedance is further lowered if C_{GD} is included.

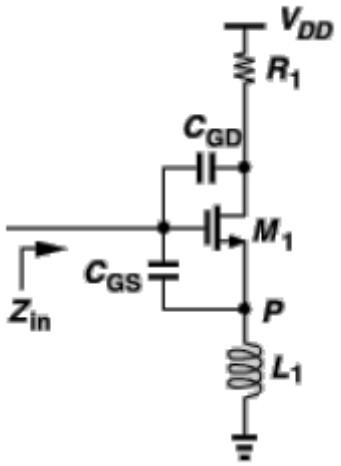

Fig.1.13 Input Impedance in presence of C_{GD}

We observe that the input resistance falls by a factor of (1- $\frac{2C_{GD}}{C_{GS}}$) which becomes 1 if effect of C_{GD} is neglected.

With C_{GD}, input pad capacitance of MOSFET also lowers the input impedance which should also be taken care of.

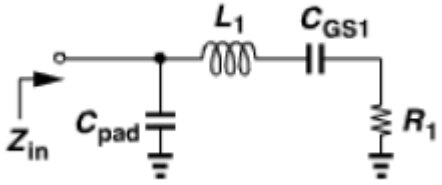

Fig.1.14 Impedance in presence of pad capacitance

On inclusion of pad capacitance we observe that the degeneration inductor is not sufficient enough to resonate with the capacitance to provide an input matching of 50Ω. Hence we place an inductor in series to achieve the required inductance value to achieve impedance matching.

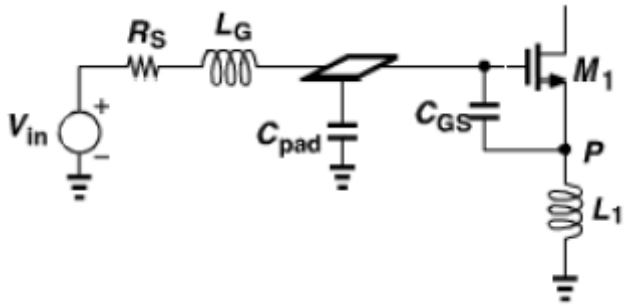

Fig.1.15 Addition of L for impedance matching

Noise figure of above configuration is computed to be :

$$NF = 1 + g_m R_S \gamma . \left(\frac{w_o}{w_t}\right) \text{^}2$$

Where w_o is the frequency of interest, w_t is the transit frequency.

1.8.6 NOISE CANCELLING LNA

In calculations related to noise figures of the above configuration we obtained terms signifying the noise because of resistor R_S, noise due to load resistor and the noise contribution of the transistor. The noise added because of the resistor cannot be removed as the charge carriers will exhibit random agitation in presence of ambient heat. In noise cancelling LNA's we aim to reduce the effect of noise added by the input transistor. These LNA's work on the principle that if two signals with opposite polarities are added they cancel each other's effect and if two signals with same polarity are added the resultant signal has an increased strength.. We identify two nodes in LNA where the required signal appears at opposite polarity and noise appears with same polarity. We can scale up the signals at the available nodes and add them further such that the signal components add up and the noise components cancel each other..

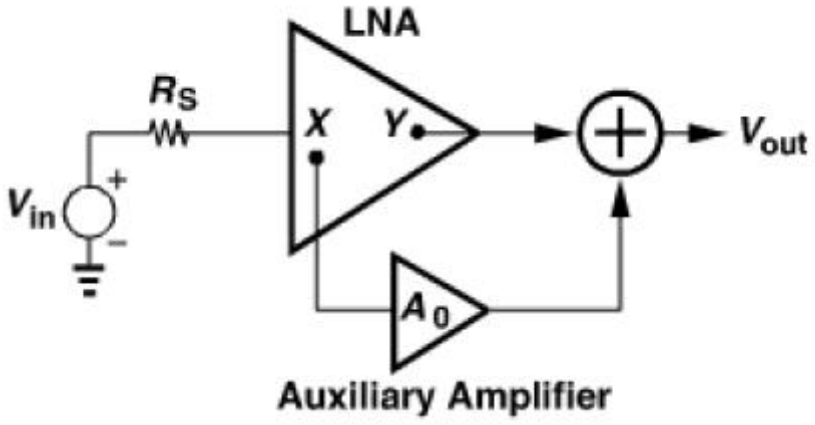

Fig.1.16 Noise cancelling LNA

We observe that CS stage with resistive feedback provides two nodes within the circuit with required polarities between the signal and the noise. Two nodes available are the gate and drain of the transistor. Noise current of the resistors appear at the gate and drain terminal with the same polarity whereas the signal reaching the nodes experience inversion.

1.8.7 REACTANCE CANCELLING LNA

This configuration is designed such that it cancels the effect of its own input capacitance.

This configuration is designed by the idea that input inductive impedance can be exploited to cancel the effect of input capacitance. The methodology used for obtaining input matching holds for frequencies up to the frequency of interest i.e. input matching provided depends on the frequency of interest as well.

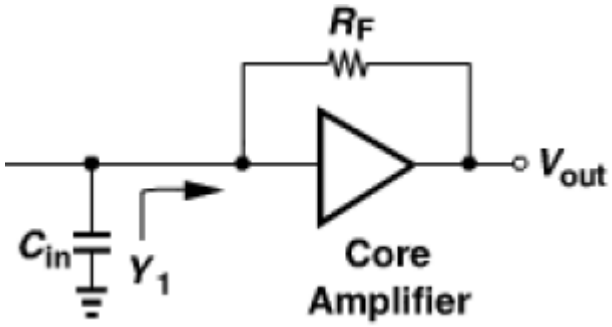

Fig.1.17 Reactance Cancelling LNA topology

Apart from these basic topologies numerous topologies have been reported which utilise these configurations only and then further modify them according to the requirements so as to which parameter is to be optimised. Out of these configurations Common Gate and Common Source cascode configuration are the most extensively used as far as practical applications are concerned.

CHAPTER 2
LITERATURE SURVEY

Before we proceed with any design we must have an understanding of the previous work done in the particular field. Every new design incorporates a new technique that can be helpful in understanding the design process in a better way.

Muhammad Waqas Qadir et.al reported a Low Noise Amplifier that was implemented using CMOS 130-nm technology.[33] The reported amplifier was designed for wireless communications i.e. frequency of operation was restricted to 2.4 GHz. The reported amplifier was provided with an output matching using a NMOS varactor diode along with additional circuitry. Having multiplex register control along with data-path interconnect assisted to achieve minimum ripples in the pass band of the amplifier. The amplifier was implemented using cascode topology with inductive degeneration and also implemented it using a differential structure. The reported amplifier also used multigrain control technique and different modes were also available. Modes could be chosen using signals which were known as gate bias control signals V_{LOW} and V_{MID} with V_{SLEEP} control.

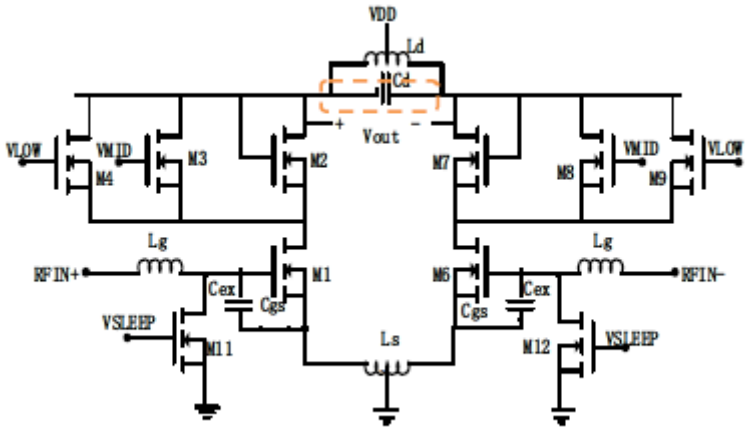

Fig.2.1 LNA with multigrain control(reproduced from[33])

The amplifier consists of a differential structure designed with the help of transistors M6-M7 and also includes the transistors M1-M2 in the core design. These transistors were biased such that they operated in saturation regions and obtaining a larger value of transconductance became easier.[34] Different modes had different gains and it could be controlled with the help of some mechanism which used control signals to do so. Transistors M3-M4 were added in parallel to the transistor M2 without disturbing the input matching of the circuit and this lowered the gain of the amplifier by 3-4 dB. Similar transistors were connected on the other side of the differential structure. This amplifier

was reported to have three different modes having different parameter values. Gains offered by different modes were 25/20/10 dB that were controlled by the gate control signals in the circuit.

Lei Liao et. al[35] reported a receiver system which was intended to be used in Bluetooth Low Energy Applications and consisted of LNA, mixer and a complex band pass filter whose bandwidth could be varied. We are concerned with only the LNA design, hence we do not need to study the other blocks thoroughly. The complete receiver system front-end was implemented in 130nm technology and operated with a supply voltage of 1.2 V and the current was found to be 2.7 mA. LNA design in this receiver front-end used common gate topology. This topology was chosen for this receiver system because the common gate topology is seen to offer a highly linear circuit but at the cost increasing Noise Figure which comes around 3 dB. This topology was considered apt for this receiver system because this system was designed for BLE applications which are used in short range wireless communications. Hence the noise requirements of the system are relaxed in comparison to other circuits.

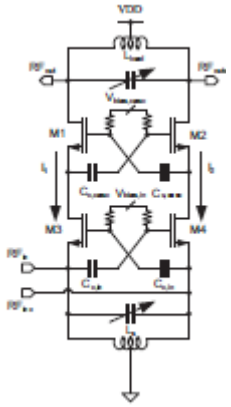

Fig. 2.2 Differential Common Gate LNA

Along-with high linearity improved noise performance was obtained by this circuit using a technique in which cross-coupling was used without disturbing the salient features offered by common-gate amplifier. This LNA offered a gain of 23 dB and a noise figure of 3 dB was obtained at the frequency 2.4 GHz which makes it apt for wireless communications. This LNA circuit was seen to have very large variations in the values of Noise Figure which is not desired and not under acceptable limits. To reduce these variations certain modifications were made to the circuit using an additional bias circuit. This bias circuit consisted of a current mirror using MOS and was connected with the main LNA design. LNA formed a complete differential structure and the performance of LNA remained unaltered with the introduction of the new bias circuit. The current

consumption of the circuit also remained unaltered if the current mirror factor was se according to requirement and was chosen large enough. Introducing this additional bias circuit reduced the variation in Noise Figure and gain of the circuit by a significant amount.

As discussed before LNA with all parameters with perfect values is very difficult to design as there is a trade-off between the design parameters of LNA. LNA's with high gains are reported as well LNA with high linearity are also considered equally important as it is also one of the most important parameter of LNA design.

Rahul Sreekumar[36] et.al reported a LNA which was highly linear and was designed in CMOS 45nm technology. LNA was implemented using the most widely used topology i.e. cascode topology. This LNA was intended for use in Bluetooth applications and hence the operating frequency was confined to 2.4 GHz.

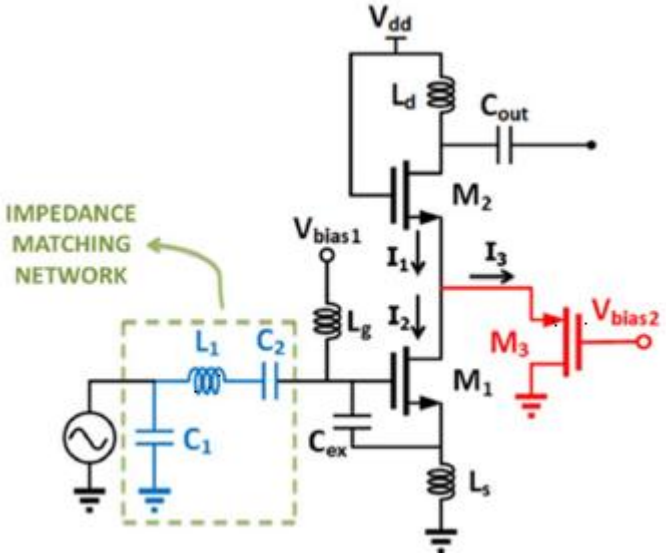

Fig.2.3 Cascode stage based LNA (reproduced from [36])

The reported amplifier used IMD (Intermodulation Distortion) technique to achieve high linearity.[37] This technique improved the linearity of the circuit by adding a PMOS as a IMD sink to the circuit. PMOS used was biased such that it cancelled the first and third order transconductance of the transistor M1 and hence the non-linearity effects by the input transistor M1 were nullified by the externally connected PMOS. This technique had an advantage that using PMOS did not affect the matching of the circuit and hence prevented power losses in comparison to the other techniques.[38] The amplifier was reported to provide a gain of 14.1 dB at the intended frequency i.e. 2.4 GHz.

The circuit operated on a 1V supply and had a input return loss of -18.35 dB at the

required frequency. Noise Figure of the circuit was 1.42 dB and the power dissipation of the circuit was also very less which was reported to be 1.9 mw. 1db compression point of the circuit was reported to be -9.87 dBm.

Sinyong Kim et. al [39]reported a receiver system that was designed to consume ultra-low power and was intended to work at frequency used for wireless communications i.e. 2.4 GHz. The prototype of this receiver system was implemented in 65nm technology. The receiver system reported composed of a LNA and a mixer block which was equipped with quadrature-G_m stage which was helpful in reducing the power consumption in Local Oscillator path of the receiver. Using a quadrature stage reduces the power consumption because other additional which are required in a typical receiver system need not be employed in this system and hence it reduces the power requirements of the circuit. Quadrature signals are generated in the Local Oscillator path and other blocks are required for generation of these signals. A significant amount of power is consumed by these blocks. In this system these quadrature signals are generated within the mixer itself and additional blocks are not required which therefore reduces the power requirements of the circuit.

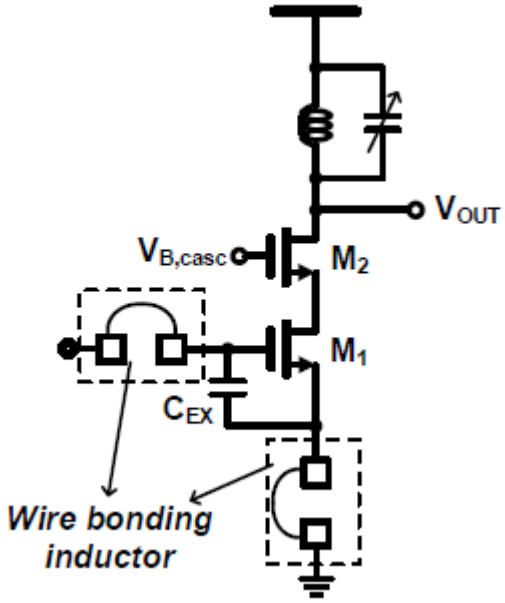

Fig. 2.4 CS stage LNA (reproduced from [39])

LNA used in this receiver system used wire-bound inductors which tend to decrease the chip area of the system. Using a cascode stage for LNA gave an advantage of better isolation between the input and the output stage and a higher gain as well. The receiver system was found to consume a power of 0.9 mW which is very low as far as complete receiver system is concerned and this system can be chosen for BLE applications. The

complete system was reported to provide a conversion gain of 36 dB which is very good value for a system to be used in BLE applications. NF of the system was found to be 2.1 dB and had an IIP3 value of -26 dBm. The input return loss of the system was found to be -10 dB in the frequency band of interest.

Lin Min[40] et. al reported an amplifier which was also intended for Bluetooth applications and was designed in 180nm CMOS process. The reported amplifier was designed to provide a gain of 25 dB and consumed 16 mW power operating on a 1.5 V supply. Noise Figure of the amplifier was reported to be 2 dB which is a very good value if the amount of power consumed by the circuit is also checked upon. This amplifier used Common Source configuration along with a cascode MOS to reduce the effect of miller capacitance. The reported amplifier also used differential structure which helped to reject the common mode signals and reduce the amount of interference from these signals. Using differential structure in amplifier also assisted to keep all MOS used in core LNA to be stable when operated in saturation region.

To improve the noise performance of the circuit, additional measures were taken that helped to reduce the components of the noise by a significant amount.

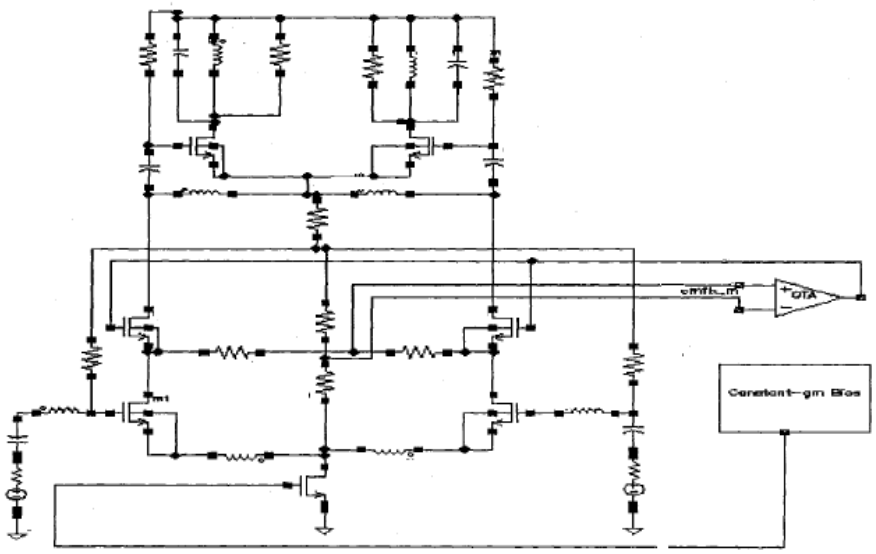

Fig. 2.5 Schematic of LNA(reproduced from [40])

Distributed gate resistance of the device was reduced by interdigitating the gate of the device. Using MOS model to analyze the noise performance of the circuit helped to decide the dimensions of the device which will provide a better noise performance. Power consumption of the device was kept under constraint while designing the LNA with minimum Noise Figure. Minimum Noise Figure of the device was found to be 1.6 dB and was observed at a frequency of 2.4 GHz. IIP3 of the LNA was found to be 8.5 dBm which

is in accordance with the Bluetooth standards. Noise results obtained from virtual simulations are better whereas the results get lowered if practical observations are considered because simulations are not able to include all practical aspects.

Zeenal Afreen Khan [41] et. al reported a LNA which was capable of providing optimum performance over a wide range of frequencies i.e. a broadband amplifier. Darlington amplifier is a great choice if broadband amplifier is to be implemented. This amplifier was designed in steps which included the design of input – output matching networks and the core amplifier which was designed in darlington configuration which is ought to provide a broadband characteristics. This LNA was designed with an objective that a better gain has to be provided to the signals and reflections are to be minimised providing a better noise performance. Amplifier design was broken into three parts which were input matching network, intermediate stage and the output matching network.

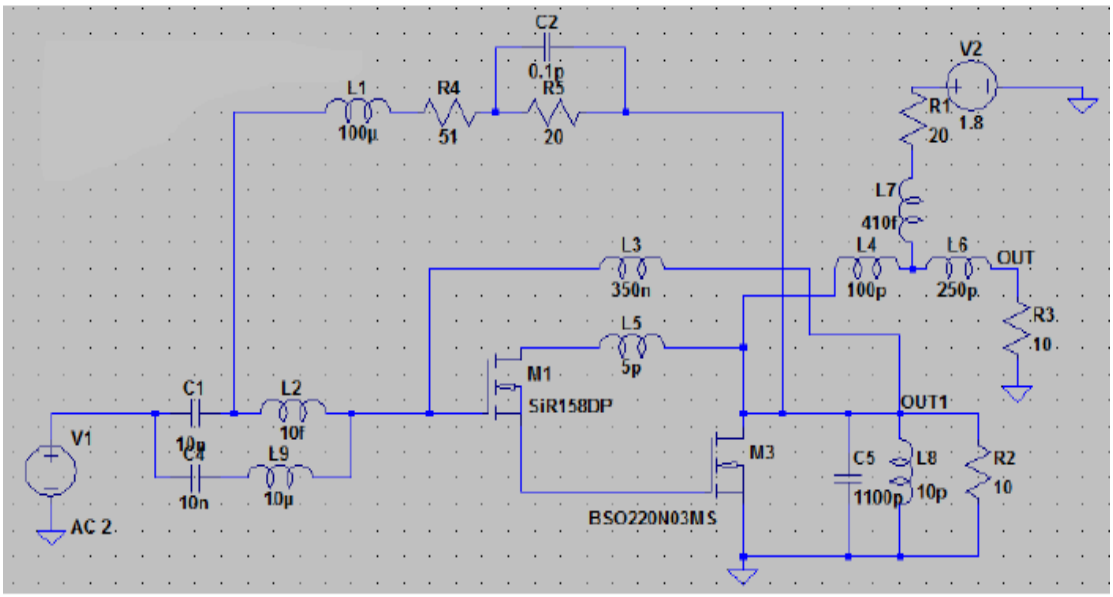

Fig. 2.6 Schematic of LNA (reproduced from [41])

Input and output matching networks were designed using LC elements and worked on the principle of resonance. Intermediate stage was followed by two two parts, one was intended to provide broad bandwidth to the amplifier and the other part of the circuit was dedicated to enhance the gain curve of the amplifier. In double order gain flatting technique of the amplifier double order inductive feedback was provided from the output stage to input stage which provided stability to the circuit and also reduces the reflection of the amplifier. The part of the circuit which was used to enhance bandwidth used a low-pass and a high-pass filter which were designed using filter theory. Input return loss for this LNA was found to be < -10 dB for the frequency range from 1GHz to 10GHz and

minimum value goes up to -52 dB. Current gain provided by this circuit was 22 dB at a frequency of 1.2 GHz. Power consumption of this LNA was very low i.e. 809.11 pW.

Bhushan R Widale[42] et. al also reported a wideband amplifier which was designed for multiple band applications. This LNA was unique in its design as it was designed using micro-strip line and also employed negative feedback along-with a matching circuit. Apart from using micro-strip line it also utilised passive elements in its circuit. The author explained to complete design process of LNA giving detailed explanation of factors that are to be kept in mind for designing an efficient amplifier in terms of all important parameters. The amplifier was designed to provide optimum performance for wide band of frequencies and hence required stability analysis for all frequencies of interest so that it could be used for multiband applications without any modifications. Achieving optimum results for a wide band is very difficult to realise, hence strip-line structure was used to realise this amplifier. Using strip-line structure provided good gain and minimum noise figure over the wide band. The amplifier was suitable for applications in the frequency band of 500 MHz to 6 GHz.

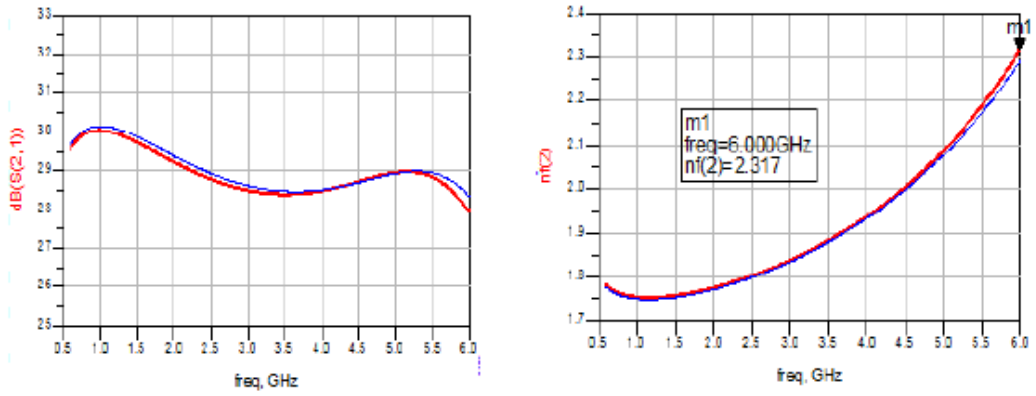

Fig. 2.7 (a)Gain Vs Frequency

2.7 (b) Noise Figure Vs Frequency

Gain curve of the amplifier provided a gain of 30 dB with a variation of 1 dB over the entire bandwidth and the curves representing other parameters also provided optimum performance within the frequency range specified. Negative feedback provided in the circuit played a major role in delivering optimum performance without sacrificing noise performance of the circuit. If proper technique is used to provide negative feedback it improves the response provided by the circuit and also provides better impedance matching. Negative feedback in the circuit enhanced the stability of the circuit and also reduced the amount of distortion produced in the signals. It also helped to reduce the effect

of temperature changes in the circuit performance. Noise Figure of the circuit was less than 3 dB for the entire band. The circuit performance was also analyzed at different values of temperature which showed that the parameters of the circuit did not vary much with temperature changes and the circuit was immune to temperature variations as well. Ayari Nadia et. al [43] reported an LNA dedicated for Bluetooth applications and fabricated in 130 nm CMOS technology. Aim of the design was to reduce power consumption of the circuit while maintaining the other parameters and retaining the noise performance, gain and input –output matching of the circuit. The amplifier used cascode structure along-with inductive degeneration i.e. placing an inductor at the source of the MOS transistor used in cascode structure. An inductor was placed at the gate to achieve input matching. Value of C_{gs} and g_m are also selected as per the input matching requirement of the circuit.

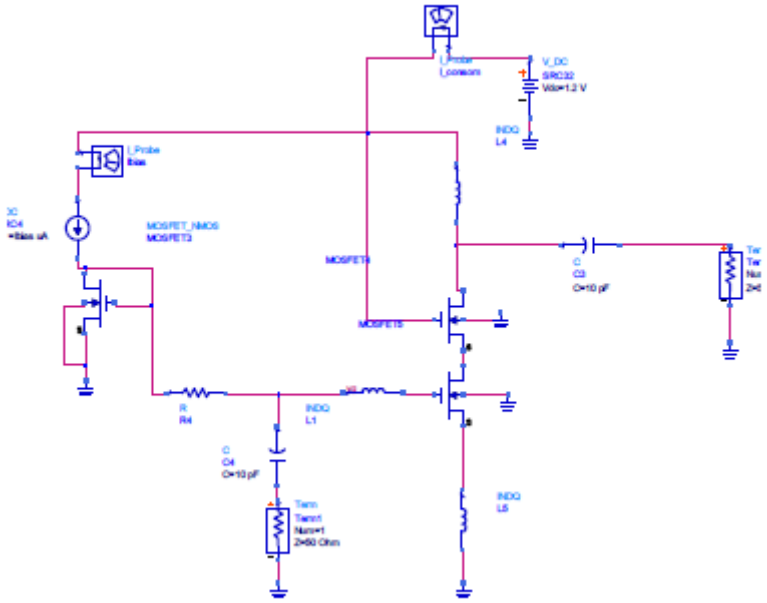

Fig. 2.8 Schematic of LNA(reproduced from [43])

Cascode structure uses a common source structure in cascade with common gate which increases the output impedance of the device. Additional cascode device is also used which is configured as a diode. Inductor connected to the gate of the cascode structure prevents any reflection from the main circuit to the source. Value of this inductor determines the gain response of the circuit and the gain response can be altered by changing the value of this inductor. The circuit operated at a supply voltage of 1.2 V and achieved a maximum gain of 20.343 dB at the frequency 2.4 GHz. Noise figure of the circuit was found to be 1.98dB and 3dB and these values were obtained for the

frequency 2.4-2.5 GHz. Results of simulations justified the observation that a highly linear circuit with a good dynamic range was designed. Circuit had a value of IIP3 equal to 10 dBm which indicates a highly linear circuit. Power consumption of circuit was found to be only 7.99 mW. LNA reported in[43] was reported to have a power consumption of 7.3 mW which is considerably high if we desire to use LNA in BLE applications. Power consumption of the circuit solely determines the application area of the LNA. If power consumed is relatively low it is considered suitable for BLE applications otherwise it may be restricted to Bluetooth applications only.

Florian Krug et. al [44] reported a switched LNA which was designed to be integrated on chip and optimized according to a mixer stage with a input capacitance of 150 fF.

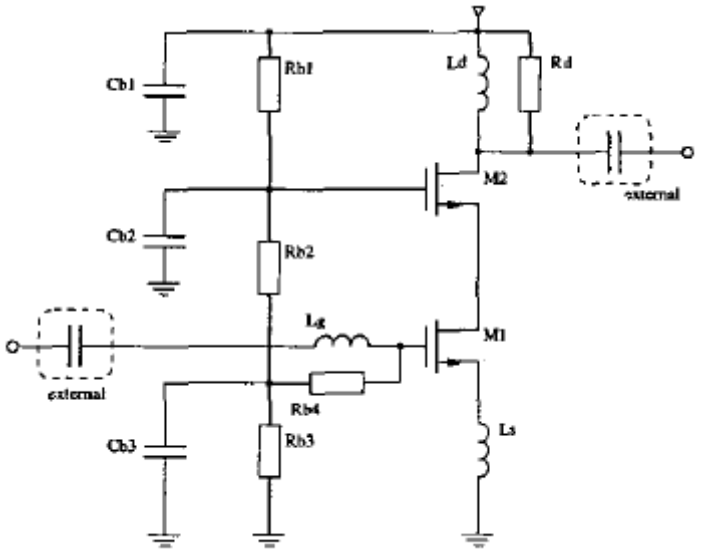

Fig. 2.9 Schematic of core LNA

The LNA was designed in 180 nm CMOS technology of Taiwan Semiconductor Manufacturing Co. (TSMC) which provided an option of copper interconnects between the top two metal layers out of the available six metal layers. The LNA used cascode configuration with inductive degeneration to meet the requirements of a LNA circuit. The width of the transistor in Common Source amplifier was set to 300µm and the one in common gate configuration had a width of 200µm. Circuit was designed to operate at a voltage of 1.8 V. Output stage of the LNA was designed in accordance with the next stage mixer which helped to improve the gain provided by the LNA in collaboration with the mixer stage. Switched LNA consists of core LNA with additional circuit for attenuation. The circuit consists of network used for switching and an attenuation network. In case we do not require to attenuate the signal, the attenuation network should affect the gain of the

circuit. In attenuation mode the core LNA circuit should not be functional which could be controlled by using a switching network which is done by placing an inverted in path of supply voltage. Noise figure of the LNA was found to be 3 dB at the operating frequency 2.4 GHz. Gain provided by the LNA was 7 dB and the gain provided with the mixer stage was found to be 16 dB. Power consumption of the circuit was 7.6 mw which is very low and is suitable for Bluetooth applications. The attenuation provided by the circuit was -17 dB when a 50Ω load was connected.

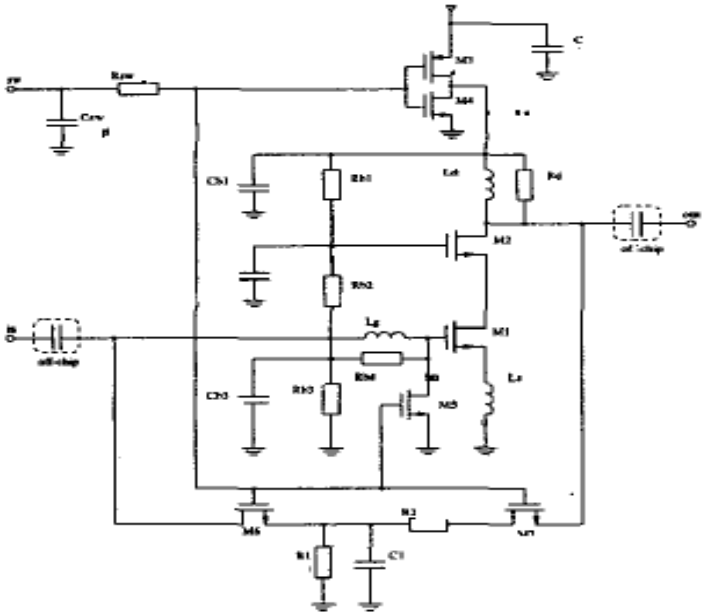

Fig. 2.10 Schematic of switched LNA

M Zamin Khan et. al[45] reported a LNA that was designed in 180nm technology and consumed very less power on operating from a supply voltage of 0.65 V. Cascode topology in the most common topology for implementing LNA but it cannot be operated on low supply voltages. The proposed topology offered circuit operation on low supply voltages as well. Inductive degeneration was also used to provide isolation between the input and output as well as achieve better noise performance. Cascode LNA was made to work at lower supply voltage by forward biasing the well source junction of the NMOS transistors. This modification lowered the threshold voltage of the transistor and facilitated low voltage operation of cascode device.

$$V_T = V_{T0} + \gamma[\sqrt{2\emptyset_F - V_{SB}} - \sqrt{2\emptyset_F}\ ]$$

Where V_{T0} is the threshold voltage when substrate is connected to ground,

γ is the body-effect coefficient,

$\emptyset_F$ is the surface inversion potential,

And V_{SB} is the bulk-source voltage

MOS M_b was used to provide bias for transistor in common-source configuration and the MOS used at the output terminal of the LNA was used as a buffer for output matching. Capacitor between the two stages was connected as a blocking capacitor to block Dc and allow ac signal to follow the path and enter the source terminal of the MOS connected in Common- gate configuration. Inductors which were small in magnitude (< 5 nH) were placed on chip and other larger inductors were placed off-chip. Noise Figure of the circuit was found to be 1.1 dB at frequency 2.4 GHz and a forward gain of 27dB at the same frequency. Circuit achieved good input matching as well which was justified by the value of parameter S_{11} which is found to be -11 dB at the desired frequency.

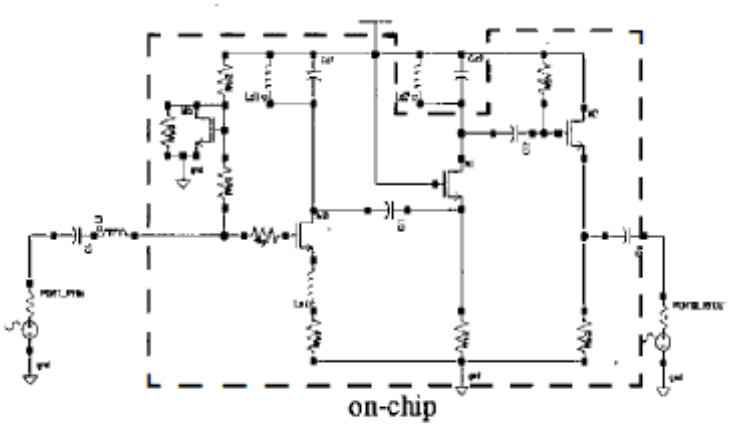

Fig. 2.11 Schematic of LNA (reproduced from [45])

IIP3 value of the LNA was found to be -30 dBm.

New technologies have improved the quality of circuits and the features provided by these technologies have made System on Chip(SoC) feasible. New CMOS technologies provide low cost, low power consumption and high integration along-with compatibility with other circuits makes them versatile for application in any domain. Wang Wen Qi et. al [46] reported a LNA in 250 nm technology and could be used in Bluetooth communications in accordance with the simulation results that were obtained as the values of parameters were found to satisfy Bluetooth standards. Inductors connected at the source and the gate of the MOS were used for input matching and the inductor and capacitor connected at the output terminals were used for output matching. Current mirror formed by the MOS NM0 and NM2 was connected to provide biasing to the input port. Value of the R_{bias} was selected to reduce the noise current in the circuit. Resistor R_{ref} was connected to adjust the drain current flowing into the MOS so that we can control the

power dissipation of the circuit according to the Bluetooth standards. Gate length and width of both the transistors used LNA was taken to be the same. Length and width of the transistor used for biasing were chosen according to the current requirement of the circuit which in turn decides the power consumption of the circuit.

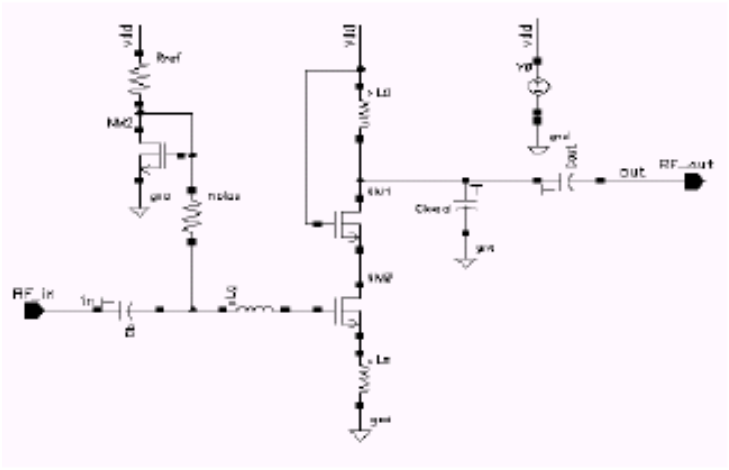

Fig. 2.12 Circuit showing single ended LNA

Formula for calculating the Noise Figure of this amplifier was found to be:

$$NF = 1 + \left(\frac{4\gamma}{g_m Q_{in}^2 R_s}\right)$$

.....Where Q_{in} is given by $R_S w_o C_{gs}$.

Above formula indicates that the noise figure of the circuit can be improved by increasing the value of Q_{in} or g_m. Gain of the amplifier at the required frequency i.e. 2.4 GHz was found to be 16.95 dB. Noise Figure of the LNA was found to be 2.96 dB. Power consumption of the circuit was 17.5 mW. Area of the complete chip was found to be 0.9 X 0.9 mm^2. This area also included the pads. Simulation results obtained were also compared with the results obtained after implementing it in practical applications. Practical results were in sync with the results obtained by simulations.

Table. 1 Comparison Table(Reproduced from 46)

	Simulation values	Practical values
Supply Voltage (V)	2.5	2.5
Gain (dB)	17.18	16.95
Noise Figure (dB)	2.82	2.96
IIP3 (dBm)	-5.1587	-
Operating frequency (GHz)	2.45	2.45
Power Consumption (mW)	13.5	17.5

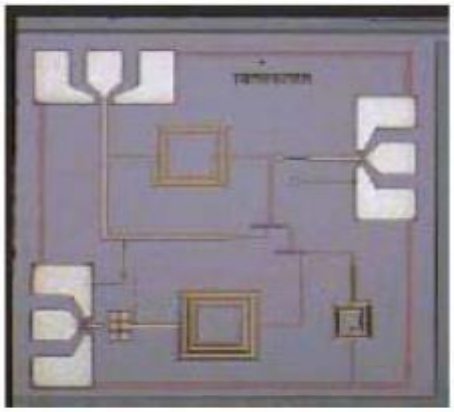

Fig. 2.13 LNA die after fabrication(Reproduced from(46)

The results obtained in tabular form are given below and these were also compared with the practical results:

CHAPTER 3

EXPERIMENTAL WORK AND RESULTS

We can use different circuits as load in our amplifier design and these circuits play a major role in the performance of the amplifier. We have implemented four major output matching networks in our LNA and compared the simulation results obtained to address the best output matching network for LNA circuits.

We observe a trade-off between the various parameters of the LNA. Change in one parameter of the LNA affects the other parameters as well. We observe a trade-off between the gain of the LNA and the linearity of the circuit. We desire a high gain LNA, however a higher affects the non-linearity of the subsequent stages of the receiver. Hence we need to confine our gain so that the non-linearity of the subsequent stages does not become prominent.

Before the LNA block, generally a pre-select filter is placed before the LNA. The filter is sensitive to the impedance matching at its output terminals.[10 from comparative study] Hence in our circuit design we need to focus on impedance matching networks at the input terminal also. Cascode configuration implemented by us incorporates inductors and capacitors to provide this input matching. Inductor placed at the input terminal and the inductor placed at the source end of the mosfet along-with the capacitance (C_{gs}) create an input matching network for our configuration. Other matching networks are also studied for this configuration and on comparison we observe the best circuit design.

We proceed with the design by considering the most commonly used configuration with inductive degeneration. Matching circuits used in a circuit play an important role in achieving desired circuit performance. Two matching circuits need to be employed in our circuit one of them provides input matching to the circuit and the other network provides output matching to the circuit. Output matching circuit is also referred to as load. Basic configuration remains same for all the circuits i.e. cascode topology with inductive degeneration and the technology used for all circuit designs is 45nm CMOS technology.

Before proceeding to fabrication of a design we perform simulations using simulation tools available that helps us to analyze circuit performance at different frequencies. Advanced Design Systems (ADS) is one such tool which is used in high frequency analysis of circuits and since we are operating at 2.4 GHz which is high frequency we use this tool to perform our simulations.

We proceed with a previously used circuit configuration and make improvements in the

parameters of the circuit which improves our design. Since we intend to design a circuit for Bluetooth and BLE applications we must keep a record of power consumption of the circuit as well. Power consumption of circuit dedicated for BLE applications must be less.

3.1 LNA WITH L-MATCHING AT INPUT AND RLC AS LOAD

First circuit design simulated used an inductor to provide input matching and used a RLC network at the output matching network. Inductor along-with the capacitance of the MOS including pad capacitance resonates at the required frequency and provides input matching of 50Ω. Inductor at the output of the network resonates with the capacitor connected in the network and the capacitor connected at the load of the circuit. This network is connected to provide matching at the output of the circuit at 2.4 GHz. Circuit is operated on a supply voltage of 1V. MOS is operated on saturation region.

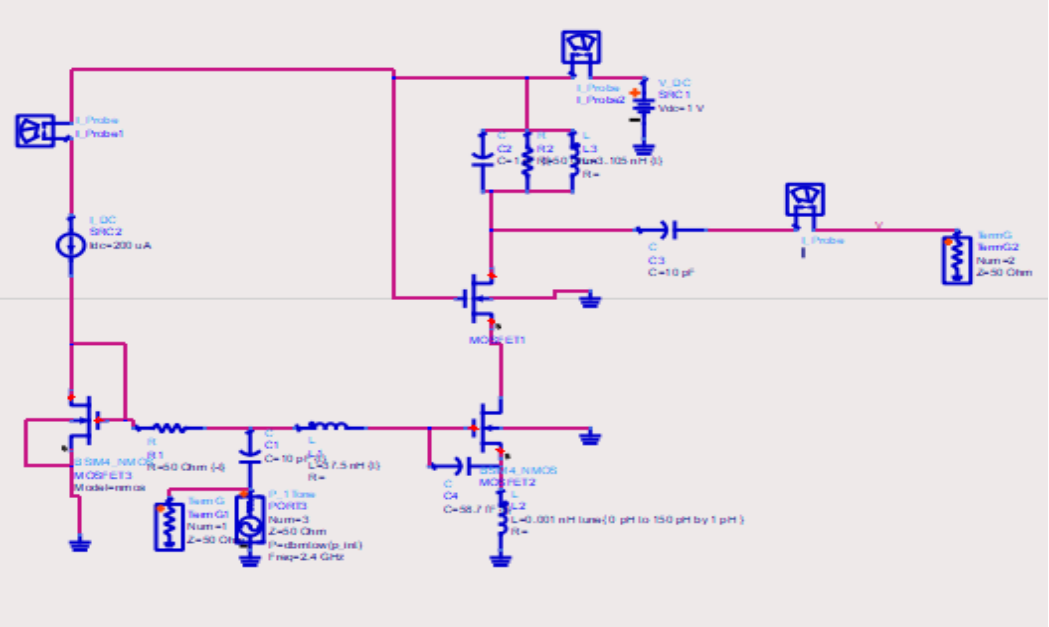

Fig. 3.1 Schematic of LNA (Circuit 1) implemented in ADS

We proceed with placing the circuit components and then perform simulation to obtain the results. BSIM4 Model of MOS is used with the required value of the width and the length set using edit component parameters option in ADS. After placing all the circuit components we need to perform S-parameter simulation because the circuit is operating at high frequency and at higher frequencies circuit performance is analyzed by S-parameters. S_{11} gives a measure of the input return loss of the circuit i.e. input matching of the circuit and S_{22} gives a measure of the output matching of the circuit. S_{21} provides the gain performance of the circuit and S_{12} provides the value of the reverse gain of the circuit. While performing S parameter simulation we need to specify the frequency of simulation

and also the intervals after which the simulation is to be performed.

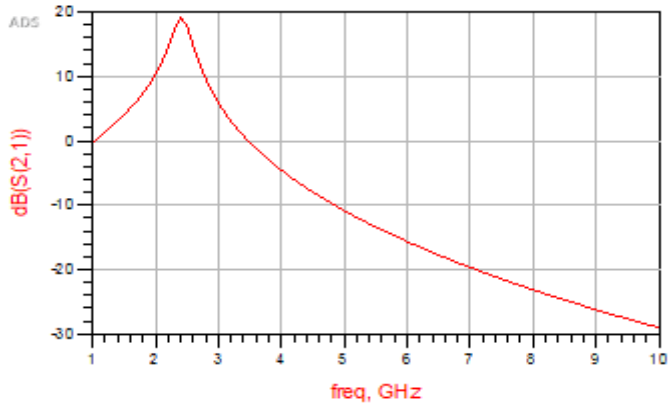

Fig. 3.2 S_{21} (Gain) of LNA (Circuit 1)

LNA offered a gain of around 20 dB at the required frequency which is a very good value in Bluetooth applications. Hence this circuit provided a performance in terms of parameter S_{21} i.e. the gain of the circuit was high. The above gain was observed at a frequency of 2.4 GHz which made this circuit suitable for Bluetooth applications as the operating frequency of Bluetooth and BLE is 2.4 GHz. Next parameter to be analyzed is the input return loss of the circuit i.e. S_{11}. Value of input return loss should be as low as possible as it is a measure of reflections occurring the circuit. The signals which are reflected back by the circuit should be attenuated or the amount of signals reflected should be less. Ideally zero reflections should occur but it is not possible to achieve zero reflections in practical circuits.

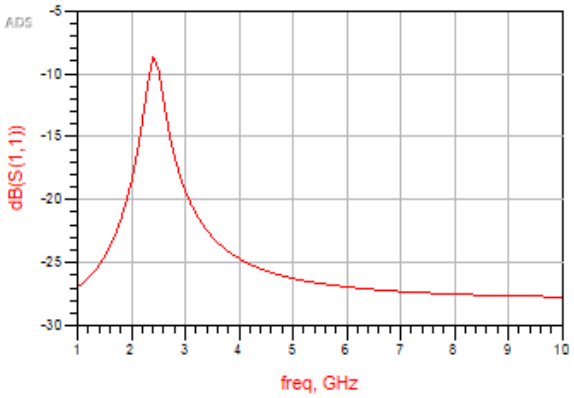

Fig. 3.3 S_{11} (Input Return Loss) of LNA (Circuit 1)

At the frequency of interest i.e. 2.4 GHz we observe that the S_{11} of the circuit is -9 dB which indicates poor input matching. Moreover the value of S_{11} at other frequencies was better than the desired frequency which indicates that the matching network in circuit 1 is not properly designed to provide proper input matching at the desired frequency. This

effect may arise because of the presence of spurious capacitances in the circuit which may affect the matching network of the circuit. Next parameter to be analyzed is the reverse gain or the attenuation of the circuit. S_{12} gives a measure of attenuation suffered by the signals which are reflected from the output port to the input port. This parameter should also be lowest as possible i.e. the attenuation suffered by the backward propagating signals should be more.

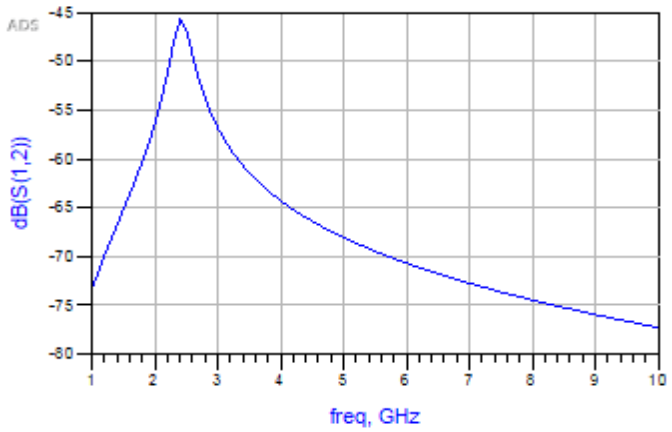

Fig. 3.4 S_{12}(Reverse Gain) of the LNA (Circuit 1)

From the curves obtained by simulations we observe that the reverse gain of the circuit at desired frequency is -44 dB which is an acceptable value and considered as a good value of this parameter. This indicates that the signals which tend to propagate in backward directions suffer huge loss and are attenuated by a significant amount. Next parameter to be studied is S_{22} which gives a measure of output matching provided by the network used at load. S_{22} is known as output reflection coefficient i.e. power reflected at port 2 when power is incident at port 2. Value of output reflection coefficient at 2.4 GHz should be the best value of the circuit if the output matching network is properly designed to work at 2.4 GHz. From the curve obtained for S_{22} after simulation we observe that the output matching of the circuit is properly designed to be operated at 2.4 GHz and the circuit's output reflection coefficient is -29 dB at the frequency of interest. Curve obtained after simulations indicate that the output port is perfectly matched to the 50Ω termination provided at the output terminals of the circuit. From the S_{22} we also observe that the best value of the parameter is obtained at the frequency of interest i.e. 2.4 GHz.

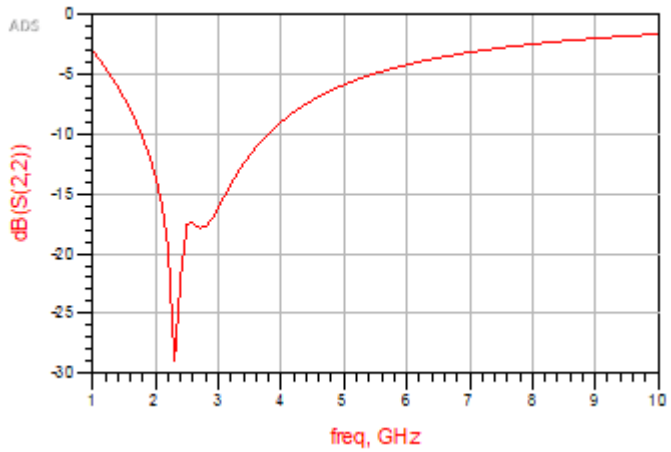

Fig. 3.5 S_{22} (Output Reflection Coefficient) of LNA (Circuit 1)

From S-parameter simulation we can also obtain the value of the Noise Figure of the circuit by making certain modification in the simulation settings. Before simulations we need to provide the input and output port for noise calculations. Noise input port is the port at which the source is placed in simulations i.e. input port is port 1 and output port is port 2. From the curve obtained for Noise Figure we can obtain the value of Noise Figure of the circuit at the particular frequency.

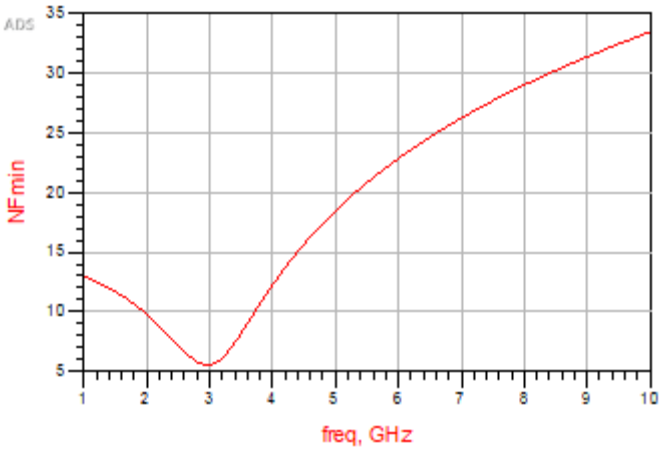

Fig. 3.6 NF (Noise Figure) of LNA (Circuit 1)

From the curve obtained after simulations we found the value of NF to be 4 dB which is a very high value if performance standards of LNA are considered. Noise performance of this circuit is very poor and modifications are required to be made in order to improve the noise performance of the circuit.

After S-parameter simulation we should also analyze the linearity of the circuit which is given by the value of Input Third Order Intercept (IIP3). IIP3 value of a circuit can be calculated by plotting the first and the third order harmonics. These curves are obtained by performing harmonic simulation of the circuit. To perform the harmonic simulation of

the circuit we need to provide two input signals to the circuit both having different frequency and the frequency should be chosen such that the interferer falls in the required channel so that we can study the effect of the interferer on the required channel.

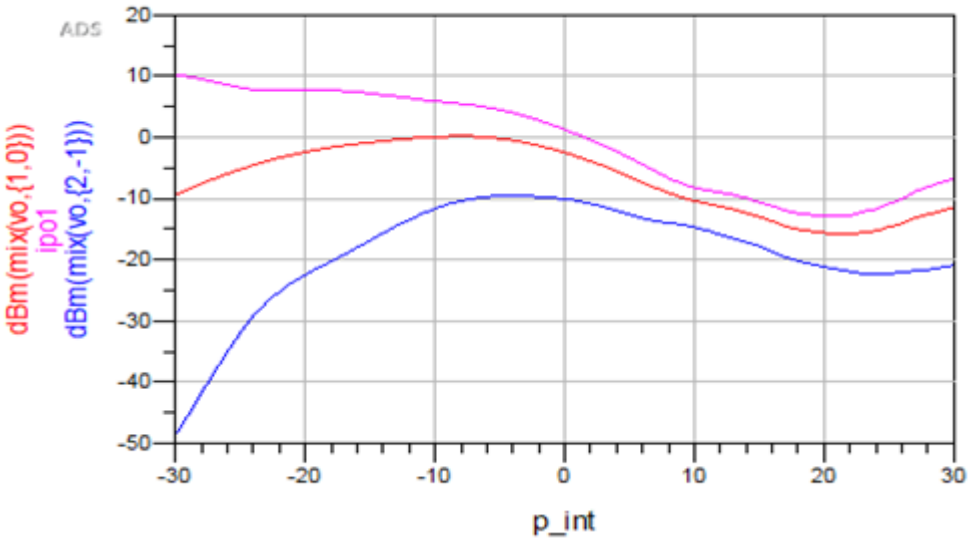

Fig. 3.7 Fundamental Harmonic and Third order harmonic curves for LNA (Circuit 1)

To obtain the curves for calculations of IIP3 value two tone test is used in ADS and Harmonic Balance Simulation is performed. Ideally the curves obtained for the harmonics should be a straight line but due to non-linearity the curve obtained is not a straight line.

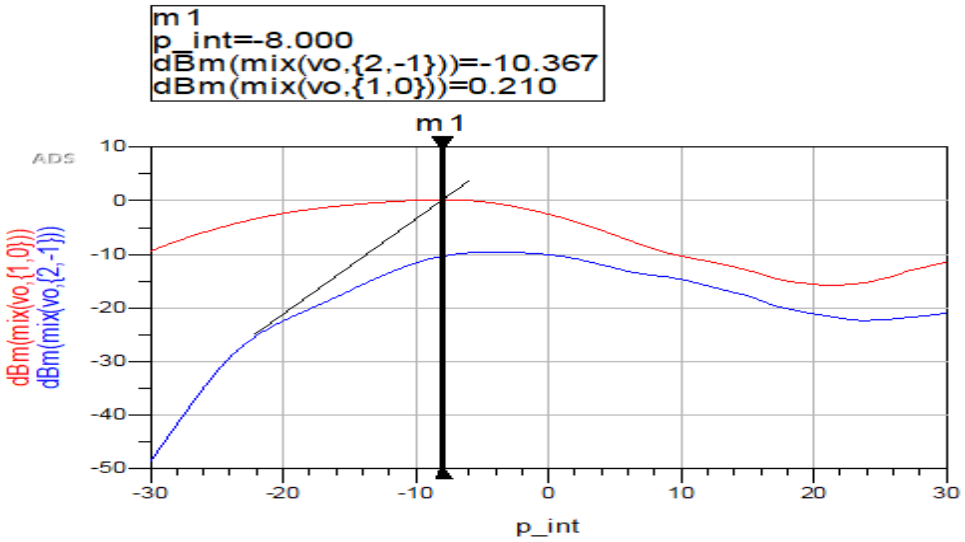

Fig. 3.8 Calculation of IIP3 for LNA(Circuit 1)

To calculate the value of the IIP3 we extend the curve in a linear manner and the curve is extended to intersect the fundamental harmonic curve. The point at which the curve intersects gives the value of IIP3 and it can be calculated as the input power at this point of intersection. IIP3 value of this circuit is found to be -8dBm which is not dependent on

frequency. This value indicates that the circuit has a high linearity and is in accordance to the standards of LNA.

One of the most important parameter when applications of LNA in Bluetooth and BLE are considered is the power consumed by the device. Power consumption of the device should be very less if it is to be utilised in Bluetooth and BLE applications.

Table 2. Parameter values (Circuit 1)

Parameter	Value
S_{11}(dB)	-9
S_{12}(dB)	-44
S_{21}(dB)	20
S_{22}(dB)	-29
NF_{min}	4
IIP3(dBm)	-8
Power Consumption(mW)	12.33

3.2 LNA WITH L-MATCHING AND R AS LOAD

Next design considered by us is the L-matching at the input and resistance is used as load at the output. Resistive load offers less gain and also it does not provide proper matching which at higher frequency creates a hindrance to the proper functioning of the circuit. This observation is made according to theoretical computations and hence we observe the results obtained after simulations and justify the fact after analyzing the results obtained by simulations.

This configuration offered a gain of 17 dB at the frequency 2.4 GHz which is a good value but other configurations ought to offer more gain than this configuration which uses resistance as a load. However circuit offered a gain which is sufficient enough for short-range communication. The gain curve of this configuration is given below and the value of S_{21} can be found out for other frequencies as well but maximum gain of the circuit occurs at 2.4 GHz only.

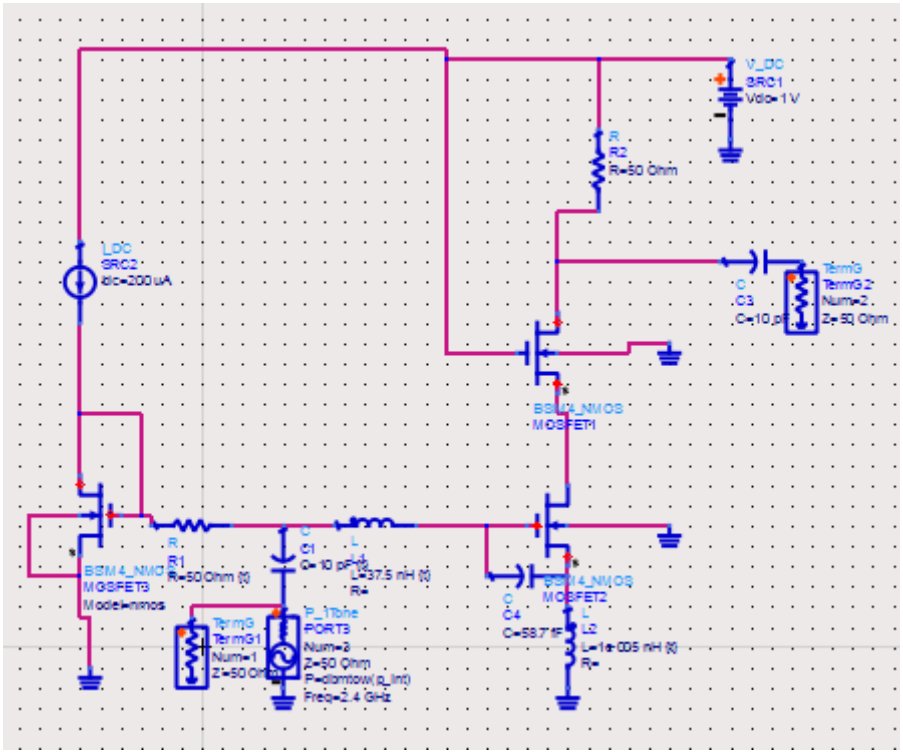

Fig. 3.9 Schematic of LNA (Circuit 2)

Curve obtained for S_{11} parameter of the configuration gives the value of input return loss of the circuit. Input return loss is given by the ratio of power reflected from port 1 to the power incident at the port 1 i.e. gives a measure of mismatch of impedances between the two stages. Using R as load in the configuration restricts the operation of

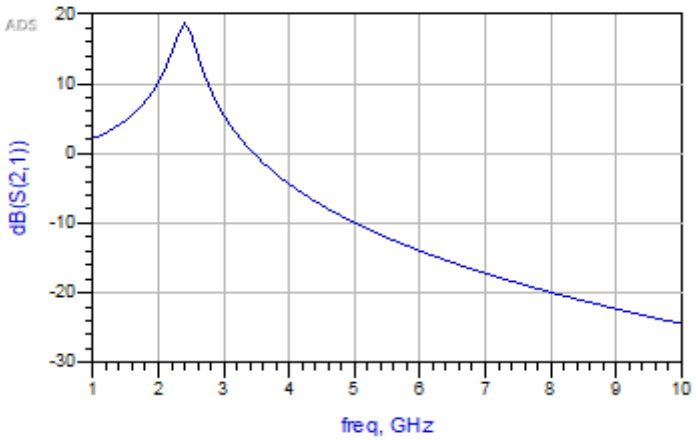

Fig. 3.10 S_{21}(Gain) of the LNA (Circuit 2)

the device at higher frequencies and does not provide good matching at the port. Value of input return loss at the desired frequency is found to be -8 dB which indicates that matching is not efficient enough to prevent reflections.

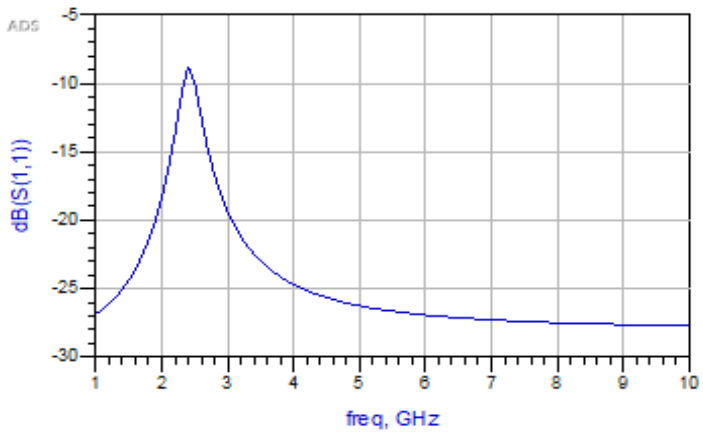

Fig. 3.11 S_{11}(Input Return Loss) of the LNA (Circuit 2)

S_{12}(Reverse gain) gives the measure of attenuation suffered by signals travelling from the output port to the input port. Signals propagating backwards should be heavily attenuated to prevent destruction of the circuit components. This circuit had a S_{12} value of -46 dB at the required frequency. However circuit heavily attenuated the signals at other frequencies of operation also.

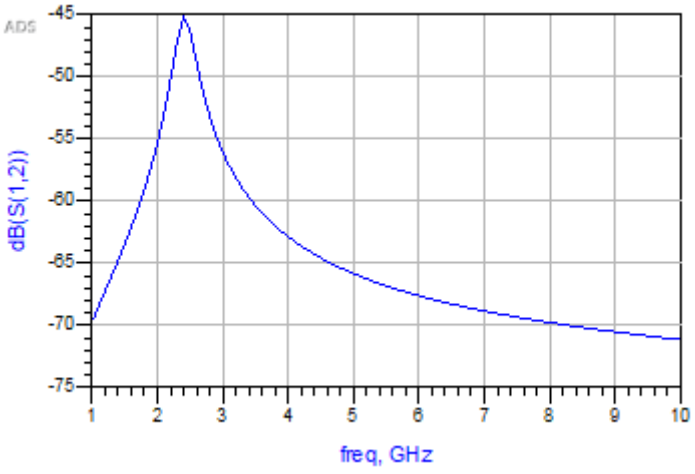

Fig. 3.12 S_{12}(Reverse Gain) of the LNA (Circuit 2)

Similar to the input matching, output matching network is also used to provide matching at the output terminals of the circuit. S_{22} which is the output reflection

coeffficient gives a measure of the output matching . Value of S_{22} for this configuration is found to be -11 dB at the frequency of interest.

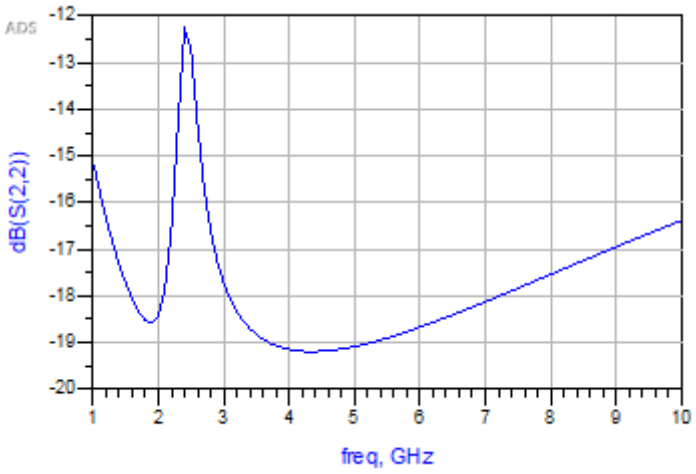

Fig. 3.13 S_{22}(Output Reflection Coefficient) of the LNA (Circuit 2)

Noise Figure of the circuit is also measured using S-parameter simulation and the curve obtained gives the value of the Noise Figure of the circuit at all frequencies of simulations. NF for this configuration is meassured to be 3.7 dB at the frequency of interest.

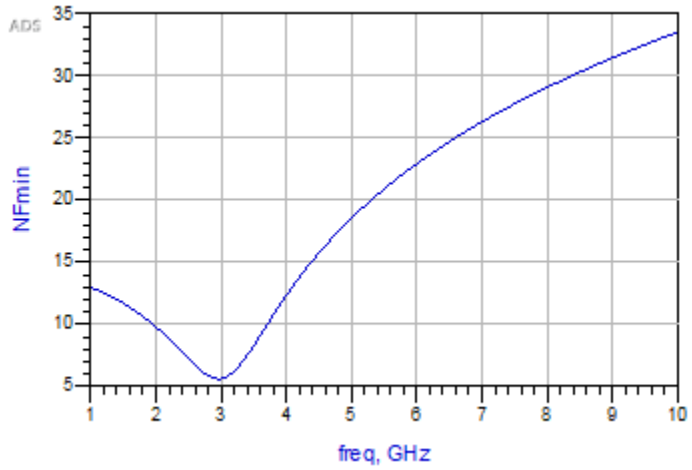

Fig. 3.14 NF_{min} of the LNA (Circuit 2)

If we try to imporve the noise performance of the circuit we observe that the gain of the circuits gets compressed and desired operation is not achieved at the frequency of interest. NF of the circuit can be improved using additional measures can be taken to reduce the effect of noise. These additional techniques were studied in literature survey

as well and further new techniques can also be utilised in present circuit to enhance the noise performance further.

As discussed before non-linearity in a system is not desirable as it creates a restriction to proper operation of circuit. Extent of non-linearity can be measured by obtaining the fundamental harmonic and other harmonics curves and obtain the required values. From the curve obtained above we can calculate the IIP3 of this circuit. By using the similar procedure we obtain the value of IIP3 of the circuit to be -7 dBm which is acceptable value of IIP3 and indicates a high-linearity circuit.

Similar to procedure used in previous IIP3 calculations we extend the curve in a linear manner by extending the curve with a straight line to obtain the point for IIP3 calculations.

Summarizing the results together helps us to identify the positive aspects of our design as well as the drawbacks of our design that are to be corrected in future designs. Results obtained from the simulations for this circuit are listed in tabular form in Table 3.

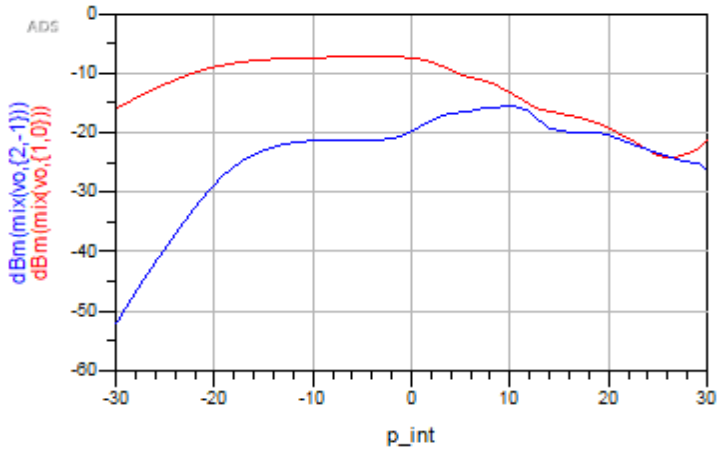

Fig. 3.15 Fundamental Harmonic and Third order harmonic curves for LNA (Circuit 2)

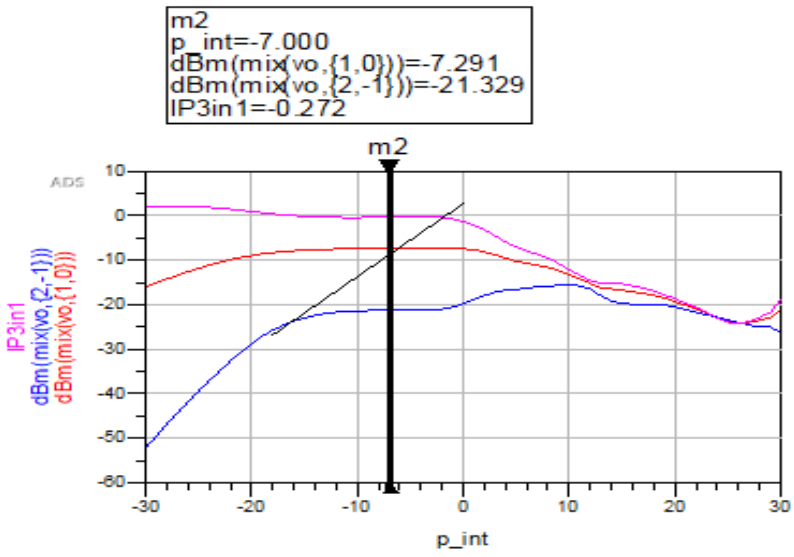

Fig. 3.16 Calculation of IIP3 (Circuit 2)

Table 3. Parameter values (Circuit 2)

Parameter	Value
S_{11}(dB)	-8
S_{12}(dB)	-45
S_{21}(dB)	17
S_{22}(dB)	-11
NF_{min}	3.7
IIP3(dBm)	-7
Power Consumption(mW)	11.45

3.3 LNA WITH L-MATCHING AND TANK CIRCUIT AS LOAD

Next circuit design considered by us used the same cascode configuration with input matching using an inductor and capacitor and the load used in the circuit was a tank circuit. Ideally inductor should suffer zero losses but it is not so in practical circuits and inductor losses have to be modelled using a resistance. Load considered in this circuit does not include the effect of inductor losses and considers the inductor to be an ideal one and hence no resistance is being included in the circuit to model the loss. Other specifications remain the same as above circuits.

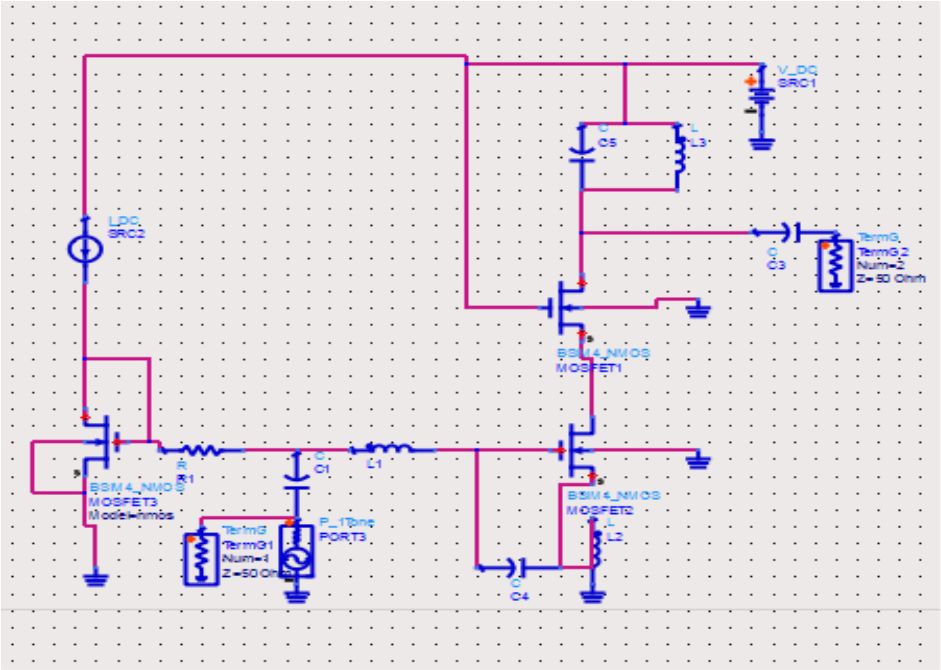

Fig. 3.17 Schematic of LNA (Circuit 3)

Schematic of the circuit implemented is shown above in the Fig. After S-parameter simulation we obtain the required curves for the circuit. First we study the gain provided by this circuit which is the parameter considered by us for optimisation because trade-off exists between the parameters of LNA. If we try to optimise one parameter other parameters get degraded. From the curve obtained for S_{21} we found the value of gain to be 28 dB at the desired frequency which is considered as an impressive value of gain if Bluetooth and BLE applications are considered.

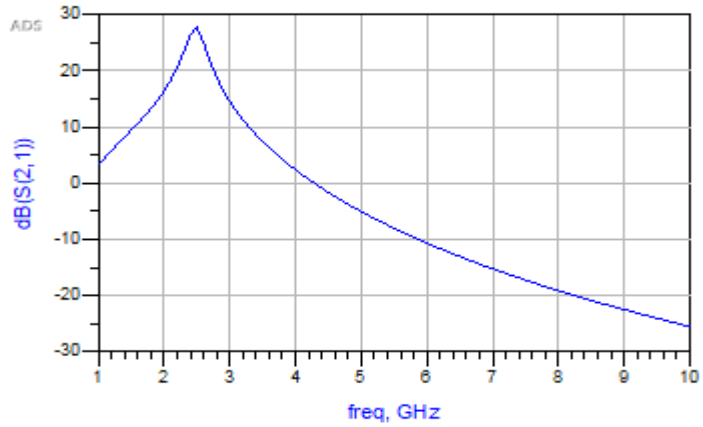

Fig. 3.18 S_{21}(Gain) of the LNA (Circuit 3)

Next we measure the performance of the input matching circuit which can be measured by the S-parameter S_{11} which gives the input return loss of a circuit and should be as low as possible for a circuit with good input matching network. From the curve obtained fo S_{11} we obtain the value of S_{11} at the operating frequency is -3dB which indicates a very poor matching. This parameter indicates that the input matching used in this configuration is not suitable to be used for

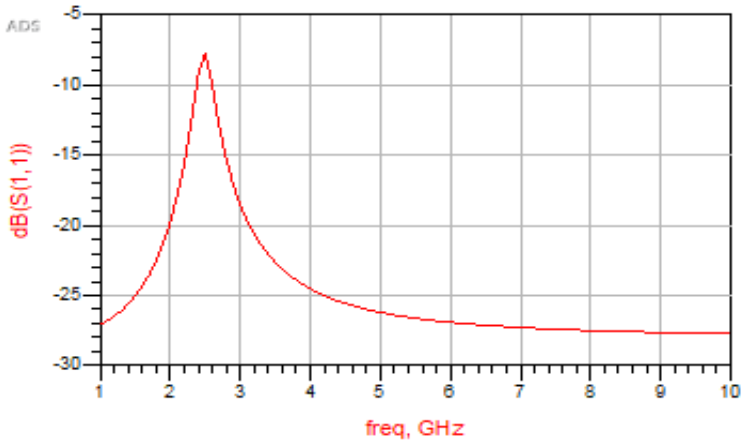

Fig. 3.19 S_{11}(Input Return Loss) of the LNA (Circuit 3)

used for implementing LNA as the results indicate that the input mtaching network is not efficient enough to provide a good matching at the operating frequency.

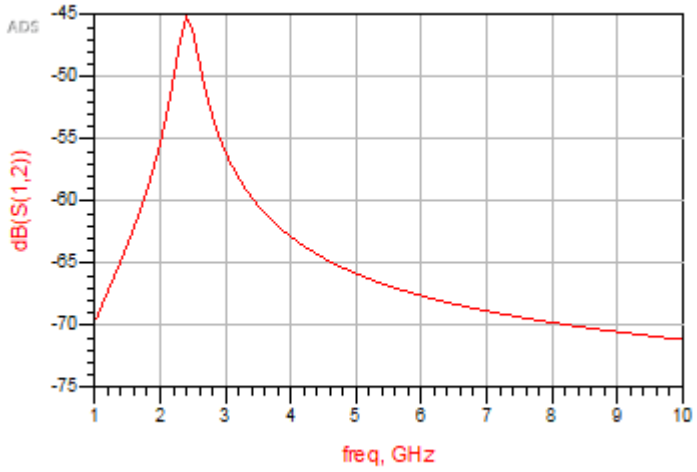

Fig. 3.20 S_{12}(Reverse Gain) of the LNA (Circuit 3)

Reverse gain or the attenuation offered by the circuit to backward propogating signals was found to be -43 dB which is as sufficient amount of attenaution for a LNA and is adhering to the standards of LNA. Output reflection coefficient of the LNA gives a measure of the output matching of the LNA and indicates the amount of power reflected back from output port of the circuit when power is incident at port 2.

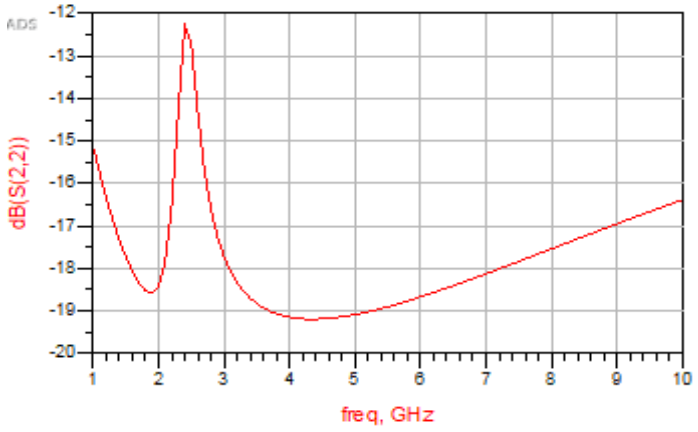

Fig. 3.21 S_{22}(Ouput reflection Coefficient) of the LNA (Circuit 3)

Output Reflection Coefficient of the LNA was found to be -4dB which is not a good observation as far as output matching is considered. It indicates that the output matching networks efficieny is very less and it is not able to provide proper output matching.

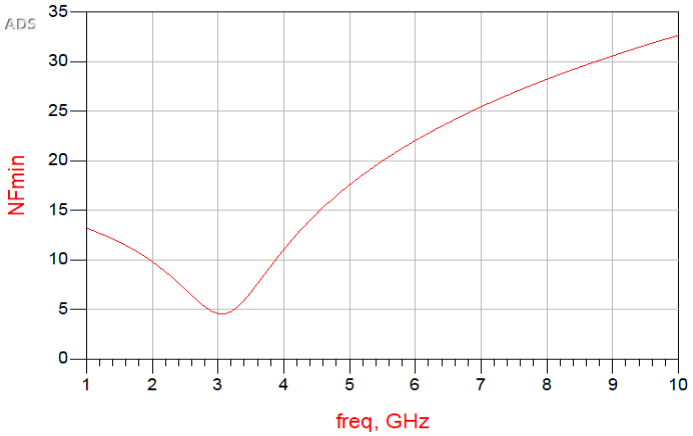

Fig. 3.22 NF_{min} of the LNA(Circuit 3)

Noise Figure of the circuit is also measured using S-parameter simulation and the curve obtained gives the value of the Noise Figure of the circuit at all frequencies of

simulations. NF for this configuration is meassured to be 3.7 dB at the frequency of interest.

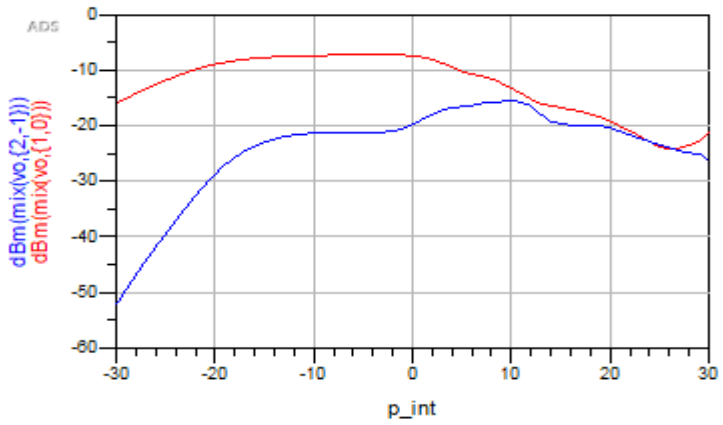

Fig. 3.23 Fundamental Harmonic and Third order harmonic curves for LNA (Circuit 3)

Next parameter to be considered is the IIP3 vlaue of the circuit which from observations is found to be -7 dBm which indicates a high-linearity circuit according to the standards set for a LNA.

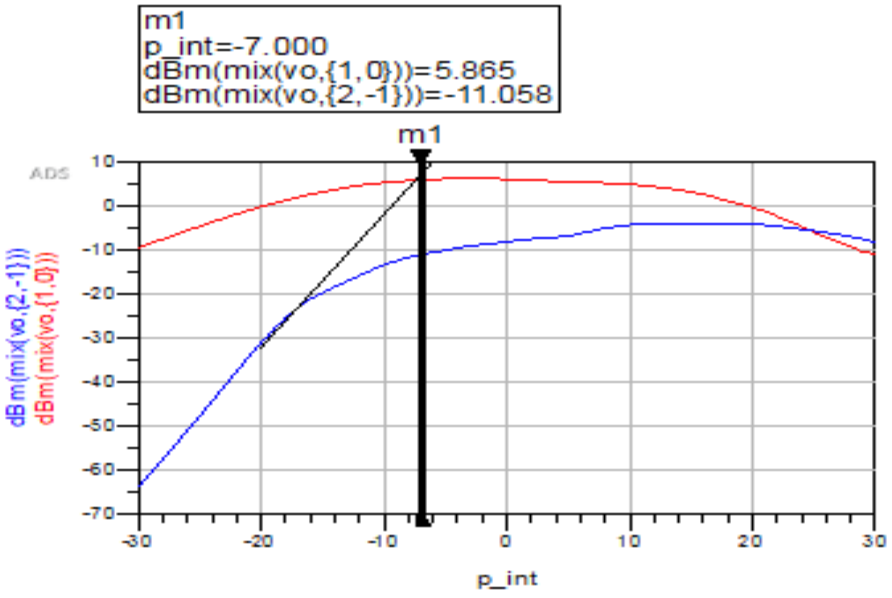

Fig. 3.24 Calculating IIP3 of LNA (Circuit 3)

Results obtained for this design are summarized in a tabular form given below.

Table 4. Parameter values (Circuit 3)

Parameter	Value
S_{11}(dB)	-3
S_{12}(dB)	-43
S_{21}(dB)	28
S_{22}(dB)	-4
NF_{min}	3.7
IIP3(dBm)	-7
Power Consumption(mW)	11.45

3.4 LNA WITH L-MATCHING AND INDUCTOR AS LOAD

Next design considered by us is the circuit which utilises the cascode configuration with L-matching at the input and uses an inductor as a load. Using inductor as load helps to achieve output matching by resonating with the capacitor connected at the load at the operating frequency. Efficiency of this circuit design can be analyzed by studying the simulation results obtained after S-parameter simulation and harmonic balance simulation.

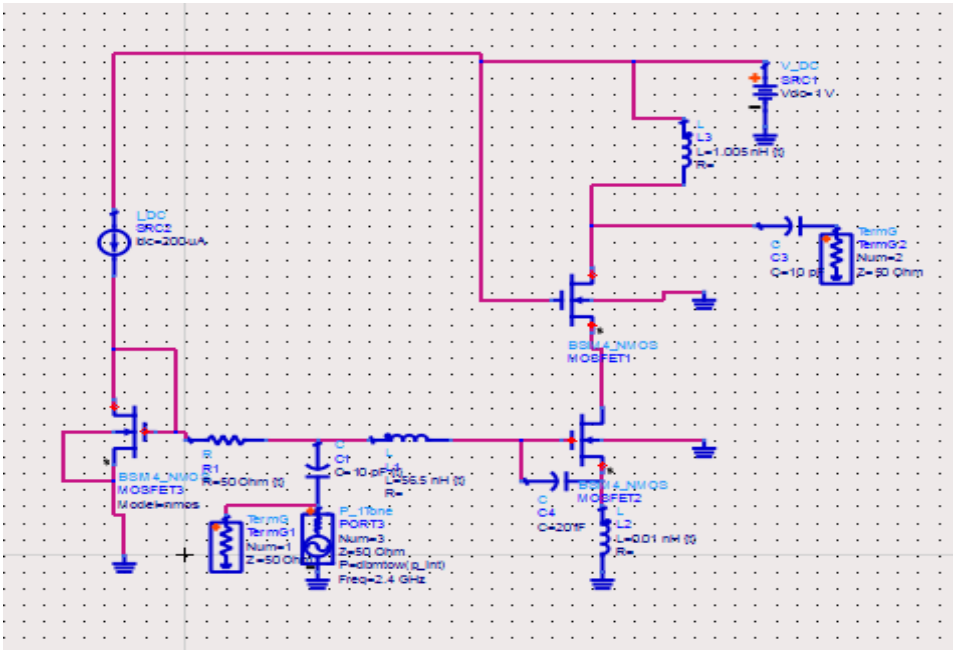

Fig. 3.25 Schematic of LNA (Circuit 4)

Schematic of LNA implemented is shown above. Gain offered by circuit is found to be 22 dB at the operating frequency 2.4 GHz and is well within the acceptable limits .Gain curve of the LNA is shown below :

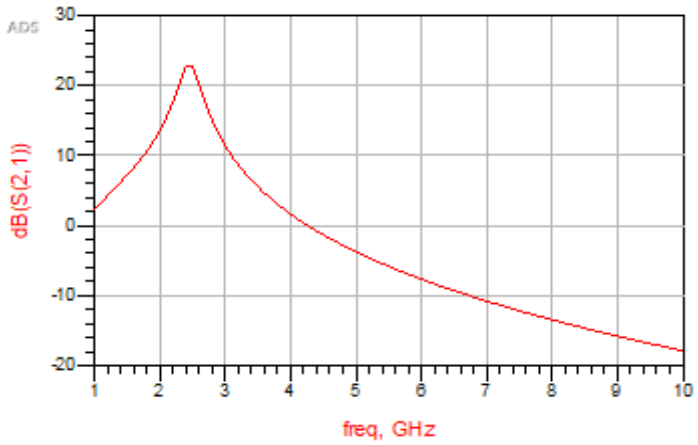

Fig. 3.26 S_{21}(Gain) of the LNA (Circuit 4)

Next parameter to be studied is the input return loss i.e. S_{11} of the LNA which is an indicator of the input mismatch of the circuit. S_{11} of his circuit is found to be -12 dB at the operating frequency. Input return loss of this circuit is indicating that the matching network is able to provide better performance in this configuration. S_{11} curve for this circuit is given below:

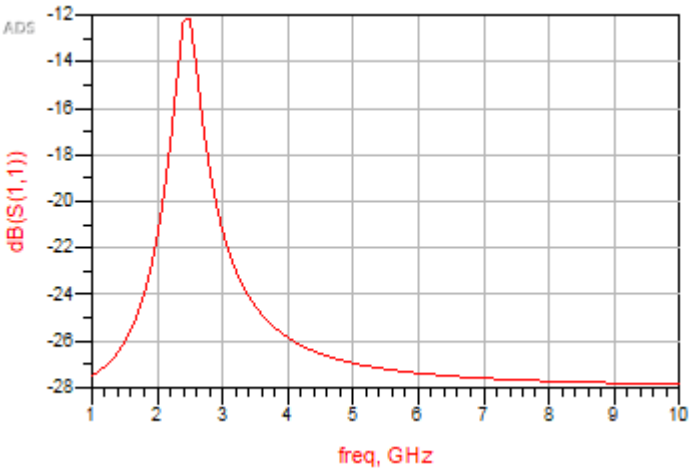

Fig. 3.27 S_{11}(Input Return Loss) of the LNA (Circuit 4)

Next parameter to be measured is the reverse gain of this circuit which is found to be -43 dB for this circuit and is close to the reverse gain of the previously studied circuits.

Fig. 3.28 S_{12}(Reverse Gain) of the LNA (Circuit 4)

After the reverse gain we study the results obtained for parameter S_{22} i.e. the output reflection coefficient of the circuit. Output reflection coefficient results obtained for this circuit indicate that the output matching used in this circuit delivers a very poor performance and the value of the parameter S_{22} at the frequency of operation is found to be -0.5 dB which indicates poor performance by the output matching network. Curve obtained for Output Reflection Coefficient is given below :

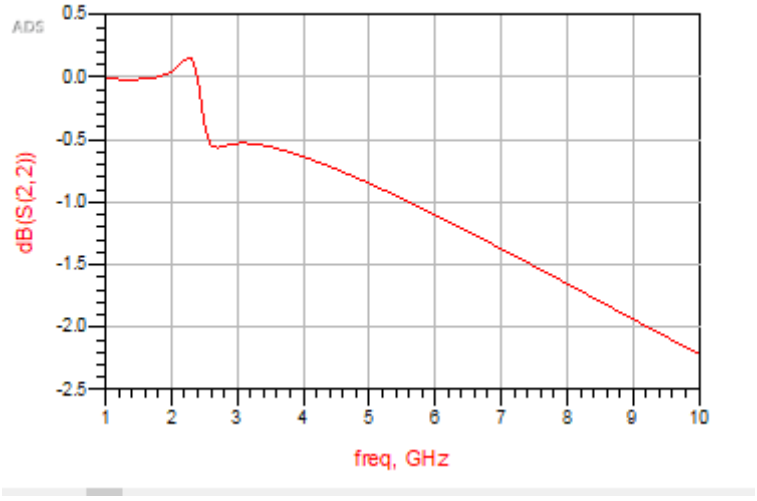

Fig. 3.29 S_{22}(Output Reflection Coefficient) of the LNA(Circuit 4)

Next parameter is the Noise Figure of the circuit which is found to be 6 dB at the operating frequency which indicates very poor noise performance and also indicate that this circuit is not suitable to be used as an LNA as it is not able to provide desired noise

performance. NF value of the circuit is not within the acceptable limits. Curve obtained for NF_{min} of this circuit is given below:

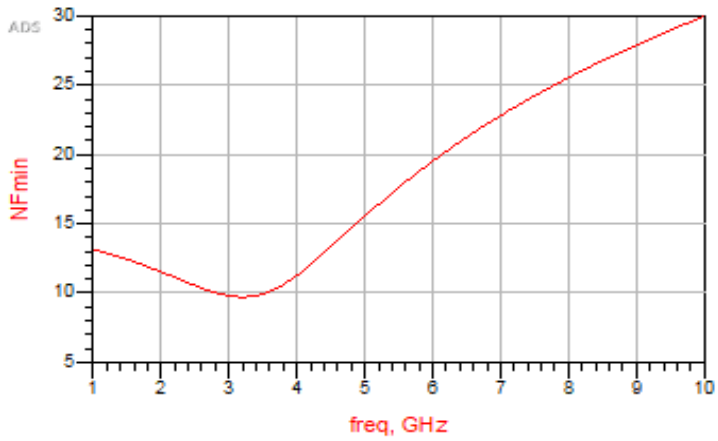

Fig. 3.30 NF_{min} of the LNA(Circuit 4)

After analyzing the results obtained from S-parameter simulations we need to perform Harmonic Balance simulation of the circuit and obtain the curves for IIP3 calculation s using two- tone test in ADS. The curves obtained for IIP3 calculations are given below:

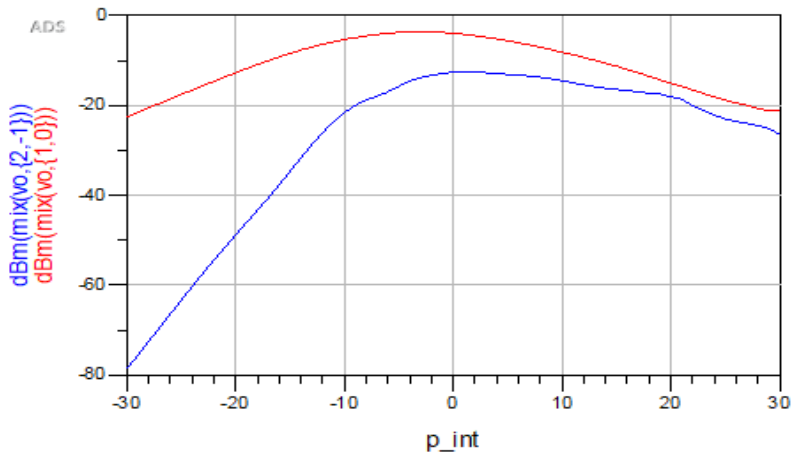

Fig. 3.31 Fundamental Harmonic and Third order harmonic curves for LNA (Circuit 4)

Value of IIP3 obtained from the curve is -4 dBm which indicates a highly-linear circuit and the value of IIP3 is within the acceptable standards of LNA. Calculations of IIP3 from the curves obtained is shown below in the Fig.. Results obtained after the simulations are represented in tabular form in the below table which makes it easire to compare the performance of the circuit in terms of different parameters.

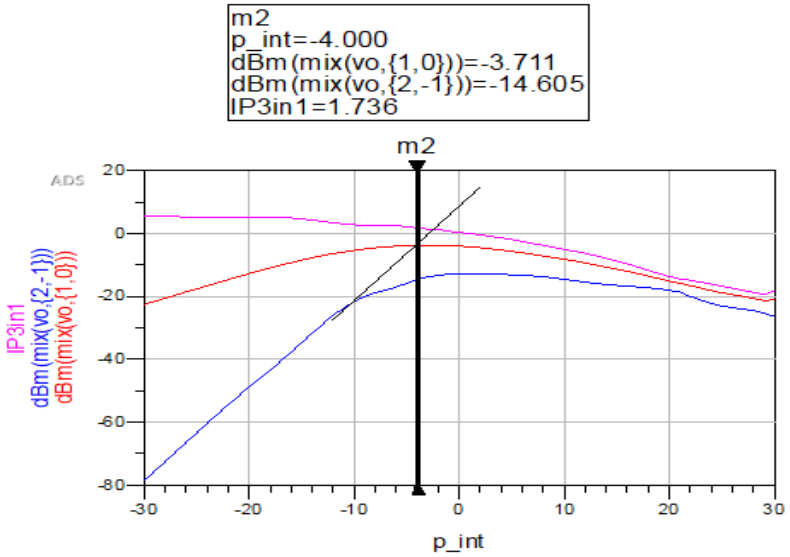

Fig. 3.32 IIP3 of the LNA(Circuit 4)

Table 5. Parameter values (Circuit 4)

Parameter	Value
S_{11}(dB)	-12
S_{21}(dB)	22
S_{12}(dB)	-43
S_{22}(dB)	-0.5
NF_{min}	6
IIP3(dBm)	-4
Power Consumption(mW)	10.31

3.5 LNA WITH LC AS LOAD AND T- MATCHING

From the circuit designs simulated above we observe the best gain obtained for the circuit using tank circuit as load and we also observe that the matching network used at the input of the circuit was not efficient enough to provide good performance in terms of input matching which could be seen from the results obtained by simulations as well.

We try to improve the matching network of the circuit by changes the components topology and the design of the matching network as well which may provide an improved performance than the previously simulated circuits.

Next design considered by us utilises cascode configuration and a tank circuit as a load. The matching network used in the design is connected in T configuration and is designed using a synthesis tool in ADS which is used to design circuits for impedance matching. Tool matches the source impedance to the load impedance by creating a matching network using passive as well as active elements which depends on type of impedances to be matched. Out f all available matching networks T-matching is used to obtain impedance matching.

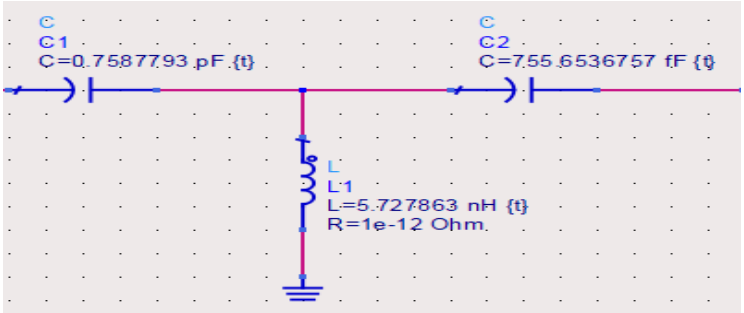

Fig. 3.33 Matching Network for the LNA (Circuit 5)

Network given in Fig. above is used for impedance matching and it can be seen that only active elements are used to achieve impedance matching. Value of components being used is decided by the appropriate calculations used for transforming source to load impedance and using synthesis tool available in ADS.

Above Fig. shows the schematic of LNA implemented with matching network same as discussed above. From S-parameter simulations we obtain the results for the parameters required to analyze the performance of LNA. First parameter to be analyzed is the gain offered by the circuit that is given by the parameter S_{21}. Curve obtained for the gain of the circuit is given below:

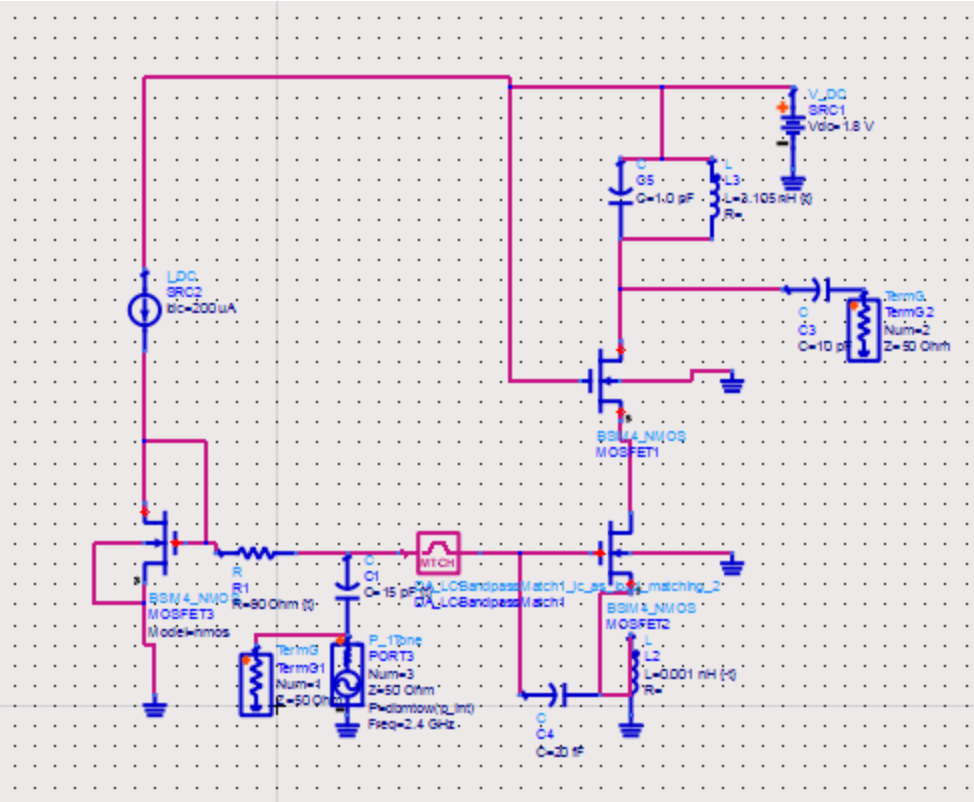

Fig. 3.34 Schematic of LNA implemented (Circuit 5)

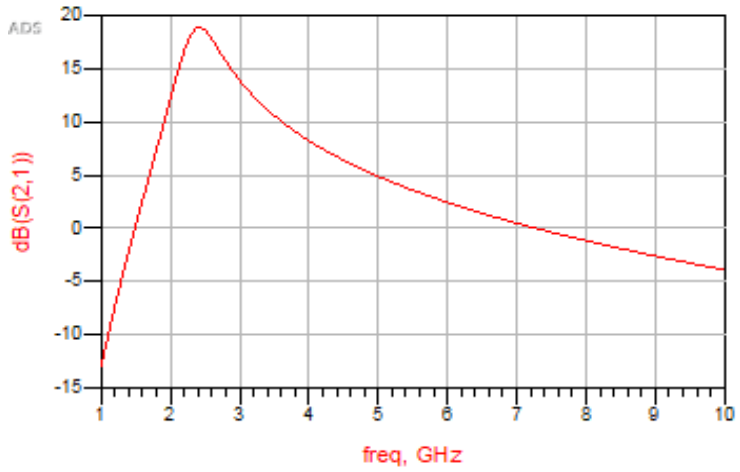

Fig. 3.35 S_{21}(Gain) of the LNA (Circuit 4)

From the curve obtained for gain of the amplifier value of gain is found to be 19 dB at the operating frequency. Next parameter to be analyzed is the Input Return Loss of the circuit which is found to be -1dB at the operating frequency and is a very poor performance in terms of input matching circuit used.

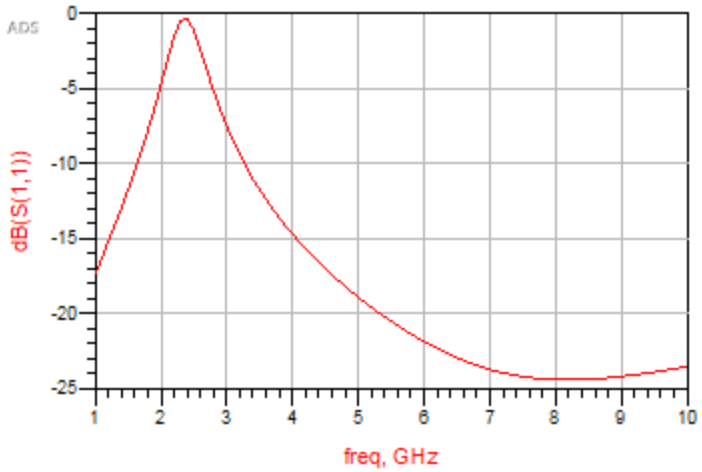

Fig. 3.36 S_{11}(Input Return Loss) of the LNA (Circuit 5)

Next parameter is the reverse gain offered by the circuit which is found to be -53 dB which is a very good value of attenuation offered by the LNA. Curve obtained for S_{12} is given below:

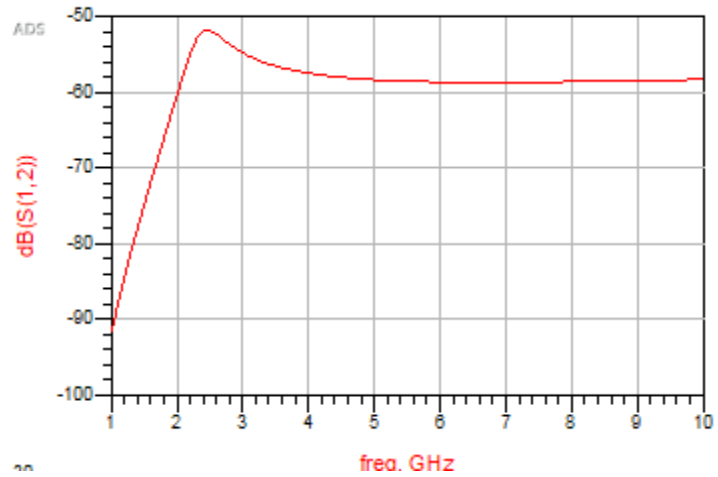

Fig. 3.37 S_{12}(Reverse Gain) of the LNA(Circuit 5)

A good value of reverse gain also indicates good isolation between the output and the input port of the circuit which is desirable for proper circuit operation. Next parameter to be studied is the output reflection coefficient of the circuit which is obtained from the curve of S_{22}. Curve obtained for output reflection coefficient indicates that the matching at the output is perfect at the required frequency. However the value of the parameter is not good enough. S_{22} obtained from the curve is -1.48 dB at the operating frequency of 2.4 GHz.

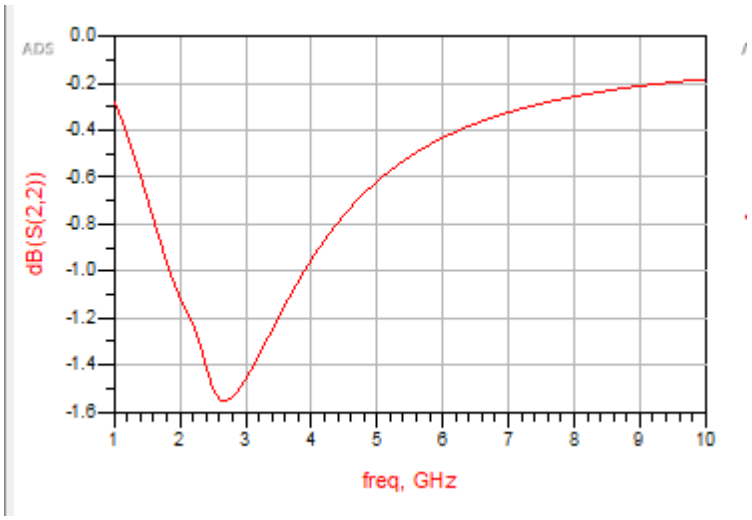

Fig. 3.38 S_{22}(Output Reflection Coefficient) of the LNA (Circuit 5)

Noise figure of the LNA implemented above was observed to be within the acceptable standards of a LNA circuit and was found to be 2.8 dB at the operating frequency. Curve obtained for the Noise Figure of the circuit is given below:

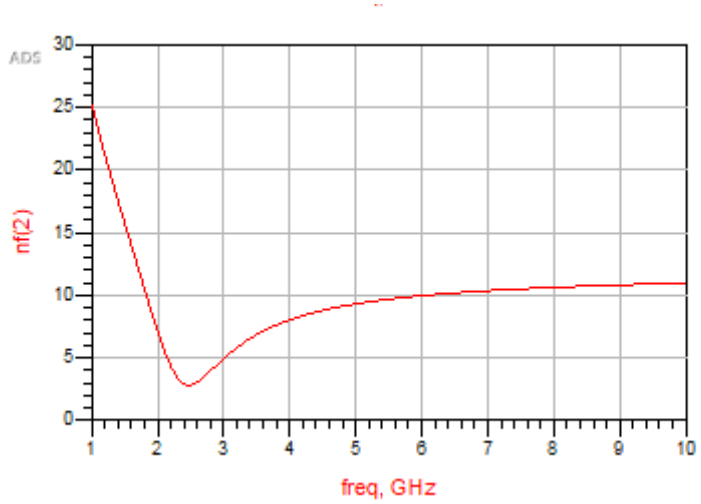

Fig. 3.39 NF of the LNA (Circuit 5)

After analyzing the results obtained from the S-parameter simulation we proceed to Harmonic Balance simulation of the circuit to analyze the linearity of the circuit. After HB simulation of the circuit the curves obtained for IIP3 calculations are shown below:

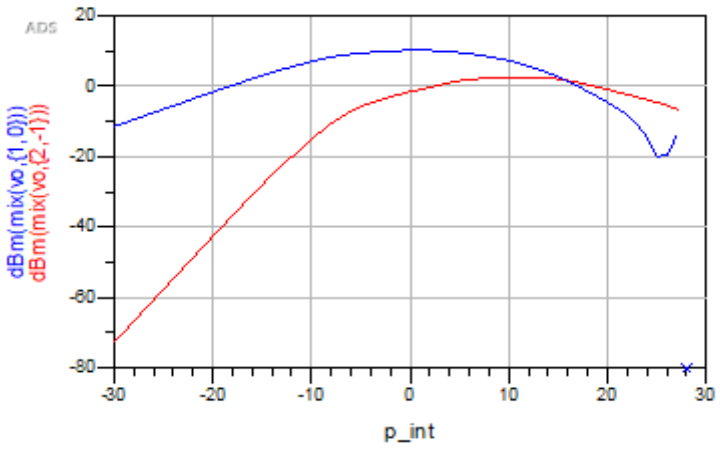

Fig. 3.40 Fundamental Harmonic and Third order harmonic curves for LNA (Circuit 5)

From the curves obtained above IIP3 value can be obtained for the circuit and it is found to be -2 dBm which shows an improved linearity from the previously analyzed circuits. Value of IIP3 was calculated from the curve as shown below:

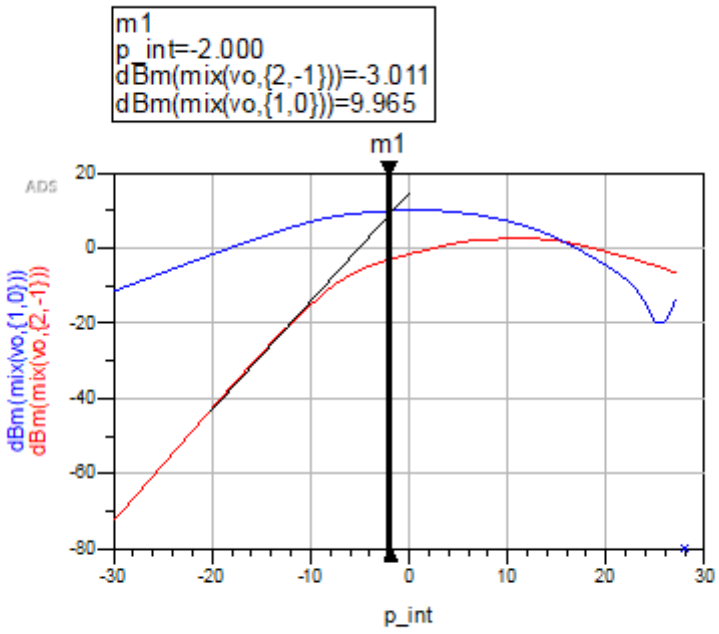

Fig. 3.41 IIP3 of the LNA (Circuit 5)

Results obtained are summarized in tabular form and are listed below:

Table 6. Parameter values (Circuit 5)

Parameter	Value
S_{11}(dB)	19
S_{12}(dB)	-1
S_{21}(dB)	-53
S_{22}(dB)	-1.48
NF_{min}(dB)	2.8
IIP3(dBm)	-2.00
Power Consumption(mW)	10.91

3.6 LNA WITH NEW MATCHING NETWORK AND TANK CIRCUIT AS LOAD

Next circuit analyzed is LNA which is in cascode configuration and uses a new matching network designed by us as the input matching network and a tank circuit as the load. The inductor connected at the load resonates with the capacitor connected to improve the output matching of the circuit. Matching network is designed using a tool used for impedance matching. Matching network used two capacitors and one inductor connected in the configuration as shown below to provide impedance matching.

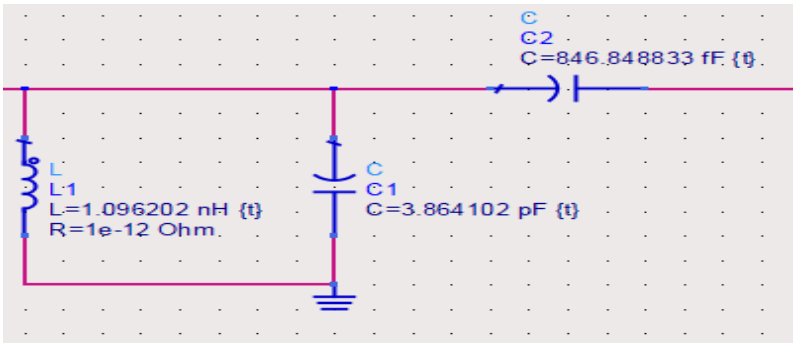

Fig. 3.42 New Matching Circuit used in LNA (Circuit 6)

Schematic of the LNA which uses the new matching network implemented in ADS is shown below:

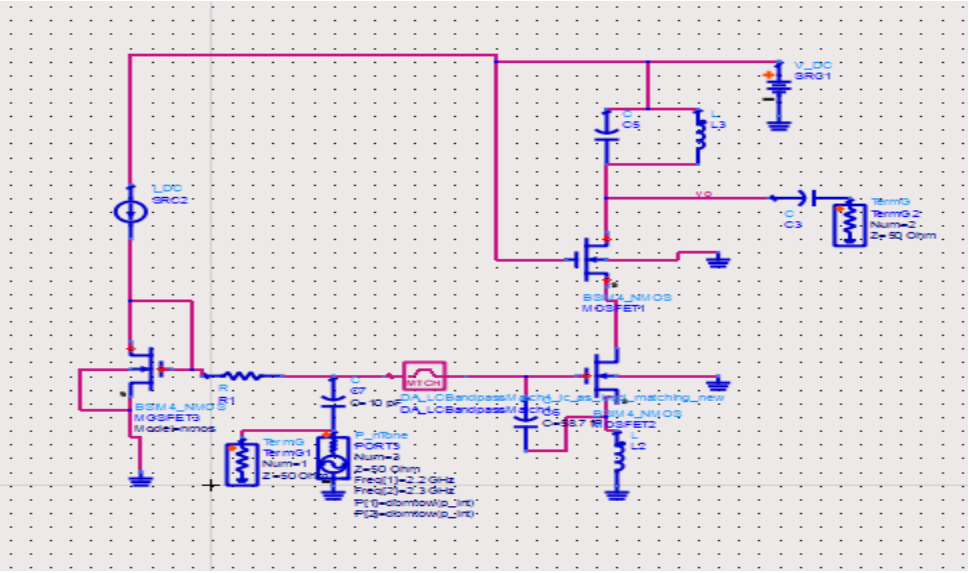

Fig. 3.43 Schematic of LNA (Circuit 6)

S-parameter simulation is to be carried out to obtain the results for various performance parameters of LNA. On the basis of the curves obtained after S-parameter simulation we obtain the values of LNA parameters. First parameter to be analysed is the gain offered by the LNA. From the curve obtained for S_{21} gain of the LNA is found to be 9.1 dB at the operating frequency of 2.4 GHz. Gain offered by the circuit is sufficient for Bluetooth and BLE applications . Curve obtained for S_{21} is given below:

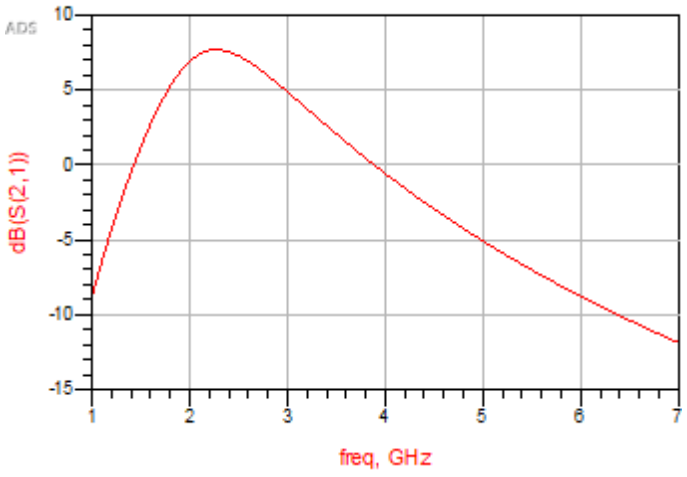

Fig. 3.44 S_{21}(Gain) of the LNA (Circuit 6)

Next parameter to be analysed is the input return loss i.e. S_{11} of the circuit. Value of S_{11} at the operating frequency indicates that the matching achieved by this matching

network is perfect and a good value of S_{11} is obtained. Curve obtained for S_{11} is given below:

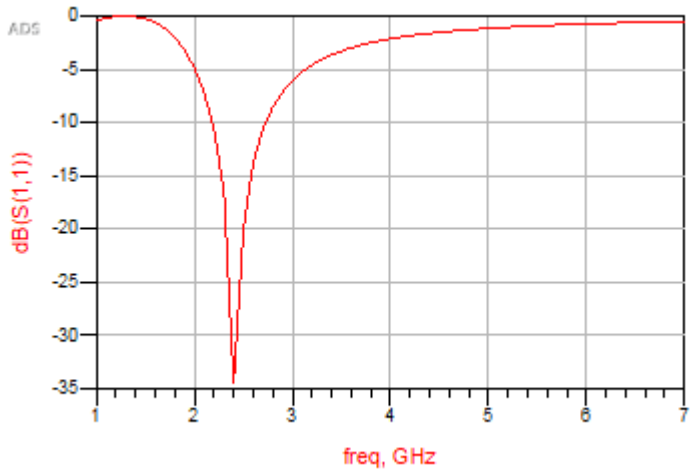

Fig. 3.45 S_{11}(Input Return Loss) of the LNA(Circuit 6)

Next parameter to be analyzed is the reverse gain of the LNA which is analyzed by the curve obtained for S_{12}. From the curve obtained for the parameter S_{12} we found out the value of reverse gain to be equal tp -63 dB which indicates excellent isolation betweeen the input and ouput ports of the circuit. Isolation from output to input is necessary to ensure porper operation of the circuit even if some power leakages occur form the ouput to the input port. Curve obtained for S_{12} is given below:

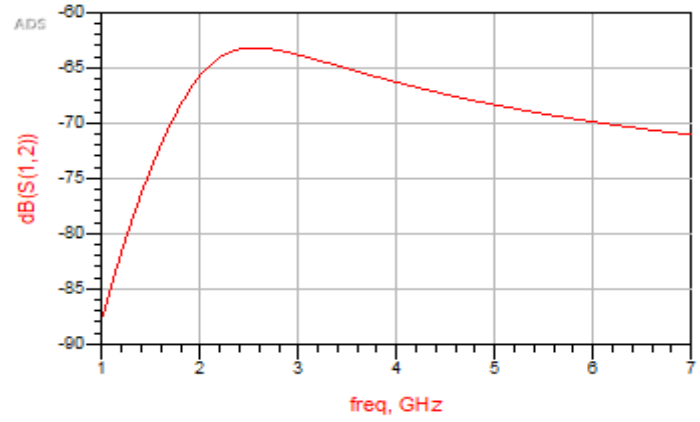

Fig. 3.46 S_{12}(Reverse Gain) of the LNA(Circuit 6)

Next S parameter to be analyzed is the output reflection coefficient of the circuit which is obtained by the value of the parametr S_{22}. Value of parameter S_{22} obtained from the curve is found to be -1.45 dB at the operating frquency of 2.4 GHz. Curve obtained for S_{22} is given below:

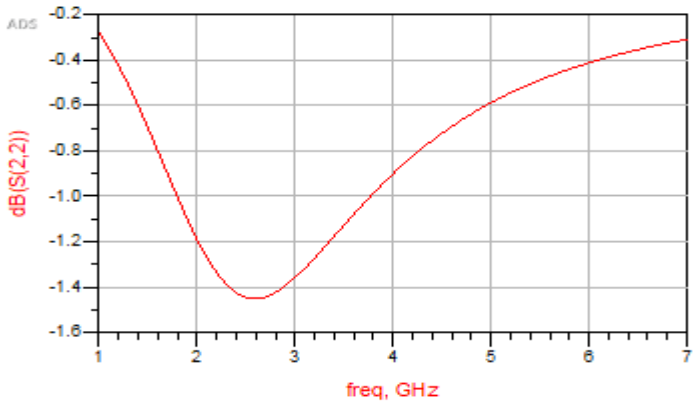

Fig. 3.47 S_{22}(Output Reflection Coefficient) of LNA(Circuit 6)

Next important parameter of the LNA is the Noise Figure of the circuit which is given by the curve obtained for the $NF_{min.}$ From the curve obtained we found the minimun NF to be 0.8 dB. NF of the circuit is found to be within the standards of LNA. Curve obtained for the Noise Figure is given below:

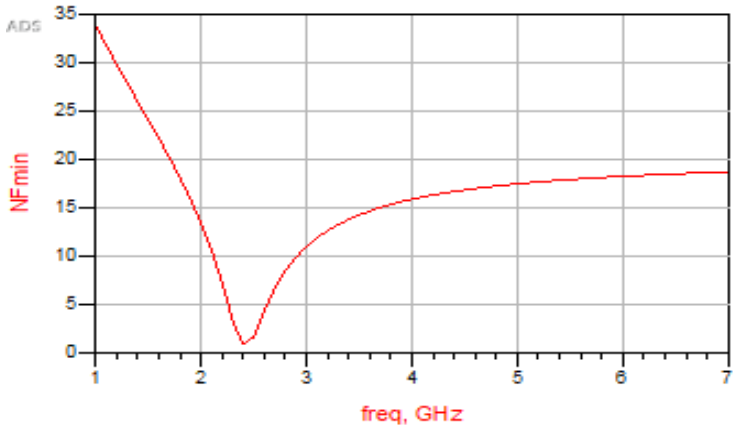

Fig. 3.48 NF_{min} of the LNA(Circuit 6)

After the S-parameter simulation we proceed to Harmonic Balance Simulation which is used to obtain the curves used for calculation of IIP3. Harmonics curves for calculation of IIP3 are obtained using two-tine test during simulation in ADS. Fundamental harmonic and the higher order harmonics can be obtained using Hb simulation in ADS.Value of IIP3 can be obtained by extending these curves and obtaining the point of intersection of these curves. Curves obtained for the fundamental and third order harmonics are given in the Fig 3.49.

Value of IIP3 obtained from the curves is found to be 10 dBm which indicates a highly linear circuit and is considered a very good value of IIP3 for a circuit. IIP3 value indicates that the circuit is highly linear and the calculations for the IIP3 of the LNA are shown in

the curve given below figure. Results obtained after simulation are listde in tabular form below

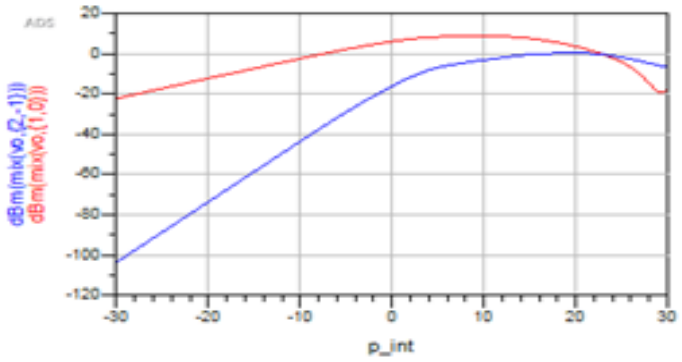

Fig. 3.49 Fundamental Harmonic and Third order harmonic curves for LNA (Circuit 6)

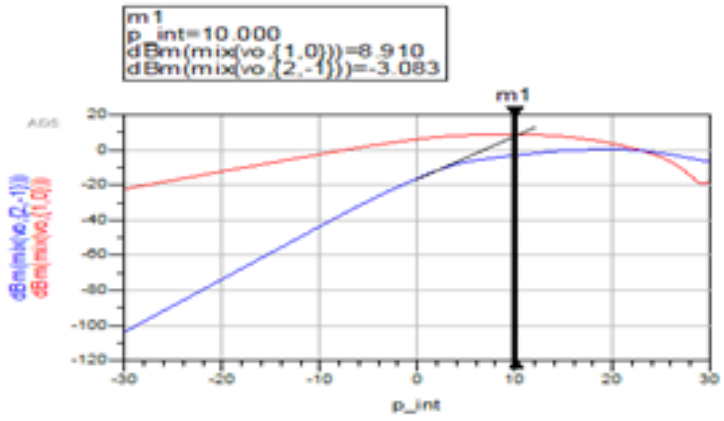

Fig. 3.50 IIP3 of the LNA(Circuit 6)

. Table 7. Parameter values (Circuit 6)

Parameter	Value
S_{11}(dB)	-35
S_{12}(dB)	-63
S_{21}(dB)	9.1
S_{22}(dB)	-1.45
NF_{min} (dB)	0.8
IIP3(dBm)	10
Power Consumption(mW)	9.37

CHAPTER 5
CONCLUSION AND FUTURE SCOPE

Results obtained by the simulations for the different circuits are compiled in a tabular form as given below which makes the comparison of performance easier. After simulations of circuits we compare the results obtained to identify the circuit with best performance among all these circuits. From the results obtained we observe that the circuit designed by us which used a new matching circuit provided the best performance than the other circuits reported.

Table 8. Combined Comparison Table

Parameter	Circuit 1	Circuit 2	Circuit 3	Circuit 4	Circuit 5	Circuit 6
S_{11}(dB)	-9	-8	-3	-12	-1	-35
S_{12}(dB)	-44	-45	-43	-43	-53	-63
S_{21}(dB)	20	17	28	22	19	9.1
S_{22}(dB)	-29	-11	-4	-0.5	-1.48	-1.45
NF_{min}	4	3.7	3.7	6	2.8	0.8
IIP3(dBm)	-8	-7	-7	-4.23	-2.00	10
Power (mw)	12.33	11.45	11.45	10.13	10.91	9.37

All the topologies studied so far emphasized on certain fixed parameters which were to be optimized .Future research in this particular area will also focus only on those parameters. Further improvements can be done in these topologies to improve their performance and increase their efficiency in real time application for signal recording and analysis. The discussion can be made endless as there are many different architectures that have been suggested so far for implementing LNA in bluetooth applications .LNA in bluetooth applications can be extended by making changes in the existing architectures and simulating them to see their performance variations.LNA should mainly have a very low noise efficiency factor as the name suggests LNA should have low noise and also it should have a considerable gain sufficient for signal analysis.

Till date many new technologies have arrived. The circuits can be optimised and simulated on the new technologies as well and the improvements obtained in the parameter values can be analysed. Researchers have started working on more thin

technologies now, which include 45nm technology as well. We may implement this circuit on new technologies as well and compare the difference in the parameter values.

With the increasing work on the Internet of things(IoT), bluetooth devices have also become a topic of research as Bluetooth low energy(BLE) devices are a proper solution for wireless devices in IoT.

The fabrication of passive inductor requires larger Si area and it is not scalable as technology scale. Various active inductor design techniques can be used. Active inductor based LNA design requires less Si area but it adds more noise and consumes more power. However the noise figure and power consumption of active inductor based design can be reduced by using noise cancelling techniques and low power LNA design. New design techniques can always be inculcated to improve the performance provided by the LNA and LNA's which consume drastically low power can be designed which are best suitable for BLE applications.

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APPENDIX – I

LIST OF PUBLISHED PAPERS

1. **Malti Bansal, Diksha Singh, " Low Noise Amplifier for Neural Applications ", International Journal of Computer & Mathematical Sciences IJCMS ISSN 2347 – 8527 Volume 6, pp -74-81, Issue 11, November 2017**
2. **Malti Bansal, Diksha Singh, "Low Noise Amplifier In Bluetooth And Bluetooth Low Energy (Ble) Applications", In Proceedings Of National Conference On Emerging Trends in Electronics and Communication-2019, pp. 110-113**
3. **Malti Bansal, Diksha Singh, "Design and Implementation of Low Noise Amplifier in Neural Signal Analysis", in proceedings of International Conference on Information, Communication and Computing Technology ICCICT 2019, pp. 1-11**
4. **Malti Bansal, Diksha Singh, "Cascode Common Source LNA With Inductive Degeneration Topology Utilizing Different Output Matching Circuits In 45nm CMOS Technology ", in proceedings of International Conference in Communications and Electronics Systems(ICCES 2019), pp. 594-598**
5. **Malti Bansal, Diksha Singh, "Different Input Impedance Matching Circuits For Cascode Common Source LNA With Inductive Degeneration Topology In 45nm CMOS Technology", in proceedings of International Conference in Communications and Electronics Systems(ICCES 2019), pp. 589-593**

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LNA for Neural Applications

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Abstract: *LNA is an important component of transceivers and is widely used in neural signal analysis. In this paper, we review the different topologies and configurations used for LNA in neural applications. We compare the different topologies and conclude which one is the best topology among the ones studied on basis of certain parameters that govern the performance of a LNA for neural applications. According to our analysis, CMOS bipotential amplifier is the most appropriate neural amplifier in terms of all design parameters taken into consideration for use of LNA in neural applications.*

Keywords: LNA, SNR, Neural, Feedback Amplifier, Differential, Impedance.

I. INTRODUCTION

Nowadays, diseases are being diagnosed on the basis of analysis of the signals produced as a result of chemical reactions in our body. Neural signals produced in our brain are very weak signals and noise gets added as they are passed through various components which are used in their analysis. Noise degrades the signal to noise ratio of these neural signals and as a consequence of addition of noise, it becomes difficult to study brain activity pertaining to these signals. Low Noise Amplifiers (LNAs) are best suited to analyze these weak signals. LNA amplifies the signal received at the input; and very less noise is added due to its components, to the received signal. Hence, the SNR of the signal is maintained at an appropriate level which is suitable for analysis of neural signals. In this paper, we review the different topologies and configurations used for LNA in neural applications. We compare the different topologies and conclude which one is the best topology among the ones studied on the basis of certain predefined parameters. Section I of the paper is an introduction to the topic, section II briefly reports about an LNA, section III reviews the use of LNA for neural applications and compares the different topologies of LNA utilized for neural applications and finally section IV gives conclusion and future scope of this area.

II. LNA

As an amplifier is an active device, its components add additional noise to the signal and the signal to noise ratio (SNR) of the signal is decreased. Amplifier should be chosen such that it adds very little noise to the signal which passes through it. Low Noise Amplifier serves this purpose and it is designed such that, noise added due to its configuration is very low. LNA is placed at the initial stage of the receiver or the transceiver. Placing the LNA at the initial stage of the receiver reduces the cascaded effect of noise due to other components of the system which may include mixer, oscillator, etc. Noise performance of the LNA governs the performance of the complete receiver system. LNA should be designed such that it has a very high gain and improved noise efficiency factor (NEF). LNA need to be connected to other components of the receiver system, so input and output impedance should be high enough to prevent loading effect on other components connected. Loading effect tends to decrease the gain of the amplifier as effective load resistance of the amplifier decreases as a consequence of low resistance of the adjacent components. A proper matching network need to be used for complete transmission of signals without loss [1]. However, many other parameters also govern the performance of a LNA. For example, power consumption for an LNA should be low, CMRR should be high, chip area being utilized should be as minimum as possible and various other design parameters should also be considered.

Yuhki Imai et. al [2] reported various steps involved in the design of LNA which includes biasing, proper transistor choice, frequency stabilization, etc. They stated that the very first step involves the proper selection of the transistor to be used. We should check if the components of the amplifier are stable at the frequency of operation, if not then

techniques should be used to make the operation stable at the required frequency. Proper biasing needs to be done to optimize the parameters like noise, gain, power dissipation, etc.

III. Use of LNA for Neural Applications

Detailed examination of neural signals produced in our brain helps us to understand the brain activities. Detailed analysis also provides a better understanding of disorders related to brain i.e., Parkinson's disease, Alzheimer's disease and various others [3][4]. Electrodes are used for interfacing these with the tissues present in the brain [5]. Multiple sites can also be observed at the same point of tine i.e., activities in different parts of brain can be studied by using multichannel neural amplifiers. Multichannel LNA are capable of observing multiple neuron activities at the same instance but the area occupied by these amplifiers is increased because multiple amplifiers are to be fabricated on a single chip. However, many multi-channel amplifiers reported so far were also found to use a very small chip area. Neural signals lie in the range of few millvolts and are therefore considered as very weak signals. LNA is suitable for analysis of these signals because the noise added by this type of amplifier is very less and does not degrade the SNR of the signal. Neurons may generate a rhythmic pattern of action potentials or spikes and if they generate action potentials in sync, this gives rise to local field potentials. Neural signal can also be considered as superimposition of action potentials or spikes on low frequency local field potentials. Frequency range for these signals is different. Action potentials lie in higher frequency range (300-6000 Hz) in comparison to local field potentials (1-200 Hz) [6]. LNA's are specially designed to study these signals separately in their respective frequency band. Some configurations focus on action potential analysis and some on local field potential analysis; because of the different frequency range. Noise that affects the LNA in neural signal analysis can be thermal noise, flicker noise, background noise, etc. Amplitude of neural signals is weak and frequency is also not much large, so these signals can easily be sensed from skin surface [7]. Electrodes acquire the required signals generated from the neurons [8].

A basic LNA for neural applications always uses an operational transconductance amplifier (OTA) along with additional circuitry. AC coupling is always provided to the neural amplifier to block DC voltages developed .This can be achieved by using a capacitor in the circuit which requires a larger chip area. Later on , telescopic OTA were used which provided better performance than other OTA structures available. These were observed to provide low noise and power consumption in comparison to other architectures [8][9][10]. Telescopic OTA can only be used for signals which have low swing amplitude. However, these were used in neural signal analysis with some modification because neural signals have weak amplitudes. Bulk driven method was observed to improve the output swing [11]. Various configurations of LNA which have been used for neural applications have been described below.

(i)Feedback Configuration

Using feedback in amplifier significantly improves the noise figure (NF) of the amplifier. Capacitive feedback is most widely used in case of LNAs. We discuss the different types of capacitive feedback topologies employed for LNA in neural applications. H. S. Kim et.al [12] have reported a low power, low noise neural LNA for implantable biomedical devices. This configuration used an OTA with capacitive-feedback. The capacitive feedback used helps to obtain an accurate gain. Use of capacitive feedback also improves the gain and in this configuration, it was found to depend on the ratio of the capacitances C_{IN} and C_F used in the circuit of this amplifier. Gain obtained in this topology was around 46 dB which was obtained on the basis of capacitance values C_{IN} and C_F used in this configuration. In general, the frequency range of the amplifier should be sufficient enough to include all types of signals produced by the neuron activities. In this topology, the high pass cutoff frequency was determined by the value of the capacitor placed at the input terminal of OTA. The low pass cutoff frequency was determined by $G_M/(A_M.C_L)$ where G_M is the transconductance of the OTA used. AC coupling was also used to remove the large offset DC voltage which was developed due to chemical reactions at the neuron interface. AC coupling can be achieved by placing a capacitor at the input terminal of the OTA. A capacitor acts as short circuit for the AC signals and it acts as an open circuit for DC signals and blocks them. The configuration used has been shown in the Figure 1.

International Journal of Computer & Mathematical Sciences
IJCMS
ISSN 2347 – 8527
Volume 6, Issue 11
November 2017

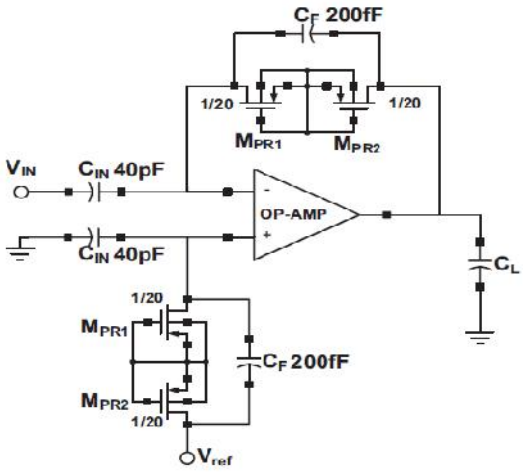

Fig.1: Block diagram of the neural amplifier (reproduced from [12])

Positive terminal of the OTA was grounded and the input was applied at the negative terminal. A capacitor C_{IN} was also placed at the input negative terminal to provide AC coupling because the capacitor blocks the DC signals. C_F is the feedback capacitor and it provides a negative feedback to the amplifier. A capacitor is also connected to the positive terminal of the OTA along with additional circuit. The architecture of the OTA used in the amplifier is held responsible for the performance of the LNA. This neural amplifier used two stage architecture for the OTA and it helped to obtain high gain and large output swing. The first stage of the OTA was designed to obtain better noise performance, mainly focused on flicker noise. Current mirrors used as load were implemented using source degeneration resistors which provided a better noise performance. Miller capacitor was also used to improve the bandwidth of the OTA.

This configuration was found to consume very low power; and other parameters were also found to be in sufficient range to analyze the neural signals. This amplifier was designed on a 0.18µm CMOS process and occupied a chip area of 0.136 mm^2. A NEF of 2.6 was obtained which was found to be better than pervious works done in the similar configuration. S. Dwivedi et.al [13] reported a low power neural recording amplifier for recording local field potentials. Local field potentials are related to the spikes formed during neuron interaction. This amplifier was specifically designed for analyzing the local field potential developed due to neuron interactions. This amplifier also used an OTA along with a capacitive feedback. The architecture uses a capacitor which is connected at the negative terminal of the OTA and a reference voltage source connected to the positive terminal of the OTA. The feedback circuit uses a capacitor and MOS pseudo resistor elements $M_{a,b,c}$ which are biased such that they exhibit a high resistive value .The neural signals are connected to the input terminal via a capacitor which blocks unwanted DC signals rising due to the electrode and tissue interaction .The use of pseudo resistors decreases the chip area because high-resistance elements can be implemented in a small chip area by using MOS. Gain of the amplifier can be calculated by the ratio of the capacitance values used; one at the input terminal of OTA and other as feedback element. Using a capacitor at the input also helps to remove DC signals and filter out the irrelevant signals. The high cutoff frequency was determined by the value of the capacitor connected in the feedback circuit and the equivalent resistance of the MOS elements which were used in the feedback circuit. The low cutoff frequency was determined by the capacitor C_L connected at the load terminal. The capacitor values should be chosen such that the cutoff frequencies are able to cover up the frequency range of the signals produced by neurons. This configuration used 0.18µm CMOS technology at 27ºC. This amplifier occupied a chip area of about 0.10 mm^2 which was found to be very much area efficient. This amplifier used very low power for its operation. However, noise efficiency was not improved significantly in this configuration.

(ii) Cascode Configuration

This is a two stage configuration which can improve the bandwidth of the amplifier, input and output impedance or the gain of the amplifier in case of BJT amplifiers. Telescopic and folded cascade amplifiers were used where low noise, large DC gain, high unity gain frequency were required as the important characteristics [14]. Telescopic architecture provided better power efficiency and folded cascade was seen to provide higher output swing. Further changes were done in these architectures to improve the various performance parameters. AC path and DC path were separated and the transistors were split to ensure proper matching [15]. Sammy Cerida et.al [16] reported a low-noise amplifier which was based on fully differential recycling cascade architecture. This amplifier is based on recycling architecture [17] which provides an improvement in gain and bandwidth. The architecture of this amplifier

International Journal of Computer & Mathematical Sciences
IJCMS
ISSN 2347 – 8527
Volume 6, Issue 11
November 2017

(Figure 2) consists of two current mirrors M3a-M3b and M4a-M4b in which currents were reused, which was not implemented in any of the earlier architectures .These current mirrors improved the gain of this amplifier and bandwidth was also improved. The architecture was observed to have symmetry on both the sides of the amplifier and hence all the parameters were observed to be the same. The symmetry was a result of fully differential architecture of the amplifier. In this architecture M3a-M3b,M4a-M4b,M9,M10 were required to operate in strong inversion and a large V_{ov} was maintained to do so. Operating these transistors in strong inversion reduces the thermal noise. Through analysis, they found that value of K should be as small as possible but greater than one. For reducing flicker noise, it was found that value of K should be smaller than one. So K was chosen to be greater and close to 1. The differential pair transistors were operated in weak inversion by keeping the V_{OV} small. These were operated in weak inversion for increasing the transconductance which resulted in increase in gain. This architecture was simulated on a 0.35µm CMOS process and offered a gain of around 42 dB. Power consumption was found to be 66µW and noise efficiency factor of 2.58 was obtained. This work was compared with the previous works and the NEF was improved however the power consumption was higher than others.

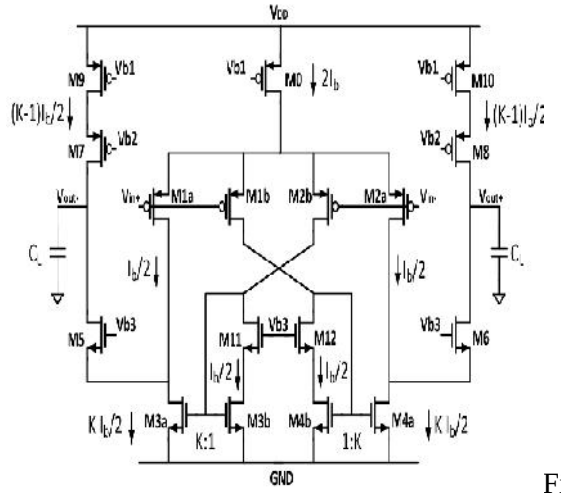

Fig. 2: Fully-differential recycling folded cascode amplifier (reproduced from [17])

Vahid Majidzadeh et.al [18] reported an amplifier intended for recording activities of multiple neurons at a single point of time. Brain activities can only be studied by analyzing signals from multiple neurons, so amplifier designed should be efficient when implemented in multichannel mode. Therefore, chip area occupied by an amplifier becomes an important factor in implementing multi channel amplifier for neural signal analysis. This amplifier was designed on partial OTA sharing technique (Figure 3) which decreased the area occupied by the amplifier on chip .This sharing architecture OTA also decreased the chip area by sharing the bulk capacitor required for circuit implementation. Power consumption was maintained within the prescribed limits such that it did not have an adverse effect on the brain tissues [19].

Transistor M_{c0} was operated in weak inversion region which ensures that no extra circuitry is required for generating voltages required for the transistor M_{d0} to operate in saturation region. All the theoretical improvements were simulated on a 0.18µm CMOS process. Total area occupied by an array of four amplifiers was found and effective area for one amplifier was found to be 0.0625 mm^2. The gain obtained was 39.4 dB. NEF reported was one of the best values obtained. NEF of 3.35 was achieved for an array of four amplifiers. However, a better NEF could be achieved by reducing the flicker noise contribution by size of the devices. Since it was a multichannel amplifier, crosstalk between adjacent channels was also taken into consideration and efforts were made to reduce it for effective observations. CMRR was measured to be 70.1 dB which was within the desired limits. PSRR of 63.8 dB was obtained for this amplifier.

Carolina Mora Lopez et.al [20] reported an amplifier which was multi-channel and consisted of 16 channels and each channel had a low noise fully differential amplifier (Figure 4).

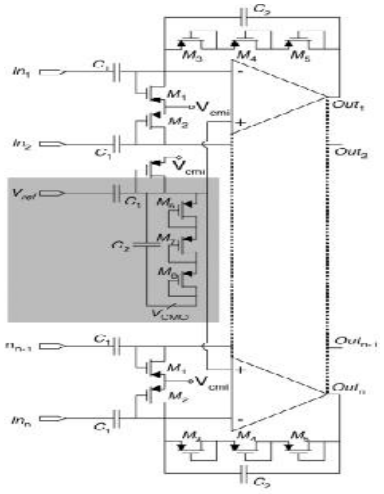

Fig.3: Partial sharing OTA architecture (reproduced from [18])

International Journal of Computer & Mathematical Sciences
IJCMS
ISSN 2347 – 8527
Volume 6, Issue 11
November 2017

Noise analysis of this amplifier considered all the sources in the circuit that could contribute to the noise of the amplifier. Electrodes used were also a source of noise and the electronic circuitry also adds noise to the signal produced by the neurons. Thermal and flicker noise were kept lower than electrode noise, this helped to reduced contribution of overall noise. Design of the amplifier involved various parameters like power consumption, chip area, etc. In this architecture a single channel was using a fully differential folded cascade OTA. Gain of the amplifier was calculated by the ratio of value of the capacitor placed in the feedback circuit and the value of capacitor placed at the input terminal. The differential pair in this amplifier used PMOS which were operated in weak inversion. Weak inversion region operation of the transistors ensured that the transconductance was high and hence, it reduced the effect of noise [21]. M4-M5 and M10-M11 were operated in strong inversion to reduce the effect of noise. Flicker noise was also minimized by increasing the size of the transistors. Pseudo resistors were effective in decreasing the chip area because they can realize high resistance values [21].

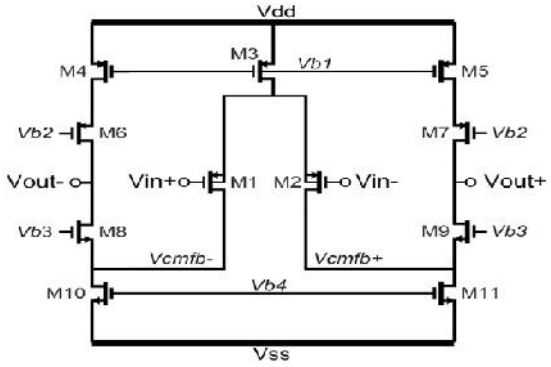

Fig.4: Fully differential folded cascade input amplifier (reproduced from [20])

N. Ghaderi et.al [22] reported LNA which used a bulk driven cascade current mirror as load. This used a new telescopic OTA which was found to have a better output swing than other telescopic OTA. Output swing could be increased by reducing the voltage drop on the load. Bulk driven cascade current mirror was used along with telescopic OTA to increase the output swing in this amplifier reported. Gate driven cascade current mirror was also used in some architectures but it had certain limitations which restricted its use to only single stage telescopic amplifiers [23]. BD cascade current mirror (BDCCM) (Figure 5) was reported to decrease the threshold voltage of the transistors used as a result of which output swing was found to increase.

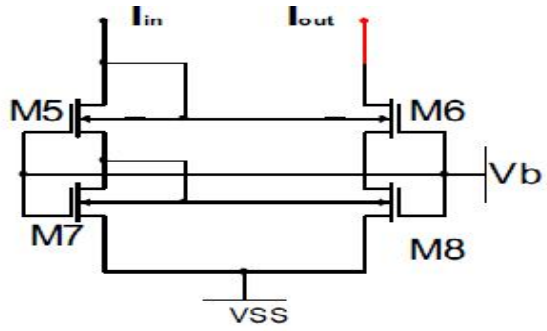

Fig.5: BDCCM (reproduced from [22])

Architectures with BDCCM as a load had a better noise efficiency and gain as compared to architectures without BDCCM as a load. This amplifier had a gain equal to 38.9 dB, power consumption of 6.9 µw, NEF of 2.2 and output swing of 0.7V. This was capable of amplifying wide range of neural signals produced in body.

(iii) Bipotential Configuration

Tan Yang et.al [24] reported an array of neural amplifiers which was found to be suitable for large scale integration. Array of neural amplifiers is capable of analyzing activities of multiple neurons simultaneously and it provides a better understanding of the associated brain disorder if any.

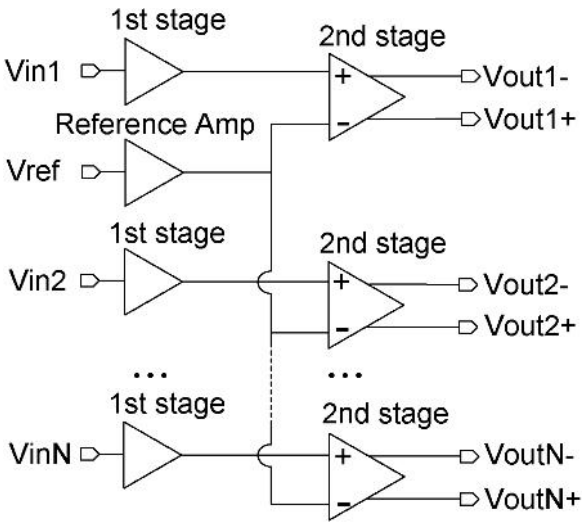

Fig. 6: Multichannel Bipotential Amplifier (reproduced from [24])

This particular configuration used two stage amplifier (Figure 6) in combination with Current Reuse Complimentary Input (CRCI) technique [25]

International Journal of Computer & Mathematical Sciences
IJCMS
ISSN 2347 – 8527
Volume 6, Issue 11
November 2017

to achieve the desired performance of the neural amplifier. The first stage used an amplifier which was found to use a capacitive feedback and CRCI technique. This stage achieved good noise efficiency but the Power Supply Rejection Ratio was found to be below desired value. Hence, a second stage was used to improve the value of the PSRR. The second stage used fully differential OTA along with capacitive feedback. A reference amplifier was also used which was common to all the channels and the architecture of this reference amplifier was responsible for significant reduction in power dissipation. Noise was equally coupled to the first stage and the reference amplifier. Noise was suppressed by the second stage as a common mode signal and it improved the noise performance of this LNA. The first stage amplifier and the reference amplifier were matched to each other in terms of gain which helped to achieve a good PSRR and CMRR. Mismatch between the first stage and the reference amplifier gave rise to a poor value of PSRR. Capacitive feedback was used in the first stage and the reference amplifier which helped to achieve a good gain accuracy and linearity. This configuration was found to achieve a NEF of 1.93 which is convincing and a PSRR of 50 dB which is sufficient for typical use. Each channel occupied a chip area of 0.137 mm^2. NEF of this configuration could be further improved by making certain changes such as sharing the reference amplifier between more number of channels.

(iv) Reconfigurable configuration

Jose Luis Valtierra et. al [26] reported a 4 mode reconfigurable low noise amplifier. Two types of signals are produced in the brain: action potentials and local field potentials. These signals have different amplitudes and frequency range. This amplifier was capable of analyzing both types of signals produced in the brain. Bandwidth could be selected to analyze these signals separately or at the same point of time. Analog front end amplifier should have low power consumption to prevent tissue damage, input referred noise should be less than background noise and the architecture should be able to reject DC offsets produced. This amplifier was capable of selecting different modes which could select different neural signal frequency ranges (Figure 7). It was designed such that its circuit was changed and value of capacitor was also changed when it was switched from one mode to another with the help of control signals.

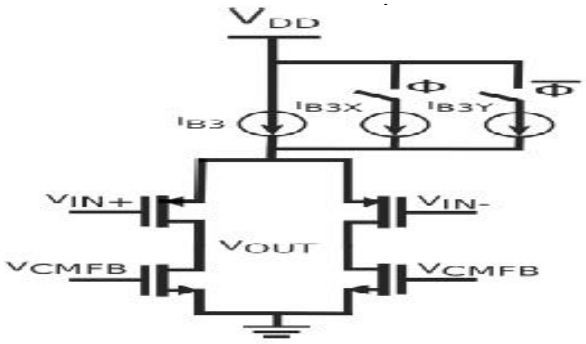

Fig.7: Simple programmable OTA (reproduced from [26])

The four modes which were available were fast ripple mode, action potential mode, local field potential mode and full bandwidth mode. Full bandwidth mode covered both the frequency bands of action potentials as well as local field potentials. Local field potential mode covered the frequency range of action potentials. Fast ripple mode covered the high pass pole of action potential range and low pass pole of local field potential range. Power consumption could be further reduced. Gain obtained was different for the four modes which were available in this architecture.

IV. Comparison of Different Configurations of LNA for Neural Applications

After analysis of different architectures / configurations, we compare the architectures / configurations in terms of different parameters such as NEF, power, gain, bandwidth, etc. As discussed so far, neural signals are weak signals and hence the gain of the architecture chosen should be high enough to increase the amplitude to a threshold level which makes these signals suitable for analysis. However the best architecture could be different depending on the real time requirements. For example, some application may require a better noise efficiency, some other application may require a particular bandwidth depending on the signals to be analyzed (action potentials and local filed potentials), etc. We have considered 10 parameters to analyze the performance of the amplifiers and represented the data in a tabular form (Table 1 and Table 2). We have considered NEF and gain as dominant parameters.

International Journal of Computer & Mathematical Sciences
IJCMS
ISSN 2347 – 8527
Volume 6, Issue 11
November 2017

Table 1: Different Parameters of LNA for neural applications

Parameter	[12]	[24]	[13]	[26]	[26]
CMOS Technology(µm)	0.18	0.09	0.18	0.18	0.18
Bandwidth(Hz)	13800	4900-10500	3-164	0.129-590	224-6800
Input-referred Noise (µVrms)	5	3.04	5.62	4.2	4.1
Power (µW)	-	-	-	0.454	0.454
NEF (Noise Efficiency Factor)	2.6	1.93	6.33	4.5	1.31
Gain (dB)	46.2	58.7	31.7	48	48
Supply voltage (V)	1.2	1	0.8	1	1
CMRR (dB)	>66	>45	-	-	-
PSRR (dB)	>74	>50	54	-	-
Chip area (mm^2)	0.136	-	0.098	-	-

Table 1 continued

Parameter	[16]	[20]	[18]	[22]
CMOS Technology(µm)	0.35	0.35	0.18	0.18
Bandwidth(Hz)	6023	6000	7200	89-7000
Input- referred noise(µVrms)	1.16	1.9	3.5	2.45
Power(µW)	66.03	66	7.92	6.9
NEF(Noise Efficiency Factor)	2.58	1.9	3.5	2.2
Gain(dB)	42.1	33.98	39.4	38.9
Supply Voltage(V)	3.3	3.3	1.8	±0.9
CMRR	-	-	70.1	-
PSRR	-	-	63.8	-
Chip Area(mm^2)	-	-	0.0625 mm^2	-

V. CONCLUSION AND FUTURE SCOPE

All the topologies studied so far emphasized on certain fixed parameters which were to be optimized. Future research in this particular area will also focus only on these parameters. Further improvements can be done in these topologies to improve their performance and increase their efficiency for real time applications for signal recording and analysis. Study of LNA in neural applications can be extended by making changes in the existing architectures and simulating them to see their performance variations. LNA should have low noise and also it should have a considerable gain, sufficient for neural signal analysis. As per the architectures / configurations considered by us, bipotential amplifier proves to be the best LNA for use in neural applications. It was reported to have a noise efficiency factor of 1.9 and a gain of 58.7 dB, which are the best figures reported till date.

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LOW NOISE AMPLIFIER IN BLUETOOTH AND BLUETOOTH LOW ENERGY (BLE) APPLICATIONS

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Abstract: LNA is an important component of transceivers and is used in different applications. In this paper, we analyze the advantages of Bluetooth Low Energy (BLE) over classic Bluetooth.We review the salient features of LNA's implemented in Bluetooth and BLE applications and what additional steps can be taken to improve their performance in wireless domain. We come to a conclusion that BLE will replace Bluetooth as it has a lower power consumption, which gives BLE an upper edge over Bluetooth.

Keywords:Wireless,LNA,BLE, Bluetooth

I. INTRODUCTION

Wireless communication has become an important necessity of today's world. Demand of technologies that are compatible with changing trends in technology is increasing and end-users desire that their devices should support new technologies i.e. WiMax, 3G, 4G, 5G and so on. Household devices may not be connected to wireless devices at this time but in coming future this will also become possible as Internet of Things is the hottest topic of research today. This increases the necessity of designing RF circuits that can be implemented for wireless communication as well as maximising the circuit complexity i.e., integrating a large number of elements on a single chip. All these technologies combined together can contribute to bright future of RF circuits. Designing of RF circuits requires a good understanding of many disciplines that include understanding of RF and microwave theory, VLSI and other basic concepts of RF circuits. Transceiver is one of the basic components of RF circuits. The transceiver is responsible for transmitting as well as receiving information at the same point of time i.e., it performs the work of a transmitter as well as a receiver.At the receiver end, generally the first block is a Low Noise Amplifier(LNA). If we restrict to wireless communication, the operating frequency gets fixed to 2.4 GHz because itis the only available frequency which does not require a license for its use. Bluetooth technology also works on the same frequency.

With the increasing need for the Internet of things (IoT), Bluetooth low energy (BLE) technology has become a popular solution for wireless devices.When compared to classic bluetooth, BLE has an advantage of low power consumption. Hence it will be apt for IoT based applications.

II. LNA

LNA is generally the first block in the receiver systems. It is seen to govern the performance of the whole receiver block. Hence we need to minimise the Noise Figure of the LNA, i.e. noise efficiency of
complete receiver block will be improved by the noise efficiency of the LNA itself.LNA with all parameters perfectly within the limit cannot be designed as trade-off always exists between the different parameters of a circuit. Based on our application area, we need to focus on the parameter to be optimised and accordingly the LNA design procedure is carried out further.Application of LNA also decides the components that can be utilised in the circuit design. For example, if we require a system on chip, we should avoid components which occupy larger chip area.Design steps for LNA remains the same even if the applications are different. Low noise amplifiers are being used in receiver systems, biomedical domain, wireless communication, ISM band etc. If we wish to have a higher gain, again we can contain connect multiple stages in cascade with each other; they will provide an optimised gain with reduced performance in terms of other parameters. If we wish to optimise chip area occupied by the amplifier, we should use a single stage amplifier because increasing the number of stages increases the chip area that is being occupied. We should also avoid using bulk elements i.e., the elements which occupy larger chip area. If we wish to have lower power consumption we should avoid using multiple stages in our amplifier. The parameter that is to be optimised plays an important role in design specification and the amplifier is to be designed accordingly.However, the basic circuit design steps are same irrespective of the application. Initial step in LNA design is choosing a proper transistor that would be apt for operation at high frequency. Transistor should be chosen such that it is able to work properly at microwave frequencies and keeping in mind the trade-offs regarding the device operation. Secondly, we need to figure out the biasing circuit for the LNA. Biasing circuit should be designed such that it gives a stable operating point for the LNA. Many techniques are proposed for biasing circuits. However, the technique should be chosen so as to be suitable for the application of LNA. Generally divider biasing, transistor biasing, current mirror etc. are used for the purpose of

biasing. Biasing circuit should be chosen such that it does not disturb the stability of the system i.e., stability analysis should be considered while choosing a biasing circuit. For analysing stability at high frequencies, S parameters play a major role. One more important step includes the matching of output and input terminals. Output and input terminals should be properly matched to the successive stages to allow maximum power transfer. If the matching networks are not efficient enough, maximum power transfer will not take place and reflections will increase which in turn will reduce the efficiency of the system. Hence we need to provide input and output matching network for LNA as well. One important parameter at high frequency is the linearity of the circuit. When we operate in small signal range, we approximate the circuit by small signal models of its circuit elements. However, non-linearity is also a factor of circuit performance and it may lead to certain interesting phenomena. If we apply a sinusoidal signal to a non-linear system, the output consists of harmonics of the input frequency. The harmonics generated may dominate the fundamental component due to which the desired signal may get suppressed. We need to reduce the non-linearity i.e., we need to reduce the effect of harmonics on the fundamental frequency component.

A measure of non-linearity of an amplifier can be estimated by calculating IIP3 i.e., Input Third Order Intercept Point. A circuit with higher value of IIP3 is said to be more linear as compared to a circuit with lower value of IIP3. However, a better IIP3 value is achieved at the cost of reduced gain.We need to make a choice between a highly linear circuit or a circuit with the high gain; we can only optimise one of these parameters. IIP3 can be depicted graphically as:

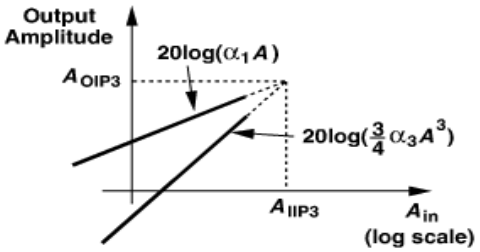

Fig. 1: IIP3 (Reproduced from [1])

To calculate the value of IIP3 for any circuit amplifier, we use two tone test in Advanced Design System. However, we can also carry out theoretical calculations for IIP3 using relevant formulae. The result obtained using theoretical calculation is an approximate value of IIP3 as it assumes that only third order nonlinearity exists and it ignores the higher harmonics.

LNA is used in receiver circuits over a wide range of frequencies. A single LNA can also be designed such that it provides an attractive performance over a broad bandwidth and can work till very high frequencies. This desirable performance can be achieved by using a darlington amplifier also[2]. The cascode amplifier is the most popular solution for LNA since it provides the highest gain over the widest bandwidth with only a slight sacrifice in NF performanceand design complexity.The structure of a cascode amplifier combines a common source (CS) stage and a common gate (CG) stage. The CS stage provides the greatest stability which has better sensitivity to process, temperature variation immunity, power supply, and component variations.Therefore, a cascode amplifier is implemented in the LNA design of the BLE front-end receiver

III. Bluetooth and Bluetooth Low Energy (BLE)

Low power is necessary for mobile devices because consumers are expected to use thedevices for extended periods without charging or changing the power source. Making a sustainable device requires more energy storage, low power consumption, or both.However, the energy storage in the device demands additional space. The large device size also means that manufacturing costs are higher, so increasing the energy storage is an inefficient solution for long-period usage. Therefore, lowering the power of the device not only reduces manufacturing cost but also improves battery usage. Since more power is needed for the device, more space is preserved for the power source or battery.BLE offers a low power consumption that is in accordance with BLE standards.

Bluetooth is widely used for short range communications. Bluetooth is known to work at a frequency of 2.4 GHz and provides us with data connectivity upto a range of 50m. Maximum data rate that is achieved in bluetooth is upto 440 Kbps. Bluetooth connections setup should adhere to specifications which are already listed in Bluetooth specifications. These specifications provide with the allowable range of carrierfrequency, modulation, transmitted power, etc. Bluetooth standard states that the modulcation scheme used should be Gaussian Frequency Shift Keying (GFSK) with index prescribed in the specifications[3][4].

BLE devices slow down the data transfer rate;although it effectively decreases the power consumption. Unlike classic Bluetooth (BT) devices, BLE devices do not need to be at the highest speed possible. For example, while one uses the smartphone to switch on the airconditioner and adjust the room temperature, these applications do not have significant data to transfer. The device

simply needs to send the package containing "power on" and "increase/decrease temperature" from the transmitter to the receiver. On the other hand,while one uses a smartphone to stream television through a BT connection, it is not a simple package containing a single command; instead, it can be a high definition (HD) video or high quality (HQ) music file that must be smoothly played on television. Otherwise, the user will never replace the wired connection with wireless.

Depending on the application requirement, Bluetooth emerged to have different modes of operation. If devices need to operate for longer time, we cannot achieve higher data rates and if higher data rates are desired, power consumption will increase. A trade-off always exists in higher data rates and power consumption of the circuit.

IV. LNA in BT and BLE Applications

LNA in BLE puts a constraint on power consumption of the circuit and it is a difficult task to adhere to power consumption specifications as well as fulfil other system specifications[5].

LNA's are being widely used in designing receivers for Bluetooth as well as BLE. However the basic difference lies in the fact that the power consumption is drastically low in BLE applications. BLE has an advantage of low power consumption which makes it suitable for machine to machine communication. BLE devices can last for years once placed in machine and makes it suitable for IoT devices. Higher speed may not be obtained but longer battery life is surely obtained.

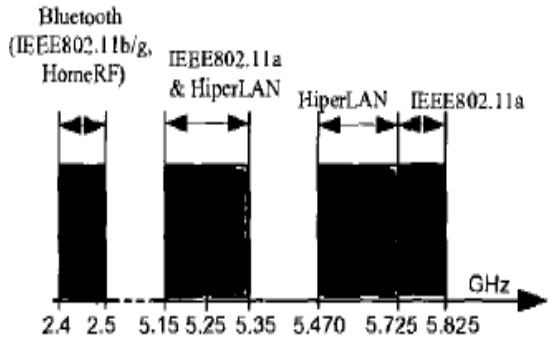

Fig. 2: Wireless Frequency Bands (reproduced from[9])

LNA reported in [6] was intended for Bluetooth and power consumption reported was about 4.6 mW.However, LNA reported in [7]was found to have a power consumption of 1.2 mW which is much lower as compared to power consumption of LNA's for Bluetooth.

LNA reported in[8] was found to have a power consumption of 7.3 mW which is considerably high if we desire to use LNA in BLE applications. Power consumption of the circuit solely determines the application area of the LNA. If power consumed is relatively low, it is considered suitable for BLE applications; otherwise it may be restricted to Bluetooth applications only.

Table 1. LNA for Bluetooth vs. BLE Applications

Reference	[6]	[7]	[8]
Technology	180nm	130 nm	130 nm
Power Consumption	4.6 mW	1.2 mW	7.33 mW
Gain	27 dB	20.34 dB	20.3 dB
Noise Figure(NF)	1.1 dB	3.2 dB	1.98 dB

LNA circuits with power consumption in nW have also been reported, which provide excellent performance in terms of BLE standards. New CMOS technologies further increase the possibility of low power consumption circuits.

V. CONCLUSION

In this paper, we analysed the important parameters of LNA for BT and BLE applications and comparedfew reported circuits of LNA for Bluetooth and BLE applications. We come to the conclusion that BLE circuits consume less power and can be an appropriate choice for IoT based applications. Design of LNA for a different CMOS technology is still a challenge that needs to be tackled everytime a technology change is observed. Redesign of an RF circuit involves reduction of voltage supply for newer technologies that creates a research topic to be explored[10].

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Design & Implementation of Low Noise Amplifier in Neural Signal Analysis

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Abstract. LNA is an important component of transceivers and is widely used in neural signal analysis. In this paper, we review the different topologies and configurations used for LNA in neural applications. We compare the different topologies and conclude which one is the best topology among the ones studied on basis of certain parameters that govern the performance of a LNA for neural applications. According to our analysis, CMOS bipotential amplifier is the most appropriate neural amplifier in terms of all design parameters taken into consideration for use of LNA in neural applications.

Keywords: LNA, SNR, Neural, Feedback Amplifier, Differential, Impedance

1 Introduction

Nowadays, diseases are being diagnosed on the basis of analysis of the signals produced as a result of chemical reactions in our body. Brain activities are also studied by analyzing the neural signals produced in our brain. These neural signals produced are very weak signals and noise gets added as they are passed through various components which are used in their analysis. Noise degrades the signal to noise ratio of these neural signals and as a consequence of addition of noise, it becomes difficult to study brain activity pertaining to these signals. To analyze these signals in an appropriate manner, they need to be amplified up to a certain threshold level without much noise being added to them. Low Noise Amplifiers are best suited to analyze these weak signals and achieve this function. LNA amplifies the signal received at the input; and very less noise is added due to its components to the received signal. Hence, the SNR of the signal is maintained at an appropriate level which is suitable for analysis of neural signals. LNA can be utilized for neural signal analysis with different design techniques to improve the performance of LNA. In this paper, we review the different topologies and configurations used for LNA in neural applications. We compare the different topologies and conclude which one is the best topology among the ones studied on basis of certain parameters that govern the performance of a LNA for neural applications. Section I of the paper is an introduction to the topic, section II briefly reports about an LNA, section III reviews the use of LNA for neural applications, section IV compares the different topologies of LNA utilized for neural applications and finally section V presents conclusion and future scope of this area.

2 Low Noise Amplifier

Amplitude of signals decreases as they pass through environment and additional noise also gets added to them. Amplifiers amplify the signals received at the input but they also amplify the noise along with the signal. As an amplifier is an active device, its components also add additional noise to the signal and the signal to noise ratio (SNR) of the signal is decreased. Amplifier should be chosen such that it adds very little noise to the signal which passes through it. Low Noise Amplifier serves this purpose and it is designed such that, noise added due to its configuration is very low. LNA is placed at the initial stage of the receiver or the transceiver. Placing the LNA at the initial stage of the receiver reduces the cascaded effect of noise due to other components of the system which may include mixer, oscillator etc. Noise performance of the LNA governs the performance of the complete receiver system. LNA should be designed such that it has a very high gain and improved noise efficiency factor (NEF). LNA need to be connected to other components of the receiver system, so input and output impedance should be high enough to prevent loading effect on other components connected. Loading effect tend to decrease the gain of the amplifier as effective load resistance of the amplifier decreases as a consequence of low resistance of the adjacent components. A proper matching network needs to be used for complete transmission of signals without loss [1]. However, many other parameters also govern the performance of a LNA. For example, power consumption for an LNA should be low, CMRR should be high, chip area being utilized should be as minimum as possible and various other design parameters should also be considered. Yuhki Imai et.al [2] reported various steps involved in the design of LNA which includes biasing, proper transistor choice, frequency stabilization, etc. It stated that the very first step involves the proper selection of the transistor to be used. We should check if the components of the amplifier are stable at the frequency of operation, if not then techniques should be used to make the operation stable at the required frequency. Proper biasing needs to be done to optimize the parameters like noise, gain, power dissipation etc.

3 Use of LNA for Neural Applications

Detailed examination of neural signals produced in our brain helps us to understand the brain activities .Detailed analysis also provides a better understanding of disorders related to brain i.e. Parkinson's disease, Alzheimer's disease and various others [3][4]. Electrodes are used for interfacing these with the tissues present in the brain [5]. Multiple sites can also be observed at the same point of tine i.e., activities in different parts of brain can be studied by using multichannel neural amplifiers. Multichannel LNA are capable of observing multiple neuron activities at the same instance but the area occupied by these amplifiers is increased because multiple amplifiers are to be fabricated on a single chip. However, many multi-channel amplifiers reported so far were also found to use a very small chip area.

Neural signals lie in the range of few millivolts and are therefore considered as very weak signals and they may get degraded if more noise gets added to them. LNA is suitable for analysis of these signals because the noise added by this type of amplifier is very less and does not degrade the SNR of the signal. Power consumption is a very crucial factor in case of neural amplifiers as high power may result in increase of temperature and this may damage the brain tissues. An important requirement for the use of LNA for neural applications is that they should be designed in such a way that power consumed by them for operation is very low. Neurons may generate a rhythmic pattern of action potentials or spikes and if they generate action potentials in sync, this gives rise to local field potentials. Neural signal can also be considered as superimposition of action potentials or spikes on low frequency local field potentials. Frequency range for these signals is different .Action potentials lie in higher frequency range (300-6000 Hz) in comparison to local field potentials (1-200 Hz)[6]. LNA's are specially designed to study these signals separately in their respective frequency band. Some configurations focus on action potential analysis and some on local field potential analysis; because of the different frequency range .However some amplifiers used filters which filtered out the desired frequencies to handle Action potentials as well as local field potential simultaneously. In any circumstances, the gain of the LNA should be high because the signals associated are always weak signals. Noise that affects the LNA in neural signal analysis can be thermal noise, flicker noise, background noise, etc. The frequency of the signals is very low hence the flicker noise is more as compared to other types of noise in case of these signals. Amplitude of neural signals is weak and frequency is also not much large so these signals can easily be sensed from skin surface [7]. Electrodes acquire the required signals generated from the neurons. The position of the electron from the neuron also governs the background noise added to the signal [8]. We analyze the different neural amplifiers developed so far and study their performance with respect to different parameters such as noise, gain, power consumption, chip area, etc.

A basic LNA for neural applications always uses an operational transconductance amplifier (OTA) along with additional circuitry. Additional circuitry with an OTA may be a feedback circuit or it may differ in type of load connected. Current mirrors may be used as load in some configurations. Cascade configuration is also used in some LNA's which may further be modified as folded cascode to improve the performance of the LNA. AC coupling is always provided to the neural amplifier to block DC voltages developed. This can be achieved by using a capacitor in the circuit which requires a larger chip area. Telescopic OTA were used which provided better performance than other OTA structures available. These were observed to provide low noise and power consumption in comparison to other architectures [8][9][10]. Telescopic OTA can only be used for signals which have low swing amplitude. However, these were used in neural signal analysis with some modification because neural signals have weak amplitudes. Bulk Driven method was used which was observed to improve the output swing [11].

(i) Feedback Configuration: Using feedback in amplifier significantly improves the noise figure (NF) of the amplifier. Feedback can be provided by using a capacitor in general. However, pseudo resistors using MOS along with the capacitor were also used in some feedback circuits. Capacitive feedback is most widely used in case of LNAs. We discuss the different types of capacitive feedback topologies employed for LNA in neural applications. H. S. Kim et.al [12] reported a low power, low noise neural LNA for implantable biomedical devices. This configuration used an OTA block which was provided with capacitive-feedback. The feedback provided using a capacitor helped to obtain an accurate gain. Use of capacitive feedback also improved the gain and in this configuration, it was found to depend on the ratio of the capacitances C_{IN} and C_F used in the circuit of this amplifier. Gain obtained in this topology was around 46 dB which was obtained on the basis of capacitance values C_{IN} and C_F used in this configuration.

In general, the frequency range of the amplifier should be sufficient enough to include all types of signals produced by the neuron activities. In this topology, the higher cutoff frequency was obtained by using the value of the capacitor placed at the input terminal of OTA. The lower cutoff frequency was obtained by expression: $G_M/(A_M.C_L)$ where G_M is the transconductance of the OTA used. AC coupling was also used to remove the large offset DC voltage which was develops due to chemical reactions at the neuron interface. AC coupling can be achieved by placing a capacitor at the input pin of the OTA block. A capacitor acts as short circuit for the AC signals and it acts as an open circuit for DC signals and blocks them. The configuration was as shown in the Fig. 1. Positive terminal of the OTA was grounded and the input was applied at the negative terminal. A capacitor C_{IN} was also placed at the input negative terminal to provide AC coupling because the capacitor blocks the DC signals. C_F is the feedback capacitor and it provides a negative feedback to the amplifier. A capacitor is also connected to the non-inverting terminal of the OTA along with additional circuit. The architecture of the OTA used in the amplifier is held responsible for the performance of the LNA. This neural amplifier used a two stage architecture for the OTA and it helped to obtain a large gain and a large output swing. The first stage of the OTA was designed to obtained better noise performance mainly focused on flicker noise. Current mirrors used as load were implemented using source degeneration resistors which provided a better noise performance. Miller capacitor was also used to improve the bandwidth of the OTA. This configuration was found to consume very low power; and other parameters were also found to be in sufficient range to analyze the neural signals. This amplifier was designed on a 0.18µm CMOS process and occupied a chip area of 0.136 mm^2. A NEF of 2.6 was obtained which was found to be better than pervious works done in the similar configuration. Shashank Dwivedi et.al [13] reported a neural amplifier for recording local field potentials and consumed low power. Local field potentials are related to the spikes formed during neuron interaction. This amplifier was specifically designed for analyzing the local field potential developed due to neuron interactions. This amplifier reported also used an OTA along with a capacitive feedback (Fig. 2). The architecture uses a capacitor which is connected at the inverting terminal of the OTA and a reference voltage source connected to the positive terminal of the OTA. The feedback circuit uses a capacitor and MOS pseudo resistor elements $M_{a,b,c}$ which are biased such that they exhibit a high resistive value. The neural signals are connected to the input terminal via a capacitor which blocks unwanted DC signals rising due to the electrode and tissue interaction. The use of pseudo resistors decreases the chip area because elements with large values of resistance can be implemented in a small chip area by using MOS.

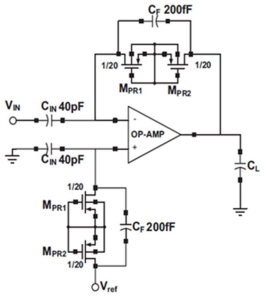

Fig. 1: Basic diagram of a Neural Amplifier (Reproduced from [12])

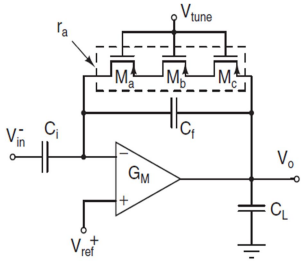

Fig. 2: Schematic of Neural Amplifier (Reproduced from [13])

Gain of the amplifier can be calculated by the ratio of the capacitance values used; one at the input terminal of OTA (Fig. 3) and other as feedback element. Using a capacitor at the input

also helps to remove DC signals and filter out the irrelevant signals. The high cutoff frequency was determined by the value of the capacitor connected in the feedback circuit and the equivalent resistance of the MOS elements which were used in the feedback circuit. The lower cutoff frequency was obtained by the capacitor C_L connected at the load terminal. The capacitor values should be chosen such that the cutoff frequencies are able to cover up the frequency range of the signals produced by neurons. Noise analysis for this configuration can be done by using the circuit for OTA being used in this neural amplifier. Only the transistors in the architecture which lie along the signal path added noise to the signal. Others do not add noise because of common mode cancellation. This configuration used 0.18µm CMOS technology at 27ºC. This amplifier occupied a chip area of about 0.10 mm^2 which was found to be very much area efficient. This amplifier used a very low power for its operation. However noise efficiency was not improved significantly in this configuration.

(ii) Cascode Configuration: Cascode configuration is obtained by connecting a common emitter stage in cascade with a common base stage in case of bipolar junction transistors. This configuration may improve the bandwidth of the amplifier, input and output impedance or the gain of the amplifier. Telescopic and folded cascade amplifiers were used where low noise, large DC gain, high unity gain frequency were required as the important characteristics [14]. Telescopic architecture provided better power efficiency and folded cascade was seen to provide higher output swing. Further changes were done in these architectures to improve the various performance parameters. AC path and DC path were separated and the transistors were split to ensure proper matching [15]. Many other modifications were done but those cascode configurations were not intended to be utilized in neural applications. Sammy Cerida et.al [16] reported a low-noise amplifier which was based on fully differential recycling cascode architecture. This amplifier was based on recycling architecture [17] (Fig. 4) which provided a better gain and bandwidth efficiency.

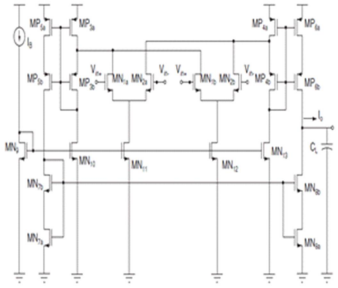

Fig. 3: Architecture of OTA used
(Reproduced from [13])

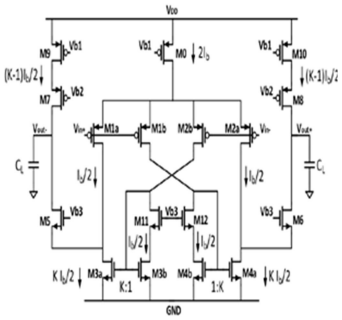

Fig. 4: Fully Differential Recycling Folded Cascode Amplifier
(Reproduced from [17])

The architecture of this amplifier consisted of two current mirrors M3a-M3b and M4a-M4b in which currents were reused; which was not implemented in any of the earlier architectures. These current mirrors improved the gain of this amplifier and bandwidth was also improved. The architecture was observed to have symmetry on both the sides of the amplifier and hence all the parameters were observed to be the same. The symmetry was a result of fully differential architecture of the amplifier. The gain of the amplifier was found to be dependent on the transconductance and output impedance. Parameters for this architecture also depend on the value of K which was termed as the current gain in the recycling path. Depending on the overdrive

voltage, transistors operate in weak, moderate and strong inversion. In this architecture, M3a-M3b, M4a-M4b, M9, M10 were required to operate in strong inversion and a large V_{ov} was maintained to do so. Operating these transistors in strong inversion reduces the thermal noise. Through analysis, they found that value of K should be as small as possible but greater than one. For reducing flicker noise, it was found that value of K should be smaller than one. So K was chosen to be greater and close to 1. The differential pair transistors were operated in weak inversion by keeping the V_{OV} small. These were operated in weak inversion for increasing the transconductance which resulted in increase in gain. The current mirrors used in the recycling path which was realized using the transistors M3a-M3b; M4a-M4b may add a pole-zero pair near to the frequencies relevant. Hence, they may tend to generate stability problems. The pole-zero pair should have been such that it is far from frequencies relevant. This architecture was simulated on a 0.35µm CMOS process and offered a gain of around 42 dB. Power consumption was found to be 66µW and noise efficiency factor of 2.58 was obtained. This work was compared with the previous works and the NEF was improved; however the power consumption was higher than others.

Vahid Majidzadeh et.al [18] reported an amplifier intended for recording activities of multiple neurons at a single point of time. Brain activities can only be studied by analyzing signals from multiple neurons so amplifier designed should be efficient when implemented in multi-channel mode. Therefore chip area occupied by an amplifier becomes an important factor in implementing multichannel amplifier for neural signal analysis. This amplifier was designed on partial OTA sharing technique (Fig. 5) which decreased the area occupied by the amplifier on chip. This sharing architecture OTA also decreased the chip area by sharing the bulk capacitor required for circuit implementation. Power consumption was maintained within the prescribed limits such that it did not have an adverse effect on the brain tissues [19]. Transistor M_{c0} was operated in weak inversion region which ensured that no extra circuitry was required for generating voltages required for the transistor M_{d0} to operate in saturation region. All the theoretical improvements were simulated on a 0.18µm CMOS process. Total area occupied by an array of four amplifiers was found and effective area for one amplifier was found to be 0.0625 mm^2.The gain obtained was 39.4 dB. NEF reported was one of the best values obtained. NEF of 3.35 was achieved for an array of four amplifiers. However, a better NEF could be achieved by reducing the flicker noise contribution by size of the devices. Since it was a multichannel amplifier, crosstalk between adjacent channels was also taken into consideration and efforts were made to reduce it for effective observations. CMRR was measured to be 70.1 dB which was within the desired limits. PSRR of 63.8 dB was obtained for this amplifier.

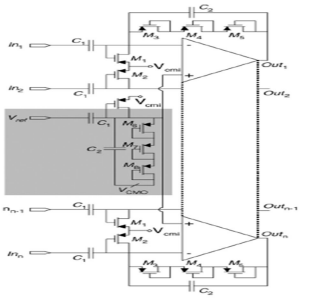

Fig. 5 (a): Partial Sharing OTA Architecture
(Reproduced from [18])

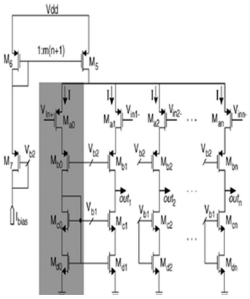

Fig. 5 (b): Circuit of Partial Sharing OTA
(Reproduced [18])

Carolina Mora Lopez et.al [20] reported an amplifier which was multi-channel and consisted of 16 channels and each channel had a low noise fully differential amplifier (Fig. 6). Each

channel had a AC coupling and was using fourth order filter which helped to attenuate the out of band frequency noise and also large DC input offsets were rejected. This amplifier was designed to operate in two modes: one mode was to operate all channels at the same point of time to observe activities of multiple neurons. Other mode was to operate a single channel at a time using a multiplexer. In single channel mode, the channels that were not in use were switched off to save power. Noise analysis of this amplifier considered all the sources in the circuit that could contribute to the noise of the amplifier. Electrodes used were also a source of noise and the electronic circuitry also adds noise to the signal produced by the neurons. Thermal and flicker noise was kept lower than electrode noise, this helped to reduce contribution of overall noise. Design of the amplifier involved various parameters like power consumption, chip area, etc. In this architecture, a single channel was using a fully differential folded cascade OTA. Gain of the amplifier was calculated by the ratio of value of the capacitor placed in the feedback circuit and the value of capacitor placed at the input terminal. The differential pair in this amplifier used PMOS, which were operated in weak inversion. Weak inversion region operation of the transistors ensured that the transconductance was high and hence, it reduced the effect of noise [21]. M4-M5 and M10-M11 were operated in strong inversion to reduce the effect of noise. Flicker noise was also minimized by increasing the size of the transistors. Pseudo resistors were effective in decreasing the chip area because they can realize high resistance values [21].

Noushin Ghaderi et.al [22] reported LNA which used a bulk driven cascade current mirror as load. This used a new telescopic OTA which was found to have a better output swing than other telescopic OTA. Output swing could be increased by reducing the voltage drop on the load. Bulk driven cascade current mirror was used along with telescopic OTA to increase the output swing in this amplifier reported. Gate driven cascade current mirror was also used in some architectures but it had certain limitations which restricted its use to only single stage telescopic amplifiers [23]. BD cascade current mirror (BDCCM) (Fig. 7) was reported to decrease the threshold voltage of the transistors used, as a result of which output swing was found to increase. Architectures with BDCCM as a load had a better noise efficiency and gain as compared to architectures without BDCCM as a load. Noise aspects of the amplifier depended on the transistors used and their transconductance values. The input noise was found to be given as:

$$V_{n,in,eff} = \int_{fl}^{fH} \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 V^2{}_{n,in,OTA}.df \tag{1}$$

Where C_1, C_2, C_{in} were the capacitors used in the circuit of the amplifier. These parts of noise were minimized to increase the noise efficiency of the amplifier. Flicker noise was reduced by using PMOS in the circuit and the thermal noise was minimized by adjusting transconductance values of the transistors used in OTA. This amplifier had a gain equal to 38.9 dB, power consumption of 6.9µw, NEF of 2.2 and output swing of 0.7V.This was capable of amplifying all types of neural signals produced in body.

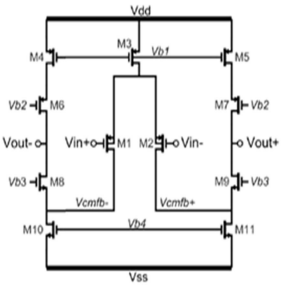

Fig. 6: Fully Differential Folded Cascade Input Amplifier (Reproduced from [20])

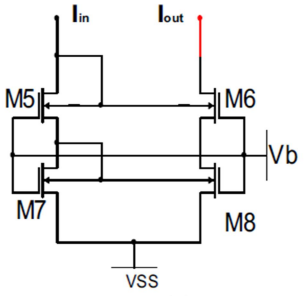

Fig.7: BDCCM (Reproduced from [22])

(iii) Bipotential Configuration: Tan Yang et.al [24] reported an array of neural amplifiers which were found to be suitable for large scale integration. Array of neural amplifiers is capable of analyzing activities of multiple neurons simultaneously and it provides a better understanding of the associated brain disorder if any. This particular configuration used two stage amplifier (Fig. 8) in combination with Current Reuse Complimentary Input (CRCI) technique [25] to achieve the desired performance of the neural amplifier. The first stage used an amplifier which was found to use a capacitive feedback and CRCI technique. This stage achieved good noise efficiency but the Power Supply Rejection Ratio was found to be below desired value. Hence, a second stage was used to improve the value of the PSRR. The second stage used fully differential OTA along with capacitive feedback. A reference amplifier was also used which was common to all the channels and the architecture of this reference amplifier was responsible for significant reduction in power dissipation. Noise was equally coupled to the first stage and the reference amplifier was suppressed by the second stage as a common mode signal and it improved the noise performance of this LNA. Similar to other configurations, large DC offsets should be removed which was done with the help of MOS-bipolar pseudo resistors with high resistance; and on-chip capacitors were also employed. The first stage amplifier and the reference amplifier were matched to each other in terms of gain which helped to achieve a good PSRR and CMRR. Mismatch between the first stage and the reference amplifier gave rise to a poor value of PSRR. Capacitive feedback was used in the first stage and the reference amplifier, which helped to achieve a good gain, accuracy and linearity. Since it was a multichannel amplifier, crosstalk was a major factor which affected the performance and this was minimized using a careful layout. This configuration was found to achieve a NEF of 1.93 which is convincing and a PSRR of 50 dB which is sufficient for typical use. Each channel occupied a chip area of 0.137 mm^2. NEF of this configuration could be further improved by making certain changes to the reference amplifier, which could be shared between more number of channels.

(iv) Reconfigurable configuration: Jose Luis Valtierra et. al [26] reported a 4 mode reconfigurable low noise amplifier. Two types of signals are produced in the brain: action potentials and local field potentials. These signals have different amplitudes and frequency range, so this amplifier was capable of analyzing both the signals produced in the brain. Bandwidth could be selected to analyze these signals separately or at the same point of time. Analog Front End amplifier should have low power consumption to prevent tissue damage, input referred noise should be less than background noise and the architecture should be able to reject DC offsets produced. This amplifier was capable of selecting different modes, which could select different neural signal frequency ranges. It was designed such that its circuit changed (Fig. 9) and value of capacitor was also changed when it was switched from one mode to another with the help of control signals. The four modes which were available were fast ripple mode, action potential mode, local field potential mode and full bandwidth mode. Full bandwidth mode covered both the frequency bands of action potentials as well as local field potentials. Local field potential mode covered the frequency range of action potentials. Local field potential mode covered frequency range of local field potentials. Fast ripple mode covered the high pass pole of action potential range and low pass pole of local field potential range. The differential pairs used were operated in weak inversion region. Noise which was considerable in this architecture was produced by differential pair of the OTA. This was considered to consume the lowest power among the similar reported circuits. If small channel length transistors are used, power consumption can be further reduced. Gain obtained was different for the four modes, which were available in this architecture.

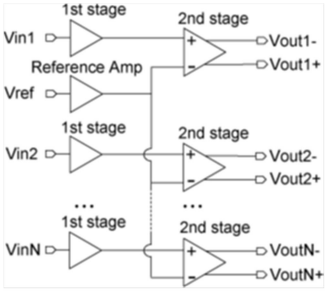

Fig. 8: Multichannel Bipotential Amplifier
(Reproduced from [24])

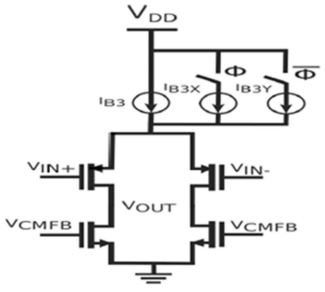

Fig.9: Simple Programmable OTA
(Reproduced from [26])

4 Comparison of Architectures

After analysis of different architecture discussed so far, we compare the architectures with the help of different parameters such as NEF, power, gain, bandwidth, etc. Out of the different architectures studied, we try to find out the best architecture for use in neural applications. As discussed so far, neural signals are weak signals and hence, the gain of the architecture chosen should be high enough to increase the amplitude to a threshold level which makes these signals suitable for analysis. However, the best architecture could be different depending on the real time requirements. Some may require a better noise efficiency, some may require a particular bandwidth depending on the signals to be analyzed (action potentials and local filed potentials), etc. We have considered 10 parameters to analyze the performance of the amplifiers and represented the data in tabular form (Table 1). In this discussion, NEF and gain are considered as dominant aspects. Hence, best architecture has been primarily finalized on the basis of these parameter values.

Table 1. Comparison of LNA Architectures for Neural Amplifiers

Parameter	[12]	[24]	[13]	[26 (a)]	[26 (b)]	[16]	[20]	[18]	[22]
CMOS Technology(µm)	0.18	0.09	0.18	0.18	0.18	0.35	0.35	0.18	0.18
Bandwidth(Hz)	13800	4900-10500	3-164	0.129-590	224-6800	6023	6000	7200	89-7000
Input-referred Noise (µVrms)	5	3.04	5.62	4.2	4.1	1.16	1.9	3.5	2.45
Power (µW)	-	-	-	0.454	0.454	66.03	66	7.92	6.9
NEF (Noise Efficiency Factor)	2.6	1.93	6.33	4.5	1.31	2.58	1.9	3.5	2.2
Gain (dB)	46.2	58.7	31.7	48	48	42.1	33.98	39.4	38.9
Supply voltage (V)	1.2	1	0.8	1	1	3.3	3.3	1.8	±0.9
CMRR (dB)	>66	>45	-	-	-	-	-	70.1	-
PSRR (dB)	>74	>50	54	-	-	-	-	63.8	-
Chip area (mm^2)	0.136	-	0.098	-	-	-	-	0.0625 mm^2	-

5 Conclusion & Future Scope

All the topologies studied so far emphasized on certain fixed parameters which were to be optimized. Future research in this particular area will also focus only on those parameters. Further improvements can be done in these topologies to improve their performance and increase their efficiency in real time application for signal recording and analysis. The discussion can be endless as there are many different architectures that have been suggested so far for implementing LNA in neural signal analysis. LNA in neural applications can be extended by making changes in the existing architectures and simulating them to see their performance

variations. LNA should mainly have a very low noise efficiency factor. As the name suggests, LNA should have low noise; and also it should have a considerable gain, sufficient for neural signal analysis. As per the above discussion, Bipotential amplifier proves to be the best LNA for use in neural applications. It was reported to have a noise efficiency factor of 1.9 and a gain of 58.7 which are the best figures as observed by us.

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Different Input Impedance Matching Circuits for Cascode Common Source LNA with Inductive Degeneration Topology in 45nm CMOS Technology

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***Abstract*— This paper presents various input impedance matching networks that can be used for cascode common source LNA with inductive degeneration topology in 45 nm CMOS technology. We review the matching networks being used and analyze their performance using simulations. Based on our simulation results, we further conclude that T-Matching network is the best input impedance matching network for cascode common source LNA with inductive degeneration topology in 45 nm CMOS technology.**

Keywords—LNA, IoT, SNR, Inductive Degeneration, Cascode

I. INTRODUCTION

It is an era of amazing developments in technologies. Wireless technologies are improving faster than anything. Alternate options are being explored and efforts are being done to design devices that would save energy. The advancements in technology aim to create sustainable future and are focused on creating devices that are reduced in size and consume less resources. Market for wireless technologies is increasing at a rate faster than one can imagine. Emerging wireless technologies require a receiver system that is compatible with the latest methodologies of wireless systems. Wireless technologies demand a receiver system that provides an optimum performance and consumes low power; which makes it suitable to run for a longer duration of time. Low power receivers are in demand because they also felicitate battery less operation [1]. Recent wireless technologies include ZigBee, Bluetooth, Bluetooth low energy (BLE), etc. which aim at providing a solution for obtaining low energy solutions and also making IoT a future possibility in every aspect of life. With brisk increase in communication technology, additional burden of larger integration also follows up. Better performance delivering integrated circuits are in demand with spectacular improvements in technology. CMOS scaling technologies are also improving day by day which is able to provide better performance at a lower cost and lower chip area. These developments in CMOS process technologies have made realizing a system on chip feasible, for use in almost all domains of life [2]. With scaling of technology integration of circuit is more compact i.e., more no of elements can be placed in a smaller area. This increases the complexity of the circuits. Digital circuits can be easily redesigned according to the changes in the CMOS technology. However redesign of analog circuits to cope up with the advancements in technology has become a challenge for the researchers [3]. This paper is organized in 5 sections. Section I gives a brief review about the recent technologies in wireless communication. Section II of the paper discusses about the Low Noise Amplifier (LNA), its importance in wireless communications and its utility in other domains as well. Further in section III, we discuss the design aspects of the LNA with reference to matching networks and other design parameters as well. Section IV is about the simulation results obtained and further in Section V, we select the preferred matching network based on our analysis.

II. LNA IN WIRELESS COMMUNICATION

A. Low Noise Amplifier(LNA)

At the receiver block, the signal needs to be received and processed further which includes filtering the undesired frequencies, amplification of the signal while maintaining a good value of signal-to-noise ratio (SNR). Signal-to-Noise ratio gives an idea of extent up-to which the signal is affected by noise. A large value of SNR signifies good signal strength and low value of SNR signifies poor signal strength. In most of the receiver architectures, first block in the receiver after the antenna is the Low Noise Amplifier [4]. A low-noise amplifier is an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio. It may be preceded by a band select filter in some architectures. LNA is responsible for the overall performance of the receiver to a large extent as it is the first block in the receiver chain and its noise performance dominates the noise performance of the complete receiver. LNA amplifies the signal present at its input and adds a very little noise by the virtue of its components. Hence, it is preferred in many receiver architectures and other domains as well. LNA should provide a high gain, low noise figure, high linearity, low power consumption, etc. LNA's performance is determined by the value of these design parameters [5]. LNA needs to be connected to other components of the receiver system, so input and output impedance should be high enough to prevent loading effect on other components connected. Loading effect tends to decrease the gain of the amplifier as effective load resistance of the amplifier decreases as a consequence of low resistance of the adjacent components. A fully-integrated LNA is the best option. Finally, power consumption is a concern, especially for portable devices. LNA with all parameters perfectly within the limit cannot be designed as trade-off always exists between the different parameters of a LNA. Based on our application area, we need to focus on the parameter to be optimized and accordingly the LNA design procedure is carried out further.

B. LNA in wireless communication

Applications of low noise amplifier involve different frequency ranges but when we want to implement it for

wireless applications, the frequency that is to be considered is 2.4 GHz or a higher frequency than this as well. Wireless communication is carried out using a narrow band of frequencies or single frequency. Hence we do not need to focus obtaining an optimum performance over a wide range of frequencies. However, there are applications which require wideband LNA's i.e., optimum performance over a wider range of frequency. Darlington amplifier proves to be best for applications for wideband performance [6].

C. Applications of LNA

Applications of LNA also decide the components that can be utilized in the circuit design. If we require a system on chip, we should avoid components which occupy larger chip area, etc. LNAs are used in many applications like industrial scientific and medical band (ISM band), cellular telephones, biomedical applications (at low frequency), satellite communications, etc. For biomedical applications, the low noise amplifier should be designed such that the power consumed by it is within the limit because it may increase the temperature of the tissues; and higher temperature may damage the brain tissues.

III. DESIGN PROCESS

The first step in the design of any circuit or system is creating an outline of expected performance of the circuit or the system. Application for which the circuit is to be designed is the most crucial factor that determines the design process. Unless application is specified, the design process cannot be initiated as the application determines the parameters of concern and we need to proceed with the design following those parameters. The trade-offs like impedance matching, choosing the amplifier technology (such as low-noise component) and selecting the low noise biasing conditions are important parameters for designing a low noise amplifier. Apart from this, low power consumption, small chip area and low cost are also desirable [7]. LNA design process can be categorised into 4 major parts that can be listed as: topology, matching networks, transistor selection and biasing [8].

A. Topology

LNA can be implemented using many topologies such as common-gate, common-source, cascode, etc. Out of all these available topologies, most widely used topology is cascode i.e., common source connected in cascade with common gate transistor [9]. This topology provides an improved performance over others and also improved bandwidth. These topologies can further be enhanced with additional circuitry to provide an improved performance. Common- Gate topology provides a highly linear circuit but noise performance of this topology is relatively low [10]. Inspite of a high noise figure, it can be utilized in wireless communication as it satisfies the standards of the wireless systems. Moreover, with the help of different techniques, desired noise performance can also be achieved by this topology.

B. Matching Networks

LNA is generally placed after the antenna which denotes an impedance of 50Ω. For maximum power transfer between two stages, the output impedance of the first stage should be matched with the input impedance of the second stage. If impedance mismatch occurs between the two stages, maximum power transfer will not take place and reflections are ought to occur. Hence, LNA's input impedance needs to be matched with antenna's output impedance to achieve complete power transfer. This can be achieved by using an input matching network that performs this task of matching the input impedance and it is very crucial for LNA's performance. Matching networks also have different topologies and numerous components are available that can provide matching between two stages. However, choosing a proper matching network that enhances the performance of the circuit is a tedious task that needs to be done properly. A change in matching network affects the circuit performance and hence, a comparison can be done to find which matching network is best for our circuit design.

Similar to the input stage, output matching also needs to be accomplished in order to transfer maximum power to the next stage after the LNA in the receiver block. Different output matching circuits also affect circuit performance.

C. Transistor Selection

Proper selection of transistor is crucial for performance of the circuit. Fabrication process also affects the circuit performance to a large extent. Basically, MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is used to realise LNA, along with additional components.

D. Biasing

After the accumulation of the circuit components as desired, we need to provide biasing to give the device a stable operating point. If the biasing provided to the circuit is not able to provide a stable operating point, it will ruin the circuit performance at the desired frequency, and the circuit will become prone to oscillations and this may destroy the circuit completely. Hence, stability analysis is very crucial for a device's proper operation. Many methods are used to provide biasing to the circuit such as resistive divider biasing, current mirror, etc. Out of these methods, we prefer current mirror biasing as MOSFET current mirror tends to reduce the chip area of the circuit and also provides a good stable operating point to our device. After the design process is complete, we need to convert our design into end-product which can be achieved by fabrication of the circuit. Before fabrication process start,s we need to perform simulations and analyze the stability of the circuit in real time.

IV. SIMULATION RESULTS

We performed the simulations in ADS (Advanced Design System) software and obtained the results required. ADS is a tool which is used by RF designers to simulate circuits and analyze their performance before process of fabrication begins. It helps to reduce the cost of device as its properties can be studied before fabrication, saving unnecessary cost of fabrication. Different from other digital circuits, the value of RLC in RF circuits must be extremely precise due to the sensitivity of the frequency response. A slight change of the value of the circuit components such as inductor, capacitor, etc. within the RF circuit can cause a considerable effect that ruins the expected performance. LNA implemented uses a cascode pair in its basic circuit and a tank circuit is used as a load as it is ought to offer better performance than other

available output loads. We simulate the LNA circuit using 3 different input impedance matching networks and analyze the results obtained, on the basis of LNA parameter specifications. Cascode configuration provides better performance than other configurations and using inductive degeneration enhances the noise performance as well as the gain of the LNA [11]. Input impedance matching is achieved using different input impedance matching circuits and the circuits are simulated.

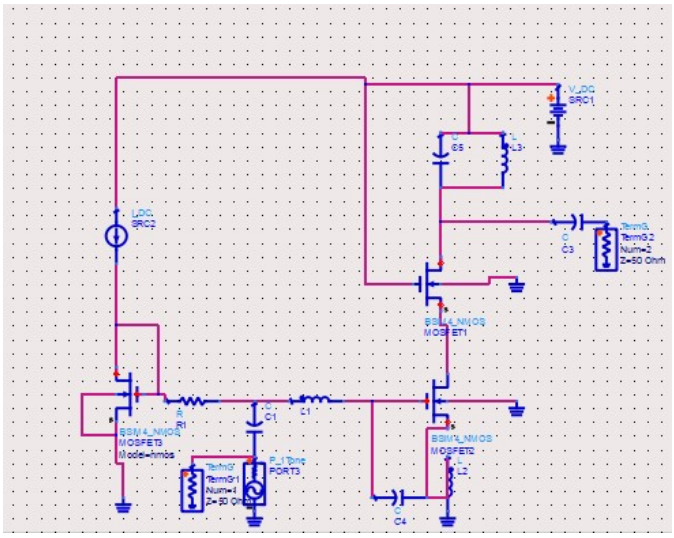

Fig. 1:Implemented LNA

LNA design cannot be perfect in all parameter values a s a trade-off will always exist between the parameters. Input impedance matching circuit can be designed in many configurations such as L matching, T-matching, π-matching, etc. Apart from these configurations, any matching network can be formed using components available that may include inductor, capacitor, transmisson line, stub-matching, etc. For LNA matching, we avoid using matching networks consisting of transmission lines as it may give rise to crosstalk, as the system being designed is going to be fabricated on a chip. Matching networks chosen for analysis are L matching network, T- matching network and third matching network is designed with different configuration than the available matching networks.

A measure of linearity of circuit is obtained by value of its Input Third Order Intercept point (IIP3). A high value of IIP3 implies a high linearity circuit. From the simulation results obtained, we infer that T matching provides a highly linear circuit than the other two combinations.

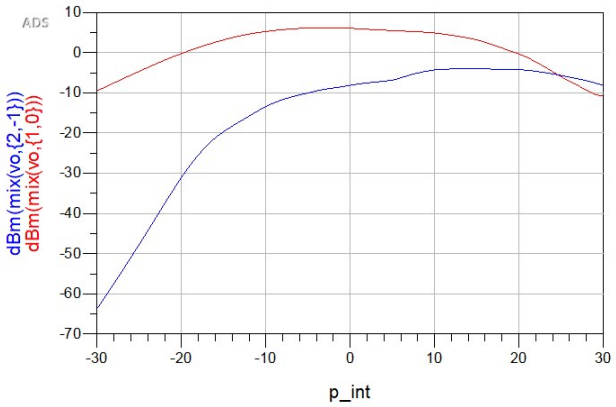

Fig. 2: IIP3 for the LNA circuit with matching network 1

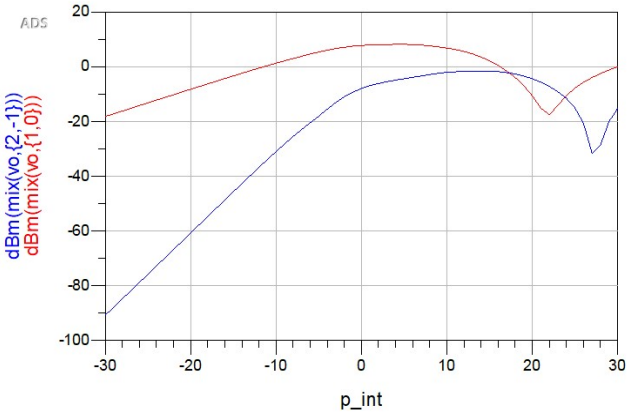

Fig. 3: IIP3 for the LNA circuit with matching network 2

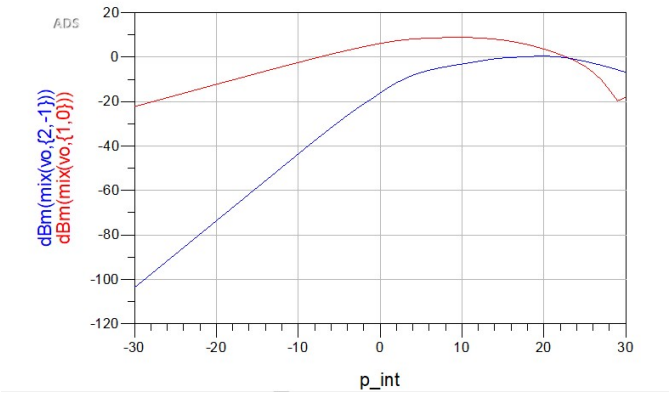

Fig. 4: IIP3 for the LNA circuit with matching network 3

An important parameter in LNA design is the gain offered by the amplifier. In many applications, where the signal to be processed is very weak, gain offered by the circuit is very crucial for the receiver performance. Gain of the system should be sufficiently high so that the effect of noise is suppressed and the SNR maintains a good value. L matching i.e., matching network 1, offers the maximum gain out of the three matching networks. Gain offered by this circuit is sufficiently high with a value of 26.52 dB which is good enough to process signals with very weak amplitudes. Gain offered by matching network 3 was the lowest and hence we conclude that it is not preferable for processing signals which are very weak.

Noise performance of the low noise amplifier is a very critical parameter. As the name implies, the LNA circuit should have a very low noise figure i.e., a good noise performance. It determines the overall noise performance of the receiver system, hence considering this parameter is essential during our design. On the basis of results obtained by simulations, we conclude that the noise figure of the circuit using matching network 2 and 3 is better than using matching network 1.

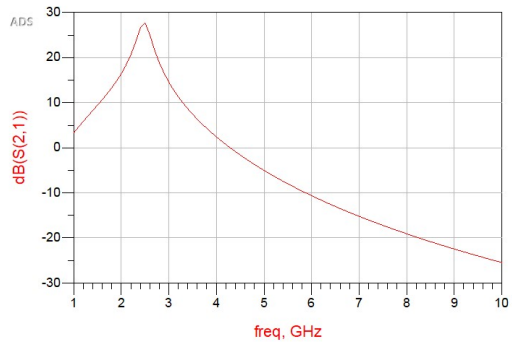

Fig. 5: S_{21} (Gain) of the LNA circuit with matching network 1

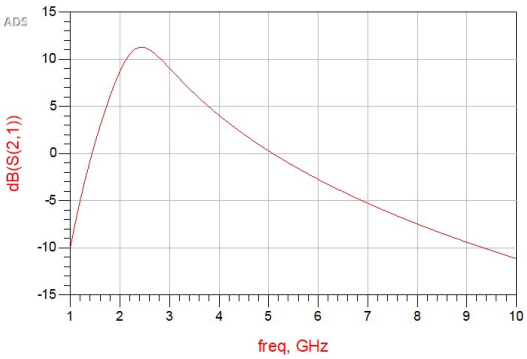

Fig. 6: S_{21} (Gain) of the LNA circuit with matching network 2

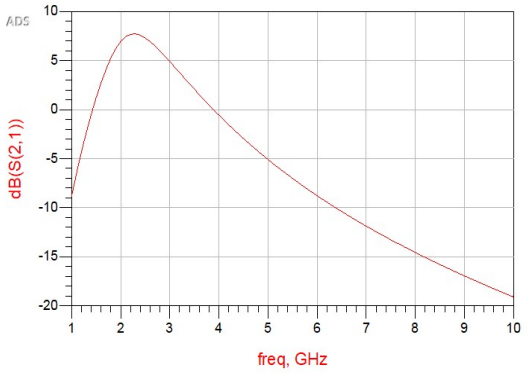

Fig. 7: S_{21} (Gain) of the LNA circuit with matching network 3

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Either of the two circuits provides a good noise performance. Noise performance of the device is determined by the components being used in the circuit design.

V. CONCLUSION

It is very difficult to design a LNA with all the parameter values perfectly within the limits, which creates a restriction on choosing best circuit among given choices. If we require high gain in our system, while compromising with the noise performance, we can adopt L matching network in our design. On the other hand if we want a circuit with better noise performance, we can adopt T- matching network.

Fig. 8: Noise Figure of the LNA circuit with matching network 1

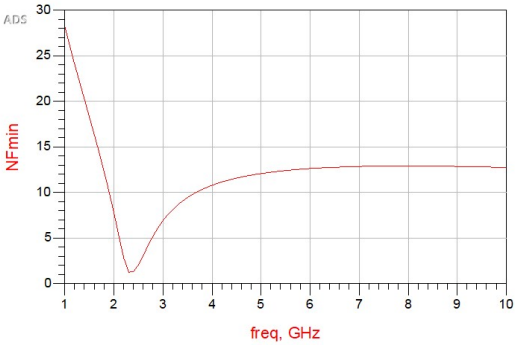

Fig. 9: Noise Figure of the LNA circuit with matching network 2

The results obtained are summarized in tabular form in the table 1.

Table 1: Results obtained for Cascode Common Source LNA with Inductive Degeneration Topology utilizing different input matching circuits

Parameters	Matching network 1 (L matching)	Matching network 2 (T matching)	Matching network 3
Technology	45nm	45nm	45nm
S_{11} (dB)	-12.041	-4.146	-36.5
S_{21}(dB)	26.52	11.281	7.705
S_{22}(dB)	-0.08	-1.202	-1.452
S_{12}(dB)	-51.28	-54.259	-63.25
Noise Figure (dB)	7.464	1.293	1.124
IIP3 (dB)	4.774	9.785	8.765
Power Consumption (mW)	5.45	8.91	9.37

We have simulated and analyzed Cascode Common Source LNA with Inductive Degeneration Topology in 45 nm technology using three different input matching networks and on the basis of the results obtained, we infer that T-matching network provides better overall performance when compared to the other matching networks.

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Cascode Common Source LNA with Inductive Degeneration Topology utilizing Different Output Matching Circuits in 45nm CMOS Technology

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***Abstract*— One of the most essential component of transceivers is Low Noise Amplifier (LNA). LNA is placed at the initial stage of the receivers and hence, it governs the overall performance of the receiver. This paper compares Cascode Common Source LNA with Inductive Degeneration Topology utilizing different output matching circuits. We list the specific application domains of the different circuits analyzed, on the basis of the results obtained through simulations. We further conclude that RLC circuit is the best one to be used as an output matching network in terms of minimum power consumption and highest linearity.**

Keywords— IoT, Wireless, LNA, Cascode, Inductive Degeneration

I. INTRODUCTION

One of the hottest topics of research nowadays is 'Internet of Things' (IoT) i.e., connecting everything to the Internet to make the dream of smart homes come true. Researchers are working in order to design devices which can be made compatible with the IoT standards. Connecting everything to Internet puts an additional constraint on the components that are being designed. Researchers work to achieve best results using minimum resources in order to make a component that is able to cope up with the rapid growth in technologies day by day. Ability to communicate by the means of wireless medium is the most important feature required in the systems nowadays. For this we require a receiver which should be capable of providing an optimum performance when implemented in real-time systems. LNA is generally the first block in most of the receiver's architectures and hence its performance is crucial for the entire receiver system [1]. Choosing an LNA which is best in terms of performance parameters increases the efficiency of the receiver's system. However with expeditious growth in wireless communication industry, manufacturers aim to design a circuit which is able to deliver best results among the already available hardware at present. In case of LNA performance, target is to achieve a low noise figure, high gain, low loss, high IIP3, etc. [2]. RF circuits have created a tremendous scope of research and this comes due to advancements in semiconductor technologies which makes system level integration more flexible. These have also gained popularity due to their low cost which makes RF more attractive technology to work on. CMOS technology advancements have proved to be beneficial for both analog and digital circuits. However redesign of digital circuits for a newer technology is an uncomplicated process. This is not so in case of redesigning an analog circuit for a newer technology. It is a challenge to redesign analog circuits for newer technologies [3]. The paper is organized into 5 sections. Section I being the introduction followed by Section II that gives a brief about LNA in wireless communication. Further we move to Section III that discusses the topologies prominent for implementing LNA and in Section IV, we discuss the results achieved by us during simulations. In the last section of the paper, we summarize our results and state the application areas depending on the topology being discussed.

II. LNA IN WIRELESS COMMUNICATION

In recent times, focus on technologies consuming low-power has increased and these are being utilized in wireless communications as well. Low power consumption, high gain, low noise figure, etc. are the constraints that are the most important for implementing LNA in wireless communication. Apart from bluetooth communication, low power wireless devices are in demand for other application areas as well. These application areas include neural signal analysis, medical applications, etc. [4]. Since LNA determines the receiver performance, designing a LNA with consideration of all parameters within specified limits presents a demanding situation for all the researchers. Most of the LNA's are generally single band LNA i.e., they are designed to operate at a single frequency. However multiple band LNA's are also being introduced i.e., they are capable of operation at more than one frequency. Operating a single LNA over multiple frequencies increases the complexity of the circuit but it also makes it versatile for multi-standard applications. However LNA's are reported that operate at two frequencies i.e., they are dual band LNA's. Multiple band LNA's are less common as achieving optimum performance at multiple frequencies increases the overheads as well as increases the cost of the LNA. Moreover, it also results in increase in power requirements of the circuit as well as increase in the chip area occupied by the circuit [5]. If we wish to design a broadband LNA, we generally use a single transistor which is being used in common-source configuration [6]. Darlington amplifier is used in case of broadband applications i.e. optimum performance over a larger bandwidth [7]. Wireless communication is generally limited to short distances as compared to other forms of communication. Designing a LNA for short distance communication (up-to 10m) is a smooth process in comparison to designing a LNA for long distance communication (more than 10 m). LNA for long distance communication where the distance between the transmitter and receiver is more than the specified range requires high sensitivity which in turn leads to increase in complex design process. LNA for short distance communication where the distance between the transmitter and receiver module is less than 10 m drives the next block into compression because of the signal at the input being strong in amplitude. This signal leads to an output signal which is distorted. In this scenario we need a LNA that can overcome this problem by

suppressing the input signal to prevent this condition [8]. Bluetooth is also a form of wireless communication which is more prevalent and everybody is more familiar with this form of wireless communication. For Bluetooth communication also, we need a transmitter and receiver and the receiver end utilizes an LNA as the first block of the system. LNA for this particular application will have different characteristics than the LNA for other forms of communication as LNA parameters depend on the application for which they are being designed. More specifically a LNA for Bluetooth applications should provide a higher gain and consume less power than others. Bluetooth Low Energy (BLE) focuses on reducing the power consumption of the circuit and is apt for IoT applications. BLE devices can work for longer hours as they consume less power.

III. LNA TOPOLOGIES

LNA's utilize configurations that were used traditionally to design amplifiers. Other than configuration, additional steps need to be taken to achieve the desired performance. The desired performance can be obtained by introducing a change in the biasing network or it can be through a change in matching networks being used. Most common LNA topologies are common-gate, common-source, cascode, etc. Each of the above topology has its own advantages and disadvantages. In-spite of their own merits and demerits, the cascode configuration is the most common configuration used for implementing LNA. Common source configuration can be used with resistive load as well as inductive load. Resistive load offers less gain and also it does not provide proper matching, which at higher frequency creates a hindrance to the proper functioning of the circuit. Inductive load overcomes the disadvantages offered by resistive load configuration. In the common source configuration, the inductor placed at the output node is responsible for output matching. We also need to provide input matching network to match the input impedance of the amplifier with that of the antenna. In this configuration, a capacitor is also connected across the gate and drain of the transistor which denotes the gate-drain overlap capacitance. The effect of the capacitor is nullified by using an inductor in parallel with the resistance. Since the capacitor is of smaller value, the inductor that should be connected across it should be of a higher value. Using an inductor of large value introduces parasitic capacitances at the ouput node and input node of the circuit and thus degrades the performance of the amplifier. Hence, this topology is rarely used in practical LNA design. Common source stage with resistive feedback is also a possible topology that can be used to implement low noise amplifier. In this topology, a resistor is connected across the output and input nodes i.e., R_F provides a feedback from the output node to the input node. R_F sends a current signal as a feedback to the gate terminal of the transistor depending on the voltage at the output node. This topology does not suffer from the drawbacks as that of common source stage with resistive load. Gain offered by this topology is not restricted by the supply voltage as in case of resistive load. The trade-off between the gain and supply voltage is overcome in this particular topology and hence it is preferable over common source stage with resistive load. Resistive load in case of any transistor configuration i.e., common source or common gate, always creates a trade-off between the supply voltage and the gain of the circuit. Hence, resistive load is not preferred in any practical application, unless required.

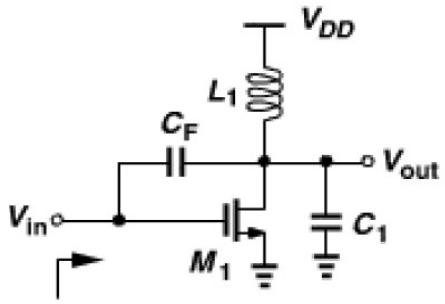

Fig. 1: Common Source Stage in presence of capacitance (reproduced from [9])

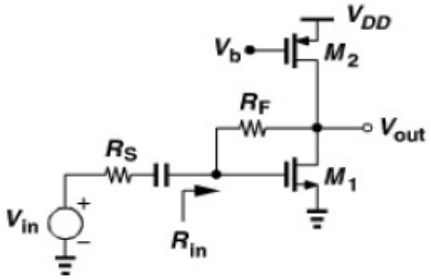

Fig. 2: Common Source Stage with resistive feedback (reproduced from [9])

Apart from common source configuration, common gate configuration can also be used to implement LNA for practical applications. Low input impedance offered by this configuration makes it suitable for practical applications. Inductor is used as a load in this configuration. If the inductor possesses ideal characteristics, it can be connected across the output terminals but if a practical inductor is to be used, a resistor should also be connected across it to model the losses offered by the inductor. Noise performance of this configuration is not optimum as it accounts for a lower gain i.e., better noise efficiency will result in a lower gain. Most widely used configuration is cascode common source stage. This configuration tries to overcome the drawbacks of the topologies discussed so far by introducing certain changes in the circuit. In this configuration, we use active devices to achieve input impedance matching of 50Ω, which limits the noise contribution that was added due to the passive devices in the circuit. One method to achieve this is inductive degeneration that is most widely used in LNA design. The value of the degenerative inductor is crucial in this design process. To achieve an impedance matching of 50Ω, an inductor having a value of about 50 pH, is to be realized. It is difficult to realize an inductor with this value accurately. Hence, in order to realize this inductor, a different method is used. If we wish to achieve impedance matching using degenerative inductor, we need to reduce the f_T of the transistor which can be done by adding an additional

capacitance across the MOSFET terminals. When we start the design process of the cascode LNA, we need to find out the value of the degeneration inductor according to the design specifications.

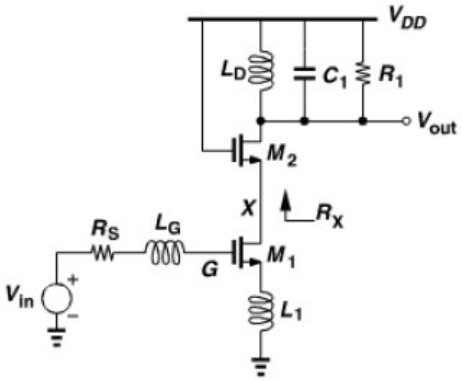

Fig. 3: Cascode Common Source Stage with Inductive Degeneration (reproduced from [9])

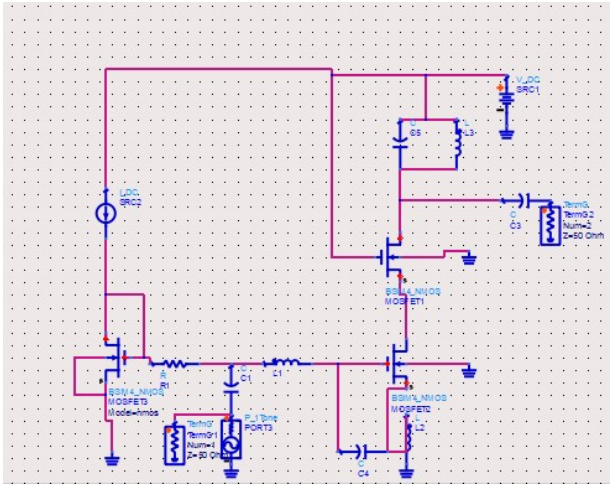

Fig. 4: Implemented LNA

Many other configurations also exist for LNA implementation but they are not widely used in practical applications as their design process is much more complex than these basic configurations. These topologies can be used if we want to design an application specific LNA. Noise cancelling LNA's are available i.e., their design process focuses on improving the noise performance of the LNA, etc.

IV. SIMULATION RESULTS

We can use different circuits as load in our low noise amplifier design and these circuits play a major role in the performance of the low noise amplifier. We have implemented four major output matching networks in our LNA and compared the simulation results obtained to find out the best output matching network for LNA circuits. We observe a trade-off between the various parameters of the LNA. Change in one parameter of the LNA affects the other parameters as well. We observe a trade-off between the gain of the LNA and the linearity of the circuit. We desire a high gain LNA; however a higher gain affects the linearity of the subsequent stages of the receiver. Hence, we need to confine our gain so that the non-linearity of the subsequent stages of the receiver does not become prominent. Generally a pre-select filter is placed before the LNA. This filter is sensitive to the impedance matching at its output terminals [10]. Hence, in our circuit design, we need to focus on impedance matching networks at the input terminal also. Cascode configuration implemented by us incorporates inductors and capacitors to provide this input matching. Inductor placed at the input terminal and the inductor placed at the source end of the MOSFET along-with the capacitance (C_{gs}) creates an input matching network for our configuration. Using a cascode configuration also has a benefit of providing required isolation between the input and output nodes. Isolation is necessary in circuits so that the signals from the output do not leak back to the input terminal. If proper isolation is not provided, signals may leak back and this creates a hindrance in proper operation of the circuit.

Using a resistance as a load is the most common practice but is does not prove to be the best output matching network based on our analysis. When resistance is used as a load, it is observed that it does not provide proper matching and maximum power is not delivered to the output node, which in turn results in more reflected power and losses.

$$|A_V| = g_m.R_D \qquad \text{..... (1)}$$

After substituting the values, we get the gain in terms of voltages as:

$$|A_V| = 2.VRD$$
$$V_{GS}-V_{TH} \qquad \text{.....(2)}$$

Gain obtained in this circuit is lower as it depends on the supply voltage and the voltage drop across the resistance. For new technologies, we work on lower voltages and hence, the gain is further reduced if we use resistance in our circuit. On the basis of results obtained, we conclude that using R as a load in our circuit is not preferable as it ought to increase the noise figure of the circuit as well as it is observed to provide a low value of IIP3. High frequency operation of the circuit is also restricted as the resistance does not provide proper matching at frequency of interest. Thus, this circuit does not provide optimum performance. Using an inductor as a load, overcomes the disadvantages offered by resistive network. Inductor sustains a lower voltage drop than a resistor and hence it can operate at a lower supply voltage as well. Moreover, inductor resonates with the capacitor at the load to offer matching at higher frequency. Value of the inductor is chosen first and then accordingly, the value of the output or load capacitance is chosen such that it will provide matching for desired frequency. Hence, using an inductor in our circuit solves the issue of obtaining matching at our frequency of interest. Using L as a load in our amplifier design overcomes the disadvantages that are observed in circuit with resistance as a load; and it is better to use an inductor in our circuit than using resistance because using a resistance limits the circuit performance and may not deliver the required results.

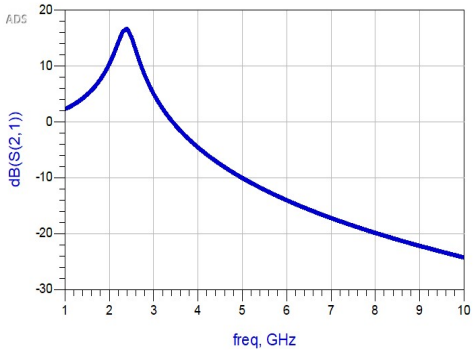

Fig. 5: Gain (S_{21}) obtained when R is used as load

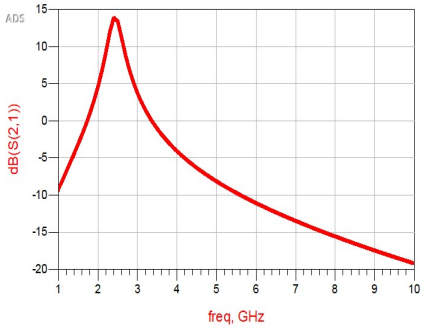

Fig. 6: Gain (S_{21}) obtained when L is used as load

Using LC as a load provides even better results as the inductor being used to realize the circuit is assumed to be a real inductor. Practical inductors suffer from losses which can be modeled by placing a resistor in parallel with the configuration of L and C. It can also be verified from the results obtained during simulation that when a practical inductor is being used in our circuit, the results get downgraded as the inductor being used to achieve output matching is not ideal inductor. Practical inductor properties are also being considered.

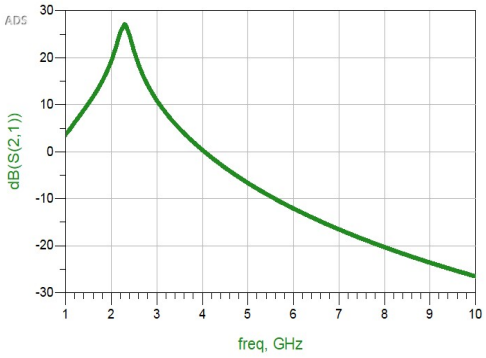

Fig. 7: Gain (S_{21}) obtained when LC is used as load

We know that ideal characteristics never exist. We should prefer the configuration that takes practical aspects into consideration. Using circuit design that is more close to the practical values, is always more realistic to use, as it always provides a better understanding of the real time performance of the circuit. Design process following practical aspects always yields results which are more close to real-time performance of the circuits.

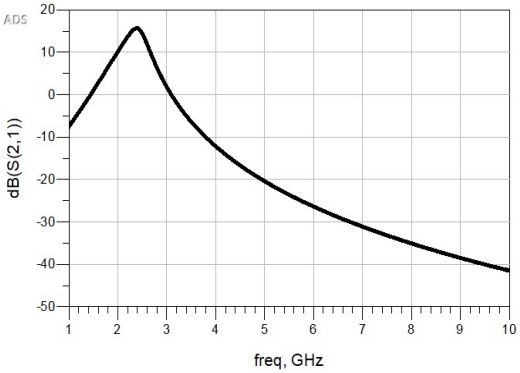

Fig. 8: Gain (S_{21}) obtained when RLC is used as load

We summarize the results obtained in tabular form. However, we compare the performance only on the basis of the gain provided by the circuit. Other parameters can also be used to compare different circuits; and analyze their performance on the basis of parameter values obtained. We need to make a choice of optimizing only one design parameter, keeping others at stake. While implementing these circuits practically, wire bound inductors can be used to realize the given inductance values. Using these inductors reduces the chip area occupied by our circuit design but at the cost of an additional overhead of placing the inductor off-chip rather than integrating on chip [11]. LNA design involves higher level of integration with minimum cost but it also creates a challenge to achieve a better noise performance. MOSFET is being used to implement LNA which possesses a noisy nature; and the noise sources in the MOSET are many. Dominant noise sources are channel noise, gate noise generated due to distributed gate resistance of the MOSFET, etc. These sources degrade the noise efficiency of the LNA. These can be controlled by properly choosing the size of the transistor which provides minimum noise figure. Cascode LNA with inductive degeneration configuration is ought to provide better noise performance and higher gain as compared to other configurations [12].

V. CONCLUSION

We cannot come to a conclusion stating that a particular circuit proves to be the best in terms of all parameters. Every circuit design possesses its own pros and cons making it suitable for one application and not suitable for a different application. This comes forward as a consequence of trade-off between the parameter values of LNA, which makes it a bit difficult to design a circuit with all values perfectly within the limits. On analysis of the results obtained after simulations, we can see the fact come true that there is always a trade-off between the LNA parameters. We observe that one circuit is suitable for application requiring high gain while other circuit is suitable for an application where low noise figure is required. Henceforth, every circuit has its own utility in one application or the other. We need to make a preference in terms of which parameter needs to be optimized and proceed with that aim to design.

Table 1: Results obtained for Cascode Common Source LNA with Inductive Degeneration Topology utilizing different output matching circuits

Parameter	R as load	L as load	LC as Load	RLC as Load
S_{11} (dB)	-13.44	-12.79	-12.041	-14.58
S_{22} (dB)	-11.26	-0.006	-0.08	-19.5
S_{12} (dB)	-47.44	-50.96	-51.28	-50.02
S_{21} (dB)	16.65	13.91	26.52	15.84
Noise Figure (dB)	7.802	8.419	7.464	7.784
IIP3 (dB)	7.023	4.026	5.243	9.783
Power Consumed (mW)	2.95	2.51	5.011	1.98

If we restrict our analysis by considering the gain of the system, LC as a load is observed to be the best design as it offers the maximum gain out of all the above configurations. Even RLC as load offers a sufficient amount of gain. Both these configurations are considered suitable to be utilized in any low noise amplifier design. If we desire a circuit which is highly linear, we need to consider IIP3 value of the circuit. For applications which require a highly linear amplifier, RLC can be utilized as the output matching network as it is observed to provide a higher value of IIP3. Based on our results, we also conclude that if we want to restrict the power consumption of the circuit, we should utilize RLC network in our circuit design, which is observed to consume less power as compared to others. Application specific LNA's are designed by optimizing one parameter and keeping others in the specified limit as trade-off cannot be ignored completely.

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APPENDIX – II

CERTIFICATES OF PUBLICATIONS

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Venue: **Institution of Electronics and Telecommunication Engineers, 62 Indiranagar, Erandwane, Pune, Maharashtra, India on 12th November 2017**

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Diksha Singh

Department of Electronics & Communication Engineering, Delhi Technological University (DTU), Delhi, India

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4th International conference on Science, Technology & Management (ICSTM-2017)

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Certificate of Presentation

This is to certify that

Diksha Singh

Department of Electronics & Communication Engineering, Delhi Technological University (DTU), Delhi, India

Presented a paper Titled as

"LNA for Neural Applications"

in the conference organized by Conference Info in association with Academic Science on 12th November 2017

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Dr. K. Agarwal
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Ajay Kumar Garg Engineering College, Ghaziabad

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This certificate is awarded to Ms./Mr./Dr./Prof ....DIKSHA SINGH.....

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He/She has presented a paper entitled ....LOW NOISE AMPLIFIER IN BLUETOOTH AND BLUETOOTH LOW ENERGY (BLE) (Best Paper).....

Prof. (Dr.) P. K. Chopra
Convenor & HoD,
ECE Department

Rkagarwal

Dr. R.K. Agarwal
Director

Springer CCIS

ICICCT-2019

jims Sector - 5, Rohini, Delhi

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Design & Implementation of Low Noise Amplifier in Neural Signal Analysis

at 4th International Conference on Information, Communication & Computing Technology (ICICCT - 2019) in collaboration with Springer CCIS and Computer Society of India, held on 11th May 2019 conducted by Jagan Institute of Management Studies (JIMS) Sector-05, Rohini, New Delhi, India.

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has presented a paper titled

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at the 4th International Conference on Communication and Electronics Systems (ICCES 2019) organized by PPG Institute of Technology during 17-19, July 2019 at Coimbatore, India.

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