DESIGN & IMPLEMENTATION OF CMOS LNA FOR WIRELESS APPLICATIONS

A Dissertation

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In
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Candidate's Declaration

I GAURAV SRIVASTAVA, Roll No. 2K17/MOC/12 student of M.Tech (Microwave & Optical Communication), hereby declare that the project Dissertation titled "Design & Implementation of CMOS LNA for Wireless Applications" which is being submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology in Microwave & Optical Communication, is original and bonafide record without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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Certificate

I hereby certify that the Project Dissertation titled "Design & Implementation of CMOS LNA for Wireless Applications" which is being submitted by GAURAV SRIVASTAVA, Roll No (2K17/MOC/12) Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a bonafide record of the project work carried out by the student under my supervision. To the best of my knowledge, this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Acknowledgement

Someone wise had once said, “If the destination is beautiful, don’t ask about the pains of the journey, and if the journey is beautiful don’t ask to which destination it will lead.” And I have a lot of people to thank who have made my study journey and destination both beautiful. This dissertation is the result of work of almost two years, whereby I have been accompanied and supported by many people, to whom I would like to express my gratitude.

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The two people to whom I believe I owe all and saying just ‘Thanks’ will be insufficient, are my parents. I would like to thank them and my siblings for believing in me and supporting me.

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Abstract

In recent years the advancement in the wireless communication technologies especially in the RF range including all the major applications like (satellite communication, mobile communication, IOTs). The basic characteristics of the RF transceiver system is determined by the major components which includes mixer, LNA, Filters, ADC and DAC converters. However, the properties of RF transceiver is mainly affected by the designing of Mixers and LNA. In this thesis LNA for 2.4 GHz ISM band that is (Industrial, Scientific and Medical band) for RF transceiver system is designed and implemented. The basic parameters of LNA includes low power consumption, small supply voltage and low chip area. Apart from this LNA should have high matching network for (minimum return loss) , low noise figure, optimum gain and high linearity. The LNA is implemented in 180 nm and 45nm TSMC Technology on Advance Designing Software (ADS). The LNA is implemented using major topologies like Common source, Common gate and Cascoded Topology. The mode of implementation of LNA with CS or CG depends upon the mode of applications. The most common and efficient topology is common source with inductor degenerate cascoded with Common gate topology. The LNA attains the NF of 1.23 and third order intercept point (IIP3) (measure of linearity) of 56.85 dBm which is best so far.

List of Published Papers

1. **Malti Bansal, Gaurav Srivastava, "LNA for Biomedical Applications," International Journal of Engineering Technology Science & Research (IJESTR) ISSN 2394-3386,Volume 4 pp- 295-300,Issue 11, November 2017.**
2. **Malti Bansal, Gaurav Srivastava, " High Linearity and Low Power Cascode CMOS LNA for RF Front-End Applications," in proceedings of Third International conference on Intelligent Computing and Control Systems(ICICCS-2019),pp-1-4.**
3. **Malti Bansal, Gaurav Srivastava, " Design and Implementation of LNA for Biomedical Applications", in proceedings of International Conference on Intelligent Computing ,Information and Control Systems(ICICCS-2019),pp-151-160.**

List of Communicated Papers

1. **Malti Bansal, Gaurav Srivastava, "High Linearity High Stability Cascode CMOS LNA for RF Front-End Applications.**
2. **Gaurav Srivastava, Malti Bansal, "A High Linearity Shunt Capacitive Feedback LNA for Wireless Applications**

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LIST OF ABBREVIATIONS

Abbreviations	Full Form
VLSI	Very Large Scale Integration
RFIC	Radio Frequency Integrated Circuits
CDMA	Code Division Multiple Access
GSM	Global System for Mobile Communications
LAN	Local Area Network
LTE	Long Term Evolution
ISM	Industrial, Scientific and Medical
RF	Radio Frequency
IC	Integrated Circuits
LNA	Low Noise Amplifier
ADC	Analog to Digital Converter
IIP3	Third Order Intercept Point
SNR	Signal to the Noise Ratio
IR	Infrared Radiations
AM	Amplitude Modulation
SSB	Single Side Band
QPSK	Quadrature Phase Shift Keying
QAM	Quadrature Amplitude Modulation
BJTs	Bipolar Junction Transistors
MOSFETs	Metal Oxide Semiconductor Field Effect Transistor
FET	Field Effect Transistors
WSN	Wireless Switching Network
ITU	International Telecommunication Union
NFC	Near Field Communication
GHz	Gigahertz
CCRLNA	Complementary Current Reuse Low Noise

	Amplifier.
CMRR	Common Mode Rejection Ratio
OTA	Operational Transistor Amplifier
FIFO	First Input First Output
FPGA	Field Programmable Gate Array
DSP	Digital Signal Processor
CMOS	Complementary Metal Oxide Semiconductor
SOC	Silicon on Chip
UWB	Ultra-Wideband

CHAPTER 1 INTRODUCTION

1.1 BACKGROUND

The need of wireless communication is pushing many VLSI Designers to continue research in RFICs design and transceivers systems. Different wireless standards CDMA ,GSM, wireless LAN(IEEE 802.11a),Bluetooth, Zigbee, wimax and LTE are operated at different frequencies with different modulation methods which has exponentially increased the use of wireless application devices. The concept of IEEE 802.15.4 provides data rate of 250kbps over a distance of 10m.The band of 802.15.4 corresponds to the license free radio band which are available all across the globe. The 2.4 GHz (ISM band) or unlicensed band are the internationally reserved radio spectrum intended for scientific ,medical and industrial requirements. Nowadays, wireless devices are designed keeping important parameters like compact size,less power dissipation and less cost.[1] Current mobile phones and handsets having RF transceiver system consisting of complex circuitry includes amplifiers, mixers, oscillators fabricated on a single chip . Thus, occupying a large chip area on a single IC and consuming more power so, For controlling these parameters single wideband RF front end devices supporting all wireless communication standards are favoured. Therefore, designing of LNA plays a crucial and important role in determining the performance of an RF transceiver system.

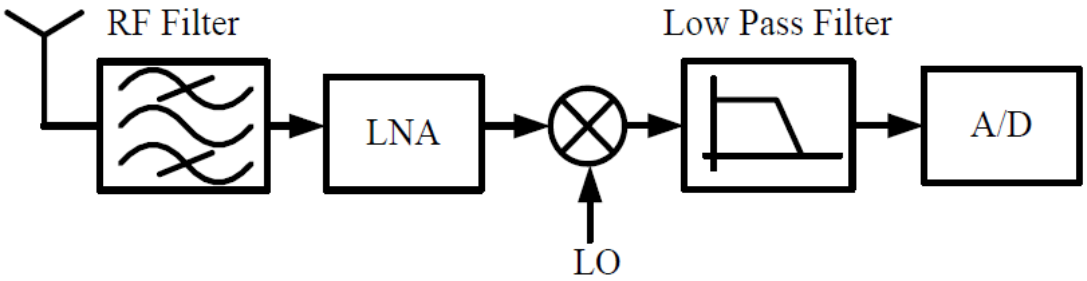


Fig 1.1 Block Diagram of RF Transceiver System

All RF transceiver systems are being integrated on a single chip consisting of hardware components and wires having parasitic effects [2]. The receiver having such effects are called as universal receiver. Ideal RF transceiver system cannot be designed because of its tough designing requirements of (ADC) (Analog to Digital converters). the main components of ADC consist of mixers and LNA. The LNA[3] are calibrated on the basis of noise figure, gain ,linearity and IIP3 parameters. Hence, LNA plays a important role

in any RF receivers. The design of LNA is still a challenging task. Presently , the amplifiers designed for specific wireless standards consumes more power and is having a high cost.In fig 1.1 [2] the system consist of RF filter which filters frequency of specific range the LNA used for amplifying the signal by adding a very little noise to the system. Since the system cannot be the ideal one therefore LNA adds very little noise and SNR obtain is approximately equals to 1. The local oscillator causes the up conversion or down conversion of the frequency. The low pass filter selects the required frequency. In addition[4],LNA is matched to the output of the filters to prevent the back and forth signal reflection between the LNA and antenna, Other parameters in designing of the LNA includes topologies with efficient input matching, biasing circuits, source degenerate feedback circuit and output matching circuits. Further, designing of LNA involves resistors, inductors and capacitors circuit theory.

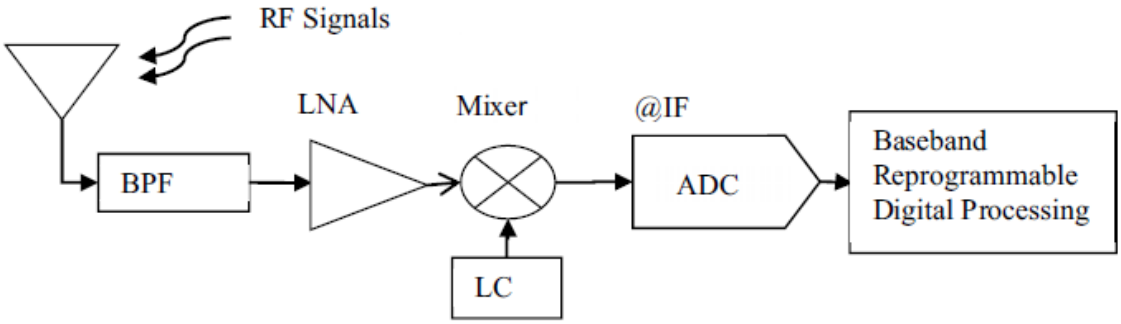


Fig 1.2

The above figure represents designing of LNA for universal RF receiver which is a difficult process. But the universal receiver has the key advantage over the superhetrodyne receiver such as low complexity, no image frequency as compared to superhetrodyne receiver. [5]The RF receiver is implemented using digital and analog. The components like mixers and filters are replaced by digital counterpart but these are found to be having high sampling rate and high SNR, therefore the SNR of the input signal need to be increased. Analog RF receiver [3] is implemented by the method of discrete fourier transform between the antenna and digital signal processor. A software defined ratio selects (SDR) a required frequency from channel bandwidth but system still suffer from the problem of high sampling rate.

The RF module stands for radio frequency as the name suggests. the range of frequency for RF module ranges from 30 KHz to 300 GHz. the information is carried in the form of

digital data represented as variation of amplitudes in carrier waves. This type of modulation scheme is called as amplitude shift keying (ASK). The other modulation schemes consist of frequency shift keying (FSK) phase shift keying(PSK) in which frequency and phases are varied. The modulation method carries the actual information in the form of audio,video or data. the receiver need to perform number of actions so that the information can be processed and deciphered. Receivers need to perform effectively even in the presence of noise and interfering signals. Therefore, selectivity and sensitivity are the important characteristics of the receivers.

Transmission through RF is more convenient then IR mode due to many reasons. signals through RF are capable of travelling long distances they can even travel with the obstruction between the transmitter and receiver. these are generated at high frequency so highly directive and strong at specific frequency. The IR mostly operates in line of sight mode so they get affected by the obstruction in there path. The IR emitting sources are not as effective as RF module.

The RF Transceiver module consist of RF transmitter and RF receiver. The transmission and reception takes place at specific frequency the RF transmitter receives serial data and transmit wirelessly through RF antenna. The transmission occour at a rate around 1-100(kbps). Depending upon the mode of frequency band and sampling rate. The data transmitted at the receiver is at the same frequency as that of the transmitter.

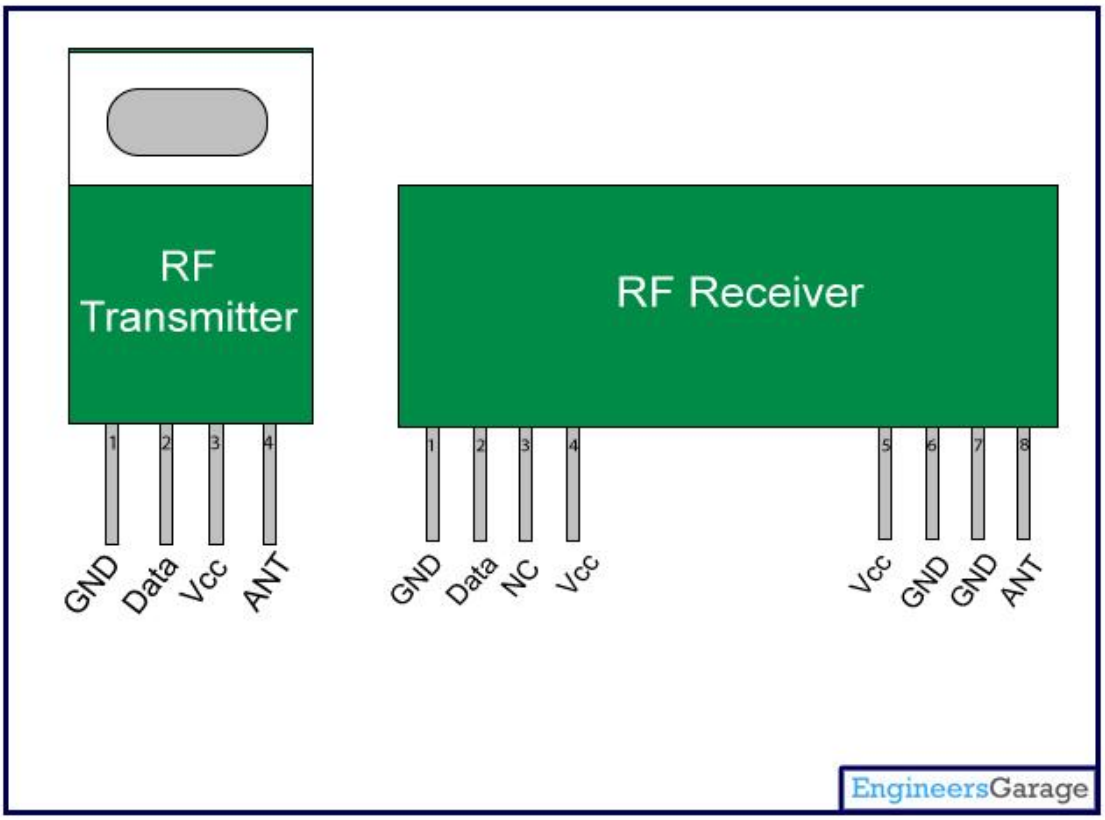


Fig 1.3 RF Transceiver System

1.2 TYPES OF RF RECEIVERS

a)**Tuned Radio Frequency(TRF) Receiver-** the mixed signal obtained from antenna is filtered extracting the desired signal. It consisted of three stages 1. Filtering 2. Tuning 3.Selectivity provided at the Radio frequency stages. Previous TRF Receivers used crystal sets having tuned network consisting of numbers of coils tuning in this stage is provided by simple crystal or diode detector. It consisted of three stages

1.)Tuned Radio Frequency Stages- it consists of one or more amplifying tuning stages .

2.) Signal Detector- enabling extraction of the audio signals from amplitude modulation. the system consisted of a envelope detection and diode for rectifying signal.

3.)Audio amplifier Stage- Audio stage to provide audio amplification.

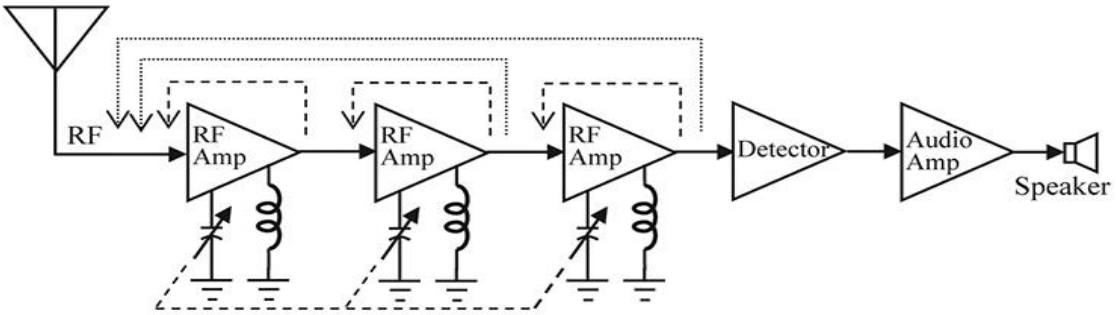


Fig 1.4 Tuned Frequency Receiver (TRF)

b.) **Regenerative Receivers**-it consisted of small number of valves or tubes providing high level of gain and selectivity. the main supply was batteries therefore minimising the number of stages was key. the positive feedback in the receiver circuit increased the gain and selectivity of the system. The received signal is in same phase with the input signal which increased the gain by 1000 or more which causes the quality factor to be multiplied thus, circuit have high selectivity.it consist of three stages 1.) **AM Reception** 2.) **Morse/CW reception** 3.) **SSB Reception.**

c.) **Super regenerative Receiver-** the super regenerative receiver works on regeneration of the stage further.it consist of second low frequency oscillator that quenches the regenerative loop of the main RF oscillation. It works around audio range of 25 kHz to 100 KHz. Although the gain of the amplifier is fixed some of the output is fed back to the input node in phase. It consist of negative resistance reducing the overall resistance of the circuit and quality factor of the circuit is also improved. The quenching oscillation causes RF signal to build up to a very high value.

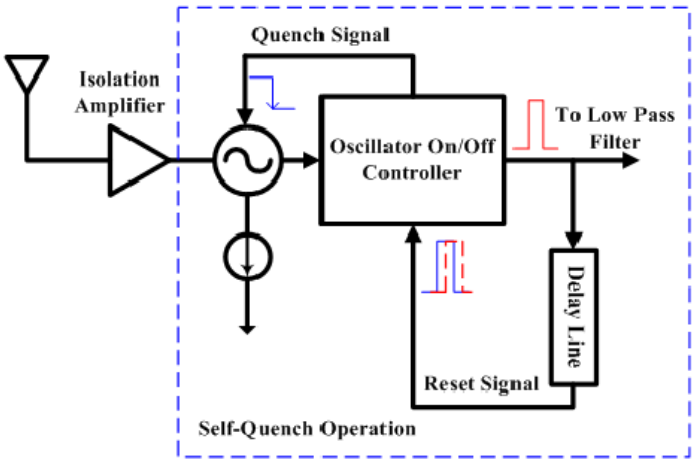


Fig 1.5 Super Regenerative Receiver

Super Heterodyne Receivers-The superheterodyne receiver involves the process of mixing of two signals together. the up conversion and down conversion results in the modulation of the signal. the mixing of RF and local oscillator frequency results in infrared frequency(IF) frequency and varying the frequency of the local oscillator causes the tuning of the circuit to different frequencies.it suffers from the problem of image frequency in the IF stage which is removed by selecting only required range of frequency. Therefore, good image rejection ratio is one of the key features of radio receivers.

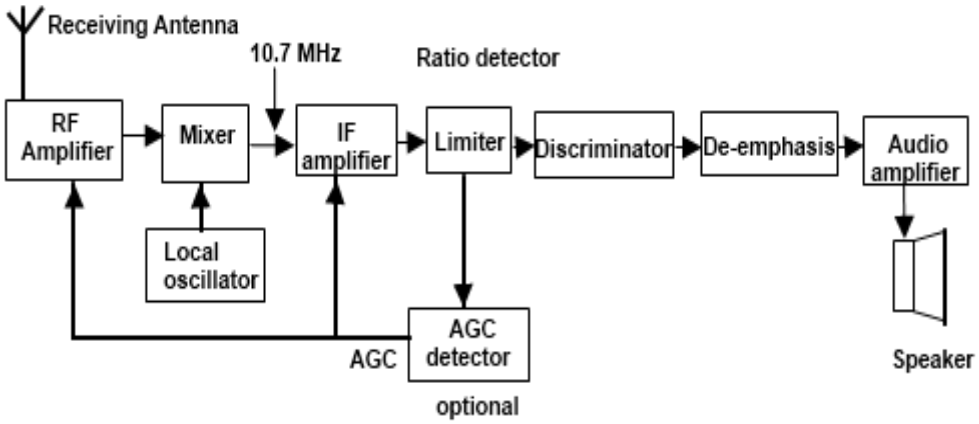


Fig 1.6 Super Heterodyne Receivers

Direct Conversion Receiver- This type of receiver are based on radio formats for converting signals directly to the baseband frequency. The previous method used AM, FSK modulation methods for transmission of the signal but now digital communication transmission method PSK , BPSK ,QPSK methods are used for transmission of the message signal the IQ demodulators of QPSK takes the advantages over PSK and QAM scheme.

Many of theses widespread radio receivers are used today. Each radio receiver has its own characterstics that leads to a particular application.

1.3 AMPLIFIER BASICS

An amplifier is a general term which describes a circuit producing an increased or amplified version of an input signal. However, all amplifier circuits are different based on the modes of operation and circuit configuration[6]. In electronics, designing of an

amplifier starts from small signal amplifier at low frequency having the ability to amplify a relatively small input signal.for eg. Transducer used in microphones, power amplifier, sensors in photo-devices amplifying a signal into an output signal.

Table 1.3.1 Types of Amplifiers

Types of Signal	Types of Confrigation	Classification	Frequency of operation
Small Signal	Common Emitter	Class A amplifier	Direct Current
Large signal	Common Base	Class B amplifier	Audio Frequencies (AF)
	Common Collector	Class AB amplifier	Radio Frequencies(RF)
		Class C amplifier	VHF,UHF,and SHF frequencies

Amplifiers are simple box containing amplifying devices BJTs, field effect transistors or operational amplifiers(op-Amps) having two input and output terminals. An ideal amplifier has three main properties input resistance ,(R_{IN}), output resistance(R_{out}) and amplification factor gain or A.

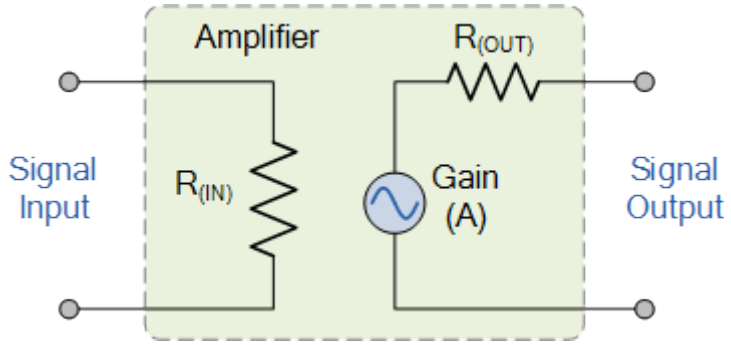


Fig 1.7 Basics Amplifier

Amplifier Gain- It is defined as the ratio of output signal and input signal. there are three different types of Voltage Gain(A_v), Amplifier gain, Current gain (Ai) and power gain (Ap) depending upon the measurement of quantity.

$$\text{Voltage Gain } (A_v) = \frac{Vout}{Vin} \qquad \text{Eq 1.3.1}$$

$$\text{Current Gain } (A_i) = \frac{Iout}{Iin} \qquad \text{Eq 1.3.2}$$

$$\text{Power amplifier Gain } (A_p) = A_v * A_I$$

The power gain A_p or power levels of the amplifier can be expressed in Decibels(dB).

The most commonly used mode of operation of BJT amplifiers are Common Emitter, Common collector and Common base mode of configuration. Whereas in MOSFETs common gate Common source and Common Drain configuration are the different modes of configuration used for amplification.

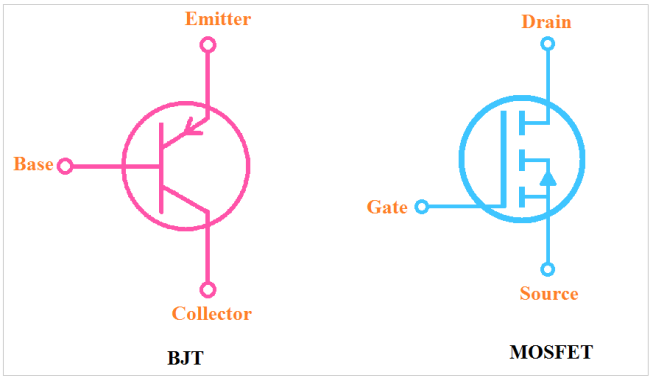


Fig 1.8 Basic BJT & MOS Circuit

Different modes of MOSFET configuration-

a.) Common Source- this is most widely and commonly used FET circuit. The circuit produces medium input and output impedances. Current and the voltage gain have 180^0 phase change.

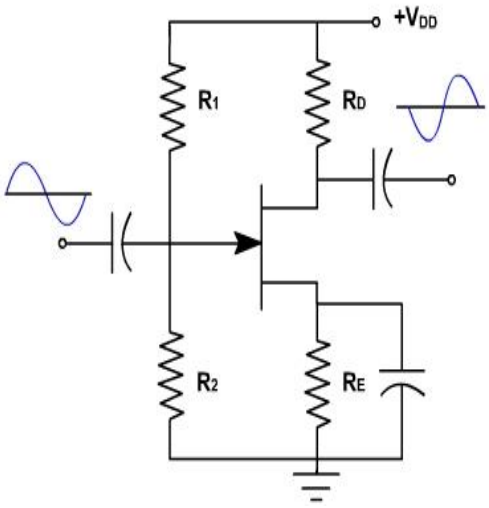


Fig 1.9 CS Amplifier

Eq 1.3.3 $A_v = -gmR_D||r_0$

To keep the device in the saturation mode of operation

Eq 1.3.4 $V_{DS} = V_{DD} - I_D R_D > V_{DS,\,Sat}$

b.) Common Drain- this type of FET [7]is also called as source follower circuit as it provides a high level of buffering and input impedance. The input resistance of FET is very high which means that the circuit is capable of providing excellent performance as a buffer. The voltage gain is unity and current gain is high and at the O/P the input and output signals are in phase.

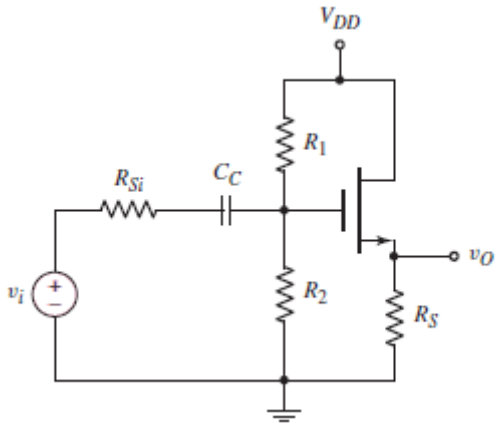


Fig 1.10 Common Drain Amplifier

Eq 1.3.5 $A_v = \frac{gmRs}{1+gmRs} = 1$

However to drive the device into saturation the amount of threshold voltage applied should be greater than the device work function

$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2$$

Eq 1.3.7

$$V_{GS} = V_T + \sqrt{\frac{2I_{DS}}{\mu C_{ox} \frac{W}{L}}}$$

Weak I_{DS} dependence

Eq 1.3.8

$$V_{Tn} = V_{TOn} + \gamma_n \left[\sqrt{(V_{OUT} - V^-) - 2\phi_p} - \sqrt{2\phi_p} \right]$$

Eq 1.3.9

c.) Common Gate- The common gate amplifier [7] is also called as current buffer amplifier because the amplifier is having a low input resistance and output resistance of the amplifier is found to be high. The other parameters like current gain of the amplifier is low and therefore, the power gain of the amplifier is also low as compared to other FET configuration circuits. The input and output are also found in phase.

$$A_v = g_m R_D$$ Eq 1.3.10

Table 1.3.2 Comparison Table

FET CONFIGURATION	**COMMON GATE**	**COMMON DRAIN**	**COMMON SOURCE**
VOLTAGE GAIN	High	Low	Medium
CURRENT GAIN	Low	High	Medium
POWER GAIN	Low	Medium	High
INPUT RESISTANCE	Low	High	Medium
OUTPUT RESISTANCE	High	Low	Medium
I/P PHASE RELATION	0^0	0^0	180^0

1.4 LNA BASICS

The low noise amplifier (LNA) are devices capable of amplifying extremely weak signals and providing voltage levels for analog to digital conversion or further analog processing[8]. These are employed in the circuit consisting of transducer and antenna. When the strength of the signal is low system is dominated by noise and gain introduced in the first stage. Thus , selection of the LNA is an important factor for complete experimental setup. Consider ,LNA with a gain (G) the desired signal S_i represents the input signal having an unavoidable noise N_i at the output both the signal and noise are amplified by a factor of G. the parasitic effect and thermal effect results in generation of additional noise factor N_{ampl} for amplifying a low level signal.

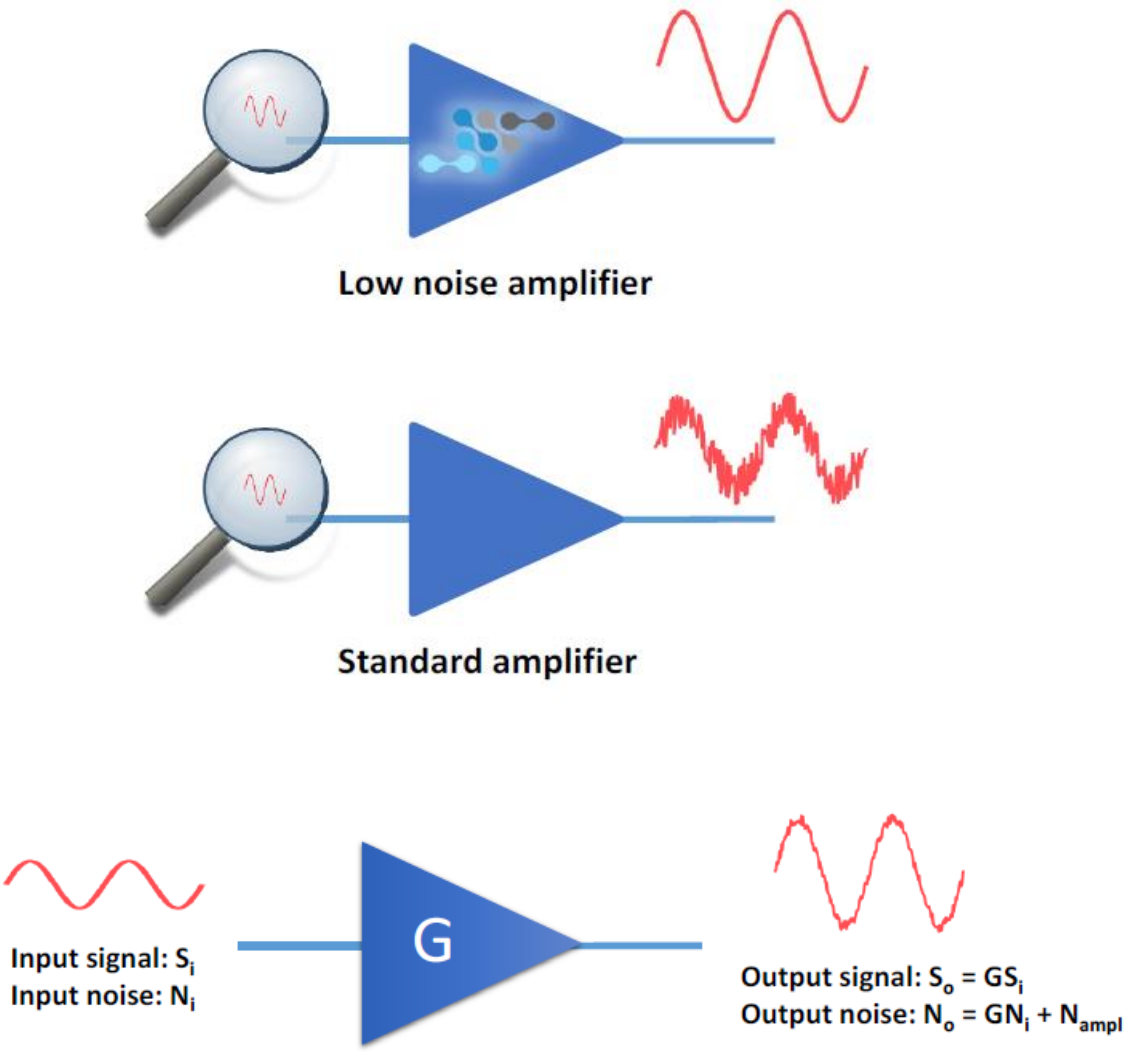


Fig 1.11 Basic LNA

The objective of my thesis is to design a low noise amplifier for IEEE standard 802.15.a and RF front end application. The designing of LNA is determined by input and output matching network and determination of some common parameters like S parameters, noise figure, IIP_3 linearity and stability factor. The optimal value of these parameters determines the stability and efficient performance of the system.

1.5 PARAMETERS OF LNA

The front end of the transceiver system consist of transmitting and receiving path while transmission the perseverance of exiting signal or the wanted signal is required. This clarifies the designing of transmitting end and issues such as interference rejection, noise and selectivity can be ignored. Thus , designing of receiver is complicated as it involves the factors like S parameters, input and output matching networks noise figure, stability, sensitivity and linearity.

2-port network- a two-port network represents a universal way of analysing RF circuits.it consist of "black box" discussing the flow of the voltages and currents from port 1 to port 2. this determines the characteristics of the system without analysing the whole circuit.

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \qquad \text{Eq 1.4.1}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \qquad \text{Eq 1.4.2}$$

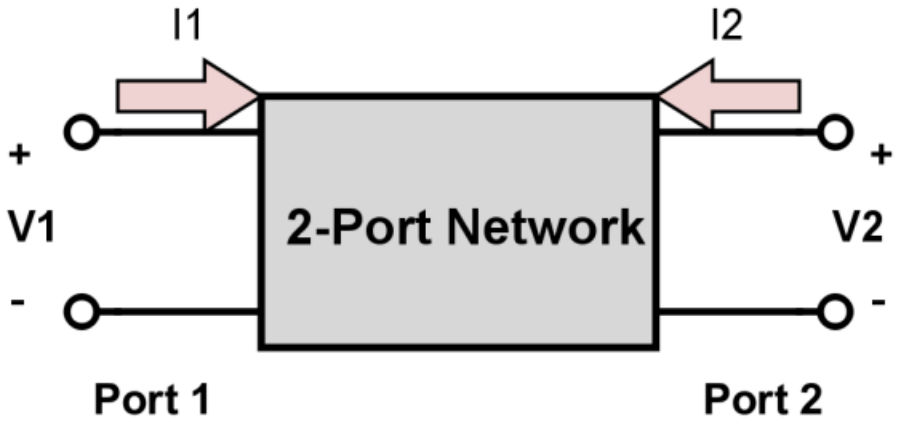


Fig 1.12 Port N/W with Voltage Source V1 & V2

In the above network the I_1 and I_2 are the independent parameters V_1 and V_2 are the dependent parameters. The analysis is made by considering either of the port as short or open circuit considering only one at a time. These parameters are crucial at low frequency

analysis at high frequency the transmission coefficients, reflection coefficient, forward gain, reverse gain become significant. Therefore, the role of S parameters becomes significant and analysis are made considerably.

S parameters also called as scattering parameters that relays the information of the travelling waves. Theses waves are scattered back and forth when transmission line is introduced in an n-port networks. S parameters are widely used in the analysis of amplifier, active devices and transistor circuit. For eg- these are measured when the instruments and RF circuits are embedded between a source and a 50 Ω load.

S parameters are a common way of describing a network . unlike V and I, it do not change at the terminals of the circuits. The changes are obtained along the length of the transmission line whenever a mismatch between the load and source load is observed. However, at high frequency parasitic effects causes the change in the load impedances.

The two port network defining S parameters consist of variables a_1 and a_2 as normalised incident voltages.

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave incident on port 1}}{\sqrt{Z_0}} = \frac{V_{i1}}{\sqrt{Z_0}}$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave incident on port 2}}{\sqrt{Z_0}} = \frac{V_{i2}}{\sqrt{Z_0}} \qquad \text{Eq 1.5.1}$$

Where Z_0 refers to the single positive real impedances.

While the b_1 and b_2 are the normalised reflected voltage coefficients

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave reflected on port 1}}{\sqrt{Z_0}} = \frac{V_{r1}}{\sqrt{Z_0}}$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{\text{voltage wave reflected on port 2}}{\sqrt{Z_0}} = \frac{V_{r2}}{\sqrt{Z_0}} \qquad \text{Eq 1.5.2}$$

Now the S parameter equation for two port network is given by as-

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad \text{Eq1.5.3}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \qquad \text{Eq 1.5.4}$$

the S parameters coefficients are given by-

$S_{11} = \frac{b_1}{a_1}$ when a_2=0 (Port 1 reflection coefficient when port 2 is terminated by a matched load $Z_L=Z_0$)

$S_{12} = \frac{b_1}{a_2}$ when a_1=0 (Reverse transmission gain when port 1 is terminated by a matched load)

$S_{21} = \frac{b_2}{a_1}$ when a_2=0(Forward transmission gain when port 2 is terminated by a matched load)

$S_{22} = \frac{b_2}{a_2}$ when a_1=0 (Port 2 reflection coefficient when port 1 is terminated by a matched load)

Overall, S parameters help the designers to predict the nature and desired performance of the system.

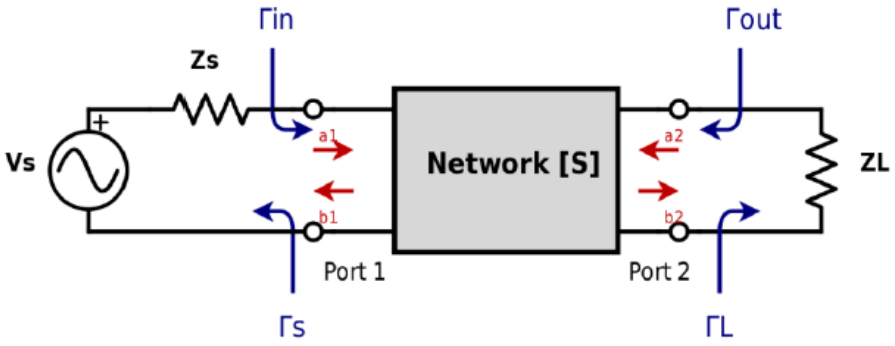


Fig 1.13

Considering the load and the source coefficients Γ_s and Γ_L given by

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad \text{Eq1.5.5}$$

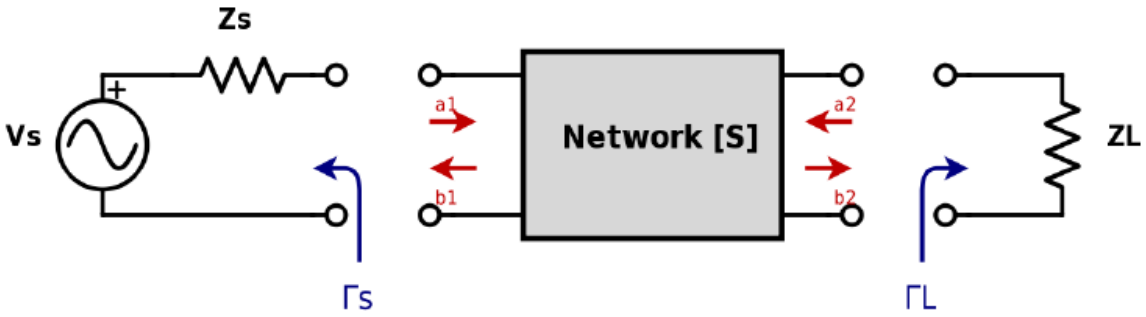


Fig 1.14 Reflection Coefficient Representation

$$\Gamma_{in} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

$$\Gamma_{out} = \frac{b_1}{a_2} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \qquad \text{Eq 1.5.6}$$

The power gain of the system is defined as ratio of the power delivered to the load end to the power available from the source end P_{in}

$$G_p = \frac{P_L}{P_{in}}$$

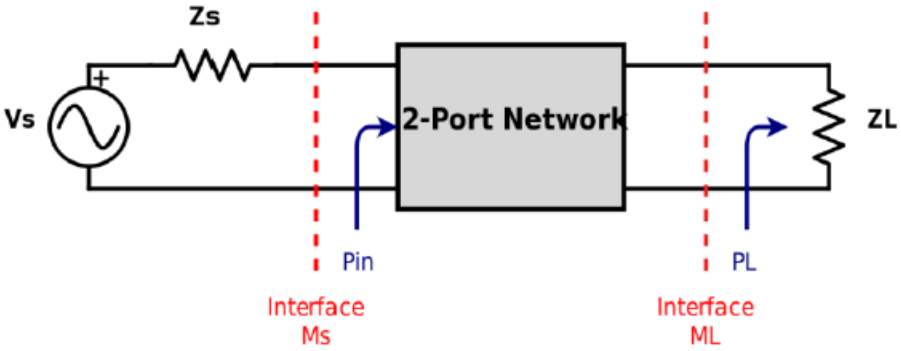


Fig 1.15

$$P_L = \frac{1}{2}|b_2|^2(1 - |\Gamma_L|^2)$$

$$P_{in} = \frac{1}{2}|a_1|^2(1 - |\Gamma_{in}|^2) \qquad \text{Eq 1.5.7}$$

$$G_p = \frac{1}{1 - |\Gamma_{in}|^2}|S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \qquad \text{Eq 1.5.8}$$

Finally, the available power gain G_a is defined as output network power available to the ratio of the source power available.the mismatch factor M_L is defined as mismatch between load and the output.

$$G_a = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \qquad \text{Eq 1.5.9}$$

The above equation gives the expression for available power gain G_a.

2.)**MATCHING INPUT AND OUTPUT IMPEDANCES**- Power gain at low frequency is obtained using thevenin equivalent and maximum power transfer theorem. But, due to power lossess the power gain of the circuit is usually deficient which is observed from one stage to the other because of thermal resistance and load impedance. therefore, RF circuit designing mainly focuses on impedance matching assuming RF circuit is represented by a simple voltage source having a source impedance (Z_s) and a load impedance (Z_L).

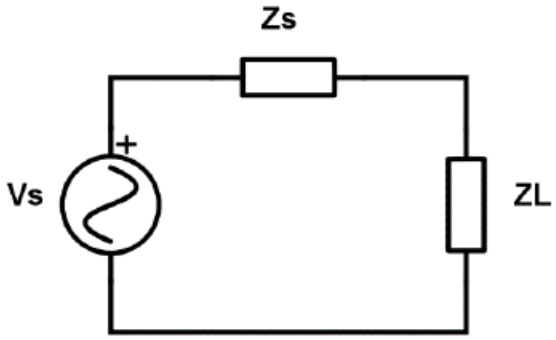


Fig 1.16 RF Simplified Series RLC Circuits

It is considered that the component losses are minimum but the parasitic effects are considered. For matching we consider the different combinations of R, L and C. the source impedance Z_s can be written as source resistance R_s in series with the impedance X_s. while the load impedances can be expressed load R_L in series with X_L. therefore maximum power transfer can be represented as

$$P_L = \frac{V_L^2}{R_L} = \frac{R_L V_s^2}{(R_L+R_s)^2+(X_L+X_s)^2} \qquad \text{Eq 1.5.10}$$

When the load X_L is equal to X_s imaginary terms cancel out R_L should be equal to R_s. for maximum power transfer. At high frequency circuits we have three types of matching circuits L matching, T matching and pie matching circuits.

L -Matching Circuits- For the L- matching circuit the concept of series and parallel transformation is necessary. Like for example the impedance Z_{AB} can be transformed as

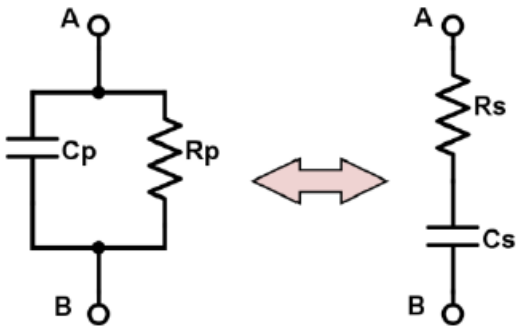


Fig 1.17

$R_p = R_s(1+ Q^2)$ Eq 1.5.11

$X_P = X_s(\frac{1+Q^2}{Q^2})$ Eq 1.5.12

Where X_s denotes $\frac{1}{\omega c_s}$ and X_P denotes $\frac{1}{\omega Cp}$ in the L matching circuit the load impedances can be expressed as upward or downward and R_s and R_p can be transformed into each other.

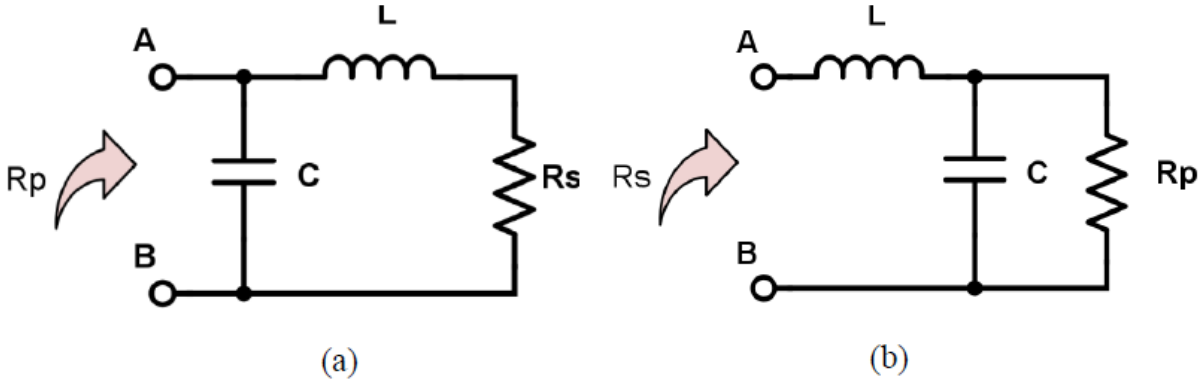


Fig 1.18

The quality factor serves as the measurement of reactivity of the circuit and is defined as the ratio of energy stored in the elements and energy dissipated by the components.

$$Q = \frac{x_L}{R_L} \qquad \text{Eq 1.5.13}$$

$$Q = \frac{w \cdot L}{R_L} \quad \text{or } Q = \frac{1}{\omega c R_L} \qquad \text{Eq 1.5.14}$$

Therefore, the quality factor can be written as the ratio of R_L/R_S

$$Q \cong \sqrt{\frac{R_P}{R_s}} \qquad \text{Eq 1.5.15}$$

The conjugate matching results in the cancellation of reactive terms therefore, the effect of inductor and capacitor becomes insignificant. Therefore, the designer can manipulate the positions of impedances to obtain the low pass or high pass circuit.

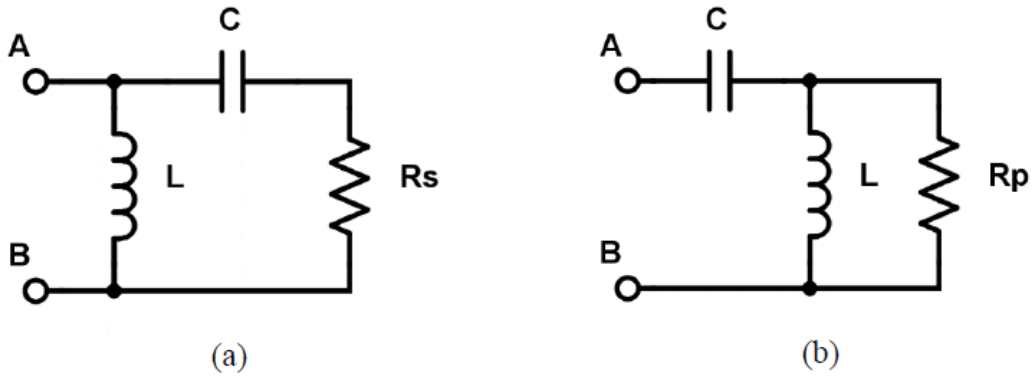


Fig 1.19

The quality factor of the circuit is obtained by a particular value of R_L and R_S due to which quality factor of the circuit is fixed and design of the circuit gets frozen meaning no more changes can be made providing only one degree of freedom.

∏ or pie matching circuit- it improves the limitation of L- matching circuits. The limiting factor consist of Q, impedance transformation ratio and centre frequency. L matching circuit consist of only two manipulative components whereas ∏ or T matching circuit adds extra components giving a designer a extra degree of freedom for optimising the circuits.

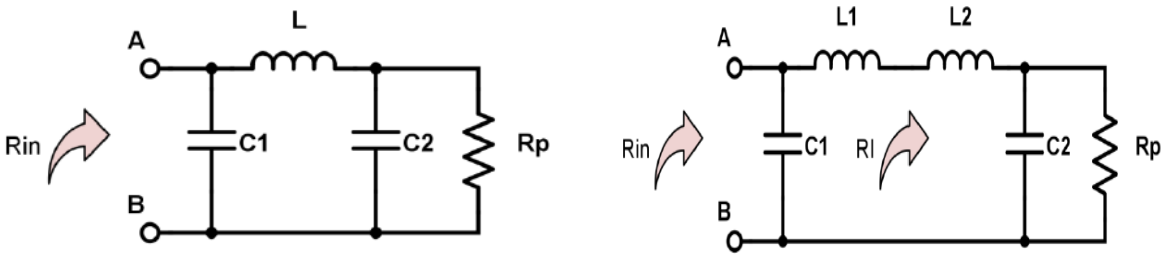


Fig 1.20

Adding the component or making it T or pie adds extra degree of freedom controlling the value of Q added to the circuit. Adding extra components causes bandwidth improvements while decreases the value of Q. adding inductance in series makes the circuit more inductive in nature and adding C capacitive in parallel causes the circuit to become more capacitive in nature.

$$Q_{CD} = \frac{\omega_0 L_2}{R_I} = \sqrt{\frac{R_P}{R_I} - 1}$$

Eq 1.5.16

Where the ratio of $\frac{R_P}{R_I}$ is the transformation ratio.

T- matching circuits- this matching circuit consist[9] of connecting two L matching circuits back to back. The capacitor C_1 and C_2 are connected in parallel combination. The formulas of Q,L and C can be derived from pie matching circuit.

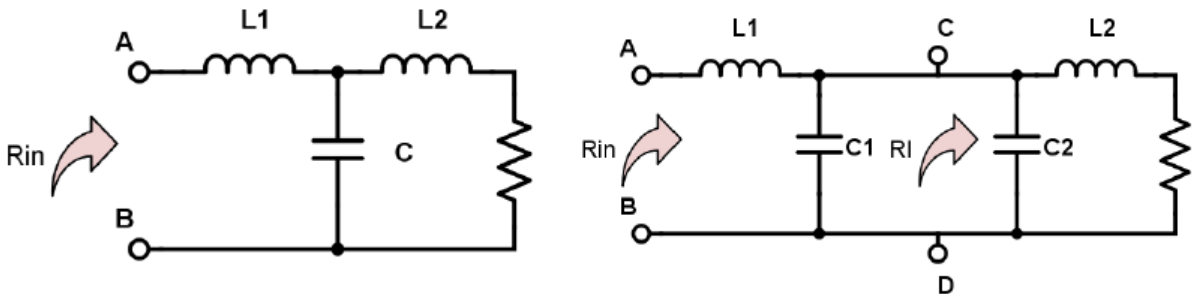


Fig 1.21

$$Q_{ov} = Q_{AB} + Q_{CD} = \omega_0 R_I (C_1 + C_2) = \sqrt{\frac{R_I}{R_{in}} - 1} + \sqrt{\frac{R_I}{R_S} - 1}$$

$$C_1 + C_2 = \frac{Q_{ov}}{\omega_0 R_I}$$

$$L_1 = \frac{Q_{AB} R_{in}}{\omega_0}$$

$$L_2 = \frac{Q_{CD} R_S}{\omega_0}$$

Eq 1.5.17

These are used when the source and load impedances are inductive in nature. these are capable of absorbing parasitic inductor of the matching circuit and are preferred when high quality factor is desirable.

BANDWIDTH- It is the crucial factor for designing of RF circuits. Different WSN have different frequency ranges. For eg- the Bluetooth technology has a frequency range from 2.40 GHz to 2.438 GHz. Estimating the bandwidth of RF circuits with hand calculations is very difficult as it requires one to find (peak frequency) fpeak and also -3dB points of the circuits.for finding these values the total impedances of the circuits must be calculated first. It involves the impedances both at the output and input ends consisting of parasitic resistances and imaginary components (like inductor and capacitors).however, conventional ways of finding the impedances is called as open circuit time constant (OTC) or zero value time constants.

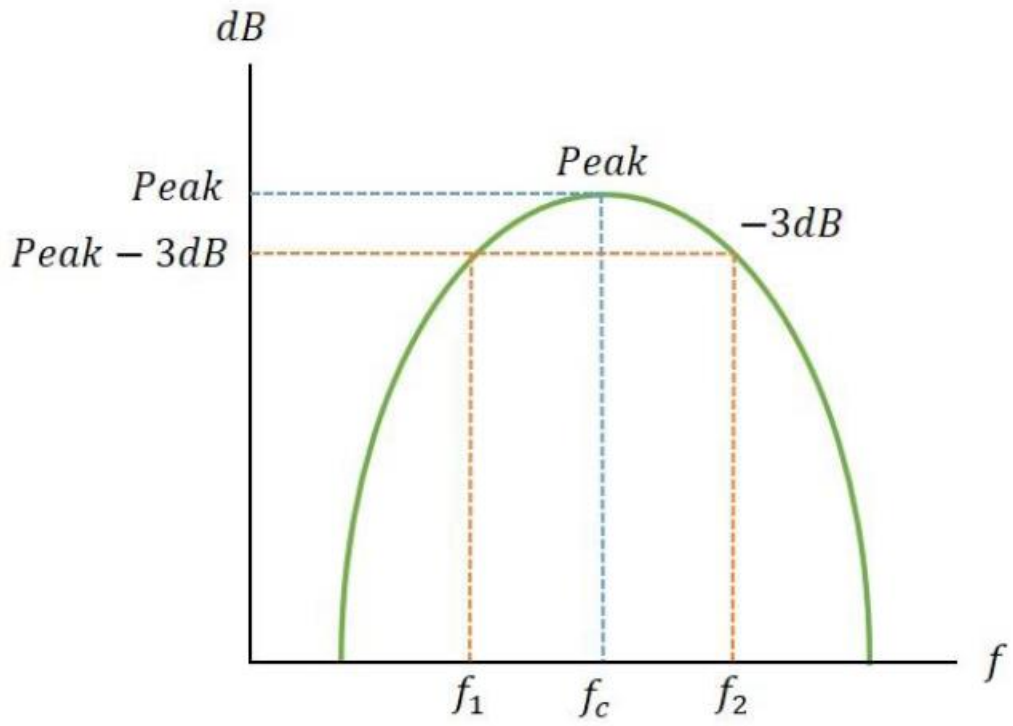


Fig 1.22 3-dB Bandwidth with Peak frequency

OCT gives the bandwidth of the system obtained by inspecting from nodes. OCT specifies the elements and factor causing bandwidth limitations.

$$\frac{V_o(s)}{V_i(s)} = \frac{a_0}{(\tau_1 s + 1)(\tau_2 s + 1) \dots (\tau_n s + 1)} \quad \text{Eq 1.5.18}$$

The Industrial, Scientific and medical (ISM) frequency band are designed for radio frequency bands defined by ITU regulations. These frequency bands are used for RF applications other then telecommunication. Telecommunication equipment's operating at such frequency are interrupted by microwave ovens, electromagnetic interference (EMI),RF heating devices.

The most common use of the ISM band are low power, short range telecommunications such as Bluetooth ,Zigbee Wifi, Wireless Telephones NFC and RFID. In recent times, ISM band [10] is also shared with (non-ISM) license free-tolerant communication devices like (WSN) in 915 MHz and 2.4 GHz and 5.8 GHz in cordless and wireless LANs applications.

NOISE FIGURE-noise is defined as unavoidable and undesirable effect occurring in electronics and RF circuits. It is expressed as spectral density in voltage or current/Hz

that is V^2/Hz or A^2/Hz.The spectral density specifies the noise parameters. The characteristics equation representing a noise source is integrated over a frequency for specifying the spectral density of a noisy source. Therefore, differentiating a noisy source and its cause is required for minimizing its effects to an acceptable degree. In electronics circuit we have five types of noise effecting the performance of the amplifiers. These are thermal noise, shot noise, flicker noise burst noise and avalanche noise.

THERMAL NOISE-this type of noise is generated due to the random motion of the electrons. The agitation in the charge carrier due to applied voltages causes generation of the electrons within the electrical conductors. The vibration of the charge carriers about their mean position is only effected by the temperature variation higher the temperature more will be the agitation resulting in high thermal noise. The noise power generated is proportional to the bandwidth. Therefore, the generalised expression of thermal noise is given by-

$$V_n^2 = 4KT \int_{f1}^{f2} R \, df \qquad \text{Eq 1.5.19}$$

Where V_n represent the integrated rms voltages between frequency f_1 and f_2

R denotes the resistive components in Ω (impedances) and T is measured in degrees kelvin. The equation is further simplified as where Δf is the bandwidth in Hz.

$$V_n = \sqrt{4KT\Delta f R} \qquad \text{Eq 1.5.20}$$

SHOT NOISE- it is caused due to the current flow generated when a large number of charge carrier crosses a potential barrier, which is a random event. Thus, the instantaneous current I, represents a large number of random motions of the independent currents having average value I_D. the charge carriers consist of discrete sets of bundles in discontinuous form of currents. This is observed when electrons crosses energy barriers and the difference in the arrival time.

$$I_n^2 = 2qI_{DC}\Delta f \qquad \text{Eq 1.5.21}$$

Where I_n represents the rms current having bandwidth.q is the charge I_{DC} represents the current through an energy barrier and Δ f is the bandwidth.

FLICKER NOISE- it is defined as inversely proportional to the frequency. It is found in all active devices. It is always associated with the DC current. It is mainly found in carbon composite resistors in addition to the thermal noise. Since it is proportional to the d.c. current when the current is low system is dominated by thermal noise. The shot noise and thermal noise dominates the high frequency regions. As it is inversely proportional to frequency it is expressed as

$$N^2 = \frac{K}{f^n}\Delta f \qquad \text{Eq 1.5.22}$$

Where N represent the RMS noise signal which is either in the form of voltage or current, K is the empirical device parameters and Δf is bandwidth in Hz.

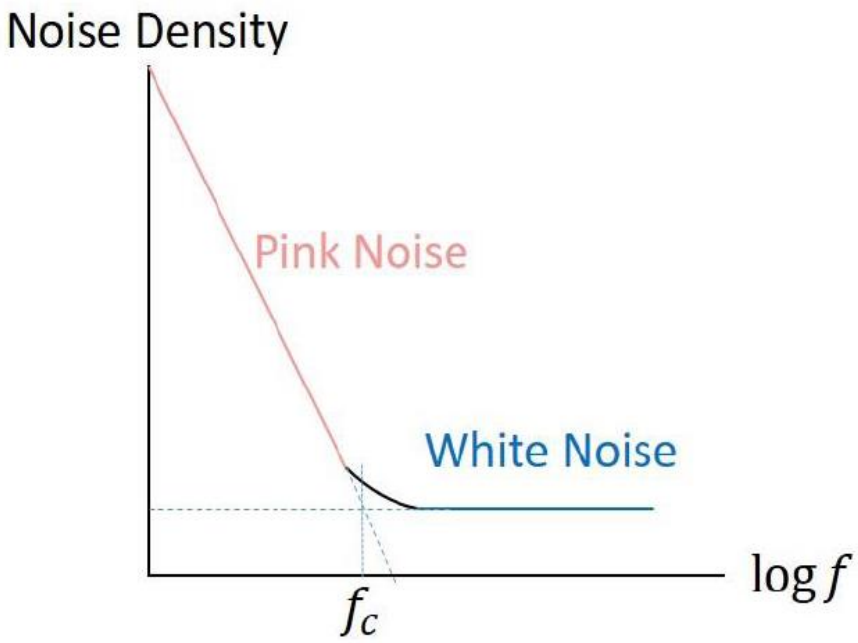


Fig 1.23 Noise Spectral Density

NOISE FIGURE – It is defined as the noise performance of a two port network.it is defined as the ratio of output noise power to the noise power of the input source. When expressed in decibels it is called as noise figure.

$$\text{SNR} = \frac{\text{P}_{\text{signal}}}{\text{P}_{\text{noise}}}$$

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_i/N_i}{S_o/N_o} \qquad NF = 10\log F$$ Eq 1.5.23

Where S_i and S_0 are the signal power at the input and output source and N_i and N_0 are noise power at the input and the output port .

For an ideal case SNR_{in} and SNR_{out} should be equal. This is due to the desired signal and noise are amplified by the same gain. So therefore, SNR_{in} and SNR_{out} are having the same values. When the signal is allowed to pass through system. The receiving circuit generate its own noise by components and degrades SNR. Additional noise signal (N_a) and network gain(G) are related as

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{GS_i/(N_a + GN_i)} = \frac{N_a + GN_i}{GN_i}$$

$$F = \frac{N_a + KT_0BG}{KT_0BG}$$

Eq 1.5.24

Where K is 1.38*(10)^(-23) Joules/K^0

B is network bandwidth in Hz.

G is the gain.

The noise figure of the multistage amplifier is expressed as

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \ldots A_{p(m-1)}}$$ Eq 1.5.25

The first stage of the RF system contributes major portion of the overall noise. Therefore, the first stage of amplifier circuit mainly consist of LNA which plays a crucial role in overall noise figure calculations.

LINEARITY- If the nature of the system does not change with time and all the intial conditions are found to be zero then the system is called as a linear system. Linearity is an important factor in the designing of LNA. LNA must uphold, property of linearity

when the signal is weak or strong even in the presence of interfering signal[11]. There are two types of linearity 1-dB compression point and third order intercept point (IIP_3) which improves the performance of LNA.

1 dB- Compression point- the input and output power is found to be linear at a specific frequency for the amplifier having a solid gain. The slope represents the power gain in dBm. For the gradual increase in the input power at one point output power saturates. 1 dB compression point is defined as that point where the output power saturates for the increase in the input power signifying that when the signal is received by the amplifier it becomes non-linear causing signal distortion, as a result harmonics are produced due to intermodulation distortion.

Assume that sinusoidal input signal is applied to a non-linear system. For the explanations of P_{1dB} compression point. The output signal can be represented by

$$x(t) = A\cos\omega t$$

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t$$

$$y(t) = \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \quad \text{Eq 1.5.26}$$

In above the desired signal is *coswt*. Byproducts of the input signal in eq() are also called as harmonic distortion. The signal coefficients $\alpha_1\alpha_3$ signifies the characterstics of amplifier. If the coefficient $\alpha_1\alpha_3>0$ then the output is increasing with the increase in the input signal. This phenomena is mainly observed in BJTs since MOSFETs saturates at certain point. Therefore, $\alpha_1\alpha_3<0$ is considered for comprehensive characteristics which are more suitable for LNA design.

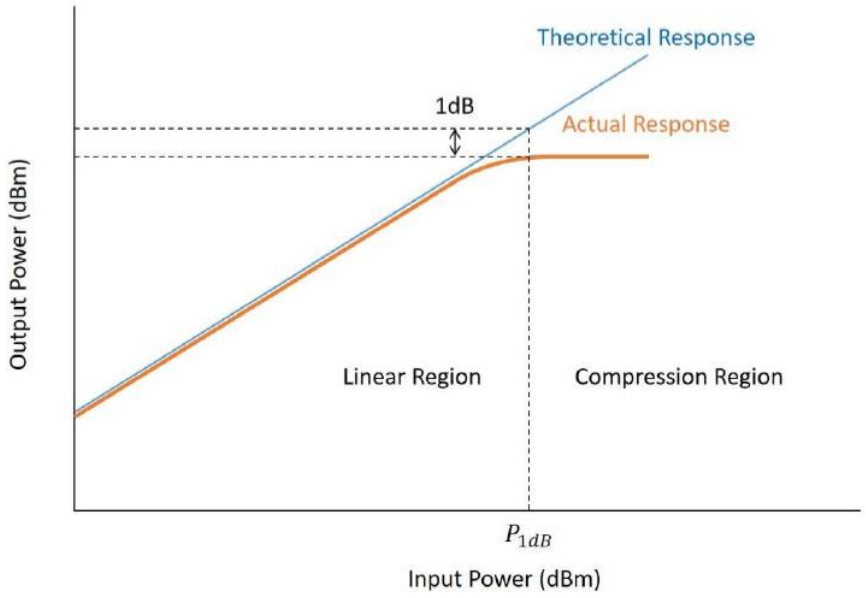


Fig 1.24 P1-dB compression Point

Finally, P_{1dB} is 1 dB below expected output power by giving the input signals

$$10\log\left|\alpha_1 + \frac{3\alpha_3 A^2}{4}\right| = 10\log|\alpha_1| - 1dB \qquad \text{Eq 1.5.27}$$

where:

$\alpha_1 + \frac{3\alpha_3 A^2}{4}$ is actual power response

α_1 is expected power response

Third- order intercept point (IIP_3)- assuming [2] the input signal of the amplifier is a sinusoidal signals when amplifier becomes non-linear it consist of harmonics of cos2*wt* and cos3*wt*. the highest harmonics are insignificant since the system consist of finite bandwidth . however, non-linearity produces two signals because of intermodulation distortion.

The sum and the difference of the frequencies at the receiving end are called as intermodulation products. The interfering signals are not filtered out since it consist of desired signal. Several methods like signal levels, biasing control and other factor ensures the linearity and significantly reducing the intermodulation distortion (IMD) products.

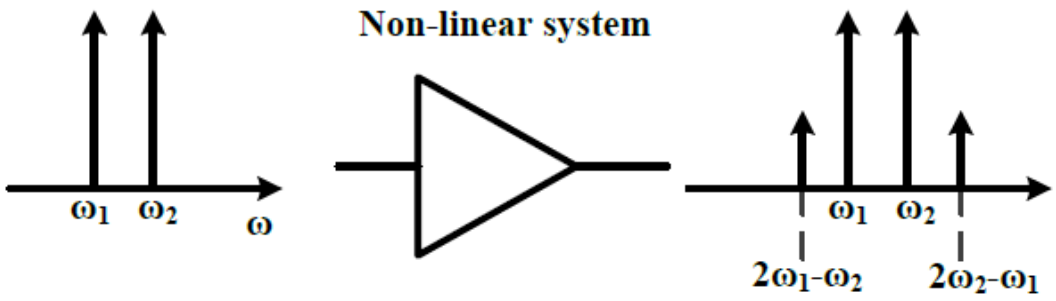


Fig 1.25

However, at the receiving end w_1 and w_2 produces $w_1 + w_2$ and $w_1 - w_2$ and $2w_1 + w_2$ and $2w_2 - w_1$. These sets of frequency ranges produces second , third and fourth harmonics of the interfering signals. The IP3 is defined as the point where the first order of the input signal is found to be equal to the third harmonics of the desired signal.

$$|\alpha_1 P_{IIP3}| = \left|\frac{3\alpha_3 {P_{IIP3}}^3}{4}\right|$$

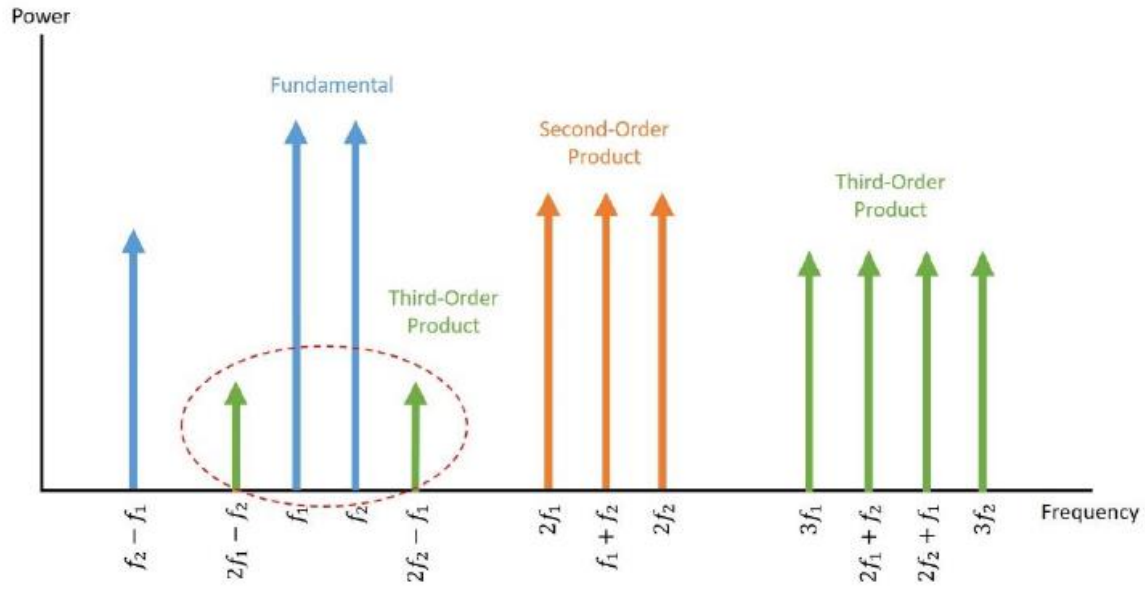


Fig 1.26 Measure of Third order Intercept point

$$P_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}$$

Eq 1.5.28

Note IP3 is a theortical concept that is never obtained in present scenario. However, it's a tool in determining the linearity of the amplifier.

STABILITY FACTOR-it is defined as immunity against spurious oscillations. The circuit becomes unstable for specific combination of source and load impedances. An LNA designed oscillate at extreme of voltage variation for low or high frequency. Therefore, the stability of an amplifier is given by two factors K and Δ where K denotes rollet's stability factor or stern stability factor.

For unconditionally stable system K>1 and Δ<1. The points considered under such region denotes that the circuit do not oscillate for any combination of source and load impedances.

Eq 1.5.29

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

Where

$$\Delta_s = S_{11}S_{22} - S_{12}\,S_{21}$$

SENSITIVITY- it is defined as minimum signal level detected by a receiver with "acceptable quality" when the signal is interrupted by noise it carries little information. Acceptable quality is defined as sufficient signal to noise ratio depending upon the type of modulation and corruption that signal can tolerate. Typically, (SNR) ranges from 6 to 25 dB.

$$P_{sig} = P_{RS}.F.SNR_{out}$$

Eq 1.5.30

When the signal is distributed both side of the channel the equation is integrated over the bandwidth so the mean square power is given by-

$$P_{sig,tot} = P_{RS}.F.SNR_{out}.B$$

Eq 1.5.31

Therefore, the overall sensitivity of the system includes the channel bandwidth, NF, SNR expressed in dB and the channel bandwidth B in Hz.

$$P_{sig,\min\ |dB} = P_{RS|dB/Hz} + NF + SNR_{\text{out,min}\ |dB} + 10logB \quad \text{Eq 1.5.32}$$

Where $P_{sig,min}$ is the minimum power achieving $SNR_{out,min}$ in dB.

TABLE 1.6.1 DIFFERENT TYPES OF TOPOLOGIES OF LNA

BASIC LNA TOPOLOGIES	ALTERNATE LNA TOPOLOGIES	NONLINEARITY OF LNAs
CS stage using Inductive load	Types of CS LNA	Nonlinearity Calculations
CS stage implemented with Resistive Feedback	Noise- Cancellation LNAs	Differential and Quasi-Differential LNAs
CS stage with Inductive Degeneration	Differential LNAs	

In this section LNA is divided into five parts topologies, I/P and O/P matching circuits, source degenerate feedback, biasing circuits. Further, the key factors such as S parameters, Stability factor, Noise figure is estimated and presented with schematic in chapter 3 for RF front end applications.

Table 1.6.2 Common Design Specifications

PARAMETERS	SPECIFICATIONS
a.) Power Supply	1-3 (V)
b.) Power Dissipation	1-20 (mW)
c.) Input and Output Impedances	50 Ω
d.) NF	<3(dB)
e.) Gain	< 10(dB)
f.) IIP3	(-10)(dBm)

LNA is implemented mainly using three topologies which are common source, common gate and cascode topology which provides the perfect input output isolation and increases the stability of the system.

1.6.1 **COMMON SOURCE TOPOLOGY**- LNA[12] implemented with a common source topology provides proper input/output matching network. The common source with resistive termination provides 50Ω input impedances. For this R_1 is placed in parallel with the input matching network of LNA. However, this confrigation is less preferred because of the tradeoff between voltage gain and supply voltage. Furthermore, the o/p node becomes inappropriate as the resistor generates noise.

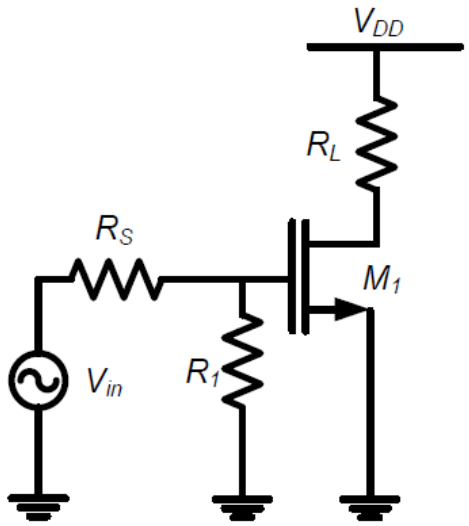


Fig 1.27

The noise figure calculation of the circuit is given by

$$F = \frac{\overline{v_{n,out}^2}}{\overline{v_{n,o,Rs}^2}} = \frac{\overline{v_{n,o,Rs}^2} + \overline{v_{n,o,R1}^2} + \overline{v_{n,o,M1}^2}}{\overline{v_{n,o,Rs}^2}} \quad \text{Eq 1.6.1}$$

$$= \frac{4kT(R_s//R_1)g_m^2R_L^2\Delta f + \overline{i_{n,d}^2}R_L^2}{\frac{1}{4}g_m^2R_L^2}\frac{1}{4kTR_s\Delta f} \quad \text{Eq 1.6.2}$$

1.6.2**COMMON SOURCE WITH INDUCTIVE DEGENERATE TOPOLOGY**- This is the most preferred topology[13] as it provide the most efficient I/P and O/P matching. Introducing a inductor at the source of the mosfets improves the linearity of

circuit. In this configuration the high value of the inductor is not preferred as it causes the circuit to have low gain. The input impedance has a resistive term which shows that resistance is directly proportional to inductor and the circuit do not generate thermal noises like other resistive networks and circuit of reactance becomes noiseless. The 50Ω input impedances is equal to g_mL_s/C_{gs} controlling the value of the transconductance of amplifier so high value of g_m causes the mosfet to leave linear mode of operation.

Zin= g_mL_s/C_{gs}

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \qquad \text{Eq 1.6.3}$$

$$z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega Cgs} + \frac{gmL_s}{Cgs} \qquad \text{Eq 1.6.4}$$

So therefore the equation for voltage gain is given by as-

$$\frac{v_0}{v_{in}} = \frac{R_1}{2 \cdot L_1 \omega_0} \qquad \text{Eq 1.6.5}$$

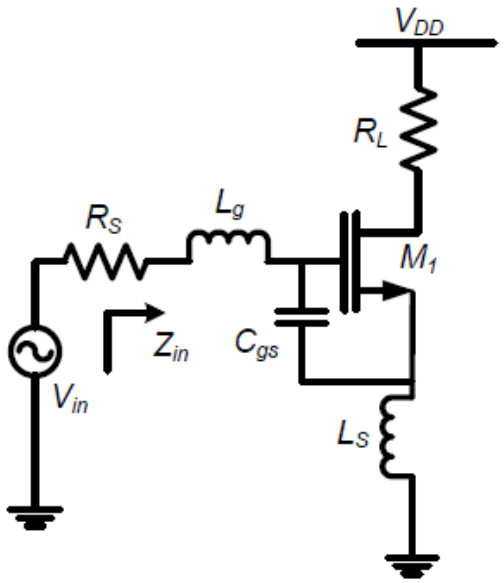


Fig 1.28

1.6.3 **COMMON SOURCE STAGE WITH SHUNT FEEDBACK LNA**- in this [14] the R_{fB} acts as a feedback element. The circuit is having a 50 Ω input impedances. The input impedances is expressed as from miller theorem

$$Z_{in} \approx R_{fb}/(1 + |A_v|)$$ Eq 1.6.6

Where R_{fB} denotes the feedback resistor and A_v denotes the voltage gain of the circuit. The voltage gain is equal to

$$[1 - g_m(R_L//R_{fb})]$$ Eq 1.6.7

And the noise factor of the circuit is expressed as-

$$F = 1 + \left(\frac{G_s + G_{fb}}{g_m - G_{fb}}\right)^2 R_s(G_L + \gamma g_{d0}) + \left(\frac{G_s + g_m}{g_m - G_{fb}}\right)^2 R_s G_{fb}$$ Eq 1.6.8

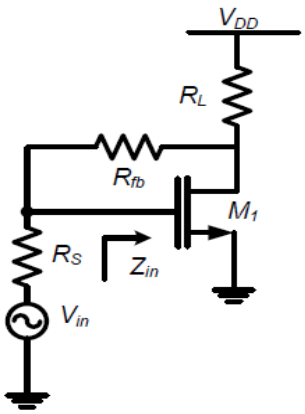


Fig 1.29

b.) **COMMON SOURCE STAGE WITH INDUCTIVE LOAD-** it operates at a very low frequency with low supply voltage as the inductor sustains a small d.c. drop as the resistors [15]. Moreover, the inductor oscillate with capacitors at the output node capable of operating at high frequency than does the resistively loaded counterparts. The common source topology with inductive load is considered as it generates the required number of poles and zeros. The gain of this circuit is given by

$$Av = g_m R_D$$ Eq 1.6.9

When the overdrive voltages are considered $\frac{2v_{RD}}{v_{g_S - v_{th}}}$ Eq 1.6.10

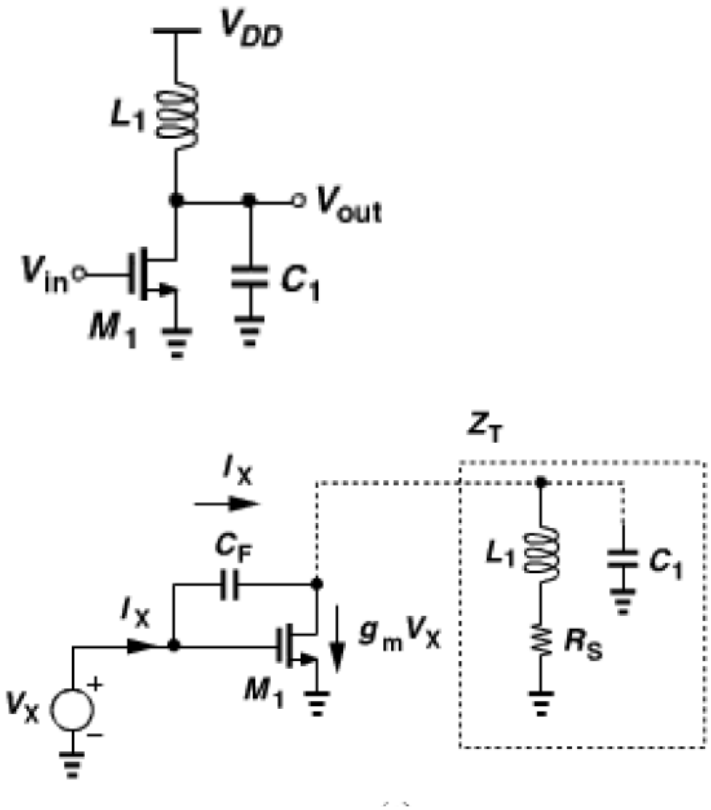


Fig 1.30 Input Impedance with C_F

When the effect of Cgd overlapping capacitance is considered ignoring the effect of gate to source capacitances. The losses across the inductor is modelled by a series resistance Rs in parallel to the capacitance C_1. However, for the purpose of nullifying the effects of capacitor C_F a parallel inductor L_F is considered.

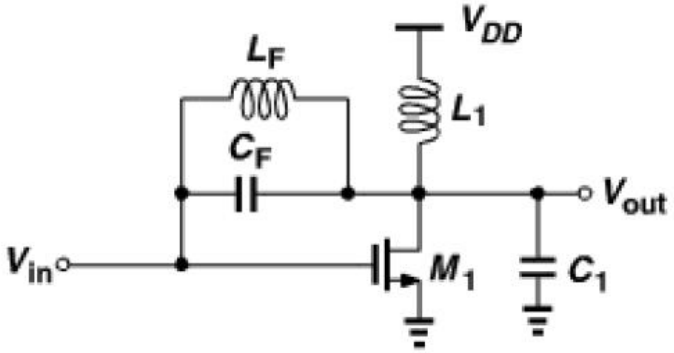


Fig 1.31 Neutralising the C_F by L_F

b.) **COMMON GATE TOPOLOGY**- the common gate (CG-LNA) is [16] widely used for wide band applications. The voltage gain and input impedances of CG LNA is given by as-

$$A = g_m R_L \qquad \text{Eq 1.6.11}$$

$$Z_{in} = \frac{1}{g_m} \qquad \text{Eq 1.6.12}$$

For matching the input matching network g_m is equal to $1/R_s$ due to which the load resistance R_L is a design variable. For the matching networks, the transconductance of the input transistor cannot be made high thus optimised or low value of noise factor is obtained. The noise factor is proportional to γ/α which is reasonable and acceptable however, the other factor like gate induced noise and substrate noise can degrade the performance of the circuit substantially. The load contribute thermal noise and biasing causes shot noises when these effects are considered gain of the system decreases so a common gate with cascode topology is mostly preferred.

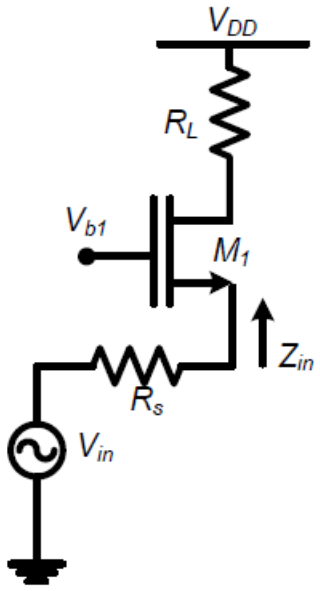


Fig 1.32 Common Gate LNA

1.6.7 **COMMON GATE STAGE WITH RESISTIVE FEEDBACK TOPOLOGY**- In this[2] topology resistance is used as a feedback element. At deep micron, CMOS technology channel length modulation significantly effects the behaviour of the common gate stage. The positive feedback through r_0 raises the input impedances. Since the drain

source currents of M_1 is equal to $-g_mV_x$. the net amount of current flowing through the r_0 is equal to $(I_x - g_mV_x)$. across it. The current Ix flowing through the output loop or tank circuit causes a voltage drop of IxR_1. This causes the voltage drop across r_0 to be equal to

$$\frac{v_x}{\overline{1}_x} = \frac{\dot{R}_1 + r_0}{1 + gmr_0}$$

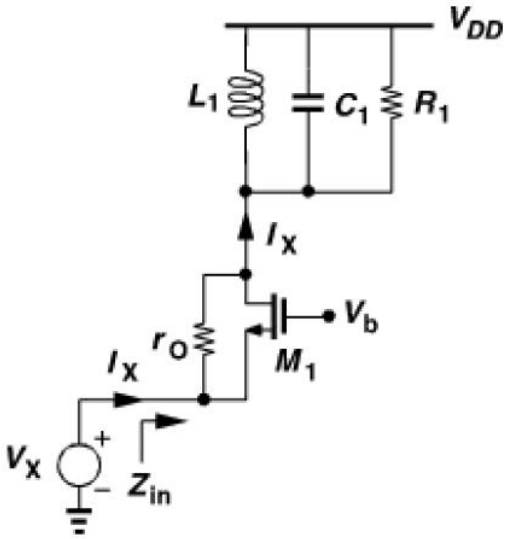


Fig 1.33 Input Impedance in the presence of r_0

Therefore the net input resistance of the circuit increases which can be compensated by using cascode topology which consist of common gate with resistive feedback connected to cascaded CG stage.

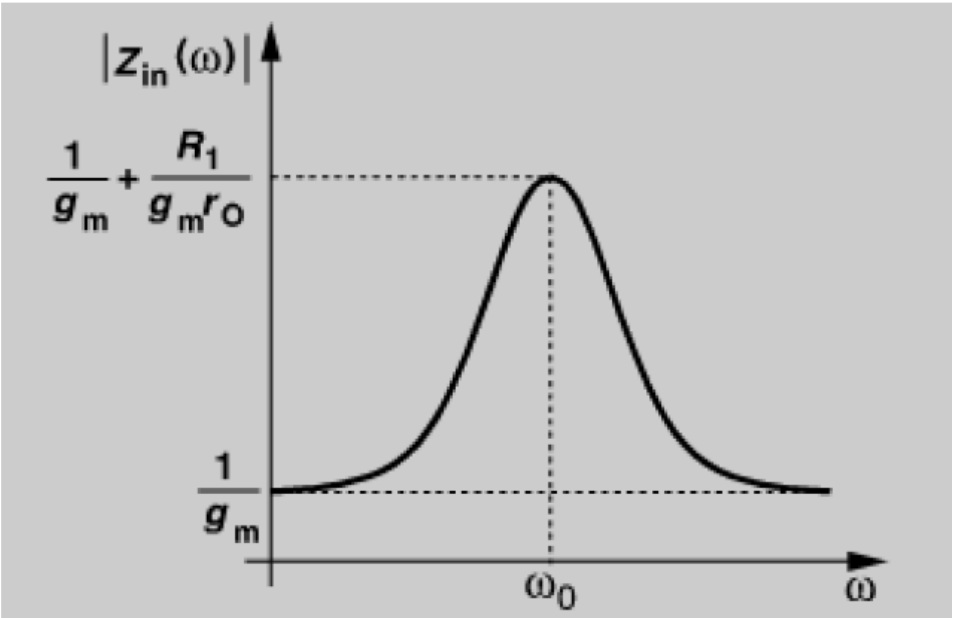


Fig 1.34

So, therefore the cascoded topology of the above configuration reduces the net resistance and optimises the gain of the circuit.

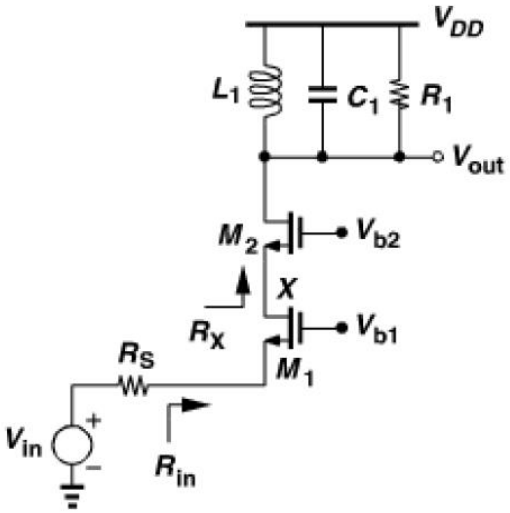


Fig 1.35 Cascode CG Stage

Therefore the overall input impedances of the circuit reduces to

$$R_{in} = \frac{1}{g_m} + \frac{R_1}{g_{m_1} r_{01} g m_2 r o_2} + \frac{1}{g m_1 r_{o_1} g_{M_2}}$$

Which finally becomes equal to $1/g_m$. Eq 1.6.13

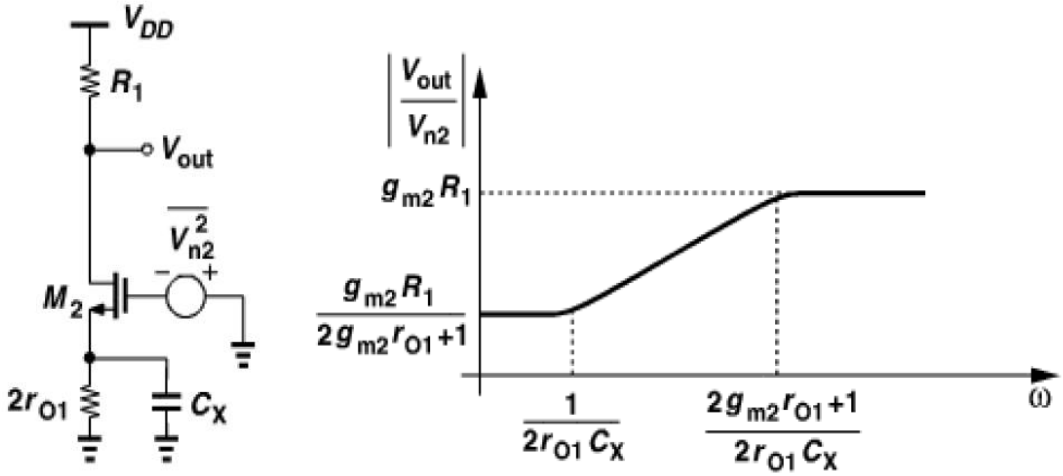


Fig 1.36 Cascoded Transistor Noise and Frequency Response

1.6.8 **CASCODE TOPOLOGY-** in amplifier designing cascode topology is preferred which means adding a transistor or mosfets which means isolating the input from the

output. This isolation between the output and the input end stabalises the circuit. The advantages of cascode topology are-

- Better stability
- Better noise figure
- High gain
- Better reverse isolation
- Input and output matching network

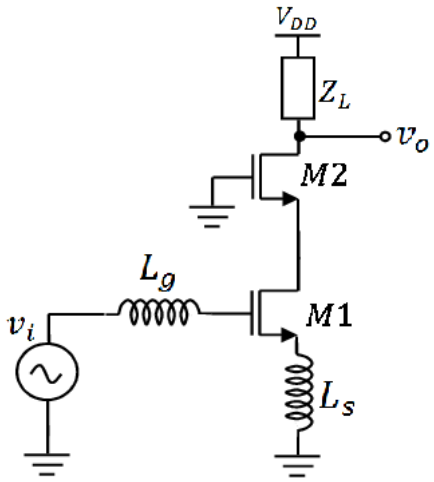


Fig 1.37

Spiral inductors are less preferred due to the limitation of occupying a large chip area, capacitive and resistive losses. Therefore, active inductor can be implemented with reasonable good physical size. Traditionally, active inductor [17] are implemented using high gain operational amplifier with a negative feedback but these are unsuitable for operating in frequencies of GHz. Another type of active inductor are implemented by considering parasitic capacitances. However, varying the value of I_1 and I_2 the optimised value of the inductor is obtained. This circuit has two limitation 1.) the circuit has poor linearity 2.) the circuit has poor noise performance. The active inductors are always more noisier then the parasitic devices due to parasitic effects.

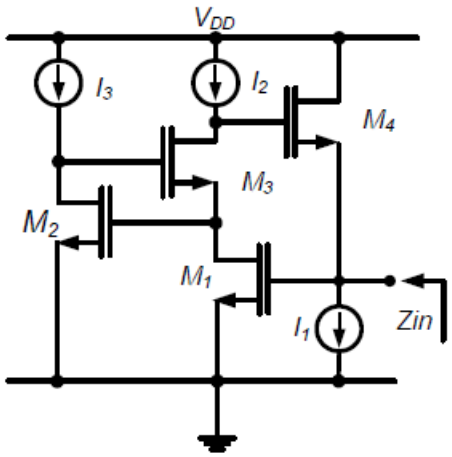


Fig 1.38 Schematic representation of Inductor

ULTRA LOW POWER LNA DESIGN- the conventional L-CS LNA are widely used for narrow band applications having high gain and low noise figure. For low power consumption different topologies are used. But, for obtaining low noise figure design of amplifier becomes stringent. For eg, cascode CS source with inter stage inductor can enhance the gain of the amplifier at the input stage. LNA with a low power of 0.8mW and noise figure of 4.1 dB is obtained. However, due to the requirement of on chip inductors the design results in large chip area. The technique like gm boosting or gain boosting technique enhances the gain of the amplifier and reduces the noise figure. Therefore, it [18] is used for narrow band applications. But this LNA consumes 6.48 mW of dc power and have a noise figure of 3 dB. Therefore this is considered for low power consumption .

Even order distortion significantly degrades the performance of direct of direct conversion Rx. The circuit realised in differential form, exhibits a high IP_2 having mixers and LNA effecting the design of receivers in amplifiers. The noise figure of the circuits gets converted to the differential form. Since the antenna and preselect filters are typically single ended therefore, transformer precedes the LNA to perform single-to-differential conversion. A cascade processes the signal differential from the input port to the end of baseband section of LNA. This transformer is called “balun” balanced to unbalanced conversion when its two ports are swapped.

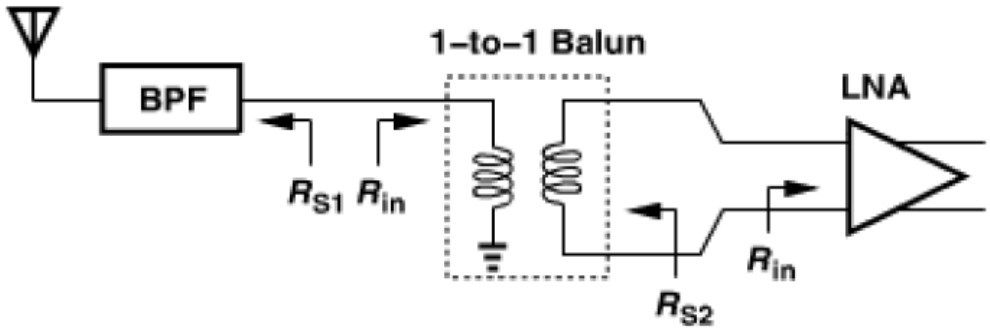


Fig 1.39 Balun Rx I/P

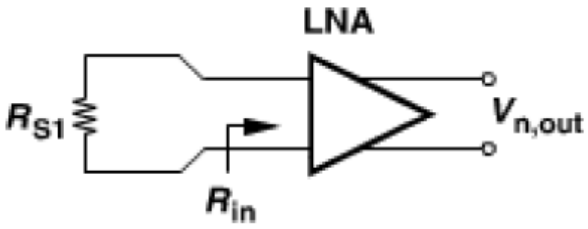


Fig 1.40 Basic Balun Amplifier Circuit

In addition lowering the value of Cgd the input pad capacitance also lowers the values of input resistance. For formulating these effects we consider the circuit consisting of Cgs_1, L_1 and R_1. From the analysis,[19] the observations like lowering the value of f_T is not required for matching impedances R_1=50Ω. Second , the degenerate inductors Rin=50Ω is insufficient to resonate with $Cgs_1 + C_{padd}$. Therefore, another inductor is placed in series with the gate where Lg acts as a off chip inductors.

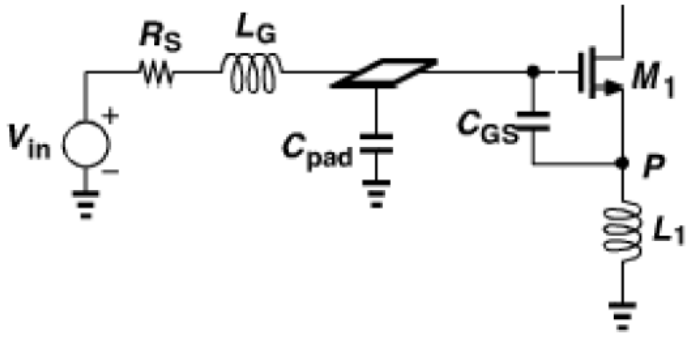


Fig 1.41 Padding of Capacitance

1.6.9 **DIFFRERENTIAL CG LNAs-** After the circuit gets converted into differential form the impedances between each I/P and the ground becomes equals to $Rs_1/2$. That means each CG transistor is providing an input resistance of 25Ω. Now from the symmetry of the circuit the o/p noise is given by summation of each half circuits. The

voltage gain of the circuit reduces to $R_1/(2R_{s1}/2)$ where R_1 is called as load resistance of the CG half circuits. Now, the output noise consist of 1.) input transistor 2.)load resistance contributions ,3.) the source impedances contributions.

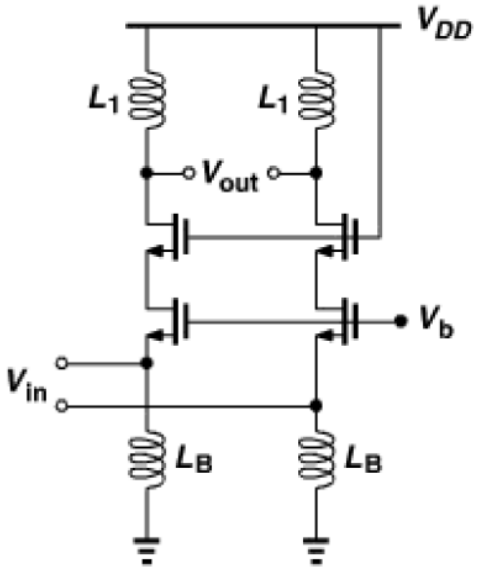


Fig 1.42 Differential CG LNA

the output noise is given by $V_{n,out}^2=V_{n1,out}^2 + V_{n2,out}^2$

$$\overline{V_{n,out1}^2} = kT\gamma\frac{R_1^2}{R_{S1}/2} + 4kTR_1 + 4kT\frac{R_{S1}}{2}\left(\frac{R_1}{\frac{2R_{S1}}{2}}\right)^2. \quad \text{Eq 1.6.14}$$

$$\begin{aligned} \text{NF} &= \frac{\overline{V_{n,out}^2}}{A_v^2}\cdot\frac{1}{4kTR_{S1}} \\ &= 1 + \gamma + \frac{2R_{S1}}{R_1}. \end{aligned} \quad \text{Eq 1.6.15}$$

1.6.10 **COMMON SOURCE DIFFERENTIAL AMPLIFIERS**- the properties of common source differential LNA is different from its common gate counterparts . the i/p resistance of each halves circuits is equal to L_1w_T. the voltage gain of the circuit is equal to $R_1/(2L_1w_0)$ is doubled. Assuming that the width and bias current of each transistor is same as those of single ended LNAs. However, when the i/p is matched half of the noise current from input flows to the o/p node. The transistor contribution is halved due to g_m and hence, the transistor noise currents remain unchanged. When the transconductance of

the circuit gets doubled. The differential output currents contains noise currents of both M1 and M2 equals to $2(KT\gamma gm_1)$.

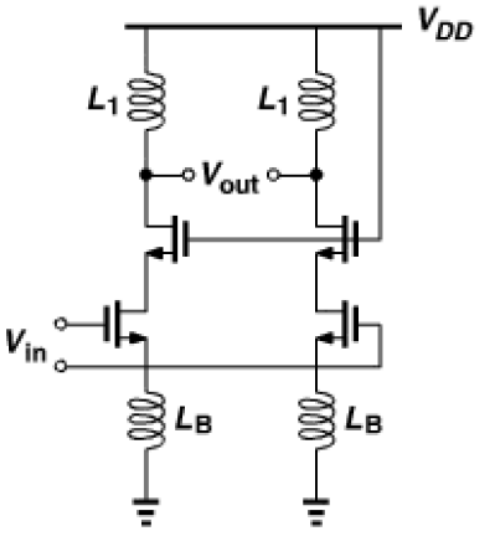
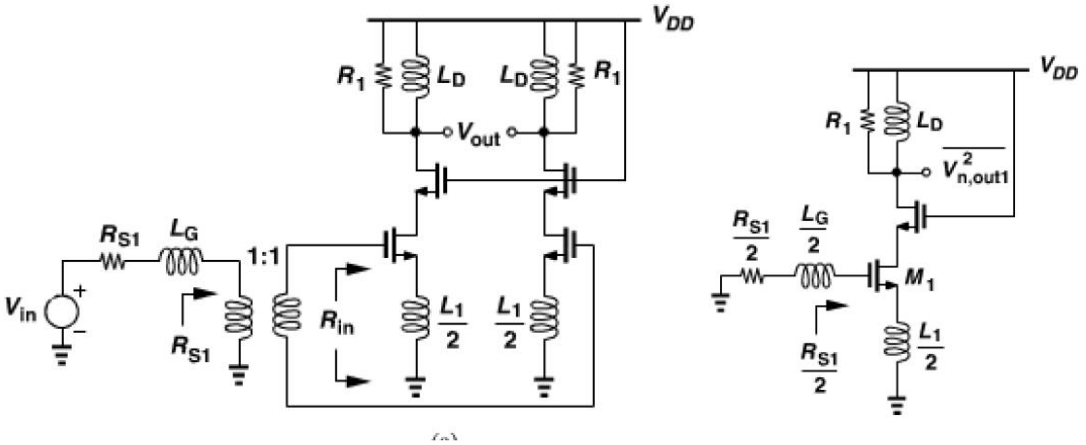


Fig 1.43 Differential CS LNA

$$\overline{V_{n,out1}^2} = kT\gamma g_{m1}R_1^2 + 4kTR_1 + 4kT\frac{R_{S1}}{2}\left(\frac{R_1}{L_1\omega_0}\right)^2$$

Eq 1.6.16



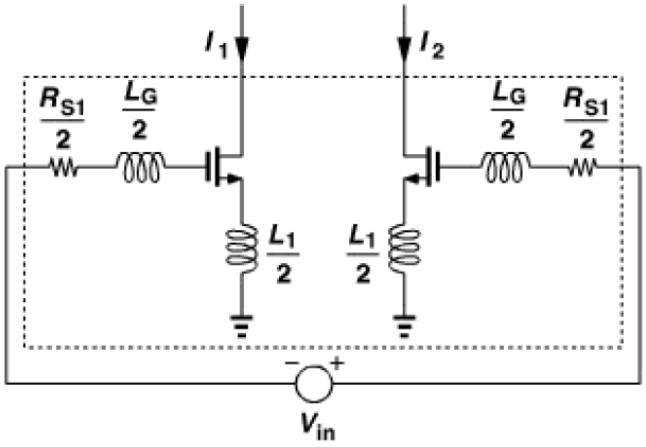


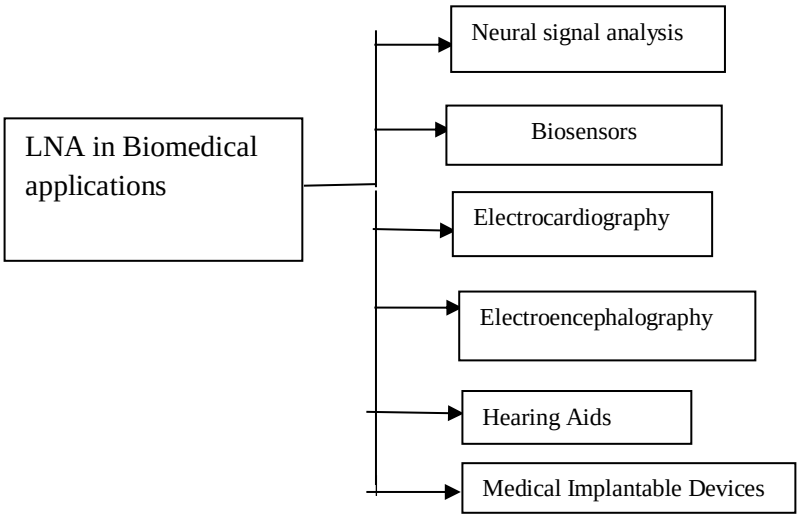
Fig 1.44 Differential CS stage Transconductor

Table 1.6.3 Characteristics of Amplifier

CHARACTERSTICS	COMMON SOURCE	COMMON GATE	CASCODE TOPOLOGY
NF	Lowest	Rises rapidly with frequency	Slightly higher than CS
LINEARITY	Moderate	High	Highest
GAIN	Moderate	Lowest	Broad
BANDWIDTH	Narrow	Fairly broad	Higher
STABILITY	Requires compensation	Higher	Higher
REVERSE ISOLATION	Low	Higher	Higher

1.7 USE OF LNA IN BIOMEDICAL APPLICATIONS

it is defined as combining biomedical and engineering applications into one common domain or reducing the gap between engineering and medicine.



In biomedical applications we deal with weak signals LNA implemented with many topologies like cascode degenerate topology achieves low noise figure and high gain. LNA is required to have low power consumption and small size. For eg- LNA with inductor degenerate topology are less preferred due to large chip area. In[20] full differential RF front end amplifier is designed on 0.13µm CMOS technology for obtaining low power and direct conversion of short range radio signal at low cost.the RF signal is down converted to a baseband signal containing dc offsets and flicker noise corrupting the SNR.therefore (CG-LNA) is used instead of (CS-LNA).Eliminating on chip inductor and provides a good input matching.it also improves stability, linearity and provides robustness against PVT variation in CS topology of small size and low power consumption are preferred in biomedical application. therefore [21] LNA using g_m boost technique is implemented on a 130nm IBM technology and processed providing a good matching of 600Ω and current consumption up to 500µA. in ultra-low power design. LNA with CG topology is preferred as it consumes less power and resistance attaining less sensitivity. In [21] RF front end for biomedical is implemented using ultra low power 401-406 MHz medical Device Radio communication service designed for biomedical quantization application implemented on 0.18µm technology. It uses single ended compatible current-reuse (LNA) . Capable of achieving a power gain of 20 dB with IIP3 of -8.1dBm and noise figure of 2.8dB.the RF front end consist of coupling CCRLNA with

quadrature folded mixer with local oscillator buffer achieves a conversion gain of 28.7dB and NF of 5.5dB consuming less power of 500µW with chip area of 0.7mm^2.

LNA IN NEURAL APPLICATIONS- In biomedical application neural signals are dealt with the learning and comprehensive study of brain function and its healing, curative prosthetic application. Neural signal are interfaced in large number of channels for the study of neurons specifically for brain microcircuits. The entire system consists of dealing with important parameters like noise performance, CMRR and power consumptions. The entire system consist of action potential carrying information to the neural cells.these are formed by the process of polarisation and depolarisation occurring across neural cell membrane or these are caused due to the fast movements of ions across cell membrane. In animal cells the ion's like $Na^+/K^+$are powered by ATP molecules forming basic building blocks in animal cells. Whenever channel consist of ions are activated electrically or biochemically through mechanisms like depolarisation causes voltage sensitivity resulting in the opening of ions membrane containing Na^+ to open first the arrival of large number of positive charges across cell increases potential rapidly. However, the balance is obtained by the inflow of K^+ ions across the cell membrane. For getting sneak peak for action potential an amplifying method is required.the neural amplifier should reject the dc offsets of the resulting signal amplitudes. The amplifier should have have high (SNR) and proper CMRR and PSRR.the majority of neural amplifier successfully extracts I/P referred noise between 3-7µVrms. Without the controlling mechanism the system is dominated by noise. . the main component of noise are mainly from muscle contraction affecting neural recording and intensifying brain activity environmental noise includes the noise from radio and electrical signals which degrades the performance drastically. The main noise are thermal and flicker noise caused by intrinsic property of the semiconductor. The LNA implemented with (OTA) topology with two stage op-amps and current mirror OTA's. the folded cascaded combinations. is implemented in different modes should have considerably large phase margin and swing margin. The LNA implemented with capacitive feedback topology. These are optimized with very low noise power. These are operated through a dedicated circuit design topology. the desired architecture achieved a gain of 39.5dB, power consumption of 80µW and NEF of 4. In [22] achieved a modified and optimized capacitor feedback topology having a power consumption of 7.92µw and I/P reffered noise of 3.5µV_{rms}. LNA implemented with Active feedback topology a segment of

filtered signal is used as a feedback for suppressing a signal component. this is one of the efficient way of extracting the low frequency component of a signal which makes it a very stable system. This topology is mainly used in EEG biomedical application. LNA implemented with a MOS bipolar pseudo resistor(implemented using a cross coupled configuration) are used for implementing AC coupling and rejecting the large DC offsets caused due to contact potential.every transistor in MOS diode is connected such that a parasitic source-bulk diode is obtained in anti-parallel now if the voltage across the device is small then neither of the diode conducts since the effective resistance is very large.>(10GΩ) so for minimizing the I/P reffered noise two strategy are adopted.first amplifier is reduced to a single branch which is operating at a full current.the reference current so obtained is found to be 10 times the amplifier bias current which do not contributes in the total power consumption.

LNA IN BIOSENSORS APPLICATIONS - The term 'Biosensor' is a short for "biological sensor" the device consist of transducer and biological elements consisting of enzymes,antibody or nucleic acids. The bioelements interact with the analyte being tested and biological response are converted to electrical signal by transducers.the biological response of biosensors obtained are examined by biocatalytic membrane achieving the conversions of reactant to the product. Immobilised enzymes provides a large number of advantages making them applicable for biological systems. These can be reused ensuring catalytic activity for a series of analyses. thus, biosensors are widely used in the field of healthcare, medical diagnosis, etc. in [23] CMOS on chip sensor is used for measuring the dielectric constant of an organic chemicals .the dielectric constants is measured by changes observed in the tank capacitance producing LC oscillation in VCO due to the exposure to the liquid. VCO is placed in a frequency synthesisers frequency change causes change in the voltage measured using on chip digitised analog to digital converter.the calibration of sensor is used for the measurements of dielectrics.the measurements are made in frequency ranging from 7-9GHz. The advancement in wireless communication and network technologies has lead to the significant advancement in wearable and implantable sensors creating an impact on e-health and telemetry systems. m-health biosensors comprises of mobile computing,medical sensors and communication technologies.for diagonsis and monitoring of diseases .for eg diseases like diabities a large number of biosensors are worn and implanted.the interconnection

are made inside a human body and the entire system is called BASN body area sensor network performing two operations.

1.) The transmitting of processed data.

2.) A secured channel for transmitting of data between human body and biosensors placed at the same node.

The BASN differentiates between the individual based on their pyscological and behavioural characterstics.

The BASN differentiates between the individual based on their pyscological and behavioural characterstics.

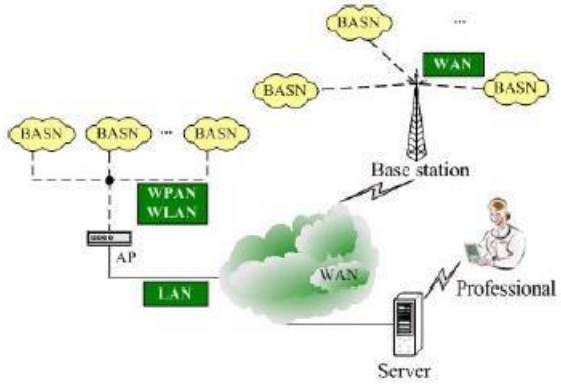


Fig 1.45 BASN Network

LNA IN ECG SIGNALS- Biomedical signals is the study of physiological activities of organism produced by gene and protein sequences observed in neural and cardiac pattern. the well known biosignals are (ECG),(EEG),(EMG) and (MMG). ECG is the acquisition of electrical activity observed from the heart captured by the electrodes attached to the skin. these are very weak signal produced during strenuous or ambulatory conditions and because of this weak nature noise gets added for which signal processing is required. The ECG or electrocardiography signals are produced due to the potential difference between the two electrodes and since these are recorded for long time the compression of data is required both at transmitting and receiver ends. The contraction of the muscles and cardiac pattern ECG signals are coupled with noise.therefore filtering is not possible.

To solve ensembled averages techniques for time aligning heartbeats and reducing muscle noise is used. The three algorithm applied are

- Stress testing
- Ambulatory monitoring

- Intensive care monitoring

For the purpose of monitoring ECG signals. In [24] The low power and compact wearable sensors are designed. The signals are wirelessly transmitted and monitored using ECG filtering and QRS detection methods which carries less number of bits for transmission. LNA with differential topology is implemented using successive approximations(SAR) ADC using 2 SPI interfaces and on chip SRAM having central control unit of 8 Kbits.

The ECG signals are sampled at a rate of 256Hz using QRS complexes and the ECG signals are then continuously wrote on asynchronous FIFO and are forwarded to CPU thus consuming less power. In [25] the bio signals obtained with Nyquist rate are reproduced without degrading the characteristics of the bio signals the low power bio signal is provided at analog front ends of the amplifiers having a bandwidth with a dynamic range of (40-70 dB).

The conditioned bio signal is received by the encoder from a low noise amplifier and compression of N I/P sample gives M O/P samples which are digitised and transmitted using ADC.the RF front elements are made to operate at Nyquist having a conversion factor of [N/M] which is greater then 1 and these signals are down converted at O/P y(t).

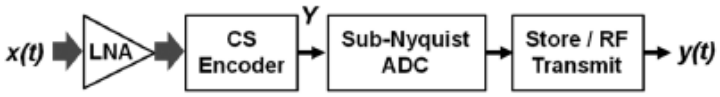


Fig 1.46

LNA IN EEG APPLICATIONS- The EEG signal which stands for electroencephalogram is a signal produced due to the electrical activity of the brain and recorded from the scalp. the recorded waveform consist of cortial, electrical activity. These are very weak signal and measured in microvolts. The main frequency of the human EEG wave consist of

- Delta[frequency of 3 Hz or below]
- Theta[frequency of 3.5Hz and 7.5Hz]
- Alpha [frequency between 7.5 and 13Hz]
- Beta [frequency> 14 Hz]

Since these are weak signal the voltage fluctuation measured at the electodes are very small,the recorded data is digitised and sent to LNA. The LNA processes data which is then displayed as a sequence of voltage values. This is one of the fastest imaging techniques having high sampling rate.

In [26] EEG are examined using HHT(Hibertz-Huang Transform) process. For this a de-noising process is applied for smoothening of EEG signals and based on EMD(empirical mode decomposition) and Monte Carol process. The EEG signals are filtered with Hilbert -Huang transform process and crucial information are extracted based on the results obtained in the form of Hilbert spectrum. Through simulation it is explained that EEG processing with some unique advantages can be obtained.

LNA IN HEARING AIDS APPLICATIONS- Hearing aids comprise of electroacoustic devices. Typically worn in or behind the ears and modulating sound for hearing impaired. The microphone transforms sound to electrical signals which on further amplification is converted back to the sound by receiver the entire process is powered by a source of a battery.

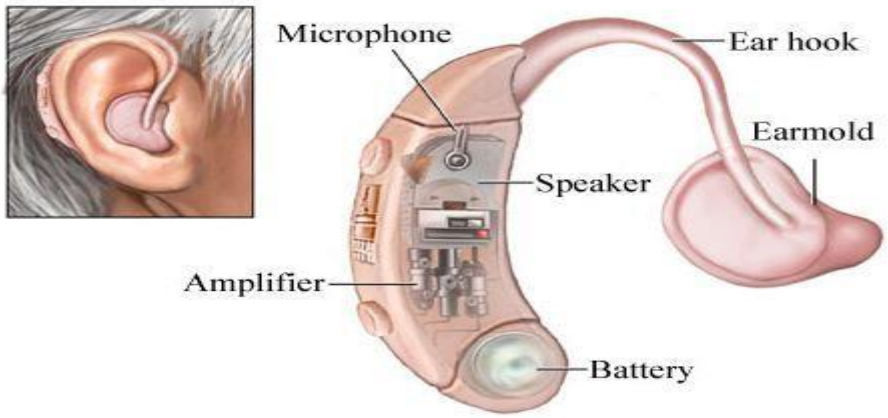


Fig 1.47 LNA in Hearing Aids Application

In [27] binaural hearing aids are designed such that they can communicate wirelessly to both multimedia devices and smart phones.in this paper a wireless multimedia device along with a customised Bluetooth device with adapter is designed. It is provided with a fitting parameters controlling process which can control volume of the hearing aids using graphical user interface. thus, a system designed is efficient enough without any controlling mechanism. the wireless communication control panel is designed using a FPGA kits implemented using a DSP processor.

LNA IN RF FRONT END APPLICATIONS- the designing and development of high performance RF transceivers or reconfigurable receiver for a novel and unconventional RF front end application is tough task. The performance of the system can be improved by increasing supply voltage, width and additional circuitry at the o/p stage. But this causes increases in size and power consumption.in [28] LNA is designed with high performance and low operating voltages of 1.8 V on TSMC 0.18µm using an intel core 2 duo CPU E7400@ 2.80 GHz processor in ADS.

In the RF receiver, boosting of the incoming signal is performed by the amplifier before the process of frequency conversion this step is important and prevents the mixer from dominating the noise performance of the front end of the amplifier. Therefore, the specification of the RF amplifier is determined from gain, third order intercept point and noise figure. LNA is supposed to have low noise figure and high gain otherwise a strong inband interference will desensitizes the circuit. This process is called blocking and the interfere is called blocker. In recent years, the wideband LNA are more preferred then narrowband LNA as wideband can be used for multi-band frequency ranges. A narrowband LNA is preferred for stable performances over a frequency range of MHz. for eg- GSM applications for reducing interference and distortion LNA with a moderate gain is preferred. While in GPS the gain and noise figure are given more priority then linearity which should be around 20 dB. Similarly for personal area communication (PCS) LNA with high linearity and moderate gain is preferred. For WCDMA application linearity is important factor it should have IIP3 ~0 dBm and power consumption of less then 5 mW whereas LNA for WLAN can have moderate gain and noise figure and power consumption of 10 mW.

Table 1.7.1 Comparison of Work

References	[32]	[29]	[36]	[22]	[24]
Frequency(GHz)	1.23	1.9	0-2	3-5	0-2
Applications	(GPS)	PCS 1900	Wideband	UWB	Wideband
Noise figure	0.8	1.8	2.4	2.3	0.8
Peak gain	20	15	13.7	9.8	0
Dissipation(mW)	9	25	35	12.6	12.6
Bandwidth	1.0	1.7(GHz)	0(Hz)	2(GHz)	0(Hz)

CHAPTER 2 LITERATURE REVIEW

1.) In [29]" Design of Low Power Direct Conversion RF Front-end with Double Balanced Current Driven Subharmonics-Mixer in 0.13µm CMOS" by Yiannos Manoli et.al has presented LNA with cascade inductor with degeneration topology provides higher gain and low noise figure. In fig(1)a fully differential RF-front end is designed and implemented using 0.13µm CMOS process. this design is espically obtained for Low-power and low-cost for direct conversion of short range radio signal for biomedical applications.this is implemented on a 380*380µm^2 active chip area.the RF signal is downconverted. To a baseband signal which contains dc-offset and flicker noise Which corrupts the SNR.in the received path. therefore in this topology(CG-LNA) is employed instead of (CS-LNA)as it eliminates the use of on-chip spiral inductor which is useful for I/P matching .it also provides superior bandwidth ,linearity ,stability and robustness to PVT variations obtained in CS topology.

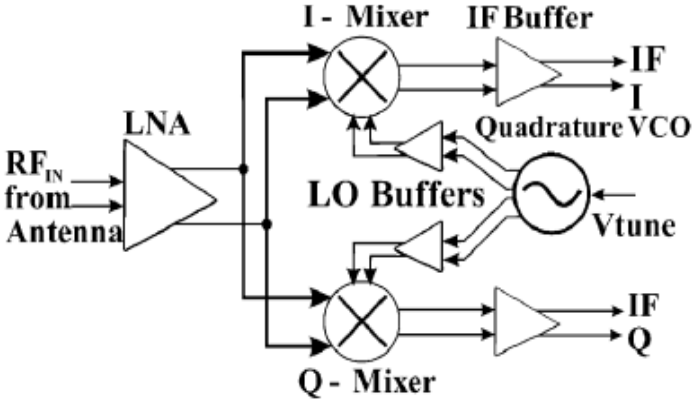


Fig 2.1

2.) In [30]"Improved Design of Low Noise Amplifiers" by A.Hameed .et.al has presented LNA for wireless communication system. LNA is a crucial element in RF receiver which amplifies the gain of the amplifier and the noise contributed by the components of the RF transceiver system. Therefore, LNA is implementation with different topologies is obtained with high gain, low noise figure and small chip area and input and output matching n/w. The active inductors are used for low power consumption and chip area in layout design.

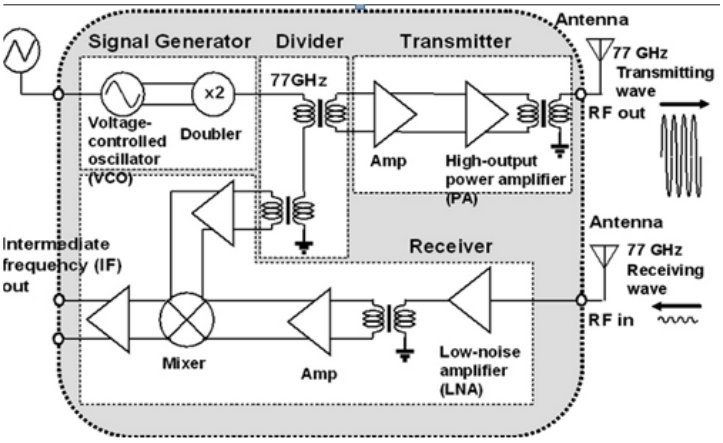


Fig 2.2

3.) In ref[31]" the design of LNA in nanometer technology for WI-MAX applications" by P.Kavyashree.et.al LNA is implemented on CMOS technology from 0.13µm to 0.18 µm by varying the size of transistor on CADENCE software having the supply voltage of V1=1.1, V2=0.6,V3=0.6 and Vgg=0.7V. the circuit attains the gain of S_{21}= 15.2dB and decreasing Vgg=0.5 V and increasing V1=1.2 V having a N.F. of 7dB and power consumption of 0.8mW with a chip area of 0.26mm^2 with good I/P and O/P matching.

4.) In ref[32] "A 280µW Sub- threshold Balun LNA for medical Radio using current reuse-technique" by K Vasudev Reddy et.al LNA is designed using g_m boost technique and having I/P impedance of 600Ω. And the current obtained is below 500µA for ultra –low power design. this is implemented on a 130nm IBM technology and simulated. The LNA implemented using CG topology attains less sensitivity drastically reducing power consumption and resistance.

5.) In ref[33]"In ref[10]"Low power 2.4 GHz transceiver in wireless sensor network for biomedical applications" by chiung et.al a wireless transceiver system is implemented using LNA for developing of network system which functions as a link budget for low power design. The low power system design so obtained will reduce a lot of power consumption but the low power system so designed occupies larger area but results in installation problem therefore transceiver system so designed is installed at 60GHz frequency.WSN is configured in indoor environment separated by a 10m distance. signal bandwidth so obtained depends upon sample rate and resolution.WSN operates by sending biomedical signal from sensor node and the signal are merged by MCU and are further converted by ADC and transmitted through 2.4 GHz band to the collecting point tuned at 60GHz.

6.) In [34] “Low noise OTA for neural amplifier applications” by Saberhosseini.et.al LNA is implemented with transconductance amplifier and current mirror OTA’s folded cascode topology allowing larger swing margin or reducing supply margin. The LNA achieves a gain of 40.5 dB NEF(4.5) and power consumption of 12.5 µW having a chip area of 0.05 mm^2.

Table 2.1 Comparison of Different Topologies

Topology	Power consumption(µW)	NEF	Mid Band Gain(dB)	Area(mm^2)
Telescopic-Cascode Closed loop amplifier	12.5	4.5	40.5	0.047
Complementry I/P Open Loop Amplifier	0.8	1.9	36	0.046
Complementry I/P Closed Loop amplifier	12.1	2.9	40	0.072

7.) In [35]” A Sub-Microwatt Low- Noise Amplifier” by Brian Otis.et.al a pre-amplifier for neural recording is designed LNA is implemented in open loop configuration for achieving extremely low power dissipation and current re-use technique the LNA exhibits 3.5 µVr.m.s having a digitally controlled gain between 36 to 44dB. The circuit is implemented on 0.5 µm SOI-BICMOS process and consuming 805nA from 1.0 V supply and attaining a NEF of 1.8 which is lowest so far for such topology.

8.) In [36]”combined LNA and mixer circuits for 2.4 GHz ISM band “ by Seese.T.M.et.al is implemented with low area and low power it uses narrow band cascode LNA with inductive degenerate using a single balanced mixer. When both circuits are integrated in the same receiver as shown in fig [48], the LNA uses transistor M1 to convert the input voltage into a current, that is re-converted to a

voltage by the output load. This voltage, that feeds the mixer input, is again converted to a current that will be mixed with the local oscillator signal (VCO). The mixer down-converts the RF current by switching the current from one side to the other at the LO frequency. Thus, the use of the two circuits of figure 1 as separate blocks requires two conversions, one from current to voltage at the LNA output, and the other from voltage to current at the mixer input.

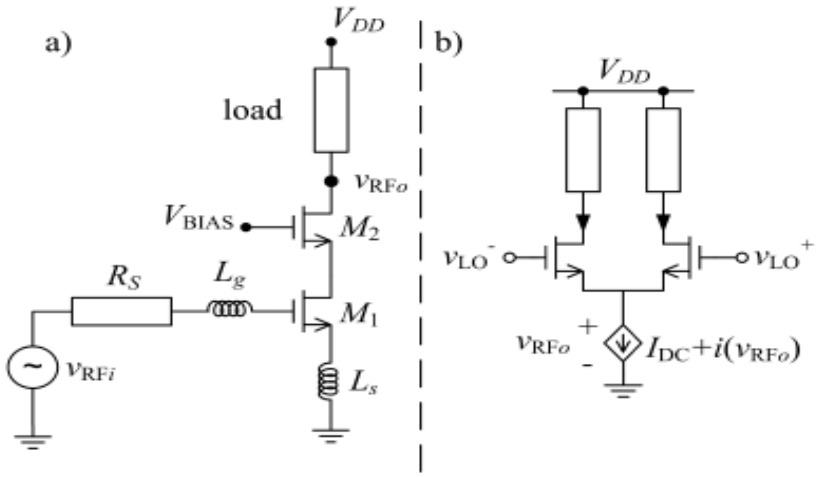


Fig 2.3

9.) In ref[37]" design and analysis of low noise amplifier for ISM band application" by R.Harrison.et.al is implemented .it used GaAs FET amplifier for attaining low noise figure and high electron mobility transistors providing good input and output matching this was implemented in ADS at 2.4 GHz band attaining noise figure of 0.21dB input return loss S_{11} of -21.49dB and output return loss of -21.46dB.

10.)In ref[38] "current re-used ultra –low power amplifier low noise LNA " by Viet Hoang.et.al is implemented along with a mixer at 2.4GHz zig bee band at 0.18µm technology to obtain a voltage gain of 21dB and 6dB noise figure at 300KHz flicker noise frequency and average current of 0.9mA at 1.8V and consuming 1.6mW of powers.

11.)In ref[39] "A low power low noise VCO and a high gain LNA for WSN applications" by Arnav Mukherjee.et.al focuses on two core building blocks of WSN systems.the system consist of LNA and VCO these two blocks are designed and simulated at 2.4GHz ISM band implemented using 130nm RF technology this method uses inductive source degeneration to design LNA attaining a noise

figure of 0.472dB and gain S_{21} of 15.390dB.this circuit designed is found to be stable between 1GHz to 5GHz.the VCO is designed to have a low phase noise of -130dB at 1 MHz with a low power consumption of 0.023mW which is good for WSN applications.

12.) In ref[40]"a high gain high linear LNA for low power receiver front –end applications", this paper uses UMC 0.18-um technology based on cascode topology adopted with gain boosting Technique. To improve linearity feed forward cancellation (FDC) technique is used.in this LNA cascode topology is commonly used (as shown in fig 3) followed by CS stage cascoded with CG stage in the same DC paths .for implementation of the circuit and attaining high input impedance matching pi-matching is adapted because comparative to T matching pi- matching have good power gain. which enhances power gain so that at low power reasonable linearity can be achieved, the degraded gain due to improvement in linearity is compensated by gain boosting technique. The LNA is designed for 2.4GHz ISM band applications. It is consuming 2.6mW power from 1V power supply by giving S11 = -13.9dB, S21 = 20.98dB. The Noise figure is 4.2dB and IIP3 is -5.17dBm.

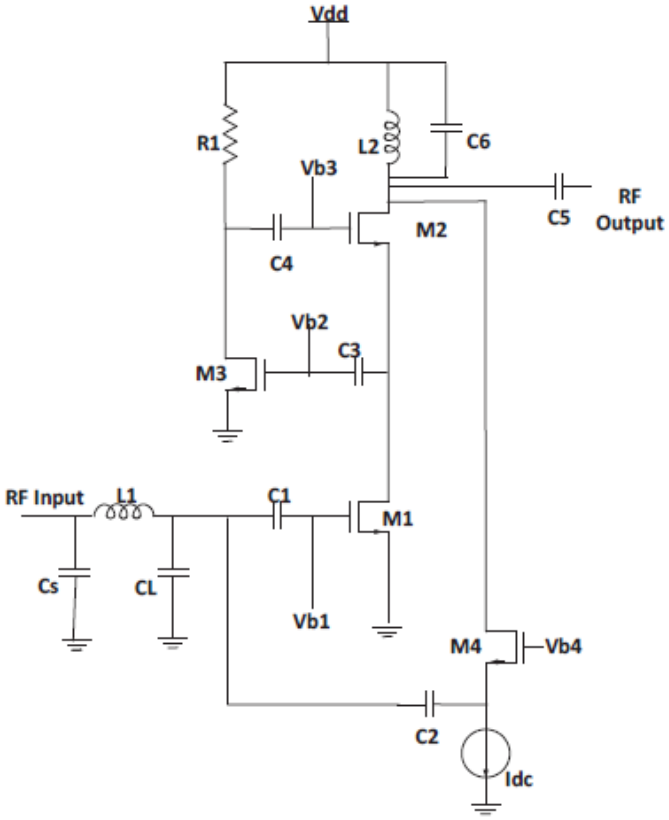


Fig 2.4 schematic of proposed LNA

13.)In ref[41] ”A low power low noise CMOS amplifier for Neural Recording Applications” by Harrison .et.al implemented LNA with capacitive Feedback topology for neural application . for controlling power consumption a feedback loop is provided for controlling the linear response a small chip scaled capacitor with a MOSFET based resistor creating low pass response. The circuit achieves a gain of 39.5 dB and a power consumption of 80µW and NEF of 4.

14.)In ref [42]”A low power 2.4 GHz Receiver for Wireless Implantable Neural Stimulators” by S.A.Mirbozorgi .et.al presented a low voltage, low power 2.4 GHz CMOS OOK receiver which includes a modified current reuse two common source LNA implemented with a gilbert topology providing enhanced gain and noise figure. After simulation digits 0 and 1’s are obtained at time instants of 10 nsec. This means that the receiver successfully operates on OOK data at 100 Mbps. The system operates at a frequency between 2.4 and 2.5 GHz and a circuit exhibits a gain of 15 dB a noise figure of 1 dB and S_{11} of -16dB. CMOS implemented on a 0.18µm CMOS technology attaining a speed of 100 Mbps. The circuit consumes power of 7mW. The entire circuit occupies an area of 0.38mm^2.

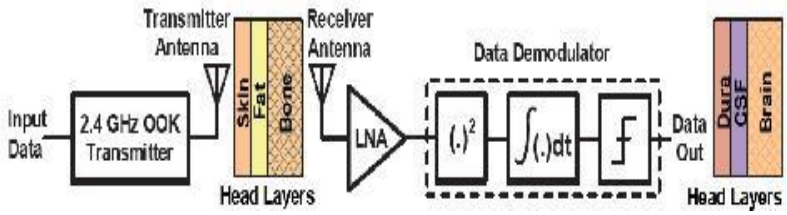


Fig 2.5

15.) In ref [43] “A Low Power Low Noise Amplifier for Biomedical Applications” by Deepansh Dubey et.al the amplifier is implemented with a EKV model for setting a bias current for the transistor. For minimising flicker noise, PMOS transistor in weak inversion mode and large gate area is implemented. The use of switched biasing causes transistors to periodically switch between accumulation and inversion region. This allows reduction in the I/P noise without increasing the currents. Thus, reducing the flicker noise of the transistor. The circuit achieves 2.89µVrms in the desired bandwidth having a power consumption of 15.174µW. the gain of 76.2 dB with a phase margin of 74^0 and CMRR >120dB at all

frequencies. The entire circuitry is simulated on cadence virtuoso at 36.9 ^{0}C temperature with all the process corners TT,FF,SS,SP and FS.

16.)In ref[44] "A wireless wearable ECG Sensor for Long Term Applications" by Ebrahim Nemati .et.al proposed a model of health care ubiquitous sensing using wireless medical sensors providing flexibility to the conventional method. A wearable ECG sensor is proposed. The ANT protocols enables-low data rates reducing power consumption and size of the sensor capacitive ECG sensing avoids direct contact with skin providing maximum convinence to user. In this a cotton T-shirts integrated with signal processing and transmitting board with printed circuit board design. The entire system is small, thin and consumes less power then ECG monitoring system. The ECG signals are compared with conventional glued electrodes and interpreted by cardiologist.

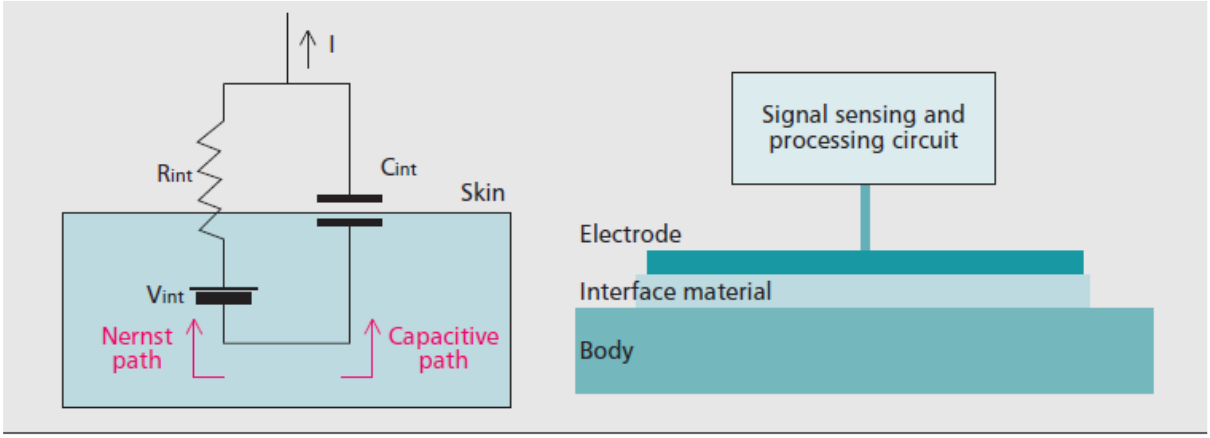


Fig 2.6

17.) In [45] "An Ultra- wearable, Wireless and Low Power ECG Monitoring System" by Chulsung Park .et.al. states that in today's wearable electrocardiograph(CG) monitoring system requires skin preparation with gels and pastes providing electrical contacts with skin. These are not preferable due to high noise spikes appearing in the data. A wearable and ultra low power wireless sensor called eco is presented. Experimental results states that the wireless interface sensors provides minimal size and weight to the system providing reliable and unethered operations. These have high performance compared to gold standard ECG electrodes.

18.) in [46] " Compressed Sensing Analog Front -end for Biosensors Applications" by Daibashish .et.al states that in a conventional Bio-sensors, key signalling features are acquired using Nyquist rate analog to digital conversions without exploiting the

the typical bio-signal characterstics in some domains e.g.(time,frequency) compressed signal is a signal processing prototype exploiting the sparsity for proportional alias-free sub Nyquist acquisition by enabling the power saving. A severe energy constrained sensor eliminates the need for digital signal processing (DSP). A fully integrable low power CS analog front end (CS-AFE) is used as electro-cardiogram sensors) switched capacitive circuit having high accuracy and low power is preferred. It is implemented on 0.13µm ($2*3mm^2$) prototype comprising of 384 bits Fibonacci – galois hybrid linear feedback shift register having 64 – digitally selected Fibonacci-galois hybrid linear feedback shift register with 64 digitally selected CS channels with 6-bits C-2C MDAC/integrator having a clock frequency of 2 KHz, power dissipation of 28 nW and 1.8µW for one and 64 active channels. (CS-AFE) comprises of compressive sampling of biosignals that are sparse in arbitrary domain.

Fig 2.7

19.) in [47] "A self -sustained CMOS Microwave Chemical Sensor using Frequency Synthesizer" by Ahmed A.Helmy .et.al presented a on-chip CMOS sensor for measuring dielectric constant of organic chemicals measured by oscillation of LC voltage controlled oscillator(VCO) caused due to change in the tank capacitance VCO embedded in a frequency synthesizers for converting frequency shift into voltage that can be digitized with on chip analog to digital converter. The dielectric constant of different organic liquid is measured in frequency range of (7-9)GHz with an accuracy of 3-7% compared with the sample volume of (10-20 µL). the sensor is capable of estimating fractional volume of constituting material with 1%-2% accuracy.

20.) In [48] " Biomedical Digital Assistant for Ubiquitous Healthcare" by Tae-Soo Lee .et.al presented the concept of Ubiquitous healthcare services emerged as one of the measure for solving healthcare problems in aged society that the person can receive messages and concern on prevention, diagnosis, therapy and prognosis management at any time and place with advance information and communication technology. This service provides not only biomedical digital assistant but it also continuously monitors patient health conditional regardless of time and place. But with the help of telemedicine server doctor can monitor data on patient present health conditions. The

device implemented and fabricated is capable of measuring ECG and PPG signals having minimum size, weight and power consumption it is capable of operating 24 hrs with high portability and wearable it can measure heart rate, step counts and respiratory rates. The biomedical signal receiving devices is implemented in PDA and cellular phones however PDA operating system operates for only 6 hours. This problem is sorted by decreasing the loading capacity and storage functions of sensors. The device is helpful for cronic- aged persons.

21.) in [49] " A High Efficiency Differential 60 GHz VCO in a 65nm CMOS technology for WSN Applications" presents a differential voltage controlled oscillator (VCO) implemented on a 65nm bulk CMOS technology for the unlicensed 60 GHz band. The system achieves a efficiency of 4.9 % with a maximum differential O/P power of -0.9 dBm drawing a current of 16.5 mA from 1V supply. The VCO is perfectly suitable for fully integrated 60 GHz transceiver battery powered wireless sensor networks. The minimum phase noise is -90.3dBc/Hz at 1 MHz offset and -112dBc/Hz at 10 MHz offset measured tune range reaching 57.6 to 60.8 GHz.

CHAPTER 3 EXPERIMENTAL WORK AND RESULTS

In this chapter, the schematic design of LNA on ADS (advance designing software) is presented. The LNA is implemented on 45nm and 180 nm TSMC technology. The circuitry of LNA is divided into 5 parts a.) topology b.) I/P and O/P matching network c.) source degenerate topology d.) biasing circuits. The important factors such as S-parameters, NF, IIP3, stability are obtained from simulation and power consumption is calculated. The LNA is implemented for RF Front end applications of the systems.

The most common topology is cascode topology which provides high stability, perfect I/P and O/P isolation minimum noise figure. The circuit with cascode topology and matching network is represented by-

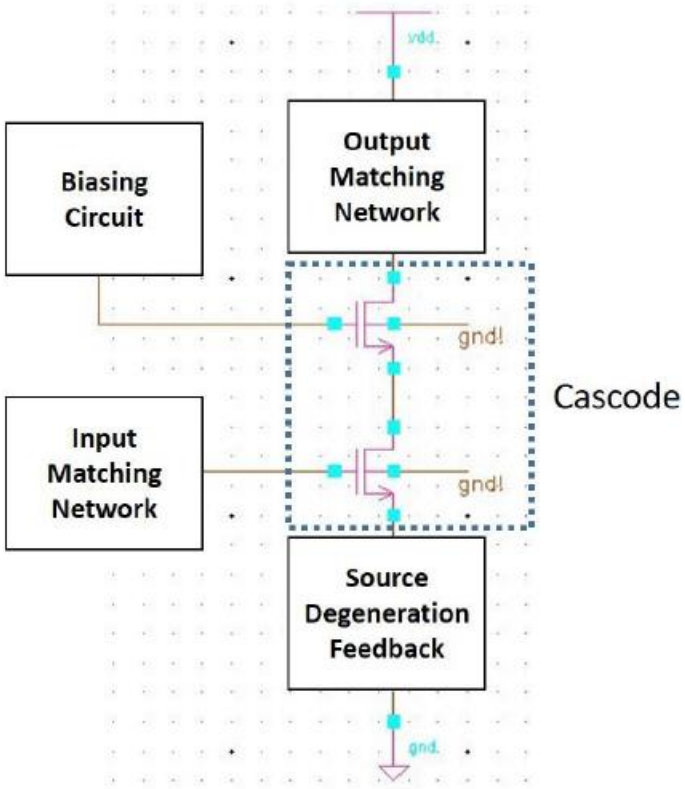


Fig 3.1

3.1 **SOURCE DEGENERATE FEEDBACK**- It is implemented by placing a source inductor (Ls). The purpose is to obtain optimised admittance (Yopt) and concurrently converging I/P admittance (Yin) represented in smith chart. Yopt is the input admittance point with minimum noise factor(NF). The value of Ls is calculated and optimised to avoid instability in the system due to small and large feedbacks. The smith chart is used

for obtaining Sopt and its Gin and Gout conjugate for maximum gain and NF cannot be calculated for same impedance state. Overall source degenerate improves linearity of LNA and stability for some amount of gain.

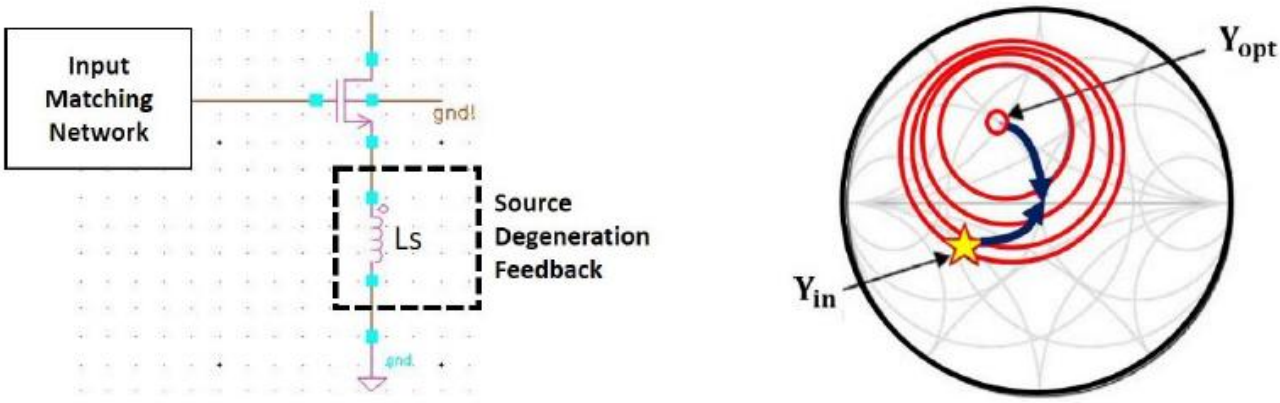


Fig 3.2

I/P matching network achieves the maximum power transfer rate this happens only when impedance matching is obtained. The LNA connected to a voltage source receives a signal from antenna and then its simulation is performed. The source impedance of antenna is specified as 50Ω. Therefore, for maximum power transfer the source impedance of LNA should be equal to 50Ω.

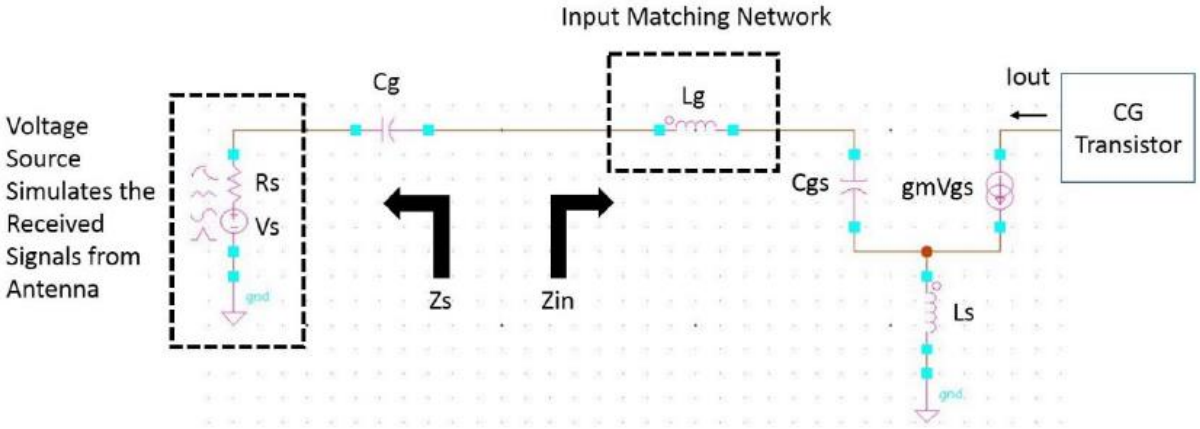


Fig 3.3

For obtaining the O/P matching network proper I/P matching for max power transfer need to be specified. Not only Zin but Zout has to be equal to 50Ω. With real part equal to 50Ω and imaginery part equals to 0 causing a circuit to resonate at a particular frequency.

Therefore, O/P matching network consist of resistance (Rd), Capacitive (Cd) and inductor (Ld).

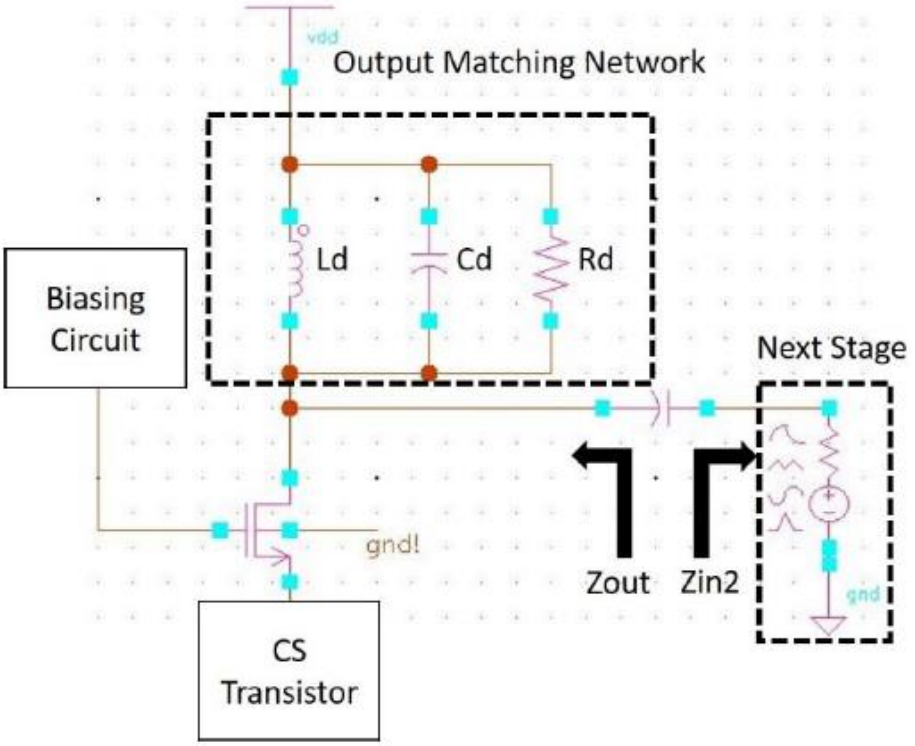


Fig 3.4

3.2 **BIASING CIRCUITS USING CURRENT MIRROR**- For BLE, low supply is needed so that the system can operate for longer periods without charging. The circuit should have a power consumption close to 1 mW. The supply voltage is generally set to 1V providing biasing two transistors (CS and CG). The circuit is implemented to have a current flow close to 1mA. For eg- in above diagram transistors M_3 and M_1 forms a current mirror. The ratio of the current flowing through two transistors depends upon the width of M_2 and M_1. The I_{bias} denotes the reference current and Ids denotes current through the cascode combination of M_1 and M_2. For constraining the power consumption to 1 mW . the designing of I_{bias} is according M1,M2 and M3 operating in saturation mode. The current equations for M3 transistor operating in saturation mode is given by

$$I_{bias} = \frac{1}{2}\mu_n C_{ox}\frac{W_3}{L}(V_{gs3} - V_{th3})^2$$

Eq 3.2.1

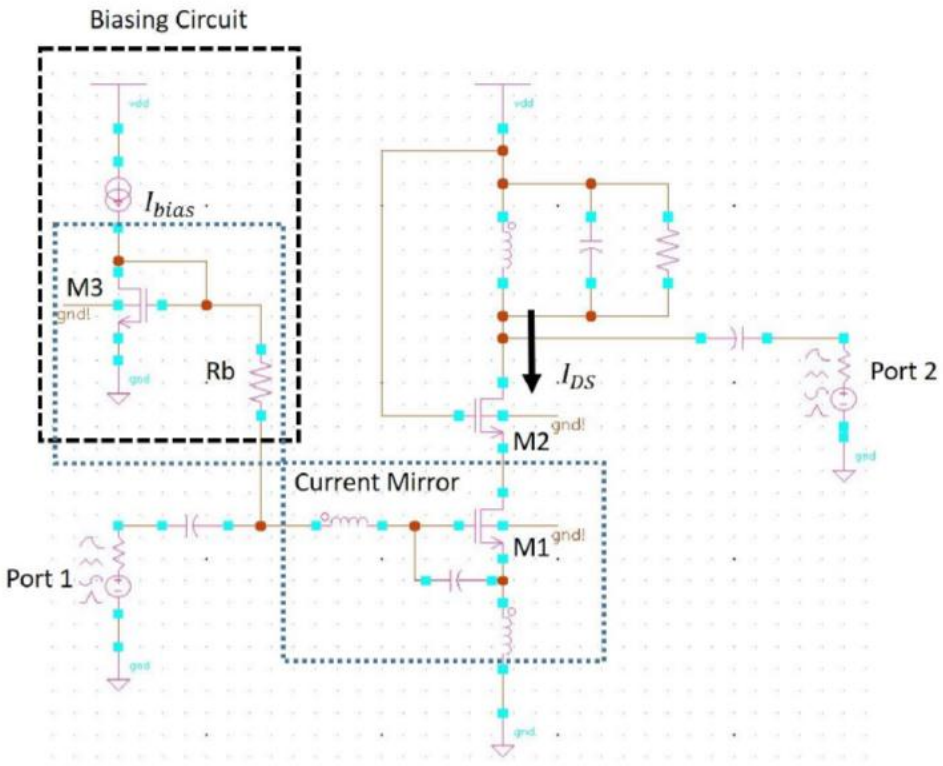


Fig 3.5

Now , in the schematic LNA with high Linearity Low power cascode CMOS LNA for RF front End Application is presented. In todays scenrio the need for wireless application devices has increased tremendously one of the major wireless application is bluetooth which requires low energy devices these devices are ecofriendly devices that are developed for facilitating “internet of things”these devices are found to be having less power consumption and energy.bluetooth IEEE 802.15.4 [50] holds the capability of becoming the choice for setting the adhoc network in the future because of its key features of low power consumption and potential low cost.bluetooth low energy devices are used in 2.4GHz (ISM)band or unlicensed band that are internationally reserved radio spectrum intended for scientific medical and industrial requirements.

LNA (low noise amplifier)plays a key role in radio receiver performances.the [51]receiver performance is measured in terms of receivers sensitivity,selectivity or proclivity to reception errors the RF front end performance is determined by the first active device in the block.there are 5 characterstics of LNA that are directly under the designers control and directly effecting receivers sensitivity.these are linearity,bandwidth ,noise figure ,Gain and dynamic range of operation controlling these parameters requires

sufficient knowledge of active devices ,impedance matching and method of assembling and fabrication of amplifiers and achieving optimal performance with fewer tradeoff.

Organisation of this paper is as follows.Section II gives the brief discription of the topologies,feed forward cancellation method and matching circuits .Section III describes the circuits and simulation results and comparison of work.Section IV conclusion is given.

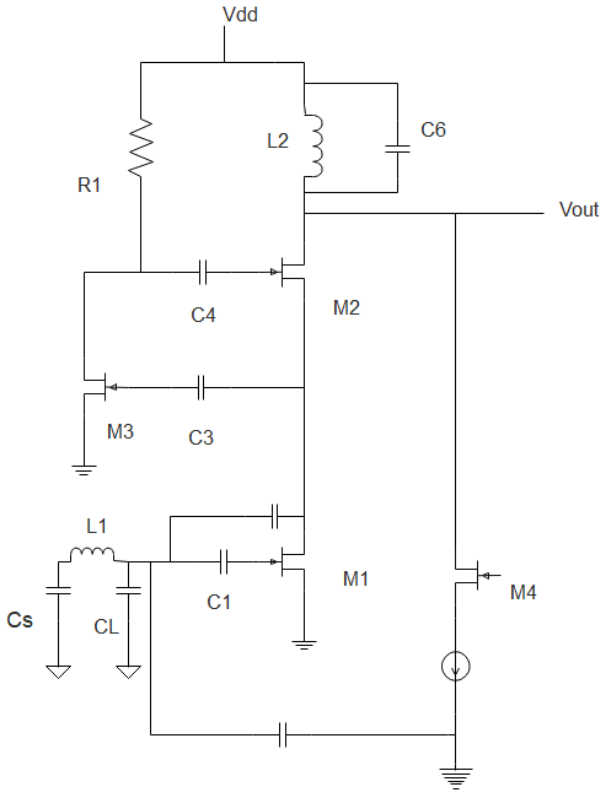
3.3 CASCODE LNA TOPOLOGY

LNA cascoded topology consist of connecting the two mosfets one with common source topology cascoded with the common gate topology of the other mosfet following the same DC path.the cascoded topology is preffered when the isolation between input and output is required which improves the stablity of the circuits cascoded topology provides better stability,better noise figure,higher gain,better reverse isolation and inependent input and output matching.gain boosting technique is the method of increasing the gain of the amplifier by amplifying the transconductance and increasing the power gain of narrow band RF (LNA) by using the negative resistance obtained from the cascode combination.the noise factor[52] can be improved by increasing the transconductance that leads to the method of reducing the input resistance and noise factor the g_m boosting technique effectively limits the power reduces noise and enhances the gain simultaneously.

While designing LNA[53] one can achieve high gain,low noise with low linearity when operated at low desired signals or high linearity low gain and large noise figure with large signal interferences.therefore,feed forward cancellation method is adopted which involves the method of adding an auxillary amplifier and its effect on the signal and noise voltage obtained at the output node.for attaining low noise figure or good amplifier the performance of LNA[54] depends strongly on input impedance and the choice of impedance matching topologies.this paper is implemented using pie matching technique. The different types of matching techniques are L,T and pie matching.in L matching the designing parameters depends on R_L and R_s therefore it provides only one degree of freedom whereas in pie matching[55] we get step up and down forth so tuning of the component is possible.pie matching provides two degree of freedom and enhances the gain with the small effect on the linearity.

$$R_{in} = \frac{1}{w_0^2 c_g^2 R_{\ddot{F}}}$$

The below circuit is implemented using a pie matching at resonance the input impedance purely becomes resitive 50Ω.the C_{gd} provides input matching and controlling mechanism for stability and linearity.however due to miller effects net compensation of gain is obtained so for isolating input and output cascoded combination with M_1 in common source and M_2 in common drain combination is obtained for improving gain. Gain boosting technique is implemented using M_2 and M_3 which amplifies the gain by enhancing transconductance of the amplifier. [55]The parallel combination of inductor L_2 and C_6 capacitor forms a load.M_4 is acting as an auxillary transistor used in commom gate mode for improving linearity in the circuits.the feed forward cancellation method is used for reducing noise figure by cancelling the effects of g_m' and g_m'' without effecting the g_m is used for obtaining linearity in the circuit.



I.

Fig. 3.6 Diagram of proposed LNA

$$I_D = g_m Vgs + g_m^1 Vg_s^2 + g_m^{11} V_{g_s} 3 \qquad \text{Eq 3.2.2}$$

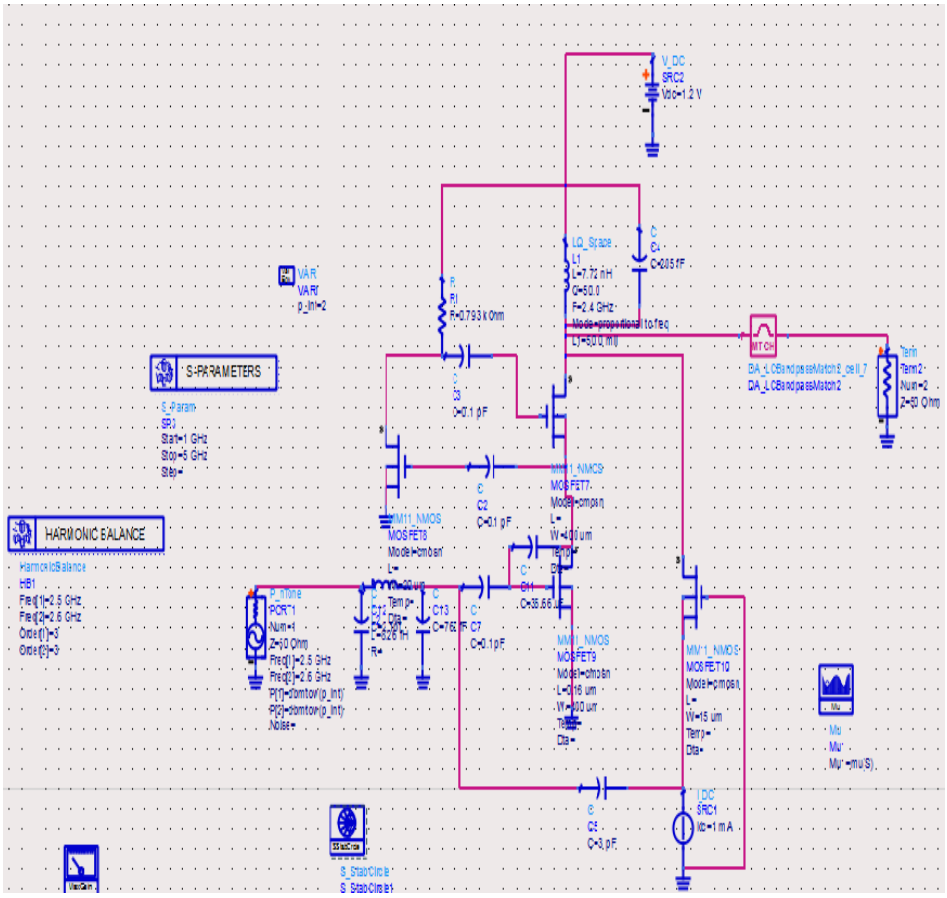


Fig. 3.7 Schematic Diagram

3.4 SIMULATION RESULTS AND COMPARISON

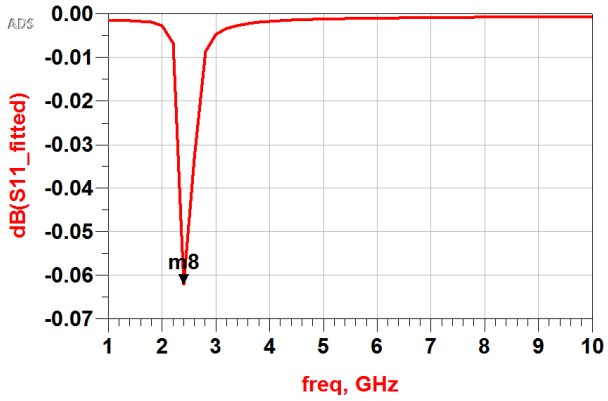


Fig. 3.8 Input return loss

The S_{11} is referred as input port voltage reflection Coefficient,it determines the input signal reflected back.the S_{11} parameter at 2.4 GHz is found to be -0.062dB.

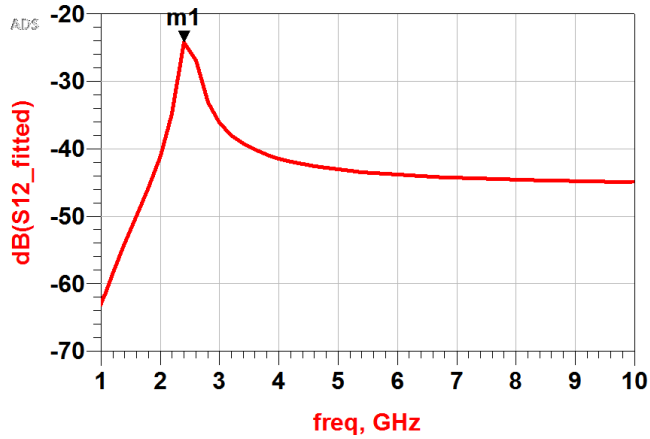


Fig. 3.9 Reverse transmission coefficient

The S_{12} is also called as reverse transmission coefficient or reverse voltage gain it measures the isolation of the input from the output .the S_{12} parakmeter at 2.4 GHz is found to be -24.239dB.

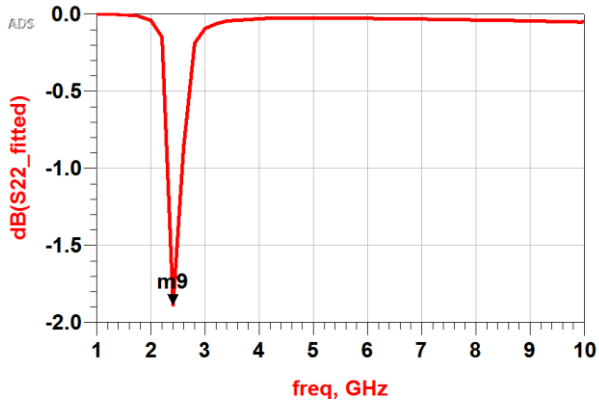


Fig. 3.10 Output reflection coefficient

The S_{22} is the output port voltage reflection coefficient it measures the output signal reflected back.the S_{22} parameter at 2.4GHz is found to be -1.884dB.

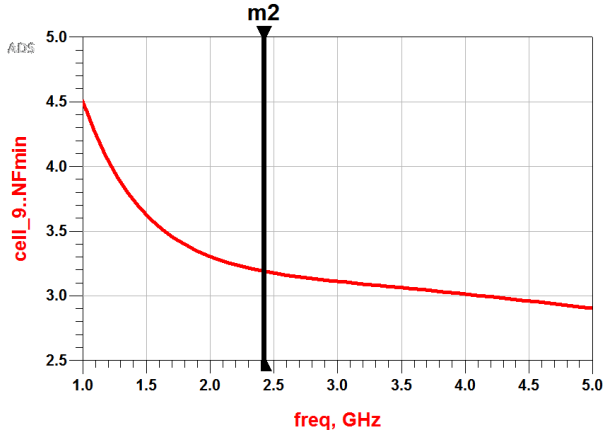


Fig. 3.11 Noise figure

The noise figure is a measure of (SNR)signal to the noise ratio caused by the component present in a circuit or signal chain.The noise figure is expressed in dB.the noise figure at 2.4 GHz for this circuit is 3.190dB.

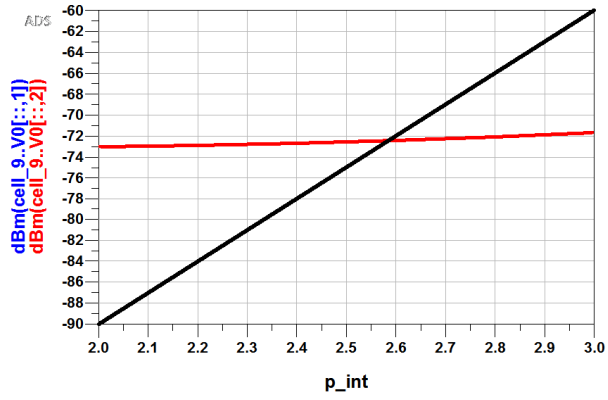


Fig. 3.12 Third order intercept point

LNA characterstics along with having high amplification and noise figure should also have high linearity.the third order intercept point is a measure of linearity of the circuit for this circuit it is found to be 2.6dBm which shows that the circuit is having good gain and good linearity withour effecting the noise performance infact good linearity of the circuit also causes the system to become more stable. Thus,it implies that the circuit can have either high gain,noise figure with poor linearity or low gain low noise figure or high linearity.

$$IIP_3 = 10\log\left(\frac{4}{3}\left|\frac{g_m}{g_m^{11}}\right|\right)$$

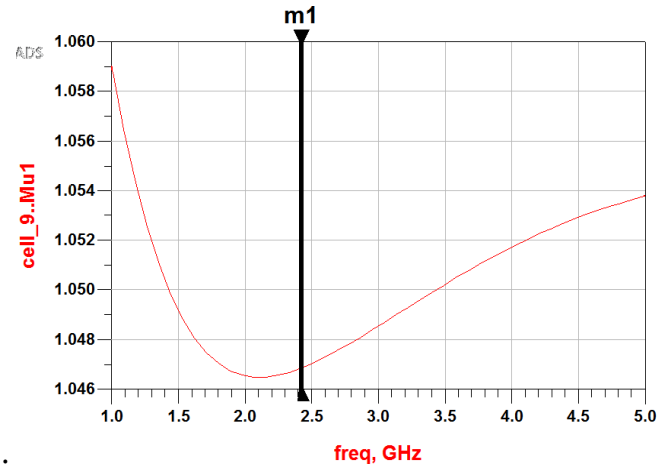


Fig. 3.14 Stability

Stability [56]of an LNA is its tendancy to oscillate and maximum available gain is the measure of figure of merit for the LNA. In stability prospective,an LNA can be either potentially unstable or unconditionally stable.Oscillation occour when there is a improper matching or due to improper load and source termination both at the input and output the three reasons for this scenario are excessive gain for out of band frequency,internal feedback,external feedback and the role of the reflection coefficient both at the load and source end in the stable region of the smith chart.

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

Where $\Delta_s = S_{11}S_{22} - S_{12}\,S_{21}$

Table 3.1 Comparison of Proposed LNA with other Published Works

Ref.No.	[52]	[53]	[54]	This work
Tech(µm)	0.18	0.18	0.18	0.18
NF(dB)	2.7	2	3.08	3.10
S_{11}(dB)	-4.3	-11.1	-36.3	-0.062
PDC(mW)	8.04	10.44	17.53	1.34
IIP_3(dBm)	-8.9	-4.3	-14	2.6
Supply	1	1.8	-	1
Freq(GHz)	2.4	5.15	5.7	2.4

The above CMOS LNA is implemented using cascoded topologyfor input and output isolation and gain boosting method is used for enhancing gain with feed forward cancellation method the circuit is found to be consuming 1.34 mW of power which is low so far and noise figure of 3.190 dB at 2.4 GHz ISM band. The circuit is found to be attaining IIP_3 of 2.6 dBm and stability factor of 1.04.

SECTION II

In second schematic High Linearity Highly Stable LNA for RF front End Application is presented Radio frequency refers to the electromagnetic signals used in wireless communication..this includes the waves ranging from few 3 KHz to 300 GHz Where frequency refers to the rate of oscillations (of the radio waves).the waves propagate at the speed of light in free space carrying voice,video and data at microwave frequency.[56] RF communication includes many industrial applications like mobile platform networking ,radar system,remote monitoring and many more.In , contrast RF modules,transceivers and SOCs often includes data link layer for supporting one or more communication protocols.one of the major wireless application Zigbee IEEE 802.15.4 [57] at 2.4 GHz

requires devices with low power consumption ,high data rate with simple networking protocols. With its application like WPANs(wireless personal area network) and internet of things are Implemented using mesh networking topologies in which the network setup consist of nodes capable of interacting with each other.

The major block of the RF front end receiver section includes low noise amplifier which increases the amplitude of the weak RF signal for its processing at the receiver end without adding noise or distortion to the signals.the transceiver architecture designed for wireless sensor network requires low power consumption and its configuration and designing is based on designers requirements.Its important [58] characterstics includes dynamic range,selectivity ,sensitivity linearity,leakage effect and image band rejection ratio.however,the important characterstics of LNA are bandwidth of operation,stability,linearity supply voltage and chip area optimising and controlling these parameters requires adequate knowledge of active devices and components and there method of fabrication with fewer tradeoff. this paper is simulated at 2.45GHz ISM band which stands for industrial, scientific and medical band defined by ITU radio regulations which are internationally reserved for radio frequency applications.

Organisation of this paper is as follows section II gives the brief description of the topologies ,intermodulation technique and matching circuits.section III describes the circuit and simulation results and comparison of work is made.section IV conclusion is given.

In this paper the circuit is implemented using a cascoded topology[60] which consist of commom source stage of the I amplifier connected to the common gate stage of the second amplifier.This topology provides better stability,better gain input output isolation and high slew rate.However, it causes higher input impedance due to the miller effect causing reduction in the gain which can be optimized using gain boosting technique or adjusting the biasing currents.the source degenerate topology with inductive termination provides an efficient input matching network of 50 Ω input resistance without the resitive thermal noise.the source degenerate reactance causes the wideband CMOS LNA to attain minimum noise figure and for attaining minimum input power condition another inductor is placed at the gate of the mosfets so that the combined network including C_{ex} can resonate at the desired frequency of operation.however,the excessive source inductance can cause LNA to oscillate because of higher gain at high frequency.The input matching network allows the system to attain minimum S_{11} [52] without introducing additional

noise.main transistor section ensures that the system attains high linearity,high gain and minimum noise figure at the time of proper input and output matching network.the input and output impedance matching network ensures the maximum power transfer by minimizing the reflections which is attained when $Z_L=Zs^*$.intermodulation distortion technique is defined as a method of interaction of two or more signals in a nonlinear ways.the intermodulation product generates signals due to the addition and differences of the original set of signals.this method improves the third order intercept point by using the passive components which forbids the use of auxillary amplifier for the suppression of the third order distortion components and therefore circuit do not incurs extra power consumptions.

The given circuit is implemented using a pie matching network through $C_{1,}L_1$ and C_2 having 2 degree of freedom.the M1 forms a source degenerate topology with inductor Ls to provide a 50Ω termination. Thus,improving the linearity and gain of the circuit.the external inductance Lg and Ls and capacitance Cex are found to be resonating at 2.45GHz frequency.the M2 forms the cascoded structure. Which provides the input and output isolation.the increase in the input resistance of the circuit causes the gain of the circuit to reduce which is optimized by adjusting the biasing currents.the resistance at the input of the M2 causes the reduction in the noise figure of the circuits .the linearity or IIP3 is improved by IMD technique implemented using M3 PMOS folded transistor by cancelling the first and third g_{m1} and g_{m3} with those of M1.

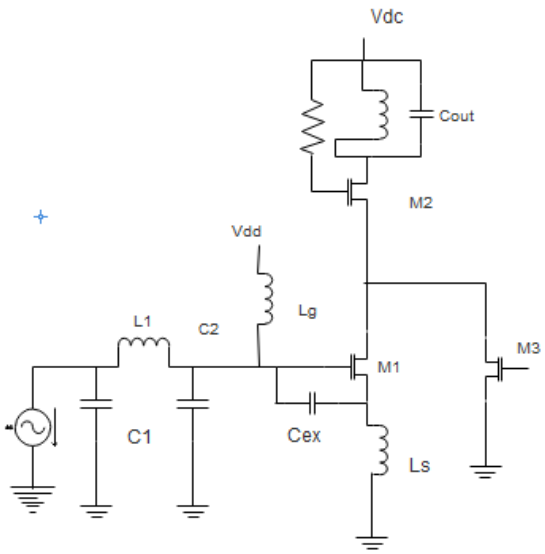


Fig.3.15

$$z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega Cgs} + \frac{gmL_s}{Cgs}$$

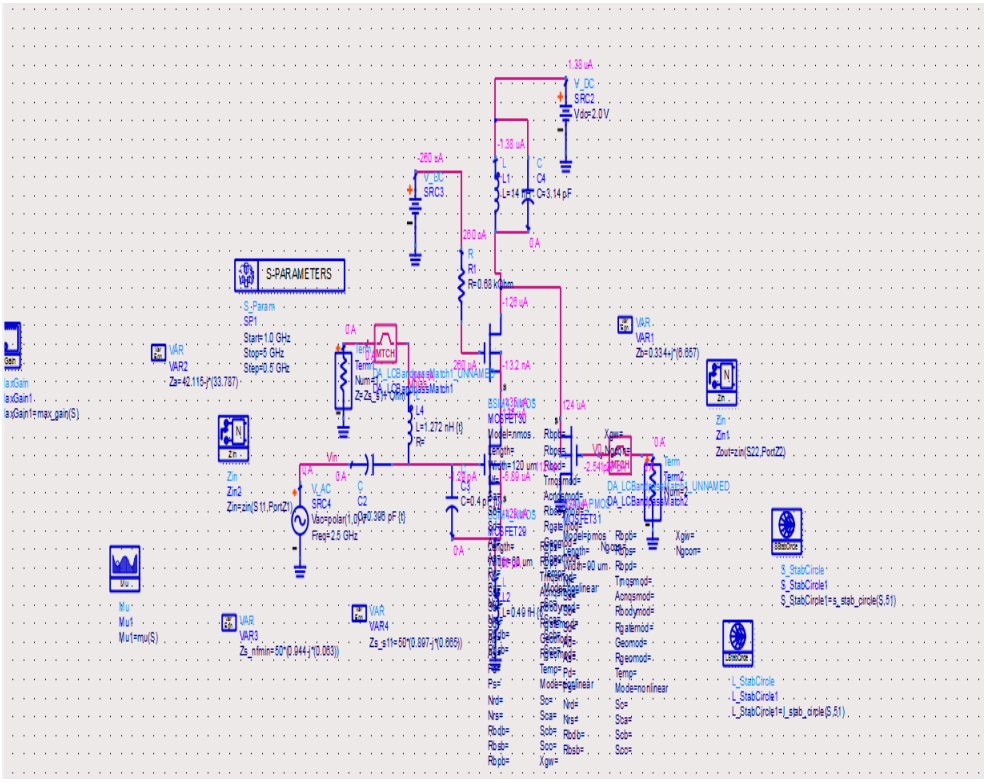


Fig.3.16 Schematic for Proposed LNA

3.5 **SIMULATED RESULTS AND COMPARISON**

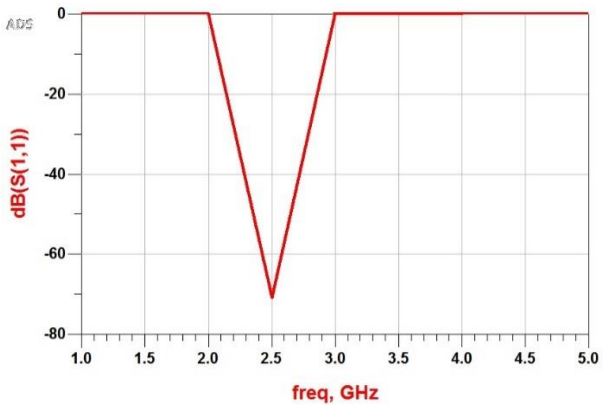


Fig. 3.17 Input Return Loss

The S_{11} parameter is called input voltage reflection coefficient it gives the estimate of the input RF signal bounced of the LNA at 2.45 GHz S_{11} is -70.841dB.

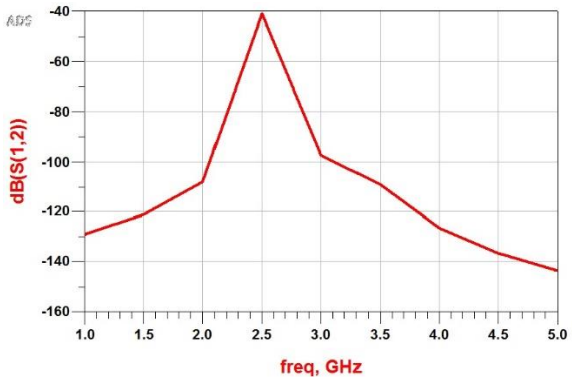


Fig. 3.18 Reverse Transmission Coefficient

S_{12} is also called as reverse transmission coefficient.it determines the amount of input signal reflected back or the amount of isolation between the input and the output ends.The S_{12} parameter at 2.45GHz is found to be -41.067dB.

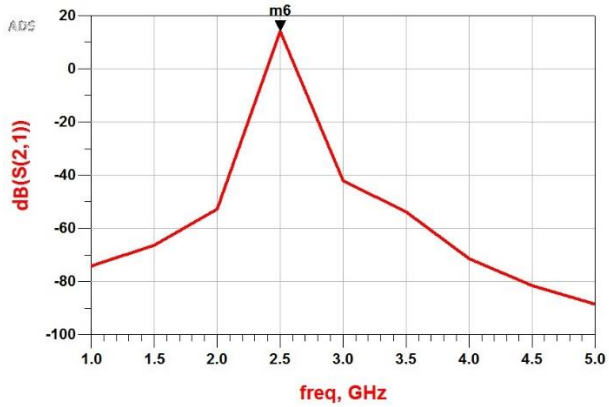


Fig. 3.19 Forward Transmission Coefficient

S_{21} is also called as forward voltage gain or forward transmission coefficient it measures the power gain of the LNA.the S_{21} parameter at 2.45 GHz is found to be 14.073dB.

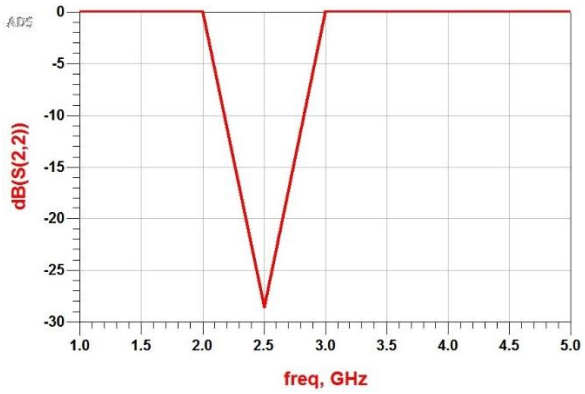


Fig. 3.20 Output Reflection Coefficient

The S_{22} is also called as output voltage reflection coefficient it determines the matching between the load impedance and output impedance. for this circuit the S_{22} parameter is found to be -28.018dB at 2.45 GHz frequency

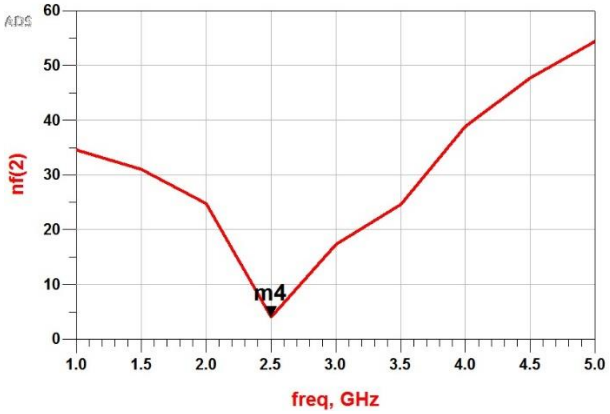


Fig. 3.21 Noise Figure

The noise figure is a measure of degradation in the signal to the noise ratio.the lower the value of a noise figure the better is the performance of the receiver.at 2.45GHz the noise figure for the circuit is found to be 4.060dB.

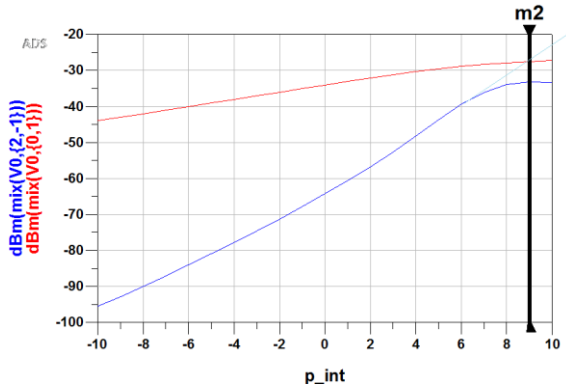


Fig. 3.22 IIP3 (Linearity)

LNA characterstics along with having high amplification and noise figure should also have high linearity.the third order intercept point is a measure of linearity of the circuit for this circuit it is found to be 9.0 dBm which shows that the circuit is having good gain and good linearity without effecting the noise performance infact good linearity of the circuit also causes the system to become more stable. Thus,it [6]implies that the circuit can have either high gain,noise figure with poor linearity or low gain low noise figure or high linearity.

$$IIP_3 = 10\log\left(\frac{4}{3}\left|\frac{g_m}{g_m^{11}}\right|\right)$$

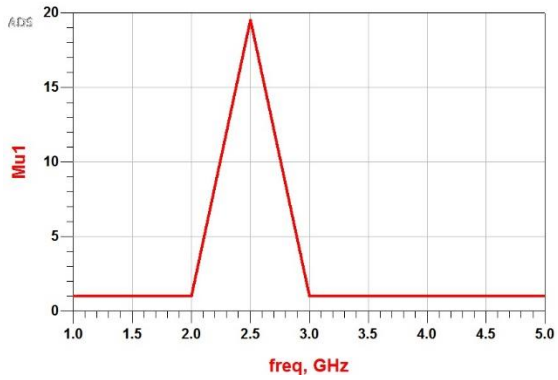


Fig. 3.23 Stability

Stability of an LNA[60] measures the tendency of an amplifier to oscillate.from LNA prospective it can be either unconditionally stable or potentially unstable.oscillation occour when there is an improper matching between the output impedance and load impedance or at the source end the stability factor of an LNA is determined by two factors Rollett stability factor or Mu.(Mu>1)is the sufficient and necessary condition for an unconditional stability for a two port network.

Rollett stability factor or K>1 for unconditionally stability.

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

Where

$\Delta_s = S_{11}S_{22} - S_{12}\,S_{21}$ Cont (1.5.29)

Table 3.2 Comparison of Proposed LNA with other Published Works

Ref.No.	[57]	[58]	[59]	This work
Tech(µm)	0.13	90nm	45nm	45nm
NF(dB)	3.34	4.34	1.42	4.060
S_{11}(dB)	-16.5	-11.32	-18.43	-41.067
Pdc(mW)	3.9	17.4	1.98	3.54
IIP_3(dBm)	-10	8.7	-9.87	9.0
Supply(V)	0.9	1	1	1
Freq(GHz)	2.44	2.44	2.45	2.45

The above circuit is implemented using a source degenerate topology providing an efficient input matching of 50Ω and noise figure of 4.060dB.it is followed by cascoded topology which provides input and output isolation with better stability. The circuit is found to be consuming 3.54mW of power for RF front end applications and attain a S_{11}=-41.067dB and IIP3 of 9.0dBm with a stability factor of 18 which is best so far.

In the third schematic LNA for wireless application is presented using cascode topology of common source and common gate with capacitive feedback topology .

SECTION III

Wireless communication is the process of transmitting information over a distance without cables, wires and other electrical network. In RF domain the wireless communication occours through electromagnetic spectrum ranging from 30 Hz to 300 GHz. In modern era the wireless communication involving RF front end circuits are designed for applications like IOTs (internet of things), LTE and 5G connectivity [61]]. Modern and future mobile devices need to support increasing number of frequency band and wireless standards and the applications like Bluetooth, Wi-Fi(802.11/a/b/g/n) standards ranging in 2.4 and 5 GHz band and mobile television. It should also support 4G LTE networking [62] consisting of 40 frequency band globally ranging from 700 MHz to 6 GHz. Other wireless application lies in UWB which is defined as data transmission in the form of radio energy spreaded over the entire bandwidth with a low power spectral density. The frequency range of UWB ranges from 3.1- 10.2 GHz. In [63] a wideband amplifier with a resitive feedback topology is implemented for UWB applications the LNA consist of input-matching network and single to differential amplifier acting as a voltage buffer for improving power gain. However, it faces challenges like pulse shape distortion (low powered signal distorted by transmission link), channel estimation, high frequency synchronization and low transmission power. As compared to 4G network 5G network requires to be versatile, scalable and energy smart for the hyper connected IOE world. In [64] By using advanced modulation methods massive MIMO and beam forcing techniques 5G connectivity are expected to achieve data rate of (10 Gbps) with universal coverage having high efficiency and spatial diversity.[65] 5G spectrum has three key frequency for widespread coverage capable of supporting all users and cases. Three frequency ranges are sub-1GHz, 1-6 GHz and above 6 GHz. 6 GHz radio (LANs) are less prone to interfere with the spectrum for

fixed microwave, satellite digital radio , telecom backhauls. Therefore, 6 GHz draft plan is under study with a goal of ensuring its use in wideband channel applications. The LNA designed for such wireless applications are required to have matching network for selecting specific range of frequencies, good linearity flat gain with low noise figure. The designing of LNA should be such that it consumes less power and occupies less chip area.

Organisation of this paper is as follows section II gives the brief description of the topologies, shunt capacitive feedback topology and matching circuits. section III describes the circuit and simulation results and comparison of work is made.Section IV conclusion is given.

LNA implementation involves three basic topology common source , common gate and cascode topology . the choice of the CS or CG is determined by the robustness of the I/P and O/P matching network or low noise figure in the circuitry. CS stage provides low noise figure as compared to CG stage. In the present circuit common source stage is cascoded with the common gate stage which provides better I/P and O/P matching, isolation, better stability and low noise figure. [66] The capacitance feedback topology provides additional optimization of NF. However, this topology provides high linearity, gain and low noise figure. The present circuit is implemented with pie matching network providing two degrees of freedom in the form of quality factor of the circuit. For attaining the ideal resistance of 50 Ω. common source with inductor degenerate is implemented.

In the given circuit C1, C2 and inductor L2 forms a pie matching network. The shunt capacitance C3 along with source degenerate inductor L3 attains I/P impedances of 50Ω. The mosfet M1 with common source and M2 with common gate topology forms a cascoded stage providing isolation between input and output and circuit attains high linearity and low noise figure. The feedback capacitor C3 is in shunt configuration. Thus, the circuit attains negative feedback causing the system to become unconditionally stable which improves the gain lower noise figure and causes the circuit to attain high linearity. The DC blocking is obtained through capacitor C4. the inductor L3 and resistance R2 in series acts as a loading element of the cascode stage and for further increasing the gain and bandwidth the second stage of source follower M3 is used.

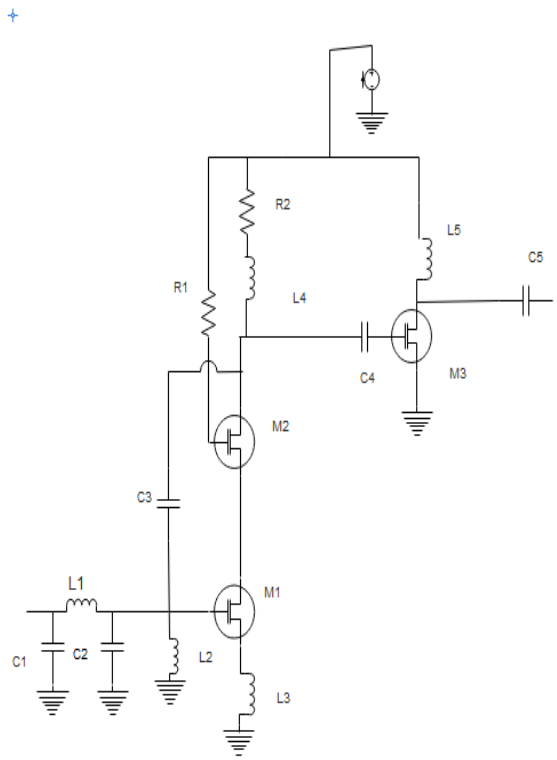


Fig. 3.24 Circuit Diagram for Proposed LNA

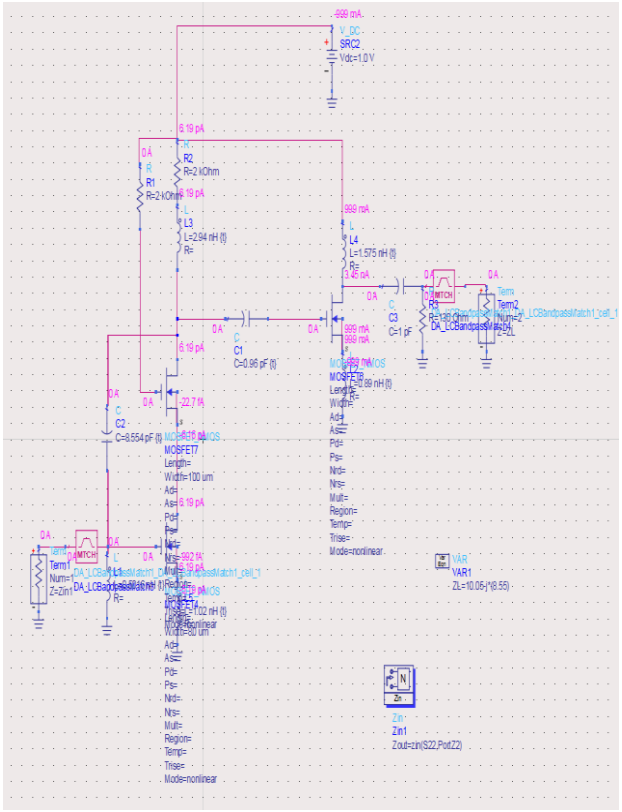


Fig. 3.25 Schematic for Proposed LNA

3.10 SIMULATED RESULTS AND COMPARISON

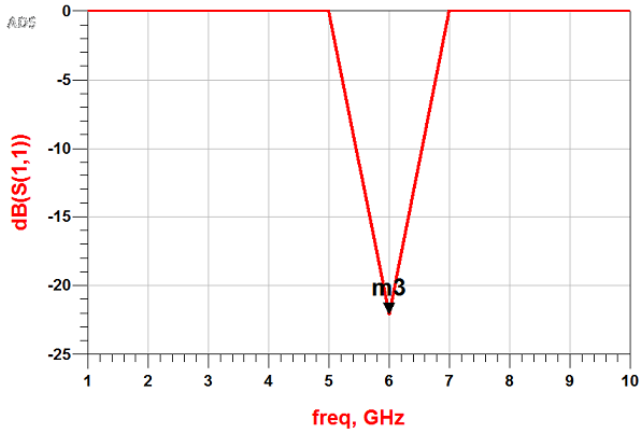


Fig.3.26 Input Return Loss

The parameter S_{11} denotes the input return loss or reflection coefficient. For measuring S_{11}, a signal injected at input port and then the signal reflected back is measured. In this no signal is coupled to the output port. So it denotes the matching between the input and the reference impedances. For 6 GHz the S_{11} obtained is -22.096 dB as shown in fig (3)

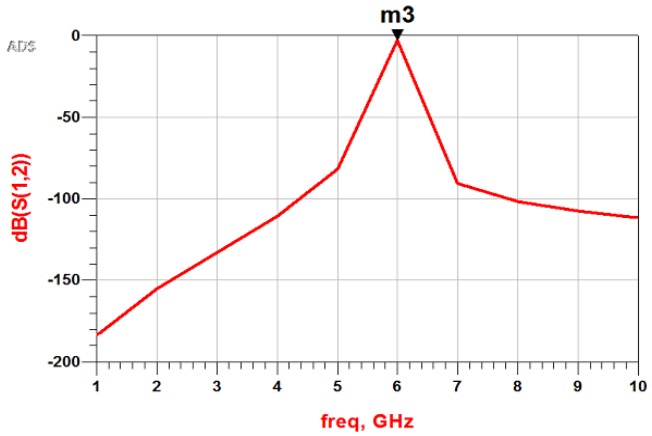


Fig. 3.27 Reverse Transmission Coefficient

S_{12} is also called as reverse transmission coefficient.it calculates the I/P signal reflected back or measures the isolation b/w the I/P and O/P port. The S_{12} parameters for this circuit is -2.755 dB.

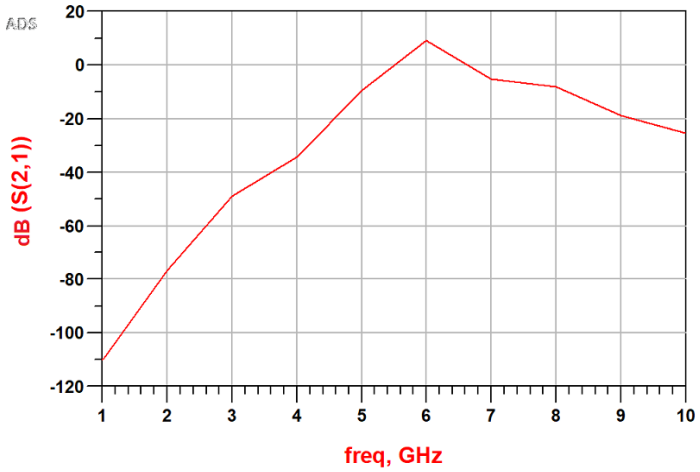


Fig. 3.28 Forward Transmission Coefficient

S_{21} is also called as forward voltage gain or forward transmission coefficient it measures the signal transmitted from the I/P to the O/P or the intensity of the signal reaching the O/P for this circuit the S_{21} obtained is equal to 9.4 dB.

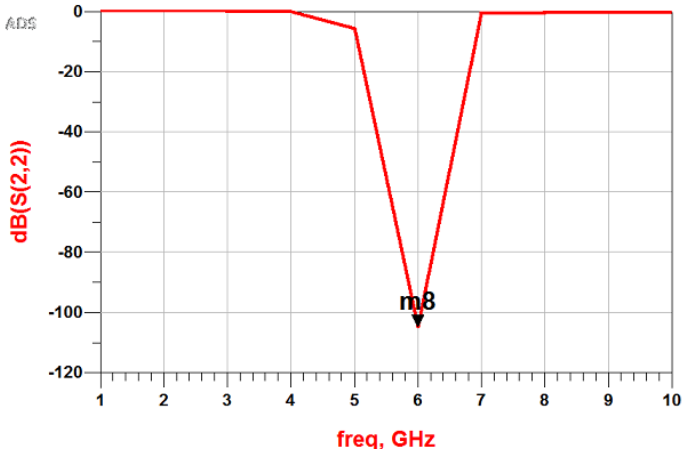


Fig. 3.29 Output Reflection Coefficient

The S_{22} is also called as output voltage reflection coefficient or output return loss. For measuring S_{22} a signal is injected at the O/P port and the reflected signal is measured. In this no coupling of a signal to the input port takes place. So it denotes the matching between the output and the reference impedances. For 6 GHz the S_{22} obtained is equal to -104.855 dB.

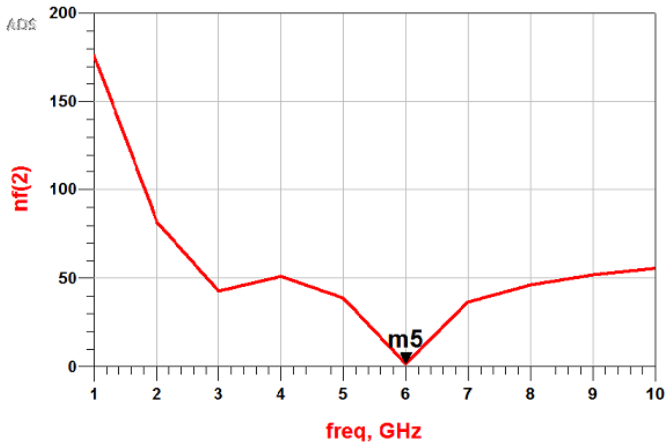


Fig. 3.30 Noise Figure

The parameter NF (noise Figure) is a measure of SNR. It calculates the degradation in the signal to noise ratio. The lower value of the NF denotes the better performance of the circuit. For this NF=1.235 dB as shown in the fig (6).

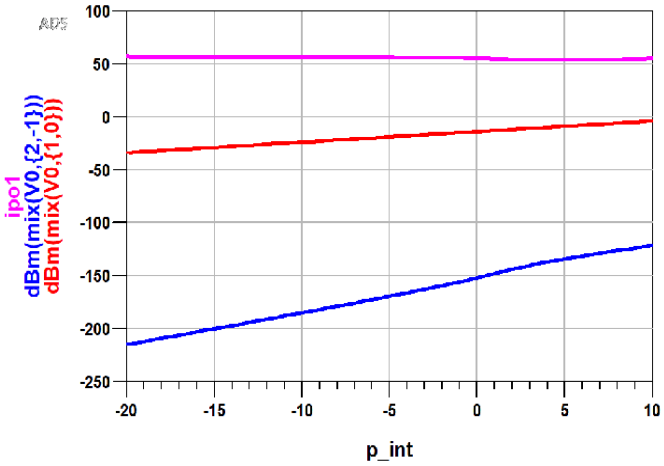


Fig. 3.31 Third Order Intercept Point

The characteristics of LNA are determined by high amplification factor and low noise figure along with it circuit should have high linearity. The third order intercept point (IIP_3) is a measure of linearity of the circuit. In this circuit the IIP_3 is found to be 56.895 dBm which denotes the circuit with low noise figure attains high linearity causing system to become relatively more stable.Thus , it implies that[67] from the fact that circuit can either have moderate gain , low noise figure or high linearity or moderate gain with high noise figure and low linearity.

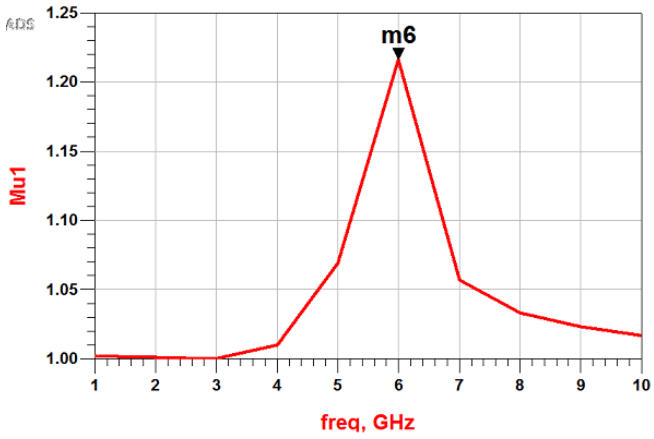


Fig. 3.32 Stability

Stability of an LNA [67] measures the tendency of an amplifier to oscillate. it is defined as immunity against spurious oscillations. The circuit becomes unstable for specific combination of source and load impedances. An LNA designed oscillate at extreme of voltage variation for low or high frequency. Therefore, the stability of an amplifier is given by two factors K and Δ where K denotes rollet's stability factor or stern stability factor. The stability factor of this circuit is 1.216.

Rollett stability factor or K>1 for unconditionally stability.

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

Where $\Delta_s = S_{11}S_{22} - S_{12}\,S_{21}$ Cont (1.5.29)

The proposed CMOS LNA is implemented using cascode topology for input and output isolation and shunt capacitive feedback topology providing high linearity to the circuit it is implemented with source degenerate inductor topology to achieve matching circuit of 50Ω. The circuit is found to consuming 0.035 mW of power and noise figure of 1.235 dB at 6 GHz band for wireless application . The circuit is found to attain IIP3 of 56.825 dBm and stability factor of 1.216 with output return loss or S_{22}= -104.855 dB which is best so far.

Table 3.3 Comparison of Proposed LNA with other Published Works

Ref.No.	[64]	[65]	[66]	This Work
Tech(μm)	0.18	0.18	0.13	0.18
NF(dB)	2.5-3.5	2.7-3.38	1.8	1.235
S_{11}(dB)	-12.6	-10.61	-1.3	-22.062
Pdc(mW)	8.14	8.65	-	0.035
IIP_3(dBm)	-	-	3	56.895
Supply(V)	1	1.2	1.2	1
Freq(GHz)	2-6	3-11	3.1-10.6	6

Table 3.4 Comparison of Work

Topology	Cascode Topology with Gain Boosting Technique	CS inductor degenerate Cascode Topology	Shunt Capacitive Feedback with CS inductive degenerate Topology
Tech(µm)	0.18	45	0.18
S_{11}(dB)	-0.062	-47.536	-22.062
S_{12}(dB)	-24.239	-41.536	-22.062
S_{21}(dB)	-	14.074dBm	9.4
S_{22}(dB)	-1.884	-28.018	-104.85
N.F.(dB)	3.190	4.060	1.23
Pdc(mW)	1.34	3.54	0.035
IIP_3(dBm)	2.6	9.0	56.86
Frequency(GHz)	2.4	2.4	6

In this thesis LNA implementation with different topologies like common source, common gate and cascode topology is discussed. In this simulation part LNA implemented with shunt capacitive feedback attains NF=1.235 dB and IIP_3= 56.825 dBm with a power consumption of 0.035 mW which is best so far. The circuit attains optimised gain of 9.4dB which can be improved further. Additionally, the implementation of LNA on 45nm TSMC technology file is obtained saving lots of space on integrated circuits.

LNA is a crucial element for the RF Front end designing. For effective designing of the RF Front end receiver the future course of work should focus on designing of balun and Mixers. LNA and Mixers form a common circuitry for obtaining high bandwidth and good intermodulation distortion (IMD). The entire circuitry should be monothically integrated on a single chip. So that the system becomes less sensitive to load matching. Balun, on the other hand is implemented using differential amplifier with improved designing of these two specific components. The entire system can attain high gain and linearity.

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Appendix I

List of Published Papers

1. **Malti Bansal, Gaurav Srivastava, "LNA for Biomedical Applications," International Journal of Engineering Technology Science & Research (IJESTR) ISSN 2394-3386,Volume 4 pp- 295-300,Issue 11, November 2017.**
2. **Malti Bansal, Gaurav Srivastava, " High Linearity and Low Power Cascode CMOS LNA for RF Front-End Applications," in proceedings of Third International conference on Intelligent Computing and Control Systems(ICICCS-2019),pp-1-4.**
3. **Malti Bansal, Gaurav Srivastava, " Design and Implementation of LNA for Biomedical Applications", in proceedings of International Conference on Intelligent Computing ,Information and Control Systems(ICICCS-2019),pp-151-160.**

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LNA for Biomedical Applications

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Abstract: *LNA, which stands for low noise amplifier, as the name suggests, is used for amplifying weak and very low power signals. LNA is an important part of transceiver system. It is the fundamental building block of communication systems. LNA is used in industrial, scientific and medical bands (ISM). Radios, cellular telephones, GPS receiver, and satellite communication, etc. employ LNA. In this paper, we have discussed about various topologies of LNA and their mode of implementation in biomedical applications. Biomedical applications involve the use of LNA in neural applications, biosensors, ECG applications, etc. Comparison of the different topologies in terms of power consumption, chip area and mode of implementation has been done.*

Keywords- LNA, Biomedical applications, Neural applications, ECG, Biosensors, etc.

I. Introduction

LNA is an amplifier that amplifies a very low power signal without degrading its signal to noise ratio (SNR). An amplifier amplifies both the signal and the noise, which is present at its input but the low noise amplifier, amplifies the signal present at its input but adds very little noise to the signal. The purpose of LNA is to get larger gain with very low noise figure. Also, we desire low power consumption, small chip area, low cost and good input and output matching for the LNA used in RF communication. For example, an outdoor antenna is connected to the receiver end with the help of transmission line called as feed line. During the transmission, it causes a loss of around 3dB which can be compensated by placing LNA close to the receiver end, which provides sufficient gain to reduce the losses.

II. LNA for Biomedical Applications

In biomedical applications, we encounter very weak signals. For the amplification of very weak signals, especially in biomedical applications, LNA is used. In [1], LNA with cascade inductor with degeneration topology has been used, which provides higher gain and low noise figure. LNA in biomedical applications requires extremely low power consumption as well as small size. LNAs designed using inductor loaded topology, are found to be less favourable for biomedical implants as they are bigger in size. Therefore in [2], LNA was designed using g_m boost technique having input impedance of 600Ω. And the current obtained was below 500µA for ultra–low power design. This was implemented on 130nm IBM technology and simulated. The LNA implemented using common gate (CG) topology attained less sensitivity and drastically reduced power consumption and resistance. The federal commission introduced medical radio communication for providing secure, un-scattered health monitoring in homes and hospitals. The operating range for this application is 401-406 MHz. This is done to provide continuous communication for both implantable and wearable medical devices. The RF front –end was designed using balun LNA topology in UMC 0.18µm CMOS technology. This was configured by stacking power phase splitter on top of inductively degenerated common source topology. It attained a gain of 19dB and consumed 280µA current from 1V supply.

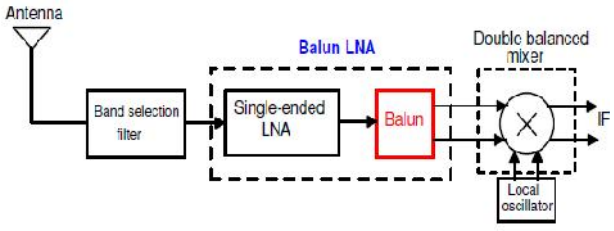

Fig.1: Receiver with balun LNA (reproduced from [2])

In [3], a wireless transceiver system was implemented using LNA for developing of network

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system which functions as a link budget for low power design. The low power system designed so will reduce a lot of power consumption but occupies larger area and results in installation problem, therefore transceiver system so designed was installed at 60GHz frequency. WSN is configured in indoor environment separated by a 10m distance. Signal bandwidth so obtained depends upon sample rate and resolution. WSN operates by sending biomedical signal from sensor node; and the signal are merged by MCU and are further converted by ADC and transmitted through 2.4 GHz band to the collecting point tuned at 60GHz.

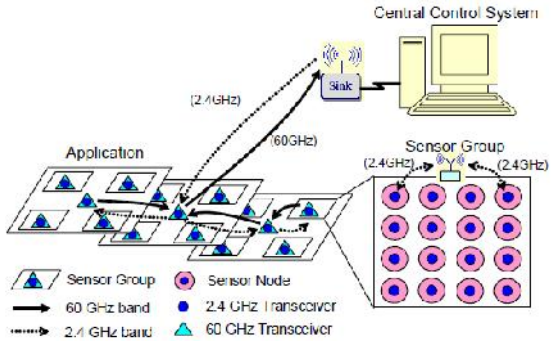

Fig.2: Hierarchical architecture of WSN system (reproduced from [3])

Use of LNA in Neural Applications

Neural signals in biomedical applications deal with the study of and understanding of brain function and its therapeutic and prosthetic applications. Neural interfacing consists of large number of channels for the study of neurons for specific brain microcircuits. It entirely deals with important parameters like power consumption, noise performance and CMRR. The Na^+/K^+ are powered by the ATP molecules which are the main energy molecules in animal cells. Whenever ionic channel becomes activated electrically, biochemically or through other mechanism, depolarization caused is generally the result of voltage sensitivity, causing the channel containing Na^+ to open first which causes the influx of positive charges across the cell, causing the potential to increase rapidly. However, balance is obtained when after a while K^+ channel is opened, which causes the influx of ions across the cell membrane.

In [4], the most common topology used for implementing low-noise amplifier are OTAs which are implemented using two stage op-amp and current mirror OTA. The folded cascade combination when compared to differential mode has larger swing margin and phase margin. Chae.M.et.al [7] implemented a self biased OTA which attained a gain of 40.5dB, NEF of 4.5 and a power consumption of 12.5µw. In [5], for low power application in biomedical domain, the wireless medical telemetry requires a portable device which can operate at a low supply voltage using a battery or with the help of energy source. Super –regenerative RF receiver is designed keeping this configuration in mind. In a non-coherent front end RF receiver, the LNA and energy detector are crucial designing elements of the module. For ON-OFF keying, RF envelope detector requires a high precise local oscillator for which receiver is required to have phase locked loop but this configuration increases power consumption. However, for demodulating at the receiver, RF input signal is sent to mixer which converts it to a baseband signal. A Gilbert Cell has been used in this work; such circuit offers high conversion gain and port to port isolation; therefore it is implemented using bipolar or CMOS simulation process.

LNA designed using current-reuse technique consumes more power so cascode topology is used but since it is inefficient at low supply voltage, so folded topology is used. For low supply voltage and low power consumption, a current reused two stage common source topology is proposed for RF front end amplifiers.

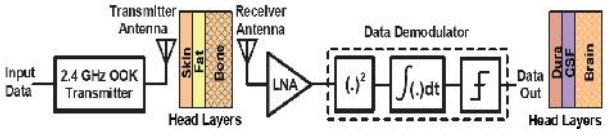

Fig. 3:: Conceptual block diagram of wireless link including transmitter, LNA , head tissue layer ,OOK data detector (reproduced from [5])

The above is a low voltage, low power 2.4 GHz CMOS OOK receiver; that includes modified current reuse two common source LNA topology to provide enhanced gain and noise figure. After simulation, the digits ‘0’ and ‘1’ are obtained at a time instant of 10ns. This means receiver successfully recovers OOK data at 100Mbps.

The two noises which dominates at lower frequency are thermal and flicker noise; therefore in [6] EKV model is used for biasing current and for reducing flicker noise. PMOS input transistors are used with

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large gate area and they are operated in weak inversion mode. Using such technique, the power consumed by the circuit is found to be 15.17µW. Measurement of very weak neural signal ranging between 0.5-5mV and frequency from 100Hz to 7 KHz is necessary for clinical and neuro-prosthetic applications; and also for neuroscience research. PMOS acts here as input for minimizing flicker noise.

The Input noise power density is given by

$$E_n^2 = \frac{8kT\gamma}{g_{m1}} + 8kT\gamma\left(\frac{g_{m5}}{g_{m1}}\right)^2 + \frac{2K_p^{1/f}}{C_{ox}W_1L_1f} + \frac{2K_n^{1/f}}{C_{ox}W_5L_5f}\left(\frac{g_{m5}}{g_{m1}}\right)^2$$

We can approximate:

$$g_{m1} \gg g_{m5},$$

And thus,

$$\left(\frac{W}{L}\right)_1 \gg \left(\frac{W}{L}\right)_5$$

which gives noise power density as:

$$E_n^2 = \frac{8kT\gamma}{g_{m1}} + \frac{2K_p^{1/f}}{C_{ox}W_1L_1f}$$

The noise efficiency factor is obtained by:

$$NEF = Vrms\sqrt{\frac{2I_{tot}}{\pi U_T 4kT.\,BW}}$$

where Vrms is the input noise voltage and I_{tot} is the total current And BW is the amplifier bandwidth.

On comparison, we observe that the neural amplifier implemented using OOK modulation scheme results in low power consumption of 7mW.

Use of LNA in Biosensors Applications

Biosensors are analytical devices that detect the analyte (chemical species) and combines a biological component with physicochemical detector. The sensitive biological elements consists of tissue, microorganism, cell receptors, etc). These are made to interact with analyte under study. The transducer or the detection elements consists of optical, piezoelectric and electrochemical sensors that transform the signals after interaction with analyte, to another form, which can be measured and analysed. The increasing demands for the biological information in medical diagnostics, healthcare, etc has resulted in tremendous interest in biological sensors.

In [13], m-health (mobile computing , medical sensors and communication technologies) is considered wherein an increasing number of biosensors are worn and implanted in an individual for monitoring and diagonisis of diseases. The interconnection of biosensors inside the single human body produces a system called as a body area sensor network (BASN). The BASN performs two functions: (i)The passive function of transmitting the data for processing; (ii)To avail data to the biosensors, which are present at the same node inside the human body and communicate through a secure channel. The BASN identifies the individual based on biometric or identifying individual on pyshcological and behavioural characterstics. In [18], several systems focus on providing physical aspect of a person at the expense of emotional aspects. However,the negative emotions can lead to social and mental health problem. To cope with the negative emotions, a system has been designed that focuses on emotional aspects. The system has been designed using an AR (augmented reality), using cognitive behavioral therapy, providing 3-D virtual world. The system can interact with the help of kinect which interacts freely with the virtual world. Sensors measure biological signals like EEG and ECG to detect and analyse the emotions of the user.

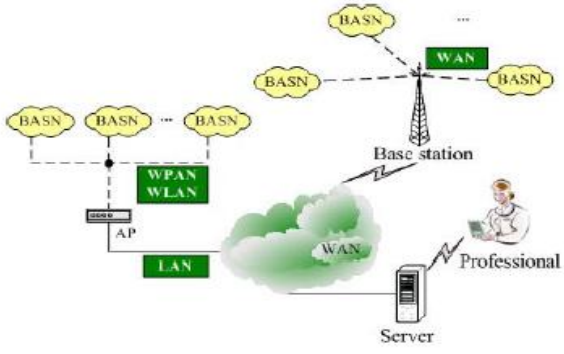

Fig.4: A BASN combined health model [reproduced from 16]

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In [14], the WBSN plays an important role in health care monitoring system. In this, each wireless sensor network receives the packets from the other sensor node and selects the adjacent sensor node for the trnasmitting of data, depending upon the header containing the address of the adjacent node. The WBSN is further seperated in communication and control path for biomedical applications. A communication cycle which is constructed also synchronises the whole WBSN system. The control system works by adding control signals which add the controllability and scheduling to the architecture.

Table 1:LNA in Biosensor Applications

S.No.	[14]	[15]	[16]
Implementation	TSMC 0.18 µm	0.5µm CMOS	0.7µm CMOS
Chip size	-	2.5mm^2	4.5mm^2
Power consumption	1440µW	-	-
Supply (V)	1.8	2.7-5.5	2.5-5.5
Current (µA)	800	130µA	75µA

Use of LNA in ECG Applications

Since we know that the biomedical signals are very weak signals, the measurement of ECG signals involves the accuracy and reproducibility. The ECG signals are generally recorded during ambulatory or strenous conditions. The resultant signals get affected by noise, for which signal processing is applied. The ECG signals are sometimes recorded for longer duration of time. For e.g. in case of cardiac problems like irregular heart rhytm, data recording is huge and requires extra space, therefore extra space is required. Therefore, it needs to be compressed both at the receiver and transmitter end, for transmission through public telephonic network. Another example is contraction of muscles that results in overlaping of ECG and muscle noise, therefore filtering becomes difficult.

After receving of ECG signals, signal processing is done for quantifying heart rhytm and heartbeat morphological properties. In [8], the authors report the use of sensor systems combined with wireless protocol for data communication with capacitive ECG sensing and processing. The system uses a ANT protocol and a low data rate wireless module to reduce power consumption and chip area. The entire design is integrated in a cotton T-shirt, together having a signal processing and two layer standard printed circuit board design technology. The entire system is found to have small size and thus, occupies low area and has low power consumption. The ECG signal acquired is amplified, filtered , digitized and transmitted to the differential amplifier. The amplifier diffrentiates the signal and sends it to ADC block. Unwanted frequency is removed by low, high and notch filters used at 60GHz frequency and it improves the SNR. The processed signal is then digitised into small packets and wirelessly transmitted to the main module. In [9], bio signals are acquired using nyquist rate analog –to-digital conversion without exploiting the bio signals characterstics. A fully integrated low power CS compressed signal at analog front end acts as a ECG sensor). Key biosignals have a small bandwidth and dynamic range (40-70dB). The basic circuit consists of analog front end with signal conditioning and a Nyquist analog to digital converter. The encoder receives a conditioned biosignal from LNA and compression of N input samples results in M output samples which are digitised and transmitted. The ADC and RF are made to operate at nyquist rate and since a compression factor N/M is greater then 1, the signal is downconverted into the output y(t).

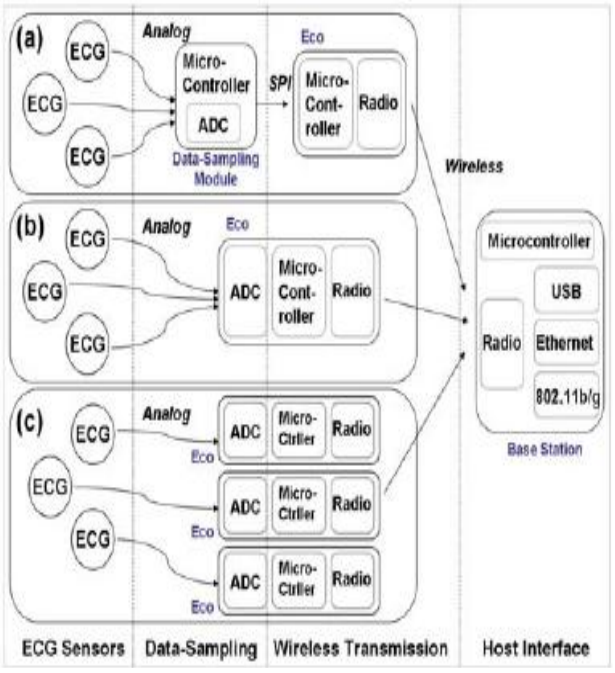

Fig.5: System architecture of ECG monitoring system [reproduced from 13]

Table 2: LNA in ECG Applications

S.No.	[11]	[12]	[13]	[9]
Technology	Using SAC and QRS detection	Capacitive sensing	Ultra low power	Nyquist rate
Implementation	On body	On cloth	Wire-less	0.13µm CMOS
Power Consumption	9.6µW	30µW	1mW	1.8µW
Area	5.74 mm^2	-	57 mm^2	6 mm^2

III. Conclusion and Future Scope

Biomedical engineering involves the knowledge of medicine and biology for health care applications. In this paper, use of LNA for biomedical applications like neural applications, biosensors and ECG is discussed. The other applications of biomedical engineering include EEG, EKG, PPG, echo normal(for chest pain), etc. which are yet to be discussed.

Acknowledgement

One of the authors (Gaurav Srivastava) acknowledges the fellowship support he is receiving from Delhi Technological University (DTU), for carrying out this work, as a part of his Master of Technology Thesis work in the domain of Microwave and Optical Communication. He also acknowledges the guidance support from his thesis mentor, Dr Malti Bansal, Assistant Professor, Department of Electronics and Communication Engineering, DTU, for carrying out this research work.

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HIGH LINEARITY AND LOW POWER CASCODE CMOS LNA FOR RF FRONT END APPLICATIONS

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Abstract— **In this paper, model of low power high linearity CMOS amplifier with low noise figure is presented. LNA is implemented in ADS using TSMC 0.18um technology based on cascode topology with gain boosting technique. In order to improve linearity, feed forward cancellation method is used. The LNA is found to have S_{11}=-0.062dB, S_{12}=-24.239dB, S_{22}=-1.884dB and noise figure of 3.190dB and IIP_3 of 2.6dBm. LNA is consuming 1.34mW of power from 1V power supply and is designed for 2.4GHz ISM band applications.**

Index terms- LNA, cascode topology, feed forward cancellation (FDC).

I. INTRODUCTION

In today's scenario, the need for wireless application devices has increased tremendously. One of the major wireless application is bluetooth which requires low energy devices. These devices are ecofriendly devices that are developed for facilitating "internet of things". These devices are found to be having less power consumption and energy. Bluetooth IEEE 802.15.4 [1] holds the capability of becoming the choice for setting the adhoc network in the future because of its key features of low power consumption and potential low cost. Bluetooth low energy devices are used in 2.4GHz (ISM) band or unlicensed band that are internationally reserved radio spectrum intended for scientific medical and industrial requirements.

LNA (low noise amplifier) plays a key role in radio receiver performances.The receiver performance is measured in terms of receivers' sensitivity, selectivity or proclivity to reception errors [2]. The RF front end performance is determined by the first active device in the block. here are 5 characterstics of LNA that are directly under the designer's control and directly affect receivers' sensitivity. These are linearity, bandwidth, noise figure , gain and dynamic range of operation. Controlling these parameters requires sufficient knowledge of active devices, impedance matching and method of assembling and fabrication of amplifiers and achieving optimal performance with fewer tradeoffs [3].

Organisation of this paper is as follows. Section II gives the brief description of the topology, feed forward cancellation method and matching circuits. Section III describes the circuit and simulation results and also presents comparison of reported work with other published works. Section IV presents conclusion.

II. CASCODE LNA TOPOLOGY

LNA cascode topology consists of two MOSFETs connected together; one with common source topology cascoded with the common gate topology of the other MOSFET following the same DC path. The cascode topology is preferred when the isolation between input and output is required which improves the stablity of the circuits. Cascode topology provides better stability, better noise figure, higher gain, better reverse isolation and independent input and output matching. Gain boosting technique is the method for increasing the gain of the amplifier by amplifying the transconductance and increasing the power gain of narrow band RF LNA by using the negative resistance obtained from the cascode combination. The noise factor [4] can be improved by increasing the transconductance, that leads to the method of reducing the input resistance and noise factor. The g_m boosting technique effectively limits the power, reduces noise and enhances the gain simultaneously.

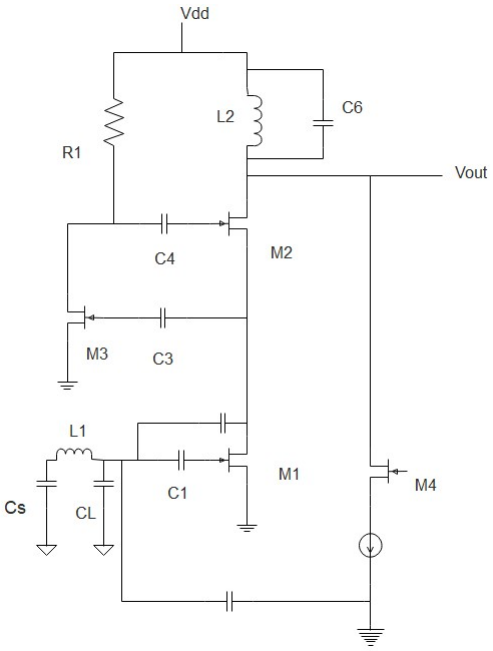
While designing LNA [5], one can achieve high gain, low noise with low linearity when operated at low desired signals or high linearity, low gain and large noise figure with large signal interferences. Therefore, feed forward cancellation method is adopted which involves the method of adding an auxillary amplifier and its effect on the signal and noise voltage is obtained at the output node. For attaining low noise figure or good amplifier, the performance of LNA [6] depends strongly on input impedance and the choice of impedance matching topologies. This paper is implemented using pie matching technique. The different types of matching techniques are L,T and pie matching. In L matching, the design parameters depend on R_L and R_s , therefore it provides only one degree of freedom whereas in pie matching [7], we get step up and down forth, so tuning of the components is possible. Pie matching provides two degrees of freedom and enhances the gain with small effect on the linearity.

$$R_{in} = \frac{1}{w_0^2 c_g^2 R_F} \qquad \text{.....(1)}$$

III. CIRCUIT DESIGN

The proposed circuit is implemented using pie matching. At resonance, the input impedance purely becomes resitive (50Ω). The C_{gd} provides input matching and controlling mechanism for stability and linearity. However, due to miller effects, net compensation of gain is obtained. So, for isolating input and output, cascode combination with M_1 in common source and M_2 in common drain mode is used, for improving gain. Gain boosting technique is implemented using M_2 and M_3

which amplifies the gain by enhancing transconductance of the amplifier [8]. The parallel combination of inductor L_2 and capacitor C_6 forms a load. M_4 is acting as an auxillary transistor used in commom gate mode for improving linearity in the circuit. The feed forward cancellation method is used for reducing noise figure by cancelling the effects of g_m' and g_m''. The g_m is used for obtaining linearity in the circuit.



I.

Fig. 1: Circuit Diagram for Proposed LNA

$$I_D = g_m Vgs + g_m^1 Vg_s^2 + g_m^{11} V_{g_s} 3 \quad \ldots\ldots (2)$$

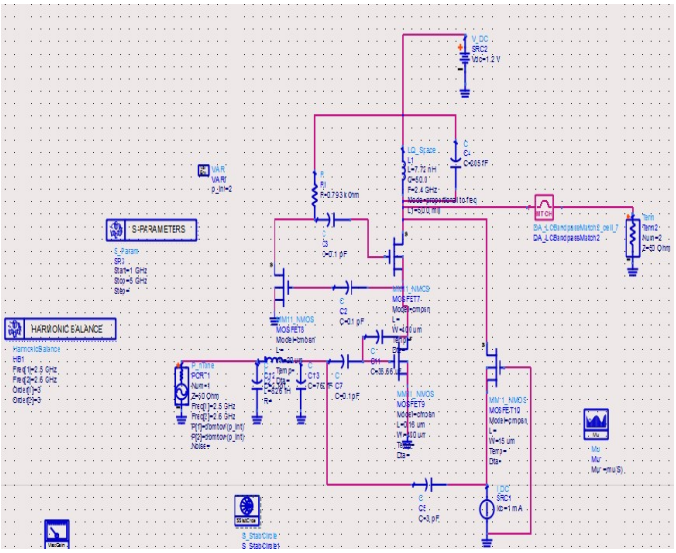


Fig. 2: Schematic for Proposed LNA

IV. SIMULATION RESULTS AND COMPARISON

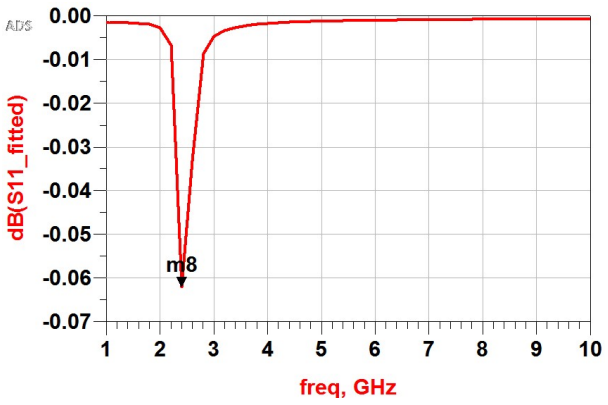


Fig. 3: Input Return Loss

The S_{11} is referred to as input port voltage reflection coefficient. It determines the input signal reflected back. The S_{11} parameter at 2.4 GHz is found to be -0.062dB.

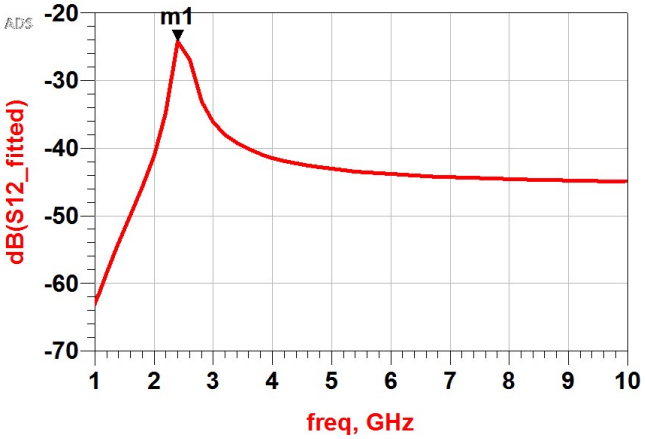


Fig. 4: Reverse Transmission Coefficient

The S_{12} is also called as reverse transmission coefficient or reverse voltage gain. It measures the isolation of the input from the output. The S_{12} parameter at 2.4 GHz is found to be -24.239dB.

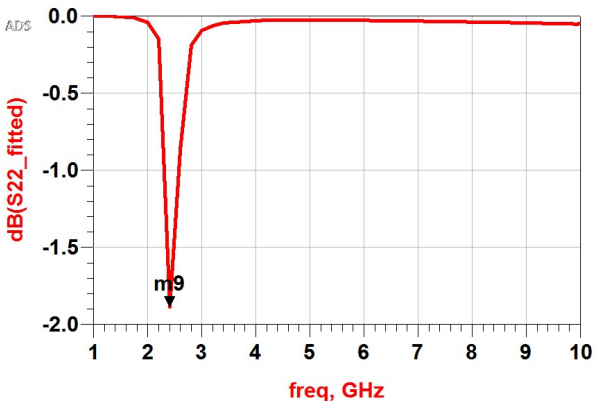


Fig. 5: Output Reflection Coefficient

The S_{22} is the output port voltage reflection coefficient. It measures the output signal reflected back. The S_{22} parameter at 2.4GHz is found to be -1.884dB.

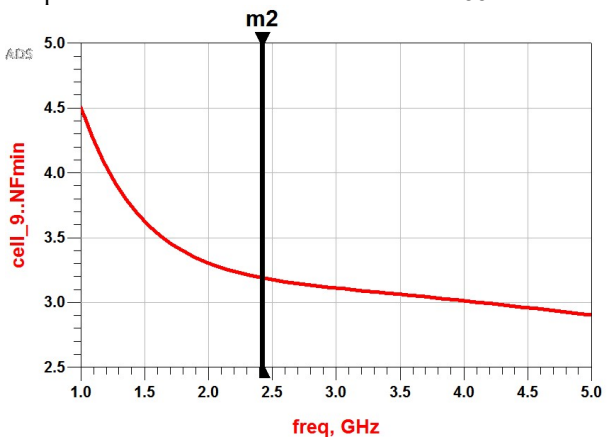


Fig. 6: Noise Figure

The noise figure is a measure of signal to noise ratio (SNR) in the circuit or signal chain. The noise figure is expressed in dB. The noise figure at 2.4 GHz for this circuit is found to be 3.190 dB.

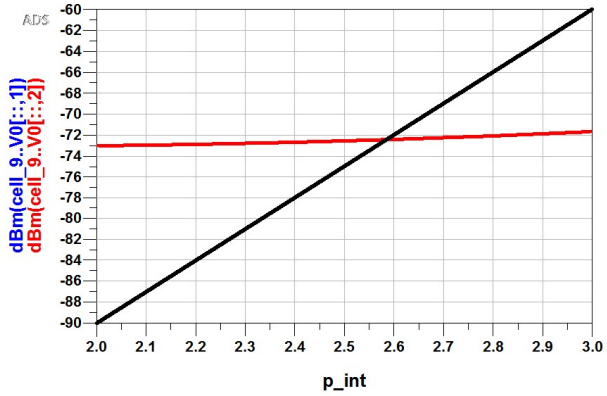


Fig. 7: Third Order Intercept Point

LNA along with having high amplification and low noise figure, should also have high linearity. The third order intercept point is a measure of linearity of the circuit. For this circuit, it is found to be 2.6 dBm, which shows that the circuit is having good gain and good linearity, without affecting the noise performance. Infact good linearity of the circuit also causes the system to become more stable.

$$IIP_3 = 10\log\left(\frac{4}{3}\left|\frac{g_m}{g_m^{11}}\right|\right) \quad \text{.....(3)}$$

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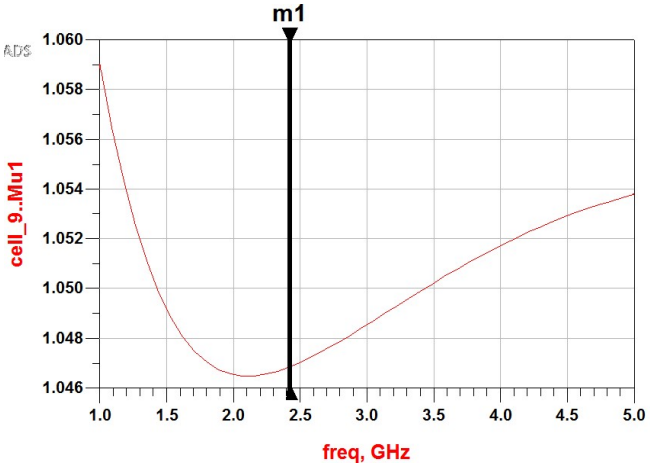

Fig. 8: Stability

Stability [9] of an LNA is its tendancy to oscillate; and maximum available gain is the measure of figure of merit for the LNA. From stability perspective, an LNA can be either potentially unstable or unconditionally stable. Oscillations occur when there is an improper matching; or due to improper load and source termination, both at the input and output. We define stability factor (k) as:

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

.....(4)

where

$$\Delta_s = S_{11}S_{22} - S_{12}S_{21}$$

Table 1: Results obtained for Proposed LNA

Technology(µm)	0.18	IIP_3(dBm)	2.6
S_{11}(dB)	-0.062	Power consumption(mW)	1.34
S_{12}(dB)	-24.23	Frequency(GHz)	2.4
NF(dB)	3.190	Supply Voltage (V)	1
S_{22}(dB)	-1.884	-	-

Table 2: Comparison of Proposed LNA with other Published Works

Ref.No.	[10]	[11]	[12]	This work
Tech(μm)	0.18	0.18	0.18	0.18
NF(dB)	2.7	2	3.08	3.10
S_{11}(dB)	-4.3	-11.1	-36.3	-0.062
P_{DC}(mW)	8.04	10.44	17.53	1.34
IIP_3(dBm)	-8.9	-4.3	-14	2.6
Supply	1	1.8	-	1
Freq.(GHz)	2.4	5.15	5.7	2.4

IV. CONCLUSION

The proposed CMOS LNA is implemented using cascode topology for input and output isolation and gain boosting technique is used for enhancing gain with feed forward cancellation method. The circuit is found to consume 1.34 mW of power which is lowest reported so far and noise figure of 3.190 dB at 2.4 GHz ISM band. The circuit is found to attain IIP_3 of 2.6 dBm and stability factor of 1.04.

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Design and Implementation of LNA for Biomedical Applications

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Abstract-LNA (low noise amplifier) is the key element of RF transceiver system. These are used for amplifying a weak, low power signal without degrading its signal to noise ratio. LNA used in radio communication system and ISM band application is capable of handling wide dynamic range of input signal without getting overloaded and undergoing saturation. In this paper, use of LNA in biomedical applications which includes neural, biosensors, ECG and EEG application is demonstrated and comparison of different LNA topologies in terms of chip area, power consumption and method of implementation has been done.

Keywords-LNA, neural, biosensors, ECG, EEG.

Introduction

LNA stands for low noise amplifier. In an RF system, LNA is used for amplifying a signal of very low strength received from antenna. These are significant part of transceiver components of an RF system. LNA is the first component of receiver which intercepts the signals and modulates the signal to noise ratio (SNR). These are low power devices having a current consumption ranging from 10 to 100 mA. LNA in biomedical domain [1] is usually implemented via cascade inductor with degenerate topology for amplifying a weak signal and providing low noise figure and high gain. In [2], fully differential RF front end amplifier is designed on 0.13µm CMOS technology for obtaining low power and direct conversion of short range radio signal at low cost. The RF signal is down-converted to a baseband signal containing dc offsets and flicker noise corrupting the SNR. Therefore common gate LNA (CG-LNA) is used instead of common source LNA (CS-LNA). Eliminating on chip inductor and providing a good input matching, it improves stability, linearity and robustness against PVT variation in CS topology. LNA of small size and low power consumption are preferred in biomedical applications. Therefore in [3], LNA using g_m boost technique is implemented on 130nm IBM technology and processed, providing a good matching of 600Ω and current consumption up to 500µA. LNA with CG topology is preferred as it consumes less power and has less sensitivity.

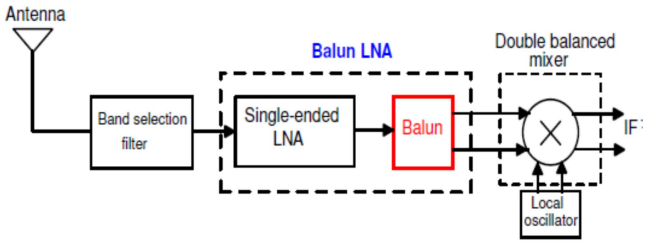

Fig. 1: BALUN LNA [3]

In [38], RF front end for biomedical applications is implemented using ultra low power and using 0.18µm technology. It uses single ended compatible current-reuse LNA (CRLNA). The LNA is capable of achieving a power gain of 20 dB with IIP3 of -8.1dBm and noise figure of 2.8dB. The RF front end consists of coupling CRLNA with quadrature folded mixer, with local oscillator buffer, achieving a conversion gain of 28.7dB and NF of 5.5dB, consuming less power of 500µW, with chip area of 0.7mm^2.

(i) LNA in Neural Applications

In biomedical applications, neural signals are dealt with the learning and comprehensive study of brain function and its healing, curative and prosthetic application. Neural signals are interfaced in large number of channels for the study of neurons specifically for brain microcircuits. The entire system consists of dealing with important parameters like noise performance, CMRR and power consumption. The entire system consists of action potentials carrying information to the neural cells. These are formed by the process of polarisation and depolarisation occurring across neural cell membrane; or these are caused due to the fast movements of ions across cell membrane. In animal cells, the ion's like Na^+/K^+ are powered by ATP molecules forming basic building blocks. Whenever channel consisting of ions is activated electrically or biochemically through mechanisms like depolarisation, voltage sensitivity is caused resulting in the opening of ions membrane containing Na^+ to open large number of positive charges across cell. However, the balance is obtained by the inflow of K^+ ions across the cell membrane. For getting sneak peak for action potential, an amplifying method is required. The neural amplifier should reject the dc offsets of the resulting signal amplitudes. The amplifier should have high SNR and proper CMRR and PSRR. The majority of neural amplifiers successfully extract input referred noise between 3-7µVrms. Without the controlling mechanism, this is entirely dominated by noise. The action potentials (Aps) across the cell membrane are found to be at 100mV. The main component of noise is mainly from muscle contraction, affecting neural

recording and intensifying brain activity. Environmental noise includes the noise from radio and electrical signals which degrade the performance drastically. Thermal and flicker noise are caused by intrinsic property of the semiconductor. In [4], the topology like Operational Transconductance Amplifier (OTA) which is common for executing LNA, is executed using two stage op-amps and current mirror OTA's. The folded cascaded combinations are shown in fig. 3]. It is expected that the topology should yield zero leakage current when compared to different amplifiers. Chae.M. et. al[5] implemented OTA with self biased topology, attaining gain of 40.5 dB and Noise Efficiency Factor (NEF) of 4.5 and consuming power up to 12.5µW. However current feedback instrumentation amplifier possesses a high impedance and an offset in mV range. Chopping at high frequency modulates noise, resulting in white band noise. This chopping at a high frequency is effectively reduced by using a notch filter in passband

Capacitive feedback topology

The capacitive feedback topology is shown in fig. 4. It is optimized for very low noise power operation through a dedicated circuit design topology. The architecture achieved a gain of 39.5dB, power consumption of 80µW and NEF of 4. Majidzadeh.V.et.al [6] achieved a modified and optimized capacitor feedback topology having a power consumption of 7.92µw and input referred noise of 3.5µV_{rms}.

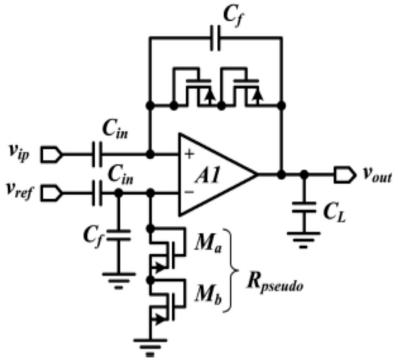

Fig. 2: Folded Cascaded Active feedback topology [5]

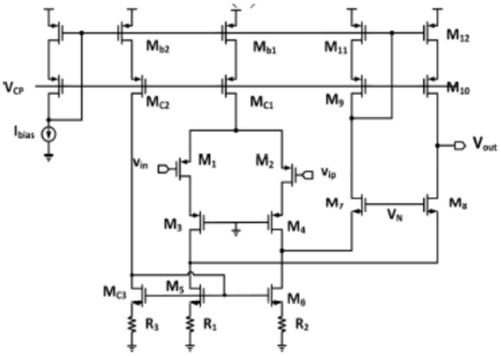

Fig. 3: Capacitive Feedback topology [6]

In this topology, a segment of a signal was filtered out, which was used as a feedback for suppressing a signal component. This is one of the efficient ways for extracting the low frequency component of a signal, which makes it a very stable system. Wei et. al employed topology for active feedback, attaining 6µW power consumption and NEF of 3.1, having a bandwidth of 8.9 KHz and a midband gain of 46dB on a chip area of 0.022mm^2. In [7], as shown in fig. 5, a MOS bipolar pseudo resistor (implemented using a cross coupled configuration) was used for implementing AC coupling and to reject the large DC offsets caused due to contact potential. Every transistor in MOS diode is connected such that a parasitic source-bulk diode is obtained in anti-parallel. If the voltage across the device is small, then neither of the diode conducts, since the effective resistance is very large (> 10GΩ). For minimizing the input referred noise, two strategies are adopted; first amplifier is reduced to a single branch which is operating at full current. The reference current so obtained is found to be 10 times the amplifier bias current, which does not contribute to the total power consumption. The second strategy [8] is to drive the gate of MP_1 and MN_1. Since the input is AC coupled, the gates of transistor MP_1 and MN_1 are avoided of DC coupling by operating it within a range of frequency. This results in doubling of the transconductance of common source amplifier while keeping output noise constant and scaling the input noise by a factor of 2. The aspect ratio of MP_1 and MN_1 are chosen for maximizing the g_m/I_d ratio and these are operated in weak inversion region. The reference current is adjusted to maximize the bias current at 770nA and obtaining the highest gain of 44dB and a bandwidth of 1.9 KHz. Thus, this topology provides the method for detection of action potentials required for neural recording.

Table1: LNA in Neural Applications

S. No.	[9]	[6]	[10]	[11]	[7]	[12]
Gain(dB)	40-56	39.4	60	76.2	39.2	15
Bandwidth (kHz)	1-10	7.2-10	<9.1-10	-	7.2	2.4-2.5(GHz)
Noise (rms)(µV)	2.2	3.5	4.8	2.89	2.2	-
Power Consumption	68	7.92	50	15.174	80	7mW
CMRR	N/A	70.1	N/A	>120dB	83	
NEF	6.62	3.35	11.42	2.35	2.9	

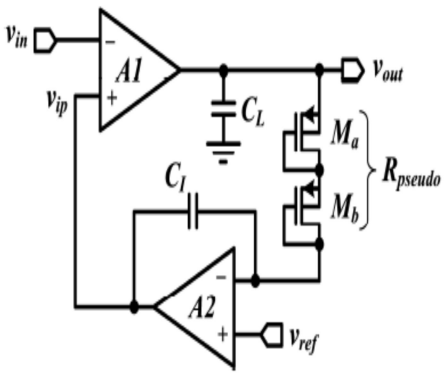

Fig. 4: Active feedback LNA Topology

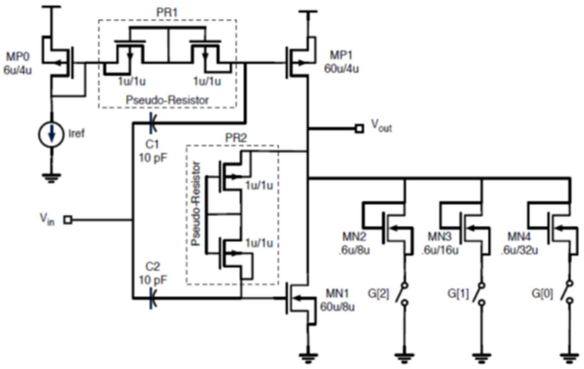

Fig. 5: Bipolar Pseudo Resistor [7]

In [11], for low power application, the LNA is executed with a wireless medical telemetry requiring a portable device capable of operating at a low supply voltage, provided from a battery and a energy source. A non coherent RF front end receiver and super-regenerative RF receiver are crucial design parameters of this module. An RF envelope detector implemented using ON-OFF keying requires a specific local oscillator executed using phase locked loop. This causes increase in the power consumption. However, for the demodulation at the RF receiver, the input signal is mixed with the signal from mixer by the process of down and upconversion of frequency. The signal is converted back to the baseband signal. Example of this is gilbert cell implemented with a CMOS simulation process, having high conversion gain and port to port isolation.

LNA are implemented using cascaded topology and since LNA implemented using current reuse technique consumes more power and because its efficiency is low at low power, these are implemented using folded topology. However for low power consumption and low voltage, RF front end amplifier are implemented using two stage common source topology. In [12], CMOS OOK is implemented at 2.4GHz requiring low voltage. LNA topology is implemented using current reuse method providing high gain and noise figure. After post simulation at 10 nano sec., digits 0 and 1 are received successfully recovering OOK data's at 100 Mbits/sec. At low frequency, the noise factor is high due to presence of two noises: thermal and flicker noise. In [11], EKV model using PMOS transistors was executed for reducing flicker noise. It had large gate area and was operated in weak inversion mode Such techniques consumed 2.89µVrms at the supply current of 4.8µA. And power consumed was 15-17µW. This can be used for neuroscience research, as the system is capable of measuring weak neural signals ranging from (0.5-5mV) and for clinical and neuro prosthetic applications having frequency ranging from 100 Hz to 7 KHz. LNA designed consisted of single ended output in which M_1 and M_2 served as a PMOS I/P transistors and M_3 and M_4 as PMOS cascade stage transistors. NMOS transistors M5 and M_6 made current mirror load. M_7 and M_8 acted as current mirror circuits. For minimising flicker noise, PMOS acted as an input for which noise power density was given by

$$E_n^2 = \frac{8kT\gamma}{g_{m1}} + 8kT\gamma\left(\frac{g_{m5}}{g_{m1}}\right)^2 + \frac{2K_p^{1/f}}{C_{ox}W_1L_1f} + \frac{2K_n^{1/f}}{C_{ox}W_5L_5f}\left(\frac{g_{m5}}{g_{m1}}\right)^2 \qquad g_{m1} \gg g_{m5},$$

And since,

$$\left(\frac{W}{L}\right)_1 \gg \left(\frac{W}{L}\right)_5$$

$$E_n^2 = \frac{8kT\gamma}{g_{m1}} + \frac{2K_p^{1/f}}{C_{ox}W_1L_1f}$$

The circuit was designed on cadence virtuso 6.1.3 and simulated on spectra simulator at a temprature of 36.9^0 C and oprating at 100 Hz frequency and having a duty cycle of 10. The noise efficiency factor was obtained by

$$NEF = Vrms\sqrt{\frac{2I_{tot}}{\pi U_T 4kT.\,BW}}$$

In the above formula, V_{rms} represents an input noise voltage and BW represents amplifiers bandwidth.

(ii) LNA in Biosensors

The term 'Biosensor' is short for "biological sensor". The device consists of transducer and biological elements consisting of enzymes, antibody or nucleic acids. The bioelements interact with the analyte being tested and biological response is converted to electrical signal by transducers. The obtained biological response of biosensors is examined by biocatalytic membrane, achieving the conversions of reactant to the product. Immobilised enzymes provide a large number of advantages making them applicable for biological systems. These can be reused ensuring catalytic activity for a series of analyses. Thus, biosensors are widely used in the field of healthcare, medical diagnosis, etc. In [13], CMOS on chip sensor was used for measuring the dielectric constant of an organic chemical. The dielectric constant was measured by observing changes in the tank capacitance producing LC oscillation in VCO, due to the exposure to the liquid. Frequency change causes change in the voltage measured, using on chip digitised analog to digital converter. The calibration of sensor was used for the measurements of dielectrics. The measurements were made for frequency ranging from 7-9 GHz. The advancements in wireless communication and network technologies have led to the significant advancement in wearable and implantable sensors creating an impact on e-health and telemetry systems. In[14], m-health comprised of mobile computing, medical sensors and communication technologies. For diagonsis and monotoring of diseases like diabetes, a large number of biosensors are worn and implanted. The interconnections are made inside a human body and the entire system is called BASN (body area sensor network) performing two operations: the transmitting of processed data and; through a secured channel, transmitting of data takes place between human body and biosensors placed at the same node. The BASN differentiates between the individuals based on their psycological and behavioural characterstics. Introduction of the ubiquitous (present everywhere) technology in healthy living regimen and medical field is called as ubiquitous healthcare [U-health] [15]which means the patient can collect and accept the information of the diagnosis therapy and prognosis management with information and communication technology. The patient is provided with biomedical digital assistant, monitoring patient health at any moment through wireless and wired mode of telecommunication. The biomedical signal is sent through a biomedical digital assistant through a remote server, providing doctor with the relevant information about patient. These devices are portable and wearable to patient. They are expected to have light weight and should be operable for 24 hours a day. The biosesnors used are ECG and PPG sensors. The biomedical devices are implemented using two methods: cellular phones and PDAs. However, wired sesnors implemented using PDA have shorter time, therefore they should be implemented wirelessly, which improves the processing and storage function of the sensors.

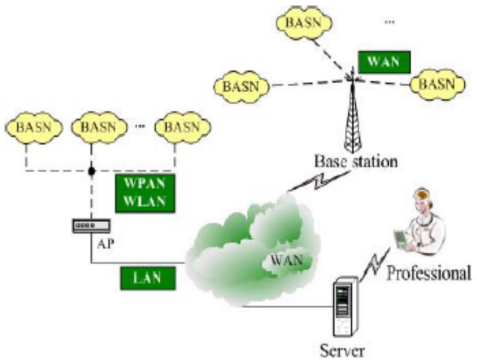

Fig. 6: BASN Health Model [14]

In [17], WBSN in health care and monitoring system was implemented consisting of wireless sensors forming a network. The data was collected through these sensors and adjacent sensors were decided by the header containing the address of adjacent node. The WBSN consisted of control path and wireless communication nodes isolated from each other. Control path added controllability and scheduling of the system at the transceiver.

Table 2: LNA in Biosensors

S. No.	[17]	[18]	[19]
Power Consumption	1440µW	4mW	2.34mW
Chip area	-	(91.4*123)μm^2	350*20μm^2
Implementation	TSMC	0.65µm	0.35µm

	(0.18µm)	CMOS	(CMOS)
Current(µA)	800	52fA	1-10µA
Supply(V)	1.8	-	3.3

(iii) LNA in ECG

Biomedical signals provide information about the physiological activities of organisms, produced by gene and protein sequences. The well-known bio signals are ECG, EEG, EMG and MMG. ECG is the acquisition of electrical activity observed from the heart and captured by the electrodes attached to the skin. These are very weak signals and because of their weak nature, noise gets added, for which signal processing is required. The ECG or electrocardiography signals are produced due to the potential difference between the two electrodes and since these are recorded for long time, the compression of data is required both at transmitting and receiver ends. The contraction of the muscles and cardiac pattern ECG signals are coupled with noise. Therefore, filtering is not easy. To solve this problem, the three algorithms applied are stress testing, ambulatory monitoring and intensive care monitoring. After signal processing of received ECG signals, its morphological characteristics and specific heart rhythms are rectified. In [20], low power and compact wearable sensors were designed. The signals were wirelessly transmitted and monitored using ECG filtering and QRS detection methods. This topology was implemented using successive approximations register (SAR) ADC using 2 SPI interfaces and on chip SRAM having central control unit of 8 Kbits. The ECG signals were sampled at a rate of 256Hz using QRS complexes and the ECG signals were then continuously written on asynchronous FIFO and were forwarded to CPU, thus consuming less power. Wearable ECG monitoring systems use electrode that requires the skin preparation in advance, so these are not suitable for high level of activity due to high level of spikes of noise that appears in the data. Therefore in [22], as shown in fig. 8, a new wearable and ultra low power wireless sensor node called eco was formed. This reduced the size and weight of the system and provided reliable operation. In [23], the conditioned biosignal was received by the encoder from a low noise amplifier and compression of N input samples gave M output samples and these were digitised and transmitted using ADC. The RF front elements were made to operate at Nyquist rate, having a conversion factor of N/M which was greater than 1, and these signals were downconverted to output y(t).

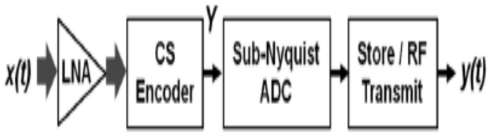

Fig. 7: LNA in ECG Measurement System

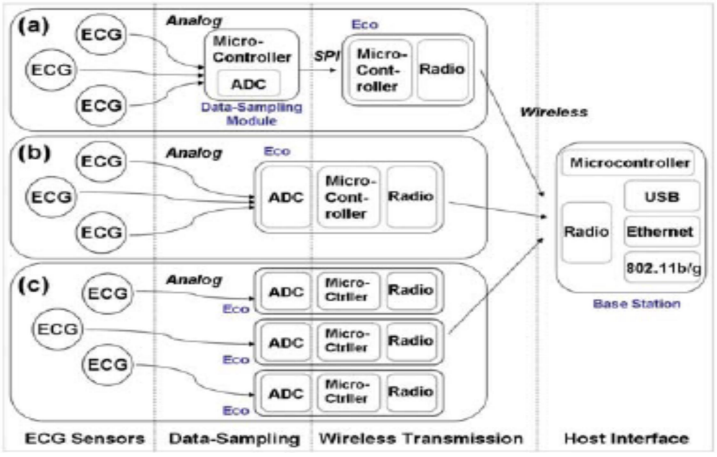

Fig. 8: Architecture of ECG monitoring system [22]

Table 3: LNA in ECG

S. No.	[21]	[22]	[24]	[25]	[26]
Implementation	On body	On cloth	0.18µm CMOS (TSMC)	0.5µm CMOS	0.18µm CMOS
Power	9.6µW	30µW	-	30µW	110µW

Consumption					
Technology	QRS and SAC diagnosis	Capacitive sensing	ARM displayer	Adaptive sampling with DSP	Current F/B topology
Area	5.74mm^2	-	-	-	-

(iv) LNA in EEG

The EEG signal which stands for electroencephalogram is a signal produced due to the electrical activity of the brain and recorded from the scalp. The recorded waveform consists of cortical, electrical activity. These are very weak signal and are measured in microvolts. The main frequency of the human EEG wave consists of Delta (frequency of 3 Hz or below), Theta (frequency of 3.5Hz and 7.5Hz), Alpha (frequency between 7.5 and 13Hz) and Beta (frequency> 14 Hz). Since these are weak signal, the voltage fluctuation measured at the electrodes is very small; the recorded data is then digitised and sent to amplifier. The amplified data can then be displayed as a sequence of voltage values. This is one of the fastest imaging techniques having high sampling rate. In [26], brain computer interfacing as a technique was used for setting up a communication path between the brain and outside environment. The authors described the method of signal acquisition and signal pre-processing. Signal acquisition using non invasion methods like electroencephalography (EEG), fMRI, NIRS and MES is considered a good practice. EEG signals are non-stationary and have low spatial resolution EEG signals are prone to artefacts caused due to muscle activities, heartbeat, blinking of eyes or eye movements, etc. Signal pre-processing is defined as a process of signal enhancement. The contamination of a signal received is caused due to artefacts and noise. Various signal processing methods include Common average deferencing (CAR), ICA (independent component analysis), etc. In [27], EEG signals were extracted through brain computer interface (BCI) techniques during mental activity. In [28], for neurological diagnosis, lossless compression of EEG signals played a crucial role. The authors presented a predictor and adaptive error modelling technique. In [29], EEG was examined using HHT (Hibertz-Huang Transform) process. For this, a de-noising process was applied for smoothening of EEG signals and was based on EMD (empirical mode decomposition) and Monte Carlo process. In [30], EEG analysis was carried out at different frequency. Experimental analysis was carried out to obtain different EEG data.

(v) LNA in Hearing Aids

Hearing aids comprise of electroacoustic devices. They are typically worn in or behind the ears and they modulate sound for hearing impaired. The microphone transforms sound to electrical signals which on further amplification is converted back to the sound by receiver. The entire process is powered by a source of a battery.

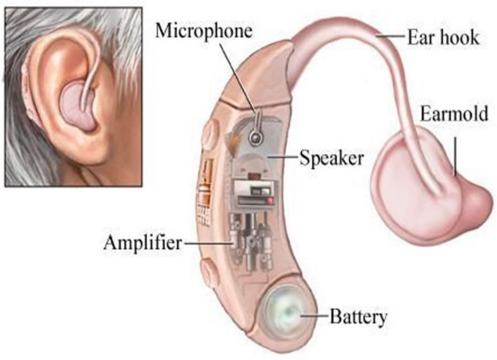

Fig. 9: Hearing Aid Device

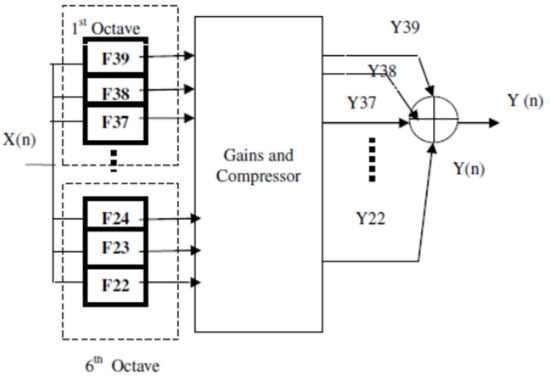

Fig.10: Parallel Band Structure [31]

In [31], the digital signal processing technique eased the filter bank designing for various applications. Filter bank algorithms were subsequently used in noise reduction, speech encoding and auditory compensation methods. The entire system design depended upon the type of filter used. In [32], binaural hearing aids were designed such that they can communicate wirelessly to both multimedia devices and smart phones. A wireless multimedia device was used along with a customised Bluetooth device with adapter. This was provided with fitting parameters controlling process which can control volume of the hearing aids using graphical user interface. Thus, system designed was efficient enough without any controlling mechanism. The wireless communication control panel was designed using FPGA kits implemented using a DSP processor. This system was capable of attaining a data rate or baud rate of 4.6 bits/sec and device was having a height of 12mm, length 46mm and width 15mm. In [33], an energy efficient analog front end circuit was designed and executed for hearing aid applications. Adaptive-SNR (ASNR) and combined gain control technique was implemented having low power consumption. The ASNR technique operated by changing the value of SNR, according to the input amplitudes, for

optimising SNR; and reducing power consumption. The method was capable of achieving 86dB SNR at a supply voltage of 0.9V. An automatic gain control was required for preamplifying hearing ability and to avoid unnecessary loud sounds.

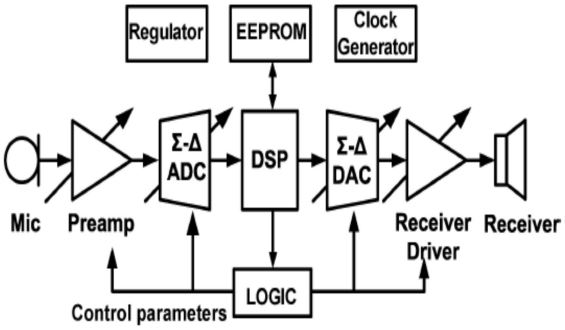

Fig. 11: Block Diagram of Hearing-Aid System [33]

(vi) LNA in Medical Implantable Devices

An implant is a medical device built for replacing a misplaced biological structure or supporting an injured biological structure. Some implantable devices are bioactive which are subcutaneous and are present in the form of implantable pills or drug eluting-stents. Implantable devices are residing within human body and are used for monitoring, diagnostic or therapeutic purposes because of their unique responsivity and rational module. These are facilitated with minimum damage caused when host tissue or biomolecule are removed. Their application areas include orthopaedic, dental, cardiovascular, etc.

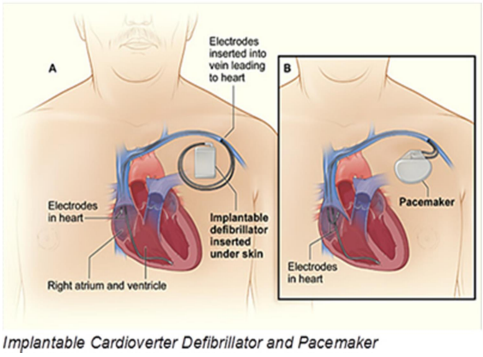

Fig. 12: Medical Implantable Device

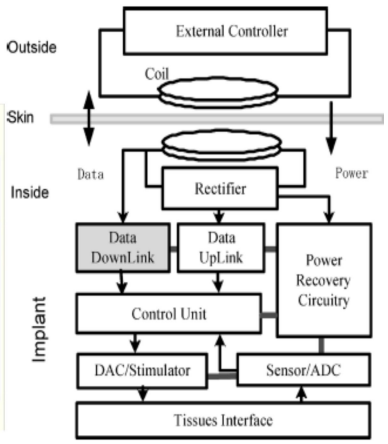

Fig. 13: Inductive Link to Transmit Power/Data [37]

In [34], biomedical implantable devices (IMDs) were designed with traditional goals such as safety and utility; without compromising the patient health. It consisted of drug delivery system, neurostimulators, pacemakers, etc. These are helpful in determination of diseases like diabetes, cardiac arrhythmia, etc. IMD ubiquitous continues to safeguard 25 million US citizens and gaining their confidence for life critical functions. In today's scenario, IMD's provide with the features of delivering telemetry for remote monitoring over a long distance and providing high wireless bandwidth and forming a communication channel with other IMDs. In [35], implantable medical devices were electronic devices implanted within a human body for therapeutic monitoring and authentication. Because of their different nature, IMD's are not fully secured or effective. However, these are only accessible by IMD programmer and medical personnel. However, the attacks like compilation of fake commands and stealing of the health related data ensures that IMD is not fully secured. Till now, we don't have distinct security standards. The authors presented basic architecture with access controlling mechanism with logics using different controlling models. The biomedical IMDs can be designed with wireless inductive link capable of consuming less power and communication of data through wireless modes. In [36], BPSK modulator was used for designing COSTAS loop topology dedicated to medical devices. The analysis revealed data rate or baud rate of 1.12Mbps; and power less than 0.7mW was consumed with a supply voltage of 1.8V. The coupling of BPSK modulator along with passive modulator allowed full duplex data transmission between the controller and the medical IMDs. This ensures and increases the durability of the entire system.

In [37], wireless implantable medical devices required a continuous source of power supply which poses a threat to the health related issues. Here, the system was setup consisting of antenna and capable of operating at MHz frequency range. So that the large number of losses from the tissues could be compensated. This work presented an antenna having a size much smaller; and provided with the same power efficiency in the specified range of frequency of operation.

Conclusion

Biomedical applications in the field of biomedical engineering include the development and designing of biomedical instruments capable of solving medical and health related problems. These instruments range from cosmic imaging systems like standard X ray, magnetic resonance imaging, etc. to the evolution of numerous therapeutic medical devices like EEG, MRI, etc. used for diagnosis. Here, in this paper, we have reviewed the designing and implementation of LNA using various topologies in biomedical applications like neural applications, biosensors, ECG, EEG, hearing aids, medical implantable devices, etc.

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Appendix-II

List of Communicated Papers

1. **Malti Bansal, Gaurav Srivastava, "High Linearity High Stability Cascode CMOS LNA for RF Front-End Applications.**
2. **Gaurav Srivastava, Malti Bansal, "A High Linearity Shunt Capacitive Feedback LNA for Wireless Applications**

High Linearity & High Stability Cascode CMOS LNA for RF Front-End Applications

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Abstract-**In this paper, we present a high linearity and high stability CMOS LNA with source degenerate topology followed by cascode topology. The circuit is implemented in ADS using TSMC 45nm technology using Intermodulation distortion technique for RF front end applications. The LNA is observed to have S_{11}=-47.536dB, S_{12}=-41.067dB, S_{22}=-28.018dB, S_{21}=14.072dBm and NF =4.060dB from a 1V power supply and the circuit is having an IIP_3=9dBm at 2.4GHz frequency.**

Keywords—LNA, Cascode topology, Source degenerate topology, Intermodulation distortion (IMD) technique.

I. INTRODUCTION

Radio frequency refers to the electromagnetic signals used in wireless communication. This includes the waves ranging from 3 KHz to 300 GHz where frequency refers to the rate of oscillations (of the radio waves). The waves propagate at the speed of light in free space carrying voice, video and data at microwave frequency [1]. RF communication includes many industrial applications like mobile platform networking, radar system, remote monitoring and many more. In contrast, RF modules, transceivers and SOCs often include data link layer for supporting one or more communication protocols. One of the major wireless applications: Zigbee IEEE 802.15.4 [2] at 2.4 GHz requires devices with low power consumption, high data rate with simple networking protocols. Its applications like WPANs (wireless personal area network) and IoT (Internet of Things) are implemented using mesh networking topologies in which the network setup consists of nodes capable of interacting with each other.

The major block of the RF front end receiver section includes low noise amplifier (LNA) which increases the amplitude of the weak RF signal for its processing at the receiver end without adding noise or distortion to the signals. The transceiver architecture designed for wireless sensor networks requires low power consumption and its configuration and designing is based on designers requirements. Its important [3] characteristics include dynamic range, selectivity, sensitivity, linearity, leakage effect and image band rejection ratio. However, the important characteristics of LNA are bandwidth of operation, stability, linearity, supply voltage and chip area optimising and controlling these parameters requires adequate knowledge of active devices and components and there methods of fabrication; with fewer trade-offs. This paper is simulated at 2.45GHz ISM band which stands for industrial, scientific and medical band defined by ITU radio regulations which are internationally reserved for radio frequency applications.

Organisation of this paper is as follows: section II gives the brief description of the topologies, intermodulation technique and matching circuits. Section III describes the circuit and simulation results and comparison of work is done. In section IV conclusion is given.

II. PROPOSED LNA

The proposed circuit is implemented using a cascode topology [4] which consists of common source stage of the first amplifier connected to the common gate stage of the second amplifier. This topology provides better stability, better gain, input output isolation and high slew rate. However, it causes higher input impedance due to the miller effect causing reduction in the gain which can be optimized using gain boosting technique or adjusting the biasing currents. The source degenerate topology with inductive termination provides an efficient input matching network of 50 Ω input resistance without the resistive thermal noise. the source degenerate reactance causes the wideband CMOS LNA to attain minimum noise figure and for attaining minimum input power condition, another inductor is placed at the gate of the MOSFETs so that the combined network including C_{ex} can resonate at the desired frequency of operation. However, the excessive source inductance can cause LNA to oscillate because of higher gain at high frequency. The input matching network allows the system to attain minimum S_{11} [5] without introducing additional noise. Main transistor section ensures that the system attains high linearity, high gain and minimum noise figure at the time of proper input and output matching network. The input and output impedance matching network ensures the maximum power transfer by minimizing the reflections which is attained when $Z_L=Zs^*$. Intermodulation distortion technique is defined as a method of interaction of two or more signals in a nonlinear way. The intermodulation product generates signals due to the addition and differences of the original set of signals. This method improves the third order intercept point by using the passive components which forbids the use of auxiliary amplifier for the suppression of the third order distortion components and therefore circuit does not incur extra power consumption.

III. CIRCUIT DESIGN

The proposed circuit is implemented using a pie matching network through C_1, L_1 and C_2 having 2 degree of freedom. The M1 forms a source degenerate topology with inductor Ls to provide a 50Ω termination, thus, improving the linearity and gain of the circuit. The external inductance Lg and Ls and capacitance Cex are found to be resonating at 2.45GHz frequency. The M2 forms the cascoded structure which provides the input and output isolation. The increase in the input resistance of the circuit causes the gain of the

circuit to reduce which is optimized by adjusting the biasing currents. The resistance at the input of M2 causes the reduction in the noise figure of the circuit. The linearity or IIP3 is improved by IMD technique implemented using M3 PMOS folded transistor by cancelling the first and third g_{m1} and g_{m3} with those of M1.

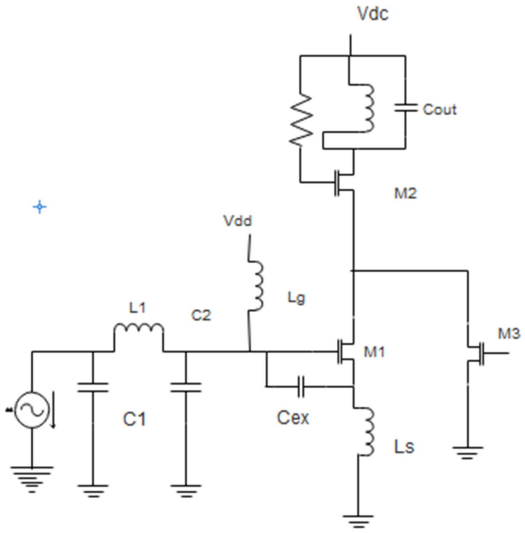

Fig. 1: Circuit Diagram for Proposed LNA

$$z_{in} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega Cgs} + \frac{gmL_s}{Cgs}$$

.....(1)

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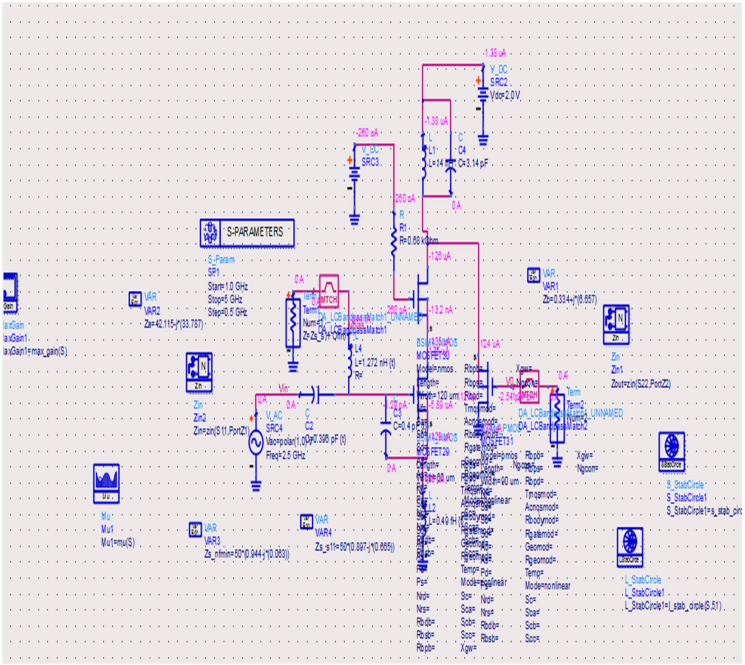

Fig. 2: Schematic for Proposed LNA

IV. SIMULATION RESULTS AND COMPARISON

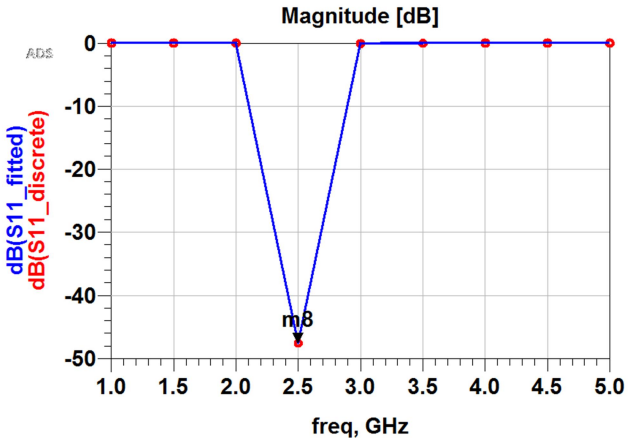

Fig. 3: Input Return Loss

The S_{11} parameter is called input voltage reflection coefficient and it gives the estimate of the input RF signal bounced of the LNA at 2.45 GHz. S_{11} for proposed LNA is -47.536dB.

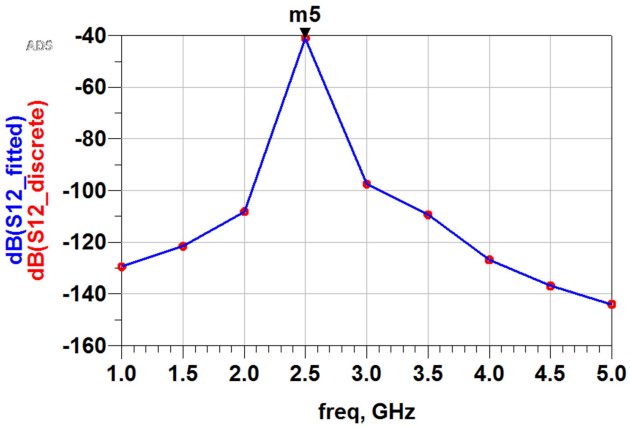

Fig. 4: Reverse Transmission Coefficient

S_{12} is also called as reverse transmission coefficient. It determines the amount of input signal reflected back or the amount of isolation between the input and the output ends. The S_{12} parameter at 2.45GHz for the proposed LNA is found to be -41.067dB.

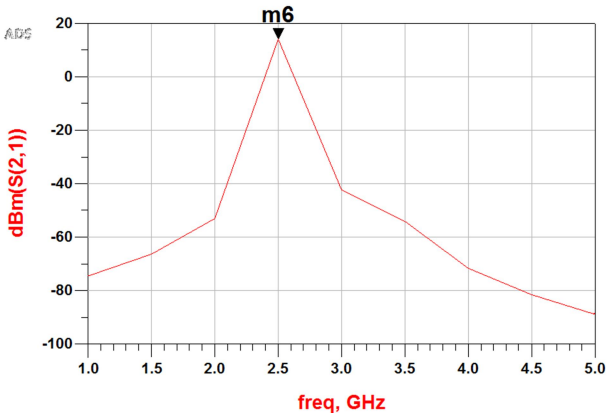

Fig. 5: Forward Transmission Coefficient

S_{21} is also called as forward voltage gain or forward transmission coefficient. It measures the power gain of the

LNA. The S_{21} parameter at 2.45 GHz for the proposed LNA is found to be 14.074dBm.

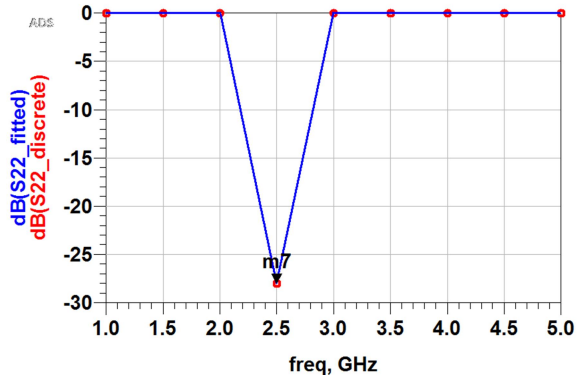

Fig. 6: Output Reflection Coefficient

The S_{22} is also called as output voltage reflection coefficient. It determines the matching between the load impedance and output impedance. The S_{22} parameter is found to be -8.018dB at 2.45 GHz frequency for the proposed LNA.

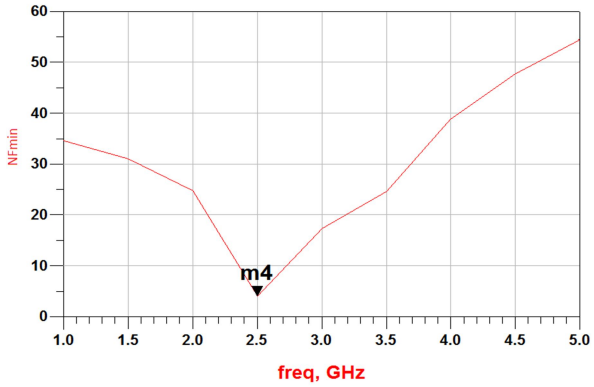

Fig. 7: Noise Figure

The noise figure is a measure of degradation in the signal to the noise ratio. The lower the value of noise figure, the better is the performance of the receiver. At 2.45GHz, the noise figure for the proposed circuit is found to be 4.060dB.

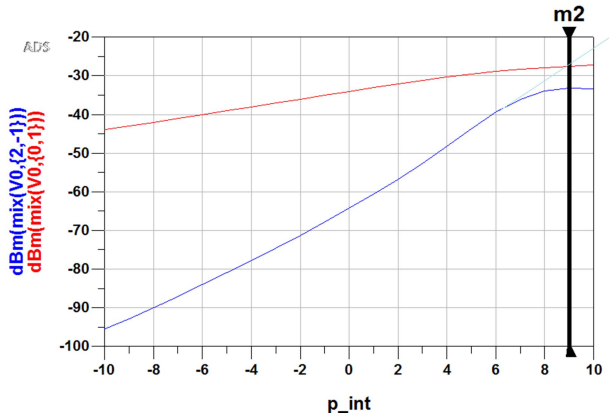

Fig. 8: Third Order Intercept Point

An ideal LNA along with having high amplification and low noise figure, should also have high linearity. The third order intercept point is a measure of linearity of the circuit. For our circuit, third order intercept point is found to be 9.0 dBm which shows that the circuit is having good gain and good linearity without affecting the noise performance. Infact, good linearity of the circuit also causes the system to become more stable.

$$IIP_3 = 10\log\left(\frac{4}{3}\left|\frac{g_m}{g_m^{11}}\right|\right)$$

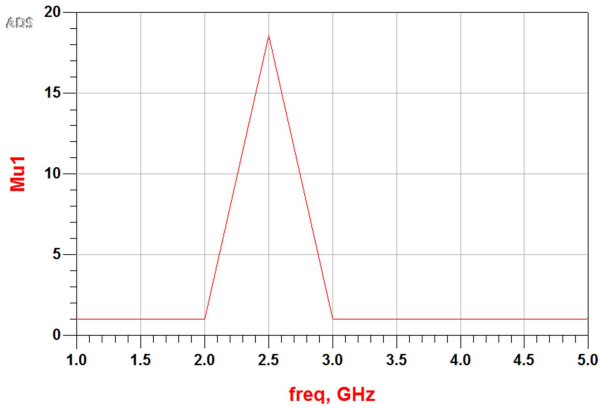

Fig. 9: Stability

Stability of an LNA measures the tendency of an amplifier to oscillate [7]. From LNA prospective, it can be either unconditionally stable or potentially unstable. Oscillations occur when there is an improper matching between the output impedance and load impedance or at the source end. The stability factor of an LNA is determined by two factors: Rollett stability factor or Mu. (Mu>1)is the sufficient and necessary condition for unconditional stability for a two port network.

Rollett stability factor or K>1 for unconditionally stability:

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

where

$$\Delta_s = S_{11}S_{22} - S_{12}\,S_{21}$$

Table 1: Results obtained for Proposed LNA

Technology	45nm	IIP_3(dBm)	9.0
S_{11}(dB)	-47.536	Power consumption (mW)	3.59
S_{12}(dB)	-41.067	Frequency (GHz)	2.45
NF(dB)	4.060	Supply Voltage (V)	1
S_{22}(dB)	-28.018	S_{21}(dBm)	14.074

Table 2: Comparison of Proposed LNA with other Published Works

Ref. No.	[8]	[9]	[10]	This work
Technology	130 nm	90nm	45nm	45nm
NF(dB)	3.34	4.34	1.42	4.060
S_{11}(dB)	-16.5	-11.32	-18.43	-41.067
P_{DC} (mW)	3.9	17.4	1.98	3.54
IIP_3 (dBm)	-10	8.7	-9.87	9.0
Supply (V)	0.9	1	1	1
Frequency (GHz)	2.44	2.44	2.45	2.45

V. CONCLUSION

The proposed LNA circuit is implemented using a source degenerate topology providing an efficient input matching of 50Ω and noise figure of 4.060dB. It is followed by cascode topology which provides input and output isolation with better stability. The circuit is found to be consuming 3.54mW of power and attains a S_{11}= -41.067dB and IIP3 of 9.0dBm with a stability factor of 18; which is the best reported so far. Hence, we have designed a high linearity and high stability cascode CMOS LNA for RF front end applications.

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A High Linearity Shunt Capacitive Feedback LNA for Wireless Applications

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***Abstract*-In this paper, CMOS LNA with low noise and high linearity with shunt capacitive and CS with inductive degenerate topology is presented . LNA is implemented in ADS on 0.18µm TSMC technology. The LNA is designed for RF Front end so the important parameters are gain, linearity and noise figure. The circuit designed exhibits a good I/P and O/P reflection coefficients with low power consumption which is crucial for LNA designing. The presents circuit attains S_{11}=-22.06 dB, S_{12}=-2.77 dB, S_{21}=9.4 dB, and S_{22}=-104.85 dB and NF= 1.23 dB and IIP3= 56.86 dBm for 6 GHz frequency band used for future mobile communication or 5G technology.**

Keywords—*Cascode topology,LNA,pie matching,shunt capacitive feedback ,Source degenerate topology .*

I INTRODUCTION

Wireless communication is the procedure of information transmission over a distance without the need for cables, wires and other electrical network. In RF domain the wireless communication occours through electromagnetic spectrum ranging from 30 Hz to 300 GHz. In modern era the wireless communication involving RF front end circuits are designed for applications like IOTs (internet of things), LTE and 5G connectivity [1]. Modern and future mobile devices need to support increasing number of frequency band and wireless standards and the applications like Bluetooth, Wi-Fi (802.11/a/b/g/n) standards ranging in 2.4 and 5 GHz band and mobile television. It should also support 4G LTE networking [2] consisting of 40 frequency band globally ranging from 700 MHz to 6 GHz. Other wireless application lies in UWB which is defined as data transmission in the form of radio energy spreaded over the entire bandwidth with a low power spectral density. The frequency range of UWB ranges from 3.1- 10.2 GHz. In [3] a wideband amplifier with a resitive feedback topology is implemented for UWB applications the LNA consist of input-matching network and single to differential amplifier acting as a voltage buffer for improving power gain. However, it faces challenges like pulse shape distortion (low powered signal distorted by transmission link), low transmission power , channel estimation and high frequency synchronisation . As compared to 4G network 5G network requires to be versatile, scalable and energy smart for the hyper connected IOE world. In [4] By using advanced modulation methods massive MIMO and beam forcing techniques 5G connectivity are expected to achieve data rate of (10 Gbps) with universal coverage having high efficiency and spatial diversity.[5] 5G spectrum has three key frequency for widespread coverage capable of supporting all users and cases. Three frequency ranges are sub-1GHz, 1-6 GHz and above 6 GHz. 6 GHz radio (LANs) are less prone to interfere with the spectrum for fixed microwave, satellite digital radio , telecom backhauls. Therefore, 6 GHz draft plan is under study with a goal of ensuring its use in wideband channel applications. The LNA designed for such wireless applications are required to have matching network for selecting specific range of frequencies, good linearity flat gain with low noise figure. The LNA designed should have low power consumption and area occupied should be less.

Organisation of the content for this paper is as follows section II gives the brief description of the topologies, shunt capacitive feedback topology and matching circuits. Section III description of the circuit followed by simulation results. Section IV conclusion and comparison of work is made.

II DESIGN METHODOLOGY

LNA implementation involves three basic topologies like common source , common gate and cascode topology . The choice of the CS or CG is determined by the robustness of the I/P and O/P matching network or low noise figure in the circuitry. CS stage provides low noise figure as compared to CG stage. In the present circuit common source stage is cascoded with the common gate stage which provides better I/P and O/P matching, isolation, better stability and low noise figure. [6] The capacitance feedback topology provides additional optimization of NF. However, this topology provides high linearity, low noise figure and gain. The present circuit is implemented with pie matching network providing two degrees of freedom in the form of quality factor of the circuit and For attaining the ideal resistance of 50 Ω a common source with inductor degenerate is implemented.

III. CIRCUIT DESIGN

In the given circuit C1, C2 and inductor L2 forms a pie matching network. The shunt capacitance C3 along with source degenerate inductor L3 attains I/P impedances of 50Ω. The mosfet M1 with common source and M2 with common gate topology forms a cascoded stage providing isolation between input and output and circuit attains high linearity with low noise figure. The feedback capacitor C3 is in shunt configuration. Thus, the circuit attains negative feedback causing the system to become unconditionally stable which improves the gain lower noise figure and causes the circuit to attain high linearity. The DC blocking is obtained through capacitor C4. The series network of L3 and resistance R2 acts as a loading element of the cascode stage and for further increasing the gain and bandwidth the second stage of source follower M3 is used.

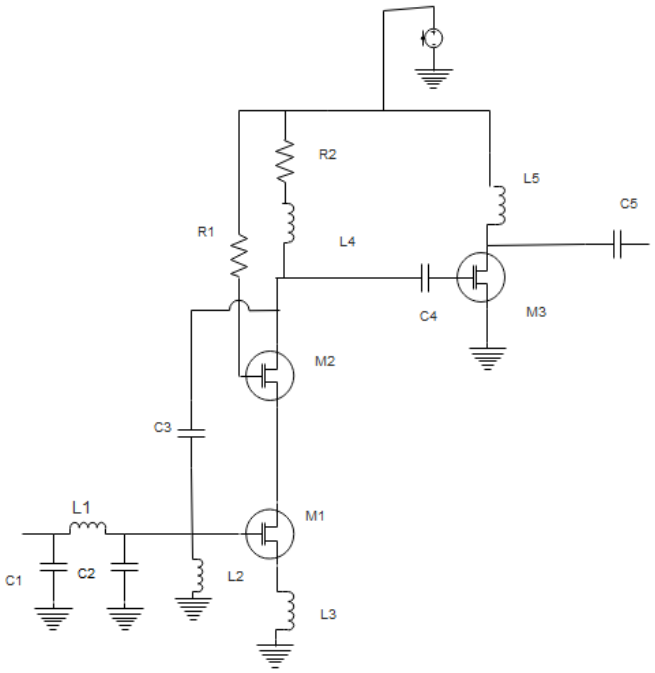

Fig. 1: Circuit Diagram for Proposed LNA

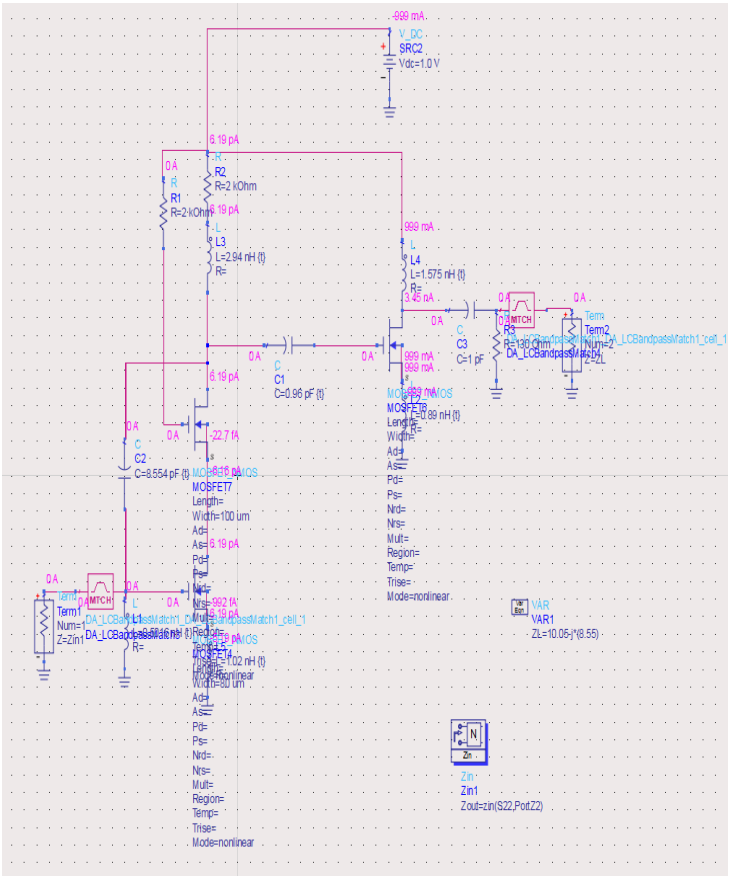

Fig. 2: Schematic for Proposed LNA

IV RESULTS AND COMPARATIVE ANALYSIS

Fig. 3: Input Return Loss

The parameter S_{11} denotes the input return loss or reflection coefficient. For measuring S_{11}, at I/P port signal is injected and reflected signal at the same port is measured for this no signal is coupled to the output port so, it denotes the matching between the input and characteristics impedance or reference impedances. For 6 GHz the S_{11} obtained is -22.09 dB as shown in fig (3)

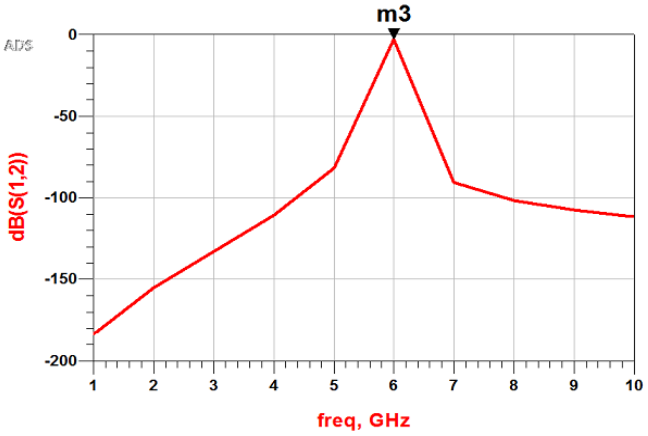

Fig. 4: Reverse Transmission Coefficient

S_{12} is also called as reverse transmission coefficient.It calculates the I/P signal reflected back or measures the isolation b/w the I/P and O/P port. The S_{12} parameters for this circuit is -2.75 dB.

S_{21} is also called as forward voltage gain or forward transmission coefficient it measures the signal transmitted from the I/P to the O/P or the intensity of the signal reaching the O/P for this circuit the S_{21} obtained is equal to 9.4 dB as shown in fig(5).

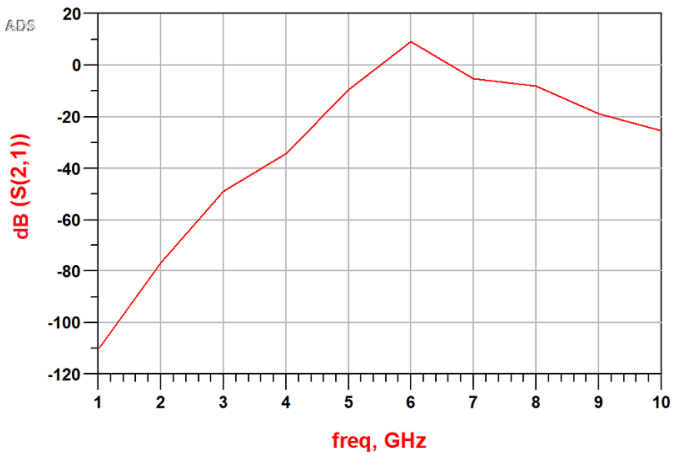

Fig. 5: Forward Transmission Coefficient

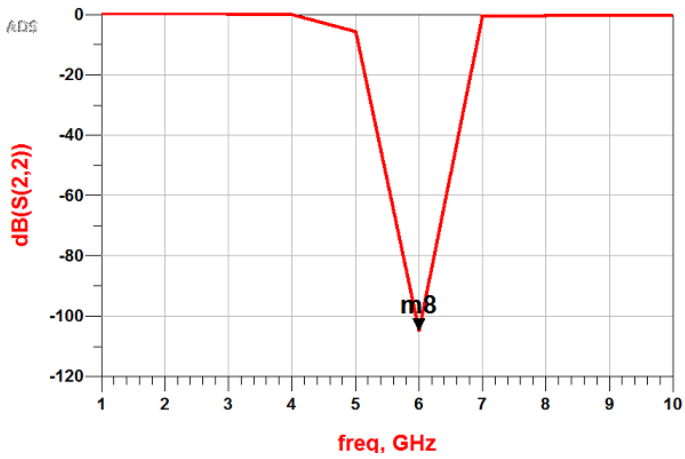

Fig. 6: Output Reflection Coefficient

The S_{22} is also called as output voltage reflection coefficient or output return loss. For measuring S_{22} at O/P port signal is injected and the reflected signal at the same port is measured for this no coupling of signal takes place so, it denotes the matching between the output and the reference impedances. For 6 GHz the S_{22} obtained is equal to -104.85 dB.

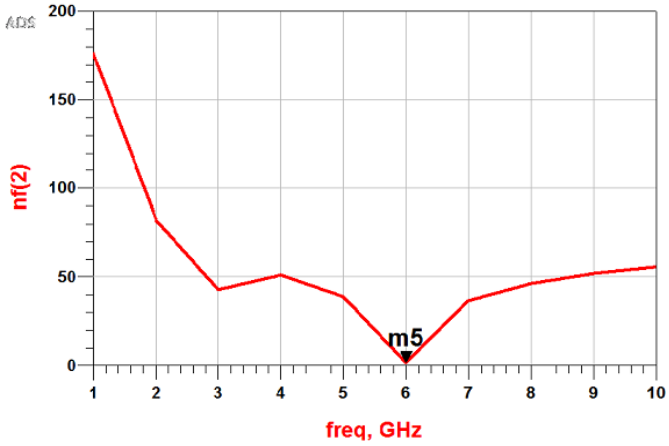

Fig. 7: Noise Figure

The parameter NF (noise Figure) is a measure of SNR. It calculates the degradation in the signal to noise ratio. The small value of the NF denotes the performance of the circuit is better for the present circuit NF=1.23 dB as shown in the fig (6).

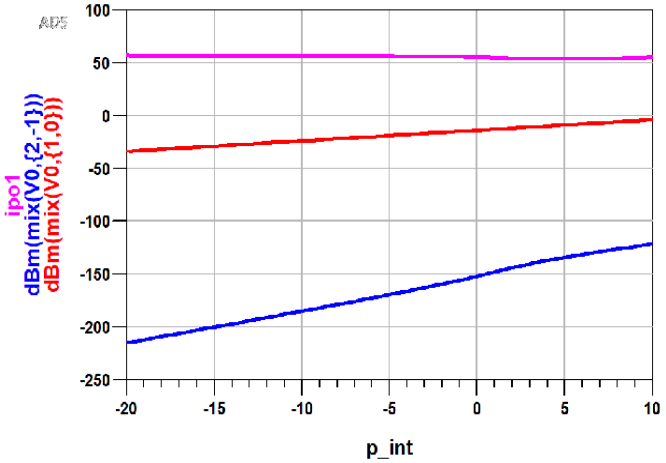

Fig. 8: Third Order Intercept Point

The characteristics of LNA are determined by high amplification factor and low noise figure along with it circuit should have high linearity. Linearity of the circuit is measured by third order intercept point. In this circuit the IIP_3 is found to be 56.89 dBm which denotes the circuit with low noise figure attains high linearity causing system to become relatively more stable.Thus , it implies that[7] from the fact that circuit can either have moderate gain , low noise figure or high linearity or moderate gain with high noise figure and low linearity.

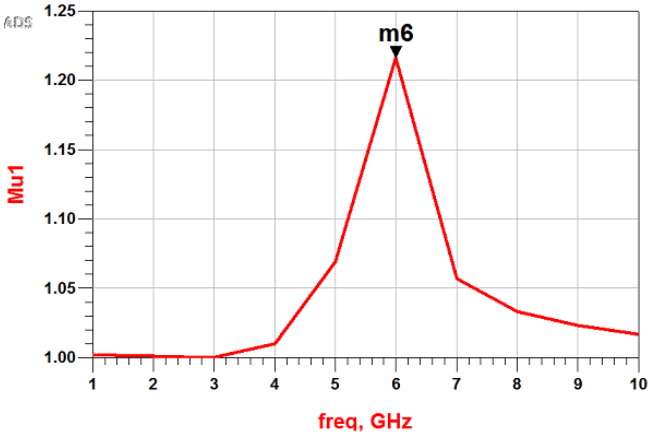

Fig. 9: Stability

Stability of an LNA [7] measures the tendency of an amplifier to oscillate. It is defined as immunity against spurious oscillations. The circuit becomes unstable for specific combination of source and load impedances. An LNA designed oscillate at extreme of voltage variation for low or high frequency. Therefore, the stability of an amplifier is given by two factors K and Δ where K denotes rollet's stability factor or stern stability factor. The stability factor of this circuit is 1.21.

Rollett stability factor or K>1 for unconditionally stability.

$$k = \frac{1 - |s_{22}|^2 - |s_{11}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} > 1$$

Where $\Delta_s = S_{11}S_{22} - S_{12}S_{21}$

V CONCLUSIONS

The proposed CMOS LNA is implemented using cascode topology for input and output isolation and shunt capacitive feedback topology providing high linearity to the circuit it is implemented with source degenerate inductor topology to achieve matching circuit of 50Ω. The circuit is found to consuming 0.035 mW of power and noise figure of 1.23 dB at 6 GHz band for wireless application . The circuit is found to attain IIP3 of 56.82 dBm and stability factor of 1.21 with output return loss or S_{22}= -104.85dB which is best so far.

Table 1 Comparison of Proposed LNA with other Published Works

Ref.No.	[8]	[9]	[10]	This Work
Tech(µm)	0.13	0.18	0.18	0.18
NF(dB)	1.8	2.7-3.38	2.5-3.5	1.23
S_{11}(dB)	-1.3	-10.61	-12.6	-22.06
Pdc(mW)	-	8.65	8.14	0.035
IIP_3(dBm)	3	-	-	56.89
Supply(V)	1.2	1.2	1	1
Freq(GHz)	3.1-10.6	3-11	2-6	6

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