Current Differencing Current Conveyor and its Applications

A thesis submitted in fulfillment of the requirements for the award of the

Degree

of

Doctor of Philosophy

by

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Certificate

Certified that the thesis entitled, '**Current Differencing Current Conveyor and Its Applications**', which is being submitted by Shri Alok Kumar Singh for the award of Doctor of Philosophy in Electronics and Communication Engineering, Delhi Technological University, Delhi, is a record of student's own work carried out by him under our supervision and guidance. The matter embodied in this thesis has not been submitted for any other degree.

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गुशब्दस्त्वन्धकारः स्यात् **रु**शब्दस्तन्निरोधकः।
अन्धकारनिरोधित्वात् **गुरु**रित्यभिधीयते॥ १६॥

The syllable *gu* means darkness, the syllable *ru*, he who dispels them,
Because of the power to dispel darkness, the guru is thus named.
— Advayataraka Upanishad, Verse 16

गुरुर्ब्रह्मा गुरुर्विष्णु र्गुरुर्देवो महेश्वरः
गुरु साक्षात परब्रह्मा तस्मै श्रीगुरवे नमः

Guru is the Creator (Brahma), Guru is the Preserver(Vishnu), GuruDeva is Destroyer(Maheshwara)
Guru is the absolute (singular) Lord himself, Salutations to that Sri Guru.

गुरू पारस को अन्तरो, जानत हैं सब संत।
वह लोहा कंचन करे, ये करि लेय महंत।।

पारस मणी के विषय जग विख्यात है कि उसके स्पर्श से लोहा सोने का बन जाता है।
All the wise men know the difference between Guru and Paras. The subject of Paras Mani, the world is famous that with its touch iron becomes gold.
किन्तु गुरु भी इतने महान हैं कि अपने गुण-ज्ञान मे ढालकर शिष्य को अपने जैसा ही महान बना लेते हैं।
But the gurus are so great that they can make the disciple as great as their own in their knowledge.

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(Alok Kumar Singh)

Index

List of Figures

List of Tables

List of abbreviations used in the thesis

ABBs	Active Building Blocks
ASIC	Application Specific IC
BP	Band Pass
CA	Current Amplifier
CBTA	Current Backward Transconductance Amplifier
CCCCTA	Current Controlled Current Conveyor Transconductance Amplifier
CCCDTA	Current Controlled Current Differencing Transconductance Amplifier
CC-CFA	Current Controlled Current Feedback Amplifier
CCCFCC	Current Controlled Current Follower Current Conveyor
CCCFTA	Current Controlled Current Follower Transconductance Amplifier
CCCII	Second–Generation Current Controlled Conveyor
CCII	Second–Generation Current Conveyor
CCIII	Third–Generation Current Conveyor
CCII-TA	Second-Generation Current Conveyor Transconductance Amplifier
CDBA	Current Differencing Buffered Amplifier
CDCC	Current Differencing Current Conveyor
CDDIBA	Current Differencing Differential Input Buffered Amplifier
CDDIDOBA	Current Differencing Differential Input Differential Output Buffered Amplifier
CDDITA	Current Differencing Differential Input Transconductance Amplifier
CDDOBA	Current Differencing Differential Output Buffered Amplifier
CDOA	Current Differencing Operational Amplifier
CDTA	Current Differencing Transconductance Amplifier
CDU	Current Differencing Unit
CF	Current Followers
CFBCCII	Current-Controlled Fully Balanced Second Generation Current Conveyor
CFCC	Current Follower Current Conveyor
CF-MOCC	Current Follower Multiple-Output Current Conveyor
CFOA	Current Feedback Operational Amplifier
CFTA	Current Follower Transconductance Amplifier
CI	Current Inverter

CICC	Current Inverter Current Follower
CM	Current Mode
CM	Current Mirror
CMOS	Complementary Metal Oxide Semiconductor
CTTA	Current Through Transconductance Amplifier
CVBA	Current Voltage Buffered Amplifier
CVCC	Current Voltage Current Conveyor
CVDIBA	Current Voltage Differential Input Buffered Amplifier
CVDOBA	Current Voltage Differential Output Buffered Amplifier
CVTA	Current Voltage Transconductance Amplifier
DACA	Digitally Adjustable Current Amplifier
DBTA	Differential-Input Buffered Transconductance Amplifier
DCCII	Differential Current Conveyor
DDA	Differential Differential Amplifier
DIBOCOA	Differential Input Balanced Output Current Operational Amplifier
DVCC	Differential Voltage Current Conveyor
DVCCCTA	Differential Voltage Current-Controlled Conveyor Transconductance Amplifier
DXCCII	Dual X Second–Generation Current Conveyor
FBDDA	Fully Balanced Differential Difference Amplifier
FBFTFN	Fully Balanced Four-Terminal Floating Nullor
FBFTFNs	Fully Balanced Four Terminal Floating Nullor
FDCCII	Fully Differential Second Generation Current Conveyor
FD-CF	Fully-Differential Current Follower
FDCFOA	Fully Differential Current Feedback Operational Amplifier
FDCMUF	Fully-Differential Current-Mode Universal Filter
FDNR	Frequency Dependent Negative Resistance
FTFN	Four-Terminal Floating Nullor
GVCCIII	Gain–Variable Third-Generation Current Conveyor
LP	Low Pass
MCDTA	Modified Current Differencing Transconductance Amplifier
MCFOA	Modified Current Feedback Operational Amplifier
MICCI	Modified Inverting First-Generation Current Conveyor

MO-CCCDTA	Multiple-Output Current Controlled Current Differencing Transconductance Amplifier
MOCCII	Multi-Output Second Generation Current Conveyor
MO-CFCC	Multiple-Output Current Follower Current Conveyor
MO-CFTA	Multiple-Output-Current Follower Transconductance Amplifier
MO-CICC	Multiple-Output-Current Inverter Current Conveyor
MO-CITA	Multiple-Output Current Inverter Transcondctance Amplifier
MOTA	Multi- Output Operational Transconductance Amplifier
OTA	Operational Transconductance Amplifier
OTRA	Operational Trans-Resistance Amplifier
S-E	Single-Ended
SIMO	Single Input Multi-Output
TSMC	Taiwan Semiconductor Manufacturing Compancy
VCR	Voltage Controlled Resistors
VDBA	Voltage Differencing Buffered Amplifier
VDCC	Voltage Differencing Current Conveyor
VD-DIBA	Voltage Differencing-Differential Input Buffered Amplifier
VDIBA	Voltage Differencing Inverting Voltage Buffered Amplifier
VDTA	Voltage Differencing Transconductance Amplifier
VDU	Voltage Differencing Unit
VF	Voltage Follower
ZC CFCCC	Z-Copy Current Follower Current Controlled Conveyor
ZC-CDBA	Z-Copy CDBA
ZC-CDTA	Z-Copy CDTA
ZC-CFTA	Z-Copy Current Follower Transconductance Amplifier

Chapter 1

Introduction

After reviewing the evolution of the various active circuit elements in a historical perspective, it has been pointed out that the current differencing current conveyor (CDCC) or any variant of this have not received much attention in the literature in the context of the synthesis and design of analog electronic circuits. It has been pointed out that this void has been the main reason for exploring the characterisation and applications of the CDCC for the research reported in this thesis.

1.1 Introduction

This thesis deals with a new analog circuit building block known as Current Differencing Current Conveyor (CDCC) and its variants and their applications in circuit synthesis and design.

In modern integrated circuits, analog and digital signal processing circuits both are required to be integrated on the same chip. In contrast to the conventional voltage mode, which utilizes electric voltages, the current mode circuits can exhibit under certain conditions among other things higher bandwidth and better signal linearity. Moreover, there is continued demand for the circuits to operate on lower power supplies, because of which low voltage analog design with wide dynamic range and high linearity is challenging. This is one of the main reasons for a lot of research work being carried out in the current mode (CM) circuits in which the principal signals are in the form of currents, rather than voltages [1]. The CM circuits offer one or more of the following attractive features in several applications: superior bandwidth, lower operating voltages, enhanced linearity, low power consumption, and simple architecture. Apart from using discrete transistors, analog signal processing was traditionally carried out with the help of Integrated circuit amplifiers (Operational Amplifiers, Operational Transconductance Amplifiers etc.). With the introduction of current conveyor and current feedback amplifier ICs (CCII01, PA630, AD844) these ICs are also being used in analog signal processing.

More recently, the advent of CM signal processing alongwith developments in modern IC fabrication technology, has seen a new trend in analog signal processing research wherein new active building blocks (ABBs) comprised of a combination of current conveyor blocks, transconductance blocks, current differencing blocks, voltage buffers and current buffers, current mirrors have emerged. Since the work presented in this thesis deals with a modern active building block named CDCC, it is worthwhile to present a brief overview of the

evolution of the various new active building blocks since the time of introduction of the integrated circuit operational amplifiers.

1.2 Active building blocks available as Off-the-shelf ICs

The introduction of the integrated circuit operational amplifier in mid-sixties was a natural consequence of the developments taking place in semiconductor fabrication technology and the advantages offered by ICs (reduction in size, power consumption, economy of scales etc.). Though operational amplifiers had come around early 40s, these were vacuum tube based and occupied very large space. The first mass produced IC operational amplifier was Fairchild's μA741 which came around 1966-67. It was an internally compensated voltage amplifier with differential-input but single-ended output. Internal frequency compensation was provided by an on-chip compensating capacitor of typical value in the range 25pF-30pF. The amplifier had a unity gain bandwidth of around 1MHz. Several excellent text books have appeared in literature in which details of the architecture of this amplifier, its analysis and its various applications have been presented [2]- [5].

Another very important integrated circuit amplifier, CA 3080 which became very popular with analog circuit designers was introduced in 1969 at RCA. It was a transconductance amplifier whose gain could be controlled externally by changing its bias current.

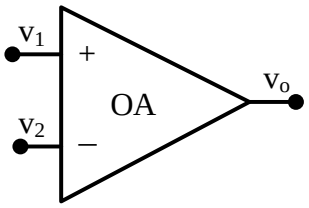
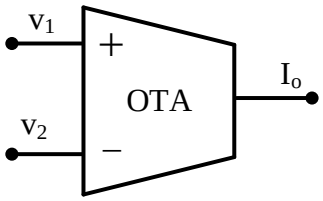
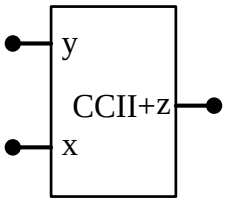
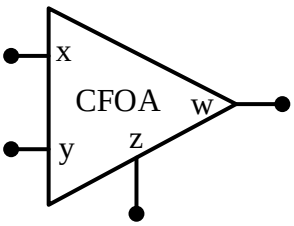
The current-mode approach in analog signal processing had started gaining currency during this time and appearance of an integrated circuit amplifier with a current output became very handy in implementing a number of current-mode circuits. The front end of this amplifier was a differential amplifier and thus the linear range of this amplifier was restricted to less than $\pm 2V_T$. In later versions of this IC such as LM13600/13700 diode linearization scheme was used to enhance its linear range. Applications of this amplifier in analog signal processing have been well documented. Some of these may be found in [6]-[11] and the references cited therein.

The second half of sixties witnessed a lot of research and development activities in analog signal processing. The introduction of current conveyors [12], [13] by Sedra and Smith was one such development. The current conveyors have attracted lot of attention from the analog signal processing community worldwide and it is also available in integrated circuit form from several semiconductor manufactures namely CCII01 from LTP Electronics, PA630 from Phototronics Limited and AD844 from Analog devices. Though AD844 is not available by the name of current conveyor but it contains a CCII+ whose terminals are externally accessible. The current conveyor can also be thought of as among the first active building blocks which combined the characteristics of two functionally independent blocks, namely, a voltage follower and a current follower. The current conveyor IC had one very low impedance input terminal 'x' and a very high impedance terminal 'y'. Its output current is available at a very high output impedance terminal 'z'. Like the operational transconductance amplifier, the current conveyor and its numerous variants have been used to implement all kinds of analog signal processing/generation circuits. A research monograph on current conveyors containing most of the important implementations, applications and other related aspects has appeared in literature recently [14].

The development of truly complementary bipolar process with PNP and NPN transistors having comparable performance characteristics led to the introduction of a new amplifier architecture, namely, the trans-impedance amplifier, alternatively referred to as current feedback amplifier. This nomenclature was assigned to this structure so as to distinguish it from the conventional voltage amplifier architecture in which the feedback employed was voltage. This architecture offered several advantages over the conventional voltage feedback amplifier viz. (i) very high slew rate (ii) constant bandwidth operation for medium to moderately large values of the closed loop gain. Typical values of slew rate attainable are in the range 2000-9000V/us. The first integrated circuit current feedback op-amps (CFOA) were AD844 from

Analog Devices Inc. (Designed by Barrie Gilbert) introduced in 1984 and the other one introduced by Elantec in 1987. A CFOA is functionally equivalent to a CCII+ followed by a voltage buffer. The external compensation pin available separately in AD844 makes possible the use of this IC as second generation current conveyors of both kinds (CCII+ using one AD844 and CCII- using two AD844s). If the compensation pin is left open, then this IC is pin-compatible with μA741 type integrated circuit operational amplifiers. Different Bipolar/CMOS architectures of the current feedback amplifiers and their numerous applications in analog circuits have been given in [15]. The Table 1.2.1 given below gives the terminal equations and the standard symbols used to describe these active building blocks.

Table 1.2.1 Basic Active Elements (available as off-the-shelf ICs)

Symbol and Port-relationship	
 $V_o = A_0(V_1 - V_2); V_1 = V_2; I_1 = I_2 = 0$	 $I_1 = I_2 = 0; I_o = g_m(V_1 - V_2)$
 $I_y = 0; V_x = V_y; I_z = I_x$	 $I_y = 0; V_x = V_y; I_z = I_x; V_w = V_z$

1.3 Other active elements

The developments in the semiconductor fabrication technology, largely on account of concurrent developments in fast processors and industrial applications of computers and

microcontrollers during the last couple of decades have led to many developments in the field of analog signal processing. Application specific ICs (ASIC) are a reality now. The simultaneous integration of analog and digital circuits on the same piece of silicon requires ever decreasing supply voltages for these ICs to be used in various portable applications. Newer techniques and ideas for processing of analog signals are needed to keep pace with such developments. Various new active building blocks, integrable versions of which (both CMOS and Bipolar) have been proposed by researchers, came up in response to either overcome some of the major limitations of the existing building blocks e.g. very small value of slew rate of voltage operational amplifiers or its gain-bandwidth conflict, very small linear range of operation of transconductance amplifiers or specific signal processing problems (e.g. realisation of a particular filter configuration with all grounded passive elements and independently tunable parameters, realisation of a harmonic oscillator with fully decoupled control of condition of oscillation and frequency of oscillation etc.). Some of the important active building blocks so developed are now described briefly.

OTRA: Chen, Tsao and Chen in 1992 introduced the new active building block namely, Operational Trans-resistance Amplifier (OTRA). The CMOS implementation of the OTRA did not suffer from the gain-bandwidth conflict. Inverting amplifier, non-inverting amplifier and MOSFET-C differentiator realizations using the OTRA have been presented in [16].

CDBA: In 1999, Acar and Özoğuz proposed Current Differencing Buffered Amplifier (CDBA) as a versatile active building block useful for realization of analog filters. Its CMOS realization and an alternate realization using commercially available ICs (AD844) have been presented in [17].

CDTA: Biolek, in 2003, presented the Current Differencing Transconductance Amplifier (CDTA) as a versatile active building block especially suitable for current-mode signal

processing. It had currents as the input and output variables. Several application examples using CDTA in realization of current-mode filters were also presented in [18].

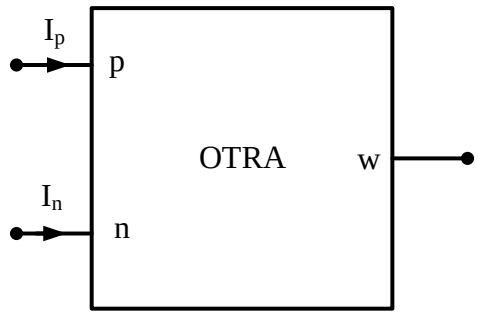
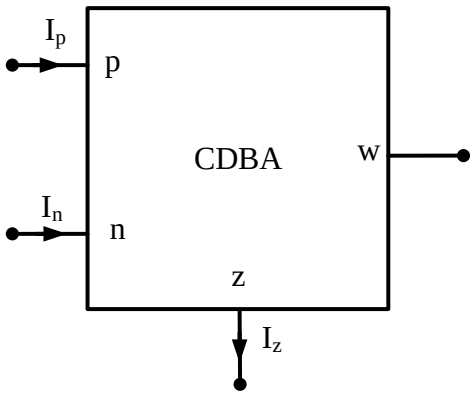
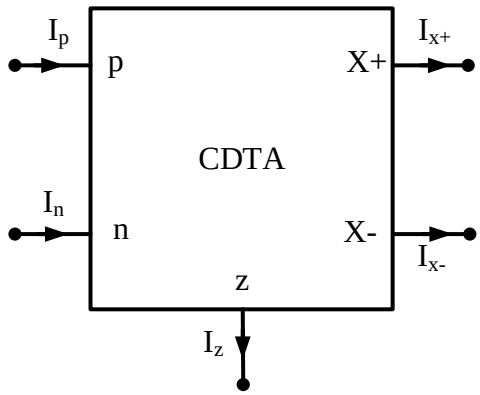
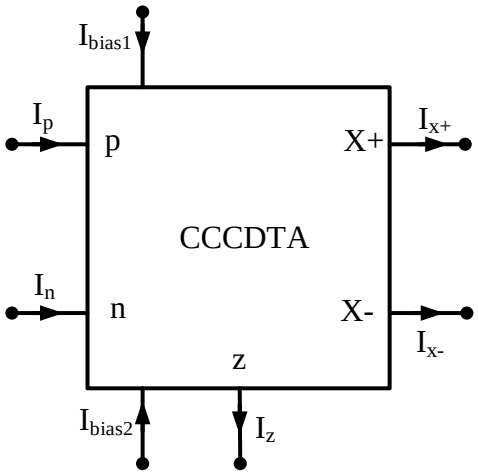
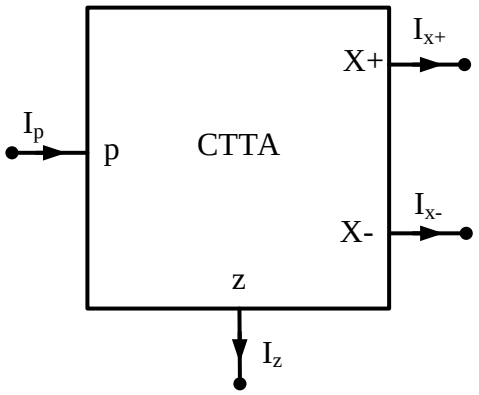
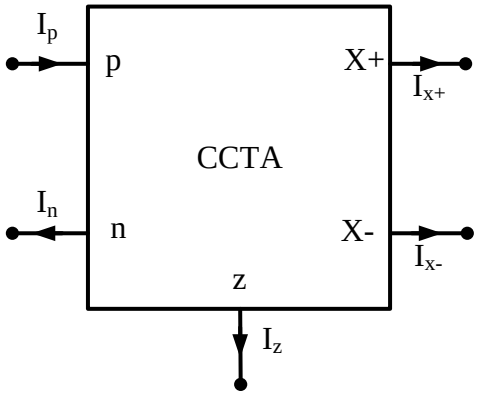
CTTA: The active building block Current through Transconductance Amplifier (CTTA), presented in [19] was also introduced by Biolek and Gubek in 2004. This amplifier had characteristics similar to that of the CDTA except the input current differencing unit which was replaced by a current 'through' unit which presented a short circuit to the input current. The application of CTTA in realization of current controlled impedance has been presented in [19]. The difficulties in realization of the 'current through unit' led to the development of CCTA, the Current Conveyor Transconductance Amplifier by Prokop and Musil [20] in 2005. In CCCTA, a current controlled conveyor is used to sense the input current.

Like several variants of the basic current conveyors, numerous variants of CDBA, CDTA and CCTA have appeared in literature for use in various kinds of signal processing and generation circuits. A detailed discussion of these variants and their applications is beyond the scope of this thesis and hence has not been attempted here. Table 1.3.1 shows the symbols and terminal/port relations of the active building blocks described above.

1.4 Novel Active Elements

In 2008 Biolek, Senani, Biolkova, and Kolka,[21] presented a very comprehensive review of the developments of various active building blocks employed in analog signal processing. They had given a different perspective to the development of the existing active building blocks in terms of fundamental building blocks viz. voltage followers (VF), current followers (CF), voltage differencing units (VDU), current differencing units (CDU), current inverters (CI) and current mirrors (CM). The terminal equations of most of the existing active building blocks were shown to be derivable from an interconnection of these fundamental blocks.

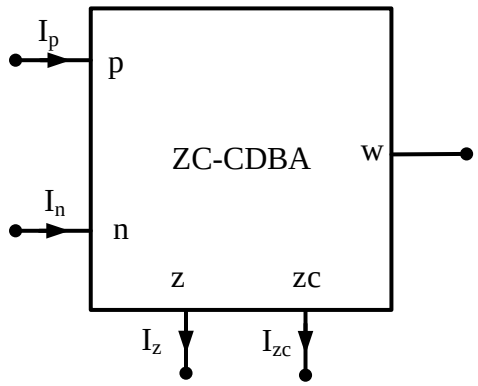
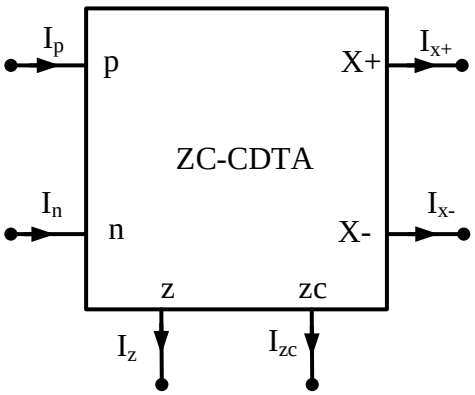
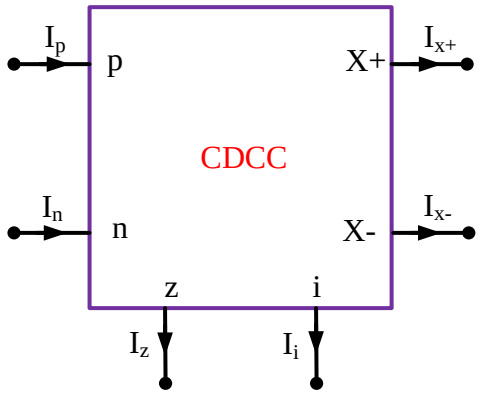
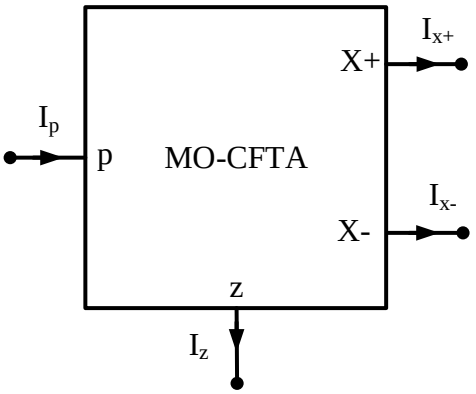
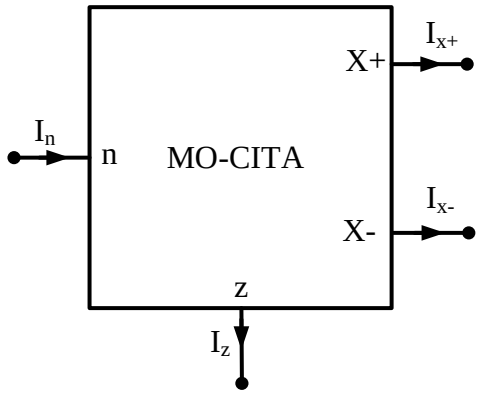
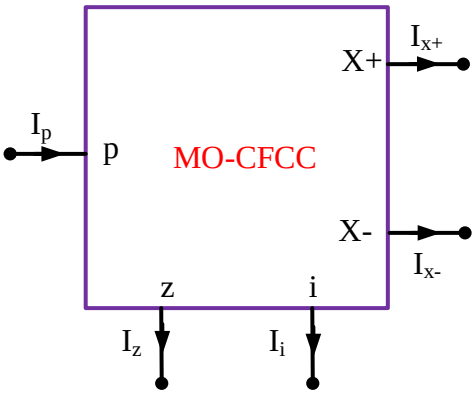
Table 1.3.1 Some other active elements

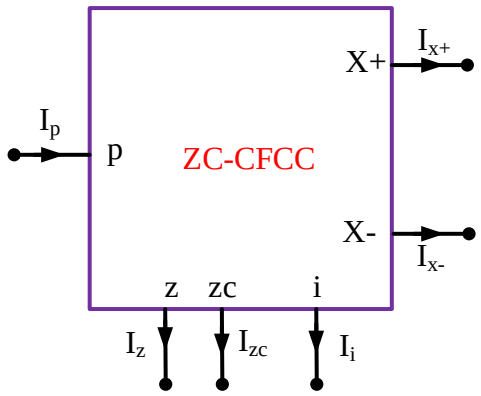
Port-relationships of various ABBs	
	
$V_p = V_n = 0; V_w = R_M (I_p - I_n)$	$V_p = V_n = 0; I_z = (I_p - I_n); V_w = V_z$
	
$V_p = V_n = 0; I_z = (I_p - I_n); I_{x+} = -I_{x-} = g_m V_z$	$V_p = R_p I_p; V_n = R_n I_n; I_z = I_p - I_n; I_{x+} = -I_{x-} = g_m V_z$
	
$I_z = I_p; V_w = R_M (I_p - I_n); V_p = 0; I_{x+} = -I_{x-} = g_m V_z$	$I_p = I_n; V_n = V_p; I_z = I_n; I_{x+} = -I_{x-} = g_m V_z$

In addition, they also took cognisance of the existence of standard amplifiers like operational amplifiers, operational transconductance amplifiers, current conveyors and current feedback amplifiers etc. and proposed a set of new active building blocks in which these amplifier configurations and combinations of VF/CF/VDU/CDU/CI/CM have been used. The following novel elements were proposed in this paper: Z-copy CDBA (ZC-CDBA), Z-Copy CDTA (ZC-CDTA), current differencing external transconductance amplifier (CDeTA), current differencing current conveyor (CDCC), multiple-output-current follower transconductance amplifier (MO-CFTA), multiple-output current inverter transcondctance amplifier (MO-CITA), multiple-output current follower current conveyor (MO-CFCC), multiple-output-current inverter current conveyor (MO-CICC), voltage differencing buffered amplifier (VDBA), voltage differencing transcoductance amplifier (VDTA), voltage differencing current conveyor (VDCC), current differencing differential input buffered amplifier (CDDIBA), current differencing differential input transconductance amplifier (CDDITA), current differencing differential output buffered amplifier (CDDOBA), current differencing differential input differential output buffered amplifier (CDDIDOBA), current voltage transconductance amplifier (CVTA), current voltage current conveyor (CVCC), current voltage buffered amplifier (CVBA), current differencing operational amplifier (CDOA), current voltage differential input buffered amplifier (CVDIBA) and current voltage differential output buffered amplifier (CVDOBA). The terminal relation-ships of these ABBs are given in Table 1.4.1.

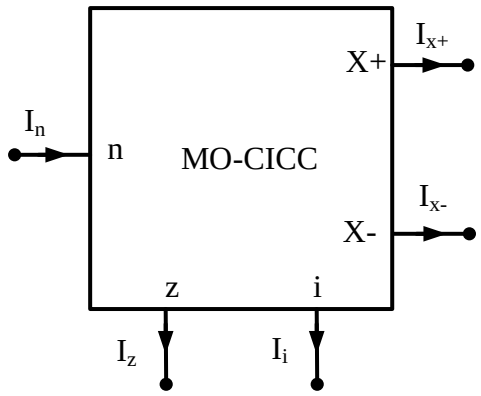
Many of these newly proposed active building blocks and other similar blocks have been used by various researchers in various signal processing and signal generation applications (see [22-48] and the references cited therein).

Table 1.4.1 Novel active elements introduced in [21]

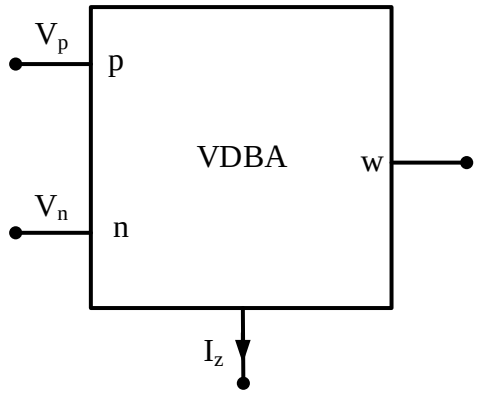
Port-relationships of various ABBs	
 $V_p = V_n = 0; I_z = I_{zc} = (I_p - I_n); V_w = V_z$	 $V_p = V_n = 0; I_z = I_{zc} = I_p - I_n; I_{x+} = -I_{x-} = g_m V_z$
 $V_p = V_n = 0; I_z = (I_p - I_n); V_i = V_z; I_{x+} = -I_{x-} = I_i$	 $V_p = 0; I_z = I_p; I_{x+} = -I_{x-} = g_m V_z$
 $V_n = 0; I_z = -I_n; I_{x+} = -I_{x-} = g_m V_z$	 $V_p = 0; I_z = I_p; V_i = V_z; I_{x+} = -I_{x-} = I_i$



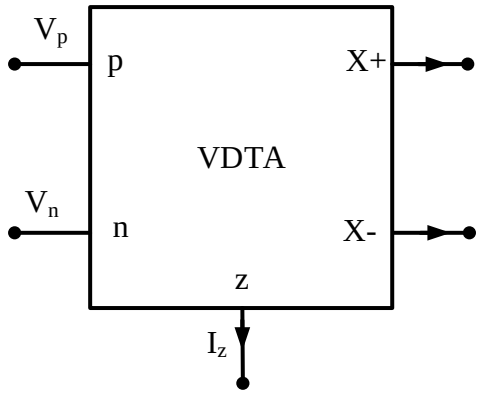
$V_p = 0; I_z = I_{zc} = I_p; V_i = V_z; I_{x+} = -I_{x-} = I_i$



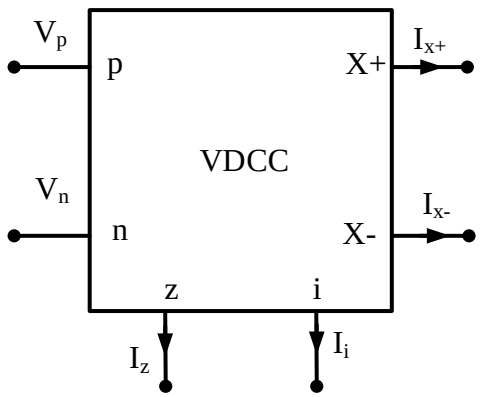
$V_n = 0; I_z = -I_n; V_i = V_z; I_{x+} = -I_{x-} = I_i$



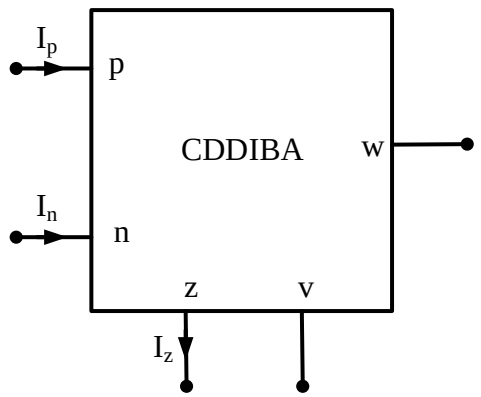
$I_p = I_n = 0;\ I_z = g_m\left(V_p - V_n\right); V_w = V_z$



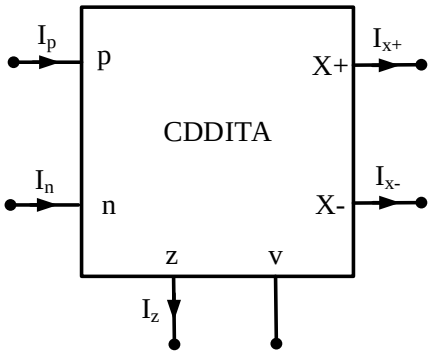
$I_p = I_n = 0; I_z = g_{m1}\left(V_p - V_n\right); I_{x+} = -I_{x-} = g_{m2} V_z$



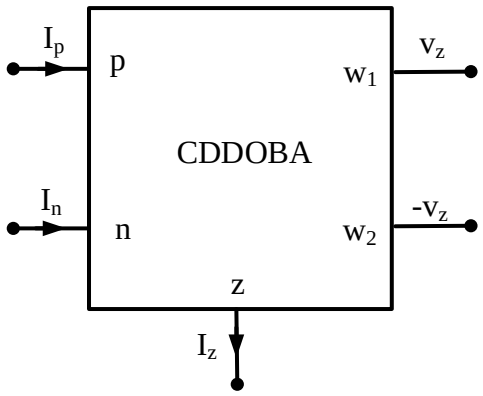
$I_p = I_n = 0; I_z = g_m\left(V_p - V_n\right); V_i = V_z; I_{x+} = -I_{x-} = I_i$



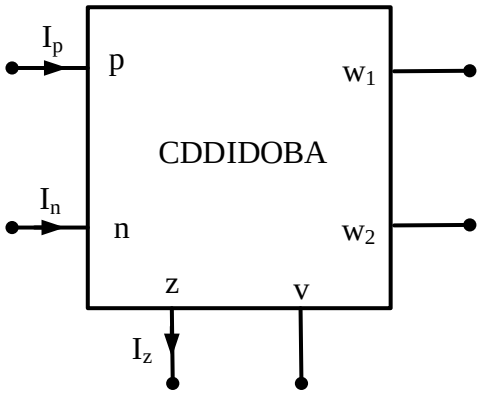
$V_p = V_n = 0;\ I_z = (I_p - I_n); V_w = V_z - V_v$



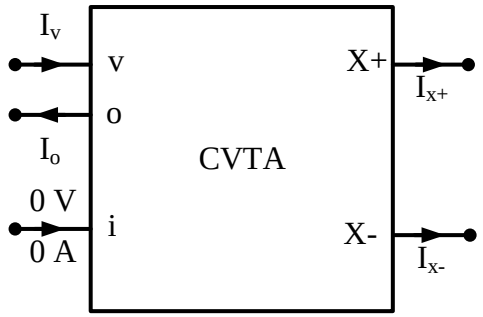
$$V_p = V_n = 0; I_z = (I_p - I_n); I_{x+} = -I_{x-} = g_m (V_z - V_v)$$



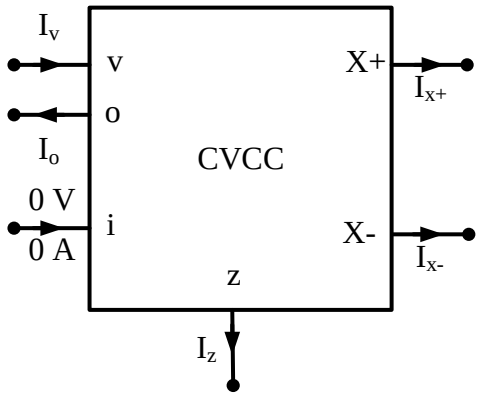
$$V_p = V_n = 0; I_z = (I_p - I_n); V_{w_1} = -V_{w_2} = V_z$$



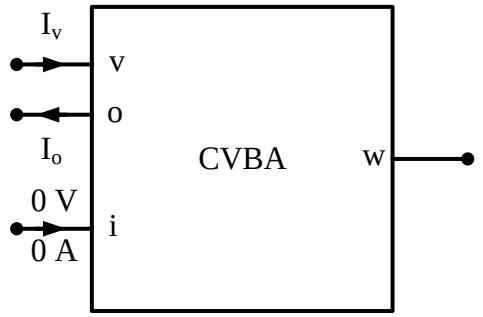
$$V_p = V_n = 0; I_z = (I_p - I_n); V_{w_1} = -V_{w_2} = V_z - V_v$$



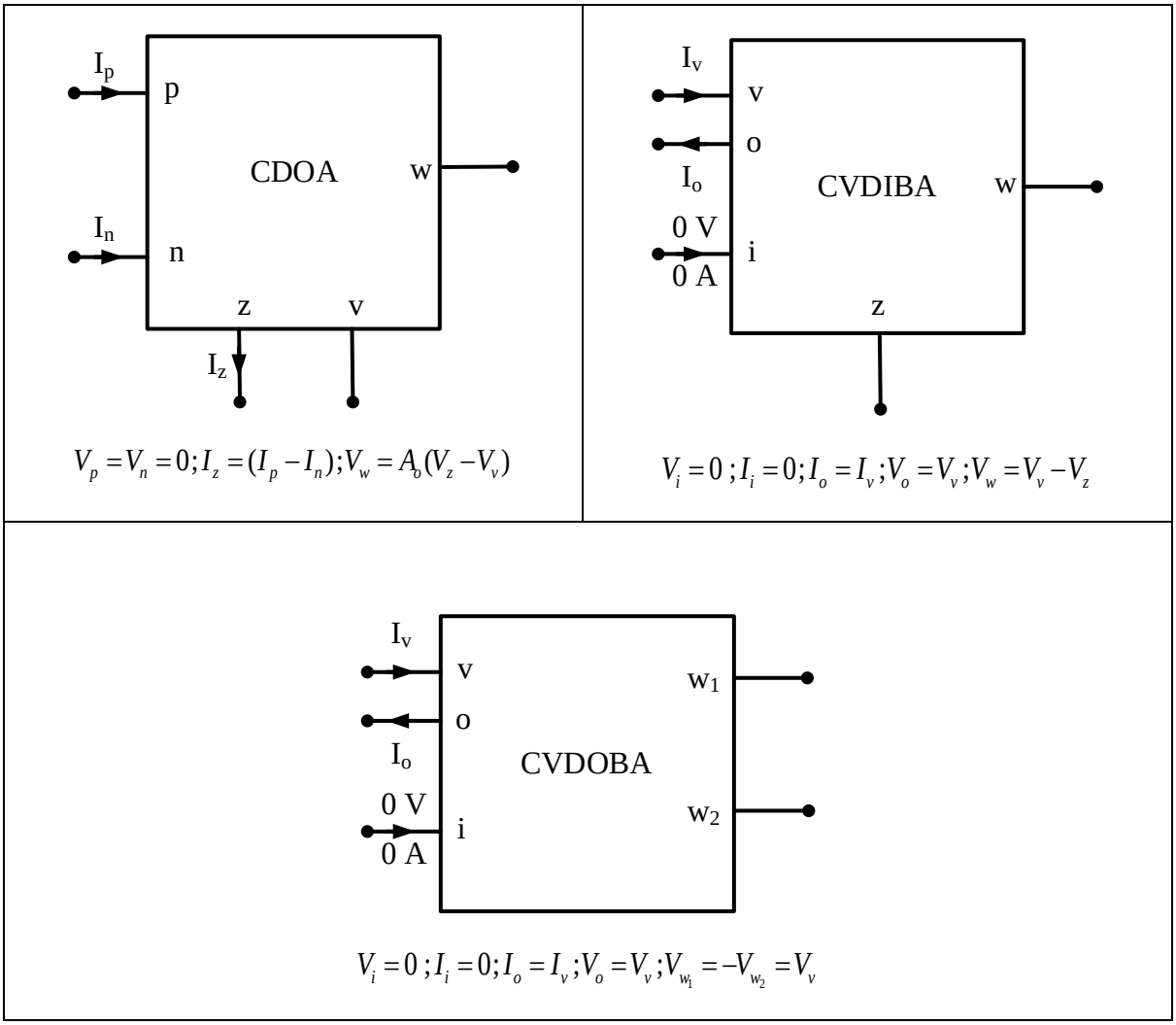
$$V_i = 0; I_i = 0; I_o = I_v; V_o = V_v; I_{x+} = -I_{x-} = g_m (V_i - V_v)$$



$$V_i = 0; I_i = 0; I_o = I_v; V_o = V_v; I_{x+} = -I_{x-} = I_z$$



$$V_i = 0; I_i = 0; I_o = I_v; V_o = V_v; V_w = V_v$$



1.5 The Current Differencing Current Conveyor (CDCC)

From the literature survey it was found that amongst the proposed novel active elements given in Table 1.4.1, CDCC and its variants viz. CFCC /ZC-CFCC had not received any attention in open literature as compared to other building blocks till the time the work proposed in the thesis started (November 2011)[1]. It was thus decided to investigate the CDCC and some of its variants (CFCC/ZC-CFCC) and their applications for the work reported in this thesis.

The behavioural model of the current differencing current conveyor (CDCC) was given in [21] and is shown below in Fig.1.5.1

[1] Although two publications on CDCC [49], [50] did appear later during the course of this work (November, 2011-September, 2018).

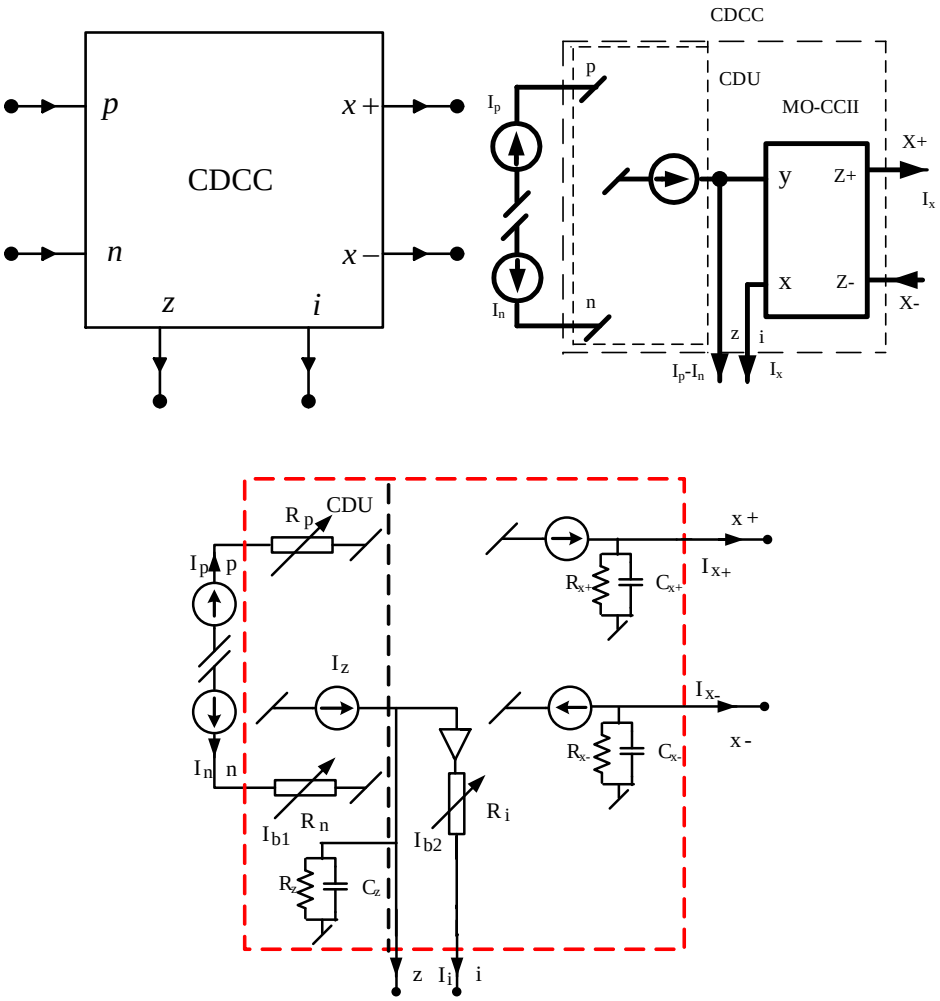


Fig.1.5.1 (a) Circuit symbol of CDCC (b) Behavioural model [21] (c) Modified behavioural model considering parasitics

The port relationship of the CDCC can be described by equation (1.5.1)

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_i \end{bmatrix} \tag{1.5.1}$$

1.5.1 CMOS implementation of the CDCC

From the behavioural model of the CDCC shown in Fig.1.5.1 it may be noted that the CMOS implementation of this block will require (i) a current differencing unit and (ii) a multiple

output current conveyor. Both the units can be realized using translinear voltage buffer(s) and current mirrors/ cross coupled current mirrors.

Translinear Voltage Buffer: A translinear voltage buffer is shown below in Fig. 1.5.1.1. Fig.1.5.1.1 shows the voltage buffer based on translinear loop formed by transistors. We now present an analysis of this circuit [51]. KVL in the loop comprising $M_1 - M_4$ gives:

$$V_{xy} = V_{GS1} - V_{GS2} = V_{GS3} - V_{GS4} \qquad (1.5.1.1a)$$

where V_{GSi} (i = 1,2,3,4) represent gate to source voltage of transistor M_i. KCL at node x gives (as $I_2 = I_{D2} = I_{S2}$ and $I_4 = I_{D4} = I_{S4}$)

$$i_x = I_4 - I_2 \qquad (1.5.1.1b)$$

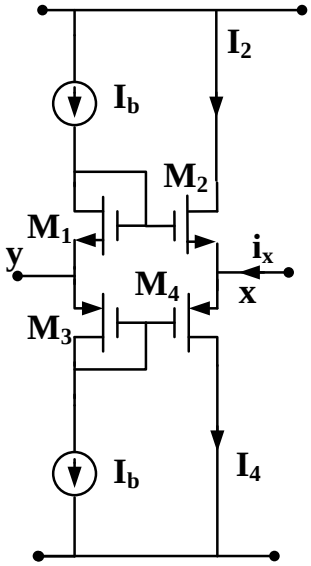


Fig.1.5.1.1 Translinear Voltage buffer

Assuming saturation region operating region of all the transistors, (1.5.1.1a) can be written as

$$V_{xy} \cong \sqrt{\frac{I_b}{\frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}}} - \sqrt{\frac{I_2}{\frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}}} \qquad (1.5.1.2a)$$

$$V_{xy} \cong \sqrt{\frac{I_4}{\frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}}} - \sqrt{\frac{I_b}{\frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}}} \qquad (1.5.1.2b)$$

=where I_b, I_2 and I_4 represent bias current and drain currents of transistor M_2 and M_4 respectively.

Therefore, from (1.5.1.2a) and (1.5.1.2b)

$$i_x = V_{xy}^2 \frac{C_{ox}}{2}\left(\frac{\mu_p W_p}{L_p} - \frac{\mu_n W_n}{L_n}\right) + V_{xy}\sqrt{2I_b C_{ox}}\left(\sqrt{\frac{\mu_p W_p}{L_p}} + \sqrt{\frac{\mu_n W_n}{L_n}}\right) \quad (1.5.1.3)$$

If we select the aspect ratios of the MOSFETs as per the following equation

$$\frac{\mu_p W_p}{L_p} \cong \frac{\mu_n W_n}{L_n} \quad (1.5.1.4)$$

then the equation 1.5.1.3 can be expressed as

$$V_x \cong V_y + \frac{i_x}{\sqrt{2I_b C_{ox}}\left(\sqrt{\frac{\mu_p W_p}{L_p}} + \sqrt{\frac{\mu_n W_n}{L_n}}\right)} \quad (1.5.1.5)$$

$$V_x \cong V_y + i_x R_x \quad (1.5.1.6)$$

where R_x is the output resistance of the voltage buffer as shown in Fig. 1.5.1.2.

$$R_x \cong \frac{1}{\sqrt{2I_b C_{ox}}\left(\sqrt{\frac{\mu_p W_p}{L_p}} + \sqrt{\frac{\mu_n W_n}{L_n}}\right)} \quad (1.5.1.7)$$

If $i_x \leq\leq \sqrt{2I_b}$ then

$$V_x \cong V_y \quad (1.5.1.8)$$

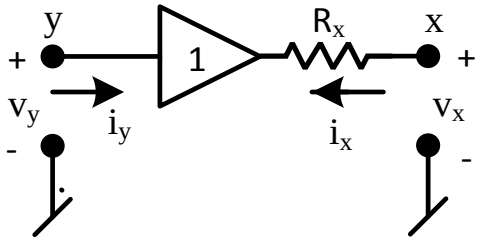
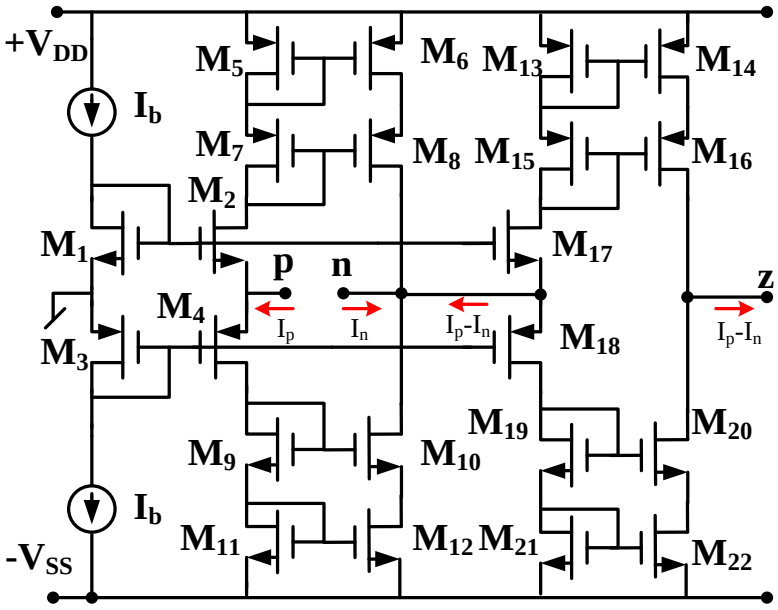


Fig.1.5.1.2 Equivalent circuit of translinear voltage buffer

Current Differencing Unit: The current differencing unit is shown in Fig.1.5.1.3.



$$V_p = V_n = 0; I_z = I_p - I_n$$

Fig. 1.5.1.3 Current differencing unit (CDU)

It uses two translinear voltage buffers formed by (M_1, M_2, M_3, M_4) and (M_1,M_3,M_{17}, M_{18}). The input terminals of both the buffers (junction of S1 and S3) is connected to ground resulting in a virtual ground at the p and n terminal of the CDU. Further, the CDU uses four cascode current mirrors formed by transistors (M_5-M_8), (M_9 – M_{12}), (M_{13} – M_{16}) and (M_{19}-M_{23}). We have used cascode configuration of current mirrors to have a higher value of output resistance of the CDU. A routine analysis of the circuit, assuming no channel length modulation in all the MOSFETs, by writing KCL at p, n and z nodes gives

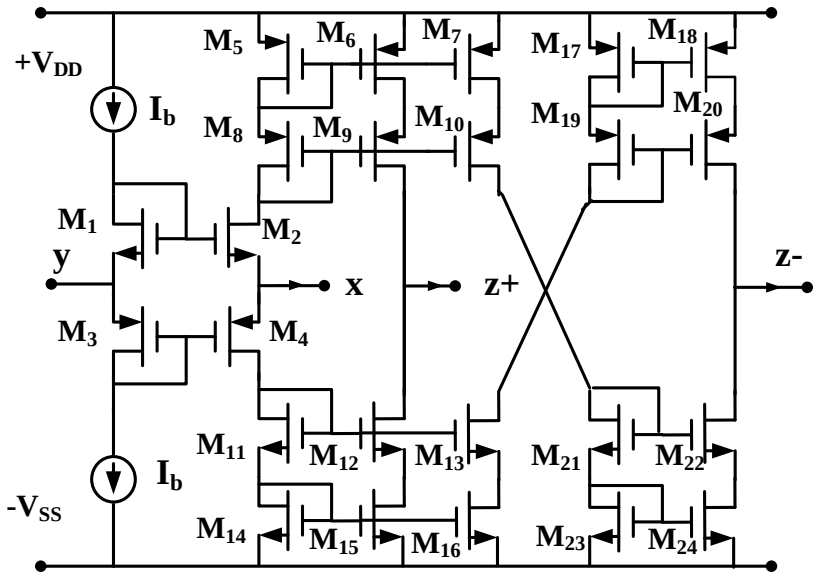
$$i_p = I_4 - I_2 \qquad (1.5.1.9)$$

Multiple output Current Conveyor: A multiple output current conveyor can be realized by a voltage buffer, and current mirrors as shown below in Fig. 1.5.1.4 The x terminal of the current conveyor is available at the output of the voltage buffer (junction of S2 and S4), y terminal at the input of the voltage buffer (junction of S1 and S3) while the positive output terminal and

the negative output terminals are available at the junction of (drain of M_{10} and M_{12}) and (drain of M_{20} and M_{22}) respectively. For ix<<I_b as discussed above, the voltage at x terminal tracks the voltage at the z terminal with a very small error. The current flowing into x terminal is replicated at z_+ through cascode mirrors formed by transistors M_5, M_6, M_8, M_9 and M_{11}, M_{12}, M_{14}, M_{15}. The inverted current at z- terminal is transferred through cross coupled current mirror formed by transistors $M_{17} - M_{20}$ and $M_{21} - M_{24}$.

The complete CDCC can thus be implemented by simply interconnecting these constitutive sub-blocks appropriately as specified in the behavioral model shown in Fig. 1.5.1. Fig.1.5.1.5 shows the complete CMOS realization of the CDCC.

In this implementation, the transistors $M_1 - M_{22}$ realize the CDU while the multiple-output current conveyor comprises of the transistors $M_{23} - M_{46}$. The aspect ratios details are given in Table1.5.2.1.



$$I_y = 0; V_x = V_y; I_{z+} = I_x; I_{z-} = -I_x$$

Fig.1.5.1.4 MOCCII

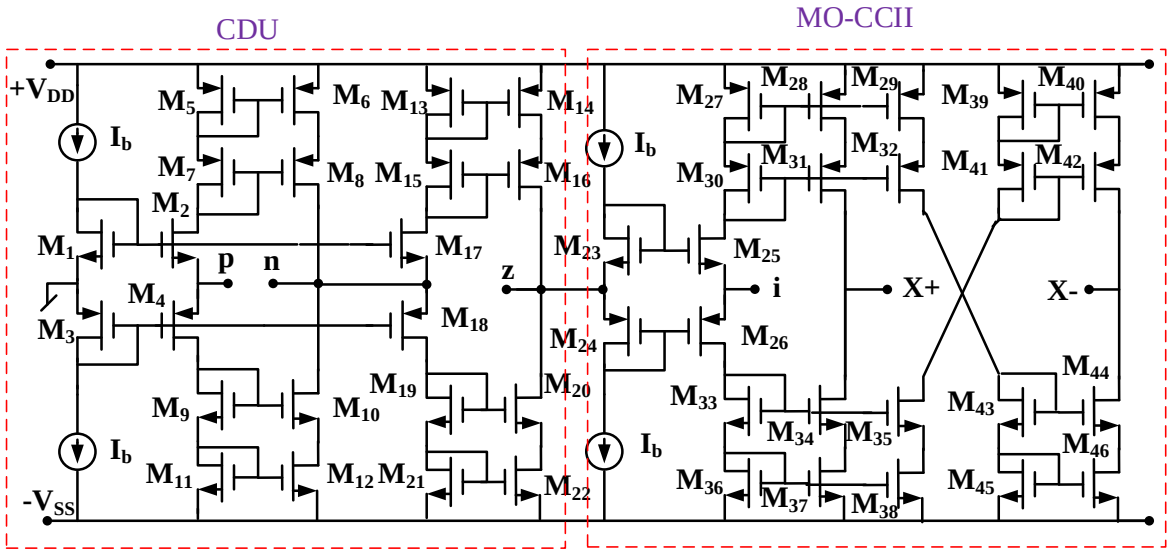


Fig.1.5.1.5 Proposed CMOS implementation of CDCC

1.5.2 Characterization of the CMOS CDCC

The CMOS CDCC was implemented with TSMC CMOS 0.35 µm technology parameters. Bias current and I_b and bias voltages V_{SS} and V_{DD} were taken as 80 µA, -5V and +5V respectively. The aspect ratios of the MOSFETs are given below in Table 1.5.2.1.

Table 1.5.2.1 Aspect ratios of MOSFETs used in CDCC realization

MOSFETs	*W/L*(*µm/µm*)
M_1,M_2,M_{17},M_{23},M_{25}	50/0.5
M_3,M_4,M_{18},M_{24},M_{26}	100/0.5
M_5– M_{16},M_{19}– M_{22},M_{27}– M_{46}	3.33/0.5

.

Voltage and current transfer characteristics: The DC current transfer characteristic are given in Fig. 1.5.2.1 (a) obtained when one input of CDCC is open circuited (i.e. either p or n). The various voltage and current transfer characteristics are shown below in Fig.1.5.2.1.

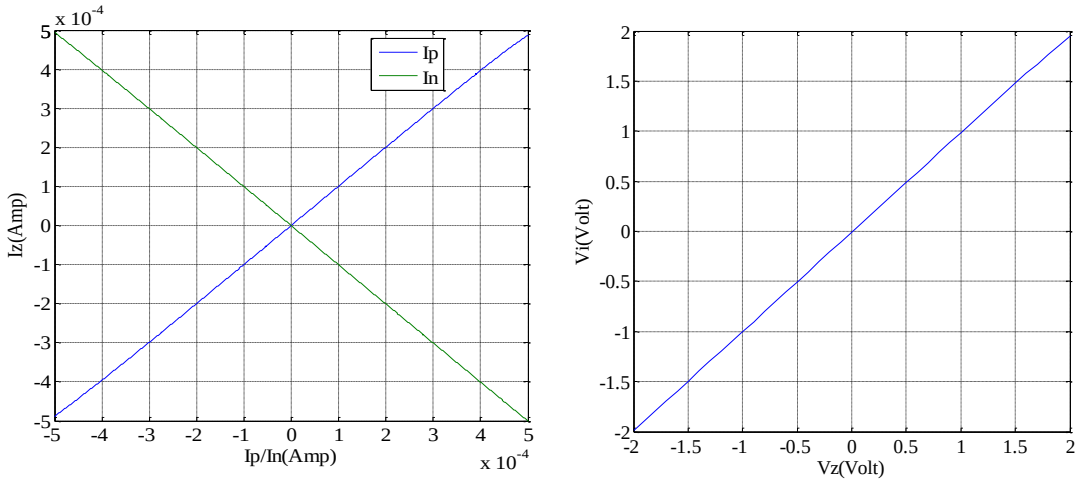


Fig. 1.5.2.1(a) DC Current transfer from I_p and I_n to I_z (b) DC Voltage Transfer from V_z to V_i

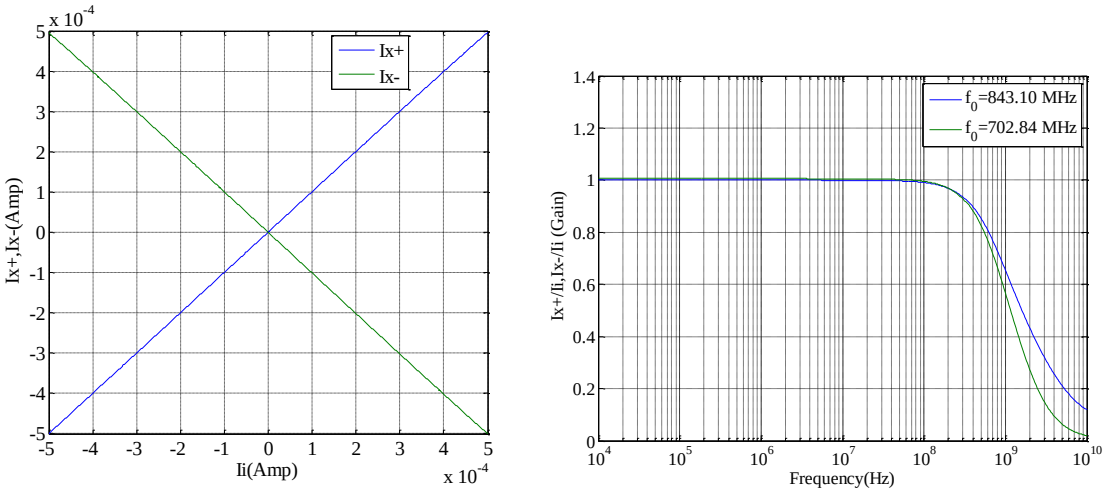


Fig. 1.5.2.1 (c) DC current transfer characteristics from I_i to I_{x+} and I_{x-} (d). Frequency Response of I_{x+}/ I_i and I_{x-}/I_i for proposed CDCC

CDCC as an Amplifier: CDCC was configured as a fully differential current amplifier to verify the workability of this active building block as shown in Fig.1.5.2.2 where the z and i terminals of the CDCC are terminated into impedances Z_1 and Z_2. By straight forward analysis, the output currents are given by

$$i_0 = -i_0^{'} = \frac{Z_1}{Z_2}\left(i_{in} - i_{in}^{'}\right) \qquad (1.5.2.1)$$

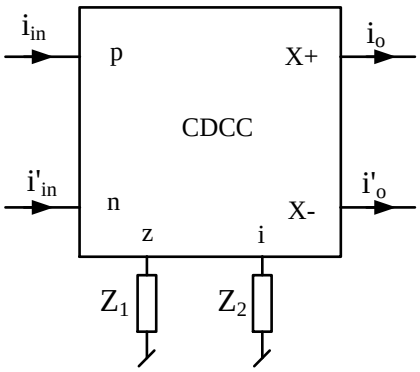


Fig. 1.5.2.2 CDCC as an amplifier

If Z_1 and Z_2 are pure resistances than this will work as a fully differential amplifier with a gain of $\frac{Z_1}{Z_2}$.

In Fig.1.5.2.2 terminal i is terminated with 10KΩ and z terminal is terminated with 10 kΩ, 20 kΩ and 30 kΩ respectively. The frequency response of differential current gain is shown in Fig.1.5.2.3 (a). Transient response for an input current of 5 µA and -5µA when the gain is 1 ($Z_1 = Z_1 = 10K\Omega$) is shown in Fig. 1.5.2.3(b).

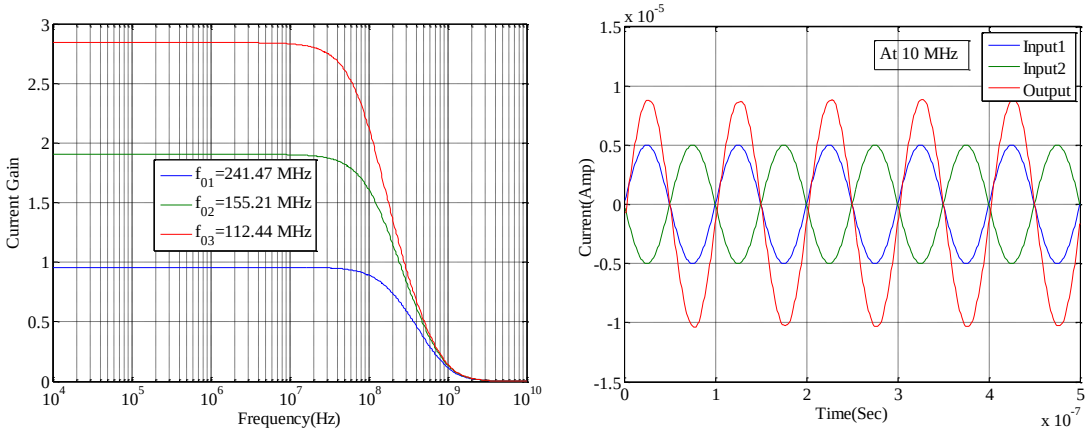


Fig.**1.5.2.3**. (a) Frequency response of fully-differential amplifier (b) Transient Response

1.6 Z-copy current follower current conveyor

The CDCC structure is a very comprehensive structure; if we use only one of the input terminals, then the device can be termed as current follower current conveyor (CFCC) or

current inverter current follower (CICC) [21]. CFCC thus turns out to be a five-port active building block whose symbolic notation is shown in Fig. 1.6.1

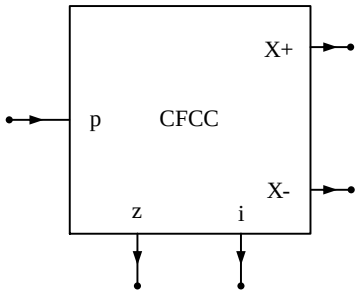


Fig.1.6.1 Symbolic notation of CFCC

The current at the z terminal is an inverted copy of the input current at 'p' terminal. The terminal 'i' tracks the potential at the terminal z. Two complementary currents at the output terminals are available which are copies of the current at the 'i' terminal. To provide addition functionality to the CFCC a copy of the current at the 'z' terminal may also be provided resulting in the Z-copy CFCC. The symbolic notation and behavioral model of ZC-CFCC is shown in Fig.1.6.2.

Mathematically, a ZC-CFCC can be characterized by the following matrix equation:

$$\begin{bmatrix} V_p \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \\ I_{zc} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ V_z \\ I_i \\ V_{x+} \\ V_{x-} \\ V_{zc} \end{bmatrix} \tag{1.6.1}$$

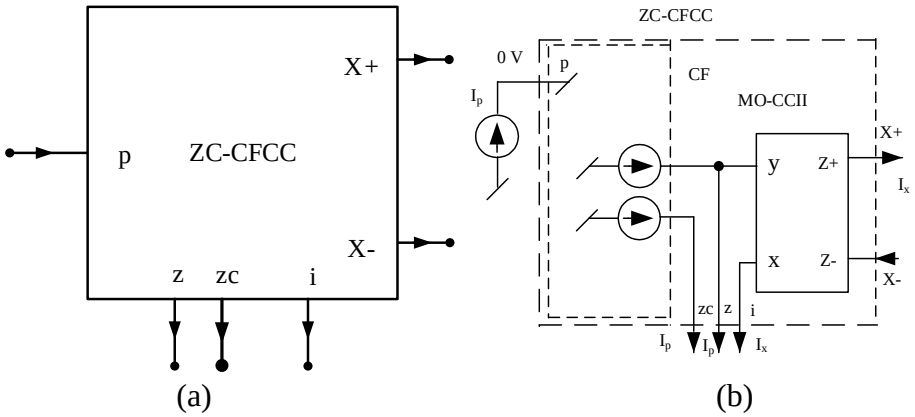


Fig.1.6.2 Symbolic notation of (a) ZC-CFCC and (b) behavioral model [21]

1.6.1 CMOS implementation of Z-copy current follower current conveyor

Using the behavioral model of the Z-copy CFCC, we have developed its CMOS implementation by appropriately interconnecting the basic cells discussed in section 1.6.1. The complete CMOS realization of the ZC-CFCC is shown in Fig.1.6.1.1. In this realization, the transistors $M_1 - M_{24}$ realize the Current follower (CF) and an additional copy of Current (ZC-CF) while the multiple-output current conveyor (MO-CII) comprises of the transistors $M_{25} - M_{48}$.

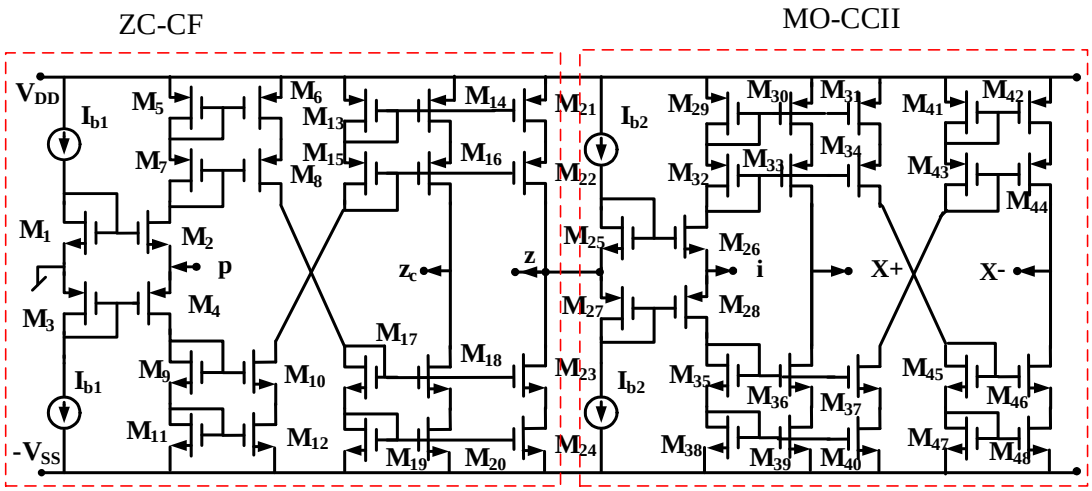


Fig.1.6.1.1 Proposed CMOS implementation of ZC-CFCC

1.6.2 Characterization of the ZC-CFCC

The CMOS implementation of the ZC-CFCC shown in Fig. 1.6.1.1 has been used to verify the workability of the ZC-CFCC based circuits developed in this thesis. The circuit was implemented with MOSFETS using 0.18 micron TSMC CMOS technology. The aspect ratios of the MOSFETS employed are given in Table 1.6.2.1 .The values of the DC bias currents and voltages were taken as 40 µA and ± 2.5V respectively.

Table 1.6.2.1 Aspect ratios of MOSFETs used in ZC-CFCC

MOSFETs	W/L (µm/µm)
M_1, M_2, M_{25}, M_{26}	25/0.25
M_3, M_4, M_{27}, M_{28}	50/0.25
M_5 - M_{24}, M_{29} -M_{48}	2.5/0.25

DC and AC transfer characteristics: The DC current transfer characteristic are given in Fig. 1.6.2.1 (a) obtained when current is applied at p terminal of ZC-CFCC and output current is measured at z and zc terminals. The input stage transfers the current with good accuracy. The DC voltage transfer characteristics of V_i against V_z is shown in Fig. 1.6.2.1 (b). The current transfers I_{x+} and I_{x-} with respect to I_i are given in Fig. 1.6.2.1 (c).The AC characteristics of the ZC-CFCC, namely, frequency response I_{x+}/ I_i and I_{x-}/I_i are shown in Fig. 1.6.2.1 (d).

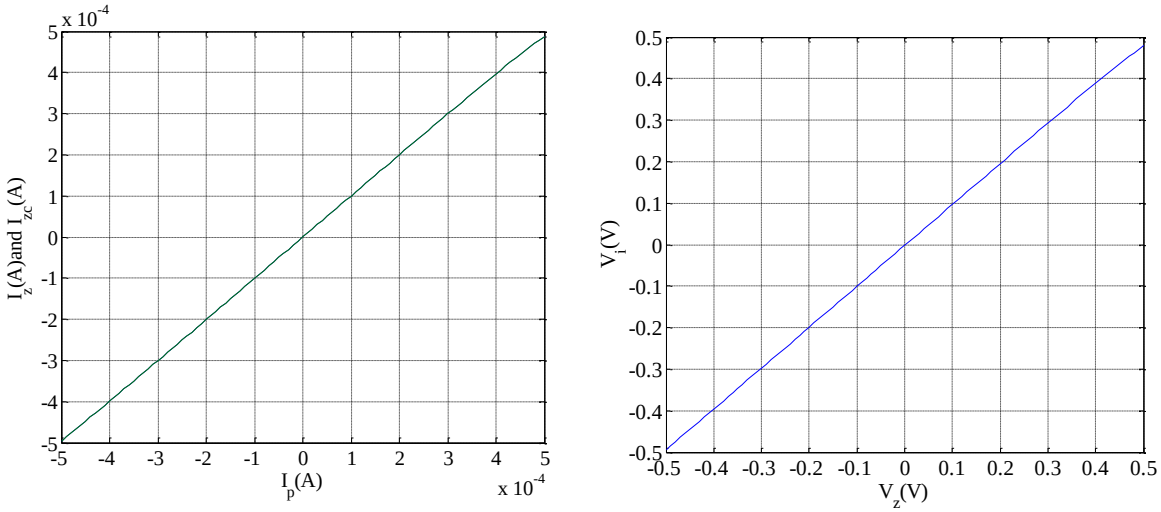


Fig. 1.6.2.1 (a) DC Current transfer from I_p to I_z and I_{zc} (b) DC Voltage Transfer from V_z to V_i

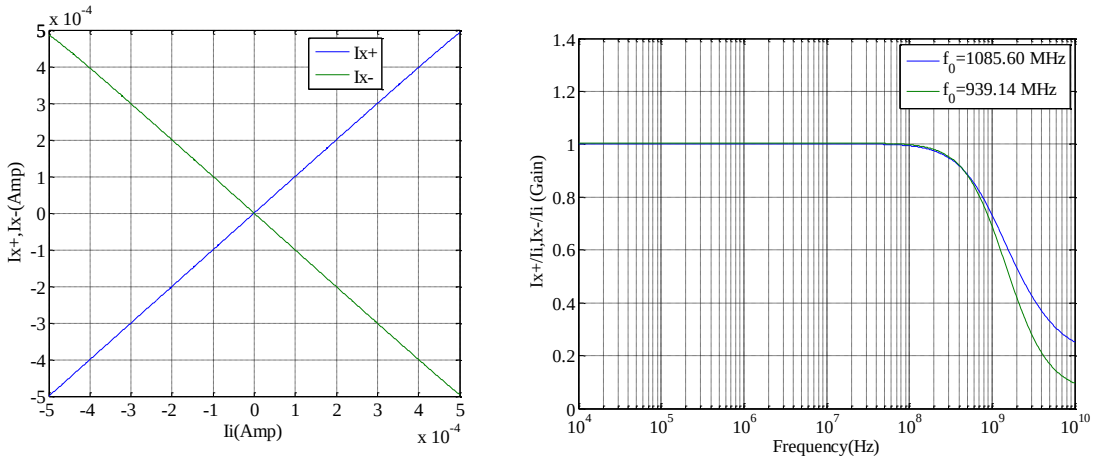


Fig. 1.6.2.1 (c) DC Transfer characteristics between I_i and I_{x+} and I_{x-} (b)Frequency response of I_{x+}/ I_i and I_{x-}/I_i for proposed ZC-CFCC

1.7 Scope of the present work

As pointed out earlier, till the time the work reported in this thesis began (Nov.2011) nothing had appeared in open literature on CDCC hence, it was taken up for detailed investigation for applications in (i) immittance simulation (ii) design of alternative topologies of biquad and higher order filters (in fully differential form) and (iii) harmonic oscillators. The work presented in the thesis has been organized as follows:

Chapter 2 presents realization of fully differential current mode universal biquad filter configurations using CDCC.

Chapter 3 presents a family of single CFCC/ZC-CFCC based grounded lossy and lossless immittance simulators.

Chapter 4 presents electronically tunable grounded and floating inductance simulators using current controlled current follower current conveyor (CCCFCC).

Chapter 5 presents a systematic method for realization of fully differential current-mode higher-order filters with all grounded elements using CDCC.

Chapter 6 presents quadrature oscillator realizations using CFCC and CDCC as ABB.

In **Chapter 7** of the thesis, a summary of the work presented in this thesis and some suggestions for further work on the ideas explored in this thesis are given.

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Chapter 2

A Novel Fully Differential Current Mode Universal Filter

Universal filters with different tunability properties employing CDCCs and all grounded passive elements have been presented

2.1 Introduction

Fully-differential filters offer many advantages compared to their single-ended counterparts in terms of higher rejection capabilities to clock-feed through, charge injection errors and power supply noise. These filter structures have inherently large dynamic range and reduced harmonic distortion [1]. Because of these attributes fully-differential filters have started receiving greater attention from the analog circuit designers in mixed mode circuit solutions where both analog as well as digital circuits are integrated on the same chip. Many active building blocks have been used for designing fully-differential biquad filters in current mode during the past few decades. Before we present the proposed work, it is worthwhile to present the important works done on the realization of fully-differential current-mode biquad filters presented so far.

In [2] modified multiple output differential difference current conveyors have been used to design second order fully-differential band pass (BP) and low pass (LP) filters in which eight grounded passive elements (4R-4C) are used. In [3] a CMOS fully balanced four terminal floating nullor has been used to design fully-differential current mode universal filter in which three active elements (FBFTFNs) and ten passive components (all floating) are used. In [4] differential-input balanced-output current operational amplifiers have been used to realize current mode LP and BP filters with as many as fourteen passive components (10R-4C), in which all the passive components are floating except the output current resistor. A fully-differential current-mode universal filter has been presented in [5] which is based on the nullor concept and uses six passive elements (2R-4C) and six current conveyors. The filter does not have independent tunability of all parameters. A novel fully-differential current- mode universal filter has been presented in [6] which uses three fully-differential current followers (FD-CF), four floating resistors and two floating capacitors. In [7] a fully-differential current-mode universal filter is presented which uses one fully-differential current follower (FD-CF), two multi- output operational transconductance amplifiers (MOTA) and two floating

capacitors. The pole frequency of the band pass filter can be tuned by two MOTA elements. In [8] two fully-differential adjustable band pass filters have been proposed. The circuits use multiple current followers and digitally adjustable current amplifiers in which six passive elements (4R-2C) and five to seven active elements have been used. The circuit 'Q' can be adjusted by adjusting the gain 'A' of the amplifier. In [9], a novel topology for a fully-differential log- domain second order low-pass filter is presented. The structure was implemented using differential input–differential output logarithmic and exponential cells and four grounded capacitors. The biquad permits an orthogonal tuning of its main parameters viz. low-frequency gain, cut-off frequency and quality factor. This can be done continuously by simply changing DC bias currents. A new fully-differential filter structure of the second-order current-mode universal filter is described in [10]. Presented filter is also proposed in a single-ended (S-E) form in order to compare behaviour of single-ended and fully-differential structures. Signal-flow graphs method is used to design both the filters. Two MOTAs, one digitally adjustable current amplifier (DACA), one fully-differential current follower (FD-CF) and two floating capacitors are used in the proposed fully-differential filters. The pole frequency and quality factor of the filter can be tuned independent of each other.

From the literature review it was observed that no fully- differential current-mode biquads using CDCC existed till the time this work started (November 2011), which permit independent tuning of all the parameters of the biquad while employing only two grounded capacitors and all grounded resistances[2].

We now present a family of fully-differential current-mode universal biquad filter which use current differencing current conveyor (CDCC) [11] as the active building block.

[2] Although a minimal FDCMUF which requires only two resistors and two grounded capacitors had been investigated earlier [12], the circuit therein, however, did not have any independent tunability.

2.2 CDCC-based fully-differential current-mode universal filter with independently tunable gain, pole frequency and bandwidth[3]

The CDCC is a six-terminal device whose symbolic notation is given below in Fig.2.2.1 and its port relations are given in equation (2.2.1). This active building block is especially suited for fully-differential current-mode signal processing as it has differential input terminals as well as fully balanced output terminals.

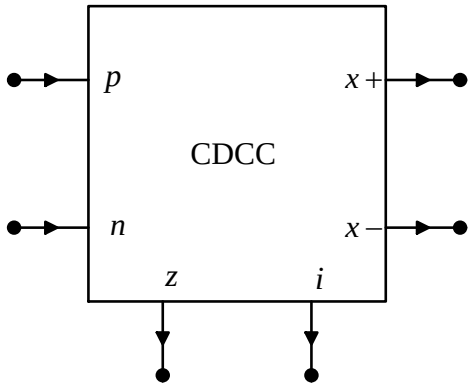


Fig.2.2.1 Symbolic notation of CDCC

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_i \end{bmatrix} \tag{2.2.1}$$

The proposed filters are based on the realization of the block diagram representation of a two integrator loop topology shown in Fig.2.2.2

[3] The material in this section is an expanded form of some preliminary ideas presented in: A.K. Singh and P. Kumar, 'A novel fully differential current mode universal filter', In *Circuits and Systems (MWSCAS), 2014 IEEE 57th International Midwest Symposium on* pp. 579-582.

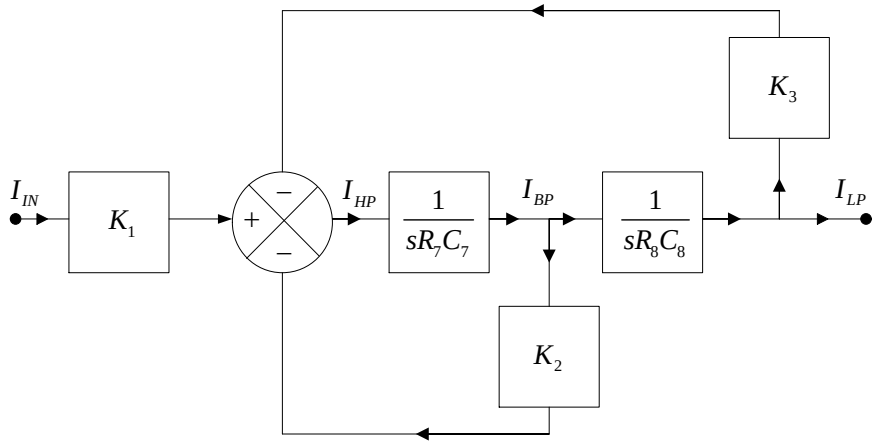


Fig.2.2.2 Block diagram representation of the single ended two-integrator in a loop structure

With fully-differential integrators, fully-differential constant multipliers and fully- differential algebraic summers implemented with CDCC, the fully-differential current-mode universal filter is shown below in Fig.2.2.3.

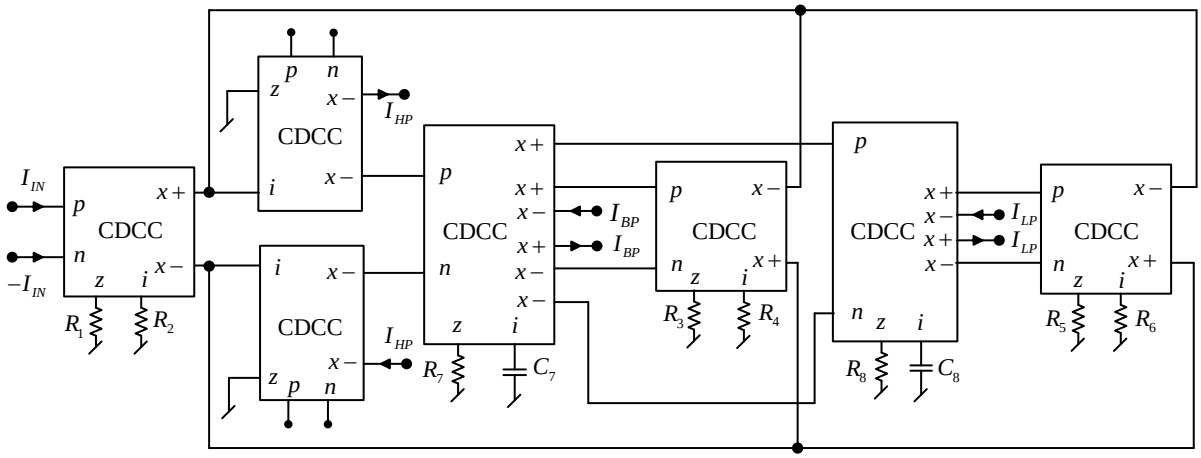


Fig.2.2.3 Fully-differential current mode universal filter employing seven CDCC with independently tunable gain, bandwidth and pole frequency

It may be mentioned here that the summing block used for the filter may also be implemented with a simple fully-differential current follower which may be implemented with a simpler structure but our aim here is to present a fully-differential structure of the current-mode universal filter which uses only one type of active building block.

A routine analysis of the circuit using the terminal equations of the CDCC gives the following current transfer functions

$$\frac{I_{HP}}{I_{IN}} = H_{HP}\frac{s^2}{\Delta} \qquad (2.2.2a)$$

$$\frac{I_{BP}}{I_{IN}} = H_{BP}\frac{2sK_2}{R_7C_7\Delta} \qquad (2.2.2b)$$

$$\frac{I_{LP}}{I_{IN}} = H_{LP}\frac{4K_3}{R_7R_8C_7C_8\Delta} \qquad (2.2.2c)$$

$$where\ \Delta = s^2 + 2s\frac{K_2}{R_7C_7} + 4\frac{K_3}{R_7R_8C_7C_8};$$

$$K_1 = 2\frac{R_1}{R_2}; K_2 = 2\frac{R_3}{R_4}; K_3 = 2\frac{R_5}{R_6};$$

$$H_{HP} = K_1; H_{BP} = \frac{K_1}{K_2}\ and\ H_{LP} = \frac{K_1}{K_3}$$

The highpass (HP) and lowpass (LP) outputs can be combined to get the band elimination (BE) response (for K_3 =1) and the high pass, complementary bandpass (BP) and lowpass responses (for K_2 = K_3 =1) can be combined to get the all pass (AP) response. From the transfer functions given above the various parameters of the biquad filter are found to be

$$H_{HP} = K_1 = 2\frac{R_1}{R_2}; H_{BP} = \frac{K_1}{K_2} = \frac{R_1R_4}{R_2R_3}\ and\ H_{LP} = \frac{K_1}{K_3} = \frac{R_1R_6}{R_2R_5} \qquad (2.2.3a)$$

$$f_0 = \frac{1}{\pi}\sqrt{\frac{K_3}{R_7R_8C_7C_8}} \qquad (2.2.3b)$$

$$\nabla f = \frac{K_2}{\pi R_7C_7} \qquad (2.2.3c)$$

From the above expressions it may be noted that the pole frequency f_0 for the filters can be tuned by tuning the coefficient K_3 without changing either the bandwidth ∇f or the relevant gains for the highpass, bandpass and lowpass responses. Similarly the bandwidth ∇f can be

tuned by varying K_2 without changing either the pole frequency or the relevant gains. Finally the relevant gains can also be tuned by appropriately changing the values of K_1, K_2 and K_3.

2.3 Non-ideality analysis

From the structure of the current mode fully-differential universal filter given in Fig. 2.2.3 it is interesting to note that the parasitic immittances associated with z and I terminals of various CDCCs can very easily be compensated in the terminating impedances at these terminals. However, the other parasitic immittances will degrade the performance of the realized filters. In the following we present an analysis of the circuit given in Fig. 2.2.3 which takes into account the various frequency independent tracking errors associated with different voltage and current transfers.

Under non-zero tracking error in voltage and current, let α_{kp} and α_{kn} represent the current tracking coefficients between the p and n terminals of the CDCC to its z terminal and α_{ki} represent the current tracking error between the terminal i and x of the kth CDCC (k=1-7). Similarly, β_k represents the voltage tracking coefficient between the terminal z and i of the kth CDCC. These coefficients will have a nominal value which is very close to unity. The modified voltage and current transfers can thus be represented by

$$I_{kz} = \alpha_{kp} I_p - \alpha_{kn} I_n \qquad (2.3.1a)$$

$$V_{ki} = \beta_k V_{kz} \qquad (2.3.1b)$$

$$I_{kx} = \alpha_{ki} I_{ki} \qquad (2.3.1c)$$

$$V_p = V_n = 0 \qquad (2.3.1d)$$

The modified transfer functions of the circuit are now found to b

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2 K_1 \alpha_{2i} \beta_1 \alpha_{1i} \left(\alpha_{1p} + \alpha_{1n}\right)}{2D(s)} \qquad (2.3.2a)$$

$$\frac{I_{BP}}{I_{IN}} = \frac{sK_1 \alpha_{2i} \beta_1 \alpha_{1i} \left(\alpha_{1p} + \alpha_{1n}\right) \alpha_{4i} \beta_4 \left(\alpha_{4p} + \alpha_{4n}\right)}{2R_7 C_7 D(s)} \qquad (2.3.2b)$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\alpha_{2i} K_1 \beta_1 \alpha_{1i} \left(\alpha_{1p} + \alpha_{1n}\right) \alpha_{4i} \beta_4 \left(\alpha_{4p} + \alpha_{4n}\right) \alpha_{6i} \beta_6 \left(\alpha_{6p} + \alpha_{6n}\right)}{2R_7 R_8 C_7 C_8 D(s)} \qquad (2.3.2c)$$

$$D(s) = s^2 + s \frac{K_2 \alpha_{5i} \beta_5 \left(\alpha_{5p} + \alpha_{5n}\right) \alpha_{4i} \beta_4 \left(\alpha_{4p} + \alpha_{4n}\right)}{2R_7 C_7} + \frac{K_3 \alpha_{2i} \beta_7 \alpha_{7i} \left(\alpha_{7p} + \alpha_{7n}\right) \alpha_{6i} \beta_6 \left(\alpha_{6p} + \alpha_{6n}\right) \alpha_{4i} \beta_4 \left(\alpha_{4p} + \alpha_{4n}\right)}{2R_7 R_8 C_7 C_8}$$

and $K_1 = 2\frac{R_1}{R_2}; K_2 = 2\frac{R_3}{R_4}; K_3 = 2\frac{R_5}{R_6}$

The f_0 and ∇f parameters can now be written as follows:

$$f_o = \frac{1}{2\pi} \sqrt{\frac{K_3 \alpha_{2i} \beta_7 \alpha_{7i} \left(\alpha_{7p} + \alpha_{7n}\right) \alpha_{6i} \beta_6 \left(\alpha_{6p} + \alpha_{6n}\right) \alpha_{4i} \beta_4 \left(\alpha_{4p} + \alpha_{4n}\right)}{2R_7 R_8 C_7 C_8}} \qquad (2.3.3a)$$

$$\nabla f = \frac{K_2 \alpha_{5i} \beta_5 \left(\alpha_{5p} + \alpha_{5n}\right) \alpha_{4i} \beta_4 \left(\alpha_{4p} + \alpha_{4n}\right)}{4\pi R_7 C_7} \qquad (2.3.3b)$$

If $\alpha_{kp} = \alpha_{kn} = \alpha_{ki} = \beta_k = 0.98$, then the error in pole frequency is found to be 9.6 percent for a nominal design value of 1.8760 MHz . The active and passive sensitivities are not more than $\pm\frac{1}{2}$ in magnitude and magnitude of $\alpha_{kp}, \alpha_{kn}, \beta_k$ and $\alpha_{ki} < 1$. Another contributing factor in the error in the pole frequency and bandwidth are the uncompensated parasitic capacitances and resistances at the terminal ports. These errors have been measured in simulation and are given in Table 2.4.2.

2.4 Simulation results

The CMOS implementation of CDCC presented in Fig.1.6.1.3, redrawn here has been used to verify the workability of the circuits presented. The aspect ratios details are given in Table 2.4.1. The values of DC bias currents and voltages are 80 μA and ± 5 V respectively.

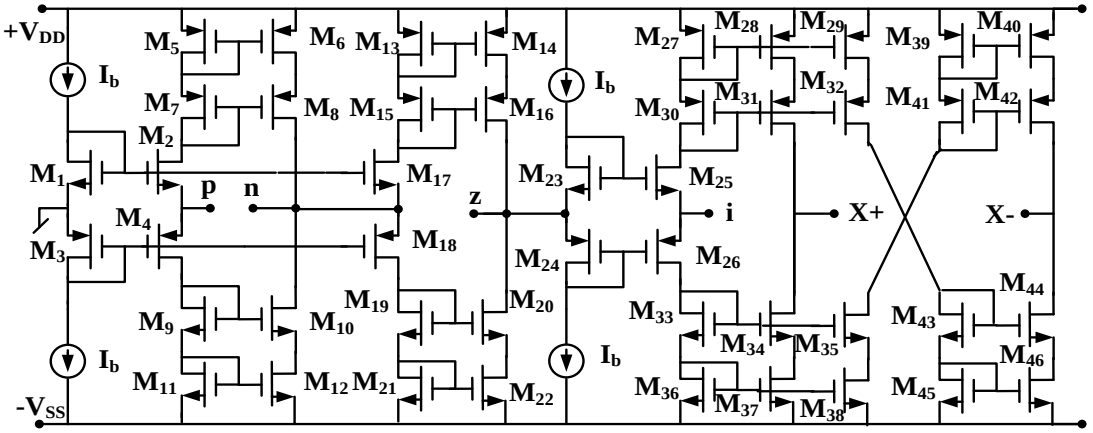


Fig.2.4.1 CMOS implementation of CDCC

Table 2.4.1 Aspect ratios of MOSFETs used in CDCC realization.

MOSFETs	$W/L(\mu m/\mu m)$
M_1,M_2,M_{17},M_{23},M_{25}	50/0.5
M_3,M_4,M_{18},M_{24},M_{26}	100/0.5
M_5– M_{16},M_{19}– M_{22},M_{27}– M_{46}	3.33/0.5

The fully-differential current-mode universal filter was designed to operate at the nominal values of f_0, ∇f and H as 1.8759 MHz, 2.6526 MHz and 1 respectively by selecting R_1= R_3 = R_5=10 kΩ, R_2 = R_4 = R_6 = 20 kΩ, R_7= R_8=10 kΩ , C_7= 12 pF and C_8 =24 pF. Fig. 2.4.2(a) and Fig. 2.4.2(b) show the magnitude and time response of the universal filter with these nominal values respectively.

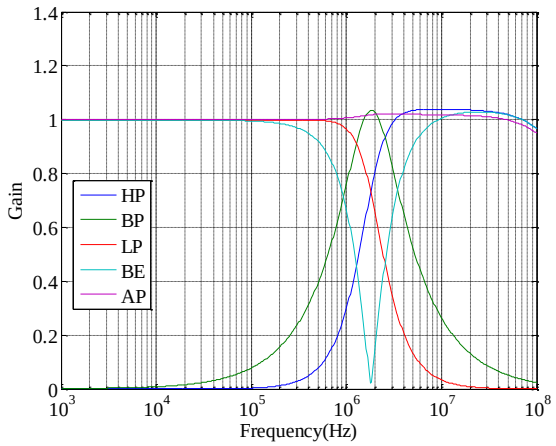


Fig.2.4.2 (a) Magnitude response of HP, BP, LP, AP & BE filters for a pole frequency of 1.8759 MHz.

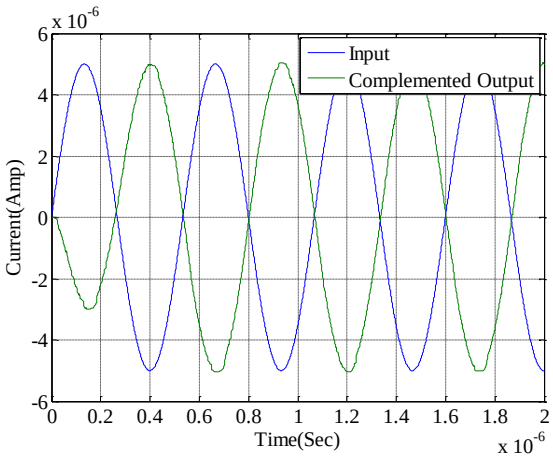


Fig.2.4.2 (b) Time response of the BP filter for an input current of $5\mu A$ at 1.8759 MHz

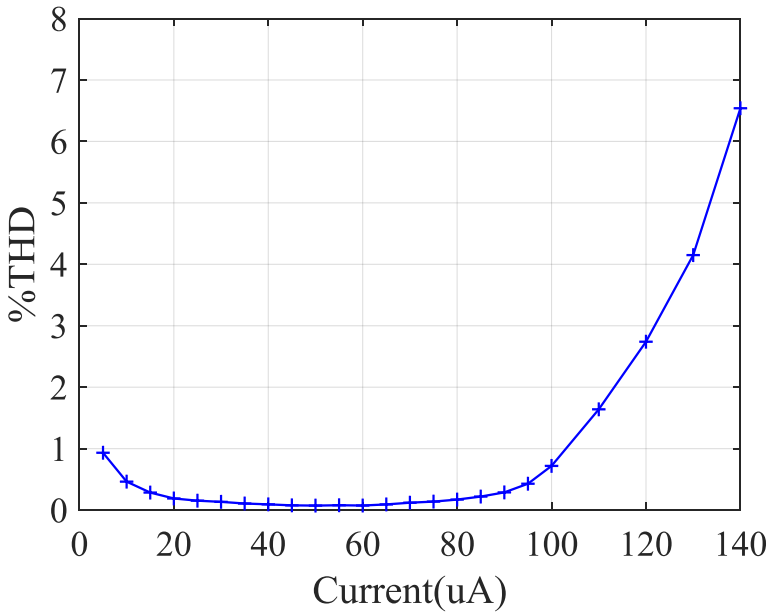


Fig.2.4.2 (c) Variation of THD with applied input Current for Fully- differential BP filter at 1.8759 MHz

To test for various tunability, the following simulations were carried out.

Gain tunability: To change the pole frequency gain of the bandpass filter without changing its bandwidth (2.6526 MHz) and the pole frequency (1.8759 MHz), the value of $K_1(=\frac{2R_1}{R_2})$ was varied from 1 to 5 while keeping the values of K_2 and K_3 as 1. The values of R_1=10 kΩ,

20 kΩ and 50 kΩ with R_2 = 20 kΩ results in K_1 becoming equal to 1, 2 and 5. Fig.2.4.3 (a) shows the tunability of gain.

Pole frequency tunability: To change the pole frequency without changing the gain (1) and bandwidth (2.6526 MHz) the value of $K_3(=\frac{2R_5}{R_6})$ was changed while keeping K_1 and K_2 as 1. The values of R_5=40 kΩ, 10 kΩ and 2.5 kΩ with R_6 = 80 kΩ results in K_3 be coming equal to 1, 0.25 and 0.0625. This results in pole frequency assuming the values 1.8759 MHz, 0.9380 MHz and 0.4690 MHz respectively. Fig.2.4.3 (b) shows the tunability of pole frequency.

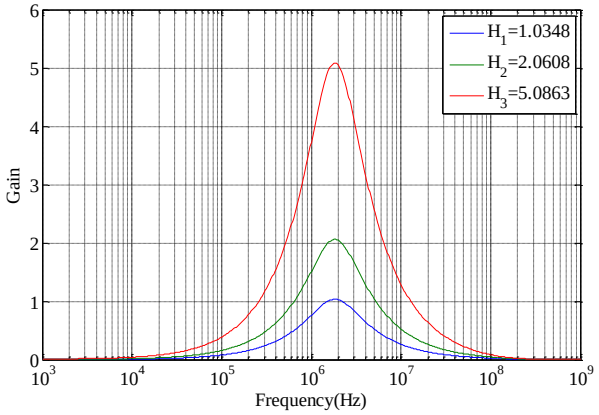


Fig.2.4.3 (a) Magnitude response showing showing tunability of pole frequency f_0.

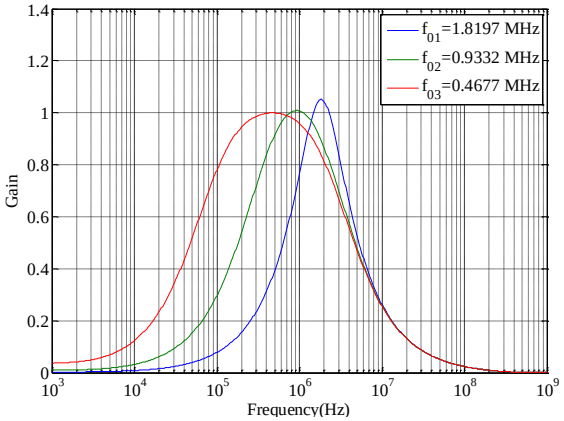


Fig.2.4.3 (b) Magnitude response tunability of gain H.

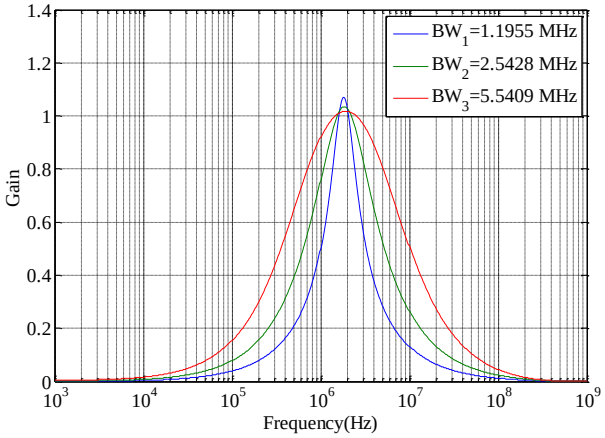


Fig. 2.4.3(c) Magnitude response showing tenability of bandwidth ∇f .

Bandwidth tunability: To change the bandwidth without changing the gain (1) and pole frequency (1.8759 MHz) the value of $K_2(=\frac{2R_3}{R_4})$ and $K_1(=\frac{2R_1}{R_2})$ were changed (since a change in bandwidth requires changing the value of $K_2(=\frac{2R_3}{R_4})$, which will affect the gain $H_{BP}=\frac{K_1}{K_2}=\frac{R_1R_4}{R_2R_3}$ of bandpass filter) while keeping K_3 as 1. The values of $R_1 = R_3$ has been selected as 20 kΩ, 10 kΩ and 5 kΩ respectively while $R_2 = R_4$ remained at 20 kΩ .This results in K_2 becoming equal to 2, 1, and 0.5 respectively thus changing the bandwidth to 5.3052 MHz, 2.6526 MHz and 1.3263 MHz respectively. Fig.2.4.3 (c) shows the tunability of bandwidth.

The detailed results of simulations are summarized in Table 2.4.2.

Table 2.4.2 Summary of calculated and simulated results.

Tuneability	Component Values		Nominal Values(Calculated)			Simulated Values		
			H	f_0 (MHz)	∇f (MHz)	H	f_0 (MHz)	∇f (MHz)
Gain(H)- Fig.2.4.3a	$R_2=R_4=R_6=20k\Omega;$ $R_3=R_5=R_7=R_8=10k\Omega;$ $C_7=12pF, C_8=24pF;$	$R_1=10k\Omega$	1	1.8759	2.6526	1.0348	1.8197	2.5428
		$R_1=20k\Omega$	2	1.8759	2.6526	2.0608	1.8197	2.5426
		$R_1=50k\Omega$	5	1.8759	2.6526	5.0863	1.8197	2.5411
Pole Frequency (f_0) Fig.2.4.3b	$R_2=R_4=20k\Omega, R_6=80k\Omega;$ $R_1=R_3=R_7=R_8=10k\Omega;$ $C_7=12pF, C_8=24pF;$	$R_5=40k\Omega$	1	1.8760	2.6526	1.0428	1.8197	2.5002
		$R_5=10k\Omega$	1	0.9380	2.6526	1.0068	0.9332	2.6116
		$R_5=2.5k\Omega$	1	0.4690	2.6526	0.9992	0.4677	2.6359
Bandwidth (∇f) Fig.2.4.3c	$R_2=R_4=R_6=20k\Omega;$ $R_5=R_7=R_8=10k\Omega;$ $C_7=12pF, C_8=24pF;$	$R_1=R_3=20k\Omega$	1	1.8759	5.3052	1.0179	1.8197	5.5409
		$R_1=R_3=10k\Omega$	1	1.8759	2.6526	1.0384	1.8197	2.5428
		$R_1=R_3=5k\Omega$	1	1.8759	1.3263	1.0708	1.8197	1.1955

Table 2.4.2 Summary of calculated and simulated results.

% Error in H	% Error in f_0	% Error in ∇f
3.48	3.00	4.44
3.04	0.511	4.14
1.726	0.28	9.86

From the percentage errors computed above it is observed that the degradation in the performance is not appreciable (<10%).

2.5 Fully-differential current-mode filter with limited tunability of parameters

It has been found that if we do not want tunability of all the parameters simultaneously then the number of ABBs and passive components may be reduced. In the following we present these reduced component based circuits.

2.5.1 Fully-differential current-mode universal filter with independent tunability of gain and pole frequency

We now present a circuit of six- CDCC based current-mode universal biquad, which has been derived systematically from the circuit given in Fig.2.2.3 by removing the ABB and passive components corresponding to K_2, resulting in the circuit of Fig.2.5.1 1.

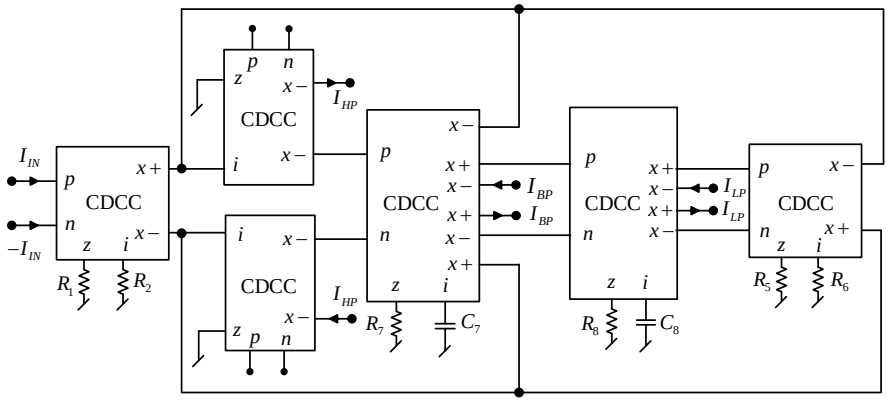


Fig.2.5.1.1 FDCMUF employing six- CDCC both independently tunable gain and pole frequency with fixed bandwidth

A routine analysis of the circuit gives the following transfer function

$$\frac{I_{HP}}{I_{IN}} = H_{HP}\frac{s^2}{\Delta} \qquad (2.5.1.1a)$$

$$\frac{I_{BP}}{I_{IN}} = H_{BP}\frac{2s}{R_7C_7\Delta} \qquad (2.5.1.1b)$$

$$\frac{I_{LP}}{I_{IN}} = H_{LP}\frac{4K_3}{R_7R_8C_7C_8\Delta} \qquad (2.5.1.1c)$$

$$where\ \Delta = s^2 + \frac{2s}{R_7C_7} + 4\frac{K_3}{R_7R_8C_7C_8};$$

$$K_1 = 2\frac{R_1}{R_2}\ and\ K_3 = 2\frac{R_5}{R_6};$$

$$H_{HP} = H_{BP} = K_1\ and\ H_{LP} = \frac{K_1}{K_3}$$

Thus the various parameters of the above biquad filter are found to be

$$H_{HP} = H_{BP} = K_1 = 2\frac{R_1}{R_2}\ and\ H_{LP} = \frac{K_1}{K_3} = \frac{R_1R_6}{R_2R_5} \qquad (2.5.1.2a)$$

$$f_0 = \frac{1}{\pi}\sqrt{\frac{K_3}{R_7R_8C_7C_8}} = \frac{1}{\pi}\sqrt{\frac{2R_5}{R_6R_7R_8C_7C_8}} \qquad (2.5.1.2b)$$

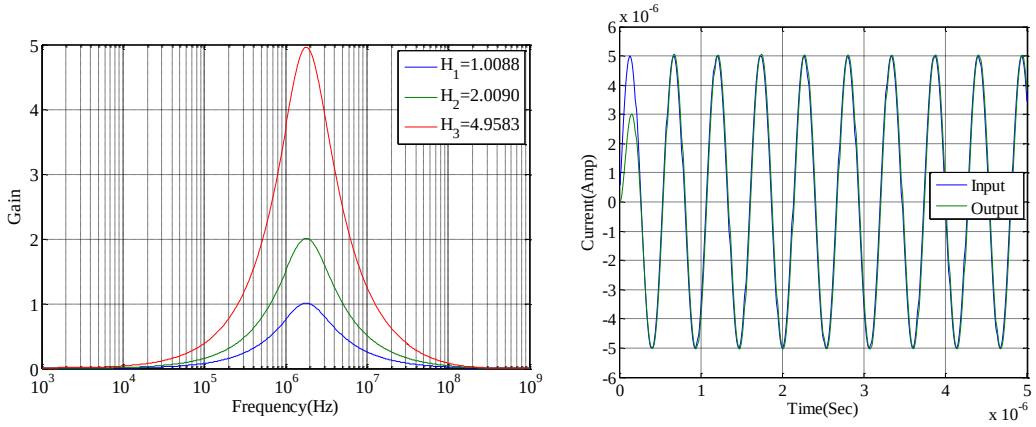
$$\nabla f = \frac{1}{\pi R_7C_7} \qquad (2.5.1.2c)$$

From equation 2.5.1.2 it is observed that we can vary gain and pole frequency of bandpass filter independently while keeping its bandwidth constant.

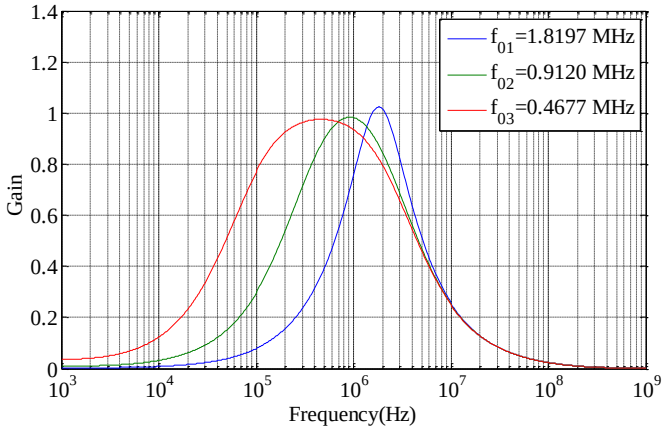
2.5.1.1 Simulation results

Gain tunability: To change the pole frequency gain of the bandpass filter without changing the bandwidth (2.6526 MHz) and the pole frequency (1.8759 MHz), the values of $K_1(=\frac{2R_1}{R_2})$ was varied from 1 to 5 while keeping the values of K_3 =1 . The values of R_1=10 kΩ, 20 kΩ and

50 kΩ with R_2 = 20 kΩ results in K_1 becoming equal to 1, 2 and 5. Fig.2.5.1.2 (a) and (b) show the tunability of gain and time response of filter.



(a) **(b)**



(c)

Fig. 2.5.1.2 **(a)** Magnitude response showing tunability of gain H **(b)** Time response of the Bandpass filter for an input of 5μA at 1.8759 MHz of Fig.2.5.1.1 **(c)** Magnitude response showing tunability of pole frequency f_0. of Fig.2.5.1.1

Pole frequency tunability: To change the pole frequency without changing the gain (1) and bandwidth (2.6526 MHz) the value of $K_3(=\frac{2R_5}{R_6})$ was changed while keeping K_1equal to 1. The values of R_5=40 kΩ, 10 kΩ and 2.5 kΩ with R_6 = 80 kΩ results in K_3 becoming equal to 1, 0.25 and 0.0625 respectively .This results in pole frequency assuming the values equals to 1.8759 MHz, 0.9380 MHz and 0.4690 MHz respectively. Fig.2.5.1.2(c) shows the tunability of pole frequency.

2.5.2 Fully-differential current-mode universal filter with fixed gain, fixed pole frequency and tunable gain

The second six-CDCC based fully-differential current-mode universal filter configuration is shown in Fig.2.5.2.1.This circuit has also been derived from the circuit given in Fig.2.2.3 by removing ABB and passive components corresponding to K_3 .

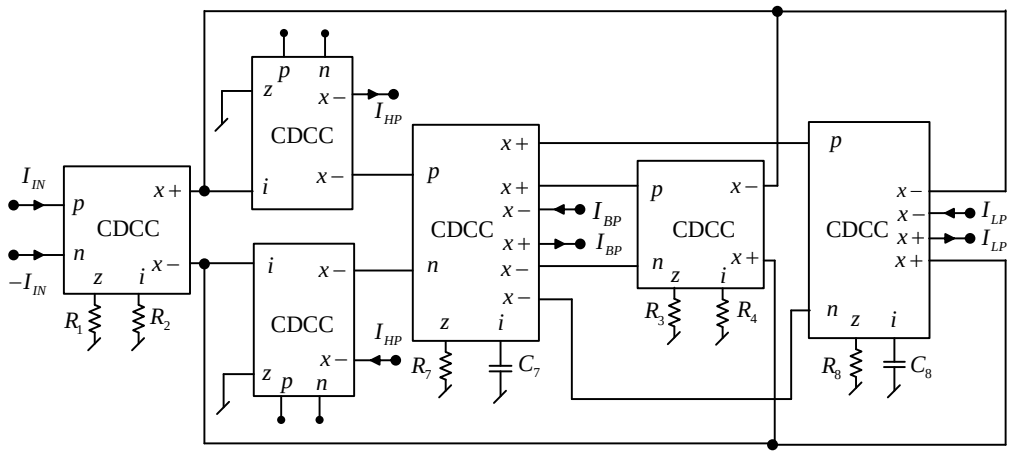


Fig.2.5.2.1 FDCMUF employing six CDCC independently tunable bandwidth for fixed pole frequency and fixed gain

A routine analysis of the circuit gives the following transfer function

$$\frac{I_{HP}}{I_{IN}} = H_{HP}\frac{s^2}{\Delta} \qquad (2.5.2.1a)$$

$$\frac{I_{BP}}{I_{IN}} = H_{BP}\frac{2sK_2}{R_7C_7\Delta} \qquad (2.5.2.1b)$$

$$\frac{I_{LP}}{I_{IN}} = H_{LP}\frac{4}{R_7R_8C_7C_8\Delta} \qquad (2.5.2.1c)$$

$$where\ \Delta = s^2 + 2s\frac{K_2}{R_7C_7} + \frac{4}{R_7R_8C_7C_8};K_1 = 2\frac{R_1}{R_2},K_2 = 2\frac{R_3}{R_4};H_{HP} = H_{LP} = K_1\ and\ H_{BP} = \frac{K_1}{K_2} = \frac{R_1R_4}{R_2R_3}$$

The various parameters of the above biquad filter are found to be

$$H_{LP} = H_{HP} = 2\frac{R_1}{R_2} \; and \; H_{BP} = \frac{R_1 R_4}{R_2 R_3} \qquad (2.5.2.2a)$$

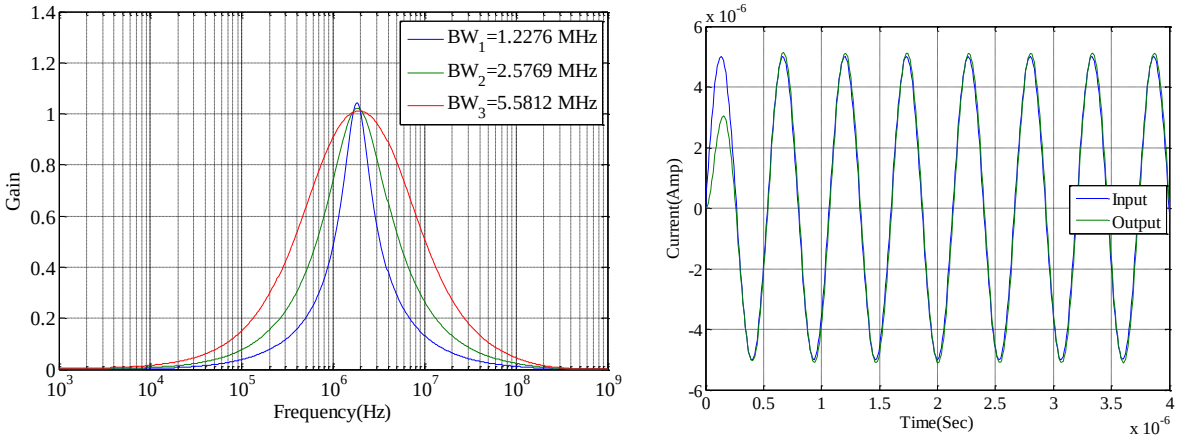
$$f_0 = \frac{1}{\pi}\sqrt{\frac{1}{R_7 R_8 C_7 C_8}} \qquad (2.5.2.2b)$$

$$\nabla f = \frac{K_2}{\pi R_7 C_7} = \frac{2R_3}{\pi R_4 R_7 C_7} \qquad (2.5.2.2c)$$

From equation 2.5.2.2 it is clear that we can vary bandwidth independently while keeping pole frequency and gain of the filter constant.

2.5.2.1 Simulation results

Bandwidth tunability: To change the bandwidth without changing the gain (1) and pole frequency (1.8759 MHz) the value of $K_2(=\frac{2R_3}{R_4})$ and $K_1(=\frac{2R_1}{R_2})$ were varied simultaneously [since a change in bandwidth requires changing the value of $K_2(=\frac{2R_3}{R_4})$, which will affect the gain $H_{BP} = \frac{K_1}{K_2} = \frac{R_1 R_4}{R_2 R_3}$ of bandpass filter]. The values of $R_1 = R_3$ has been selected as 20 kΩ, 10 kΩ and 5 kΩ respectively, while $R_2 = R_4$ remained at 20 kΩ.This results in K_2 becoming equal to 2, 1, and 0.5 respectively thus changing the bandwidth to 5.3052 MHz, 2.6526 MHz and 1.3263 MHz respectively. Fig.2.5.2.2 (a) and (b) show the tunability of bandwidth and time response of bandpass filter.



(a) **(b)**

Fig. 2.5.2.2 **(a)** Magnitude response showing tunability of bandwidth **(b)** Time response of the Bandpass filter for an input of $5\mu A$ at 1.8759 MHz of Fig. 2.5.2.1

2.5.3 Fully-differential current-mode universal filter with fixed pole frequency, fixed bandwidth and tunable gain

We now present a five CDCC-based fully-differential current-mode universal biquad , which has been derived systematically from the circuit given in Fig.2.2.3 by removing ABBs and passive components corresponding to both K_2 and K_3 resulting in the circuit of Fig.2.5.3.1.

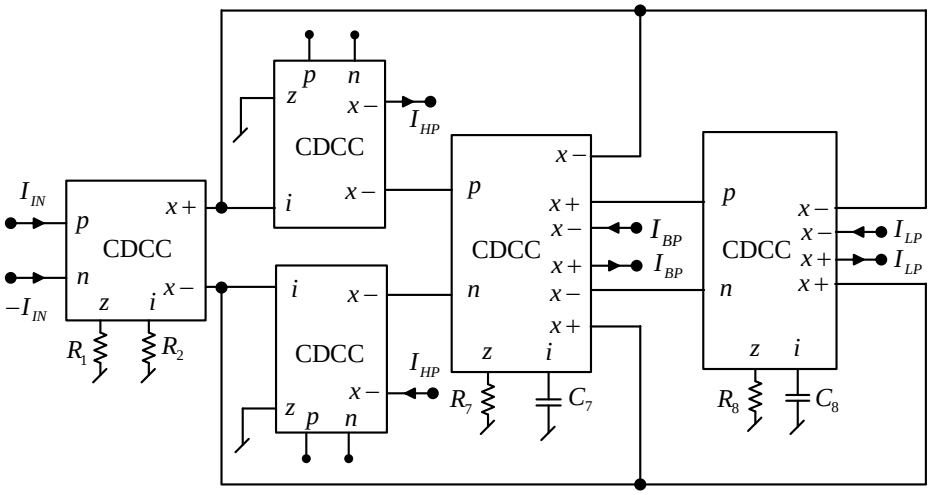


Fig.2.5.3.1 FDCMUF employing five CDCC with fixed bandwidth, fixed pole frequency and independently tunable gain

A routine analysis of the circuit of Fig.2.5.3.1 gives the following current transfer functions

$$\frac{I_{HP}}{I_{IN}} = H_{HP}\frac{s^2}{\Delta} \qquad (2.5.3.1a)$$

$$\frac{I_{BP}}{I_{IN}} = H_{BP}\frac{2s}{R_7C_7\Delta} \qquad (2.5.3.1b)$$

$$\frac{I_{LP}}{I_{IN}} = H_{LP}\frac{4}{R_7R_8C_7C_8\Delta} \qquad (2.5.2.1c)$$

$$where\ \Delta = s^2 + \frac{2s}{R_7C_7} + \frac{4}{R_7R_8C_7C_8}; H_{HP} = H_{LP} = H_{BP} = K_1 = 2\frac{R_1}{R_2}$$

The various parameters of the above biquad filter are found to be

$$H_{LP} = H_{HP} = H_{BP} = 2\frac{R_1}{R_2} \qquad (2.5.3.2a)$$

$$f_0 = \frac{1}{\pi}\sqrt{\frac{1}{R_7R_8C_7C_8}} \qquad (2.5.3.2b)$$

$$\nabla f = \frac{1}{\pi R_7C_7} \qquad (2.5.3.2c)$$

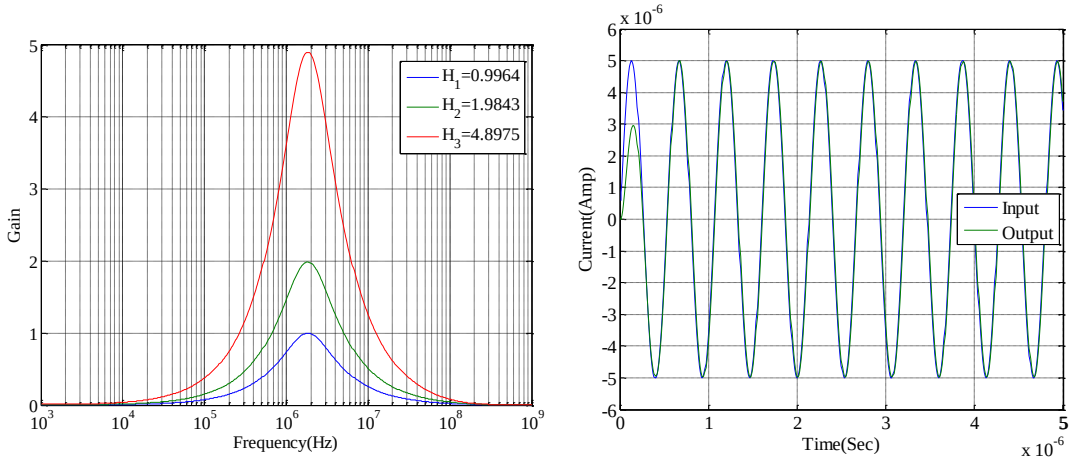
From equation 5.2.3.2 it is clear that we can vary gain of the filter while keeping pole frequency and bandwidth of the filter fixed.

2.5.3.1 Simulation results

Gain tunability: To change the pole frequency gain of the bandpass filter without changing the bandwidth (2.6526 MHz) and the pole frequency (1.8759 MHz), the values of $K_1(=\frac{2R_1}{R_2})$ was varied from 1, 2 and 5 . The values of R_1=10 kΩ, 20 kΩ and 50 kΩ with R_2 =20 kΩ results in K_1 becoming equal to 1, 2 and 5.Fig.2.5.3.2 (a) and (b) show the tunability of gain and time response of the filter.

2.5.4 Fully-differential current-mode universal filter with fixed gain, fixed bandwidth and independently tunable pole frequency.

The second five-CDCC based fully-differential current-mode universal filter configuration is shown in Fig.2.5.4.1.This circuit has also been derived from the circuit given in Fig.2.2.3 by removing ABB and passive components corresponding to both K_1 and K_2 .



(a) **(b)**

Fig. 2.5.3.2 **(a)** Magnitude response showing tunability of gain H **(b)** Time response of the bandpass filter for an input of 5μA at 1.8759 MHz of Fig.2.5.3.1.

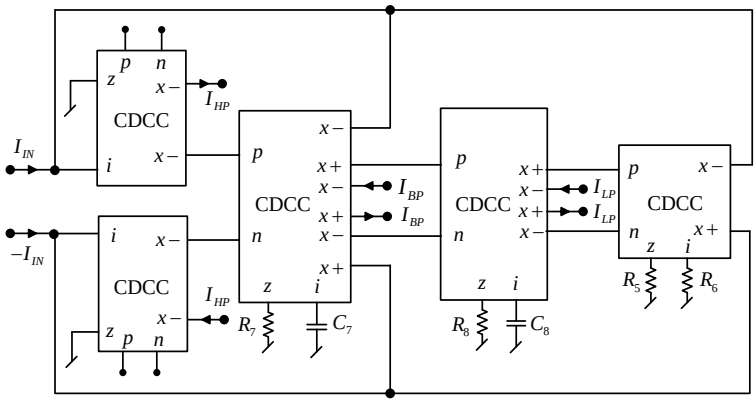


Fig.2.5.4.1 FDCMUF employing five CDCC with fixed bandwidth, fixed gain and independently tunable pole frequency

A routine analysis of the circuit gives the following transfer function

$$\frac{I_{HP}}{I_{IN}} = H_{HP}\frac{s^2}{\Delta} \qquad 2.5.4.1(a)$$

$$\frac{I_{BP}}{I_{IN}} = H_{BP}\frac{2s}{R_7C_7\Delta} \qquad 2.5.4.1(b)$$

$$\frac{I_{LP}}{I_{IN}} = H_{LP}\frac{4K_3}{R_7R_8C_7C_8\Delta} \qquad 2.5.4.1(c)$$

$$where\ \Delta = s^2 + \frac{2s}{R_7C_7} + 4\frac{K_3}{R_7R_8C_7C_8};\ H_{HP} = H_{BP} = K_1 = 1,\ K_3 = 2\frac{R_5}{R_6}\ and\ H_{LP} = \frac{K_1}{K_3} = \frac{R_6}{2R_5}$$

Thus the various parameters of the above biquad filter are given by

$$H_{HP} = H_{BP} = 1 and\ H_{LP} = \frac{1}{K_3} = \frac{R_6}{2R_5} \qquad (2.5.4.2a)$$

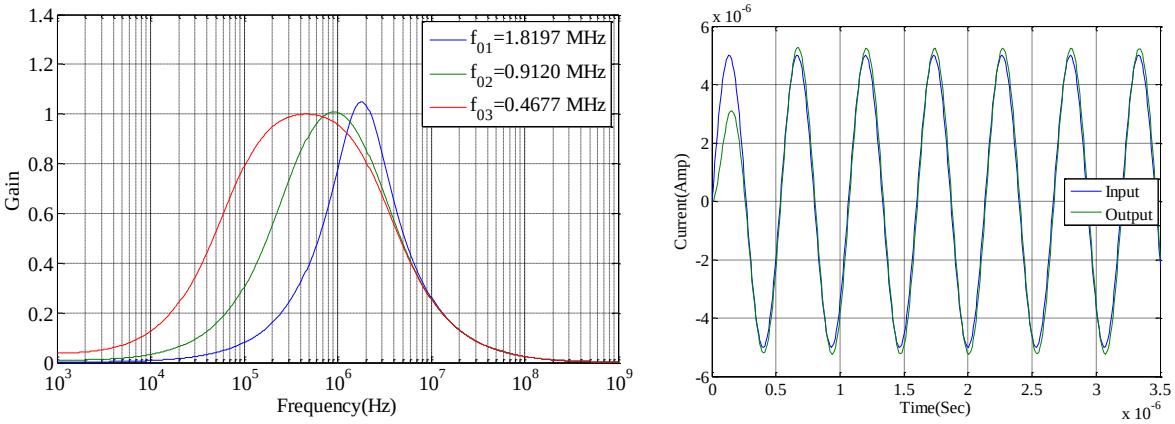
$$f_0 = \frac{1}{\pi}\sqrt{\frac{K_3}{R_7R_8C_7C_8}} = \frac{1}{\pi}\sqrt{\frac{2R_5}{R_6R_7R_8C_7C_8}} \qquad (2.5.4.2b)$$

$$\nabla f = \frac{1}{\pi R_7C_7} \qquad (2.5.4.2c)$$

From equation 5.2.4.2 it is observed that we can vary pole frequency of the filter while keeping gain and bandwidth of the filter fixed.

2.5.4.1 Simulation results

Pole frequency tunability: To change the pole frequency without changing the gain (1) and bandwidth (2.6526 MHz) the value of $K_3(=\frac{2R_5}{R_6})$ was changed. The values of R_5=40 kΩ, 10 kΩ and 2.5 kΩ with R_6=80 kΩ results in K_3 becoming equal to 1, 0.25 and 0.0625. This results in pole frequency assuming the values equals to 1.8759 MHz, 0.9380 MHz and 0.4690 MHz respectively. Fig.2.5.4.2 (a) and (b) show the tunability of pole frequency and time response.



(a) **(b)**

Fig. 2.5.4.2 **(a)** Magnitude response showing tunability of pole frequency f_0 **(b)** Time response of the bandpass filter for an input of 5μA at 1.8759 MHz of of Fig.2.5.4.1.

Now we can summarize the various parameters of six and five CDCC-based fully-differential current-mode universal filters in Table 5.2

Table 2.5.1 Summary of the filter parameters for the circuits of six and five CDCC-based FDCMUF

Circuit	Gain	f_0	∇f
Fig.2.5.1.1	$H_{LP}=\frac{R_1R_6}{R_2R_5}; H_{BP}=2\frac{R_1}{R_2}$ *and* $H_{HP}=2\frac{R_1}{R_2}$	$\frac{1}{\pi}\sqrt{\frac{2R_5}{R_6R_7R_8C_7C_8}}$	$\frac{1}{\pi R_7C_7}$
Fig. 2.5.2.1	$H_{LP}=2\frac{R_1}{R_2}; H_{BP}=\frac{R_1R_4}{R_2R_3}$ *and* $H_{HP}=2\frac{R_1}{R_2}$	$\frac{1}{\pi}\sqrt{\frac{1}{R_7R_8C_7C_8}}$	$\frac{2R_3}{\pi R_4R_7C_7}$
Fig. 2.5.3.1	$H_{LP}=2\frac{R_1}{R_2}; H_{BP}=2\frac{R_1}{R_2}$ *and* $H_{HP}=2\frac{R_1}{R_2}$	$\frac{1}{\pi}\sqrt{\frac{1}{R_7R_8C_7C_8}}$	$\frac{1}{\pi R_7C_7}$
Fig. 2.5.4.1	$H_{LP}=\frac{R_6}{2R_5}; H_{BP}=1$ *and* $H_{HP}=1$	$\frac{1}{\pi}\sqrt{\frac{2R_5}{R_6R_7R_8C_7C_8}}$	$\frac{1}{\pi R_7C_7}$

2.6 Concluding Remarks

The main contributions made in the present chapter can be summarized as follows:

Five new CDCC based single input multi-output (SIMO) type FDCMUF have been introduced. These circuits give explicit current output for all the five filters from high output impedance

nodes. The seven–CDCC based FDCMUF has all the filter parameters independently tunable. The six-CDCC-based filters have two structures; one gives the independent tenability of gain and pole frequency while keeping bandwidth of bandpass filter constant. Another structure of six- CDCC- based filter provides independent tunability of bandwidth while keeping gain and pole frequency of bandpass filter constant. Similarly the five-CDCC-based filters have two structures, one gives the independent tunability of gain while keeping pole frequency and bandwidth of bandpass filter constant. Another configuration of five- CDCC- based filter provides independent tunability of pole frequency while keeping gain and bandwidth of bandpass filter constant. The number of passive elements used in this seven-CDCC based FDCMUF is minimum when compared to other fully-differential universal filter circuits with similar tunability properties and compares well with a single ended electronically tunable biquad filter of [13] with similar tunability properties.

The workability of all these circuits has been established through PSPICE simulations using CMOS CDCC architectures implementable in 0.35-micron technology.

2.7 References

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Chapter 3

Grounded Immittance Simulators Employing a Single CFCC

A number of new immittance simulators employing a single current follower current conveyor (CFCC) and Z-copy current follower current conveyor (ZC-CFCC) which are variants of the basic current differencing current conveyor and three passive components are proposed.

3.1 Introduction[4]

Because of their potential applications in a number of methods of the design of analog filters and oscillators, active simulation of immittances has been a widely researched topic in the area of analog integrated circuits and signal processing. Apart from the classical integrated circuit operational amplifiers (opamp), operational transconductance amplifiers (OTA) and transistor–based simulators, which still evoke interest of researchers in this area [1]-[7], various other active building blocks such as current conveyors (CC) and their different variants [8]-[32], current feedback operational amplifiers (CFOA) [33]-[42], four-terminal floating nullors (FTFN) [43]-[45], operational transresistance amplifiers (OTRA) [46]-[50], current amplifiers (CA) [51] etc. have also been employed for the simulation of immittances of different types.

In recent years, many new synthetic active building blocks, which combine the features of more than one active building block (ABB), have been introduced in the area of analog signal processing and their applications and bipolar and/or CMOS implementation have also been suggested [52]-[71]; see [59] for a classification, review and proposals of several new synthetic active building blocks. Over the years, several of these ABBs have also been used for the realization of synthetic immittances. Among the new ABBs, current differencing buffered amplifier (CDBA) [53],[54], current differencing transconductance amplifier (CDTA) [58], voltage differencing differential input buffered amplifier (VD-DIBA) [60],[61], voltage differencing transconductance amplifier (VDTA) [62],[63], current follower transconductance amplifier (CFTA) [64], voltage differencing current conveyor (VDCC) [65],[66], voltage differencing buffered amplifier (VDBA) [67], current backward transconductance amplifier (CBTA) [68],[69] and current differencing current conveyor (CDCC) [71] have received

[4] The material presented in this chapter has been published in: Alok Kumar Singh, Pragati Kumar and Raj Senani, "New grounded immittance simulators employing a single CFCC," The Journal of Engineering, (IET) Vol.8, pp. 435-447, 2017.

comparatively more attention in the realization of different types of active immittances because of the reason that these simulated immittances, in general, do not suffer from the limitation(s) of the earlier generation of immittance simulators based upon conventional op-amps and provide the circuit designer with a variety of alternatives to choose from.

The immittance simulation circuits presented in [8]-[15] use one-to-three basic current conveyers of type I/II/III with single or dual outputs along with two to four resistors and one capacitor to realize grounded/floating inductors. The generic architecture of the current conveyor has the possibility of adding more functionalities to the core current conveyor and many researchers have modified the architecture of the basic current conveyors and used the new modified current conveyors like modified inverting second–generation current conyeor (MICCII–) [16], gain–variable third–generation current conveyor (GVCCIII) [17], modified inverting first–generation current conveyor (MICCI–) [18], fully differential second–generation current conveyor (FDCCII) [19], dual X second–generation current conveyor (DXCCII) [20]-[22], second–generation current controlled conveyor (CCCII) [23], [24], third–generation current conveyor (CCIII) [25], differential difference current conveyor (DDCC) [26],[27], differential voltage current conveyor (DVCC) [28]-[30], differential current conveyor (DCCII) [31],[32] to realize different types of inductors, namely, lossless inductors with matching constraints [16]-[18], [21], [22], [27], [31] and lossless/lossy inductors without any component matching conditions [19], [25], [28], [29],[32]. Most of these circuits, except those reported in [28, fig.2b] and [32] use a single grounded capacitor as preferred for integrated circuit (IC) implementation. In [30], lossless floating inductor has been realized with two DVCC without any component matching. However, the value of the realized inductors in any of these realizations cannot be tuned. By contrast, in [20] lossless voltage-controlled tuneable grounded inductor has been realized with two DXCCIIs without any component matching condition while employing a single grounded capacitor. Likewise, in [23], lossless

current-controlled tuneable floating inductor has been realized with three/four CCCII/DO-CCCII elements without any component matching with all grounded passive elements. Furthermore, in [24], lossless current-controlled tuneable grounded inductor has been realized without any component matching and with two CCCIIs and a single grounded capacitor.

It is well known now that an ABB, which is closely related to the CC, is the so-called current feedback operational amplifier (CFOA) which is internally a cascade of a CCII+ and a unity gain voltage follower. Among the various immittance simulators using CFOAs, the circuits of [33] attain realization of R-L and C-D immittances using a single CFOA, two resistors and two capacitors whereas in [34], a negative immittance circuit has been presented wherein the simulated immittance values can be orthogonally adjusted. In [35], [36] modified current feedback operational Amplifier (MCFOA) has been used to realize floating and grounded immittance simulators using a minimum number (only three: two resistors and a capacitor) of passive components while employing a grounded capacitor and not needing any component matching constraints for realization of the floating immittances. In [37], four lossy inductors using a canonic number of CFOAs and passive components, without using component matching constraints, has been presented. With a new CFOA, two resistors and a capacitor, four lossless inductors have also been presented. In [38], a method for reducing the effects of CFOA parasitics on the simulated inductor has been discussed. In [39], four new topologies for inductance simulation using a single CFOA have been presented. In [40], using a unified representation for single CFOA-based immittance function simulator, new lossy and lossless grounded inductors have been realized. None of these CFOA-based immittance simulators depends on any passive component matching constraints for the realization of the intended type of immittances. In [41], two lossy and one lossless grounded inductance simulators have been presented which use an inverting type CFOA, two resistors and a single capacitor wherein the authors have also given a CMOS realization of the inverting type CFOA along with its

realization with commercially available AD844 ICs. It may be pointed out that a comprehensive bibliography of various types of immittance simulation circuits using CFOAs has recently been made available in [42].

Besides different varieties of CCs and CFOAs, other ABBs such as FTFNs and OTRAs have also been used to realize different types of lossless/lossy immittances. For various immittance simulation circuits using one/two FTFNs and three-to-seven passive components, (see [43]-[45]). On the other hand, in [46]-[48], a number of single-OTRA-based grounded lossless/lossy, positive/negative inductors have been presented which employ two-to-five resistors and one-to-two capacitors but suffer from the requirement of passive component matching for the realization of the inductors, as in [46], [47]. In [49], grounded lossless inductor using an OTRA and voltage follower employing two capacitors and two resistors has been presented. There is a component matching constraint (equality of two capacitors) for the realization of the inductor. In [50], two grounded lossy inductors as well as a lossless inductor have been presented using two OTRAs, four to five resistors and one capacitor. In the lossless inductor realization, there is a component matching condition whereas in lossy inductor, there is no matching constraint.

A review of the immittance simulators using other miscellaneous active elements, including several of comparatively more recent origin, reveals the following. In [51], two current amplifiers and a grounded capacitor have been used for the realization of a lossless grounded as well as floating inductor. In [53], two floating inductance simulator circuits using three-to-four CDBAs, a single grounded capacitor and four MOS-controlled resistors have been presented. In [54], three single-CDBA-based grounded inductance (both lossless as well as lossy) circuits have been presented. A lossless grounded inductor without any component matching constraint using two CDTAs and a single grounded capacitor has been presented in [58], whereas, a floating inductor has been realized with three CDTAs and a grounded

capacitor but needs the equality of two transconductaces for the intended realization. In [60], two/three VD-DIBAs and a grounded capacitor have been used to realize lossless grounded/floating inductance, whereas a single VD-DIBA, one grounded capacitor and one floating resistor has been used to realize an electronically-tuneable lossless grounded inductor. An electronically-tuneable floating inductance simulator using two VD-DIBAs, a single grounded capacitor and a floating resistor has also been presented in [61]. In [62], a single/two VDTA-based electronically-tunable grounded/floating inductance simulators employing a single grounded capacitor have been presented. On the other hand in [63], a Z-copy VDTA has been used to realize a floating lossless inductance employing a single grounded capacitor. In [64] two/three CFTAs have been used to realize a grounded/floating gyrator circuit. A new building block called VDCC [65], [66] has been used to realize a number of grounded lossy/lossless grounded/floating inductances using a single VDCC, one resistor and one capacitor. In [67], a single VDBA has been used to realize a lossless grounded inductor employing one resistor and one capacitor. Current backward transconductance amplifier (CBTA) has been used in [68],[69] to simulate a floating inductance using two CBTA and three grounded passive elements in [68] and one CBTA and two grounded passive components in [69]. In [71], a single CDCC with one grounded capacitor and two resistors has been uses to simulate four circuits of lossy inductors.

In retrospection, it has been found that the various published circuits for simulation of grounded and floating inductors can be broadly categorized into three major classes: Class I- circuits employing commercially available IC building blocks namely, IC operational amplifiers, IC operational transconductance amplifiers, conventional current conveyors and IC current feedback amplifiers [3], [5], [8]-[13],[33],[34],[37]-[40] , Class II- circuits using newer building blocks which are although not available as off-the-shelf ICs but their bipolar and/or CMOS implementations have been known/proposed and utilized in the simulations [4], [6],

[7], [14]-[30],[31],[32], [35], [36], [45], [46], [48], [51],[53], [58], [61]-[71] and class III in which those composite building blocks have been employed which have been shown to be realizable employing commercially available ICs [17],[31],[32] [36], [37], [41], [43], [44], [46], [47], [49], [50], [54], [60], [67].

In this chapter, we present a family of active immittances realized with a single current follower current conveyor (CFCC) or Z-copy CFCC (ZC-CFCC). Although the MOCFCC was also introduced in [59], to the best knowledge of the authors, its use has not yet been fully exploited for the realization of synthetic immittances. The main intention of this communication is, therefore, to present a variety of single CFCC-based lossy/lossless immittance simulators falling within the class II mentioned above.

3.2 Current follower current conveyor (CFCC)

CFCC [59] is a five-port active building block whose symbolic notation is shown in Fig. 3.2.1.

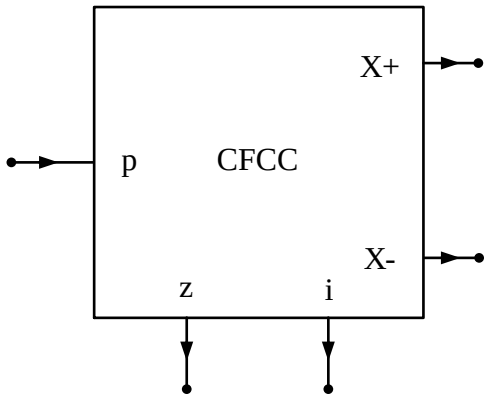


Fig.3.2.1 Symbolic notation of CFCC

The current at the z terminal is an inverted copy of the input current at ‘p’ terminal. The terminal ‘i’ tracks the potential at the terminal z. Two complementary currents at the output terminals are available which are copies of the current at the ‘i’ terminal. To provide addition functionality to the CFCC a copy of the current at the ‘z’ terminal has also been provided resulting in the Z-copy CFCC. The CMOS implementation of ZC-CFCC is shown in Fig.3.2.2

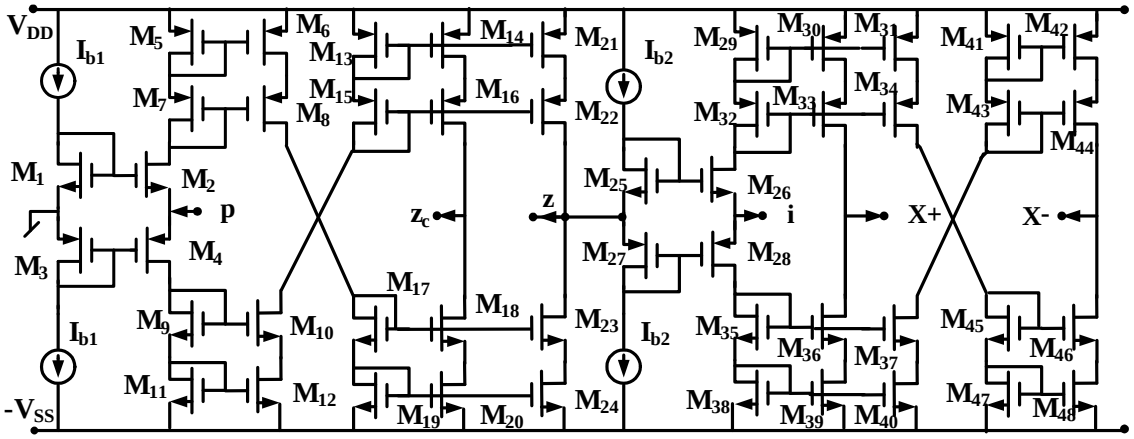


Fig.3.2.2 CMOS implementation of ZC-CFCC

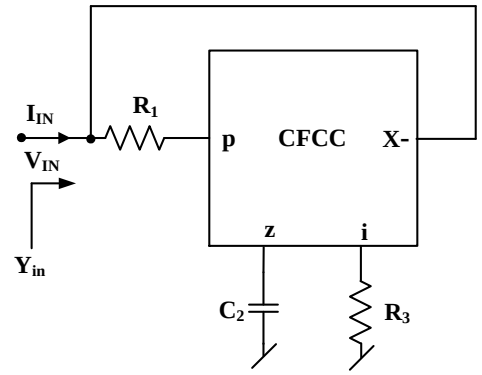
Mathematically, a ZC-CFCC can be characterized by the following matrix equation:

$$\begin{bmatrix} V_p \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \\ I_{zc} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ V_z \\ I_i \\ V_{x+} \\ V_{x-} \\ V_{zc} \end{bmatrix} \tag{3.2.1}$$

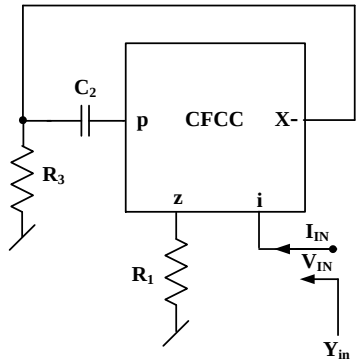
3.3 Proposed CFCC-based immittance simulators

Fig.3.3.1 and Fig.3.3.2 show the proposed simulated immittance networks.

It is seen that, the circuits of Fig. 3.3.1(a), realizes a positive parallel RL, while those of Fig. 3.3.1(b) realize, parallel of a positive/ negative resistor and negative inductor and the circuits given in Fig. 3.3.1(c) realizes a positive series RL and a negative series RL without any conditions providing single resistance control of relevant equivalent parameter value.

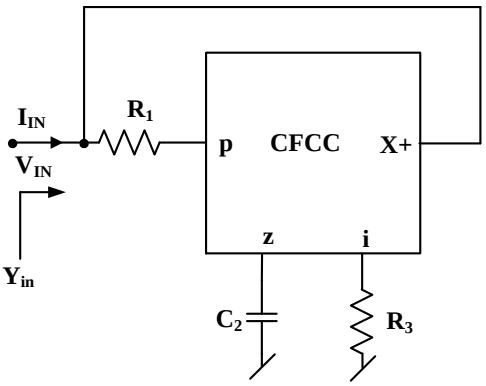


$$Y_{in} = \frac{1}{R_1} + \frac{1}{sR_1R_3C_2}$$

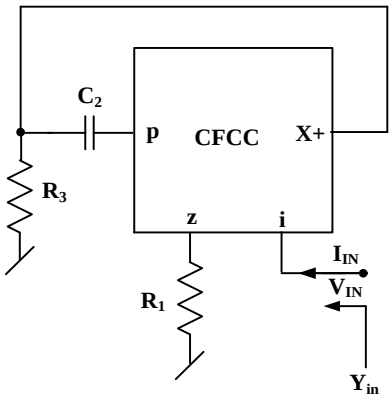


$$Y_{in} = \frac{1}{R_1} + \frac{1}{sR_1R_3C_2}$$

(a)

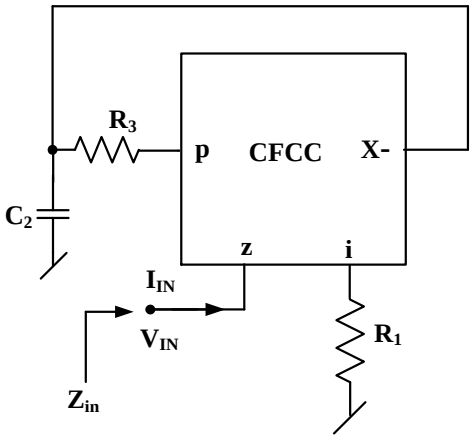


$$Y_{in} = \frac{1}{R_1} - \frac{1}{sR_1R_3C_2}$$

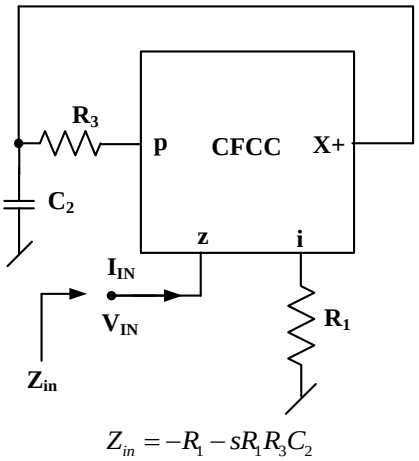


$$Y_{in} = -\frac{1}{R_1} - \frac{1}{sR_1R_3C_2}$$

(b)



$$Z_{in} = R_1 + sR_1R_3C_2$$



$$Z_{in} = -R_1 - sR_1R_3C_2$$

(c)

Fig. 3.3.1 Various non-ideal immitttance simulators realized using a single CFCC

On the other hand, the circuit of Fig.3.3.2 (a) realizes a lossless grounded inductance, that of Fig.3.3.2 (b) realizes a negative inductance and that of Fig. 3.3.2(c) realizes an ideal frequency

dependent negative resistance (FDNR) with no component-matching constraints required and with the value of the realized impedance being single-resistance tunable in all the cases. If the resistors R_1 , R_2 and R_3 shown in Fig. 3.3.1 and Fig. 3.3.2 are replaced with linear voltage controlled resistors (VCR) realized with CMOS circuit of [72, Fig. 6e therein], then all the circuits would attain electronic tunability of the various realized parameters through control voltages V_{pi} and/or V_{ni} for i=1-3. On the other hand, the resistors connected at the p terminal and the i terminal can altogether be expoloited by the appropriate choice of the bias current to realize current controlled lossless grounded inductors also [73].

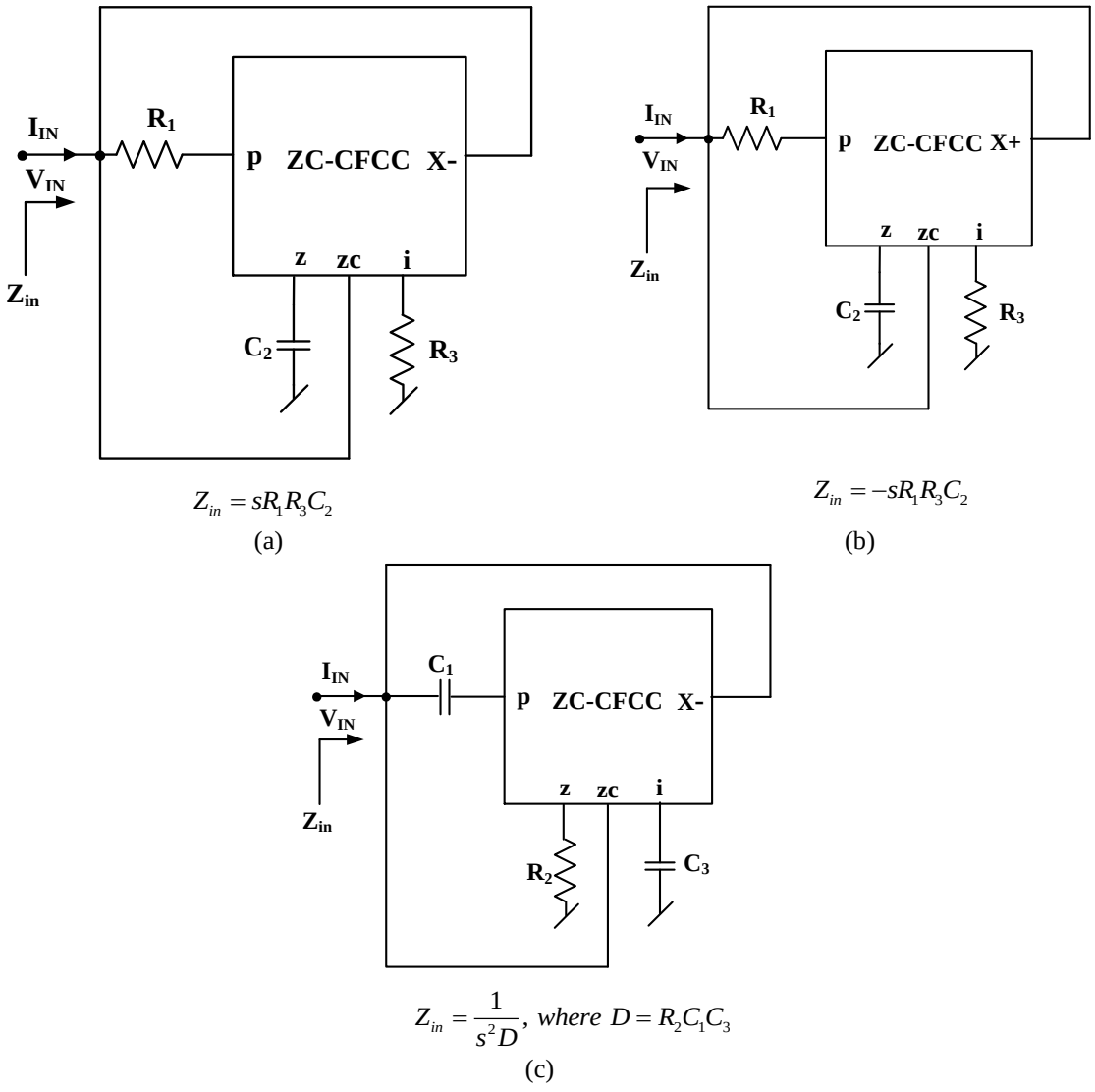


Fig. 3.3.2 Various ideal immitttance simulators realized using a single ZC-CFCC

3.4 Non-ideal analysis

A non-ideal behavioral model of the ZC-CFCC [59] is shown in Fig.3.4.1 (a). In this model, R_p represents the parasitic input resistances of the p port whereas R_z, C_z represent the resistance and capacitance at z-terminal of the ZC-CFCC. Similarly, R_{zc} and C_{zc} represent resistance and capacitance at zc terminal while R_i represents the output resistance of the voltage buffer of the MO-CCII (resistance at i terminal). On the other hand, R_{x+} and C_{x+} represent output resistance and output capacitance at the x+ terminals of the ZC-CFCC and finally, R_{x-} and C_{x-} represent the output resistance and the output capacitance at the x-terminals of the ZC-CFCC. The relations between the various port variables for the non-ideal ZC-CFCC, with additional zc terminal, are given by:

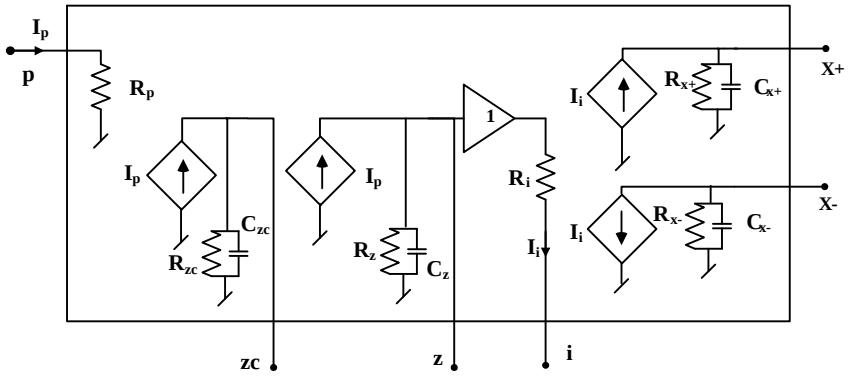
$$\begin{bmatrix} V_p \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \\ I_{zc} \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 & 0 & 0 \\ 1 & -\left(\frac{1}{R_z}+sC_z\right) & 0 & 0 & 0 & 0 \\ 0 & 1 & -R_i & 0 & 0 & 0 \\ 0 & 0 & 1 & -\left(\frac{1}{R_{x+}}+sC_{x+}\right) & 0 & 0 \\ 0 & 0 & -1 & 0 & -\left(\frac{1}{R_{x-}}+sC_{x-}\right) & 0 \\ 1 & 0 & 0 & 0 & 0 & -\left(\frac{1}{R_{zc}}+sC_{zc}\right) \end{bmatrix} \begin{bmatrix} I_p \\ V_z \\ I_i \\ V_{x+} \\ V_{x-} \\ V_{zc} \end{bmatrix} \quad (3.4.1)$$

The determination of the non-ideal expressions for Z_{in} or Y_{in} for the various circuits by considering the parasitic impedances of the CFCC is straightforward and therefore, instead of presenting such expressions for all the proposed circuits, these have been given in the following only for some representative cases.

3.4.1 Non-ideal analysis of the lossy inductor of Fig.3.3.1(a)

A straightforward analysis of this circuit shows that the admittance using non-ideal model of the CFCC, is given by

$$Y_{in1} = \frac{1}{R_1 + R_p} + \frac{1}{R_{x-}} + sC_{x-} + X \qquad (3.4.1.1)$$

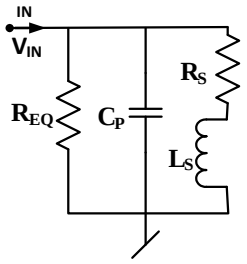


(a)

Fig. 3.4.1 (a) Non-ideal equivalent circuit of the ZC-CFCC with additional zc terminal

$$where \quad X = \frac{1}{\frac{(R_1 + R_p)(R_3 + R_i)}{R_z} + s(R_1 + R_p)(R_3 + R_i)(C_2 + C_z)}$$

A passive equivalent of this admittance can, thus, be constructed as shown in Fig. 3.4.1(b)



(b)

Fig. 3.4.1 (b) Passive equivalent circuit for lossy and lossless inductor as shown in Fig. 3.3.1(a) and Fig. 3.3.2(a)

where

$$R_{EQ} = (R_1 + R_p) \,||\, R_{x-}, C_p = C_{x-}, R_s = \frac{(R_1 + R_p)(R_3 + R_i)}{R_z} \;\; and$$

$$L_s = (R_1 + R_p)(R_3 + R_i)(C_2 + C_z) \qquad (3.4.1.2)$$

From the equivalent circuit of the lossy inductor (R||L) it is observed that the various parasitics of the CFCC, namely R_p (ideal value=0), R_z (ideal value=∞), R_i (ideal value=0), R_{x-} (ideal

value=∞) introduce a parallel capacitor C_p and a series resistance R_s in the lossy inductor. The measured value of R_p ,R_i , R_z and R_{x-} are given in Table 3.8.1.

As these valued are very close to the ideal values of these parsitics, it may be concluded that the effect of the CFCC parasitics on the Q factor of the lossy inductor will not be appreciable.

3.4.2 Non-ideal analysis of the lossless ınductor of Fig.3.3.2(a)

The non-ideal expression of the lossless grounded inductor of Fig. 3.3.2(a), using the non-ideal model of CFCC with additional zc terminal, is found to be

$$Y_{in2} = \frac{1}{R_{zc} \,||\, R_{x-}} + s(C_{zc} + C_{x-}) + X \qquad (3.4.2.1)$$

This gives the values of the different passive components in the general equivalent circuit shown in Fig. 3.4.1(b), as

$$R_{EQ} = R_{zc} \,||\, R_{x-}, C_p = C_{zc} + C_{x-}, R_s = \frac{(R_1 + R_p)(R_3 + R_i)}{R_z}$$

$$and\ L_s = (R_1 + R_p)(R_3 + R_i)(C_2 + C_Z) \qquad (3.4.2.2)$$

3.4.3 Non-ideal analysis of the FDNR of Fig.3.3.2(c)

The non-ideal input impedance of the FDNR circuit of Fig. 3.3.2(c), with the ZC-CFCC replaced with its non-ideal model given in expression (3.4.1), is found to be

$$Z_{in} = \frac{1}{\dfrac{s^2 C_1 C_3 R}{(1 + sR_i C_3)(1 + sR_p C_1)(1 + sRC)} + \dfrac{(1 + sR_k C_k)}{R_k}} \qquad (3.4.3.1)$$

$$where\ R = R_2 \,||\, R_z, C = C_z, R_k = R_{zc} \,||\, R_{x-}\ and\ C_k = C_{zc} + C_{x-}.$$

Unfortunately, the non-ideal expression (3.4.3.1) does not appear to lead to a simple equivalent circuit like that of Fig. 3.4.1(b).

3.5 SPICE simulation results

The CMOS implementation of the ZC-CFCC shown in Fig. 3.2.2 has been used to verify the workability of the circuits presented in this chapter. The aspect ratios of the MOSFETS employed are given in Table 3.5.1. The values of the DC bias currents and voltages were taken as 40 µA and ± 2.5V respectively.

Table 3.5.1 Aspect ratios of MOSFETs used in ZC-CFCC given in Fig. 3.2.2

MOSFETs	W/L (µm/µm)
M_1, M_2, M_{25}, M_{26}	25/0.25
M_3, M_4, M_{27}, M_{28}	50/0.25
M_5 - M_{24}, M_{29} -M_{48}	2.5/0.25

To verify the workability of the proposed structures we now present some sample application circuits and the results of their verification using SPICE simulations

Time response and frequency response of the simulated grounded inductor: The lossless grounded inductor of Fig.3.3.2 (a) was designed to have a value of 1mH (by choosing $R_1 = R_3 = 10K\Omega$, $C_2 = 0.01nF$). The control voltages for the voltage controlled CMOS resistors used in the simulation {shown in Fig. 3.5.1(d)} were taken as $V_n = -V_p = 997mV$. An input current with a triangular waveform (5 µA amplitude) was applied to the proposed inductor (1mH) shown in Fig.3.3.2 (a). The output voltage, a square wave, is obtained as shown in Fig. 3.5.1(a).

The frequency response of the simulated lossless inductor was determined through PSPICE simulations and is shown in Fig. 3.5.1(b). It is observed that the lossless inductor can be used satisfactorily up to a frequency of 5.4 MHz (with the error in the simulated value of inductance being no more than 10 % in this range). Fig. 3.5.1(c) shows the impedance magnitude and phase for inductor (value 1mH). The simulated results agree quite well with the theoretical ones. The discrepancy between theoretical and simulated results is mainly attributed to the non-ideal gain and parasitic impedance effects of the ZC-CFCC.

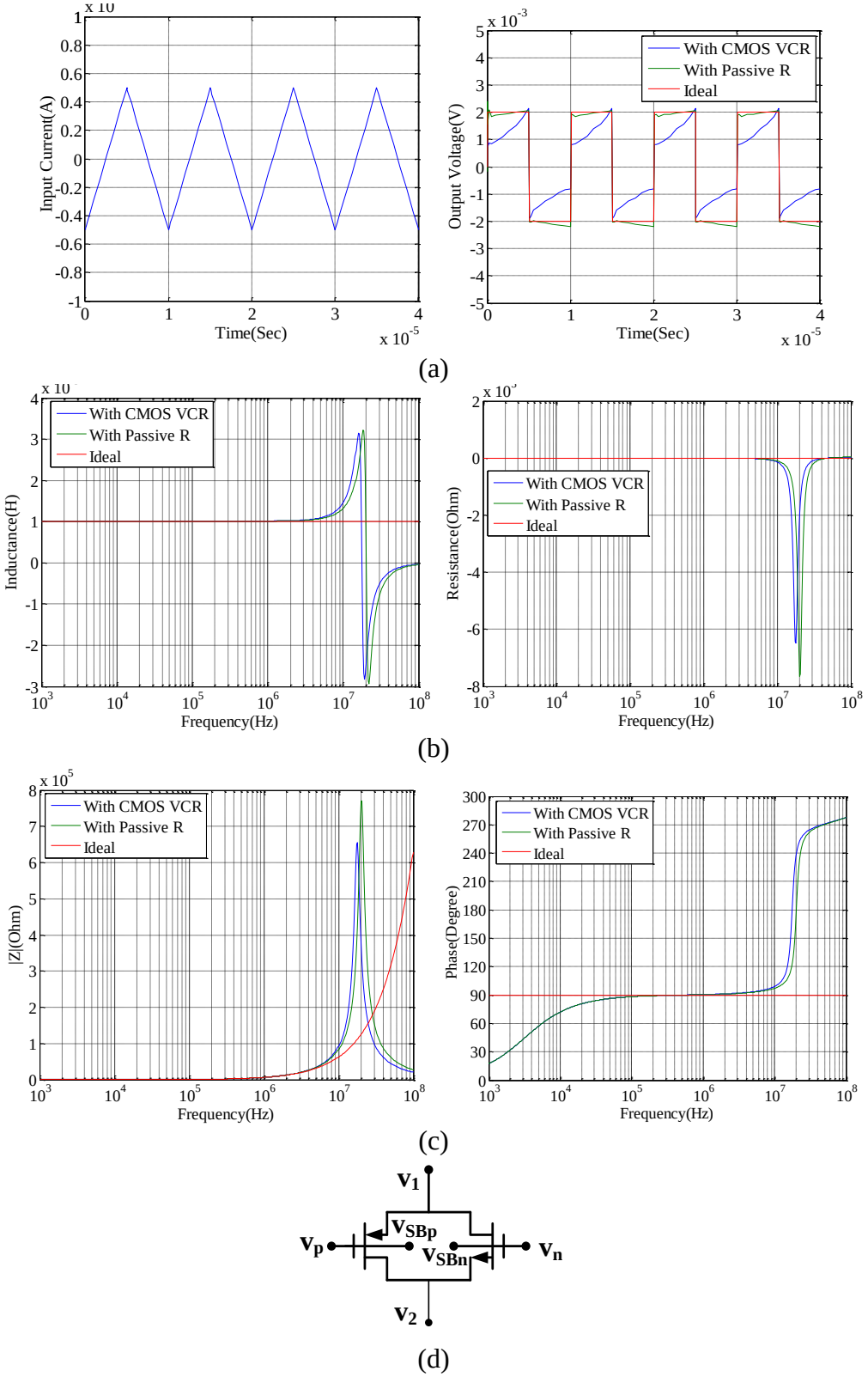


Fig. 3.5.1 Time response and Frequency response of the simulated lossless inductor (a) Time response of the simulated inductor(b) Variation of inductive and resistive part with frequency (ideal value of associated resistance being 0 Ω) (c) Magnitude and phase response of the proposed grounded inductor (d) CMOS VCR given in [72, Fig. 6e therein]

Second order RLC high pass filter using simulated inductor: The simulated lossy inductor (R= 10 kΩ‖L=10mH) realized from Fig. 3.3.1(a) has been used to design a second order high pass filter with cutoff frequency of 225 kHz for which the corresponding active realization is given in Fig.3.5.2 The high pass transfer function is given as

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + s\left(\frac{1}{R_1 C_1}\right) + \left(\frac{1}{LC_1}\right)} \tag{3.5.1}$$

The pole frequency is given by

$$f_o = \frac{1}{2\pi\sqrt{LC_1}} \tag{3.5.2}$$

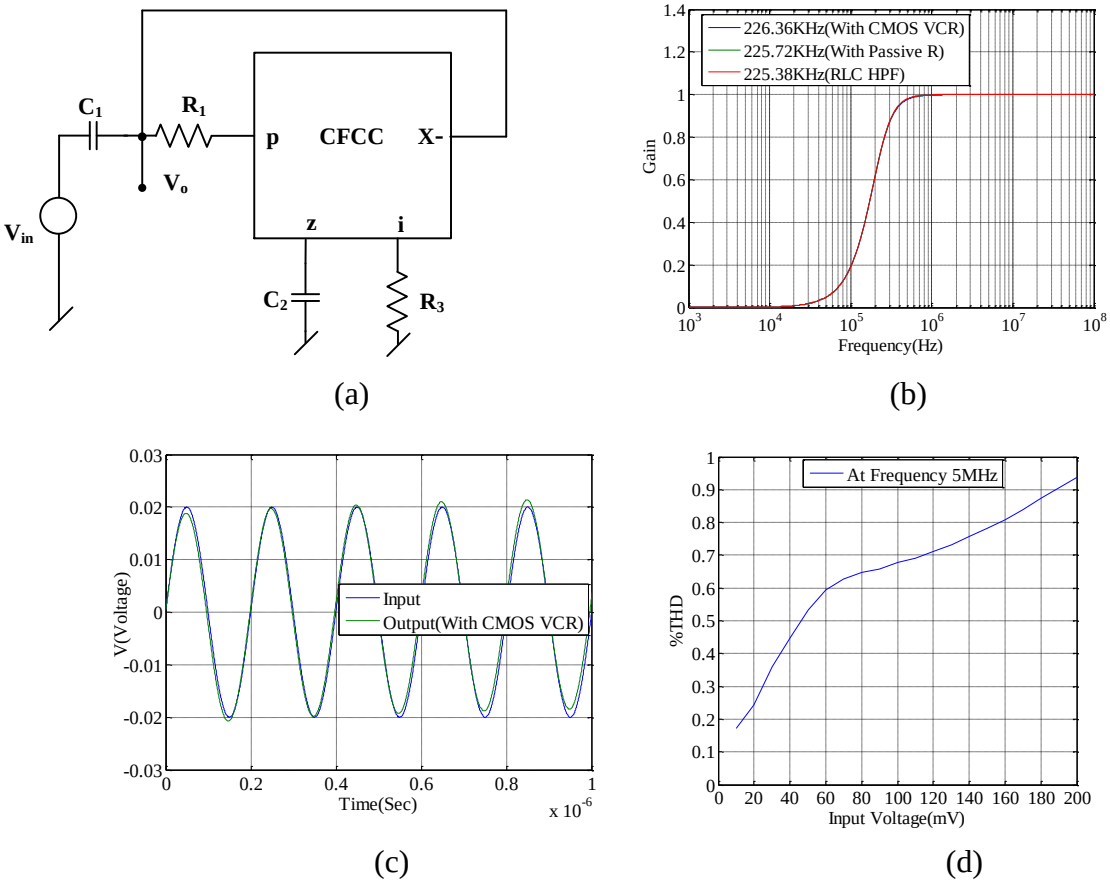


Fig.3.5.2 Second order RLC high pass filter using simulated inductor (a) Active realization (b) Magnitude response for the circuit(c)Transient Response(d)Variation of THD with applied input voltage at 5MHz

The following values of components were chosen to simulate the lossy inductor: R_1 = 10 kΩ, R_3 = 10 kΩ, C_2 = 0.1 nF with C_1=0.0.5 nF. We have superimposed the frequency responses of the active high pass filter realized with (i) R_1 and R_3 as passive resistors and (ii) R_1 and R_3 realized with voltage controlled CMOS resistors (control voltages $V_n = -V_p$ = 981 mV) which are shown in Fig. 3.5.2b. The simulated values of the pole frequency were found to be 225.72 KHz and 226.36 KHz respectively, which are seen to be in good agreement. Fig 3.5.2c-Fig.3.2.2d show the transient response of the filter for an input amplitude of 20 mV at a frequency of 5 MHz and the % THD in the output when the input amplitude was varied in the range of 10-200 mV.

Second order RLC band pass filter using simulated inductor: Lossless inductor (L=1mH) realized from the circuit of Fig. 3.3.2a has been used to design a second order bandpass filter with the pole frequency of 503.29 KHz and BW=1.5915 MHz for which the corresponding active realization are given in Fig.3.5.3a. The bandpass transfer function is given as

$$\frac{V_o}{V_{in}} = \frac{s\left(\frac{1}{RC}\right)}{s^2 + s\left(\frac{1}{RC}\right) + \left(\frac{1}{LC}\right)} \tag{3.5.3}$$

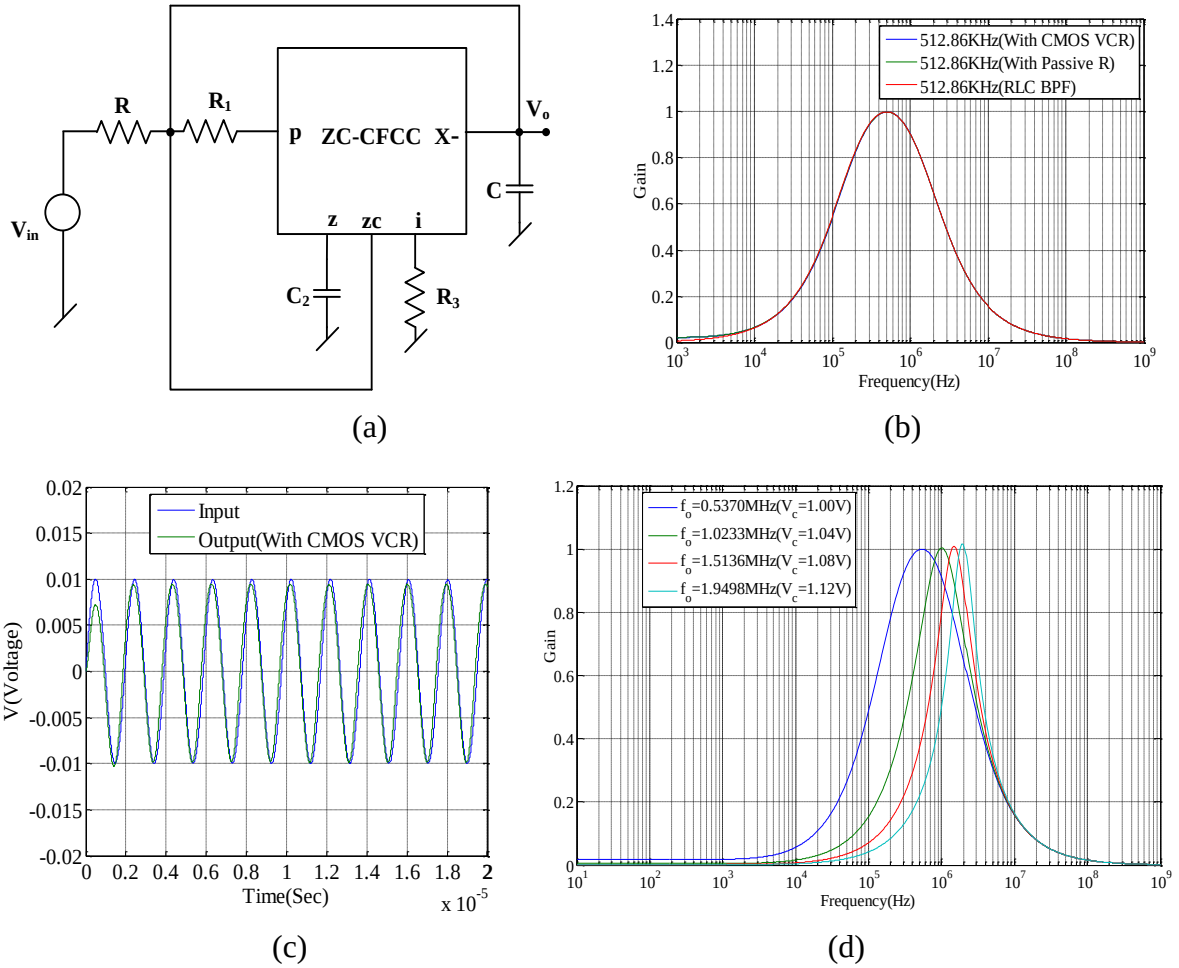


Fig. 3.5.3 Second order RLC band pass filter realization (a) Active realization (b) Magnitude response for the circuit(c)Transient Response (d)Tunability of the pole frequency with control voltage

The pole frequency and the bandwidth are given by

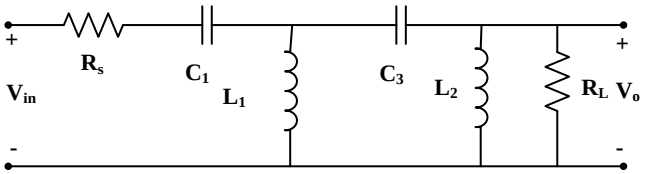
$$f_o = \frac{1}{2\pi\sqrt{LC}} \qquad BW = \frac{1}{2\pi RC}$$

The lossless inductor was designed with the following values of the passive components R_1 = R_3 = 10KΩ, C_2 = 0.01nF. The control voltages for the voltage controlled CMOS resistors were taken as $V_n = -V_p$ = 997mV. With R = 1 kΩ, C = 0.1nF, the simulated value of the pole frequency was found to be 512.86 KHz whereas the bandwidth was found to be 1.5870 MHz. The frequency response obtained from SPICE simulations is shown in Fig. 3.5.3(b). Fig

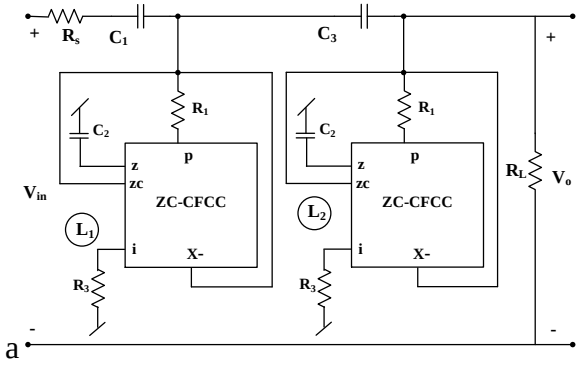
3.5.3(c) shows the transient response of the filter for an input amplitude of 10 mV at a frequency of 512.86 KHz .

The value of the voltage controlled CMOS resistors can be varied by changing the control voltages thereby making the simulated immittances electronically tunable. The second order bandpass filter shown in Fig. 3.5.3(a) was used to check the tunability of the center frequency of the bandpass filter by changing the control voltages V_p and V_n ($V_c = V_n = -V_p$). Fig. 3.5.3(d) shows the variation of center frequency of the tunable bandpass filter, obtained by changing V_p and V_n, which confirm the electronic variability of the lossless inductor of Fig. 3.3.2(a).

Fourth order Butterworth high pass filter: Another example of the application of the electronically-tunable, lossless grounded inductor is in the realization of a fourth order Butterworth high pass filter. A prototype fourth order high pass filter is shown in Fig.3.5.4(a).The normalized component values for cut off frequency of 1Hz, are : $R_s=R_L=1\Omega$, , $L_1=L_2=0.1217$H, $C_1=0.2768$F and $C_3=0.0780$F [45]. After performing appropriate frequency and impedance scaling on the prototype for cut-off frequency of 1.59MHz, the final values of components are $R_s=R_L=1$ kΩ, $L_1=L_2=$ 76.54uH, $C_1=$1.74.1pF and $C_3=$49.1pF. The inductor of 76.54uH was simulated with control voltage $V_c = V_n = -V_p=1.1056$V. The active realization of the filter is shown in Fig. 3.5.4b.Value of the simulated cut-off frequency was found to be $f_0=1.5952$MHz. The frequency response and transient response of the Filter for an input amplitude of 10 mV at a frequency of 5 MHz is shown in Fig.3.5.4(c) and Fig.3.5.4(d) respectively.



(a)



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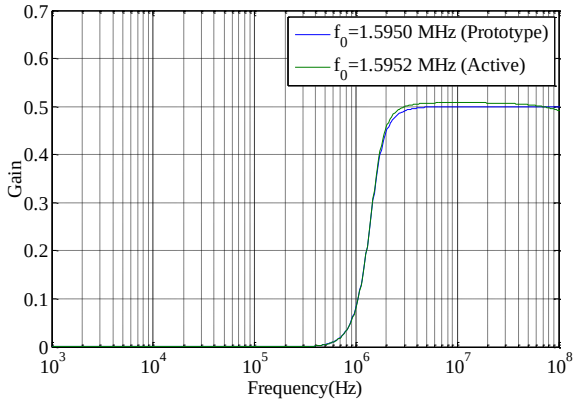
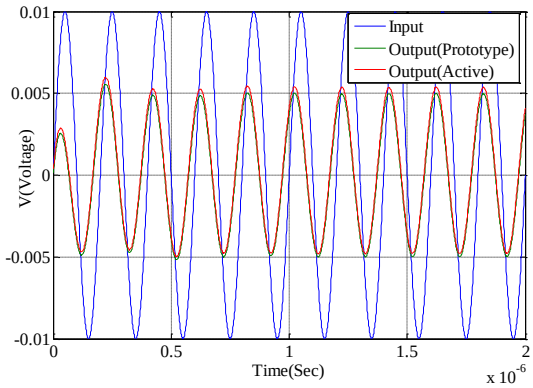


(c)



(d)

Fig. 3.5.4 Fourth order high pass Butterworth filter realization (a) Prototype (b) Active realization (c) Magnitude response for the circuit (d) Transient response

Second order RCD low pass filter using simulated FDNR: The simulated ideal grounded FDNR of Fig. 3.3.2(c) was used to design a second order low pass filter, by applying Bruton's transform to the passive second order filter shown in Fig. 3.5.5(a). The transformed FDNR filter realization is shown in Fig. 3.5.5(b) for which the transfer function is given by

$$\frac{V_o}{V_{in}} = \frac{\left(\frac{1}{RD}\right)}{s^2 + s\frac{(RC^2 + D)}{RCD} + \left(\frac{2}{RD}\right)} \qquad (3.5.4)$$

The circuit realizes a second order RCD low pass filter for which the filter parameters are given by

Pole frequency $f_o = \frac{1}{\pi\sqrt{2RD}}$ Quality Factor $Q = \frac{C}{(RC^2 + D)}\sqrt{2RD}$

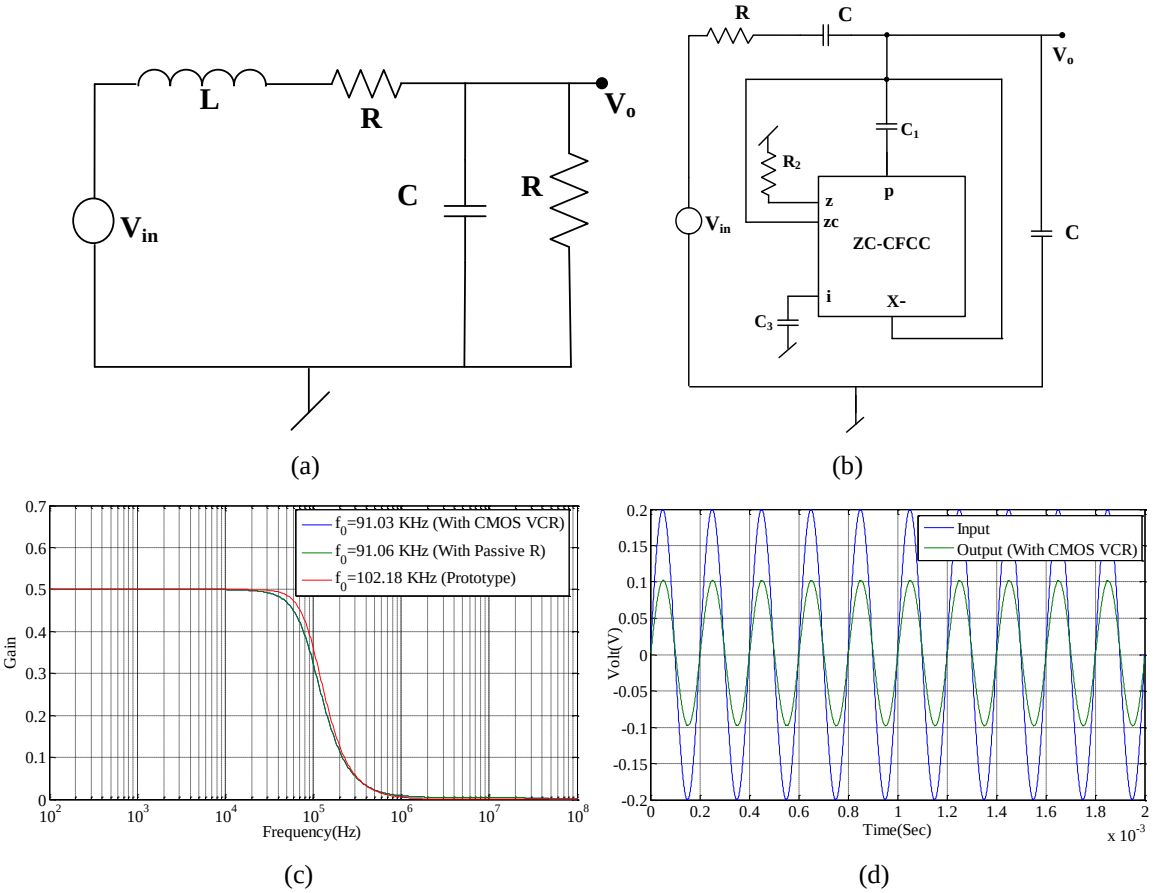


Fig. 3.5.5 Second order RCD low pass filter realization (a) Prototype (b) Active realization (c) Magnitude response for the circuit(d) Transient response

The FDNR was designed with the following passive component C_1 = 0.22nF, R_2 = 10 kΩ, C_3 = 0.22nF, (D = $R_2C_1C_3$), with R = 10 kΩ, C = 0.22nF, to have a pole frequency of 102.31KHz. The simulate value of the pole frequency was found to be 91.06 KHz.When R_2 was replaced by a voltage controlled CMOS resistor (control voltages $V_n = -V_p$= 880.5mV) the simulated value of pole frequency were found to be 91.03KHz {Fig.3.5.5(b)}. The difference between the designed pole frequency and the simulated value may be attributed to the uncompensated parasitic impedance at the z-terminal of the ZC-CFCC. However, this should not be a cause of

concern as the same can be adjusted by varying the control voltage. For correcting the frequency response at DC a large resistor R_c=2.32 MΩ shunting the series C (Bruton transformed series R) was required as is normally needed in RCD filters [70]. Fig.3.5.5(c)-Fig.3.5.5 (d) show the frequency response and transient response of the filter for an input amplitude of 200 mV at a frequency of 5KHz. The percentage THD in the output when the input amplitude was varied in the range of 5-200 mV was found to be less than one percent. For simulating the FDNR the rail voltage was kept at ± 1.9 V.

The SPICE simulations shown in this section demonstrate the viability of new proposed immittance simulators using CFCC.

3.6 Comparison with recently published grounded inductance simulators

We now present a comparison of the proposed inductance simulators with the existing single active building blocks –based grounded inductance simulators in Table 3.6.1

Table 3.6.1: Comparison with other recently published grounded inductors realized with single active building block

Ref.	Inductance Type* G	Single Active element Class	Number of resistors used	Number of Capacitors used	Whether free from passive component matching	Availability of Electronic Tunability	Technology	Power Supply voltage	Power Dissipation
[14]	Lossless	CCI [II]	4	1F	No	No	0.35µm	±1.65V	NA
[15]	Lossy	CCIII [II]	2	1G/F	Yes	No	0.6µm	±2.5V	1.5mW
[16]	Lossless	MICCII− [II]	2	1F	No	No	0.35µm	±2.5V	17.6mW
[17]	Lossy	GVCCIII [II/III]	2	1F	Yes	No	0.25µm AD844	±1.5V ±15V	NA
	Losslss	GVCCIII [II/III]	2	1F	No	No	0.25µm AD844	±1.5V ±15V	NA
[18]	Lossless	MICCI− [II]	2	1F	No	No	0.35µm	±1.5V	NA
[19]	Lossless	FDCCII [II]	2	1G	Yes	No	0.35µm	±1.5V	NA
[21]	Lossless	DXCCII [II]	2	1F	No	No	0.35µm	±1.5V	NA

[22]	Lossless	DXCCII [II]	2/3	1F	No	No	0.35µm	±1.65V	NA
[25]	Lossy	CCIII+ [II]	2/3	1F	Yes	No	PNP/NPN Array B101/102	±10V	NA
[27]	Lossless	MDO-DDCC [II]	2	1G	No	No	0.35µm	±1.5V	NA
[28]	Lossy	DVCC [II]	2	1G/1F	Yes	No	0.5µm	±2.5V	NA
[31]	Lossless	DCCII [II/III]	2	1G	No	No	Bipolar Array ALA400 AD844	±2.5V ±15V	NA
[32]	Lossless	DCCII [II/III]	2	1F	Yes	No	0.25µm AD844	±1.25V ±15V	NA
[33]	Lossy	CFOA [I]	2	2G	No	No	Discrete AD844	NA	NA
[34]	Lossy(−)	CFOA [I]	2	2(1G+1F)	Yes	No	Discrete AD844	NA	NA
[36]	Lossless	MCFOA [II/III]	2	1G	Yes	No	0.25µm AD844	±1.5V	NA
[37]	Lossy	CFOA [I]	2	1F	Yes	No	Discrete AD844	±15V	NA
	Losslss	New CFOA [III]	2	1F	Yes	No	Discrete AD844		
[39]	Lossless (−)	CFOA [I]	2	1F	Yes	No	Discrete AD844	±10V	NA
	Lossy (+/−)	CFOA [I]	2	1F	Yes	No	Discrete AD844	±10V	NA
[40]	Lossy (+/−)	CFOA [I]	2/3	1F	Yes	No	Discrete AD844	±15V	NA
	Lossless (−)	CFOA [I]	2	1F	Yes	No	Discrete AD844	±15V	NA
[41]	Lossy	CFOA-[III]	2	1G	Yes	No	0.13µm AD844	±0.75V	0.89mW
	Losslss	CFOA-[III]	2	1F	Yes	No	0.13µm AD844	±0.75V	0.89mW
[43]	Lossy (+/−)	FTFN [III]	2	1F	Yes	No	Discrete AD844	NA	NA
[45]	Lossless	PFTFN [II]	4	1F	No	No	0.35µm	±5V	NA
[46]	Lossless	OTRA [II/III]	3	2F	No	No	0.5µm AD844	±01.5V ±5V	0.809mW 260mW
[47]	Lossless (−)	OTRA [III]	5	1F	No	No	Discrete AD844	NA	NA
[48]	Lossy	OTRA [II]	2/3	1F	Yes	No	1.2µm	±5V	NA

[54]	Lossy	CDBA [III]	2	1F	Yes	No	Discrete AD844	±12V	NA
	Losslss	CDBA [III]	4	1F	No	No	Discrete AD844	±12V	NA
[61]	Lossless	VD-DIBA [II]	1	1G	Yes	Yes by changing g_m	0.35µm	±2V	NA
[62]	Lossless	VDTA [II]	0	1G	Yes	Yes by changing g_m	0.18µm	±0.9V	NA
[65]	Lossless/ lossy	VDCC [II]	1	1G	Yes	Yes by changing g_m	0.18µm	±0.9V	0.869mW
[67]	Losslss	VDBA [II/III]	1	1F	Yes	Yes by changing g_m	Discrete OPA860	±5V	NA
[69]	Lossless	CBTA [II]	1	1G	Yes	Yes by changing g_m	0.25µm	±2.5V	NA
[71]	Lossy	CDCC [II]	1	1G	Yes	No	0.35µm	±1.5V	NA
Proposed	lossy	CFCC [II]	2	1G/1F	Yes	No	0.18 µm	±2.5V	1.78mW
	lossy	CFCC [II]	2[VCR]	1G/1F	Yes	Yes			
Proposed	Lossless	ZC-CFCC [II]	2[VCR]	1G	Yes	Yes	0.18 µm	±2.5V	1.95mW

*F: Floating, G: Grounded, NA: (concerned data/information) not available

When compared with recently published immittance simulators realized with single active building blocks it is revealed that, with the exception of the earlier circuits presented in [61], [62], [65], [67], [69] which provide electronic tunability through the variation of the transconductance parameter, the proposed circuits are the only one's which provide the following advantageous features *simultaneousl*y (i) use of a single ABB (ii) employment of a cannonic number of RC elements (iii) use of grounded capacitor in several cases (iv) complete absence of any passive element matching conditions (v) electronic tunability through an external voltage signal (vi) reasonably low-voltage operation coupled with very low-power consumption and (vii) suitability for CMOS implementation. It may also be mentioned here that the input dynamic range of the circuits using inductance in case of simulators presented in [61], [62], [65], [67], [69] is constrained by the linear range of operation of the active device

being used. By contrast, there is no such constraint for the proposed simulators as the tunability of immittances is affected by changing the value of the CMOS VCR which is quite linear.

3.7 Concluding remarks

In this chapter, a number of new electronically-controllable grounded immittance simulation circuits were proposed all of which employ only a single CFCC along with a canonical number of passive elements without requiring any passive component-matching conditions. When compared with the previously known circuits, the proposed synthetic immittance circuits possess several advantageous features as elaborated in section 3.6. The workability of the proposed new configurations has been verified by SPICE simulations of a number of application circuits implemented with CFCC architectures suitable for CMOS implementation in 0.18 µm CMOS technology. The proposed single-CFCC-based simulators, thus, add new useful alternatives to the existing repertoire of single-active-building-block-based grounded immittance simulators as given in Table 3.6.1

3.8 Appendix

Measured values of the non-ideal parameters of the ZC-CFCC shown in Fig. 3.4.1(a) at DC bias voltage ± 2.5V and DC bias currents 40µA have been found to be as given in Table 3.8.1.

Table 3.8.1 Characteristic parameters of ZC-CFCC

S.No.	Parameter	Value
1	R_p	591 Ω
2	R_z	4.9178 MΩ
3	C_z	6.3234×10^{-14} F,
4	R_{zc}	4.9178 MΩ
5	C_{zc}	7.2123×10^{-15} F,
6	$R_x(-)$	4.79990 MΩ
7	$C_x(-)$	7.3772×10^{-15} F
8	R_i	591 Ω
9	3 dB Bandwidth	201.4719 MHz
10	Power consumption	2.47 mW

3.9 References

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Chapter 4

Electronically-tunable grounded/floating inductance simulators using z-copy CFCC

A new electronically-tunable grounded and floating inductance simulators employing Z-copy current follower current controlled conveyor (ZC CFCCC) and one grounded capacitor have been presented and workability has been verified by some illustrative examples.

4.1 Introduction[5]

Over the past several years, many new active building blocks (ABBs) have been used to implement various signal processing/generation functions including the simulation of inductors, realization of universal biquadratic filters, sinusoidal oscillators and non-sinusoidal waveform generators [1]-[10]. The various building blocks which have been prominently employed in the past for simulating the inductors include, Operational Transresistance Amplifier (OTRA) [11],[12], Differential Voltage Current Conveyor (DVCC) [13], Current Differencing Buffered Amplifier (CDBA) [14], Current Differencing Transconductance Amplifier CDTA [15], Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA) [16,17], Voltage Differencing Transconductance Amplifier (VDTA) [18], [19], Voltage Differencing Current Conveyor (VDCC) [20], [21], Voltage Differencing Buffered Amplifier (VDBA) [22], Current Controlled Current Conveyor Transconductance Amplifier (CCCCTA) [23], Current Controlled Current Differencing Transconductance Amplifier (CCCDTA) [24], [25], Current Controlled Current Feedback Amplifier (CC-CFA) [26], Current Follower Transconductance Amplifier (CFTA) [27], Current Controlled Current Follower Transconductance Amplifier (CCCFTA) [28] and Current Backward Transconductance Amplifier (CBTA) [29].

In the following, we present new electronically-tunable, grounded/floating inductance simulators realized with the active building block, named the Z-copy Curent Follower Current Controlled Current Conveyor (ZC-CFCCC). To the best knowledge of the authors, ZC-CFCCC has not been put to use yet for the realization of electronically-controllable simulated inductors.

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4.2 Electronically-tunable grounded inductor

A Current Follower Multiple-output Current Conveyor (CF-MOCC) was introduced in [1] . In the present work, we have modified its structure by taking out an additional Z copy of the input current and used a current controlled conveyor in its second stage to realize a ZC-CFCCC. Thus, the ZC-CFCCC is a five-port active building block characterized by the following terminal equation

$$\begin{bmatrix} V_p \\ V_i \\ I_z \\ I_{zc} \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 & 0 \\ 0 & -R_i & 1 & 0 & 0 \\ 1 & 0 & -Y_z & 0 & 0 \\ 1 & 0 & 0 & -Y_{zc} & 0 \\ 0 & 1 & 0 & 0 & -Y_x \end{bmatrix} \begin{bmatrix} I_p \\ I_i \\ V_z \\ V_{zc} \\ V_x \end{bmatrix} \tag{4.2.1}$$

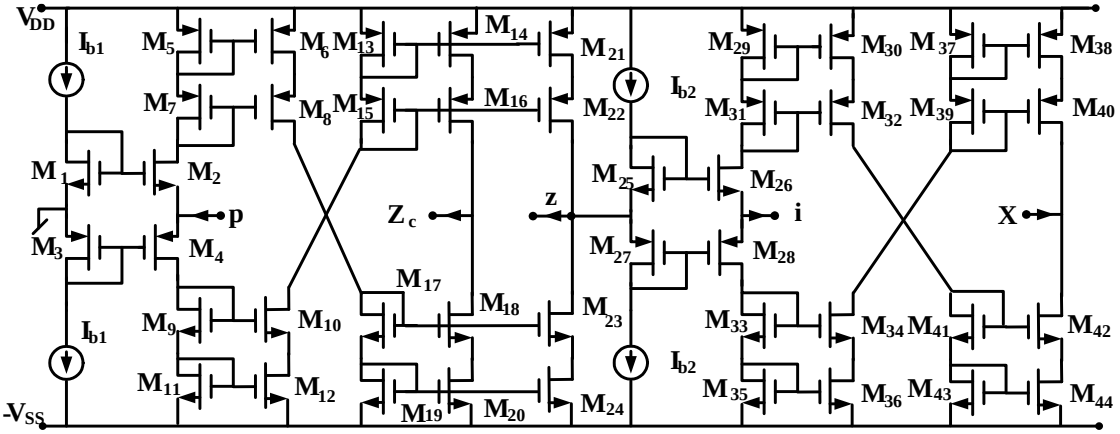


Figure 4.2.1 An exemplary CMOS implementation of the ZC-CFCCC

where R_p represents the input resistances of the p port while R_i represents the output resistance of the voltage buffer implemented between port z and port i. Y_z, Y_{zc} and Y_x each comprise a parallel combination of a resistor and a capacitor and represent the parasitic admittances associated with the ports z, zc and x. When implemented in CMOS hardware such as the one shown in Fig. 4.2.1, the values of R_p and R_i are given by

$$R_p = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b1}}}, R_i = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b2}}} \tag{4.2.2}$$

Thus, $R_{p,}$ and R_i can be controlled by external DC bias currents $I_{b1}$and I_{b2} [23], [24], [28].

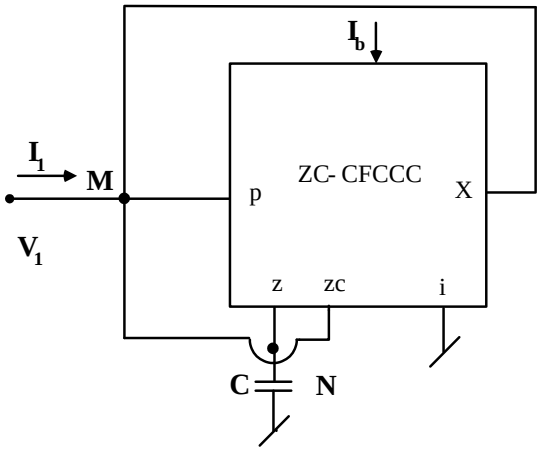


Fig.4.2.2 The proposed new electronically-tunable grounded inductor

Consider now the proposed new realization of the electronically-tunable grounded inductor which is shown in Fig.4.2.2. A straight forward analysis of this circuit, using the port relationships of the ZC-CFCCC given in (4.2.1), gives the input impedance of the circuit as (when Y_z, Y_{zc} and $Y_{x,}$ the parasitic admittances at ports z, zc and i are taken to be zero),

$$Z_i = sR_pR_iC \tag{4.2.3}$$

$$where\ R_p = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right)I_{b1}}}\ \text{and}\ R_i = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right)I_{b2}}}$$

If I_{b1}= I_{b2}= I_b, then the simulated inductance value is given by:

$$L_s = C\frac{1}{\left(8\mu_n C_{ox}\left(\frac{W}{L}\right)I_b\right)} \tag{4.2.4a}$$

It may be noted here that both R_p as well as R_i need not be equal. Availability of two external currents for realization of a given value of inductance results in more flexibility in selecting these current sources. In case only one current is available to control the value of the simulated inductor then the other resistor required will be a fixed-valued resistor. Therefore, the realized inductance can be varied electronically over a wider range.

It may be noted here that both R_p as well as R_i need not be equal. Availability of two external currents for realization of a given value of inductance results in more flexibility in selecting these current sources. In case only one current is available to control the value of the simulated inductor then the other resistor required will be a fixed-valued resistor. Therefore, the realized inductance can be varied electronically over a wider range.

On the other hand, if these parasitic elements are taken into consideration then the impedance Z_{in} is given by

$$Z_{in}(j\omega) = R_s + j\omega L_s \tag{4.2.4b}$$

$$R_s(\omega) = \frac{\omega^2(a_1b_1 - a_0b_2) + a_0b_0}{\omega^4 b_2^2 + \omega^2(b_1^2 - 2b_0b_2) + b_0^2} \tag{4.2.4c}$$

$$L_s(\omega) = \frac{-a_1b_2\omega^2 + (a_1b_0 - a_0b_1)}{\omega^4 b_2^2 + \omega^2(b_1^2 - 2b_0b_2) + b_0^2} \tag{4.2.4d}$$

and the quality factor

$$Q(\omega) = \frac{\omega\left[-a_1b_2\omega^2 + (a_1b_0 - a_0b_1)\right]}{\omega^2(a_1b_1 - a_0b_2) + a_0b_0} \tag{4.2.4e}$$

$$\text{where } a_1 = R_pR_iR_xR_zR_{zc}(C + C_z); a_0 = R_pR_iR_xR_{zc}; b_2 = R_pR_iR_xR_zR_{zc}(C + C_z)(C_x + C_{zc}); \tag{4.2.4f}$$
$$b_1 = \left[R_pR_iR_z(C + C_z)(R_x + R_{zc}) + R_pR_iR_xR_{zc}(C_x + C_{zc})\right]; b_0 = R_pR_i(R_x + R_{zc}) + R_xR_zR_{zc}.$$

4.3 Electronically-tunable floating inductor

From the circuit of the proposed electronically tunable grounded inductor, it is observed that the configuration implements an active gyrator with its input port being the node M and the output port being the node N. A straightforward analysis of this gyrator circuit, results in the following short circuit admittance matrix:

$$[Y]=\begin{bmatrix} 0 & \frac{1}{R_i} \\ -\frac{1}{R_p} & 0 \end{bmatrix} \tag{4.3.1}$$

Therefore, using two such active gyrators and one grounded capacitor embedded between them, an electronically-tunable floating inductor (FI) can be realized as shown in Fig.4.3.1, for which the short circuit admittance matrix of the FI is found to be

$$[Y]=\frac{1}{sC}\begin{bmatrix} \frac{1}{R_iR_p} & -\frac{1}{R_i^2} \\ -\frac{1}{R_p^2} & \frac{1}{R_iR_p} \end{bmatrix}=\frac{1}{sCR^2}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{4.3.2}$$

$$where\ \ R_p=R_i=R=\frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right)I_b}}$$

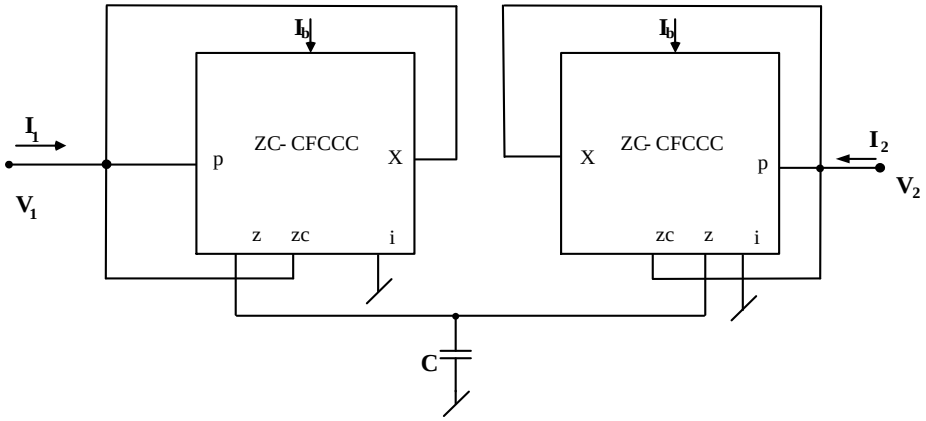


Fig.4.3.1 The proposed new electronically-tunable floating inductor

Thus, the value of the realized floating inductance can be varied by changing the external bias current I_b. It may be noted that this can be implemented quite easily by supplying equal DC bias currents to the two ZC-CFCCCs unlike the constraints imposed by passive component matching as prevalent in many of the classical floating inductance simulation circuits using op-amps. If the parasitic admittances associated with ports z, zc and x are taken into account then the non-ideal short circuit admittance parameters (for $I_{b1}= I_{b2}= I_b$, $R_i=R_p=R$) are found to be

$$y_{11}=\frac{\left(\frac{1}{R_{EQ}^2}+\frac{1}{R_{EQ}R_z}+\frac{1}{R^2}\right)+\left(2\frac{C_P}{R_{EQ}}+\frac{C}{R_{EQ}}+\frac{C_P}{R_z}+\frac{C_z}{R_{EQ}}\right)s+\left(C_P^2+C_PC+C_PC_z\right)s^2}{\left(\frac{1}{R_{EQ}}+\frac{1}{R_z}+\left(C_P+C_z+C\right)s\right)} \tag{4.3.3}$$

$$y_{12}=\frac{-\frac{1}{R^2}}{\left(\frac{1}{R_{EQ}}+\frac{1}{R_z}+\left(C_P+C_z+C\right)s\right)}=y_{21} \tag{4.3.4}$$

$$y_{22}=\frac{\left(\frac{1}{R_z^2}+\frac{1}{R_{EQ}R_z}+\frac{1}{R^2}\right)+\left(2\frac{C_z}{R_z}+\frac{C}{R_z}+\frac{C_P}{R_z}+\frac{C_z}{R_{EQ}}\right)s+\left(C_z^2+C_zC+C_PC_z\right)s^2}{\left(\frac{1}{R_{EQ}}+\frac{1}{R_z}+\left(C_P+C_z+C\right)s\right)} \tag{4.3.5}$$

$$\text{where } R_{EQ}=R_{zc}\parallel R_x, C_P=C_{zc}+C_x, R_s=\frac{R_pR_i}{R_z} \text{ and } L_s=R_pR_i\left(C+C_z\right) \tag{4.3.6}$$

The expressions for the y-parameters, as above, appear to be quite formidable and do not lend themselves to meaningful interpretations directly. We have, therefore, measured the y-parameters of the circuits using PSPICE simulations and plotted their frequency responses along with the theoretical plot of the equations (4.3.3 -4.3.5) in MATLAB in the next section.

4.4 SPICE simulations, application examples and results

The CMOS implementation of the proposed ZC-CFCCC using 0.18 micron TSMC process technology has been used to verify the workability of the circuits presented in this chapter. Measured values of the characterizing parameters of the ZC-CFCCC given in equation (4.2.1) at DC bias voltage ± 2.5 V and DC bias currents 40 µA are given in Table 4.4.1, whereas the aspect ratios of the various MOSFETs are shown in Table 4.4.2. The measured value of THD of an amplifier configured with ZC-CFCCC when the input current was varied between 20-80 µA was found to vary between 0.75% to 3.5% at 1 MHz (when z and i terminals are terminated with equal resistance of 10 KΩ).

Table 4.4.1 Characteristic parameters of ZC-CFCCC

S.No.	Parameter	Value
1	R_p	591Ω
2	R_z	4.9178 MΩ
3	C_z	$6.3234x10^{-14}$ F,
4	R_{zc}	4.9178 MΩ
5	C_{zc}	$7.2123x10^{-15}$ F,
6	R_x	4.79990MΩ
7	C_x	$7.3772 x10^{-15}$ F
8	R_i	591 Ω
9	Power consumption	2.47mW
10	Linear range of current transfers I_p/I_z, I_p/I_{zc} and I_i/I_x (mA)	-0.8 to +0.75 with gain 1.00049
11	Linear range of voltage transfers(V) V_z/V_i	-3.0 to +3.0 with gain 0.9882
12	3dB Bandwidth (MHz) (i)I_p/I_z,and I_p/I_{zc} (ii) I_x/I_i (iii) V_i/V_z	 527 1215.8 2860

Table 4.4 2 Aspect ratios of MOSFETs used in ZC-CFCCC realization

MOSFETs	W/L (μm/μm)
M_1, M_2, M_{25}, M_{26}	25/0.25
M_3, M_4, M_{27}, M_{28}	50/0.25
M_5 - M_{24}, M_{29} -M_{44}	2.5/0.25

The proposed grounded inductor circuit was simulated with C = 1nF for different values of bias current I_b starting from 0.01 μA. to 200 μA. The variation of inductance with bias current is shown in Fig.4.4.1, which is similar to the variation of inductance with bias current for other electronically tunable lossless grounded inductance circuits such as the one given in [20]. It was found that inductance value could be varied from 998 H to 135 μH, over the above range. The typical value of inductance for a bias current of 40 μA was found to be 350 μH while the power consumption was 2.47 mW.

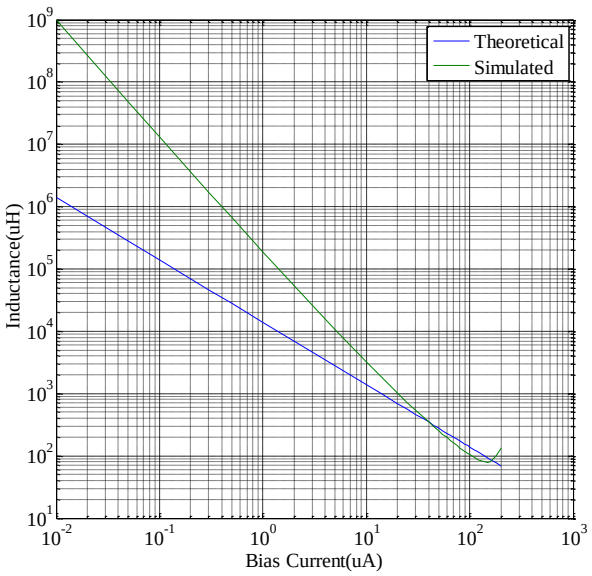
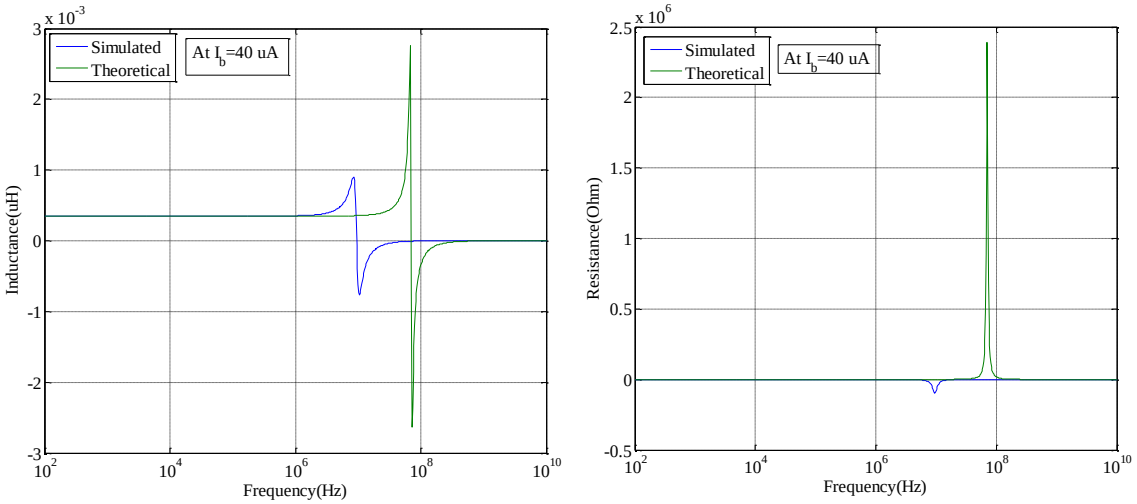


Fig.4.4.1 Variation of inductance with bias current



(a) (b)

Fig.4.4.2 Frequency response of simulated lossless grounded inductor (a)Variation of inductance value with frequency (b)Variation of parasitic resistance with frequency

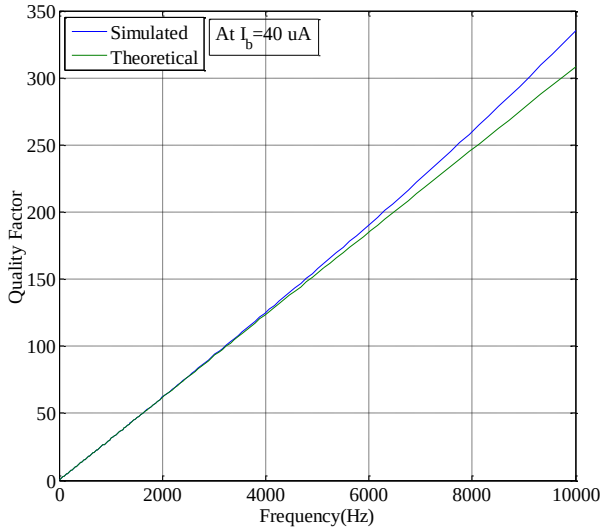
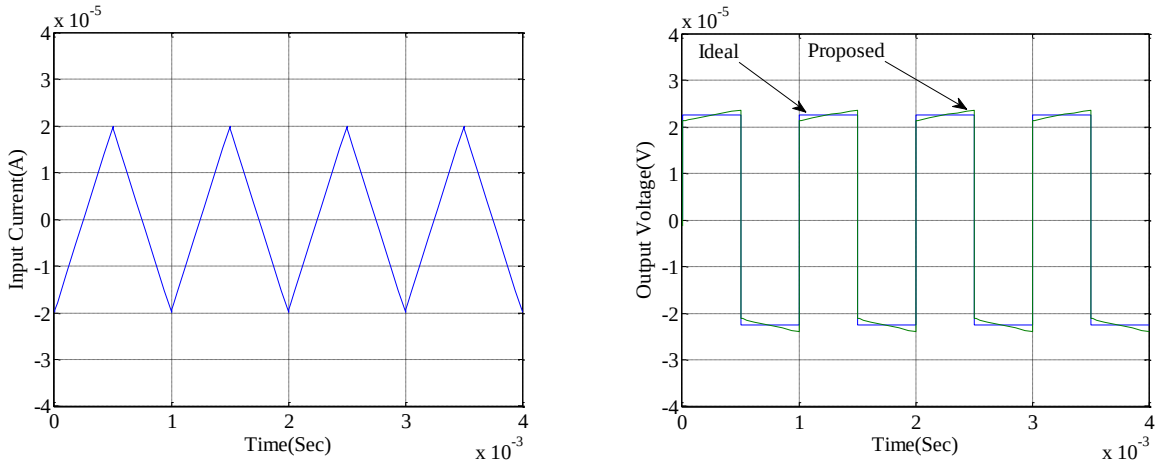


Fig.4.4.3 Variation of quality factor with frequency

The frequency response of the simulated inductor was also determined in PSPICE (for I_b= 40 µA) and is shown in Figure 4.4.2 (L =350.04 µH at a frequency of 35.3 KHz). Independent simulations have shown that the value of the inductance remains within a tolerance value of 10% up to a frequency of 2.99 MHz. We have also superimposed on the frequency response the theoretical plots as obtained from equations (4.2.4c) and (4.2.4d). From the frequency response plots it is observed that the inductance value remains nearly constant only upto a particular frequency. This is corroborated by the behavior of simulated lossless grounded inductors realized with other active building blocks [15] - [18]. Though, the parasitic resistance associated with the simulated inductor becomes negative at higher frequencies the application circuits have not shown any unstable behavior. The quality factor of the simulated grounded inductor (for bias current of 40 µA) was also measured and found to be 335 at 10 KHz. Figure 4.4.3 shows the variation of quality factor with frequency. The simulated results agree quite well with the theoretical ones. The discrepancy between theoretical and simulated results mainly stems from non-ideal gain and parasitic impedance effects of the ZC-CFCCC.

An input current with a triangular waveform (20 µA amplitude and 1 KHz frequency) was applied to the proposed inductor (46.45µH). The output voltage, a square wave (22 µV at 1 KHz) as shown in Figure 4.4.4, was obtained which further confirmed the workability of the electronically- tunable grounded inductor.



(a) (b)

Fig.4.4. 4 Time domain analysis of the proposed grounded inductor: (a)Input current waveform (b) output voltage waveform

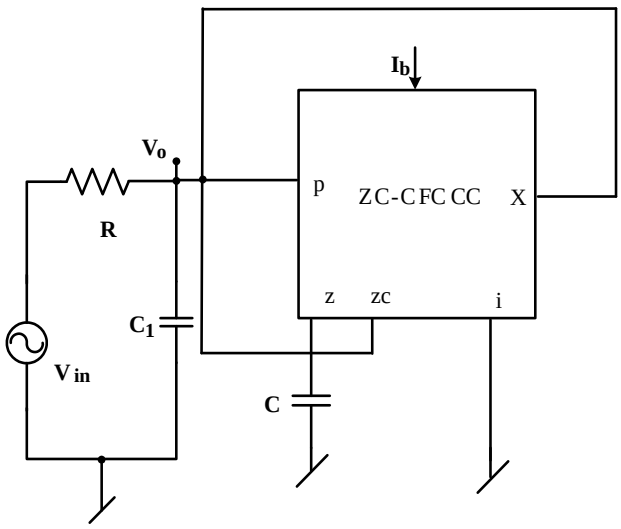


Fig.4.4.5 Tunable second order RLC band pass filter

A second order band pass filter shown in Fig.4.4.5 was used to verify the tunability of the pole frequency with bias current. The pole frequency and the bandwidth of the filter are given by: pole frequency $f_o = \frac{1}{2\pi\sqrt{LC_1}}$ and bandwidth $BW = \frac{1}{2\pi RC_1}$.

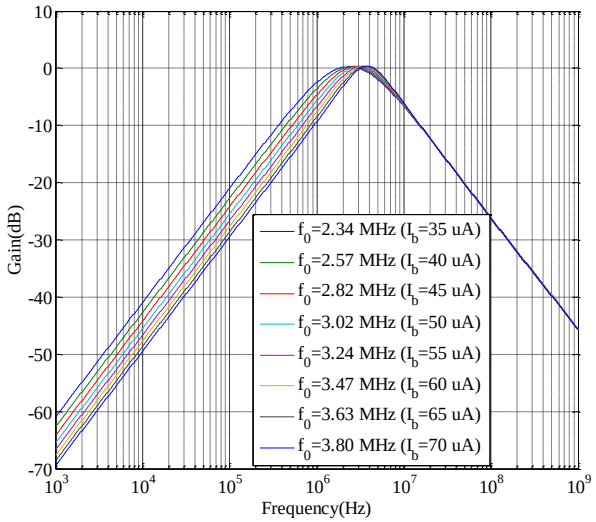


Fig. 4.4.6 Frequency response of second order BPF for different values of bias current

The band pass filter was designed with following component values: R=3 kΩ, C = 1 nF, C_1 = 10 pF and bias current was varied from 35 µA to 70 µA to vary the pole frequency without affecting the bandwidth. Fig.4.4.6 shows the frequency response of the band pass filter with different values for the pole frequency. These results are in close agreement with the theoretical values ($f_0 \propto \sqrt{I_b}$) with the maximum error in the pole frequency being less than 10%. The maximum error in bandwidth has been found to be about 2%. The THD in the output was also measured and found to lie within 0.3-2.4% when the input amplitude was varied in the range of 10-150 mV.

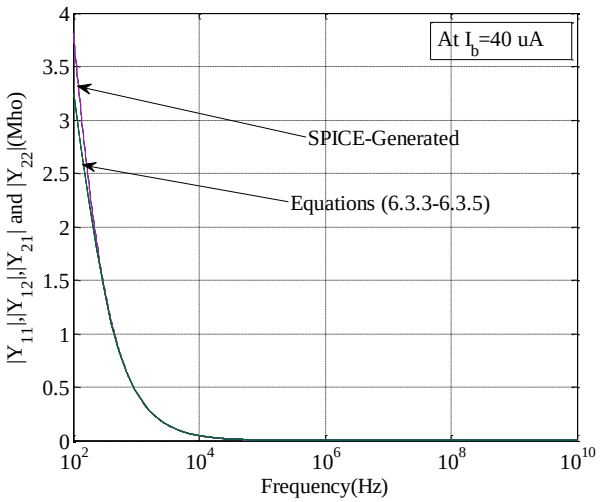


Fig.4.4.7 Frequency response of the y parameters of the simulated floating inductor

The frequency response of the floating inductor was determined through PSPICE simulations to find its usable frequency range. Fig.4.4.7 shows the frequency response of the short circuit admittance parameters. We have also superimposed the frequency response as computed from equations (4.3.3-4.3.5). There is a very close agreement between these three plots. Independent simulations have indicated that the floating inductor can be used up to a frequency of 2.94 MHz (at I_b=40 µA), the simulated inductance was within 10% of the designed value of 350 µH while the associated resistance was varying between less than 142 mΩ to −579.20 Ω up to a frequency of 2.94 MHz.

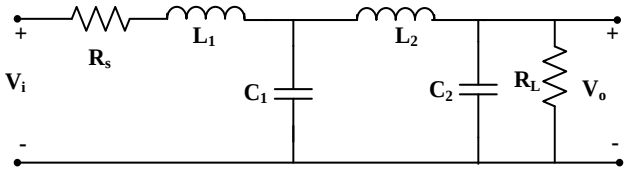


Fig. 4.4.8 Prototype fourth order low pass Butterworth filter

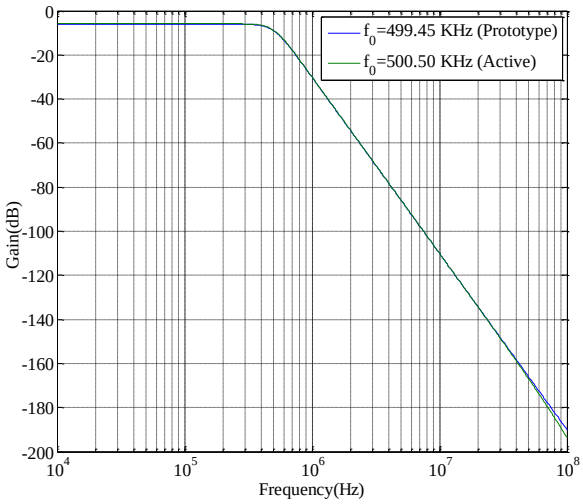


Fig.4.4.9 Frequency response of the fourth order low pass Butterworth filter

We have used the proposed floating inductor to implement a fourth order Butterworth low pass filter as shown in Fig.4.4.8 Starting from the nominal values of the components for the normalized low pass filter 1 Hz as: $R_s = R_L = 1\ \Omega$, $L_1 = 0.7654$ H, $L_2 = 1.8478$ H, $C_1 = 1.8478$ F and $C_2 = 0.7654$ F [30], after appropriate frequency and impedance scaling we get the following values of passive components for the filter cut-off frequency of 500 KHz: $R_S = R_L =$ 1 kΩ, , $C_1 = 0.5884$ nF, $C_2 = 0.2437$ nF, $L_1 = 0.2437$ mH (C =1 nF, $I_b = 51.46$ µA) and $L_2 =$ 0.5884 mH (C = 1 nF, $I_b = 28.37$ µA). This finally resulted in a fouth order active filter structure using all grounded capacitors, as preferred for IC implementation. Frequency response of the resulting fourth order low pass Butterworth filter is shown in Fig.4.4.9. The value of the cut-off frequency found from the simulation was 500.50 KHz, showing a very close agreement with the theoretical value of 500 KHz. The THD in the output was also measured when the amplitude of the input voltage was varied between 10 mV- 150 mV and found to vary between 0.2-7%.

To study the effect of mismatches in the component values within the floating inductors on the performance of the circuit of the fourth-order low pass Butterworth filter, Monte Carlo simulations have been carried out by allocating 1% tolerances to the component values

(capacitors C=1nF) within both the floating inductors and performing 100 runs. The results for the 1% tolerance have been shown in Fig.4.4.10. The value of the simulated cut-off frequency was found to be 500.50 KHz and Monte Carlo analysis shows that median value of cut-off frequency is f_0=500.21 KHz, which indicates that the mismatch in the component values within the proposed floating inductors do not have large effect on the realized cut-off frequency.

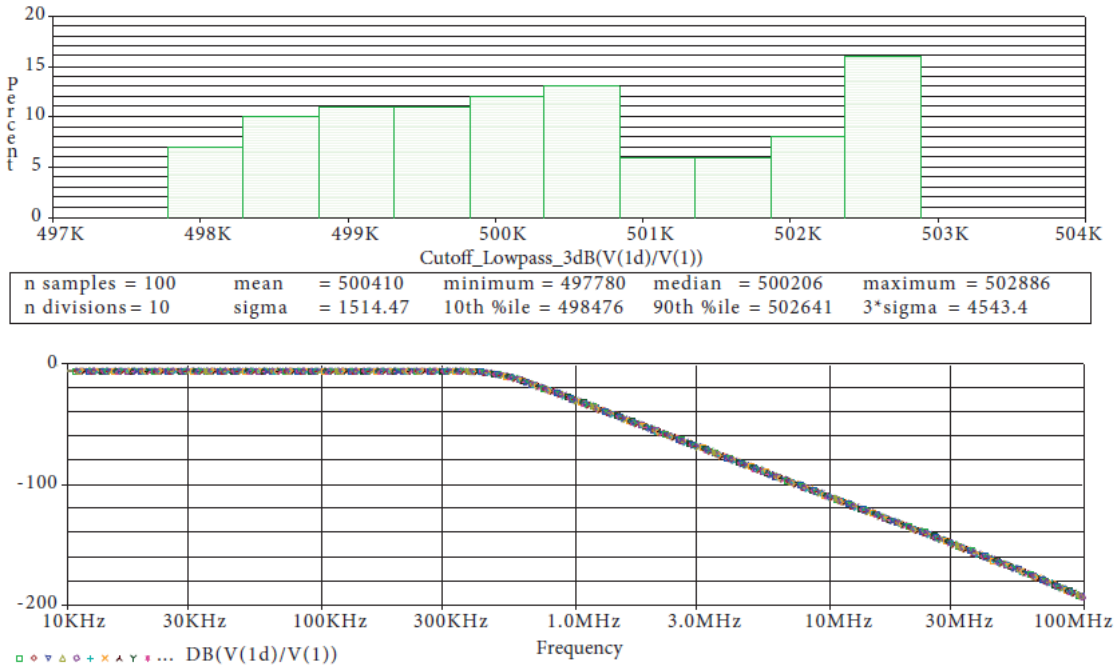


Fig.4.4.10 Simulation results of Monte Carlo analysis for fourth order low pass Butterworth filter

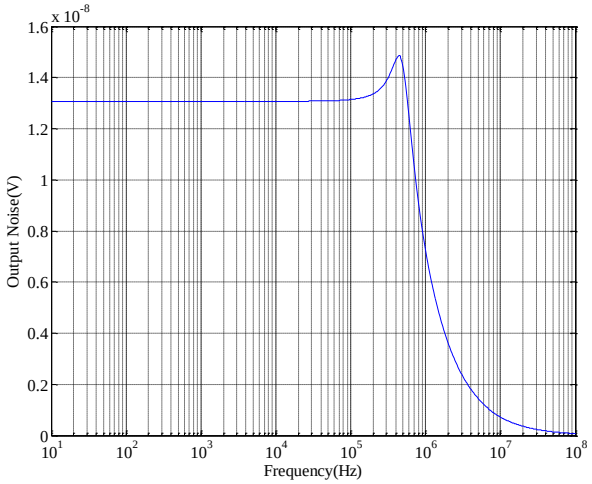


Fig.4.4.11 output noise variation for fourth order low pass Butterworth filter

PSPICE noise analysis has also been performed on the fourth order low pass filter and variations in the output noise have been shown in Fig.4.4.11

The PSPICE simulation results presented in this section thus establish the workability and applications of the proposed new inductance simulators using ZC-CFCCC.

4.5 Comparison with previously published circuits

A comparison of the various salient features of the proposed configurations as compared to other previously known lossless grounded and FI simulators realized with synthetic active building blocks is now in order and has been presented in Table 4.5.1. It is observed from the above table that the proposed circuits, with the exceptions of the circuits given in [18,19, 28], are the only circuits which realize an electronically tunable *lossless* grounded inductor employing a single active building block, no passive resistors, and a single grounded capacitor and do not require any passive component matching constraint. It may be mentioned here that because of the terminal equations of the ZC-CFCCC, CC-CDTA, and CC-CCTA being somewhat similar, the proposed inductance simulation circuits may appear to be somewhat similar to the circuits proposed in [23,25], where CC-CCTA and CC- CDTA were used as ABBs. On the other hand, yet another building block proposed in [1], namely the CDCC [31], [32], can also be configured as a ZC-CFCCC if we do not use one of its input current terminals and use a current-controlled conveyor (instead of CCII) in the second stage. The grounded inductance simulators used here can directly be used in the simulation of LC ladders in contrast to the lossy inductance simulators realized with other active building blocks of recent origin [34–44].

4.6 Concluding remarks

In this chapter, new electronically-tunable, lossless grounded and floating inductance simulation circuits using the ZC-CFCCC as active element were proposed. The proposed

circuits employ only a single ZC-CFCCC for grounded inductance simulation and two ZC-CFCCCs for floating inductance simulation along with a single grounded capacitor as preferred for IC implementation. Thus, the new circuits provide a number of advantageous features simultaneously, such as use of a canonic number of active and passive elements, electronic tunability by means of external bias currents, complete absence of passive component matching, and employment of a single grounded capacitor, as preferred for IC implementation. For simulation of floating inductance, the only constraint required is the equality of the two bias currents, which can be easily met by using current copier cells. The workability of the new propositions as well as their two typical application circuits has been verified through PSPICE simulations using 0.18-µm TSMC CMOS technology parameters. It is believed that the proposed ZC- CFCCC-based electronically tunable inductance simulators add new alternatives to the existing repertoire of synthetic ABB-based inductance simulators, as shown in Table 4.5.1. This table also contains modified CFOAs and modified inverting second-generation current conveyor-based inductance simulators [45–48] but does not include circuits based upon traditional current conveyors (see those in [33], [49–51] and the references cited therein).

Table 4.5.1 Comparison with other previously published lossless grounded and floating inductors realized with synthetic active building blocks

Ref.	Type*	Number of ABB	Number of resistors	Number of capacitors	Whether free from passive component matching	Tunability	Technology	Power Supply	Power Dissipation
[11]	G	2:OTRA	5	1F	No	No	Discrete (AD844)	±10V	NA
[12]	G	1:OTRA	3	2F	No	No	0.5µm/ AD844	±1.5V/±5V	0.809/260 mW
[13]	F	2:DVCC	2	1G	Yes	No	0.18µm	±1.25V	NA
[14]	F	3/4 :CDBA	4[VCR]	1G	Yes	Yes	0.5µm	±2.5V	NA
[15]	G	2:CDTA	0	1G	Yes	Yes	0.5µm	±2.5V	NA
	F	3:CDTA	0	1G	Yes	Yes	0.5µm	±2.5V	NA
[16]	G	2:VD-DIBA	0	1G	Yes	Yes	Discrete ((AD844)+ CA3080))	±1V	62.5mW
	F	3:VD-DIBA	0	1G	Yes	Yes	Discrete ((AD844)+ CA3080))	±1V	62.5mW
[17]	G	1:VD-DIBA	1	1G	Yes	Yes	0.35µm	±2V	NA
	F	2:VD-DIBA	1	1G	No	Yes	0.35µm	±2V	NA
[18]	G	1:VDTA	0	1G	Yes	Yes	0.18µm	±0.9V	NA
	F	2:VDTA	0	1G	Yes	Yes	0.18µm	±0.9V	NA
[19]	F	1:ZC-VDTA	0	1G	Yes	Yes	0.18µm	±0.9V	1.25mW
[20]	G	1:VDCC	1	1G	Yes	Yes	0.18µm	±0.9V	0.869mW
[21]	F	1:VDCC	1	1G	Yes	Yes	0.18µm	±0.9V	NA
[22]	G	1:VDBA	1	1F	Yes	Yes	Discrete (OPA860)	±5V	NA
[23]	G	1:CCCCTA	0	1G	Yes	Yes	0.35µm	±1.5V	899 µW

[24]	F	1:CCCDTA, 2:VB	0	IG	Yes	Yes	0.35µm	±1.5V	1.48mW
[25]	F	1:CCCDTA, 2:VB	0	1G	Yes	Yes	Bipolar ALA400	±1.5V	1.23mW
[26]	G	2:CC-CFA	0	1G	Yes	Yes	(ALA400+ 0.35µm)	±1.5V	4.16mW
[27]	F	3:CFTA	0	1G	Yes	Yes	Bipolar ALA400	±1.5V	NA
[28]	G	1:CCCFTA	0	1G	Yes	Yes	0.5 µm	±2.0V	NA
[29]	F	2:CBTA	2	1G	Yes	Yes	0.25µm	±2.5V	NA
[45]	F	1:MCFOA	2	1G	Yes	No	0.35µm	±1.5V	NA
[46]	G	1:New CFOA	2	1F	Yes	No	Discrete	±15V	NA
[47]	G	1:CFOA-	2	1F	Yes	No	0.13µm	±6V/0.75V	890µW
[48]	G	1:MICCII−	2	1F	No	No	0.35µm	±2.5V	17.6mW
Proposed	G	1:ZC-CFCCC	0	1G	Yes	Yes	0.18µm	±2.5V	2.47mW
Proposed	F	2: ZC-CFCCC	0	1G	Yes	Yes	0.18µm	±2.5V	4.94mW

*F: Floating, G: Grounded

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Chapter 5

Fully-Differential Current-Mode Higher Order Filters Using All Grounded Passive Elements

A methodology has been developed to realize n^{th} order ($n \geq 3$) fully-differential current-mode filters using Current Differencing Current Conveyors (CDCC) which results in circuits employing *all grounded passive elements*. The cut-off frequency of the realized filter can be electronically tuned when all the grounded resistors associated with the integrators are implemented by identical CMOS grounded voltage-controlled-resistors driven by a common control voltage.

5.1 Introduction

Higher order RC active filters (of order **n** ≥3) are useful as anti-aliasing filtering in data converters and also find use in display of radar target tracks and high quality audio applications. When realized in fully-differential form, they have the advantage of lower harmonic distortion, higher dynamic range and immunity to power supply induced common mode noise. A large number of research papers have been published in the past on single-ended biquads and higher order filters (for instance, see [1]-[20] and the references cited therein) which have also been documented in a number of recent books (for example, see [21],[22]).On the other hand, fully-differential biquads and fully-differential higher order filters have also been investigated by several researchers, for instance, see [23]-[53].The works mentioned in references [23], [28]-[30],[33]-[35], [37],[40], [41], [43], [45]-[48], [51], [52] deal with fully-differential voltage-mode (VM)/current-mode (CM) higher order filters.

To put the work presented in this chapter in right perspective, it appears necessary to present a brief overview of the earlier works on the design of fully-differential VM and CM higher order filters. In this context, it is found that many different active building blocks (ABB) have been employed in the past to realize fully-differential filters exhibiting different properties. The ABBs employed so far include Voltage–mode operational amplifier [38], Dual output Operational Amplifier (Dual OA) [34], [40], [43], [47], four-input-two-output OA (four-input two-output Operational amplifier) [25], [52], Operational Transconductance Amplifier (OTA) [23], [28], [29], [33], [35], [37], [51], Fully Differential Second Generation Current Conveyor (FDCCII) [24], [39], Fully Balanced Differential Difference Amplifier (FBDDA) [26], Fully Balanced Four-terminal Floating Nullor (FBFTFN) [27], Current mode Differential Wave-port Terminator [30], Fully Differential Current Feedback Operational Amplifier (FDCFOA) [31], Differential Input Balanced Output Current Operational Amplifier (DIBOCOA) [32], Multi-output Second Generation Current Conveyor (MOCCII) [36], Current-controlled Fully

Balanced Second Generation Current Conveyor (CFBCCII) [41], [45], Fully Differential Current Follower (FD-CF) [42], [44], [46], [53], Multi-output Transconductance Amplifier (MOTA) [44], [53], Differential Differential Amplifier (DDA) [48], Multi-output Current Follower (MO-CF), Dual Output Current Follower (DO-CF), Digitally Adjustable Current Amplifier (DACA) [49] Current Differencing Current Conveyor (CDCC) [see chapter 2], Fully Differential Current Follower (FD-CF), Digitally Adjustable Current Amplifier (DACA) and Multi-output Transconductance Amplifier (MOTA) [53]. Table 5.1.1 summarizes the salient features of the earlier works done on the higher-order fully-differential filters realized with the various ABBs mentioned above.

Table 5.1.1 An overview of fully-differential higher order filter structures using different ABBs

Ref.	No of ABBs	Order and type	R count	C count	All Grounded passive elements	Electronic Tunability	Technology	Supply Voltage	Power Dissipation
[23]	OTA: 10 BUFFER: 2	7; VM (Elliptic)	-	13	No	Yes	1 µm	±2.5V	75mW
[28]	OTA:8	4;VM (Butterworth)	-	8	Yes	Yes	0.35µm	±2.7V	NA
[29]	OTA:5	5;VM (Elliptic)	32	18	No	Yes	0.18um	0.5V	NA
[30]	WPT:6	3; CM (Elliptic)	-	6	No	Yes	0.35µm	±2.5V	NA
[33]	OTA:9	7;VM (Equi-ripple with gain boost)	-	14	Yes	Yes	0.25µm	2V	216mW
[34]	Dual OA:4	4;VM (Chebyshev)	18 (VCR)	8	No	Yes	0.35µm	3.3V	16mW
[35]	OTA:3	3;CM (Butterworth)	-	6	Yes	Yes	0.35µm	1.5V	NA
[37]	OTA:7	3;CM (Butterworth)	-	6	Yes	No	0.18um	1.8V	16.77mW
[40]	Dual OA:6	6;VM (Chebyshev)	26	12	No	Yes	0.18um	±1.8V	NA
[41]	CFBCCII:4	4;CM (Butterworth)	-	8 (2n)	Yes	Yes	0.35µm	±1.65V	NA
[43]	Dual OA:10	5;VM (Complex Chebyshev)	64	20	No	Yes	0.18um	1.8V	NA
[45]	CFBCCII:7	3; CM (Elliptic)	8	6	Yes	Yes	0.35µm	±1.65V	22mW
[46]	FD-CF:4	4;CM (Butterworth)	6	5 (n+1)	No	No	NA	NA	NA
		4;CM (Butterworth)	5	6 (n+2)	No	No	NA	NA	NA

[47]	Dual OA:6	6;VM (Inverse Chebychev)	36	12	No	Yes	0.13µm	1.5V	9.45mW
[48]	DDA:2	5;VM (Bessel)	10	20	No	Yes	0.18µm	3.3V	1mW
	DDA:3	7;VM (Bessel)	14	28	No	Yes	0.18 µm	3.3V	1.5mW
[51]	OTA:2n	VM(High Even order Biquadratic)	-	2n	Yes	No	0.35µm	±2V	NA
[52]	Four-input-Two-output OAs:3	6;VM (Sallen-Key)	12	12	No	Yes	0.35µm	1.2V	12.6mW

NA: Data not available

Although Operational Transconductance Amplifiers (OTA) and Current Conveyors (CC) are commercially available as off-the-shelf ICs whereas a CDCC is not and therefore, the comparison of the proposed CDCC-based structure with those employing OTAs and CCs may appear to be somewhat unjustified, however, for the sake of giving a complete picture the same have also been included in Table 5.1.1. From Table 5.1.1, it is observed that earlier known fully-differential higher order filters suffer from one or more of the following drawbacks:

(i) Use of either more than double the number of capacitors per filter pole [29], [43], [48] or twice the number of capacitors per filter pole [28], [30], [33]-[35], [37], [40], [41], [45], [47] or use of more than one capacitor per filter pole but less than double the number of capacitors per filter pole [23], [46]

(ii) Use of *floating* passive elements [23], [29], [30], [34], [40], [43], [46]- [48], [52]

(iii) Non-availability of electronic tuning of the cut-off frequency [37], [46], [51].

It is also observed from Table 1.1 that except in the works [41], [46], [51], no other general methodology for the realization of an n^{th} order fully-differential CM filters appears to have been reported *explicitly* in the open literature earlier.

We now present in Table 5.1.2 the salient features of the fully-differential CM filters realized with the general methodologies proposed in [41], [46], [51], *vis-à-vis* those realizable with the methodology being proposed in this chapter, to put the proposed methodology/circuits in right perspective.

From Table 5.1.2, it is revealed that the CDCC-based general methodology to realize a fully-differential CM higher order filter being presented here would provide the following features *simultaneously* which are not available simultaneously in any of the previously known methods/circuits presented in Table 5.1.2.

Table 5.1.2 Comparison of the proposed methodology with the existing general methodologies for n^{th} order fully-differential CM filters.

Ref.	ABB count	Order and type (n)	R count	C count	All Grounded passive elements	Electronic Tunability	Technology	Supply Voltage	Power Dissipation
[41]	CFBCCII:n	n (Butterworth)	-	2n	Yes	Yes	0.35µm	±1.65V	NA
[46]	FD-CF:n	n (Butterworth)	n+2	n+1	No	No	NA	NA	NA
		n (Butterworth)	n+1	n+2	No	No	NA	NA	NA
[51]	OTA:2n	n (Cascaded-biquads)	-	2n	Yes	No	0.35µm	±2V	NA
Proposed	CDCC:2n	n (Butterworth)	3n	n	Yes	Yes	0.18µm	±2.5V	26.9m W

NA: Data not available

(i) use of all grounded passive elements

(ii) employment of only one capacitor per pole and

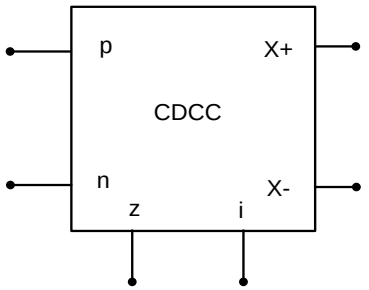
(iii) facilitation of electronic tunability of the cut off frequency.

It is worth mentioning that the methodology employed here may appear to be somewhat similar to the one proposed earlier in [41] but in contrast to the structures proposed in [41] which use double the number of capacitors, we use no more than one capacitor per pole.

5.2 Realization of CDCC-based fully-differential current-mode higher order filters

CDCC [54] is a six-terminal ABB whose symbolic representation and the instantaneous port relations are shown in Fig. 5.2.1. The current at the 'z' terminal is the difference of the two input currents and the potential at the terminal 'i' tracks the potential at the terminal 'z'. Two

complementary currents at the output terminals ‘x+’ and x- are available which are copies of the current leaving the ‘i’ terminal.



$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_i \end{bmatrix}$$

Fig. 5.2.1 Symbolic notation and port-relations of the CDCC

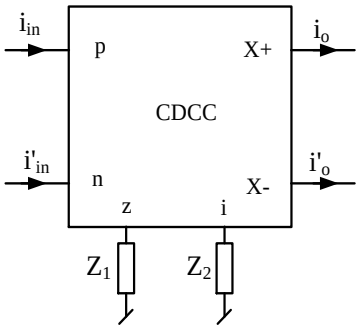


Fig. 5.2.2 The general configuration to realize a scalar, lossless integrator or lossy integrator

Consider now the CDCC block of Fig. 5.2.2 whose z and i terminals are terminated into impedances Z_1 and Z_2. By straight forward analysis, the output currents are given by

$$i_o = -i_o^{'} = \frac{Z_1}{Z_2}\left(i_{in} - i_{in}^{'}\right) \tag{5.2.1}$$

Thus, depending upon the choice (resistive/capacitive) of the impedances Z_1 and Z_2, this block can realize fully differential scalar, lossless integrator and lossy integrator. Fully-differential integrators, constant multipliers and summing/differencing elements may be then used to realize the given transfer function whose general form can be expresses as:

$$T(s)=\frac{b}{a_n s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots\ldots + a_2 s^2 + a_1 s + a_0} = \frac{\frac{b}{a_n s^n}}{1+\frac{a_{n-1}}{a_n s}+\frac{a_{n-2}}{a_n s^2}+\ldots\ldots+\frac{a_2}{a_n s^{n-2}}+\frac{a_1}{a_n s^{n-1}}+\frac{a_0}{a_n s^n}} \quad (5.2.2)$$

where b, a_n, a_{n-1},…..a_3, a_2, a_1, a_0, are real positive constants

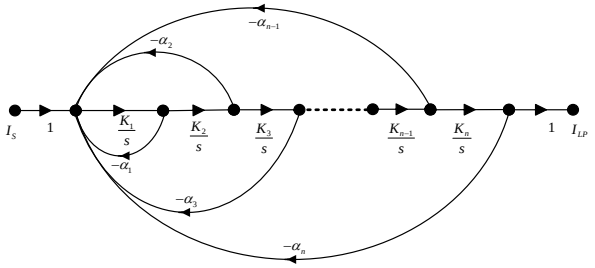


Fig.5.2.3 Signal flow graph corresponding to an nth-order all pole transfer function

A signal flow graph is now constructed as shown in Fig. 5.2.3. Using Mason's Gain formula [55], the transfer function is given by:

$$\frac{I_{LP}}{I_s}=\frac{\frac{K_1K_2.....K_3K_4K_n}{s^n}}{1+\alpha_1\frac{K_1}{s}+\alpha_2\frac{K_1K_2}{s^2}+\alpha_3\frac{K_1K_2K_3}{s^3}+.....+\alpha_{n-1}\frac{K_1K_2K_3....K_{n-1}}{s^{n-1}}+\alpha_n\frac{K_1K_2K_3.....K_n}{s^n}}$$

The above can be further rearranged as

$$\frac{I_{LP}}{I_s}=\frac{1}{\frac{s^n}{K_1K_2K_3.....K_n}+\alpha_1\frac{s^{n-1}}{K_2K_3.....K_n}+.....+\alpha_{n-1}\frac{s}{K_n}+\alpha_n} \quad (5.2.3)$$

When the integrators and scalar-multipliers are realized in their fully-differential forms then the complete realization of the transfer function turns out to be as shown Fig. 5.2.4.

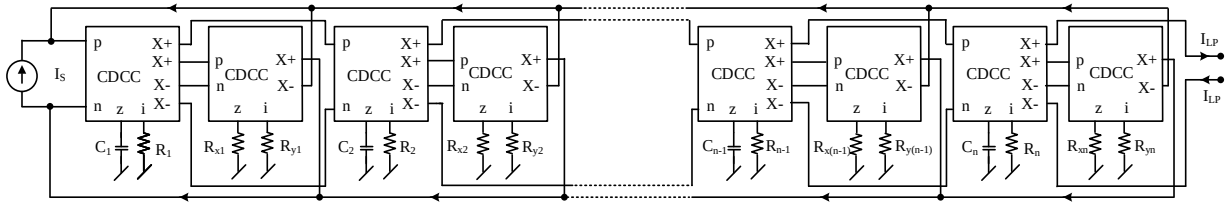


Fig. 5.2.4 n^{th} order fully-differential current-mode transfer function realization

A straight forward analysis of the circuit of Fig.5.2.4 results in the following transfer function

$$\frac{I_{LP}}{I_s} = \frac{1}{s^n\left(\frac{R_1C_1}{2}\right)\left(\frac{R_2C_2}{2}\right)\ldots\left(\frac{R_nC_n}{2}\right) + s^{n-1}\left(\frac{2R_{x1}}{R_{y1}}\right)\left(\frac{R_2C_2}{2}\right)\ldots\left(\frac{R_nC_n}{2}\right) + \ldots + s\left(\frac{2R_{x(n-1)}}{R_{y(n-1)}}\right)\left(\frac{R_nC_n}{2}\right) + \left(\frac{2R_{xn}}{R_{yn}}\right)} \quad (5.2.4)$$

It is, thus, evident from the realization of Fig.5.2.4 that if the integrator time constants and scalar multiplier gains are chosen appropriately, then by comparing the coefficients of the denominator polynomials of equations (5.2.3) and (5.2.4), the values of the various resistors and capacitors required to realize a given transfer function may be calculated based on the values of α_i and K_i (i=1-n). For instance, by comparing the coefficients of the various terms containing different degree of 's' with a normalized/denorrmalized Butterworth transfer function, the values of different resistors and capacitors used in the circuit of Fig. 5.2.4 to realize such a transfer function can be found. It may be noted that the scalar-multipliers added along with each integrator do result in somewhat larger number of active and passive components, however, this has been done purposely to ensure that all the grounded capacitors in the circuit can have equal values as desired in IC fabrication; also, all the resistors associated with the integrators too can be made equal-valued which is helpful in obtaining the electronic tunability of the cut-off frequency of the realised filter by replacing all of these grounded resistors by identical VCRs controlled by a single external control voltage.

5.3 **Design examples**:

We now illustrate the above methodology with two specific design examples, namely fully- differential fifth order lowpass Butterworth filter and fully-differential fifth order lowpass Chebyshev filter

5.3.1 Fifth order lowpass Butterworth filter design

We start with the deformalized transfer function of a fifth order lowpass Buterworth filter with a cut-off frequency f_c

$$T(s)=\frac{I_{LP}}{I_S}=\frac{1}{s^5\left(\frac{1}{2\pi f_c}\right)^5+b_4s^4\left(\frac{1}{2\pi f_c}\right)^4+b_3s^3\left(\frac{1}{2\pi f_c}\right)^3+b_2s^2\left(\frac{1}{2\pi f_c}\right)^2+b_1s\left(\frac{1}{2\pi f_c}\right)+b_0} \quad (5.3.1.1)$$

where b_5=1, b_4=3.2360680, b_3=5.2360680, b_2=5.2360680, b_1=3.2360680, b_0=1

The realization of the filter is shown in Fig. 5.3.1.1

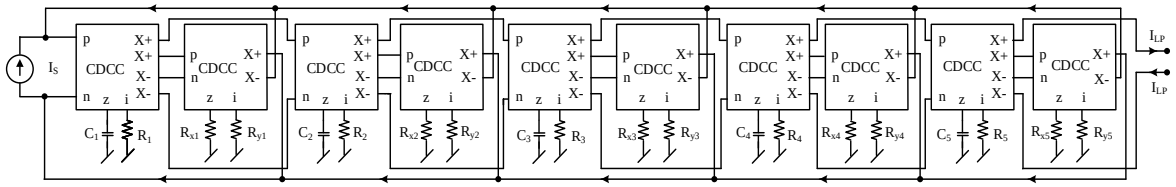


Fig. 5.3.1.1 Fifth order fully-differential current-mode lowpass filter

An analysis of the circuit shown above gives the transfer function

$$\frac{I_{LP}}{I_S}=\frac{1}{\begin{aligned}&s^5\left(\frac{R_1C_1}{2}\right)\left(\frac{R_2C_2}{2}\right)\left(\frac{R_3C_3}{2}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)+s^4\left(\frac{2R_{x1}}{R_{y1}}\right)\left(\frac{R_2C_2}{2}\right)\left(\frac{R_3C_3}{2}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)\\&+s^3\left(\frac{2R_{x2}}{R_{y2}}\right)\left(\frac{R_3C_3}{2}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)+s^2\left(\frac{2R_{x3}}{R_{y3}}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)+s\left(\frac{2R_{x4}}{R_{y4}}\right)\left(\frac{R_5C_5}{2}\right)+\left(\frac{2R_{x5}}{R_{y5}}\right)\end{aligned}}$$

Choosing R_1= R_2= R_3= R_4= R_5 =R and C_1= C_2=C_3= C_4=C_5 =C, we can write

$$\frac{I_{LP}}{I_S}=\frac{1}{s^5\left(\frac{RC}{2}\right)^5+s^4\left(\frac{2R_{x1}}{R_{y1}}\right)\left(\frac{RC}{2}\right)^4+s^3\left(\frac{2R_{x2}}{R_{y2}}\right)\left(\frac{RC}{2}\right)^3+s^2\left(\frac{2R_{x3}}{R_{y3}}\right)\left(\frac{RC}{2}\right)^2+s\left(\frac{2R_{x4}}{R_{y4}}\right)\left(\frac{RC}{2}\right)+\left(\frac{2R_{x5}}{R_{y5}}\right)} \quad (5.3.1.2)$$

Comparing (5.3.1.1) and (5.3.1.2), the values of the various resistors and capacitors, in terms of f_c and b_i (i=0-5) are obtained as:

$$f_c=\frac{1}{\pi RC} \quad (5.3.1.3)$$

$$\frac{R_{x1}}{R_{y1}}=\frac{b_4}{2}=1.618,\frac{R_{x2}}{R_{y2}}=\frac{b_3}{2}=2.618,\ \frac{R_{x3}}{R_{y3}}=\frac{b_2}{2}=2.618,\frac{R_{x4}}{R_{y4}}=\frac{b_1}{2}=1.618\ \ and\ \frac{R_{x5}}{R_{y5}}=\frac{b_0}{2}=0.5 \qquad (5.3.1.4)$$

It is observed from equations (5.3.1.3) that cut-off frequency f_c can be tuned (electronically) if we replace all the resistors of value R used in the realization of the fully-differential integrators by identical MOS VCRs for which , for simplicity, we have chosen the two-MOSFET VCR shown in Fig. 5.3.1.2 [50], keeping the associated capacitors C_i all of the same value. The equivalent resistance R_i realized by the circuit of Fig. 5.3.1.2 is given by [50]

$$R_i=\frac{1}{2\mu C_{ox}\left(\frac{W}{L}\right)\left(V_{C_i}-V_T\right)} \qquad (5.3.1.5)$$

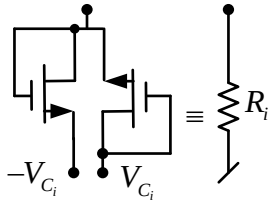


Fig. 5.3.1.2 The MOS VCR adopted from [50]

PSPICE simulation results

The CMOS implementation of the CDCC [see chapter 2] shown in Fig.5.3.1.3 using 0.18 µm TSMC process technology has been employed to verify the workability of the circuits designed in the previous section. The values of the DC bias currents and voltages were taken as 40 µA and ±2.5V respectively. The W/L of the various MOSFETs was taken as shown in Table 5.3.1.1.

R_p and R_n represent the parasitic input resistances of the p-port and n-port respectively whereas R_z, C_z represent the output resistance and output capacitance looking into the z-terminal of the CDCC. R_i represents the output resistance of the voltage buffer of the MO-CCII (resistance looking into the i terminal). On the other hand, R_{x+} and C_{x+} represent output resistance and output capacitance looking into the x+ terminals of the CDCC and finally, R_{x-} and C_{x-} represent

the output resistance and the output capacitance looking into the `x-` terminal of the CDCC. The mmeasured values of the various parasitics of the CDCC, at 40µA DC bias current and ±2.5V DC bias voltage, are found to be as shown in Table 5.3.1.2.

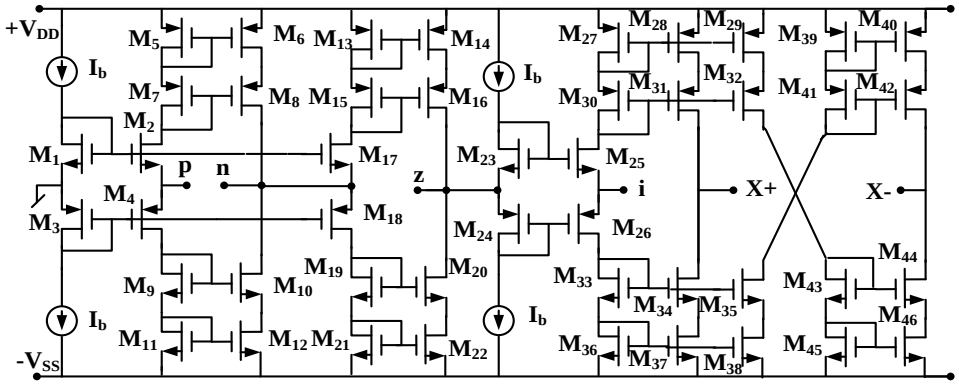


Fig. 5.3.1.3 CMOS implementation of the CDCC [see chapter 2]

Table 5.3.1.1 Aspect ratios of the various MOSFETs used in CDCC realization

MOSFETs	W/L (µm/µm)
M_1, M_2, M_{17}, M_{23}, M_{25}	25/0.25
M_3, M_4, M_{18}, M_{24}, M_{26}	50/0.25
M_5 - M_{16}, M_{19} - M_{22}, M_{27} - M_{46}	2.5/0.25

Table 5.3.1.2 The SPICE-measured values of the various parasitics of the CMOS CDCC

S.No.	Parameter	Value
1	R_p	591 Ω
2	R_n	591 Ω
3	R_z	4.9389 MΩ
4	C_z	6.2988×10^{-14} F
5	R_i	591 Ω
6	R_{x+}	4.9950 MΩ
7	C_{x+}	7.3833×10^{-15} F
8	R_{x-}	4.7990 MΩ
9	C_{x-}	7.3700×10^{-15} F

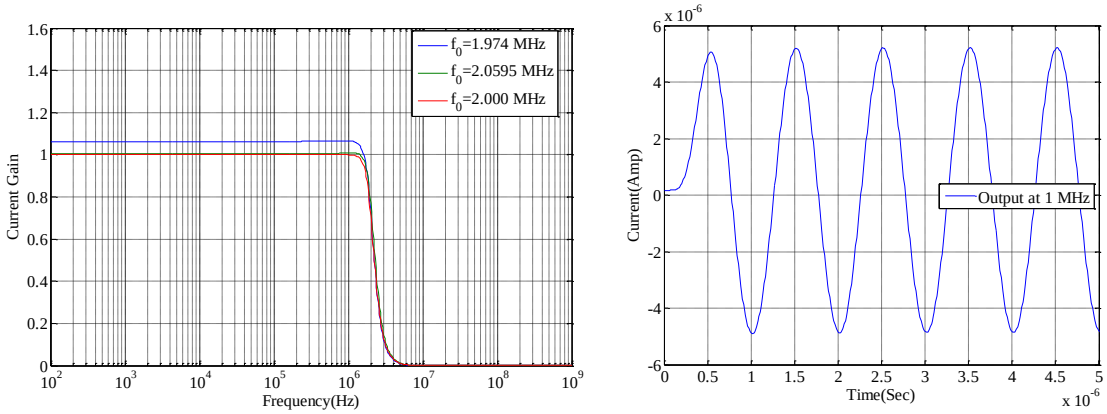
We now present some SPICE simulation results to demonstrate the workability of the proposed fully-differential current-mode fifth order Butterworth filter (see Fig. 5.3.1.1)

The frequency response and the transient response of the fully-differential current node fifth order lowpass Butterworth filter: The filter was designed for a cut-off frequency of 2.0 MHz by appropriately selecting the passive resistors and capacitors as: R_{x5}=5 kΩ, R_{y5}=10 kΩ, R_{x4}=16.18 kΩ, R_{y4}=10 kΩ, R_{x3}=26.18 kΩ, R_{y3}=10 kΩ, R_{x2}=26.18 kΩ, R_{y2}=10 kΩ, R_{x1}=16.18 kΩ , R_{y1}=10 kΩ, R_1= R_2= R_3= R_4= R_5 = R=10 kΩ and C_1= C_2=C_3= C_4=C_5 =15.92 pF. From Table 5.3.1.2, it is revealed that the parasitic capacitances are generally very small and their effect on the circuit performance can be minimised by taking the external capacitors much larger than them, however, the parasitic input resistances at the ports **p**, **n** and **i** are about 0.591 kΩ and cannot be ignored. Hence, they must be absorbed in the external resistors to compensate for their adverse effect for which all the resistances terminated at 'i' ports have been *pre-distorted* by subtracting 0.591 kΩ from their design values. The new values of the resistors and capacitors, after accounting these parasitics are: R_{x5}=5 kΩ, R_{y5}=9.409 kΩ, R_{x4}=16.18 kΩ, R_{y4}=9.409 kΩ, R_{x3}=26.18 kΩ, R_{y3}=9.409 kΩ, R_{x2}=26.18 kΩ, R_{y2}=9.409 kΩ, R_{x1}=16.18 kΩ, R_{y1}=9.409 kΩ, R_1= R_2= R_3= R_4= R_5 = R=9.409 kΩ and C_1=C_2=C_3=C_4=C_5=15.92 pF. The frequency responses of the normal design and the one using *pre-distorted* values of all the resistors at port **i** of the CDCCs, both obtained from SPICE simulations, have been plotted against the ideal response (obtained through MATLAB) in Fig. 5.3.1.4(a) whereas the transient response of the designed filter, with an input current of 5.0 μA amplitude at 1.0 MHz, is shown in Fig. 5.3.1.4 (b).

The results of Fig. 5.3.1.4 confirm the validity of the theory.

Electronic-tunability: From equation (5.3.1.3), it is observed that the cut-off frequency of the filter can be varied by simultaneously changing the time constants of *all* the integrators i.e. by

varying all R_i while keeping the values of all the capacitors of the integrators and the resistors in the scalar-multipliers *unchanged.*



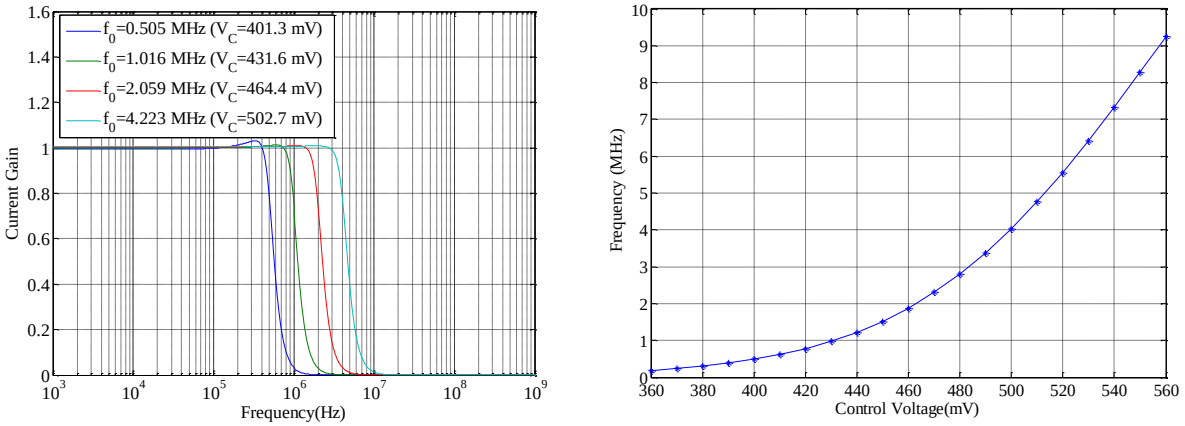
(a) (b)

Fig. 5.3.1.4 PSPICE simulation results of the fully-differential current-mode fifth order lowpass Butterworth Filter (a) Frequency response (i)----Normal (ii)----Using pre-distorted resistor values at ports `i` (iii) -----Ideal (obtained using MATLAB) (b) Transient response

Fifth order Butterworth filter: As an example, it has been found that to vary the cut-off frequencies as 0.5 MHz, 1.0 MHz, 2.0 MHz and 4.0 MHz we must choose R_i = 40 kΩ, 20 kΩ, 10 kΩ and 5 kΩ. After considering the parasitics at the 'i' ports, Choosing the control voltages as $V_C = V_{Ci} = -V_{Ci}$= 401.3 mV, 431.6 mV, 464.4 mV and 502.7 mV respectively, it has been found that VCRs realize equivalent resistance values as 39.44 kΩ, 19.42 kΩ, 9.40 kΩ and 4.41 kΩ respectively which, along with the intrinsic parasitic resistance of 0.591 kΩ, become *approximately equal to* 40 kΩ, 20 kΩ, 10 kΩ and 5 kΩ respectively, as required. Fig. 5.3.1.5(a) shows the frequency responses for different values of the control voltage V_c while Fig. 5.3.1.5 (b) shows the variation of the cut-off frequency with different values of the control voltage V_c.

Monte-Carlo analysis: To study the effect of mismatches in the component values in the designed fifth order Butterworth filter , Monte Carlo simulations have been carried out by allocating 1% tolerances to the component values (capacitors C=15.92 pF) for all the five grounded capacitors and performing 100 runs. The results for the 1% tolerance have been

shown in Fig.5.3.1.6. The value of the cut-off frequency obtained from the simulations was found to be 2.0595 MHz. Monte Carlo analysis shows the median value of cut-off frequency as f_0=2.0584 MHz, which indicates that the mismatch in the component values do not have large effect on the realized cut-off frequency.



(a) (b)

Fig. 5.3.1.5 PSPICE simulation results (a) Tunability of cut-off frequency with Control Voltage and (b) Variation of the cut-off frequency with control voltage V_c

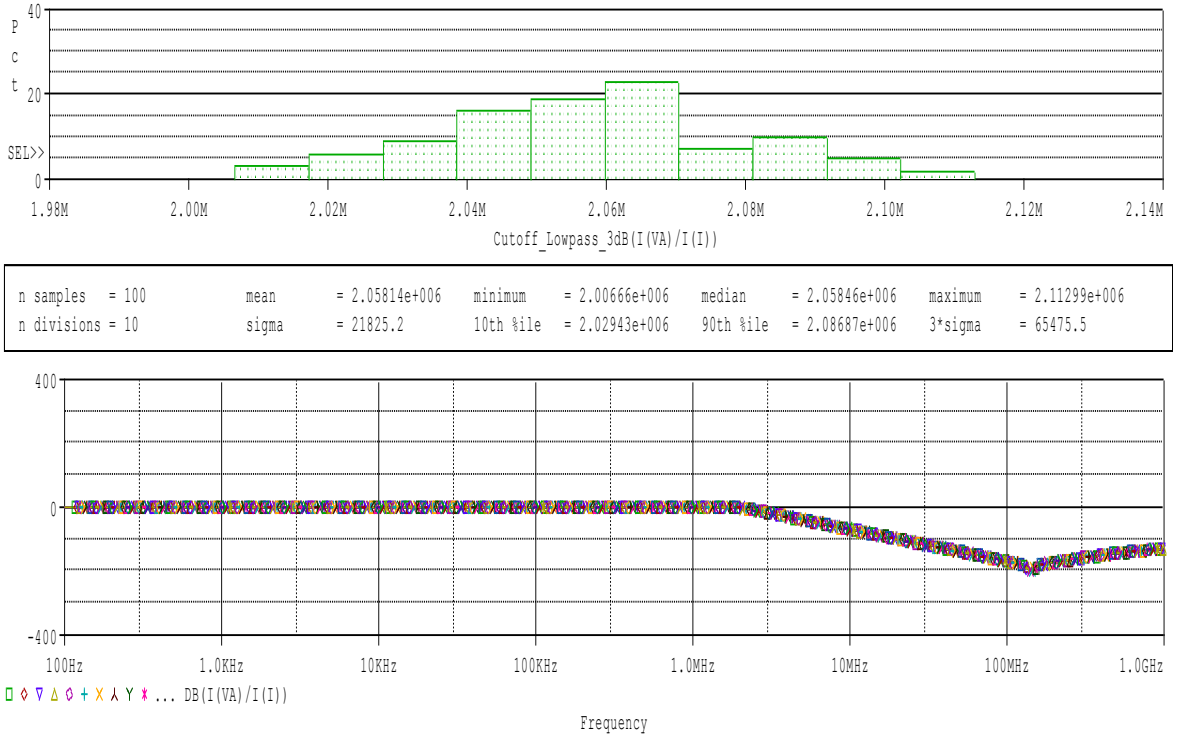


Fig. 5.3.1.6 Results of Monte Carlo analysis for fully-differential current-mode fifth order low pass Butterworth filter.

Reduced-component version: In the structure of Fig.5.3.1.1, in all the integrators we have employed all equal-valued capacitors (as desirable for IC fabrication) and all equal-valued resistors (which facilitate simultaneous variation of all of them when they are replaced by identical CMOS-VCRs driven by a common control voltage). In view of this, it was necessary to employ scalar-multipliers along with each integrator to accommodate the required coefficients of the denominator polynomial of the filter transfer function. However, if all the scalar-multipliers are dispensed with, then a reduced-component-count version is possible which is shown in Fig. 5.3.1.7. For the same cut-off frequency i.e. 2.0 MHz, the component values for this version have also been calculated according to the same fifth order Butterworth transfer function along with pre-distorted values of resistances (as explained earlier) and are given as: $C_1 = C_2 = C_3 = C_4 = C_5 = C = 9.84$ pF; $R_{i1} = 4.409$ kΩ, $R_{i2} = 9.409$ kΩ, $R_{i3} = 15.589$ kΩ, $R_{i4} = 25.589$ kΩ and $R_{i5} = 51.769$ kΩ. A SPICE check has indicated that this circuit too works well but in this reduced-component design, the electronic-tunability feature is sacrificed.

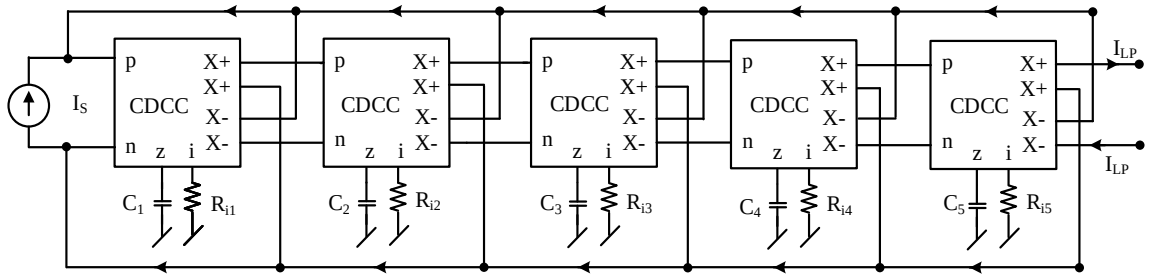


Fig. 5.3..1.7 Fifth order fully-differential CM lowpass filter with reduced-component-count

5.3.2 Fifth order lowpass Chebyshev filter design

We start with the denormalized transfer function of a fifth order lowpass Chebycshev filter with a cut-off frequency f_c , α_{max}=0.5dB in $0 \le f \le f_c$ Hz.

$$T(s) = \frac{I_{LP}}{I_S} = \frac{1}{b_5 s^5 \left(\frac{1}{2\pi f_c}\right)^5 + b_4 s^4 \left(\frac{1}{2\pi f_c}\right)^4 + b_3 s^3 \left(\frac{1}{2\pi f_c}\right)^3 + b_2 s^2 \left(\frac{1}{2\pi f_c}\right)^2 + b_1 s \left(\frac{1}{2\pi f_c}\right) + b_0} \qquad (5.3.2.1)$$

Where b_5=5.5888, b_4=6.5523, b_3=10.8272, b_2 =7.3185, b_1=4.2056, b_0=1

The realization of the filter using fully differential integrators and fully-differential multipliers realized with CDCCs can be done from same Fig.5.3.1.1

Comparing (5.3.2.1) and (5.3.1.2), the values of the various resistors and capacitors, in terms of f_c and b_i (i=0-5) are obtained as:

$$f_c = \frac{\left(b_5\right)^{\left(\frac{1}{5}\right)}}{\pi RC} = \frac{1.4108}{\pi RC} \tag{5.3.2.2}$$

$$\frac{R_{x1}}{R_{y1}} = \frac{b_4}{2\left(b_5^{(\frac{1}{5})}\right)^4} = 0.827, \frac{R_{x2}}{R_{y2}} = \frac{b_3}{2\left(b_5^{(\frac{1}{5})}\right)^3} = 1.928, \frac{R_{x3}}{R_{y3}} = \frac{b_2}{2\left(b_5^{(\frac{1}{5})}\right)^2} = 1.838,$$
$$\frac{R_{x4}}{R_{y4}} = \frac{b_1}{2\left(b_5^{(\frac{1}{5})}\right)^1} = 1.4905 \ \ and \ \frac{R_{x5}}{R_{y5}} = \frac{b_0}{2\left(b_5^{(\frac{1}{5})}\right)^0} = 0.5 \tag{5.3.2.3}$$

It is observed from equations (5.3.2.2) that cut-off frequency f_c can be tuned (electronically) if we replace all the resistors of value R used in the realization of the fully-differential integrators by identical MOS VCRs.

PSPICE simulation results

Frequency and transient response of the proposed fully-differential current-mode fifth order lowpass Chebyshev filter: The proposed filter was designed for a cut-off frequency of 2 MHz by appropriately selecting the passive resistors as follows: R_{x5}=10 kΩ, R_{y5}=20 kΩ, R_{x4}=14.905 kΩ, R_{y4}=10 kΩ, R_{x3}=9.19 kΩ, R_{y3}=5 kΩ, R_{x2}=9.64 kΩ, R_{y2}=5 kΩ, R_{x1}=23.57 kΩ, R_{y1}=28.5 kΩ, R=R_1= R_2= R_3= R_4= R_5 =10 KΩ and C=C_1= C_2=C_3= C_4=C_5 =22.45 pF.

From Table 5.3.1.2**,** it is revealed that the parasitic capacitances are generally very small and their effect on the circuit performance can be minimised by taking the external capacitors much larger than them, however, the parasitic input resistances at the ports **p**, **n** and **i** are about 0.591

kΩ and cannot be ignored. Hence, they must be absorbed in the external resistors to compensate for their adverse effect for which all the resistances terminated at 'i' ports have been *pre-distorted* by subtracting 0.591 kΩ from their design values. The new values of the resistors and capacitors, after accounting these parasitics are : R_{x5}=10 KΩ, R_{y5}=19.409 KΩ, R_{x4}=14.905 KΩ, R_{y4}=9.409 KΩ, R_{x3}=9.19 KΩ, R_{y3}=4.409 KΩ, R_{x2}=9.64 KΩ, R_{y2}=4.409 KΩ, R_{x1}=23.57 KΩ, R_{y1}=27.909 KΩ, R=R_1= R_2= R_3= R_4= R_5 =9.409 KΩ and C=C_1= C_2=C_3= C_4=C_5 =22.45 pF. The frequency responses of the one using *pre-distorted* values of all the resistors at port **i** of the CDCCs, obtained from SPICE simulations, have been plotted against the ideal response (obtained through MATLAB) in Fig. 5.3.2.1(a) whereas the transient response of the designed filter, with an input current of 5.0 μA amplitude at 1.0 MHz, is shown in Fig. 5.3.2.1 (b). The results of Fig. 5.3.2.1, confirm the validity of the theory

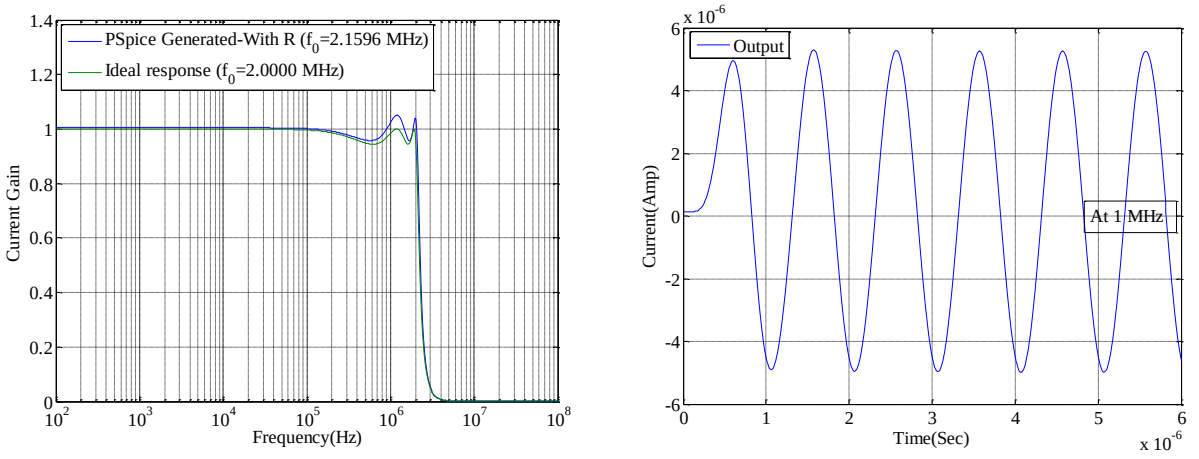


Fig. 5.3.2.1 PSPICE simulation results of the fully-differential current-mode fifth order lowpass Chebyshev Filter (a) Frequency response (i)------Using pre-distorted resistor values at ports `i` (iii) -----Ideal (obtained using MATLAB) (b) Transient response

Electronic-tunability: From equation (5.3.2.2), it is observed that the cut-off frequency of the filter can be varied by simultaneously changing the time constants of *all* the integrators i.e. by varying all R_i while keeping the values of all the capacitors of the integrators and the resistors in the scalar-multipliers *unchanged.*

Fifth order Chebyshev filter: As an example, it has been found from equation (5.3.2.2) that to get the cut-off frequencies as 1.0 MHz, for C=22.45 pF, R_i = 20 kΩ. After considering the parasitics at the 'i' ports, Choosing the control voltages as V_C= V_{Ci}=−V_{Ci}= 431.6 mV, it has been found that VCRs realize equivalent resistance values as 19.42 KΩ which, along with the intrinsic parasitic resistance of 0.591 kΩ, become *approximately equal to* 20 kΩ as required. Fig. 5.3.2.2(a) shows the tunability of cut-off frequency with Control Voltage (frequency responses for given control voltage V_c =431.6 mV) while Fig. 5.3.2.2 (b) shows the variation of the cut-off frequency with different values of the control voltage V_c.

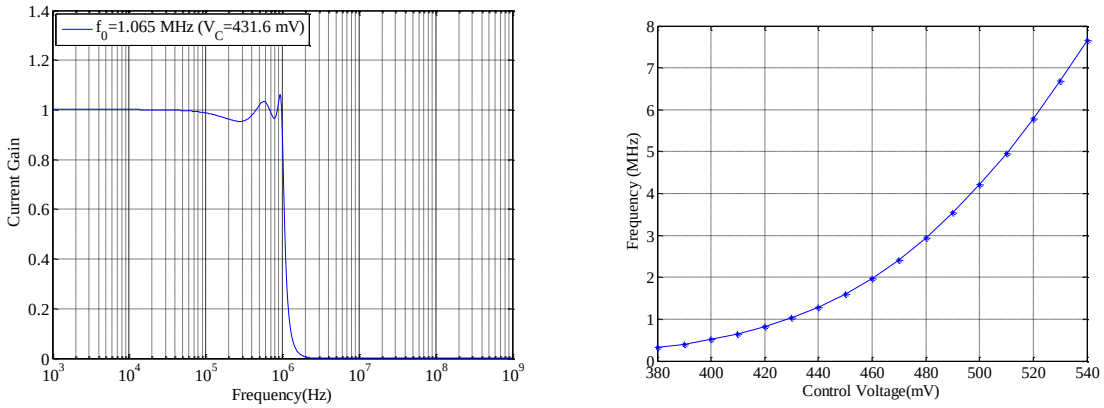


Fig. 5.3.2.2 PSPICE simulation results (a) Tunability of cut-off frequency with Control Voltage and (b) Variation of the cut-off frequency with control voltage V_c

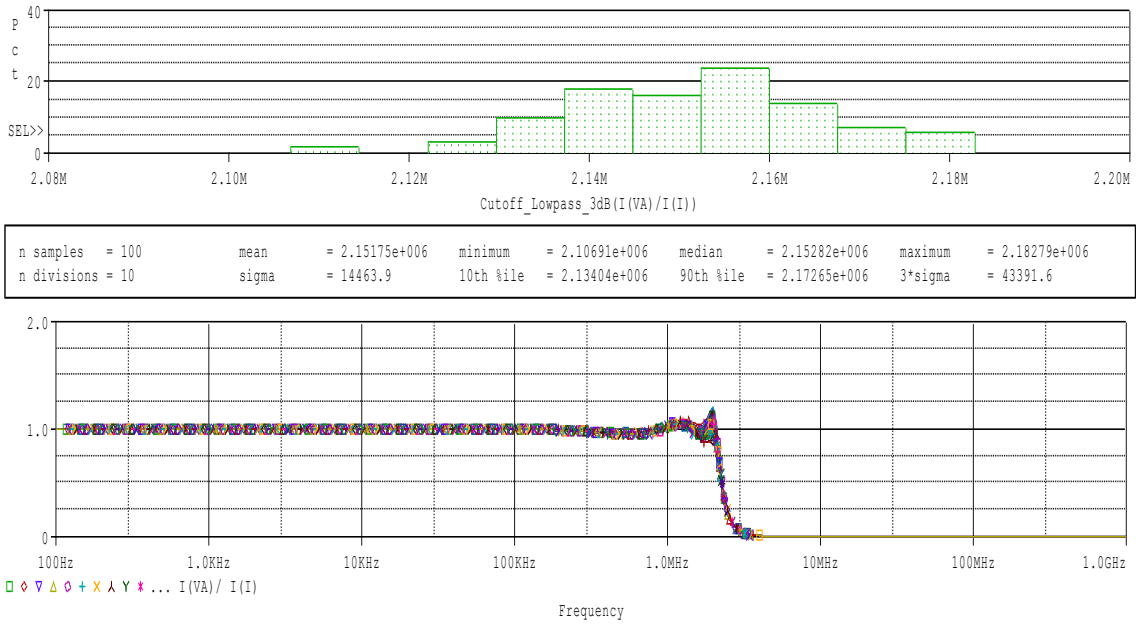


Fig. 5.3.2.3 Results of Monte Carlo analysis for fully-differential current-mode fifth order low pass Chebyshev filter.

Monte-Carlo analysis:

Similarly, in the designed fifth order Chebyshev filter, Monte Carlo simulations have been carried out by allocating 1% tolerances to the component values (capacitors C=22.45 pF) within five grounded capacitors and performing 100 runs. The results for the 1% tolerance have been shown in Fig.5.3.2.3. The value of the cut-off frequency obtained from the simulations was found to be 2.1596 MHz. Monte Carlo analysis shows the median value of cut-off frequency as f_0=2.1528 MHz, which indicates that the mismatch in the component values do not have large effect on the realized cut-off frequency.

5.4 Concluding remarks

In this chapter, we have presented a methodology for the design of an n^{th} order fully-differential current-mode higher order filter using CDCCs as active elements. The methodology is general and results in filter configurations which employ *all grounded passive elements.* Design examples of a fifth order Butterworth and Chebyshev filters design have been presented whose workability has been substantiated using SPICE simulations based upon a CMOS CDCC using 0.18 µm TSMC technology process parameters. The proposed methodology of designing CDCC-based fully-differential higher order ($n \geq 3$) CM filter achieves the following three advantageous features simultaneously which have not been achieved simultaneously in any of the earlier works:

(i) use of all grounded passive elements

(ii) employment of only one capacitor per pole, and

(iii) facilitation of electronic-tunability of the cut-off frequency.

A reduced-component-version of the designed fifth order Butterworth filter has also been presented which too employs all grounded RC components but does not have electronic tunability.

Lastly, it may be mentioned that although *multifunction capability* has been demonstrated in a class of higher order filters in some earlier works such as that in [17], the filters presented therein have single-ended input and single-ended output. From the review of previously known fully-differential higher order filters it is revealed that to the best of authors' knowledge, multi-function capability has not been explored in the realization of fully-differential structures so far. This appears to be interesting for further investigations.

5.5 References

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Chapter 6

Current-Mode Quadrature Oscillators

In this Chapter, Current Follower Current Conveyor (CFCC) and Current Differencing Current Conveyor (CDCC) based quadrature oscillator circuits have been proposed.

6.1 Introduction

Quadrature sinusoidal oscillator (QSO) circuit provides two sinusoids with 90^0 phase difference and finds several applications in communication and measurement systems. In communication systems they are used in quadrature mixers, single-sideband generators and direct-conversion receivers while in measurement systems such oscillators are used in vector generators or selective voltmeters [1].

During the last two decades, many new active building blocks have been proposed in the domain of analog signal processing, a comprehensive review of which was presented in [2] wherein several new active building blocks (ABB) were also proposed. Many of the new ABBs proposed in [2] have received world-wide attention of researchers and have been employed in the past for various signal processing and signal generation applications.

The new ABBs which have been used in the realization of QSOs earlier include Current Differencing Buffered Amplifier (CDBA) [3, 4], Voltage Differencing Buffered Amplifier (VDBA) [5], Voltage Differencing Transconductance Amplifier (VDTA) [6], Voltage Differencing Current Conveyor (VDCC) [7], Current Differencing Transconductance Amplifier (CDTA) [8]-[12], Multiple-Output Current Controlled Current Differencing Transconductance Amplifier (MO-CCCDTA) [13], Modified Current Differencing Transconductance Amplifier (MCDTA) [14], Current Follower Transconductance Amplifier (CFTA) [15], Z-copy Current Follower Transconductance Amplifier (ZC-CFTA) [16], Second-Generation Current Conveyor Transconductance Amplifier (CCII-TA) [17], Differential-Input Buffered and Transconductance Amplifier (DBTA) [18], Current-Feedback Operational Amplifier (CFOA) [19], Differential Voltage Current Conveyor (DVCC)[20], Differential Voltage Current-Controlled Conveyor Transconductance Amplifier (DVCCCTA) [21], Voltage Differencing Inverting Voltage Buffered Amplifier (VDIBA) [22], Voltage

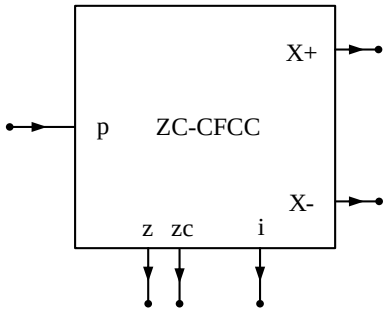
Differencing-Differential Input Buffered Amplifiers (VD-DIBA)[23], [24] and Programmable Current Amplifier [25].

It may be mentioned that while the QSOs presented in [3]-[5],[7], [16]-[24] operate in voltage mode (VM), those presented in the references [6], [8]-[17], [21], [25] operate in current mode (CM). Also, of the various QSO circuits quoted above, only the circuits presented in [3], [4] and [12] offer fully decoupled condition of oscillation and frequency of oscillation. Furthermore, out of [3], [4] and [12], the QSOs described in [3], [4] are VM oscillators while the QSO described in [12] is a CM oscillator.

It has been observed from the literature survey that Multi-output Current Follower Current Conveyor (MO-CFCC) or CDCC [2] have not been utilized for the realization of QSOs so far while its applications in the realization of simulated impedances and fully differential filters have been reported in this thesis [in chapter 2,3 and 4]. In this chapter, we propose some QSOs realized with CFCCs to fill this void. The workability of the proposed oscillators has been verified using PSPICE simulations in 0.18 micron TSMC technology.

6.2 CFCC-based realization of the current-mode quadrature oscillator

As already explained earlier a CFCC [2] is a five-terminal ABB. The current at the z terminal is an inverted copy of the input current at ‘p’ terminal. The terminal ‘i’ tracks the potential at the terminal z. Two complementary currents at the output terminals are available which are copies of the current at the ‘i’ terminal. To provide additional functionality to the CFCC, a copy of the current at the ‘z’ terminal may also be provided resulting in the Z-copy CFCC (ZC-CFCC). The symbolic representation and port relations for this ABB are shown in Fig.6.2.1.



$$\begin{bmatrix} V_p \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \\ I_{zc} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ V_z \\ I_i \\ V_{x+} \\ V_{x-} \\ V_{zc} \end{bmatrix} \quad (6.2.1)$$

Fig.6.2.1 Symbolic notation of the ZC-CFCC

The first proposed current-mode quadrature oscillator circuit using CFCCs is shown in Fig. 6.2.2 which is devised using a parallel RLC resonator consisting of CFCC, R_4, R_5, C_1 and C_2 and a NIC-simulated negative resistor realized with ZC-CFCC alongwith the resistors R_1, R_2 and R_3 .

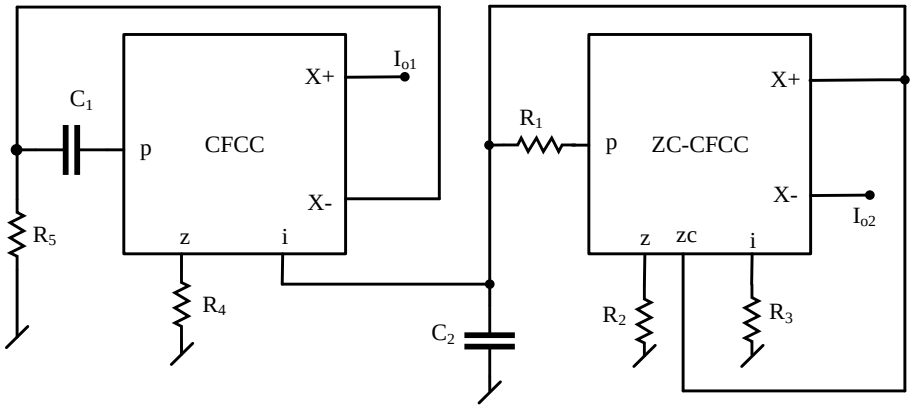


Fig.6.2.2 The proposed CFCC-based current mode quadrature oscillator

A routine analysis of the circuit of Fig.6.2.2 yields the following characteristic equation (CE):

$$s^2 R_1 R_3 R_4 R_5 C_1 C_2 + s R_5 C_1 \left(R_1 R_3 - R_2 R_4 \right) + R_1 R_3 = 0 \quad (6.2.2)$$

From equation (6.2.2), the condition of oscillation (CO) and frequency of oscillation (FO) are found to be:

CO:

$$R_1 R_3 = R_2 R_4 \quad (6.2.3)$$

FO:

$$\omega_{osc} = \frac{1}{\sqrt{R_4 R_5 C_1 C_2}} \tag{6.2.4}$$

However, for quadrature oscillator design, we must look into the interrelationship between I_{01} and I_{02} which is found to be

$$\frac{I_{01}}{I_{02}} = -\frac{R_1 R_3}{sR_2 R_4 R_5 C_1} \tag{6.2.5}$$

Under sinusoidal steady state, equation (6.2.5) reduces to

$$\frac{I_{01}}{I_{02}} = \frac{j}{\omega_0 R_5 C_1} \tag{6.2.6}$$

The phase difference φ is, thus, equal to 90°.

6.3 CFCC-based current-mode quadrature oscillator with grounded capacitors

It may be observed from Fig.6.2.2 that one of the capacitors in the QSO is not grounded. Now we present another QSO shown in Fig.6.3.1 in which both the capacitors are grounded.

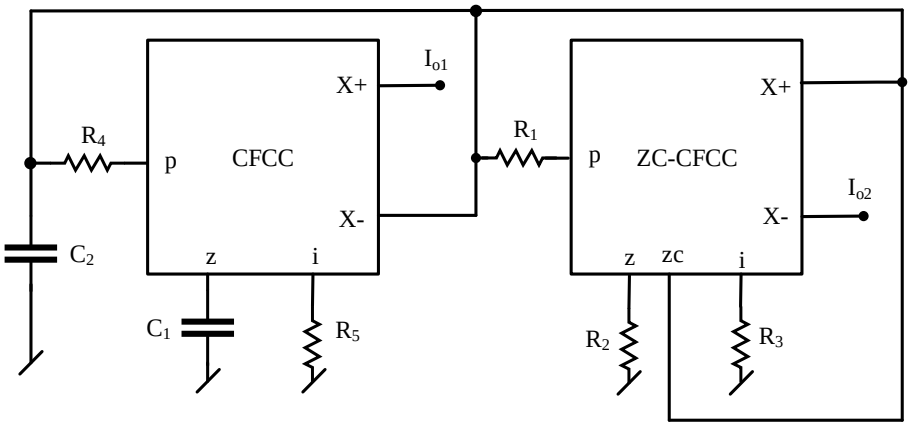


Fig.6.3.1 CFCC-based current mode quadrature oscillator with grounded capacitors

This structure follows the same design principle, as used in structure of Fig. 6.2.2, of generating sinusoidal oscillation using a combination of parallel RLC resonator and a negative resistor to cancel the resistive component of the resonator. The resonator in this QSO consists of CFCC,

R_4, R_5 and grounded capacitors C_1 and C_2 whereas NIC-simulated negative resistor is realized by the ZC-CFCC alongwith the resistors R_1, R_2 and R_3.

A routine analysis of the circuit given in Fig.6.3.1 yields the following characteristic equation (CE):

$$s^2 R_1 R_3 R_4 R_5 C_1 C_2 + s R_5 C_1 \left(R_1 R_3 - R_2 R_4 \right) + R_1 R_3 = 0 \tag{6.3.1}$$

From equation (6.3.1), the condition of oscillation (CO) and frequency of oscillation (FO) are found to be:

CO:

$$R_1 R_3 = R_2 R_4 \tag{6.3.2}$$

FO:

$$\omega_{osc} = \frac{1}{\sqrt{R_4 R_5 C_1 C_2}} \tag{6.3.3}$$

The interrelationship between I_{01} and I_{02} for the proposed QO is found to be

$$\frac{I_{01}}{I_{02}} = -\frac{R_1 R_3}{s R_2 R_4 R_5 C_1} \tag{6.3.4}$$

Under sinusoidal steady state , equation (6.3.4) reduces to

$$\frac{I_{01}}{I_{02}} = \frac{j}{\omega_0 R_5 C_1} \tag{6.3.5}$$

The phase difference φ is, thus, equal to 90^o.

6.4 Non-ideal consideration

In the analysis so far the CFCC and ZC-CFCC were considered to be ideal. To analyse the practical response of the proposed circuit the effect of various parasitic resistances and capacitances associated with the different terminals of the ZC-CFCC need to be taken into account. In the non-ideal model of ZC-CFCC, R_p represents the parasitic input resistance of the p port whereas R_z, C_z represent the resistance and capacitance at the z-terminal of the CFCC. Similarly, R_{zc} and C_{zc} represent resistance and capacitance at the zc terminal while R_i represents the output resistance of the voltage buffer of the MO-CCII (resistance looking into the i terminal). On the other hand, R_{x+} and C_{x+} represent output resistance and output capacitance at the x+ terminals of the CFCC and finally, R_{x-} and C_{x-} represent the output resistance and the output capacitance at the x-terminals of the CFCC.

We have chosen second circuit (Fig.6.3.1) for a non-ideal analysis. The non-ideal model of the proposed oscillator circuit shown in Fig.6.4.1.

We have measured the values of the various parasitic resistances and capacitances of the CFCC employed in the present work (see Fig. 6.5.1) by carrying out detailed PSPICE simulations. The measured values of these non-ideal parameters are summarized in Table 6.4.1.

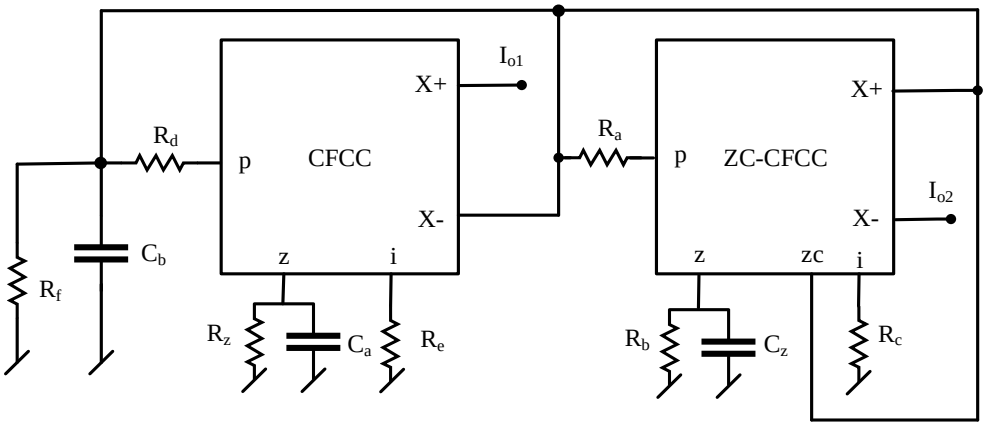


Fig.6.4.1 Non-ideal model of CFCC- based current mode quadrature oscillator

A straight forward analysis of proposed oscillator, incorporating all the parasitic immittances described above, gives the following third ordered characteristic equation:

$$s^3 R_a R_b R_c R_d R_e R_f R_z C_a C_b C_z + s^2 (R_a R_c R_d R_e R_f R_z C_a C_b + R_a R_b R_c R_e R_f R_z C_a C_z + R_a R_b R_c R_d R_e R_z C_a C_z + R_a R_b R_c R_d R_e R_f C_b C_z) + s(R_a R_c R_e R_f R_z C_a + R_a R_c R_d R_e R_z C_a + R_a R_c R_d R_e R_f C_b + R_a R_b R_c R_f R_z C_z + R_a R_b R_c R_e R_f C_z + R_a R_b R_c R_d R_e C_z - R_b R_d R_e R_f R_z C_a) + R_a R_c R_f R_z + R_a R_c R_e R_f + R_a R_c R_d R_e - R_b R_d R_e R_f = 0 \quad (6.4.1)$$

where $R_a = R_1 + R_p, R_b = R_2 \| R_z$, $R_c = R_3 + R_i$, $R_d = R_4 + R_p, R_e = R_5 + R_i$,
$R_f = R_{x+} \| R_{x-} \| R_{zc}, C_a = C_1 + C_z$ *and* $C_b = C_2 + C_{zc} + C_{x+} + C_{x-}$

Table 6.4.1 The SPICE-measured values of the various parasitics of the CMOS ZC-CFCC

S.No.	Parameter	Value
1	R_p	591Ω
2	R_i	591Ω
3	R_z	4.9178 M Ω
4	C_z	6.2988×10^{-14}F
5	R_{zc}	4.9178 M Ω
6	C_{zc}	7.3938×10^{-15}F
7	R_{x+}	4.9862 MΩ
8	C_{x+}	7.3954×10^{-15}F
9	R_{x-}	4.7752 MΩ
10	C_{x-}	7.4062×10^{-15}F

The following approximations (ensured by selecting appropriate values of the terminating resistances and capacitances) R_1 , R_2, R_3 ,R_4 ,R_5, << R_f and C_1 ,C_2>>C_{x+}, C_{x-}, C_z and C_{zc} lead to the second order approximation of the CE from which the non-ideal CO and FO are now given by

CO:

$$(R_1 + R_p)(R_3 + R_i) = (R_2 \| R_z)(R_4 + R_p) \quad (6.4.2)$$

FO:

$$\omega_{osc}^{'} = \omega_{osc} \frac{1}{\sqrt{\left(1+\frac{R_p}{R_4}\right)\left(1+\frac{R_i}{R_5}\right)\left(1+\frac{C_z}{C_1}\right)\left(1+\frac{(C_{zc}+C_{x+}+C_{x-})}{C_2}\right)}} \tag{6.4.3}$$

The interrelationship between I_{01} and I_{02} is found to be

$$\frac{I_{01}}{I_{02}} = -\frac{R_z(1+sR_bC_z)}{R_e(1+sR_zC_a)} = -\frac{R_z[1+s(R_2 \| R_z)C_z]}{(R_5+R_i)[1+sR_z(C_1+C_z)]} \tag{6.4.5}$$

The non-ideal expression of the phase difference φ is given by

$$\begin{aligned}\varphi &= \tan^{-1}\omega_{osc}^{'}R_zC_a - \tan^{-1}\omega_{osc}^{'}R_bC_z \\ &= \tan^{-1}R_z\sqrt{\frac{(C_1+C_z)}{(C_2+C_{zc}+C_{x+}+C_{x-})(R_1+R_p)(R_5+R_i)}} \\ &- \tan^{-1}\frac{(R_2 \| R_z)C_z}{\sqrt{(R_1+R_p)(R_5+R_i)(C_1+C_z)(C_2+C_{zc}+C_{x+}+C_{x-})}}\end{aligned} \tag{6.4.6}$$

Subject to the approximations used in the non-ideal analysis, it may be observed that the phase difference between the two output currents would be very close to 90^o (as the angle corresponding to the argument of the first arctangent term will be close to ninety degree because of the very large value of R_z while the angle corresponding to the argument of the second arctangent term will be very small because of the very small value of C_z).

6.5 PSPICE simulation results

We now present some SPICE simulation results to demonstrate the workability of the proposed structure. The CMOS implementation of the CFCC shown in Fig. 6.5.1 using 0.18 micron TSMC process technology has been used to verify the workability of the circuit presented in this paper. The values of the DC bias currents and voltages were taken as 40 μA and ± 2.5V respectively. Aspect ratios of the various MOSFETs were taken as shown in Table 6.5.1. The proposed oscillator was designed for a frequency of 1.59 MHz by appropriately selecting the passive components as follows: C_1= C_2=10 pF, R_1=10 kΩ, R_2=10700 Ω, R_3=10 kΩ, R_4=10 kΩ,

R_5=10 kΩ. From SPICE simulations the oscillation frequency was found to be 1.50 MHz. The output waveforms for $I_{o1}$and I_{o2} are shown in Fig.6.5.2 (a) and the quadrature relationship of the generated waveform is indicated by the Lissajous pattern shown in Fig.6.5.2 (b). The measured phase difference was found to be 90.91°. We have calculated the phase difference using the values of different parasitic resistances and capacitances given in Table 6.4.1 as per equation (6.4.6) and found it to be equal to 89.52° for a design frequency of 1.59 MHz. The FFT for current outputs $I_{o1}$and I_{o2} are shown in Fig.6.5.3(a) and (b) respectively. Total harmonic distortion (THD) for current output I_{01} was found to be 3.2 % and for current output I_{02} as 5.3 %.

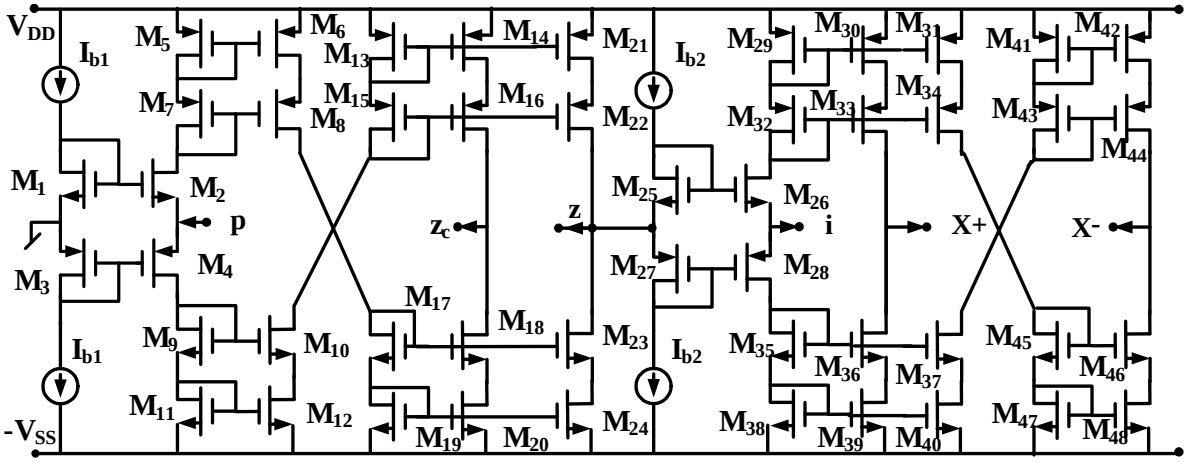
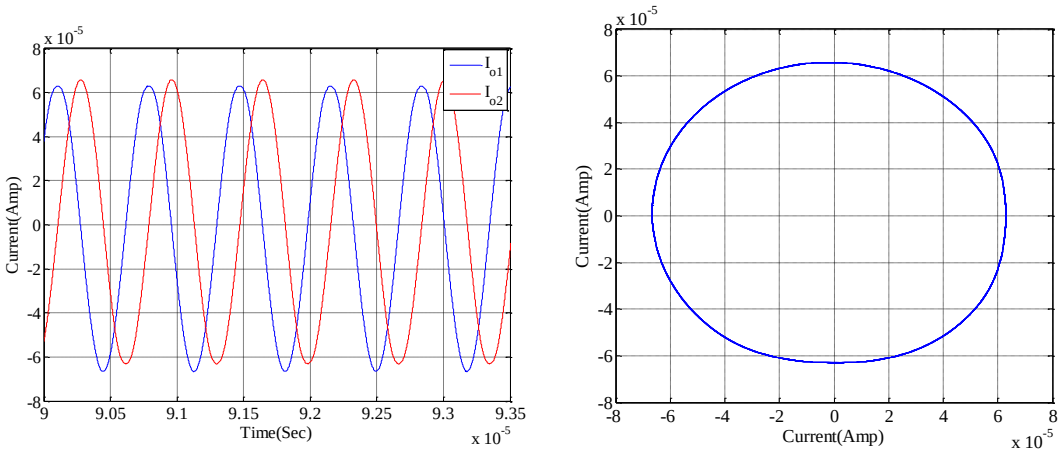


Fig.6.5.1 An exemplary CMOS implementation of the ZC-CFCC [see chapter 2]

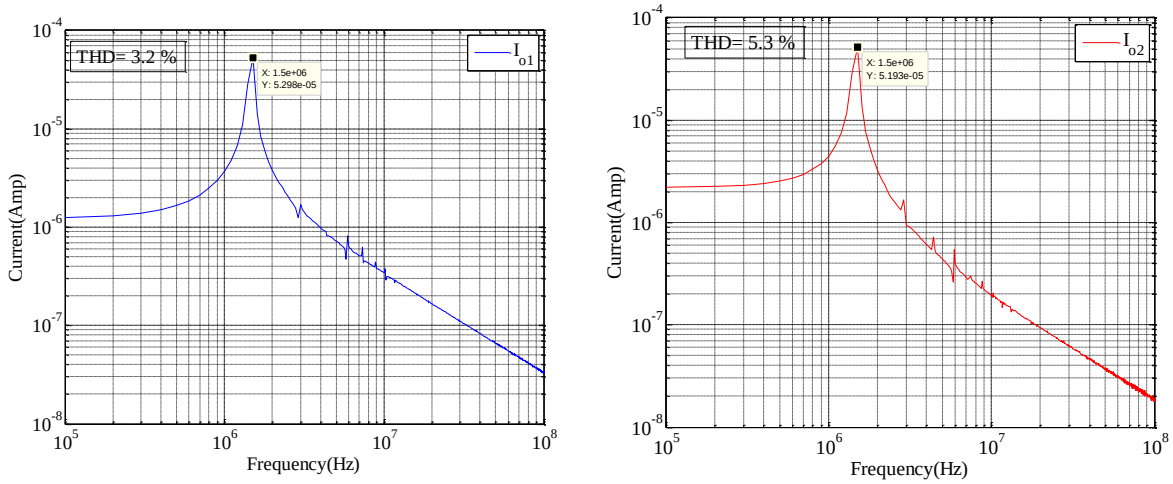
Table 6.5.1 Aspect ratios of the MOSFETs used in the ZC-CFCC realization

MOSFETs	W/L (µm/µm)
M_1, M_2, M_{25}, M_{26}	25/0.25
M_3, M_4, M_{27}, M_{28}	50/0.25
M_5 - M_{24}, M_{29} -M_{48}	2.5/0.25



(a) (b)

Fig.6.5.2 PSPICE Simulation Results (a) Quadrature oscillator waveforms (b) Lissajous pattern

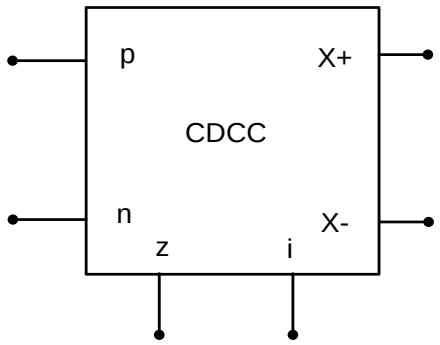


(a) (b)

Fig.6.5.3 FFT of the waveforms of $I_{o1}$and I_{o2} at 1.50 MHz

6.6 CDCC-based realization of current-mode quadrature oscillator

As explained earlier, CDCC [2] is a six-terminal ABB whose symbolic representation and port relations are shown in Fig.6.6.1. The current at the 'z' terminal is the difference of the two input currents and the potential at the terminal 'i' tracks the potential at the terminal 'z'. Two complementary currents at the output terminals 'x+' and x- are available which are copies of the current leaving the 'i' terminal.

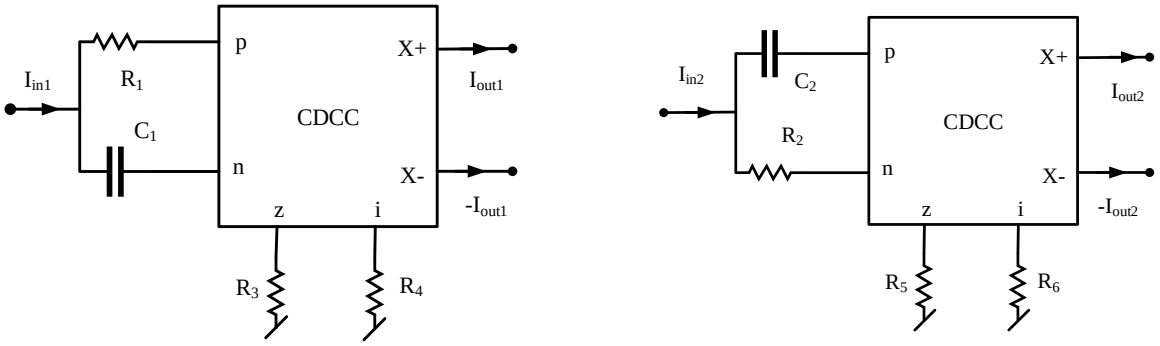


$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_i \end{bmatrix} \qquad (6.6.1)$$

Fig.6.6.1 Symbolic notation and port-relations of the CDCC

All pass (AP) filters are widely used in analog signal processing in order to shift the phase while keeping the amplitude constant, to produce various types of filter characteristics and to implement high-Q frequency selective circuits. The current transfer function for the AP filter of Fig.6.2.2 (a) is

$$H_1(s) = \frac{I_{out1}(s)}{I_{in1}(s)} = \frac{R_3(1 - sR_1C_1)}{R_4(1 + sR_1C_1)} \qquad (6.6.2)$$



(a) (b)

Fig.6.6.2 Two variants of CDCC-based current mode all pass filters

The circuit of Fig. 6.6.2 (a) provides a phase shift of

$$\varphi_1(\omega) = -2\arctan(\omega R_1 C_1) \qquad (6.6.3)$$

The current transfer function for the AP filter of Fig.6.2.2 (b) is

$$H_2(s) = \frac{I_{out2}(s)}{I_{in2}(s)} = -\frac{R_5(1 - sR_2C_2)}{R_6(1 + sR_2C_2)} \tag{6.6.4}$$

This circuit provide a phase shift of

$$\varphi_2(\omega) = 180^0 - 2\arctan(\omega R_2C_2) \tag{6.6.5}$$

The proposed current-mode quadrature oscillator circuit is shown in Fig.6.6.3.

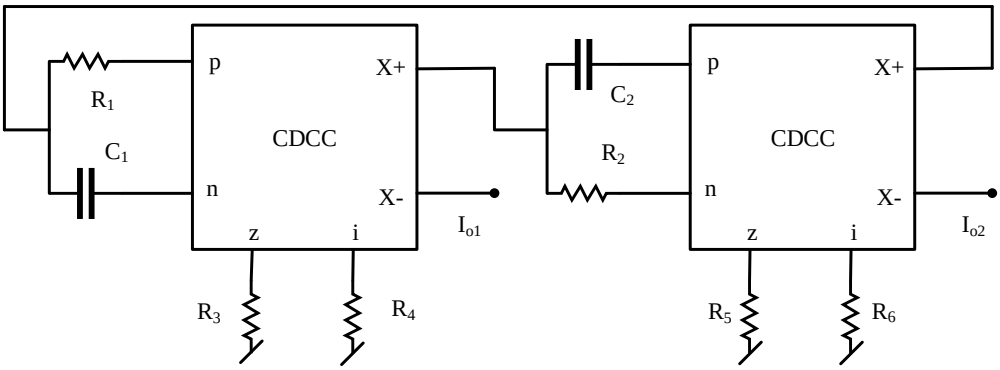


Fig.6.6.3 Proposed CDCC-based current mode quadrature oscillator

A routine analysis of the circuit given in Fig.6.6.3 yields the following characteristic equation (CE):

$$s^2R_1R_2C_1C_2\left(1 + \frac{R_3R_5}{R_4R_6}\right) + s\left(R_1C_1 + R_2C_2\right)\left(1 - \frac{R_3R_5}{R_4R_6}\right) + \left(1 + \frac{R_3R_5}{R_4R_6}\right) = 0 \tag{6.6.6}$$

From equation (6.6.6), the condition of oscillation (CO) and frequency of oscillation (FO) is given by

CO:

$$R_4R_6 = R_3R_5 \tag{6.6.7}$$

FO:

$$\omega_{0sc} = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{6.6.8}$$

It may be noted that if we select $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then the current outputs I_{01} and I_{02} will constitute a quadrature pair. The characteristic equation thus reduces to

$$s^2R^2C^2\left(1+\frac{R_3R_5}{R_4R_6}\right)+2sRC\left(1-\frac{R_3R_5}{R_4R_6}\right)+\left(1+\frac{R_3R_5}{R_4R_6}\right)=0 \qquad (6.6.9)$$

from equation (6.6.7) and (6.6.8) it is clear that both CO and FO are independently controlled by different passive resistances.

6.7 Non-ideal consideration

We have constructed a non-ideal model of the proposed oscillator circuit by considering R_p and R_n as the parasitics associated with p and n ports of the CDCC respectively with R_i representing the output resistance of the voltage buffer implemented between port z and port i. The parasitic resistance and parasitic capacitance of the z port of CDCC R_z and C_z and the the parasitic resistance and parasitic capacitance of the x+ port and x- port of CDCC(R_{x+} , C_{x+} , R_{x-} and C_{x-}) have also been considered in the non-ideal equivalent circuit shown below in Fig. 6.7.1.

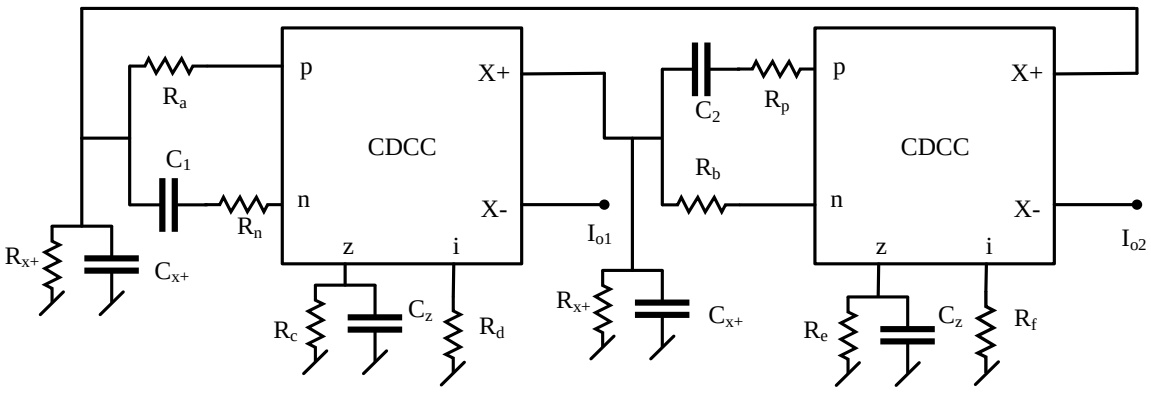


Fig.6.7.1 Non-ideal model of CDCC based current mode quadrature oscillator

A routine analysis of the circuit shown in Fig. 6.7.1 gives the following eighth ordered characteristic equation

$$R_c R_e R_x^2[\{1+sC_1(R_n-R_a)\}\{sC_2(R_b-R_p)-1\}(1+sC_1R_n)(1+sC_2R_p)]-$$
$$R_d R_f[\{1+s(R_nC_1+R_cC_z)+s^2R_nC_1R_cC_z\}\{1+s(R_eC_z+R_pC_2)+s^2R_eC_zR_pC_2\}$$
$$\{R_b+R_x+s(R_bR_pC_2+R_xR_pC_2+R_xR_bC_2+R_xR_bC_x)+s^2R_xR_pR_bC_xC_2\}$$
$$\{R_a+R_x+s(R_aR_nC_1+R_xR_nC_1+R_xR_aC_1+R_xR_aC_x)+s^2R_xR_nR_aC_xC_1\}]=0 \quad (6.7.1)$$

We have measured the values of the various parasitic resistances and capacitances of the CDCC employed in the present work (see Fig. 6.8.1) by carrying out detailed PSPICE simulations. The measured values of these non-ideal parameters are summarized in Table 6.7.1.

Table 6.7.1 The SPICE-measured values of the various parasitics of the CMOS CDCC

S.No.	Parameter	Value
1	R_p	591Ω
2	R_n	591Ω
3	R_z	4.9389MΩ
4	C_z	6.2988×10^{-14}F
5	R_i	591Ω
6	R_{x+}	4.9862 MΩ
7	C_{x+}	7.3954×10^{-15}F
8	R_{x-}	4.7752 MΩ
9	C_{x-}	7.4062×10^{-15}F

The following approximations (ensured by selecting appropriate values of the terminating resistances and capacitances) $R_{x+}>>(R_1+R_p)$, $R_{x+}>>(R_2+R_n)$, $R_z>>R_3$, $R_z>>R_5$, R_4, $R_6>>R_i$ and C_1 ,$C_2>>C_{x+}$ leads to the second order approximation given by

$$s^2R_aR_bC_1C_2\left(1+\frac{R_dR_f}{R_cR_e}\right)+s\left(R_aC_1+R_bC_2\right)\left(1-\frac{R_dR_f}{R_cR_e}\right)+\left(1+\frac{R_dR_f}{R_cR_e}\right)=0 \quad (6.7.2)$$

where $R_a=R_1+R_p, R_b=R_2+R_n$, $R_c=R_3\,||\,R_z, R_d=R_4+R_i, R_e=R_5\,||\,R_z$ *and* $R_f=R_6+R_i$

From equation (6.7.2), the condition of oscillation (CO) and frequency of oscillation (FO) is given by

CO:

$$\left(R_4 + R_i\right)\left(R_6 + R_i\right) = \left(R_3 \parallel R_z\right)\left(R_5 \parallel R_z\right) \tag{6.7.3}$$

FO:

$$\omega_{osc}^{'} = \frac{1}{\sqrt{R_a R_b C_1 C_2}} = \frac{1}{\sqrt{R_1 R_2 C_1 C_2 \left(1 + \frac{R_p}{R_1}\right)\left(1 + \frac{R_n}{R_2}\right)}} = \frac{\omega_{0sc}}{\sqrt{\left(1 + \frac{R_p}{R_1}\right)\left(1 + \frac{R_n}{R_2}\right)}} \tag{6.7.4}$$

From equation (6.7.3) and (6.7.4) it is evident that, even under the influence of parasitics, the independent controls of CO and FO remain intact; that of the former through R_3, R_4, R_5 R_6 and that of latter through R_1 and/or R_2, subject to the fulfilment of the approximations mentioned earlier. Further, if we choose R_1 and R_2 much larger than R_p and R_n, the error in oscillation frequency will be less.

6.8 PSPICE simulation results

We now present some SPICE simulation results to demonstrate the workability of the proposed structure. The CMOS implementation of the CDCC shown in Fig. 6.8.1 using 0.18 micron TSMC process technology has been used to verify the workability of the circuits presented in this paper. The values of the DC bias currents and voltages were taken as 40 µA and ± 2.5V respectively. Aspect ratios of the various MOSFETs were taken as shown in Table 6.8.1. The proposed current mode quadrature oscillator was designed for a frequency of 2 MHz by appropriately selecting the passive components as follows: C_1= C_2=10 pF, R_1=7.95 kΩ, R_2=7.95 kΩ, R_3=10 kΩ, R_4=10 kΩ, R_5=10 kΩ, and R_6= 6.8 kΩ. As the parasitic input resistances at the ports p, n and i are about 0.591 kΩ and thus cannot be ignored with respect to the external impedances connected at these ports hence, they have been absorbed in the external resistors R_1, R_2, R_4 and R_6 to compensate for their

adverse effect for which these resistances have been *pre-distorted* by subtracting 0.591 kΩ from their design values. The output frequency in simulation was found to be 1.9 MHz. The output waveforms are shown in Fig.6.8.2 (a).For generated waveforms quadrature relationship has been confirmed by Lissajous pattern shown in Fig. 6.8.2 (b) (the phase difference was found to be 89.89^{o}) . Fig.6.8.3 shows the FFT response of the quadrature oscillator. Total harmonic distortion for current output I_{01} was found to be 3.6 % and for current output I_{02} as 7.5 %.

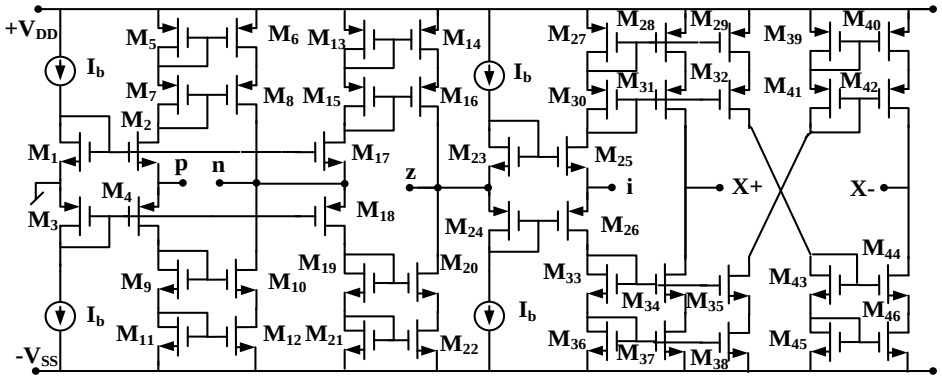
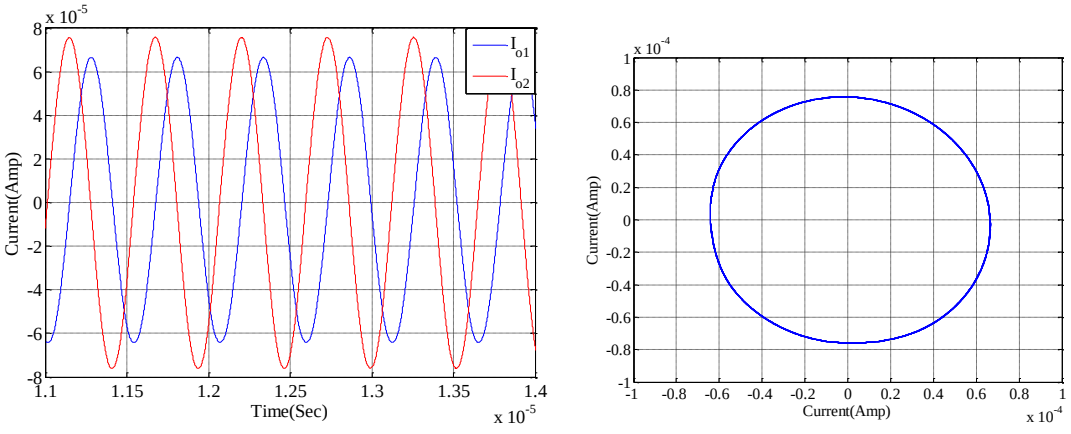


Fig.6.8.1 CMOS implementation of the CDCC [chapter 2]

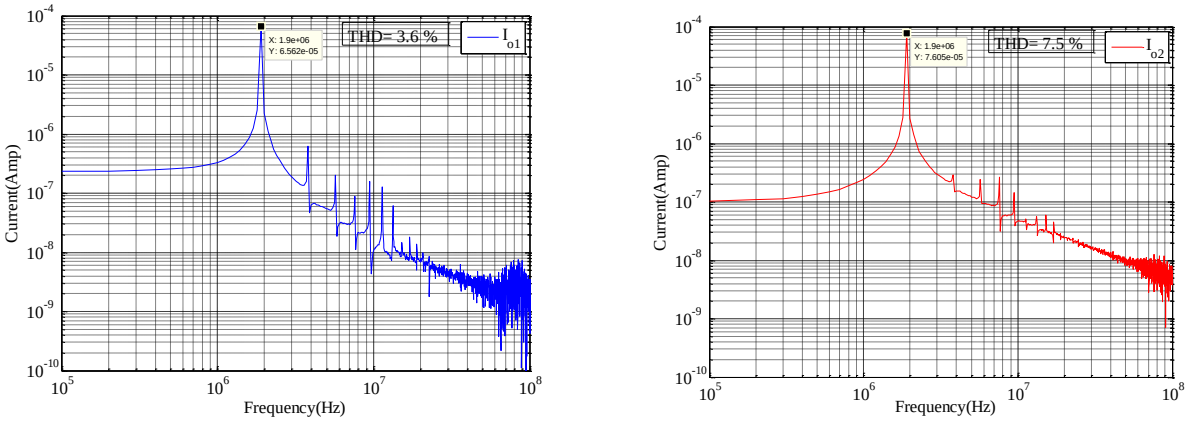
Table 6.8.1 Aspect ratios of MOSFETs used in CDCC realization

MOSFETs	W/L (µm/µm)
M_1, M_2, M_{17}, M_{23}, M_{25}	25/0.25
M_3, M_4, M_{18}, M_{24}, M_{26}	50/0.25
M_5 - M_{16}, M_{19} - M_{22}, M_{27} - M_{46}	2.5/0.25



(a) (b)

Fig.6.8.2 PSPICE Simulation Results (a) Quadrature oscillator waveforms (b) Lissajous pattern



(a) (b)

Fig.6.8.3 FFT response of designed oscillator at 2 MHz

6.9 Experimental results

Since the CDCC block is not available as an off-the shelf IC, for hardware implementation, we have used commercially available IC AD844 to implement the CDCC block. The schematic and hardware realization of the proposed CDCC based quadrature oscillator using AD 844ICAs have been shown in Fig 6.9.1 (a) and Fig 6.9.1 (b) respectively. The proposed current mode quadrature oscillator circuit was designed for an oscillation frequency of f_0 = 28.40 KHz by appropriately selecting the passive components as follows: R_1=5.6 kΩ, R_2=5.6 kΩ, R_3=10 kΩ, R_4=10 kΩ, R_5=10 kΩ, R_6=2.2 kΩ+7.2 kΩ (10 kΩ variable pot), R_{L1}=10 kΩ R_{L2}=10 kΩ and C_1=1 nF and C_2=1 nF. Fig.6.9.2 and Fig.6.9.3 shows the experimental results. The measured frequencies of the two quadrature outputs were found to be 28.99 kHz and 29.04 kHz.

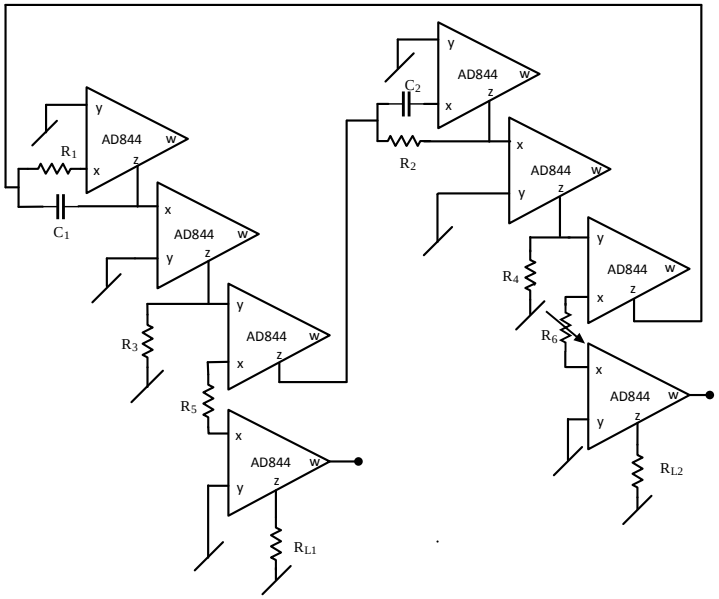


Fig. 6.9.1(a) Schematic realization of the proposed CDCC-based oscillator using AD844 ICs

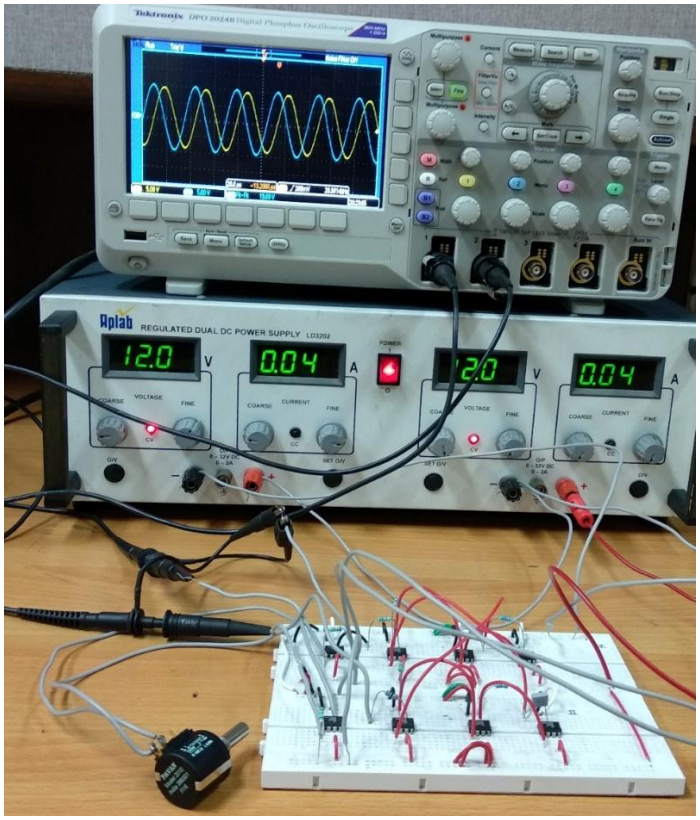
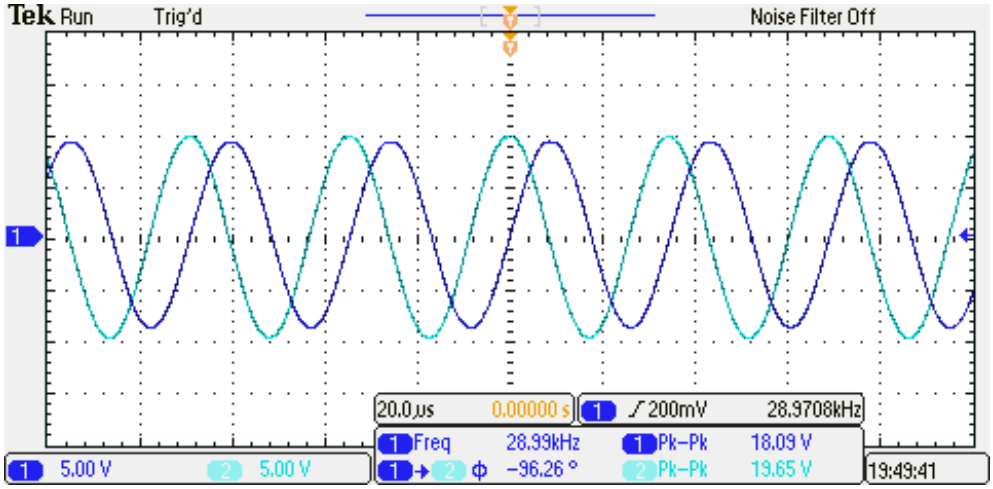
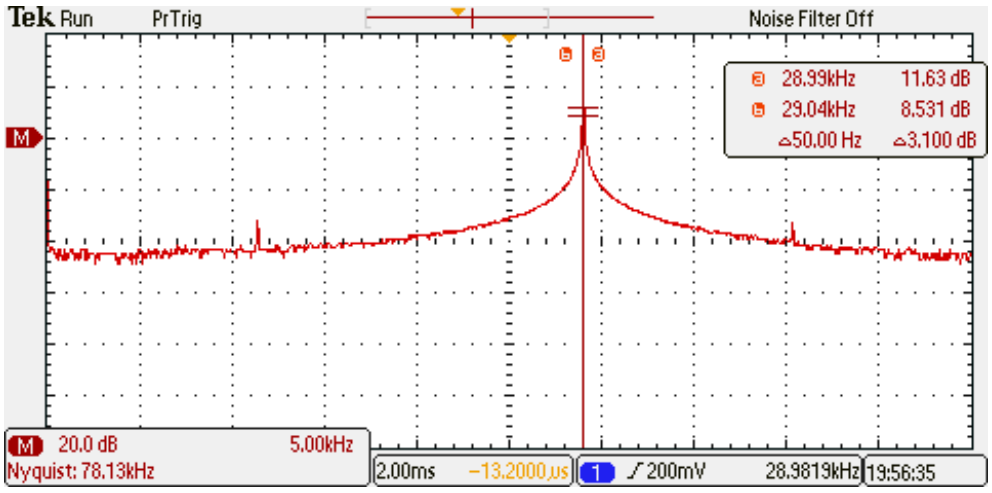


Fig. 6.9.1(b) Hardware realization of the proposed CDCC-based oscillator using AD844 ICs



(a)



(b)

Fig.6.9.2 Hardware results of quadrature oscillator (a) Transient response (b) FFT waveform

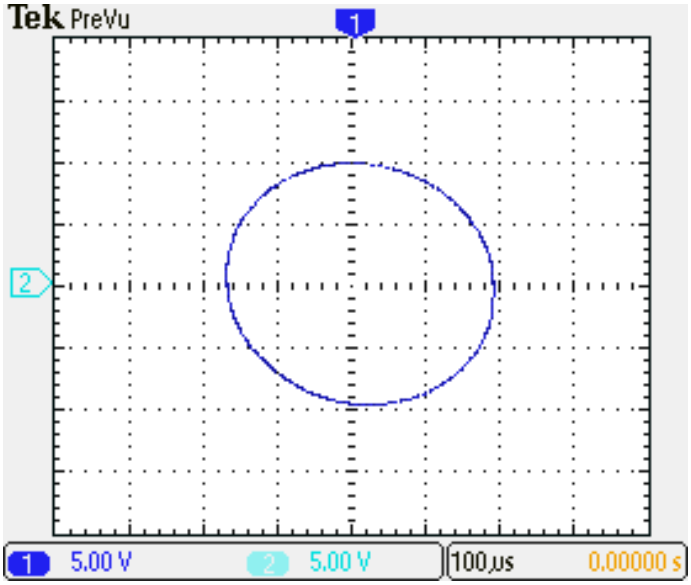


Fig.6.9.3 Lissajous pattern of proposed quadrature oscillator

6.10 Concluding remarks

In this chapter, three new quadrature oscillator circuits have been presented. Two of the quadrature oscillator circuits are implemented using the resonator-negative resistor concept; the resonator as well as the negative resistors have been implemented using some of the lossy and lossless immittance simulators presented in chapter 3. These quadrature oscillators employ one CFCC, one ZC-CFCC and five resistors and one capacitor. The quadrature outputs are available in the form of currents at high output impedance terminals. The workability of CFCC-based circuit has been established by SPICE simulations based on a CMOS CFCC implementable in 0.18 μm CMOS technology. The third quadrature oscillator circuit is based on two allpass filters in a loop configuration and uses CDCC as active elements. The circuit employs six resistors and two capacitors. The circuit offers decoupled control of CO and FO of the quadrature oscillator and the quadrature current outputs are again available at high output impedance A hardware realization of the CDCC using off-the shelf available component (AD844 CFOA) and PSPICE simulations using a CMOS CDCC have been used to realize this quadrature oscillator. The chapter has, thus, added a new application of the CFCC and CDCC in the area of quadrature oscillator realization, whose applications so far were explored in this thesis only in the realization of the simulated impedances of various kinds and fully differential filters.

6.11 References

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Chapter 7

Conclusions

Summary of the work carried out in the thesis has been presented and some suggestions for further research have been made.

The last few decades have seen the emergence of a very large number of active building blocks which have come as a consequence of developments in CMOS technology. These active building blocks offer certain additional degree of freedom to the circuit designers in development of various analog signal processing circuits. For instance, the inductance simulation circuits realized with off-the shelf available components required some passive component matching constraints for the realization of ideal/floating inductances. But many immittance simulation circuits realized with these modern active building blocks do not require any passive component matching constraints. Similarly, it becomes very easy to control the various parameters of the realized circuits electronically when these circuits are realized with the modern active building blocks. The additional degree of freedom which these building blocks provide mainly comes from the facts that these blocks combine the features of functionally different discrete building blocks like operational amplifiers, operational transconductance amplifiers, current conveyors and current feedback amplifiers. It is relatively easy to make multiple copies of some intermediate currents using current mirrors in modern day IC fabrication technology.

We have chosen current differencing current conveyor (CDCC) and some of its variants which were proposed alongwith a host of new active building block in [reference 21 of chapter1] as they have received very little attention in realization of various analog signal processing applications. The various circuits using CDCC, CFCC, ZC-CFCC, ZC-CFCCC etc. proposed in this thesis have been verified using CMOS implementation. It must be mentioned that since the work reported in this thesis covers a relatively longer span (Nov. 2011 onwards) some of the earlier results have been based upon 0.35 μm CMOS technology, however, the relatively more recent onces have employed the more prevalent 0.18 μm CMOS technology.

7.1 Summary of the Work Presented in the Thesis

In chapter 1 of the thesis after discussing the general features of analog signal processing, from the point of view of low voltage and current-mode operations, a brief overview of the off-the-shelf available components used in analog signal processing has been presented. The developments in the area of new active building blocks which have taken place during the last two decades have also been presented. The behavioral models of the active building block CDCC, CFCC and the other active elements proposed in [reference 21of chapter 1] have been presented. The behavioral model of CDCC and CFCC has been used to propose CMOS realization of these blocks. Finally PSPICE–based characterization of these blocks has also been presented in this chapter.

In chapter 2 of the thesis six new CDCC-based single input multi-output (SIMO) type fully differential current mode universal filters (FDCMUF) have been presented. These circuits give explicit current output for all the five filters from high output impedance nodes. The seven–CDCC based FDCMUF has all the filter parameters independently tunable. Apart from seven CDCCs, the filter employs only eight grounded resistances and two grounded capacitors. The six/five CDCC-based versions of this filter have two/one independently tunable parameters but possess all other properties of their seven-CDCC based predecessor. The number of passive elements used in these circuits is minimum when compared with other fully differential universal filter circuits with similar tunability properties and compares well with a single ended electronically tunable biquad filter with similar tunability properties. All the proposed fully differential biquad filters use only two capacitors, a novel feature not present in earlier circuits except the circuit presented in [reference 6-8 of chapter 2]. It may however be pointed that in these filters some of the passive elements are floating in contrast to the circuits proposed in this thesis where all the passive elements are grounded.

In chapter 3 of the thesis a number of new grounded immittance simulation circuits (six lossy inductors, one positive lossless inductor, one negative lossless inductor and a frequency dependent negative resistor) have been proposed. All the simulated immittance circuits employ only a single CFCC along with a canonical number of passive elements without requiring any passive component-matching conditions. When compared with the previously known circuits, the proposed active immittance circuits possess following advantageous features simultaneously (i) use of a single ABB (ii) employment of a cannonic number of RC elements (iii) use of grounded capacitor in several cases (iv) complete absence of any passive element matching conditions (v) electronic tunability through an external voltage signal (vi) reasonably low-voltage operation coupled with very low-power consumption and (vii) suitability for CMOS implementation. Simulated inductor has been used to implement RLC resonator derived highpass filter, bandpass filter and a fourth order Butterworth highpass filter. The simulated FDNR is used to realize second order RCD lowpass filter.

In chapter 4 of the thesis new electronically-tunable, lossless grounded and floating inductance simulation circuits using the ZC-CFCCC as active element have been presented. In these circuits the input impedance of the current follower and the output impedance of the voltage follower employed in the realization of the ZC-CFCCC have been used as design parameters as these impedances can be controlled by DC bias current in the translinear implementation of these followers. These circuits employ only a single ZC-CFCCC for grounded inductance simulation and two ZC-CFCCCs for floating inductance simulation along with a single grounded capacitor as preferred for IC implementation. These new circuits provide a number of advantageous features simultaneously such as: (i) use of a canonic number of active and passive elements (ii) electronic tunability by means of external bias currents (iii) complete absence of passive component matching and (iv) employment of a single grounded capacitor, as preferred for IC implementation. For simulation of floating inductance, the only constraint

required is the equality of the two bias currents, which can be easily met by using current copier cells. A tunable second order RLC band pass filter and a fourth order low pass Butterworth filter are realized using the proposed inductors.

In Chapter 5 a general methodology for the realization of nth order (n≥3) fully-differential current-mode filters using CDCC has been presented. The presented circuits employ all grounded passive elements. In contrast to earlier known realizations of fully-differential filters which invariably require more than one capacitors per pole, the proposed realization employs only one capacitor per pole. The cut-off frequency of the realized filter can be electronically tuned when all the grounded resistors associated with the integrators are implemented by identical CMOS grounded voltage-controlled-resistors driven by a common control voltage. The methodology has been illustrated by realizing fifth order Butterworth filter, and fifth order Chebychev filters as specific examples whose workability has been verified using SPICE simulations in 0.18 µm TSMC technology. A reduced-component-version of the designed fifth order Butterworth filter has also been presented which also employs all grounded RC components but does not have electronic-tunability.

In chapter 6 of this thesis three new quadrature oscillator circuits have been presented. Two of the quadrature oscillator based circuits are implemented using the resonator-negative resistor concept, The resonator as well as the negative resistors have been implemented using some of the lossy and lossless immittance simulators presented in chapter 3. These quadrature oscillators employ one CFCC, one ZC-CFCC and five resistors and one capacitor. The quadrature outputs are available in the form of currents at high output impedance terminals. The workability of CFCC-based circuit has been established by SPICE simulations based on a CMOS CFCC implementable in 0.18 µm CMOS technology. The third quadrature oscillator circuit is based on two allpass filters in a loop configuration and uses CDCC as active elements. The circuit employs six resistors and two capacitors. The circuit offers decoupled control of

CO and FO of the quadrature oscillator and the quadrature current outputs are again available at high output impedance A hardware realization of the CDCC using off-the shelf available component (AD844 CFOA) and PSPICE simulations using a CMOS CDCC have been used to realize this quadrature oscillator. The chapter has, thus, added a new application of the CFCC and CDCC in the area of quadrature oscillator realization, whose applications explored so far were only in the realization of the simulated impedances of various kinds and fully differential filters [chapter 2, 3, and 4].

7.2 Some suggestions for further work

The work reported in this thesis has mainly been concerned with the realization of fully-differential current-mode biquad filters, lossy and lossless grounded immittance simulators electronically tunable grounded and floating inductance simulators, fully differential higher order filters and sinusoidal oscillator circuits using CDCC and its variants like CFCC, ZC-CFCC and ZC-CFCCC. The work reported in this thesis has proved that besides many applications, CDCC is a particularly attractive active building block for fully differential current-mode signal processing.

However, the class of circuits investigated in this thesis has not completely exhausted the scope of the work which can be done on CDCCs. In the following we point out some of the directions in which the present work may be extended.

(i) In chapter 2 we presented the realization of fully-differential current-mode biquad filters based on the two-integrators in a loop topology. Several other topologies exist in the literature for realization of biquad filters in which the number of active building blocks needed are lesser. These topologies may be attempted for the realization of single-CDCC based fully differential biquad filters.

(ii) In chapter 3 we have presented a set of lossy and lossless grounded immittance simulators. These immittance simulators may be investigated systematically for realization of single resistance controlled current-mode oscillators with fully-decoupled control of CO and FO

(iv) In chapter 5 of the thesis we have presented a general methodology for realization of fully-differential current-mode higher order filters. In this class (higher-order) of filters very few publications exist in which multiple filter outputs are available, thus, the CDCC-based design of multifunction fully-differential higher order filters appears to be yet another interesting research problem for future investigations.

Thus, there appears to be enough scope for further extending the work presented in this thesis.

List of Research Papers

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A Novel Fully Differential Current Mode Universal Filter

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Abstract–In this communication, one of the recently proposed active building block namely Current Differencing Current Conveyor (CDCC) has been used to design a current mode universal filters in fully differential form. The proposed universal filter has the property of independently tuneable gain, bandwidth and pole frequency. Workability of the proposed circuit has been verified using PSPICE simulation based CMOS CDCC implemented in 0.35micron CMOS technology.

Keywords: **CDCC, Fully differential circuits, Universal biquad filter.**

I. INTRODUCTION

Fully differential filters offer many advantages compared to their single-ended counterparts in terms of higher rejection capabilities to clock-feed through, charge injection errors and power supply noise. These filter structures have inherently large dynamic range and reduced harmonic distortion [1]. Because of these attributes fully differential filters have started receiving greater attention from the analog circuit designers in mixed mode circuit solutions where both analog as well as digital circuits are integrated on same chip. Many active building blocks have been used for designing fully differential filters in current mode during the past decades. In [2] modified multiple output differential difference current conveyor has been used to design second order fully differential bandpass(BP) and lowpass(LP) filters in which eight grounded passive elements(4R-4C)are used. In [3] a CMOS fully balanced four terminal floating nullor has been used to design fully differential current mode universal filter in which three active elements (FBFTFNs) and ten passive components (all floating) are used. The passive components are floating and there are components matching constraints for the realization of all pass and band elimination filters. In [4] differential input balanced output current operational amplifiers have been used to realize current mode LP and BP filters with as many as fourteen passive components (10R-4C) in which all the passive components are floating except output current resistor.

In [5] differential wave port terminators are used to design differential wave active filters in which eight capacitors are used to simulate a third order elliptic wave filter in fully differential form.A fully differential current mode universal filter has been presented in [6] which is based on the nullor concept and uses six passive elements (2R-4C) and six current conveyors.The filter does not have independent tuneability of all parameters.

In [7] fully differential transconductors have been used to realize a current mode third order fully differential Butterworth low pass Gm-C filter in which seven differential transconductors and six grounded capacitors are used. In [8] current controlled fully balanced second generation current conveyors have been used to design eight multiple feedback loop based higher order filters in which the number of grounded capacitors required is double the number of grounded capacitors required for the single-ended version of the filter. In [9] two fully differential adjustable bandpass filters have been proposed. The circuit uses multiple current followers and digitally adjustable current amplifiers in which six passive elements (4R-2C) and five to seven active elements have been used. The circuit 'Q' can be adjusted by the adjusting the gain 'A' of the amplifier.

In this paper we present a fully differential current mode universal filter which uses a Current Differencing Current Conveyor (CDCC) [10] as the active building block. The pole frequency f_0 the bandwidth Δf and the relevant gain H are independently tuneable. The circuit employs only grounded passive elements.

II. CDCC-BASED FULLY DIFFERENTIAL CURRENT-MODE UNIVERSAL FILTER

The CDCC is a six-terminal device whose block diagram and port relations are given below in Fig.1. This active building block is especially suited for fully differential current mode signal processing as it has differential input terminals as well as fully balanced output terminals.

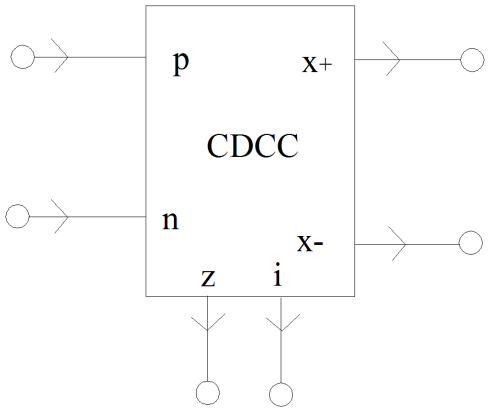

Fig.1 Symbolic notation and Port relations of CDCC

$$I_z = I_p - I_n \tag{1a}$$

$$V_i = V_z \tag{1b}$$

$$I_{x+} = I_i = -I_{x-} \tag{1c}$$

and

$$V_p = V_n = 0 \tag{1d}$$

The fully differential current mode universal filter is shown below in Fig.2.

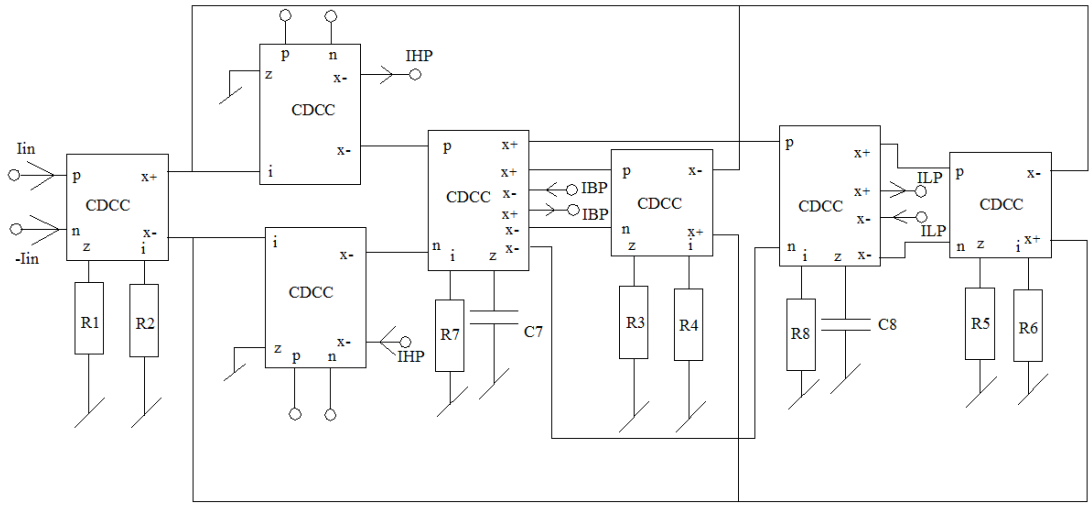

Fig.2 Fully Differential Current Mode Universal Filter employing seven CDCC with independently tunable gain, bandwidth and pole frequency

A routine analysis of the circuit given above using the terminal equations of the CDCC gives the following current transfer functions:

$$\frac{I_{HP}}{I_{in}} = H_{HP}\frac{s^2}{\Delta}$$

$$\frac{I_{BP}}{I_{in}} = H_{BP}\frac{2sK_2}{R_7C_7\Delta}$$

$$\frac{I_{LP}}{I_{in}} = H_{LP}\frac{4K_3}{R_7R_8C_7C_8\Delta}$$

Where

$$\Delta = s^2 + 2s\frac{K_2}{R_7C_7} + 4\frac{K_3}{R_7R_8C_7C_8};$$

$$K_1 = 2\frac{R_1}{R_2}; K_2 = 2\frac{R_3}{R_4}; K_3 = 2\frac{R_5}{R_6};$$

$$H_{HP} = K_1; H_{BP} = \frac{K_1}{K_2} \text{ and } H_{LP} = \frac{K_1}{K_3}$$

The highpass (HP) and lowpass (LP) outputs can be combined to get the band elimination (BE) response (for $K_3 = 1$) and the high pass, complementary bandpass (BP) and lowpass responses ($for K_2 = K_3 = 1$) can be combined to get the all pass (AP) response. From the transfer functions given above the various parameters of the biquad filter are found to be

$$H_{HP} = K_1 = 2\frac{R_1}{R_2};\ H_{BP} = \frac{K_1}{K_2} = \frac{R_1R_4}{R_2R_3}$$
$$and\ H_{LP} = \frac{K_1}{K_3} = \frac{R_1R_6}{R_2R_5} \quad (2a)$$

$$f_0 = \frac{1}{\Pi}\sqrt{\frac{K_3}{R_7R_8C_7C_8}} \quad (2b)$$

$$\Delta f = \frac{1}{\Pi}\frac{K_2}{R_7C_7} \quad (2c)$$

From the above expressions it may be noted that the pole frequency f_0 for the filters can be tuned by tuning the coefficient K_3 without changing either the bandwidth Δf or the relevant gains for the highpass, bandpass and lowpass responses. Similarly the bandwidth Δf can be tuned by varying K_2 without changing either the pole frequency or the relevant gains. Finally the relevant gains can also be tuned by changing K_1,K_2 and K_3.

III. NON IDEALITY ANALYSIS

From the structure of the current mode fully differential universal filter given in Fig. 2 it is interesting to note that the parasitic immittances associated with z and i terminals of various CDCCs can very easily be compensated in the terminating impedances at these terminals. In the following we present an analysis of the circuit given in Fig. 2 which takes into account the various frequency independent tracking errors associated with different voltage and current transfers.

$$I_{kz} = \alpha_{kp}I_p - \alpha_{kn}I_n \quad (3a)$$

$$V_{ki} = \beta_k V_{kz} \quad (3b)$$

$$I_{kx} = \alpha_{ki}I_{ki} \quad (3c)$$

$$V_p = V_n \quad (3d)$$

α_{kp} and α_{kn} represent the current tracking coefficients between the p and n terminals of the CDCC to its z terminal while α_{ki} represents the current tracking error between the terminal i and x of the kth CDCC (k=1-7). Similarly β_k represents the voltage tracking coefficient between the terminal z and i of the kth CDCC. These coefficients will have a nominal value which is very close to unity. The modified transfer functions of the circuit are given below as:

$$\frac{I_{HP}}{I_{in}} = \frac{s^2\alpha_{2i}K_1\beta_1\alpha_{1i}(\alpha_{1p}+\alpha_{1n})}{2D(s)}$$

$$\frac{I_{BP}}{I_{in}} = \frac{sK_1\alpha_{2i}\beta_1\alpha_{1i}(\alpha_{1p}+\alpha_{1n})\alpha_{4i}\beta_4(\alpha_{4p}+\alpha_{4n})}{2C_7R_7D(s)}$$

$$\frac{I_{LP}}{I_{in}} = \frac{A}{2C_7C_8R_7R_8D(s)},$$

where

$$A := \alpha_{6i}\beta_6\alpha_{4i}\beta_4 K_1\alpha_{2i}\beta_1\alpha_{1i}(\alpha_{1p}+\alpha_{1n})(\alpha_{4p}+\alpha_{4n})(\alpha_{6p}+\alpha_{6n}),$$

$$D(s) = s^2 + s\frac{K_2\alpha_{5i}\beta_5(\alpha_{5p}+\alpha_{5n})\alpha_{4i}\beta_4(\alpha_{4p}+\alpha_{4n})}{2C_7R_7}$$
$$+\frac{K_3\alpha_{2i}\beta_7\alpha_{7i}(\alpha_{7p}+\alpha_{7n})\alpha_{6i}\beta_6(\alpha_{6p}+\alpha_{6n})\alpha_{4i}\beta_4(\alpha_{4p}+\alpha_{4n})}{2C_7C_8R_7R_8};$$

and

$$K_1 = 2\frac{R_1}{R_2}; K_2 = 2\frac{R_3}{R_4}; K_3 = 2\frac{R_5}{R_6}.$$

The f_0 and Q parameters can be written as follows:

$$f_0 = \frac{1}{2\Pi}\sqrt{\frac{B}{2C_7C_8R_7R_8}}$$

$$\Delta f = \frac{K_2\alpha_{5i}\beta_5(\alpha_{5p}+\alpha_{5n})\alpha_{4i}\beta_4(\alpha_{4p}+\alpha_{4n})}{4\Pi C_7R_7},$$

where

$$B := K_3\alpha_{2i}\beta_7\alpha_{7i}(\alpha_{7p}+\alpha_{7n})\alpha_{6i}\beta_6(\alpha_{6p}+\alpha_{6n})\alpha_{4i}\beta_4(\alpha_{4p}+\alpha_{4n}).$$

If $\alpha_{kp} = \alpha_{kn} = \alpha_{ki}$=0.98= β_k, the error in pole frequency is found to be 9.6 percent for a nominal design value of 1.8760 MHz. The active and passive sensitivities are not more than $\pm\frac{1}{2}$ in magnitude and magnitude of $\alpha_{kp}, \alpha_{kn}, \beta_k$ and $\alpha_{ki} < 1$.

IV. CDCC IMPLEMENTATION

A CMOS implementation of CDCC using current differencing unit ($M_1 - M_{22}$) and translinear current conveyor with complementary z outputs ($M_{22} - M_{46}$) is shown in Fig. 3. The aspect ratios details are given in Table1. The values of DC bias currents and voltages are $80\mu A$ and $\pm$ 5V respectively

V. SIMULATION RESULTS

The workability of the circuit given in Fig. 2 has been verified by PSPICE simulation with the CMOS CDCC shown in Fig.3. The fully differential current mode universal filter was designed to operate at the nominal values of f_0, Δf and H as 1.8759MHz, 2.6526MHz and 1 respectively. Fig. 4(a) shows the magnitude response of the universal filter with these nominal values. The parameters H, f_0 and Δf were tuned independently as per equation (2a), (2b), (2c) and the simulation results are shown in fig. 4(c)-4(e). The detailed results of simulations are summarized in table 2.

TABLE 1. Aspect ratios of MOSFETs used in CDCC realization.

MOSFETs	$W/L(\mu m/\mu m)$
$M_1, M_2, M_{17}, M_{23}, M_{25}$	$50/0.5$
$M_3, M_4, M_{18}, M_{24}, M_{26}$	$100/0.5$
$M_5 - M_{16}, M_{19} - M_{22}, M_{27} - M_{46}$	$3.33/0.5$

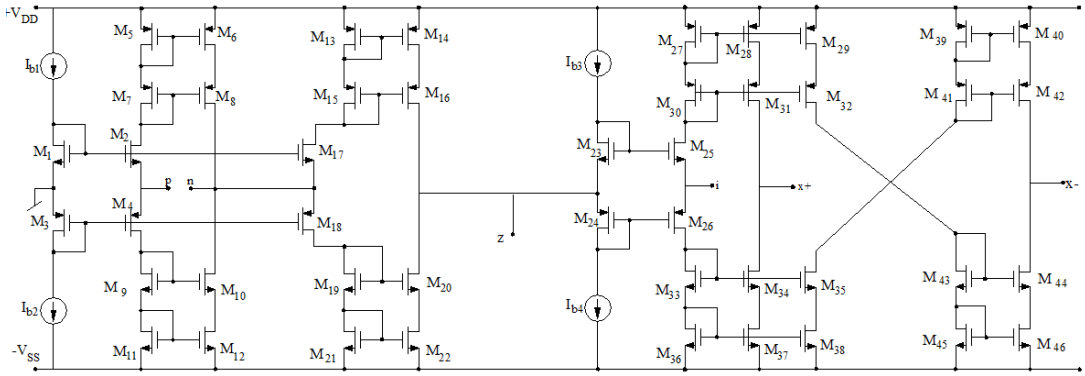

Fig.3 CMOS implementation of CDCC.

TABLE 2. Summary of calculated and simulated results.

Tuneability	Component values		Nominal Values(calculated)			Simulated values		
Gain(H)-Fig. 4 (c)			H	f_0 (MHz)	BW(MHz)	H(MHz)	f_0(MHz)	BW(MHz)
	$R_2 = R_4 = R_6$ =20kΩ; $R_3 = R_5 = R_7 = R_8$=10kΩ; C_7=12pF,C_8=24pF	R_1=10kΩ	1	1.8759	2.6526	1.0348	1.8197	2.5428
		R_1=20kΩ	2	1.8759	2.6526	2.0608	1.8197	2.5426
		R_1=50kΩ	5	1.8759	2.6526	5.0863	1.8197	2.5411
Pole Frequency (f_0) -Fig. 4(d)	$R_2 = R_4$= 20kΩ,R_6 =80kΩ $R_1 = R_3 = R_7 = R_8$=10kΩ; C_7=12pF,C_8=24pF	R_5=40kΩ	1	1.8760	2.6526	1.0428	1.8197	2.5002
		R_5=10kΩ	1	0.9380	2.6526	1.0068	0.9332	2.6116
		R_5=2.5kΩ	1	0.4690	2.6526	0.9992	0.4677	2.6359
Bandwidth (BW) -Fig. 4(e)	$R_2 = R_4 = R_6$ = 20kΩ $R_5 = R_7 = R_8$=10kΩ; C_7=12pF,C_8=24pF	$R_1 = R_3$ =20kΩ	1	1.8759	5.3052	1.0179	1.8197	5.5409
		$R_1 = R_3$ =10kΩ	1	1.8759	2.6526	1.0384	1.8197	2.5428
		$R_1 = R_3$ =5kΩ	1	1.8759	1.3263	1.0708	1.8197	1.1955

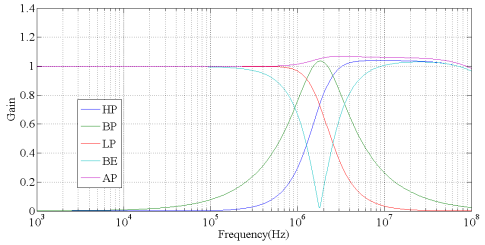

Fig. 4(a) Magnitude response of HP, BP, LP, AP & BE filters for a pole frequency of 1.8759 MHz.

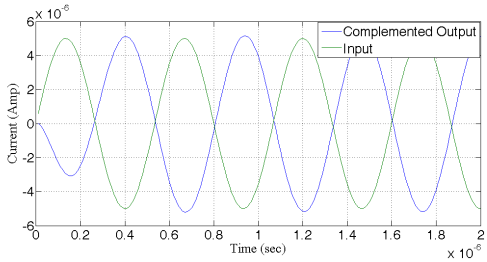

Fig.4 (b) Time response of the BP filter for an input of $5\mu A$ at 1.8759 MHz.

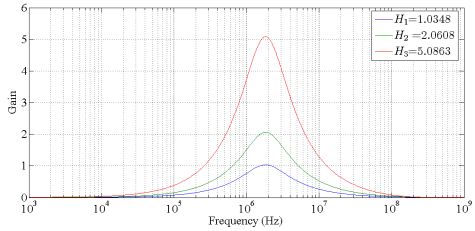

Fig. 4(c) Magnitude response showing tuneability of gain H.

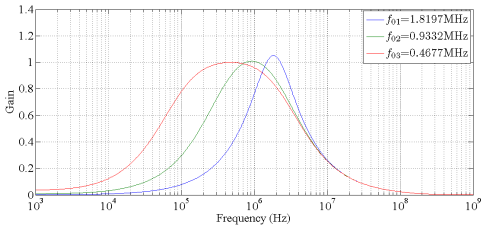

Fig.4 (d) Magnitude response showing tuneability of pole frequency f_0.

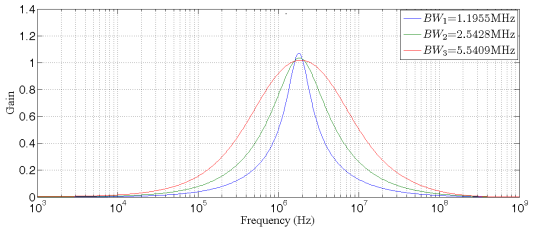

Fig. 4(e) Magnitude response showing tuneability of bandwidth Δf.

VI. CONCLUSIONS

A fully differential current mode universal filter circuit has been presented in which the filter parameters can be tuned independently. The filter employs only eight grounded resistances and two grounded capacitors (8R-2C). The number of passive elements used in this circuit is minimum when compared to other fully differential universal filter circuits with similar tuneability properties and compares well with a single ended electronically tuneable biquad filter of [11] with similar tuneablity properties. Lastly it may be mentioned that a configuration with only four grounded passive elements (2R-2C) and four CDCCs has been investigated earlier [12], but it does not possess the tuneability properties available in the proposed configuration.

VII. ACKNOWLEDGEMENT

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New grounded immittance simulators employing a single CFCC

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Abstract: In this study, a number of new immittance simulators employing a single current follower current conveyor (CFCC) and three passive components are proposed. First, six new circuit configurations have been introduced which can simulate lossy immittances of different types using a single CFCC along with a canonical number of passive and active components. Subsequently, with a little modification in the hardware of the CFCC, three other new circuits have been introduced which can simulate a variety of lossless immittances without any component matching constraints or requirement of additional active elements. When the passive resistors are replaced with complementary metal–oxide–semiconductor (CMOS) voltage controlled resistors, electronic tunability of the simulated immittances is available in all the cases. Several application examples of some of the proposed simulated immittance circuits have been presented and their workability has been verified using PSPICE simulations based on CFCC implementable in 0.18 μm CMOS technology.

1 Introduction

Due to their potential applications in a number of methods of the design of analogue filters and oscillators, active simulation of immittances has been a widely researched topic in the area of analogue integrated circuits (ICs) and signal processing. Apart from the classical IC operational amplifiers (opamp), operational transconductance amplifiers (OTA) and transistor-based simulators, which still evoke interest of researchers in this area [1–7], various other active building blocks (ABBs) such as current conveyors (CCs) and their different variants [8–32], current feedback operational amplifiers (CFOA) [33–42], four-terminal floating nullors (FTFN) [43–45], operational transresistance amplifiers (OTRA) [46–50], current amplifiers (CAs) [51] and so on have also been employed for the simulation of immittances of different types.

In recent years, many new synthetic ABBs, which combine the features of more than one ABB, have been introduced in the area of analogue signal processing and their applications and bipolar and/or complementary metal–oxide–semiconductor (CMOS) implementation have also been suggested [52–71]; see [59] for a classification, review and proposals of several new synthetic ABBs. Over the years, several of these ABBs have also been used for the realisation of synthetic immittances. Among the new ABBs, current differencing buffered amplifier (CDBA) [53, 54], current differencing transconductance amplifier (CDTA) [58], voltage differencing differential input buffered amplifier (VD-DIBA) [60, 61], voltage differencing transconductance amplifier (VDTA) [62, 63], current follower transconductance amplifier (CFTA) [64], voltage differencing CC (VDCC) [65, 66], voltage differencing buffered amplifier (VDBA) [67], current backward transconductance amplifier (CBTA) [68, 69] and current differencing CC (CDCC) [70] have received comparatively more attention in the realisation of different types of active immittances because of the reason that these simulated immittances, in general, do not suffer from the limitation(s) of the earlier generation of immittance simulators based on conventional opamps and provide the circuit designer with a variety of alternatives to choose from.

The immittance simulation circuits presented in [8–15] use one-to-three basic current conveyers of type I/II/III with single or dual outputs along with two to four resistors and one capacitor to realise grounded/floating inductors. The generic architecture of the CC has the possibility of adding more functionalities to the core CC and many researchers have modified the architecture of the basic CCs and used the new modified CCs like modified inverting second-generation current conveyor (MICCII–) [16], gain-variable third-generation CC (GVCCIII) [17], modified inverting first-generation CC (MICCI–) [18], fully differential second-generation CC (FDCCII) [19], dual X second-generation CC (DXCCII) [20–22], second-generation current controlled conveyor (CCCII) [23, 24], third-generation CC (CCIII) [25], differential difference CC (DDCC) [26, 27], differential voltage CC (DVCC) [28–30], differential CC (DCCII) [31, 32] to realise different types of inductors, namely, lossless inductors with matching constraints [16–18, 21, 22, 27, 31] and lossless/lossy inductors without any component matching conditions [19, 25, 28, 29, 32]. Most of these circuits, except those reported in [28, Fig. 2b and 32] use a single grounded capacitor as preferred for IC implementation. In [30], lossless floating inductor has been realised with two DVCC without any component matching. However, the value of the realised inductors in any of these realisations cannot be tuned. By contrast, in [20] lossless voltage-controlled tuneable grounded inductor has been realised with two DXCCIIs without any component matching condition while employing a single grounded capacitor. Likewise in [23], lossless current-controlled tuneable floating inductor has been realised with three/four CCCII/DO-CCCII elements without any component matching with all grounded passive elements. Furthermore, in [24], lossless current-controlled tuneable grounded inductor has been realised without any component matching and with two CCCIIs and a single grounded capacitor.

It is well known now that an ABB, which is closely related to the CC, is the so-called CFOA which is internally a cascade of a CCII+ and a unity gain voltage follower. Among the various immittance simulators using CFOAs, the circuits of [33] attain realisation of R-L and C-D immittances using a single CFOA, two resistors and two capacitors whereas in [34], a negative immittance circuit has been presented wherein the simulated immittance values can be orthogonally adjusted. In [35, 36], modified CFOA (MCFOA) has been used to realise floating and grounded immittance simulators using a minimum number (only three: two resistors and a capacitor) of passive components while employing a grounded capacitor and not needing any component matching constraints for realisation of the floating immittances. In [37], four lossy inductors using a canonic number of CFOAs and passive components,

without using component matching constraints, has been presented. With a new CFOA, two resistors and a capacitor, and four lossless inductors have also been presented. In [38], a method for reducing the effects of CFOA parasitics on the simulated inductor has been discussed. In [39], four new topologies for inductance simulation using a single CFOA have been presented. In [40], using a unified representation for single CFOA-based immittance function simulator, new lossy and lossless grounded inductors have been realised. None of these CFOA-based immittance simulators depends on any passive component matching constraints for the realisation of the intended type of immittances. In [41], two lossy and one lossless grounded inductance simulators have been presented which use an inverting type CFOA, two resistors and a single capacitor wherein the authors have also given a CMOS realisation of the inverting type CFOA along with its realisation with commercially available AD844 ICs. It may be pointed out that a comprehensive bibliography of various types of immittance simulation circuits using CFOAs has recently been made available in [42].

Besides different varieties of CCs and CFOAs, other ABBs such as FTFNs and OTRAs have also been used to realise different types of lossless/lossy immittances. For various immittance simulation circuits using one/two FTFNs and three-to-seven passive components, see [43–45]. On the other hand, in [46–48], a number of single-OTRA-based grounded lossless/lossy, positive/negative inductors have been presented which employ two-to-five resistors and one-to-two capacitors but suffer from the requirement of passive component matching for the realisation of the inductors, as in [46, 47]. In [49], grounded lossless inductor using an OTRA and voltage follower employing two capacitors and two resistors has been presented. There is a component matching constraint (equality of two capacitors) for the realisation of the inductor. In [50], two grounded lossy inductors as well as a lossless inductor have been presented using two OTRAs, four to five resistors and one capacitor. In the lossless inductor realisation, there is a component matching condition whereas in lossy inductor, there is no matching constraint.

A review of the immittance simulators using other miscellaneous active elements, including several of comparatively more recent origin, reveals the following. In [51], two CAs and a grounded capacitor have been used for the realisation of a lossless grounded as well as floating inductor. In [53], two floating inductance simulator circuits using three-to-four CDBAs, a single grounded capacitor and four MOS-controlled resistors have been presented. In [54], three single-CDBA-based grounded inductance (both lossless as well as lossy) circuits have been presented. A lossless grounded inductor without any component matching constraint using two CDTAs and a single grounded capacitor has been presented in [58], whereas, a floating inductor has been realised with three CDTAs and a grounded capacitor but needs the equality of two transconductances for the intended realisation. In [60], two/three VD-DIBAs and a grounded capacitor have been used to realise lossless grounded/floating inductance, whereas a single VD-DIBA, one grounded capacitor and one floating resistor has been used to realise an electronically-tuneable lossless grounded inductor. An electronically-tuneable floating inductance simulator using two VD-DIBAs, a single grounded capacitor and a floating resistor has also been presented in [61]. In [62], a single/two VDTA-based electronically-tunable grounded/floating inductance simulators employing a single grounded capacitor have been presented. On the other hand in [63], a Z-copy VDTA has been used to realise a floating lossless inductance employing a single grounded capacitor. In [64], two/three CFTAs have been used to realise a grounded/floating gyrator circuit. A new building block called VDCC [65, 66] has been used to realise a number of grounded lossy/lossless grounded/floating inductances using a single VDCC, one resistor and one capacitor. In [67], a single VDBA has been used to realise a lossless grounded inductor employing one resistor and one capacitor. CBTA has been used in [68, 69] to simulate a floating

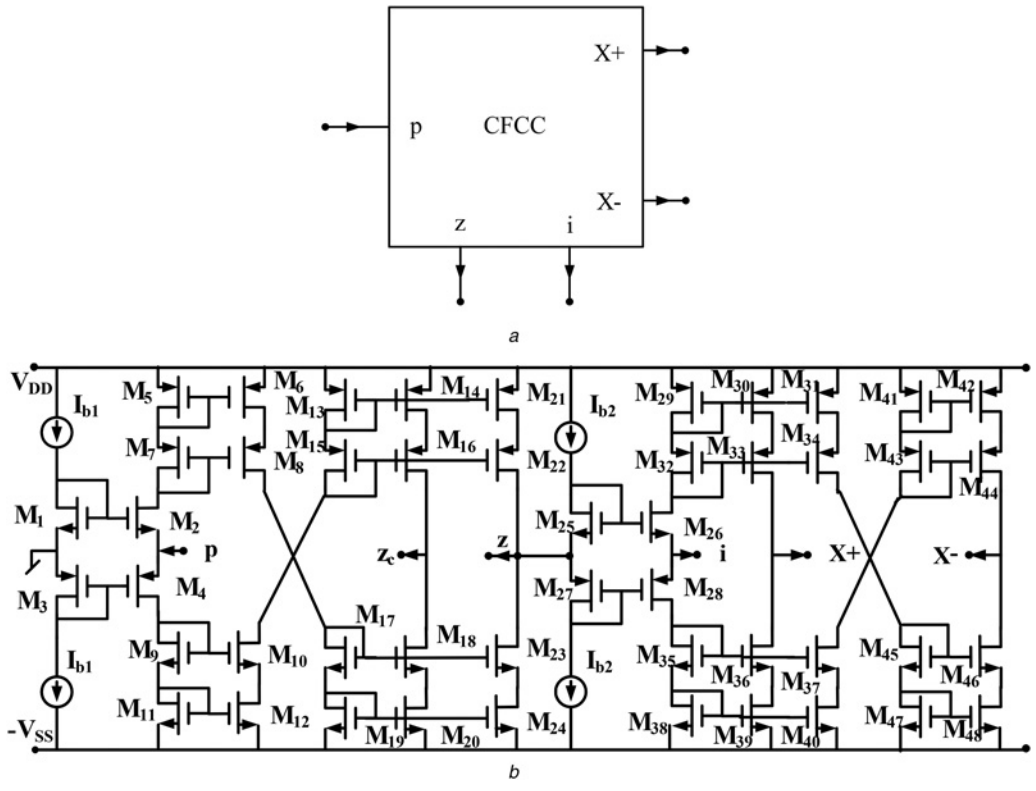

Fig. 1 *CFCC*
a Symbolic notation
b Exemplary CMOS implementation of ZC-CFCC

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inductance using two CBTA and three grounded passive elements in [68] and one CBTA and two grounded passive components in [69]. In [71], a single CDCC with one grounded capacitor and two resistors has been used to simulate four circuits of lossy inductors.

In retrospection, it has been found that the various published circuits for simulation of grounded and floating inductors can be broadly categorised into three major classes: class I – circuits employing commercially available IC building blocks namely, IC operational amplifiers, IC OTA, conventional CCs and IC current feedback amplifiers [3, 5, 8–13, 33, 34, 37–40], class II – circuits using newer building blocks which are although not available as off-the-shelf ICs but their bipolar and/or CMOS implementations have been known/proposed and utilised in the simulations

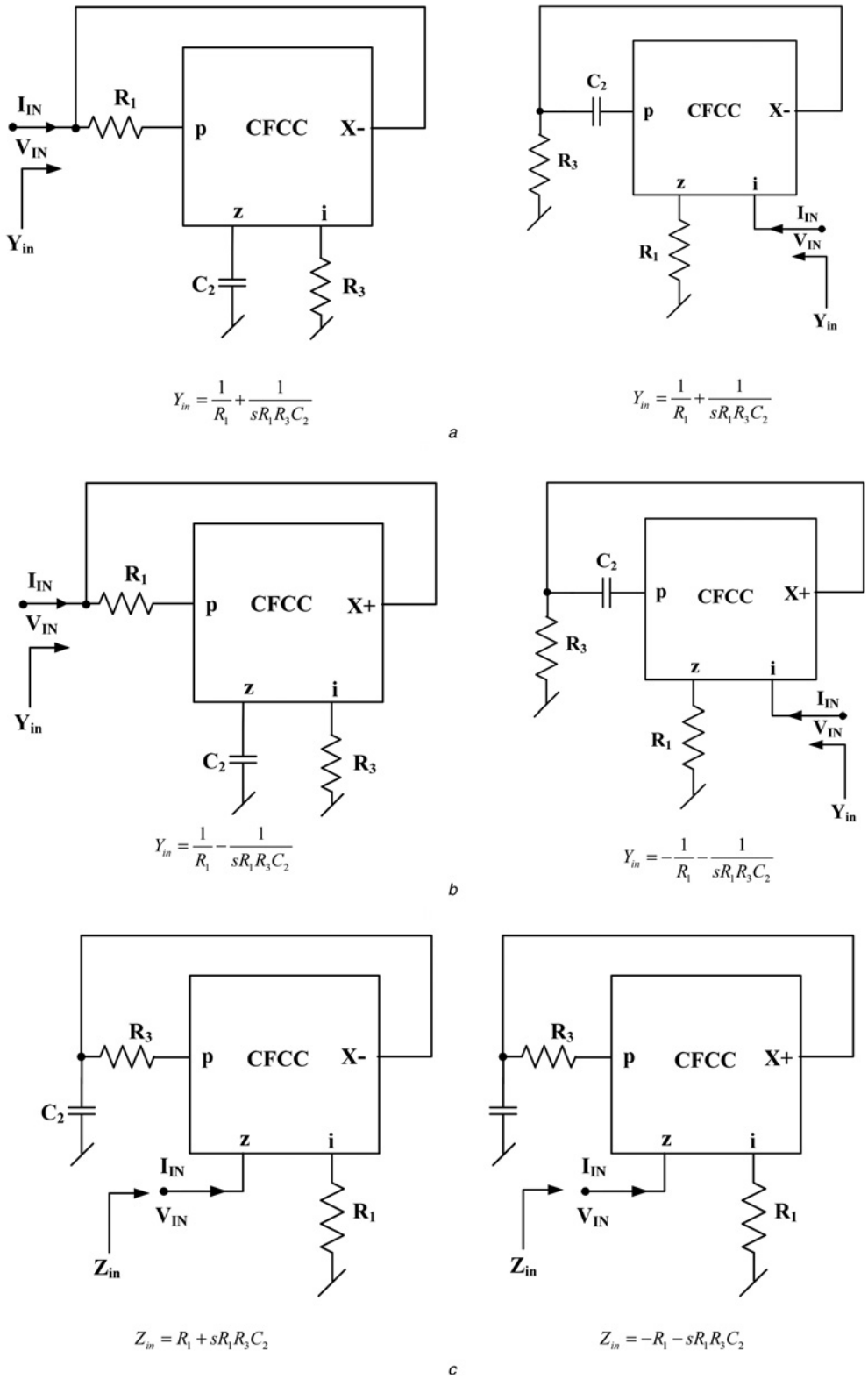

Fig. 2 *Various non-ideal inductance simulators realised using a single CFCC a–c*

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[4, 6, 7, 14–30, 31, 32, 35, 36, 45, 46, 48, 51, 53, 58, 61–71] and class III in which those composite building blocks have been employed which have been shown to be realisable employing commercially available ICs [17, 31, 32, 36, 37, 41, 43, 44, 46, 47, 49, 50, 54, 60, 67].

In this paper, we present a family of active immittances realised with a single current follower CC (CFCC) or Z-copy CFCC (ZC-CFCC). Although the MOCFCC was also introduced in [59], to the best of the authors' knowledge, its use has not yet been fully exploited for the realisation of synthetic immittances. The main intention of this communication is, therefore, to present a variety of single CFCC-based lossy/lossless inductance simulators falling within the class II mentioned above.

2 Current follower current conveyor

CFCC [59] is a five-port ABB whose symbolic notation is shown in Fig. 1*a*. The current at the *z* terminal is an inverted copy of the input current at '*p*' terminal. The terminal '*i*' tracks the potential at the terminal *z*. Two complementary currents at the output terminals are available which are copies of the current at the '*i*' terminal. To provide addition functionality to the CFCC, a copy of the current at the '*z*' terminal has also been provided resulting in the Z-copy CFCC. The CMOS implementation of ZC-CFCC is shown in Fig. 1*b* Mathematically, a ZC-CFCC can be characterised by the following matrix equation:

$$\begin{bmatrix} V_p \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \\ I_{zc} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ V_z \\ I_i \\ V_{x+} \\ V_{x-} \\ V_{zc} \end{bmatrix} \quad (1)$$

3 Proposed CFCC-based immittance simulators

Figs. 2 and 3 show the proposed simulated immittance networks.

It is seen that the circuits of Fig. 2*a* realise a positive parallel RL, while those of Fig. 2*b* realise parallel of a positive/negative resistor and negative inductor and the circuits given in Fig. 2*c* realise a positive series RL and a negative series RL without any conditions providing single resistance control of relevant equivalent parameter value. On the other hand, the circuit of Fig. 3*a* realises a lossless grounded inductance, circuit of Fig. 3*b* realises a negative inductance and circuit of Fig. 3*c* realises an ideal frequency dependent negative resistance (FDNR) with no component-matching constraints required and with the value of the realised impedance being single-resistance tunable in all the cases. If the resistors R_1, R_2 and R_3 shown in Figs. 2 and 3 are replaced with linear voltage controlled resistors (VCR) realised with CMOS circuit of

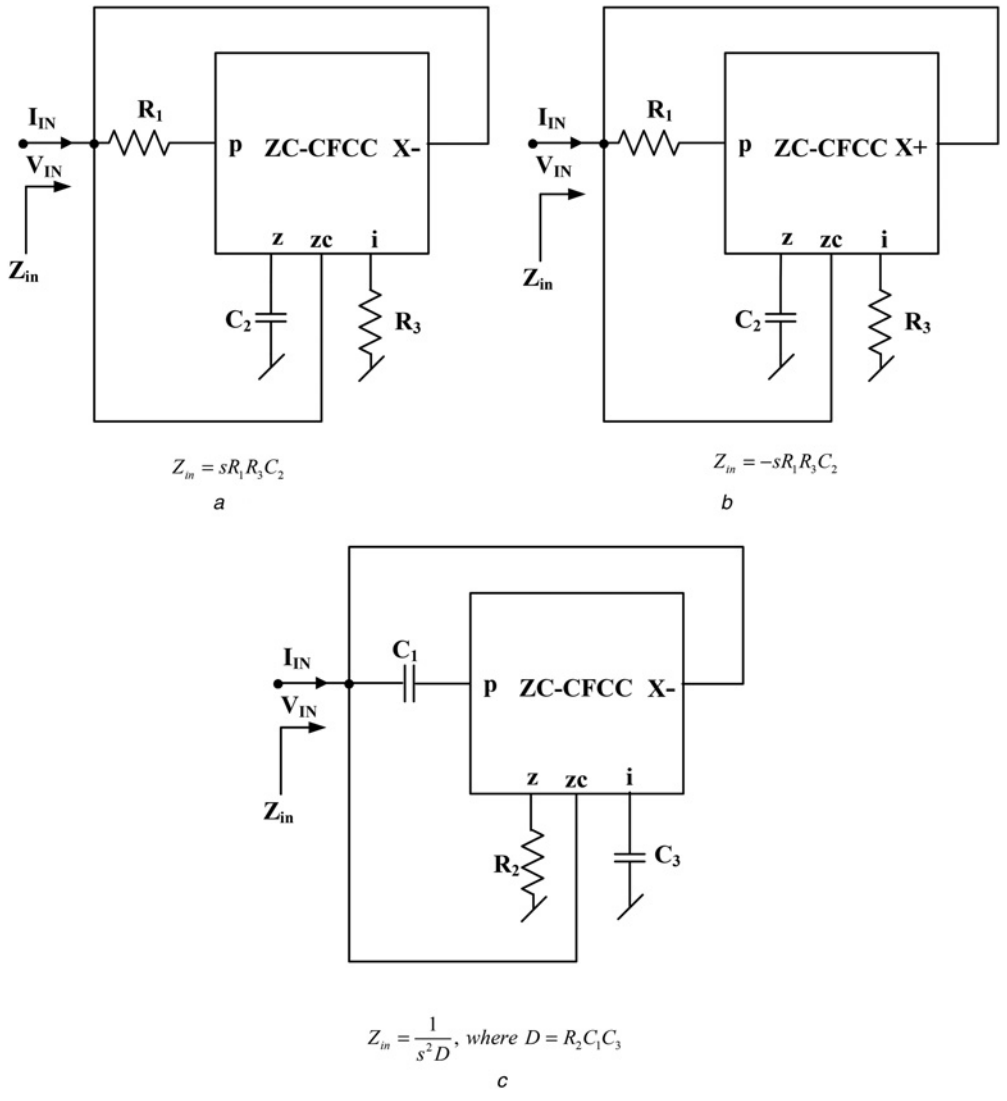

Fig. 3 *Various ideal immittance simulators realised using a single ZC-CFCC*

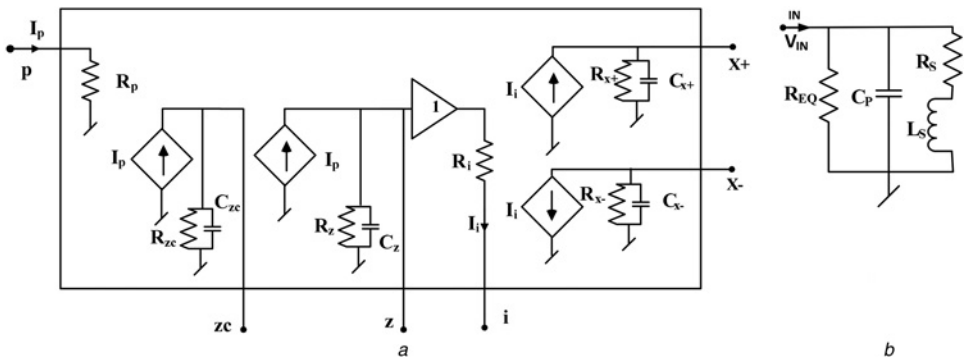

Fig. 4 *Non-ideal considerations*
a Equivalent circuit of the ZC-CFCC with additional *zc* terminal
b Equivalent circuit for lossy and lossless inductor as shown in Figs. 2*a* and 3*a*

[72, Fig. 6e therein], then all the circuits would attain electronic tunability of the various realised parameters through control voltages V_{pi} and/or V_{ni} for $i = 1$–3. On the other hand, the resistors connected at the $p(n)$ terminal and the i terminal can altogether be exploited by the appropriate choice of the bias current to realise current controlled lossless grounded inductors also [73].

4 Non-ideal analysis

A non-ideal behavioural model of the ZC-CFCC [59] is shown in Fig. 4*a*. In this model, R_p represents the parasitic input resistances of the p port whereas R_z and C_z represent the resistance and capacitance at z terminal of the ZC-CFCC. Similarly, R_{zc} and C_{zc} represent resistance and capacitance at zc terminal while R_i represents the output resistance of the voltage buffer of the MO-CCII (resistance at I terminal). On the other hand, R_{x+} and C_{x+} represent output resistance and output capacitance at the $x+$ terminals of the ZC-CFCC and finally, R_{x-} and C_{x-} represent the output resistance and the output capacitance at the x terminals of the ZC-CFCC. The relations between the various port variables for the non-ideal ZC-CFCC, with additional zc terminal, are given by
(see (2))

The determination of the non-ideal expressions for Z_{in} or Y_{in} for the various circuits by considering the parasitic impedances of the CFCC is straightforward and therefore, instead of presenting such expressions for all the proposed circuits, these have been given in the following only for some representative cases.

4.1 Non-ideal analysis of the lossy inductor of Fig. 2a

A straightforward analysis of this circuit shows that the admittance using non-ideal model of the CFCC, is given by

$$Y_{in1} = \frac{1}{R_1 + R_p} + \frac{1}{R_{x-}} + sC_{x-} + X \tag{3}$$

where

$$X = \frac{1}{\left(\left((R_1 + R_p)(R_3 + R_i)\right)/R_z\right) + s(R_1 + R_p)(R_3 + R_i)(C_2 + C_z)}$$

A passive equivalent of this admittance can, thus, be constructed as shown in Fig. 4*b* where

$$R_{EQ} = (R_1 + R_p)||R_{x-}, \quad C_p = C_{x-},$$
$$R_s = \frac{(R_1 + R_p)(R_3 + R_i)}{R_z} \text{ and} \tag{4}$$
$$L_s = (R_1 + R_p)(R_3 + R_i)(C_2 + C_z)$$

4.2 Non-ideal analysis of the lossless inductor of Fig. 3a

The non-ideal expression of the lossless grounded inductor of Fig. 3*a*, using the non-ideal model of CFCC with additional zc terminal, is found to be

$$Y_{in2} = \frac{1}{R_{zc}||R_{x-}} + s(C_{zc} + C_{x-}) + X \tag{5}$$

Table 1 Aspect ratios of MOSFETs used in ZC-CFCC given in Fig. 1*b*

MOSFETs	W/L, μm/μm
M_1, M_2, M_{25}, M_{26}	25/0.25
M_3, M_4, M_{27}, M_{28}	50/0.25
$M_5 - M_{24}$, $M_{29} - M_{48}$	2.5/0.25

$$\begin{bmatrix} V_p \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \\ I_{zc} \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 & 0 & 0 \\ 1 & -\left(\frac{1}{R_z} + sC_z\right) & 0 & 0 & 0 & 0 \\ 0 & 1 & -R_i & 0 & 0 & 0 \\ 0 & 0 & 1 & -\left(\frac{1}{R_{x+}} + sC_{x+}\right) & 0 & 0 \\ 0 & 0 & -1 & 0 & -\left(\frac{1}{R_{x-}} + sC_{x-}\right) & 0 \\ 1 & 0 & 0 & 0 & 0 & -\left(\frac{1}{R_{zc}} + sC_{zc}\right) \end{bmatrix} \begin{bmatrix} I_p \\ V_z \\ I_i \\ V_{x+} \\ V_{x-} \\ V_{zc} \end{bmatrix} \tag{2}$$

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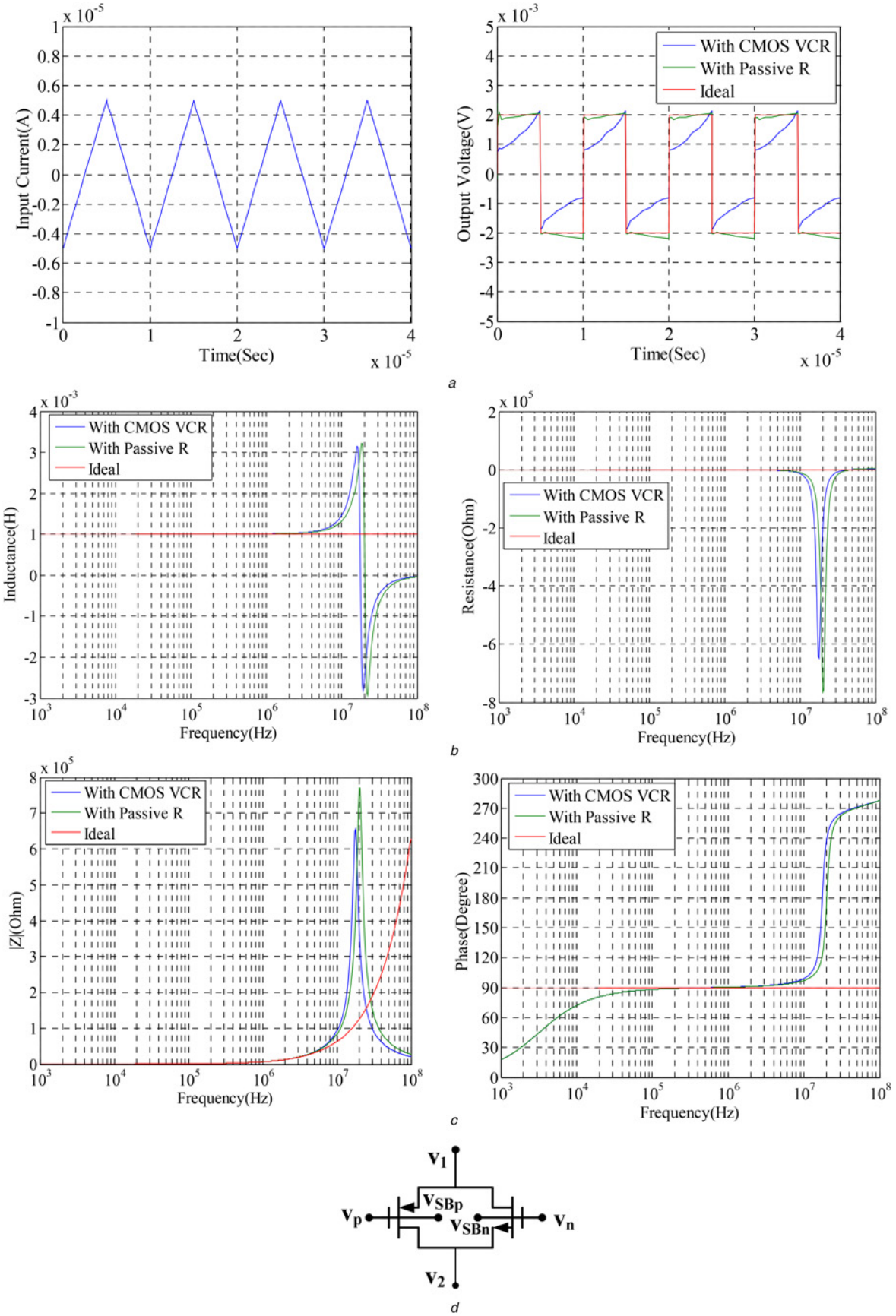

Fig. 5 *Time response and frequency response of the simulated lossless inductor*
a Time response of the simulated inductor
b Variation of inductive and resistive part with frequency (ideal value of associated resistance being 0 Ω)
c Magnitude and phase response of the proposed grounded inductor
d CMOS VCR given in [72, Fig. 6e therein]

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This gives the values of the different passive components in the general equivalent circuit shown in Fig. 4*b*, as

$$R_{\mathrm{EQ}} = R_{zc}||R_{x-}, \quad C_p = C_{zc} + C_{x-},$$
$$R_s = \frac{(R_1 + R_p)(R_3 + R_i)}{R_z} \text{ and} \tag{6}$$
$$L_s = (R_1 + R_p)(R_3 + R_i)(C_2 + C_Z)$$

4.3 *Non-ideal analysis of the FDNR of Fig. 3*c

The non-ideal input impedance of the FDNR circuit of Fig. 3*c*, with the ZC-CFCC replaced with its non-ideal model given in expression (2), is found to be (see equation (7))

where $R = R_2||R_z$, $C = C_z$, $R_k = R_{zc}||R_{x-}$ and $C_k = C_{zc} + C_{x-}$.

Unfortunately, the non-ideal expression (7) does not appear to lead to a simple equivalent circuit like that of Fig. 4*b*.

5 SPICE simulation results

The CMOS implementation of the ZC-CFCC shown in Fig. 1*b* has been used to verify the workability of the circuits presented in this paper. The aspect ratios of the metal–oxide–semiconductor field-effect transistor (MOSFETs) employed are given in Table 1. The values of the DC bias currents and voltages were taken as 40 μA and ±2.5 V, respectively.

To verify the workability of the proposed structures we now present some sample application circuits and the results of their verification using SPICE simulations.

Time response and frequency response of the simulated grounded inductor: The lossless grounded inductor of Fig. 3*a* was designed to have a value of 1 mH (by choosing $R_1 = R_3 = 10$ kΩ, $C_2 = 0.01$ nF). The control voltages for the voltage controlled CMOS resistors used in the simulation (shown in Fig. 5*d*) were taken as $V_n = -V_p = 997$ mV. An input current with a triangular waveform (5 μA amplitude) was applied to the proposed inductor (1 mH) shown in Fig. 3*a*. The output voltage, a square wave, is obtained as shown in Fig. 5*a*.

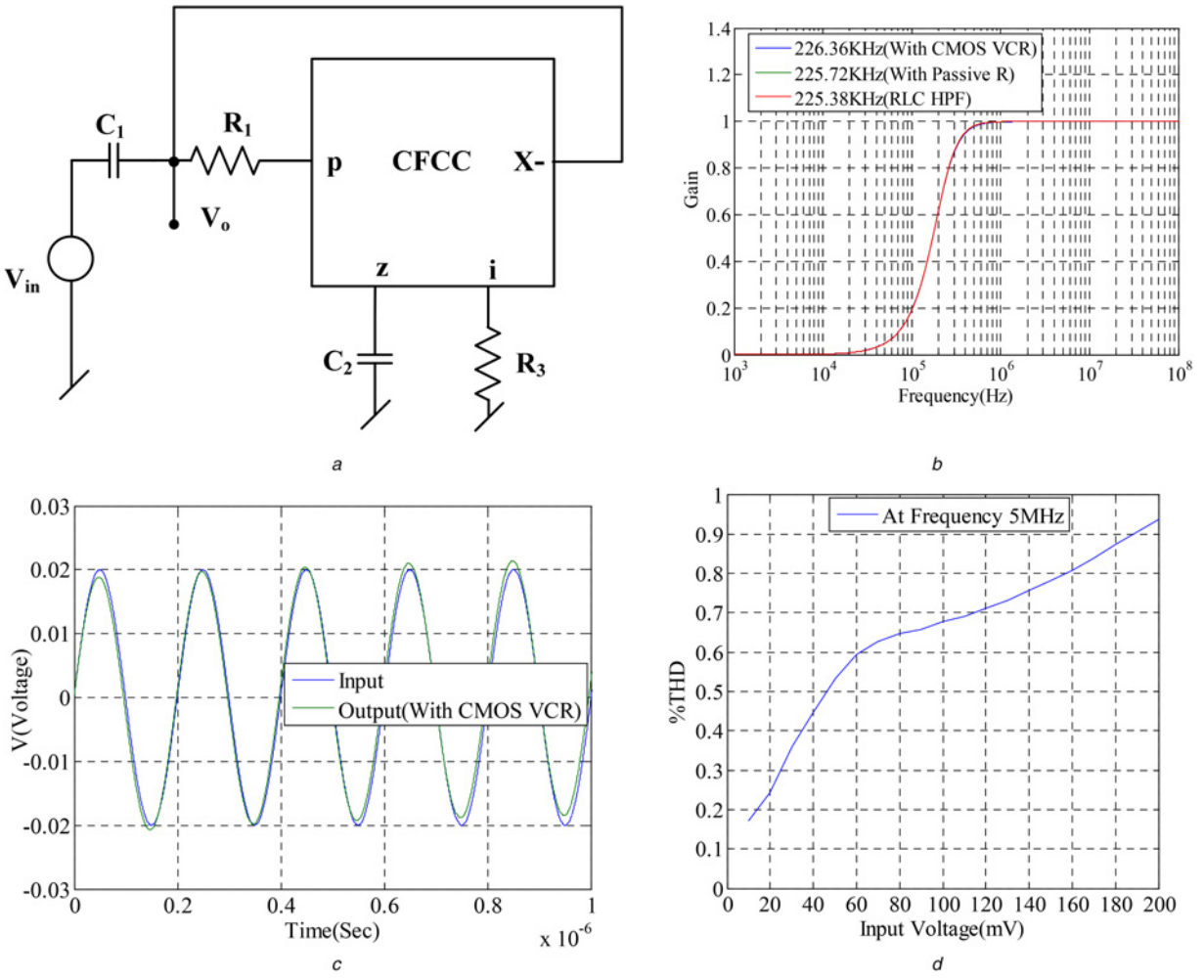

Fig. 6 *Second-order RLC high-pass filter using simulated inductor*
a Active realisation
b Magnitude response for the circuit
c Transient response
d Variation of THD with applied input voltage at 5 MHz

$$Z_{\mathrm{in}} = \frac{1}{\left((s^2 C_1 C_3 R)/\left((1 + sR_i C_3)(1 + sR_p C_1)(1 + sRC)\right)\right) + \left((1 + sR_k C_k)/R_k\right)} \tag{7}$$

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The frequency response of the simulated lossless inductor was determined through PSPICE simulations and is shown in Fig. 5*b*. It is observed that the lossless inductor can be used satisfactorily up to a frequency of 5.4 MHz (with the error in the simulated value of inductance being no more than 10% in this range). Fig. 5*c* shows the impedance magnitude and phase for inductor (value 1 mH). The simulated results agree quite well with the theoretical ones. The discrepancy between theoretical and simulated results is mainly attributed to the non-ideal gain and parasitic impedance effects of the ZC-CFCC.

Second-order RLC high-pass filter using simulated inductor: The simulated lossy inductor ($R = 10\ \text{k}\Omega \| L = 10\ \text{mH}$) realised from Fig. 2*a* has been used to design a second-order high-pass filter with cut-off frequency of 225 kHz for which the corresponding active realisation is given in Fig. 6*a*. The high-pass transfer function is given as

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + s(1/R_1C_1) + (1/LC_1)} \tag{8}$$

The pole frequency is given by

$$f_o = \frac{1}{2\pi\sqrt{LC_1}} \tag{9}$$

The following values of components were chosen to simulate the lossy inductor: $R_1 = 10\ \text{k}\Omega$, $R_3 = 10\ \text{k}\Omega$, $C_2 = 0.1$ nF with $C_1 = 0.0.5$ nF. We have superimposed the frequency responses of the active high-pass filter realised with (i) R_1 and R_2 as passive resistors and (ii) R_1 and R_2 realised with voltage controlled CMOS resistors (control voltages $V_n = -V_p = 981$ mV) which are shown in Fig. 6*b*. The simulated values of the pole frequency were found to be 225.72 and 226.36 kHz, respectively, which are seen to be in good agreement. Figs. 6*c–d* show the transient response of the filter for an input amplitude of 20 mV at a frequency of 5 MHz and the % THD in the output when the input amplitude was varied in the range of 10–200 mV.

Second-order RLC bandpass filter using simulated inductor: Lossless inductor ($L = 1$ mH) realised from the circuit of Fig. 3*a* has been used to design a second-order bandpass filter with the pole frequency of 503.29 kHz and BW = 1.5915 MHz for which the corresponding active realisation are given in Fig. 7*a*. The bandpass transfer function is given as

$$\frac{V_o}{V_{in}} = \frac{s(1/RC)}{s^2 + s(1/RC) + (1/LC)} \tag{10}$$

The pole frequency and the bandwidth are given by:

Pole frequency $f_o = (1/2\pi\sqrt{LC})$; bandwidth BW $= (1/2\pi RC)$ The lossless inductor was designed with the following values of the passive components $R_1 = R_3 = 10\ \text{k}\Omega$, $C_2 = 0.01$ nF. The control voltages for the voltage controlled CMOS resistors were taken as $V_n = -V_p = 997$ mV. With $R = 1\ \text{k}\Omega$, $C = 0.1$ nF, the simulated value of the pole frequency was found to be 512.86 kHz whereas the bandwidth was found to be 1.5870 MHz. The frequency response obtained from SPICE simulations is shown in Fig. 7*b*. Fig. 7*c* shows the transient response of the filter for an input amplitude of 10 mV at a frequency of 512.86 kHz.

The value of the voltage controlled CMOS resistors can be varied by changing the control voltages thereby making the simulated

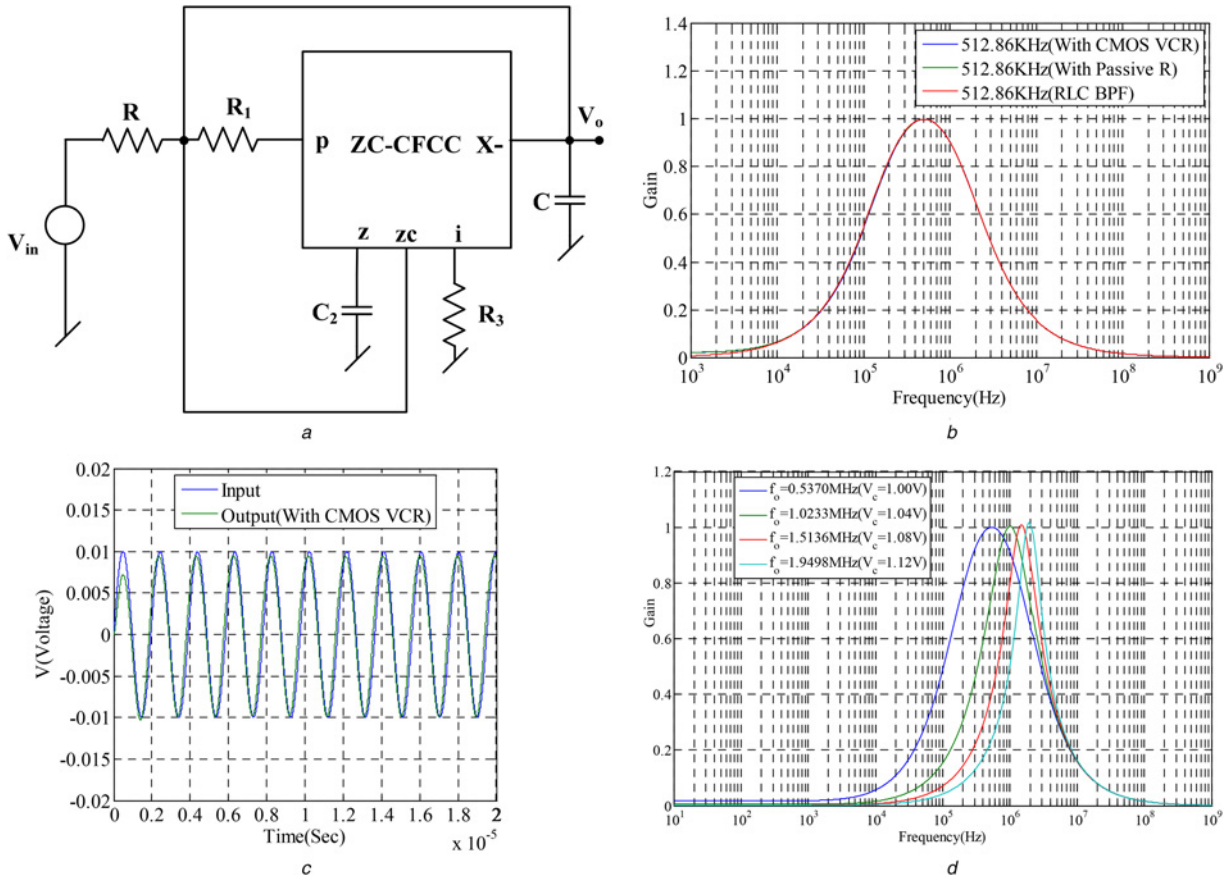

Fig. 7 *Second-order RLC bandpass filter realisation*
a Active realisation
b Magnitude response for the circuit
c Transient response
d Tunability of the pole frequency with control voltage

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immittances electronically tunable. The second-order bandpass filter shown in Fig. 7*a* was used to check the tunability of the centre frequency of the bandpass filter by changing the control voltages V_p and V_n ($V_c = V_n = -V_p$). Fig. 7*d* shows the variation of centre frequency of the tunable bandpass filter, obtained by changing V_p and V_n, which confirm the electronic variability of the lossless inductor of Fig. 3*a*.

Fourth-order Butterworth high-pass filter: Another example of the application of the electronically-tunable, lossless grounded inductor is in the realisation of a fourth-order Butterworth high-pass filter. A prototype fourth-order high-pass filter is shown in Fig. 8*a*. The normalised component values for cut-off frequency of 1 Hz are: $R_s = R_L = 1\ \Omega$, $L_1 = L_2 = 0.1217$ H, $C_1 = 0.2768$ F and $C_3 = 0.0780$ F [20]. After performing appropriate frequency and impedance scaling on the prototype for cut-off frequency of 159 kHz, the final values of components are $R_s = R_L = 1\ \text{k}\Omega$, $L_1 = L_2 = 76.54\ \mu\text{H}$, $C_1 = 1.74.1$ pF and $C_3 = 49.1$ pF. The inductor of 76.54 µH was simulated with control voltage $V_c = V_n = -V_p = 1.1056$ V. Value of the simulated cut-off frequency was found to be $f_o = 1.5952$ MHz. The frequency response of the filter is shown in Fig. 8.

Second-order RCD low-pass filter using simulated FDNR: The simulated ideal grounded FDNR of Fig. 3*c* was used to design a second-order low-pass filter, by applying Bruton's transform to the passive second-order filter shown in Fig. 9*a*. The transformed FDNR filter realisation is shown in Fig. 9*b* for which the transfer function is given by

$$\frac{V_o}{V_{in}} = \frac{(1/RD)}{s^2 + s((RC^2 + D)/RCD) + (2/RD)} \tag{11}$$

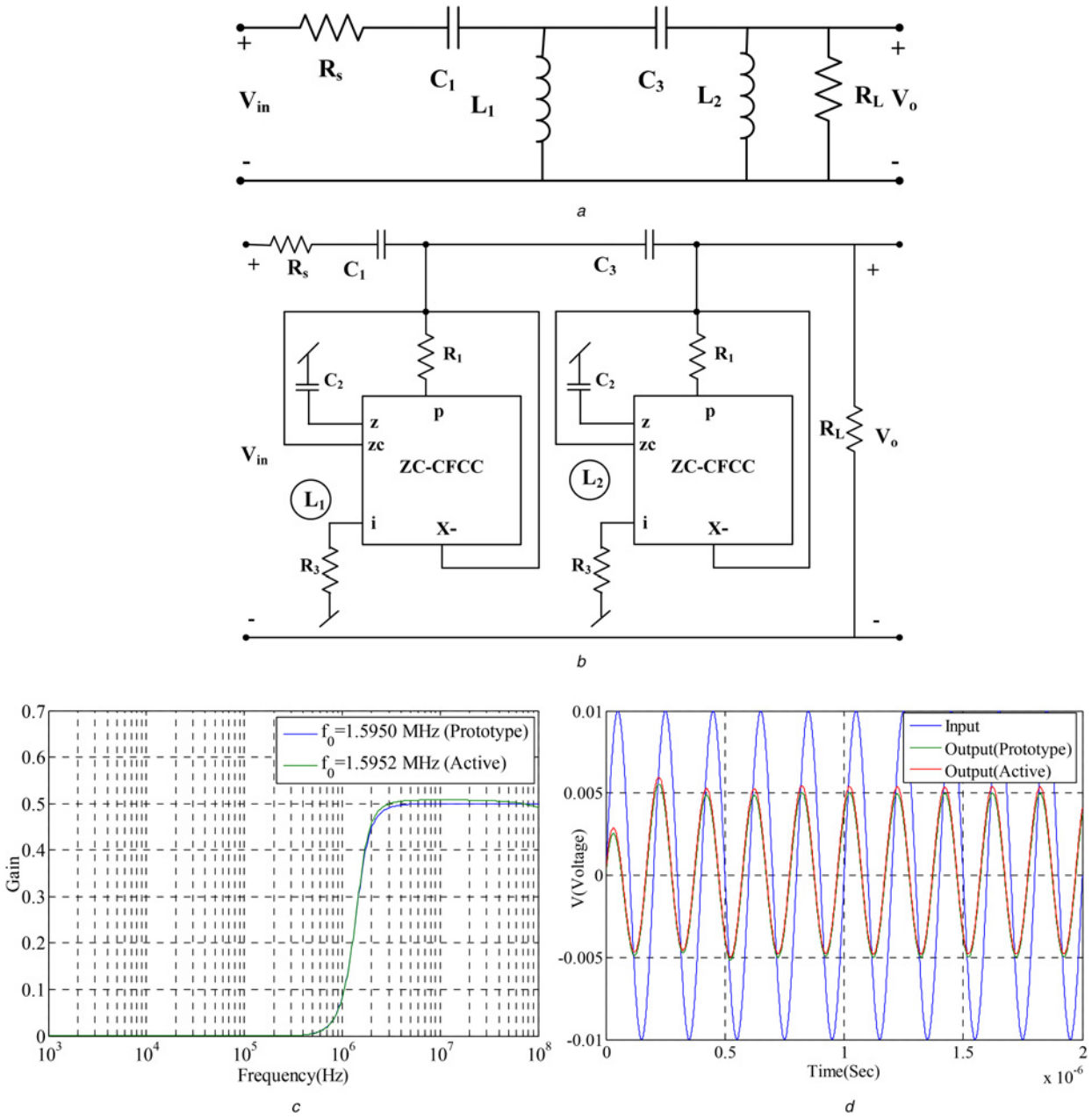

Fig. 8 *Fourth-order high-pass Butterworth filter realisation*
a Prototype
b Active realisation
c Magnitude response for the circuit
d Transient response

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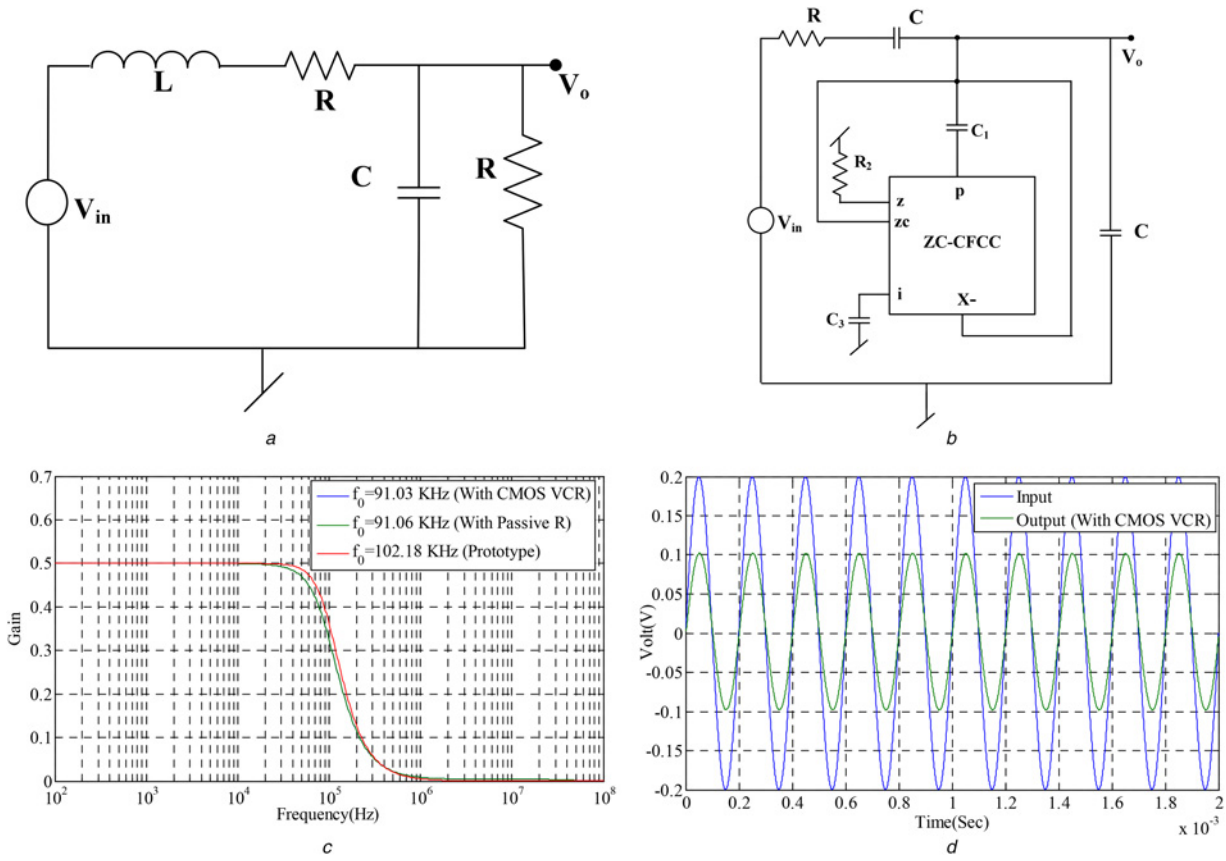

Fig. 9 *Second-order RCD low-pass filter realisation*
a Prototype
b Active realisation
c Magnitude response for the circuit
d Transient response

The circuit realises a second-order RCD low-pass filter for which the filter parameters are given by:

Pole frequency $f_o = (1/\pi\sqrt{2RD})$; quality factor $Q = (C/(RC^2 + D))\sqrt{2RD}$.

The FDNR was designed with the following passive component $C_1 = 0.22$ nF, $R_2 = 10$ kΩ, $C_3 = 0.22$ nF $(D = R_2C_1C_3)$, with $R = 10$ kΩ, $C = 0.22$ nF, to have a pole frequency of 102.31 kHz. The simulate value of the pole frequency was found to be 91.06 kHz. When R_2 was replaced by a voltage controlled CMOS resistor (control voltages $V_n = -V_p = 880.5$ mV), the simulated value of pole frequency was found to be 91.03 kHz (Fig. 8*b*). The difference between the designed pole frequency and the simulated value may be attributed to the uncompensated parasitic impedance at the *z* terminal of the ZC-CFCC. However, this should not be a cause of concern as the same can be adjusted by varying the control voltage. For correcting the frequency response at DC a large resistor $R_c = 2.32$ MΩ shunting the series C (Bruton transformed series R) was required as is normally needed in RCD filters [74]. Figs. 8*c–d* show the frequency response and transient response of the filter for an input amplitude of 200 mV at a frequency of 5 kHz. The % THD in the output when the input amplitude was varied in the range of 5–200 mV was found to be less than 1%. For simulating the FDNR the rail voltage was kept at ±1.9 V.

The SPICE simulations shown in this section demonstrate the viability of new proposed immittance simulators using CFCC.

6 Comparison with recently published grounded inductance simulators

We now present a comparison of the proposed inductance simulators with the existing single ABBs-based grounded inductance simulators in Table 2.

When compared with recently published immittance simulators realised with single ABBs it is revealed that, with the exception of the earlier circuits presented in [61, 62, 65, 67, 69] which provide electronic tunability through the variation of the transconductance parameter, the proposed circuits are the only ones which provide the following advantageous features simultaneously: (i) use of a single ABB, (ii) employment of a cannonic number of RC elements, (iii) use of grounded capacitor in several cases, (iv) complete absence of any passive element matching conditions, (v) electronic tunability through an external voltage signal, (vi) reasonably low-voltage operation coupled with very low-power consumption and (vii) suitability for CMOS implementation. It may also be mentioned here that the input dynamic range of the circuits using inductance in case of simulators presented in [61, 62, 65, 67, 69] is constrained by the linear range of operation of the active device being used. By contrast, there is no such constraint for the proposed simulators as the tunability of immittances is affected by changing the value of the CMOS VCR which is quite linear.

7 Concluding remarks

In this paper, a number of new electronically-controllable grounded immittance simulation circuits were proposed all of which employ only a single CFCC along with a canonical number of passive elements without requiring any passive component-matching conditions. When compared with the previously known circuits, the proposed synthetic immittance circuits possess several advantageous features as elaborated in Section 6. The workability of the proposed new configurations has been verified by SPICE simulations of a number of application circuits implemented with CFCC architectures suitable for CMOS implementation in 0.18 µm

Table 2 Comparison with other recently published grounded inductors realised with single ABB

Ref.	Inductance type[a] G	Single active element class	Number of resistors used	Number of capacitors used	Whether free from passive component matching	Availability of electronic tunability	Technology	Power supply voltage	Power dissipation
[14]	lossless	CCI [II]	4	1F	no	no	0.35 μm	±1.65 V	NA
[15]	lossy	CCIII [II]	2	1G/F	yes	no	0.6 μm	±2.5 V	1.5 mW
[16]	lossless	MICCII−[II]	2	1F	no	no	0.35 μm	±2.5 V	17.6 mW
[17]	lossy	GVCCIII [II/III]	2	1F	yes	no	0.25 μm AD844	±1.5 V ±15 V	NA
	losslss	GVCCIII [II/III]	2	1F	no	no	0.25 μm AD844	±1.5 V ±15 V	NA
[18]	lossless	MICCI−[II]	2	1F	no	no	0.35 μm	±1.5 V	NA
[19]	lossless	FDCCII [II]	2	1G	yes	no	0.35 μm	±1.5 V	NA
[21]	lossless	DXCCII [II]	2	1F	no	no	0.35 μm	±1.5 V	NA
[22]	lossless	DXCCII [II]	2/3	1F	no	no	0.35 μm	±1.65 V	NA
[25]	lossy	CCIII + [II]	2/3	1F	yes	no	PNP/NPN Array B101/102	±10 V	NA
[27]	lossless	MDO-DDCC [II]	2	1G	no	no	0.35 μm	±1.5 V	NA
[28]	lossy	DVCC [II]	2	1G/1F	yes	no	0.5 μm	±2.5 V	NA
[31]	lossless	DCCII [II/III]	2	1G	no	no	Bipolar Array ALA400 AD844	±2.5 V ±15 V	NA
[32]	lossless	DCCII [II/III]	2	1F	yes	no	0.25 μm AD844	±1.25 V ±15 V	NA
[33]	lossy	CFOA [I]	2	2G	no	no	Discrete AD844	NA	NA
[34]	lossy (−)	CFOA [I]	2	2(1G + 1F)	yes	no	Discrete AD844	NA	NA
[36]	lossless	MCFOA [II/III]	2	1G	yes	no	0.25 μm AD844	±1.5 V	NA
[37]	lossy	CFOA [I]	2	1F	yes	no	Discrete AD844	±15 V	NA
	losslss	New CFOA [III]	2	1F	yes	no	Discrete AD844		
[39]	lossless (−)	CFOA [I]	2	1F	yes	no	Discrete AD844	±10 V	NA
	lossy (+/−)	CFOA [I]	2	1F	yes	no	Discrete AD844	±10 V	NA
[40]	lossy (+/−)	CFOA [I]	2/3	1F	yes	no	Discrete AD844	±15 V	NA
	lossless (−)	CFOA [I]	2	1F	yes	no	Discrete AD844	±15 V	NA
[41]	lossy	CFOA-[III]	2	1G	yes	no	0.13 μm AD844	±0.75 V	0.89 mW
	losslss	CFOA-[III]	2	1F	yes	no	0.13 μm AD844	±0.75 V	0.89 mW
[43]	lossy (+/−)	FTFN [III]	2	1F	yes	no	Discrete AD844	NA	NA
[45]	lossless	PFTFN [II]	4	1F	no	no	0.35 μm	±5 V	NA
[46]	lossless	OTRA [II/III]	3	2F	no	no	0.5 μm AD844	±01.5 V ±5 V	0.809 mW 260 mW
[47]	lossless (−)	OTRA [III]	5	1F	no	no	Discrete AD844	NA	NA
[48]	lossy	OTRA [II]	2/3	1F	yes	no	1.2 μm	±5 V	NA
[54]	lossy	CDBA [III]	2	1F	yes	no	Discrete AD844	±12 V	NA
	losslss	CDBA [III]	4	1F	no	no	Discrete AD844	±12 V	NA
[61]	lossless	VD-DIBA [II]	1	1G	yes	yes by changing g_m	0.35 μm	±2 V	NA
[62]	lossless	VDTA [II]	0	1G	yes	yes by changing g_m	0.18 μm	±0.9 V	NA
[65]	lossless/ lossy	VDCC [II]	1	1G	yes	yes by changing g_m	0.18 μm	±0.9 V	0.869 mW
[67]	losslss	VDBA [II/III]	1	1F	yes	yes by changing g_m	Discrete OPA860	±5 V	NA
[69]	lossless	CBTA [II]	1	1G	yes	yes by changing g_m	0.25 μm	±2.5 V	NA
[71]	lossy	CDCC [II]	1	1G	yes	no	0.35 μm	±1.5 V	NA
Proposed	lossy	CFCC [II]	2	1G/1F	yes	no	0.18 μm	±2.5 V	1.78 mW
	lossy	CFCC [II]	2[VCR]	1G/1F	yes	yes			
Proposed	lossless	ZC-CFCC [II]	2[VCR]	1G	yes	yes	0.18 μm	±2.5 V	1.95 mW

[a]F: floating, G: grounded, NA: (concerned data/information) not available.

CMOS technology. The proposed single-CFCC-based simulators, thus, add new useful alternatives to the existing repertoire of single-active-building-block-based grounded immittance simulators as given in Table 2.

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9 Appendix

Measured values of the non-ideal parameters of the ZC-CFCC shown in Fig. 4*a* at DC bias voltage ±2.5 V and DC bias currents 40 μA have been found to be as given in Table 3.

Table 3 Characteristic parameters of ZC-CFCC

Sl. No.	Parameter	Value
1	R_p	591 Ω
2	R_z	4.9178 MΩ
3	C_z	6.3234×10^{-14} F,
4	R_{zc}	4.9178 MΩ
5	C_{zc}	7.2123×10^{-15} F,
6	R_x	4.79990 MΩ
7	C_x	7.3772×10^{-15} F
8	R_i	591 Ω
9	3 dB bandwidth	201.4719 MHz
10	power consumption	2.47 mW

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Electronically tunable grounded/floating inductance simulators using Z-copy CFCCC

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Abstract: In this paper, new electronically tunable grounded and floating inductance simulators employing a Z-copy current follower current controlled conveyor (CFCCC) and one grounded capacitor have been proposed and their workability has been demonstrated by PSPICE simulations in 0.18-μm TSMC CMOS technology.

Key words: Analog circuits, current-mode circuits, current conveyors, current followers, inductance simulators, analog filters

1. Introduction

Over the past several years, many new analog building blocks (ABBs) have been used to implement various signal processing/generation functions including the simulation of inductors, realization of universal biquadratic filters, sinusoidal oscillators, and nonsinusoidal waveform generators [1–10]. The various building blocks that have been prominently employed in the past for simulating the inductors include the operational transresistance amplifier (OTRA) [11,12], differential voltage current conveyor (DVCC) [13], current differencing buffered amplifier (CDBA) [14], current differencing transconductance amplifier (CDTA) [15], voltage differencing differential input buffered amplifier (VD-DIBA) [16,17], voltage differencing transconductance amplifier (VDTA) [18,19], voltage differencing current conveyor (VDCC) [20,21], voltage differencing buffered amplifier (VDBA) [22], current controlled current conveyor transconductance amplifier (CCCCTA) [23], current controlled current differencing transconductance amplifier (CCCDTA) [24,25], current controlled current feedback amplifier (CC-CFA) [26], current follower transconductance amplifier (CFTA) [27], current controlled current follower transconductance amplifier (CCCFTA), [28] and current backward transconductance amplifier (CBTA) [29].

In the following, we present new electronically tunable grounded/floating inductance simulators realized with the ABB named the Z-copy current follower controlled current conveyor (ZC-CFCCC). To the best knowledge of the authors, ZC-CFCCC has not been put to use yet for the realization of electronically controllable simulated inductors.

2. Electronically tunable grounded inductor

A current follower multiple-output current conveyor (CF-MOCC) was introduced in [1]. In the present work, we have modified its structure by taking out an additional Z copy of the input current and used a current controlled

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conveyor in its second stage to realize a ZC-CFCCC. Thus, the ZC-CFCCC is a five-port active building block characterized by the following terminal equation:

$$\begin{bmatrix} V_p \\ V_i \\ I_z \\ I_{zc} \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 & 0 \\ 0 & -R_i & 1 & 0 & 0 \\ 1 & 0 & -Y_z & 0 & 0 \\ 1 & 0 & 0 & -Y_{zc} & 0 \\ 0 & 1 & 0 & 0 & -Y_x \end{bmatrix} \begin{bmatrix} I_p \\ I_i \\ V_z \\ V_{zc} \\ V_x \end{bmatrix} \tag{1}$$

Here, R_p represents the input resistances of port p while R_i represents the output resistance of the voltage buffer implemented between port z and port i. Y_z, Y_{zc}, and Y_x each constitute a parallel combination of a resistor and a capacitor and represent the parasitic admittances associated with the ports z, zc, and x. When implemented in CMOS hardware such as that shown in Figure 1, the values of R_p and R_i are given by:

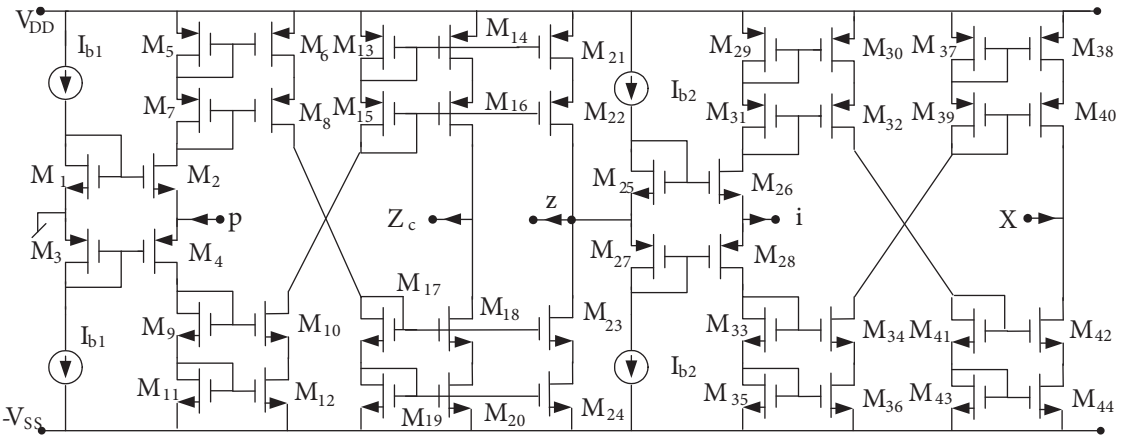

Figure 1. An exemplary CMOS implementation of the ZC-CFCCC.

$$R_p = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b1}}}, R_i = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b2}}} \tag{2}$$

Thus, R_p, and R_i can be controlled by external DC bias currents I_{b1} and I_{b2} [23,24,28].

Consider now the proposed new realization of the electronically tunable grounded inductor shown in Figure 2. A straightforward analysis of this circuit, using the port relationships of the ZC-CFCCC given in Eq. (1), gives the input impedance of the circuit as (when Y_z, Y_{zc}, and Y_x, the parasitic admittances at ports z, zc, and x, are taken to be zero):

$$Z_i = sR_pR_iC \tag{3}$$

where

$$R_p = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b1}}} \text{ and } R_i = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_{b2}}}$$

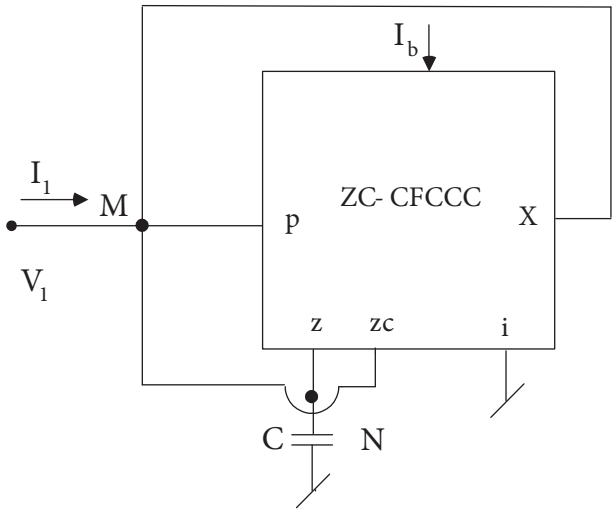

Figure 2. The proposed new electronically tunable grounded inductor.

If $I_{b1} = I_{b2} = I_b$, then the simulated inductance value is given by:

$$L_s = C\frac{1}{\left(8\mu_n C_{ox}\left(\frac{W}{L}\right) I_b\right)} \tag{4a}$$

It may be noted here that R_p and R_i need not be equal. Availability of two external currents for realization of a given value of inductance results in more flexibility in selecting these current sources. If only one current is available to control the value of the simulated inductor then the other resistor required will be a fixed-valued resistor. Therefore, the realized inductance can be varied electronically over a wider range.

On the other hand, if these parasitic elements are taken into consideration, then the impedance Z_{in} is given by:

$$Z_{in}(j\omega) = R_s + j\omega L_s \tag{4b}$$

$$R_s(\omega) = \frac{\omega^2(a_1b_1 - a_0b_2) + a_0b_0}{\omega^4 b_2^2 + \omega^2(b_1^2 - 2b_0b_2) + b_0^2} \tag{4c}$$

$$L_s(\omega) = \frac{-a_1b_2\omega^2 + (a_1b_0 - a_0b_1)}{\omega^4 b_2^2 + \omega^2(b_1^2 - 2b_0b_2) + b_0^2} \tag{4d}$$

The quality factor is:

$$Q(\omega) = \frac{\omega\left[-a_1b_2\omega^2 + (a_1b_0 - a_0b_1)\right]}{\omega^2(a_1b_1 - a_0b_2) + a_0b_0} \tag{4e}$$

where

$$\begin{aligned} &a_1 = R_pR_iR_xR_zR_{zc}(C + C_z);\quad a_0 = R_pR_iR_xR_{zc};\quad b_2 = R_pR_iR_xR_zR_{zc}(C + C_z)(C_x + C_{zc});\\ &b_1 = [R_pR_iR_z(C + C_z)(R_x + R_{zc}) + R_pR_iR_xR_{zc}(C_x + C_{zc})];\quad b_0 = R_pR_i(R_x + R_{zc}) + R_xR_zR_{zc}. \end{aligned} \tag{4f}$$

3. Electronically tunable floating inductor

From the circuit of the proposed electronically tunable grounded inductor it is observed that the configuration implements an active gyrator with its input port being node M and the output port being node N. A straightforward analysis of this gyrator circuit results in the following short circuit admittance matrix:

$$[Y] = \begin{bmatrix} 0 & \frac{1}{R_i} \\ -\frac{1}{R_p} & 0 \end{bmatrix} \tag{5}$$

Therefore, using two such active gyrators and one grounded capacitor embedded between them, an electronically tunable floating inductor (FI) can be realized as shown in Figure 3, for which the short-circuit admittance matrix is found to be:

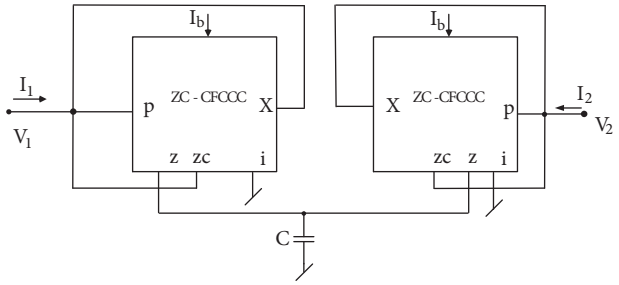

Figure 3. The proposed new electronically tunable floating inductor.

$$[Y] = \frac{1}{sC}\begin{bmatrix} \frac{1}{R_i R_p} & -\frac{1}{R_i^2} \\ -\frac{1}{R_p^2} & \frac{1}{R_i R_p} \end{bmatrix} = \frac{1}{sCR^2}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{6}$$

where

$$R_p = R_i = R = \frac{1}{\sqrt{8\mu_n C_{ox}\left(\frac{W}{L}\right) I_b}}$$

Thus, the value of the realized floating inductance can be varied by changing external bias current I_b. It may be noted that this can be implemented quite easily by supplying equal DC bias currents to the two ZC-CFCCCs, unlike the constraints imposed by passive component matching as prevalent in many of the classical floating inductance simulation circuits using op-amps. If the parasitic admittances associated with ports z, zc, and x are taken into account then the nonideal short-circuit admittance parameters (for $\mathrm{I}_{b1} = \mathrm{I}_{b2} = \mathrm{I}_b$, $\mathrm{R}_i = \mathrm{R}_p = \mathrm{R}$) are found to be:

$$y_{11} = \frac{\left(\frac{1}{R_{EQ}^2} + \frac{1}{R_{EQ}R_z} + \frac{1}{R^2}\right) + \left(2\frac{C_P}{R_{EQ}} + \frac{C}{R_{EQ}} + \frac{C_P}{R_z} + \frac{C_z}{R_{EQ}}\right)s + \left(C_P^2 + C_P C + C_P C_z\right)s^2}{\left(\frac{1}{R_{EQ}} + \frac{1}{R_z} + \left(C_P + C_z + C\right)s\right)} \tag{7}$$

$$y_{12} = \frac{-\frac{1}{R^2}}{\left(\frac{1}{R_{EQ}} + \frac{1}{R_z} + \left(C_P + C_z + C\right)s\right)} = y_{21} \tag{8}$$

$$y_{22} = \frac{\left(\frac{1}{R_z^2} + \frac{1}{R_{EQ}R_z} + \frac{1}{R^2}\right) + \left(2\frac{C_z}{R_z} + \frac{C}{R_z} + \frac{C_P}{R_z} + \frac{C_z}{R_{EQ}}\right)s + \left(C_z^2 + C_zC + C_PC_z\right)s^2}{\left(\frac{1}{R_{EQ}} + \frac{1}{R_z} + \left(C_P + C_z + C\right)s\right)} \tag{9}$$

where

$$R_{EQ} = R_{zc}||R_x, C_P = C_{zc} + C_x, R_s = \frac{R_pR_i}{R_z} \; and \; L_s = R_pR_i\left(C + C_z\right) \tag{10}$$

The expressions for the y-parameters, as above, appear to be quite formidable and do not lend themselves to meaningful interpretations directly. We therefore measure the y-parameters of the circuits using PSPICE simulations and plot their frequency responses along with the theoretical plot of Eqs. (7)–(9) in MATLAB in the next section.

4. SPICE simulations, application examples, and results

The CMOS implementation of the proposed ZC-CFCCC using 0.18-μm TSMC process technology parameters has been used to verify the workability of the circuits presented in this paper. Measured values of the characterizing parameters of the ZC-CFCCC given in Eq. (1) at DC bias voltage $\pm$2.5 V and DC bias currents 40 μA are given in Table 1, whereas the aspect ratios of the various MOSFETs are shown in Table 2. The measured value of THD of an amplifier configured with ZC-CFCCC when the input current was varied between 20 and 80 μA was found to vary between 0.75% and 3.5% at 1 MHz (when z and i terminals are terminated with equal resistance of 10 kΩ).

Table 1. Characteristic parameters of ZC-CFCCC.

S. no.	Parameter	Value
1	R_p	591 Ω
2	R_z	4.9178 MΩ
3	C_z	6.3234×10^{-14} F
4	R_{zc}	4.9178 MΩ
5	C_{zc}	7.2123×10^{-15} F
6	R_x	4.79990 MΩ
7	C_x	7.3772×10^{-15} F
8	R_i	591 Ω
9	Power consumption	2.47 mW
10	Linear range of current transfers I_p/I_z, I_p/I_{zc}, and I_i/I_x (mA)	–0.8 to +0.75 with gain 1.00049
11	Linear range of voltage transfers (V) V_z/V_i	–3.0 to +3.0 with gain 0.9882
12	3 dB bandwidth (MHz) (i) I_p/I_z,and I_p/I_{zc} (ii) I_x/I_i (iii) V_i/V_z	 527 1215.8 2860

Table 2. Aspect ratios of MOSFETs used in ZC-CFCCC realization.

MOSFETs	W/L (μm/μm)
M_1, M_2, M_{25}, M_{26}	25/0.25
M_3, M_4, M_{27}, M_{28}	50/0.25
M_5–M_{24}, M_{29}–M_{44}	2.5/0.25

The proposed grounded inductor circuit was simulated with C = 1 nF for different values of bias current I_b starting from 0.01 μA to 200 μA. The variation of inductance with bias current is shown in Figure 4, which is similar to the variation of inductance with bias current for other electronically tunable lossless grounded inductance circuits, such as the one given in [20]. It was found that inductance value could be varied from 998 H to 135 μH, over the above range. The typical value of inductance for a bias current of 40 μA was found to be 350 μH while the power consumption was 2.47 mW.

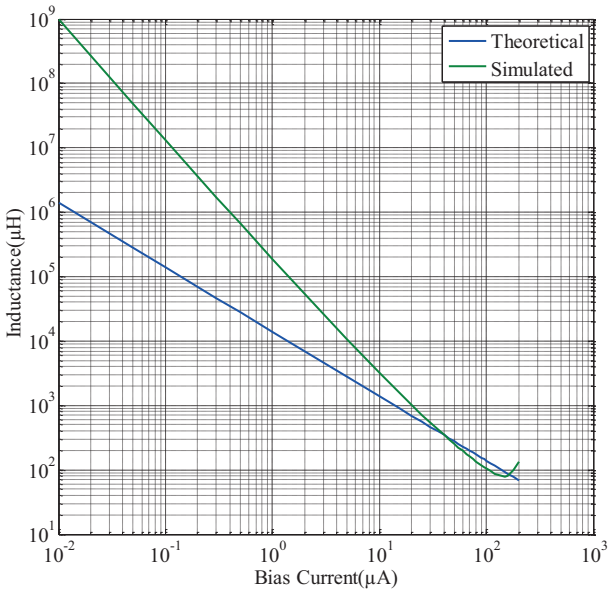

Figure 4. Variation of inductance with bias current.

The frequency response of the simulated inductor was also determined in PSPICE (for I_b = 40 μA) and is shown in Figure 5 (L = 350.04 μH at a frequency of 35.3 KHz). Independent simulations have shown that the value of the inductance remains within a tolerance value of 10% up to a frequency of 2.99 MHz. We have also superimposed on the frequency response the theoretical plots as obtained from Eqs. (4c) and (4d). From the frequency response plots it is observed that the inductance value remains nearly constant only up to a particular frequency. This is corroborated by the behavior of simulated lossless grounded inductors realized with other active building blocks [15–18]. Though the parasitic resistance associated with the simulated inductor becomes negative at higher frequencies, the application circuits have not shown any unstable behavior. The quality factor of the simulated grounded inductor (for bias current of 40 μA) was also measured and found to be 335 at 10 kHz. Figure 6 shows the variation of quality factor with frequency. The simulated results agree quite well with the theoretical ones. The discrepancy between theoretical and simulated results mainly stems from nonideal gain and parasitic impedance effects of the ZC-CFCCC.

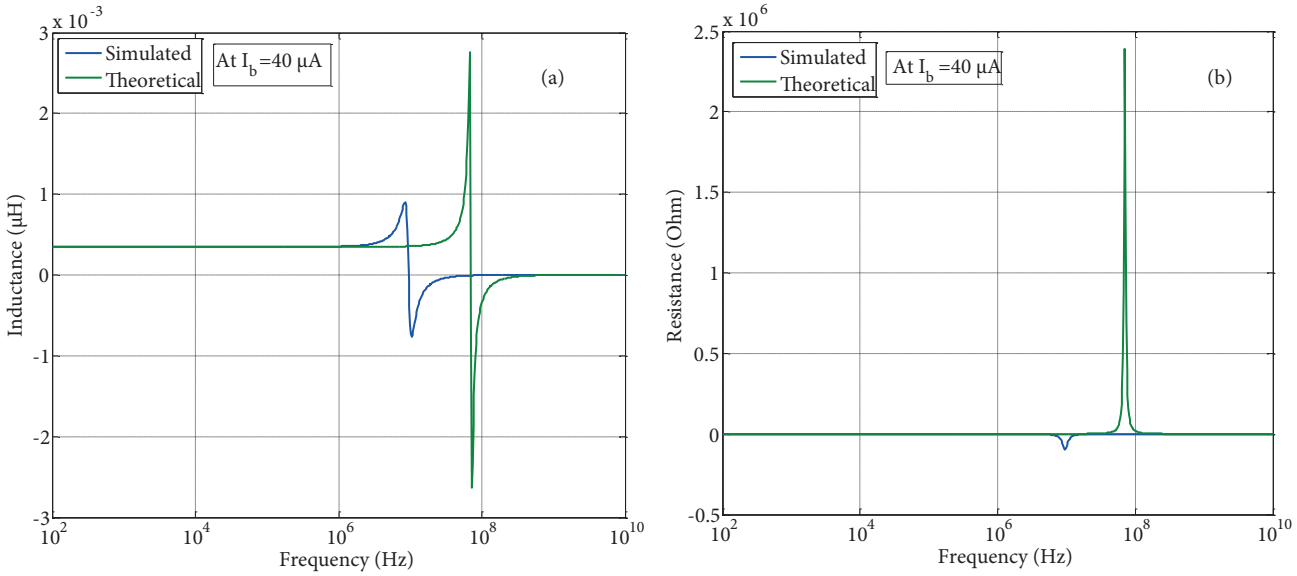

Figure 5. Frequency response of simulated lossless grounded inductor: a) variation of inductance value with frequency; b) variation of parasitic resistance with frequency.

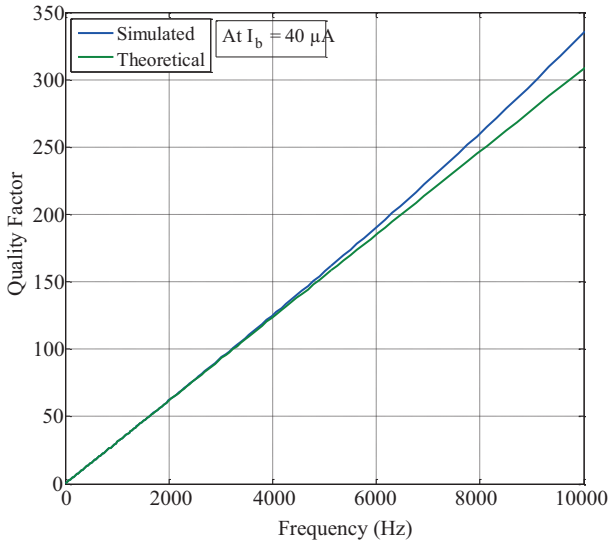

Figure 6. Variation of quality factor with frequency.

An input current with a triangular waveform (20 μA amplitude and 1 kHz frequency) was applied to the proposed inductor (46.45 μH). The output voltage, a square wave (22 μV at 1 KHz) as shown in Figure 7, was obtained, which further confirmed the workability of the electronically tunable grounded inductor.

The second-order band-pass filter shown in Figure 8 was used to verify the tunability of the pole frequency with bias current. The pole frequency and the bandwidth of the filter are given by pole frequency $f_o = \frac{1}{2\pi\sqrt{LC_1}}$ and bandwidth $BW = \frac{1}{2\pi RC_1}$.

The band-pass filter was designed with the following component values: R = 3 kΩ, C = 1 nF, C_1 = 10 pF, and bias current varied from 35 μA to 70 μA to vary the pole frequency without affecting the bandwidth.

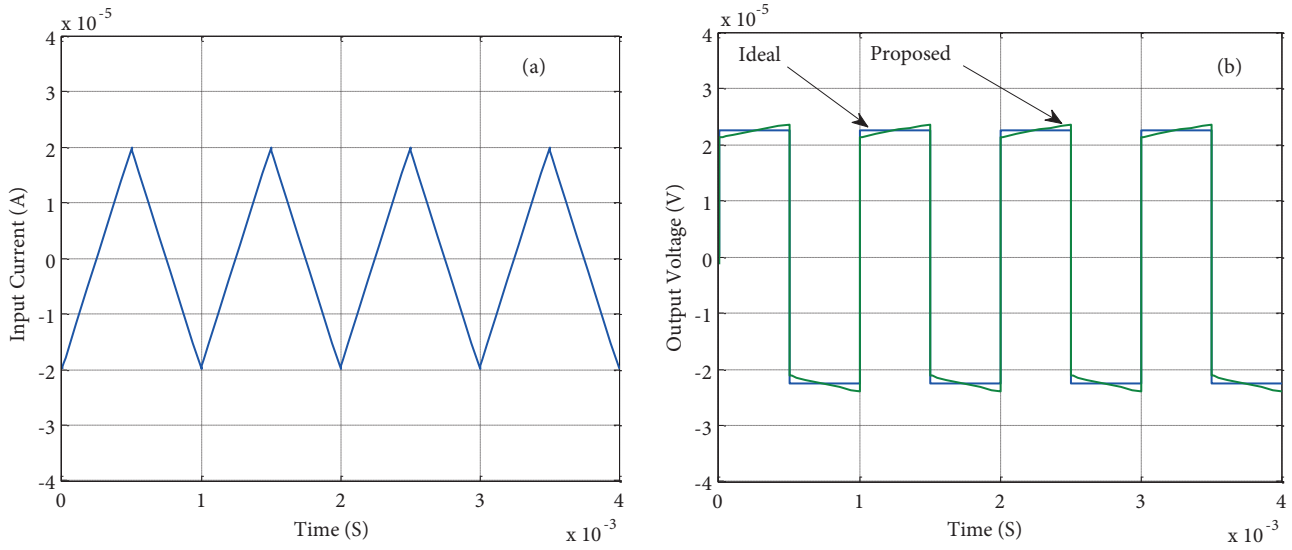

Figure 7. Time domain analysis of the proposed grounded inductor: a) input current waveform; b) output voltage waveform.

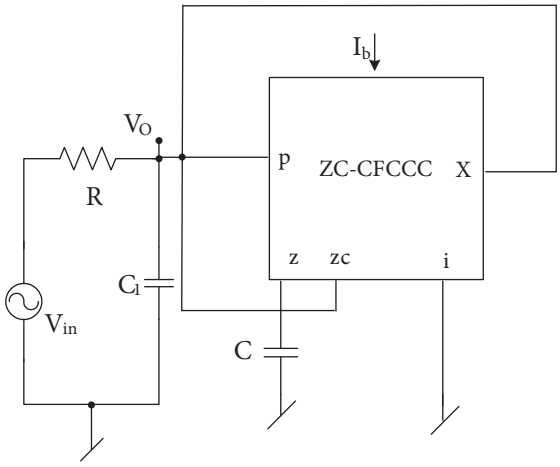

Figure 8. Tunable second-order RLC band-pass filter.

Figure 9 shows the frequency response of the band-pass filter with different values for the pole frequency. These results are in close agreement with the theoretical values ($f_0 \propto \sqrt{I_b}$) with the maximum error in the pole frequency being less than 10%. The maximum error in bandwidth has been found to be about 2%. The THD in the output was also measured and found to lie within 0.3%–2.4% when the input amplitude was varied in the range of 10–150 mV.

The frequency response of the floating inductor was determined through PSPICE simulations to find its usable frequency range. Figure 10 shows the frequency response of the short-circuit admittance parameters. We have also superimposed the frequency response as computed from Eqs. (7)–(9). There is a very close agreement between these three plots. Independent simulations have indicated that the floating inductor can be used up to a frequency of 2.94 MHz (at $I_b = 40$ μA); the simulated inductance was within 10% of the designed value of 350 μH while the associated resistance was varying between less than 142 mΩ to –579.20 Ω up to a frequency of 2.94 MHz.

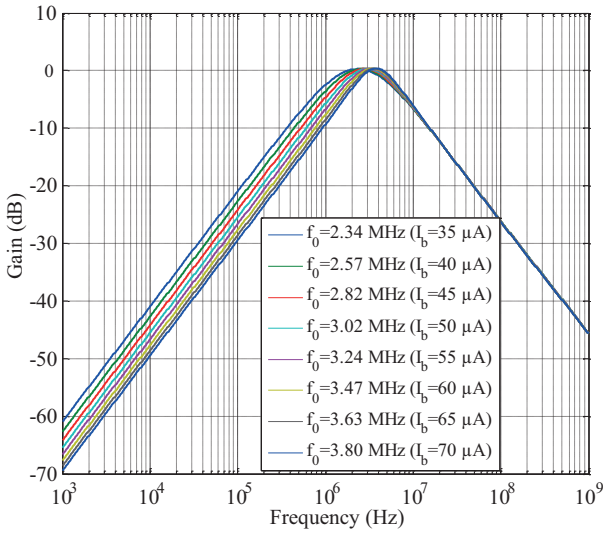

Figure 9. Frequency response second-order BPF for different values of bias current.

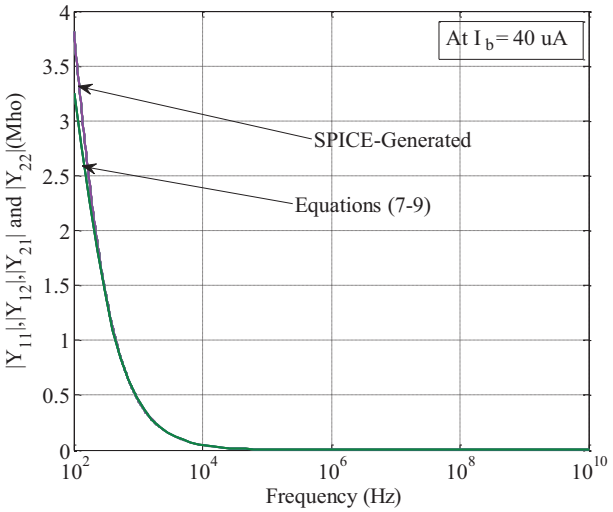

Figure 10. Frequency response of the y parameters of the simulated floating inductor.

We have used the proposed floating inductor to implement a fourth-order Butterworth low-pass filter as shown in Figure 11. Starting from the nominal values of the components for the normalized low-pass filter at 1 Hz as $R_s = R_L = 1\ \Omega$, $L_1 = 0.7654$ H, $L_2 = 1.8478$ H, $C_1 = 1.8478$ F, and $C_2 = 0.7654$ F [30], after appropriate frequency and impedance scaling we get the following values of passive components for the filter cut-off frequency of 500 kHz: $R_S = R_L = 1$ KΩ, $L_1 = 0.2437$ mH (C =1 nF, $I_b = 51.46\ \mu$A), and $L_2 = 0.5884$ mH (C = 1 nF, $I_b = 28.37\ \mu$A). This finally resulted in a fourth-order active filter structure using all grounded capacitors, as preferred for IC implementation. Frequency response of the resulting fourth-order low-pass Butterworth filter is shown in Figure 12. The value of the cut-off frequency found from the simulation was 500.50 kHz, showing a very close agreement with the theoretical value of 500 kHz. The THD in the output

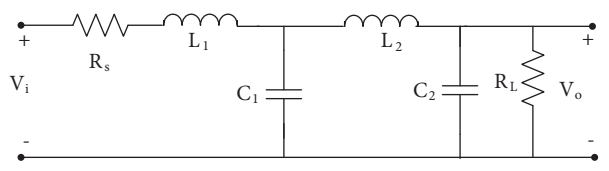

Figure 11. Prototype fourth-order low-pass Butterworth filter.

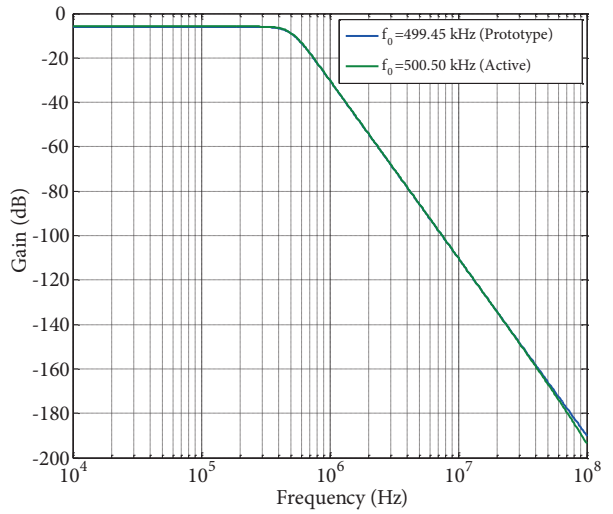

Figure 12. Frequency response of the fourth-order low-pass Butterworth filter.

was also measured when the amplitude of the input voltage was varied between 10 mV and 150 mV and found to vary between 0.2% and 7%.

To study the effect of mismatches in the component values within the floating inductors on the performance of the circuit of the fourth-order low-pass Butterworth filter, Monte Carlo simulations have been carried out by allocating 1% tolerances to the component values (capacitors C = 1 nF) within both of the floating inductors and performing 100 runs. The results for the 1% tolerance are shown in Figure 13. The value of the simulated cut-off frequency was found to be 500.50 kHz and Monte Carlo analysis shows that the median value

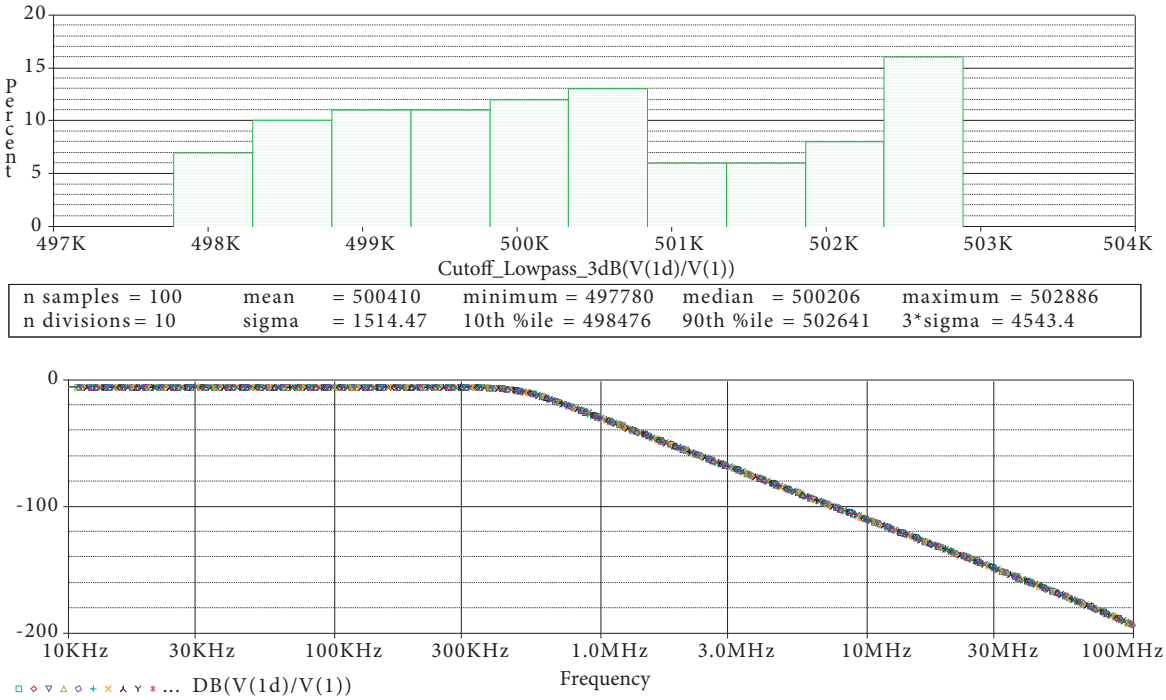

Figure 13. Simulation results of Monte Carlo analysis for fourth-order low-pass Butterworth filter.

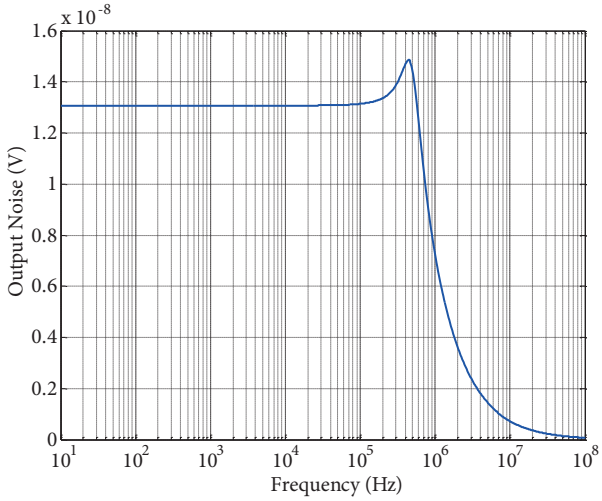

Figure 14. Output noise variation for fourth-order low-pass Butterworth filter.

Table 3. Comparison with other previously published lossless grounded and floating inductors realized with synthetic active building blocks.

Ref.	Type*	Number of ABBs	Number of resistors	Number of capacitors	Free from component passive matching?	Tunability	Technology	Power supply	Power dissipation
[11]	G	2: OTRA	5	1F	No	No	Discrete (AD844)	±10 V	NA
[12]	G	1: OTRA	3	2F	No	No	0.5 μm/AD844	±1.5 V/±5 V	0.809/260 mW
[13]	F	2: DVCC	2	1G	Yes	No	0.18 μm	±1.25 V	NA
[14]	F	3/4: CDBA	4 [VCR]	1G	Yes	Yes	0.5 μm	±2.5 V	NA
[15]	G	2: CDTA	0	1G	Yes	Yes	0.5 μm	±2.5 V	NA
	F	3: CDTA	0	1G	Yes	Yes	0.5 μm	±2.5 V	NA
[16]	G	2: VD-DIBA	0	1G	Yes	Yes	Discrete ((AD844) + CA3080))	±1 V	62.5 mW
	F	3: VD-DIBA	0	1G	Yes	Yes	Discrete ((AD844) + CA3080))	±1 V	62.5 mW
[17]	G	1: VD-DIBA	1	1G	Yes	Yes	0.35 μm	±2 V	NA
	F	2: VD-DIBA	1	1G	No	Yes	0.35 μm	±2 V	NA
[18]	G	1: VDTA	0	1G	Yes	Yes	0.18 μm	±0.9 V	NA
	F	2: VDTA	0	1G	Yes	Yes	0.18 μm	±0.9 V	NA
[19]	F	1: ZC-VDTA	0	1G	Yes	Yes	0.18 μm	±0.9 V	1.25 mW
[20]	G	1: VDCC	1	1G	Yes	Yes	0.18 μm	±0.9 V	0.869 mW
[21]	F	1: VDCC	1	1G	Yes	Yes	0.18 μm	±0.9 V	NA
[22]	G	1: VDBA	1	1F	Yes	Yes	Discrete (OPA860)	±5 V	NA
[23]	G	1: CCCCTA	0	1G	Yes	Yes	0.35 μm	±1.5 V	899 μW
[24]	F	1: CCCDTA, 2: VB	0	IG	Yes	Yes	0.35 μm	±1.5 V	1.48 mW
[25]	F	1: CCCDTA, 2: VB	0	1G	Yes	Yes	Bipolar ALA400	±1.5 V	1.23 mW
[26]	G	2: CC-CFA	0	1G	Yes	Yes	(ALA400 + 0.35 μm)	±1.5 V	4.16 mW
[27]	F	3: CFTA	0	1G	Yes	Yes	Bipolar ALA400	±1.5 V	NA
[28]	G	1: CCCFTA	0	1G	Yes	Yes	0.5 μm	±2.0 V	NA
[29]	F	2: CBTA	2	1G	Yes	Yes	0.25 μm	±2.5 V	NA
[45]	F	1: MCFOA	2	1G	Yes	No	0.35 μm	±1.5 V	NA
[46]	G	1: New CFOA	2	1F	Yes	No	Discrete	±15 V	NA
[47]	G	1: CFOA–	2	1F	Yes	No	0.13 μm	±6 V/0.75 V	890 μW
[48]	G	1: MICCII–	2	1F	No	No	0.35 μm	±2.5 V	17.6 mW
Proposed	G	1: ZC-CFCCC	0	1G	Yes	Yes	0.18 μm	±2.5 V	2.47 mW
Proposed	F	2: ZC-CFCCC	0	1G	Yes	Yes	0.18 μm	±2.5 V	4.94 mW

*F: Floating, G: grounded.

of cut-off frequency is f_0 = 500.41 kHz, which indicates that the mismatch in the component values within the proposed floating inductors does not have a large effect on the realized cut-off frequency.

PSPICE noise analysis has also been performed on the fourth-order low-pass Butterworth filter and variations in the output noise are shown in Figure 14.

The PSPICE simulation results presented in this section thus establish the workability and applications of the proposed new inductance simulators using ZC-CFCCC.

5. Comparison with previously published circuits

A comparison of the various salient features of the proposed configurations as compared to other previously known lossless grounded and FI simulators realized with synthetic active building blocks is now in order, presented in Table 3. It is observed from the table that the proposed circuits, with the exceptions of the circuits given in [18,19,28], are the only circuits that realize an electronically tunable lossless grounded inductor employing a single active building block, no passive resistors, and a single grounded capacitor and do not require any passive component matching constraint. It may be mentioned here that because of the terminal equations of the ZC-CFCCC, CC-CDTA, and CC-CCTA being somewhat similar, the proposed inductance simulation circuits may appear to be somewhat similar to the circuits proposed in [23,25], where CC-CCTA and CC-CDTA were used as ABBs. On the other hand, yet another building block proposed in [1], namely the CDCC [31–33], can also be configured as a ZC-CFCCC if we do not use one of its input current terminals and use a current-controlled conveyor (instead of CCII) in the second stage. The grounded inductance simulators used here can directly be used in the simulation of LC ladders in contrast to the lossy inductance simulators realized with other active building blocks of recent origin [34–44].

6. Concluding remarks

In this paper, new electronically tunable, lossless grounded and floating inductance simulation circuits using the ZC-CFCCC as an active element were proposed. The proposed circuits employ only a single ZC-CFCCC for grounded inductance simulation and two ZC-CFCCCs for floating inductance simulation along with a single grounded capacitor as preferred for IC implementation. Thus, the new circuits provide a number of advantageous features simultaneously, such as use of a canonic number of active and passive elements, electronic tunability by means of external bias currents, complete absence of passive component matching, and employment of a single grounded capacitor, as preferred for IC implementation. For simulation of floating inductance, the only constraint required is the equality of the two bias currents, which can be easily met by using current copier cells. The workability of the new propositions as well as their two typical application circuits has been verified through PSPICE simulations using 0.18-μm TSMC CMOS technology parameters. It is believed that the proposed ZC-CFCCC-based electronically tunable inductance simulators add new alternatives to the existing repertoire of synthetic ABB-based inductance simulators, as shown in Table 3. This table also contains modified CFOAs and modified inverting second-generation current conveyor-based inductance simulators [45–48] but does not include circuits based upon traditional current conveyors (see those in [49–52] and the references cited therein).

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Regular paper

Fully-differential current-mode higher order filters using all grounded passive elements

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ABSTRACT

In this paper the realization of nth order ($n \geq 3$) fully-differential current-mode filters using Current Differencing Current Conveyors (CDCC) has been presented which results in circuits employing *all grounded passive elements*. In contrast to earlier known realizations of fully-differential filters which invariably require more than one capacitors per pole, the proposed realization employs only one capacitor per pole. The cut-off frequency of the realized filter can be electronically tuned when all the grounded resistors associated with the integrators are implemented by identical CMOS grounded voltage-controlled-resistors (VCR) driven by a common control voltage. The methodology has been illustrated by realizing a fifth order Butterworth filter as a specific example whose workability has been verified using SPICE simulations in 0.18 μm TSMC technology. A reduced-component-version of the designed fifth order Butterworth filter has also been presented which also employs all grounded RC components but does not have electronic-tunability. Some representative simulation results have been included.

1. Introduction

Higher order RC active filters (of order $\mathbf{n} \geq 3$) are useful as anti-aliasing filtering in data converters and also find use in display of radar target tracks and high quality audio applications. When realized in fully-differential form, they have the advantage of lower harmonic distortion, higher dynamic range and immunity to power supply induced common mode noise. A large number of research papers have been published in the past on single-ended biquads and higher order filters (for instance, see [1–23] and the references cited therein) which have also been documented in a number of recent books (for example, see [24,25]). On the other hand, fully-differential biquads and fully-differential higher order filters have also been investigated by several researchers, for instance, see [26–56]. The works mentioned in references [26,31–33,36–38,40,43,44,46,48–51,54,55] deal with fully-differential voltage-mode (VM)/current-mode (CM) higher order filters.

To put the work presented in this paper in right perspective, it appears necessary to present a brief overview of the earlier works on the design of fully-differential VM and CM higher order filters. In this context, it is found that many different active building blocks (ABB) have been employed in the past to realize fully-differential filters exhibiting different properties. The ABBs employed so far include Voltage–mode operational amplifier [41], Dual output Operational Amplifier (Dual OA) [37,43,46,50], four-input-two-output OA (four-input two-output Operational amplifier) [28,55], Operational Transconductance Amplifier (OTA) [26,31,32,36,38,40,54], Fully Differential Second Generation Current Conveyor (FDCCII) [27,42], Fully Balanced Differential Difference Amplifier (FBDDA) [29], Fully Balanced Four-terminal Floating Nullor (FBFTFN) [30], Current mode Differential Waveport Terminator [33], Fully Differential Current Feedback Operational Amplifier (FDCFOA) [34], Differential Input Balanced Output Current Operational Amplifier (DIBOCOA) [35], Multi-output Second Generation Current Conveyor (MOCCII) [39], Current-controlled Fully Balanced Second Generation Current Conveyor (CFBCCII) [44,48], Fully Differential Current Follower (FD-CF) [45,47,49,56], Multi-output Transconductance Amplifier (MOTA) [47,56], Differential Difference Amplifier (DDA) [51], Multi-output Current Follower (MO-CF), Dual Output Current Follower (DO-CF), Digitally Adjustable Current Amplifier (DACA) [52] Current Differencing Current Conveyor (CDCC) [53], Fully Differential Current Follower (FD-CF), Digitally Adjustable Current Amplifier (DACA) and Multi-output Transconductance Amplifier (MOTA) [56]. Table 1 summarizes the salient features of the earlier works

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Table 1
An overview of fully-differential higher order filter structures using different ABBs.

Ref.	No of ABBs	Order and type	R count	C count	All Grounded passive elements	Electronic tunability	Technology	Supply voltage	Power dissipation
[26]	OTA: 10 BUFFER: 2	7; VM (Elliptic)	–	13	No	Yes	1 μm	±2.5 V	75 mW
[31]	OTA:8	4;VM (Butterworth)	–	8	Yes	Yes	0.35 μm	±2.7 V	NA
[32]	OTA:5	5;VM (Elliptic)	32	18	No	Yes	0.18 μm	0.5 V	NA
[33]	WPT:6	3; CM (Elliptic)	–	6	No	Yes	0.35 μm	±2.5 V	NA
[36]	OTA:9	7;VM (Equi-ripple with gain boost)	–	14	Yes	Yes	0.25 μm	2 V	216 mW
[37]	Dual OA:4	4;VM (Chebyshev)	18 (VCR)	8	No	Yes	0.35 μm	3.3 V	16 mW
[38]	OTA:3	3;CM (Butterworth)	–	6	Yes	Yes	0.35 μm	1.5 V	NA
[40]	OTA:7	3;CM (Butterworth)	–	6	Yes	No	0.18 μm	1.8 V	16.77 mW
[43]	Dual OA:6	6;VM (Chebyshev)	26	12	No	Yes	0.18 μm	±1.8 V	NA
[44]	CFBCCII:4	4;CM (Butterworth)	–	8 (2n)	Yes	Yes	0.35 μm	±1.65 V	NA
[46]	Dual OA:10	5;VM (Complex Chebyshev)	64	20	No	Yes	0.18 μm	1.8 V	NA
[48]	CFBCCII:7	3; CM (Elliptic)	8	6	Yes	Yes	0.35 μm	±1.65 V	22 mW
[49]	FD-CF:4	4;CM (Butterworth)	6	5 (n + 1)	No	No	NA	NA	NA
		4;CM (Butterworth)	5	6 (n + 2)	No	No	NA	NA	NA
[50]	Dual OA:6	6;VM (Inverse Chebychev)	36	12	No	Yes	0.13 μm	1.5 V	9.45 mW
[51]	DDA:2	5;VM (Bessel)	10	20	No	Yes	0.18 μm	3.3 V	1 mW
	DDA:3	7;VM (Bessel)	14	28	No	Yes	0.18 μm	3.3 V	1.5 mW
[54]	OTA:2n	VM (High Even order Biquadratic)	–	2n	Yes	No	0.35 μm	±2 V	NA
[55]	Four-input-Two-output OAs:3	6;VM (Sallen-Key)	12	12	No	Yes	0.35 μm	1.2 V	12.6 mW

NA: Data not available.

done on the higher-order fully-differential filters realized with the various ABBs mentioned above.

Although Operational Transconductance Amplifiers (OTA) and Current Conveyors (CC) are commercially available as off-the-shelf ICs whereas a CDCC is not and therefore, the comparison of the proposed CDCC-based structure with those employing OTAs and CCs may appear to be somewhat unjustified, however, for the sake of giving a complete picture the same have also been included in Table 1. From Table 1, it is observed that earlier known fully-differential higher order filters suffer from one or more of the following drawbacks:

(i) Use of either more than double the number of capacitors per filter pole [32,46,51] or twice the number of capacitors per filter pole [31,33,36–38,40,43,44,48,50] or use of more than one capacitor per filter pole but less than double the number of capacitors per filter pole [26,49].
(ii) Use of *floating* passive elements [26,32,33,37,43,46,49–51,55].
(iii) Non-availability of electronic tuning of the cut-off frequency [40,49,54].

It is also observed from Table 1 that except in the works [44,49,54], no other general methodology for the realization of an nth order fully-differential CM filters appears to have been reported *explicitly* in the open literature earlier.

We now present in Table 2 the salient features of the fully-differential CM filters realized with the general methodologies proposed in [44,49,54], *vis-à-vis* those realizable with the methodology being proposed in this paper, to put the proposed methodology/circuits in right perspective.

From Table 2, it is revealed that the CDCC-based general methodology to realize a fully-differential CM higher order filter being presented here would provide the following features *simultaneously* which are not available simultaneously in any of the previously known methods/circuits presented in Table 2.

(i) use of all grounded passive elements
(ii) employment of only one capacitor per pole and
(iii) facilitation of electronic tunability of the cut off frequency.

It is worth mentioning that the methodology employed here may appear to be somewhat similar to the one proposed earlier in [44] but in contrast to the structures proposed in [44] which use double the number of capacitors, we use no more than one capacitor per pole. On the other hand the decomposition of higher-order current-mode transfer functions and the realization of electronically tunable higher order filters with all grounded passive elements for single ended filters have been presented in [21,22].

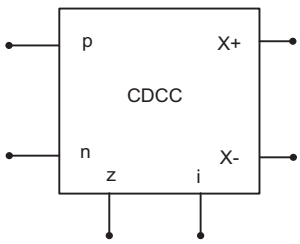
2. Realization of CDCC-based fully-differential current-mode higher order filters

CDCC [57] is a six-terminal ABB whose symbolic representation and the instantaneous port relations are shown in Fig. 1. The current at the 'z' terminal is the difference of the two input currents and the potential at the terminal 'i' tracks the potential at the

Table 2
Comparison of the proposed methodology with the existing general methodologies for nth order fully-differential CM filters.

Ref.	ABB count	Order and type (n)	R count	C count	All Grounded passive elements	Electronic tunability	Technology	Supply voltage	Power dissipation
[44]	CFBCCII:n	n (Butterworth)	–	2n	Yes	Yes	0.35 μm	±1.65 V	NA
[49]	FD-CF:n	n (Butterworth)	n + 2	n + 1	No	No	NA	NA	NA
		n (Butterworth)	n + 1	n + 2	No	No	NA	NA	NA
[54]	OTA:2n	n (Cascaded-biquads)	–	2n	Yes	No	0.35 μm	±2 V	NA
Proposed	CDCC:2n	n (Butterworth)	3n	n	Yes	Yes	0.18 μm	±2.5 V	26.1 m W

NA: Data not available.



$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_i \end{bmatrix}$$

Fig. 1. Symbolic notation and port-relations of the CDCC.

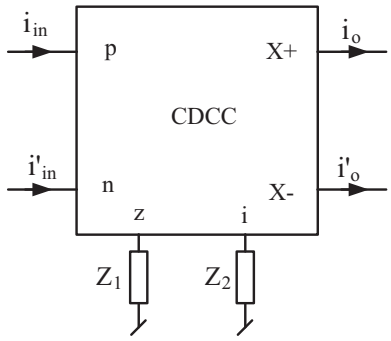


Fig. 2. The general configuration to realize a scalar, lossless integrator or lossy integrator.

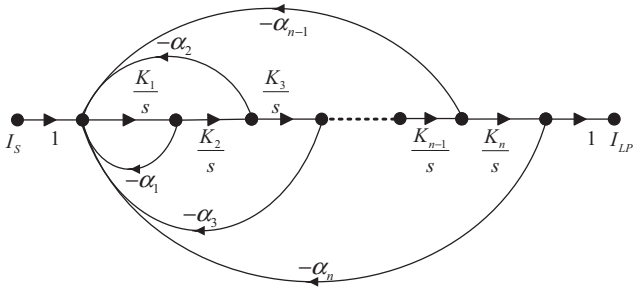


Fig. 3. Signal flow graph corresponding to an nth-order all pole transfer function.

terminal 'z'. Two complementary currents at the output terminals 'x+' and x- are available which are copies of the current leaving the 'i' terminal.

Consider now the CDCC block of Fig. 2 whose z and i terminals are terminated into impedances Z_1 and Z_2. By straight forward analysis, the output currents are given by

$$i_o = -i'_o = \frac{Z_1}{Z_2}(i_{in} - i'_{in}) \tag{1}$$

Thus, depending upon the choice (resistive/capacitive) of the impedances Z_1 and Z_2, this block can realize fully differential scalar, lossless integrator and lossy integrator.

Now any given transfer function can be decomposed into its controllable canonical form (CCF) following [58] and fully-differential integrators, constant multipliers and summing/differencing elements may be then used to realize the given transfer function whose general form can be expressed as:

$$T(s) = \frac{b}{a_n s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots\ldots + a_2 s^2 + a_1 s + a_0} = \frac{\frac{b}{a_n s^n}}{1 + \frac{a_{n-1}}{a_n s} + \frac{a_{n-2}}{a_n s^2} + \ldots\ldots + \frac{a_2}{a_n s^{n-2}} + \frac{a_1}{a_n s^{n-1}} + \frac{a_0}{a_n s^n}} \tag{2}$$

where b, a_n, a_{n-1},. . ...a_3, a_2, a_1, a_0, are real positive constants

A signal flow graph is now constructed as shown in Fig. 3. Using Mason's Gain formula [58], the transfer function is given by:

$$\frac{I_{LP}}{I_s} = \frac{\frac{K_1 K_2 \ldots\ldots K_3 K_4 K_n}{s^n}}{1 + \alpha_1 \frac{K_1}{s} + \alpha_2 \frac{K_1 K_2}{s^2} + \alpha_3 \frac{K_1 K_2 K_3}{s^3} + \ldots\ldots\ldots + \alpha_{n-1} \frac{K_1 K_2 K_3 \ldots K_{n-1}}{s^{n-1}} + \alpha_n \frac{K_1 K_2 K_3 \ldots\ldots K_n}{s^n}} \tag{3}$$

The above can be further rearranged as

$$\frac{I_{LP}}{I_s} = \frac{1}{\frac{s^n}{K_1 K_2 K_3 \ldots\ldots K_n} + \alpha_1 \frac{s^{n-1}}{K_2 K_3 \ldots\ldots K_n} + \ldots\ldots + \alpha_{n-1}\frac{s}{K_n} + \alpha_n} \tag{4}$$

When the integrators and scalar-multipliers are realized in their fully-differential forms then the complete realization of the transfer function turns out to be as shown Fig. 4.

A straight forward analysis of the circuit of Fig. 4 results in the following transfer function

$$\frac{I_{LP}}{I_s} = \frac{1}{s^n \left(\frac{R_1 C_1}{2}\right)\left(\frac{R_2 C_2}{2}\right)\ldots\left(\frac{R_n C_n}{2}\right) + s^{n-1}\left(\frac{2R_{x1}}{R_{y1}}\right)\left(\frac{R_2 C_2}{2}\right)\ldots\left(\frac{R_n C_n}{2}\right) + \ldots + s\left(\frac{2R_{x(n-1)}}{R_{y(n-1)}}\right)\left(\frac{R_n C_n}{2}\right) + \left(\frac{2R_{xn}}{R_{yn}}\right)} \tag{5}$$

It is, thus, evident from the realization of Fig. 4 that if the integrator time constants and scalar multiplier gains are chosen appropriately, then by comparing the coefficients of the denominator polynomials of Eqs. (4) and (5), the values of the various resistors and capacitors required to realize a given transfer function may be calculated based on the values of α_i and K_i (i = 1 – n). For instance, by comparing the coefficients of the various terms containing different degree of 's' with a normalized/denormalized Butterworth transfer function, the values of different resistors and capacitors used in the circuit of Fig. 4 to realize such a transfer function can be found. It may be noted that the scalar-multipliers added along with each integrator do result in somewhat larger number of active and passive components, however, this has been done purposely to ensure that all the grounded capacitors in the circuit can have equal values as desired in IC fabrication; also, all the resistors associated with the integrators too can be made equal-valued which is helpful in obtaining the

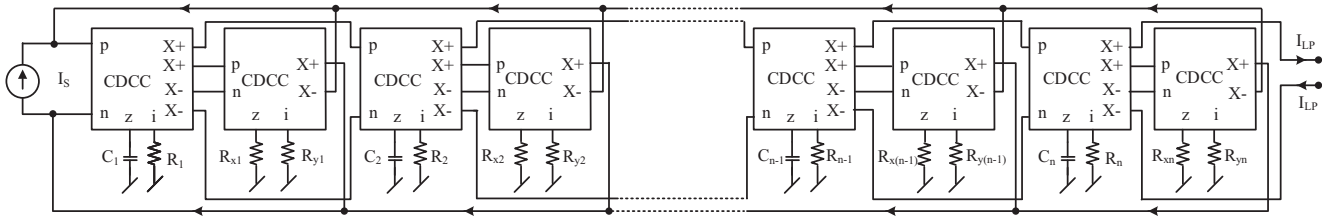


Fig. 4. nth order fully-differential current-mode transfer function realization.

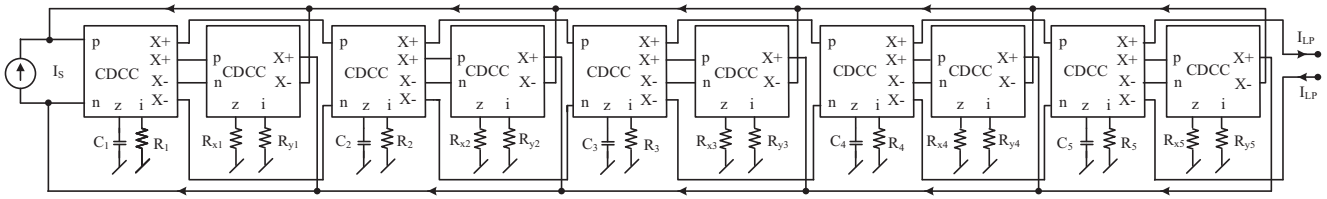


Fig. 5. Fifth order fully-differential current-mode lowpass filter.

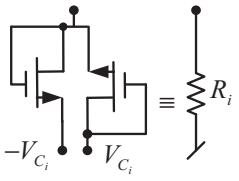


Fig. 6. The MOS VCR . adopted from [59]

electronic tunability of the cut-off frequency of the realised filter by replacing all of these grounded resistors by identical VCRs controlled by a single external control voltage.

3. Design example

We now illustrate the above methodology with the example of a fifth order lowpass Butterworth filter design. We start with the denormalized transfer function of a fifth order lowpass Buterworth filter with a cut-off frequency f_c

$$T(s)=\frac{I_{LP}}{I_S}=\frac{1}{s^5\left(\frac{1}{2\pi f_c}\right)^5+b_4s^4\left(\frac{1}{2\pi f_c}\right)^4+b_3s^3\left(\frac{1}{2\pi f_c}\right)^3+b_2s^2\left(\frac{1}{2\pi f_c}\right)^2+b_1s\left(\frac{1}{2\pi f_c}\right)+b_0} \tag{6}$$

where $b_5 = 1$, $b_4 = 3.2360680$, $b_3 = 5.2360680$, $b_2 = 5.2360680$, $b_1 = 3.2360680$, $b_0 = 1$

The realization of the filter is shown in Fig. 5.

An analysis of the circuit shown above gives the transfer function

$$\frac{I_{LP}}{I_S}=\frac{1}{s^5\left(\frac{R_1C_1}{2}\right)\left(\frac{R_2C_2}{2}\right)\left(\frac{R_3C_3}{2}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)+s^4\left(\frac{2R_{x1}}{R_{y1}}\right)\left(\frac{R_2C_2}{2}\right)\left(\frac{R_3C_3}{2}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)} \\ +s^3\left(\frac{2R_{x2}}{R_{y2}}\right)\left(\frac{R_3C_3}{2}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)+s^2\left(\frac{2R_{x3}}{R_{y3}}\right)\left(\frac{R_4C_4}{2}\right)\left(\frac{R_5C_5}{2}\right)+s\left(\frac{2R_{x4}}{R_{y4}}\right)\left(\frac{R_5C_5}{2}\right)+\left(\frac{2R_{x5}}{R_{y5}}\right) \tag{7}$$

Choosing $R_1 = R_2 = R_3 = R_4 = R_5 = R$ and $C_1 = C_2 = C_3 = C_4 = C_5 = C$, we can write

$$\frac{I_{LP}}{I_S}=\frac{1}{s^5\left(\frac{RC}{2}\right)^5+s^4\left(\frac{2R_{x1}}{R_{y1}}\right)\left(\frac{RC}{2}\right)^4+s^3\left(\frac{2R_{x2}}{R_{y2}}\right)\left(\frac{RC}{2}\right)^3+s^2\left(\frac{2R_{x3}}{R_{y3}}\right)\left(\frac{RC}{2}\right)^2+s\left(\frac{2R_{x4}}{R_{y4}}\right)\left(\frac{RC}{2}\right)+\left(\frac{2R_{x5}}{R_{y5}}\right)} \tag{8}$$

Comparing (6) and (8), the values of the various resistors and capacitors, in terms of f_c and b_i (i = 0–5) are obtained as:

$$f_c=\frac{1}{\pi RC} \tag{9}$$

$$\frac{R_{x1}}{R_{y1}}=\frac{b_4}{2}=1.618,\frac{R_{x2}}{R_{y2}}=\frac{b_3}{2}=2.618,\ \frac{R_{x3}}{R_{y3}}=\frac{b_2}{2}=2.618, \\ \frac{R_{x4}}{R_{y4}}=\frac{b_1}{2}=1.618\ \ and\ \frac{R_{x5}}{R_{y5}}=\frac{b_0}{2}=0.5 \tag{10}$$

It is observed from Eq. (9) that cut-off frequency f_c can be tuned (electronically) if we replace all the resistors of value R used in the realization of the fully-differential integrators by identical MOS VCRs for which, for simplicity, we have chosen the two-MOSFET VCR shown in Fig. 6 [59], keeping the associated capacitors C_i all of the same value. The equivalent resistance R_i realized by the circuit of Fig. 6 is given by [59]

$$R_i=\frac{1}{2\mu C_{ox}\left(\frac{W}{L}\right)\left(V_{C_i}-V_T\right)} \tag{11}$$

4. PSPICE simulation results

The CMOS implementation of the CDCC [53] shown in Fig. 7 using 0.18 μm TSMC process technology has been employed to verify the workability of the circuits designed in the previous section. The values of the DC bias currents and voltages were taken as 40 μA and ±2.5 V respectively. The aspect ratios of the various MOSFETs have been taken as given in Table 3 where the lengths of the MOSFETs have been taken as an integral multiple of 0.18 μm, as per the prevalent practice.

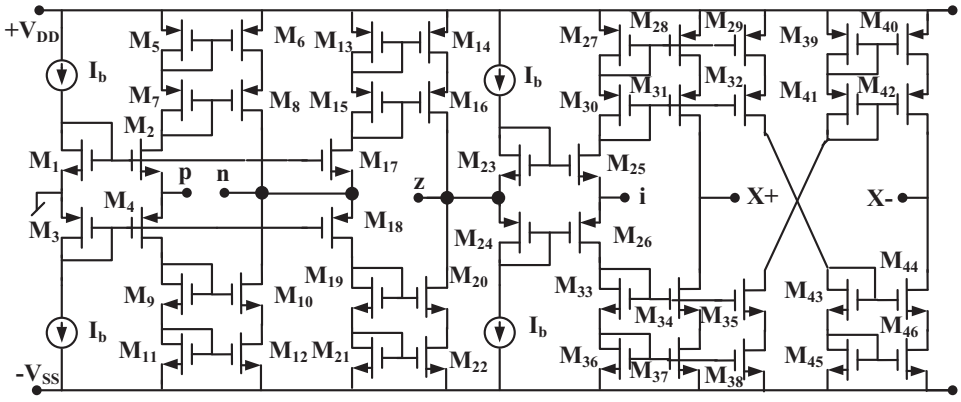


Fig. 7. CMOS implementation of the CDCC [53].

Table 3
Aspect ratios of the various MOSFETs used in CDCC realization.

MOSFETs	W/L (μm/μm)
M_1, M_2, M_{17}, M_{23}, M_{25}	36/0.36
M_3, M_4, M_{18}, M_{24}, M_{26}	72/0.36
M_5–M_{16}, M_{19}–M_{22}, M_{27}–M_{46}	3.6/0.36

Table 4
The SPICE-measured values of the various parasitics of the CMOS CDCC.

S. No.	Parameter	Value
1	R_p	604 Ω
2	R_n	604 Ω
3	R_z	10.898 MΩ
4	C_z	9.02836×10^{-14} F
5	R_i	604 Ω
6	R_{x+}	11.087 MΩ
7	C_{x+}	1.0572×10^{-14} F
8	R_{x-}	10.962 MΩ
9	C_{x-}	1.0563×10^{-14} F

R_p and R_n represent the parasitic input resistances of the p-port and n-port respectively whereas R_z, C_z represent the output resistance and output capacitance looking into the z-terminal of the CDCC. R_i represents the output resistance of the voltage buffer of the MO-CCII (resistance looking into the i terminal). On the other hand, R_{x+} and C_{x+} represent output resistance and output capacitance looking into the x+ terminals of the CDCC and finally, R_{x-} and C_{x-} represent the output resistance and the output capacitance looking into the 'x-' terminal of the CDCC. The measured values of the various parasitics of the CDCC, at 40 μA DC bias current and ±2.5 V DC bias voltage, are found to be as shown in Table 4.

We now present some SPICE simulation results to demonstrate the workability of the designed circuit of Fig. 5.

4.1. The frequency response and the transient response of the fully-differential CM fifth order lowpass Butterworth filter

The filter was designed for a cut-off frequency of 2.0 MHz by appropriately selecting the passive resistors and capacitors as:

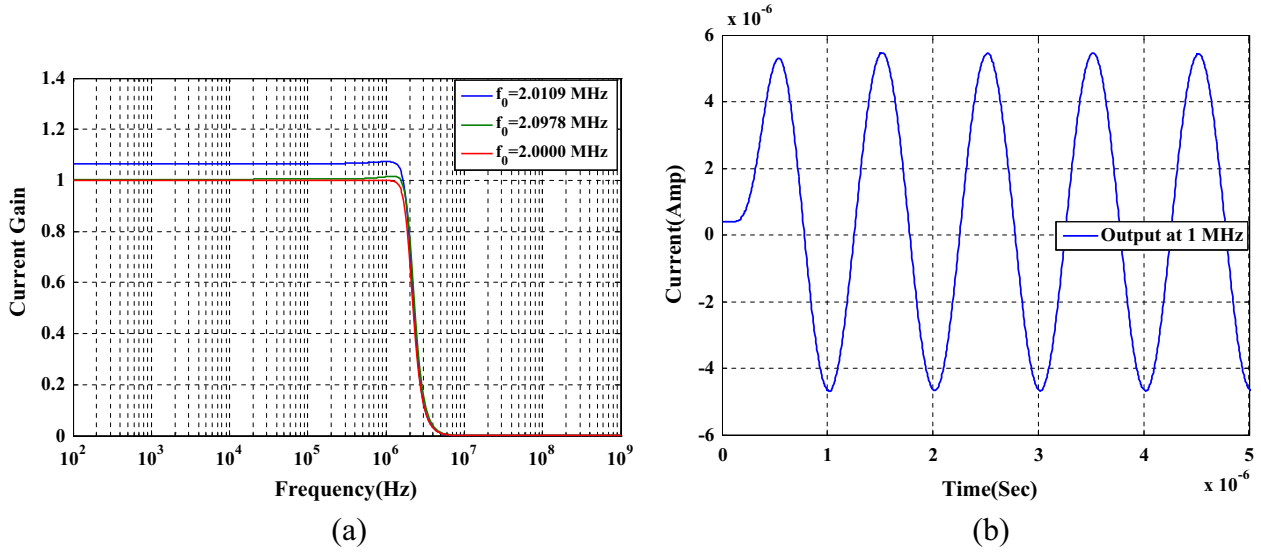


Fig. 8. PSPICE simulation results of the fully-differential current-mode fifth order lowpass Butterworth Filter (a) Frequency response (i)——Normal (ii)——Using pre-distorted resistor values at ports 'i' (iii) ———Ideal (obtained using MATLAB) (b) Transient response.

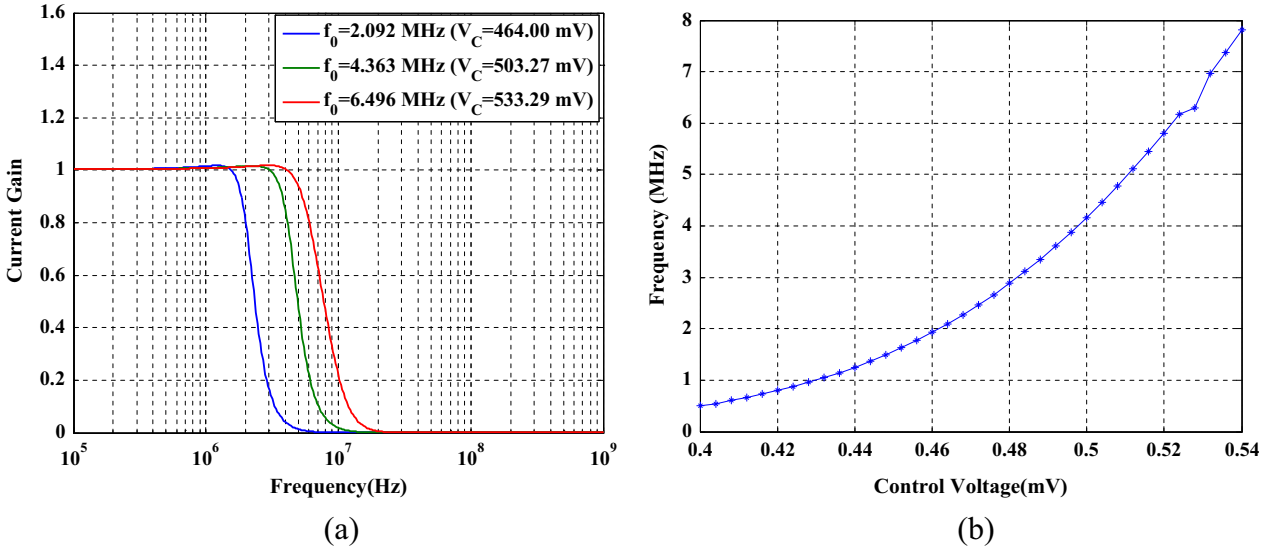
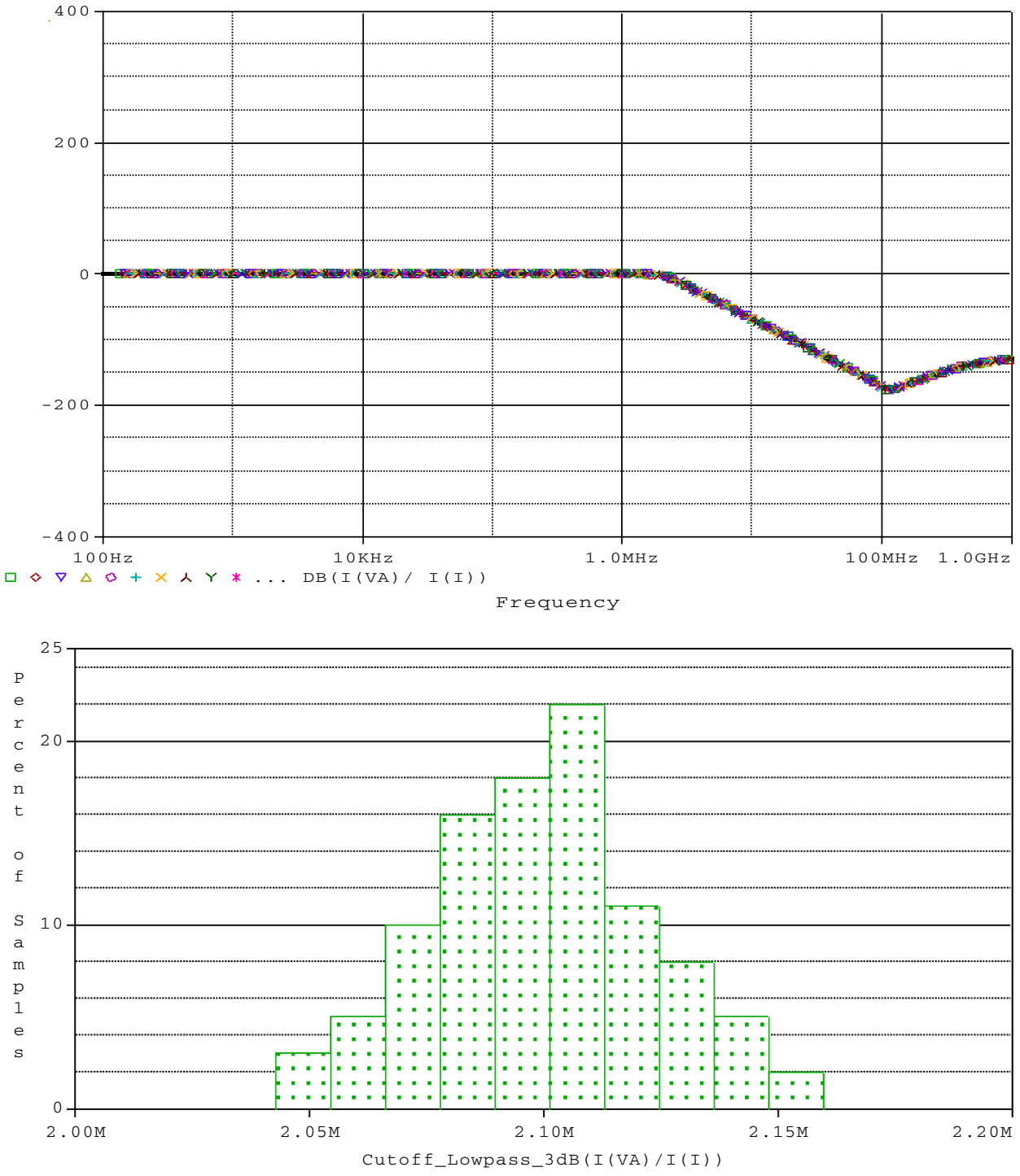


Fig. 9. PSPICE simulation results (a) Tunability of cut-off frequency with Control Voltage and (b) Variation of the cut-off frequency with control voltage V_c.



n samples	= 100	10th %ile	= 2.06943e+006
n divisions	= 10	median	= 2.10022e+006
mean	= 2.09964e+006	90th %ile	= 2.13341e+006
sigma	= 23959.4	maximum	= 2.15974e+006
minimum	= 2.04288e+006	3*sigma	= 71878.2

Fig. 10. Results of Monte Carlo analysis for fully-differential current-mode fifth order low pass Butterworth filter.

R_{x5} = 5 KΩ, R_{y5} = 10 KΩ, R_{x4} = 16.18 KΩ, R_{y4} = 10 KΩ, R_{x3} = 26.18 KΩ, R_{y3} = 10 KΩ, R_{x2} = 26.18 KΩ, R_{y2} = 10 KΩ, R_{x1} = 16.18 KΩ, R_{y1} = 10 KΩ, $R_1 = R_2 = R_3 = R_4 = R_5 = R$ = 10 KΩ and $C_1 = C_2 = C_3 = C_4 = C_5$ = 15.92 pF. From Table 4 it is revealed that the parasitic capacitances are generally very small and their effect on the circuit performance can be minimised by taking the external capacitors much larger than them, however, the parasitic input resistances at the ports **p**, **n** and **i** are about 0.604 KΩ and cannot be ignored. Hence, they

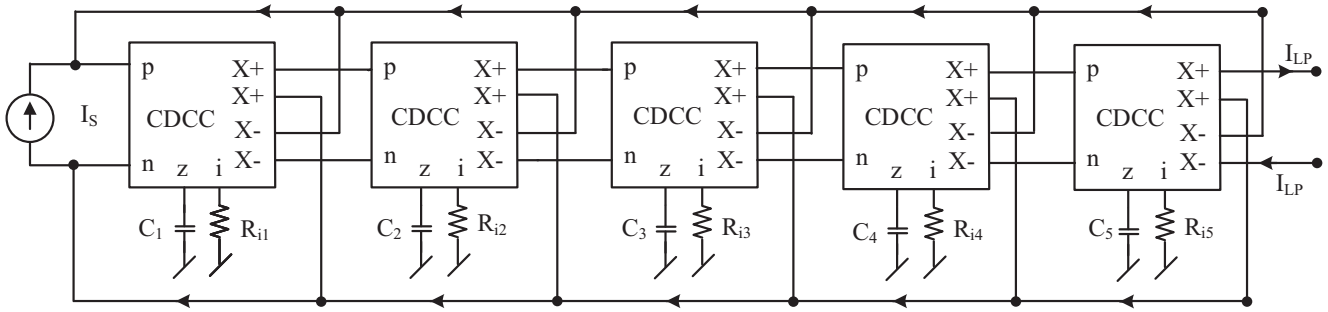


Fig. 11. Fifth order fully-differential CM lowpass filter with reduced-component-count.

must be absorbed in the external resistors to compensate for their adverse effect for which all the resistances terminated at 'i' ports have been *pre-distorted* by subtracting 0.604 KΩ from their design values. The new values of the resistors and capacitors, after accounting these parasitics are: R_{x5} = 5 KΩ, R_{y5} = 9.396 KΩ, R_{x4} = 16.18 KΩ, R_{y4} = 9.396 KΩ, R_{x3} = 26.18 KΩ, R_{y3} = 9.396 KΩ, R_{x2} = 26.18 KΩ, R_{y2} = 9.396 KΩ, R_{x1} = 16.18 KΩ, R_{y1} = 9.396 KΩ, $R_1 = R_2 = R_3 = R_4 = R_5 = R$ = 9.396 KΩ and $C_1 = C_2 = C_3 = C_4 = C_5$ = 15.92 pF. The frequency responses of the normal design and the one using *pre-distorted* values of all the resistors at port **i** of the CDCCs, both obtained from SPICE simulations, have been plotted against the ideal response (obtained through MATLAB) in Fig. 8 (a) whereas the transient response of the designed filter, with an input current of 5.0 μA amplitude at 1.0 MHz, is shown in Fig. 8(b).

The results of Fig. 8 confirm the validity of the theory.

4.2. Electronic-tunability

From Eq. (9), it is observed that the cut-off frequency of the filter can be varied by simultaneously changing the time constants of *all* the integrators i.e. by varying all R_i while keeping the values of all the capacitors of the integrators and the resistors in the scalar-multipliers *unchanged.* As an example, it has been found that to vary the cut-off frequencies as 2.0 MHz ,4.0 MHz and 6.0 MHz we must choose R_i = 10 KΩ, 5 KΩ and 3.332 KΩ. After considering the parasitics at the 'i' ports, choosing the control voltages as $V_C = V_{Ci} = -V_{Ci}$ = 464.00 mV, 503.27 mV and 533.29 mV respectively, it has been found that VCRs realize equivalent resistance values as 9.396 KΩ, 4.396 KΩ and 2.728 KΩ respectively which, along with the intrinsic parasitic resistance of 0.604 KΩ, become *approximately equal to* 10 KΩ, 5 KΩ and 3.332 KΩ respectively, as required. Fig. 9(a) shows the frequency responses for different values of the control voltage V_c while Fig. 9(b) shows the variation of the cut-off frequency with different values of the control voltage V_c.

4.3. Monte-Carlo analysis

To study the effect of mismatches in the component values in the designed fifth order Butterworth filter of Fig. 5, Monte Carlo simulations have been carried out by allocating 1% tolerances to the component values (capacitors C = 15.92 pF) for all the five grounded capacitors and performing 100 runs. The results for the 1% tolerance have been shown in Fig. 10. The value of the cut-off frequency obtained from the simulations was found to be 2.0978 MHz. Monte Carlo analysis shows the median value of cut-off frequency as f_0 = 2.1002 MHz, which indicates that the mismatch in the component values do not have large effect on the realized cut-off frequency.

4.4. Reduced-Component version

In the structure of Fig. 5, in all the integrators we have employed all equal-valued capacitors (as desirable for IC fabrication) and all equal-valued resistors (which facilitate simultaneous variation of all of them when they are replaced by identical CMOS-VCRs driven by a common control voltage). In view of this, it was necessary to employ scalar-multipliers along with each integrator to accommodate the required coefficients of the denominator polynomial of the filter transfer function. However, if all the scalar-multipliers are dispensed with, then a reduced-component-count version is possible which is shown in Fig. 11. For the same cut-off frequency i.e. 2.0 MHz, the component values for this version have also been calculated according to the same fifth order Butterworth transfer function along with pre-distorted values of resistances (as explained earlier) and are given as: $C_1 = C_2 = C_3 = C_4 = C_5 = C$ = 9.84 pF; R_{i1} = 4.396 KΩ, R_{i2} = 9.396 KΩ, R_{i3} = 15.576 KΩ, R_{i4} = 25.576 KΩ and R_{i5} = 51.756 KΩ. A SPICE check has indicated that this circuit too works well but in this reduced-component design, the electronic-tunability feature is sacrificed.

5. Concluding remarks

In this paper, we have presented a methodology for the design of an nth order fully-differential current-mode higher order filter using CDCCs as active elements. The methodology is general and results in filter configurations which employ *all grounded passive elements.* An illustrative example of a fifth order Butterworth filter design has been presented whose workability has been substantiated using SPICE simulations based upon a CMOS CDCC using 0.18 μm TSMC technology process parameters. The proposed methodology of designing CDCC-based fully-differential higher order ($n \geq 3$) CM filter achieves the following three advantageous features simultaneously which have not been achieved simultaneously in any of the earlier works:

(i) use of all grounded passive elements
(ii) employment of only one capacitor per pole, and
(iii) facilitation of electronic-tunability of the cut-off frequency.

A reduced-component-version of the designed fifth order Butterworth filter has also been presented which too employs all grounded RC components but does not have electronic tunability.

Lastly, it may be mentioned that although *multifunction capability* has been demonstrated in a class of higher order filters in some earlier works such as that in [17,21,22], the filters presented therein have single-ended input and single-ended output. From the review of previously known fully-differential higher order filters it is revealed that to the best of authors' knowledge, multifunction capability has not been explored in the realization of fully-differential structures so far. This appears to be interesting for further investigations.

Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.aeue.2018.10.009.

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Current-mode Quadrature Oscillator Using CFCC

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Abstract In this communication, a Current Follower Current Conveyor (CFCC)-based quadrature oscillator circuit has been proposed which employs a resonator-negative resistor configuration and provides oscillations in quadrature from two high impedance current output terminals of the CFCCs. The workability of the quadrature oscillator has been verified using PSPICE simulations using a CMOS CFCC implementable in 0.18 micron TSMC technology.

Keywords: *current follower, current conveyor, current-follower-current-conveyor, quadrature oscillator, current-mode oscillator, current- mode circuits*

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1. Introduction

A quadrature sinusoidal oscillator (QSO) circuit provides two sinusoids with 90^0 phase difference and finds several applications in communication and measurement systems. In communication systems they are used in quadrature mixers, single-sideband generators and direct-conversion receivers while in measurement systems such oscillators are used in vector generators or selective voltmeters (see [1] and references cited therein).

During the last two decades, many new active building blocks have been proposed in the domain of analog signal processing, a comprehensive review of which was presented in [2], wherein several new active building blocks (ABB) were also proposed. Many of the new ABBs proposed in [2] have been employed in the past to realize QSOs and other signal processing applications, which include Current Differencing Buffered Amplifier (CDBA) [3,4], Voltage Differencing Buffered Amplifier (VDBA) [5], Voltage Differencing Transconductance Amplifier (VDTA) [6], Voltage Differencing current conveyor (VDCC) [7], Current Differencing Transconductance Amplifier (CDTA) [8-12], Multiple-Output Current Controlled Current Differencing Transconductance Amplifier (MO-CCCDTA) [13], Modified Current Differencing Transconductance Amplifier (MCDTA) [14], Current Follower Transconductance Amplifier (CFTA) [15], Z-copy Current Follower Transconductance Amplifier (ZC-CFTA) [16], Second-Generation Current Conveyor Transconductance Amplifier (CCII-TA) [17], Differential-Input Buffered and Transconductance Amplifier (DBTA) [18], Current-Feedback Operational Amplifier (CFOA) [19], Differential Voltage Current Conveyor (DVCC) [20], Differential Voltage Current-Controlled Conveyor Transconductance Amplifier (DVCCCTA) [21], Voltage Differencing Inverting Voltage Buffered Amplifier (VDIBA) [22], Voltage Differencing-Differential Input Buffered Amplifiers (VD-DIBA) [23,24] and Programmable Current Amplifier [25].

It may be mentioned that while the QSOs presented in [3,4,5,7,16-24] operate in voltage mode (VM), those presented in [6,8-17,21,25] operate in current mode (CM). Also, of the various QSO circuits quoted above, only the circuits presented in [3,4] and [12] offer fully-decoupled condition of oscillation and frequency of oscillation. Furthermore, out of [3,4] and [12], the QSOs described in [3,4] are VM oscillators while the QSO described in [12] is a CM oscillator.

It has been observed from the literature survey that a new building block named Multi-output Current Follower Current Conveyor (MO-CFCC) which was also proposed in [2] has not been utilized for the realization of QSOs so far while recently its applications in the realization of simulated impedances have been reported in [26,27]. In this letter, we propose a QSO realized with CFCC to fill this void. The workability of the proposed oscillator has been verified using PSPICE simulations in 0.18 micron TSMC technology.

2. CFCC-based Realization of the Current-mode Quadrature Oscillator

CFCC [2] is a five-terminal ABB with the following functionalities: the current at the z terminal is an inverted copy of the input current at 'p' terminal; the terminal 'i' tracks the potential at the terminal z and two complementary currents at the output terminals are available which are copies of the current at the 'i' terminal. To provide

additional functionality to the CFCC, a copy of the current at the 'z' terminal may also be provided resulting in the Z-copy CFCC (ZC-CFCC). The symbolic representation and relations between the various port variables for this ABB are shown in Figure 1, and equation (1) respectively.

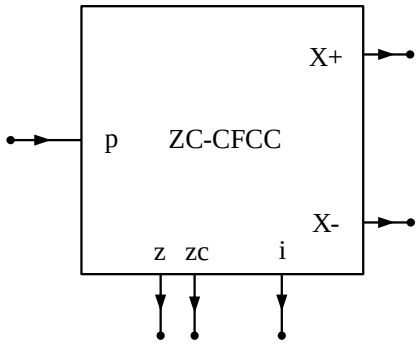

Figure 1. Symbolic notation of the ZC-CFCC

$$\begin{bmatrix} V_p \\ I_z \\ V_i \\ I_{x+} \\ I_{x-} \\ I_{zc} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ V_z \\ I_i \\ V_{x+} \\ V_{x-} \\ V_{zc} \end{bmatrix}. \quad (1)$$

The proposed current-mode quadrature oscillator circuit using CFCCs is shown in Figure 2 which consists of a parallel RLC resonator made from the CFCC along with R_4, R_5, C_1 and C_2 and a NIC-simulated negative resistor realized by the ZC-CFCC along with the resistors R_1, R_2 and R_3.

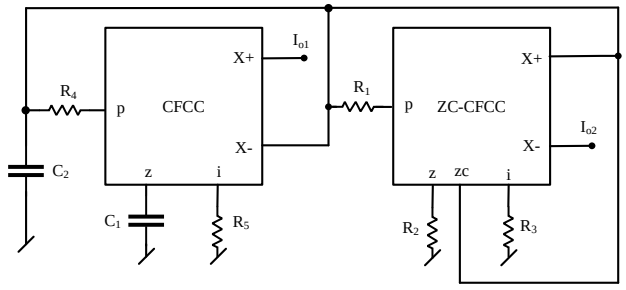

Figure 2. The proposed CFCC-based current mode quadrature oscillator

A straight forward routine analysis of the circuit given in Figure 2 yields the following characteristic equation (CE):

$$s^2 R_1 R_3 R_4 R_5 C_1 C_2 + sR_5 C_1 \left(R_1 R_3 - R_2 R_4\right) + R_1 R_3 = 0. \quad (2)$$

From equation (2), the condition of oscillation (CO) and frequency of oscillation (FO) are found to be:

CO:

$$R_1 R_3 = R_2 R_4. \quad (3)$$

FO:

$$\omega_{osc} = \frac{1}{\sqrt{R_4 R_5 C_1 C_2}} \quad (4)$$

However, for quadrature oscillator design, we must look into the interrelationship between I_{01} and I_{02} which is found to be

$$\frac{I_{01}}{I_{02}} = -\frac{R_1 R_3}{sR_2 R_4 R_5 C_1}. \quad (5)$$

Under sinusoidal steady state, equation (5) reduces to

$$\frac{I_{01}}{I_{02}} = \frac{j}{\omega_0 R_5 C_1}. \quad (6)$$

The phase difference φ is, thus, equal to 90^o.

3. Non-ideal Considerations

For a non-ideal analysis of the proposed oscillator, we have considered the various parasitic resistances and capacitances associated with the different terminals of the CFCC as follows: R_p represents the parasitic input resistance of the **p** port whereas R_z, C_z represent the resistance and capacitance at the z-terminal of the CFCC; similarly, R_{zc} and C_{zc} represent resistance and capacitance at the **zc** terminal while R_i represents the output resistance of the voltage buffer of the MO-CCII (resistance looking into the i terminal); on the other hand, R_{x+} and C_{x+} represent output resistance and output capacitance at the x+ terminals of the CFCC and finally, R_{x-} and C_{x-} represent the output resistance and the output capacitance at the x-terminals of the CFCC. A straight forward analysis of the proposed oscillator, incorporating all the parasitic immittances described above, gives the following third order characteristic equation:

$$\begin{aligned} & s^3 R_a R_b R_c R_d R_e R_f R_z C_a C_b C_z \\ & + s^2 (R_a R_c R_d R_e R_f R_z C_a C_b + \\ & R_a R_b R_c R_e R_f R_z C_a C_z + R_a R_b R_c R_d R_e R_z C_a C_z \\ & + R_a R_b R_c R_d R_e R_f C_b C_z) \\ & + s(R_a R_c R_e R_f R_z C_a + R_a R_c R_d R_e R_z C_a \\ & + R_a R_c R_d R_e R_f C_b + R_a R_b R_c R_f R_z C_z \\ & + R_a R_b R_c R_e R_f C_z + R_a R_b R_c R_d R_e C_z \\ & - R_b R_d R_e R_f R_z C_a) + R_a R_c R_f R_z \\ & + R_a R_c R_e R_f + R_a R_c R_d R_e - R_b R_d R_e R_f = 0 \end{aligned} \quad (7)$$

where

$$\begin{aligned} & R_a = R_1 + R_p,\ R_b = R_2 \parallel R_z, \\ & R_c = R_3 + R_i,\ R_d = R_4 + R_p, \\ & R_e = R_5 + R_i,\ R_f = R_{x+} \parallel R_{x-} \parallel R_{zc}, \\ & C_a = C_1 + C_z \text{ and } C_b = C_2 + C_{zc} + C_{x+} + C_{x-}. \end{aligned}$$

We have measured the values of the various parasitic resistances and capacitances of the CFCC employed in the present work (see Figure 3) by carrying out detailed PSPICE simulations. The measured values of these non ideal parameters are found to be as summarized in Table 1.

Table 1. The SPICE-measured values of the various parasitics of the CMOS ZC-CFCC

S.No.	Parameter	Value
1	**R_p**	**591Ω**
2	**R_i**	**591Ω**
3	**R_z**	**4.9178 M Ω**
4	**C_z**	**6.2988x10^{-14}F**
5	**R_{zc}**	**4.9178 M Ω**
6	**C_{zc}**	**7.3938x10^{-15}F**
7	**R_{x+}**	**4.9862 MΩ**
8	**C_{x+}**	**7.3954x10^{-15}F**
9	**R_{x-}**	**4.7752 MΩ**
10	**C_{x-}**	**7.4062x10^{-15}F**

The following approximations (ensured by selecting appropriate values of the terminating resistances and capacitances) R_1 , R_2, R_3 ,R_4 ,R_5, << R_f and C_1, C_2>>C_{x+}, C_{x-}, C_z and C_{zc} lead to a second order approximation of the CE from which the non-ideal CO and FO are now given by

CO:

$$(R_1 + R_p)(R_3 + R_i) = (R_2 \parallel R_z)(R_4 + R_p) \tag{8}$$

FO:

$$\omega_{osc}^{'} = \omega_{osc} \frac{1}{\sqrt{\left[\left(1+\frac{R_p}{R_4}\right)\left(1+\frac{R_i}{R_5}\right)\left(1+\frac{C_z}{C_1}\right)\times\left(1+\frac{(C_{zc}+C_{x+}+C_{x-})}{C_2}\right)\right]}}. \tag{9}$$

The interrelationship between I_{01} and I_{02} is found to be

$$\begin{aligned}\frac{I_{01}}{I_{02}} &= -\frac{R_z(1+sR_bC_z)}{R_e(1+sR_zC_a)} \\ &= -\frac{R_z[1+s(R_2 \parallel R_z)C_z]}{(R_5+R_i)[1+sR_z(C_1+C_z)]}.\end{aligned} \tag{10}$$

The non-ideal expression of the phase difference φ is given by

$$\begin{aligned}\varphi &= \tan^{-1}\omega_{osc}^{'}R_zC_a - \tan^{-1}\omega_{osc}^{'}R_bC_z \\ &= \tan^{-1}R_z\sqrt{\frac{(C_1+C_z)}{\left[\begin{matrix}(C_2+C_{zc}+C_{x+}+C_{x-})\\ \times(R_1+R_p)(R_5+R_i)\end{matrix}\right]}} \\ &\quad -\tan^{-1}\frac{(R_2 \parallel R_z)C_z}{\sqrt{\left[\begin{matrix}(R_1+R_p)(R_5+R_i)(C_1+C_z)\\ \times(C_2+C_{zc}+C_{x+}+C_{x-})\end{matrix}\right]}}.\end{aligned} \tag{11}$$

Subject to the approximations used in the non-ideal analysis, it may be observed that the phase difference between the two output currents would be very close to 90^o (as the angle corresponding to the argument of the first arctangent term will be close to ninety degree because of the very large value of R_z while the angle corresponding to the argument of the second arctangent term will be very small because of the very small value of C_z). We have calculated the phase difference using the values of different parasitic resistances and capacitances given in Table 1 as per equation (11) and found it to be equal to 89.52^o for a design frequency of 1.59 MHz.

4. PSPICE Simulation Results

We now present some SPICE simulation results to demonstrate the workability of the proposed structure. The CMOS implementation of the CFCC [27] shown in Fig. 3 using 0.18 micron TSMC process technology has been used to verify the workability of the circuit presented in this paper. The values of the DC bias currents and voltages were taken as 40 µA and ± 2.5V respectively. The oscillator was designed for a frequency of 1.59 MHz by appropriately selecting the passive components as follows: C_1= C_2=10 pF, R_1=10 kΩ, R_2=10700 Ω, R_3=10 kΩ, R_4=10 kΩ, R_5=10 kΩ. From SPICE simulations the oscillation frequency was found to be 1.50 MHz. The output waveforms are shown in Figure 4(a). The quadrature relationship of the generated waveform is indicated by the Lissajous pattern shown in Figure 4(b). The measured phase difference was found to be 90.91^o. Figure 5 shows the FFT of the generated waveforms. Total harmonic distortion (THD) for current output I_{01} was found to be 3.2 % and for the current output I_{02} as 5.3 %. These simulation results thus, prove the workability of the proposed circuit.

5. Concluding Remarks

In this letter, a recently proposed active building block, namely, the CFCC has been used to devise a current-mode QSO. The workability of the circuit has been substantiated by SPICE simulations based on a CMOS CFCC implementable in 0.18 µm CMOS technology. The letter has, thus, added a new application of the CFCC in the area of quadrature oscillator realization, whose applications explored and known so far were only in the realization of the simulated impedances of various kinds [26,27].

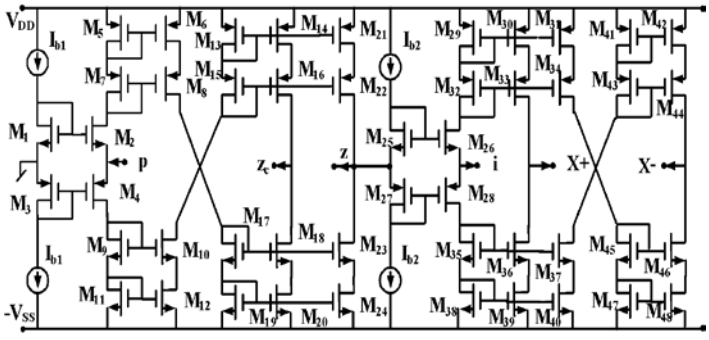

Figure 3. An exemplary CMOS implementation of the ZC-CFCC [26]

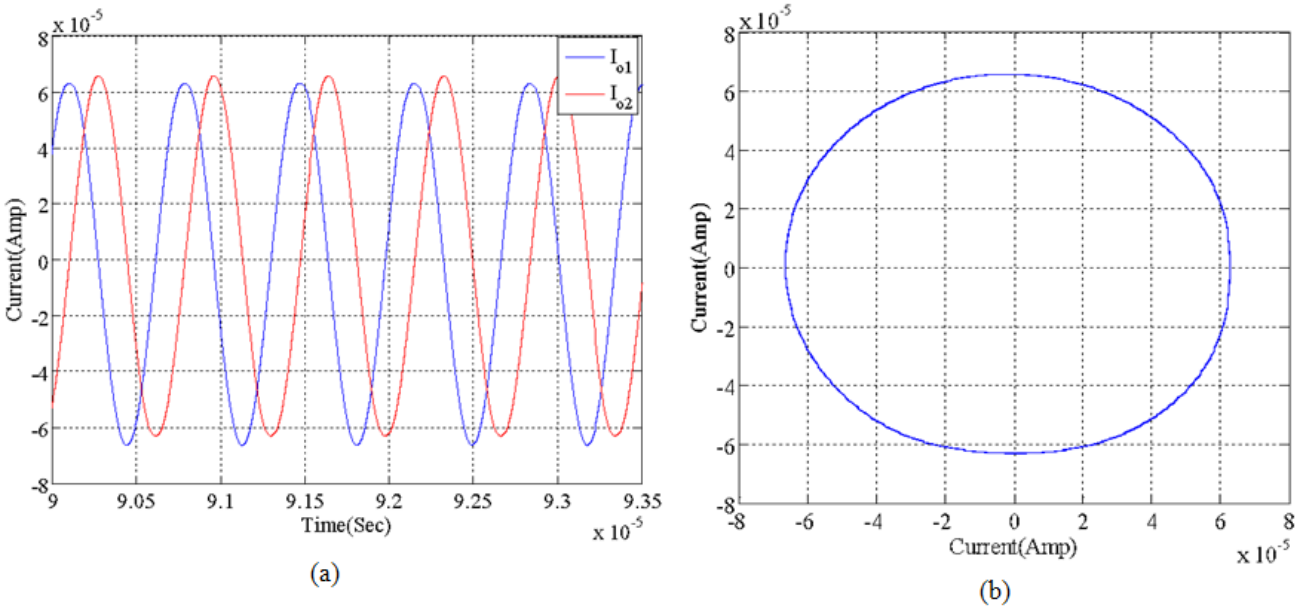

Figure 4. PSPICE Simulation Results (a) Quadrature oscillator waveforms (b) Lissajous pattern

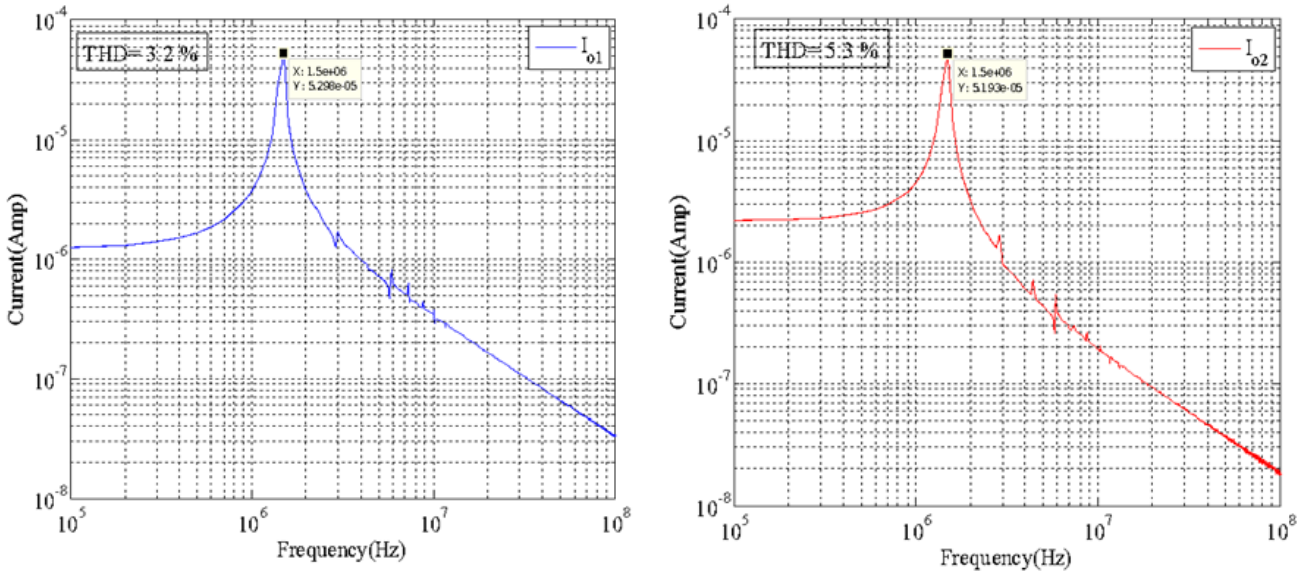

Figure 5. FFT of the waveforms of $I_{o1}$and I_{o2} at 1.50 MHz

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Biography

Alok Kumar Singh received B.Sc. from University of Allahabad in 1984 and B. Tech. (Electronics and Telecommunication Engineering) and M.Tech. (Electronics) from J.K. Institute of Applied Physics, University of Allahabad in 1987 and 1991 respectively. He served BHPV Ltd. (a Government of India undertaking) in various capacities from 1991 to 1998. He worked in Ambedkar Polytechnic/Institute (under Directorate of Training and Technical Education) from 1998 to 2004.In 2004, he joined as a Lecturer in the Department of Electronics and Communication Engineering, Delhi Technological University (Formerly Delhi college of Engineering), Delhi. Currently, he is working as Associate Professor in the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi. His areas of interest are VLSI Design, Analog Devices, Analog Integrated Circuits and Signal Processing.