An application of DTMOS based OpAmp

DISSERTATION

Submitted in fulfillment of the requirement for the award of the degree
Of
Master of Technology
In
VLSI DESIGN
By
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Under the Guidance of
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY

CERTIFICATE

This is to undertake that the work presented in this M. Tech. Dissertation titled **"An application of DTMOS based OpAmp"** is an authentic record of my own work carried out during the period from January 2017 to June 2017 under the supervision of **Mr. A.K. Singh, Associate Professor,** Department of Electronics & Communication Engineering. It is submitted in fulfilment of the requirements for the award of the **Master of Technology in VLSI Design** at Department of Electronics & Communication Engineering, Delhi Technological University. The matter presented in this project has not been submitted by me for the award of any other degree elsewhere.

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This is to certify that the above statement made by the candidate is correct to the best of my knowledge and can be awarded required marks.

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I wish to convey my sincere gratitude to all the faculty members of Electronics & Communication Engineering Department, who have enlightened me during my studies related to this project.

I would also like to thank my parents and my friends for their tremendous contributions and support morally towards the completion of this project

ABSTRACT

A bandgap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits. BGR is a basic design block of any analog circuit. The BGR generator circuit is designed to achieve the insensitive behaviour with respect to process, voltage and temperature (PVT) corners. The BGR supplies the reference voltage and the reference current to the analog design blocks such as a charge pump and a memory circuit. It commonly has an output voltage around 1.25V, close to the theoretical 1.22 eV bandgap of silicon at 0 K. This circuit concept was first published by David Hilbiber in 1964. An important part in the design of analog integrated circuits is to create reference voltages and currents with well defined values. To accomplish this on chip, so called bandgap reference circuits are commonly used. A typical application for this reference voltage is in analog to digital conversion, where the input voltage is compared to several reference levels in order to determine the corresponding digital value.

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ABBREVIATIONS

[1] **BGR** : Bandgap reference circuit

[2] **CMOS** : Complementary metal oxide semi-conductor

[3] **CTAT** : Complementary to absolute temperature voltage

[4] **NTC** : Negative temperature coefficient

[5] **PTC** : Positive temperature coefficient

[6] **PTAT**: Proportional to absolute temperature

[7] **MOSFET**: Metal oxide semiconductor field effect transistor

[8] **OPAMP** : Operational amplifier

[9] **CS :** Common source

CHAPTER 1

INTRODUCTION

Voltage reference design is a well-researched area of analog design. All data converters require an accurate, reliable reference voltage for proper conversion. A faulty reference voltage can have devastating effects on data conversion and ultimately the entire system. Temperature-insensitive bandgap voltage references have been a staple of analog and mixed signal system design.

Simply put, a device which produces a constant voltage irrespective of the variations in the device it is baising is called a constant voltage reference device. A wide variety of voltage references find application in power supplies, analog-to-digital converters, digital-to-analog converters, and other measurement and control systems. Voltage references vary widely in performance; a regulator for a computer power supply may only hold its value to within a few per cent of the nominal value, whereas laboratory voltage standards have precisions and stability measured in parts per million. The Clark cell and Weston cell are the earliest voltage references or standards, which are still used in some laboratory and calibration application.

Precision voltage reference circuits are important for accurate working of mixed and analog integrated circuits such as oscillators, PLLs, Data Converters and Dynamic Random Access Memories (DRAM's). These voltage references should be insensitive to variations in process, temperature and supply voltage. The performance of many mixed analog/digital systems is limited by inaccuracies and power supply noise coupling errors in integrated voltage references. So precision voltage reference circuits forms an integral part of almost all integrated circuit designs.

Desired characteristics of a voltage ref circuit are:

- Silicon implementable
- Stable and accurate
- Independent of output loading
- Insensitive to power supply variations (especially for battery operated devices)
- Insensitive to temperature

Most popular reference voltage generators are:

- Zener-based Voltage References
- Enhancement and depletion references

- Bandgap Voltage References

1.1 Zener Based Voltage References

Zener-based temperature compensated voltage reference circuits were popular few years back. These devices have breakdown voltages greater than 6V, putting a lower limit on the supply voltage requirements. So mainly because of the power supply requirements zener-based voltage references are no more popular in the latest integrated circuits.

1.2 Enhancement and Depletion References

The magnitude of the reference voltage is determined by the sum of the absolute values of the threshold voltage of the enhancement mode and the depletion mode MOSFET. Ref circuits that are based on the absolute value of a ref voltage cannot be controlled accurately because they results in high temperature sensitivity. The variation of the ref voltage w.r.t the temperature arises from the temperature dependence of

(a) the threshold voltage difference
(b) the drain bias current
(c) the mobility

1.3 Bandgap Voltage Reference

Bandgap voltage reference circuit uses the negative temperature coefficient of emitter base voltage in conjunction with the positive temperature coefficient of emitter-base voltage differential of two transistors operating at different current densities to make a zero temperature coefficient reference. Bandgap reference circuits gained popularity for the reasons discussed below .

1.4 Advantages of Bandgap Reference circuit

- The base-emitter voltage of a bipolar transistor is most predictable and well understood parameter
- Temperature insensitive
- Can operate at low supply voltages
- Capable of producing “arbitrary” output voltages
- Circuit can be easily incorporated in a monolithic IC design

1.5 Applications of Voltage Reference Circuit

- They serve as a biasing circuit to be employed in any type of analog or mixed type circuit.
- Voltage Regulators
- Data Converters
- Oscillators, PLL's
- Dynamic Random Access memories (DRAM's)

1.6 Basic terms used in the work

A brief explanation of frequently used terms in this document are given here-

1.6.1 Bandgap Voltage

Bandgap voltage refers to the voltage difference between the valence band and conduction band of the semiconductor material, which has a constant value and its variation with temperature, is significantly less.

1.6.2 PTAT Voltage

PTAT stands for Proportional to Absolute Temperature Voltage, meaning the variations in voltage is proportional to temperature, or voltage increases with temperature.

1.6.3 CTAT Voltage

CTAT stands for Complementary to Absolute Temperature Voltage, meaning the variations in voltage is complementary to temperature, or voltage decreases with increase in temperature.

1.6.4 Bandgap Reference Circuit (BGR)

BGR is a precision voltage reference circuit, in which the negative temperature dependency of a voltage source is cancelled by the positive voltage dependency of another voltage source, resulting in a stable voltage at the reference temperature which is equal to the bandgap voltage of the semiconductor at the reference temperature.

1.6.5 V_{BE}

It is the potential drop across a forward biased diode connected bipolar junction transistor (BJT).

1.7 Work Flow

This work is based on the comprehensive study of Bandgap Reference Circuits.

- Conventional Bandgap Reference Circuit has been designed producing a reference voltage of around 1.2V.
- The BGR circuits used in this work use a two stage Operational Amplifier.
- Finally a BGR circuit is proposed which can be used to produce reference voltage with less power dissipation using DTMOS based operational amplifier

CHAPTER 2

BANDGAP REFERENCE CIRCUIT

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Bob Widlar designed the first bandgap voltage reference in the 1970s, which was used in LM309 5-volt regulator IC from National Semiconductor. It needed only three terminals which made it inexpensive and easy to use.

2.1 PRINCIPLE

The basic principle of BGR is to add a voltage that has PTC to one that has NTC. If the two coefficients have equal value but opposite signs, the cumulative effect come out to be temperature independent as shown in the Figure 2.1. The equation of reference voltage is

$$V_{REF}(T) = K.V_{PTAT}(T) + V_{CTAT}(T) \quad (2.1)$$

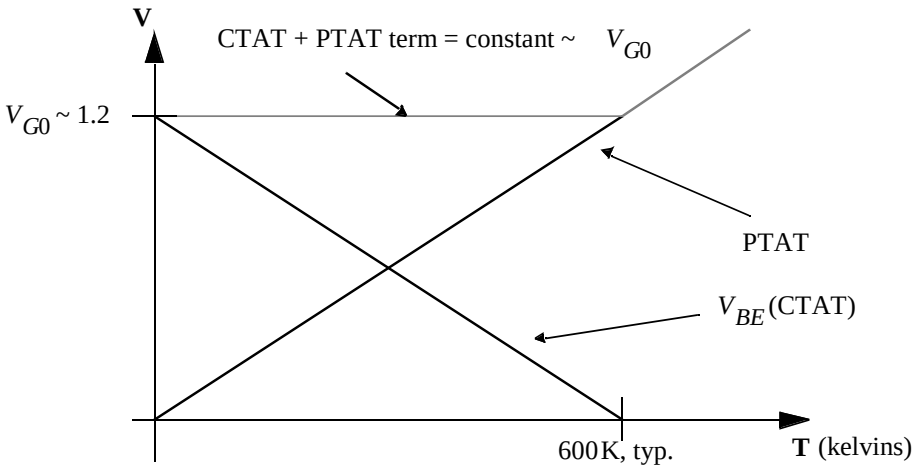

Figure 2.1: Principle of PTAT and CTAT

A plot of V_{BE} wrt temperature is shown in Figure 2.2.

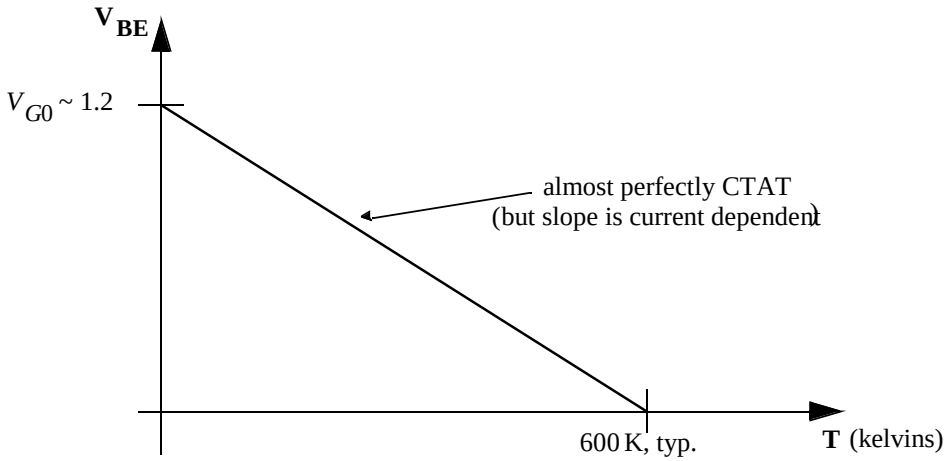

Figure 2.2: Plot of Base-emitter Voltage Vs Temperature

The pn junction voltage (V_{BE}) decreases (≈ -2mV/ ^{0}C) almost linearly with temperature making it CTAT.As shown in Figure 2.3 we can observe how the PTAT and CTAT circuits when used in conjunction to each other provide a constant biasing output voltage.

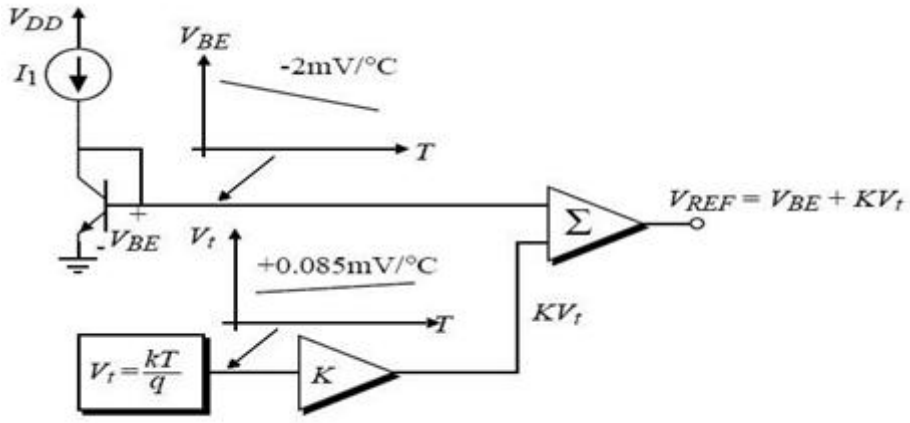

Figure 2.3: Reference voltage using PTAT and CTAT

2.2 DESIGN OF BANDGAP REFERENCE CIRCUIT

In order to produce a constant reference voltage, a PTAT voltage must be added to a CTAT voltage, both having equal magnitude.

CTAT

2.2.1 ANALYSIS :

Starting with the density of collector current for forward biased V_{BE} of a transistor:

$$J_C = \frac{q\overline{D_n}n_{p_o}}{W_B}\exp\left(\frac{V_{BE}}{V_t}\right) \quad (2.2)$$

Where Jc = Ic/Area = collector current density

$\overline{D_n}$ = average diffusion constant for electron

W_B = base width

V_{BE} = base emitter voltage

$$V_t = \frac{kT}{q}$$

k = Boltzmann's Constant (1.38 X 10^{-23} J/˚K)

T = absolute temperature

$n_{p_o} = \frac{n_i^2}{N_A}$ = equilibrium concentration of electron in the base

$n_i^2 = DT^3\exp\left(\frac{-V_{Go}}{V_t}\right)$

D = Temperature independent constant

V_{Go} = Bandgap voltage of Silicon (1.205 V)

Combine the above relationship into one:

$$J_C = \frac{q\overline{D_n}}{N_A W_B}\mathrm{D}T^3\exp\left(\frac{V_{BE}-V_{Go}}{V_t}\right)$$

$$J_C = AT^{\gamma}\exp\left(\frac{V_{BE}-V_{Go}}{V_t}\right)$$

Where, γ = 3

The value of Jc at a reference temperature of T = To,

$$J_C = ATo^{\gamma}\exp\left[\frac{q}{kTo}(V_{BEo}-V_{Go})\right]$$

While the value of Jc at general temperature T is

$$J_C = AT^{\gamma}\exp\left[\frac{q}{kT}(V_{BE}-V_{Go})\right]$$

The ratio of Jc/Jco can be expressed as

$$\frac{J_C}{J_{CO}} = \left(\frac{T}{To}\right)^{\gamma} exp\left[\frac{q}{k}\left(\frac{V_{BE}-V_{Go}}{T}-\frac{V_{BEo}-V_{Go}}{To}\right)\right]$$

Or

$$\ln\left(\frac{J_C}{J_{CO}}\right) = \gamma\ln\left(\frac{T}{To}\right)+\frac{q}{kT}\left[V_{BE}-V_{Go}-\frac{T}{To}(V_{BEo}-V_{Go})\right]$$

Where V_{BEo} is the value of V_{BE} at T = To

Solving for V_{BE} from the above results gives

$$V_{BE}(T) = V_{Go}\left(1 - \frac{T}{To}\right) + V_{BEo}\left(\frac{T}{To}\right) + \frac{\gamma kT}{q}\ln\left(\frac{T}{To}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{CO}}\right) \quad (2.3)$$

This is the CTAT voltage.

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_{Go}}{\partial T}\left(1 - \frac{T}{To}\right) - \frac{V_{Go}}{To} + \frac{V_{BEo}}{To} + \frac{\gamma kT\,\partial \ln\left(\frac{To}{T}\right)}{q\,\partial T} + \ln\left(\frac{T}{To}\right)\frac{\partial\left(\frac{\gamma kT}{q}\right)}{\partial T} + \frac{kT}{q}\left(\frac{\partial \ln\left(\frac{J_C}{J_{CO}}\right)}{\partial T}\right) + \frac{k}{q}\ln\left(\frac{J_C}{J_{CO}}\right)$$

Assume that T = To which means Jc = Jco, since $\frac{\partial V_{Go}}{\partial T}$ = 0

Therefore,

$$\frac{\partial V_{BE}}{\partial T} = -\frac{V_{Go}}{To} + \frac{V_{BEo}}{To} + \frac{\gamma kT\,\partial \ln\left(\frac{To}{T}\right)}{q\,\partial T} + \frac{kT}{q}\left(\frac{\partial \ln\left(\frac{J_C}{J_{CO}}\right)}{\partial T}\right)$$

Note that,

$$\frac{\partial \ln\left(\frac{To}{T}\right)}{\partial T} = \frac{T}{To}\frac{\partial(T/To)}{\partial T} = \frac{T}{To}\left(\frac{-To}{T^2}\right) = \frac{-1}{T}$$

and

$$\frac{\partial \ln\left(\frac{J_C}{J_{CO}}\right)}{\partial T} = \frac{J_C}{J_{CO}}\frac{\partial\left(\frac{J_C}{J_{CO}}\right)}{\partial T} = \frac{J_{CO}}{J_C}\left(\frac{\alpha}{T}\frac{J_C}{J_{CO}}\right) = \frac{\alpha}{T}$$

Therefore, $\frac{\partial V_{BE}}{\partial T}$ $at\ T = To\ is$

$$\frac{\partial V_{BE}}{\partial T} = -\frac{V_{Go}}{To} + \frac{V_{BEo}}{To} - \frac{\gamma k}{q} + \frac{\alpha k}{q}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BEo} - V_{Go}}{To} + (\alpha - \gamma)\frac{k}{q} \quad (2.4)$$

Now, considering the typical values of α and γ as 1 and 3.2. If $V_{BEo} = 0.6$ V at room temperature then, substituting the values in equation 2.4, we get,

$$\frac{\partial V_{BE}}{\partial T} = \frac{0.6 - 1.205}{300} + (1 - 3.2)\frac{0.026}{300} = -1.826\ mV/°C$$

This shows V_{BE} is a CTAT voltage, i.e, it decreases with the increasing temperature with above derived rate.

PTAT

2.2.2 ANALYSIS :

Two identical pn junctions are considered with different current densities as shown in Figure 2.4.

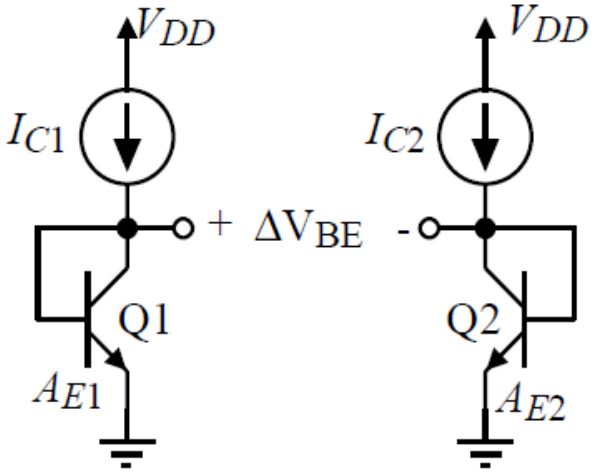

Figure 2.4: Generation of PTAT Voltage

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{2.5}$$

Substituting $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$ in equation 2.5, we get

$$\Delta V_{BE} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right)$$

$$\Delta V_{BE} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\frac{I_{S2}}{I_{C2}}\right) = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\right)$$

$$\Delta V_{BE} = V_T \ln\left(\frac{A_{E2}}{A_{E1}}\right)$$

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{A_{E2}}{A_{E1}}\right)$$

Differentiating ΔV_{BE} w.r.t. temperature results in

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{V_T}{T} \ln \frac{J_{C1}}{J_{C2}}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln \frac{J_{C1}}{J_{C2}}$$

2.2.3 DERIVATION OF THE GAIN 'K' OF THE BGR

For zero TC at Temp(T) = To, the following condition must hold true:

$$0 = \frac{\partial V_{BE}}{\partial T} + K'' \frac{\partial \Delta V_{BE}}{\partial T}$$

$$0 = K'' \left(\frac{V_{To}}{To}\right) \ln \frac{J_{C1}}{J_{C2}} + \frac{V_{BEo} - V_{Go}}{To} + (\alpha - \gamma) \frac{V_{To}}{To}$$

Define $K = K'' \ln \frac{J_{C1}}{J_{C2}}$ therefore,

$$0 = K \left(\frac{V_{To}}{To}\right) + \frac{V_{BEo} - V_{Go}}{To} + (\alpha - \gamma) \frac{V_{To}}{To}$$

Solving for K gives

$$K = \frac{V_{Go} - V_{BEo} - V_{To}(\alpha - \gamma)}{V_{to}}$$

2.3 BANDGAP REFERENCED CIRCUITS IN CMOS TECHNOLOGY

Parisitic bipolar devices in inherent in CMOS technology can be used to implement the Band-gap-referenced biasing as shown in figure 2.5.

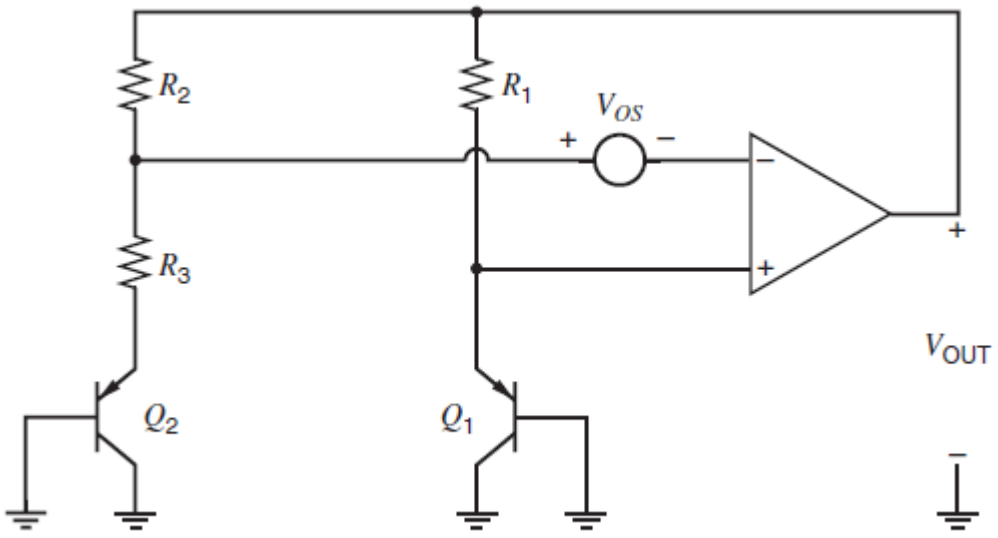

Figure 2.5: BGR using CMOS Technology

Assumptions:

a. CMOS op amp gain -> ∞.

b. $V_{OS} \neq 0$.

Due to mismatch of the threshold and the low transconductance per current of CMOS transistors, the offset of op amps in CMOS technologies is usually larger than in bipolar technologies. With the offset voltage, the voltage across R3 is

$$V_{R3} = \Delta V_{EB} + V_{OS} = V_{EB1} - V_{EB2} + V_{OS}$$

The emitter-base voltages are used here because the base-emitter voltages of the pnp transistors operating in the forward-active region are negative. Then the voltage across R2 is

$$V_{R2} = \frac{R_2}{R_3} V_{R3} = \frac{R_2}{R_3} (\Delta V_{EB} + V_{OS})$$

and the output voltage is

$$V_{OUT} = V_{EB2} + V_{R3} + V_{R2}$$

$$V_{OUT} = V_{EB2} + \left(1 + \frac{R_2}{R_3}\right) (\Delta V_{EB} + V_{OS})$$

The thermal voltage drives the difference between base emitter voltages.

So, $V_{OS} = 0$, shows that the gain K is proportional to (1 + *R*2/*R*3).

$$V_{OUT} = V_{EB2} + \left(1 + \frac{R_2}{R_3}\right) (\Delta V_{EB}) + V_{OS(out)}$$

where the output-referred offset is

$$V_{OS(out)} = \left(1 + \frac{R_2}{R_3}\right) V_{OS}$$

2.4 USE OF OP-AMP IN THE DESIGN

The main principle behind the design of BGR circuit is to add PTAT and CTAT voltage.

To generate a PTAT voltage, a basic principle is shown below. We need two things:

1. The voltage $V_1 = V_2$

2. The currents in the two branches equal.

The above functions could be performed by:

1. Current Mirror

2. Operational Amplifier.

In case of Current Mirror shown in 2.6, due to Channel length modulation, proper mirroring action could not takes place. And also the power supply dependency is more in this case. Hence a better option is to use an op-amp for performing the above two functions.

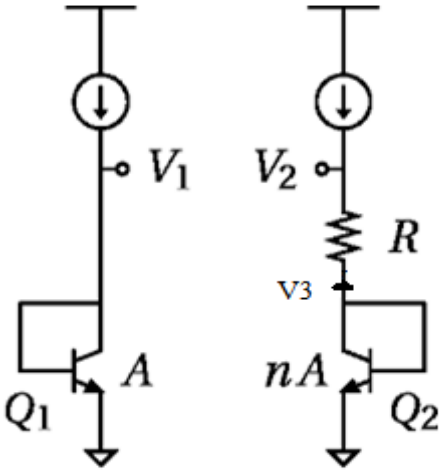

Figure 2.6: Current Mirroring action

If the op-amp makes the two voltages and the currents equal, then

$I_1 = I_2$

$I_1 = Is\ e^{V1/VT}$

$I_2 = n\ Is\ e^{V3/VT}$

$V_3 = V_T \ln \frac{I2}{nIS}$

$V_1 = V_T \ln \frac{I1}{IS}$

$V_1 - V_3 = V_T \ln (n)$ (2.6)

where $V_T = \frac{KT}{q}$

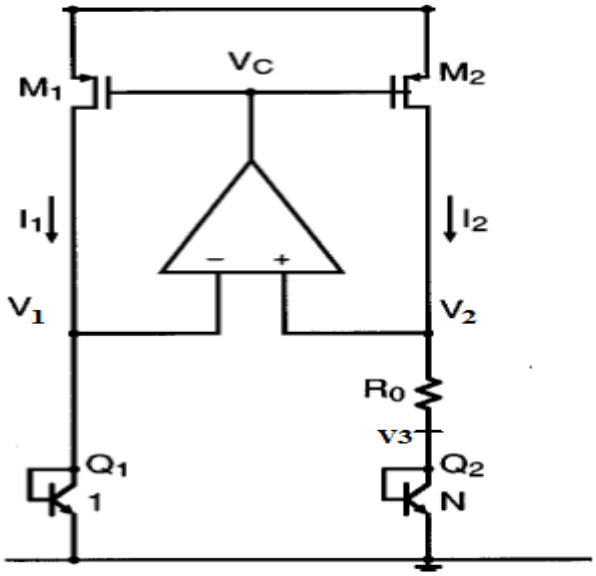

Figure 2.7: Use of Op-amp in BGR

A op-amp has been used in negative feedback which forces its inputs to be equal.

$V_1 = V_2$

Hence from equation 2.6,

$V_2 - V_3 = V_T \ln (n)$

Hence $V2- V3$ is a PTAT voltage, ie, the voltage across the resistor R_0 is a PTAT voltage.

Thus the op-amp makes the drain voltage of M_1 and M_2 equal and hence proper mirroring of currents take place here and a PTAT voltage is generated.

CHAPTER 3

OPERATIONAL AMPLIFIER

The operational amplifier also fondly known as OPAMP, one of the earliest and most used component in AIC design. These building blocks have a property of high forward gain and in negative feedback configuration so that when negative feedback is applied, the closed loop transfer function is practically independent of the gain of the op-amp. One of the most popular and important op-amps is a two- stage op-amp. This is a simple yet robust implementation of an op-amp and second, it can be used as the starting point for the development of other types of op-amp. The op-amp will be designed and is an integral part of the BGR circuit.

3.1 Two Stage Op-Amp

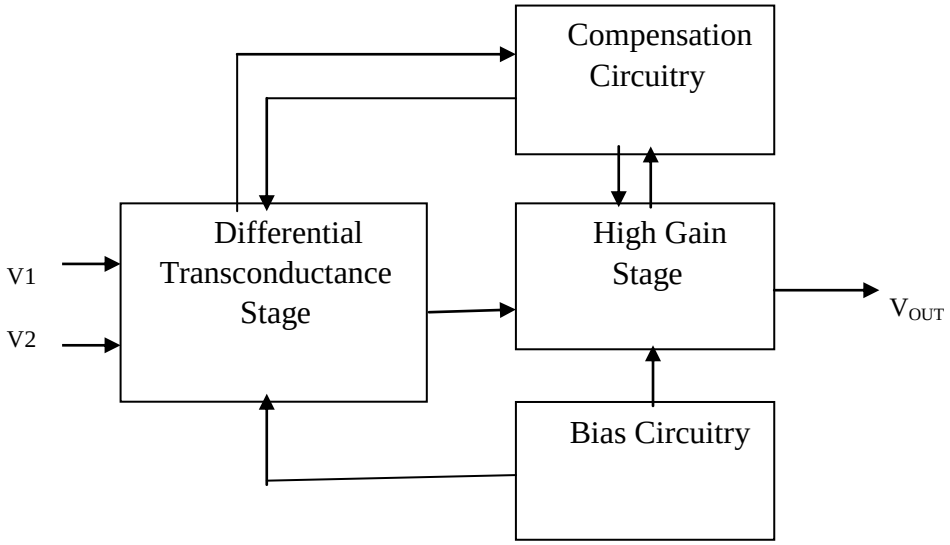

Figure 3.1: Block Diagram Of Op-Amp Used in BGR

The two terminals shown in the above figure by v_2 and v_1 are non-inverting and inverting terminal.

$$V_{out} = A_v(V_2 - V_1)$$

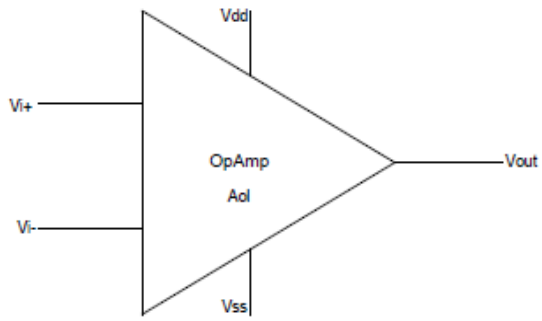

Figure 3.2: Symbol Of Op-Amp Used In BGR

Where the notations on the symbol stand for:

- Open- loop Gain A_{0l}
- Non-inverting input Vi+
- Inverting input Vi-
- Positive Supply Voltage Vdd
- Negative supply voltage Vss
- Output Voltage Vout

3.2 IDEAL OP-AMP

In the past, most Op-Amps were designed to be used in many applications. This means that they have been designed as general purpose building blocks. The transparent symbol for an ideal Op-Amp is shown below.

An ideal op-amp has the following characteristics:

- Infinite open-loop voltage gain, $Aol \approx \infty$.
- Infinite input resistance, $R_{id} \approx \infty$.
- Zero output resistance, $R_o \approx 0$.
- The output voltage $V_{out}=0$; when $V_{id} = V_+ - V_- = 0$.
- Change of output with respect to input, slew rate = ∞.

- Change in output voltage with Temp., $\partial V_o/\partial V_i=0$

In practice, an Op-Amp with zero and infinitive parameters cannot be realized. There are always limitations (e.g., maximum output voltage swing) and trade-offs between the parameters (e.g. the trade-off between open-loop gain and speed) that should be considered during the design process. As a result, there need to be an appropriate specification for each application to device a compromise acceptable for all parameters.

3.3 BASIC CHARACTERISTICS OF OP-AMP

Op-Amps cannot be perfect. Due to the circuitry limitations and trade-offs that exist in analogue design there are a number of imperfections in Op-Amps.

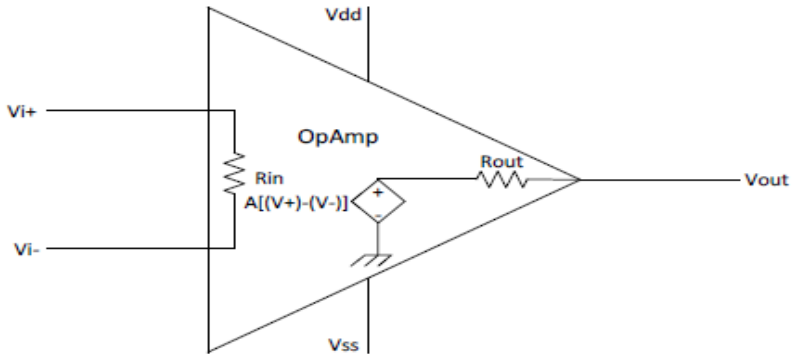

Figure 3.3: Symbol Of Practical Op-Amp

3.3.1 Finite Gain

Typically, Op-Amps exhibit open-loop DC gain between 50dB to over 60dB thus a finite gain.

Open loop configuration is the basic op amp without any feedback. G_o is defined as the ratio of the output voltage to the input voltage without feedback. This is a dimensionless quantity that may be listed on a specification sheet in terms of volts per millivolt (V/mV) or in decibels (dB).

$G_0 = V_{out} / V_{in}$ [V/mV]

$G_0 = 20 \log (V_{out} / V_{in})$ [dB]

3.3.2 Finite Input Impedance

The assumption of infinite input impedance of the Op-Amps stems from the assumption of zero input current for the MOSFETs. Typically, the input impedance of the operational amplifier designed with MOSFETs is within the range of 100 to 1000 Mega Ohms.

3.3.3 Non-Zero Output Impedance

Coming to the output impedance, Op-Amps can be thought of as voltage sources with internal resistance. The voltage drop across the output impedance of the Op-Amp causes power dissipation and delivers less power to the load. The situation is getting worse as the load impedance of the amplifier decreases. However, the use of negative feedback topologies in most applications comes to designer's assistance. Negative feedback lowers the output impedance and reduces output errors accordingly. Typical output impedance for the open-loop operational amplifiers is in the range of 25-100 Ohms which will be much lower when using the Op-Amp in the negative feedback topology (almost a few Ohms). So, the assumption of zero output impedance is quite fair.

3.3.4 Output Swing

Obviously output voltage of the operational amplifier cannot reach to the supply voltages level because of the transistors' overdrive voltages. An amplifier with voltage swing that allows output signal to go very close to supply voltages is called rail-to-rail amplifier. The output swing limits the linearity of the circuits, especially in low voltage applications. One way to reach high output swing is to use fully differential Op-Amps.

3.3.5 Input Current

Input current of the Op-Amps includes biasing current and leakage current of the input transistors. Input current for the MOSFETs is much smaller than BJTs or JFETs and it is about a few Pico amperes. Assuming symmetric circuit and matched input current, error will not be introduced to the differential output of the Op-Amp but it shows itself as a DC offset and limits the output swing. An Op-Amp with a high CMRR can help reducing the offset.

3.3.6 Input Offset Voltage

When no i/p is applied to the opamp there should be 0 o/p ideally but due to imperfection and mismatches in the internal transistors and resistors of the Op-Amp and can be summed up as a DC voltage source and applied in series to one of the inputs of the Op-Amp.

3.3.7 Common-Mode Gain

In An ideal operational amplifier, common-mode gain is zero and the amplifier amplifies only the differential input signal. However, in real amplifiers the voltages that are common to both inputs are amplified to some extent. This amplification is due to imperfections in tail current sources and mismatches between the transistors and resistors of differential pair. The standard measurement factor created to be used when comparing differential circuits is CMRR (Common Mode Rejection Ratio) which can be calculated using this equation:

$CMRR=20\log (G_0 / G_{cm}) \text{ dB}$

CMRR is the ratio of the magnitude of the dc open loop gain, |Go|, to the magnitude of the common-mode gain, |Gcm|.

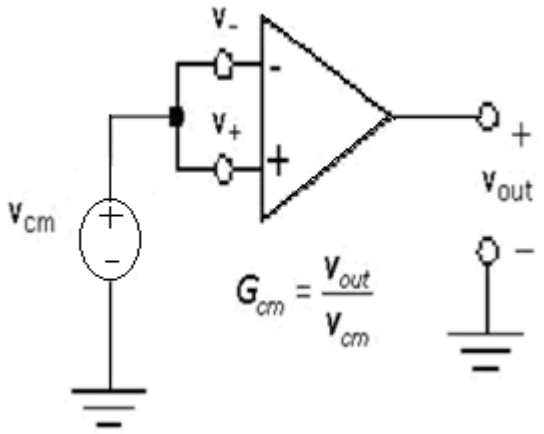

Figure 3.4: Connections For Common Mode

Unity Gain Configuration An amplifier in this configuration has a feedback between inverting input and output terminal while input is connected to the non inverting terminal.

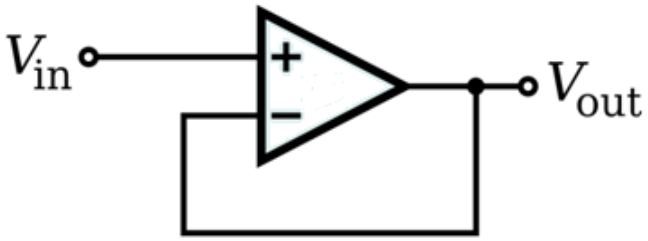

Figure 3.5: Unity Gain Configuration

If the difference between V+ and V- is negligibly small so that V+ = V- we must have:

Vout = Vin

3.3.8 Input Common Mode Range

It specifies over what range of common mode voltages the amplifier continues to sense and amplify the difference signal with the same gain.

3.3.9 Power-Supply Rejection

As opposed to the ideal case, supply noises play an important role in real amplifiers. Thus, the performance of amplifier in presence of supply ripples is of concern to many applications, especially mixed-signal applications that often deal with noisy digital supply lines. There is a factor called PSRR determines the ability of Op-Amps to reject the changes in the power supply.

3.3.10 Noise

Noise exists in amplifiers similar to all analogue circuits. The amount of noise puts a specification for minimum input on the requirement list of the amplifier. If the input signal would be less than this minimum, then it cannot be processed safely. This noise mostly consists of thermal noise and flicker noise of the devices in the circuit. Some of these devices contribute more than others, for example input transistors of the Op-Amp. Those devices should be taken care of by widening and applying more bias current.

There is a trade-off between maximum output swing and noise. In order to have more swing, with the same bias current, the overdrive of the transistors can be lowered to allow more swing. As the overdrive voltage goes down, the transconductance of the amplifier increases which causes more drain noise current. For applications with demands on higher gain or bandwidth, noise becomes an important issue.

3.3.11 Finite Bandwidth

The Op-Amp gain calculated at DC will not stay the same at higher frequencies. As the operational frequency of the circuit increases the gain decreases. At first the gain drop is not significant to be considered as system failure, but after the 3-dB frequency the change in DC gain cannot be ignored. In Figure 3.6, the gain characteristic of an Op-Amp is plotted.

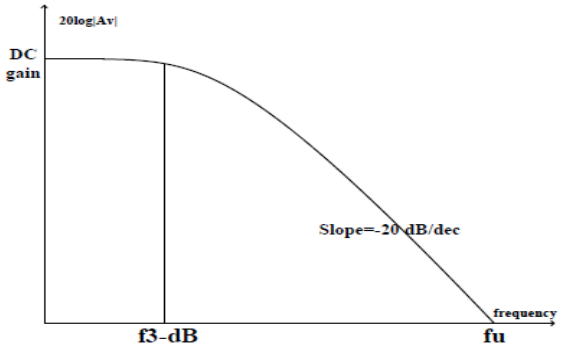

Figure 3.6: Gain Bandwidth Plot Of Op-Amp

High frequency behaviour of the Op-Amp is critical for many applications, especially for those who need high precision gain. The unity-gain frequency of the operational amplifier, "fu", the frequency at which gain drops to zero dB, is a good measure of small-signal bandwidth. Today, using CMOS technology, unity-gain frequencies larger than 1GHz can be achieved.

3.3.12 Nonlinearity

Nonlinearity exists in all analog circuits including Op-Amps. There are several sources that introduce nonlinearity to the circuit. Transistors of the circuit can be considered as one of the main sources as they are inherently nonlinear devices. This source's impact on nonlinearity can be controlled by choosing larger transistor or higher overdrive voltage, especially for input transistors which play a significant role in this case. Considering power and area requirements for circuits, one should be cautious about using these approaches on a large scale.

Another source of nonlinearity is the output swing of Op-Amps. The output voltage is limited between a minimum and maximum value near the supply voltages. When the output voltage crosses these boundaries, mostly due to high voltage gain, saturation occurs and causes output signal damage. Slewing can be considered as one of the other sources of nonlinearity. Reaching the maximum changing rate, the Op-Amp's output voltage will not follow further voltage increase of the input. Internal capacitances are responsible for this effect. The problem can be partly remedied using fully differential circuits in order to suppress second-order harmonics. Furthermore, having higher open-loop gain helps the circuit to have more linearity in closed-loop system.

3.3.13 Stability

The phase difference between input and output leads to oscillation if it becomes 180 degrees in a closed-loop configuration. This means that the amplifier is not stable. Even if the

amplifier is stable, it can suffer from ringing which will affect settling time of the Op-Amp. To measure stability of an amplifier, the concept of phase-margin comes to assist.

3.3.14 Slew Rate

The maximum rate of change of the Op-Amp's output is called slew rate. It also means the maximum available current to charge the load capacitor. Slew rate (SR) is specified in volts per microsecond (V/μs) and is measured by applying a large step to the input and using the equation below.

$$\frac{dVout}{dt} = \text{SR} = \frac{Imax}{CL}$$

When applying a step to the amplifier's input, the step response of the feedback system is proportional to the final output voltage of the system. Therefore, when applying larger steps to the input the output change rate will increase, up to the point where the amplifier enters slewing phase. In slewing phase the load capacitor will be charged by the maximum available current in output stage and the change rate will remain constant (SR).Figure below explains the concept of slewing. It can be seen that increasing the input voltage level wouldn't increase the output change rate after a certain level.

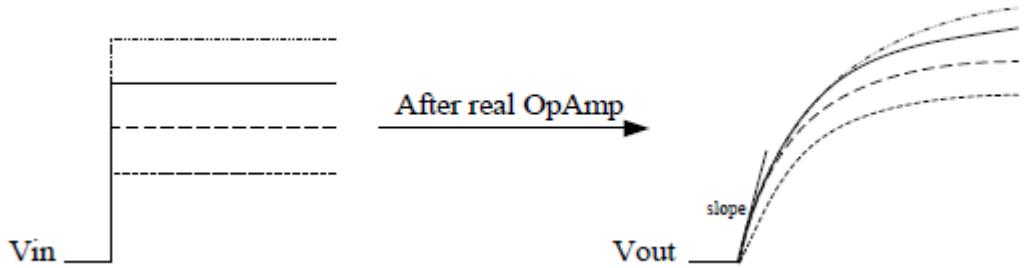

Figure 3.7: Slewing Effect

CHAPTER-4

DYNAMIC THRESHOLD MOSFET

4.1 INTRODUCTION

In 1994, dynamic threshold mosfet (DTMOS) transistor was proposed by Assederaghi et al, As shown in Figure 4.1 take a normal mosfet and just short the gate and body thus turning it into a DTMOS. Thus changing the threshold voltage according to the mode of the working given by eqn (4.1)

Where

ϕ_O - total surface band bending,

γ - a constant body factor,

V_{TO} - threshold voltage at 0 voltage

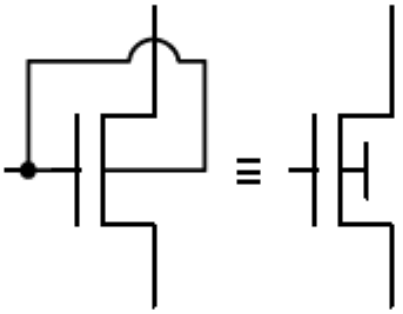

Figure 4.1: DTMOS And Its Symbol

$$V_{TH} = V_{TO} + \gamma \left(\sqrt{(\phi_o + V_{SB})} - \sqrt{\phi_O}\right) \quad (4.1)$$

and zero bias threshold voltage V_{TO} is defined by

$$V_{TO} = V_{FB} + \phi_O + \gamma \sqrt{\phi_O} \quad (4.2)$$

V_{FB} is the flat band voltage and γ is the body effect factor. It is given by

$$\gamma = \frac{\sqrt{2q\varepsilon_{SI}N_A}}{C_{ox}} \quad (4.3)$$

usually,

$$\phi_o = 2\phi_F + \alpha\phi_t \quad (4.4)$$

ϕ_F – Fermi level

$\alpha\phi_t$ – constant multiplied by thermal voltage

DTMOS transistor are fabricated just by connecting the gate and the body of the transistor using a metal contact shown in fig 4.2

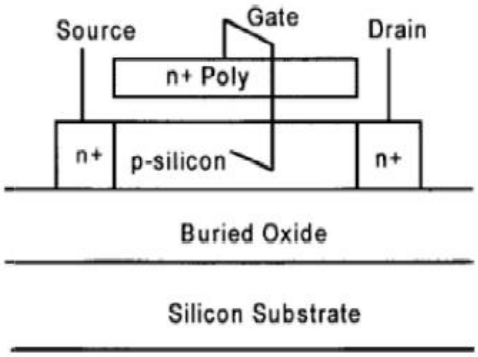

Figure4.2: SOI NMOS Transistor Connected In DTMOS

From Figure 4.2, it is seen that there is a lateral bipolar transistor consisting of two source body and drain body junctions which might latch up and causes very I_B. A very high I_{SB} and I_{DB} is a source of problem. DTMOS is not suitable for voltages over 0.6V. But with the use of extra limiter transistors we could use higher voltage but will affect chip area, robustness, power dissipation thus the performance of the device. So i have used around 0.6 V for each DTMOS used in the circuit.

DTMOS transistor, under the same VGS voltage behaves as a high-transconductance MOSFET as shown in fig 4.3

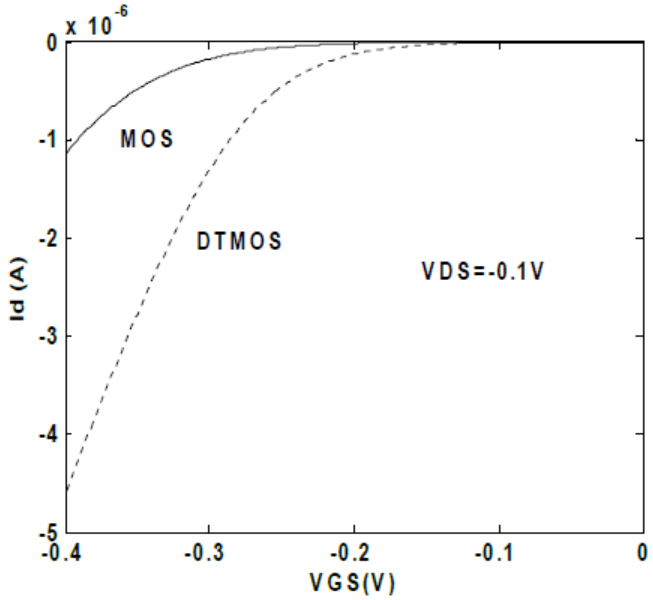

Figure 4.3: The Current Change of DTMOS and MOS Transistors versus V_{GS}

At low voltages normal transistor work in subthreshold region, this is a power saving region for low frequency mode thus I is not proportional to V^0.5 but exponential given by eqn 4.5

$$I_d = \frac{W}{L} I_{d0} e^{\frac{qV_{GS}}{nkT}} \quad (4.5)$$

We can see from eqn 4.6 that g_m is proportional to I like BJT thus the ratio between them is given by 4.8 which is highest

$$g_m = \frac{q}{nkT} I_d \tag{4.6}$$

Subthreshold swing (S) can be approximately calculated by the equation in (4.8).

$$S = \left(\frac{\partial \log Id}{\partial V_{GS}}\right)^{-1} \tag{4.7}$$

$$S = 2.3\frac{nkT}{q} \tag{4.8}$$

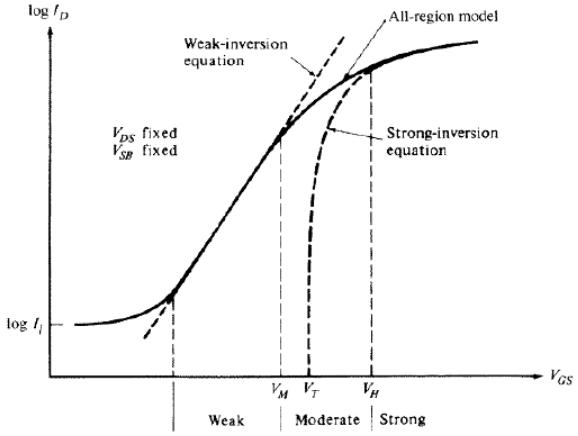

Figure 4.4: Graphical Comparison of Weak And Strong Inversion Models [11].

$$\mathrm{n} = \left(\frac{\partial \psi_s}{\partial V_{GB}}\right)^{-1} = 1 + \frac{C_b}{C_{ox}} \tag{4.9}$$

where ψ_s is surface potential, C_b and C_{ox} are capacitances related to body and oxide respectively.

Thus, for mosfet

$$\mathrm{S} = 2.3\ (1 + \frac{C_b}{C_{ox}})\frac{nkT}{q} \tag{4.10}$$

For DTMOS gate and body are connected thus n becomes equal to unity exactly like ideal case and S for DTMOS becomes.

$$\mathrm{S} = 2.3\ \frac{kT}{q} \tag{4.11}$$

For DTMOS, the drain current is given by 4.12 & 4.13 as follows:

Linear region*:*

$$I_d = \frac{W}{L}\mu_n C_{ox}\{(V_G - V_T(V_{BS}))V_{DS} - \frac{m}{2}{V_{ds}}^2\} \tag{4.12}$$

Saturation region:

$$I_d = \frac{W}{L}\mu_n C_{ox}(V_G - V_T(V_{BS})^2/m \tag{4.13}$$

$$m = 1+ \partial \tag{4.14}$$

$$\partial = -\frac{dV_T}{dV_{BS}} = \frac{1}{C_{ox}}\sqrt{\frac{q\varepsilon_{SI}N_A}{2(2\phi_f - V_{BS})}} \quad (4.15)$$

m is the body effect coefficient.

It should be noted that, because the DTMOS transistors are operated by connecting the gate with the substrate, the substrate bias may thus be given as

$$V_{BS} = \alpha V_G \ (0 \leq \alpha \leq 1) \quad (4.16)$$

The α is defined as a constant ratio of the dynamical biases between the gate and the substrate.

4.2 SMALL SIGNAL MODEL OF DTMOS

DTMOS behaves exactly like mosfet just with the addition of body conductance (g_{mb}). Small signal analysis of DTMOS is figure 4.5.

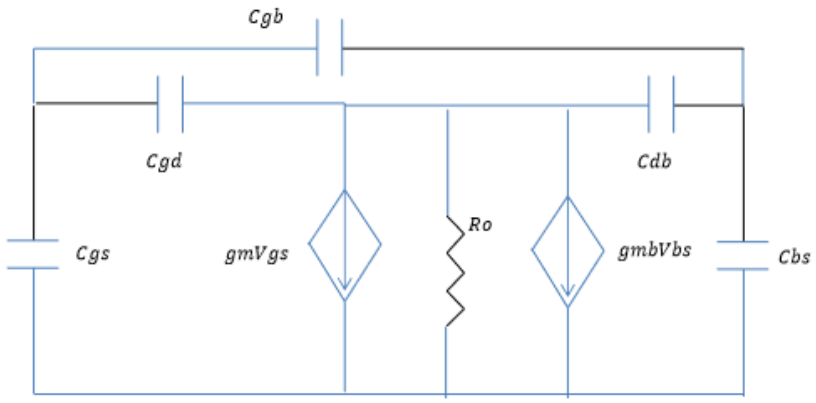

Figure 4.5: Small Signal Analysis of DTMOS

g_m= transconductance of the MOSFET.

c_{gs}= Capacitance between gate and source

c_{gd} = Capacitance between gate and drain

For DTMOS, value of transition frequency is given by 4.17-

$$F_t = \frac{g_m + g_{mb}}{2\pi(C_{gs} + C_{gd})} \quad (4.17)$$

g_{mb} = transconductance due to body terminal

Hence due to increase in the overall transconductance, transition frequency increases and hence the bandwidth of the circuit is increased. In gate-driven technique, the i/p is applied to the gate terminal of MOS; hence only gate transconductance (*gm*) contributes to the conduction current.

CHAPTER-5

ANALYSIS OF OPERATIONAL AMPLIFIER

5.1 TWO STAGE OPERATIONAL AMPLIFIER

We have studied two stages of Opamp in this chapter first was differential amplifier and second is common source amplifier now we have to see how to join them as one single stage.

Table 5.1: Differential Amplifier Parameter

CIRCUIT ELEMENTS/PARAMETER	**PERFORMANCE PARAMETER**
I_0	SLEW RATE
M_1 , M_2	GAIN BANDWIDTH PRODUCT
M_3 , M_4	$ICMR_+$
M_5	$ICMR_-$
M_8	I_0 and M_5

The above table 5.1 shows the relationship between circuit parameters of differential amplifier and performance parameters

In general, Op Amps require at least two gain stages which introduce number of poles in the frequency response. Each pole gives -90º phase shift and causes phase margin to reach -180º, thus leading to oscillation of the system. To stabilize this we need "compensation".

5.1.1 FIRST APPROACH (UNCOMPENSATED OPAMP):

They can be joined in a cascade manner firstly the differential amplifier stage then CS amplifier stage.

From small signal figure 5.2 we can see that two poles of the direct connection would be $1/R_1C_1$ and $1/R_2C_L$ where R_1 (R_2) is the resistance to ground seen from the output of the first (second) stage and C_1 (C_2) is the capacitance to ground seen from the output of the first (second) stage $C_1= C_{DS2}+C_{DS4}$+gate capp of M_6 and C_L is the load capacitance.

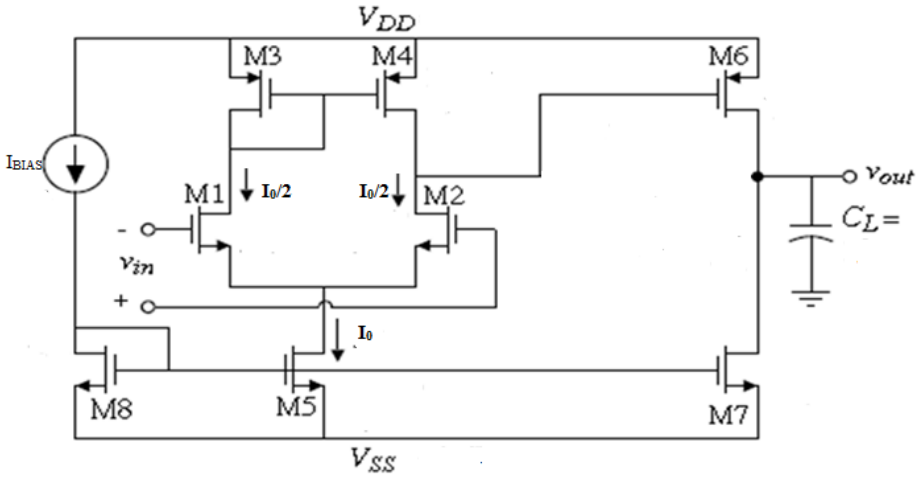

Figure 5.1: Uncompensated Operational Amplifier

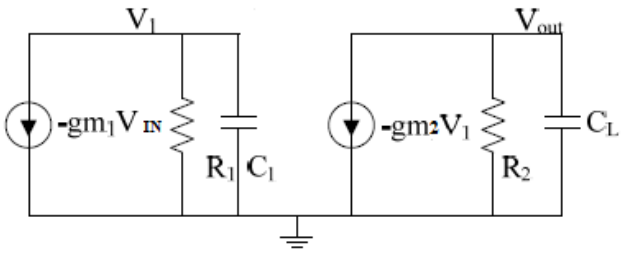

Figure 5.2: Small Signal Analysis of Uncompensated Opamp

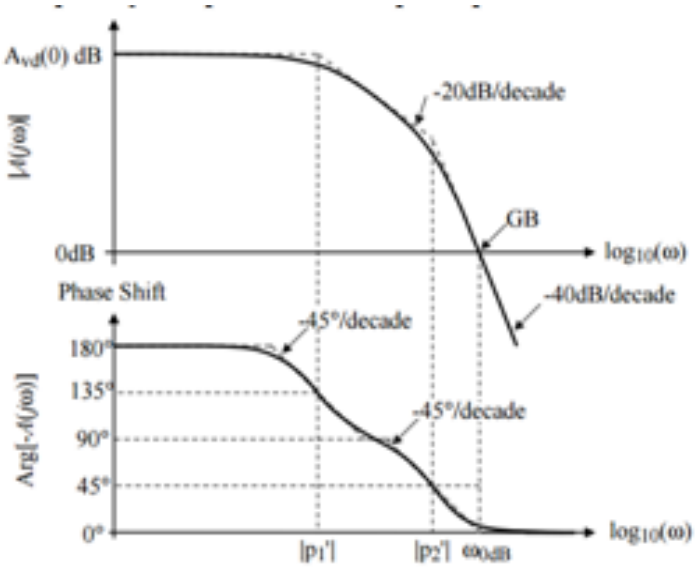

Figure 5.3: Frequency Response of Uncompensated Opamp

The Phase Margin is much less than 45° as can be seen from above figure 5.7. Therefore, before using it in a closed-loop configuration the op amp must be compensated.

5.1.2 SECOND APPROACH (COMPENSATED OPAMP)

MILLER CAPACITANCE-The more straightforward approach is to make the gain drop faster in order for the phase margin to be less than -180° at the gain crossover frequency.

Thus, achieving stability by reducing the bandwidth of the amplifier. The most widely used compensation technique in analog circuit and systems design is undoubtedly pole splitting. A miller capacitor is used to split the poles, which causes the dominant pole to move to a much lower frequency and thus reducing the bandwidth and providing ample stability.

Figure 5.4 shows the block diagram of a two-stage operational amplifier employing Miller Compensation or Direct compensation technique. The Op Amp consists of an input differential pair with gain A1. The second stage (output stage) is biased from the output of the differential stage and driving a large capacitive load. Before the compensation, the poles of the two stage cascade are given as $p_1=1/R_1C_1$ and $p_2 = 1/R_2C_2$.

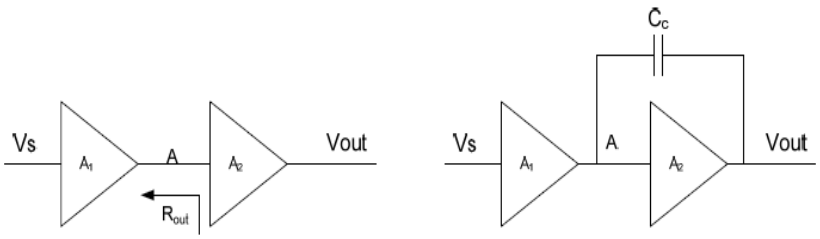

Figure 5.4: Miller Compensation Technique

In order to achieve dominant pole stabilization of the Op amp, Miller compensation is used to perform pole splitting. A capacitor is place between the output of the amplifier and the output of the first stage as shown Figure 5.4 used as a compensator. The capacitor seen at node A due to the miller effect is $(1+A_2)C_c$. This kind of compensation splits the two poles apart as shown in Figure 5.11. The dominant pole moves to near origin, hence reducing the bandwidth, while the non-dominant pole is moved to a higher frequency. However the miller capacitor also introduces a zero in right half plane due to the feed forward current from the o/p of the internal stage to o/p of the amplifier. Figure 5.6 shows the small signal model of this technique.

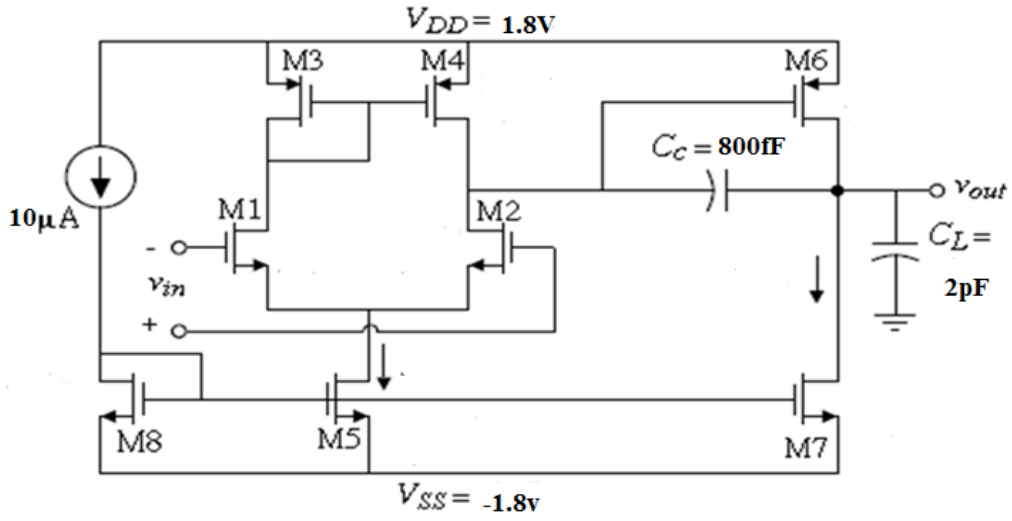

Figure 5.5: Two Stage Compensated Opamp

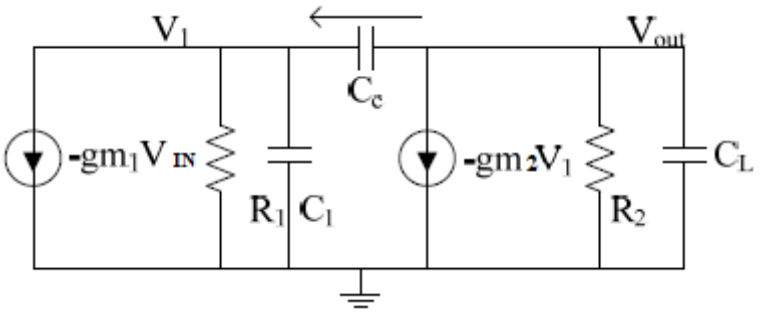

Figure 5.6: Small Signal Analysis of Two Stage Compensated Opamp

The small signal transfer function for the two stage amplifier with miller compensation is given as

Using KVL equations at node V_1 and V_0

$$\frac{V_1}{\frac{1}{sC_1}} + \frac{V_1}{R_1} + gm_1V_{IN} + \frac{V_1 - V_{out}}{\frac{1}{sC_C}} = 0 \tag{5.1}$$

$$\frac{V_{out} - V_1}{\frac{1}{sC_C}} + \frac{V_{out}}{R_2} + \frac{V_{out}}{\frac{1}{sC_2}} + gm_2V_1 = 0 \tag{5.2}$$

Solving these two equations we get

$$\frac{V_{out}}{V_{IN}} = \frac{gm_1gm_2R_1R_2\left(1-\frac{sC_C}{gm_2}\right)}{s^2R_1R_2(C_1C_L+C_2C_c+C_CC_L)+ s(R_2(C_C+C_L)+R_1(C_C+C_1)+gm_2R_1R_2C_C)+1} \tag{5.3}$$

Now C_L is much greater than C_1 and C_c is greater than C_1

Thus general form of transfer function would become

$$\frac{V_{out}}{V_{IN}} = \frac{gm_1gm_2R_1R_2\left(1-\frac{s}{Z_1}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} \tag{5.4}$$

Now comparing equation 5.18 and 5.19 we get

$$Z_1 = \frac{gm_2}{C_C} \quad (5.5)$$

The dominant pole is located at

$$p_1 = \frac{-1}{gm_2 R_2 R_1 C_c} \quad (5.6)$$

$$p_2 = \frac{-gm_2}{C_L} \quad (5.7)$$

Gain of overall opamp is

$$A_V = gm_1 gm_2 R_1 R_2 \quad (5.8)$$

$$GBW = A_V p_1 = \frac{gm_1}{C_C} \quad (5.9)$$

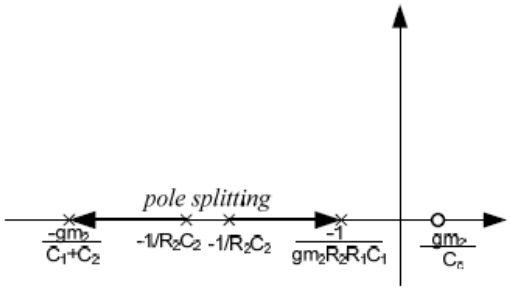

Figure 5.7: Position of Poles After Compensation

Now performance parameter of the opamp

1) **Slew Rate (SR)**: it simply tells how quickly an output can change. If we consider a case from figure 5.5 where M_1 is off and M_2 is on then M_1, M_3 would have no current flowing and so is M_4 due to current mirror action. M_2 will conduct because of C_C which would give

   $SR=I_0/C_C$ (5.10)

   Now considering another case in which M_2 is off and M_1 is on so is M_3 and M_4 so here also current will towards C_C thus giving the same relation as above.

2) Phase Margin: It should be maintained between 45 deg to 60 deg atleast. For this we have to keep p_2 away from GB for this we assume

   Z >= 10*GB

   Thus giving

   P_2 >= 2.2*GB (5.11)

   C_C >= 0.22C_L (5.12)

Table 5.2: Operational Amplifier Parameters

CIRCUIT ELEMENTS/PARAMETER	PERFORMANCE PARAMETER
$I_0 = I_5$	SLEW RATE
M_1 , M_2	GAIN BANDWIDTH PRODUCT
M_3 , M_4	$ICMR_+$
M_5	$ICMR_-$
M_6	Gain,M_3& M_5
M_7	M_5
C_L	C_C
C_C	Phase margin

Table 5.2 gives the relationship between circuit and performance parameters.

Now some general equations used for the analysis and designing of Opamp

Transconductance and aspect ratio of transistor 1 is

$$gm_1 = GBC_C 2\pi \tag{5.13}$$

$$(\frac{W}{L})_1 = \frac{gm_1^2}{\mu_n C_{ox} 2I_d} = (\frac{W}{L})_2 \tag{5.14}$$

Input common mode (max) range is given by 5.15

$$ICMR_+ \leq V_{D1} + V_{t1} = V_{DD} - (\sqrt{\frac{2I_3}{\beta}} + |V_{t3}|)_{max} + V_{t1} \tag{5.15}$$

Aspect ratio of transistor 3 is

$$(\frac{W}{L})_3 = 2\frac{I_{D3}}{\mu_p C_{ox}(V_{DD} - ICMR_+ - V_{t3max} + V_{t1min})^2} \tag{5.16}$$

Input common mode (min) range is given by 5.17

$$ICMR_- \geq \sqrt{\frac{2I_{D1}}{\beta_1}} + V_{t1max} + V_{DSAT} \tag{5.17}$$

Aspect ratio of transistor 5 can be found from 5.18

$$I_{D5} = \frac{\mu_n C_{ox}(\frac{W}{L})_5}{2} {V_{DSAT}}^2 \tag{5.18}$$

$$V_{DS3} = V_{gs4} = V_{DS6} = V_{GS3} \tag{5.19}$$

Aspect ratio of transistor 6:

$$\frac{(\frac{W}{L})_6}{(\frac{W}{L})_4} = \frac{I_6}{I_4} = \frac{g_{m6}}{g_{m4}} \quad (5.20)$$

$$V_{gs5} = V_{gs7} \quad (5.21)$$

Aspect ratio of transistor 5 can be found from 5.22

$$\frac{I_7}{I_5} = \frac{(\frac{W}{L})_7}{(\frac{W}{L})_5} \quad (5.22)$$

5.2 FULL DTMOS OPERATIONAL AMPLIFIER

Differential Transconductance Stage

Transistors M1, M2, M3 and M4 form the first stage i.e. differential stage. This provides conversion from differential to single ended by use of M3 and M4. The inverting input at M1 and non inverting input at M2 transistor are provided. The differential signal applied will be amplified according to the gain of the differential stage. Transistors M3 and M4 acts as active load transistors i.e. current mirror.

High Gain Stage

The second stage is the CS amplifier with PMOS M6 acting as amplifier and M7 as NMOS load. This provide additional gain in the amplifier.

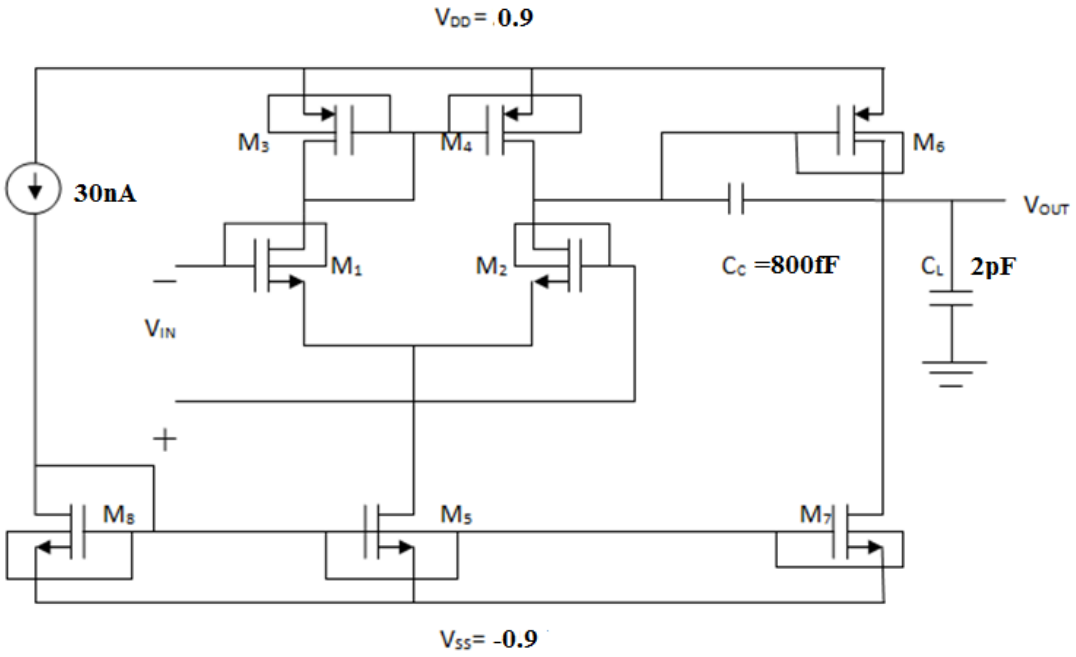

Figure 5.8: Proposed Structure Full DTMOS Opamp

.

Biasing Circuit

The biasing of the Op Amp is achieved with the help of simple current mirror bias i.e. transistors M5, M7 and M8 which make sure that the transistors are operating in the saturation region. The bias current used here is 30nA.

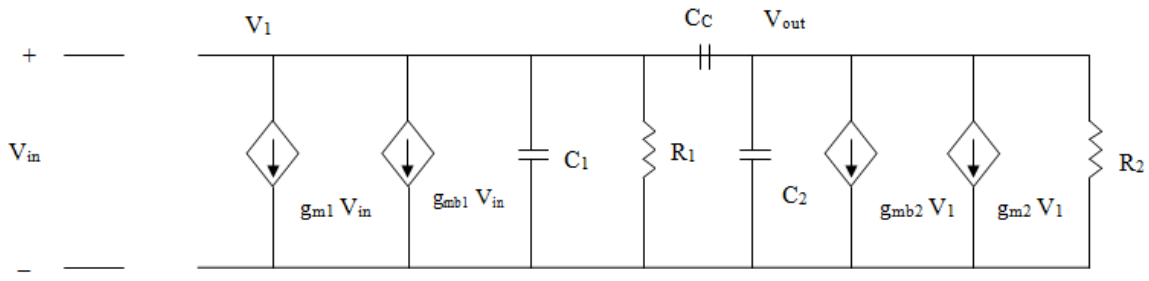

Figure 5.9: Small Signal Analysis of Proposed Structure - Full DTMOS Opamp

Node equation at V_1

$$\frac{V_1}{\frac{1}{sC_1}} + \frac{V_1}{R_1} + gm_1V_{IN} + gm_{b1}V_{IN} + \frac{V_1 - V_{out}}{\frac{1}{sC_C}} = 0 \quad (5.23)$$

Node equation at V_{out}

$$\frac{V_{out} - V_1}{\frac{1}{sC_C}} + \frac{V_{out}}{R_2} + \frac{V_{out}}{\frac{1}{sC_2}} + gm_2V_1 + gm_{b2}V_1 = 0 \quad (5.24)$$

Using these 2 equations we get

$$\frac{V_{out}}{V_{IN}} = \frac{(gm_1+gm_{b1})gm_2R_1R_2(1-\frac{sC_C}{gm_2})}{s^2R_1R_2(C_1C_L+C_2C_c+C_CC_L)+ s(R_2(C_C+C_L)+R_1(C_C+C_1)+(gm_2+gm_{b2})R_1R_2C_C)+1} \quad (5.25)$$

Now comparing this equation with general equation of transfer function of equation 5.4

$$A_V = (gm_1 + gm_{b1})(gm_2 + gm_{b2})R_1R_2 \quad (5.26)$$

$$Z_1 = \frac{(gm_2+gm_{b2})}{C_C} \quad (5.27)$$

The dominant pole is located at

$$p_1 = \frac{-1}{(gm_2+gm_{b2})R_2R_1C_c} \quad (5.28)$$

$$p_2 = \frac{-(gm_2+gm_{b2})}{C_L} \quad (5.29)$$

$$GBW = A_Vp_1 = \frac{(gm_1+gm_{b1})}{C_C} \quad (5.30)$$

This is the complete analysis of both the opamp

CHAPTER 6

DESIGN AND SIMULATION

6.1 SIMULATIONS OF TWO STAGE CMOS AMPLIFIER

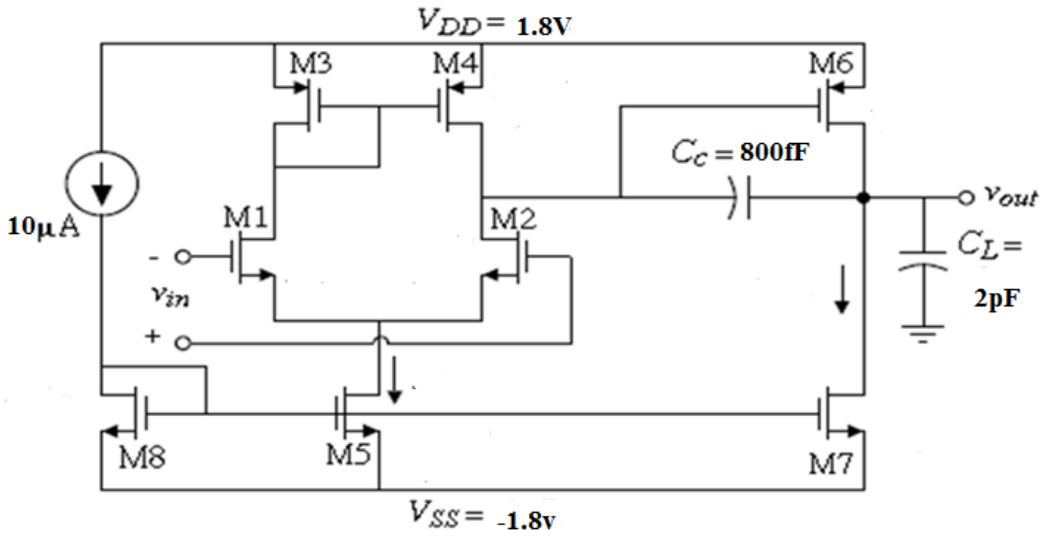

Figure 6.1: Two Stage CMOS Opamp

Everything is same as the explanation given in chapter 5 for figure 5. Except the bias current used here is 10uA.

SIMULATIONS:

1) OPEN LOOP DC SIMULATION-

OFFSET VOLTAGE- Ideally when no i/p is given to opamp the o/p should be zero as the difference is zero at the i/p terminal, but there is always some o/p corresponding to that known as offset voltage. Here the offset voltage calculated for the op-amp is 0.04V.

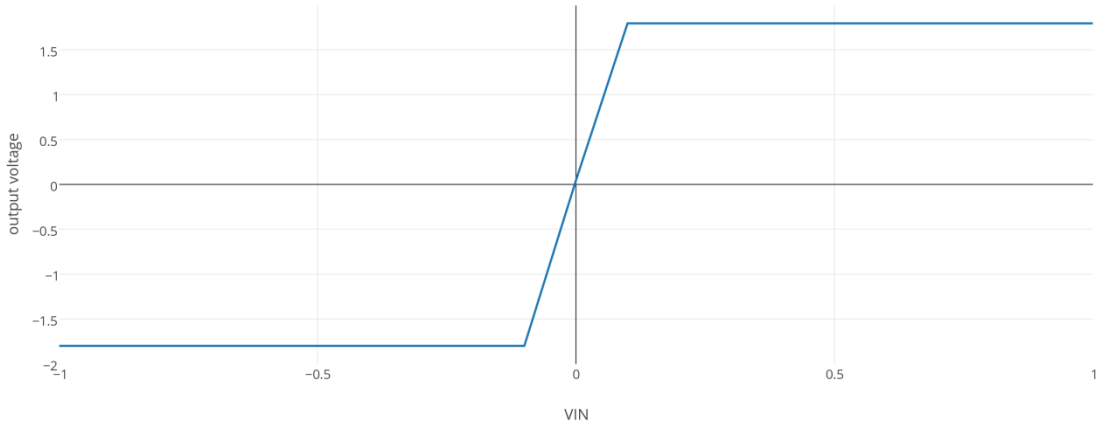

Figure 6.2: DC Characteristic of Two Stage CMOS OPAMP

2) **OPEN LOOP AC SIMULATION-** It is done to calculate the gain margin and phase margin of the system. The ratio of the output parameter to the input parameter is defined as gain. Here the input voltage given as sine wave with 1V amplitude. Bandwidth is the maximum allowable range of the frequencies. Here the

bandwidth - 21 MHz for unity gain

3dB - 30kHz .

GAIN=60db

Phase margin = 106deg

GBP = 21M

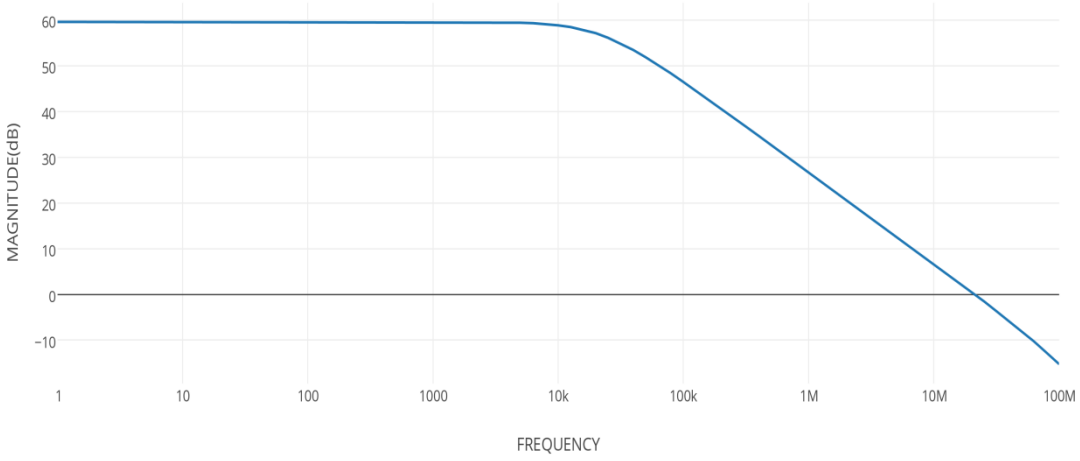

Figure 6.3: AC Characteristic (magnitude) Of Two Stage CMOS OPAMP

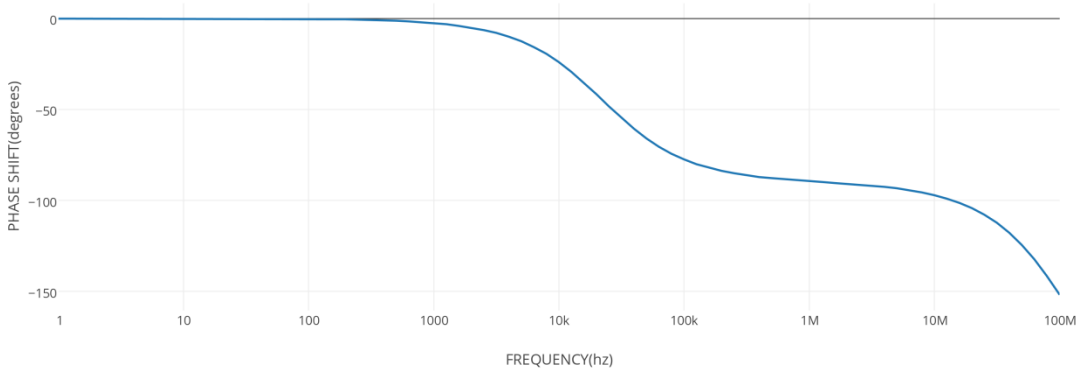

Figure 6.4: AC Characteristic (phase) Of Two Stage CMOS OPAMP

3) CMRR:

COMMON GAIN (A_C) = -3.87 dB

DIFFERENTIAL GAIN(A_D) = 60db

CMRR= $A_D - A_C$ = 63.87db

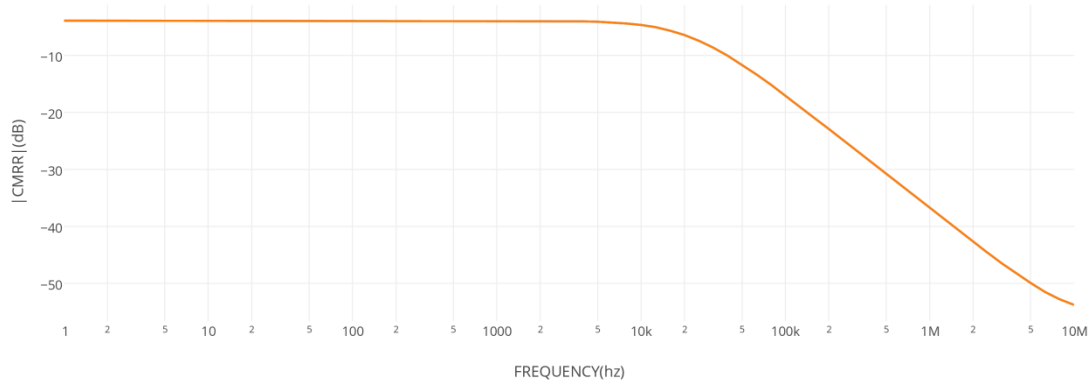

Figure 6.5: CMRR Of Two Stage CMOS OPAMP

4) UNITY GAIN CONFIGURATION PARAMETERS:

a) **ICMR**- it is found to be +-1.6V

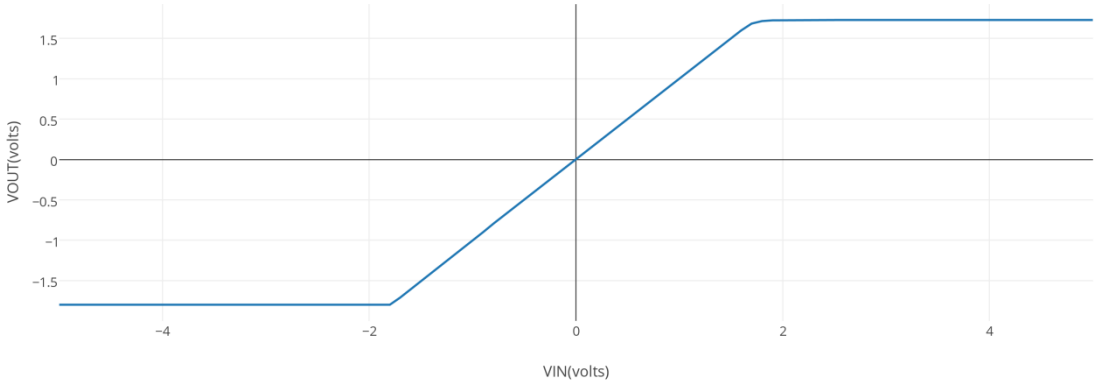

Figure 6.6: ICMR Of Two Stage CMOS OPAMP

b) **PSRR$^+$ and PSRR$^-$** - For PSRR we give ac supply to V_{DD} and V_{SS} for PSRR$^+$ and PSRR$^-$ respectively and give input zero.

Values of PSRR$^+$=65.23dB

PSRR$^-$=81.69dB

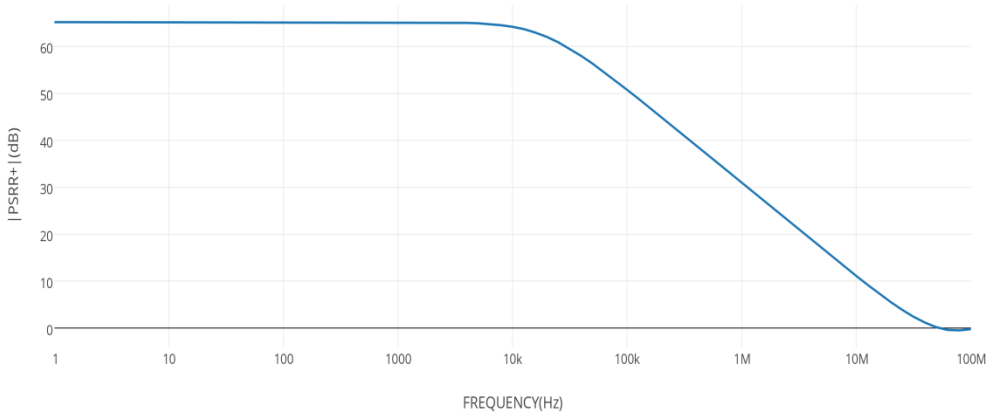

Figure 6.7: PSRR^{+} Of Two Stage CMOS OPAMP

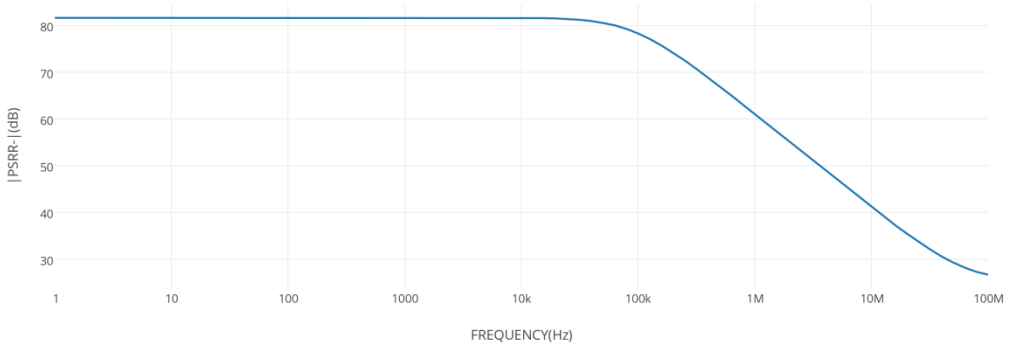

Figure 6.8: PSRR^{-} Of Two Stage CMOS OPAMP

c) SLEW RATE:

Slew rate = 20.2v/µs

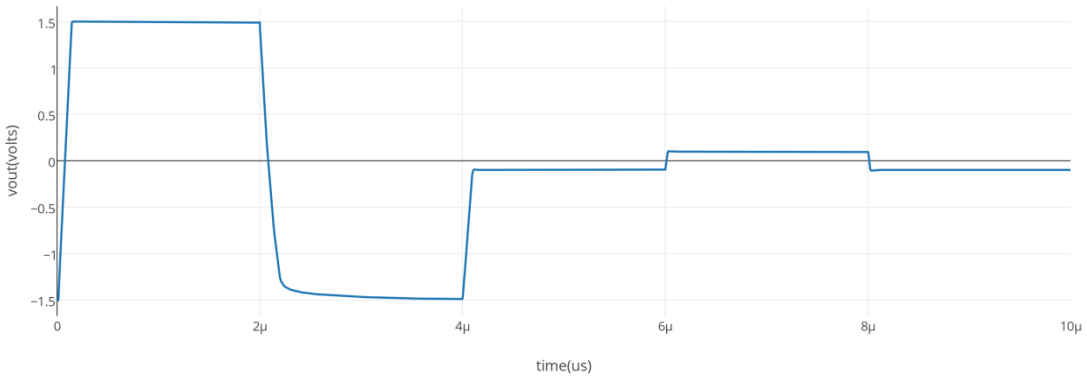

Figure 6.9: Slew Rate Of Two Stage CMOS OPAMP

ADVANTAGES

This opamp provides:

- Open-loop voltage gain is high
- Output swing is rail-to-rail
- Common-mode input range is large

- Only one frequency compensation capacitor
- Transistors are less in number

6.2 SIMULATIONS OF TWO STAGE DTMOS OPERATIONAL AMPLIFIER

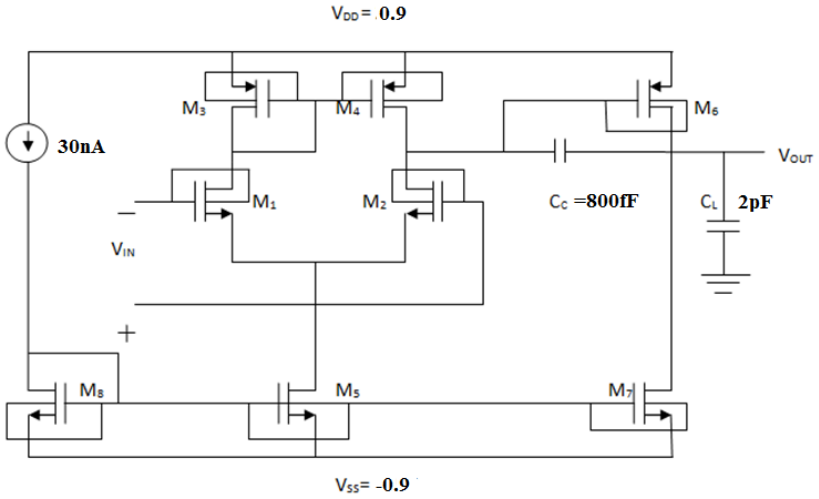

Figure 6.10: Two Stage DTMOS Opamp

1) OPEN LOOP DC SIMULATION-

It is found to be .138V

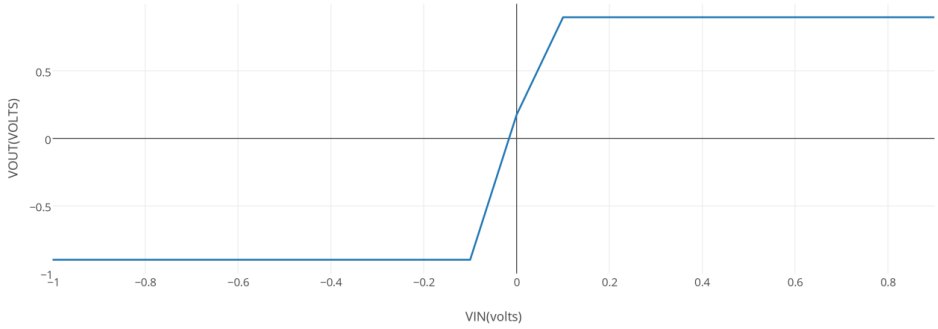

Figure 6.11: DC characteristics of Two Stage DTMOS Opamp

2) OPEN LOOP AC SIMULATION

It is done to find the gain and phase margin of the system.

GAIN=58.2db

Phase margin = 102deg

GBP = 100kHz

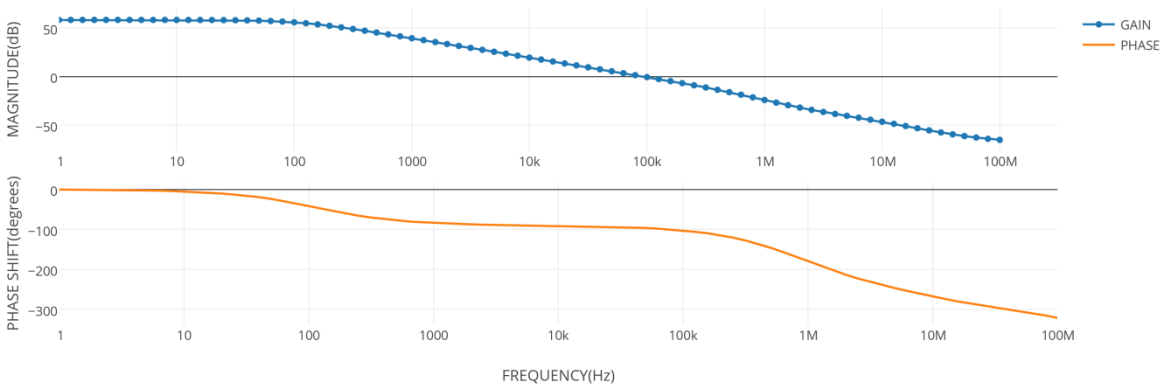

Figure 6.12: AC characteristics of Two Stage DTMOS Opamp

3) CMRR

COMMON GAIN (A_C) = -3.5 dB

DIFFERENTIAL GAIN (A_D) = 58.2db

CMRR= $A_D - A_C$ = 61.7db

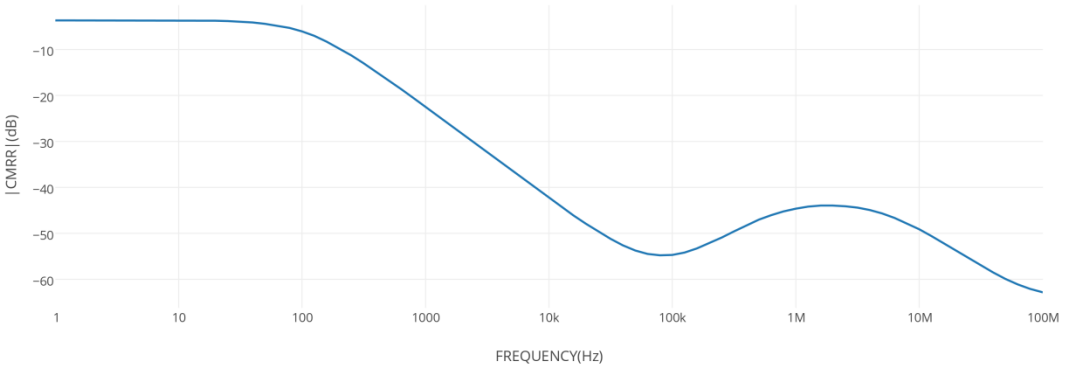

Figure 6.13: CMRR of Two Stage DTMOS Opamp

4) UNITY GAIN CONFIGURATION SIMULATION

a) $PSRR^+$ and $PSRR^-$

$PSRR^+$ - 66dB

$PSRR^-$ 78.6dB

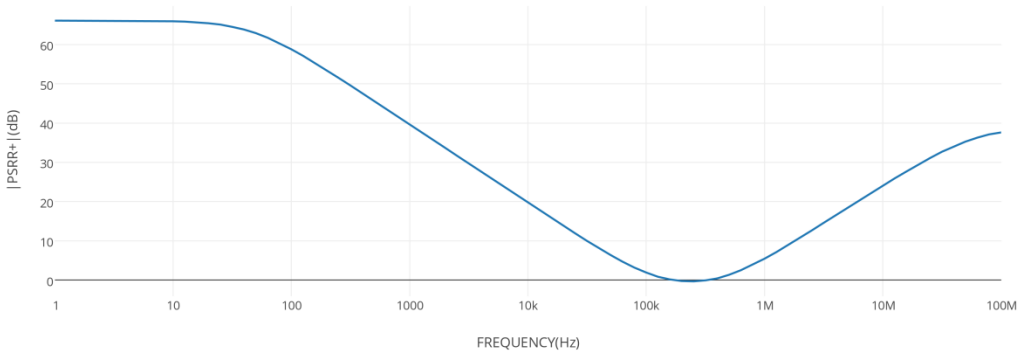

Figure 6.14: PSRR^{+} Two Stage DTMOS Opamp

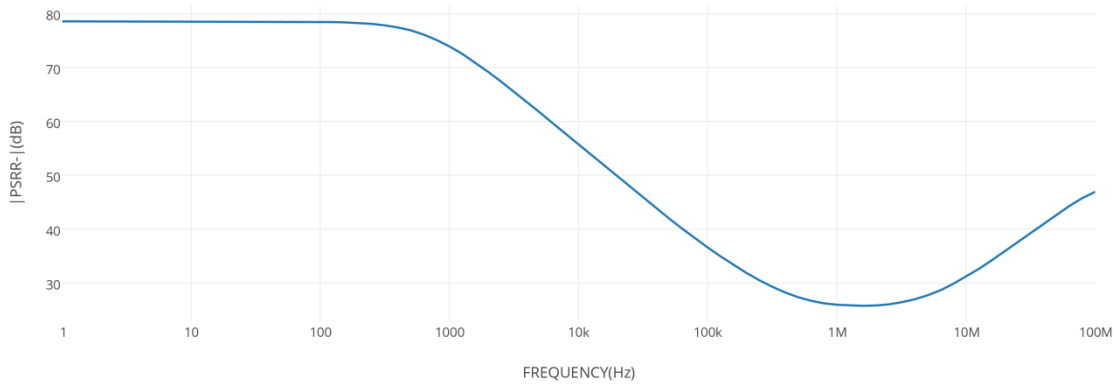

Figure 6.15: PSRR^{-} of Two Stage DTMOS Opamp

b) **ICMR-** it is found to be +-0.7

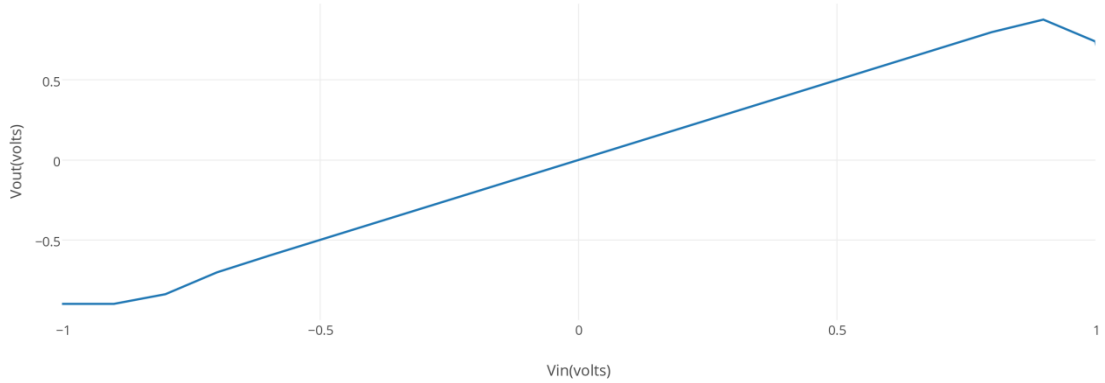

Figure 6.16: ICMR of Two Stage DTMOS Opamp

c) SLEW RATE : it is found to be 10V/µs

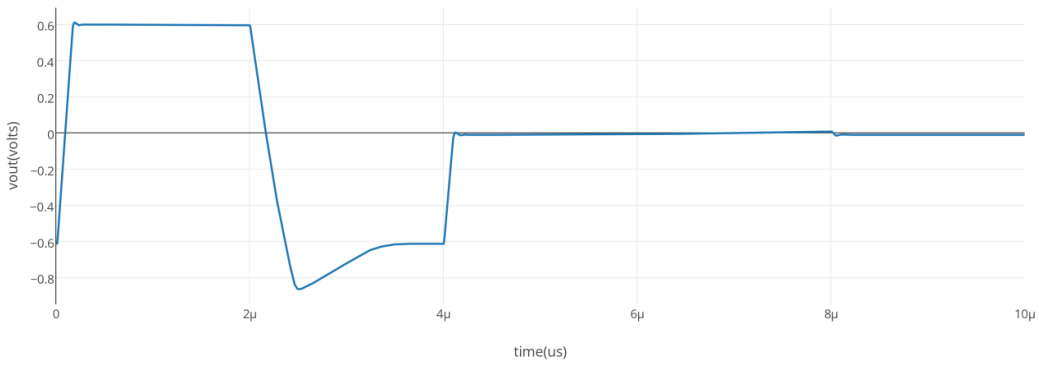

Figure 6.17: Slew Rate of Two Stage DTMOS Opamp

ADVANTAGES

- As compared to the conventional structure very low bias current is needed
- It proves to be very effective in maintaining the proper balance between various parameters.
- Very low power dissipation.

6.3 BGR WITH 2 STAGE CMOS OP-AMP

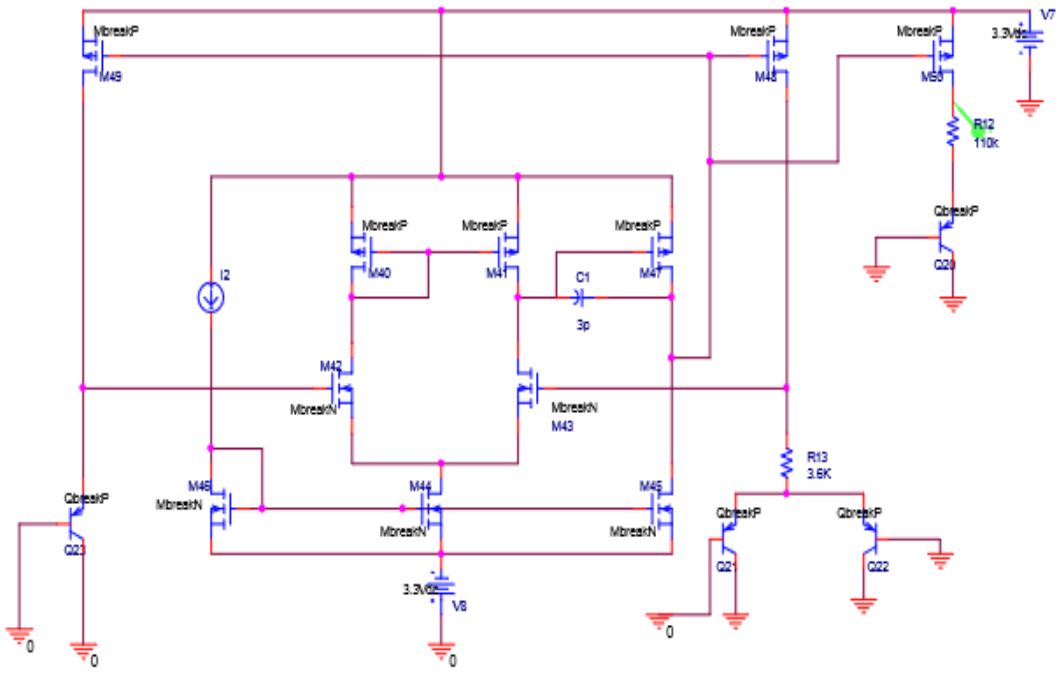

Figure 6.18: BGR With 2 Stage OP-AMP

Two stage cmos op-amp shown in fig 6.1 is embedded in this BGR. It can be seen in fig 6.18, this 2 stage cmos op-amp and its biasing circuitry forms the PTAT and the bjt at output forms the CTAT circuit and combination of both gives the BGR. Fig 6.19 shows the output voltage variation with temperature giving 1.184 V at 0 degree and 1.112 V at 100 degree yielding 1.33% and 7.3% but in mid band it gives a real constant value. Fig 6.20 shows the variation of this output voltage at different values of Vdd it also gives the output of 1.2 V but it saturates before 1.5 V of Vdd.

Fig 6.21 shows variation of Vdd and variation of temperatures simultaneously thus we can say that the value is almost constant near 1.2 V. Fig 6.22 shows with time and temperature variation there is no change in output voltage.

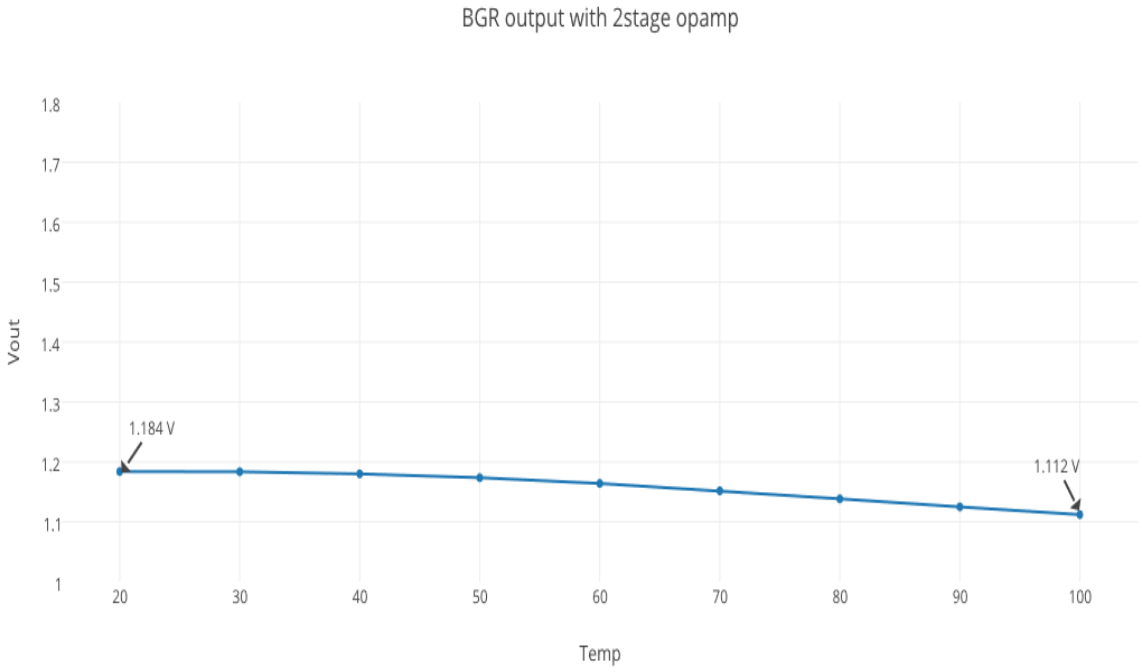

Figure 6.19: BGR Output Of 2 Stage CMOS OP-AMP With Temperature Variations

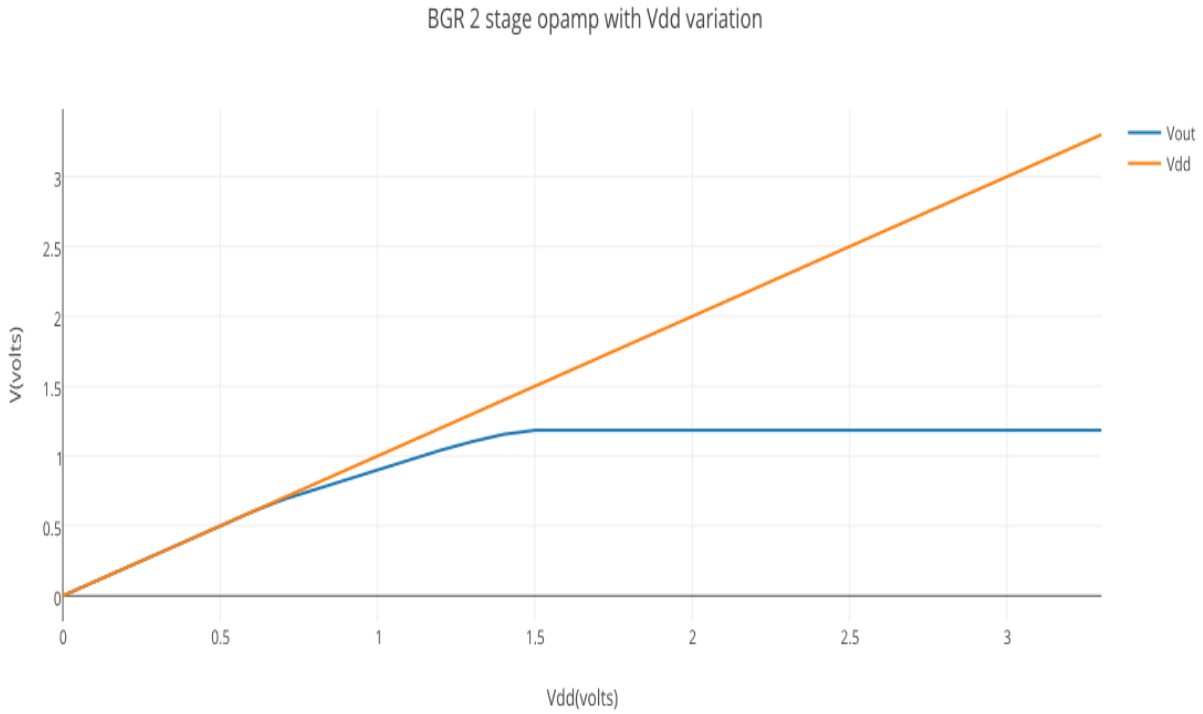

Figure 6.20: BGR Output Of CMOS OP-AMP With Vdd Variation

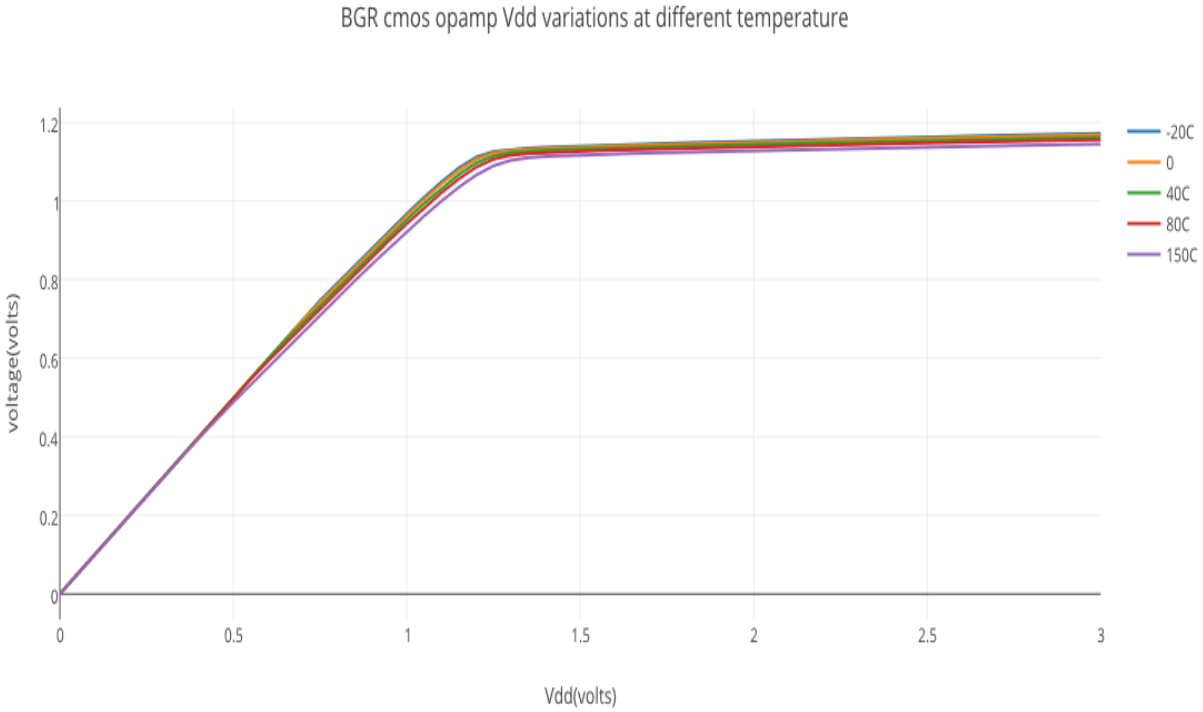

Figure 6.21: BGR 2 Stage CMOS OP-AMP Output Vdd Variation At Different Temperatures

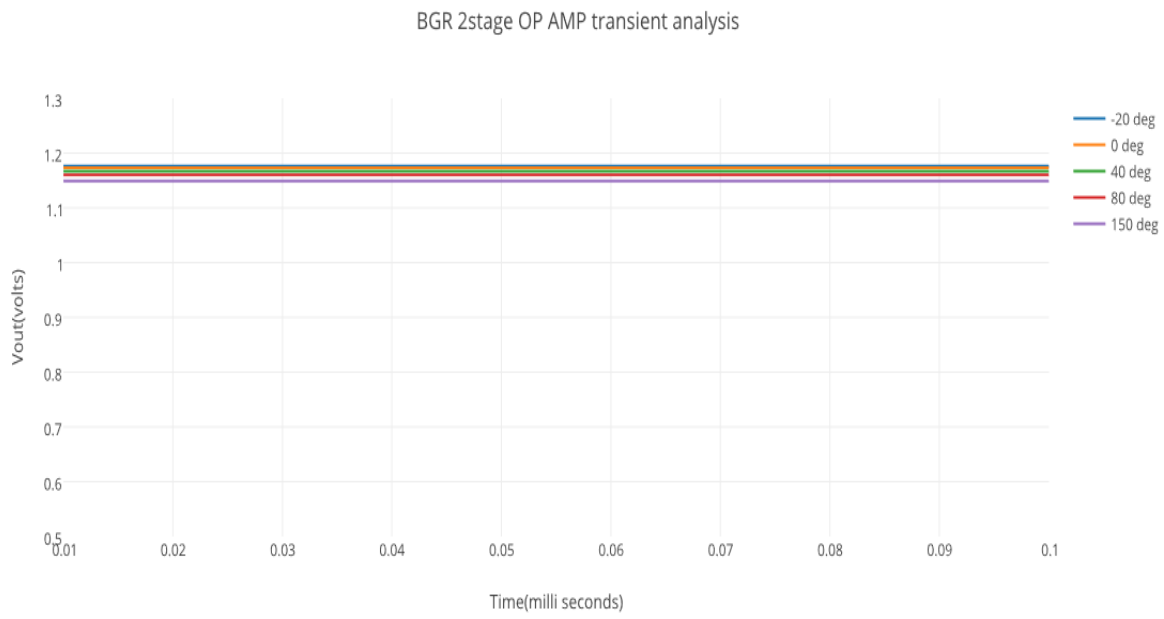

Figure 6.22: Transient Analysis Of Two Stage CMOS At Different Temperature

6.4 BGR WITH TWO STAGE DTMOS OP-AMP

Fig 6.23 shows the modified version of 2 stage cmos op-amp where we have used dtmos, with dtmos added advantage of low power and low values of bias and supply voltages is there. Thus static and dynamic power dissipations are really low.

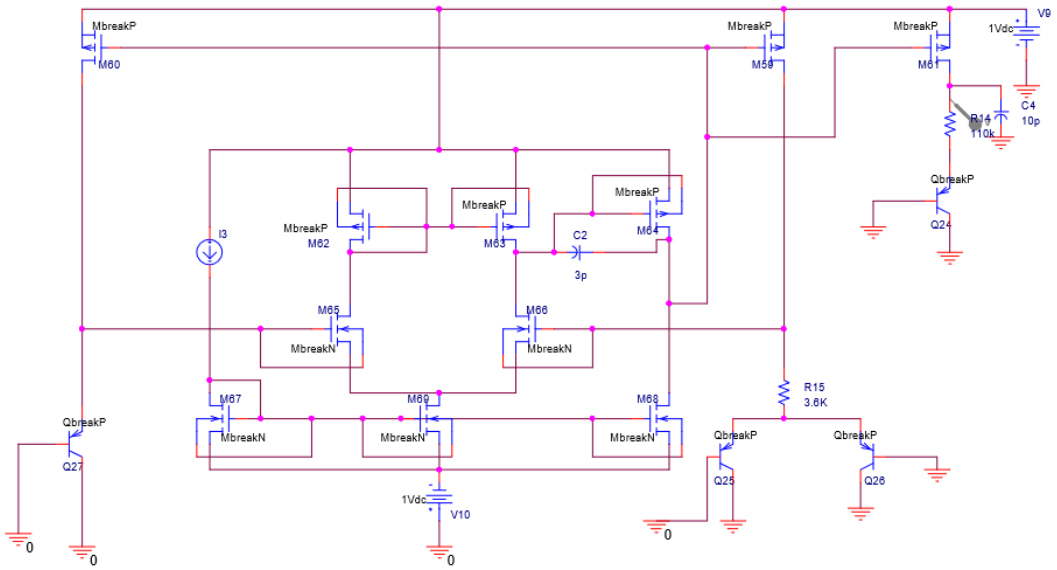

Figure 6.23: DTMOS BGR

Here, also like previous structures dtmos with its bias circuitry, it forms PTAT and the bjt at output forms CTAT. Thus in full it forms BGR. Because of power supply given 1 V it gives voltage below 1V that can be shown in fig 6.24 but the difference between extremes is of only 25 mV which is not observed previosly. Voltage at 0 degree is 0.960 V and at 100 degree is 0.935 V giving error of 4 and 6.5 % respectively.

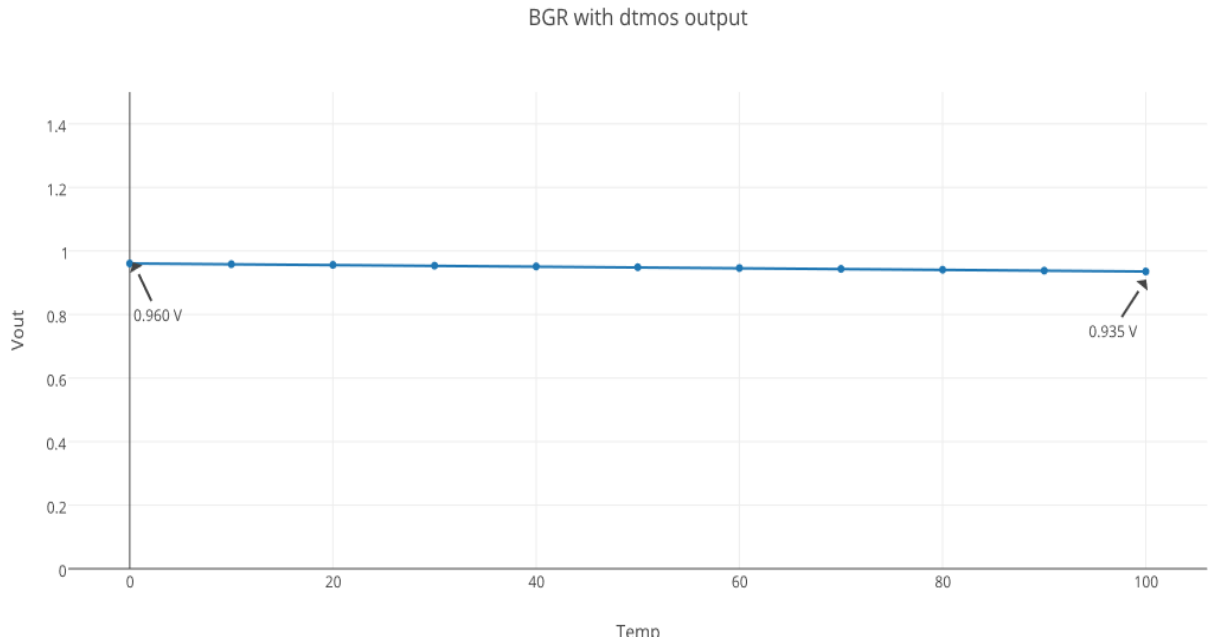

Figure 6.24: BGR DTMOS Output With Temperature Variations

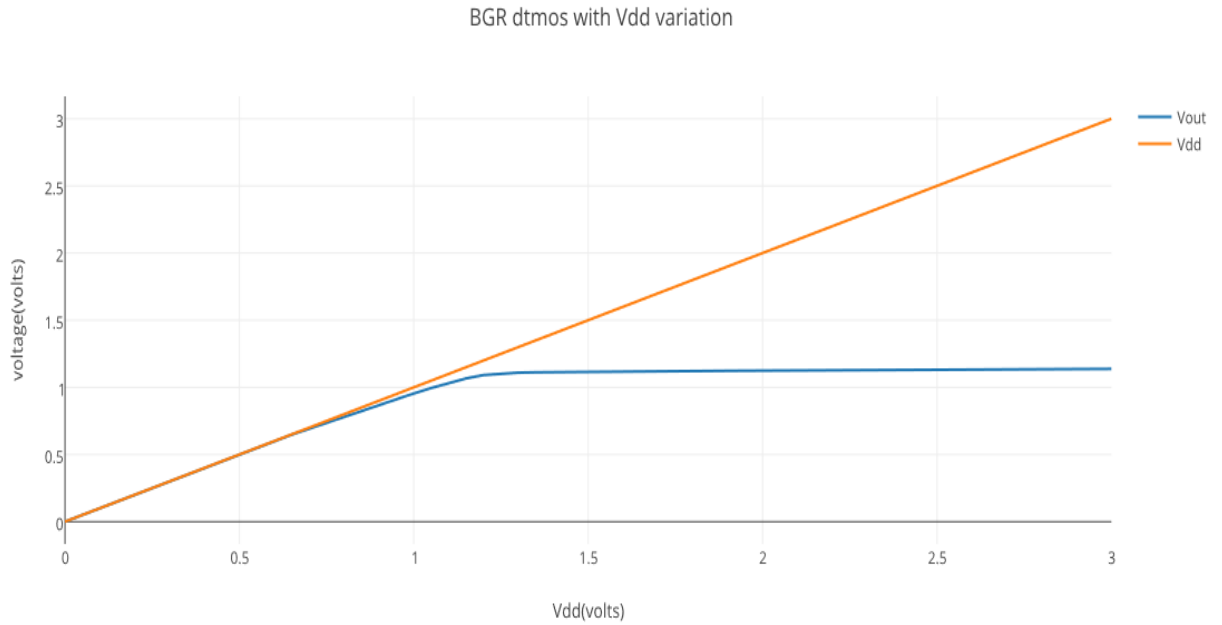

Figure 6.25: DTMOS BGR With VDD Variation

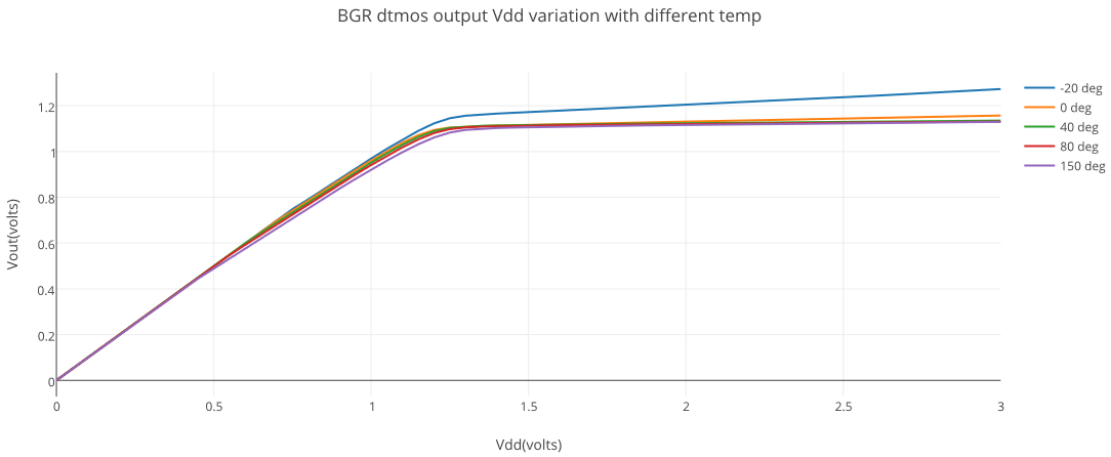

Figure 6.26: BGR DTMOS Output VDD Variation With Different Temperatures

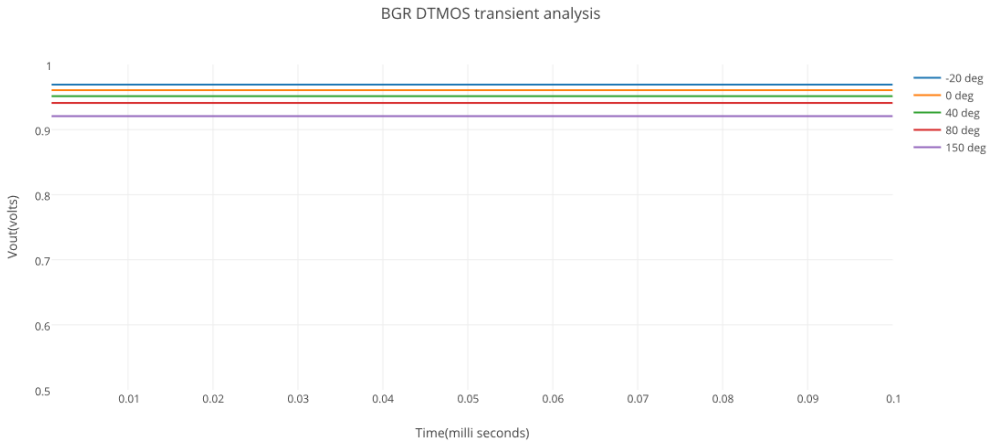

FIGURE 6.27: BGR DTMOS Transient Analysis At Different Temperatures

Fig 6.25 and 6.26 are Vdd and time variation at different temperatures are there respectively. There is no such change infact in fig 6.26 we can see it saturates much before 1.5 V which was not observed in any case. And in fig 6.27 we can see there is no diffrence of temperature in transient of output signal.

CHAPTER 7

CONCLUSION & FUTURE WORK

In this work, effort is made to understand the basics of Bandgap Reference Circuit and the limitations of conventional BGR are identified that why it is difficult to be used for low supply voltages. The conventional BGR gives output voltage as 1.23 which is equal to bandgap of silicon and hence limited for low supply voltage circuits.

Fig 6.19 shows the output voltage variation with the temperature giving 1.184 V at 0 degree and 1.112 V at 100 degree yielding 1.33% and 7.3% but in mid band it gives a real constant value. Fig 6.20 shows the variation of this output voltage at different values of V_{dd} it also gives the output of 1.2 V but it saturates before 1.5 V of V_{dd}. Fig 26 shows variation of V_{dd} and variation of temperatures simultaneously thus we can say that the value is almost constant near 1.2 V.

Fig 6.23 shows the modified version of 2 stage cmos op amp where we have used dtmos, with dtmos added advantage of low power and low values of bias and supply voltages is there. Thus static and dynamic power dissipations are really low. Voltage at 0 degree is 0.960 V and at 100 degree is 0.935 V giving error of 4 and 6.5 % respectively.

Table 7.1: Comparison Of All The Variants OF BGR

BGR CIRCUITS	ERROR AT LOW TEMPERATURE	ERROR AT HIGH TEMPERATURE	SATURATION POINT OF OUTPUT VOLTAGE
BASIC BGR CIRCUIT	5.83%	1.25%	1.75V
BGR USING OPAMP IC 741	0.67%	6.67%.	1.5V
BGR USING 2 STAGE OPAMP	1.33%	7.3%	1.5V
BGR USING DTMOS BASED OPAMP	4%	6.5 %	1.22V

Basic BGR circuit and BGR using OPAMP IC 741 simulations are not shown in this thesis

Thus, the circuit can be designed using lower voltages and lower current consumption to give low output voltage and consuming less power.

As future work, I intend to analyse the effects of fabrication process and noise on the proposed Op amp based bandgap reference circuit. Then optimize the circuit for noise protection and load variation as well as fabrication process effects. Moreover, I intend to carry the post layout simulation and study the effect of parasitic elements on the performance of circuit and later design the chip

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