LC LADDER BUTTERWORTH FILTER DESIGN USING VOLTAGE DIFFERENCING TRANSCONDUCTANCE AMPLIFIER

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CERTIFICATE

This is to certify that the dissertation title "LC LADDER BUTTERWORTH FILTER DESIGN USING VOLTAGE DIFFERENCING TRANSCONDUCTANCE AMPLIFIER" submitted by **Ms. Sangita Sarkar, Roll. No. 2K16/C&I/17** in partial fulfillment for the award of degree of Master Of Technology in "Control and Instrumentation(C&I)", run by department of Electrical Engineering in Delhi Technological University during the year 2016-2018, is a bonafide record of student's own work carried out by her under my supervision and guidance in the academic session 2016-2018. To the best of my belief and knowledge the matter embodied in dissertation has not been submitted for the award of any other degree or certificate in this or any other university or institute.

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DECLARATION

I hereby declare that all the information in this document has been obtained and presented in accordance with academic rules and ethical conduct. This report is my own work to the best of my belief and knowledge. I have fully cited all material by others which I have used in my work. It is being submitted for the degree of Master of Technology in Control and Instrumentation at Delhi Technological University. To the best of my belief and knowledge it has not been submitted before any degree or examination in any other university.

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ABSTRACT

This paper deals with the LC ladder Butterworth filter design using VDTA. As we know, there are many approaches to realize the LC ladder filter. We have adopted the element replacement method where the inductor in the LC ladder filter is replaced by the active element, i.e. VDTA as inductor cannot be realized physically due to its large size and other complexity associated with it. The non-ideal effect of VDTA is also taken into consideration. The LC ladder filter has an excellent feature of having low sensitivity to parameter variation and Butterworth filter has the maximally flat response in its pass-band so the attenuation or ripple is very less. So, these filters combine the advantages of both features. Here, I have realized low-pass, high-pass, band-pass and band-stop filters using VDTA. Its response curve is observed and transient response of output input has been checked to see the proper working of the filters designed. I also realized the inductor, floating and grounded both, and after checking its inductive equivalent characteristics, then I used it in the main filter design. The power consumption and THD% is also checked in simulation.

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LIST OF ABBREVIATIONS

VDTA - Voltage Differencing Trans-conductance Amplifier

g_m - Trans-conductance gain

Z_{in} - Input Impedance

OTA - Operational Trans-conductance Amplifier

MO-OTA- Multiple Output Operational Trans-conductance Amplifier

VC-Voltage Conveyor

CC- Current Conveyor

DCVC+ - Differential Current Voltage Conveyor

CCII – Second Generation Current Conveyor

DO-CCII- Dual Output Second Generation Current Conveyor

CDBA- Current Differencing Buffered Amplifier

CDTA-Current Differencing Trans-conductance Amplifier

FDNR-Frequency Dependent Negative Resistor

OTRA- Operational Trans-resistor Amplifier

SFG- Signal Flow Graph

L_{equ} – Equivalent Inductance

CFTA- Current Feedback trans-conductance Amplifier

CFOA- Current Feedback Operational Amplifier

OPAMP- Operational Amplifier

FI- Floating Inductor

GI- Grounded Inductor

OMA- Operational Mirrored Amplifier

R- resistor

L- inductor

C- capacitor

I_{in} –Input Current

V_{in}-Input Voltage

CCCII- Current Controlled Conveyor II

Biquad – Biquadratic Filter

CHAPTER – 1

INTRODUCTION

1.1. INTRODUCTION

We use filters generally [1] to select a particular frequency band or reject a particular frequency range. Voltage mode and Current mode filters are getting popularity as it has an excellent feature in terms of low power consumption, less circuitry, less complexity, larger bandwidth and wide dynamic range and linearity. Some of the current mode active building blocks are Current conveyors [2] which combines all three generations and Current Feedback Operational Amplifier.

In past years, many new active building blocks have been introduced which has brought revolution in terms of using less number of components used and also all the other parameters what a designer should take care of to have a performance of good quality. But still there are need of realizing new active building blocks to meet the requirements and specification what a designer is looking for while designing filters and also the advantages in terms of all the features listed above, are also being considered.

Now a days, researchers are giving emphasis on Current Mode Active Building Block as it has overcome the problems associated with the Voltage mode filter design in terms of Bandwidth and slew rate. So, many new prototypes of active building blocks have come into existence in analog filter design, design of sinusoidal oscillator or multi-vibrators. The proposed circuit is basically working on the current mode where the source is the voltage mode based.

The thesis is basically on the analog active block VDTA and how it can be used for LC ladder filter design. VDTA is generally operated at low voltage. In electronic integrated circuit and mobile communication system, it is desired to have a circuit that will exhibit high speed, low power consumption and the ideal performance. So, the analog designers are

trying to design filters to fulfill aforesaid features using LV methodology. The proposed circuit is basically having bulk CMOS driven architecture.

1.2. ORGANIZTION OF THESIS

The thesis is organized as follows:

Chapter one presents the overall introduction regarding the project and offers overall summary regarding a number of the active building blocks. This additionally consists of the objectives of the thesis and organization of the thesis work.

Chapter two presents the literature review that is on the previous work of the research scholars in the relevant field. VDTA is utilized in this thesis for realizing different kind of LC ladder Butterworth filters. This Chapter additionally introduces works outlined to this point.

In Chapter three, the new architecture of Voltage Differencing Trans-conductance amplifier is discussed and DC transfer characteristics of VDTA is also presented. The CMOS implementation is also given here.

In Chapter four, it is focusing on synthesis of floating and grounded inductor that is going to be utilized in LC ladder filter simulation. I adopted the element replacement methodology in simulation of LC ladder filter in which we have a tendency to exploit the idea of gyrator.

In Chapter five, it focuses on the main thesis work i.e. the simulation of various sort of LC ladder Butterworth filter (3rd , 4th , 5th, 6^{th} LC ladder low-pass, 6^{th} order high-pass filter, 8^{th} order band-pass and 10^{th} order band-reject filter). This chapter presents different analysis of the proposed filters.

In Chapter six, the conclusion and future scope are discussed. Different methodologies, which are being adopted and how these methods are having an effect on different parameters of the filters such as noise and also non ideality of the filter, is mentioned.

1.3. STATE OF ART

Due to disadvantages of standard inductors that were utilized in past decades, active element-based inductor came into existence. Throughout the previous few years or say decades, different floating inductors are simulated using different active building blocks. That's the explanation behind replacement of standard inductors by synthesis of passive LC ladder filters. These filters have a unique feature of low sensitivity to parameter variation.

Current conveyors are basically used in analog signal processing in current mode. It was first introduced in late 60's [5]. After some time, second generation current conveyor came [6], and in the middle of 90's, third-generation current conveyor came into existence [7]. Current conveyors have an excellent performance as an amplifier, used in current mode in analog signal processing. These current conveyors gained much popularity compared to the conventional op-amp. It is useful for amplifiers as it does not require high precision passive components and it has the better performance in terms of gain, response, speed, bandwidth and accuracy. In recent year with the growing diffusion of current mode approach as a way to design LV LP circuits, current conveyors have gained an increased popularity.

The necessity of the emergence of a current conveyor, having more than one output, current conveyor with light-emitting diode leads to the invention of DO-CCII (Dual-Output CCII), which is the combination of both positive and negative second generation current conveyors, as it gives the z terminal current in both direction [8]. If each current has identical polarity, the device are essentially leads to the fabrication of Current Follower CCII,(both p and n type wherever p or n symbolizes positive or negative current conveyor) [9]. Other variety is the Differential Voltage Current Conveyor [10], these devices is flexible to be used in any mode of signal processing, be it current mode, voltage mode or mixed mode.

Operational Trans-conductance Amplifier (OTA) [11] falls below one of the mostly used active parts, employed for on-chip module fabrication of filters that exhibit excellent frequency response. This device is essentially a device that based on voltage source and

generates signal in the form of current. Electronic tune-ability can be achieved by adjusting trans-conductance value.

Recently, Multiple Output Operational Transconductance amplifier abbreviated as MO-OTA has been come into existence. It is a replica, described by bipolar OTA and this is very useful for the design of bi-quad filters [12], [13]. But, the shortcomings of these element implementations aren't stressed. Many of such factors have been mentioned in [14]: But, these elements have high sensitivity to the matching error constraints in comparison to those of the conventional ones.

The voltage conveyor (VC) has come into existence in 1981 [15], in the documentation of current conveyors, all varieties of voltage conveyors have been discussed in [15], [16], [17], [18]. The one of the popular Voltage conveyor is positive differential current voltage conveyor (DCVC+) [19] that's usually referred as differentiated and buffered current type of amplifier termed as Current Differencing Buffered Amplifier (CDBA) [20].

By introducing some of changes in CDBA or substituting Voltage Follower by the OTA [21], CDTA has been published [22].

A change has been made on the already existing active building blocks to consider changes in the voltage at the input terminals instead of considering the current, which leads to the introduction of VDTA [23].

Recently, many works were proposed regarding passive ladder filter simulation via employing different active elements discussed so far. Direct simulation by adopting replacement method of either inductor or capacitor by synthesizing it by some of the active block, wave active filter using scattering phenomenon and indirect simulation via Bruton’s frequency transformation of passive resistively terminated LC block and its further approach to FDNR implementation, which leads to leap-frog structured filter, is used to realize LC ladder filter.

In such circuits, active parts used are CDBA [24-26], Current Amplifiers [27], Multi-Output CCCIIs [28], CDTAs [29-31], OTRAs (Operational Trans-resistance Amplifier) [32], Differential Voltage Current Conveyor [33], Second generation current conveyors and

current feedback amplifier [34], [35], DO-OTA (Differential-Output OTAs) [36], MO-OTAs (Multiple-Output OTA) [37], and a combination of conventional Operational Amplifiers and Operational trans-conductance amplifiers [38]. The disadvantage it has is that it leads to the complexity in circuitry. The filter may have a bulk number of components to realize the floating or grounded immittance synthesis technique, which only adds to the complexity to the proposed filter. This problem can be overcome using CBTA to exploit ordinal order of ladder filter realization [39], [40].

The above discussion clearly states crux of simulation of ladder filters exploitation in such a way that it will employ active blocks that might encourage artificial synthesis of passive elements (inductors in most of cases). Throughout this thesis, VDTA is implemented to synthesize the inductor in artificial way, then it is used in LC ladder filter implementation.

1.4. THESIS OBJECTIVE

1. To outline VDTA (Voltage Differencing Trans-conductance Amplifier) for the effective synthesis of filter simulating LC ladder structure. The CMOS implementation of VDTA is adopted and its DC transfer characteristic is determined.

2. The second aim is to perform synthesis. The thesis deals with LC ladder simulation on the principle of element replacement by artificial electrical device (GIC is used basically in this case where GIC is realized with the help of VDTA and in GIC, the input resistance is inversely proportional to the load impedance). The floating inductor is synthesized via newly introduced VDTA that is intended in the first part of the thesis. All the methods are cross-checked in two steps: in the beginning, the theoretical analyses are done . To verify the complicated behavior of the projected circuits, PSPICE simulations are performed in PSpice AD, utilizing transistor-level models of active parts (CMOS during this case). For this,

DC transfer Characteristics are observed and tested with PSPICE to verify the theoretical results with the simulation ones. For all the filters that are simulated in this thesis work, the calculation part is done to get the required cutoff frequency, and it's then matched with the simulation result to envision the error. Our objective is to have the error to be smallest. In filter synthesis, the result of attenuation in the pass-band is taken into account to have the ripple as low as possible so the LC ladder filters, employing the inductor synthesized by VDTA, showing the low sensitivity to component tolerances that is our prime goal to get.

3. To get the proposed floating and grounded inductor that is utilized in LC ladder implementation. For this it's expected to verify whether or not the synthesized component works as inductor or not. It is verified by the behavior of its reactive behavior with the change in frequency. The inductive behavior of the synthesized part by active element can be verified by using it in a RLC circuit in the place of inductor and obtaining its frequency response, that is ought to be just like that of a band pass filter with the desired center frequency and bandwidth.

CHAPTER-2

LITERATURE REVIEW

2.1. INTRODUCTION

Different strategies like element replacement method (it is either synthesized resistance, inductance or capacitor) and wave technique (where scattering parameters are thought of to imagine voltage and current as wave) are prototyped for his or her active LC realization. In the first procedure, a symbolic graph (SFG) is intended from the relationship between voltage and current of this epitome ladder. Lossy and lossless, both type of integrators are used to implement SFG simulation. Lossless integrators is troublesome to comprehend, owing to non-ideal parasitic effect resulted from already used active and passive elements. The complexness of the structure will increase because the order of filter will increase. In the second procedure, part substitution method, the inductors of the filters are substituted by resistance or capacitive simulators using blocks like voltage differencing trans-conductance amplifier (VDTA) [49], current follower trans-conductance amplifier (CFTA) [50] and current backward trans-conductance amplifier (CBTA) [51] and so on. The requirement for floating capacitance in the synthesized filter topology makes the performance of the filter not appropriate in high frequency. In wave filter technique [52,53], that is that the third technique, filter realization depends on the representation of incident and reflected voltage wave that is resolved by explanation and determination of scattering matrix. Every part of element of filter is substituted by its equivalent wave form. The benefits of aforesaid method are—the filter module is standard in design. It also employs solely measuring device that is not lossless in nature. There are options that have light-emitting diode. Researchers want to implement wave active filter structure using different active components. Amplifiers [52, 53], operational trans-conductance amplifier (OTA) [54], CFOA [55], DVCCTA [56], DVCCCTA [57], CCDDCCTA [58], OTRA [59], VDTA [60] are used to design higher order filters being supported by this approach.

Most of the works of LC ladder filter in the literature is subjected to the first design technique adopted by Darlington, Cauer, Bader etc., which might be delineated as follows: ranging from a driving-point resistance of respective LC two-port network or another equivalent demonstration, remove low-order realizable lossless sub-networks. Every sub network is employed to comprehend a selected transmission zero. The strategy of extracting a sub network typically is predicated on the name of the transmission zero that is being extracted. Once every extraction step is finished, the rest resistance is achieved. The entire method is being perennial till the rest resistance becomes exhausted.

2.2. DIFFERENT RESEARCH METHODOLOGIES FOR LC LADDER FILTER

2.2.1. LC LADDER FILTER SIMULATION USING ELEMENT REPLACEMENT METHOD

Element replacement technique is often performed with the help of three methods:

1. Using Gyrator (General Impedance Converter abbreviated as GIC)
2. Gorski-Popiel's Embedding Technique
3. Bruton's FDNR transformation technique

Element replacement technique is performed by replacement of the inductance which might not be realized physically due to its large size and different difficulties that emerge beside it. It is often done either by using Gyrator, where the load resistance is inversely proportional to the supply resistance. Thus, if we use capacitor at the load, we'll get the inductive resistance at the supply terminal. Another approach is FDNR, where we tend to perform scaling of the transfer function by s (simply by dividing) and thereby get the Frequency Dependent Negative Resistance (FDNR), which is realized by VDTA.

A few years back, Reddy [61] presented, which is said to Hilberman's theorem [62], two lossless FI circuits that used 3 op amps. After some times, in [63], Rathore and Singhi

introduced a method to synthesize general floating impedances. Recently, GRM [64] has been devised subjected to adopting FI configuration.

Many approaches are adopted to simulate floating, grounded and FDNR.

Floating and grounded inductors are realized using many different approaches. I adopted the approaches depicted in [65], [66], [67].

The inductances, each floating and grounded are realized. Conjointly, the non ideal implementation of the inductors is also taken into consideration.

2.2.2. GYRATOR

The gyrator, or could also be termed as positive resistance electrical converter, could be a terribly enticing development enforced on two-port, as a result of it are often adopted to simulate inductance. Its image and transmission matrix is represented in Fig. 3.3. This definition of gyrator through its transmission matrix, with $g_1 \neq g_2$ and positive, denotes the active gyrator. However, if $g_1 = g_2 = g$, it refers to the gyrator of having passive two-port. Clearly, the gyrator could be a unreciprocated two-port device, since

$$a_{11}a_{22} - a_{12}a_{21} \neq 1 \tag{2.1}$$

It is necessary for network synthesis from the side that, if it's terminated at port two by a capacitance C_L, the resistance are often seen on port one, consistent with atomic weight. (2.2), is

$$Z_i = G_b s C_L = s\frac{C_L}{g_1 g_2} = sL_{eq} \tag{2.2}$$

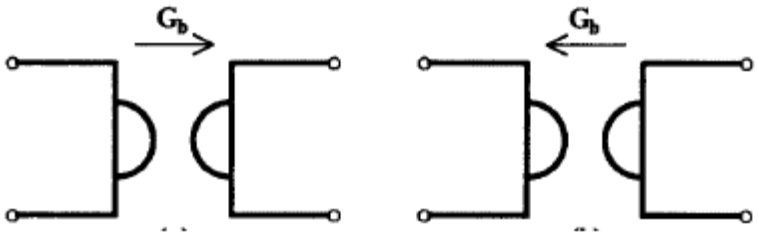

Fig.2.1. Gyrator [92]

i.e., the resistance of a similar inductance is given as

$$L_{eq} = \frac{C_L}{g_1 g_2} \tag{2.3}$$

The gyrator is often synthesized using totally different active building blocks. There are several approaches being adopted to simulate inductance. A perfect negative-impedance invertor (Lundry type) that uses a voltage-controlled voltage supply is outlined. This is configured using an operational amplifier in [68].

It's utilized in a mixture of negative-impedance convertors to implement new gyrator circuits. An alternative configuration for a gyrator that is realized from 2 commercially available trans-impedance operational amplifiers (OPAMPs) and three passive elements that is described in [69].

A new resistive capacitive circuit which is active in nature is depicted to get implementd. Floating inductance which is lossless in nature in [70] realized using three opamps as gain summers having magnitude equal to one, three resistors and one capacitance. In contrast to different 3 amplifiers, the new circuit realizes inductance that's controlled through one resistance.

OTA based implementation of inductance is represented in [71]. The parasitic result and open loop information is being taken into account. OTA-based inductance which might be thought of to be each grounded and floating topologies is depicted as shown below in Fig 2.2.

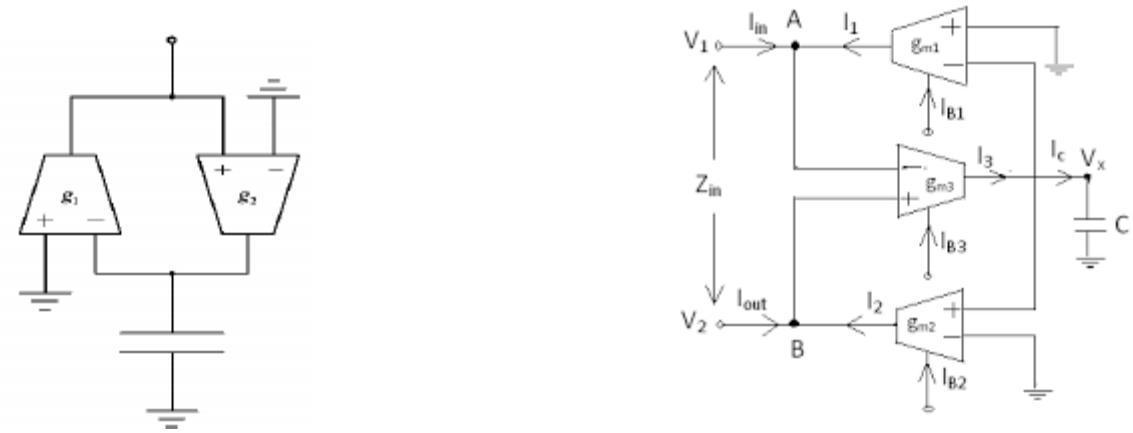

Fig.2.2. OTA Based Inductor [71]

In [72], two structures for realizing inductance, capacitance and frequency-dependent negative resistance (FDNR) simulators (all are floating type), simulated by the passive elements , are being introduced. This can be done by employing the active building block namely modified current feedback operational amplifier (MCFOA). This requires also a very few number of passive components to realize the filter. Proposed floating inductor and Farm Credit System employ a capacitance (basically grounded one) therefore the proposed circuits suited to completely computer circuit (IC) design. Also, the projected circuits does not need any reasonably important passive element matching conditions, therefore reduces matching error and/or cancellation constraints.

Four operational mirrored amplifier (OMA) based floating resistance configurations are presented in [73] that use a minimum range of (three) OMAs in contrast to four OMAs depicted in the antecedently documented circuits, having all advantageous features over its earlier implementation using four OMAs.

Three newly published active RC artificial FIs is described in [74] that depicts lossless floating inductance and series and parallel RL resistance, using current conveyors of second generation (CCII) as major components for this purpose. The unique key-points of this newly introduced prototype is stated as under

1. It is distinctive to already existing typical op-amps for floating inductors, the prototype mentioned in the above discussion don't ought to select element matching to obtain the required realization;
2. All the circuits that have been introduced in the past and also in recent times, the magnitude of inductance is controlled by varying one resistance. Thus electronic tunabilty and suppleness are often obtained.
3. These circuits employ a very few number of passive elements (generally 2 resistors and a capacitor). Therefore, the circuit complexity is less.

2.2.3. LC LADDER METHODOLOGIES

The objective of the thesis is to simulate LC ladder filter using VDTA. Apart from VDTA, several approaches are done so far using totally different active building block to simulate LC Ladder Butterworth Filter. In [75], the idea of LC Ladder Filter using OTA has been projected. This contributes to a unique feature to reduce noises for the applications which is operated at high frequency to own a better performance.

The step by step procedure for synthesizing low-pass and band-pass ladder filters having leapfrog structure is bestowed in [76]. The projected design uses 2 typical active elements, i.e., employing op-amps and a Current Controlled Conveyor II (CCCII), which does not comprise of any reasonably external passive part.

In [77], Operational Trans-Resistance amplifier (OTRA) based implementation of LC-ladder filter is mentioned. This projected configuration uses a technique that is taken into account to be a scientific approach to the design of LC-ladder filter having leap frog structure. Operational trans-resistor amplifier is essentially an active element having low resistance at both input and output ports. This energized part is often chosen for realizing voltage output filter.

An insight into Butterworth Filter is bestowed in [78] where four parameters in an elaborated way is mentioned i.e. attenuation in pass-band, attenuation in stop band and frequency at which passing and stopping of signal happens.

Switched capacitance filters are being used to simulate LC Ladder Filter as mentioned in [79]. The LC ladder works on primarily by extracting LC network from research tables and reworking it into a similar switched capacitance configuration. It has the advantage is that it has least sensitivity to method variation, however has the disadvantage that it's difficult to design a filter that's not delineated during a look-up table. The strategy is widely used owing to its doubly terminated terminals with resistors. LC ladder structure that focuses on its behavior with respect to the pass-band magnitude sensitivity, though it is observed that this quite often goes beyond normal range by sensitivity in terms of phase i.e. the variation due to the phase change is not of good quality.

Another technique for doubly resistive terminated ladder filters synthesis was bestowed in [80]. Constantinides and Dimopoulos proposed a new method that is predicted on the implementation of voltage mode instead of current mode to realize doubly resistive terminated LC ladder filters. There are a variety of realizations of passive components adopting another technique which are discussed. An elaborated illustration of a 3^{rd} order low-pass filter has been done with the proposed technique and comparison is made with the ideas proposed by Rathor and Khott.

In [81], discussions are made on a scientific approach for designing a wave active filter realization employing voltage differencing trans-conductance amplifier. This structure does not need the use of any resistor. This proposed filter employs only a capacitance that is grounded and conjointly having the feature of electronic tunability of cut-off frequency just by adjusting bias current.

In [82], a scientific technique for explaning the RLC filter has been proposed; which is CFOA based filter employing capacitors. All capacitors are grounded. This filter is useful in current mode analog signal processing. It is based on the operational simulation of filter

where we are more interested in modeling circuit equations and the voltage current relationships of the element. This approach basically focuses on the operation rather than its components. This method can also be utilized in realizing LC ladder filter operated in voltage mode. These filters use a very few number of capacitors that contributes to very less amount to the total capacitance. Such filters are very useful for the design of IC circuits and also contribute to the design of computer architecture.

In [83], it represents a simplified scattering synthesis procedure and its application within the development of a bug for synthesizing LC ladder networks. The new approach relates to the scattering transfer matrix theory that has never been applied earlier to ladder synthesis technique. The primary step during this synthesis procedure is trying to find the determination of a scattering synthesis strategy for choosing the sequence of extracting transmission zero.

In [84], another synthesizing technique is taken into account to simulate LC ladder filter in leap frog structure. The incorporation of general simulations of LC ladder networks offers matched correspondence between reactive components, thereby reducing matching error related constraints. This is achieved by maintaining integrators by introducing special type of “port reciprocators” that depicts the active parts that can be depicted by signal flow graph procedure and a variety of thumb-rules to interconnect the elements constructs a whole active synthesis technique.

In [85], another replacement frequency technique is introduced that is taken into account to be a compensation technique of the second generation current conveyors, that is used to synthesize floating inductor. To obtain the desired electronic tunablility of the proposed inductor, a trans-linear CCII is employed where its series parasitic resistance at its X terminal is being compensated to reduce the non-ideality of the filter. After getting the desired frequency characteristics of this prototype, some restrictions have been imposed on frequency of the conventional second generation current conveyor based simulated adjustable floating type of inductor, that doesn't depend upon standardization current, is being analyzed. To root out this drawback, a pole or zero cancellation technique has been

adopted. Hence an external resistor of 650Ω has been used in series and it outlined a negative resistor, suggested by that of the current conveyors. Simulation results exhibit that this cancellation method enhances the standardization range of varying proposed inductor. Moreover, a special arrangement is presented so the cancellation method isn't sensitive to the fluctuation of current that's used for standardization the inductance value.

In [86], some work has been done for having relation between magnitude and phase sensitivity, that is a prime tool to measure in a qualitative manner to see how these parameters have an impact on element variation and parasitic loss due to non-ideal phenomenon associated with the circuit, that may have an effect to get a deviated response from the nominal filter response.

In [87], the popular leap frog structure was no more found useful in designing LC ladder filter as it has the finite range of transmission zeros. This design was having some drawbacks in the application of the strategy to comprehend high pass and band stop filters. Hence, these issues are often sorted through the active RC filter synthesis technique, that is predicated on emulating mesh current of RLC ladder filters. In this work, a singular relevance model that incorporates coupled feed-forward Tow-Thomas bi-quadric filter is adopted. This design has been used to simulate all categories of LC low pass and high pass ladder filters. All type of filters can easily be realized just by applying the frequency transformation technique implemented on the nominal low pass filter prototypes and frequency scaling are performed afterward to get the frequency range for which the filter is expected to operate.

In [88], a widely known leap frog structure has been projected to simulate LC ladder filter by using MO-CCCII and grounded passive capacitors. Electronic tunability is taken into account and matching constraints is not taken into account for the design part.

CHAPTER-3

VOLTAGE DIFFERENCING TRANSCONDUCTANCE AMPLIFIER

3.1. INTRODUCTION

Active parts have a widespread use in signal processing in analog domain, adore filters design, resonators modeling, oscillators and inductance synthesizing etc. Several active parts were used for this purpose due to the fact that they're having vital options with relevancy one another, adore i/p and/or o/p terminal having similar or dissimilar options, any of the parameters will be controlled by the adjustment of external voltage or current etc. New approaches are being proposed by researchers with these newly introduced active parts. At present, active parts are being considered under review and several other new parts are being enforced and synthesized. However, the implementation of the newly introduced active parts doesn't seem to be declared. One amongst those newly introduced active parts is VDTA. It may be compared with its typical current mode counterpart, Current Differencing Transconductance Amplifier, where the input is considered to be current signals. CDTA is an antecedently projected non-passive element. In CDTA, difference of input currents (I_p, I_n) is translated to a proportional current via first transconductance g_{m1} at Z port. In VDTA, in the place of input currents, difference of input voltage (V_p ,V_n) is being considered. These voltages applied at input terminal is translated to current at the terminal Z by multiplying the difference of voltage with 1st trans-conductance gain g_{m1} and therefore proportional voltage produced at the terminal Z (due to the current at Z terminal) is copied to current at the terminals X+ and X- ports by multiplying it with second trans-conductance gain (g_{m2}). The trans-conductance can be varied by changing external bias currents. If comparisons are made, alternative non-passive building blocks, the advantages VDTA is having is that it offers two completely different values of trans-conductance so many applications like design of bi-quad filters (e.g, KHN Biquads, Tow-Thomas Biquads), oscillator, inductance and FDNR (frequency dependent negative resistor)

circuitry will be made with the help of one active block using one or two capacitors. In alternative words, these implementation need less range of passive parts thereby reducing the circuit complexity and additionally helps in reducing power consumption. Another advantage, this block has is that, it will be used simply at trans-conductance mode applications which implies that voltage is applied at the input terminal and current is taken out from the output terminal. In this paper, an illustration has been stated to show how CMOS can be used to design VDTA. By choosing input terminal voltages, this formation or orientation of VDTA will generate any reasonably normal filter functions. No parameter matching condition is needed in this case.

3.2. VDTA(VOLTAGE DIFFERENCING TRANSCONDUCTANCE AMPLIFIER)

The voltage differencing trans-conductance amplifier (VDTA) is the main active block for designing proposed filter. It was introduced in 2012 by Yesil et al. Its symbol is illustrated in Fig.3.1. The input voltage at P and N terminals (V_P and V_N) are applied and then its difference is taken and it is copied to be current at z terminal (I_z) using 1st trans-conductance (g_{m1}). This trans-conductance is set as per the 1st input bias current (I_{B1}).

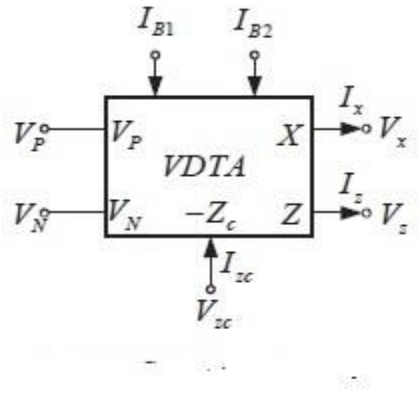

Fig.3.1. Circuit Symbol Of VDTA [89]

To make associated degree of extension to the employment of VDTA, the output current, specifically z copy terminal (Z_c) is employed. At Z_c terminal, (I_{zc}) is translated from current at z terminal. The voltage at z terminal (V_z), is translated to be current using second trans-conductance (g_{m2}) that is electronically adjusted by varied I_{B2}. As voltage being the input and current being the output, this active part is attributed to act as a trans-conductance amplifier. The voltage and current relationship at input and output terminal is shown by equivalent (3.1)

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \tag{3.1}$$

which refers to,

$$I_Z = gm1(V_P - V_N) \tag{3.2}$$

$$I_{X+} = g_{m2} V_Z \tag{3.3}$$

$$I_{X-} = -g_{m2} V_Z \tag{3.4}$$

As a consequence, the above describing-equations, the input stage and output stage will be merely employed by floating current sources. As per input terminals, the proportional output current at Z terminal is obtained. The intermediate voltage of Z terminal is then translated to output currents. In this paper, VDTA is thought to be an active analog building block, attributable to the subsequent reasons:

(i) The straightforward implementation of VDTA using CMOS,

(ii) There use of two trans-conductance amplifiers that offers resistance less realization,

(iii) The trans-conductance gain of VDTA which may be modified via varied bias current, thus providing the electronic tunability and suppleness to designed filter.

3.3. CMOS IMPLEMENTATION OF VDTA

The intermediate voltage at Z terminal is copied to output currents. The new CMOS implementation of the VDTA is shown in Fig. 3.2.

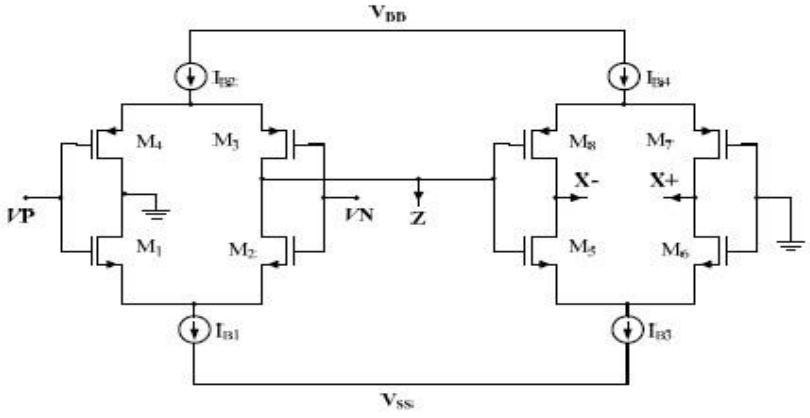

Fig 3.2. CMOS Implementation Of VDTA [89]

The above figure demonstrates the CMOS implementation of the VDTA block. NMOS M_1 and M_2 and PMOS M_3 and M_4 form the primary main active a part of VDTA. M_1, M_4, and M_3, M_2 forms the first CMOS differential amplifier. Another differential amplifier, that is identical to first differential amplifier by using NMOS M_5 and M_6 and PMOS M_7 and $M_{8,}$ is used. The circuit operation starts operating as follows: in the presence of CMOS differential amplifier, the output is obtained at port z, which is mainly due to the difference between the input signals at port p and port n. This is then amplified in the 1st amplifier. The output voltage obtained at port z is then taken to be fed into the secondary amplifier where one terminal that's grounded, guaranteeing that there's no loss in signal. Finally, the amplified output is taken out at port x+ and x-. With the help of differential input voltage, there's an increase in trans-conductance gain in the primary block i.e., g_{m1} gets magnified. There's associated degree of magnified feed of output in the secondary block, is largely due to the secondary trans-conductance g_{m2}, there's final increase in output current as a result of what finally offers associated degree of overall gain and signal amplification.

The newly introduced circuit uses two Arbel-Goldminz trans-conductance. Input and output trans-conductance parameters of VDTA part in the circuit is determined by the trans-conductance of outputs transistors. Associated degree approximation will be written as

$$g_{m1} = \left(\frac{g_3 + g_4}{2}\right) \tag{3.5}$$

$$g_{m2} = \left(\frac{g_5 + g_8}{2}\right)$$

Or,

$$g_{m1} = \left(\frac{g_6 + g_7}{2}\right) \tag{3.6}$$

where g_j is the transconductance value of *j*th transistor described by

$$g_j = \sqrt{I_{Bj}\mu_j C_{OX}\left[\frac{W}{L}\right]_j} \tag{3.7}$$

μ_j is (j = n, p) the quality of the carrier for NMOS (n) and PMOS (p) transistors, C_{OX} is that the capacitance between gate-oxide per unit space, W is that the effective channel-width, L is that the effective channel-length and I_{Bj} is bias current of j^{th} semiconductor.

3.4. VDTA REALIZATION USING OPERATIONAL TRANSCONDUCTANCE AMPLIFIER USING OTA

For the broad perspective, we need to understand the design of VDTA using OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) as shown in the 3.3.

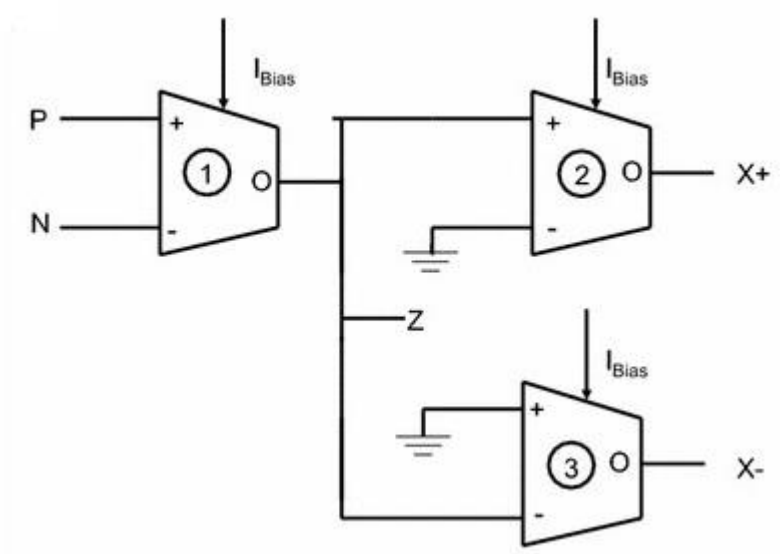

Fig.3.3. VDTA Realization Using OTA [89]

The output of the primary OTA is thought to be Z terminal of VDTA, current at which is proportional to the differential voltage applied to the non-inverting and inverting terminal of the OTA. This current at Z terminal creates proportional differential voltage that is fed to two alternative OTAs as inputs in second stage and eventually produces Ix+ and Ix- proportional to applied voltage. Throughout the structure, we must always take into account the biasing current that is provided to every OTAs to form the active building block to work properly.

3.5. TRANSFER CHARACTERISTICS

We perform the simulation by PSPICE AD program with TSMC CMOS 0.18μm method parameters. The aspect ratios of the CMOS transistors used in the design is given in Tab. 1.

Supply voltages are $V_{DD} = -V_{SS} = 0.9$ V and $I_{B1} = I_{B2} = I_{B3} = I_{B4} = 150$ µA biasing currents which are used. Simulation results depict that this selection yields trans-conductance values of VDTA to be $g_{m1} = g_{m2} = 631.8$ µA/V. The DC transfer characteristic of I_{X+} and I_{X-} against V_Z for final output stage of projected VDTA is shown in Fig. 3.4.

Transistors	W(µm)	L(µm)
M_1, M_2, M_3, M_6	3.6	0.36
M_3, M_4, M_7, M_8	16.64	0.36

TABLE 3.1. Aspect Ratios Of The CMOS Used In VDTA Implementation [89]

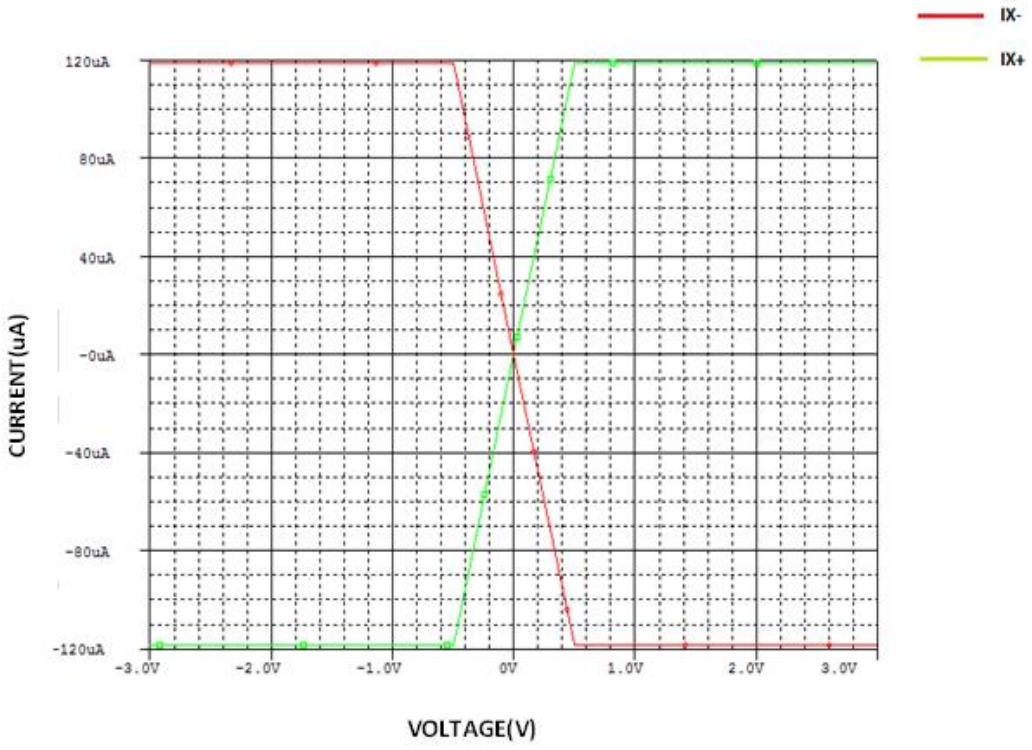

Fig. 3.4. Transfer Characteistics Of VDTA

CHAPTER-4

REALISATION OF GROUNDED INDUCTOR AND FLOATING INDUCTOR USING VDTA

4.1. INTRODUCTION

In this chapter, electronically adjustable lossless grounded inductance and floating inductance simulators using active building block Voltage Differencing Trans-conductance amplifier (VDTA) and one capacitor are synthesized.

One of the standard problems in designing frequency (RF) circuits is expounded to the idea of integrated inductors with high quality factor. It's okay with the fact that, using common semiconductor method, it also suffers from comprehending passive inductors that exhibit the same value of quality factor (e.g. Q>10) and high inductance value(e.g. a few nH) in the fabrication method.

Inspite of the many circuits and methodologies that were already presented and investigated, the term active (AIs) had appeared in the title in early 70's. Later, economical realizations of selective active filters on semiconductor, i.e., bipolar technology, were projected in 90's.

Many simulated grounded inductors (GI) and Floating Inductors using different active blocks consist of op-amps, CCs, CFOAs, FTFNs, CDBAs, CFTAs, however they suffer from following disadvantages:

1. Demand for additional variety of passive parts,
2. Needs additional variety of active parts,
3. Synthesized inductance is lossy.

Recently VDTA is introduced and it will be operated in each voltage mode and current mode applications. In the following discussion, we will have a review of some important works on grounded and floating inductance using Voltage Differencing Trans-conductance amplifier (VDTA).

4.2. GROUNDED INDUCTOR USING VDTA

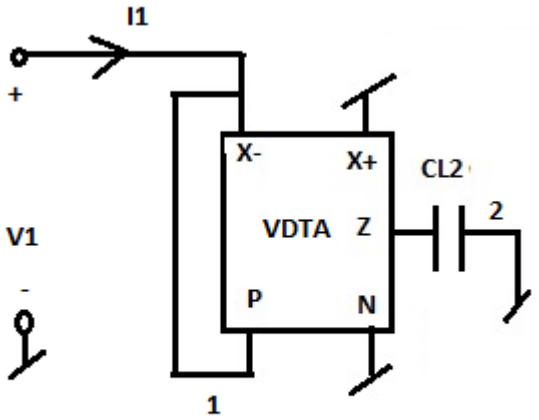

Fig. 4.1. Grounded Inductor Using VDTA [90]

The grounded inductance will be accomplished employing a single VDTA and a capacitor. [90].

We have to work out the input resistance of the circuit where V_1 is applied at terminal one. Applying KCL at node one, we have a tendency to get

$I_1 + I_x - = 0$

i.e.

$$I_x - = -I_1 \tag{4.1}$$

We know

$$Ix-= -g_{m2}V_Z \tag{4.2}$$

Therefore, $I_1 = g_{m2}V_Z$ (4.3)

Now,

$$Vz = \frac{Iz}{sC} \tag{4.4}$$

Therefore

$$I_1 = g_{m2}\frac{Iz}{sC} = \frac{gm1gm2Vp}{sC} = \frac{gm1gm2V1}{sC} \tag{4.5}$$

So the input impedance,

$$\frac{V1}{I1} = \frac{sC}{gm1gm2} \tag{4.6}$$

which is nothing but the expression for inductor,

Where

$$L_{Equ} = \frac{C}{gm1gm2} \tag{4.7}$$

Now the experiment is applied employing a 0.01nF capacitor, we are able to get the magnitude of grounded inductance as

$$L_{Equ} = \frac{C}{gm1gm2} = \frac{0.01nF}{\frac{631\mu A}{V}x627\frac{\mu A}{V}} = 25.27\mu H$$

The simulation of L_{equ} Vs Frequency is shown in Fig 4.2, wherever we have a tendency to get the inductance worth as 25.39 μH.

Error=

$$\frac{25.39 - 25.27}{25.27} x\ 100\% = 0.47\%$$

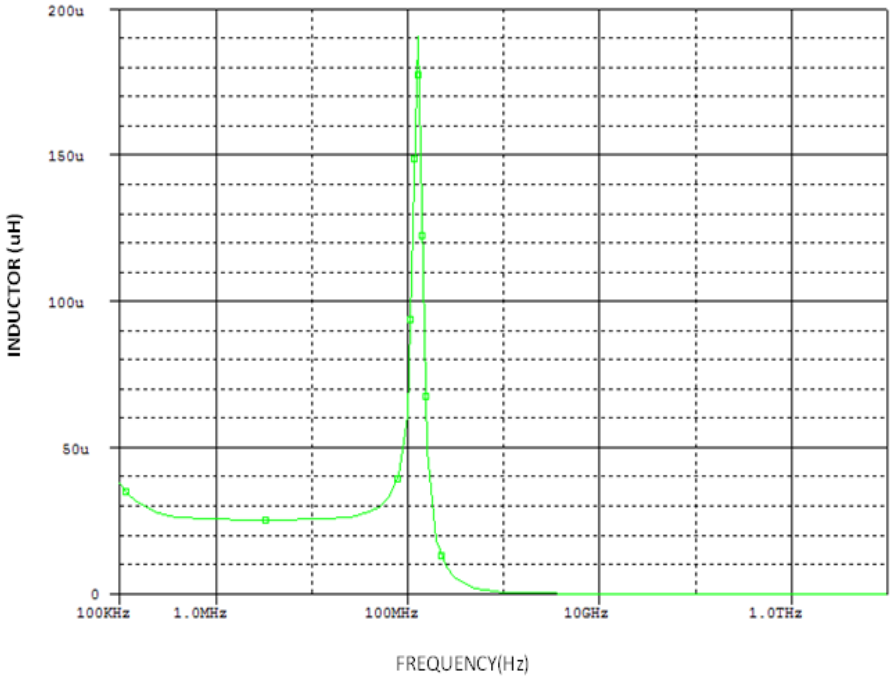

Fig 4.2. Inductor Vs Frequency for Grounded Inductor Using VDTA

Response of the new simulated inductors was verified by SPICE simulations. CMOS-based VDTA from was accustomed confirming the frequency responses of the grounded simulated inductors. The subsequent values were used for grounded inductor: C_{L2} =.01nF, $g_{m1} = g_{m2} = 631.7$ μA/V. From the frequency response of the simulated floating inductance (Fig 4.1), the inductance value remains constant up to 10MHz.

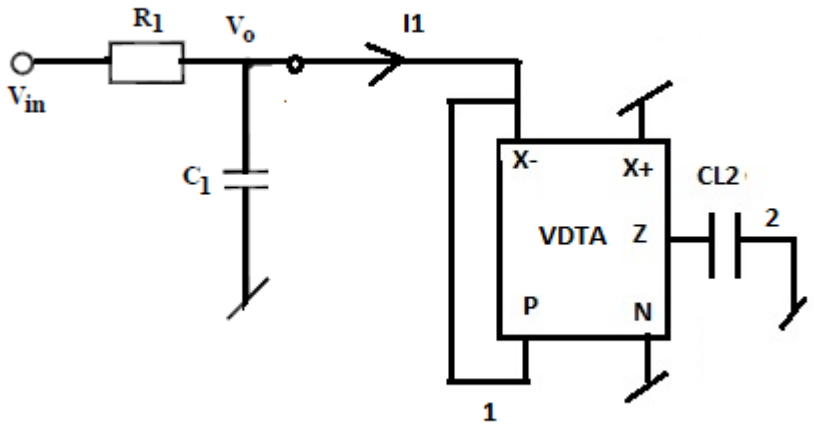

Fig 4.3. Band-pass Filter Using VDTA Based Grounded Inductor [66]

Here in fig 4.1, the L_{equ}= 23.27 μH as discussed earlier. Now the circuit will be behaved as the RLC circuit shown in figure 4.4, we can have similar circuit just by replacing the inductor by the simulated VDTA based grounded inductor as shown in Fig 4.3.

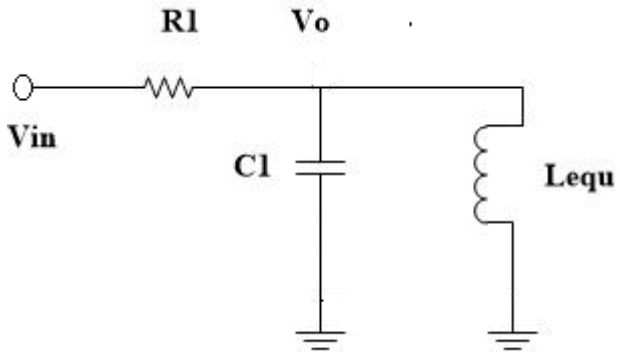

Fig 4.4. RLC Circuit

The Transfer Function of the circuit shown in Fig 4.4, will be,

$$\frac{V_o(s)}{Vin(s)} = \frac{\frac{1}{RC}\,s}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}$$

Where center frequency, $\omega_0 = \frac{1}{\sqrt{LC}}\ rad/sec$

Therefore,

$$f_0 = \frac{1}{2\pi\sqrt{LCo}} = \frac{1}{2\pi\sqrt{\frac{C_{L2}}{gm1gm2}C1}}$$

The theoretical value of the band-pass filter is calculated as 14.75MHz

By simulation as shown in Fig 4.5, we get 15.955MHz

So the error will be, $\frac{15.955-14.75}{14.75}x100\% = 8.16\%$

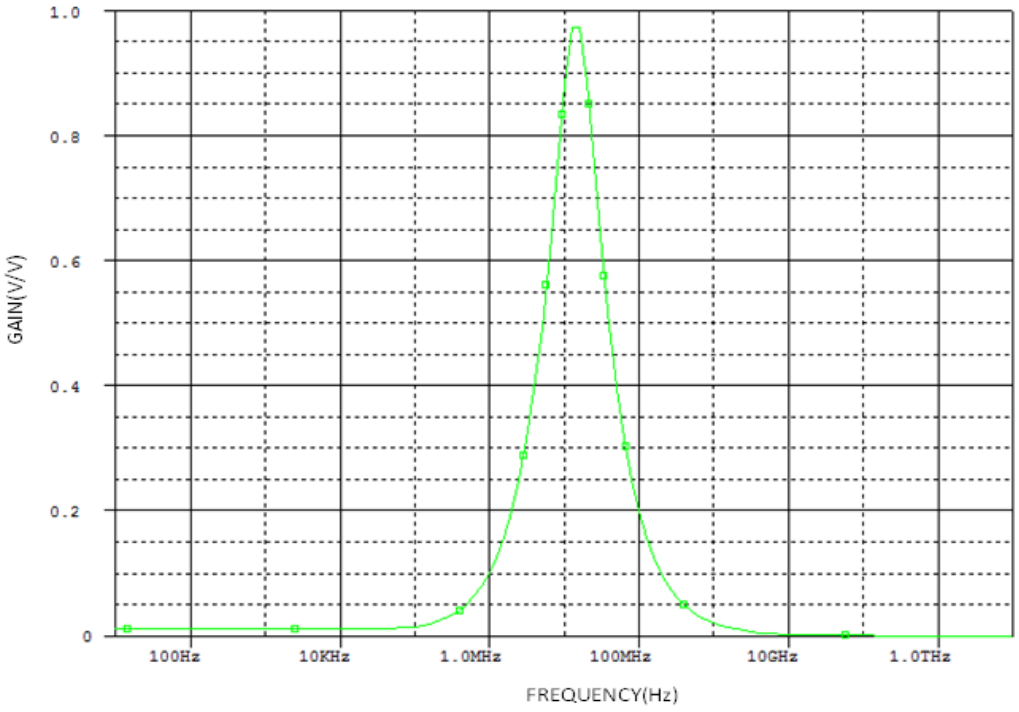

Fig 4.5. Frequency Response Of Bandpass Filter Using VDTA Based Grounded Inductor

4.2.1. NON-IDEALITY AND SENSITIVITY PERFORMANCE FOR GROUNDED INDUCTANCE VICTIMIZATION VDTA

Considering VDTA non-ideal parasitic i.e., the finite X-terminal parasitic electrical resistance consisting of a resistance Rx in parallel with capacitance 110 and therefore the parasitic electrical resistance at the Z-terminal consisting of a resistance Rz in parallel with capacitance Cz.

The non-ideal input electrical resistance for the circuit shown in Figure 4.6, is given by

$$Zin(s) = \frac{s(C + C_{x)} + \frac{1}{R_x}}{s^2 C_z (C + C_{x)} + s\left\{\frac{(C + C_{x)}}{R_z} + \frac{C_z}{R_x}\right\} + \frac{1}{R_x R_z} + g_{m1} g_{m2}} \tag{4.8}$$

From Equation (4.8) a non-ideal equivalent circuit of the grounded inductance is derived that is shown in Fig.4.6.

Where

$L_{GI} = \frac{(C+C_{x)}R_x R_z}{1+g_{m1}g_{m2}R_x R_z}$, $R' = \frac{(C+C_{x)}R_x R_z}{(C+C_{x)}R_x + CzRz}$, $C' = \frac{(C+C_{x)}R_x + CzR_z}{Rz}$, $R'' = \frac{R_z}{1+g_{m1}g_{m2}R_x R_z}$ and

$$D = (C + C_{x)}R_x R_z \tag{4.9}$$

From the on top of, the sensitivities of L_{GI} with relevance varied active and passive parts are found to be

$$S_C^{L_{GI}}=\frac{C}{(C+Cx)}\,,\ S_{Cx}^{L_{GI}}=\frac{Cx}{(C+Cx)}\,,\ S_{R_x}^{L_{GI}}=S_{R_x}^{L_{GI}}=\frac{1}{1+g_{m1}g_{m2}R_xR_z}\,,\ S_{g_{m1}}^{L_{GI}}=S_{g_{m1}}^{L_{GI}}=-\frac{g_{m1}g_{m2}R_xR_z}{1+g_{m1}g_{m2}R_xR_z}$$

(4.10)

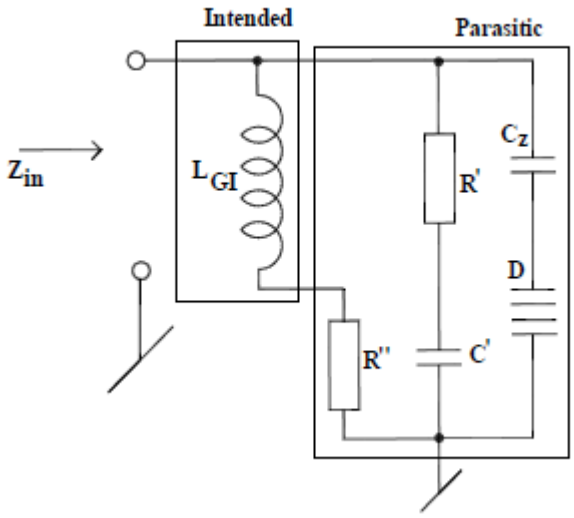

Fig 4.6. Non Ideal Structure Of VDTA Based Grounded Inductor [66]

4.3. FLOATING INDUCTOR USING VDTA

Floating inductance using VDTA [65] is shown in figure 4.7. The Floating inductance is realized using two VDTA and one single capacitor. The transfer function of floating inductance is illustrated below

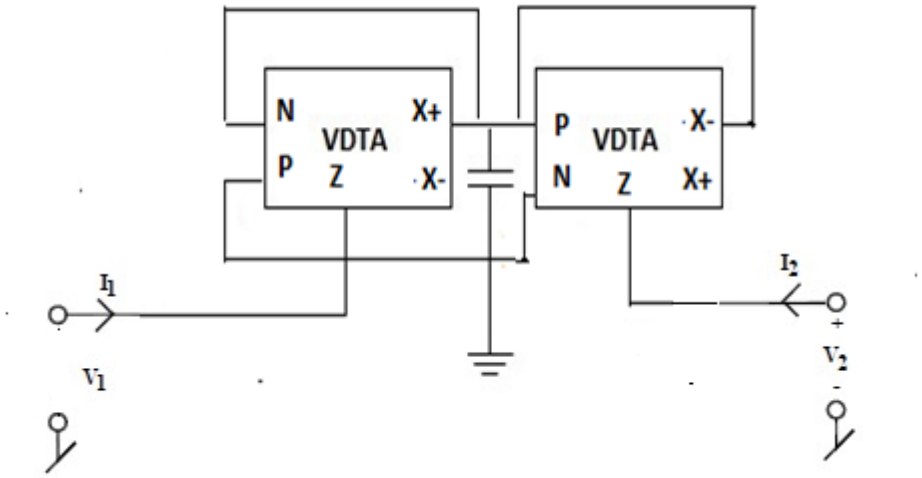

Fig 4.7. Floating Inductor Using VDTA [66]

The y matrix of the fig 4.7, is written as

$I_1=y_{11}V_1+y_{12}V_2$ (4.11)

And $I_2=y_{21}V_1+y_{22}V_2$ (4.12)

Where $y_{11} = \frac{I1}{V1}|V_2 = 0$

$y_{12} = \frac{I1}{V2}|V_1 = 0$

$y_{21} = \frac{I2}{V1}|V_2 = 0$

$y_{22} = \frac{I2}{V2}|V_1 = 0$

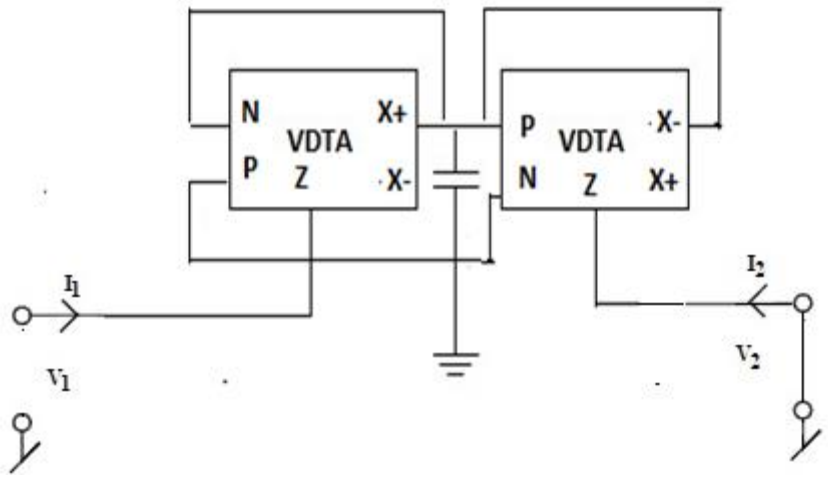

Fig 4.8(a) VDTA Based Floating Inductor with V_2 Shorted i.e. V_2=0

To derive y matrix of the circuit we short V_2 first as shown in figure 4.8(a), so that V_2=0. We need to derive the value of y_{11} and y_{21}.

Applying nodal analysis at node 1 we get ,

$$sC_1V_N = ix+= g_{m2}V_1$$

Or,

$$V_N = \frac{\text{gm2V1}}{\text{sC1}} \tag{4.13}$$

Now, $I_1 = -i_{Z1} = g_{m1}V_N = \frac{gm1gm2V1}{sC}$ (4.14)

Therefore $y_{11} = \frac{I1}{V1}|V_2 = 0 = \frac{sC}{gm1gm2}$ (4.15)

Now I_2=-i_{z2}=-$g_{m1}V_p$ (4.16)

Now sCV_p=i_{x+} =$g_{m2}V_1$ (4.17)

Or,

$$i_2 = \frac{-g_{m1}g_{m2}V_1}{sC} \tag{4.18}$$

Now, $y_{21} = \frac{V1}{i2}|v_2 = 0 = \frac{sC}{gm1gm2}$ (4.19)

Now we short V_1 terminal as shown in figure 4.8(b), so that V1=0. We need to derive y_{12} and y_{22}.

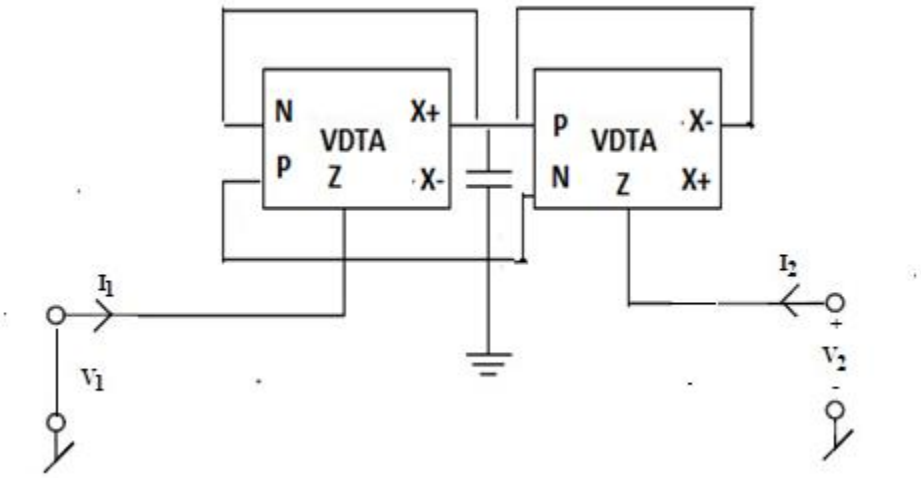

Fig 4.8(b) VDTA Based Floating Inductor With V_1 Shorted i.e. V_1=0

Applying nodal analysis at node 1, we get,

$sCV_P = ix-= -g_{m2}V_2$

Or, $Vp = \frac{-gm2V2}{sC}$ (4.20)

Now, $I_2 = -i_{z2} = -g_{m1}V_p = \frac{gm1gm2V2}{sC}$ (4.21)

Therefore $y_{22} = \frac{I2}{V2}|V_1 = 0 = \frac{sC}{gm1gm2}$ (4.22)

Now $I_1 = -i_{z1} = g_{m1}V_N$ (4.23)

Now $sCV_N = i_{x-} = -g_{m2}V_2$ (4.24)

Or, $i_1 = \frac{-gm1gm2V2}{sC}$ (4.25)

Now, $y_{12} = \frac{V2}{i1}|v_1 = 0 = -\frac{sC}{gm1gm2}$ (4.26)

So the y matrix of the circuit in Fig is described as

$$\begin{bmatrix} I1 \\ I2 \end{bmatrix} = \frac{gm1gm2}{sC}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}\begin{bmatrix} V1 \\ V2 \end{bmatrix} \quad (4.27)$$

which proves that the circuit behaves as a floating lossless, that is electronically-controllable inductance with the inductance worth given by g_{m1} and g_{m2} that is controlled by biasing current I_{bias}.

Now the experiment is carried out using a 5pF capacitor. We can get the magnitude of floating inductance as,

$$L_{Equ} = \frac{C}{gm1gm2} = \frac{5pF}{\frac{631\mu A}{V} x627 \frac{\mu A}{V}} = 12.6\mu H$$

The simulation of L_{equ} Vs Frequency is shown in Fig 4.9, where we get the inductance value as 13.14 μH.

So error=

$$\frac{13.4 - 12.6}{12.6} X100\% = 4.28\%$$

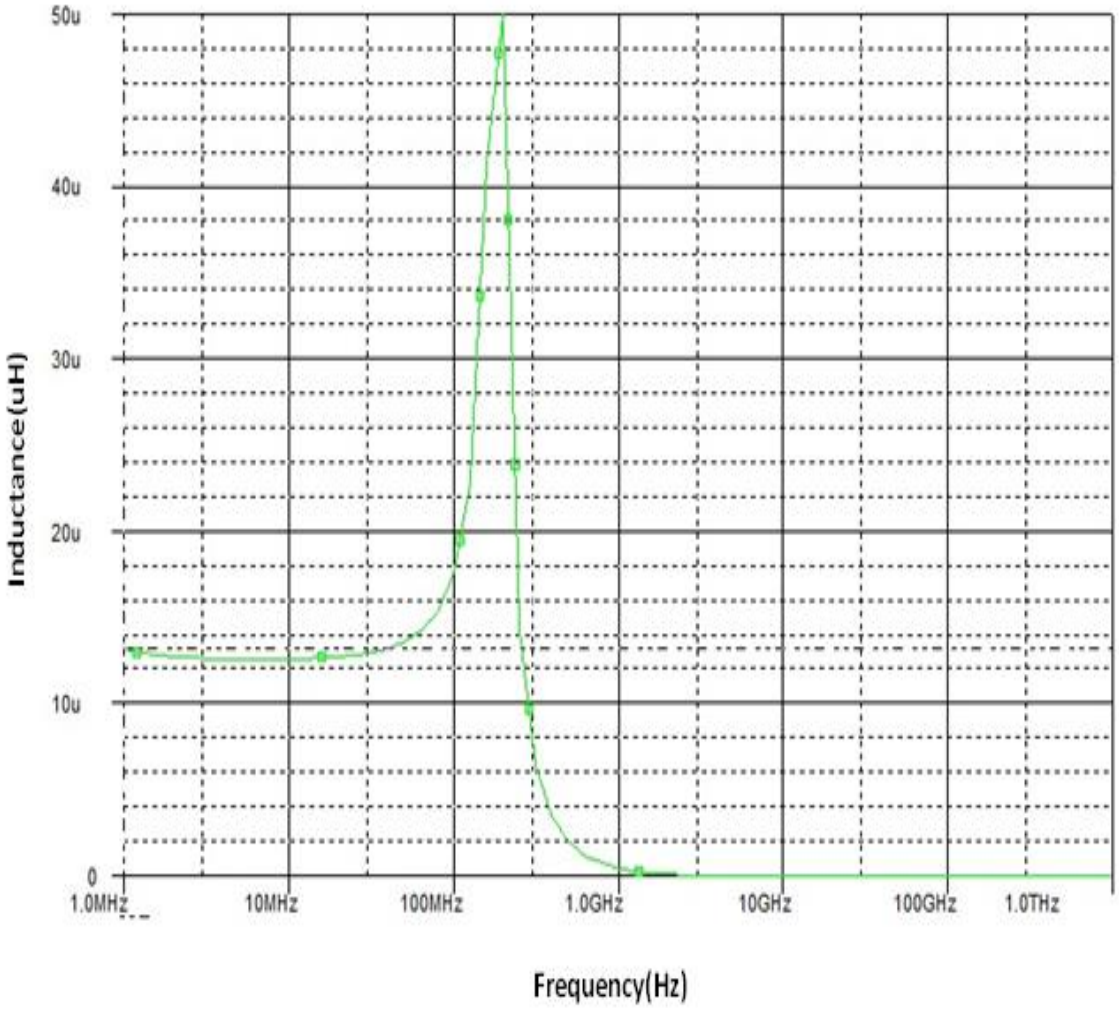

Fig 4.9. Inductance Vs Frequency For VDTA Based Floating Inductor

Performance of the new simulated inductors was verified by SPICE simulations. CMOS-based VDTA from [35] was accustomed to confirm the frequency responses of the floating simulated inductors. The subsequent values were used for grounded in addition as floating inductor: C_1 = 5pF, $g_{m1} = g_{m2}$ = 631.7 μA/V. From the frequency response of the simulated floating inductance (Figure 4.7), the inductance value remains constant up to 10MHz.

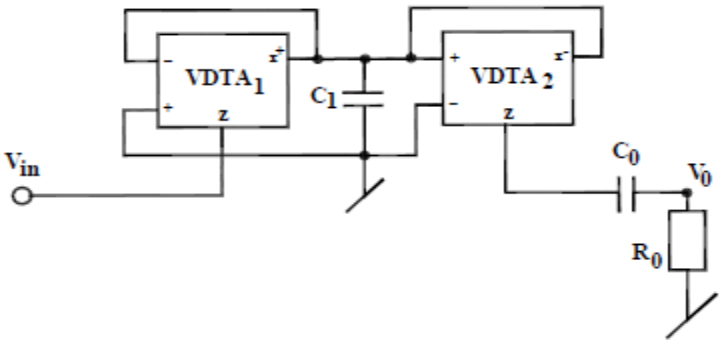

Fig 4.10. Bandpass Filter Using VDTA Based Floating Inductor [66]

Here in fig 4.10, the L_{equ}=12.6 μH as discussed earlier is used in band-pass filter configuration. Now the circuit will be behaved as the RLC series circuit shown in figure 4.11.

Whose Transfer Function is written as,

$$\frac{I(s)}{V(s)} = \frac{\frac{1}{L}s}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$$

That is the expression of band pass filter.

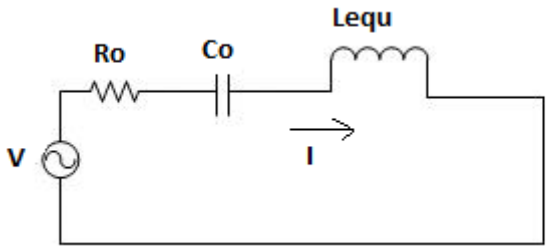

Fig 4.11. RLC Series Circuit

Where center frequency $\omega_o=\frac{1}{\sqrt{LC}}$ rad/sec therefore $fo=\frac{1}{2\pi\sqrt{LCo}}=\frac{1}{2\pi\sqrt{\frac{C1}{gm1gm2}Co}}$

The theoretical value of the band-pass filter is calculated as 14.17MHz

By simulation, we get 12.67MHz as shown in figure 4.12.

So the error will be,

$$\frac{12.67-14.17}{14.17}X100\% = -10.58\%$$

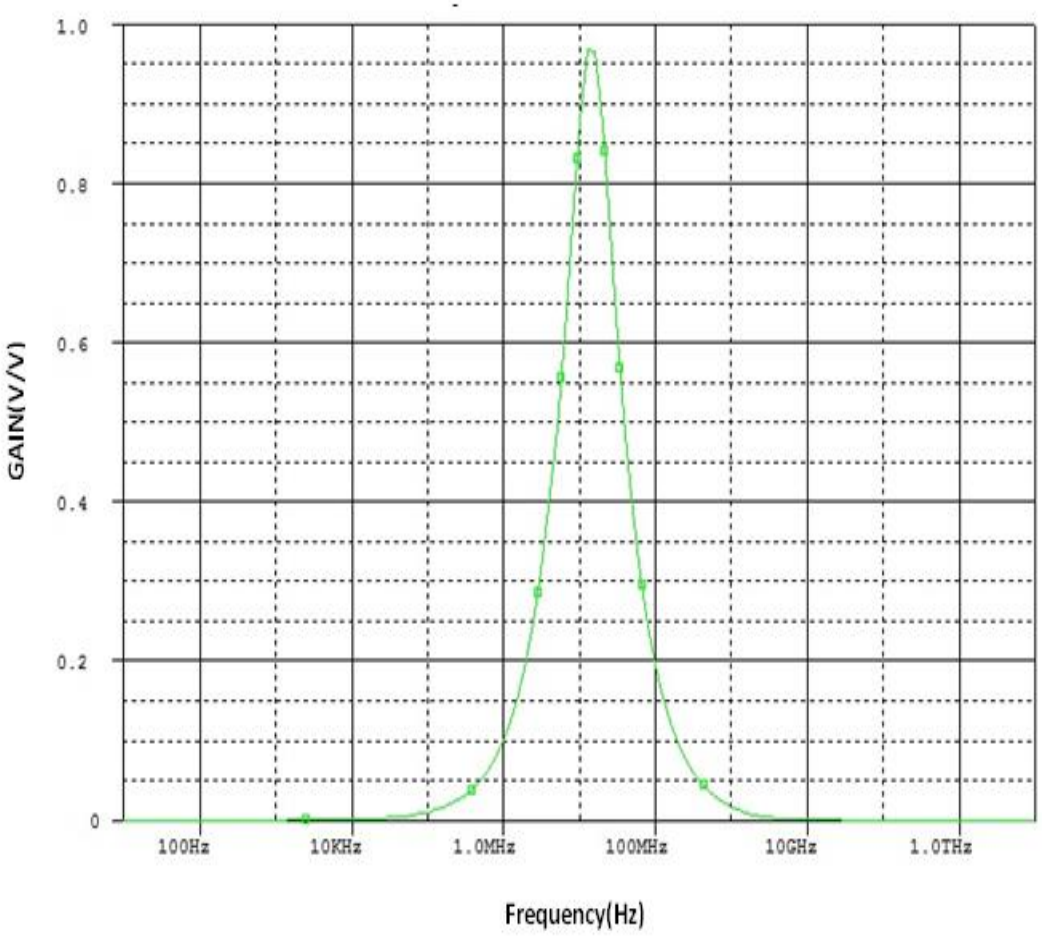

Fig 4.12. Frequency Response for Band-pass Filter Using VDTA Based Floating Inductor

4.3.1. NON-IDEALITY AND SENSITIVITY PERFORMANCE FOR FLOATING INDUCTANCE VICTIMIZATION VDTA

Considering VDTA non-ideal parasitic i.e., the finite X-terminal parasitic electrical resistance consisting of a resistance Rx in parallel with capacitance 110 and therefore the parasitic electrical resistance at the Z-terminal consisting of a resistance Rz in parallel with capacitance Cz

The non-ideal equivalent circuit of floating inductance of Figure 4.7 is derived from Equation (4.28) and is shown in Figure 4.13. Similarly, for the circuit shown in Figure 4.7, the input-output current and voltage relationships are given by:

$$\begin{bmatrix} I1 \\ I2 \end{bmatrix} = \frac{gm1gm2}{s(C+2Cx)+\frac{2}{Rx}} \begin{bmatrix} 1+\left\{s(C+2Cx)+\frac{2}{Rx}\right\}\left(sCz+\frac{1}{Rz}\right) & -1 \\ -1 & 1+\left\{s(C+2Cx)+\frac{2}{Rx}\right\}\left(sCz+\frac{1}{Rz}\right) \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix} \quad (4.28)$$

Where

$$L_{FI} = \frac{(C+2Cx)}{gm1gm2} R = \frac{2}{Rxgm1gm2}$$

The various sensitivities of L_{FI} with respect to active and passive elements are:

$$S_C^{LFI} = \frac{C}{(C+2Cx)} \; S_{Cx}^{LFI} = \frac{Cx}{(C+2Cx)}$$

$$S_{gm1}^{LFI} = -1 \; S_{Cgm2}^{LFI} = -1 \tag{4.29}$$

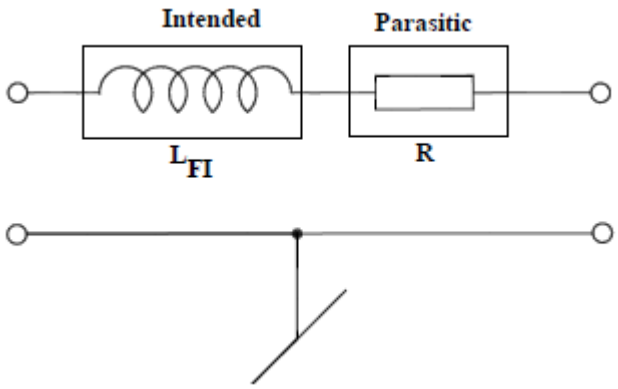

Fig 4.13. Non Ideal Structure of Floating Inductor Using VDTA [66]

CHAPTER-5

LC LADDER FILTER REALIZATION USING VDTA

5.1. INTRODUCTION

In the previous chapter we presented the realization as well as floating inductor using active building blocks VDTA.

In the present chapter we have realized 3^{rd}, 4^{th}, 5^{th}, 6^{th} order low-pass and high-pass filters, 8^{th} order band-pass filter and 10^{th} order band reject Butterworth filters. We have adopted the aforesaid filters using synthesis technique described in.

5.2. LC LADDER FILTER DESIGN

The LC ladder filter is having an excellent circuit with very less sensitivity to component tolerances. Because of the low sensitivity to component values that characterizes the doubly terminated LC ladders, these circuits are majorly used in filter applications. LC ladder is used as a model for circuits that employ active elements to simulate inductors, resistors and other elements. To obtain transfer of signal power, the ladder has a source V_s, as a rule with a source resistor R_1, and is terminated with a load resistor R_2 that dissipates the output signal energy and where the output signal is being measured. We will have keen interest in lossless ladders for the following reasons:

1. Even though the design of LC filters has its roots in antiquity, lossless ladders has its widespread use in this day for high frequency applications or where no power is available to drive the active devices.
2. LC ladder filters form prototype models that are simulated by active circuits, both with discrete components and in fully integrated form on an on-board integrated

circuit chip. The goal is to develop the active circuit in such a way that the simulation inherits the excellent sensitivity properties of lossless passive ladders.

3. Finally if we get success in developing an active simulation of the passive ladder, we will be able to make use of a bulk number of design information and tables that are readily available for LC ladders.

The low sensitivity property that we are interested in is valid for doubly terminated ladders. Sensitivities can be shown to exhibit poor response when either or both terminations are not present for example, source resistance=0 and/or load resistance=∞. We therefore are left only with ladders working between two resistors.

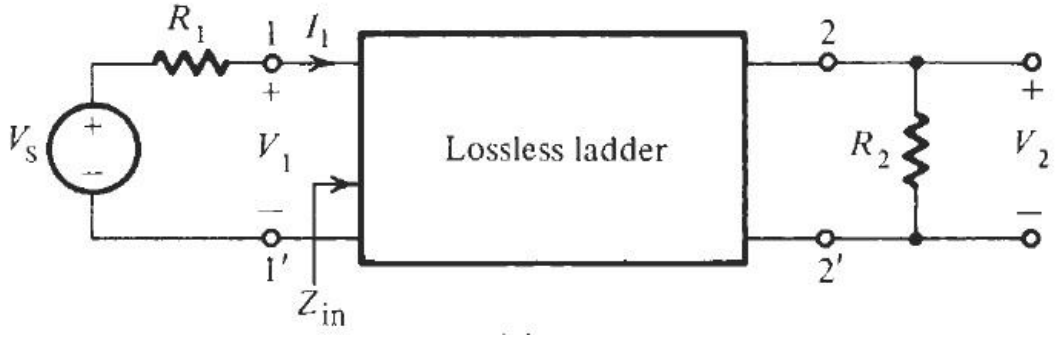

Fig 5.1. Doubly Resistively Terminated LC Ladder Lossless Filter [91]

5.3. SYNTHESIS PROCEDURE

In the doubly terminated [91] circuits in Fig 5.1 we have seen the current from the source, I_1, and its reference flowing direction, and Z_{in} seen as the input impedance of the RLC circuit what consists of the lossless ladder terminated by R_2. We assume that the circuit is under working condition in sinusoidal steady state. The input impedance is having both a real and imaginary component

$$Zin = Rin + JXin \tag{5.1}$$

And the current at the input terminal is

$$I_1 = \frac{V_S}{R_1 + Z_{in}} \tag{5.2}$$

Now since the LC circuit acts as lossless, we may make the average power equating to the circuit, P_1, equation, to that of the load. Thus,

$$P_1 = R_{in}|I_1(j\omega)|^2 = \frac{|V_2(j\omega)|^2}{R_2} \tag{5.3}$$

Substituting Eq.(2) for I_1 into this equation provides us

$$\frac{R_{in}|V_S(j\omega)|^2}{|R_1+Z_{in}|^2} = \frac{|V_2(j\omega)|^2}{R_2} \tag{5.4}$$

From this equation, we have a tendency to get the magnitude square of the required transfer perform

$$\left|\frac{V_2(j\omega)}{V_S(j\omega)}\right|^2 = |T(j\omega)|^2 = \frac{R_2R_{in}}{|R_1+Z_{in}|^2} \tag{5.5}$$

To make this expression relate to the transfer function H(s) that we represent to use for LC filter and if we take the ratio of power, we get,

$$|H(j\omega)|^2 = \frac{P_2}{P_{1,max}} = \frac{4R_1}{R_2}\left|\frac{V_2(j\omega)}{V_S(j\omega)}\right|^2 = \frac{4R_1}{R_2}\frac{R_2R_{in}}{|R_1+Z_{in}|^2} \leq 1 \tag{5.6}$$

With Eq.(1) we obtain,

$$|H(j\omega)|^2 = 1 - \frac{|R_1-Z_{in}|^2}{|R_1+Z_{in}|^2} = 1 - |\rho(j\omega)|^2 \tag{5.7}$$

where the auxiliary function ρ(s) is termed as the reflection coefficient. P(s) is a measure to know how well R_1 and Z_{in} are matched ; we have always $|\rho(j\omega)|^2 \leq 1$ and for matching purpose, ρ(s)=0. Evidently, ρ(s) is described as

$$|\rho(j\omega)|^2 = \left|\rho(s)|\rho(-s)|\right|_{s=j\omega} = \frac{|R_1-Z_{in}|^2}{|R_1+Z_{in}|^2} \tag{5.8}$$

From this equation, we can see that ρ(s) may be separated from ρ(-s) to give the result as

$$\rho(s) = \pm\frac{R_1-Z_{in}(s)}{R_1+Z_{in}(s)} \tag{5.9}$$

Clearly, this equation may be deduced for Z_{in} in terms of ρ(s) and R_1. The final result is

$$Z_{in} = R_1 \frac{1-\rho(s)}{1+\rho(s)} \tag{5.10}$$

Or $$Z_{in} = R_1 \frac{1-\rho(s)}{1+\rho(s)} \tag{5.11}$$

Observe that these expressions result into two reciprocal impedances. Now, since ρ is described in terms of the prescribed transfer function H, we have reduced the problem to determining a lossless circuit terminated in a resistor R_2 from a defined Z_{in}. Sidney Darlington (1939) showed in his classic publication that this was always possible, and so the circuit may be designed from a given Z_{in}. To depict the implementation of the strategy, consider the problem to determine circuits which have a Butterworth response where there are equal terminations with R_1=R_2=1, a normalized value that may later be magnitude scaled by de-nomalizing the element parameters to obtain the desired cutoff or centered frequency.

The Butterworth response is expressed as:

$$|H(j\omega)|^2 = \frac{1}{1+\omega^{2n}} \tag{5.12}$$

Note that this magnitude-squared function is less than or equal to unity and so it satisfies the condition of Eq. (6). Since the magnitude-squared function is

$$|H(j\omega)|^2 = \left|H(s)|H(-s)|\right|_{s=j\omega} \tag{5.13}$$

Then

$$|H(j\omega)|^2 = \frac{K_H}{|D(j\omega)|^2} = \left|\frac{K_H}{D(s)|D(-s)|}\right|_{s=j\omega} \tag{5.14}$$

The constant K_H relates to the constant K by $K_H = 2\sqrt{\frac{R_1}{R_2}}K$, and D(s) is known from our study of the Butterworth response function.

We may determine from Eq. (5.7) the auxiliary function of Eq.(5.9), We have

$$|\rho(j\omega)|^2 = 1 - \frac{1}{1+\omega^{2n}} = \frac{\omega^{2n}}{1+\omega^{2n}} \tag{5.15}$$

Since

$$\omega^{2n}|_{\omega^2=-s^2} = s^n(-s)^n \tag{5.16}$$

We see that

$$\rho(s) = \frac{s^n}{D(s)} \tag{5.17}$$

Substituting this value of ρ(s) into Eqs. (10) and (11), we get,

$$Z_{in} = R_1 \left[\frac{1-\rho(s)}{1+\rho(s)}\right]^{\pm} = R_1 \left[\frac{D(s)-s^n}{D(s)+s^n}\right]^{\pm} \tag{5.18}$$

It is convenient way to normalize the impedance level of the circuit by setting $R_1 = 1\Omega$. The realization of the n-th order transfer function uses exactly n reactance, one for each degree of freedom; such a realization is referred to be canonic. The realization of all pole low-pass filters is always considered as canonic but this is not a generalized case for LC ladders. When we use, Table 5.1, the two resistors are having equal and normalized with respect to the impedance level in that $R_1=R_2=1\Omega$ and with respect to the frequency that is considered to be 3-dB frequency, $\omega_p=1$. If $\alpha_{max}\neq 3$dB, we have to denormalize the elements to have the Butterworth frequency written as

$$\omega_B = \epsilon^{-\frac{1}{n}}\omega_P \tag{5.19}$$

Table 5.1.Table Of Element Values For Doubly Terminated Butterworth Filters For N=2 To N=10 Normalized To Half-Power Frequency of 1rad/s

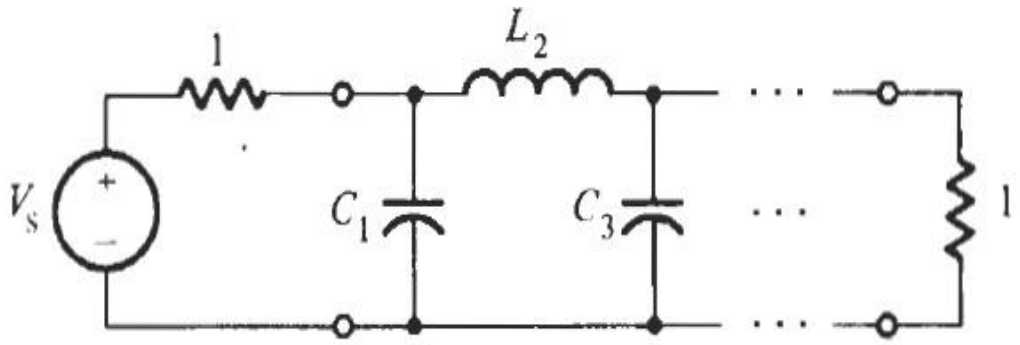

Fig 5.2(a) LC Ladder Lowpass Filter In Generalised Form (i) [91]

n	C1	L2	C3	L4	C5	L6	C7	L8	C9	L10
2	1.414	1.414								
3	1.000	2.000	1.000							
4	0.7654	1.848	1.848	0.7654						
5	0.6180	1.618	2.000	1.618	0.6180					
6	0.5176	1.414	1.932	1.932	1.414	0.5176				
7	0.4450	1.247	1.802	2.000	1.802	1.247	0.4450			
8	0.3902	1.111	1.663	1.962	1.962	1.663	1.111	0.3902		
n	L1	C2	L3	C4	L5	C6	L7	C8	L9	C10

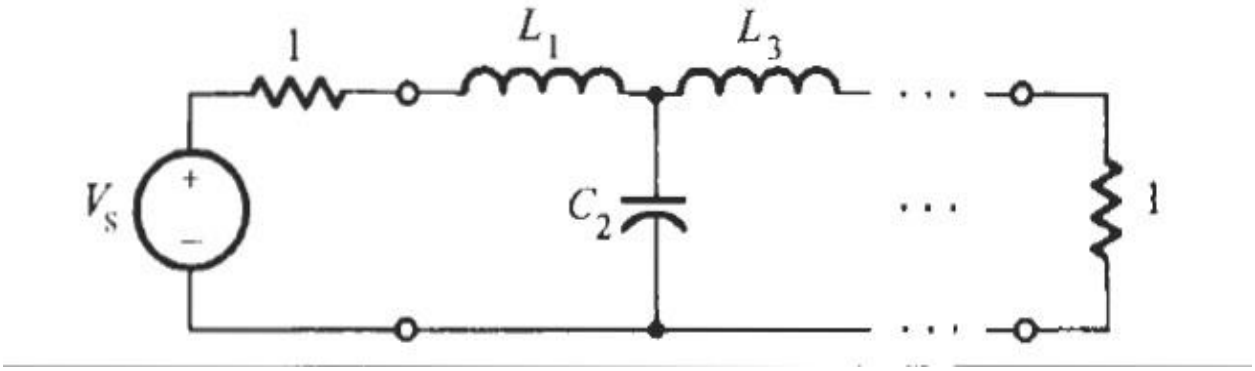

Fig 5.2(b) LC Ladder Lowpass Filter In Generalised Form (ii) [91]

5.3.1. TRANSFORMATION OF COMPONENTS

In the case of passive filters [92], as represented above, one will have the denormalized high-pass, band-pass, or band-stop filters by exploiting the antecedently introduced frequency transformations to the normalized low-pass filter prototype.

This approach isn't applicable in the case of active RC filters design apart from the case of getting a high-pass from the normalized low-pass filter. We have a tendency to examine the element substitution in detail as depicted below:

TABLE 5. 2 LC FILTERS

Lowpass-To-Lowpass Transformation $S_n \rightarrow S / \Omega_c$ With Ωc The Cutoff Frequency

Component	Electrical Resistance	New component value
L_n	$s_n L_n = \frac{s}{\omega_c} L_n$	$L = \frac{L_n}{\omega_c}$
C_n	$\frac{1}{s_n C_n} = \frac{\omega_c}{s C_n}$	$C = \frac{C_n}{\omega_c}$

Lowpass-To-Highpass Transformation $S_n \rightarrow \Omega_c / S$ With Ωc The Cutoff Frequency

Component	Electrical Resistance	New component value
Ln	$s_n L_n = \frac{\omega_c}{s} L_n$	$C = \frac{1}{\omega_c L_n}$
Cn	$\frac{1}{s_n C_n} = \frac{s}{\omega_c C_n}$	$L = \frac{1}{\omega_c C_n}$

Lowpass-To-Bandpass Transformation $sn \rightarrow \frac{\omega_o}{B}\left(\frac{s}{\omega_o} + \frac{\omega_o}{s}\right)$ With Ωc The Cutoff Frequency

Component	Electrical Resistance	New component value
L_n	$s_n L_n = \frac{\omega_o}{B}\left(\frac{s}{\omega_o} + \frac{\omega_o}{s}\right) L_n$	Series L& C $L = \frac{L_n}{B}$ and $C = \frac{B}{\omega_o^2 L_n}$
C_n	$\frac{1}{s_n C_n} = \frac{1}{\frac{\omega_o}{B}\left(\frac{s}{\omega_o} + \frac{\omega_o}{s}\right) C_n}$	Parallel L and C $L = \frac{B}{\omega_o^2 C_n}$ and C = $\frac{C_n}{B}$

Lowpass-To-Band Stop Transformation $sn \rightarrow \frac{1}{\frac{\omega_o}{B}\left(\frac{s}{\omega_o}+\frac{\omega_o}{s}\right)}$ With Ωc The Cutoff Frequency

Component	Electrical Resistance	New component value
L_n	$s_n L_n = \frac{1}{\frac{\omega_o}{B}\left(\frac{s}{\omega_o}+\frac{\omega_o}{s}\right)} L_n$	Series L& C $L = \frac{BL_n}{\omega_o^2}$ and $C = \frac{1}{BL_n}$
C_n	$\frac{1}{s_n C_n} = \frac{\frac{\omega_o}{B}\left(\frac{s}{\omega_o}+\frac{\omega_o}{s}\right)\omega_c}{C_n}$	Parallel L and C $L = \frac{1}{BC_n}$ and C = $\frac{BC_n}{\omega_o^2}$

In this thesis work, first low-pass filter is derived, then all the other filters (high-pass, band-pass and band-stop filters) are obtained from its equivalent low-pass filter prototype using the aforesaid frequency translation. The frequency scaling process has also been adopted to get the frequency for which the filters are being designed for (10MHz in this case).

5.4. PROJECT WORK

5.4.1. THIRD ORDER LC LADDER BUTTERWORTH LOWPASS FILTER USING VDTA

The LC ladder (doubly terminated) that represents a third order low-pass filter (Butterworth) [91] at 1rad/sec is depicted in Fig.5.3, where R_1=1Ω, C_1=C_2=1F and L=2H. Let us select a minimum inductance ladder so that the very first and last elements are capacitors. From the table 5.1, we get the value of the elements which is referred to the normalized frequency. But to have frequency scaling we have to de-normalize the elements which depends on source, load resistance and cut-off frequency. Let us consider α_{max}=0.7. Therefore $\varepsilon = \sqrt{10^{0.07} - 1 = 0.4182}$ so that

$\omega_B = \epsilon^{-\frac{1}{n}}\omega_P$ =2*π*(0.4182)-1/3 *10MHz = 84Mrad/sec therefore fb=13.37MHz

With these numbers, we de-normalize the resistors by multiplying by 1.5KΩ and the inductors and capacitors, by multiplying by,

$\frac{1.5\text{K}\Omega}{84\text{Mrad/sec}} = 17.857\mu H$ and $\frac{1}{1.5K\Omega \text{ x} 84\text{Mrad/sec}} = 7.9365pF$

Therefore, C_A=C_B=7.9365pF

L_1=2 x 17.857 μH=35.714 μH , therefore, C_1=$g_{m1}g_{m2}L_1$ =35.714x631 $\mu\frac{A}{V}$x627 $\mu\frac{A}{V} = 15pF$

Finally replacing the floating inductors L1 by VDTA based floating inductor presented in chapter, we get the active third order low-pass Butterworth filter as shown in Fig. 5.4.

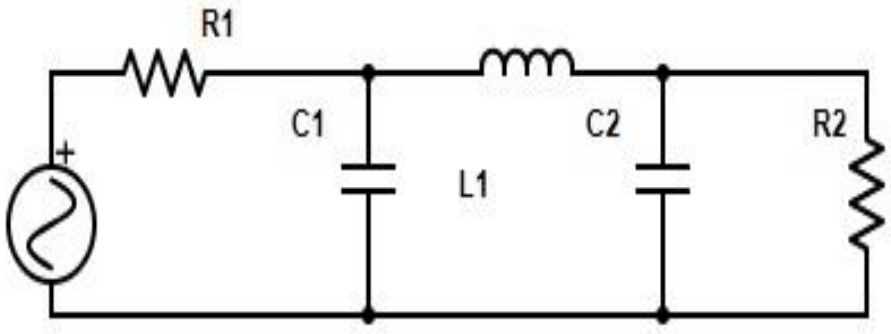

Fig 5.3. Third Order LC Ladder Butterworth Low-pass Filter

The transfer function of third order low-pass ladder filter is derived as follows:

Applying nodal analysis at node 2, we get

$$\frac{V_1}{sL_1} = \left(sC_2 + \frac{1}{sL_1} + \frac{1}{R_2}\right)V_2$$

(5.20)

Or,

$$V_1 = \frac{s^2 C_2 L_1 + sL_1 + R_2}{R_2} \mathrm{V2}$$

(5.21)

Now applying nodal analysis in node 1 we get,

$$\frac{V_{in}}{R_1} = \left(sC_1 + \frac{1}{sL_1} + \frac{1}{R_1}\right) V_1 - \frac{V_2}{sL_1}$$

(5.22)

Or,

$$\frac{V_{in}}{R_1} = \frac{s^2 L_1 C_{1R_1+sL_1+R_1}}{sR_{1L_1}} V_1 - \frac{V_2}{sL_1}$$

(5.23)

Or, ,

$$\frac{V_{in}}{R_1} = (\frac{s^2 C_{2L_1R_2+sL_1+R_2}}{R_2})(\frac{s^2 L_1 C_{1R_1+sL_1+R_1}}{sR_{1L_1}})V_2 - \frac{V_2}{sL_1}$$

(5.24)

Or,

$$\frac{V_2}{V_{in}} = \frac{L_1 R_1}{s^3 C_1 C_2 L_1^2 R_1 R_2 + s^2 L_1^2 (C_1 R_1 + C_2 R_2) 1 + s\{L_1 R_1 R_2 (C_1 + C_2) + L_1^2\} + L_1 (R_1 + R_2)}$$

(5.25)

which is nothing, but the transfer function of third order LC ladder low-pass filter.

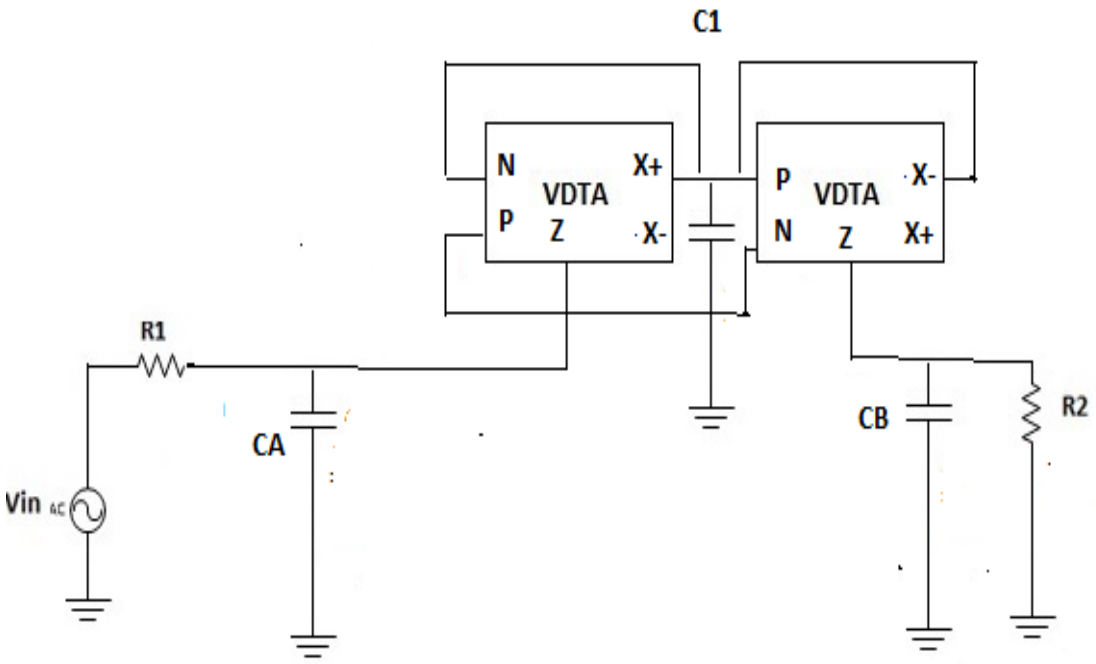

FIG 5.4. Third Order LC Ladder Butterworth Low-pass Filter Using VDTA

By simulation, as shown in Fig.5.5.we get the cutoff frequency to be 13.48MHz.

Therefore, error= $\frac{13.48-13.37}{13.37}$x100%=0.822%

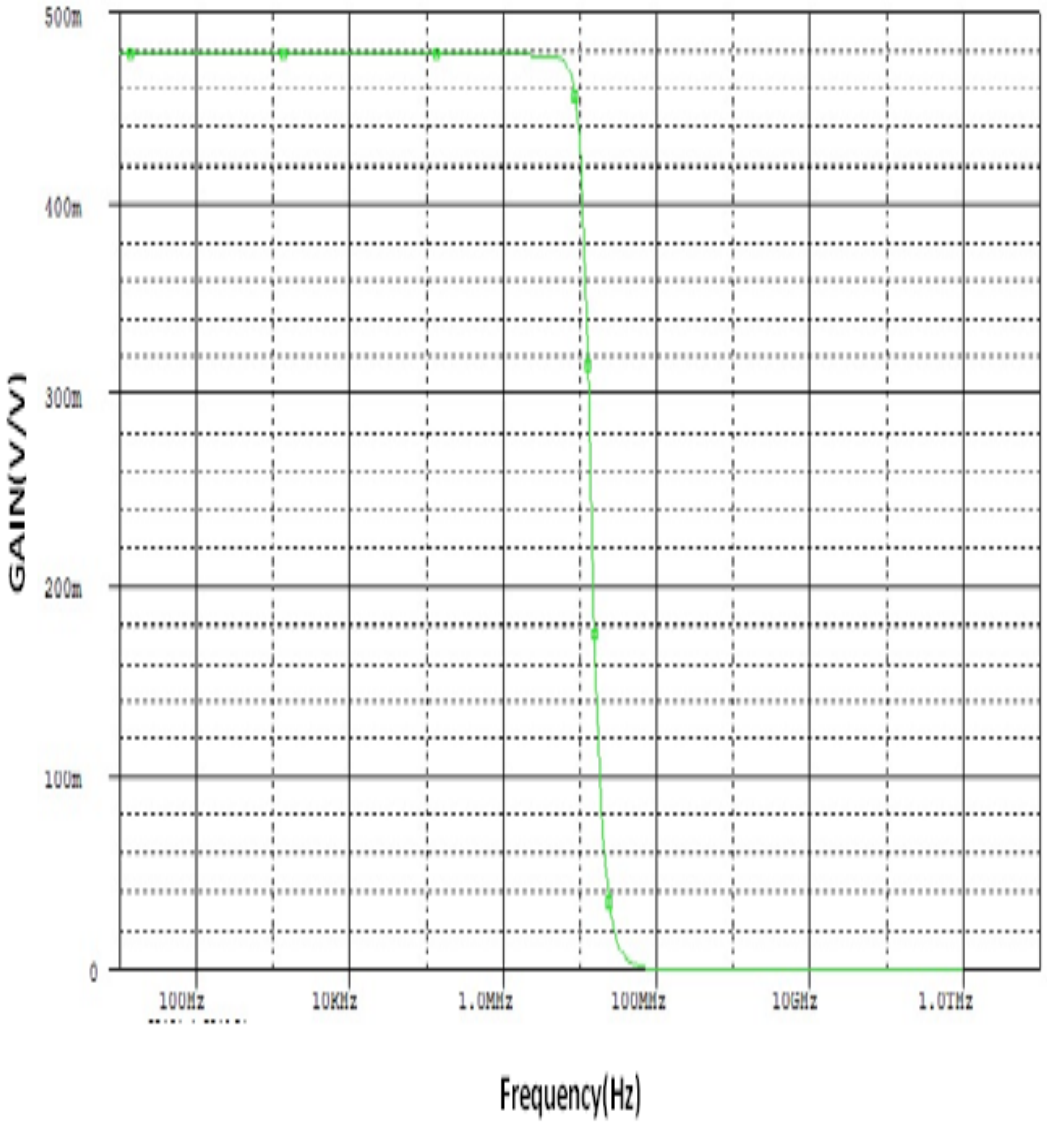

Fig.5.5. Frequency (Ac) Response Of Magnitude Gain For Third Order LC Ladder Butterworth Low-pass Filter Using VDTA

To study the time domain behavior, input signals comprised of 2 frequencies of 1MHz and amplitude of 500mV is applied. The transient response and its spectrum for input and output are shown in Fig 5.6.

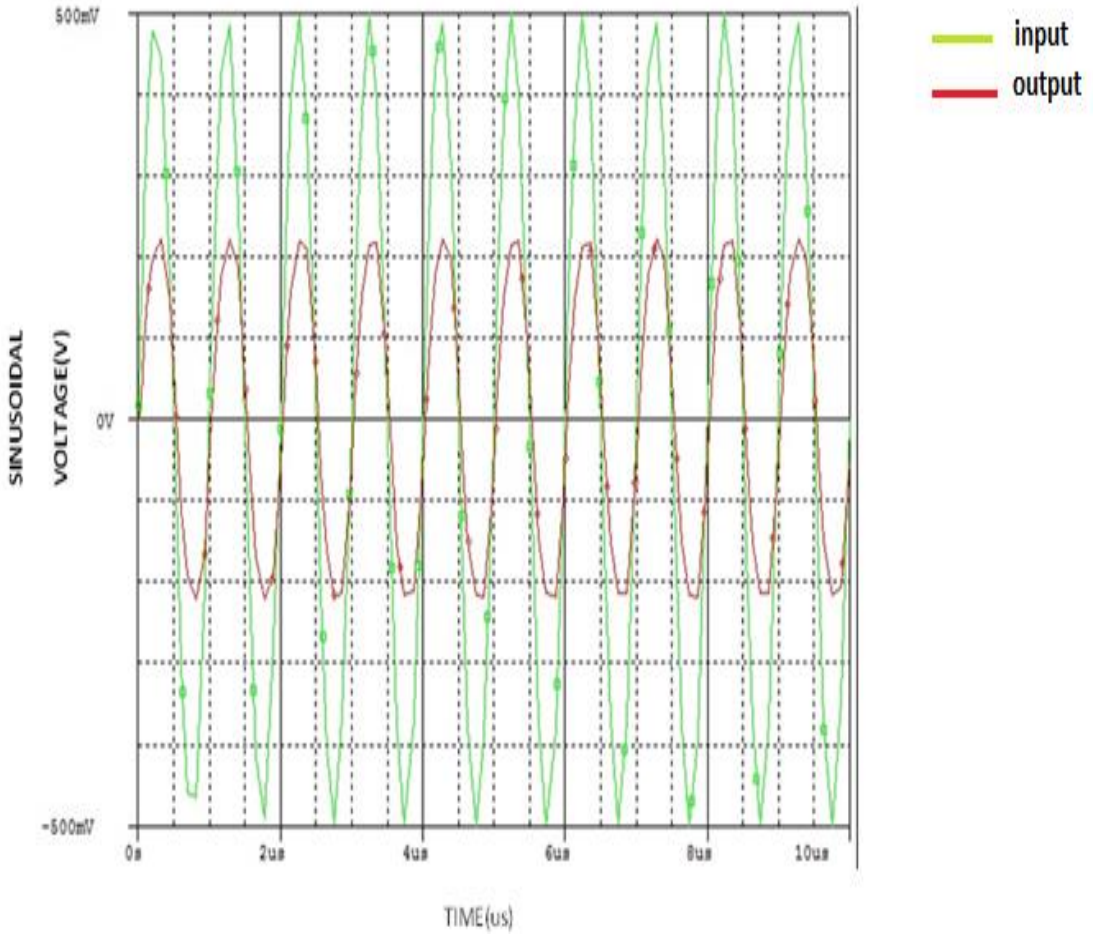

Fig 5.6. Transient Response for Input And Output For Third Order LC Ladder Butterworth Low-pass Filter Using VDTA

The filter parameter is also derived for the cutoff frequency of 10 MHz. The power dissipation for this circuit is 1.08E-03 Watts, output noise is assumed to be 5.773E-09V/Hz1/2 and %THD is within 1.614877E+02 % up to 500 mV p–p.

5.4.2. FOURTH ORDER LC LADDER BUTTERWORTH LOWPASS FILTER USING VDTA

The LC ladder (doubly terminated) representing a fourth order low-pass filter (Butterworth) [91] at 1rad/sec is shown in Fig. 5.7(a), Let us choose a minimum inductance ladder so that the first and last elements are capacitors. From the table 5.1, we get the value of the elements referred to the normalized frequency. But to have frequency scaling we have to de-normalize the elements which depends on source, load resistance and cut-off frequency. Let us consider α_{max}=0.7. Therefore $\varepsilon = \sqrt{10^{0.07} - 1 = 0.4182}$ so that

$\omega_B = \epsilon^{-\frac{1}{n}}\omega_P$ =2*π*(0.4182)-1/4 *10MHz = 78Mrad/sec therefore f_b=12.44MHz

With these numbers, we de-normalize the resistors by multiplying by 1.5KΩ and the inductors and capacitors, by multiplying by,

$\frac{1.28\text{K}\Omega}{78\text{Mrad/sec}} = 16.4\mu H$ and $\frac{1}{1.28K\Omega \text{ x} 78\text{Mrad/sec}} = 10pF$

Therefore, C_A=1.848x10pF=18.48pF and C_B=0.7654x10pF =7.654pF

L_1= 12.6 μH , therefore, $C_1=g_{m1}g_{m2}L_1$ =12.6 μH x631 $\mu A/$Vx627 $\mu\frac{A}{\text{V}} = 5pF$

and L_2= 12.6 μH , therefore, $C_2=g_{m1}g_{m2}L_2$ =30 μH x631 $\mu A/$Vx627 $\mu\frac{A}{\text{V}} = 12pF$

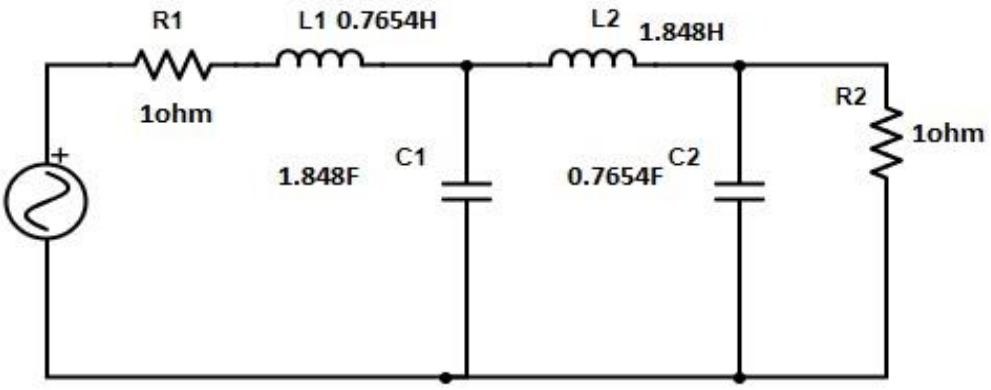

Fig 5.7(a) Fourth Order LC Ladder Butterworth Low-pass Filter

(For Normalized Frequency ω=1rad/sec)

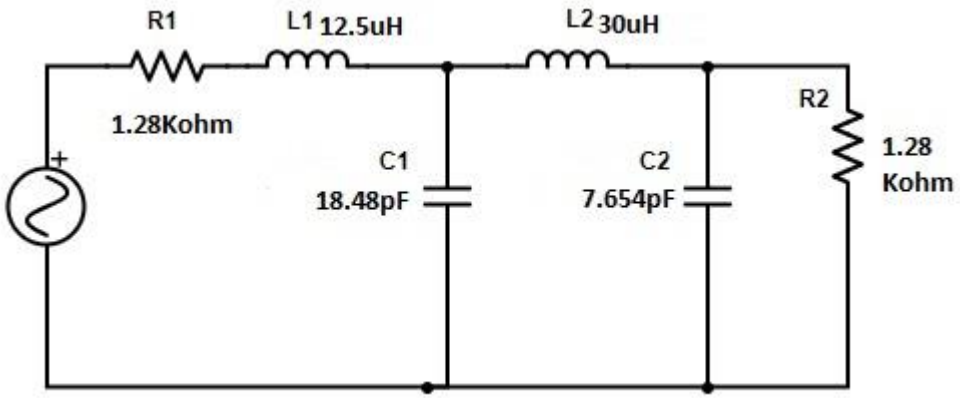

Fig 5.7(b) Fourth Order LC Ladder Butterworth Low-pass Filter

(For De-normalized For Frequency f=10MHz)

The transfer function of forth order LC ladder Butterworth filter is derived as follows:

Applying nodal analysis at node 2 we get,

$$\frac{V_1}{sL_1} = \left(sC_2 + \frac{1}{sL_2} + \frac{1}{R_2}\right)V_2 \tag{5.26}$$

Or ,

$$V_1 = \frac{s^2C_2L_2R_2 + sL_2 + R_2}{R_2}V_2 \tag{5.27}$$

Applying nodal analysis at node 1, we get

$$\frac{V_{in}}{R_1+sL_1} = \left(sC_1 + \frac{1}{sL_2} + \frac{1}{R_1 + sL_1}\right)V_1 - \frac{V_2}{sL_2} \tag{5.28}$$

Or,

$$\frac{V_{in}}{R_1+sL_1} = \left(sC_1 + \frac{1}{sL_2} + \frac{1}{R_1 + sL_1}\right)(\frac{s^2C_{2L_2R_2+sL_2+R_2}}{R_2})V_2 - \frac{V_2}{sL_2} \tag{5.29}$$

Or,

$$\frac{V_2}{V_{in}} = \frac{R_2L_2}{s^4C_1C_2L_1L_2^2R_2 + s^3L_2^2C_1(C_2R_1R_2 + L_1) + s^2\{C_2L_2R_2(L_1 + L_2\} + C_1L_2(R_1L_2 + R_2L_1) + S\{L_2R_1R_2(C_1 + C_2) + L_2(L_1+L_2)\} + L_2(R_1+R_2)} \tag{5.30}$$

The equation is the expression of the transfer function of fourth order low-pass LC ladder Butterworth filter.

Finally in Fig 5.8, replacing the floating inductors L_1 and L_2 by VDTA based floating inductor presented in chapter, we get the active fourth order low-pass Butterworth filter.

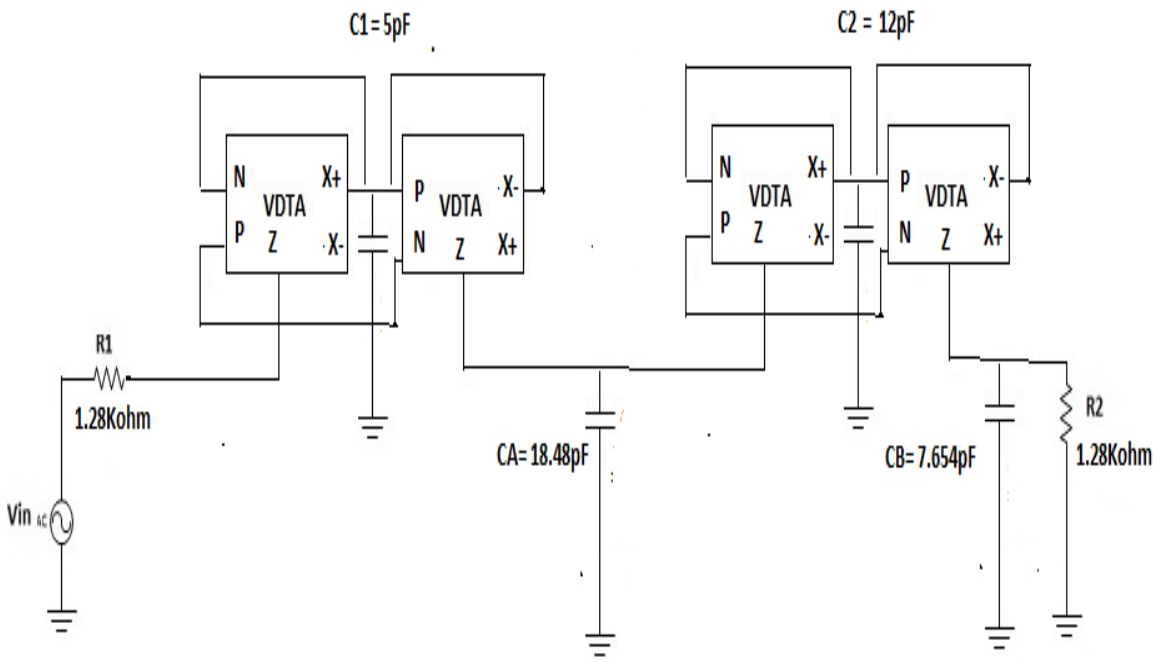

Fig.5.8. Fourth Order LC Ladder Butterworth Low-pass Filter Using VDTA

By simulation, as shown in Fig.5.9, we get the cutoff frequency to be 11.8552MHz.

Therefore, error=

$$\frac{11.8552 - 11.91}{11.91} \text{x} 100\% = -0.46\%$$

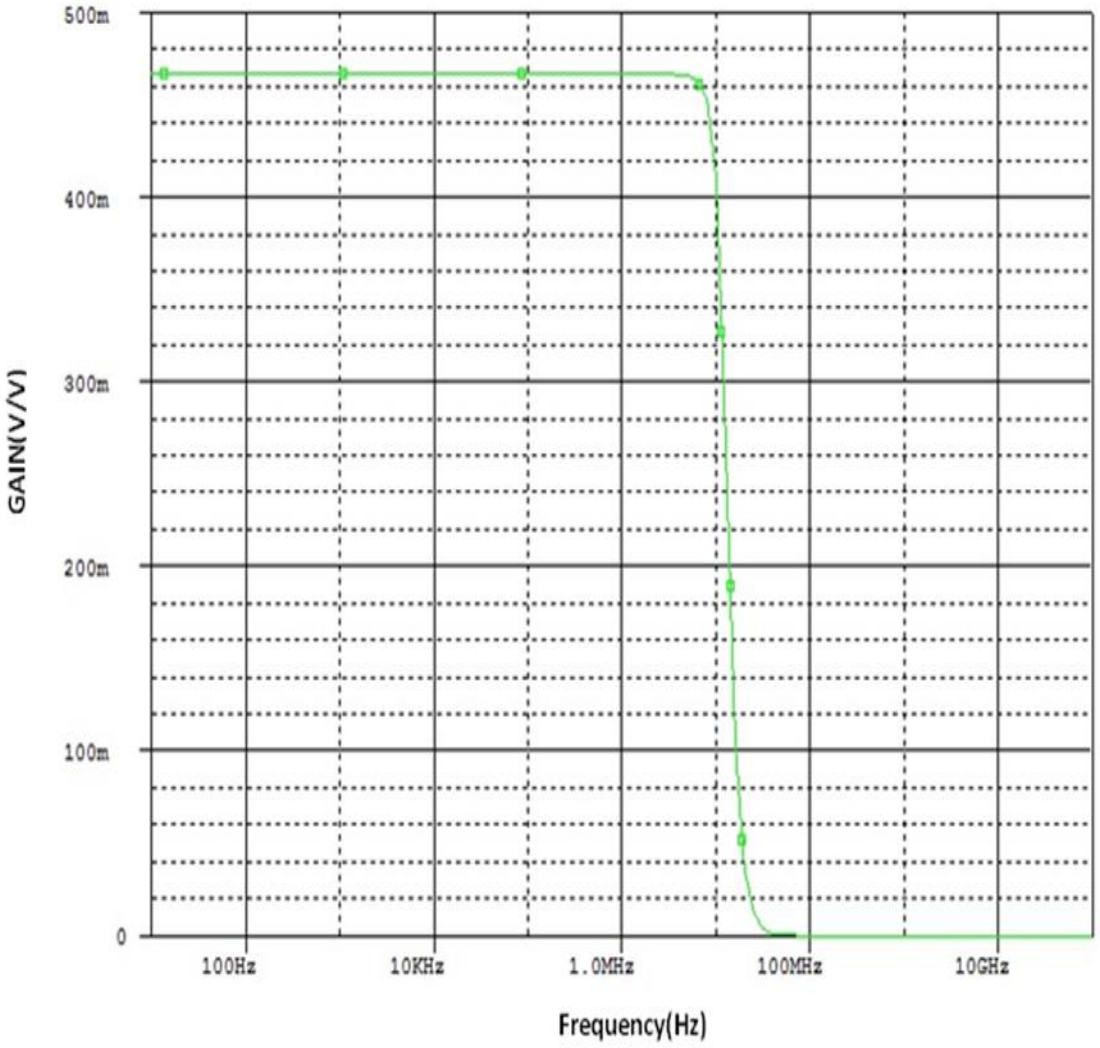

Fig.5.9. Frequency (Ac) Response Of Magnitude Gain For Fourth Order LC Ladder Butterworth Low-pass Filter Using VDTA

To study the time domain behavior, input signals comprised of 2 frequencies of 1MHz and amplitude of 500mV is applied. The transient response and its spectrum for input and output are shown severally in Fig 5.10.

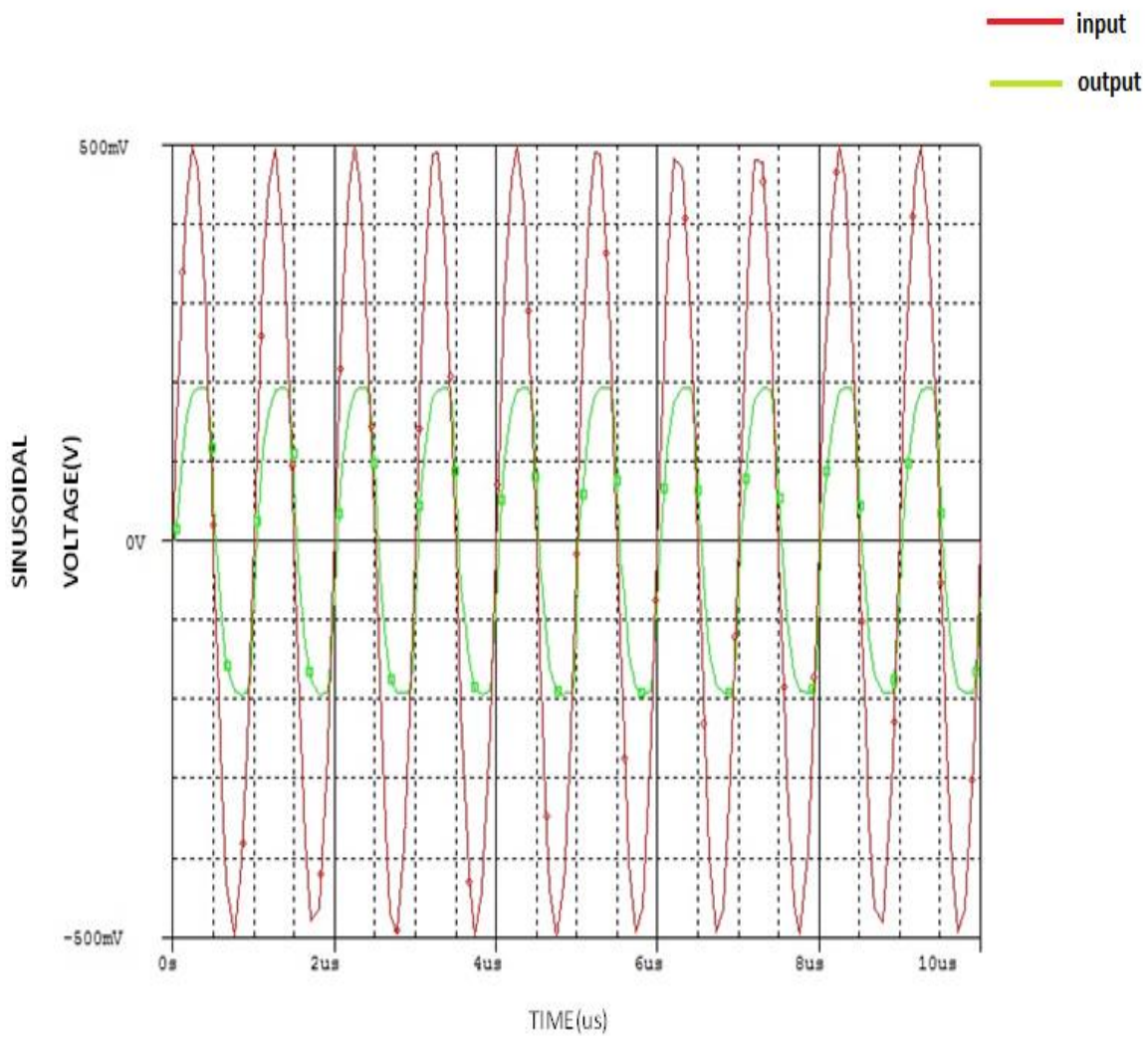

Fig 5.10. Transient Response for Input And Output For Fourth Order LC Ladder Butterworth Low-pass Filter Using VDTA

The filter parameters is also simulated for the cutoff frequency of 10 MHz. The power dissipation for this circuit is 2.16E-03watts, output noise is 5.298E-09V/Hz1/2 and %THD is within 5.926804E+01 % up to 500 mV p–p.

5.4.3. FIFTH ORDER LC LADDER BUTTERWORTH LOWPASS FILTER USING VDTA

The LC ladder (doubly terminated) representing a fifth order low-pass filter (Butterworth) at [91] 1rad/sec is shown in Fig.5.11(a) where R1=1Ω, CA=CB=1F and L=2H. Let us choose a minimum inductance ladder so that the first and last elements are capacitors. From the Table 1. We get the value of the elements referred to the normalized frequency. But to have frequency scaling we have to de-normalize the elements which depends on source, load resistance and cut-off frequency. Let us consider αmax=0.7. Therefore $\varepsilon = \sqrt{10^{0.07} - 1 = 0.4182}$ so that

$\omega_B = \epsilon^{-\frac{1}{n}}\omega_P$ =2*π*(0.4182)-1/5 *10MHz = 74.83Mrad/sec therefore f_b=11.91MHz

With these numbers, we de-normalize the resistors by multiplying by 1.5KΩ and the inductors and capacitors, by multiplying by,

$\frac{0.58\text{K}\Omega}{74.83\text{Mrad/sec}} = 7.8\mu H$ and $\frac{1}{0.58K\Omega \text{ x} 74.83\text{Mrad/sec}} = 23pF$

Therefore, C_A=C_C=0.618x23pF=14.2pF and C_B=2x23pF =46pF

L_1=L_2=12.6 μH , therefore, C_1=C_2=$g_{m1}g_{m2}L_1$ =12.6 μH x631 $\mu A/$Vx627 $\mu\frac{A}{V} = 5pF$

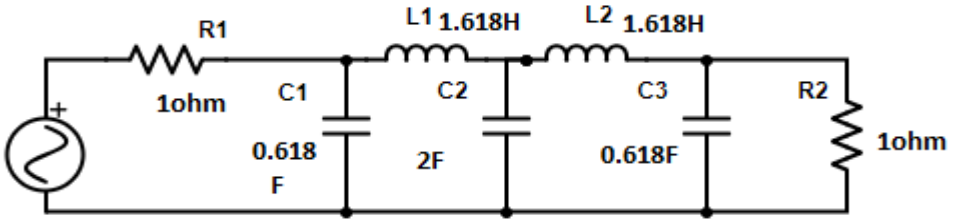

Fig 5.11(a) Fifth Order LC Ladder Butterworth Low-pass Filter (For normalized Frequency ω=1rad/sec)

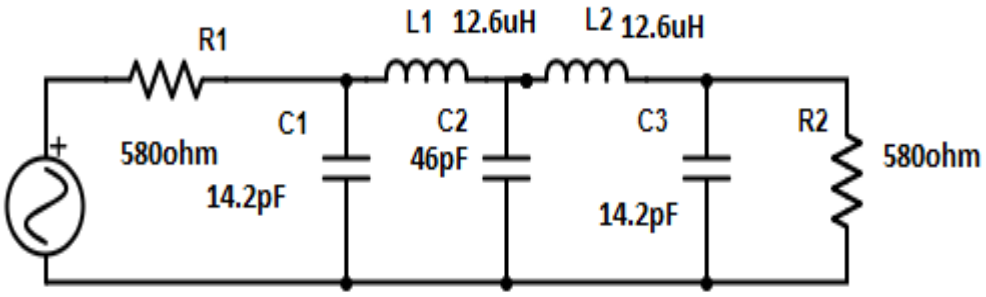

Fig 5.11(b) Fifth Order LC Ladder Butterworth Low-pass Filter

(For De-normalized For Frequency f=10MHz)

The transfer function of fifth order low-pass Butterworth filter is derived as follows:

At node 3, we get,

$$\frac{V_2}{sL_2} = (\frac{1}{R_2} + \frac{1}{sL_2} + sC_3)V_3 \tag{5.31}$$

Or,

$$V_2 = \frac{s^2L_2R_2C_3 + sL_2 + R_2}{R_2}V_3 \tag{5.32}$$

At node 2, we get,

$$\frac{V_1}{sL_1} = \left(sC_2 + \frac{1}{sL_1} + \frac{1}{sL_2}\right)V_2 - \frac{V_3}{sL_2} \tag{5.33}$$

Or,

$$V_1 = \left(s^2 L_1 C_2 + \frac{L_1}{L_2} + 1\right) V_2 - \frac{L_1}{L_2} V_3 \tag{5.34}$$

Or,

$$V_1 = \left(\frac{s^2 L_2 R_2 C_3 + s L_2 + R_2}{R_2}\right)\left(s^2 L_1 C_2 + \frac{L_1}{L_2} + 1\right) V_3 - \frac{L_1}{L_2} V_3$$

$$= \frac{s^4 L_1 L_2 C_2 C_3 R_2 + s^3 L_1 C_2 (R_2 + L_2) + s^2 C_3 R_2 (L_1 + L_2) + s(L_1 + L_2) + R_2}{R_2} V_3 \tag{5.35}$$

At node 1, we get,

$$\frac{V_{in}}{R_1} = \left(\frac{1}{R_1} + \frac{1}{sL_1} + sC_1\right) V_1 - \frac{V_2}{sL_1} \tag{5.36}$$

Or,

$$\frac{V_{in}}{R_1} = \left(\frac{s^4 L_1 L_2 C_2 C_3 R_2 + s^3 L_1 C_2 (R_2 + L_2) + s^2 C_3 R_2 (L_1 + L_2) + s(L_1 + L_2) + R_2}{R_2}\right)\left(\frac{1}{R_1} + \frac{1}{sL_1} + sC_1\right) V_3 - \left(\frac{s^2 L_2 R_2 C_3 + s L_2 + R_2}{R_2}\right)\frac{V_3}{sL_1} \tag{5.37}$$

Or,

$$\frac{V_3}{V_{in}} = \frac{R_2 L_1}{\begin{array}{c} s^5 C_1 C_2 C_3 L_1^2 L_2 R_2 + s^4\{L_1 L_2 L_3 C_1 R_2 + C_1 C_2 L_1^2 (R_2 + L_2)\} + s^3\{L_1 C_2 (R_2 + L_2) + C_1 L_1 C_3 R_2 \\ (L_1 + L_2) + L_1 L_2 C_2 C_3 R_1 R_2\} + \\ s^{2\{} C_1 L_1 (L_1 + L_2) + R_1 L_1 C_2 (R_2 + L_2) + \\ L_1 C_3 R_2 (L_1 + L_2)\} + s\{C_1 L_1 R_2 + L_1 (L_1 + L_2) + L_1 C_3 R_1 R_2\} + L_1 (R_1 + R_2) \end{array}}$$

(5.38)

This is the expression of transfer function of the fifth order LC ladder low-pass filter. To have Butterworth response the element parameters have been set accordingly.

Finally replacing the floating inductors as shown in Fig 5.12, L_1 and L_2 by VDTA based floating inductor presented in chapter 4, we get the active fifth order low-pass Butterworth filter

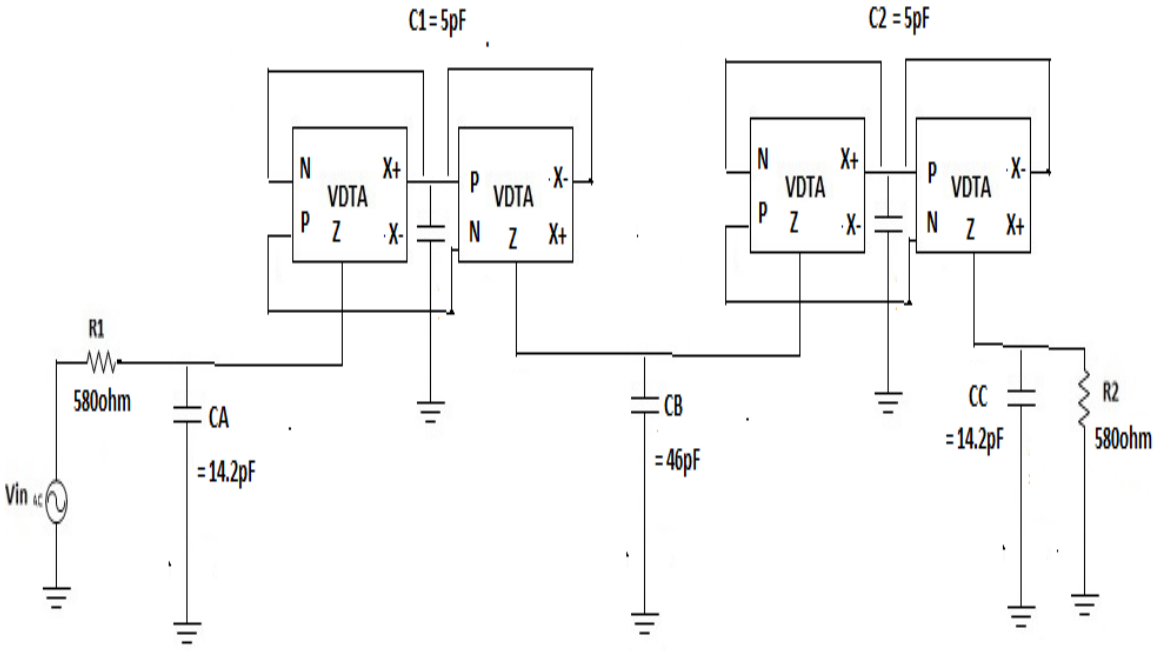

Fig 5.12. Fifth Order LC Ladder Butterworth Low-pass Filter Using VDTA

By simulation, as shown in Fig.5.13, we get the cutoff frequency to be 11.8552 MHz.

Therefore, error= $\frac{11.8552-11.91}{11.91}$x100%=-0.46%

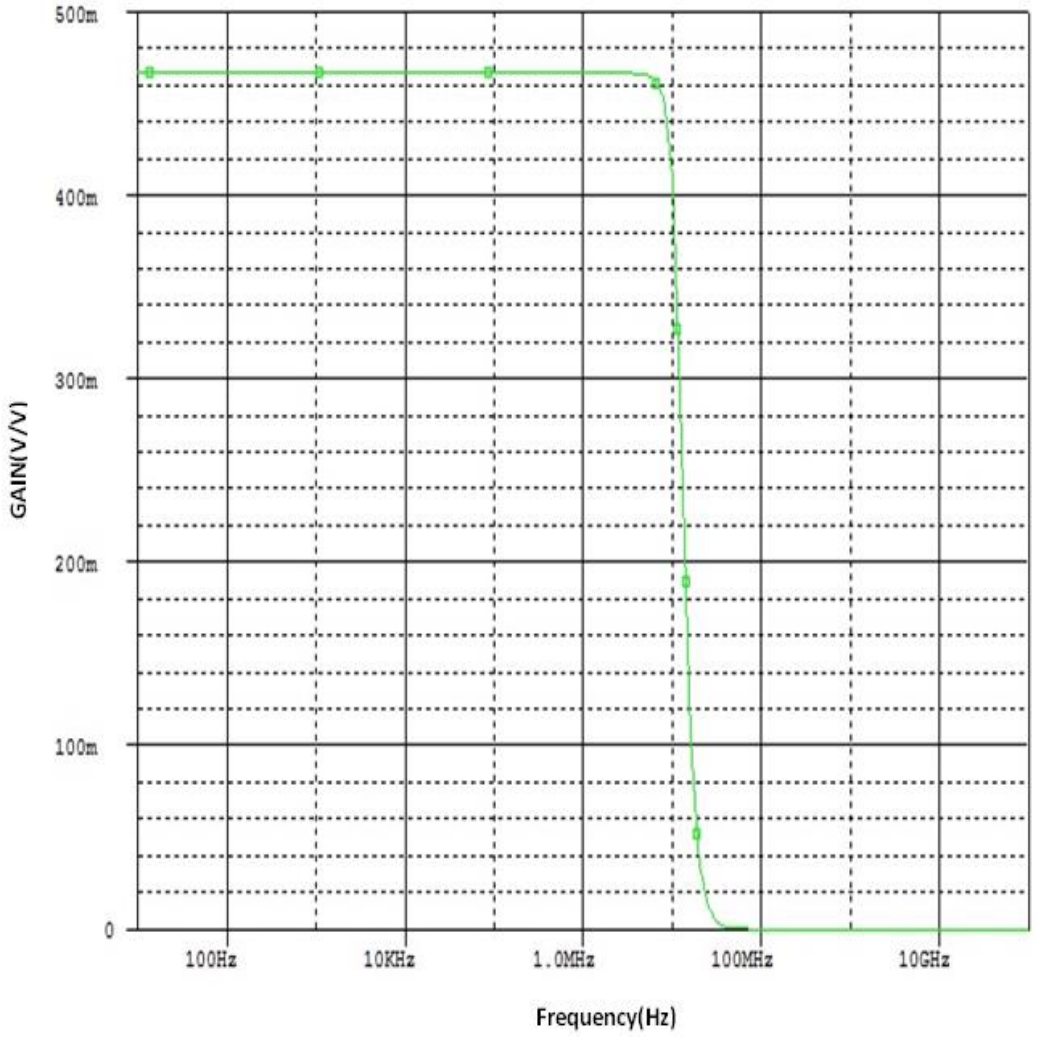

Fig 5.13. Frequency (Ac) Response Of Magnitude Gain For Fifth Order LC Ladder Butterworth Low-pass Filter Using VDTA

To study the time domain behavior, input signals comprised of 2 frequencies of 1MHz and amplitude of 500mV is applied. The transient response and its spectrum for input and output are shown in Fig 5.14.

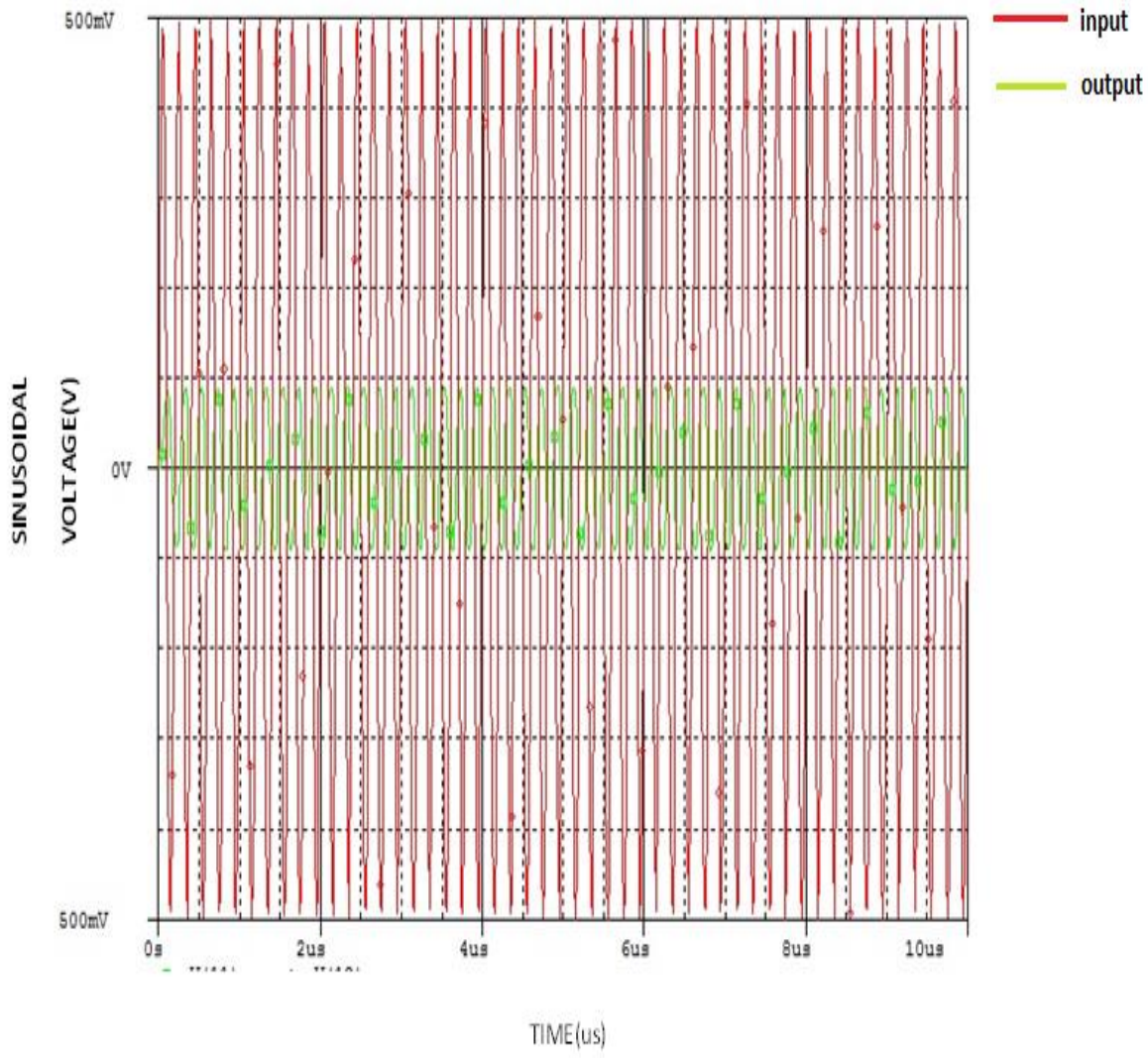

Fig 5.14. Transient Response for Input And Output For Fifth Order LC Ladder Butterworth Low-pass Filter Using VDTA

The filter parameter is also derived for the cutoff frequency of 10 MHz. The power dissipation for this circuit is 2.16E-03watts, output noise is 5.298E-09V/Hz1/2 and %THD is within 5.926804E+01 % up to 500 mV p–p.

5.4.4. SIXTH ORDER LC LADDER BUTTERWORTH LOWPASS FILTER USING VDTA

The LC ladder (doubly terminated) representing a sixth order low-pass filter (Butterworth) at [91] 1rad/sec is shown in Fig. 5.15(a), where R1=1Ω, CA=CB=1F and L=2H. Let us choose a minimum inductance ladder so that the first and last elements are capacitors. From the table 1, we get the value of the elements referred to the normalized frequency. But to have frequency scaling we have to de-normalize the elements which depends on source, load resistance and cut-off frequency. Let us consider αmax=0.7. Therefore $\varepsilon = \sqrt{10^{0.07} - 1 = 0.4182}$ so that

$\omega_B = \epsilon^{-\frac{1}{n}}\omega_P$ =2*π*(0.4182)-1/6 *10MHz = 72.63Mrad/sec therefore f_b=11.56MHz

With these numbers, we de-normalize the resistors by multiplying by 1.5KΩ and the inductors and capacitors, by multiplying by,

$\frac{1.8\text{K}\Omega}{72.63\text{Mrad/sec}} = 24.7\mu H$ and $\frac{1}{1.8K\Omega \text{ x} 72.63\text{Mrad/sec}} = 7.65pF$

Therefore, CA= 1.414x7.65pF=10.8pF, CB=1.932x7.65pF =14.78pF and CC=0.5176x7.65pF =3.95pF

L_1= 12.8 μH , therefore, C1= $g_{m1}g_{m2}L_1$ =12.8 μH x631 $\mu A/\text{V}$x627 $\mu\frac{A}{\text{V}} = 5pF$

L_2= 47.88 μH , therefore, C_2= $g_{m1}g_{m2}L_2$ =47.88 μH x631 $\mu A/\text{V}$x627 $\mu\frac{A}{\text{V}} = 18.9pF$

L_3=35 μH , therefore, C_3= $g_{m1}g_{m2}L_3$ =35 μH x631 $\mu A/\text{V}$ x 627 $\mu\frac{A}{\text{V}} = 13.8pF$

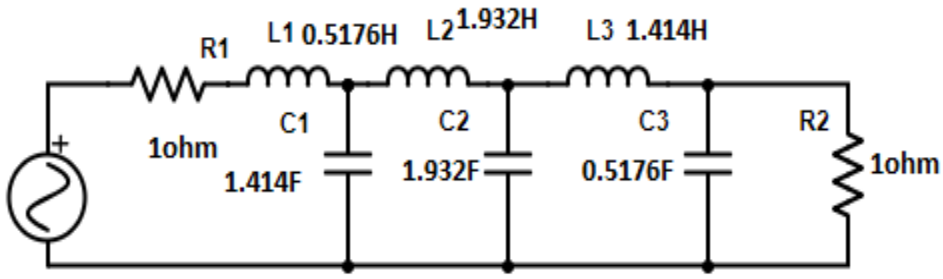

Fig 5.15(a) Sixth Order LC Ladder Butterworth Low-pass Filter

(For Normalized Frequency ω=1rad/sec)

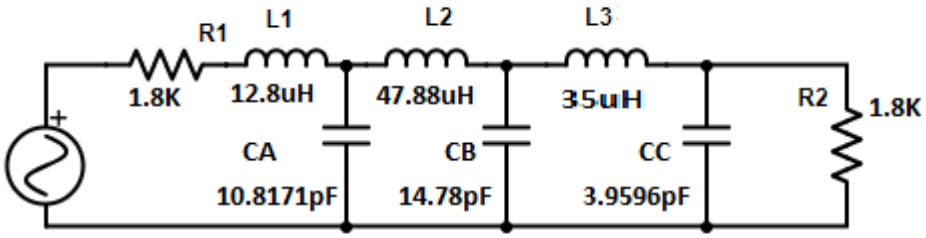

Fig 5.15(b) Sixth Order LC Ladder Butterworth Low pass Filter

(De-normalized For Frequency f=10MHz)

The transfer function of sixth order low-pass filter is derived as follows:

At node 3, we get,

$$\frac{V_2}{sL_3} = (\frac{1}{R_2} + \frac{1}{sL_3} + sC_3)V_3 \qquad (5.39)$$

Or,

$$V_2 = \frac{s^2 C_3 L_3 + sL_3 + R_2}{R_2} V_3 \tag{5.40}$$

At node 2, we get,

$$\frac{V_1}{sL_2} = \left(\frac{1}{sL_2} + \frac{1}{sL_3} + sC_2\right) V_2 - \frac{V_3}{sL_3} \tag{5.41}$$

Or,

$$\frac{V_1}{sL_2} = \left(\frac{s^2 C_3 L_3 + sL_3 + R_2}{R_2}\right) \left(\frac{1}{sL_2} + \frac{1}{sL_3} + sC_2\right) V_3 - \frac{V_3}{sL_3} \tag{5.42}$$

Or,

$$V_1 = \frac{S^4 L_2 L_3 C_2 C_3 + s^3 L_2 L_3 C_2 + S^2 (L_2 C_2 R_2 + L_2 C_3 + L_3 C_3) + S(L_2 + L_3) + R_2}{R_2} V_3 \tag{5.43}$$

At node 1, we get,

$$\frac{V_{in}}{R_1 + sL_1} = \left(\frac{1}{R_1 + sL_1} + sC_1 + \frac{1}{sL_2}\right) V_1 - \frac{V_2}{sL_2} \tag{5.44}$$

Or,

$$\frac{V_{in}}{R_1 + sL_1}$$
$$= \left(\frac{S^4 L_2 L_3 C_2 C_3 + s^3 L_2 L_3 C_2 + S^2(L_2 C_2 R_2 + L_2 C_3 + L_3 C_3) + S(L_2 + L_3) + R_2}{R_2}\right)\left(\frac{1}{R_1 + sL_1}\right.$$
$$\left. + sC_1 + \frac{1}{sL_2}\right) V_3 - \left(\frac{s^2 C_3 L_3 + sL_3 + R_2}{R_2}\right)\frac{V_3}{sL_2}$$

(5.45)

Or,

$$\frac{V_3}{V_{in}}$$
$$=$$
$$\frac{R_2 L_2}{s^6 L_1 L_2^2 L_3 C_1 C_2 C_3 + s^5 L_2^2 L_3 C_1 C_2 (L_1 + R_{1C_3}) + s^4 \begin{Bmatrix} L_1 L_2 C_1 (L_2 C_2 R_2 + C_3 L_3 + C_3 L_2) + \\ L_2^2 C_1 R_1 C_2 L_3^2 + \\ L_2 L_3 C_2 C_3 (L_1 + L_2) \end{Bmatrix}}$$
$$+$$
$$s^3\{L_1 L_2 C_1 (L_2 + L_3) + L_2 C_1 R_1$$
$$(L_2 C_2 R_2 + L_2 C_3 + L_3 C_3) + L_2 L_3 C_2 (L_1 + L_2) + L_2 L_3 C_2 C_3 R_1\} + s^2\{L_1 L_2 C_1 R_1 + L_2 C_1 R_1 (L_2 + L_3) +$$
$$L_1 (L_2 C_2 R_2 + C_3 L_2) +$$
$$L_2 (L_2 C_2 R_2 + L_2 C_3 + L_3 C_3) + R_1$$
$$L_2 L_3 C_2 C_3 + s\{C_1 L_2 R_1 R_2 + L_1 L_2 + L_2^2 + L_2 L_3 + R_1 (L_2 R_2 C_2 + C_3 L_2\} + L_2 (R_1 + R_2)$$

(5.46)

This equation is the expression of the transfer function of the sixth order LC low-pass filter. The element parameters are set so as to get Butterworth response.

Finally in Fig.5.16, replacing the floating inductors L_1 and L_2 by VDTA based floating inductor presented in chapter, we get the active sixth order low-pass Butterworth filter

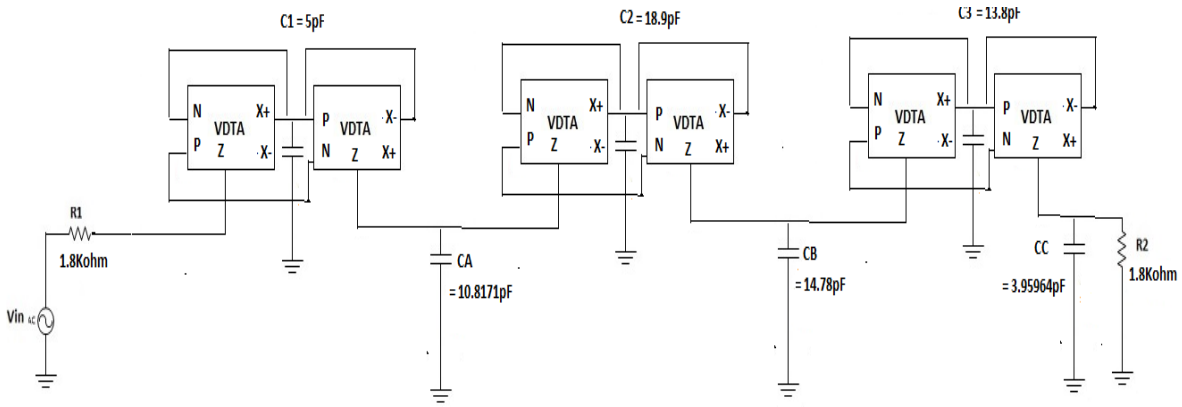

Fig 5.16. Sixth Order LC Ladder Butterworth Low-pass Filter Using VDTA

By simulation, as shown in Fig.5.17, we get the cutoff frequency to be 11.04MHz.

Therefore, error= $\frac{11.0492-11.56}{11.56}$x100%=-4.4185%

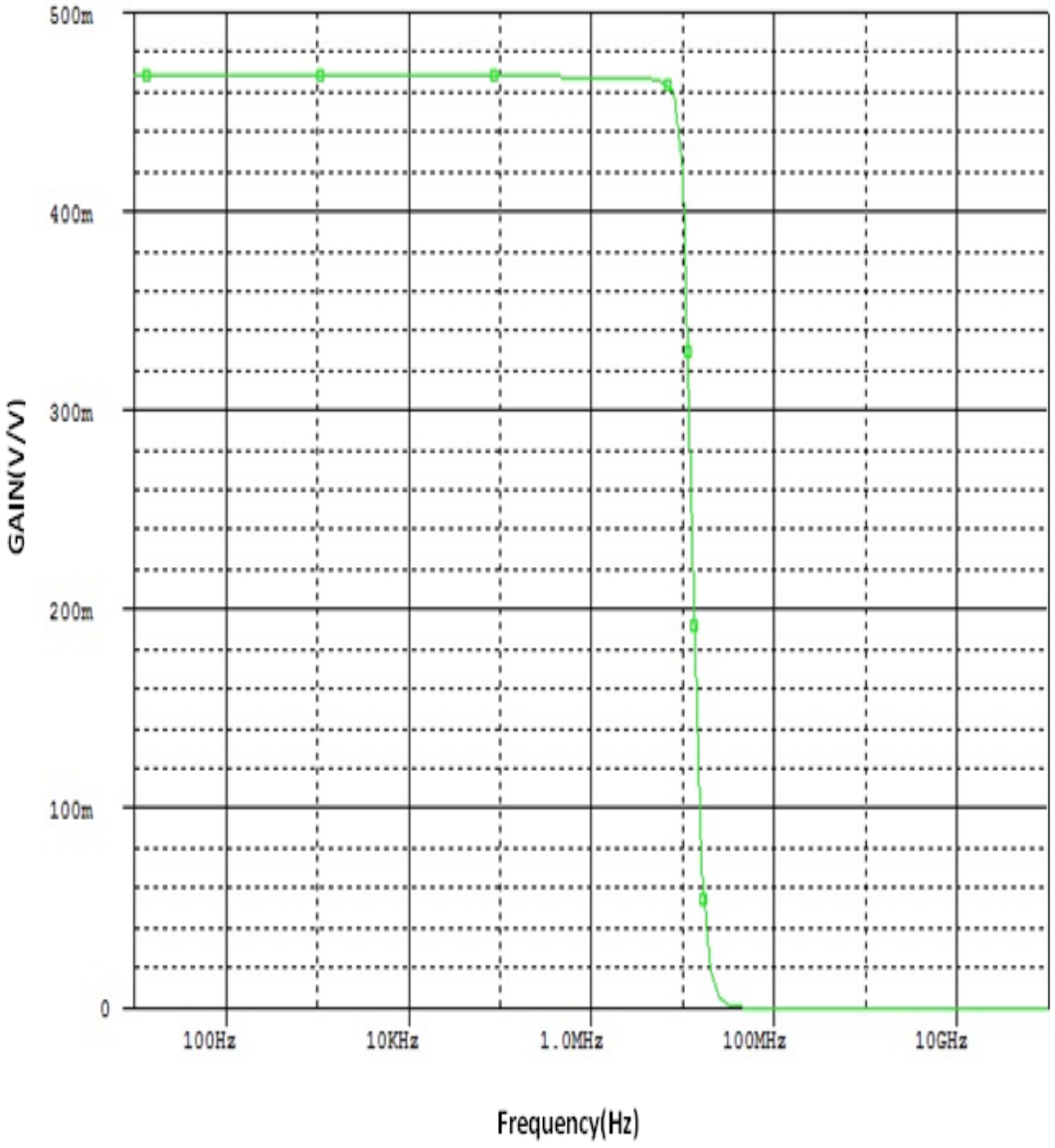

Fig.5.17. Frequency (Ac) Response Of Magnitude Gain For Sixth Order LC Ladder Butterworth Low pass Filter Using VDTA

To study the time domain behavior, input signals comprised of 2 frequencies of 1MHz and amplitude of 500mV is applied. The transient response and its spectrum for input and output are shown in Fig 5.18.

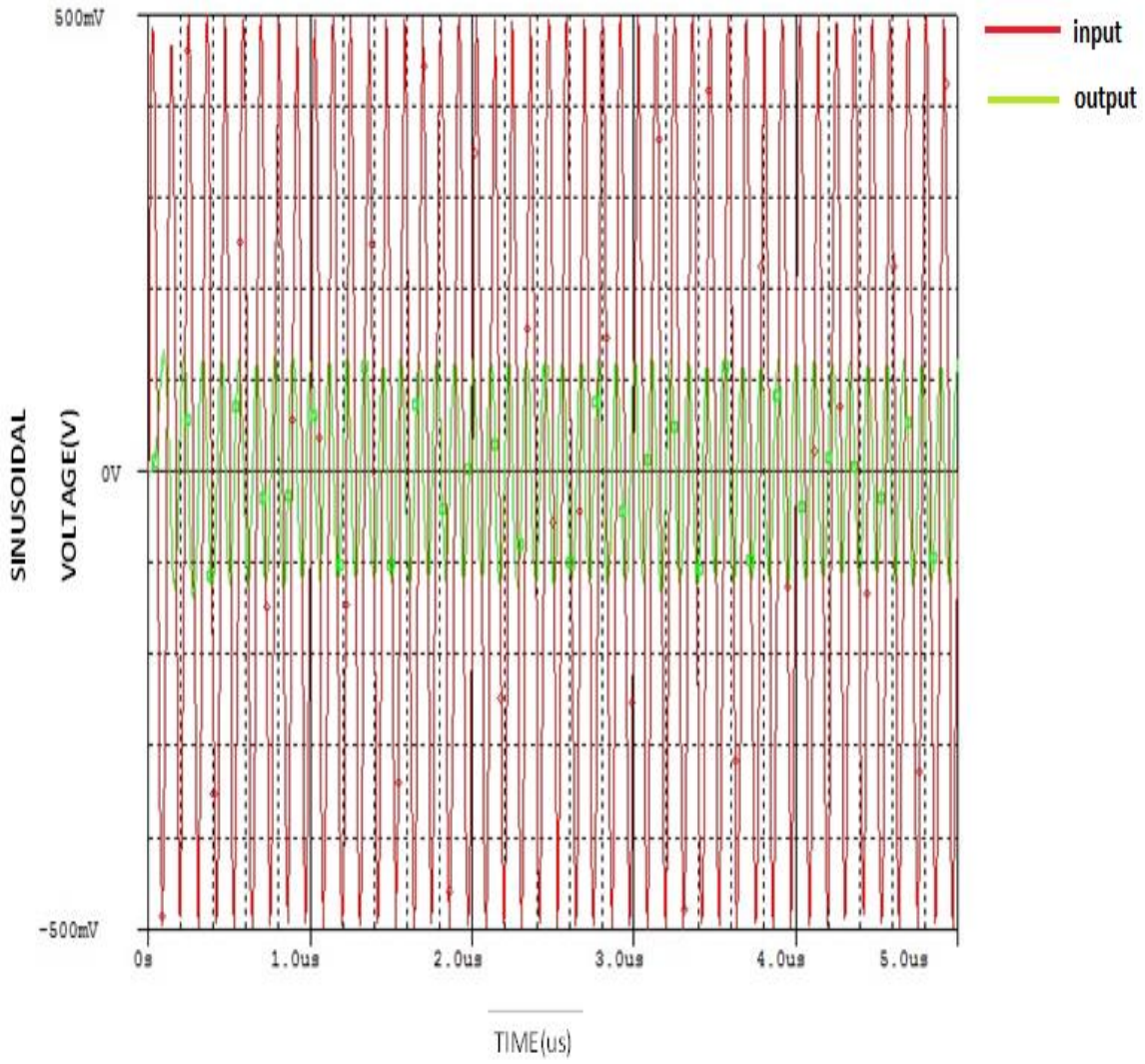

Fig 5.18. Transient Response For Input And Output For Sixth Order LC Ladder Butterworth Low pass Filter Using VDTA

The filter topology is also simulated for the same cutoff frequency of 10 MHz. The power dissipation for this circuit is 3.24E-03Watts, output noise is 9.335E-09V/Hz1/2 and %THD is within 1.974631E+00% up to 500 mV p–p.

5.4.5. 6th ORDER LC LADDER BUTTERWORTH HIGHPASS FILTER USING VDTA

We want to design a 6th order LC ladder high-pass filter [91] having high cutoff frequency at 10MHZ.

Let us consider αmax=0.7. Therefore $\varepsilon = \sqrt{10^{0.07} - 1 = 0.4182}$ so that

$\omega_B = \epsilon^{-\frac{1}{n}}\omega_P$ =2*π*(0.4182)-1/6 *10MHz = 72.63Mrad/sec therefore f_b=11.56MHz

First we determine the frequency transformation to convert the high pass specifications into those of a prototype low-pass. Let us normalize the frequency axis by ω_n=2πkrad/s; then it is expected to have the transformation as shown in Fig.5.19.

Now in high-pass specification, the capacitor in low-pass filter C_{lp} is converted to inductor in high-pass filter H_{hp} and inductor in low-pass filter H_{lp} is converted to capacitor in high-pass filter C_{hp} by the relation,

$$Hhp = \frac{R}{C_{lp}\omega_B}$$

and

$$Chp = \frac{1}{RL_{lp}\omega_B}$$

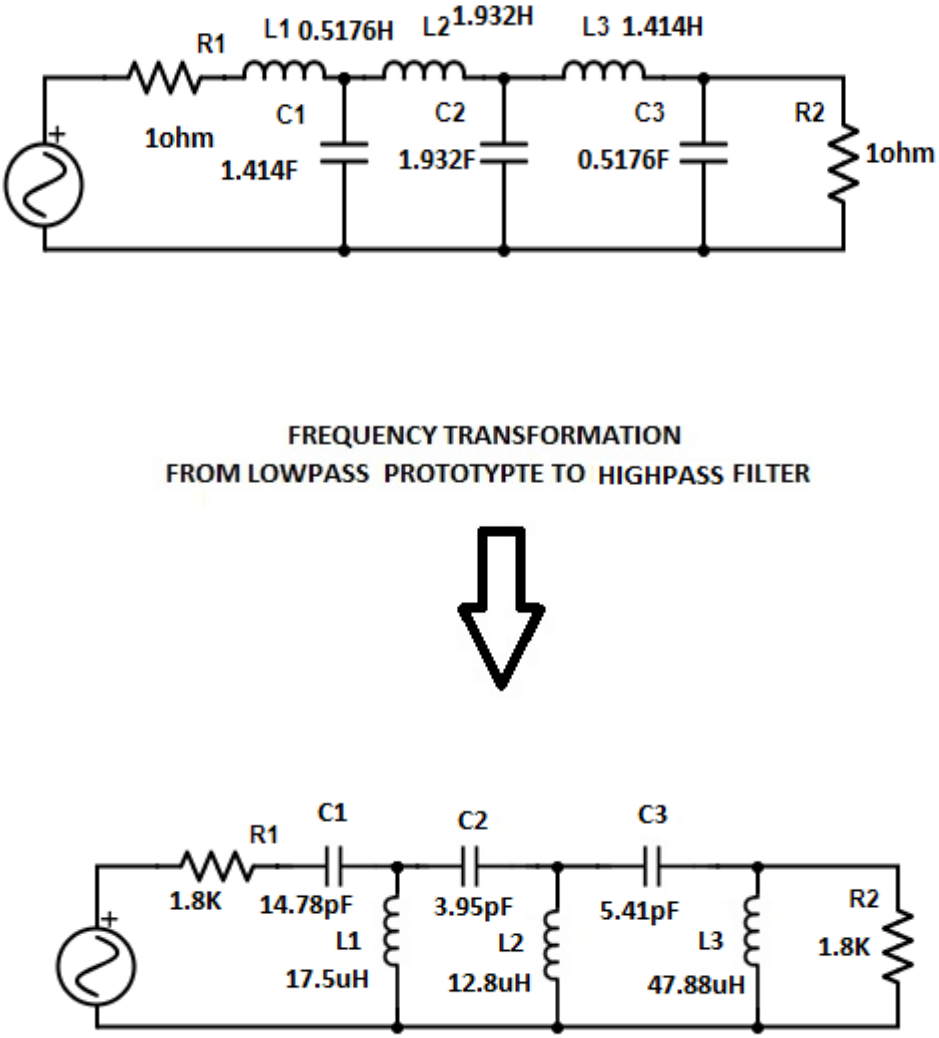

Fig.5.19. Sixth Order High-pass Filter Designed For Frequency 10MHz From Its Equivalent Low-pass Prototype

To have 11.56MHz cutoff frequency, I have de-normalized the elements accordingly and used 1.8kΩ doubly terminated resistors at source and load terminals.

The transfer function of the sixth order LC high-pass filter is derived as follows:

At node 3, we get,

$$sC_3V_2 = (\frac{1}{R_2} + \frac{1}{sL_3} + sC_3)V_3$$

(5.47)

Or,

$$V_2 = \frac{s^2L_3C_3 + sL_3 + R_2}{s^2L_3C_3R_2}V_3$$

(5.48)

At node 2, we get,

$$sC_2V_1 = \left(sC_2 + sC_3 + \frac{1}{sL_2}\right)V_2 - sC_3V_3 \quad (5.49)$$

Or,

$$sC_2V_1 = (\frac{s^2L_3C_3 + sL_3 + R_2}{s^2L_3C_3R_2})\left(sC_2 + sC_3 + \frac{1}{sL_2}\right)V_3 - sC_3V_3$$

(5.50)

Or,

$$V_1 = \frac{s^4L_2L_3C_2C_3 + s^3L_3(C_2 + C_3) + s^2\{L_3C_3 + R_2(C_2 + C_3)\} + sL_3 + R_2}{s^4L_2L_3C_2C_3R_2}V_3$$

(5.51)

At node 1, we get,

$$\frac{V_{in}}{R_1 + \frac{1}{sC_1}} = \left(\frac{1}{R_1 + \frac{1}{sC_1}} + \frac{1}{sL_1} + sC_2\right)V_1 - sC_2V_2$$

(5.52)

Or,

$$\frac{V_{in}}{R_1+\frac{1}{sC_1}}$$

$$=\left(\frac{1}{R_1+\frac{1}{sC_1}}+\frac{1}{sL_1}\right.$$

$$\left.+sC_2\right)\left(\frac{s^4L_2L_3C_2C_3+s^3L_3(C_2+C_3)+s^2\{L_3C_3+R_2(C_2+C_3)\}+sL_3+R_2}{s^4L_2L_3C_2C_3R_2}\right)V_3$$

$$-sC_2\left(\frac{s^2L_3C_3+sL_3+R_2}{s^2L_3C_3R_2}\right)V_3$$

(5.53)

Or,

$$\frac{V_3}{V_{in}}$$

$$=\frac{s^6L_1L_2L_3C_1C_2C_3R_2}{\begin{array}{c}s^6\{L_1L_3C_1C_2R_2(C_2+C_3)+L_1L_2L_3C_2C_3R_2(C_1+C_2)-L_1L_2L_3C_2C_3-\\L_1L_2L_3C_1C_2R_1)+\\s^5[L_1C_1C_2R_1\{C_3L_3+R_2(C_2+C_3)\}+L_1L_3\\(C_1+C_2)\\(C_2+C_3)+L_2L_3C_2C_3R_1\end{array}}$$

$$\begin{array}{c}-L_1L_2L_3C_2-L_1L_2C_1C_2R_1R_2]+s^4[L_1L_3C_1C_2R_1+L_1(C_1+C_2)\{C_3L_3+R_2(C_2+C_3)\}+\\L_3C_1R_1(C_2+C_3)+L_2L_3C_2C_3-L_1L_2C_2R_2]+\\s^3[C_1C_2R_1R_2+L_1L_3\,(C_1+C_2)\\+R_1C_1\{C_3L_3+R_2(C_2+C_3)\}+L_3(C_2+C_3)]+s^2\{L_1R_2(C_1+C_2)+L_3C_1R_1+C_3L_3+\\R_2(C_2+C_3)\}+s(C_1R_1+L_3)+R_2\end{array}$$

(5.54)

The equation thus derived is the expression of LC ladder high-pass filter. The element parameters are accordingly set so as to have Butterworth Response.

Now in this design we replace the grounded inductors with VDTA obtained in chapter 5.

The 6th order high-pass filter using VDTA is shown in fig 5.20.

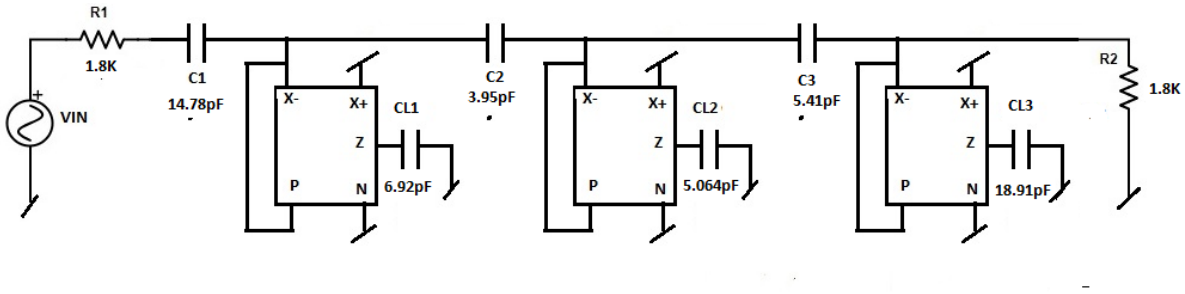

Fig.5.20. 6th Order LC Ladder Butterworth Highpass Filter Using VDTA

Where

$C_{L1}=g_{m1}g_{m2}L_1=6.92pF$

$C_{L2}=g_{m1}g_{m2}L_2=5.064pF$

$C_{L3}= g_{m1}g_{m2}L_3=18.91pF$

By simulation, as shown in Fig.5.21, we get the cut-off frequency to be 12.1032MHz

Therefore the error will be,

=

$$\frac{12.1032-11.56}{11.56}x100\% = 4.698\%$$

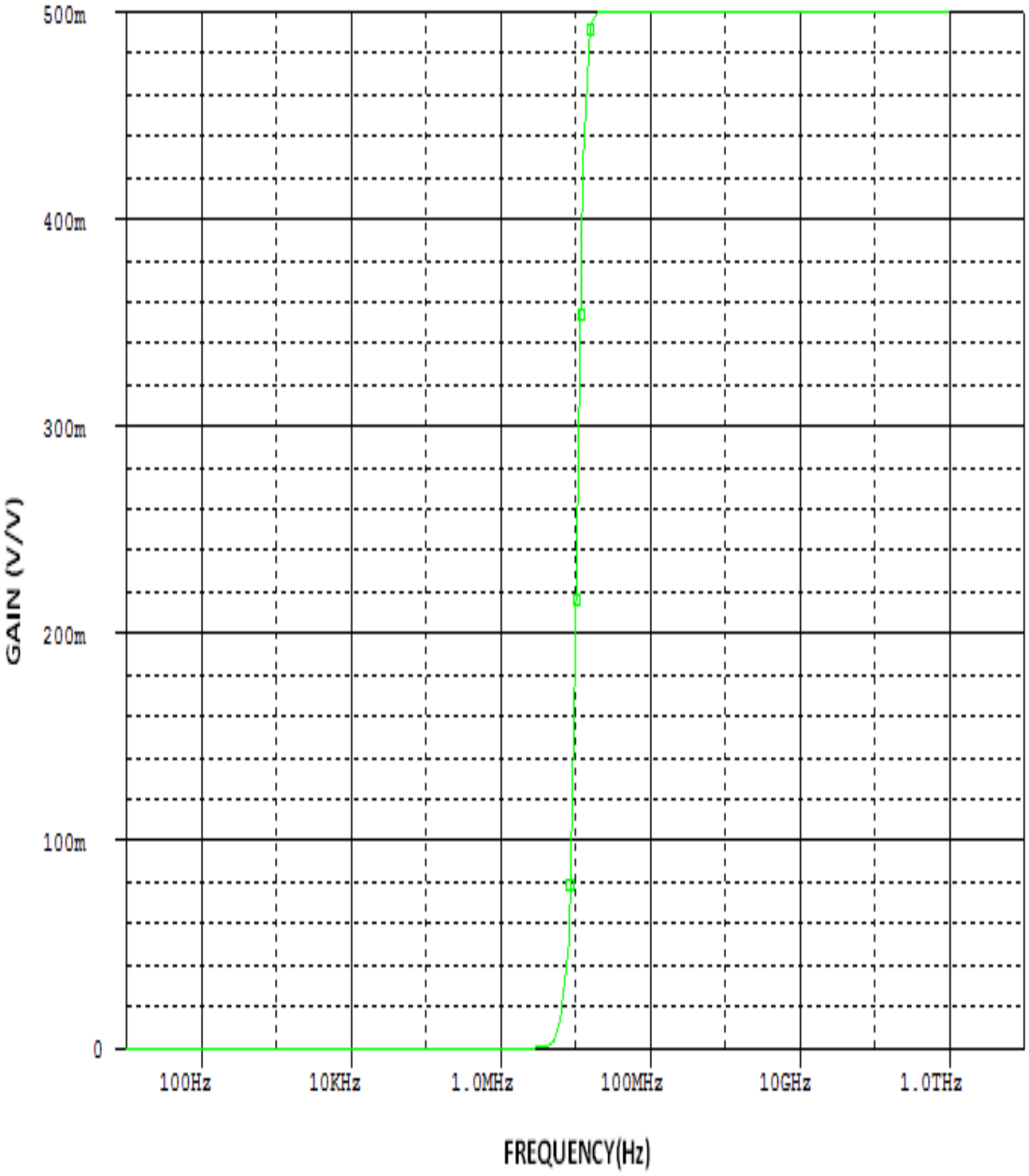

Fig.5.21. Frequency (Ac) Response of Magnitude Gain For Sixth Order LC Ladder Butterworth High-pass Filter Using VDTA

To study the time domain behavior, input signals comprised of 2 frequencies of 1MHz and amplitude of 500mV is applied. The transient response and its spectrum for input and output are shown in Fig 5.22.

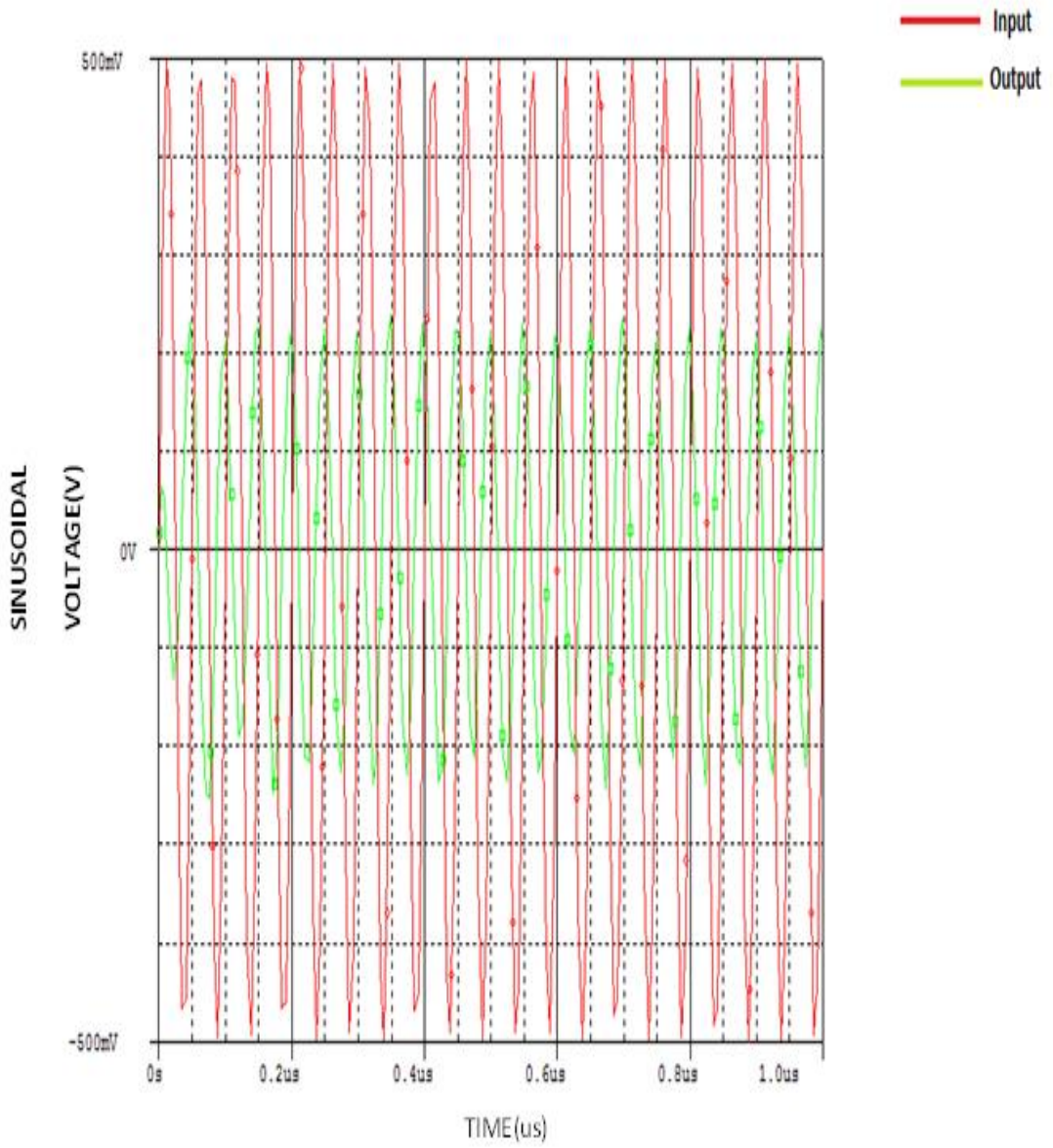

Fig 5.22. Transient Response for Input And Output For Sixth Order LC Ladder Butterworth High-pass Filter Using VDTA

The filter topology is also simulated for the same center frequency of 10 MHz. The power dissipation for this circuit is 1.62E-03Watts, output noise is 9.132E-09V/Hz1/2 and %THD is within 6.309321E+01% up to 500 mV p–p.

5.4.6. 8th ORDER LC LADDER BUTTERWORTH BANDPASS FILTER USING VDTA

We want to design a LC ladder band-pass filter [91] having pass-band Centre frequency at 10MHZ and maximally flat pass-band with bandwidth of 5 MHz.

First we determine the frequency transformation to convert the band-pass specifications into those of a prototype low-pass. Let us normalize the frequency axis by $\omega_n=2\prod$ krad/s; then, I have the transformation.

$$S = \frac{1}{B}\frac{s^2 + \omega_o^2}{s}$$

Where B is the bandwidth and ω_o is the center frequency in radian

The band-pass filter which is obtained by transformation is illustrated in fig 5.23

In band-pass filter the inductor in low-pass prototype is replaced with a series branch of inductor and capacitor whose value can be calculated as $Lseries = \frac{L}{B}xR$ and $Cseries = \frac{B}{\omega_o^2 L}x\frac{1}{R}$ and the capacitor is replaced with inductor and capacitor in parallel branch as $Lparallel = \frac{B}{\omega_o^2 C}xR$ and $Cparallel = \frac{C}{B}x\frac{1}{R}$

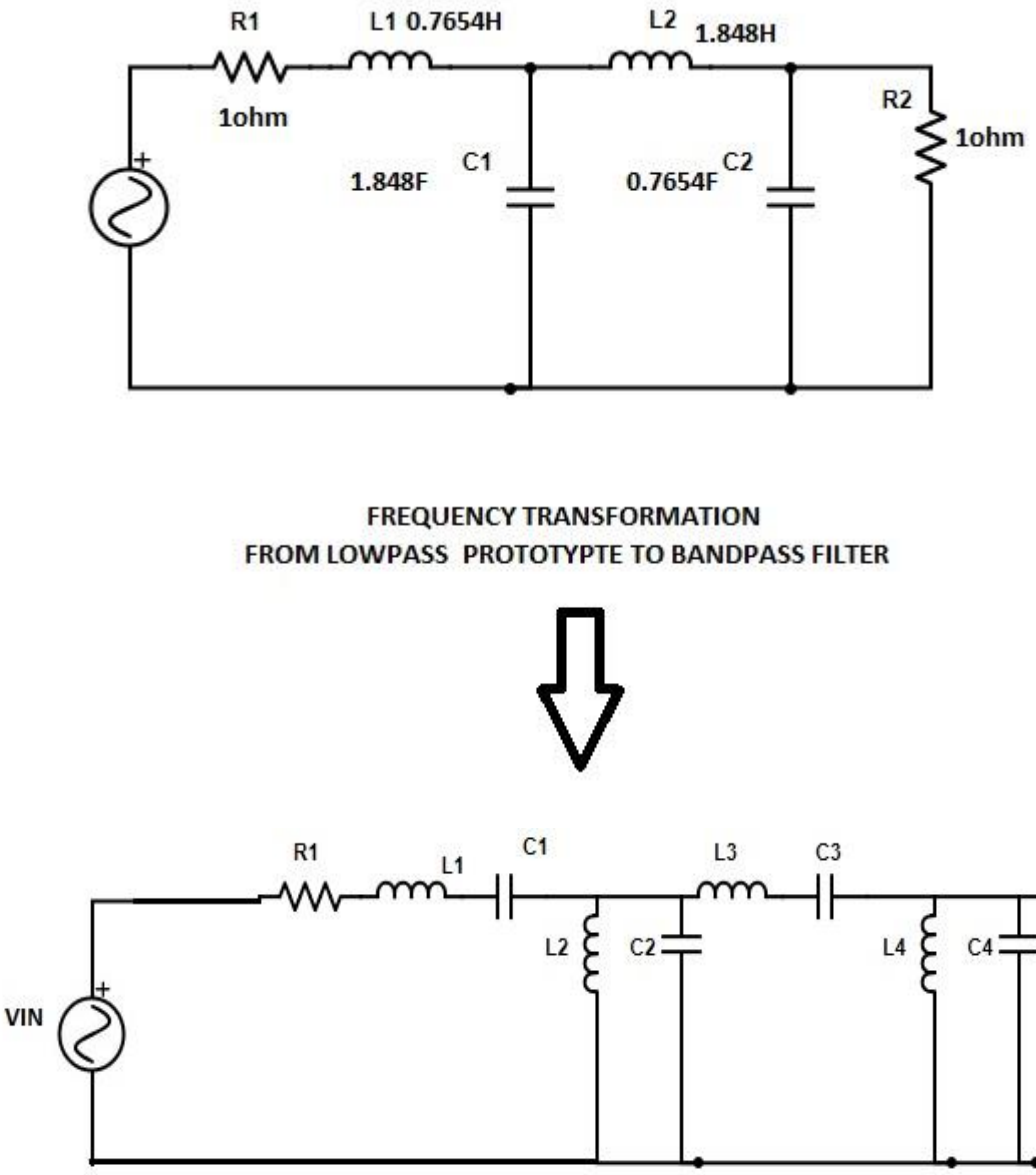

Fig.5.23. 8th Order Band-pass Filter Designed For Frequency 10MHz From Its Equivalent Low-pass Prototype

Where L_1=31.18µH L_2=5.5 µH L_3=75.3 µH L_4=13.3 µH

And C_1=8.122pF C_2=45.95pF C_3=3.36pF C_4=19pF

Now in this design we replace the floating and grounded inductors with VDTA obtained in chapter

The 8th order band-pass filter using VDTA is shown in fig 5.24.

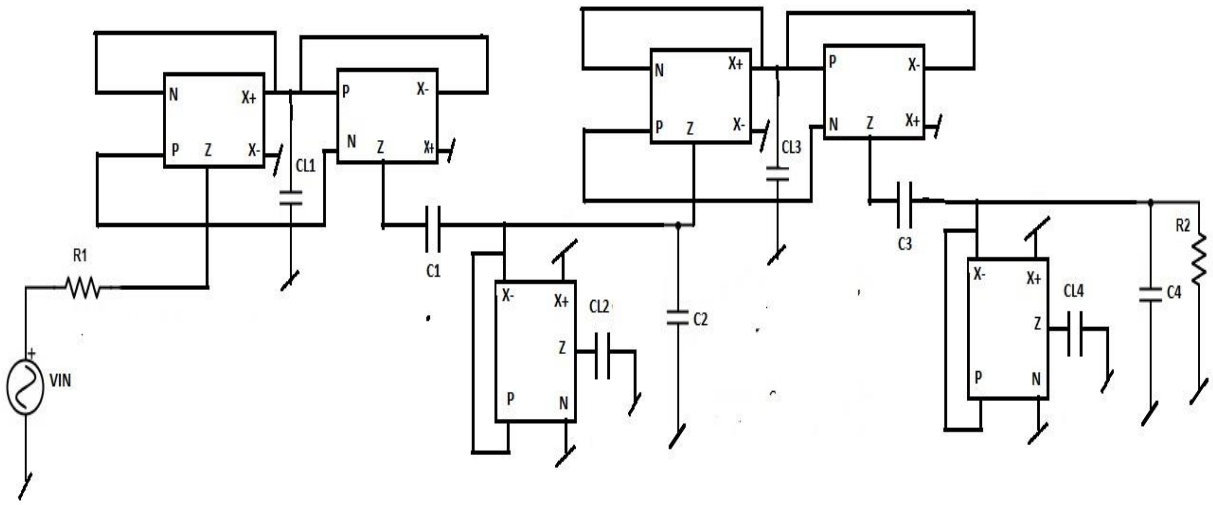

Fig.5.24. 8th Order LC Ladder Butterworth Band-pass Filter Using VDTA

Where

$C_{L1}=g_{m1}g_{m2}L_1=12.33pF$

$C_{L2}=g_{m1}g_{m2}L_2=2.18pF$

$C_{L3}= g_{m1}g_{m2}L_3=29.79pF$

$C_{L4}=g_{m1}g_{m2}L_4=5.26pF$

By simulation, as shown in Fig. 5.25 and 5.26, we get the center frequency to be 10MHZ and the bandwidth is 4.712MHz

Therefore the error will be = $\frac{4.712-5}{5}$x100%=-5.76%

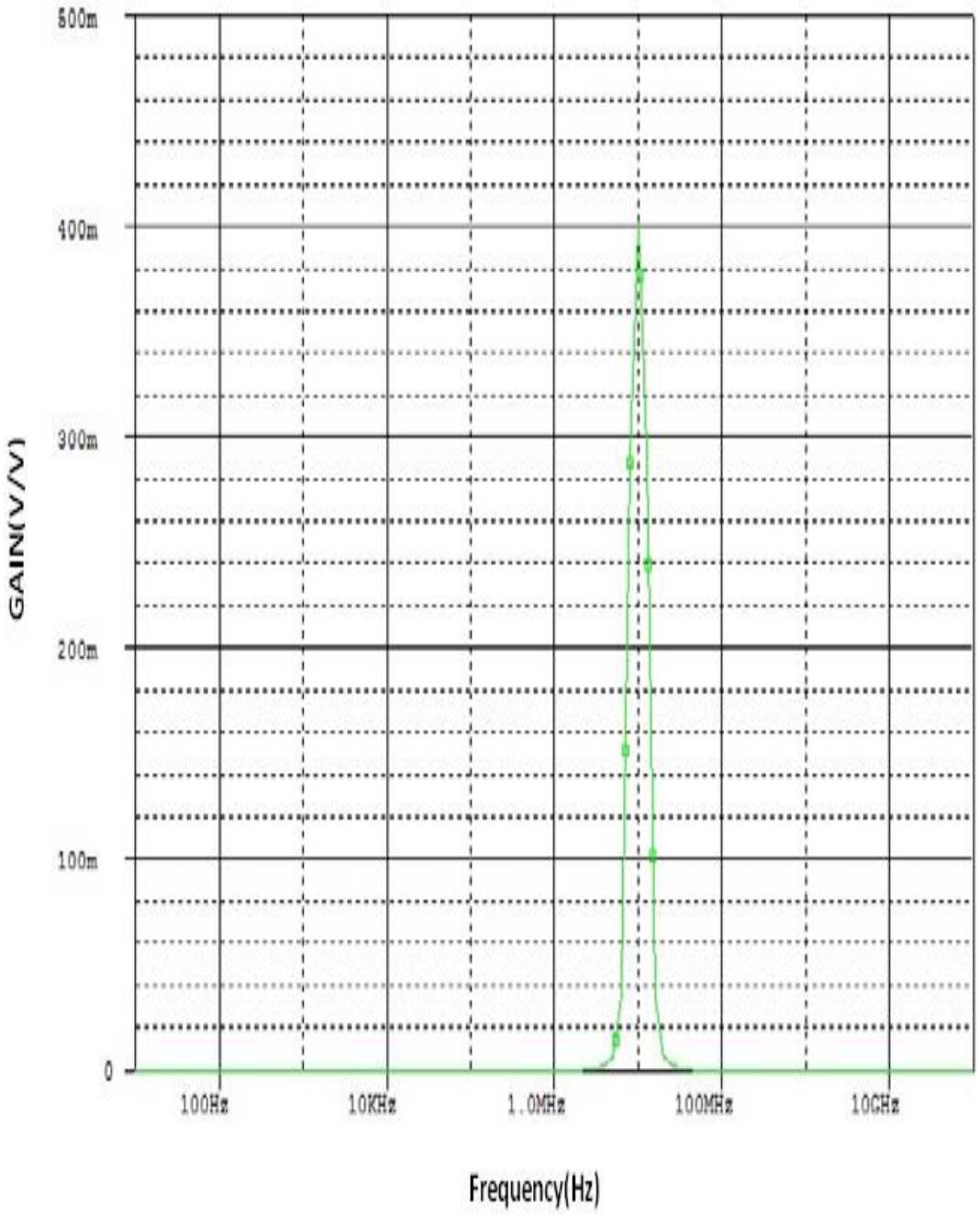

FIG.5.25. Frequency (Ac) Response Of Magnitude Gain For 8th Order LC Ladder Butterworth Band-pass Filter Using VDTA

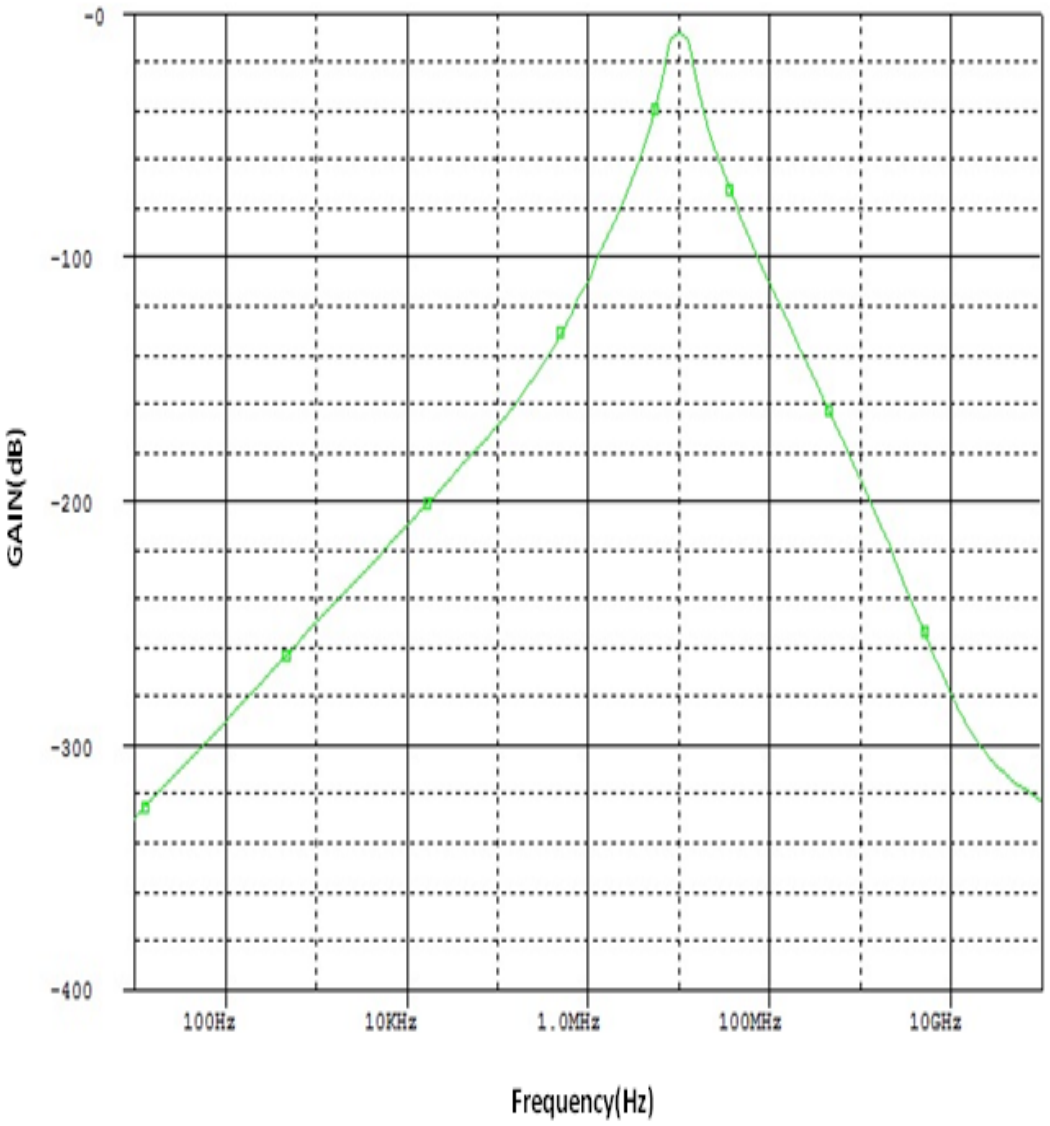

Fig. 5.26. Frequency (Ac) Response Of Magnitude Gain for 8th Order LC Ladder Butterworth Band-pass Filter Using VDTA (In Logarithmic Scale)

The filter parameters are also derived for the cutoff frequency of 10 MHz. The power dissipation for this circuit is 3.24E-03Watts, output noise is 1.273E-08V/Hz1/2 and %THD is within 5.034543E+03 % upto 500mV p–p.

5.4.7. 10th ORDER LC LADDER BUTTERWORTH BAND REJECT FILTER USING VDTA

We want to design a LC ladder band-stop filter [91] having pass-band Centre frequency at 10MHZ and maximally flat pass-band with bandwidth of 5MHz.

First we determine the frequency transformation to convert the band-stop specifications into those of a prototype low-pass. Let us normalize the frequency axis by $\omega_n=2\prod$ krad/s; then we have the transformation as shown in Fig 5.27.

In band-stop filter the inductor in low-pass prototype is replaced with inductor and capacitor in parallel branch as $Lparallel = \frac{BL}{\omega_o^2} xR$ and $Cparallel = \frac{1}{BL} x \frac{1}{R}$ and the capacitor is replaced with a series branch of inductor and capacitor whose value can be calculated as $Lseries = \frac{1}{BC} xR$ and $Cseries = \frac{BC}{\omega_o^2} x \frac{1}{R}$.

A notch filter is easily realized with the VDTA and ten external reactive elements (inductors and capacitances) as shown in Figure 5.28 which shows a 10MHz notch filter.

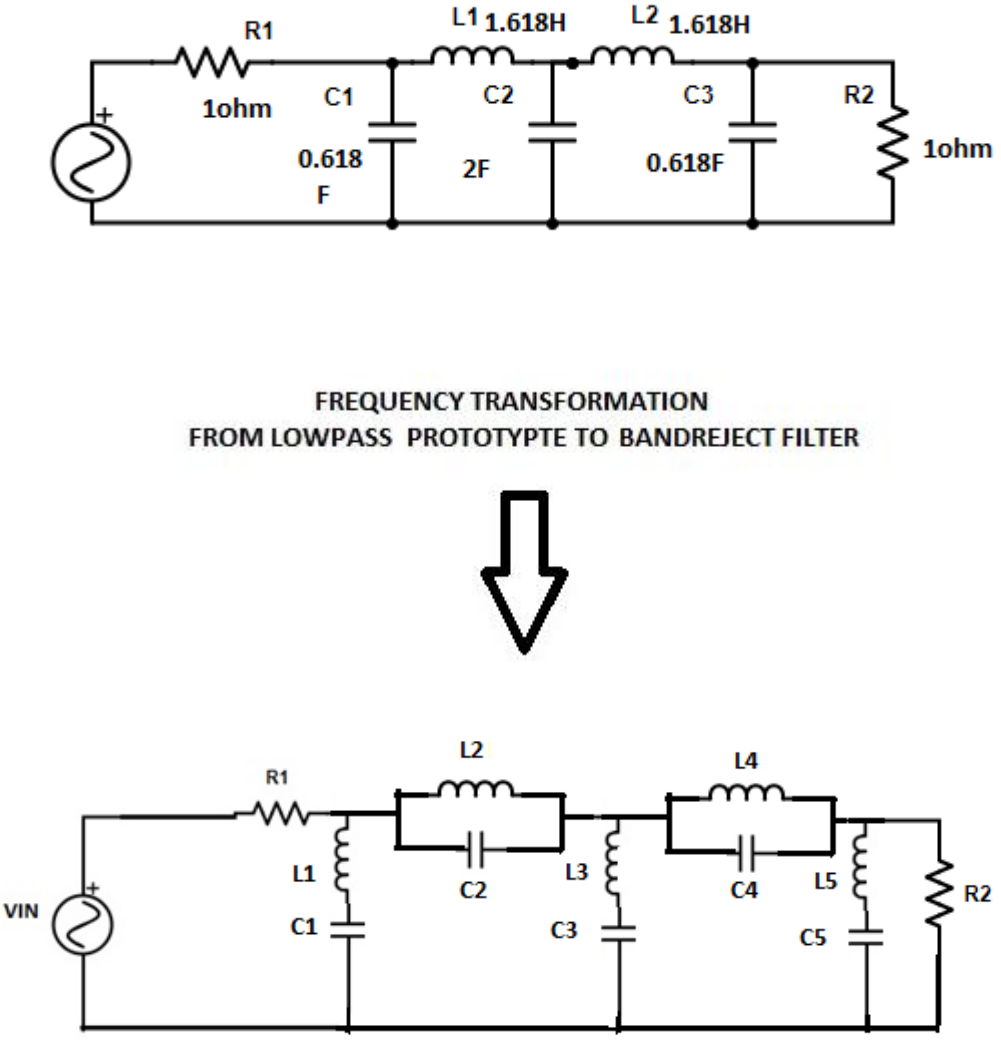

Fig.5.27. 10th ORDER Band-reject Filter Designed For Frequency 10MHz From Its Equivalent Low-pass Prototype

Where $R_1=R_2=1.59K\Omega$

$L_1=L_5=81.9\mu H$ $L_2=L_4=20.46\ \mu H$ $L_3=25.3\ \mu H$

And $C_1=C_5=3.09pF$ $C_2=C_4=12.37pF$ $C_3=10pF$

Now in this design we replace the floating and grounded inductors with VDTA obtained in chapter 4.

The 10^{th} order band-reject filter using VDTA is shown in fig 5.28.

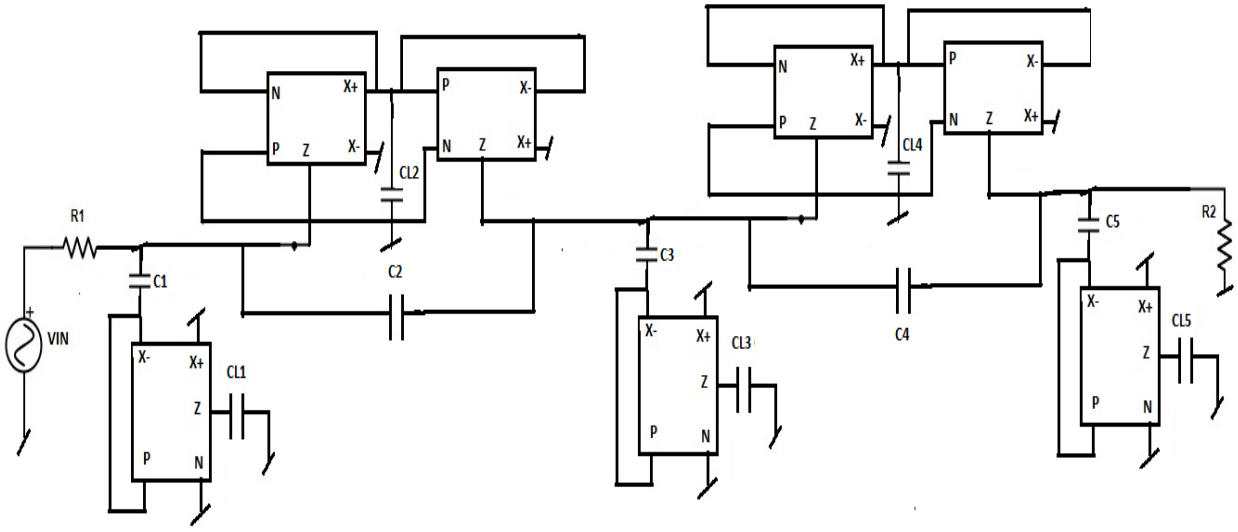

Fig.5.28. 10^{th} Order LC Ladder Butterworth Band-Reject Filter Using VDTA

Where

$C_{L1}=C_{L5}=g_{m1}g_{m2}L_1= g_{m1}g_{m2}L_5=32.4pF$

$C_{L2}= C_{L4}=g_{m1}g_{m2}L_2= g_{m1}g_{m2}L_4=8.1pF$

$C_{L3}= g_{m1}g_{m2}L_3=10pF$

By simulation, as shown in Fig 5.28, we get the center frequency to be 10MHZ.

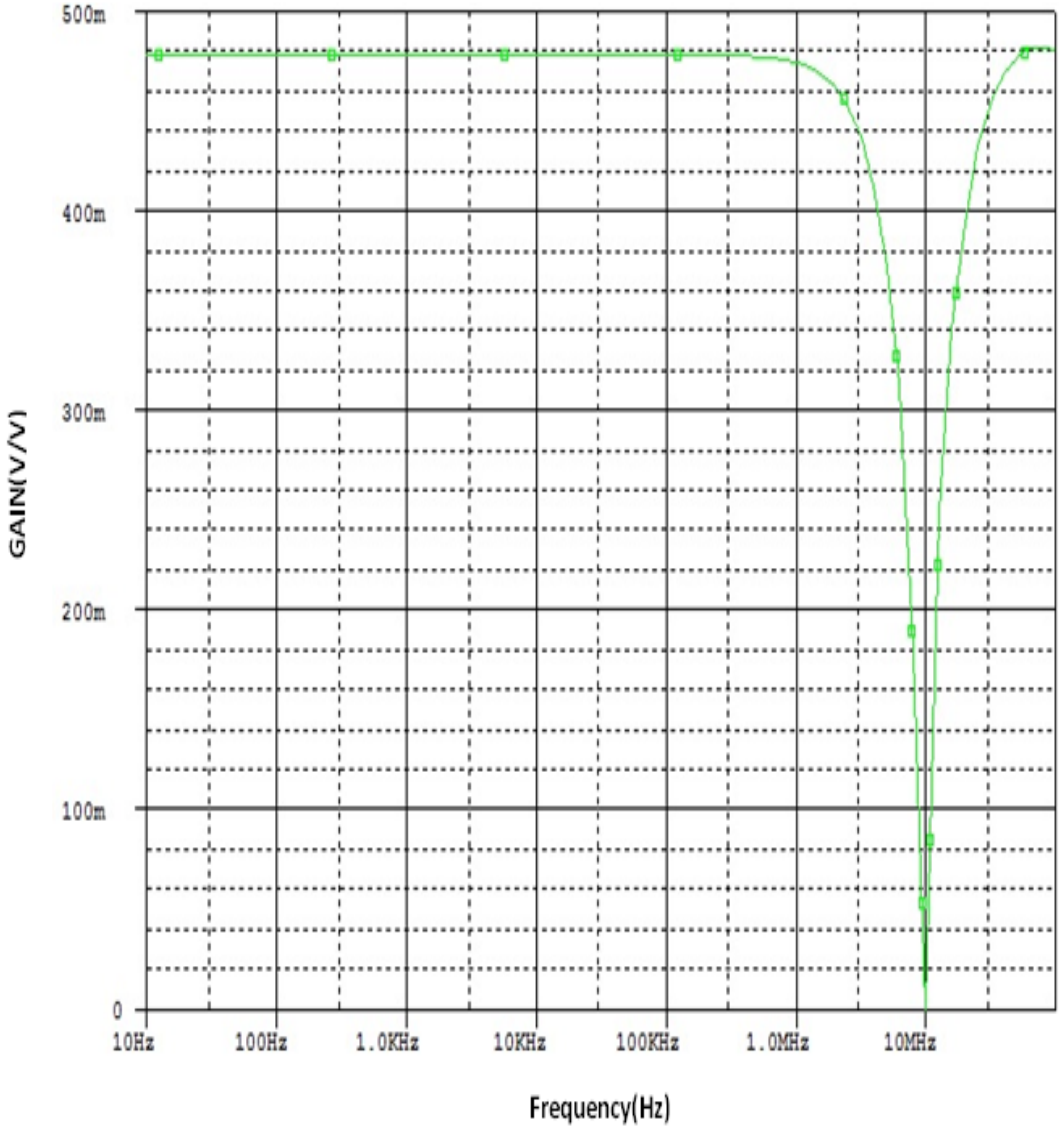

FIG.5.29. Frequency (Ac) Response Of Magnitude Gain For 10th Order Lc Ladder Butterworth Band-Reject Filter Using VDTA

The filter parameters are also derived for the same center frequency of 10 MHz. The power dissipation for this circuit is 3.78E-03Watts, output noise is 7.511E-08V/Hz1/2 and %THD is within 4.082079E+00% up to 500 mV p–p.

CHAPTER-6

CONCLUSION AND FUTURE SCOPE

A technique to get VDTA based LC Ladder filter is mentioned and documented. A VDTA as a basic building block is mentioned to simulate floating and grounded inductor. The conclusion so obtained is then organized for alternative passive part realization by creating appropriate connections. The structure is standard, and invariably employs grounded capacitors, and possesses electronic tune-ability of cutoff frequency. The part replacement technique provides modularity and a capability to synthesize higher order filter in very short period of time. It will be useful to synthesize higher order filters for this reason. By frequency transformation technique, high-pass, band-pass and band-stop filters will be completed simply via frequency transformation technique. The theoretical proposition is cross-checked for the filters by PSPICE AD simulation. There's close agreement between theoretical and experimental results obtained. The researchers can also deduce many techniques so as to have a reduced parasitic loss and noise. The sensitivity analysis technique is also an important phenomenon which should be taken care of as the low sensitivity to parameter variation is the most attractive feature of the LC ladder filter. Many sensitivity, parasitic loss and noise analysis algorithm are there and researchers are giving emphasis to continue their work in this regard. So, there is a vast scope of future work in this field.

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APPENDIX

The CMOS technology that we have used here is of 0.18µm TSMC process. So, the all the CMOS parameters in the PSpice AD as per the following model parameters. The supply voltage we are using here is $\pm 0.9V$

The characteristics of the CMOS 0.18um are given as follows

.MODEL NMOS1 NMOS

+ LEVEL = 3

+ VTO = 0.41

+ TOX = 2.2E-09

+ NSUB = 2.0E+18

+ NFS = 6.0E+12

+ XJ = 6E-8

+ LD = 9e-9

+ UO = 390

+ VMAX = 2.2E+05

+ THETA = 0.80

+ ETA = 2.8E-03

+ KAPPA = 0.2

+ GAMMA = 0.40

+ RSH = 500

+ CGSO = 3.33449e-10

+ CGDO = 3.33449e-10

```
+ CGBO = 0.0
+ CJ = 4.96491e-3
+ CJSW = 2.45744e-10
.MODEL PMOS1 PMOS
+ LEVEL = 3
+ VTO = -0.41
+ TOX = 2.2E-09
+ NSUB = 2.0E+18
+ NFS = 6.0E+12
+ XJ = 6E-8
+ LD = 9e-9
+ UO = 175
+ VMAX = 1.1E+05
+ THETA = 0.80
+ ETA = 2.8E-03
+ KAPPA = 0.2
+ GAMMA = 0.40
+ RSH = 500
+ CGSO = 3.33449e-10
+ CGDO = 3.33449e-10
+ CGBO = 0.0
```

+ CJ = 4.96491e-3

+ CJSW = 2.45744e-10