ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

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CANDIDATE'S DECLARATION

I, Dipti Singh, 2K17/VLS/08 of M.Tech VLSI Design and Embedded Systems, hereby declare that the project Dissertation titled **"Implementation of Arithmetic Logic Functions for Low Power VLSI Circuits"** which is submitted by me to the Department of Electronics and Communication, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi **DIPTI SINGH**

Date:

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CERTIFICATE

I hereby certify that the Thesis Dissertation titled **"Implementation of Arithmetic Logic Functions for Low Power VLSI Circuits"** which is submitted by **Dipti Singh, 2K17/VLS/08** Electronics and Communication, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date:

PIYUSH TEWARI

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SUPERVISOR

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ABSTRACT

For the integrated circuit implementation and design, one of the most common design methodology for the implementation of combinational logic circuits is dynamic logic, especially for those logic functions that are implemented using MOS technology. Dynamic logic has certain advantages when compared to the static equivalents in terms of faster speed and requirement of lower surface area. But the area where dynamic logic lacks is that it is more difficult to design and suffers from higher power dissipation.

In order to overcome the issues faced by dynamic logic, Domino logic circuit methods comes into play. Domino logic circuit methodology finds comprehensive use for high-performance design of advanced microprocessors because domino logic topology provides increased speed and improved area usage which is advancement over static complementary MOS(CMOS) circuits. The principal reason of domino logics capability to provide enhances and improved speed is the reduced noise margins in comparison to static logic gates. Domino logic circuits offers some crucial advantages such as improved and higher speed of operation and area saving over the conventional static CMOS logic circuits. These features make domino circuits capable of improved implementation of complex logic gates having larger fan-outs.

The power and delay characteristics of domino logic buffer, pseudo-dynamic buffer and footed quasi resistance buffer is verified by VIRTUOSO, CADENCE simulation using 180nm technology.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS, ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
XOR	Exclusive-OR
XNOR	Exclusive-NOR
PDB	Pseudo Dynamic Buffer
FQR	Footed Quasi Resistance
V_{OH}	Nominal voltage corresponding to a high logic state at the output of a logic gate for $V_I = V_{OL}$
V_{OL}	Nominal voltage corresponding to a low logic state at the output of a logic gate for $V_I = V_{OH}$
V_{IL}	Maximum input voltage that will be recognized as a low input logic level
V_{IH}	Minimum input voltage that will be recognized as a high input logic level
GND	Ground
V_{DD}	Supply Voltage
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
'	Bar
$\oplus$	Ex-OR
FA	Full Adder