M. Tech (VLSI Design & Embedded Systems) KARTIK PARCHANDA 2018

STATIC POWER REDUCTION TECHNIQUES IN DEEP SUBMICRON TECHNOLOGIES FOR VLSI APPLICATIONS

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI Design & Embedded Systems

Submitted by:

KARTIK PARCHANDA

2K16/VLS/12

Under the supervision of

Mr. A.K. SINGH
(Associate Professor)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

(Session: 2016-2018)

STATIC POWER REDUCTION TECHNIQUES IN DEEP SUBMICRON TECHNOLOGIES FOR VLSI APPLICATIONS

A PROJECT REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEMS

Submitted by:

KARTIK PARCHANDA
2K16/VLS/12

Under the supervision of

Mr. A.K. SINGH
(Associate Professor)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

(Session: 2016-2018)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, KARTIK PARCHNADA, Roll No. 2K16/VLS/12 student of M. Tech. (VLSI DESIGN AND EMBEDDED SYSTEM), hereby declare that the project Dissertation titled **"STATIC POWER REDUCTION TECHNIQUES IN DEEP SUBMICRON TECHNOLOGIES FOR VLSI APPLICATIONS"** which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

Place: Delhi **KARTIK PARCHANDA**
Date:

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled **"STATIC POWER REDUCTION TECHNIQUES IN DEEP SUBMICRON TECHNOLOGIES FOR VLSI APPLICATIONS"** which is submitted by KARTIK PARCHANDA, Roll No 2K16/VLS/12 Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date:

Mr. A. K. SINGH

SUPERVISOR

ACKNOWLEDGEMENT

I would like to thank my supervisor, Mr. A.K. Singh, Department of Electronics and Communication Engineering, DTU for the guidance, encouragement and advice he has provided throughout my time as his student. I have been extremely lucky to have a supervisor who cared so much about my work and who responded to my questions and queries so promptly. I attribute the level of my Master's degree to his encouragement and effort and without him this thesis, too, would not have been completed or written. One simply could not wish for a better or friendlier supervisor.

I am also grateful to Prof. S. Indu, HOD, Department of Electronics and Communication Engineering, DTU for her immense support. I would also acknowledge DTU for providing the right academic resources and environment for this work to be carried out.

Finally, I take this opportunity to extend my deep appreciation to my family and friends, for all that they meant to me during the crucial times of the completion of my project.

Date

KARTIK PARCHANDA

2K16/VLS/12

M.Tech (VLSI Design

and Embedded System)

ABSTRACT

As technology scales down, the size of transistors has been shrinking. The number of transistors on chip has thus increased to improve the performance of circuits. The supply voltage being one of the critical parameters has also been reduced accordingly in order to maintain the characteristics of an MOS device. Therefore, in order to maintain the transistor switching speed, the threshold voltage is also scaled down at the same rate as the supply voltage. As a result, leakage current increases dramatically with each technology generation and reducing leakage power is a great challenge. Static(Leakage) power is a serious problem particularly for CMOS circuits in nanoscale technology. So there is need of proper designing of nanoscale CMOS circuits which reduces the static power without affecting the performance and currently this has become a greater challenge for VLSI designers. In this work we address the sources of power dissipation especially the static power in CMOS circuits and its reduction techniques which reduces the static power to a greater extent. These techniques are utilized to lessen the static power dissipation in many popular combinational and sequential circuits which are the key components of digital IC design. CMOS Inverter, flip flop(DDFF) and ultra-low voltage DTMOS based buffer/Inverter circuits are modified using various leakage reduction techniques like forced Stack, Sleepy stack and LECTOR. These circuits are implemented using Symica DE tool at 45nm & 130nm PTM parameters and the result is compared with conventional circuits, which finally concluded that by using these techniques static power can be decreased to a noteworthy degree which helps circuit designers to handle the static power problem especially for chips that are used in power constrained portable systems.

TABLE OF CONTENTS

Candidate's Declaration ii

Certificate iii

Acknowledgement iv

Abstract v

Contents vi

List of Figures ix

List of Tables xi

List of Symbols, abbreviations xii

CHAPTER 1 INTRODUCTION 1-5

1.1 Motivation……..1

1.2 Relevant Literature Survey ……...……2

1.3 Organization of Thesis……..4

CHAPTER 2 STATIC POWER IN VLSI CIRCUITS & IT'S REDUCTION TECHNIQUES 6-18

2.1 Introduction……..……...……6

2.2 Sources of power consumption in CMOS circuits ……...…….…...6

2.2.1 Dynamic Power…….7

2.2.2 Static Power……..8

2.3 Sources of Static(leakage) Power…….……...……..9

2.3.1 Reversed biased PN junction current……...10

2.3.2 Gate induced drain leakage……..10

2.3.3 Gate direct tunneling or gate oxide tunneling……..10

2.3.2 Sub-threshold conduction……11

2.4 Static(Leakage) Power reduction techniques……13

2.4.1 State destructive techniques……..……..13

2.4.1.1 Dual threshold CMOS……...13

2.4.1.2 Sleep transisitor techniques……...13

2.4.2 State saving techniques.……14

2.4.2.1 Forced stack technique…….....15

2.4.2.2 Sleepy stack technique……..15

2.4.2.3 LECTOR technique……...17

CHAPTER 3 APPLICATION OF STATIC POWER REDUCTION TECHNIQUES TO CMOS INVERTER 19-28

3.1 Schematic & Simulation of various Inverters……..20

3.1.1 Conventional CMOS inverter……20

3.1.2 Forced stack CMOS inverter…….22

3.1.3 Sleepy stack CMOS inverter…….23

3.1.4 LECTOR inverter……..24

3.2 Comparison & Analysis of Simulation Results……..25

CHAPTER 4 STATIC POWER REDUCTION IN DDFF 29-40

4.1 Dual Dynamic Node Hybrid Flip Flop(DDFF).....…….....29

4.2 Implementation of DDFF……33

4.3 Static Power Reduction in DDFF……35

4.3.1 FS-DDFF……...35

4.3.2 SS-DDFF……...36

4.3.3 LECTOR-DDFF……36

4.4 Comparison of Various Flip Flops…….37

CHAPTER 5 STATIC POWER REDUCTION IN ULTRA LOW VOLTAGE CIRCUITS 41-58

5.1 DTMOS transisitor & its principle……..……..42

5.2 Schmitt Trigger & its principle……....44

5.3 Conventional ST based buffer/inverter ……...46

5.4 Forced stack VTCMOS ST buffer/inverter ……..……...…...49

5.5 Sleepy stack VTCMOS ST buffer/inverter……..49

5.6 LECTOR VTCMOS ST buffer/inverter……..50

5.7 Simulation & Analysis…….51

5.8 Comparison of various buffers/inverters…….55

CHAPTER 6 Conclusion and Future Scope 59

REFERENCES 60

LIST OF FIGURES

Fig.No	Title	Page No.
Fig 2.1	various sources of power consumption in CMOS circuits	7
Fig 2.2	Various Sources of Static Power	9
Fig 2.3	I-V Characteristics of NMOS Transistor	11
Fig 2.4	I_d vs V_{GS} Curve of NMOS Transistor	12
Fig 2.5	Structure of Sleep Transistor technique	14
Fig 2.6	Structure of Forced-Stack Technique	15
Fig 2.7	Sleepy Stack Structure	16
Fig 2.8	(a)Sleepy-stack Inverter during active mode (b) Sleepy-stack Inverter during Sleep mode	17
Fig 2.9	Lector Structure	18
Fig 3.1	CMOS Inverter model for evaluating Static power dissipation	19
Fig 3.2	Conventional CMOS inverter	20
Fig 3.3	Simulated waveform of Conventional CMOS inverter	21
Fig 3.4	Leakage current for input ‘0’ and ‘1’ in conventional CMOS inverter	22
Fig 3.5	Schematic of Forced Stack CMOS inverter	22
Fig 3.6	Schematic of Sleepy Stack CMOS inverter	23
Fig 3.7	Schematic of LECTOR inverter	24
Fig 3.8	Percentage Static Power reduction	27
Fig 3.9	Delay of Various inverters	27
Fig 4.1	Structure of DDFF	30
Fig 4.2	(a) Thold0 required by DDFF to sample “zero”	32
	(b) Thold1 required by DDFF to sample “one”	32
Fig 4.3	Implementation of DDFF at 45nm	33

Fig 4.4 Timing diagram of DDFF operated at 1Ghz frequency 34

Fig 4.5 Structure of FS- DDFF 35

Fig 4.6 Structure of SS-DDFF 36

Fig 4.7 Structure of LECTOR DDFF 37

Fig 4.8 Power leakage in standby mode(nW) with V_{tn}=0.46893 & $|V_{tp}|$=0.49158 39

Fig 4.9 Power leakage in standby mode(μW) with V_{tn}=0.3423 & $|V_{tp}|$=0.23122 40

Fig 5.1 NMOS and PMOS transistors based on DTMOS circuit topology 43

Fig 5.2 (a)Voltage transfer characteristic of a Schmitt trigger buffer 45

(b) Input and output waveforms of a Schmitt trigger buffer 45

Fig.5.3 CMOS based Schmitt trigger 46

Fig 5.4 Traditional DTMOS based CMOS ST Inverter 46

Fig 5.5 Conventional VTCMOS based Schmitt trigger Inverter / Buffer 47

Fig 5.6 FS-VTCMOS based Schmitt trigger Inverter / Buffer 49

Fig 5.7 SS-VTCMOS based Schmitt trigger Inverter / Buffer 50

Fig 5.8 LECTOR-VTCMOS based Schmitt trigger Inverter / Buffer 50

Fig 5.9 Schematic of Conventional VTCMOS ST based buffer / Inverter 51

Fig 5.10 Hysteresis Plot for a buffer using VTCMOS buffer and a Traditional Schmitt trigger inverter with a DTMOS Inverter 52

Fig 5.11 Timing diagram of all VTCMOS ST buffer 53

Fig 5.12 Static Power of VTCMOS ST buffer & FS VTCMOS ST at 45nm. 56

Fig 5.13 Static Power of VTCMOS ST buffer & FS VTCMOS ST at 130nm

LIST OF TABLES

Table No.	Title	Page No.
Table 3.1	Simulation Environment I	25
Table 3.2	Leakage Power(P_{static}) & Delay (τ_{pLH} & τ_{pHL}) of CMOS Inverter at 45nm	25
Table 3.3	Comparison of Static(leakage) Power & Delay of Various CMOS Inverters w.r.t. conventional CMOS Inverter	25
Table 3.4	Simulation Environment II	26
Table 3.5	Leakage Power(P_{static}) & Delay (τ_{pLH} & τ_{pHL}) of CMOS Inverter at 45nm	26
Table 3.6	Comparison of Static(leakage) Power & Delay of Various CMOS Inverter w.r.t conventional CMOS Inverter	26
Table 4.1	Standby leakage power of DDFF	34
Table 4.2	Power leakage in standby mode(nW) with V_{tn}=0.46893 & V_{tp}=-0.49158	38
Table 4.3	Power leakage in standby mode(nW) with V_{tn}=0.3423 & V_{tp}=-0.23122	38
Table 4.4	Comparison of timing parameters	40
Table 5.1	Static Power & delay of Conventional VTCMOS ST based Buffer	54
Table 5.2	Static Power & delay of FS VTCMOS ST based Buffer	54
Table 5.3	Static Power & delay of SS VTCMOS ST based Buffer	54
Table 5.4	Static Power & delay of LECTOR VTCMOS ST based Buffer	55
Table 5.5	Comparison table of Various VTCMOS ST buffer at 45nm Technology node	55
Table 5.6	Comparison table of Various VTCMOS ST buffer at 130nm Technology Node	57

List of abbreviations

DTMOS	Dynamic Threshold Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
ST	Schmitt Trigger
SS	Sleepy Stack
FS	Forced Stack
LCT	Leakage Control Transistor
PTM	Predictive Technology Model
VTCMOS	Variable Threshold Complementary Metal Oxide Semiconductor
GIDL	Gate Induced Drain Leakage
NMOS	N channel MOSFET
PMOS	P channel MOSFET
DDFF	Dual Dynamic node hybrid pulsed Flip Flop
Vth	Threshold Voltage
DIBL	Drain Induced Barrier Lowering
MTCMOS	Multi Threshold CMOS
I_{sub}	Subthreshold leakage current
P_{static}	Static power dissipation
V_{tn}	Threshold voltage of NMOS
V_{tp}	Threshold voltage of PMOS

CHAPTER 1

INTRODUCTION

Power consumption is an increasingly important issue in general purpose processors, particularly in the mobile computing segment. In present processors, most of the power dissipation is dynamic power dissipation, which arises due to signal transitions. Various techniques have been studied and implemented to reduce dynamic power dissipation, including clock gating, cache sub-banking, voltage scaling, and eliminating needless computation (these techniques are directly relevant to computer architects).

However, as transistors become smaller and faster, static power (also called leakage power) dissipation will become increasingly significant. Technology scaling is increasing both the absolute and relative contributions of static power dissipation.

Looking at current technology trends, it is evident that static power dissipation is growing at a fasterrate than dynamic power dissipation. According to the International Technology Roadmap for Semiconductors (ITRS) [1], Kim et al. report static power (sub-threshold leakage power dissipation) of a chip can exceed dynamic power dissipation at the 65nm technology node[2] . Using scaling theory, Borkar [3] also predicts that leakage power increases by 5 times every generation, while active power remains roughly constant.

1.1 MOTIVATION

The desire of consumers for mobile application has increased dramatically from the last few years. As we know that portable devices like mobile phone,tablets,smart watches is becoming a necessity for individuals, thus there is a need to reduce power consumption in such devices so that they can be operated for long intervals of time. The usage of smart phones,palmtop,laptop,wristbands , netbooks, tablet computers, and several other wireless devices has grown dramatically which brings about the requirement for more advanced power-aware design techniques.

From the last decade need for high performance systems had grown rapidly.As a result,the transisitor density on semiconductor chip is increased, consequently demands for expensive cooling and packaging technologies. Keeping this in view , the supply

voltage are scaled down to reduce the switching power dissipation . Morever the threshold voltage is also scaled down for performance tradeoffs. However , the scaling of threshold voltage has resulted in exponential increase in exponential increase of subthreshold leakage current causing static(leakage) power dissipation .

Static power dissipation (P_{Static}) is now growing considerably propotional to the switching dynamic power dissipation in deep submicron technologies and battery operated devices. Better leakage power savings results in the long-lasting battery life[3]-[4], which in turn demands for more advanced design techniques. Static power dissipation is mainly because of the leakage current components flowing in the transistor or CMOS circuits while the circuit is not under operation i.e. during idle or standby mode. According to the International Technology Roadmap for Semiconductors (ITRS) [1], Kim et al. report static power (sub-threshold leakage power dissipation) of a chip can exceed dynamic power dissipation at the 65nm technology node [2]. K.Roy and S.C.Prasad also anticipated that the leakage power (P_{Static}) could rise by 32 times per device [4] by 2020.

The four main sources of leakage current in a CMOS transistor are:

i) Reverse-biased PN-junction leakage current
ii) Gate induced drain leakage current
iii) Gate direct-tunnelling leakage current
iv) Subthreshold (weak inversion) leakage current (I_{SUB}).

The subthreshold leakage current (I_{SUB}) being the most predominant among all the leakage current sources becomes extremely challenging for research in current and future silicon technologies. Though, there is a intense need for new ideas and perspectives to circuit design,so as to meet the needs of power − efficient electronic equipments.

1.2 RELEVANT LITERATURE SURVEY

Researchers did enormous amount of work related to leakage current and their reduction techniques in CMOS VLSI design as the technology scaled down to deep sub-micron regime . This segment comprises of the various associated research themes as the year progresses.

A. P. Chandrakasan [5] introduced "Low-power CMOS digital design," in 1992 which was motivated by emerging portable and battery-operated applications that demand high performance, techniques are investigated which lessen power consumption in CMOS digital circuits.

In 1996, Gu, R.X and M.I Elmasry,[6] introduced "Power dissipation analysis and optimization of deep sub-micron CMOS digital circuits," which gives simple analytical model for estimating standby and switching power dissipation in deep submicron CMOS digital circuits .

Ali Keshavarzi, Kaushik Roy and Charles F. Hawkins introduced the intrinsic leakage in low power deep submicron CMOS ICs in 1997 [7]. In this they describe the various sources of leakage in MOS device and their variation with scaling .

Dual V_{TH} or MTCMOS technique was introduced in 2003, which utilizes the concept of two different V_{TH} , the high threshold NMOS gated amid of pull down network and ground terminal, in series to low threshold voltage circuitry to reduce leakage[8].

LECTOR technique was introduced in 2004 [9],which achieves reduction of leakage by the effective stacking of transistors in the path of supply voltage (V_{dd}) and ground.

In 2006 Sleepy stack technique was introduced which combine the advantages of Sleep transistor and Forced stack technique to lessen the leakage power while retaining the exact logic state[10] .

In 2012 M. Geetha Priya done the study and analysis of various leakage power reduction techniques for VLSI applications[11].

In 2015 S. Singhal done the analysis and comparison of leakage power reduction techniques in CMOS circuits[12].

In 1997,fully static single-clock CMOS latches & flip-flops were proposed. By eliminating the bottlenecks of the original true single phase clocking (TSPC) and the

existing differential latches and flipflops, both power consumptions & delays are reduced [13].

In 1998 Semi-dynamic and dynamic flip-flops with embedded logic is introduced which comprises the dynamic concept in flip flop design for high performance [14].

A set of laws for reliable evaluation of the actual performance and power features of the flip-flop and master-slave latch structures was proposed in 1999[15] .

In 2000 N. Nedovic proposed "Hybrid latch flip-flop with improved power efficiency,". in which the proposed structure comprises advantage of both static and dynamic style of design [16].

In 2006 C. K. Teh proposes "Conditional data mapping flip-flops for low-power and high performance systems,". It utilizes an output feedback structure to conditionally feed the data to the flip flop. This reduces power dissipation by eliminating redundant transitions when a unnecessary event is predicted [17] .

In 2013 "Low-Power Dual Dynamic Node Pulsed Hybrid Flip Flop Featuring Efficient Embedded Logic," was proposed by K. Absel. In this work they eliminate the huge capacitances present in the precharge node using design techniques[18] .

1.3 ORGANISATON OF THESIS

This thesis is divided into six main chapters. Chapter 1 Introduction mentions the current demands of VLSI industry and work done in order to achieve the desired performance . Various problems encountered in attaining the desired performance and discusses how this work is obliging in solving the problems associated with VLSI circuit design.

Chapter 2 discuses the various components of power dissipation in CMOS circuits and detailed study of components of static power dissipation . After that various techniques are explored to reduce static power dissipation in CMOS circuits.

Chapter 3 presents the application of static power reduction techniques to key component of digital VLSI design i.e. CMOS Inverter . After that comparison of various modified inverters is done with the conventional CMOS Inverter .

Chapter 4 presents the application of static power reduction techniques to basic memory element i.e Flip Flop . Dual Dynamic node pulsed hybrid flip flop(DDFF) is the best flip flop architecture available in literature but as we do down to lower technology node it suffers from large amount of static power dissipation. Thus various static power reduction techniques are applied to DDFF to lessen the static power dissipation. Modified DDFF reduces the static power by a good amount.

Chapter 5 discusses the application of static power reduction techniques to ultra low voltage circuits .

Chapter 6 contains the conclusion and future scope of the presented work .

CHAPTER 2

STATIC POWER IN VLSI CIRCUITS AND ITS REDUCTION TECHNIQUES

2.1 INTRODUCTION

One of the "top concern of today's CMOS VLSI design is leakage power dissipation. It become challenging task for VLSI design engineer to deal with power consumption in deep sum-micron regime. Advantage of scaling the feature size is high speed and frequency of operation i.e. higher performance. But as the technology scale down to nanometer technology node the leakage power starts dominating over dynamic power in CMOS VLSI circuits. With process geometries goes down, more and more transistors embedded into the same chip area so circuit complexity goes on increasing which may lead some secondary effects. To avoid these secondary effect supply voltage has to scale down, but keeping threshold voltage constant and scaling the supply voltage degrade the performance of the circuit. So it needs to scale down threshold voltage and oxide thickness to maintain the same performance level. Scaling down the threshold voltage further have adverse effect i.e. larger sub-threshold current which is not desirable while scaling the oxide thickness increases the gate tunneling current and also create reliability issue. Since the sub-threshold leakage current increases exponentially with decrease in device dimensions so this is matter of great concern for both hardware and software designer to reduce the leakage current. According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may dominate in total power consumption as technology feature sizes scale down beyond a limit. In following section we are going to discuss the different power components in CMOS VLSI circuits and some techniques to reduce them.

2.2 SOURCES OF POWER CONSUMPTION IN CMOS CIRCUITS

There are three sources of power consumption present in CMOS digital Integrated Circuits which can be expressed by the equation 2.1:

$$`P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{static} = \alpha C_L V_{dd}^2 f + I_{short-circuit} V_{dd} + I_{static}\, V_{dd} \quad (2.1)$$

where P_{avg} is total power dissipation , C_L is output load capacitance ,V_{dd} is power supply,f is the switching frequency, α is switching activity factor, $I_{short\text{-}circuit}$ is the short circuit current i.e. current from power supply to ground when both Pull-up and Pull-down network are on during the transition of the input signal, I_{static} is Static(leakage) current .This equation assumes that the voltage swing across load capacitance is equal to the power supply voltage(V_{dd}).

The power consumption of a CMOS circuit can be majorly classified as: dynamic, and static (or leakage) power dissipation. The different Components of power consumption are shown below in Fig. 2.1

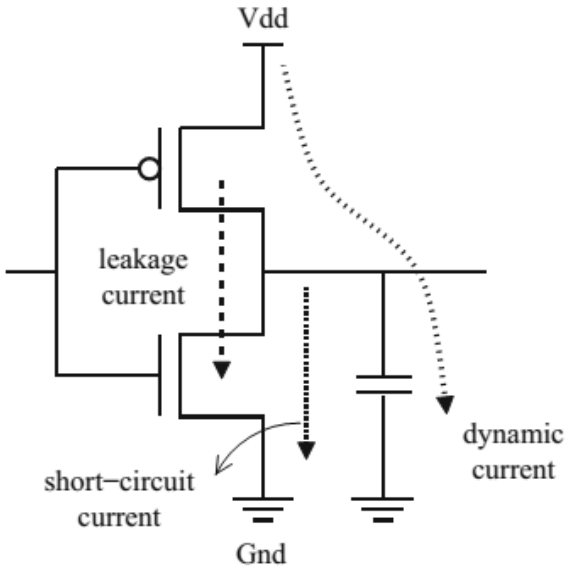

Figure 2.1 various sources of power consumption in CMOS circuits [19]

2.2.1 DYNAMIC POWER

Dynamic power dissipation consists of following mechanisms i.e. switching, short circuit, & glitch power dissipation. Each of the component depend on the output capacitance, activity factor and supply voltage(V_{dd}) of the given CMOS circuit. The first two terms of the equation. (2.1) represents the dynamic power consumption. Transfer of the data through CMOS circuit requires charging and discharging of the load capacitance of the circuit. This charging and discharging of load capacitance

draws some amount of power from the supply voltage(V_{dd}) & power dissipated is termed as switching power dissipation. As the switching power has square dependency on the supply voltage(V_{dd}) so an effective means to reduce the switching power is to lower the supply voltage(V_{dd}). It is also the function of load capacitance as well as frequency of operation as demonstrated by equation 2.1. Therefore, dynamic power can be reduced by reducing the clock frequency & maintaining the load capacitance as least as possible.

Short circuit power dissipation is another type of power consumption[19] which exists when the input signal has some finite rise and fall time . Let us consider a case where the input signal is undergoing transition from low to high then there comes a region where input asignal has a value between Vtn and Vdd – |Vtp| where Vtn and Vtp are thresholds of NMOS and PMOS reaspectively. In this region both the NMOS and PMOS will be ON forming a low resistance path between supply and ground.The short circuit current is a function of (directly proportional) to the inputs rise and fall time.It can be decreased by increasing output load capacitance.

Glitch power dissipation is the last mechanism under dynamic power dissipation. Glitches are unwanted transistion of signal in the circuit that does not comprise any required information. Since glitches results in the transition at output node, thus it results in short circuit and switched power dissipation. The probability for generation of glitch increases with increasing complexity of the circuit.

2.2.2 STATIC POWER

Static power is consumed even when a chip is not switching. CMOS has replaced nMOS processes because contention current inherent to nMOS logic limited the number of transistors that could be integrated on one chip. Static CMOS gates have no contention current. Prior to the 90 nm node, leakage power was of concern primarily during sleep mode because it was negligible compared to dynamic power. In nanometer processes with low threshold voltages and thin gate oxides, leakage can account for as much as a third of total active power. Static power occurs in the circuit when no useful tasks are performed so it is also known as leakage power (P_{Static}). The 3rd term in equation 2.1 corresponds to Static(leakage) power dissipation. As we go below 90nm technology node it is very essential to find some means to reduce

leakage power (P_{Static}) along with dynamic power. This section briefly reviews each source of static power. Because subthreshold leakage is usually the dominant source of static power, other techniques for leakage reduction are explored, including multiple threshold voltages, variable threshold voltages , and stack forcing.

Assuming the leakage current is constant so instantaneous and average power will be same, the static power dissipation is the product of total leakage current and supply voltage(Vdd).

$$P_{static} = I_{static} V_{dd} \quad (2.2)$$

2.3 SOURCES OF STATIC (LEAKAGE) POWER :

As mentioned earlier also that static power arises due to Reverse-biased PN-junction leakage current ,Gate induced drain leakage current,Gate direct-tunnelling leakage current & Subthreshold (weak inversion) leakage current (I_{SUB}). In this section we will discus these sources of static power in some detail. Fig 2.2 Shows the various sources of Static power.

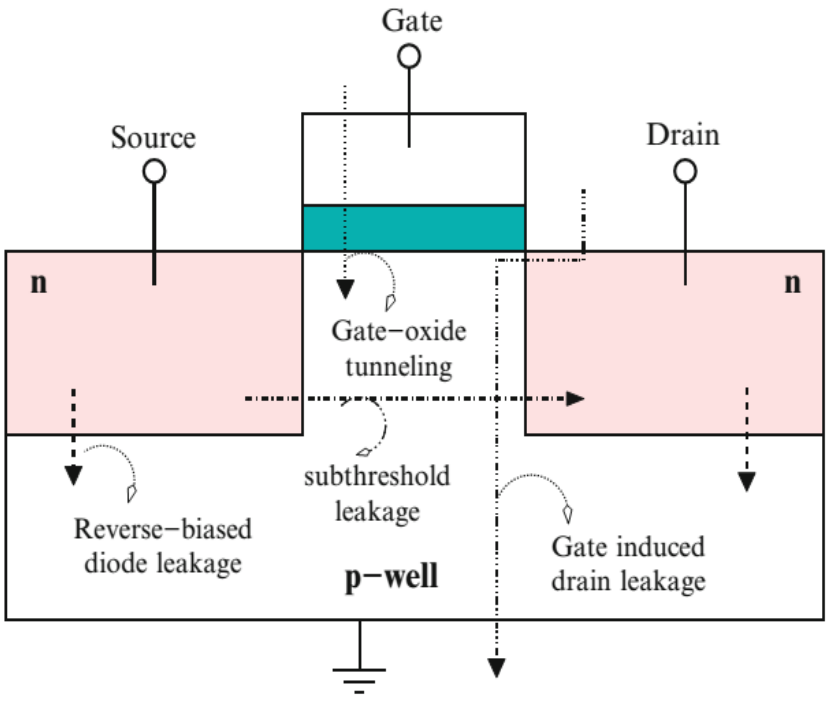

Fig 2.2 Various Sources of Static Power

2.3.1 REVERSE BIASED PN-JUNCTION CURRENT

Diode leakage occurs when a transistor is turned off and another active transistor charges up/down the drain with respect to the former's bulk potential. For example, consider an inverter with a high input voltage. The output is low, and the NMOS is on. The PMOS transistor will be turned off, but it's drain to bulk voltage will be -Vddsince the output voltage is at 0V and the bulk for PMOS is at Vdd. For the p-well to bulk diode, the leakge current is given by:

$$I_D = I_s(e^{V/V_T} - 1) \tag{2.3}$$

Where I_s is the reverse saturation current , V is the voltage across diode & V_T is the thermal voltage and is equal to $\frac{KT}{q}$.

2.3.2 GATE- INDUCED DRAIN LEAKAGE (GIDL)

Gate-Induced drain leakage (GIDL) is an undesirable short-channel effect that occurs at higher drain biases in an overdriven off state of a transistor. The GIDL is the result of a deep-depletion region that forms in the drain at high off biases" (negative for NMOS, positive for PMOS). The depletion region causes band bending which in-turn allows conductive band-to-band tunneling that creates excess current (20).

2.3.3 GATE DIRECT TUNNELING LEAKAGE OR GATE OXIDE TUNNELING

As the gate oxide under the gate electrode is becoming thinner due to scaling, consequently the effective electric field beneath the gate becomes very high which results in tunneling of electrons through gate oxide to the bulk from gate. The current which flows due to the tunneling of electrons is called gate oxide tunneling current [21]. This current may exceed all other components of leakage current if the gate oxide thickness is very thin and can also burn the device due to extreme generation of heat . Gate direct tunneling leakage or Gate oxide tunneling current ($\boldsymbol{I_{ox}}$)can be estimated by following equation

$$I_{ox} = AE_{ox}^{\ 2} e^{-\frac{B}{E_{ox}}} \tag{2.4}$$

Where E_{ox} is electric field across the gate oxide.

2.3.4 SUB-THRESHOLD CONDUCTION

Ideal transistor I-V models assumes that current only flows from source terminal to drain terminal when $V_{gs} > V_{th}$. But in real transistor the current(I_d) does not cutoff abruptly below threshold but rather drops of exponentially as expressed by equation 2.5.

$$I_{sub} = I_{sub0}\, e^{\frac{V_{GS}-V_{th}}{nV_T}} (1 - e^{\frac{-V_{DS}}{V_T}}) \quad (2.5)$$

$$I_{sub0}=\beta V_T^2 e^{1.8} \quad (2.6)$$

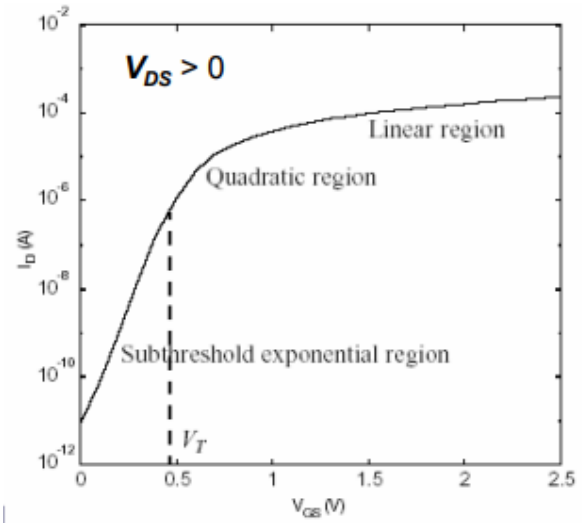

Fig 2.3. I-V Characterstics of NMOS Transistor[22]

This conduction is known as subthreshold leakage current[22]. I_{sub0} is the current at threshold volatgae(V_{th}) & is dependent on process and device dimensions, $e^{1.8}$ was found empirically,n is a term dependent on process and affected by the depletion region characterstics. The term in the brackets indicates that leakage is zero if V_{DS} is zero. But it increases to its full value when V_{DS} is few multiples of V_T.As seen from equation (2.5) that Subthreshold leakage current depends on threshold voltage V_{th} & V_T(thermal voltage). Subthreshold leakage current rises exponentially as V_{th} decreases or temperature rises, so it is becoming a major problem for chips using low supply and threshold voltages .

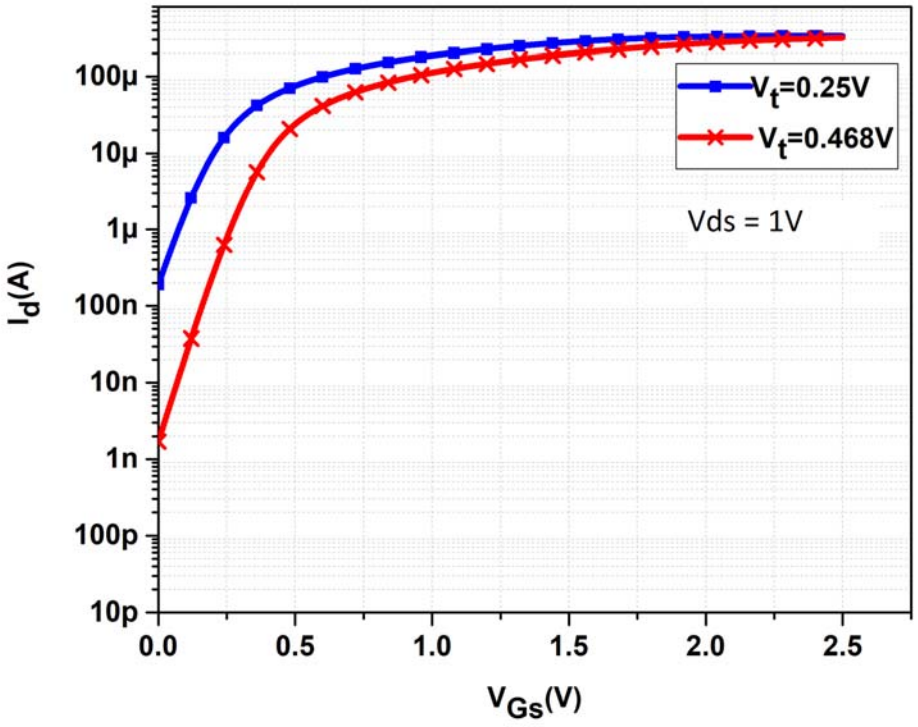

Figure 2.4 I_d vs V_{GS} Curve of NMOS Transistor

When we move down to lower technology node supply voltage(Vdd) also has to scale down to maintain the effective electric field & to reduce dynamic power as dynamic powed is directly propotional to the square of supply voltage(Vdd) . Reducing the supply voltage while keeping the threshold voltage (V_{TH}) constant degrades the performance of device. In order to have the same performance at threshold voltage (V_{TH}) also needs to be scale down . Scaling of threshold voltage (V_{TH}) results in exponential increase in subthreshold leakage due to which I_{sub} becomes the most predominant amongst all the sources of Static(leakage) current at lower technology node i.e at 70nm or below[11,22,23] .

Subtheshold leakage current is exacerbated by drain induced barrier lowering(DIBL) in which positive V_{ds} effectively reduces threshold voltage (V_{TH}) and this effect occurs in lower technology node i.e Under 100nm. DIBL effect can be modelled as

$$V'_{th} = V_{th} - \eta V_{ds} \tag{2.7}$$

where η is DIBL coefficient.

As discussed above that subthreshold leakage current is most predominamt among all the sources of leakage current in deep sub-micron regime it must be taken care atmost in order to reduce static power consumption.

2.4 STATIC (LEAKAGE) POWER REDUCTION TECHNIQUES

Static(leakage) power reduction techniques can be classified into two categories:

1. State-destructive techniques
2. State-saving or State-Preserving techniques

2.4.1 STATE-DESTRUCTIVE TECHNIQUE

State-Destructive Techniques are those in which current Boolean output value of the circuit might be lost.These techniques control the leakage power by applying the power gating method to remove the power supply from the circuit during standby mode of operation & is resumed during active mode. Examples of state-destructive techniques are Sleep transistor technique , Dual threshold CMOS technique etc.

2.4.1.1 DUAL THRESHOLD(V_{th}) CMOS

In this technique high threshold voltage transistors are assigned to non critical paths which effectively reduces the subthreshold leakage power. To maintain the performance low threshold transistors are used in critical paths. This approach makes use of an algorithm which finds for the gates where high threshold voltage transistors can be used[25-27].

2.4.1.2 MULTI-THRESHOLD CMOS OR SLEEP TRANSISTOR TECHNIQUE

In MTCMOS or sleep transistor technique high threshold transistors also known as sleep transistors are inserted in series with tansistors of logic circuit between the power supply voltage(Vdd) & ground. This techniques has two modes of operation i.e active mode & Sleep mode. During the active mode high Vth sleep transistors are “ON” so that normal operation of the circuit is not affected as there is a path between the supply and gnd. During Sleep mode high Vth sleep transistors are turned off which removes the power supply from theciruit virtually and hence reducing the leakage power during

standby mode of operation. This technique requires certain control signals to be generated in order to control the sleep transistors during active mode and sleep mode. During the sleep mode as power supply and gnd is virtually removed from the logic circuit , output of the circuit becomes floating and hence this technique is state-destructive technique. Fig 2.5 shows the structure of sleep transistor technique applied to CMOS circuit.

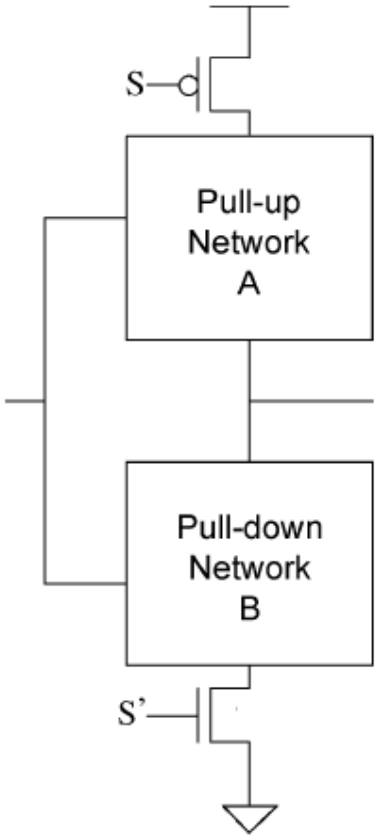

Fig 2.5 Structure of Sleep Transistor technique[10].

2.4.2 STATE-SAVING TECHNIQUES

State-Saving Techniques are those in which the current state of the circuit is retained. This technique reduces leakage current simply by inserting the transistors between power supply voltage(V_{dd}) & ground . Transistors are inserted between power supply and ground without affecting the logic functionality of the circuit. State saving techniques has an advantage over state destructive technique that a circuit can resume operation at a point much later in time without having to somehow regenerate state.

2.4.2.1 FORCED STACK TECNIQUE

This technique makes use of the fact that leakage through two series OFF transistors is much lesser than that of a single transistor because of the stack effect[27]. Fig 2.6 shows the forced stack technique , which forces a stack structure by breaking down an existing transistor into two half size transistors.

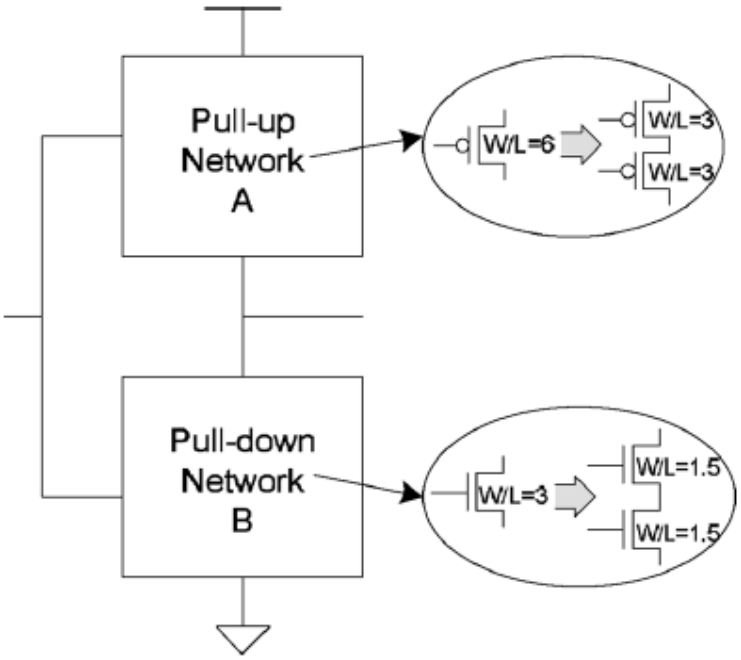

Fig 2.6 Structure of Forced-Stack Technique[10]

As the depth of the stack is increased, higher leakage power savings is observed.In some cases transistor stacking exits already for eg. Nand gate. In some circuits natural stacking does not exists , in order to reduce leakage power by utilizing stack effect force stacking is done by replacing each existing transistor of Width W with two transitors in series having Width W/2. It reduces the subthreshold leakage power by reducing sub-threshold current but increases the delay during switching operation as transitors between Vdd and ground path increases .

2.4.2.2 SLEEPY-STACK TECHNIQUE

Sleepy Stack technique has a combined structure of sleep transistor technique and forced stack technique[10]. It uses advantages of both forced stack and sleep transistor

to overcome the problem of state lost in sleep transistor technique & delay penalty in forced stack technique. Unlike forced stack technique, Sleepy stack technique can utilize high threshold transitors without delay penalty.Figure 2.7 shows the structure of sleepy stack merging the forced stack & sleep transistor technique. Here each existing transistor is replaced with two series transistors of equal width which is equal to half the width of original transitors. Then a sleep transitor is added in parallel to one of the transistors in each set of stacked transistors . Width of the sleep transistor can be varied in order to provide additional tradeoffs between power, area & delay.

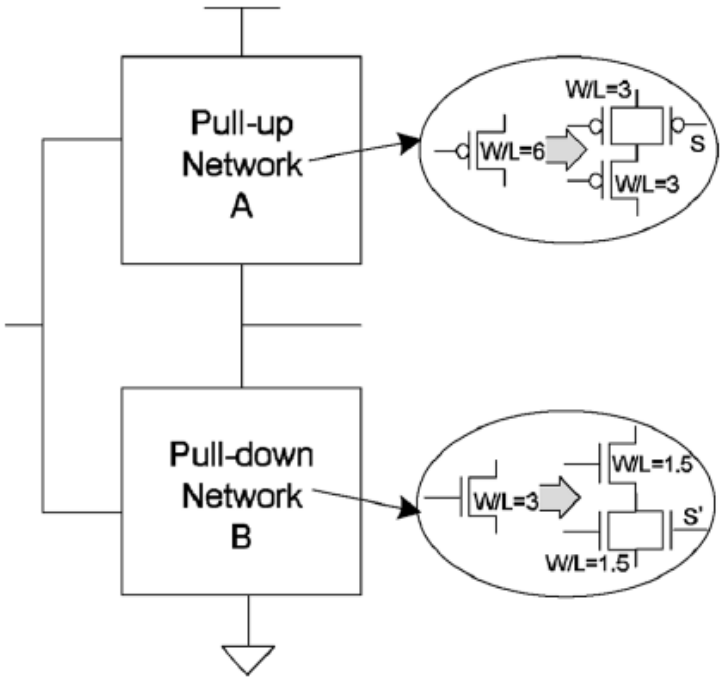

Fig 2.7 Sleepy Stack Structure[10]

Working of Sleepy-stack Technique

Similar to sleep transistor technique its working can be divided into two modes i.e active mode & sleep mode. Sleep transistors of the sleepy stack structure operate similarly to sleep transistor technique in which sleep transistors are turned on during active mode & turned off during sleep mode. Fig 2.8 explains the operation of sleepy stack inverter during active mode(a) & sleep mode(b). For active mode of operation control signals S = '0' and S'=1 are applied and both the sleep tarnsistors are turned on. Both Sleep transistors are on during active mode which takes lesser switching time than the forced stack structure. For Sleep mode S=1 & S'=0 are applied and both sleep transistors are turned off. Sleepy stack structure can retain state when the sleep

transistors are turned off. Leakage reduction in sleep mode is achieved in two ways : first leakage power(Pstatic) is suppressed by high threshold(Vth) sleep transitors & transitors parallel to it. Second , turned off & stacked transistors induce stack effect[10,27] which also reduces static power consumption. By utilizing these two effects sleepy stack approach achieves ultra- low static power dissipation in sleep mode & current state is also retained . The only disadvantage of this approach is increased area .

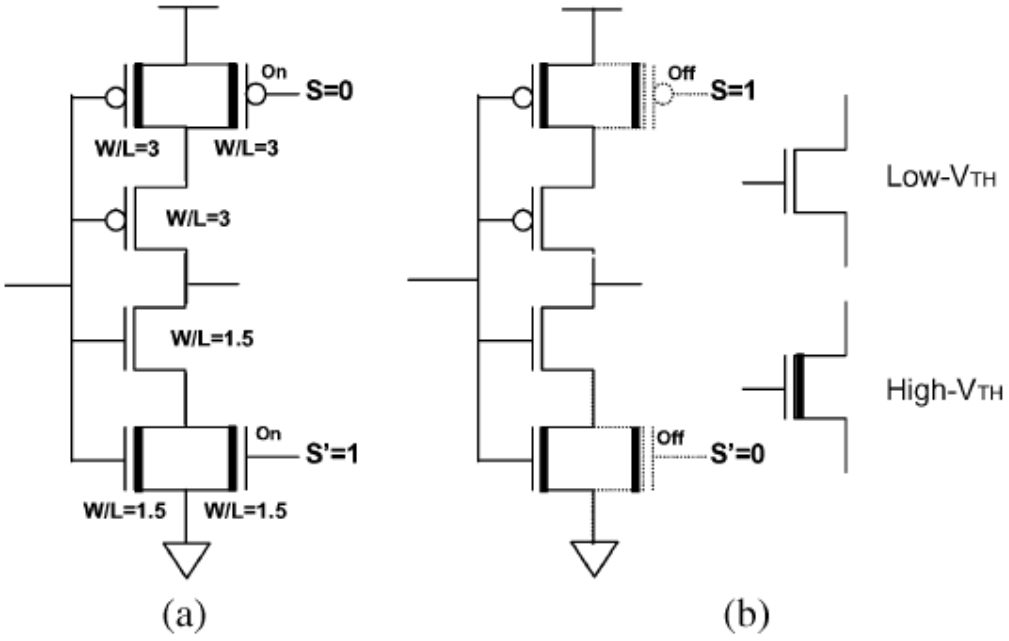

Fig 2.8 (a)Sleepy-stack Inverter during active mode. (b) Sleepy-stack Inverter during sleep mode [10]

2.4.2.3 LECTOR TECHNIQUE

This technique is based on the fact that effective stacking of transistors in the path between supply voltage(Vdd) & ground reduces leakage power. As stated in [9,27] that a state with more than one OFF transistor in a path between Vdd & gnd is far less leaky than a state with only one transitor OFF in a path between Vdd & gnd . In this technique leakage reduction is achieved by introducing two self controlled transitors (leakage control transistors(LCT)) between the pull up network & pull down network ,

such that one of the leakage controlled transistor is always near its cutoff region of operation. Fig 2.9 shows the lector structure in which gate of PMOS(Mp) is controlled by source of NMOS(Mn) & gate of NMOS(Mn) is controlled by soure of PMOS(Mp). LECTOR technique requires only two self controlling transistors out of which one will be always near its cut-off region . This increase the effective resistance of the path from supply voltage to ground thus reducing static(leakage) power .

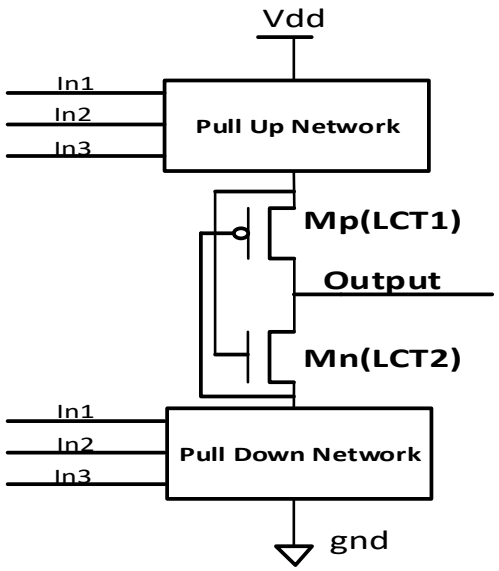

Fig 2.9 Lector Structure[9]

Thus to summarize , in this chapter we have discussed various sources of power consumption in CMOS circuits. Our main concentration was to study the various sources of static power consumption as static power increases times every generation while active power remains roughly constant . Subthreshold leakage current is most predominant amongst all the leakage current sources becomes exremely challenging for research in current and future silicon technologies . Thus for reducing static power various static power reduction techniques have been discussed and how to apply them to various circuits.

CHAPTER 3

APPLICATION OF STATIC POWER REDUCTION TECHNIQUES TO CMOS INVERTER

Inverter is actually the basis of all digital designs[28]. Once its operation and properties are clearly understood, designing more difficult structures such as NAND gates, adders, multipliers, and microprocessors is greatly simplified. The electrical behaviour of these complex circuits can be almost completely derived by extrapolating the results obtained for inverters. The analysis of inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors. So in this chapter we will first discuss the static power dissipation of CMOS inverter & application of leakage reduction techniques to CMOS Inverter.

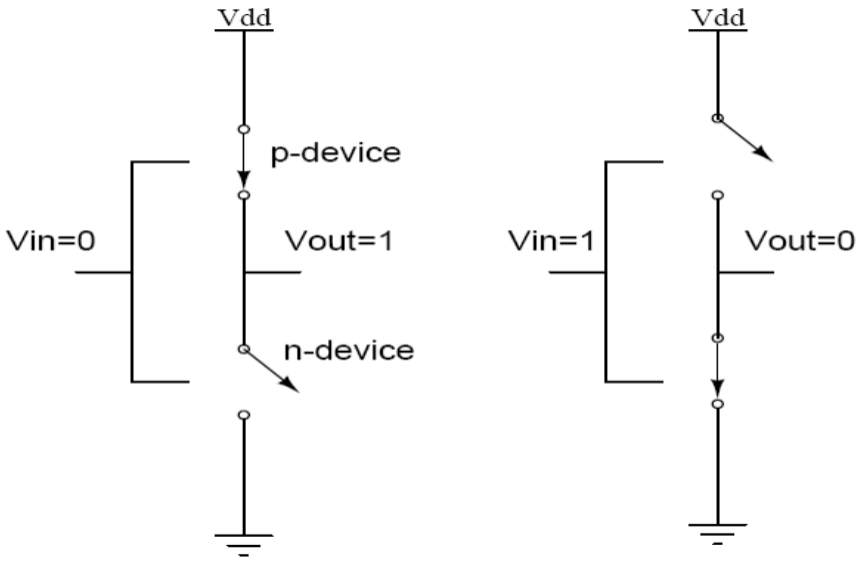

Fig 3.1 Cmos Inverter model for evaluating Static power dissipation .

Considering the static CMOS inverter shown in Figure 3.1, When input = '0', the associated n-device is OFF and the p-device is ON. The output voltage is V_{dd} or logic

'1'. When the input = '1', the associated n-device is On and the p-device turns OFF. The output voltage is '0' volts or GND . It can be seen that one of the transistors is always off when the gate is in either of these logic states. Ideally no current flows through the OFF transistor so the power dissipation is zero when the circuit is quiescent i.e. when no transistors are switching . Zero quiescent power dissipation is a primary advantage of of CMOS over other competing transitor technologies. However as discussed in Chapter 2 that due to secondary effects like subthreshold conduction, tunneling & leakage lead to small amount of static current flowing through transitors . Assuming the Static (leakage) current is constant so instantaneous & average power are the same, the static power dissipation is the product of total leakage current & supply voltage . As we go to lower technology node this static current increases exponentially thus it is required to find some means to reduce this static current & hence static power dissipation .

$$P_{static} = I_{static} V_{dd} \qquad (3.1)$$

3.1 SCHEMATIC & SIMULATION OF VARIOUS INVERTERS

All the simulation in this thesis are performed using symica DE tool at 45nm PTM parameters. Leakage power & delay is calculated for a supply voltage of 1V.

3.1.1 CONVENTIONAL CMOS INVERTER

The schematic for conventional CMOS inverter is presented in figure 3.2

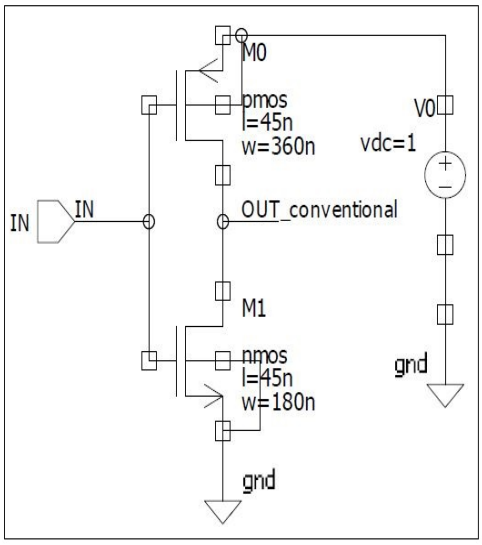

Fig 3.2 Conventinal CMOS inverter

Considering the schematic of CMOS inverter as shown in Figure 3.2 . When input = '0', the nmos is OFF and pmos is ON. The output voltage is V_{dd} or logic '1'. When the input = '1', the nmos is ON and the pmos turns OFF. The output voltage is '0' volts or GND. This working is illustrated by simulated result shown in figure 3.3.

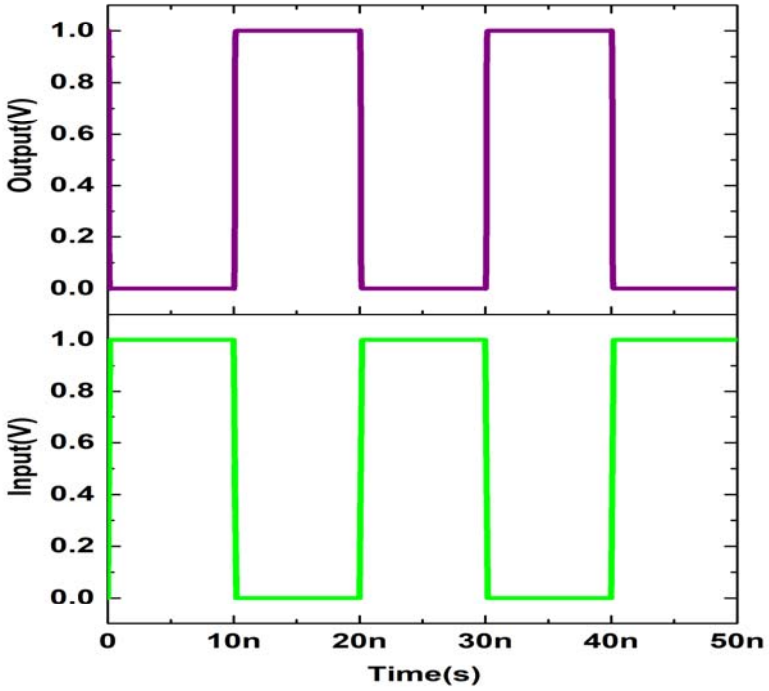

Fig 3.3 Simulated waveform of Conventional CMOS inverter

As discussed earlier , due to second order effects like subthreshold conduction etc. there flows a small amount of static(leakage) current even when the transistors are in OFF state. It is depicted in fig 3.4 which shows leakage current when input is '0' & '1' respectively".

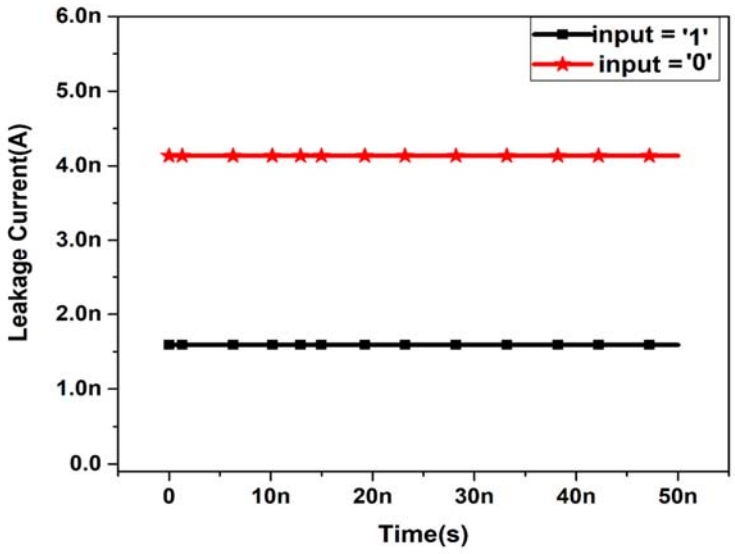

Fig 3.4 Leakage current for input '0' and '1' in conventional CMOS inverter

Calculated average leakage power & delay for CMOS inverter is 2.861nW & 4.8035ps respectively.

3.1.2 FORCED STACK CMOS INVERTER :

The schematic of Forced-Stack CMOS inverter is presented in figure 3.5

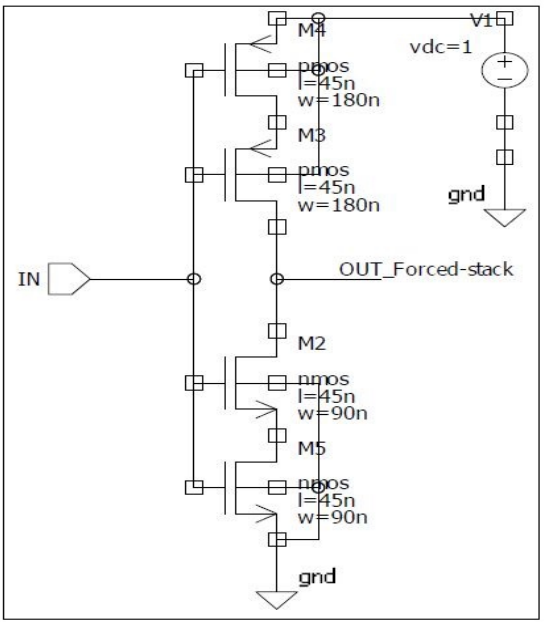

Fig 3.5 Schematic of Forced Stack CMOS inverter

As per forced stack technique each existing transistor is replaced by two two transistors each of width half of the original transistor to maintain the same input capacitance. Due to the stack effect[21] , effective resistance between Supply voltage & ground increases which reduces the leakage current and hence leakage power at the expense of delay.

Calculated average leakage power & delay for forced stack inverter is :

$$\tau_{avg} = 14.0485\ ps$$

$$P_{static} = 0.297\ nW$$

3.1.3 SLEEPY-STACK INVERTER

The schematic of Forced-Stack CMOS inverter is presented in figure 3.6

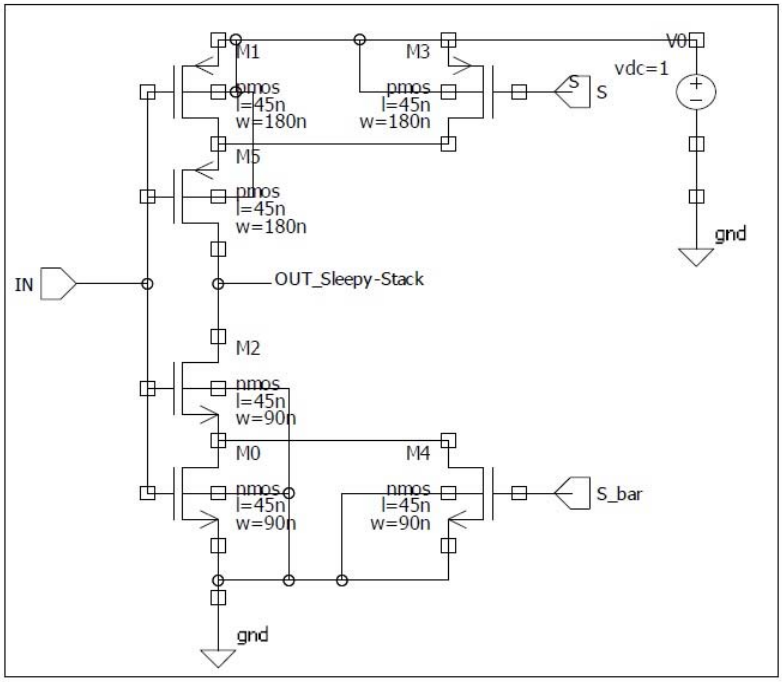

Fig 3.6 Schematic of Sleepy Stack CMOS inverter

Sleepy Stack inverter combines the advantage of both forced stack & sleep transitor inverter . Sleepy stack inverter overcomes the drawback of increased delay faced by forced stack by connecting a sleep transistor in parallel to one of the stacked transistor which in turn boosts the output driving capability. Leakage power is reduced by off sleep transistors as well as due to stacked transistors.

This advantage of increased speed is illustrated by results as given below:

$$\tau_{avg} = 6.795\ ps$$

$$P_{static} = 0.3254\ nW$$

3.1.4 LECTOR INVERTER

The schematic of LECTOR based CMOS inverter is presented in figure 3.7.

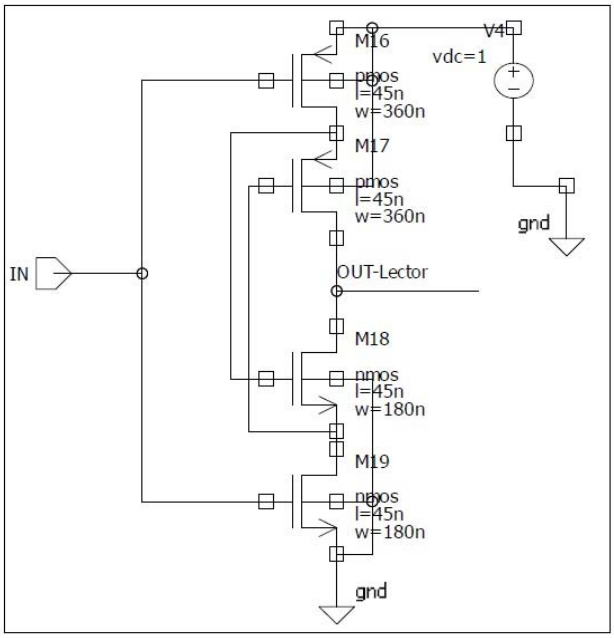

Fig 3.7 Schematic of LECTOR inverter

Lector approach introduces two self controlling transistors known as Leakage control transistors(LCT) between the Pull up network & Pull down network . Gate terminal of M18(LCT –NMOS) is connected to the source of M17(LCT-PMOS) and gate terminal of M17(LCT-PMOS) is connected to the source of M18(LCT-NMOS). Calculated average power & delay for lector inverter is :

$$\tau_{avg} = 9.565\ ps$$

$$P_{static} = 1.263\ nW$$

3.2 COMPARISON & ANALYSIS OF SIMULATION RESULTS

All the simulation in this thesis are performed using symica DE tool at 45nm PTM parameters. Static(Leakage) power & delay is calculated for a supply voltage of 1V for the following simulation environment.

Table 3.1 Simulation Environment I

Temperature	27 °C
Technology	45nm
Supply Voltage	1.0 V
Threshold voltage	V_{th} (NMOS) = 0.46893 V V_{th} (PMOS) = -0.49158 V

Table 3.2 Leakage Power(P_{static}) & Delay (τ_{pLH} & τ_{pHL}) of CMOS Inverter at 45nm

Technique	Delay(ps)		Static Power(nW)	
	τ_{pLH}	τ_{pHL}	Input= 0	Input= 1
Conventional	5.67	3.94	4.13	1.59
Forced-Stack	15.77	12.33	0.58	0.01
Sleepy-Stack	7.61	5.98	0.63	0.02
Sleepy-Stack (Dual V_{th})	11.42	6.96	0.43	0.002
Lector	12.46	6.67	2.04	0.49

Table 3.3 Comparison of Static(leakage) Power & Delay of Various CMOS Inverters w.r.t conventional CMOS Inverter.

Technique	Delay(ps)	Static Power(nW)	% Static Power Reduction
Conventional	4.80	2.86	0.00
Forced-Stack	14.05	0.30	89.61
Sleepy-Stack	6.80	0.33	88.62
Sleepy-Stack (Dual V_{th})	9.19	0.22	92.30
Lector	9.57	1.26	55.84

Table 3.4 Simulation Environment II

Temperature	27 °C
Technology	45nm
Supply Voltage	1.0 V
Threshold voltage	V_{th} (NMOS) = 0.3423 V V_{th} (PMOS) = -0.23122 V

Following results are claculated for the simulation environment mentioned in table 3.4.

Table 3.5 Leakage Power(P_{static}) & Delay (τ_{pLH} & τ_{pHL}) of CMOS Inverter at 45nm

Design	Delay(ps)		Static Power(nW)	
	τ_{pLH}	τ_{pHL}	Input= 0	Input= 1
Conventional	1.21	3.03	152.78	99.14
Forced-Stack	3.56	5.48	111.39	5.23
Sleepy-Stack	2.6	3.86	112.36	9.32
Sleepy-Stack(Dual V_{th})	8.50	0.98	87.21	0.03
Lector	0.84	3.48	133.92	73.19

Table 3.6 Comparison of Static(leakage) Power & Delay of Various CMOS Inverters w.r.t conventional CMOS Inverter

Design	Delay(ps)	Static Power(nW)	% Static Power Reduction
Conventional	2.12	125.96	0.00
Forced-Stack	4.52	58.31	53.71
Sleepy-Stack	3.06	60.84	51.70
Sleepy-Stack(Dual V_{th})	4.74	43.60	65.38
Lector	2.16	103.55	17.79

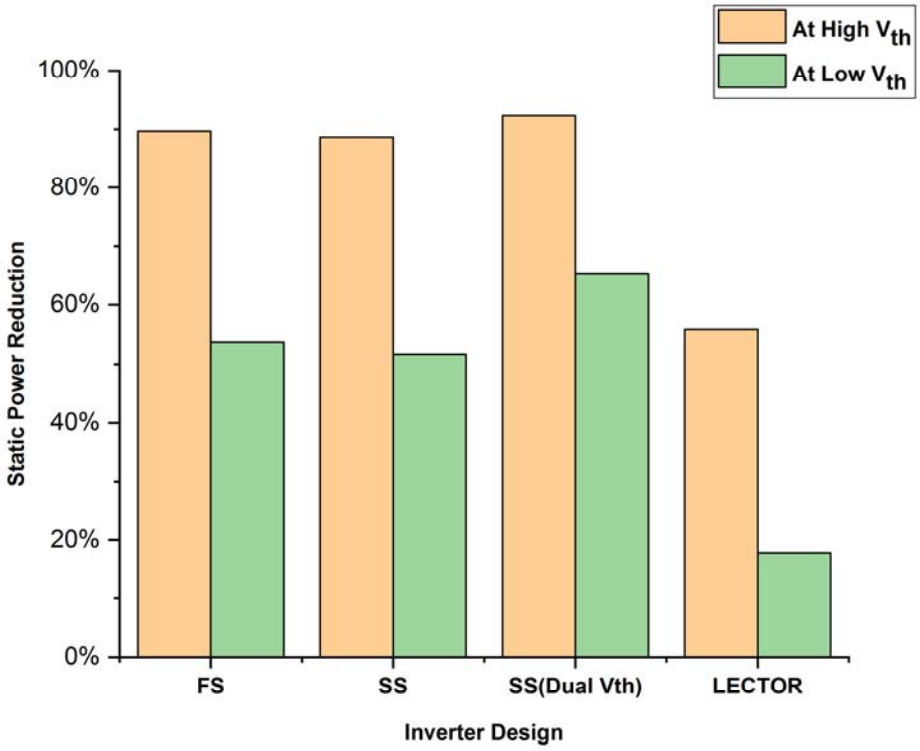

Fig 3.8 Percentage Static Power Reduction

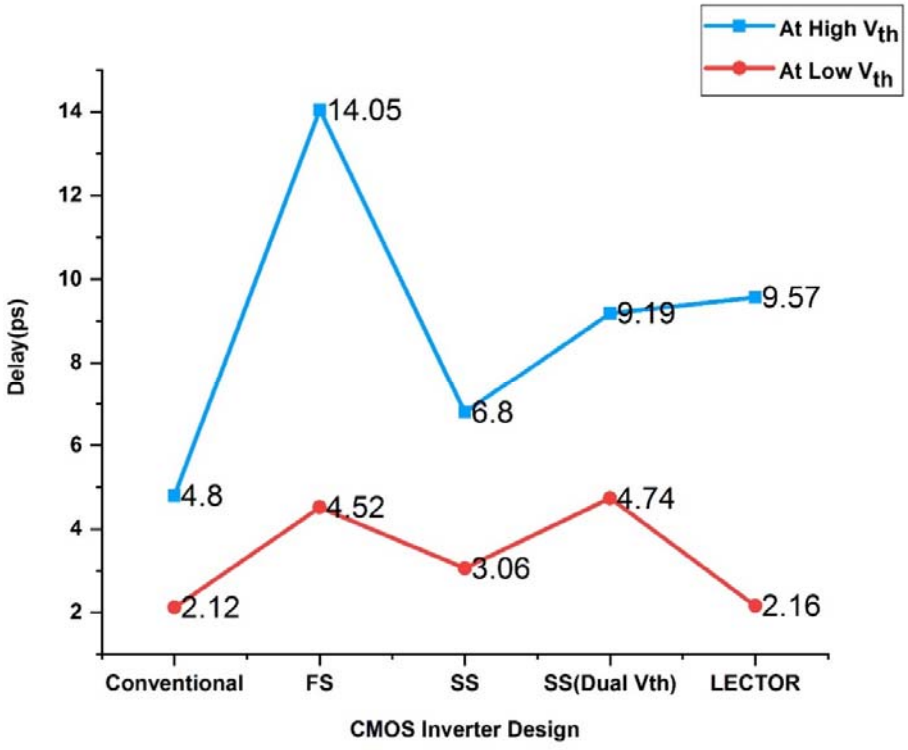

Fig 3.9 Delay of Various Inverters

As many researchers report that below 70 nm feature size static power dissipation of chip may exceed dynamic power. In this Chapter we have implemented the basic component of digital design i.e. CMOS inverter at 45nm and using simulation tool static power and delay is calculated .

In order to reduce static power CMOS inverter is modified with the help of several leakage power reduction techniques like forced stack, sleepy stack & LECTOR. Static power and delay of all the modified inverters is compared with the conventional CMOS inverter.

CHAPTER 4
STATIC POWER REDUCTION IN DDFF

Latches & Flip-Flops are the key components of the digital IC design. Sequential circuits without latches & Flip Flops are impractical. These elements are used to store information in digital form. Primary requirements for modern technology is high speed and power efficient system. As technology node is going lower & lower,the complexity goes on increasing which in turn affects the speed as well as power consumption.

One solution is to employ pipelined based design to overcome the issue of speed,but the delays involved in pipelined element (i.e Latches & FF) imposes the problem for the same. In conclusion, high performance flip-flops must be involved to achieve high speed design.

In past decades engineers in research domain has done a lot of work for improvising the throughput of the FF while considering it's effects on power because generally speed & power have inverse relation.Therefore, it necessitates the trade off between the two as per our application.

At broader level FF architectures can be categorized as static, dynamic and hybrid logic style.Dynamic style exhibits high speed and less area whereas static design style exhibits low power and higher noise margin .A hybrid design style combines the merit of low power consumption from static style and high speed from dynamic logic style. In this chapter will will concentrate on a hybrid flip flop named Dual Dynamic node pulsed hybrid flip flop(DDFF) & apply various static power reduction techniques on it to mitigate static power(Pstatic) .

4.1 DUAL DYNAMIC NODE HYBRID FLIP FLOP (DDFF)

Dual Dynamic Node Hybrid Flip-Flop (DDFF)[18] as shown below in Fig 4.1 is supposedly the most efficient flip flop architecture by far amongst all those we have discussed . In this architecture, nodes X1 and X2 are two dynamic nodes amongst which node X1 is pseudo dynamic with a weak inverter which behaves as the keeper

whereas X2 is essentially dynamic. The shut-off procedure is unconditional in DDFF as compared to a conditional one in XCFF which improves the timing charcterstics by reducing the hold time significantly.

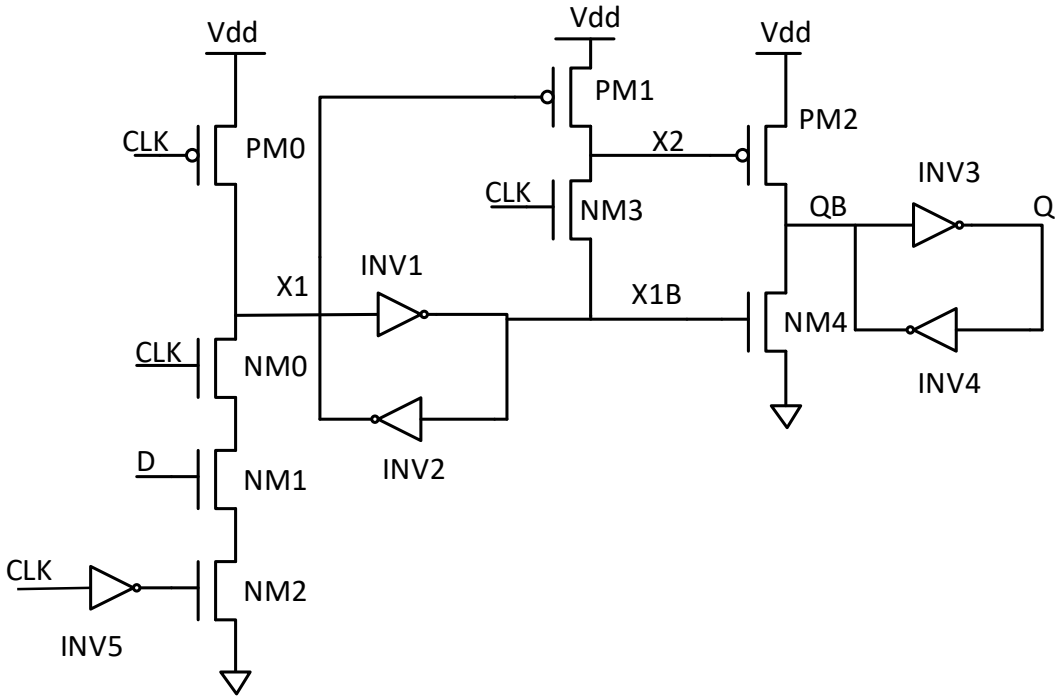

Figure 4.1 Structure of DDFF [18]

The operation of Dual Dynamic node hybrid Flip-Flop (DDFF) can be categorized into two phases namely pre-charge phase & the evaluation phase.

1) ***Precharge phase****:* When CLK falls low(i.e CLK='0'), the node X1 is pre-charged to Vdd via PM0 and the pair of inverters INV1-2 maintains the proper voltage level at Node X1. Node X1B will be at low voltage level(i.e'0') which keeps NM4 OFF. As clock is at low voltage level, NM3 is predominately OFF. Since X1 is at high voltage level, hence PM1 is also OFF. During the precharge phase node X2 is not actively driven by any transistor, therby storing the charge dynamically. Output voltage level at node Q & QB is maintained by Inverter pair INV3-INV4.
2) ***Evaluation Phase*** : Evaluation phase occurs when CLK goes from low to high this is also the end of pre-charge phase. Actual latching of Input data D occurs during the 1-1 overlap of CLK & CLKB during the evaluation phase.

Earlier to the overlap period if D is high then node *X*1 discharges via NM0-2, resulting in switching the state of the cross coupled inverter pair INV1-2 causing node *X*1*B* to go high and output *QB* to discharge via *NM*4. The low voltage level at node *X*1 is stored by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node *X*2 is kept high during the evaluation period by the pMOS transistor *PM*1. If *D* is zero before the CLK-CLKB overlapping , node *X*1 stays high and node *X*2 is dragged low through *NM*3 as the CLK rises high. Thus, node *QB* is charged high through *PM*2and *NM*4 is kept OFF. As clock falls low during the end of evaluation phase, node *X*1 remains high & *X*2 stores the charge dynamically.

A significant advantage of this architecture is that it exhibits negative setup time due to the short transparency period defined by the 1–1 overlap of CLK and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low [15].

This FF may suffer from charge sharing problem, when clock transitions from low to high state while D is kept low. Due to this charge sharing problem node X1 may fall temporary , but the inverter pair INV1-2 is skewed in a way such that it has a switching threshold well below the worst case voltage drop at node X1 .

Setup time & hold time are the important parameters for characterizing the performance of the flip flop. Setup time is defined as the minimum time before the active edge of the clock , data must be stable in order to latch the data properly . Similarly hold time is defined as the minimum time after the active edge of the CLK the data must be stable in order to work correctly. In DDFF setup and hold time depends on the CLK & CLKB overlapping period. If V_M is the switching threshold of the inverter pair INV1-2 & T_{VM} is the time required to discharge the node X1 discharges to V_M ,then the hold time expressions for input 0 & 1 respectively can be given as

$$T_{hold1} \geq T_{VM} \tag{4.1}$$

$$T_{hold0} \geq T_{OV} - T_{VM} \tag{4.2}$$

Where T_{hold1} and T_{hold0} are the hold time required for sampling data input 1 and 0 respectively & T_{ov} is the overlapping period of CLK and CLKB. T_{ov} should be greater than T_{VM} for the proper working of DDFF . Since CLKB is high prior to the low to high transition of the CLK, when *D* is high, the parasitic diffusion capacitors at the drain of *NM*1 and *NM*2 are predischarged, resulting in a low *T*vm. T_{ov} , the overlap period can be selected such that *T*hold1 and *T*hold0 in (4.1) and (4.2), respectively, are minimized. By proper sizing of the inverter pair overlapping period T_{ov} can be minimized[Rabeay reference]. Thus DDFF exits negative setup time & positive hold time close to zero which hepls in achieving better performance. Fig 4.2(a) presents the hold time for sampling input 0:

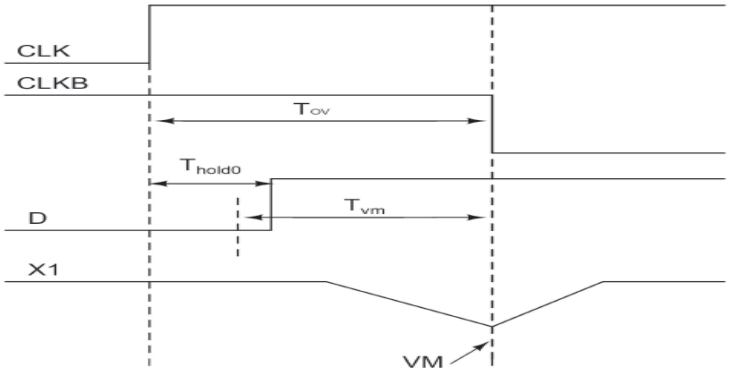

Figure 4.2(a) "Thold0 required by DDFF to sample "zero" .

In figure4.2(a) it is shown that as the data D is held zero for a time period somewhat greater than $T_{ov} - T_{vm}$ after the positive edge of CLK. This results in node X1 to discharge to a voltage level more than V_M & INV1-2 rebuilds the high voltage level leading to proper latching of zero .

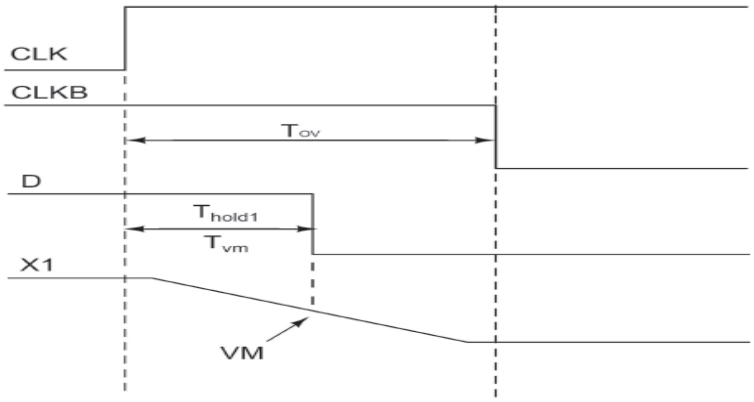

Figure 4.2(b) Thold1 required by DDFF to sample "one" .

Fig 4.2(b) presents the hold time for sampling input 1. As shown in figure, D is kept high for the duration T_{VM}, node X1 discharges to V_M & one in latched properly.

As discussed , T_{VM} plays a significant role in the hold time requirement of DDFF , the worst case hold time is governed by the the switching threshold of INV1-2. A bigger switching threshold(V_M) with a small overlapping period results in small T_{VM} and hence a smaller hold time & better performance.

4.2 IMPLEMENTATION OF DDFF

Originally DDFF was implemented by K. Absel [18] at 90nm technology node & 1.2 V power supply voltage. In this thesis we will implement DDFF at 45nm technology node & 1 V power supply voltage. Length of all the transistors is kept constant at 45nm & width of all the transistors is shown along with the transistors in figure 4.3.

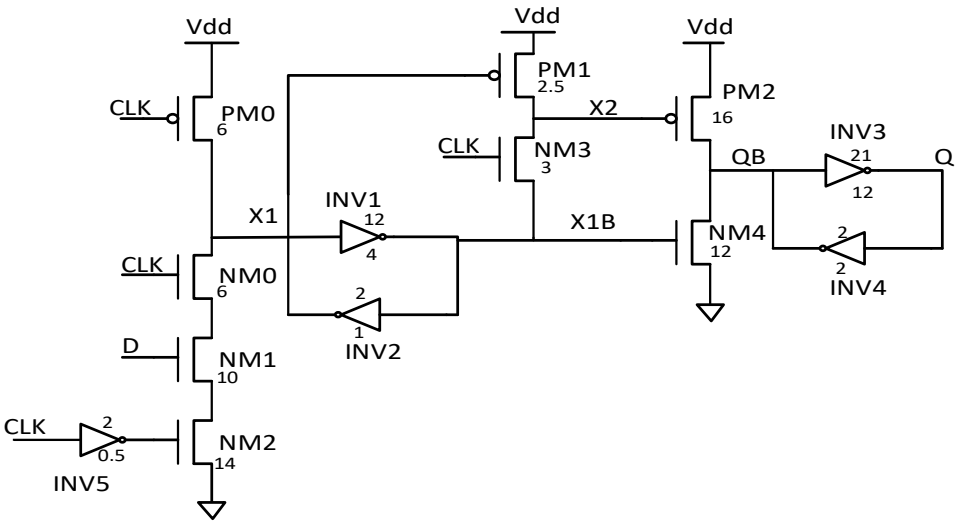

Fig 4.3 Implementation of DDFF at 45nm.

Simulation of the above circuit was done to find our several parameters like setup time, , Minimum D to Q delay and Static power. Simulation results of the DDFF at 45nm circuit is shown below:

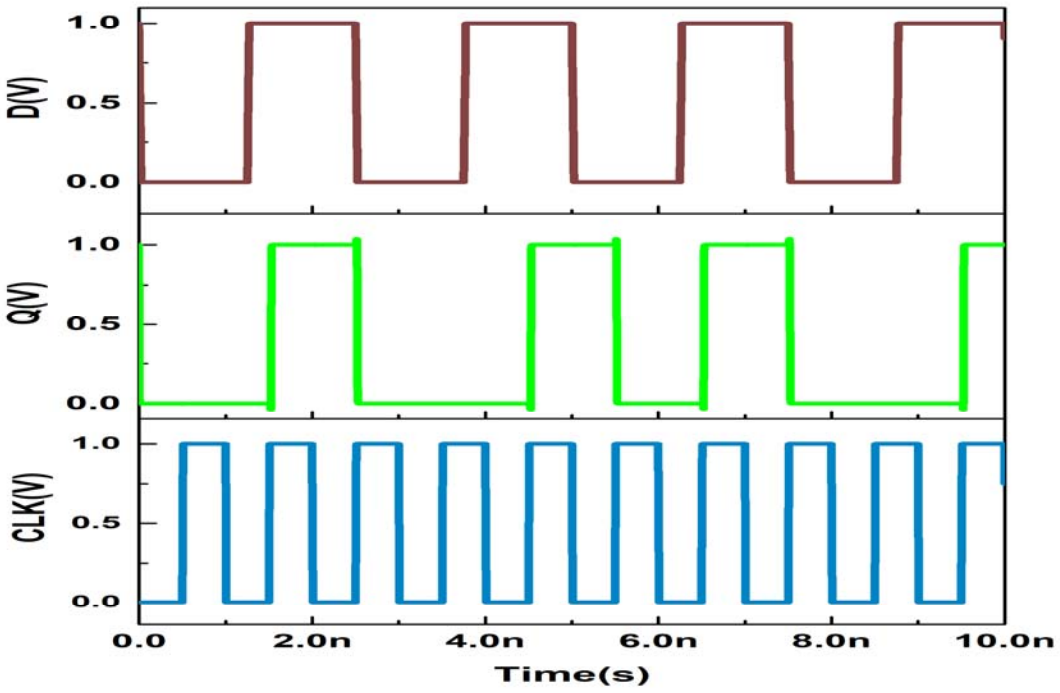

Fig 4.4 Timing diagram of DDFF operated at 1Ghz Frequency

Simulation of the above flip flop at at 27°C & 1V supply voltage measures setup time to be 6.83ps. T_{hold0} to be 30ps & T_{hold1} to be 15ps.Optimum setup time is -2.6ps with a minimum D to Q delay of 13.51ps. Table 4.1 shows the standby power consumption of DDFF at different threshold voltages & different combination of CLK & Data Signal.

Table 4.1 Standby Leakage power of DDFF

CLK,Data	Static Power(nW) at V_{tn}=0.46893 & V_{tp}=-0.49158	Static Power(µW) at V_{tn}=.3423 & V_{tp}=-0.23122
(0,0)	22.005	1.544
(0,1)	27.183	1.574
(1,0)	23.100	1.656
(1,1)	23.566	1.575
Average	23.964	1.587

It is clearly seen from the above table that as threshold voltage(V_{th}) decreases static power increases dramatically which becomes a serious problem for high performance devices. To solve this problem various techniques of leakage reduction will be applied to DDFF to reduce the leakage power without degrading the performance of DDFF.

4.3 STATIC POWER REDUCTION IN DDFF

Though many leakage reduction techniques are available in literature but only those techniques can be applied to DDFF which does not degrade the performance & does not increase the area. In this section we will discuss various modified structures of DDFF.

4.3.1 FS-DDFF

In order to reduce static power, forced stack technique is applied to DDFF. Structure of FS-DDFF is same as that of DDFF except CMOS inverters INV1-4 are replaced with forced stack CMOS inverters as shown in Fig 4.5. Forced stack inverters utilizes stack effect due to which sub-threshold current reduces which in turn reduces static power as static power is directly proportional to the sub-threshold current.

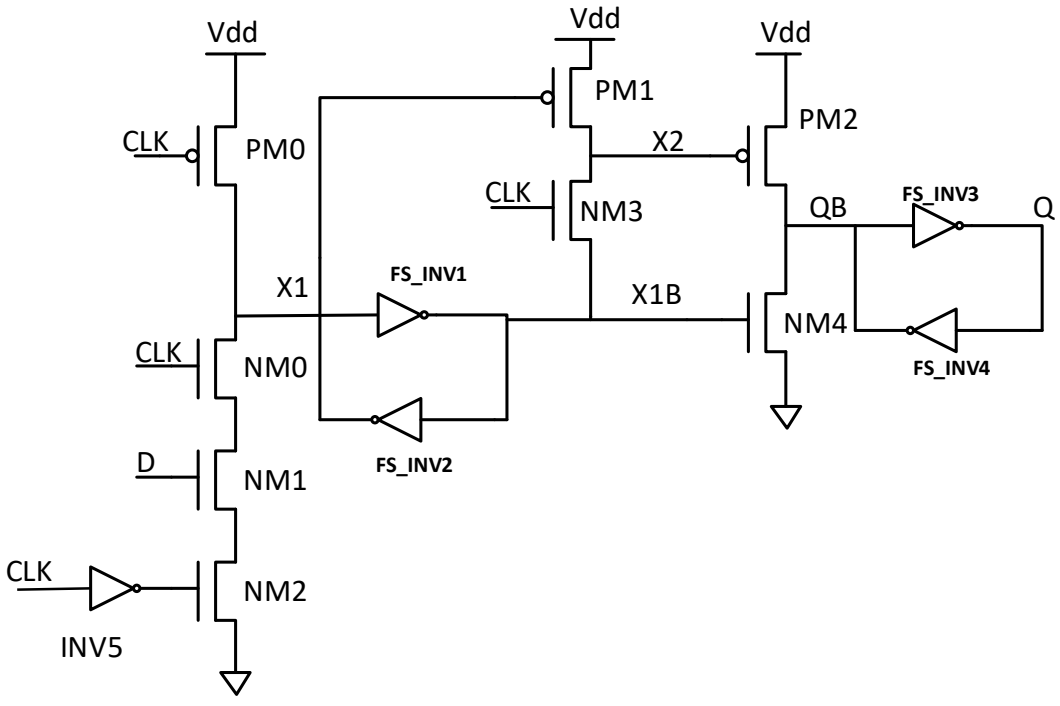

Fig 4.5 Structure of FS-DDFF

4.3.2 SS-DDFF

Structure of Sleepy Stack Inverter pair based DDFF is shown in Figure 4.6. In SS-DDFF Inverters INV1-4 present in DDFF are replaced with sleepy stack inverters which takes advantages of both techniques i.e. sleep transistor & forced stack to overcome the problem of leakage power. But sleepy stack inverters increase the area as each transistor present in CMOS inverter is replaced with three transistors .

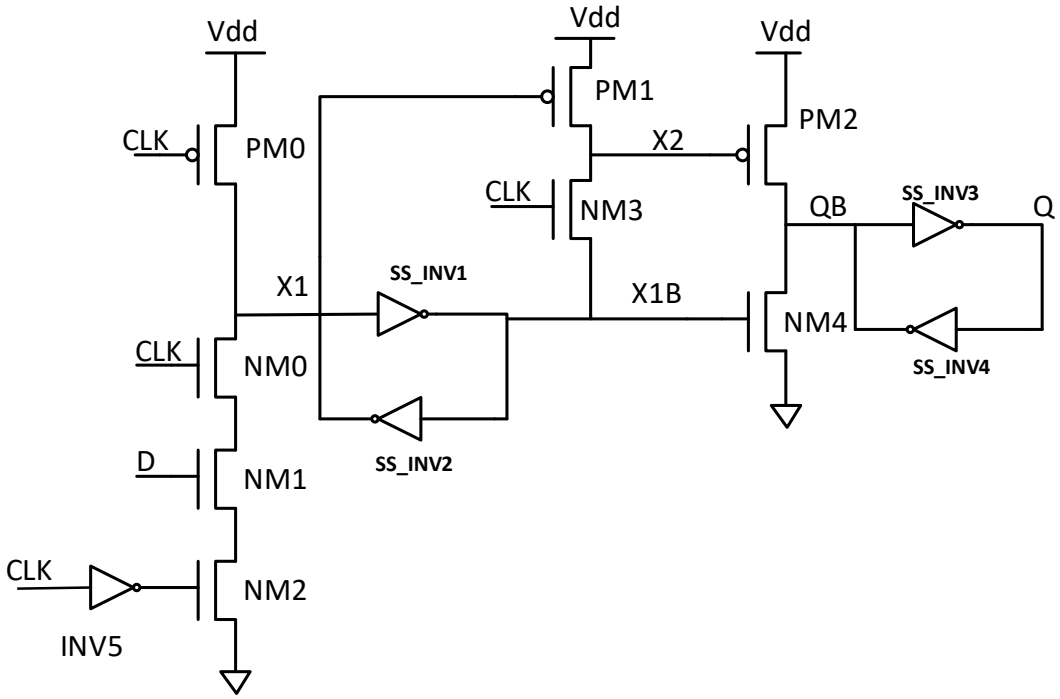

Fig 4.7 Structure of SS-DDFF

4.3.3 LECTOR DDFF

Structure of LECTOR DDFF is shown in Figure 4.7. In Lector-DDFF Inverters INV1-4 present in DDFF are replaced with lector based inverters Lector_INV1-4. In lector based inverter two leakage control transistors (LCT1 & LCT2) are inserted in between the PMOS & NMOS of CMOS inverter in such a way that one of the leakage controlling transistor is always operating in near cut-off region which reduces leakage current. The operation of Lector DDFF is same as that of the conventional DDFF.

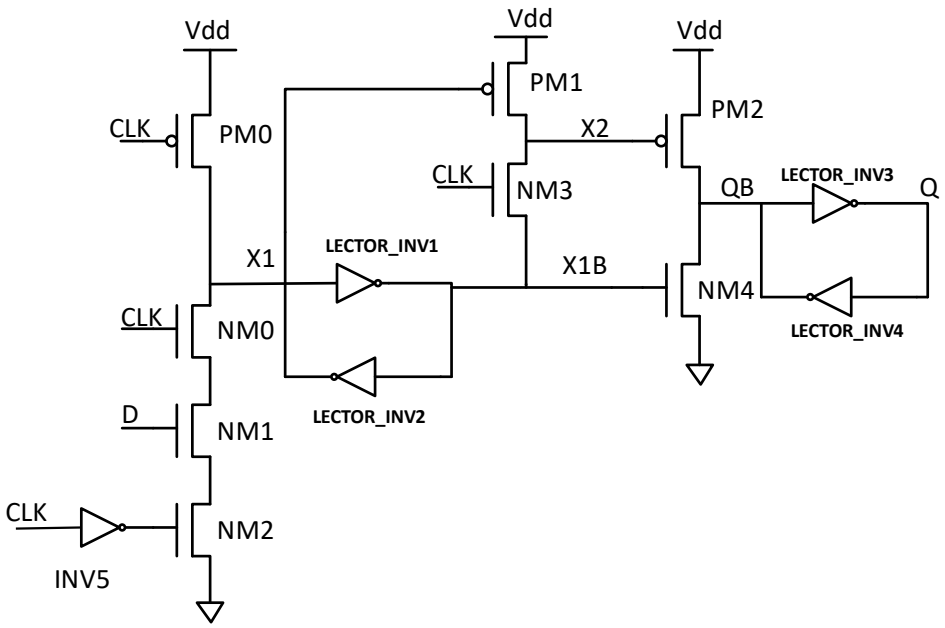

Fig 4.7 Structure of Lector-DDFF

4.4 COMPARISON OF VARIOUS FLIP FLOPS

Various performance parameters of all the presented flip flops are calculated and compared with the conventional DDFF. All the simulation results are calculated at 27°C & 1V supply voltage. The results are presented in form comparison table and the graphs to show relative variation of different parameters with different threshold voltages.

The comparison have been done at 45nm technology node with supply voltage 1.0 V and different combination of CLK and D have been taken into consideration. Table 4.2 shows the comaparison of modified DDFF design with conventional DDFF for static power with **V_{tn}=0.46893** & **V_{tp}=-0.49158.**

Table 4.2 Power leakage in standby mode(nW) with $\mathbf{V_{tn}=0.46893}$ & $\mathbf{|V_{tp}|=0.49158}$

FF Design	DDFF	FS-DDFF	SS-DDFF	Lector-DDFF
CLK,Data =(0,0)	22.005	14.707	14.748	16.970
CLK,Data =(0,1)	27.183	19.885	19.925	22.150
CLK,Data =(1,0)	23.100	9.820	9.845	14.945
CLK,Data =(1,1)	23.566	8.816	9.019	14.950
Average	23.964	13.307	13.384	17.254

Table 4.3 shows the comaparison of modified DDFF design with conventional DDFF for static power with V_{tn}=0.3423 & $|V_{tp}|$=-0.23122 at different combinations of CLK & Data.

Table 4.3 Power leakage in standby mode(μW) with $\mathbf{V_{tn}=0.3423}$ & $\mathbf{V_{tp}=-0.23122}$

FF Design	DDFF	FS-DDFF	SS-DDFF	Lector-DDFF
CLK,Data =(0,0)	1.544	1.057	1.086	4.300
CLK,Data =(0,1)	1.574	1.097	1.126	4.341
CLK,Data =(1,0)	1.656	1.022	1.052	5.586
CLK,Data =(1,1)	1.575	1.432	1.439	6.150
Average	1.587	1.152	1.176	5.094

Fig 4.8 shows the same comparison of Static power graphically which is given in table 4.2. Here we can observe that FS-DDFF , SS-DDFF, LECTOR-DDFF reduced the static power by significant amount . FS-DDFF & SS-DDFF saved consumption of static power by similar amount but greater than LECTOR-DDFF.

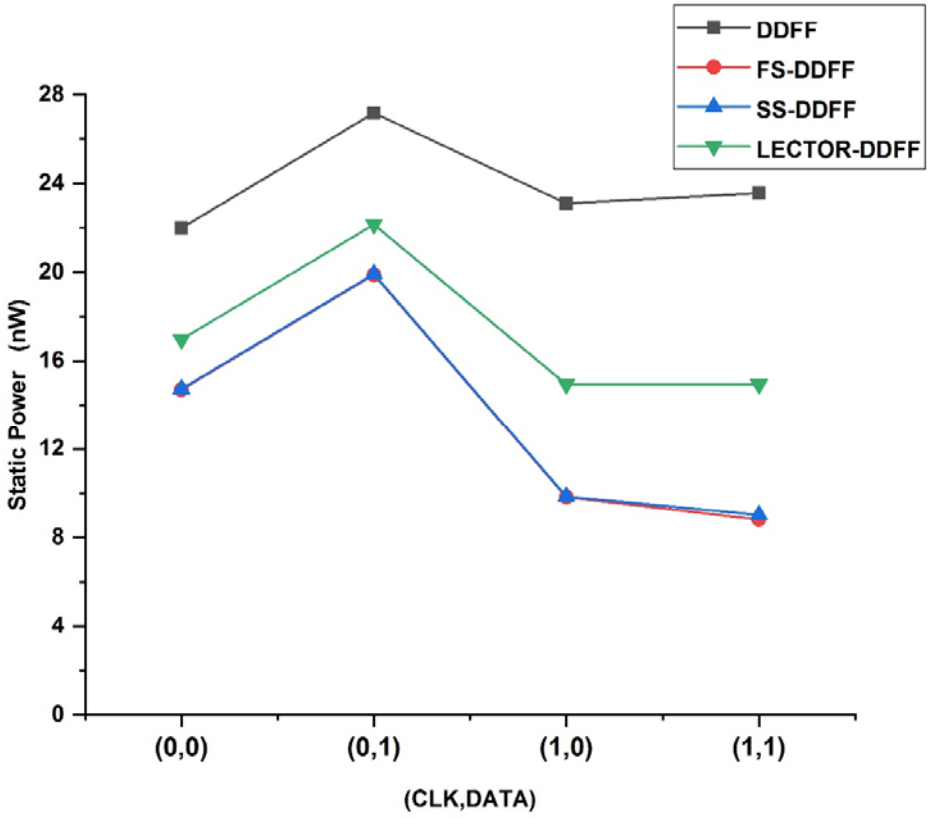

Fig 4.8 Power leakage in standby mode(nW) with V_{tn}=0.46893 & $|V_{tp}|$=0.49158

Fig 4.9 shows the same comparison of Static power graphically which is given in table 4.3. Here we can observe that FS-DDFF , SS-DDFF reduced the static power by similar amount but LECTOR-DDFF failed to reduce the static power as threshold voltage becomes lower.

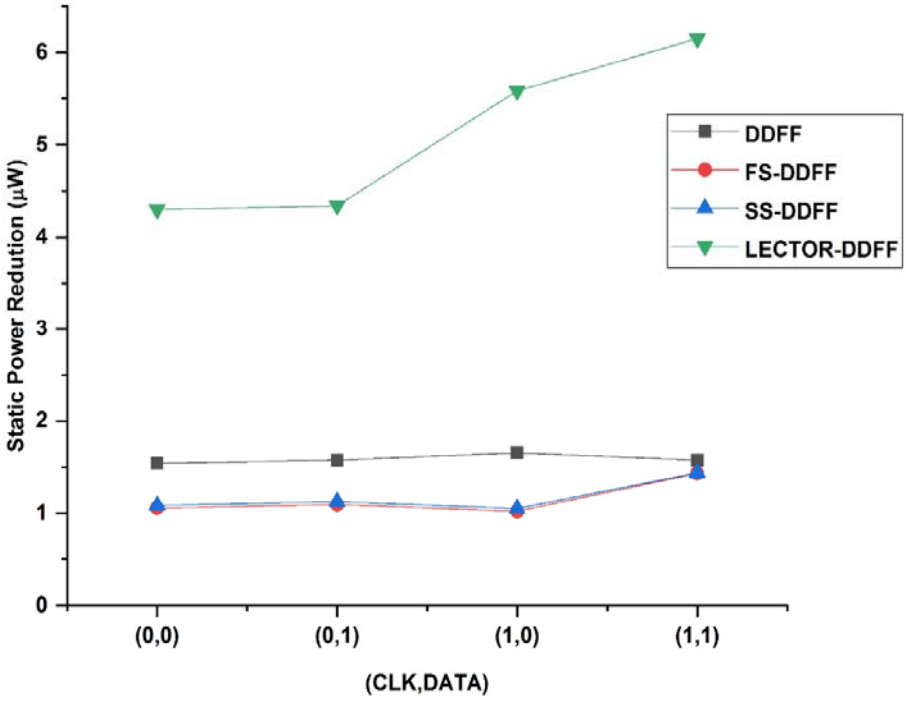

Fig 4.9 Power leakage in standby mode(µW) with V_{tn}=0.3423 & $|V_{tp}|$=0.23122

Table 4.4 shows the comaprison of setup time & minimum D-Q delay of various configuration of DDFF. We observed that FS-DDFF & SS-DDFF increases the minimum D-Q delay while Lector has similar delay as compared to conventional DDFF. Setup time is also better observed in case of LECTOR -DDFF.

Table 4.4 Comparison of timing parameters

FF Design	DDFF	FS-DDFF	SS-DDFF	Lector-DDFF
Setup time(ps)	-6.75	-8.25	-8.25	-11.50
Min D to Q delay(ps)	13.06	17.87	17.97	13.43

CHAPTER 5
STATIC POWER REDUCTION IN ULTRA-LOW VOLTAGE CIRCUITS

During the past few years demand for high-performance and low-power digital systems has grown rapidly. Several factors have contributed to this fast growth. First, laptop and notebook computers, and personal communication systems have gained popularity. Consequently, portable applications that traditionally required a modest performance (such as wrist watches and calculators), are now dominated by devices that demand a very high performance. The demand for portability of these new systems limits their battery weight and size, placing a severe constraint on their power dissipation. Second, speed, density, and size of non-portable CMOS based systems have increased considerably in recent years. Thus, power consumption that was not a concern in these systems, is now becoming a critical parameter. The most common approach for reducing power is power supply scaling. This is due to the fact that in CMOS digital circuits, delivered power is proportional to the square of power supply voltage

$$\mathbf{P= C_L V_{dd}^2 \mathit{f}} \qquad (5.1)$$

where **P** is the power consumed by one gate, $\mathbf{C_L}$ is the total switching capacitance of the gate, V_{dd} is the power supply voltage and ***f*** is the average cooperating frequency of that gate. Since power supply reduction below three times the threshold voltage (3Vt) will degrade circuit speed significantly, scaling of the power supply should be accompanied by threshold voltage reduction [29]. However, the lower limit for threshold voltage is set by the amount of off-state leakage current that can be tolerated (due to standby power consideration in static circuits, and avoidance of failure in dynamic circuits and memory arrays), and ideally should be no less than 0.4 V. It is seen that if standard MOSFET's are used, a lower bound for power supply voltage or a larger leakage current become inevitable. To extend the lower bound of power supply to ultra-low voltages (0.6 V and below), a Dynamic Threshold Voltage MOSFET (DTMOS) was introduced having a high ***Vt*** at zero bias and a low ***Vt*** at Vgs = Vdd.

Due to the growing demand for longer battery life in mobile devices, mobile integrated circuit (IC) designers have focused on reducing the power consumption of circuits, especially for supply voltage scaling. As a result, the supply voltage has been greatly reduced, and subthreshold circuits have been developed.

However, lowering the supply voltage simultaneously degrades the noise immunity of the circuit [30]–[31]. Since the threshold voltages have not scaled as aggressively as the supply voltage, the static noise margin of digital circuits has continuously decreased. Therefore, the signal itself is more vulnerable for the external noise and the immunity to electromagnetic interference (EMI) has become an important issue for IC designers, and several solutions have been proposed [32]–[41].A Schmitt trigger is one such solution that can be appropriately used to enhance the noise immunity of a circuit at the expense of delay and power consumption [42]–[43]. Unlike comparator circuits, the switching threshold of the Schmitt trigger depends on the direction of input signal transition, a phenomenon known as *hysteresis*. In the presence of hysteresis, the threshold voltage of the Schmitt trigger is higher than that of comparators for positive transitions and lower for negative transitions. If the amplitude of the input signal variation is less than the switching threshold difference, the output of the Schmitt trigger will not respond directly to input. This makes the Schmitt trigger immune to undesired electromagnetically coupled noise. Thus in this chapter we will first discus the basics of DTMOS & Schmitt trigger . After getting the basic functionality of DTMOS & Schmitt trigger we will implement a ultra low voltage VTCMOS Schmitt trigger based buffer & apply various static power reduction techniques on it .

5.1 DTMOS TRANSISTOR & ITS PRINCIPLE

DTMOS transistor shows high threshold characteristic when it is off to minimize the leakage and at the same, it behaves as a low threshold device for high current drivability under low voltage supplies. This feature makes it as a promising candidate for modern ultra-low-voltage digital circuits. As shown in Fig. 1(a), a PMOS transistor's gate and body terminals are connected without requiring any additional processing steps and it can be produced in standard CMOS technology. For NMOS DTMOS transistor SOI fabrication technology can be used. DTMOS transistor and its commonly used circuit

symbol are shown in Fig.5.1. This configuration although goes back to earlier dates [34] Assederaghi et al. extensively describe the device and express underlying reasons of its operation. The idea is to connect the gate and body of the device to dynamically change the threshold voltage of the transistor by utilizing the relation in (5.2).

$$V_{TH} = V_{T0} + \gamma(\sqrt{|2\Phi_F| + VSB} - \sqrt{|2\Phi_F|}) \quad (5.2)$$

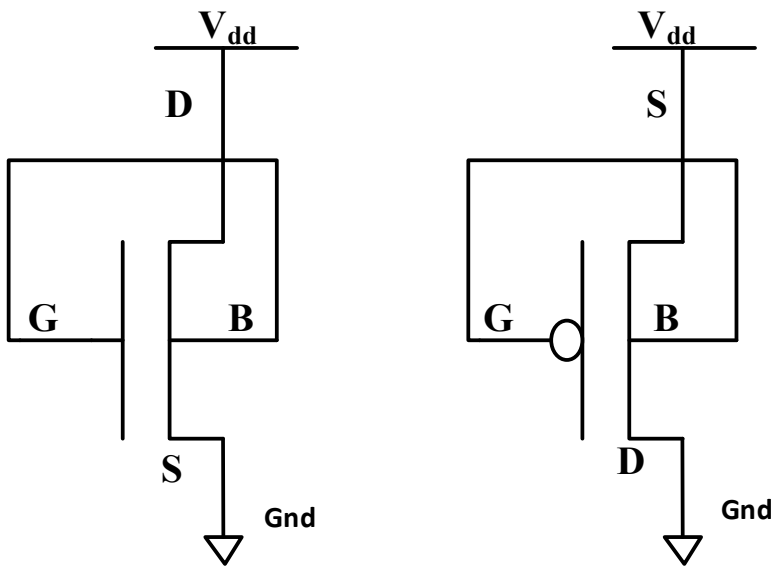

Fig 5.1: NMOS and PMOS transistors based on DTMOS circuit topology[34].

Where, Vth is threshold voltage when VSB is not zero, Vto is the zero body bias threshold voltage and mainly depends on the manufacturing process. γ is the body effect coefficient (typically equals to 0.4 V0.5) and it depends on the gate oxide capacitance, silicon permittivity, doping level and other parameters. ΦF is the surface potential at threshold (typically | − 2φF | equals 0.6 V). VSB is the source-to-body voltage. From (2) it can be seen that the threshold voltage depends on VSB which in turn affects the depletion region charge density or body charges. Forward bias across the junction reduces the junction width and hence depletion region charge density which in turn reduces Vth. Reverse bias increases the depletion region width and hence increases body charges due to which Vth also increases. As DTMOS based circuits make use of forward bias, therefore when input is high, the transistor will be on resulting in reduction of Vth and higher driving capability . When the transistor is turned off, Vth becomes high, resulting in low leakage current. Thus the threshold voltage is changed

dynamically according to the input at the gate i.e. operating state of the circuit. Thus DTMOS enables the circuit to operate under the low voltage supply hence suitable for low voltage operation due to its dynamic threshold voltage.

5.2 SCHMITT TRIGGER AND IT'S PRINCIPLE

Schmitt trigger has the useful property of showing hysteresis in its dc characteristics—its switching threshold is variable and depends upon the direction of the transition (low-to-high or high-to-low). This peculiar feature can come in handy in noisy environments.

A Schmitt trigger is a device with two important properties:

1. It responds to a slowly changing input waveform with a fast transition time at the output .
2. The voltage-transfer characteristic of the device displays different switching thresholds fo r positive- and negative-going input signals.

One of the main uses of the Schmitt trigger is to turn a noisy or slowly varying input signal into a clean digital output signal. This is illustrated in Figure 2. Notice how the hysteresis suppresses the ringing on the signal. At the same time, the fast low-to-high (and high-to-low) transitions of the output signal should be observed. For instance, steep signal slopes are beneficial in reducing power consumption by suppressing direct-path currents. The "secret" behind the Schmitt trigger concept is the use of positive feedback.

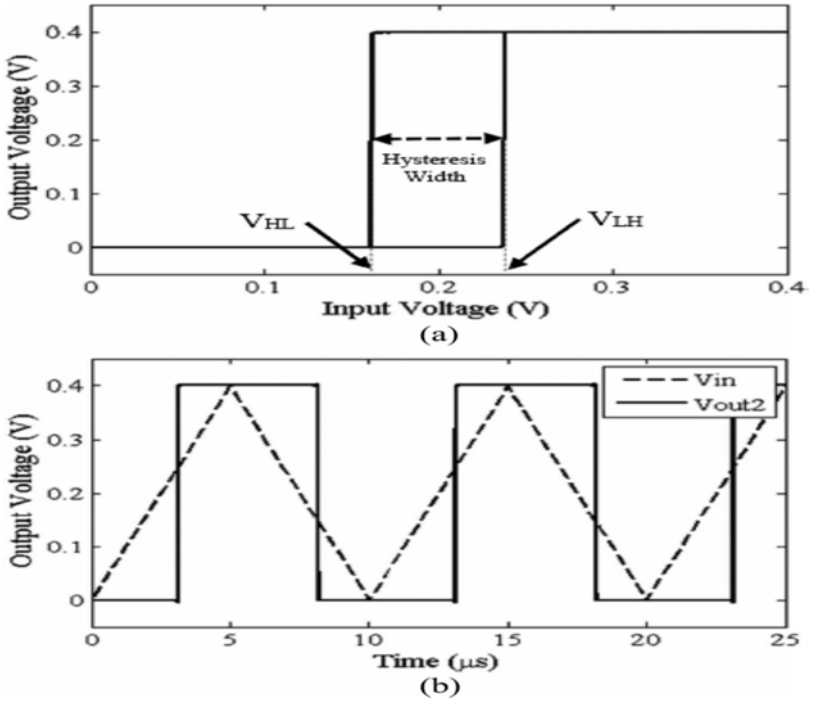

Fig 5.2. (a)Voltage transfer characteristic of a Schmitt trigger buffer. (b) Input and output waveforms of a Schmitt trigger buffer .

A Schmitt trigger is one such solution that can be appropriately used to enhance the noise immunity of a circuit at the expense of delay and power consumption [42]–[43]. Unlike comparator circuits, the switching threshold of the Schmitt trigger depends on the direction of input signal transition, a phenomenon known as *hysteresis*. In the presence of hysteresis, the threshold voltage of the Schmitt trigger is higher than that of comparators for positive transitions and lower for negative transitions. If the amplitude of the input signal variation is less than the switching threshold difference, the output of the Schmitt trigger will not respond directly to input. This makes the Schmitt trigger immune to undesired electromagnetically coupled noise.

5.3 CONVENTIONAL ST BASED INVERTER/BUFFER

Conventional CMOS Schmitt trigger Inverter present in the literature is shown below in Fig (5.3) below:

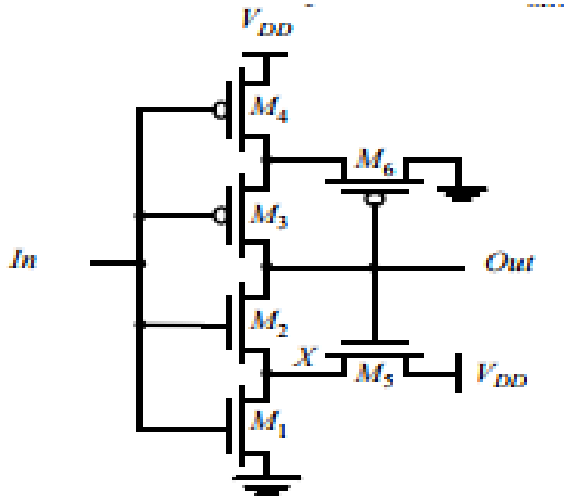

Fig.5.3 CMOS based Schmitt trigger[35]

But the above circuit is not suitable for low power applications. For low power applications DTMOS based ST based inverter was introduced as shown below.

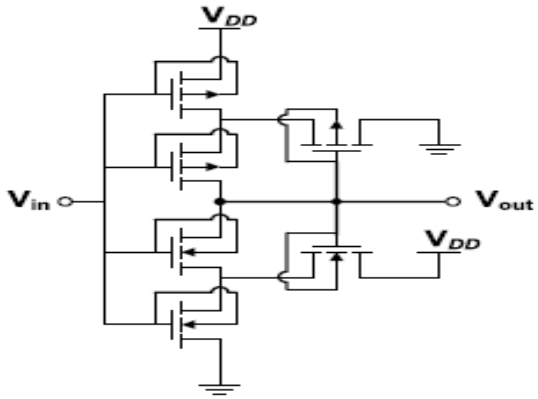

Fig 5.4. Traditional DTMOS based CMOS ST Inverter [44]

Several approaches can be used to implement Schmitt trigger circuits suitable for low-power design. Since traditional CMOS Schmitt trigger circuits requires too many extra transistors for practical implementation, the dynamic threshold voltage MOS (DTMOS) design using a reduced number of transistors was proposed in year 2003[22] , as shown in Fig 5.5.

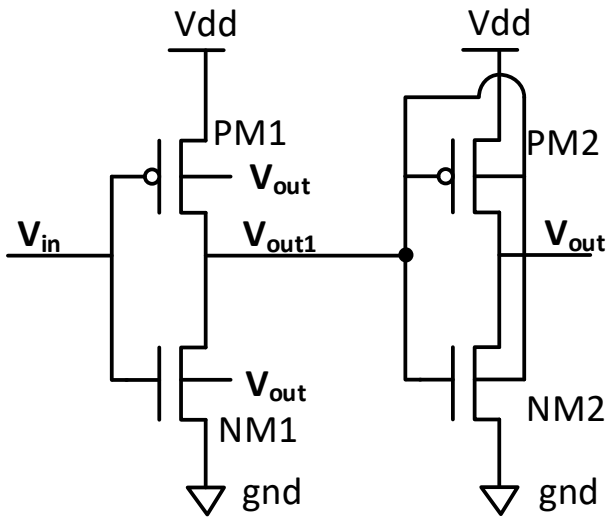

Fig 5.5 Conventional VTCMOS based Schmitt trigger Inverter / Buffer[37]

The above buffer based design approach using DTMOS for low power operation can be applied to NAND/NOR gates , which will dramatically improve the noise immunity with much lower power consumption and significant area reduction compared with significant area reduction compared with CMOS Schmitt triggers at the expense of slight increase in delay .

The traditional design schematic of the Schmitt trigger, shown in Fig. 5.4, can implement hysteresis by using an extra current path that resists the signal transition of the output node through the use of current feedback. In this case, extra power consumption is unavoidable when enhancing the noise immunity because the feedback circuit produces extra current in order to maintain the output in the presence of a noisy input signal. Therefore, the traditional design method for the Schmitt trigger is not suitable for low-power designs.

In contrast, the schematic of Fig. 5.5 shows the use of a voltage feedback path from the output of the second stage to the substrate of the first-stage inverter for hysteresis implementation. In this way, there is no extra current requirement to secure the stability of the output, which is more appropriate for low power design. In addition, the inverter output *V*out1 and the buffer output *V*out2 can be merged into one logic gate. The

threshold voltage of the DTMOS must be lowered below the supply voltage to ensure the operation of the transistor in the saturation region because the supply voltage is near the normal threshold voltage value (0.4V). To lower the threshold voltage, the gate and substrate are tied together to generate a forward body bias condition at the body-to-source junction. Utilizing the body effect with negative source-to-body bias condition, this method can decrease the threshold voltage. However, the substrate bias of the first-stage inverter, shown in Fig. 6, is connected to *V*OUT2 and is independent of its input node. Therefore, the threshold voltage of the first stage varies according to the value of *V*OUT2; this design is called variable threshold voltage CMOS (VTCMOS). Since each transistor in the first stage is set to a zero-body bias condition for the output transition, the turn-on voltage of each transistor is higher for the case shown in Fig. 6 than it is for normal DTMOS. The switching threshold voltage can be described with the following equations:

$$V_{LH} = \frac{VDD - |V_{th,\,p}| + \zeta \times V_{th0,\,(n)}}{\zeta + 1} \tag{5.3}$$

$$V_{HL} = \frac{VDD + \zeta \times V_{th,\,(n)} - |V_{th0,\,p}|}{\zeta + 1} \tag{5.4}$$

where $V_{th,p(n)}$ is the threshold voltage of the PMOS (NMOS) for the forward bias condition; $V_{th0,p(n)}$ is the threshold voltage of the zero-bias condition, $\zeta = \sqrt{(\beta n/\beta p)}$; and βn and βp are the transconductance parameters of NMOS and PMOS, respectively .

The above VTCMOS Scmitt trigger based Inverter/buffer design efficiently uses the advantages of DTMOS transistor to improve the noise immunity with much lower switching power consumption and significant area reduction as compared to CMOS based Schmitt trigger inverter. But DTMOS transistor offers the same off state leakage as that of the MOS transistor which makes is not suitable as we move towards lower technology node. Static(leakage) power dissipation(Pstatic) dominates over dynamic power dissipation in deep sub micron technologies. Thus by some method off state

leakage current must be reduced in order to make it suitable for battery operated low power applications.

5.4 FORCED –STACK VTCMOS ST BUFFER/ INVERTER

VTCMOS Schmitt trigger based buffer /inverter is the most efficient design but its performance can be further increased by applying various static power reduction tehniques like forced stack, sleepy stack & Lector with the slight increase in are overhead. Forced Stack VTCMOS buffer/inverter structure is shown in fig 5.6. Operation of this buffer is similar to the conventional VTCMOS schmutt trigger buffer . Forced stacking technique is applied to the VTCMOS Inverter by replacing the existing pmos and nmos transitor with two transistors each of width half of the original transistor respectively. Forced Stack technique utilizes stack effect to reduce the subthreshold leakage current & hence reduces the static power dissipation.

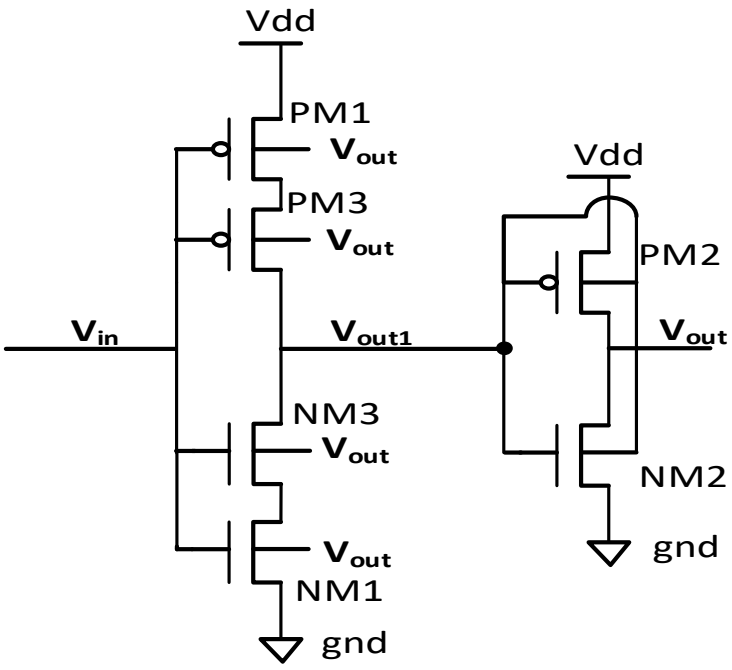

Fig 5.6 FS-VTCMOS based Schmitt trigger Inverter / Buffer

5.5 SLEEPY-STACK VTCMOS ST BUFFER /INVERTER

Structure of the Sleepy-Stack VTCMOS buffer/inverter is shown in Figure 5.7 In this structure the VTCMOS inverter is replaced with Sleepy stack VTCMOS inverter. Sleepy stack inverter pair retains the exact logic state in standy mode as compared to

that of sleep transistor in which current state may be lost. It also overcomes the delay penalty which occurs in forced stack technique. Two additional control signals are required S & S' which are connected to the gate terminal of PMOS & NMOS sleep transitor respectively

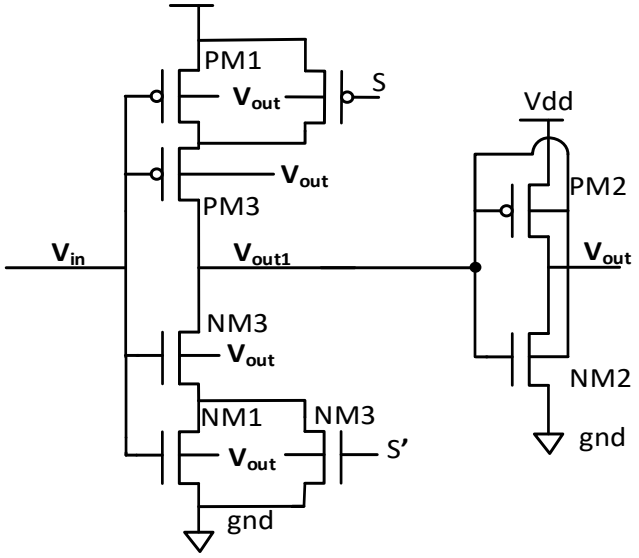

Fig 5.7 SS-VTCMOS based Schmitt trigger Inverter / Buffer

5.6 LECTOR VTCMOS ST Buffer / Inverter

Static (leakage) power dissipation (Pstatic) of conventional VTCMOS Schmitt trigger Inverter/buffer can be reduced by inserting two leakage controlling transistors beween the NMOS & PMOS of VTCMOS inverter. Lector based VTCMOS Buffer / Inverter structure is shown in figure 5.8.

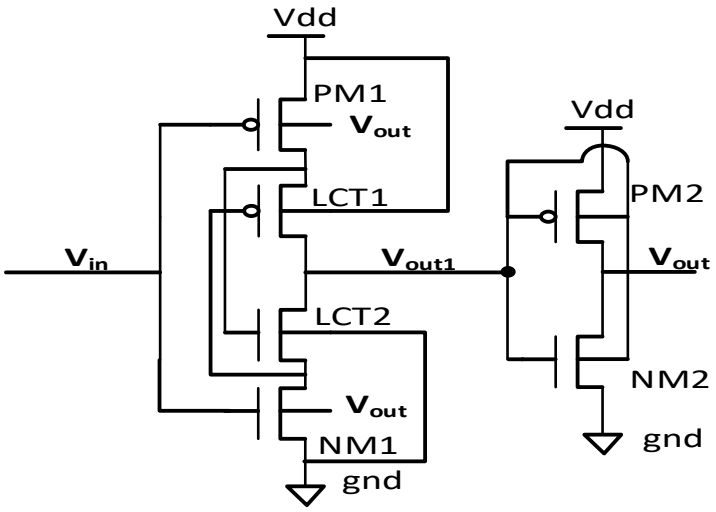

Fig 5.8 LECTOR VTCMOS based Schmitt trigger Inverter / Buffer

5.7 SIMULATION & ANALYSIS

All the ultra-low voltage VTCMOS Schmitt trigger based buffer / Inverter shown in this chapter are simulated using symica DE v3.0 at 45nm & 130nm PTM technology parameters. Static power & delay of various circuits are calculated at various temperatures with a power supply voltage of 0.4 volt. The different values of temperature are 27°C , 55°C & 120°C.

Schematic of Conventional VTCMOS Scmitt Trigger based buffer / Inverter is shown in fig 5.9 along with its hysteresis curve in figure 5.10 .

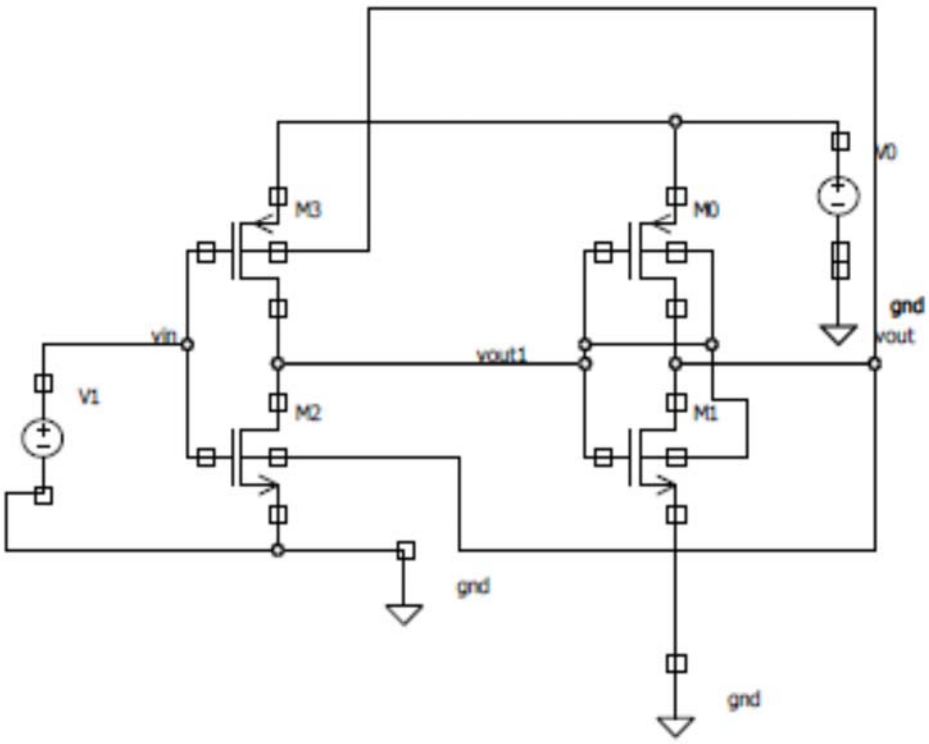

Fig 5.9 Schematic of Conventional VTCMOS ST based buffer / Inverter

Fig 5.10 shows the hysteresis plot for a buffer using VTCMOS buffer and a traditional Schmitt trigger inverter followed by DTMOS inverter. Due to the use of Variable threshold scheme VTCMOS buffer achieves higher noise immunity as compared to Traditional Schmitt trigger inverter with a DTMOS Inverter which makes it a better candidate for low voltage low power operation since the threshold voltages have not scaled as aggressively as the supply voltage, the static noise margin of digital circuits

has continuously decreased. Therefore, the signal itself is more vulnerable for the external noise and to electromagnetic interference(EMI).

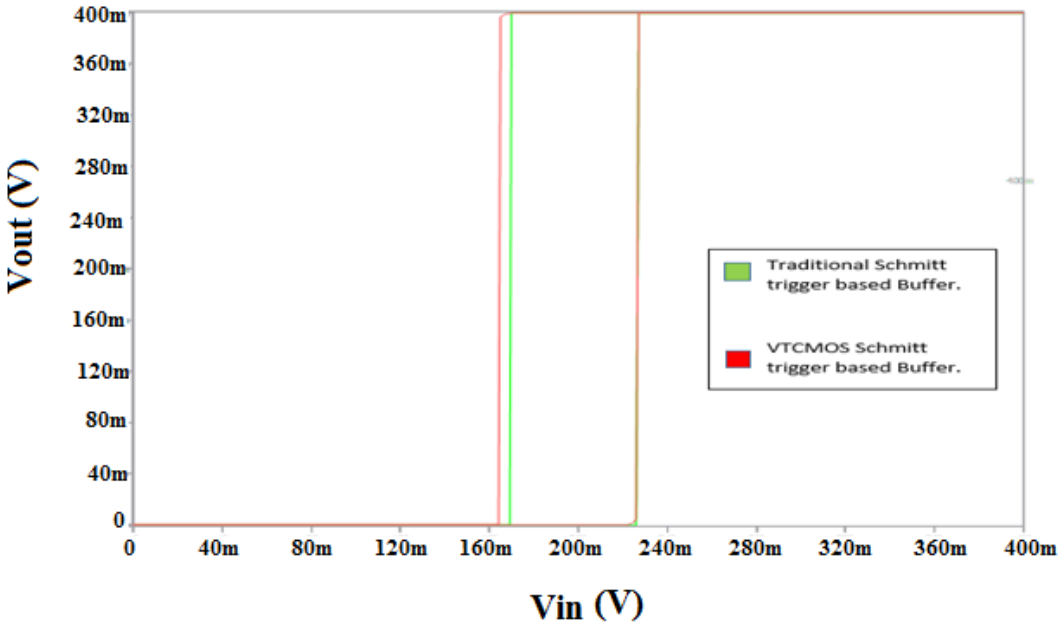

Fig 5.10 Hysteresis Plot for a buffer using VTCMOS buffer and a Traditional Schmitt trigger inverter with a DTMOS Inverter.

Figure 5.11 shows the timing diagram of all the presented VTCMOS ST based buffer. Input pulse with a period of 10μs and amplitude of 0.4 V is applied to all the VTCMOS ST based buffer . It was mandatory to check whether all the presented VTCMOS ST based buffer follows the basic functionality of buffer/inverter as well as giving higher static noise margin. From the figure it is observed that all the presented VTCMOS based buffer serves the basic functionality of buffer as well as providing better static noise margin as compared to traditional Schmitt trigger inverter with a DTMOS inverter. This all has become possible only due to the presence of VTCMOS based inveter present in VTCMOS ST based buffer.

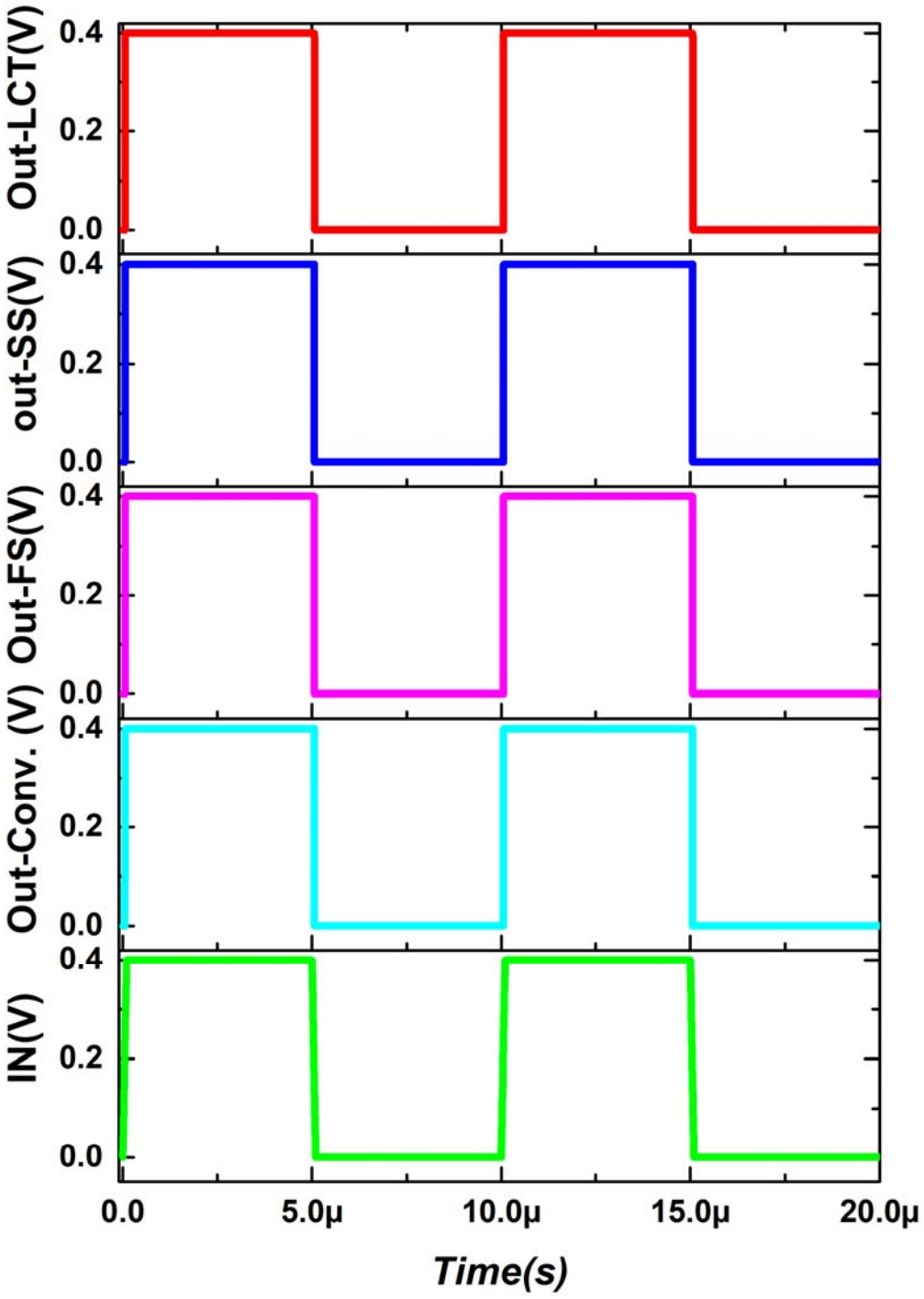

Fig 5.11 Timing diagram of all VTCMOS ST buffer

Different performance parameters of Conventional VTCMOS ST based buffer, FS-VTCMOS ST based buffer, SS-VTCMOS ST based buffer & LECTOR-VTCMOS ST based buffer are tabulated in Table 5.1, 5.2 , 5.3, 5.4 respectively.

Table 5.1 Static Power & delay of Conventional VTCMOS ST based Buffer

Technology Node	Delay(ns)	Static Power(nw)	Temperature
45nm	2.878	15.115	T=27°C
	2.6714	27.835	T=55°C
	2.148	93.962	T=120°C
130nm	4.3886	7.4895	T=27°C
	4.27684	14.835	T=55°C
	4.0662	50.289	T=120°C

Table 5.2 Static Power(Pstatic) & delay of FS VTCMOS ST based Buffer

Technology Node	Delay(ns)	Static Power(nw)	Temperature
45nm	2.8818	9.418	T=27°C
	2.62066	16.95	T=55°C
	1.988	58.115	T=120°C
130nm	5.3158	3.7185	T=27°C
	5.8554	7.51845	T=55°C
	5.59914	26.4115	T=120°C

Table 5.3 Static Power(Pstatic) & delay of SS VTCMOS ST based Buffer

Technology Node	Delay(ns)	Static Power(nw)	Temperature
45nm	4.55	9.932	T=27°C
	4.368	17.985	T=55°C
	3.938	61.87	T=120°C
130nm	5.3766	3.879	T=27°C
	5.9182	7.8291	T=55°C
	5.6624	27.8315	T=120°C

Table 5.4 Static Power(Pstatic) & delay of LECTOR VTCMOS ST based Buffer

Technology Node	Delay(ns)	Static Power(nw)	Temperature
45nm	4.9258	16.652	T=27°C
	4.662	31.105	T=55°C
	3.942	107.5712	T=120°C
130nm	7.6806	6.52955	T=27°C
	7.4628	13.1197	T=55°C
	7.0904	45.9275	T=120°C

5.8 COMPARISON OF VARIOUS BUFFER/INVERTERS

Various performance parameters of all the modified VTCMOS ST buffer/Inverter are calculated and compared with the conventional VTCMOS ST buffer/Inverter. All the simulation results are calculated at 0.4V supply voltage. The results are presented in comparison table and the graphs to show relative variation of different parameters with different temperature. The performance results are compared at different values of temperature i.e at 27°C ,55°C & 120°C.

Table 5.5 shows the comparison of all the modified VTCMOS ST Buffer with conventional VTCMOS ST based buffer at 45nm Technology node.

Table 5.5 Comparison table of Various VTCMOS ST buffer at 45nm Technology node.

45nm Technology Node			
Buffer/ Inverter Design	**Static Power(nW)**	**Delay(ns)**	**Temperature**
VTCMOS ST	15.115	2.879	T=27°C
FS-VTCMOS ST	9.418	2.882	
SS-VTCMOS ST	9.932	4.550	
LECTOR-VTCMOS ST	16.652	4.926	
VTCMOS ST	27.835	2.671	T=55°C
FS-VTCMOS ST	16.950	2.621	
SS-VTCMOS ST	17.985	4.368	
LECTOR-VTCMOS ST	31.105	4.662	

VTCMOS ST	93.962	2.148	T=120°C
FS-VTCMOS ST	58.115	1.988	
SS-VTCMOS ST	61.870	3.938	
LECTOR-VTCMOS ST	107.571	3.942	

Fig 5.12 shows the graphical comparsison of static power at 45nm . It is clear that static power dissipation increases as temperature increases. Both the buffer has very less static power dissipation and FS- VTCMOS buffer further reduces the static power as compared to conventional VTCMOS-ST. FS-VTCMOS ST buffer has less static power dissipation at every value of temperature.

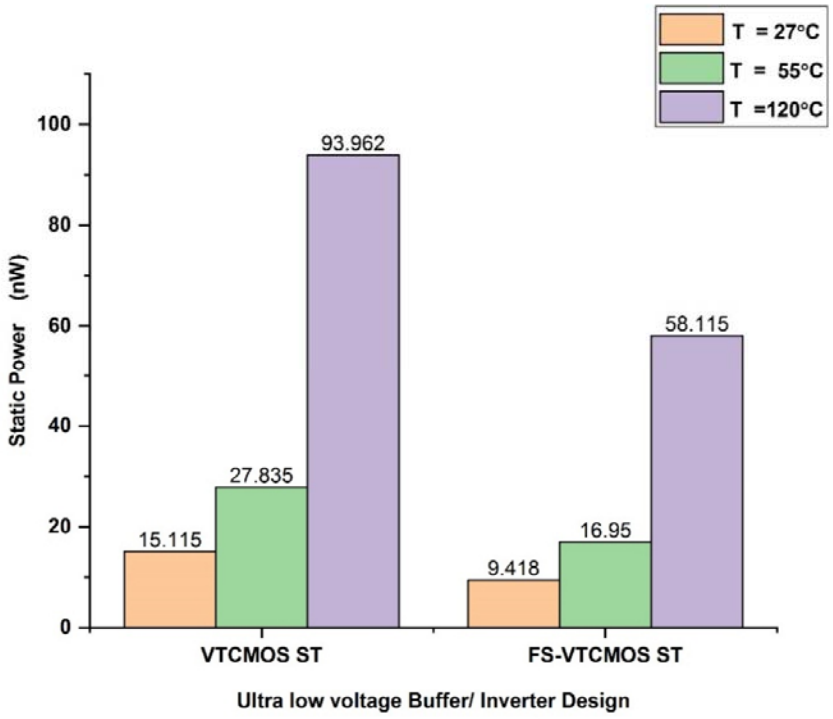

Fig 5.12 Static Power of VTCMOS ST buffer & FS VTCMOS ST buffer at 45nm.

Table 5.5 shows the comparison of all the modified VTCMOS ST Buffer with conventional VTCMOS ST based buffer at 45nm Technology node.

Table 5.6 Comparison table of Various VTCMOS ST buffer at 130nm Technologynode.

130nm Technology Node			
Buffer/ Inverter Design	**Static Power**	**Delay**	**Temperature**
VTCMOS ST	7.490	4.389	T=27°C
FS-VTCMOS ST	3.719	5.316	
SS-VTCMOS ST	3.879	5.377	
LECTOR-VTCMOS ST	6.530	7.681	
VTCMOS ST	14.835	4.277	T=55°C
FS-VTCMOS ST	7.518	5.855	
SS-VTCMOS ST	7.829	5.918	
LECTOR-VTCMOS ST	13.120	7.463	
VTCMOS ST	50.289	4.067	T=120°C
FS-VTCMOS ST	26.412	5.599	
SS-VTCMOS ST	27.382	5.662	
LECTOR-VTCMOS ST	45.928	7.090	

Fig 5.13 shows the graphical comparsison of static power at 130nm . It is clear that static power dissipation increases as temperature increases. Both the buffer has very less static power dissipation and FS- VTCMOS ST buffer further reduces the static power as compared to conventional VTCMOS-ST. FS-VTCMOS ST buffer has less static power dissipation at every value of temperature.

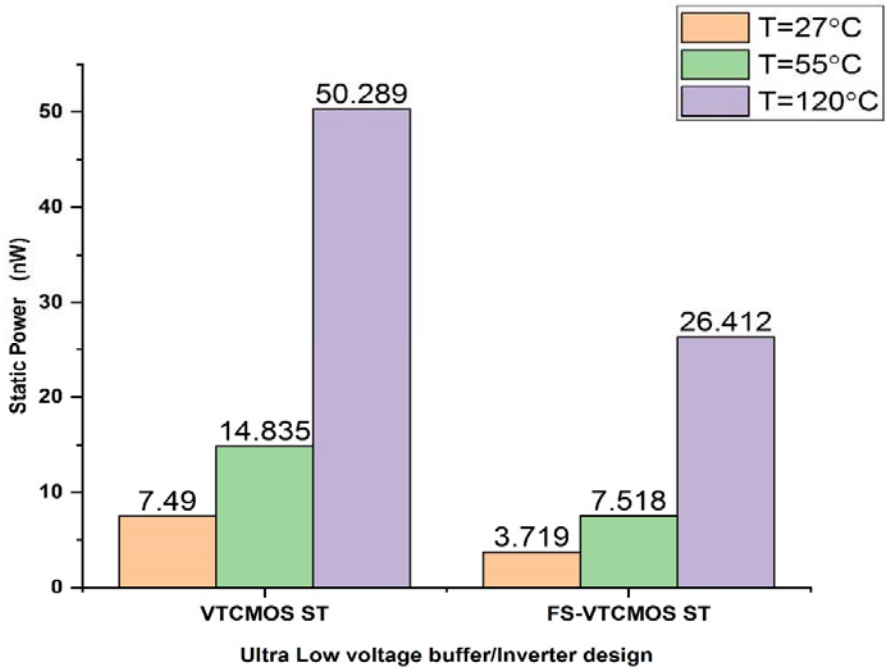

Fig 5.13 Static Power of VTCMOS ST buffer & FS VTCMOS ST buffer at 130nm.

As the supply voltage of a circuit decreases, noise immunity becomes more important to guarantee signal integrity. This chapter presents a method of improving noise immunity and reducing static power applicable to subthreshold circuits. The traditional method for immunity enhancement is to use a Schmitt trigger, which requires an additional current path to adjust the switching threshold voltage and a large area. However,by utilizing the VTMOS scheme, which adjusts the threshold voltage of the MOS transistor to implement the hysteresis of the transfer characteristics, both area and switching power consumption can be significantly reduced while simultaneously providing improved noise immunity, at the expense of a slight increase in delay. Therefore, the proposed VTCMOS based digital logic design can enable noise-immune low-power IC design . Futher for power constrained portable systems static power can be futher reduced by utilizing FS VTCMOS inverter in the first stage of VTCMOS ST buffer. FS VTCMOS ST buffer has the same propagation delay as that of conventionaln VTCMOS ST buffer.

CHAPTER 6

CONCLUSION & FUTURE SCOPE

In order to reduce power consumption voltage scaling is done as switching power has quadratic dependency on supply voltage. In order to faciliatate voltage scaling without affecting the performance threshold voltage has to be reduced. Scaling down of threshold volatage V_{th} results in exponential increase in subthreshold leakage current. As subthreshold leakage conduction being the most predominant amongst all the sources of static power consumption need to be handled carefully in order to reduce static power consumption . In sub-100nm CMOS technology, static power consumption can be nearly equal to dynamic power consumption thus, effective handling of Static power is a great challenge. Hence , efficient static power reduction techniques are very critical for the deep sub-micron and nanometer circuits. In this work efficient static power reduction techniques: 1)Forced Stack 2) Sleepy Stack 3) LECTOR has been discuseed along with their applications.

In case of CMOS inverter Sleepy stack technique (dual V_{th}) has a maximum static power reduction of about 92.3% for high V_{th} & 65.38% for low V_{th} using 45nm PTM BSIM4 . Sleepy stack (single V_{th}) provides the optimum performance by reducing static power dissipation by 88.62% and 51.70% for high and low Vth respectively. At Low Vth LECTOR technique reduces the static power dissipation by about 18% without any delay penalty.

In case of DDFF both FS & SS technique saves the static power by around 44% at high V_{th} and around 27.41% at low V_{th} with a certain increase in minimum D-Q delay. Lector technique saves 28% of static power at high V_{th} without degrading the performance of DDFF.

As most of the electronic devices we encounter in daily life are battery operated, there is immense need to save power consumption in that circuits in order have greater usage time . As the supply voltage of a circuit decreases, noise immunity becomes more

important to guarantee signal integrity. This thesis presents a method of improving noise immunity and reducing static power applicable to subthreshold circuits. The traditional method for immunity enhancement is to use a Schmitt trigger, which requires an additional current path to adjust the switching threshold voltage and a large area. However,by utilizing the VTMOS scheme, which adjusts the threshold voltage of the MOS transistor to implement the hysteresis of the transfer characteristics, both area and power consumption can be significantly reduced while simultaneously providing improved noise immunity, at the expense of a slight increase in delay. Therefore, the VTCMOS based digital logic design can enable noise-immune low-power IC design. Futher for power constrained portable systems static power can be futher reduced by utilizing FS VTCMOS inverter in the first stage of VTCMOS ST buffer. FS VTCMOS ST buffer has the same propagation delay as that of conventional VTCMOS ST buffer.

FS VTCMOS ST buffer attains the static power reduction of about 38% at different values of temperature with similar amount of delay as compared to conventional VTCMOS ST buffer/inverter.

REFERENCES

[1] "International Technology Roadmap for Semiconductors," Semiconductors Industry association, 2005.

[2] N. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J. Hu, M. Irwin,M. Kandemir, and V. Narayanan, "Leakage current: Moore's Law meets static power," *IEEE Comput*., vol. 36, no. 12, pp. 68–75, Dec 2003.

[3] V.De and S.Borkar, "Technology and design challenges for low power and high performance*," Proc. Int. Symp. Low Power Electroics and Design*, 1999, pp.163-168.

[4] K.Roy and S.C.Prasad, "Low-power CMOS VLSI ciruit design". New York: Wiley, 2000, ch. .5, pp.214-219.

[5] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits*, vol. 27, no. 4, pp.473–484, Apr. 1992.

[6] Gu, R.X and M.I Elmasry, "Power dissipation analysis and optimization of deep sub-micron CMOS digital circuits," *IEEE journal of solid-state circuits*, vol. 31, pp.707-713, 1996.

[7] A. Keshavarzi, K. Roy and C. F. Hawkins, "Intrinsic leakage in low power deep submicron CMOS ICs," *Test Conference, 1997. Proceedings., International,* Washington, DC, 1997, pp. 146-155. doi: 10.1109/TEST.1997.639607

[8] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits", In Proc. IEEE, vol. 91, pp. 305-327, Feb., 2003.

[9] N. Hanchate and N. Ranganathan, "LECTOR: a technique for leakage reduction in CMOS circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 2, pp. 196-205, Feb. 2004. doi: 10.1109/TVLSI.2003.821547

[10] J. C. Park and V. J. Mooney III, "Sleepy Stack Leakage Reduction," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 11, pp. 12501263,Nov.2006. doi10.1109/TVLSI.2006.886398

[11] M. Priya, K. Baskaran, and D. Krishnaveni, "Leakage Power Reduction Techniques in Deep Submicron Technologies for VLSI Applications," *Procedia Engineering*, vol. 30, pp. 1163–1170, 2012.

[12] S. Singhal, N. Gaur, A. Mehra, and P. Kumar, “Analysis and comparison of leakage power reduction techniques in CMOS circuits,” *2015 2nd International Conference on Signal Processing and Integrated Networks (SPIN)*, 2015.

[13] J. Yuan and C. Svensson, “New single-clock CMOS latches and flip flops with improved speed and power savings,” *IEEE J. Solid-State Circuits*, vol. 32, no. 1, pp. 62–69, Jan. 1997

[14] F. Klass, “Semi-dynamic and dynamic flip-flops with embedded logic,” in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, Jun. 1998, pp. 108–109.

[15] V. Stojanovic and V. Oklobdzija, “Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems,” *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[16] N. Nedovic and V. G. Oklobdzija, “Hybrid latch flip-flop with improved power efficiency,” in *Proc. Symp. Integr. Circuits Syst. Design*, 2000, pp.211–215.

[17] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y.Oowaki, “Conditional data mapping flip-flops for low-power and high performance systems,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*,vol. 14, no. 12, pp. 1379–1383, Dec. 2006.

[18] K. Absel, L. Manuel and R. K. Kavitha, "Low-Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Featuring Efficient Embedded Logic," in *IEEE Transactions on Very Large Scale Integration (VLSI)Systems*, vol. 21, no. 9, pp. 1693-1704, Sept. 2013. doi: 10.1109/TVLSI.2012.2213280

[19] H. Veendrick, “Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits,” *IEEE Journal of Solid-State Circuits*, vol. 19, no. 4, pp. 468–473, 1984

[20] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko and C. Hu, *Electron Device Letters, IEEE*, 8, 515 (1987).

[21] R.F. Pierret, *Semiondutor Device Fundamentals*:Reading,MA:Addison Wesley,1996

[22] N. H. E. Weste and D. M. Harris, *CMOS VLSI design: a circuits and systems perspective*. Pearson, 2015

[23] R.Krishnarnurthy, A. Alvandapour, V.De, S. Borkar, “High-Performance and Low-Power Challenges for Sub- 70 nm Microprocessor Circuits”, *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference.*

[24] L. Wei, Z. Chen, M. Johnson, K. Roy and V. De, “Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits”, *Proceedings of the 35th Design Automation Conference (DAC)*, 1998, pp. 489-494.

[25] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, , S. Shigematsu, and J. Yamada, "1V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," *IEEE Journal of Solid-State Circuits* 30, August 1995, pp. 847-854.

[26] Kao, J. T., and Chandrakasan, A. P. "Dual-Threshold Voltage Techniques for Low-power Digital Circuits," *IEEE Journal of Solid State Circuits*, vol.35, no.7, July 2000, pp.1009-1018.

[27] S. Narendra, S. Borkar, V. De, D. Antoniadis, and A. Chandrakasan, "Scaling of stack effect and itsapplication for leakage reduction," *Proc. Intl. Symp. Low Power Electronics and Design*, 2001,pp. 195–200

[28] J. M. Rabaey, A. P. Chandrakasan, and Nikolić Borivoje, *Digital integrated circuits: a design perspective*. Delhi: PHI Learning Private Limited, 2013

[29] D. Liu, C. Svensson, "Trading speed for low-power by choice of supply and threshold voltages", *IEEE J. Solid-State Circuits*, vol. 28, pp. 10-17, Jan. 1993.

[30] M. Ramdani, E. Sicard, A. Boyer, S. B. Dhia, J. J. Whalen, T. H. Hubing, M. Coenen, O. Wada, "The electromagnetic compatibility of integrated circuits—Past present and future", *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 1, pp. 78-100, Feb. 2009.

[31] D. Bol, R. Ambroise, D. Flandre, J.-D. Legat, "Interests and limitations of technology scaling for subthreshold logic", *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 17, no. 10, pp. 1508-1519, Oct. 2009.

[32] V. Golumbeanu, P. Svasta, and D. Leonescu, "The noise immunity for the low voltage logic circuits," in *Proc. 9th Mediterranean Electrotechnical Conf.*, 1998, pp. 116–119.

[33] K. L. Shepard, "Design methodologies for noise in digital integrated circuits," in *Proc. 35th Annu. Design Autom. Conf.*, 1998, pp. 94–99.

[34] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and Hu Chenming,"A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation," in *Proc. Int. Electron Devices Meet. Tech.Digest*, 1994,pp. 809–812.

[35] B. L. Doki´c, "CMOS NAND and NOR Schmitt circuits," *Microelectron. J.*, vol. 27, no. 8, pp. 757–765, Nov. 1996.

[36] H. Soeleman, K. Roy, and B. C. Paul, "Robust ultra-low power subthreshold DTMOS logic," in *Proc. IEEE Int. Symp. Low-Power Electron. Des.*,2000, pp. 25–30.

[37] C. Zhang, A. Srivastava, and P. K. Ajmera, “Low voltage CMOS Schmitt trigger circuits,” *Electron. Lett.*, vol. 39, no. 24, pp. 1696–1698, Nov. 2003.

[38] A. Richelli, “EMI susceptibility of DTMOS opamps,” *Electron. Lett.*, vol. 49, no. 2, pp. 98-99, Jan. 2013.

[39] A. Richelli, “Increasing EMI immunity in novel low-voltage CMOS opamps,” *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 4, pp. 947–950, Aug. 2012.

[40] S. Sbaraini, A. Richelli, and Z. M. Kovacs-Vajna, “EMI susceptibility in bulk-drivenMiller opamp,” *Electron. Lett.*, vol. 46, no. 16, pp. 1111–1113 ,Aug. 2010.

[41] S. F. Al-Sarawi, “Low power Schmitt trigger circuit,” *Electron. Lett.*, vol. 38, no. 18, pp. 1009–1010, Aug. 2002.

[42] J. P. Kulkarni and K. Roy, “Ultra low-voltage process-variation-tolerant schmitt-trigger-based SRAM design,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 2, pp. 319–332, Feb. 2012.

[43] N. Lotze andY.Manoli, “A 62mV0.13 um CMOS standard-cell-based design technique using Schmitt-trigger logic,” *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, Jan. 2012.

[44] K. Kim and S. Kim, “Design of Schmitt Trigger Logic Gates Using DTMOS for Enhanced Electromagnetic Immunity of Subthreshold Circuits,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 5, pp. 963–972, 2015.