M. Tech (VLSI Design & Embedded Systems) ROSHAN DEEP RANJAN 2018

FGMOS based Instrumentation Amplifier for Healthcare Applications

A Dissertation

submitted in partial fulfillment of the requirements
for the award of the degree
of

Master of Technology
in
VLSI Design &Embedded Systems

Submitted by:

ROSHAN DEEP RANJAN

2K16/VLS/19

under the supervision of

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Bawana Road, Delhi-110042

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CANDIDATE'S DECLARATION

I ROSHAN DEEP RANJAN, Roll No. 2K16/VLS/19 student of M.Tech (VLSI & Embedded System), hereby declare that the project Dissertation titled "FGMOS based Instrumentation Amplifier for Healthcare Applications" which is being submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology in VLSI Design & Embedded Systems, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: New Delhi

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CERTIFICATE

I hereby certify that the Project Dissertation titled "FGMOS based Instrumentation Amplifier for Healthcare Applications" which is being submitted by ROSHAN DEEP RANJAN, Roll No 2K16/VLS/19 Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge, this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This thesis presents a new FGMOS based instrumentation amplifier for bio-medical applications. Instrumentation amplifier is an essential block for most of the bio-medical applications as it extracts out weak potential signals that may lie between microvolt to millivolt from human body. To extract weak potential signal, an instrumentation amplifier is needed to have very high common mode rejection ratio (CMRR) so that it can minimise the effect of common mode noise and hence desired signal can be extracted out. An instrumentation amplifier with high CMRR, high gain and low power dissipation is essentially required. To operate circuit on low voltage, FGMOS is used. FGMOS is a multi-input floating gate MOSFET used to reduce threshold voltage and hence operated on low supply voltage which results in lower power dissipation. Here, FGMOS is used to simulate two stage operational amplifier and hence, by using operational amplifier, instrumentation amplifier is drawn. The main purpose of using FGMOS in the circuit is its smaller threshold voltage compared to the normal MOSFET and having threshold voltage tuning ability. Threshold voltage can be changed by changing capacitance ratio at the gate terminal. Because lower threshold voltage is required for the circuit operation, it consumes low power and is hence suitable for battery powered portable devices. The two stage operational amplifier is designed in virtuoso 90nm technology and operated on 1.8V supply. Also, the two stage operational amplifier based on FGMOS is operated on 1.35V (the minimum voltage requirement of FGMOS based circuit so that all the MOSFET remains in saturation region). Technological parameters table of two stage operational amplifiers are charted out using FGMOS and with conventional MOS.

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LIST OF ABBREVIATIONS

Abbreviation	Full form
AHDL	Analog Hardware Duscription Language
BW	Bandwidth
Cox	Oxide Capacitance
CMOS	Complementary Metal Oxide Semiconductor
DT	Direct Tunneling
EPROM	Erasable Programmable Read Only Memory
ECB	Electron Conduction band
EVB	Electron Valence band
FGMOS	Floating Gate Metal Oxide Semiconductor
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PM	Phase Margin
SiO2	Silicon Oxide
tox	Silicon Oxide thickness
Vth	Threshold Voltage
V_{THFG}	Floating gate Threshold Voltage
HVB	Hole Valence Band
UGB	Unity Gain Bandwidth
SR	Slew Rate
ICMR	Input Common Mode Range
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
IA	Instrumentation Amplifier
Rout	Output Resistance
Rin	Input Resistance
DC	Direct Current
Op amp	Operational Amplifier

CHAPTER-1

INTRODUCTION

1.1 Motivation :

The instrumentation amplifier is one of the most important block in signal acquisition system. To extract weak potential signal, highly efficient instrumentation amplifier is required. Due to growing demand of portable battery powered devices, low power consumption is essentially required. The performance of an instrumentation amplifier depends upon its technological parameters i.e., CMRR, gain, noise, power dissipation etc. Different topologies are available in the literature to increase CMRR, gain etc. and also different topologies are available to reduce power dissipation that directly depends on supply voltage. The growing demands of low power portable devices makes the designer to investigate and present new low power circuits. Due to above requirement, in this thesis FGMOS is used due to which supply voltage requirement decreases and hence power dissipation.

The need of high performance systems from the last decade had grown rapidly. That's why the transisitor density has beenincreasing subsequently which also demands an expensive cooling &packaging technologies which give rise to some drawbacks. The voltages are scaleddownto minimize the effect of drawbacks which also affects current driving capability.

Due to smallerthreshold voltage (V_{TH}) because of scaling,results inexponential rise of subthreshold leakage current and causesleakage (static) power dissipation(P_{Static}). Static power dissipation is now dominating and become a major concern indeep submicron technologieswhich results in inferior battery life.

[1-2] discusses about leakage power dissipation forbetterbattery life,that also requires advanced design techniques.$P_{Static}$is predominantly dominated byleakage current components flowing in the transistor or CMOS circuits during idle or standby mode. It is anticipated and described in [2] that theleakage power (P_{Static}) could rise by 32 times per device by 2020.

The four main roots of leakage currentin a CMOS transistor are:

i) Reverse-biased PN-junction leakage current

ii) Gate induced drain leakagecurrent

iii) Gate direct-tunnelling leakage current

iv) Subthreshold(weak inversion) leakage current (I_{SUB}).

The subthreshold leakage current(I_{SUB}) mainly doinatesamong all the leakage currentsources and has become extremely challenging research in current and for future silicon technologies. The gate direct-tunneling leakage current is dominate in FGMOS in sub-micron technologies and hence degrades the circuit performance. From last two decades, analog designers starts using FGMOS based circuit in computational design due to the features of multi-input FGMOS and threshold voltage programmability.

In the structure of FGMOS where there is no path for DC grounding, a modified simulation model is used in order to get correct result.

1.2 History of Operational Amplifier

Operational amplifier is very important block in analog and mixed signal circuits. It plays vital role in analog circuits as because with the help of this, one can perform most of the mathematical operations like addition, subtractions, logrithms, integration, differentiation etc. John R. Ragazzinidesigned it in 1947 and shows a unique kind of amplifier by selecting external components appropriately. The first& early applications of operatioanal amplifier was in analog computer [23].

1.3 Op amp Basics

Basically op amp is a voltage amplifier and hence having very high input resistance and extremely low output resistance.The op amp has very high open loop gain and hence when

used in negative feedback configuration, overall transfer function becomes independent of open loop gain and this property is very useful and hence used in most of the analog circuits. op amp in open loop configuration used as comparator, in positive feedback used as a wave generater circuit and in negative feedback used as a amplifier along with different mathematical operations and filtering.The essential requirement of an op ampis that it must have very high open loop gain to implement negative feedback configuration. Due to the frequent use of op amp is IC, two stage op amp technique need to be simple and efficient. In an op amp, the differential signal is applied and whose output is amplified versiondifferential input. The op amp is a basic differential amplifier having input stage and the output stages. The output stage of op amp is a single ended & hence,op amp is a differential to single ended circuit.As to get high swing at the output, a buffer stage is used since op amp has low output impedance. Compensation circuitry is used to make close loop op amp stable.

The block diagram of basic closed loop op amp shown in figure (1.1). The input stage is called differential amplifier. As its name suggests it processes the difference between the two input signals.It helps to remove common mode signal applied. As because most of the common mode signals are filtered out therefore, noise as well as bias voltage are also negated out. Though differential amplifier filtered out most of the common mode signal, still some common mode signal left out at the output of differential amplifier [23].

The output of differential amplifier is given by:

$$V_{out} = A_d(Vin^+ - Vin^-) + A_C((Vin^+ - Vin^-)/2) \quad (2.1)$$

Ideally, $A_C = 0$

And hence,

$$V_{out} = A_d(Vin^+ - Vin^-) \quad (2.2)$$

Where, A_C is the Common mode gain due to common mode signal and A_d is the differential mode gain of the amplifier due to differential input.

Differential amplifier helps to minimize common mode signal and left out small common mode voltage which is good and can be handeled comfortably.

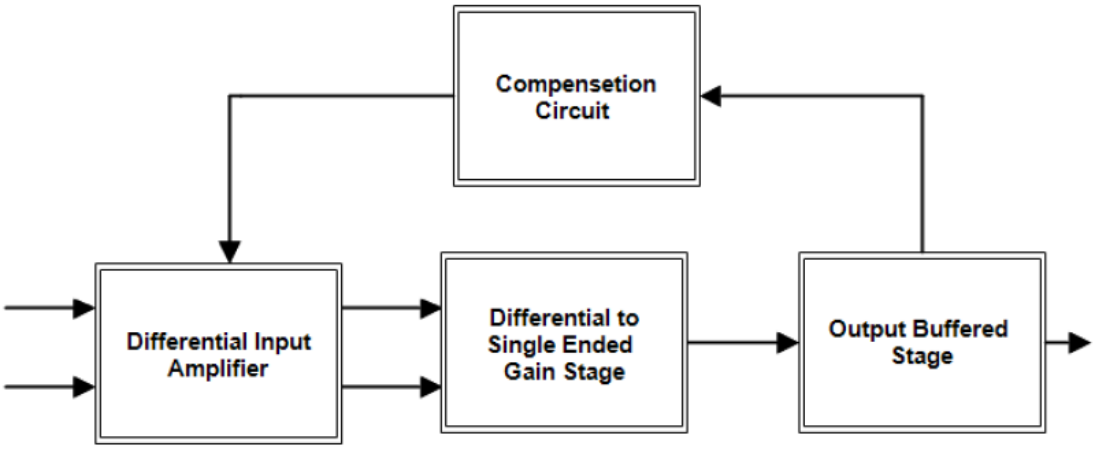

Figure 1.1 – Basic block diagram of op amp.

The CMRR of a differential amplifer specifies the common mode rejection ablility of an amplifier. And ideally it should be infinite. Mathematically, CMRR is given by:

$$\text{CMRR}=\frac{Ad}{Ac} \tag{2.3}$$

Single ended output differential amplifer is used in CMOS technology [24]. Also, from figure 1.1, it can be seen that differential to single ended gain stage is used in cascade with differential amplifier as because single ended output is used in CMOS technology. A output buffer stage is used in the output stage to get voltage output with high swing. A common source amplifier is used in the output stage as a buffer. A compensation circuit is used in the feedback to get improved performance, it improves phase margin.

1.4 Different Parameters of Operational Amplifier

Anop amp is characterized by its technological parameters and its parameters are as follows:

DC Gain: It signifies the open loop gain of the Operatioal amplifier. The ideal open loop DC gain of an Op-amp is infinite, practically it lies in between 60 dB to 100 dB.

ICMR: It is the range of common mode input voltage at which all the transistors remains in saturation & results in constant gain.

CMRR: It is defined as the ratio of differential mode gain to the common mode gain of an amplifier. Ideally, an op amp should have very high CMRR value & it would be infinite, practically CMRR should be more than 60 dB. CMRR is one of the important parameter of the op amp for biomedical system.

PSRR: It is defined as the product of ratio of the change in supply to change in output voltage of the amplifier due to the change in the power supply and open loop gain of the op amp. It also indicates how efficiently an op amp maintaining to the deviation of power

supply (both positive supply & negative supply which also might be considered as ground). Less variation at the output of an op amp corresponding to the variation of power supply results in higher PSRR. An op amp is need to have very high PSRR & practically it shouldbe greater than 60 dB.

Slew Rate: It is defined as the maximum rate of change of output voltage with respect to time. It is expressed in terms of V/us. A good op amp should have high slew rate. It determines by the charging and discharging of output capacitor by current available. Slew rate is completely depends on the current sourcing or sinking capability of the input stage rather than the output.

Settling time: It is the minimum time taken by the system to reach the steady state. For a typical op amp this value is less than 1us.

Phase Margin: It is defined as the excess of phase required to make the system marginally stable at the unit gain frequency. It is a measure of stability for close loop system.

$$PM = 180 + \phi \tag{2.4}$$

ϕ = Phase of system when gain is 0 dB.

Practically for a well designed op amp this value is around 60 degree.

For a becoming a system stable the phase margin and gain margin both are need to be positive. However, the consideration of a phase margin is very vital because it affects the transient response such as the settling time, slew rate, rise time, fall time and overshoot.

Input offset voltage: It defined as the voltage that must be applied between the two input terminals of an op amp to null or zero the output voltage.

1.5 Ideal and Practical Values of Op Amp Parameters

Table 1 shows the comparison of different Practical and Ideal technological parameters of an operational amplifier. Getting ideal values of parameters for an op amp is very tough.

Table 1: Comparison between Ideal and Practical parameters of op amp

IDEALLY	PRACTICALLY
R_{IN} = infinite	R_{IN} is very high (in terms of MΩ)
R_{OUT}=zero	R_{OUT} is a low value (in terms of KΩ)
DC GAIN = infinite	DC GAIN ≥ 60dB
BANDWIDTH =infinite	BANDWITH is very high value (in terms of MHz)
CMRR = infinite	CMRR ≥ 60dB
PSRR = infinite	PSRR ≥ 60dB
OFFSET = zero	OFFSET ≠ zero (in order of millivolts)
SLEW RATE = infinite	SLEW RATE ≥ 5 V/us

1.6 Different Parameter Test Circuit

To find different technological parameter of an op amp, different test circuits have been in this section. Schematic configuration are also present in this section.

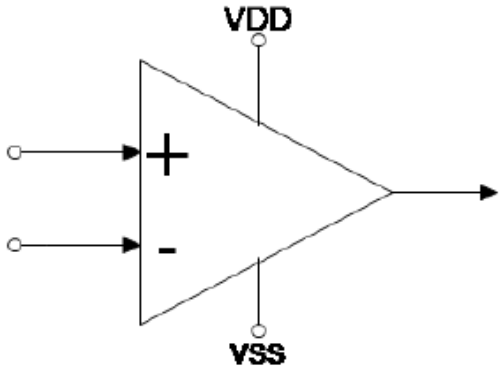

Figure 1.2- Symbol of op amp [23].

The figure 1.2 is a symbolic representation of a three terminal op amp. The left side two terminal are used to apply differential input signal and right side terminal provides amplified output. The input terminal signed as negative is known as inverting terminal & the positive indicating input terminal is known as non-inverting terminal.The op amp has a single ended output. The supply voltages are shown by the pin VDD and VSS. The op amp

generally uses dual power supply and hence, positive power supply is shown by V_{DD} & negative power supply is shown by VSS, in some cases VSS terminal is replaced by ground.

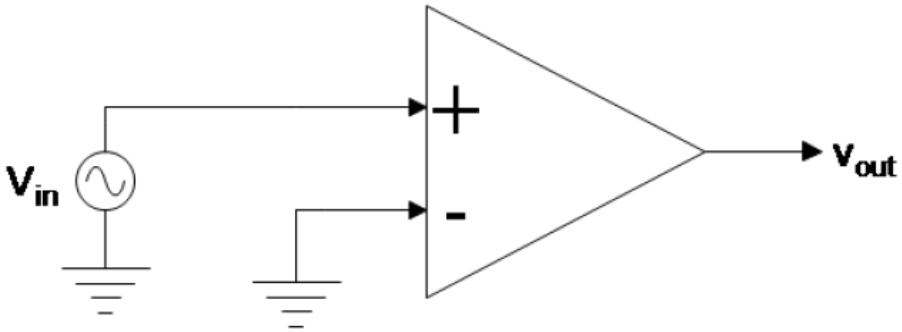

Figure 1.3- Circuit for measuring open loop gain [25].

From figure 1.3, we can find the open loop gain of operational amplifier. From the above figure 1.3, we can see that an AC signal V_{in} is applied on its non-inverting terminal & inverting terminal is AC grounded with op amp having supply voltages of VDD and VSS and AC analysis is carried out. The ratio of output to input will the open loop gain or DC gain of an op amp. Same configuration is used to findthe UGB, phase margin, 3dB bandwidth of etc.

Mathrmatically,

DC Gain $=\frac{Vo}{Vin}$ (2.5)

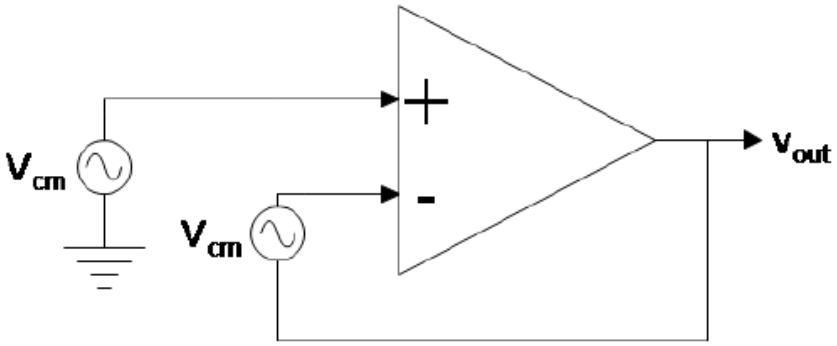

Figure 1.4- Test circuit for CMRR [25].

Figure 1.4 is used to find CMRR of an op amp. By finding differential mode gain and common mode gain, we can find CMRR. The ratio of differential mode gain to the common mode gain will give CMRR. The configuration shown above having two identical AC signal source Vcmand are tied in series with the inputs. The CMRR from above figure is given by:

$$\frac{Vout}{Vcm} = \frac{1}{CMRR} \tag{2.6}$$

Also, from equation (2.3), we can get CMRR.

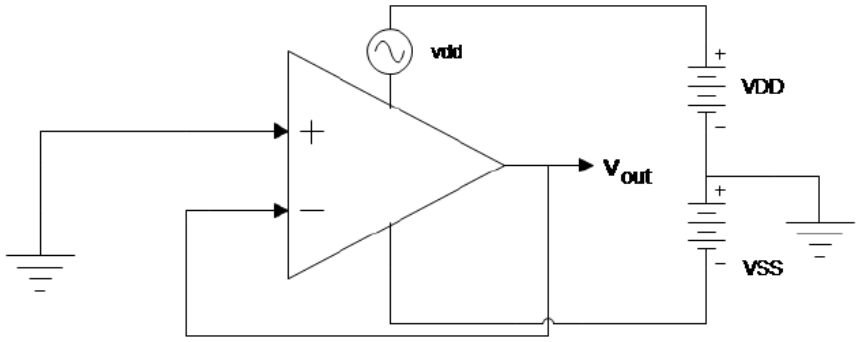

Figure 1.5- Test circuit for PSRR [25].

The figure 1.5 shown above is a configuration used to find PSRR of an op amp. To measure PSRR, an AC signal vdd is connected in series with supply VDD. An AC analysis gives out the PSRR of an op amp. From equation (2.7) we can calculate PSRR [25].

$$\text{PSRR}=\frac{Av(Vdd=0)}{Add(Vin=0)} \tag{2.7}$$

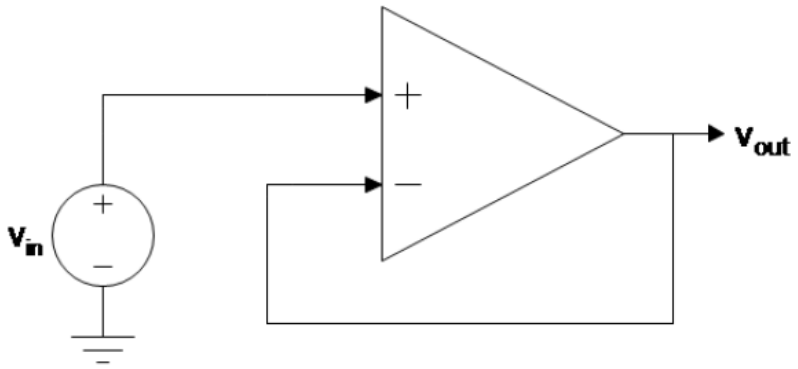

Figure 1.6- Test circuit for slew rate [25].

Figure 1.6 is used to find slew rate & settling time of an op amp. It is a basic unit gain buffer amplifier having negative feedback configuration. By applying a step input at non inverting terminal, we can find slew rate of the op amp. After a transient time, we can find the settling time, the time at which ringing settles down. Slew rate is determined by the slope of the output signal during rise or fall time.

1.7 Conventional CMOS Operational Amplifier

Figure 1.7 shows a conventional two stage operational amplifier based on CMOS technology. Transistors M1-M5 & M8 constitutes first stage circuit and the second stage of the circuit is consists of transistor M6-M7. The Miller compensating capacitor $C_C$and a

nulling resister is used between the output and input of the second stage. All transistors used in the circuit are biased in saturation region.

In first stage, the differential signal is applied into the transistor M1 & M2 from the pin V_{in}^- and V_{in}^+ the gate terminal respectively. M1 and M2 are two NMOS transistorwhich is used to drive the circuit and converts the differential voltage to differential current, these differential currents are further processed byPMOScurrent mirroredload transistor M3 and M4. The transistor M5 and M8 forms a current mirror and are used to provide reference current to the differential stage. The differential stage output is a single ended and it providesconstant gain with difference of the input signals.The single ended output of the first stage is then applied to the gate of the M6. Transistor M6 &M7 forms a second stage which is a common source configuration and offers high gain. The output of the second stage is taken from the drain terminal of the M6 [25].

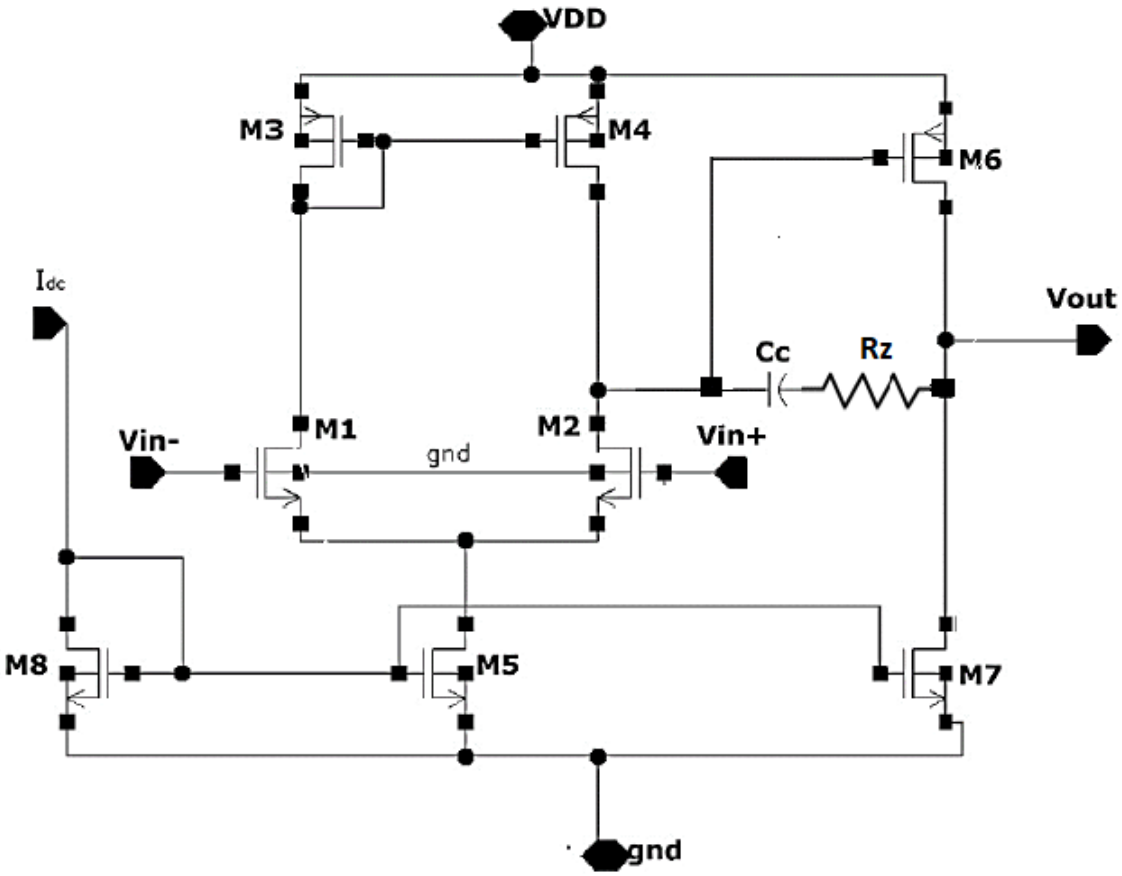

Figure 1.7- Conventional two stage op amp [25].

The design relationships for the two stage op amp are from [25] is given by:

The first stage DC gain is given by:

$$A_1 = \frac{-gm1}{gds2+gds4} \tag{2.8}$$

The second stage DC gain is given by:

$$A_2 = \frac{-gm6}{gds6+gds7} \quad (2.9)$$

The overall gain of an operational amplifier from [25] is given by:

$$A_V = A_1.A_2 \quad (2.10)$$

Therefore,

$$A_V = \frac{gm1gm6}{(gds2+gds4)(gds6+gds7)} \quad (2.11)$$

Slew Rate of two stage op amp is given by from [25]:

$$SR = \frac{I5}{Cc} \quad (2.12)$$

Where, I_5 the current flowing through of transistor M5 & is the bias current of the first stage.

The gain bandwidth product of two stage op amp is given by from [25] is:

$$GB = \frac{gm1}{Cc} \quad (2.13)$$

Positive ICMR $V_{in(max)} = V_{DD} - \sqrt{(I_5/\beta_3)} - |V_{T03}|_{(max)} + V_{T1(min)}$ (2.14)

Negative ICMR $V_{in(min)} = V_{SS} + \sqrt{(I_5/\beta_1)} + V_{T1(max)} + V_{DS5(sat)}$ (2.15)

For 60° phase margin, it is required that $gm_6 = 2.2gm_2(CL/Cc)$ provided all other roots are greater than or equal to 10GB [25].

1.8 Simulation Results of Conventional Op Amp

Figure 1.7 shows a conventional two stage op amp based on CMOS technology and is designed in gpdk 90 nm technology having supply voltage of 1.8V along with a bias current IDC of 15 uA. This op amp is simulated in Cadence circuit simulator.

All the experimental work and results are elaborated in chapter 3. Also, all the conclusion drawn from circuits are explained in chapter 4.

1.9 Organisation of Thesis:

This thesis presents a comparison study between FGMOS based two stage operational amplifier and conventional two stage operational amplifier. Also technological parameters table is charted out. The thesis emphasized on design of instrumentation amplifier based on Floating-Gate MOS two stage operational amplifier. Chapter 2 deals with literature survey and the experimental work i.e., conventional operational amplifier is simulated in chapter 3 along with FGMOS based two stage operational amplifier and instrumentation amplifier. Problem associated with sub-micron technologies in FGMOS and its possible solution is discussed in chapter 4. Also chapter 4, presents result and conclusion. Future scope is reported in chapter 5.

CHAPTER-2

LITERATURE SURVEY

2.1 Introduction

In this chapter, the floating gate transistor is dicussed. FGMOS characteristics and the problem associated with submicron technology is also discussed like, the gate leakage current that cannot be tolerated and has a significantimpact on the transistor's performance. From last one decade huge amount of research is going on in analog FGMOS based circuit.Researchers are doing enormous effort to develop circuits based on FGMOS and minimizing the leakage current in sub-micron technology.This segment comprises of the various associated research themes.

D. Kahng& S. M. Sze[3], introduced the concept of "floating gate MOS" in 1967. They proposed the circuit and simulation results which shows that floating gate can store charge for long duration and hence suitable as a memory element.

L. Richard Carley [4], describes in 1989 about electrically programmable FGMOS analog memory circuit for both positive as well as negative voltage changes & suitable for fabrication in a standard CMOS IC.

T. Shibata and T. Ohmi [5], presents a new type of MOS device based on FGMOS in 1992 and called it as "neuron MOSFET" because it perform fuctions more intelligently than conventional MOS. This transistor calculates the weighted sum of all the input voltage signal and controls the ON and OFF state of transistor based on the weighted sum result.

Y. Berg & T.S. Lande [6], described novel technique for threshold programmability using FGMOS for low power operation in 1997. The threshold voltage shifting was possible with the cost of extra polysilicon layer and the programmability in FGMOS transistor was possible by UV light activation and this gives rise to a new device called FGUVMOS transistor and is suitable for low power supply.

Y. Berg & T.S. Lande [7], presented a paper in 1999 showing area efficient threshold tuning technique for FGMOS circuits. The FGMOS is programmed by supply voltage rails & UV light, and hence additional programming circuitary is not required.

Antonio Lopez-Martin, J. Ramirez-Angulo [8], In 1999, presented a noval DAC converter the ability of the multiple input FGMOS transistor. A 6-bit DAC conversion is designed by the authors using multiple input FGMOS technique.

K. Nandhasri and J. Ngarmnil [9], in 2001, presented analog & digital comparator based on the threshold voltage characteristics of FGMOS transistor to produce a hysteresis that results in analog voltage comparator and analog comparator then used to develop digital comparator.

E. Rodríguez-Villegas, A. Rueda, and A. Yúfera [10], presented in 2001, a FGMOS transistor based translinear circuits for low voltage and low power. The technique used in [10] allows supply voltage reduction in strong inversion mode and hence suitable for low power applications.

B. A. Minch [11], presented a folded FGMOS differential pair in 2000, which is capable of providing both rail to rail input common mode range & output voltage swing with low supply voltage.

K. Moolpho. J. Ngarmnil and K. Nandhasri [12], presented wide swing FGMOS based current amplifier operated on low voltage. In [12] authors used a class AB structure which is designed with CMOS inverter and an analog inverter based on FGMOS transistor.

S. Sharma, S.S. Rajput, L.K. Magotra, and S.S. Jamuar [13], presented FGMOS based current mirror and its low power applications in 2002. It has wide operating current range and also has very high bandwidth. It also offers high output impedance, more than one megaohm for higher bias current and circuit is suitable for both N-type & P-type current mirror.

Rodriguez-Villegas and Esther [14], presented a paper in 2003, discussed about charge storage problem in FGMOS and possible solution to get rid of accumulated charge.

D. Yates, E. López-Morillo, R. G. Carvajal, J. Ramirez-Angulo and E. Rodriguez-Villegas [15] had presented a low power front end circuit for werarable biomedical systems using quasi-floating gate MOS in 2007 which rejects low frequency noise and provides higher SNR.

Patricia Mejía-Chávez, Juan C. Sánchez-García and José Velázquez-López [16], presented a differential difference amplifier based on FGMOS for ECG signal acquisition. Due to the use of FGMOS, DC offset reduced significantly.

N. G. Lopez-Martinez, A. S. Medina-Vazquez and M. A. Gurrola-Navarro [17,] presented multiple input transconductance amplifier in common source configuration based on FGMOS in 2015.

Guoqiang Hang and Guoquan Zhu [18], in 2015 presented a Schmitt trigger with adjustable hysteresis based on FGMOS threshold inverter.

Sherif M. Sharroush [19], presented a novel variable gain amplifier using FGMOS suitable for radio frequency receivers where variable gain is needed.

P. Chandrakasan,[20] introduced “Low-power CMOS digital design,” in 1992.The work was carried out by keeping the things in mind thatportable and battery-operated applications were emerging rapidly, the techniques allowslowers power consumption in CMOS digital circuits.

Gu, R.X and M.I Elmasry[21], presented a paper in 1996 wherethey evaluated stand-by as well as switching power dissipation in deep submicron technologies and a logical representation was elaborated.

A. Keshavarzi, K. Roy and C. F. Hawkins [22], presented a paper in 1997 in which they investigated various sources of leakage power in MOS device and their behavior with scaling.

2.2 FGMOS History

In 1967, FGMOS had been introduced by Sze et.al., [3] &has been used in memories widely like, EPROMs, EEPROMs, and flash because of their charge storing capabilities for long time. These charges can be controlled by:

(a) Exposing the chip on ultra violet (UV) light for finite duration of time.

(b) For tunnelling electrons through the oxide, it is required to add a high potential voltage across gate capacitor.

(c) By using hot electron injection [26] to add electrons.

FGMOS still used in digital memories but from last couple of decades, it extended to analog design [27] also. As because of FGMOS threshold voltagetenability, it is being used in analog design environment to design analog circuits that can operate at smaller supply voltage than that of the standard MOS (for same process). Also, due to multiple input feature of FGMOS transistor, the designers are havingadvantage of designing different analog applications like, multipliers, integrators, amplifiers [28-30] etc. due to sum operation at the gate.

2.3 Device Characteristics

A Floating Gate MOS transistor is similar to standard MOS transistor, but it does not have any resistive connections to its gate & also numbers of inputs that are connected above the floating gate. The multiple inputs of floating gate are only capacitively connected. Double poly structure is used in the fabrication of FGMOS in which, the first poly is the floating gate & control gate is on second poly where rest of the inputs are deposited as shown in figures 2.1 and 2.2.As there is no DC path to ground at the gate of FGMOS transistor,and having multiple inputs which are capacitivelyconnected,has changes the DC characteristics significantly from the standard MOSFET.

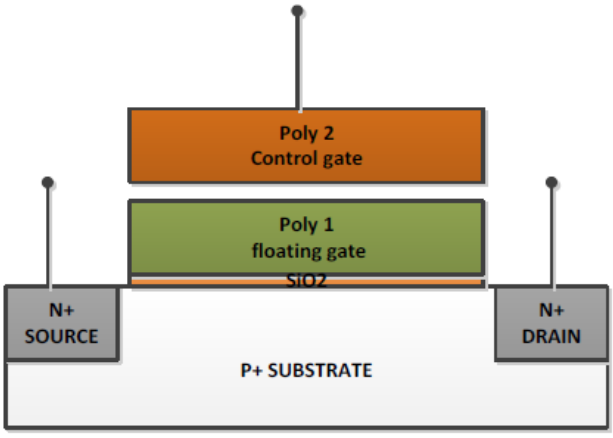

Figure 2.1- N-type FGMOS using double poly structure.

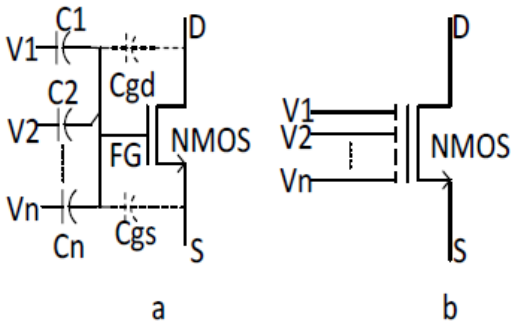

Figure 2.2- n-inputs FG MOSFET: a- equivalent circuit, b- the symbolic representation.

As because gate is electrically isolated from body due to the basic nature of FGMOS, there is no DC path to ground and hence, charge gets stored in the FG and this property of FGMOS is directly affects the drain current as well as the threshold voltage. This propertyof FGMOS helps in analog memories like Field Programmable Analogue Array (FPAA) [31].

The floating gate voltage is given by the weighted sum of all the capacitivelycoupled inputs voltages connected at the gate. By taking an assumption that there is no leakage current [32] flowing through gate terminal due to strong SiO_2 insulator at the gate, the FG voltage is given by:

$$V_{FG}= \sum_{i=1}^{N} \frac{CiVi}{CT} + \frac{QFG}{CT} \quad (3.1)$$

$$C_T= \sum_{i=1}^{N} Ci + Cgs + Cgd \quad (3.2)$$

By assumuing that, zero charge is accumulated at the gate, equation (3.1) can be re-written as:

$$V_{FG}= \frac{C1V1}{CT} + \frac{C2V2}{CT} + \frac{C3V3}{CT} + \text{-------} + \frac{CnVn}{CT} \quad (3.3)$$

From Equation (3.3), we can conclude that, FGMOS reduces complexity in certain circuitsthat require adders &also it minimizes the power requirement & noise in such circuits [33] as shown in below figure 2.3.

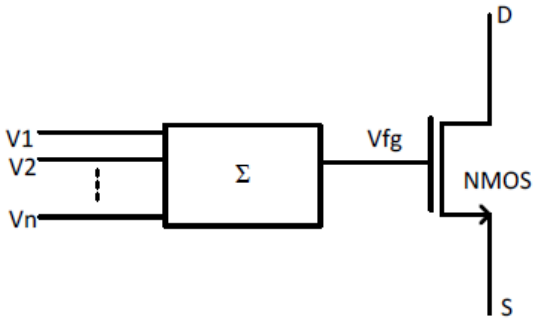

Figure 2.3-Equivalent circuit for floating gate transistor [33].

For FGMOS in saturation region, the current equations can be written as:

$$I_D = \mu_N C_{OX} \frac{W}{2L}(V_{FG}-V_T)^2 \quad (3.4)$$

By assume zero Q_{FG} and replacing V_{FG}in Equation (3.1), will result in

$$I_D = \mu_N C_{OX} \frac{W}{2L}(\sum_{i=1}^{N} \frac{CiVi}{CT} - V_T)^2 (3.5)$$

$$I_D = \mu_N C_{OX} \frac{W}{2L}\beta(\sum_{i=1}^{N} Vi - (\frac{CT}{Ci})V_T)^2 \quad (3.6)$$

$$I_D = \mu_N C_{OX} \frac{W}{2L}\beta\ (\sum_{i=1}^{N} Vi - V_{THFG})^2 \quad (3.7)$$

Where,

$\beta=\sum_{i=1}^{N}(\frac{Ci}{CT})^2$ and, $V_{THFG}= \sum_{i=1}^{N}(\frac{CT}{Ci})V_T$

From above equations, it can be seen that, drain current of FGMOS is a function of the capacitor ratio and it is the ratio of effective input voltage to the total capacitance at the gate.

Let's assume that V_1 is the effective input, then, the drain current can be written as :

$$I_D = \mu_N C_{OX} \frac{W}{2L}\beta(V_1 - (\frac{CTVT}{C1} - \frac{C2V2}{C1} - \frac{C3V3}{C1} - \text{-------} - \frac{CnVn}{C1}))^2 \quad (3.8)$$

In this case,

$$\beta= (\frac{C1}{CT})^2$$

$$V_{THFG}= (\frac{CTVT}{C1} - \frac{C2V2}{C1} - \frac{C3V3}{C1} - \text{-------} - \frac{CnVn}{C1}) \quad (3.9)$$

$$I_D = \mu_N C_{OX} \frac{W}{2L}\beta(V_1 - V_{THFG})^2 (3.10)$$

$$gm_i= \frac{Ci}{CT} \quad (3.11)$$

where, i= 1, 2, ------, N

Where, Ci are the input capacitors connected at the gate, C_{gs}&C_{gd} are the parasitic capacitors,Vi are input voltages, V_{FG} is the floating gate voltage,$V_{THFG}$is the threshold voltage of floating gate MOSFET&V_T is the threshold of standard MOS threshold voltage. L is the channel length, W is the channel width,μ_N is the mobility, $C_{OX}$is the oxide capacitance per unit area, N is the number of inputs voltages at the gate, Q_{FG}indicating charges trapped in floating gate during fabrication and, gm is the FGMOS transconductance.

From equation (3.10), we conclude that FGMOS behaves as a programmable threshold voltagedevice in which the effective threshold voltage of floating gate V_{THFG}can be reduced zero or minimum i.e., to negative value compared to standard MOS threshold as shown in figure (2.4).

Figure (2.5) indicating the tuning ability of FGMOS by taking two inputs into consideration. By sweeping one input voltage and keeping the other. By increasing the numbers of inputat the gate or the input capacitors ratio, V_{THFG} can be further reduced. This is the one of the important specificationof FGMOS that made this technique suitable for low power applications and also tunable circuit that used to compensate mismatches.

From equation (3.10) & (3.11), it can be seen that, the drain current I_D& the transconductance - gm of FGMOS is smaller than that of standard MOS transistor, as it can be seen from figure 2.4, due to the scalingwhich is a function of the coupling capacitors ratio forthe effective input. Theseare some demerits of floating gate transistor. However, analog designersovercomes them & they used this transistor in other circuits.

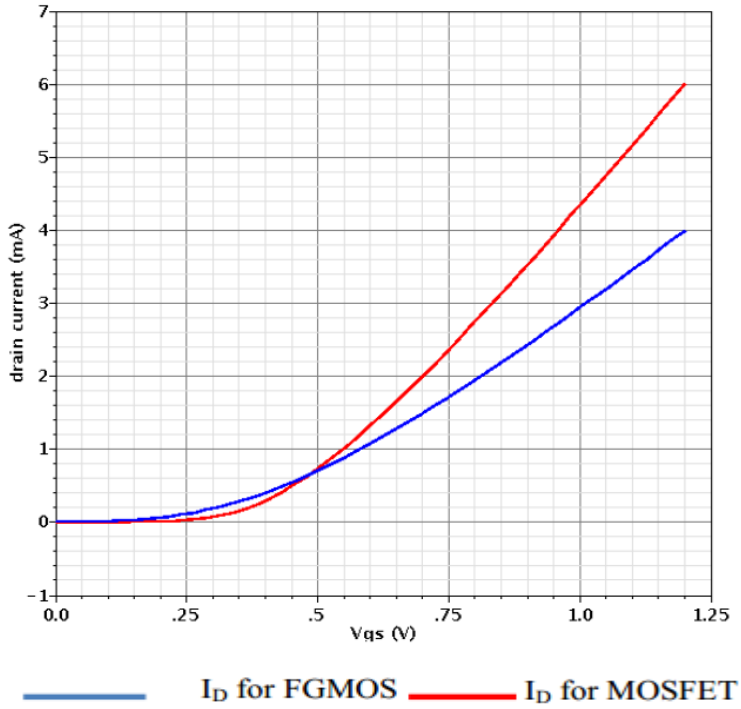

Figure 2.4- A comparison between standard MOS and FGMOS drain currents.

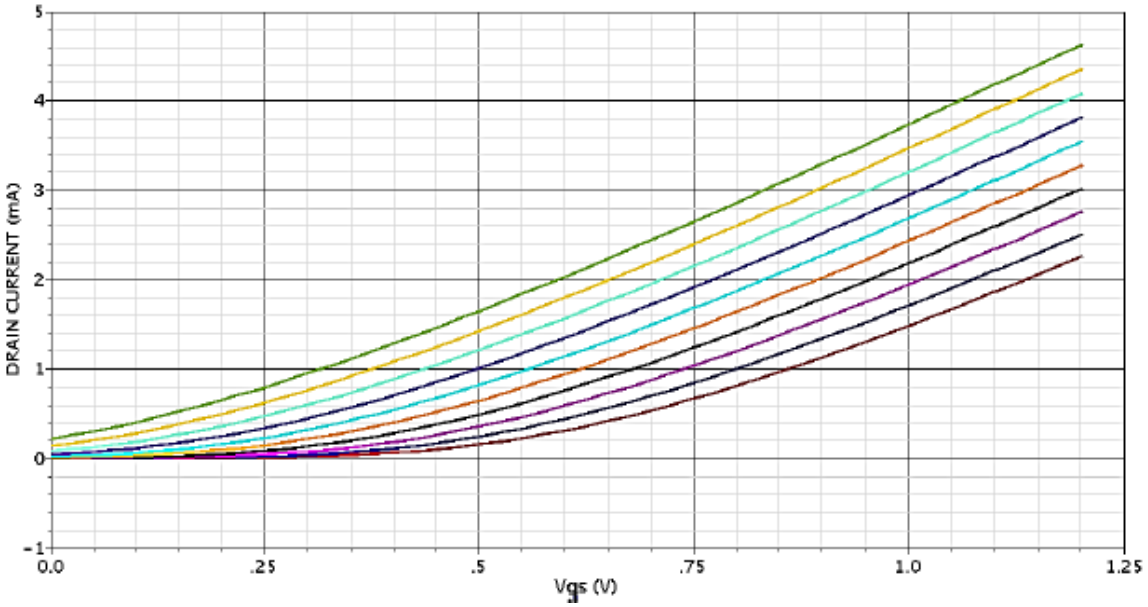

Figure 2.5- FGMOS threshold voltage programmability by sweeping one of the input voltages.

2.4 Charge Accumulation

In FGMOS, because of silicon is surrounded by gate oxide, the charge carries may be accumulated during the fabrication process and therefore, these charges affects the threshold voltage of FGMOS directly and it is indeterminate. Theaccumulated charges may result in change in fundamental operations of the circuits and hence, these charges need to be eliminated in order to work FGMOS properly.

To resolve this problem, different solutions have been reported in the literature like, as shown in [34], FGMOS is exposed to ultra voilet light to get rid of the accumulated charges at the gate. The problem associated with technology is that it is not compatible with CMOS technology since, in order to activate lighttransition in FGMOS, the passivation layer hasto be removed.

Another proposed solution as described in [35]is suggests a Fowler–Nordheimtunnelling (FN) current to remove the charges from the floating gate. As SiO_2 is an insulator that kept the electronsand hence, this electrons need high energy to cross through it, as oxide works as a barrier and therefore a high voltage applied in order to tunnel the trapped electrons through the barrier to the silicon below it. Asthe applied voltage is inversely proportional totheoxide thickness, a very high voltage is required, since the oxide thickness is very small.

A technique to get rid of trapped charges is reported in [14], this technique suggeststhat charges from the floating gateis eliminated byadding dummy contacts at the gate. This

technique is highly efficient and simple. Also, it does not requires any extra circuitry and hence, has been widely used in FGMOS analog circuits.

2.5 Challenges of Using FGMOS in Nanometer Technologies

Analog designers are facing problems when they use FGMOS in submicron technology. The direct tunneling gate current is a serious concern in FGMOS transistor thatoccurs in sub 100nm technologies where oxide thickness is very small and due to this the electrons and holes tunnel through it. This DT leakage current degrades thetransistor performance in CMOS & in FGMOS specifically. The other problem is due to the nature of FGMOS that, the need of a model it in order to carry out thesimulations in any industry simulator due to the convergence problem.

In the next sections previously simulated models for FGMOS as well as the gate leakage current will be discussed.

2.5.1 Gate Direct Tunneling in sub 100nm Technologies

From last two decades, the CMOS technology has been scaled down significantly to meet the industry demand. Scaling of CMOS technology has improved the performance by reducing thepower dissipation,small chip size, increased the speed etc., however, the scaling in transistor sizes also brings different challenges for a design engineer to predict the transistor performance.

Silicon oxide thickness has reduced to few nanometers due to continuous scaling in CMOS technology. Due to the small gate thickness oxide layer, direct tunneling (DT) current has become a growing issue foranalog designers. Tunneling of charge carriers (electronsand holes) from the gate through the oxide to the bulk and source / drain region respectively results in gate DT current.

Figure 2.6, showsa DT mechanism in NMOS transistor. Tunneling of carriers from three bands result in DT current in which, the first tunneling is due to the tunneling of electrons of the conductions band (ECB) in the gate. The second tunneling is due to electrons in the valence band (EVB) and the third is due to the tunneling of holes through thevalence band to the gate (HVB). Direct tunneling is NMOS devices is dominated by ECB and EVB whereas in PMOS is by HVB.

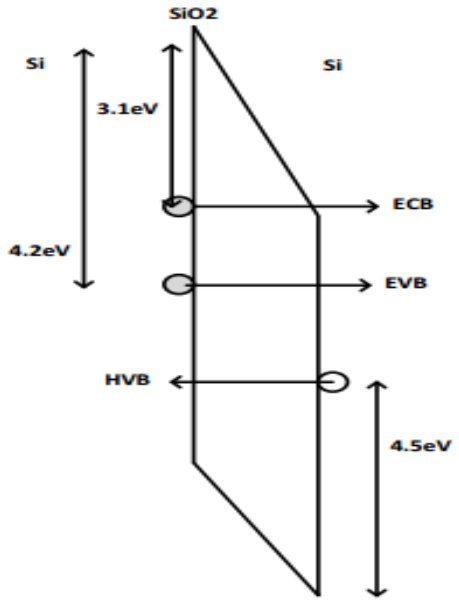

Figure 2.6- The mechanism of gate tunneling current in CMOS transistor.

TheDT gate current has three components,'Igb'the current between gate & substrate as shown in figure 2.7.also, the channel current 'Igc'. The channel current is further divided into two current components i.e., the current between the gate & the source 'Igcs' and the current between the gate & the drain 'Igcd' respectively. The total tunneling gate current thus can be written as:

$$I_G = I_{gcs} + I_{gcd} + I_{gs} + I_{gd} + I_{gb} \quad (3.12)$$

Where, Igs&Igd are the dominantfunction of gate source and gate drain terminals voltages respectively.

DT gate current for a NMOS device is one order of magnitude higher than the PMOS device because the holes in PMOS need high energy to cross the barrier than the electrons in NMOS for same value of oxide thickness and power supply [36].

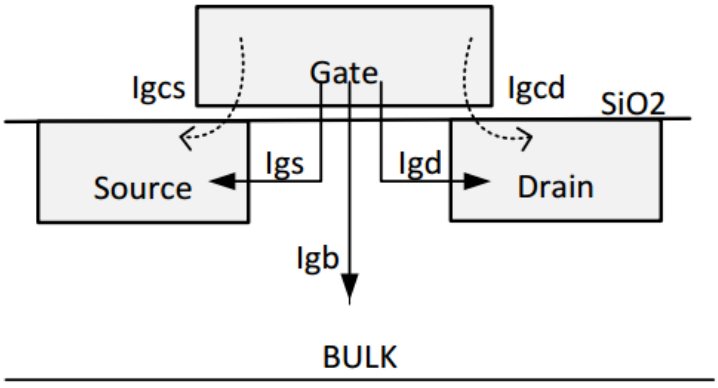

Figure 2.7- DT gate current components for NMOS [37].

2.5.2 Previous modeling of gate tunnelingcurrent in NMOS

Due to gate DT current, the circuit performance degrades. Also, static power dissipation increases due to it. Many papers in gate DT currenteffect on circuits have been reported along with simulation result [36, 38, 39].

In [36], it is described that, DT gate current increases exponentially as thickness oxide decreases, also when the gate voltage increase as because, DT gate current is an exponential function of thickness oxide as well as the potential across it.

$$I_{gs}=\frac{127.04\cdot Leff\cdot e^{(5.606\cdot Vgs-10.6\cdot tox\text{^}-2.5)}}{2} \quad (3.13)$$

$$I_{gd}=\frac{127.04\cdot Leff\cdot e^{(5.606\cdot Vgd-10.6\cdot tox\text{^}-2.5)}}{2} \quad (3.14)$$

An empirical gate leakage model is described in [36]. In themodel shown in figure 2.8,voltage dependent current sources(VCCS) is used to describethe gate to source (Igs) &gate to drain (Igd)currentsbetweengate to source& gate to drain.

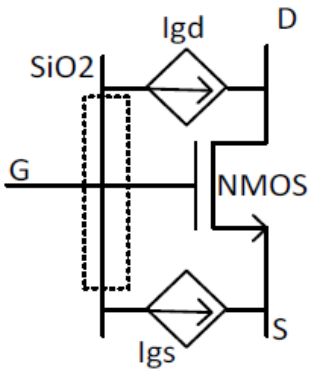

Figure 2.8- DT gate current micro model proposed in[36].

Figure 2.9 illustrates a model based on [38] for circuit simulation where three terminal transistor with the parasitic capacitors like Cgs,Cgd and Cgb are included along with the gate tunneling. Again, VCCS is used to describe the gate current as shown in below figure 2.9asIgs,Igd andIch.

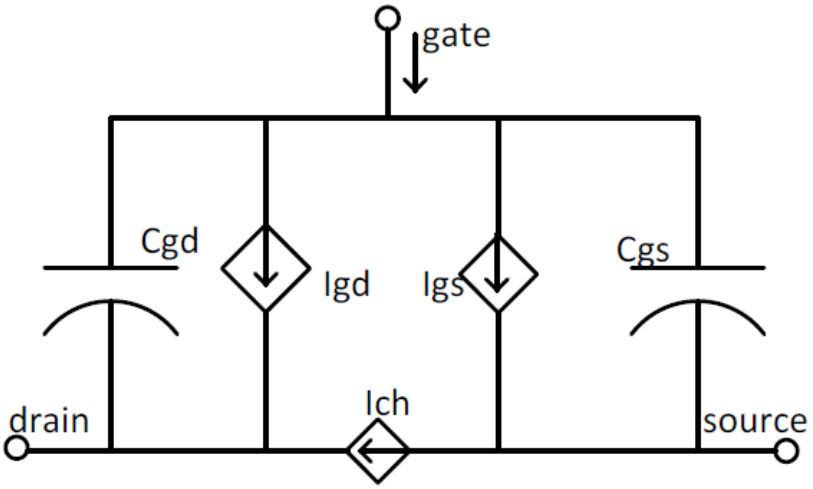

Figure 2.9- Micro model for gate tunneling for circuit simulation proposed in [38].

Figure 2.10 showing another model for the gate DT leakage current as reported in [39]. It also having voltage dependent current sources as shown in figure below and they are a function of terminal voltages. The channel current is partitioned into to Igs and Igd and it is represented using variable resistors.

$$I_{gc} = I_{gs} + I_{gd} \tag{3.15}$$

$$R_{cd} = \frac{Vcd}{Icd} \& R_{cs} = \frac{Vcs}{Ics} \tag{3.16}$$

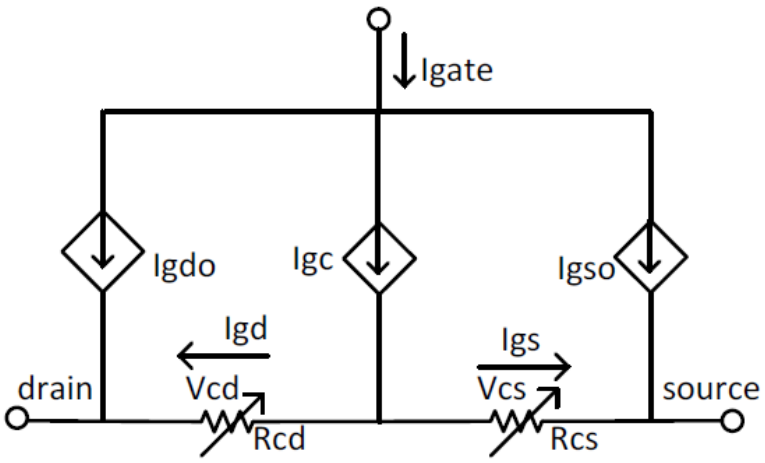

Figure 2.10- Gate DT model for circuit simulation suggested in [15].

2.6 FGMOS Simulation Models

In order the simulator to converge on a solution, simulator needs to have atleat one path to ground, also an initial conditions in each point of the circuit. As FGMOS transistor has no DC path to ground, a DC model is required to simulate it.

Some authors have presented a simulation model to solve the convergence problem. In [32], authors J. Ramirez-Anguloet. al., have presenteda simulation model in which FGMOS is suggested where a standard MOSFET is used with multiple inputs capacitively coupled to floating gate along with a large value resistor&dependant voltage source which is voltage controlled voltage source (VCVS),to provide a DC path to ground. The value of VCVS is determined by the ratio of coupling capacitors seen from the gatefor each inputs (Ci/CT) as shown in figure 2.11.

The model shown below in figure 2.11 has widely been used in simulations for simulating floating gate. The drawback of this circuit is that this circuit is unable to represent the movement of charge due to gate leakage.

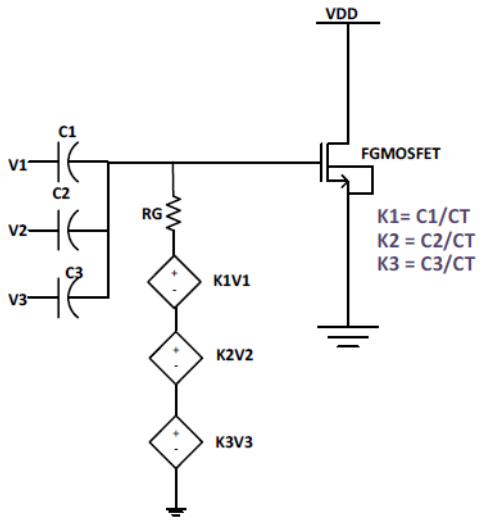

Figure 2.11- multiple inputs FGMOS simulation model proposed in [32].

Where RG is in Megaohms.

$$V_{FG}= \sum_{i=1}^{N} \frac{CiVi}{CT} + \frac{CgsVs}{CT} + \frac{CgdVD}{CT} + \frac{QFG}{CT} \quad (3.17)$$

$$C_T=\sum_{i=1}^{N} Ci + C_{gs} + C_{gd} \quad (3.18)$$

$$K_i=\sum_{i=1}^{N} \frac{Ci}{CT} \quad (3.19)$$

In [40], Liming Yin et. al., have present a model for simulating FGMOS by taking parasitics into consideration along with input coupling capacitors asinfigure 2.12. In this model, a resistor is connected in parallel with each of the input capacitosr in order to resolve the convergence problem. It is necessary to havethe RC product of each input pair branch equal.

Also, the input resistors must have very high resistance value in order not to have any effect onAC simulation. If any charge traps in the floatinggate, a voltage source is connected to the floating gate.

Where, $V_Q = Q / C_T$.

$$R_i=\frac{1}{KCi} \tag{3.20}$$

$$G_i=\frac{1}{Ri} \tag{3.21}$$

Where i=1, 2, 3 …. n and k is a constant quantity chosen to make R very large.

$$R_i\, C_i = R_{GD}\, C_{GD} = R_{GS}\, C_{GS} = R_{GB}\, C_{GB} \tag{3.22}$$

$$V_{fg}=\frac{CGBV0+CGsVs+CGdVd+\ C1V1+C2V2+---CnVn}{CT} \tag{3.23}$$

Where,Ri indicates the input resistors and Ci indicates the input capacitors, Vfgis floating gate voltage andV1, V2,----Vn are the control input voltages. V0 indicates the substrate voltage. Also, C_{GS}&$C_{GD}$are the parasitic capacitors and V_S& $V_D$are the source & drain voltages respectively.

This model also have the same drawback as the model shown in [32] by Ramírez-Angulo et. al. i.e., this model also incapable of accountingthe amount of charge movement through gate which results in gate leakage.

In [41],Ai Chen Lowet. al., also have presented a model for FGMOS using multiple input capacitors as shown in figure 2.13. In this model, there is no DC path to ground as well as there is no parasitic capacitors is assumed to have in the FGMOS transistor. Therefore an initial voltage has been connected to the input capacitors to resolve the convergence problem.Addition of a initial positive voltage to capacitor connected to floating gate through thenegative terminal signifies removal of charges from FG, while addition of a negative

initial voltage signfies to addition of charges to floating gate.

$$V_{fg}=\frac{C1}{C1+C2}V1 \quad (3.24)$$

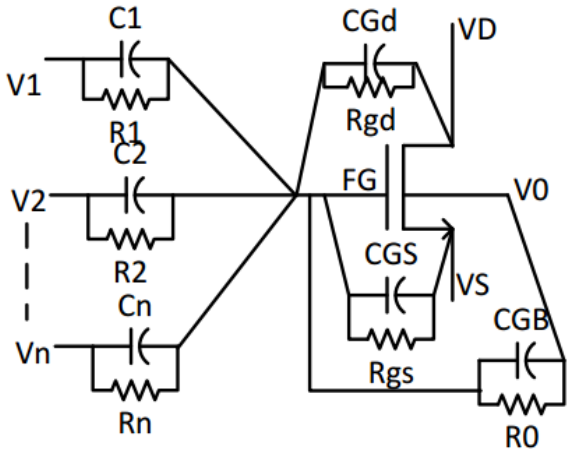

Figure 2.12- FGMOS simulation model in [40].

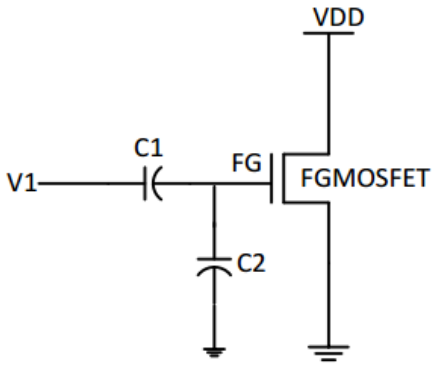

Figure 2.13- simulation model for FG transistor proposed in [41].

2.7Summary

It should be noted that, all the previous models discussed for simulating floating gate are used to model the functionality of floating gate transistor & hence, it solves the convergence problem in simulation.It should be also noted that, all the previous models did not includes gate current in there construction because, initially FGMOS transistors was fabricated using double poly technique which was having thick gate oxide i.e., thicknessis

more than 3nm and hence, gate DT current was negligible and hence has no much impact on FGMOS performance.

It is very crucial &important to model FGMOS transistor in submicron technologies using single poly layer where tox is less than 3nm.

CHAPTER-3

EXPERIENTAL WORK

3.1 Schematic of Conventional Op Amp Circuit

In this chapter, all the experimental work will be presented like conventional two stage op amp followed by two stage op amp using FGMOS and instrumentation amplifier based on FGMOS. This chapter will also present the limitation in Ramirez-Angelo's FGMOS model which is one of the most efficient &promising models available in the literature. A gate current impact on FGMOS behavior is also discussed in floating gate operational amplifier. Simulation results andcomparison are also included.

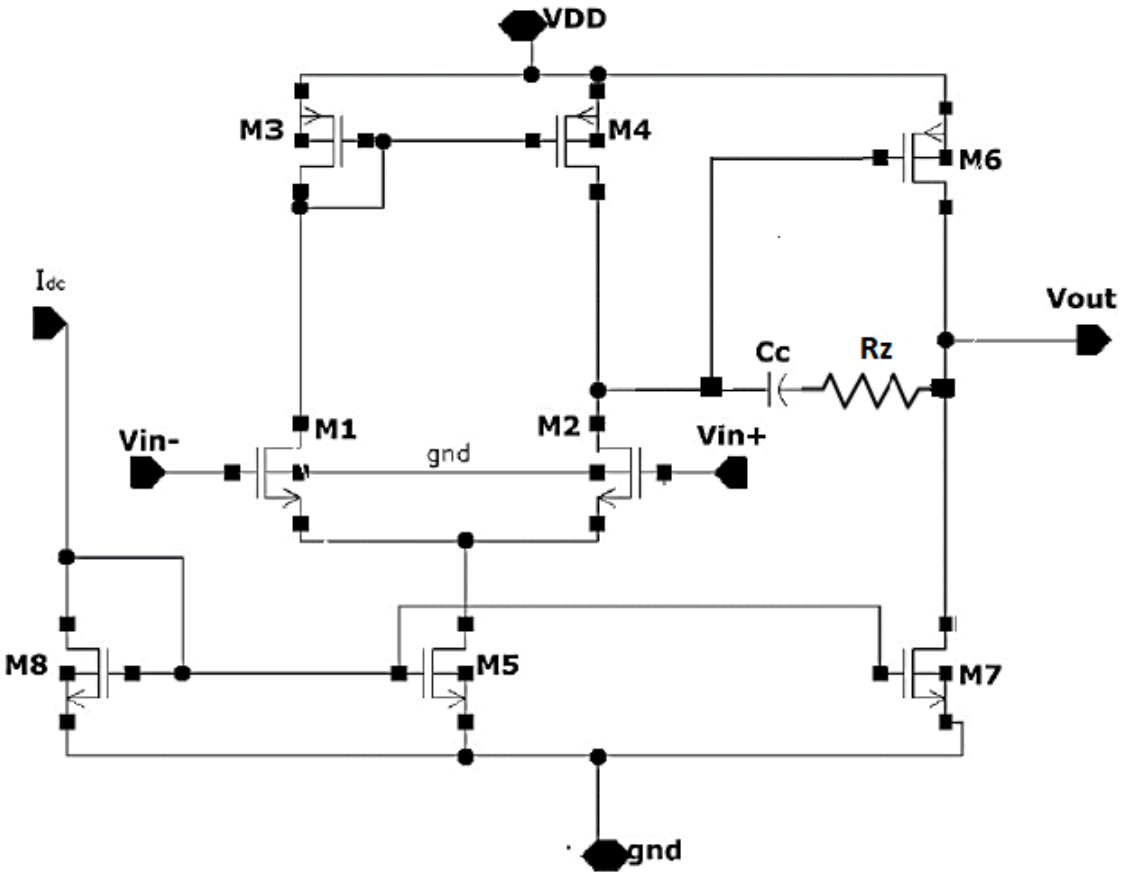

Figure 1.7- Conventional two stage op amp [25].

Figure 1.7 shown above is a schematic of conventional two stage op amp in which all the transistors are operating in a saturation region. It can be seen from above circuit that, Cc is the coupling capacitor used along with Rz which is a nulling resistor to nullify the effect of

zero from circuit and hence, increases the phase margin of the circuit. The table 2, shown be will give all the technological parameter values of conventional op amp.

Figure 3.1 shows the gain as well as phase characteristics plot of the conventional op amp circuit shown in figure 2.7. A sinusoidal signal of 1mV and a frequency of 1 kHz is applied at the non-inverting input of an op amp with common mode voltage of 1.6V. We found a DC gain of 64.0944 dB and having maximum phase of 179.72 degree. The phase margin of 82.69 degree is reported along with a UGB is 33.7 MHz is shown in figure 3.2.

3.1.1 Simulated values of conventional op amp

Table 2- Technological parameters of conventional two stage op amp.

S. No.	Parameters	Values
1.	DC Gain	64 dB
2.	Maximum Phase at 100 Hz	179.7 degree
3.	UGB	33.7 MHz
4.	Phase Margin	82.6 degree
5.	Slew Rate	25 V/us
6.	ICMR-	0.8 V
7.	ICMR+	1.2 V
8.	Common mode voltage	0.8V
9.	Supply Voltage	1.8 V
10.	Power Dissipation	436uW
11.	CMRR	104 dB

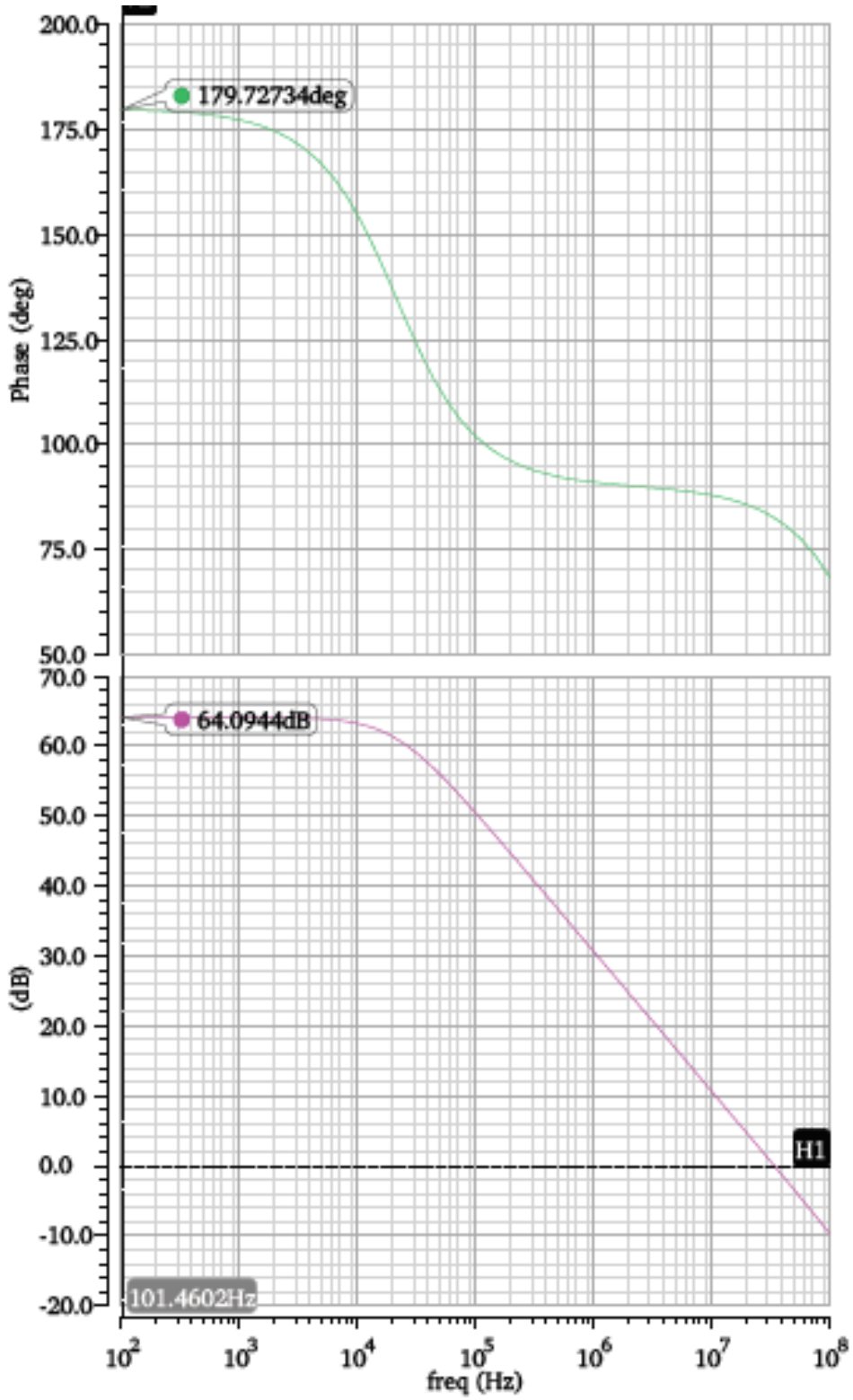

Figure 3.1- Gain and Phase plot of conventional two stage op amp.

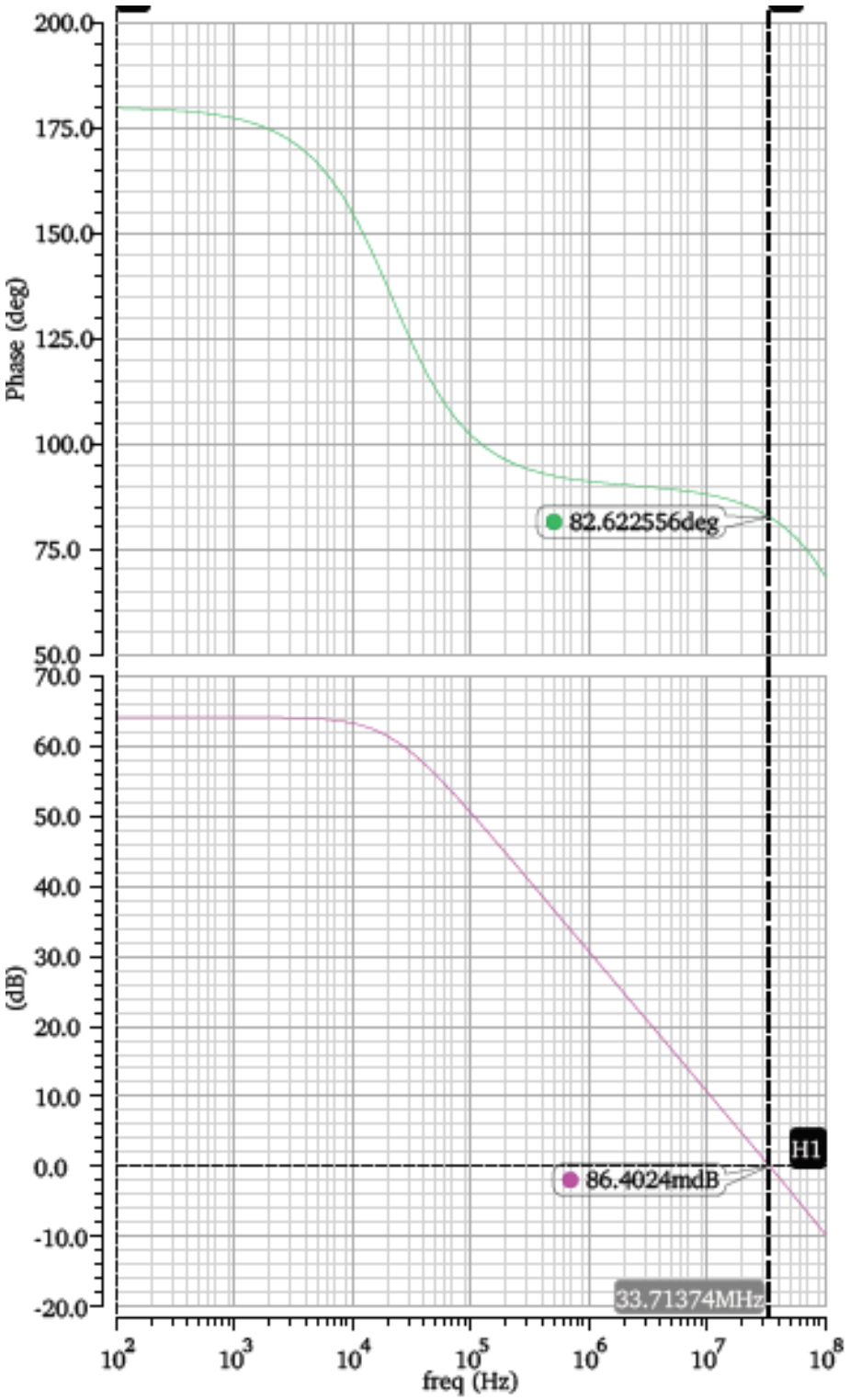

Figure 3.2- UGB and phase margin plot of conventional two stage op amp.

3.2 Schematic of FGMOSBbased Op amp Circuit

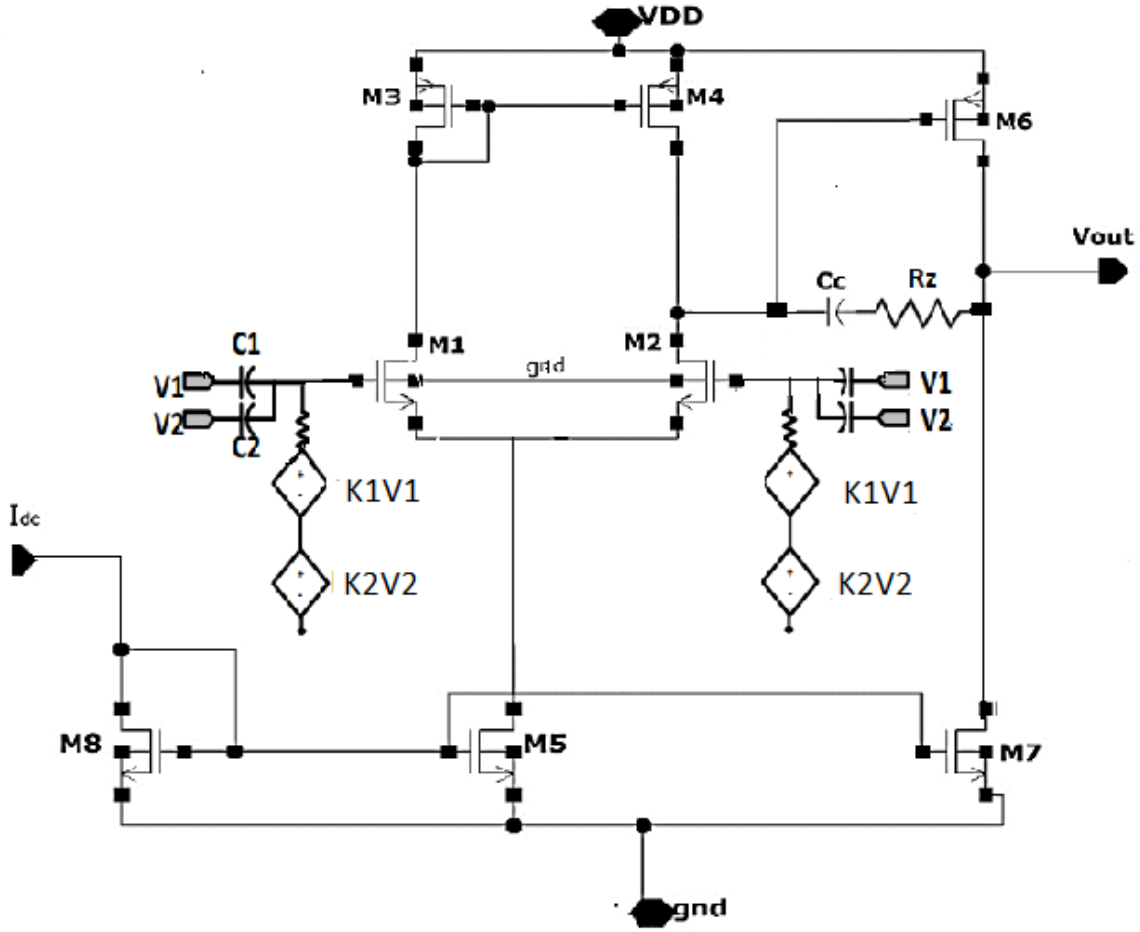

Figure 3.3- FGMOS based two stage op amp.

Figure 3.3 shown above is a two stage op amp based on FGMOS with DC input path to ground constraint taken into consideration. Here, K1V1 and K2V2 are voltage dependent voltage sources used with a large resistor to provide DC path to ground that helps to resolve convergance problem, where K is the capacitance ratio i.e., C1/CT=K1 and C2/CT= K2. Here, C1 & C2 is given as 500 femtoFarad& V1 as well as V2 is 0.67V.Hence, the resultant of K1V1 & K2V2 is given by 0.67V & resistance is given as one megaohm.

The gain of this op amp is given by 53.3 dB and has a phase margin of 73.2 degree as shown in figure 3.4, that indicates highly stable system.The UGB of this op amp is given by 30 MHz as shown in figure 3.5.also, from figure 3.6, it can be seen that the CMRR of this op amp is 93.9 dB. Table 3 shown below describes about transistor dimensions for conventional op amp and FGMOS based op amp. Also, table 3 gives all the technological parameter of FGMOS based op amp.

3.2.1 Simulated Values of FGMOS Op Amp

Table 3- Technological parameters of FGMOS based two stage op amp.

S. No.	Parameters	Values
1.	DC Gain	53 dB
2.	Maximum Phase at 100 Hz	179.8 degree
3.	UGB	30 MHz
4.	Phase Margin	73 degree
5.	Slew Rate	50 V/us
6.	PSRR	73 dB
7.	CMRR	93.9 dB
8.	Common mode voltage	0.6 V
9.	Supply Voltage	1.35 V
10.	Power Dissipation	290uW

3.3 Transistor Dimensions of Conventional and FGMOS Based Op Amp.

Table 4- FGMOS and conventional op amp transistor dimensions.

Transistor	Width (W)	Channel Length (L)
M1	3.36 um	480 nm
M2	3.36 um	480 nm
M3	890 nm	400 nm
M4	890 nm	400 nm
M5	480 nm	400 nm
M6	25.6 um	480 nm
M7	7.2 um	480 nm
M8	480 nm	400 nm

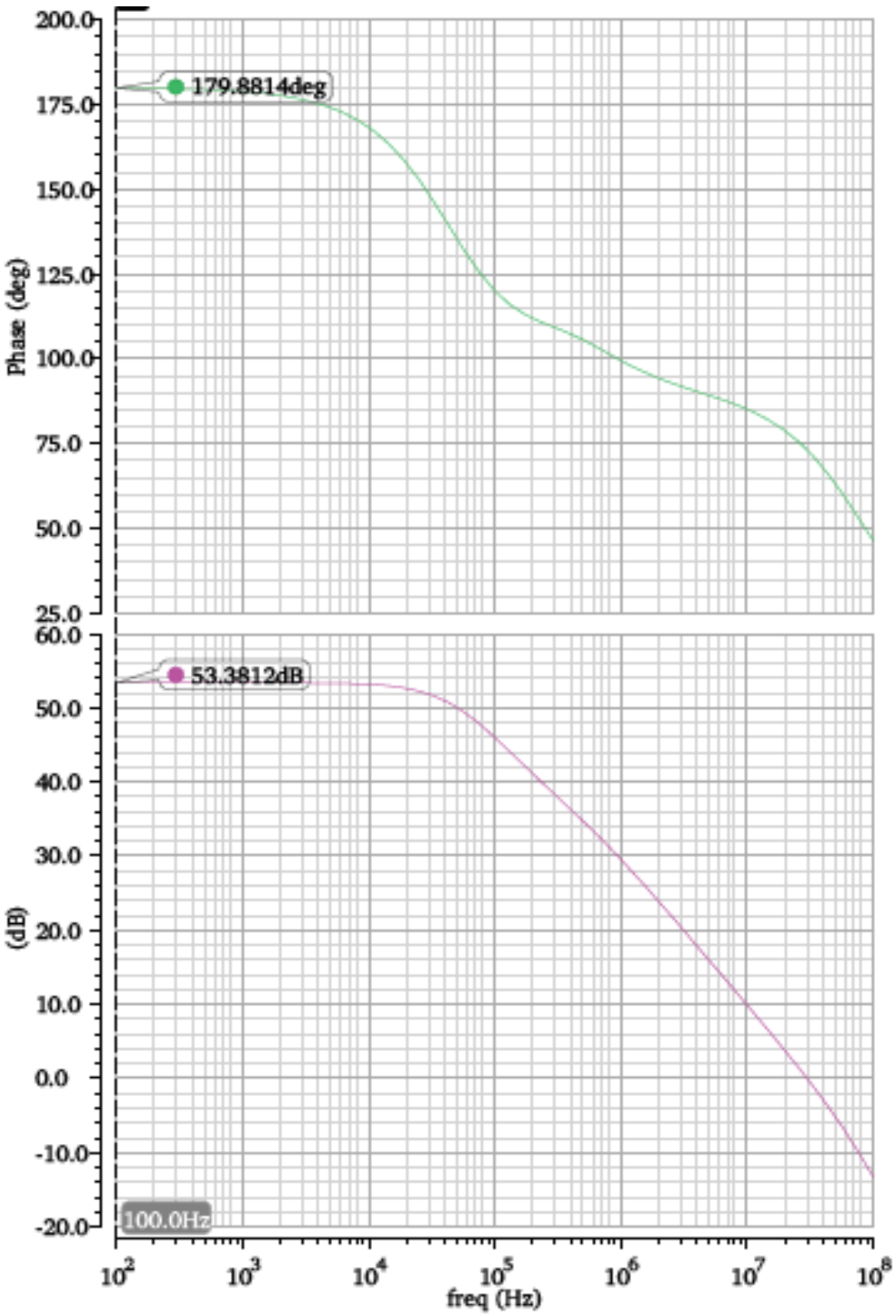

Figure 3.4- Gain and Phase plot of FGMOS based two stage op amp.

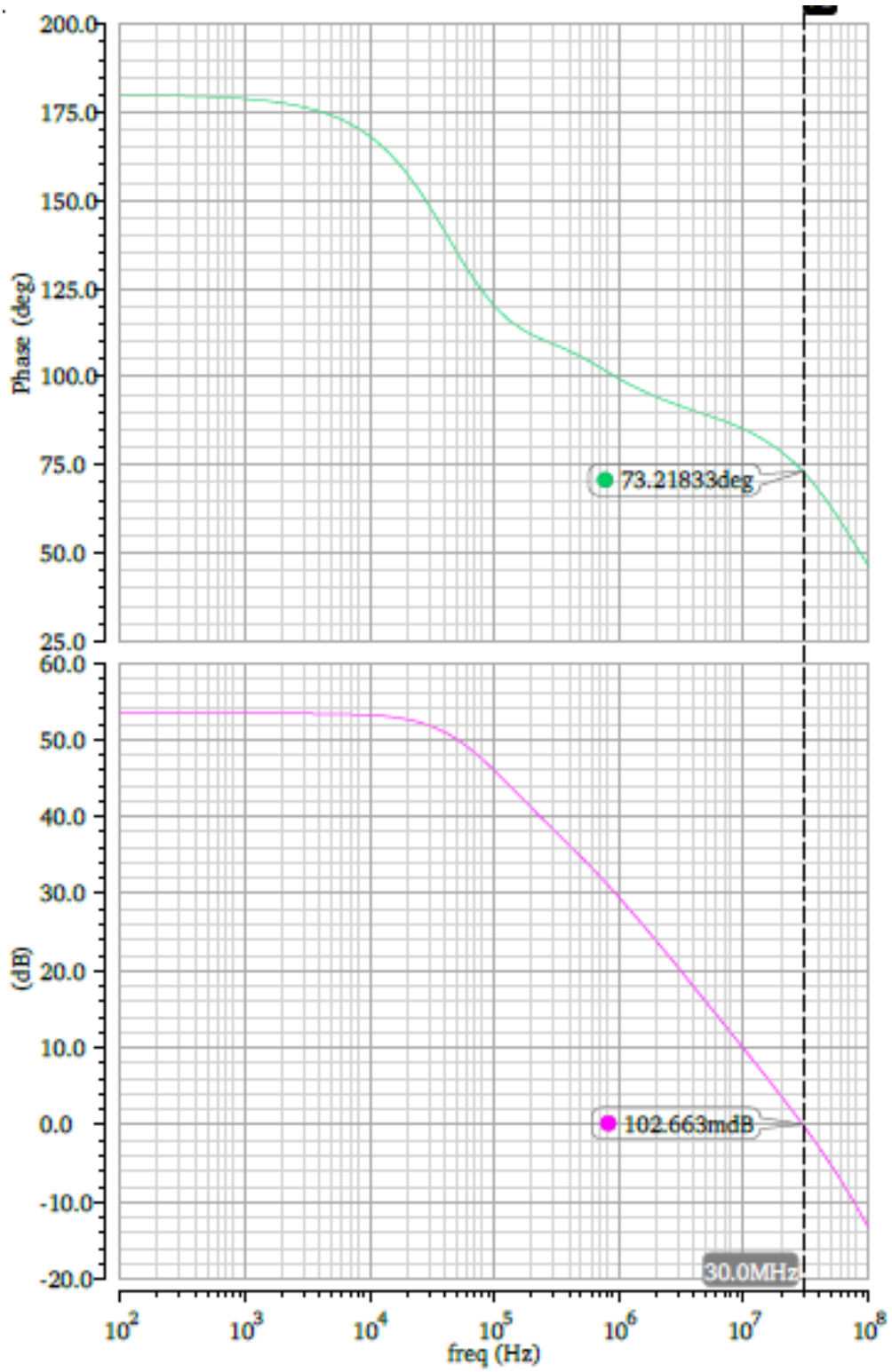

Figure 3.5- UGB and phase margin plot of FGMOS based two stage op amp.

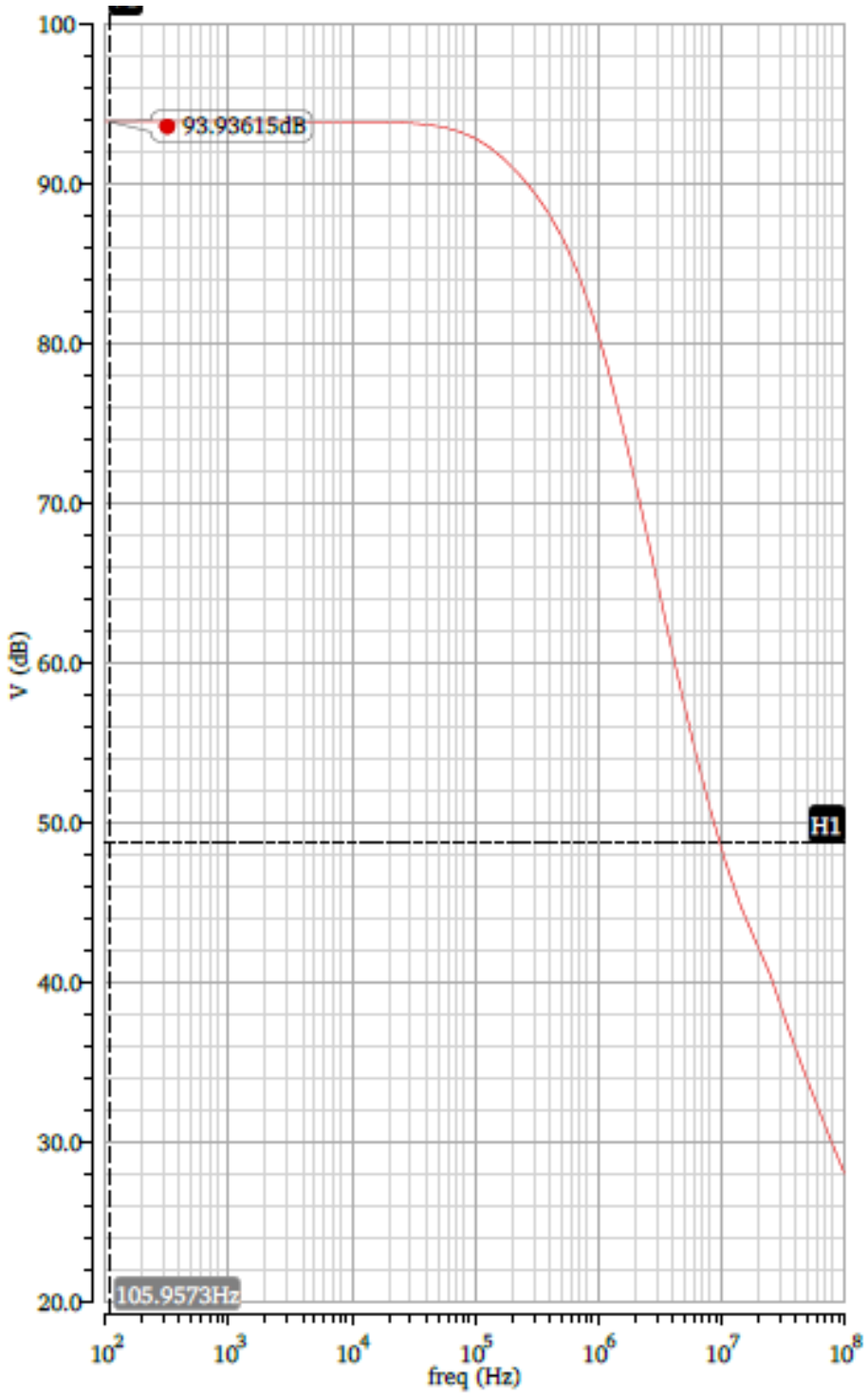

Figure 3.6- CMRR plot of FGMOS based two stage op amp.

3.4 Instrumentation Amplifier

Figure 3.7, illustrates instrumentation amplifier based on FGMOS transistor. An instrumentation amplifier is a circuit which extracts out weak potential signal and hence, it is very useful circuit for bio medical applications. This instrumentation amplifier is voltage mode amplifier. By keeping all the op amp in transistor in saturation region, op amp is drawn. This instrumentation amplifier is remains stable upto large value of gain varying resistor i.e., it remains stable upto 10Kohm of Rg. Figure 3.9 shows that phase margin of this instrumentation amplifier is more than one degree and hence, closed loop system is stable. The necessary condition for closed loop system to be stable is that, its phase margin should be more than zero degree i.e., it should have positive phase margin. Table 5 shown below gives all the technological parameters of instrumentation amplifier shown in figure 3.7.

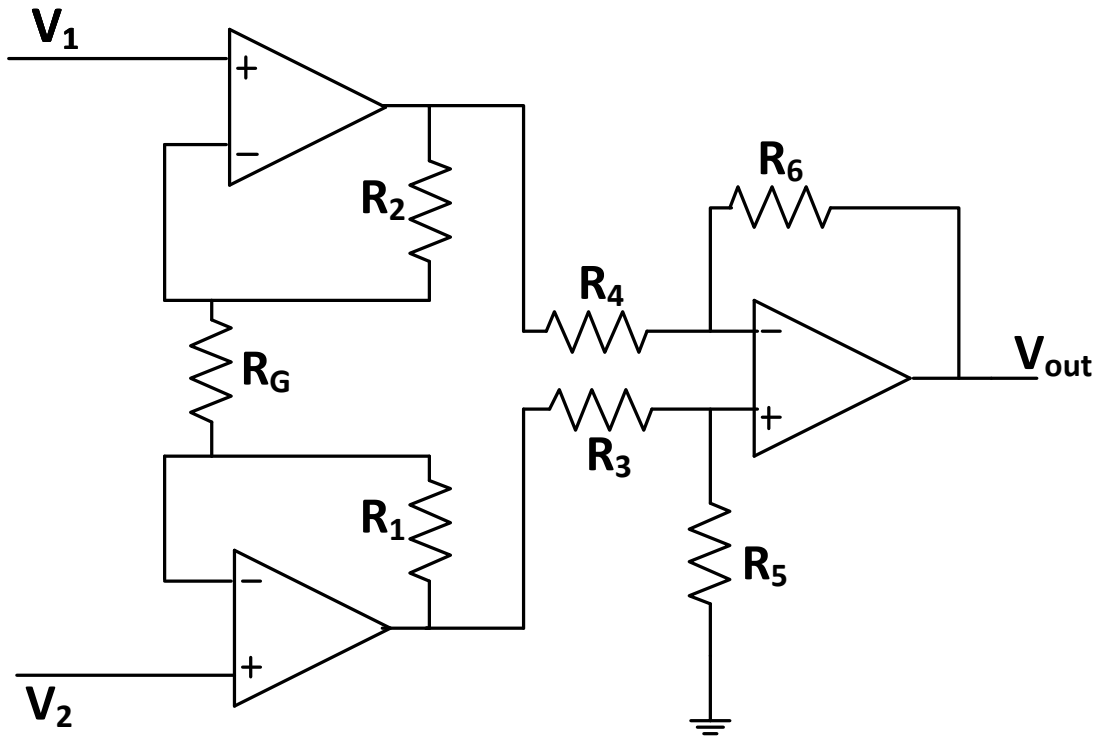

Figure 3.7- Instrumentation amplifier based on FGMOS two stage op amp.

Table 5 – Resistor Values of instrumentation amplifier.

S. No.	Resistor	Value
1.	R_G	Gain varying resistor
2.	R_1	30 Kohms
3.	R_2	30 Kohms
4.	R_3	10 Kohms
5.	R_4	10 Kohms
6.	R_5	22 Kohms
7.	R_6	22 Kohms

3.4.1 Simulated Parameters of Instrumentation Amplifier

Table 6- Technological parameters of FGMOS based instrumentation amplifier.

S. No.	Parameters	For Rg= 10 ohms	For Rg= 100 ohms	For Rg= 1 Kohms
1.	Difference mode gain	40.46 dB	39.5 dB	32.8 dB
2.	CMRR	86.7 dB	80 dB	58 dB
3.	3dB frequency	200 kHz	239.5 kHz	834.3 kHz
4.	Gain Bandwidth	10 MHz	10.5 MHz	11.5 MHz
5.	Power dissipation	719 uW	721 uW	727 uW

* all the parameters are calculated at common mode voltage of 1V.

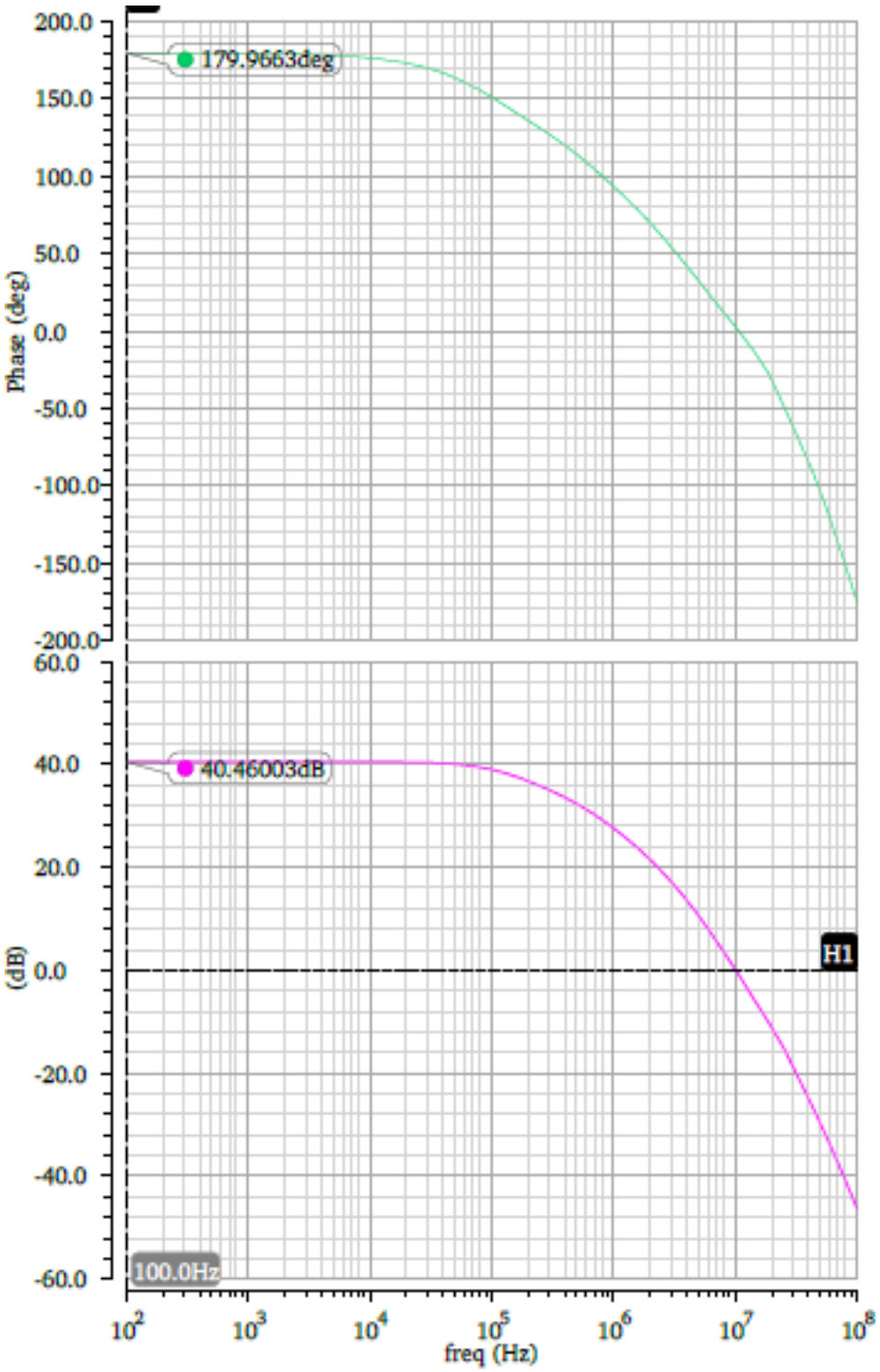

Figure 3.8- IA gain and phase plot based on FGMOS at Rg=10 ohms.

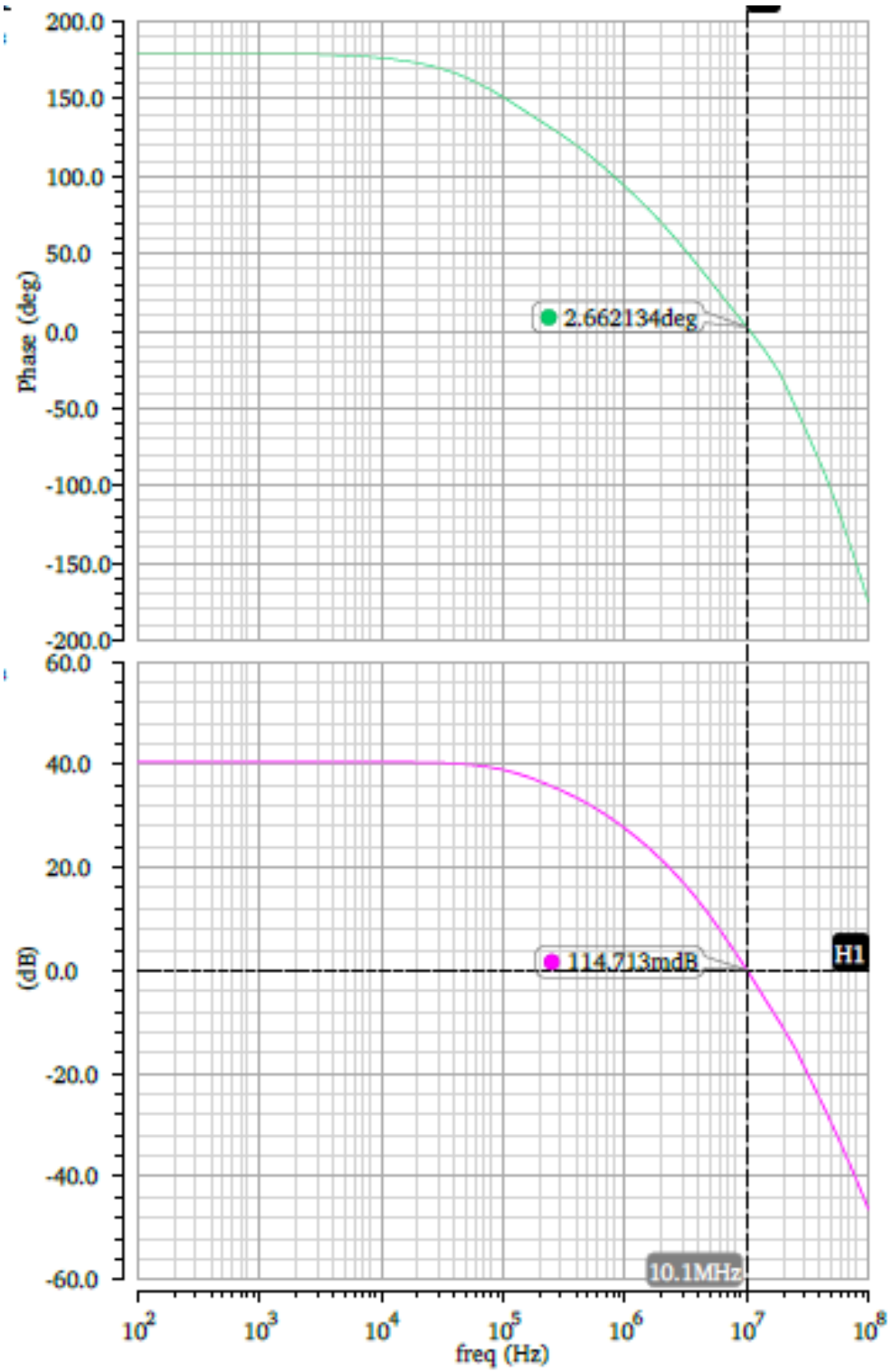

Figure 3.9- IA UGB and phase margin plot based on FGMOS at Rg=10 ohms.

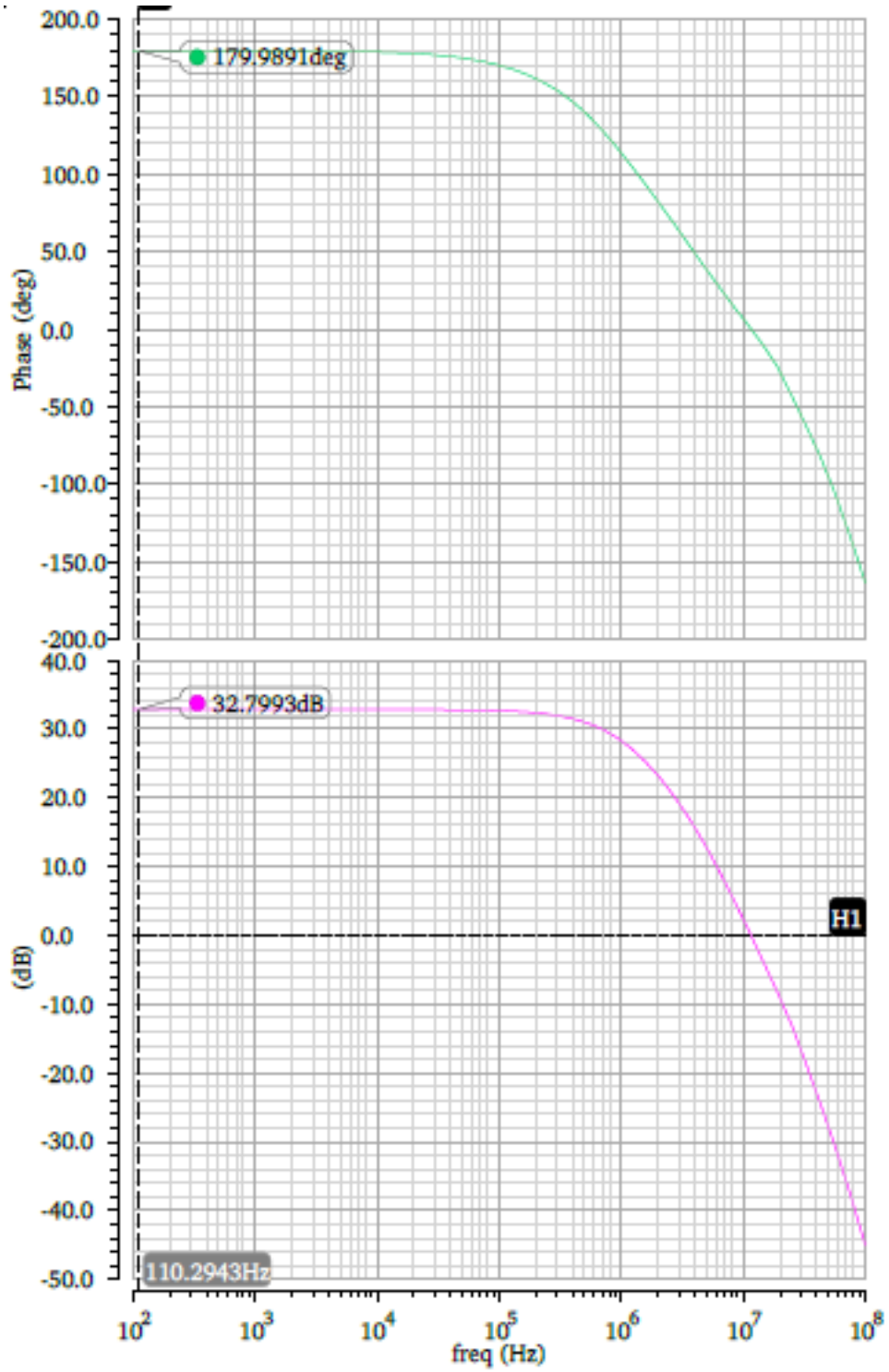

Figure 3.10- IA gain and phase plot based on FGMOS at Rg=1K ohms.

CHAPTER- 4
RESULTS AND CONCLUSION

After studying the FGMOS, simulation models and graphs were plotted in chapter 3. In this chapter we will evaluatethe result and will arrive to a possible conclusion from the data given in chapter 3.

As it can be seen from section 3.1 that, conventional op amp is simulated in virtuoso gpdk 90nm simulator. This conventional op amp is offering high unity gain bandwidth of 33MHz and having phase margin of 82.6 degree which is indicating highly stable system. The condition for a two stage op amp to be stable, its phase margin is need to have 45-60 degree.

The technological parameter for a conventional two stage op amp is charted out in table 2.

Section 3.2 of chapter 3 describes about FGMOS based op amp. Table 3 illustrates all the technological parameter of FGMOS based op amp. By comparing conventional op amp and two stage op amp, it is noted that, FGMOS based op amp offering significant power reduction for the same value of aspect ratio. The aspect ratio of both FGMOS and conventional op amp is charted out in table 4. The main advantage of using FGMOS in two stage op amp is that, it offers tuning of threshold voltage and also low power requirement.

Section 3.4 illustrates instrumentation amplifier based on FGMOS op amp. This op amp offers high CMRR and hence suitable for bio medical applications. For bio medical applications, it is required to have CMRR more than 60dB. Also, this circuit is consumes less power and hence suitable for portable powered devices.

The limitations of this op amp is that, it requires resistor trimming to get high CMRR. Also, from figure 3.7, it can be seen that, it is three op amp instrumentation amplifier and hence, requires a large chip area. Table 5 shown above gives all the technological parameters of IA.

The next section 3.5 will deal with possible challenges faced by the technology scaling to the nanometer region.Also, in section 3.5, a newsimulation model is discussed for FGMOSthat will be used in simulating FGMOS in nanometer scale technologies.

4.1 Problem Faced in FGMOS Model for Nanometer Technologies

The result based on above model of FGMOS discussed above in chapter 3 is not accurate and hence there must be some change in parameter will occur. As it cannot be applied for submicron technologies due to thin gate oxide of transistors which leads to gate leakage current.

A new model for submicron i.e., sub 100nm CMOS technologies is derived. The analysis is conducted by considerating gate leakage current into account & also the way FGMOS structure responds to it.

Gate leakage current is due tocharge movement at the oxide. It also depends on the type of transistor & the polarity across the insulator, and it can be found as:

$$Q_{leakage}=C_T V_{leakage} \tag{4.1}$$

$$\frac{dQleakage}{dt}= C\frac{dVleakage}{dt} \tag{4.2}$$

$$I_{leakage}=C_T\frac{dVleakage}{dt} \tag{4.3}$$

$$\frac{dVleakage}{dt}= \pm\frac{1}{CT}I_{leakage} \tag{4.4}$$

$$V_{leakage}= \frac{1}{CT}\int Ileakage\,dt \tag{4.5}$$

Equation (4.4) shown above suggests that, the charge movement in FGMOS oxide due to leakage can be into or out of gate oxide due to voltage change can be negative and positive quantity. Hence, floating gate voltage can increase or decrease as a function of time based charge flow & thecapacitors values and can be written as:

$$\frac{dVFG}{dt}= \frac{C1}{CT}\frac{dV1}{dt} + \frac{C2}{CT}\frac{dV2}{dt} +------+ \frac{Cn}{CT}\frac{dVn}{dt} \pm\frac{1}{CT}I_{leakage} \tag{4.6}$$

$$V_{FG}= \sum_{i=1}^{N}\frac{C1V1}{CT} + \frac{C2V2}{CT} + ----- + \frac{CnVn}{CT} \pm V_{leakage} \tag{4.7}$$

The condition to keep the transistor in saturation region is $V_{FG} > V_{TH,}$ and by aplying V_1 as the effective input, the result is given as:

$$V_1>\frac{CTVT}{C1} - \frac{C2V2}{C1} - ----- - \frac{CnVn}{C1} \pm\frac{CT}{C1}V_{leakage} \tag{4.8}$$

Hence, the equivalent threshold voltage for floating gate transistor innanometers technologies is given by:

$$V_{THFG} > \frac{CTVT}{C1} - \frac{C2V2}{C1} - \text{----- } - \frac{CnVn}{C1} \pm \frac{CT}{C1} V_{leakage} \quad (4.9)$$

Equation (4.8) showing very important implication of gate leakage current because this leakage current will increase the effective threshold voltage in NMOS transistors.

Equation (4.10) shows below showing that, the threshold voltage of a FGMOS is a function of gate leakagecurrent due to tunneling effect. The gate current is an exponential function ofgate voltage and also technology dependent parameters A and B.

$$I_G = A \cdot e^{BVG} \quad (4.10)$$

Where B and A are the technology and biasing conditions dependent parameters that are extracted out from fitting the simulation data in TSMC 90nm for gate current using BSIM4. These parameters will futherincrease as the technology scaled down to 65nm, 45nm or 28nm.

4.2 A New Model for FGMOS Transistor in Nanometer Technologies

To test the floating gate circuit without actually fabricating it, a new model is proposed. This model is arises by keeping the things in mind that the CMOS technologies continue shrinking down as tox scaled down proportionally and this causes more gate leakage current.

This new simulation model is proposed for FGMOS that are suitable for submicron technologies. This model also includes gate leakage current and is compatible with simulators likeSpectre and SPICE.

To built this model, a standard transistor from the industry i.e., TSMC 90nm with two cells from analog hardware description language AHDL library is used along with one block of verilog code to describe the gate tunneling.

As described in [36-37], the new model uses voltage dependant current source in its implemented in Verilog code embedded under Cadence / Spectretol& it is described as a function of V_{gs}terminal. As shown in figure 4.1, the circuit also includes an integrator

along with subtractor, integrator integrates the gate tunneling current to generate a voltage which is fed intosubtractor.

The model shown in below figure 4.1 is suitable with any submicron technology oxidethickness less than 3nm& suffers gate leakage current with no change in the model itself is required. However, to comply with thetechnology parameters where the gate tunnelling current exponentially increases as tox decreases, some changes need to be done to the gate tunneling cell. By addinginitial condition to the leakage current integrator, this model can be used for transient and DC simulations.

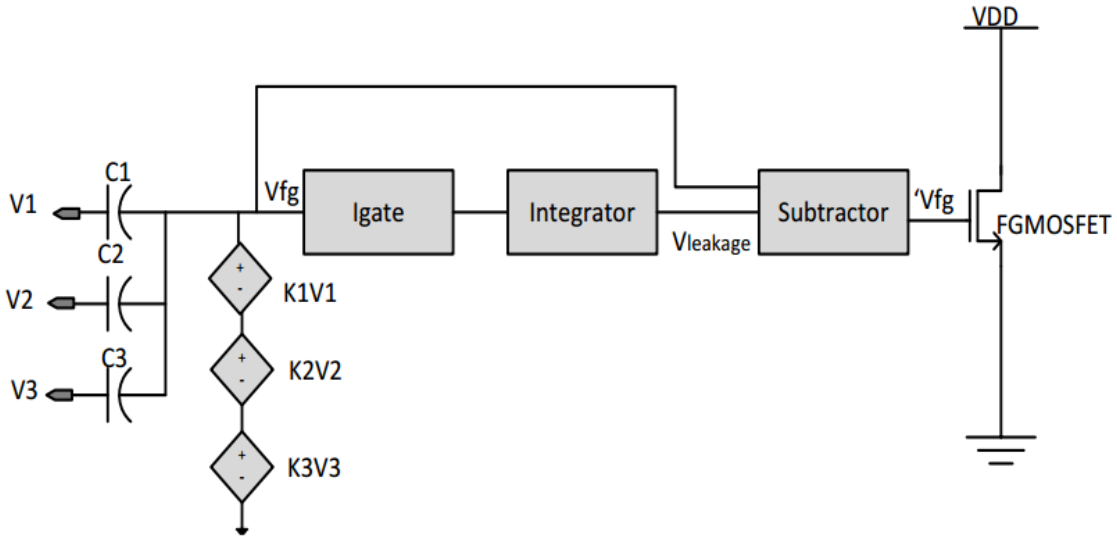

Figure 4.1: The structure of N-type FGMOS simulation model for nanometer (sub 100nm) technologies.

CHAPTER- 5
FUTURE SCOPE

In this thesis, a three op amp based IA is simulated based on the FGMOS opamp. FGMOS based op amp is derived from conventional two stage op amp in which a nulling resistor is used to nullify the effect of zero in the transfer function which increases the phase margin of the circuit. In the circuit shown in figure 1.7, where a passive resistor is used as a nulling resistor. Further modification can be done by replacing passive resistance with MOS transistor, this will help in reducing total chip area, as passive resistor is not preferred in IC. Using MOS transistor will also increase total transistor count but total chip area is less than that of passive resistor.

The instrumentation amplifier drawn above is a voltage mode IA and hence resistor trimming is required to get high CMRR which is a major drawback of this IA. Further modification can be done by replacing this IA with current mode IA. Also, passive reistance in buffer stage can be replaced by the current mirror which also helps to avoid resistor trimming constraint. As IA is a fundamental block for all the biomedical applications, it is need to have smaller chip area and also it is required to operate for longer time. Hence, current mode IA will be best suited for this.

Also, the problem with submicron technologies also taken into consideration in chapter 4. Hence, a new IA can be drawn based on that in which charge leakage can be easily controlled. All the analog devices can be futher implemented in submicron technologies based on that. It helps to get over DT leakage current problem. By taking DT leakage current into consideration, an enhanced circuit can be drawn.

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Appendix: (i) List of Published papers

CMOS Instrumentation Amplifier Design in ICSTM-Pune 2017.

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Academic Science

CMOS Instrumentation Amplifier Design

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Abstract: *CMOS instrumentation amplifier (IA) is an electronic circuit that operates on low supply voltage and requires less chip area. It is a very crucial electronic block for large number of applications since it can amplify small signals also. Its large gain can amplify smallest possible signal that may lie in between microvolts to millivolts. Its low power- low voltage characteristics make it implantable in human body. This paper reviews the design of IA for specific applications. Different design technologies have been discussed in this paper along with application based comparison table.*

Keywords: CMOS, Instrumentation Amplifier, CMRR, PSRR, DC Offset, Input Referred Noise, Gain Bandwidth.

Introduction

An instrumentation amplifier (IA) is an amplifier in electrical systems that can amplify extremely small differential voltage [1] that may lie in between microvolts to millivolts. It is basically a difference amplifier that has low DC offset, low noise, very high open loop gain and high CMRR, as desired for most of the applications. IA is used in biomedical engineering to study physiological signals like ECG, EMG, EEG, etc. [2-5]. It is playing an important role in bio-medical engineering. It helps in extracting out desired signals from human body. It helps in diagnosing human body, via which we can get idea about diseases. Since all the physiological signals are having very small amplitude and having frequency less than 1 kHz, it is desired to have an IA with high gain, which can amplify small difference also; low DC offset that occurs from electrode-body interface; high CMRR which can supress common mode gain. It also used in navigation, radar instruments, high frequency signal amplification in RF systems, to improve signal to noise ratio in audio applications, in data acquisition from automotive transducers [6], industrial process control [7-9], high frequency inductive position sensing [10], etc. An IA is used in large number of applications. Important parameters of an IA such as PSRR, CMRR, Offset etc. are also discussed in this paper.

This paper is organised as follows. Section I provides an introduction to the topic. Section II presents Conventional Instrumentation Amplifier. Section III describes CMOS IA Design; and Conclusion and Future scope is presented in Section IV.

Conventional Instrumentation Amplifier

The conventional IA as shown in figure-1, consists of three op-amps and resistive feedback network. It requires large chip area and high supply voltage because of passive resistance. Passive resistance also deteriorates the gain of IA because resistor matching is essentially required in conventional IA to get high common mode rejection ratio (CMRR). Circuit shown in figure-1 will give maximum CMRR because of matched resistor configuration. But it is not implantable in human body because of large area and huge power consumption which can drain out the bias supply voltage of the circuit quickly. To resolve this problem we can use IA with active devices such as NMOS transistor, current mirror, current conveyor etc. The brief explanation of conventional op-amp is given below. The rightmost op-amp is a basic difference amplifier that amplifies the potential difference appearing on its inverting and non-inverting terminal. The two amplifiers on the left hand side behaves as unity gain buffer amplifier when R_{gain} is open circuited and circuit offers high input resistance and the gain of the circuit is given by R_3/R_2 [2]. Common mode gain in an IA is due to the mismatch in the resistors R_3/R_2 & due to the common mode gain of two buffer amplifiers. Due to common mode gain CMRR decreases. To get high CMRR, it should be

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minimum possible and ideally common mode gain should be zero which means CMRR should tends to infinity. To minimize common mode gain, passive resistance are replaced by active devices.

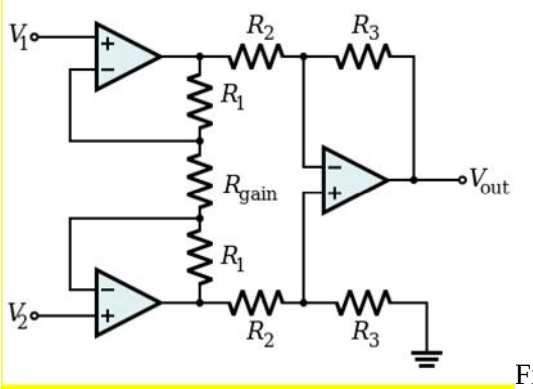

Fig-1: Conventional Instrumentation Amplifier [11]

CMOS IA Design

CMOS IA is used over conventional IA because it requires less chip area. It operates on less power and has very good CMRR. Different IA circuits are shown below. The IA shown in figure-2 consists of three op-amps, current mirrors and some resistors. CM1, CM2, CM3 and CM4 are the current mirrors used to copy current I1 flowing through resistor R1, to current I2 flowing through resistor R2; and given by I1=I2= -I3.

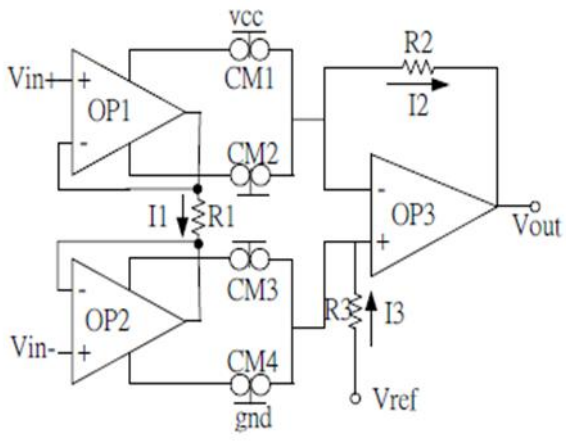

Fig-2: Instrumentation Amplifier design with current mirror [12].

The two input voltages Vin+ and Vin- sense bio-medical potential and produce a current I1. The op-amp1 and op-amp2 convert input voltage to current. Internal circuitry of op-amp1 and op-amp2 are given in figure-3.

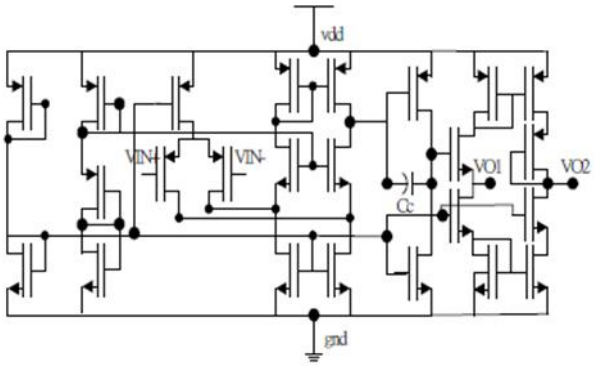

Fig-3: Voltage to current op-amp circuit using CMOS technology [12]

The circuit shown in figure-3 is having four stages; the first stage is bias circuit. In second stage, differential PMOS is used for the input. The third stage provides high gain stage and the last stage is output stage. The circuit shown in figure-2 provide high CMRR up to 160 dB & high PSRR up to 110 dB and is suitable for bio-medical engineering. Another IA with current mirror is shown in [23]. IA circuit shown in [24] consists of op-amp and active devices. The op-amp used in that IA is a two stage op-amp whose circuit is shown in figure-4 and for active devices NMOS transistors are used in place of passive resistors. All the NMOS transistors are biased in linear region so that they can behave as a resistor.

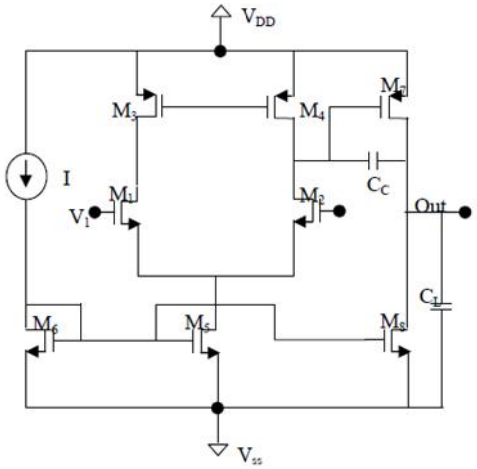

Fig-4: Two stage CMOS op-amp [13]

IA circuit proposed in [25] uses three stage op-amp (also shown in [25]) in its design and the proposed circuit also uses NMOS transistors in place of passive resistors. By using active devices chip area considerable reduces. It is desirable to have less DC offset, high CMRR, high PSRR and high gain.

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Circuit shown in [18] having DC offset cancellation circuitry in the IA block itself. [19] shows the op-amp with offset cancellation technique. Circuit shown in [22] is a current balancing IA; it provides high CMRR and less input referred noise.

All the parameters used in different applications of IA are discussed below:

(i) CMRR: The common-mode rejection ratio is used to quantify the ability of the device to reject common-mode signals. An ideal IA would have infinite CMRR which means common mode gain tends to zero. A high CMRR is required when a differential signal have to amplified large common-mode input. To increase CMRR, different techniques are available such as DDA technique [21].

(ii) PSRR: Power supply rejection ratio is used to describe the ability of an electronic circuit to suppress power supply variations in its output signal. In op-amp, the PSRR is defined as the ratio of the change in supply voltage to the change in differential output voltage it produces. An ideal operational amplifier would have infinite PSRR. It is specified in terms of the output & given by [15]:

$$PSRR = 20\log_{10}((\Delta V_{supply}/\Delta V_{out})A_v)) \text{ dB} \quad \text{(eq. 1)}$$

PSRR enhancement technique is shown in [16]

(iii) DC offset: In context of bio-medical engineering, dc offset is due to the electrochemical effects at the electrode-skin interface. These dc offsets are large and common across recording electrodes. They are typically in the range of 100mV to 500mV and are generated at the electrode electrolyte interface [17]. Different offset reduction techniques are shown in [18-19].

(iv) Gain bandwidth: It is the product of the amplifier's bandwidth and the gain at which bandwidth is measured [20]. Op-amps are designed to have a single pole frequency response and the gain bandwidth product is nearly independent of gain at which it is measured. In op-amp, the gain bandwidth product will be equal to unity gain bandwidth (the bandwidth at which amplifier gain is one) of the amplifier [20].

Different configurations of an IA are listed below:

(i) CMOS current mode IA [29 30 32].

(ii) CMOS current feedback IA [31].

(iii) CMOS current balancing IA [22].

(iv) CMOS IA design by gm/I_D methodology [33].

(v) Three stage low noise Op-amp [34].

Table 1: Parameters for different configurations of an Instrumentation Amplifier

S. No.	Parameters	Current mode IA				Current feedback IA	Current balancing IA
		[29]		[30]		[31]	[22]
1	Technology	0.18µm		90nm TSMC	130nm UMC	0.18µm	0.18µm
2	Supply voltage	1.8V		0.4V		1.8V	1.8V
3	CMRR	125dB		76dB	65dB	72dB	127dB
4	Power consumption	61.5 µW		11 µW	14 µW	2.6mW	1380.18µW
5	PSRR	PSRR+ 125.3dB	PSRR- 126dB	56.7dB	69.3dB	---	65dB
6	Layout area	---		0.023mm^2	0.021mm^2	0.08mm^2	758×377µm^2
7	Input referred noise	107nV/√Hz		3.71 µV_{RMS}	1.1 µV_{RMS}	0.24µV/√Hz	0.278µV_{RMS}

Table 1: Different Parameters for an Instrumentation Amplifier

S.No.	Parameter	[23]	[26]	[27]	[28]	[22]
1	Technology	0.35µm	---	0.7µm	0.35µm	0.18µm
2	Supply voltage	2.2V	±5V	5V	1.5V	1.8V
3	CMRR	128dB	---	-137dB	139dB at 1kHz	127dB
4	Power consumption	166µW	---	26µW	489µW	138µW
5	Layout area	350×150µ m^2	---	0.45 0.45mm ^{2}	---	758×377µ m^2
6	Simulator	Spectre	---	PSPICE	Spectre	HSPICE
7	Applications	ENG	Thermal gas flow sensor	Low frequency & micro-power applications	Piezo-resistive transducer	ECG
8	PSRR(dB)	---	PSRR +> 65 | PSRR- > 55	160	---	65dB
9	DC Gain of IA	81dB	53dB	87dB	110dB	45dB
10	UGB	580kHz	---	47kHz	---	---
11	DC Offset Voltage	---	±1 µV	0.7mV	---	0.3mV
12	Input Referred Noise Voltage	---	36nV/√Hz	---	9.6nA	0.278 µV/√Hz

Conclusion & Future Scope

CMOS IA is a basic building block for most of the electronic circuits since it requires less chip area and less power. It also improves the CMRR & DC gain, which amplifies the weak desired signal. Application based IA circuits are discussed in this paper.

Acknowledgement

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Appendix: (ii) List of communicated papers

Recent Advancement in Current Mode Instrumentation Amplifier

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Abstracts: An instrumentation amplifier (IA) is an important block for most of the signal acquisition circuit. Because of CMOS technology used in the fabrication of IA, it leads to operate the circuit on low supply voltage and low power consumption. This paper reviews the current mode instrumentation amplifier (CMIA) topology. Different technological parameters of CMIA are mentioned in this paper.

Keywords: CMOS, CMIA, CMRR, 1/f noise, GB, OTA, Current Conveyor.

I. Introduction

An Instrumentation amplifier is a basic difference amplifier which is used to amplify weak potential signals [1]. Studying IA is essentially important since, it is a vital block for most pf the applications like bio-medical engineering [2-5], sensor system [6-7], industrial process control [8-10]. CMIA is used over conventional IA to get desirable characteristics and properties. In CMIA, op-amp supply current-sensing technique is used to get high CMRR over a larger bandwidth than conventional op-amp [12]. The supply- current sensing technique has been used in different circuits like Current Conveyors, Active Filters, Precision Rectifier etc. [13-15]. Massive work have been done by C. Toumazou et. al. in the field of current sensing technique. CMIA provides better frequency range of operation & high CMRR.

Current sensing technique based on current conveyors [17] was reported by B. Wilson in 1984 which is based on current convertor [18-19] and later applied to the various applications. B. Wilson and Fabre [20-21] have previously been described the high performance current convertors by using either op-amp & current mirrors or by trans-linear circuits. Both this approach gives convertor high linearity & low distortion over a wide range of bandwidth. The circuit shown in figure-1 was proposed by Wilson shows the technique of current sensing in combination with current mirrors that formed the family of low distortion voltage to current convertors.

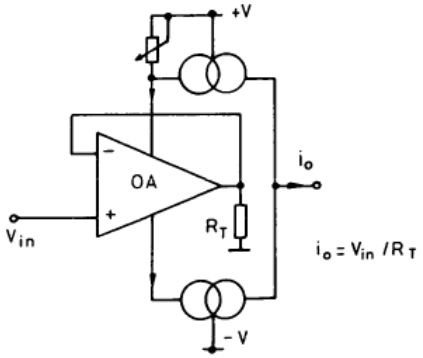

Fig-1: Wilson's voltage to current convertor [17].

There are large number of current convertors design topologies have been investigated, but the most effective design is shown in figure-2.

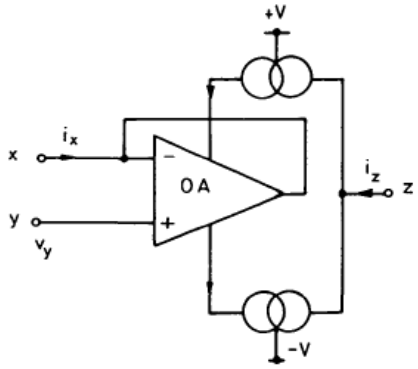

Fig-2: Precision CCII+ current conveyors [17].

The input-y of the circuit shown in figure-2 is a short circuit stable voltage input of very high impedance & used to drain op-amp input bias current. Input-x shows the voltage at terminal-y & act as open circuit current terminal. With the use of four transistor current mirror, it can be possible to reduce current transfer inaccuracy less than 1% and low distortion can be achieved for precision CCII+. Also transfer distortions from y to x & x to z of less than -70dB were measured and the capacitance at terminal-x must be low enough to avoid the conveyor performance at high frequencies.

Circuit shown in figure-3 is more appropriate where low distortion operation is required with a significant load voltage excursion.

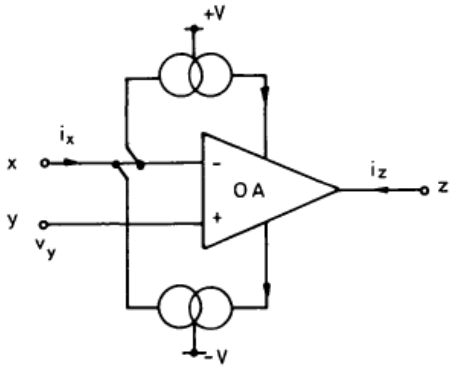

Fig-3: Feedback CCII+ current conveyor [17].

The feedback connection shown in figure-3, makes the circuit immune to distortion which normally produced in current mirror by voltage modulation effects [18].

B. Wilson CMIA is shown in figure-11. It consists of two second generation current conveyors connected in parallel.

This paper is organised as follows. Section I provides an introduction to the topic. Section II presents Conventional Instrumentation Amplifier. Section III describes CMIA Design and section IV provides enhanced CMIA followed Conclusion and Future scope is presented in Section IV.

II. Conventional Instrumentation Amplifier

The three op-amp circuit with resistive feedback network is shown in figure-4. The drawbacks of this circuit is that, matching of components are required to get high Common Mode Rejection Ratio (CMRR). Due to CMRR issue, it is less desirable to use this circuit for bio-medical applications where CMRR is a key factor. Also due to resistor trimming to get high CMRR, gain of the circuit also changes. It also requires large chip area since large number of passive components are used in the circuit and it dissipated huge power. Due to the above drawbacks, this circuit obsolete from the use in many applications, also because of miniaturization is essentially required. Many new techniques of designing of IA are available with different active analog blocks. The drawback of this circuit can be reduced by replacing passive components by active devices like current mirror, or using Operational Trans-resistance Amplifier (OTA), Current conveyors etc. in the designing of IA. Current conveyors also allows high differential gain without much reduction in bandwidth as compared with the conventional op-amp circuits. A dual high input impedance is arranged to produce a high differential gain along with unit common mode gain to enhance the performance of the conventional voltage op-amp.

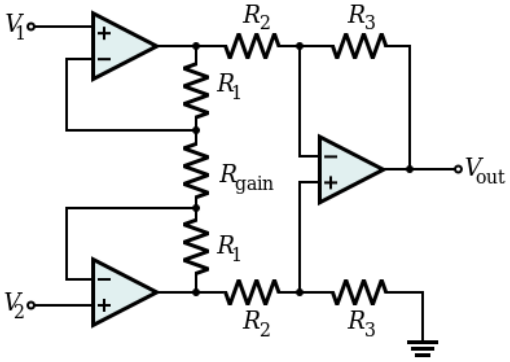

Fig-4: Conventional Instrumentation Amplifier [11].

In bio-medical applications, it is required to have an instrumentation amplifier with wide bandwidth and high CMRR. Conventional IA as shown in figure-4 is a voltage amplifier that exhibits a narrow bandwidth and it's bandwidth is also dependent on gain because of fixed gain bandwidth (GB) product of the op-amp.

III. CMIA Analysis

The CMIA reported in [12] by C. Toumazou et. al. was the basis of all the new generation IA.

The circuit shown in figure-5 is the input stage of the conventional IA. If a signal is applied to the input, it get transferred to the node A & B of the circuit and the current-I can be calculated as:

$$I= (V_2-V_1)/ R_1 \quad (i)$$

It can be seen that, the common mode signals, $V_2=V_1=V_{CM}$, current-I results in zero & $V_{02}=V_{01}=V_{CM}$, and also this stage has unity common mode voltage gain.

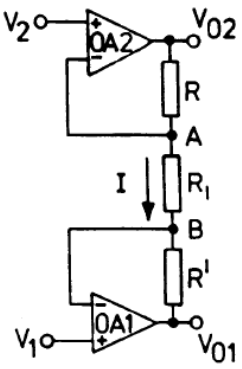

Fig-5: Differential input stage of conventional IA [12].

In conventional IA, third op-amp is used to subtract V02 from V01, results in single ended output which is proportional to V2-V1. In this part of the circuit, it is utmost required to have low common-mode gain and can be achieved by standard four resistor differential amplifier with matched resistors.

If it is possible to get the current-I at the output, it will results in zero common mode trans-conductance gain. Op-amp current sensing technique [13-15] is used to get current-I as an output parameter. A complete circuit diagram of CMIA is shown in figure-6.

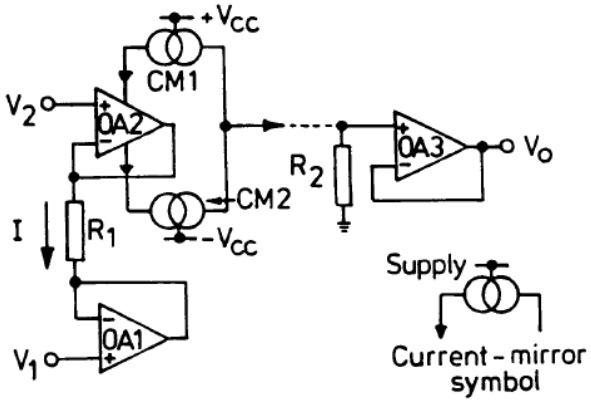

Fig-6: Novel CMIA [12].

To simplify the circuit diagram, current mirror is replaced by equivalent symbol and represented by CM. The direction of current from current mirror is also shown.

Op-amp-1 and op-amp-2 acts as high impedance input voltage buffer for the non-inverting & inverting inputs V_2 & V_1 respectively as shown in figure-6. As shown in above figure-6, the voltage across R1 is V2-V1 & it indicates the current in the feedback path of the op-amp-1 and it is sensed by the CM1 & CM2. The output of the CM1 & CM2 are recombined at a current sensing node of the last stage that comprises op-amp-3 & R2.

Assuming ideal voltage follower and current mirror, the output of op-amp-3 is given by:

$$Vo= \lambda(R_2/R_1)(V_2-V_1) \quad (ii)$$

Where, λ is current transfer ratio of the current mirrors (close to unity).

From equation-ii, it is clear that common-mode gain is zero. Since, the ideal op-amp have been assumed in the above

calculation, it can be noted that the analysis shows an infinite CMRR can be obtained without resistor trimming unlike conventional IA.

The potential difference across resistor R1 is zero in the presence of common mode input because of the action of the two voltage buffer and this results in no supply current change in either op-amp1 or op-amp2 & hence the output voltage is zero. It should also be noted that any mismatch in the λ of the CM1 & CM2 has no-effect on common-mode gain but merely causing some distortion in the output signal.

The main cause of non-zero common-mode gain in the IA is due to the GB product of the two input op-amps used in the circuit & it is proved by the small signal analysis of the circuit which indicates difference mode gain (A_{Vd}) & common mode gain of the circuit (A_{VC}) & it is given by:

$$A_{Vd} = \frac{R2(1+jkf\frac{GB1+GB2}{2GB1.GB2})}{R1(1+\frac{jkf}{GB1})(1+\frac{jkf}{GB2})} \quad \text{(iii)}$$

$$A_{VC} = \frac{R2(1+jkf\frac{GB1-GB2}{GB1.GB2})}{R1(1+\frac{jkf}{GB1})(1+\frac{jkf}{GB2})} \quad \text{(iv)}$$

Where, $k= (1+2R_0/R_1)$, R_0 is the open loop output resistance of the op-amp & GB_1 & GB_2 are the gain bandwidth products of the op-amp1 & op-amp2 respectively.

Equation-iv, indicates that the non-zero common-mode gain is due to mismatch between GB product of op-amp1 & op-amp2. Also, it can be seen that conventional IA with resistor trimming technique approaches same result. From equation-iii, it can be noted that the DC gain of the amplifier is determined by the ratio of R2/R1. Because, there is no-resistor in the feedback path of the op-amp, A_{Vd}, can be varied by varying R2 irrespective in the change of the circuit bandwidth, unlike conventional IA design where GB product is usually constant.

Important technological parameters of CMIA for most of the applications are:

(i) CMRR: It is defined as the ratio of difference mode gain to the common mode gain. By reducing common mode gain CMRR can be increased & ideally it would be infinite. It is very crucial parameter for biomedical system. For physiological signal acquisition, high CMRR is essentially required. Lots of techniques have been introduced to increase CMRR in CMIA. Zhu et. al. [23] introduced the initial modification in CMRR of Toumazou and Lidgey circuit [12] by reducing supply voltage modulation from input op-amp substantially. Circuit shown in [24] further increases the CMRR by common mode bootstrapping technique and it termed as second generation CMIA.

(ii) DC Offset: It is introduced when an IA is used I bio-medical applications. It arises because of electrochemical effect at electrode-body interface. The DC offset signal is large and often associated with recording electrodes [25]. Chopper technique is mainly used to reduce offset and flicker noise that occur in low frequency signals. Here we give a look at nested chopping technique which consist of pair of choppers and results in much lower residual offset. In a conventional CMOS amplifier at high frequencies, the input referred noise will behave as Gaussian noise i.e., thermal noise and at low frequency it is called as flicker noise because as frequency decreases the noise power increases linearly as termed as 1/f noise or flicker noise. 1/f noise corner frequency is defined as the frequency at which flicker noise dominant over thermal noise. In nested chopping technique, the input signal is initial modulated by low frequency signal followed by high frequency and amplified. This amplified signal is then demodulated by pair of choppers by their respective chopping frequencies to the baseband signal with reduced offset and flicker noise. The circuit diagram of chopper technique with IA are shown in [26]. [26][29] gives the detailed description of nested chopper technique. [27-28] shows other offset reduction technique for CMIA.

(iii) Gain: An IA with high is required in bio-medical applications to amplify weak bio-potential signals. All the physiological signals are of weak potential and needed high gain to get extracted out. A CMIA consists of differential difference current conveyors (DDCC) which enhance gain since, it consist of two stage amplifier [30]. It also increases CMRR & reduces offset as the circuit shown in [30] consists of two gain stages and one offset cancellation loop.

IV. Enhanced CMIA

Further enhancement in CMIA are reported in [31-32]. Also different topologies have been used to implement CMIA like OFCC [16], DDCC [30] etc.

(1) CMIA based on ECCII:

[31] proposes electronically controllable CMIA with high frequency performance based on ECCII. In [31] two electronically tunable second generation current conveyors are used and it does not require any passive elements which makes it suitable for IC fabrication. There are lots of CMIA are available based on current mode building blocks [33-37]. The interesting merits about most of the CMIA is that, the CMRR only depends upon the matching of active blocks not on the resistors which can be easily achieved & it also offers better frequency response as compared to the conventional IA's. By using electronically controllable characteristics of CMIA, it is possible to get variable differential mode gain without any external variable resistors and because of this it is suitable for IC fabrication as it requires less chip area. There are certain drawbacks on some electronically controllable CMIA. Considering some examples: the CMIA shown in [33] is implemented using 5- OTAs and tuning of this circuit is achieved by varying OTAs bias current. But because of the circuit uses 5-OTAs, it requires large chip area and results in high power dissipation. [34] shows CMIA based on current controlled current conveyor transconductance amplifier (CCCCTA) which is also electronically controllable & by varying bias current at x-terminal of CCCCTA differential- mode gain varied. This CMIA offers much higher bandwidth compared to most of the CMIA described in literature & also offers high CMRR. Since, the circuit is implemented using BiCMOS technology, it requires high supply voltage & consumes high power. The CMIA shown in [35] is based on three current controlled second generation current conveyors (CCCIIs) & offers very high CMRR. X-terminal impedance of CCCIIs changes to change differential-mode gain. The major drawback is its supply voltage requirement. The electronically controllable CMIA shown in [36] uses current mirrors & an electronically controlled resistor to vary differential-mode gain. It consumes less power and also requires smaller supply voltage and also offers much wider range of bandwidth. The drawback of the circuit is that, since its output signal is voltage & hence an additional voltage buffer circuit is required at the output which increases chip area. [37] uses degenerated current

mirror in its circuit design to control differential-mode gain. The major drawback is its low frequency performance of CMRR.

[31] is highly efficient circuit & it is proposed by Leila Safari and Shahram Minaei and this circuit offers significant advantage over all the above mentioned. Since, this circuit does not require matching within active elements to get high CMRR. It reduces circuit complexity & has higher frequency Performance compared to most of the CMIA. Also the input and output ports of this circuit is having low and high impedances respectively which are essentially needed in current-mode signal processing. Leila et. al. circuit design is described below starting from the existing circuits & mathematical equations. Symbolically ECCII is represented as shown in figure-7.

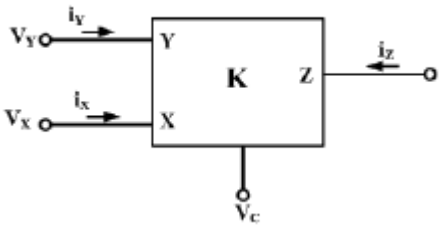

Fig-7: Symbolic representation of ECCII [38].

ECCII is characterized by:

$$V_x=V_y,\ i_Z=K\times i_x,\ i_y=0 \quad (v)$$

As seen from equation-v that, current at z-terminal is K-times x-terminal current where, K is the current gain and can be electronically varied. Since, ECCII can be realized by different topologies as shown in [38-42]. But, there exists some certain serious drawbacks like complicated structure of the circuit and need of compensating floating capacitor [38], there also present low impedance at z-terminal [39] and the need of bipolar technology for implementation of the circuit [40-42]. Also all [38-42] is having complicated internal structure. [31] shows simple and compact structure which is highly suitable for low-voltage & low-power applications. The Leila et. al. circuit is shown in figure-8 [31].

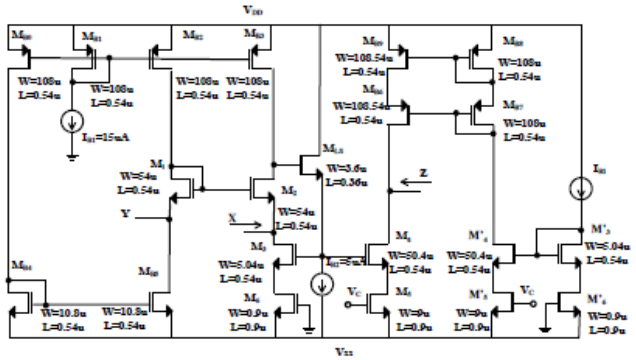

Fig-8: Proposed Leila et. al. ECCII circuit implementation [31]

The analysis gives the input and output impedances as:

$$r_x \approx gm_2^{-1}/\ gmeq(r_{o2}\|r_{oMB3}) \quad (vi)$$

where, r_{oMB3} , r_{o2} and gm_2 are the output impedances of transistor M_{B3}, M_2 and transconductance of M_2 respectively.

The gm_{eq} is also defined as:

$$gm_{eq}= gm_3/\ 1+ (gm_3 x r_{DS6}) \quad (vii)$$

Current gain can also be found as [37]:

$$K=(gm_4/gm_3)x((1+gm_3 x r_{DS6})/\ (1+gm_4\, x r_{DS5})) \quad (viii)$$

Also,

$$r_{DS5} = 1/\mu C_{OX}(W_5/L_5)(V_c-V_{SS}-V_{THN}) \quad (ix)$$

&

$$r_{DS6} = 1/\mu C_{OX}(W_6/L_6)(-V_{SS}-V_{THN}) \quad (x)$$

The Leila et. al. CMIA is shown in figure-9.

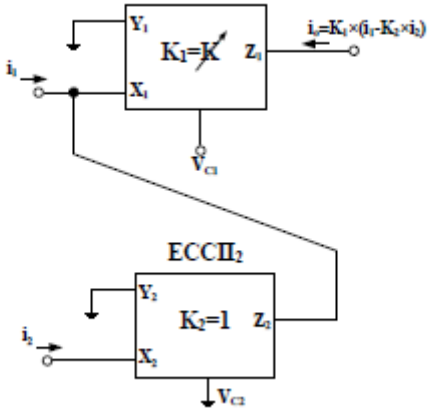

Fig-9: Leila et. al. CMIA [31]

The output current of [31] is given by:

$$Io= K_1\times(I_1-K_2\times I_2) \quad (xi)$$

K1 & K2 are the current gain of 1st & 2nd ECCII respectively.

For common mode input, we have $I_1=I_2=I_{CM}$, and therefore, the common mode gain of [31] is given by:

$$A_{CM}= Io/I_{CM}= K_1\times(1-K_2) \quad (xii)$$

The current gain of 2nd ECCII is chosen close to unity & can be expressed as:

$$K_2=1-\varepsilon i \quad (xiii)$$

Where, $\varepsilon i<<1$.

By equating equation-(xiii) in (xii), common mode gain found to be

$$A_{CMO}= K_1\times\varepsilon i \quad (xiv)$$

For differential mode input, we have $I_1=-I_2=I_{dm}/2$, and by using equation- (xi), differential mode gain is given by [31]:

$$A_{dm}=Io/I_{dm}=K_1\times(1/2+K_2/2) \quad (xv)$$

From equation- (xiii) & (xv),

$$A_{dm}= K_1 \times (1-\varepsilon i/2)\approx K_1 \quad (xvi)$$

Therefore, CMRR is defined as:

$$CMRR= A_{dm}/A_{CM}\approx 1/\varepsilon i \quad (xvii)$$

From CMRR equation, it can be seen that, to get high CMRR, current gain of second ECCII should close to unity instead of matching between active building blocks. The deviations of current gain of second ECCII is due to mismatch between transistors and can be compensated by its control voltage.

(2) OFCC based CMIA: the OFCC is a five terminal network having two input & three output ports as shown in figure-10 [16].

OFCC is described as, the port-X is low-impedance current input port & port-Y is a high impedance voltage input port. W is a low impedance voltage output port and Z+ & Z- are the high impedance current outputs having opposite polarities. OFCC used in CMIA as a basic building block. Since OFCC is a current mode device hence, it offers flexible properties with respect to the other current mode or voltage

mode devices. Some of the main advantages of this CMIA are listed below:

Fig-10: Block diagram of OFCC [16].

(a) It has higher differential- mode gain & gain independent bandwidth.
(b) It offers high CMRR without resistor matching.
(c) It also offers significant improvement in accuracy compared to other CMIA based on current conveyors.
(d) It requires less number of active building blocks.

Starting with basics of CMIA, figure-11 shows the basic CMIA based on CCII+ [22].

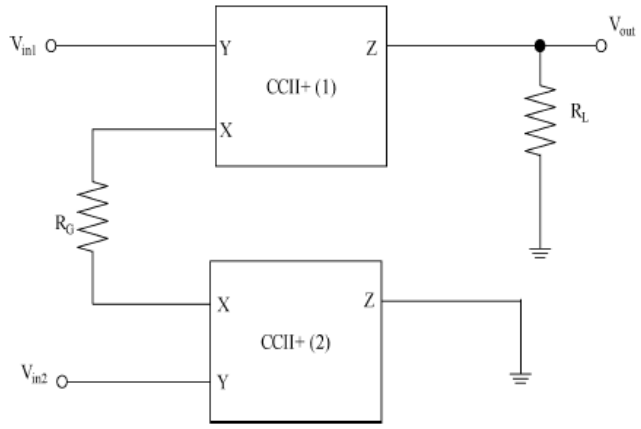

Fig-11: Wilson's CMIA [22].

The frequency dependent differential-mode gain is given by:

$A_d(s)= Vo/(V_{in1}-V_{in2})= (R_L/ (R_G-2R_X))\cdot(1/(1+sCR_L))$ (xviii)

Where, Rx is the input resistance at the X-terminal. R_G is gain setting resistor. C is the effective output capacitance of the CCII+ and R_L is the load resistor.

The main purpose of using CCII+ is that it offers high CMRR without resistor matching & it also presents simple and symmetrical circuit topology. Further enhancement in CMRR & differential- mode gain can be achieved by connecting three CCII+ as shown in figure-12 [43].

The differential-mode gain of [43] is given by:
$A_d(s)= Vo/(V_{in1}-V_{in2})= (2R_L/ (R_G+2R_X))\cdot(1/(1+sCR_L))$

(xix)

From equation (xviii) & (xix), it cn be noted that the differential-mode gain is inversely proportional to Rx. Since, the accuracy of CMIA is limited by the tolerance of Rx, which is low. To improve the accuracy of the CMIA, two op-amps are used along with two CCII+ as shown in figure-13 [44].

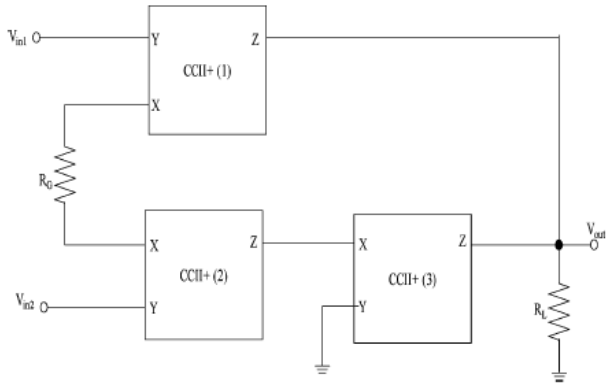

Fig-12: CMIA based on 3-CCII+ [43].

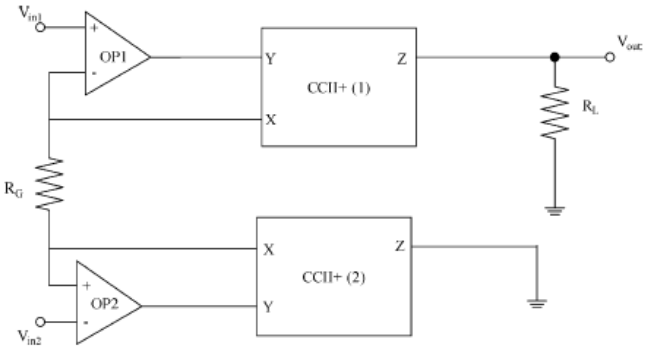

Fig-13: CMIA based on op-amps & CCs [44].

The differential mode gain of [44] is given as:
$A_d(s)= Vo/(V_{in1}-V_{in2})= (R_L/ (R_G)\cdot(1/(1+(s\tau/(1+K\beta))))$ (xx)

Where, $\beta= R_G/(2R_X+R_L)$, R_L is the load resistance, τ ie time constant & K is the low-frequency gain. K-in this case is independent of Rx but, bandwidth is still dependent on Rx.
The drawback of this topology is that, it consumes more power & has complicated circuit topology when compared with the circuit shown in figure-11 & 12. The CMIA based on OFCC has combined advantage of all these above topologies. It has improved differential-mode gain, bandwidth & CMRR. Also it has high accuracy. The transmission matrix of ideal OFCC is shown below:

$$\begin{bmatrix} i_y \\ v_x \\ v_w \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ i_w \\ v_{z+} \\ v_{z-} \end{bmatrix}$$

From above matrix, it can be seen that the OFCC operates where the input current at port-X is multiplied by the open loop transimpedance gain- Zt to produce output voltage at port-W. The input voltage at port-Y appears at port-X & thus, a voltage tracking property exists at the input port. Output current flowing at port-W is transferred in phase to port Z+ & out of phase with that current flowing into port Z-. Hence, in this case current tracking action exists at the output ports. From transmission matrix it can be seen that, the i_y & v_y are the inward current and voltage at Y-terminal respectively and i_x & v_x are the input current and voltage at X-terminal respectively. Also, i_w & v_w are the output current & voltage at w-terminal respectively. i_{z+} & v_{z+} are the output current & voltage at Z+ respectively. likewise, iz- & v_{z-} are the output current & voltage at the Z-terminal respectively. Zt indicates the impedance between X & W terminals.

The OFCC can be implemented by applying the principle of supply current sensing to a current feedback op-amp [45] as shown in figure-14 [16].

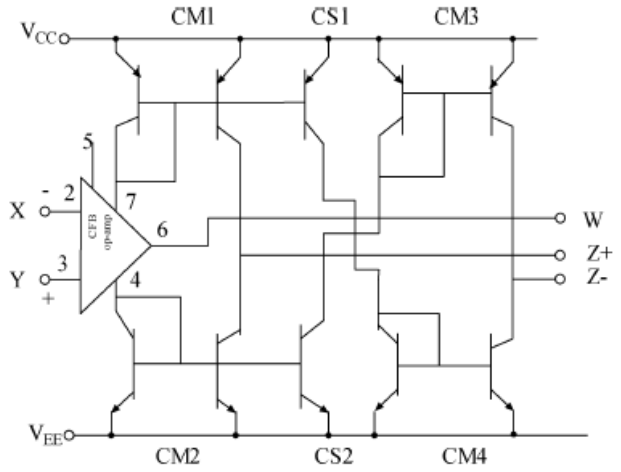

Fig-14: Circuit scheme of OFCC [16].

The current mirror CM1 & CM2 establish the output current at port-Z+. also, CM1 & CM2 with their cross coupling with the current mirror CM3 & CM4 through the current steering transistor CS1 & CS2 generate a complementary output current at port Z-. The OFCC is basically designed to be used in a closed loop configuration with current being fed back from port-W to port-X.

Yehya H. Ghallab et. al. CMIA based on OFCC is shown in figure-15 [16].

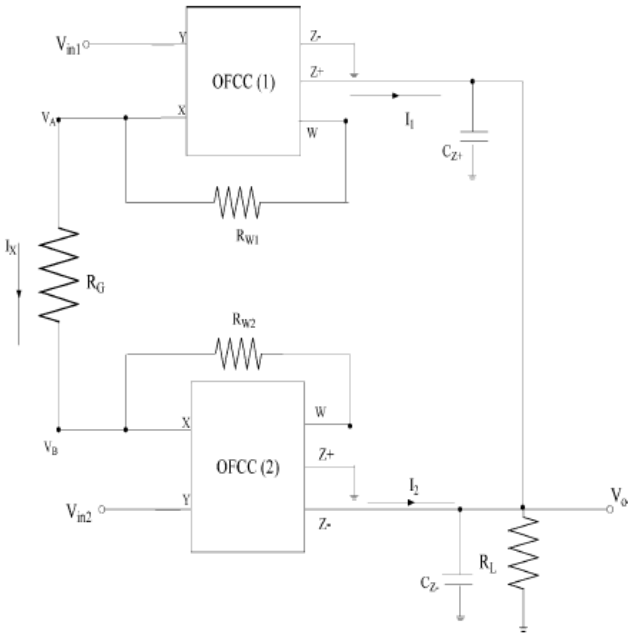

Fig-15: Yehya H. Ghallab et. al CMIA based on OFCC [16].

The circuit of figure- 15 consists of two feedback resistors (R_{W1} & R_{W2}), a gain determined resistor (R_G) and a load resistor (R_L).

After analysis, the differential- mode gain is given by:

$A_d(s)= Vo/(V_{in1}-V_{in2})= (2R_L/ R_G(1/(1+sC_2R_L))$ (xxi)

From equation-(xxi), it can be seen that, A_d can be varied by varying R_G without affecting bandwidth of the CMIA and the bandwidth can be controlled by C_2R_L.

So, by using this circuit, we get high CMRR & high differential mode gain.

(3) CMIA based on DDCC: Ugur Cini et. al. presented a CMIA based on DDCC (Differential Difference Current Conveyors) element which is having high CMRR, high differential-mode gain & low offset and this amplifier is especially suitable for AC coupled measurement. Also, it provides high output swing. Here, in [30] Ugur Cini et. al. included the general mismatch between transistors used in CC's at the differential input stage during simulation which is major cause of limited CMRR in differential amplifier.

In [30], CMIA is implemented using DDCC element. DDCC is a three input, two output terminal current conveyor that provides algebraic operations of the input transferred to the output. The ideal DDCC element is characterised as shown in matrix below:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix}$$

An improved internal structure of DDCC stage is presented that provides the ideal specification of DDCC element. Ideally, DDCC element is having low impedance at X-node & high impedance at Z-node. Also, precise current copying characteristics from node-X to node-Z is essentially required. Internal structure of DDCC is shown in figure-16 [30].

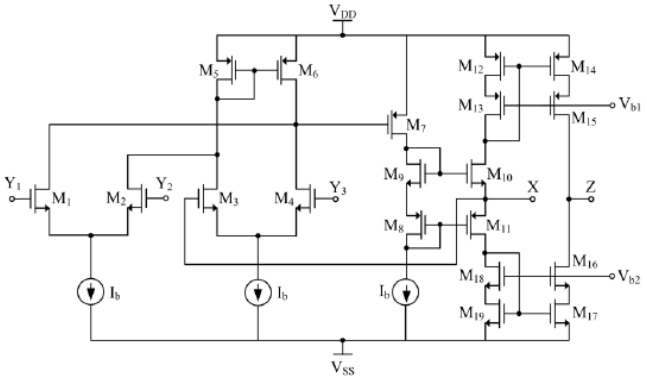

Fig-16: Internal structure of DDCC [30].

The structure provides near rail to rail output swing.

The two basic amplifier based on DDCC topologies are shown in figure-17 and figure-18 [30].

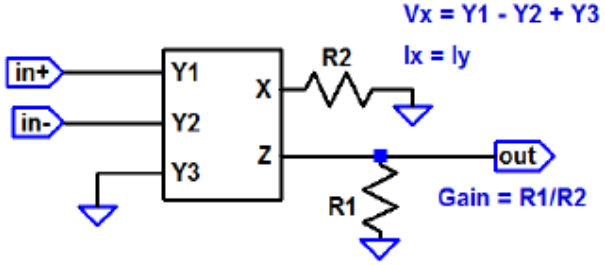

Fig-17: Basic differential amplifier using single DDCC [30].

The amplifier shown in figure-18 has similar properties as Wilson CMIA shown in Figure-11 with higher gain. The voltage gain of figure-18 is given as:

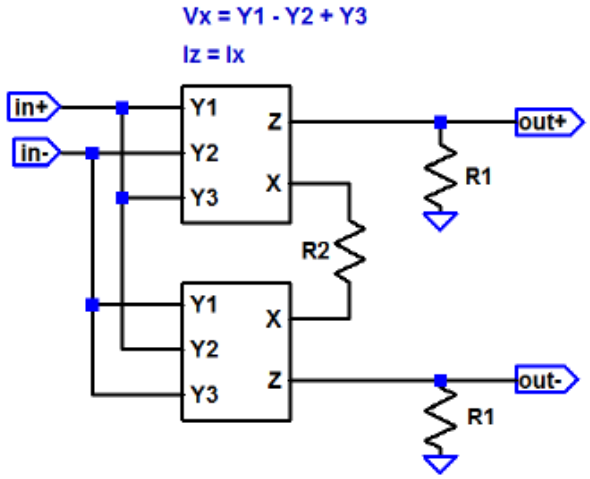

Fig-18: basic IA based on DDCC [30].

$V_{OUT+} = V_{Z1}=I_{Z1}R_1= 3R1/R2(V_{in+} V_{in-})$ and,

$V_{OUT-} = V_{Z2}=I_{Z2}R_1= -3R1/R2(V_{in+} V_{in-})$ (xxii)

The amplifier shown in figure-17 consists of single DDCC. This circuit exhibits lower CMRR whenever transistor mismatch exists which occurs inevitably in the differential input. In this case the gain equation can be written as:

$V_{OUT+} = R1/R2(V_{in+}V_{in-})$ (xxiii)

The high gain & high CMRR IA is designed using tqo of the differential amplifier given in figure-17 & 18. The Ugur Cini CMIA is shown in figure-19 [30]. It consists of pre- amplifier stage, second amplifier stage & offset cancellation loop.

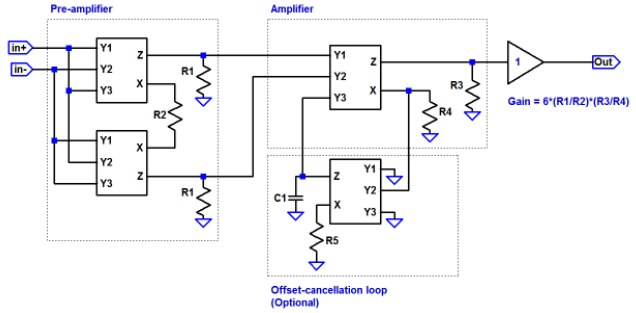

Fig-19: Ugur Cini et. al, CMIA [30].

The CMIA in figure-19, the pre-amplifier stage has low gain & used in the circuit to remove common-mode signals & differential outputs without common mode signal presents at the output of the pre amplifier. The second stage is a simple differential amplifier stage which subtracts the two differential outputs of pre-amplifier stage. The overall gain of this CMIA is given by:

$V_{OUT} =6\{R1\cdot R3/R2\cdot R4\}\cdot(V_{in+} V_{in-})$ (xxiv)

The overall gain shown in above equation- xxiv is the combination of equation-xxii & xxiii. Though the common mode-input voltage is suppressed there still exists some residual offset which may cause saturation of the output stage. To remove the residual output, an integrator based feedback stage is included in the second amplifier stage. The integrator act as a low-pass filter & integrates the output voltage and subtracts the accumulated offset voltage present from the input.

(4) A noval COA based electronically adjustable CMIA topology: Leila Safari & Shahram Minaei proposed a new topology for implementing electronically controlled CMIA. It is based on two single input and multiple output (SI-MO) current operational amplifier (COA) act as basic building block along with two resistors. For electronically controlled differential mode gain, a transistor is biased in triode region which act as variable resistor. The important feature of this circuit is that, it operates in closed loop configuration and therefore, it offers improved frequency performance, low total harmonic distortion (THD) and very low input impedance. Also, it has fully differential output which reduces the effect of noise at the output and increase number of applications. Most of the previously reported work on CMIA have two major drawbacks:

(a) Most of the IA having input and/or output are voltage signals however, in modern technologies, due to scaling in supply voltages, very limited voltage room is available. Thus, voltage input and voltage output CMIA's have the same drawbacks of Conventional voltage mode IA in terms of dynamic range & output voltage swing.

(b) Even if, the CMIA achieves differential-mode gain independent of bandwidth, the CMRR frequency response degraded.

In this paper [46] Leila et. al., presents a current input- current output CMIA which is capable of providing higher -3dB bandwidth for both differential-mode gain & CMRR. The input & output signals of this Leila et. al., CMIA are current signals & its voltage swing is negligible at the input and output terminals and making it suitable for low-voltage applications. Also this topology has fully differential output.

Circuit topology: The proposed CMIA is based on the concept stating that each voltage processing circuit can be replaced by the current processing counterpart by changing voltage op-amp with their current-mode ad joint element i.e., COA's and interchanging the input & output terminals of the circuit [47-49]. The design approach discussed in [47-49] is used here. However, to boost the DC value of differential-gain and CMRR of CMIA, instead of using single input differential output COA, single input multiple output is employed & by cross connecting the extra outputs, DC value of differential gain & CMRR enhanced.

Figure-20 shows the symbolic representation of (a) conventional voltage op-amp and (b) COA as its current mode ad joint.

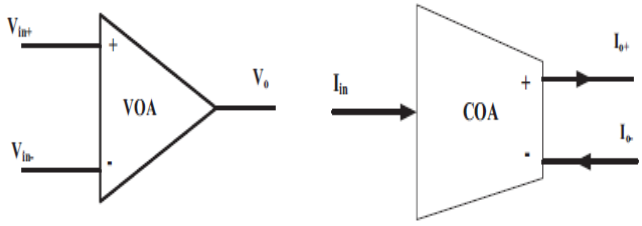

Fig-20: symbolic representation of (a) conventional voltage op-amp and (b) COA as its current mode ad joint [46].

Figure-21, shows the symbolic representation of SI-MO COA. Ideally, it has zero input impedance, infinite open loop gain and infinite output resistance.

It has four output's & the relation between input and output currents can be given as:

$$i_{01}+ = i_{02}+ = i_{01}- = i_{02}- =Ao \times i_{in}$$ (xxv)

The Leila et. al., CMIA is built by replacing voltage op-amp in voltage mode operational amplifier shown in figure-5 with a multiple output COA & interchanging the input and output ports of the circuit as shown in figure-22.

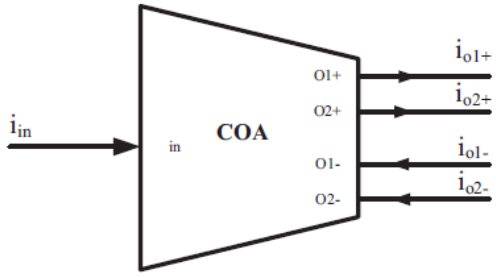

Fig-21: Circuit symbol of SI-MO COA [46].

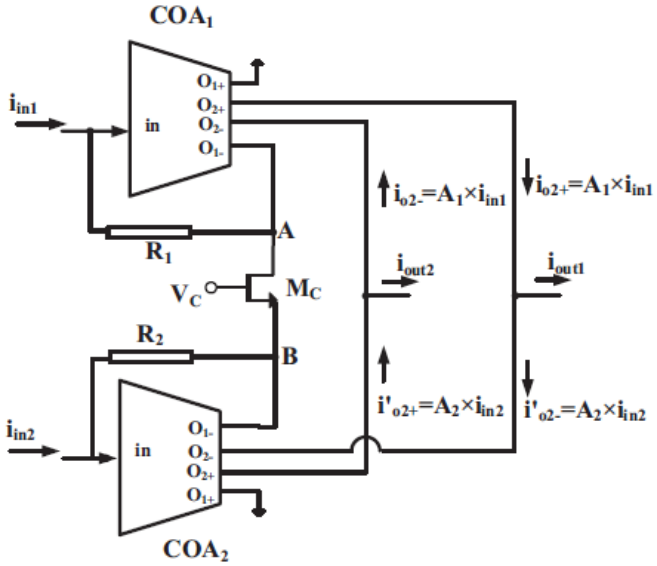

Fig-22: Leila Safari & Shahram Minaei COA CMIA [46].

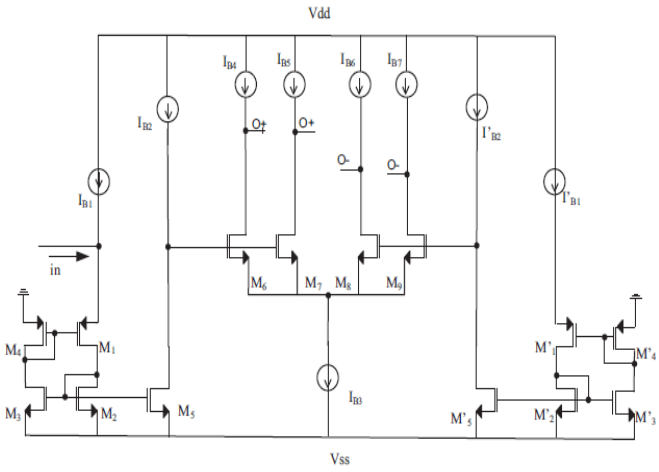

Fig-23: Simple implementation of SIMO COA [46].

The CMIA shown in figure-22, uses two SI-MO COA's & two resistors R1 & R2. A MOS transistor is operating in triode region for electronically adjust differential-mode gain and act as variable resistor. Extra outputs of SI-MO COA is used to attenuate common-mode inputs & amplify differential-mode gain. One of the negative output of COA's is used to create negative feedback loop and the other negative output of COA_1 is cross connected to the positive output of COA_2. Alike, the negative output of COA_2 is cross connected to the positive output of COA_1 as shown in above figure-22. The cross connections used in the above CMIA allows adding up differential mode signals & subtracting common-mode signals at the output nodes and the rest unused positive outputs of COA's are grounded. From above figure-22, it can be seen that, i_{in1} & i_{in2} are the input currents. The negative and positive output of COA_1 are shown as i_{oi}- & i_{oi}+ respectively where, i =1, 2 is the number of outputs. Similarly, negative and positive output of COA_2 are shown as i_{oi}'- & i_{oi}'+ respectively. the following equations hold for both of the COA's:

$$i_{01}+ = i_{02}+ = i_{01}- = i_{02}- = A_1 \times i_{in1} \quad \text{(xxvi)}$$

$$\&,\ i'_{01}+ = i'_{02}+ = i'_{01}- = i'_{02}- = A_2 \times i_{in2} \quad \text{(xxvii)}$$

Where, A_1 and A_2 are the closed loop current gain of COA_1 & COA_2 respectively.

Though, similar to conventional Voltage mode IA, circuit behaves differently for common-mode & differential-mode inputs.

After simple calculation, common-mode gain is given by:

$$|Ac| = 2\cdot\Delta A \quad \text{(xxviii)}$$

Where, ΔA is the mismatch gain between the two COA's.

From equation (xxviii), it can be noted that the common mode gain of this CMIA is very small and results in very high attenuated common-mode current at the output. It is also noted that, the common mode analysis done to derive the formula is in ideal condition. By considering practical values of the impedances and open loop current gain, the common-mode gain will be higher than the given in equation (xxviii). Due to negative feedback topology, the common-mode input impedance of this CMIA is very small and hence voltage swing at the input nodes will be negligible even for large common-mode input currents and therefore, high voltage swing at the input ports are not required.

For differential-mode gain, assuming R1=R2=R, and therefore differential–mode gain is given by:

$$|Ad| = (1+ 2R/Rc) \quad \text{(xxix)}$$

Where, Rc is the equivalent resistance of Mc.

And the CMRR of this CMIA is given by:

$$CMRR = (1+ 2R/Rc)/ 2\Delta A \quad \text{(xxx)}$$

The Leila Safari and Shahram Minaei CMIA [46] provides better -3dB bandwidth compared to most of the counterpart and is operated on less supply voltage i.e., ±0.9V and hence consumes less power. The drawback is that passive resistors used in the circuit requires laser trimming to maintain high CMRR like its voltage-mode counterpart & better result is expected from high performance COA's as the achieved result is not optimum.

V. Conclusion and Future Scope

CMIA plays important role in many applications. It offers high CMRR which is essentially required in bio-medical applications. CMIA based on CC offers variable mode gain & requires less chip area. In this paper CMIA with different topologies are discussed. All the important parameters of an IA and there enhancement techniques are discussed. The recent advances in CMIA are also described with mathematically governed equations in there support. The merits of the recent advanced CMIA are discussed like high and variable differential mode gain, high CMRR, high bandwidth, accuracy, low power consumption, number of active component used in the circuit so as to reduce chip area, low offset etc. The transistor mismatch used in active building block are need to be investigated further. From [31] discussed above, it is concluded that, it offers higher frequency response and -3dB differential mode gain but, current gain of ECCII deviates due to transistor mismatching which degrades CMRR and can be compensated by control signal which

increases the complexity of the circuit as the circuit uses compensating floating capacitor. From [16] it is concluded that, it offers gain independent bandwidth but the drawback it has complicated OFCC structure. Further investigation is done to reduce the complexity of OFCC in [50] and it offers better result in terms of CMRR and -3dB frequency but the limitations is [50] is voltage mode IA so, for OFCC of [50] need to be investigated in current mode. [30] offers high CMRR and bandwidth and it is suitable for general purpose differential amplification where high gain & bandwidth together is required. The drawback is that it uses four DDCC elements and one buffer amplifier which increases total layout area and therefore, it not suitable for bio-medical applications. For bio-medical applications using DDCC, OFCC etc. further miniaturization is essentially required. And from [46] it is concluded that, it offers better frequency response and gain independent bandwidth. Also [46] offers frequency tuning using single MOS transistor operating in triode region, also it has multiple output that might be used for different applications. The drawback of [46] is that, CMRR degrades due to the use of passive resistor used in the circuit since, resistor trimming is required like voltage mode circuits. Further investigation is required to enhance the performance of COA's for optimum result.

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FGMOS based Two Stage Operational Amplifier and its Applications

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Abstract: Operational amplifier is one of the very crucial block in anolog engineering. An analog design engineers have been using this block to design lots of analog applications like filters, circuits that can perform mathematical operations like multiplication, division, log circuits, antilog circuits etc. It is very important block for bio-medical engineering, as it is used in the design of instrumentation amplifier. In this paper FGMOS is used to design two stage operational amplifier. The simulation work is carried out in virtuoso 90nm process. A technological parameters are charted out in this paper for FGMOS based two stage op amp. The advantage of using FGMOS in the design is that it offers very high phase margin of 73 degree and has a unity gain bandwidth of 30 MHz. It also requires less supply voltage than that of conventional CMOS two stage op amp and has threshold voltage tuning capabilities.

Keywords: CMOS, UGB, PM, FGMOS, MIFG, CMRR, PSRR, SR, Instrumentation Amplifier.

I. Introduction

The basic requirement of two stage operational amplifier (op amp) is in analog circuits. It is used in positive feedback to generate square waveform of pulse signal that are generated from Schmitt trigger, monostable multivibrator etc. whereas in negative feedback it is used as an amplifier or used in voltage regulator circuits and has many applications like arithmetic circuits etc. The main concern of this device is that, it must operate on smaller supply voltage that will result in longer device life for a battery power devices. As silicon technology is continuously scaled down to meet industry demand, more and more chip is fabricated on the same IC. As the large number of chip is fabricated in an IC, supply requirement has increased and hence, to deal with this problem, there is a need of a circuit which can operate at smaller supply voltage. The possible solution is, designers are starts designing circuits that can operate at weak inversion region that is in sub-threshold region where the supply voltage requirement is considerably small & hence power dissipation is also low. The other possible solution to deal with the problem is that a certain modification is required in basic circuits. Here, FGMOS is a modified version of MOS transistor. FGMOS transistor is the possible solution for that in which threshold voltage decreases significantly and hence supply voltage requirement decreases and also power dissipation. Because of coupling capacitor at the gate of multi input FGMOS, charges gets stored in that which results in significant change in threshold voltage. The FGMOS is having multiple input and hence, one can vary threshold voltage by varying one of the input voltage and by keeping rest at some fixed DC voltage. In this paper some applications of op amp based on FGMOS is shown. Op amp based on FGMOS already exist in literature. Here, in this paper some modification has done & reported. This paper also includes a comparative study between existing topology with technological parameters and technological parameters of this paper.

This paper is organised as follows. Section I provides an introduction to the topic. Section II presents conventional two stage op amp. FGMOS based op amp is described in Section III and its applications is described in Section IV. The Conclusion and Future scope is presented in Section V.

II. Conventional Two Stage Operational Amplifier

A conventional two stage op amp is discussed in this section. It is a cascade connection of two stage in which first stage is differential amplifier stage and second stage is common source gain stage. The overall gain of the circuit is given by the multiplication of both the stage. Figure 1 shows below is a conventional two stage op amp. In this a nulling resistor is used in cascade with coupling capacitor. Nulling resistor is used to nullify the effect of zero from transfer function and hence, phase margin of the circuit increases. Generally, phase margin of a circuit is used to show its stability. In two stage op amp for a circuit to be stable, its phase margin is need to have phase margin in between 45 to 60 degree. 60 degree phase margin indicates less ringing of signal i.e., transient die out early and hence system takes less time to become stable. Coupling capacitor is used in the circuit that shifts second pole of the circuit away from first pole and hence unity gain bandwidth (UGB) increases. From the circuit shown below in figure 1, it can be seen that, first stage consists of five MOS transistors and second stage consists of two MOS transistors. Coupling capacitor and nulling resistor Rz is used to connect first stage and second stage.

Transistor M1 to M5 & M8 is used in first stage of op amp which is a differential stage that amplifies the difference between two inputs shown as Vin- & Vin+. Transistor M5 and M8 is used to provide biasing current to the circuit. Transistor M1 and M2 is used to form a differential input stage and M3 as well as M4 is used as an active load which is a PMOS transistor and forms a current mirror. The output of this stage is given to second stage which is a common source stage consists of transistor M6 & M7. First stage introduces a pole in the transfer function and represented by P1. Also, pole due to second stage is represented by P2. As current through M6 & through Cc and Rz will added up and this will result in a zero in the transfer function. This zero is represented as Z1. And hence P1 does not has significant impact on phase margin and UGB and hence can be left out. The P2 and Z1 are the main design constraint and are given below:

$$P2=\frac{-gm6}{CL} \quad (1)$$

$$Z1=\frac{gm6}{Cc} \quad (2)$$

The design equations of two stage op amp from [1] is given below:

$$A_V=\frac{gm1gm6}{(gds2+gds4)(gds6+gds7)} \quad (3)$$

$$SR=\frac{I5}{Cc} \quad (4)$$

$$GB=\frac{gm1}{Cc} \quad (5)$$

Positive ICMR: $V_{in(max)} = V_{DD}- \sqrt{(I_5/\beta_3)} - |V_{T03}|_{(max)} + V_{T1(min)}$ (6)

Negative ICMR: $V_{in(min)} = V_{SS} + \sqrt{(I_5/\beta_1)} + V_{T1(max)} + V_{DS5(sat)}$ (7)

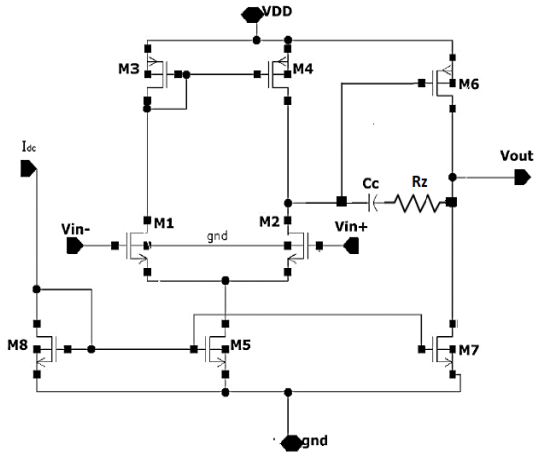

Figure 1: Conventional two stage op amp [1].

III. FGMOS based Two stage Operational Amplifier

FGMOS transistor is similar to standard MOS transistor but, it does not have any resistive connection at the gate i.e., gate of FGMOS is capacitively connected. A FGMOS has multiple inputs and hence called as multiple input floating gate (MIFG) transistor. Double poly is used in the fabrication of MIFG transistor, in which first poly is used for floating gate whereas second poly is used as for control gate. As there is no DC path to ground for MIFG transistor, it leads to change the DC characteristics of standard MOS significantly. Figure 2 shows the symbol of N-type MIFG transistor.

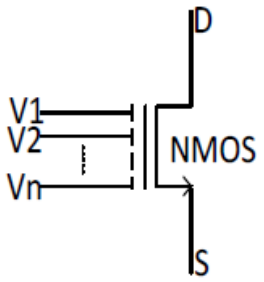

Figure 2: MIFG transistor symbol [2].

From figure 3, we can say that, floating gate voltage is the weighted sum of all the voltage connected at the gate [4].

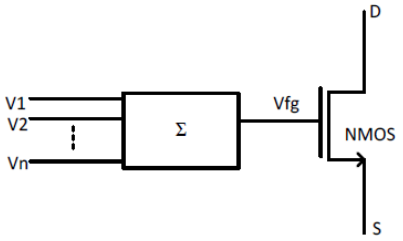

Figure 3: Equivalent circuit for floating gate transistor [3].

The floating gate voltage from [3] is given by:

$$V_{FG}=\sum_{i=1}^{N}\frac{CiVi}{CT}+\frac{QFG}{CT} \quad (8)$$

$$C_T=\sum_{i=1}^{N} Ci + Cgs + Cgd \quad (9)$$

Further from assume that the net charge at floating gate is zero, hence, voltage at floating gate is given by:

$$V_{FG}=\frac{C1V1}{CT}+\frac{C2V2}{CT}+\frac{C3V3}{CT}+\text{-------}+\frac{CnVn}{CT} \quad (10)$$

If FGMOS is biased in saturation region, the current equations can be written as:

$$I_D = \mu_N C_{OX} \cdot \frac{W}{2L}(V_{FG}-V_T)^2 \quad (11)$$

By assume zero Q_{FG} and replacing V_{FG} in Equation (3.1), will result in

$$I_D = \mu_N C_{OX} \frac{W}{2L}(\sum_{i=1}^{N} \frac{CiVi}{CT} - V_T)^2 \quad (12)$$

$$I_D = \mu_N C_{OX} \frac{W}{2L} \beta (\sum_{i=1}^{N} Vi - (\frac{CT}{Ci})V_T)^2 \quad (13)$$

$$I_D = \mu_N C_{OX} \frac{W}{2L} \beta (\sum_{i=1}^{N} Vi - V_{THFG})^2 \quad (14)$$

Where,

$$\beta = \sum_{i=1}^{N}(\frac{Ci}{CT})^2 \text{ and, } V_{THFG} = \sum_{i=1}^{N}(\frac{CT}{Ci})V_T$$

As it can be seen that the threshold voltage of FGMOS is a function of capacitance ratio and hence it can vary depending on total capacitance to the input capacitance.

From above equations (14), it can also be seen that, drain current of FGMOS is a function of the capacitor ratio and it is the ratio of effective input voltage to the total capacitance at the gate.

If we assume that, V_1 is the effective input, then, the drain current can be written as:

$$I_D = \mu_N C_{OX} \frac{W}{2L} \beta(V_1 - (\frac{CTVT}{C1} - \frac{C2V2}{C1} - \frac{C3V3}{C1} - \cdots - \frac{CnVn}{C1}))^2 \quad (15)$$

In this case, $\beta = (\frac{C1}{CT})^2$

Also, threshold voltage is given by:

$$V_{THFG} = (\frac{CTVT}{C1} - \frac{C2V2}{C1} - \frac{C3V3}{C1} - \cdots - \frac{CnVn}{C1}) \quad (16)$$

And hence,

$$I_D = \mu_N C_{OX} \frac{W}{2L} \beta(V_1 - V_{THFG})^2 \quad (17)$$

Equation (17), indicating the drain current of MIFG can be controlled by single input V_1 applied at the gate.

The overall gain of the MIFG op amp decreases when compared with conventional op amp due coupling capacitance factor. Also, overall gm-decreases and given by [4]:

$$gm_i = \frac{Ci}{CT} \cdot gm^* \quad (18)$$

Where, i= 1, 2, ------, N & gm* is the trans-conductance seen from the floating gate.

Where, Ci are the input capacitors connected at the gate, C_{gs} & C_{gd} are the parasitic capacitors.

The drain current characteristics of FGMOS and standard MOS transistor is shown in figure 4.

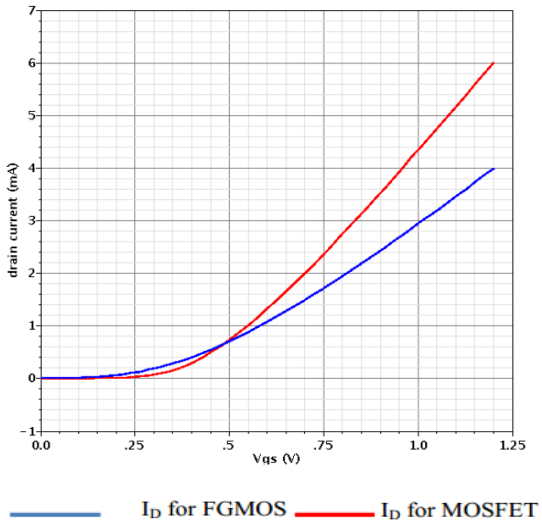

Figure 4: A comparison between standard MOS and FGMOS drain currents.

Two stage FGMOS based op amp is shown in figure 5.

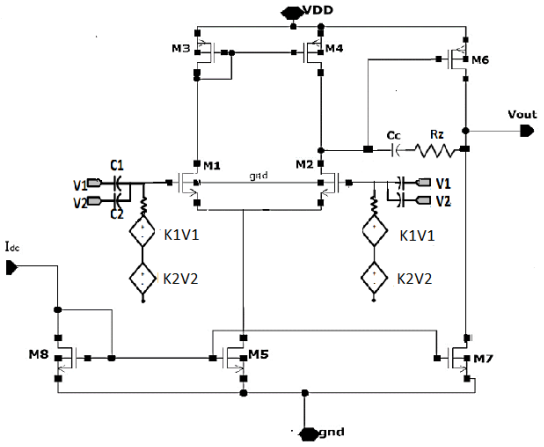

Figure 5: FGMOS based op amp with DC path to ground.

In above circuit shown in figure 5, to resolve convergence problem, a DC path to ground is connected [2]. This path is formed by a large value resistance in series with voltage controlled voltage source. Where K1V1 & K2V2 representing voltage controlled voltage source. K1 & K2 represents capacitance ratio i.e., input capacitance to total

capacitance of path V1& V2 respectively. Also, V1 & V2 are the bias voltages.

The gain and phase plot of two stage op amp is shown in figure 6.

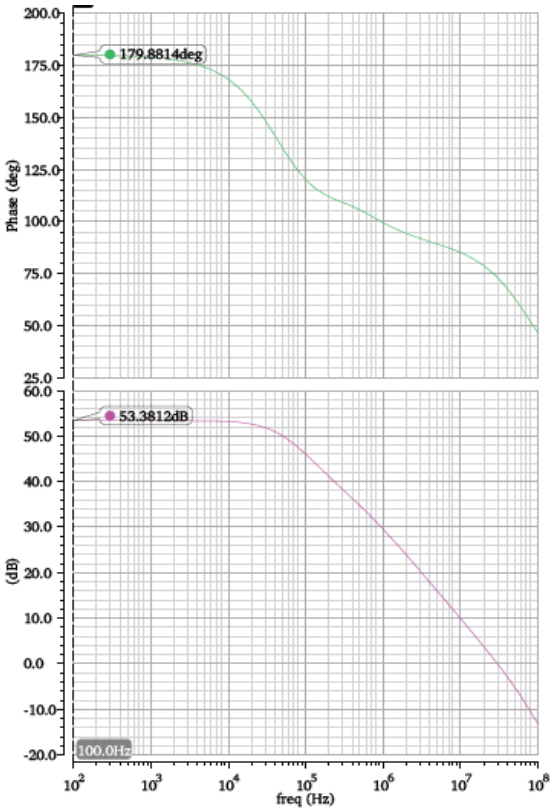

Figure 6: Gain and phase plot of FGMOS based two stage op amp.

The phase margin and UGB plot of FGMOS based two stage op amp is shown in figure 7. Also, the CMRR plot of this op amp is shown in figure 8.

From figure 6, it can be noted that, this op amp has a gain of 53.3 dB and having phase margin of 73 degree as UGB of 30 MHz as shown in figure 7. The CMRR of this op amp is 93.9 dB. All the technological parameters is charted out in table 1.

S. No.	Parameters	Values
1.	DC Gain	53 dB
2.	Maximum Phase at 100 Hz	179.8 degree
3.	UGB	30 MHz
4.	Phase Margin	73 degree
5.	ICMR-	0.4 V
6.	ICMR+	1 V
7.	CMRR	93.9 dB
8.	Common mode voltage	0.6 V
9.	Supply Voltage	1.35 V
10.	Power Dissipation	290 uW

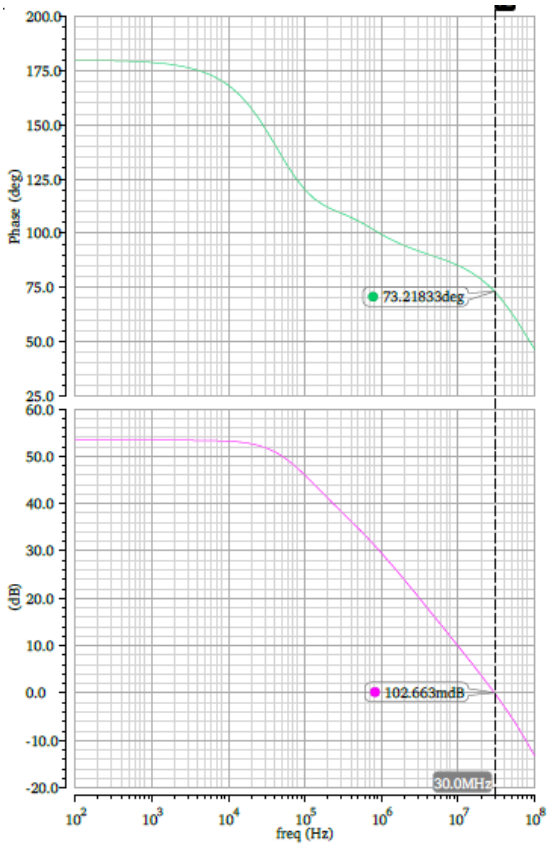

Figure 7: Phase margin & UGB plot of FGMOS based two stage op amp.

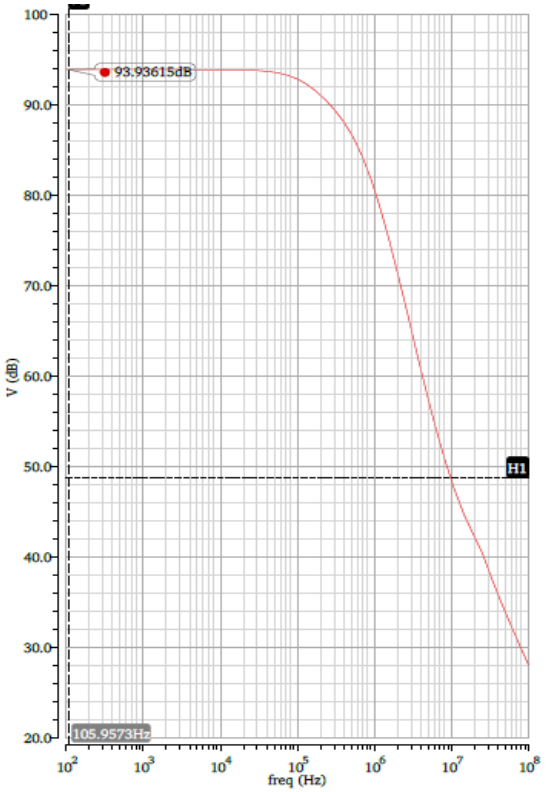

Figure 8: CMRR plot of FGMOS based two stage op amp.

IV. Applications of FGMOS based op amp

In this section, some applications of FGMOS is discussed. This are:

(i) Inverting Amplifier: An amplifier in which output signal is an inverter form of given input signal.

$$\text{Vout} = \frac{-Rf}{R} \cdot \text{Vin} \qquad (19)$$

Where, R_f is the feedback resistance and R is the series resistance.

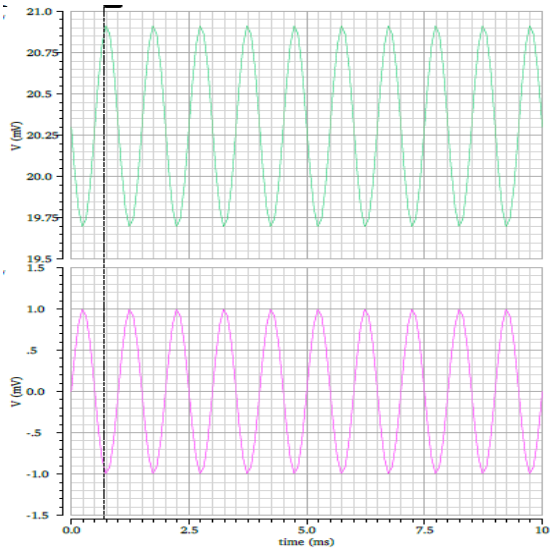

Figure 9: Plot of inverting amplifier.

(ii) Non inverting amplifier: In this output remains in phase with respect to input signal.

$$\text{Vout} = \left(1 + \frac{Rf}{R}\right) \text{Vin} \qquad (20)$$

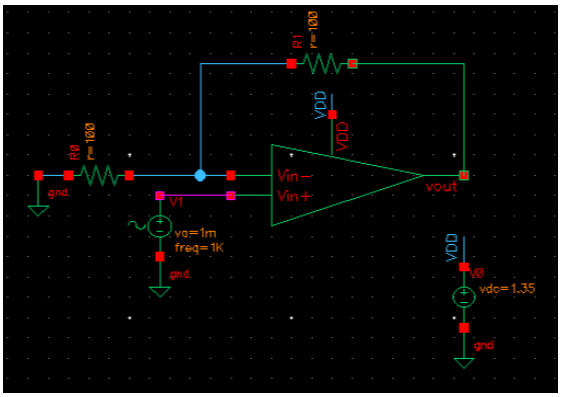

Figure 10: Non-inverting amplifier.

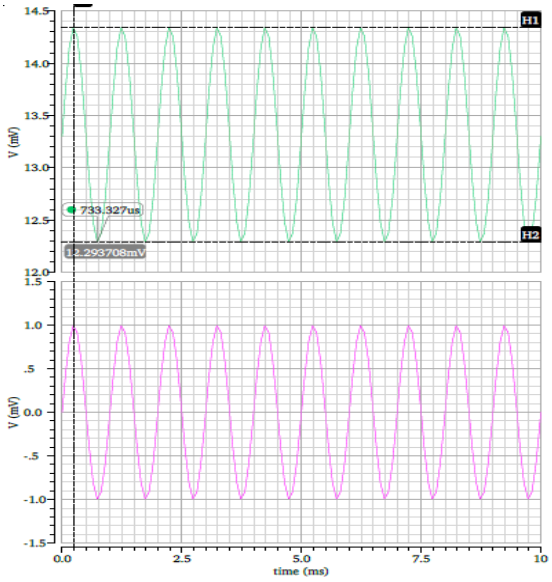

Figure 11: Plot of non-inverting amplifier.

(iii) Differentiator circuit: This circuit will differentiate the input signal. The mathematical equation of this circuit is given by:

$$\text{V}_{\text{out}} = \frac{-RCdVin}{dt} \qquad (21)$$

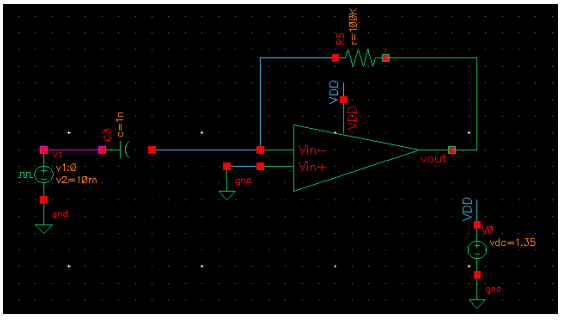

Figure 12: Differentiator circuit.

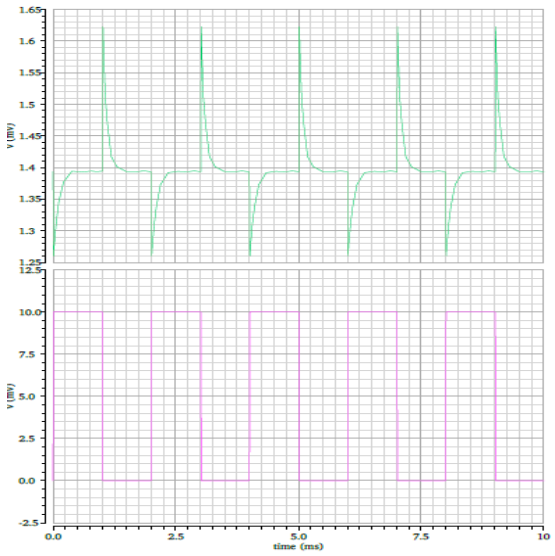

Figure 13: Output and input signal of differentiator.

V. Conclusion and Future Scope

In this paper, a modified version of FGMOS is studied. A DC path to ground is connected to resolve the convergence problem. This paper provides very high phase margin of 73 degree that means highly stable system. The power dissipation is significantly less than that of conventional op amp. This circuit is suitable for low power portable devices. One can design more circuits based on this topology in future. In sub-micron technology, gate thickness oxide is less than 3nm and hence leakage current increases. This leakage current is called direct tunnelling leakage current [5-7] due to tunnelling of charge carries through gate oxide to silicon. Some models are available in literature to deal with convergence problem and leakage current [5-7], though they are not efficient. Hence, it is required to develop a new model to deal with this problem.

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Track number: Internet of things for Healthcare Applications

Utilizing CMOS Instrumentation Amplifier for Healthcare Applications

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Abstract: CMOS instrumentation amplifier (IA) is the basic building block for a large number of electronic circuits. It basically operates at low power- low voltage and requires less chip area & it has been integrated in different technologies. The main purpose of using CMOS IA is to reduce power consumption, chip area & to get high CMRR which is suitable for healthcare applications. Physiological signals are weak potential signals that range between microvolts to millivolts so, it is desirable to have minimal flicker noise and DC offset in case of these signals. This paper reviews the use of CMOS instrumentation amplifier for healthcare applications such as ECG, EMG, EEG, etc. Design technologies along with applications are charted out in this paper. Different techniques have been discussed to reduce flicker noise and DC offset in physiological signals.

Keywords: CMOS, Instrumentation Amplifier, ECG, EEG, EMG, ERG, EGG, PPG, EOG, AAP, ENG, CMRR, PSRR, GB, Input Referred Noise Voltage.

I. Introduction

Studying bio-medical signal is important field since, it contains vital information about health. Bio-potential signals are weak electrical signals having low amplitude and low frequency. Table 1 shows the various properties of physiological signals such as ECG (Electrocardiogram), EEG (Electroencephalography), EMG (Electromyography), ERG (Electroretinography), EGG (Electrogastrogram**),** and PPG (Photoplethysmogram**).** From Table- 1, it can be noted that all the physiological signals are in range between microvolts to millivolts and having frequencies less than 1KHz, so before processing, they must be amplified. These signals can be amplified by IA which consist of different blocks for gain enhancement, offset reduction circuit (chopper circuit, Auto-zeroing circuit), residual ripple from offset reduction circuit (e.g., gm-C filter) etc. In low power applications like all these, an IA with high gain, high CMRR (Common Mode Rejection Ratio),high PSRR (Power /supply Rejection Ratio), low DC offset and low input referred noise is required. To get high CMRR, resistor matching is essentially required which is the major drawback of conventional IA which consist of three op-amp & resistors & can be resolved by designing IA using op-amp with current mirror, active MOS, with current feedback circuit etc., where matching of components is not required. To reduce DC offset, Auto-zeroing technique [30] is widely used. To remove flicker noise, different techniques are available like chopper technique [11], level shifter [6], Differential Difference Amplifier (DDA) [22] etc. Miniaturization of electronic circuits is essentially required in biomedical field. Figure-1 shows the voltage and frequency ranges for some more Physiological signals like AAP (axon action potential) and EOG (electrooculography) along with ECG, EEG & EMG.

Physiological signals	Measurement range	Gain needed (dB)	Frequency range(Hz)
EEG	25-300µV	50-72	DC-150
ERG	5-900 µV	41-86	DC-50
EGG	10-1000 µV	40-80	DC-1
ECG	0.5-4 mV	28-46	0.01-250
EMG	0.1-5mV	27-60	DC-500
PPG	5-100nA	40-66*	0.05-40

*amplified to be at 10 µA level•

Table 1: Properties of various Physiological Signals [1].

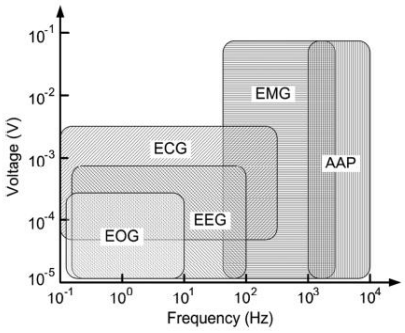

Fig-1: Voltage and Frequency ranges for EOG, ECG, EEG, EMG, AAP [11].

The block diagram of biomedical electronic system is shown in figure-2[6]. The weak biomedical signals are recorded by recording electrodes along with many unneeded interference and noise signals. However, the biomedical signals are too weak to detect, therefore an amplifier is cascaded next to electrode which can reduce the common mode noise and amplify the desired signal only. After that, signal is passed through LPF, sample and hold circuit followed by analog and digital converter (ADC) to become a digital signal. These digital signals are further processed by microprocessors.

Physiological signals	Carrier	Activity
EEG	Voltage	Brain Rhythms
ECG	Voltage	Cardiac Rhythms
EMG	Voltage	Muscle Activation
EOG	Voltage	Eye Movement
ERG	Voltage	Retinal Potential
EGG	Voltage	Stomach Activity
EIT	Impedance	Lung Activity
fNIRS	Optical	Neurovascular Activity
PPG	Optical	Blood Oxygenation

Table-2: Physiological signals along with carrier & activities [5].

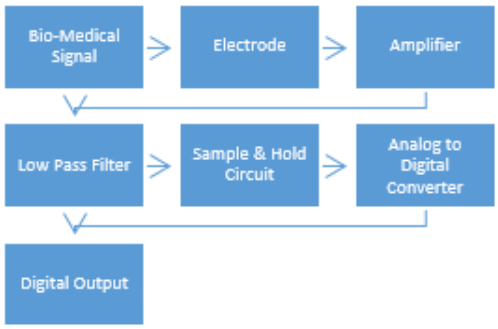

Fig-2: The biomedical electronics detecting system blocks [6].

Table-2 [5] shows various physiological signals along with carrier and activities. In this table some new physiological signals are introduced & they are EIT (Electrical Impedance Tomography) used to record lung activities and FNIRS (Functional Near-infrared Spectroscopy) used to measure neurovascular activities.
This paper is organised as follows. Section I provides an introduction to the topic. Section II presents CMOS Instrumentation Amplifier. CMOS IA for Healthcare applications is described in Section III. The Conclusion and Future scope is presented in Section IV.

II. CMOS Instrumentation Amplifier

An IA is a type of difference amplifier that have very low DC offset, low noise, very high open loop gain and high CMRR as desired. It is essentially important for all physiological signal acquisition system and used to amplify small differential sensor voltage. But, the differential sensor signals are generally associated with interference in the form of common mode voltage, the conventional IA common mode voltage. The conventional IA consists of three op-amps and a resistive feedback network along with transducer element (Rgain).
The three op-amps IA is commonly used on bio-signal processing due to its low DC offset, high gain, high CMRR & input impedances. It also suppresses the noise & the common mode signals that affect the original signal & also provides proper amplification to the input signal. The rightmost amplifier is the standard differential amplifier that amplifies the difference voltage appearing on the inverting and non-inverting nodes with gain R_3/R_2. The two amplifier on the left side is the buffer amplifier, if Rgain is open circuited, they behaves as a unity gain buffers and offer high input impedance & the circuit gain is simply equals to R_3/R_2. The Rgain increases the differential mode gain of the buffer & setting common gain equal to one, this increases the CMRR of the circuit & allowing the buffer to handle much larger common mode signal. In IA, common mode gain is due to mismatch in the resistor ratio R_3/R_2 and common mode gain of two buffer amplifiers. The ideal value of common mode gain is zero, results in infinite CMRR [12]. The drawback of conventional IA is that very good matching of resistor is required to get small common mode gain. The circuit shown is figure-4 will give minimum common mode gain because of matched resistors but, cost of IA increases considerably because of accurate resistor trimming. New

designs have been developed to save the expense of resistor trimming& increase CMRR. Some of the new designs are illustrated below:

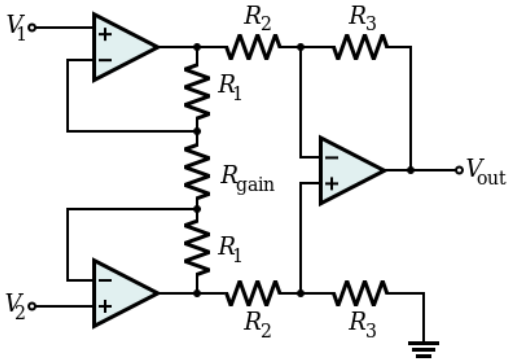

Fig-4: Conventional Instrumentation Amplifier [12].

(i) Op-amp with current mirror: figure-5 shows the new IA with current mirror [2]. In this circuit current mirror is used that increases CMRR and avoids the need of resistor matching. V_1 & V_2 are the differential inputs of the amplifier. Op-amp1 & op-amp2 are the buffer amplifier having output voltage V_{01} & V_{02} respectively. Due to virtual short concept $V_{01=}$ V_1 and $V_{02=}$ V_2. The current flowing through load resistance R given by:

$$I_R= (V1-V_2)/R \qquad \text{(eq.1)}$$

Op-amps are designed precisely such that this current must flows only from the most positive supply voltage & pass through current mirror CM_1 & CM_2. CM_1 & CM_2 measures the output stage current of op-amp1 & opamp2 i.e, I_1 &I_2, these current is equal to the current flowing into the resistor R and given by:

$$I_R= I_1= -I_2 \qquad \text{(eq.2)}$$

The CMOS current subtractor circuit is shown in figure-6[2], used to inject the current I_1-I_2 into a gain resistor R_g. The output voltage is given by:

$$V_0= V_g= I_g\times R_g= 2K(V_1-V_2) \qquad \text{(eq.3)}$$

With current through gain resistor is given by:

$$I_g= I_1-I_2= 2I_R \qquad \text{(eq.4)}$$

Where, K= programmable gain resistor & (V_1-V_2) is the differential input. And the voltage gain is given by:

$$V_0/(V_1-V_2)= V_g/(V_1-V_2)= 2\times K= 2\times(R_g/R) \qquad \text{(eq.5)}$$

The advantage of this circuit is that, the circuit will operate at low- power, low voltage, high gain & low load resistance R. A low R is required to increase the sensibility of the circuit as, the output current I_1-I_2 is proportional to 1/R. The op-amp1 and op-amp2 are identical & designed to operate at V_{DD1}=1.5V. The output stages are designed to operate at V_{DD2}= 2.2V by current mirror-1 & current mirror-2. Op-amp3 is identical to input op-amps but have capacitive load instead of resistive load. This design doesn't require expensive on chip resistors trimming since the CMRR depends on current mirror & not on a resistive feedback network. Figure-6 is a current subtractor circuit having a current mirror with two current inputs. R_g is a programmable gain resistor & realised with resistors & switch networks. The value of R_g is selected by an n-bit digital word which controls the switch networks.

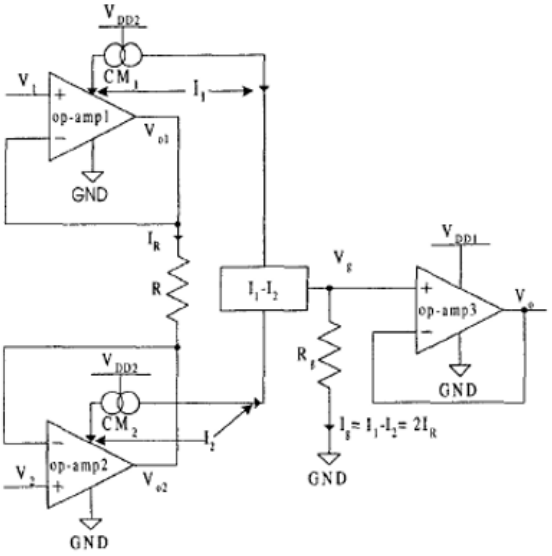

Fig-5: Instrumentation Amplifier design with current mirror [2].

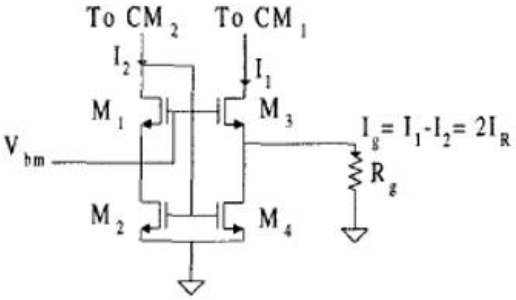

Fig-6: Current subtractor circuit [2].

The CMOS operational amplifier [2] & CMOS cascode current mirror circuits[2] are shown in figure-7 & figure-8 respectively.

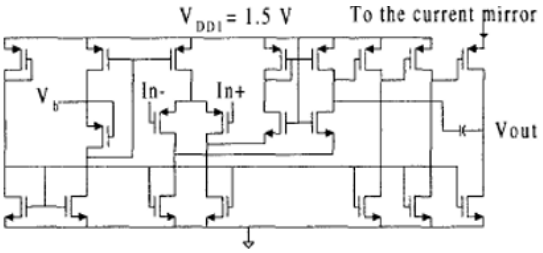

Fig-7: Op-amp schematic with CMOS technology [2].

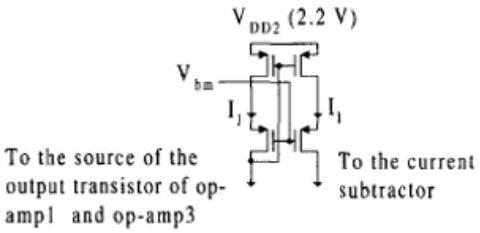

Fig-8: CMOS cascode current mirror [2].

(ii) Current Feedback Instrumentation Amplifier (CFIA): Another design of IA is shown in figure-9 [4] & corresponding schematic for a single IA is shown in figure-10 [4]. The first stage of the circuit is composed of two identical IA's whose input are connected to opposite polarity & the second stage contains another IA whose differential input is from the output of the first stage. Gain & CMRR of the given circuit amplifier in figure-9 are improved as compared to the single IA. The CMRR mainly depends upon common mode gain mismatch between first stage IA's. In CFIA, CMRR depends on the mismatch of transistor instead of resistors. To improve CMRR, the size of input transistor is larger than the minimum feature size of the technology used. To minimize the effect caused by electrode-skin interface inducing offset, a first order Gm-C HPF is used in the transimpedance stage. C_1 & C_2 realize a LPF with gain setting resistor R_2 & R_3 respectively to supress high frequency noise. The overall transfer function of this CFIA is Band Pass. Pseudo differential pair is employed in the transimpedance stage to improve linearity of the IA because, the architecture eliminates the even harmonics. Noise performance of this circuit is better.

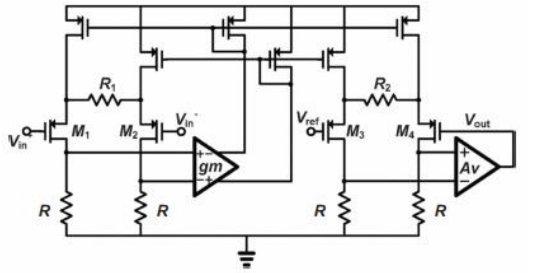

Fig-9: schematic of CFIA [4].

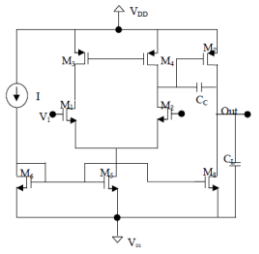

Fig-12: Two stage CMOS op-amp [7].

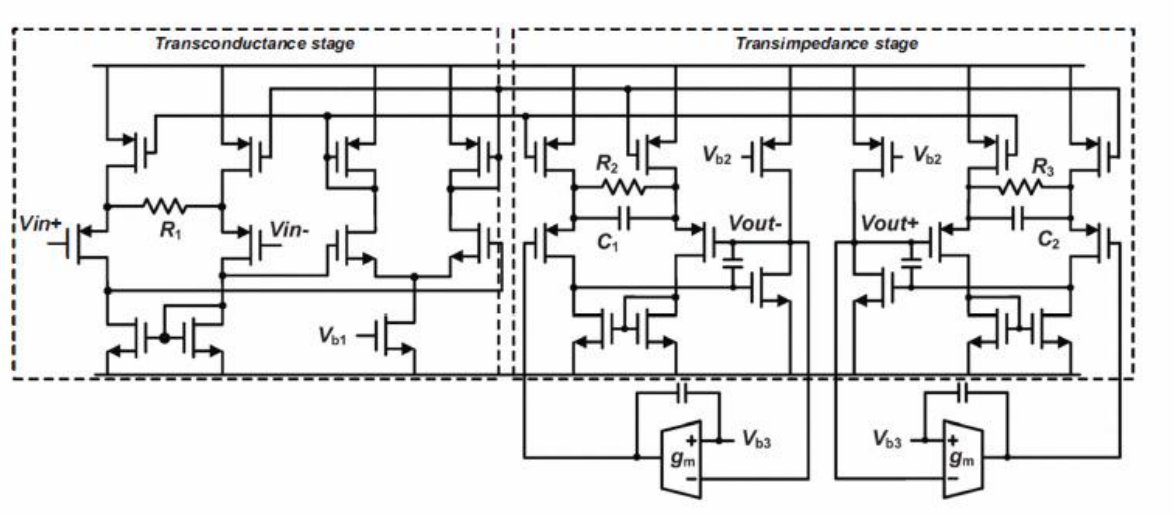

Fig-10: Schematic of single IA [4].

(iii) IA with active MOS device: In this circuits all the passive resistors of conventional op-amp are replaced by NMOS transistor. All the NMOS transistors are operating in triode region & making the circuit an active IA. The resistance value of all the transistors are calculated by using equation-6 & given by:

$$r_{DS} = L/(\mu_n Cox.W.(V_{GS}-V_{TH})) \quad \text{(eq. 6)}$$

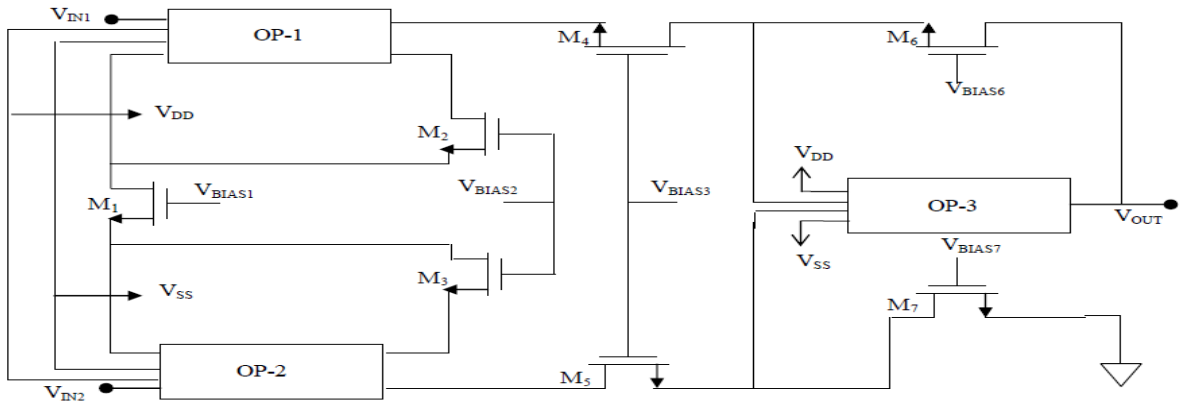

Fig-11: Instrumentation Amplifier with Active MOS device [7].

Gain of the IA can be varied by varying V_{BIAS} in the triode region, V_{BIAS} is the DC bias voltage. By using active impedances, both power consumption & temperature dependency are greatly reduced. Figure-11 shows the circuit diagram of IA with active NMOS transistors [7]. The circuit uses two stage op-amp in its design. Figure-12 shows the two stage op-amp circuit [7]. All the important parameters of IA are discussed below & noise reduction techniques as well.

(i) CMRR: The common-mode rejection ratio of a differential amplifier (or other device) is used to quantify the ability of the device to reject common-mode signals i.e., those that appear simultaneously and in-phase on both inputs. An ideal differential amplifier would have infinite CMRR. A high CMRR is required when a differential signal must be amplified in the presence of a large common-mode input. In bio-medical field, it is necessary to reject unwanted signals coming from neighbouring muscles & interference from main line. In conventional IA a high CMRR depends on resistor matching & can be resolved by new design of IA like IA with current mirror technique. To increase CMRR, a block diagram is shown in Figure-13. It consists of three IA's. The differential input signals Vip and Vin are applied simultaneously on both the IA's on the left side. However, the phase of the input signals are opposite.

The output signals of both the IA's on the left side are act as a differential input signal for IA_3. Assuming, common mode signal comes into the input of the IA_1 & IA_2. The output of IA are generated by multiplication of the common mode signal & common mode gain (A_{cm}). As because, the output of the IA_1 & IA_2 are identical & if both the left side IA are perfectly matched, it also act as common mode signal for the IA_3. Therefore, very small common mode gain is achieved. In the case of differential input, of the proposed architecture operates as a two stage differential amplifier. Therefore, a large differential gain (A_d) can be achieved. When the $V_{ip}= V_{cm}+V_i/2$ & $V_{in}= V_{cm}-V_i/2$, then output can be represented as:

$$V_{out}=(A_{cm1}.A_{cm3}/2+A_{cm2}.A_{cm3}/2+A_{cm3}.A_{d3}-A_{cm2}.A_{d3})V_{cm}+(A_{d1}.A_{cm3}/2-A_{d2}.A_{cm3}/2+A_{d1}.A_{d3}+A_{d2}.A_{d3})V_i \quad \text{(eq.7)}$$

In the ideal case, $A_{cm1}=A_{cm2}=A_{cm3}=A_{cm}$ & $A_{d1}= A_{d2}= A_{d3}= A_d$, the CMRR of the proposed architecture is given by equation-8.

$$CMRR= 2(A_d/A_{cm})^2 \quad \text{(eq.8)}$$

Equation-8 indicates, that CMRR of the proposed IA is improved by square times that of the single IA & an additional advantage is that, this technique can be applied to the any system that require high CMRR regardless of the type of the IA [4].

(ii) PSRR: Power supply rejection ratio is a term used to describe the capability of an electronic circuit to suppress any power supply variations to its output signal. In operational amplifiers, the PSRR is defined as the ratio of the change in supply voltage to the differential output voltage it produces. An ideal operational amplifier would have infinite PSRR. The formula of PSRR is specified in terms of the output & given by [54]:

$$PSRR= 20\log_{10}((\Delta V_{supply}/\Delta V_{out})A_v))\ dB \quad \text{(eq. 9)}$$

The technique to enhance PSRR are discussed below. Some of the PSRR enhancement techniques are based on low-dropout regulators (LDO) [9]. Despite these solutions provide a good PSRR at DC & at low frequencies in general, their performances tend to deteriorate when high frequency noise is coupled. In proposed technique, the current that flows through a transistor operating in saturation region depends, to a first order of approximation, on its gate-source voltage |VGS|. Transistors working as current sources have usually tied their source terminal to the supply rails & if these rails are contaminated by noise, the variations in the rail are transmitted to the source V_S, changing V_{GS} & their drain current as shown figure-14,& this introduces errors which can be relatively large. The proposed PSRR enhancement technique is depicted in Figure 15, the idea is to transfer the same variations of V_S (source voltage) to the gate terminal V_G, so V_{GS} remains constant and in this way, to a first order approximation, the drain current remains constant despite variations in the rail. Implementation of Figure-15 is straightforward if we use QFG (Quasi Floating Gate) transistors, as shown in Figure-16. The QFG technique uses a large resistive element (Rlarge) more than 10 gigahertz to set the quiescent voltage at the gate of a transistor. Rlarge is usually implemented by using a minimum size diode connected transistor that operates in cut-off region. Under dynamic conditions, the capacitor C_b is in picoFarad & cannot rapidly charge on terminal-G because of very large time constant, τ = Rlarge.C_b. This causes C_b to perform as a floating battery so that, voltage variations at terminal -S are transferred to terminal-G. In this way, frequencies above the lower cutoff Frequency $fo=1/[2\pi(Rlarge \bullet Cb)]$, which can be as low as 1Hz, there is a virtual connection between the source & the gate so that V_{GS} remains constant & as a result, the drain current remains constant independent of the variations in V_S (source voltage)[10].

(iii) DC offset: Because of electrochemical effects at the electrode-skin interface, the dc offsets signals are very large & common across recording electrodes [22]. It is the major problem in integrated bio-potential amplifier & therefore a low offset op-amp is required. This offset typically, 100mV to 500mV is generated at the electrode electrolyte interface & is many times greater than signal voltage to be measured i.e., 100-500µV & without sufficient attenuation this offset easily saturates the input stage amplifier [23]. There are lots of circuit is available nullify the effect of dc offset for IA in which a circuit is shown in Figure-17 [7]. The circuit is shown in figure-17

is added at the output of IA shown is Figure-11. This configuration tunes the lower 3dB cutoff frequency by a matched pair of floating capacitors & uses ON resistance of CMOS transmission gate to work as high pass filter for offset cancellation**.** The signal V_{OUT} from Figure-11 having an offset is applied to the input terminal of figure-17. The circuit operates in two ways:
When Clk_2 is high, then the transistors M_1 & M_4 are in ON state & thereby, passing the incoming signal which can be obtained at the output. At the same time as clock Clk_2 is out of phase of Clk_1 therefore, both the transistors M_2 and M_3 are in OFF state. The same procedure will takes place for the other half & so when full clock cycle is applied to the circuit, due to the presence of capacitors, the output of a circuit will be offset free. Instrumentation amplifier with offset cancellation technique is shown in [1][29][30] & two stage op-amp with low offset technique is shown in [23]. CMIA with DC offset cancellation technique is proposed in [24][27]. [27][31] uses nested chopper technique to reduce spike noise which results in residual DC offset. The system shown in figure-20, includes a non-overlapping clock generator & frequency dividers to achieve the chopping clocks at 10kH & 100Hz for the nested-chopping operation. The residual offset is eliminated by applying another pair of choppers which is operated at a lower frequency. In the block diagram of Figure-20, spike noise from the outer choppers can be neglected, if the chopping frequency is low enough and the spikes from the inner choppers are modulated by the outer choppers which leads to average energy of the spikes becomes zero, thus removing the residual offset. Different other techniques for spike noise removal are shown in [32-34].

(iv) Noise reduction techniques: Biosensor IA's require extremely low flicker noise because all the physiological signals are reside at low frequencies. Chopping is one of the technique to reduce flicker noise. In this the input signal is modulated to a higher frequency called f_{chop} and then demodulated back to baseband after the amplifier. The demodulator behaves as a modulator to the flicker noise of the amplifier & is removed by a low pass filter. F_{chop} needs to be at least Nyquist rate in order to prevent aliasing of the input signal & higher than the noise corner frequency which is defined as the frequency when thermal noise becomes dominant over flicker noise [11][25]. Chopper circuit is shown in figure-18 [11] & CMIA with chopping technique is shown in figure-19 [11]. CMIA is consist of second generation current conveyor (CCII) & chopper circuit. The CCII is designed using a two stage operational amplifier followed by a current mirror stage [26]. Another chopper stabilization circuit for flicker noise reduction is shown in [28]. Auto-zeroing technique is used to achieve low DC offset & low frequency noise is given in [30]. [35] shows the another noise reduction technique by low noise amplifier, the design uses two approach which is:
(a)PMOS input is used in LNA because its flicker noise is less than that of NMOS [36] &,
(b)Lateral PNP BJT input is used since it has better noise characteristics than that of MOS transistors [37].

III. CMOS Instrumentation Amplifier for Healthcare Applications

An increasing interest in continuous health monitoring system, lots of research have done on personal healthcare to easily diagnose the health. The applications include EEG, ECG, EMG, Bio-impedance spectroscopy etc. The most challenging building block for bio-medical sensor system is the IA since, the input is weak electrical pulses interference with common mode noise. Generally, the major source of error results from skin-electrode interface & flicker noise dominate at low frequency. In order to get desired signal, a high CMRR & low noise IA is required. Different type of IA's have been discussed in section II. All the physiological signals are generated from volume conduction of current made by collection of electrogenic cells. All the physiological signals are discussed below:

(i) ECG: It is the process of recording the electrical activities of heart over a period of time by using electrodes that are placed on the skin. These electrodes detect the tiny electrical changes on the skin that arises from heart muscles electrophysiologic pattern of depolarizing & repolarizing during heartbeat [13]. It is frequently used cardiology test. The goal of performing electrocardiography is to obtain the information about the structure & function of heart. An electrograph is a machine that perform electrocardiography & produces the electrocardiogram. The basic component of electrocardiograph is the IA, which is responsible for taking the voltage difference between electrodes (Lead) & amplify the signal. Table-3 shows the comparison chart of different physiological parameters for ECG.

(ii) EMG: it is an electrodiagnostic medicine technique for evaluating the electrical activity generated by skeletal muscles. It is performed by an instrument called electromyograph to produce a record called an electromyogram. An electromyograph detects the electrical potential produced by muscle cells when these cells are electrically or neurologically activated. It is used to detect medical abnormalities, activation level or to analyse the biomechanics of human or animal movement. It is also used for identifying neuromuscular disease & as a control signal for prosthetic devices such as prosthetic hands, arms & lower limbs. EMG signals are also used to guide botulinum

toxin & phenol injections into muscles. EMG is usually performed with another electrodiagnostic medicine test that measures the conducting function of nerves & called as nerve conduction studies (NCS). Needle EMG & NCS's are typically indicated when there is a pain in the limbs, weakness from spinal nerve compression or concern about some neurologic injury or disorder [14]. Table-4 shows the comparison chart of EMG.

(iii) EEG: It is an electrophysiological monitoring method to record electrical activities of the brain over the period of time. It is typically non-invasive, with multiple electrodes are placed along the scalp. It measures voltage fluctuations resulting from ionic current within the neurons of the brain. EEG mostly used to diagnose epilepsy, which causes abnormalities in EEG readings & to diagnose sleep disorders, depth of anesthesia, coma, brain death & encephalopathies. It is used to be a first-line method of diagnosis for tumors, stroke & other focal brain disorders, but this use has decreased with the advent of high-resolution imaging techniques such as magnetic resonance imaging (MRI) and computed tomography (CT). Despite limited spatial resolution, it continues to be a valuable tool for research and diagnosis. It is one of the few mobile techniques that are available and offers millisecond-range temporal resolution which is not possible with CT or MRI [15]. Table-4 shows all the parameters for EEG amplifier.

(iv) EOG: It is a technique for measuring the corneo-retinal standing potential that exists between the front and the back of the human eyes & the resulting signal is called the electrooculogram. The primary applications are found in ophthalmo- logical diagnosis & in recording eye movements. Unlike the electroretinogram (ERG), the EOG doesn't measure response to individual visual stimuli. To measure eye movement, pair of electrodes are placed either above & below the eye or to the left & right of the eye. If the eye moves from the centre position toward one of the two electrodes, this electrode see's the positive side of the retina and the opposite electrode see's the negative side of the retina & Consequently, a potential difference occurs between the electrodes. Assuming that resting potential is constant, the recorded potential is a measure of the eye's position. It is used to assess the function of the pigment epithelium [17]. Low cost EOG based controlling system design is presented in [16].

(v) EGG: An EGG is a graphic, produced by an electrogastrograph, which records the electrical signals that travel through the stomach muscles and controls the muscle contractions. An electrogastroenterogram or gastroenterogram is a similar procedure, which measure electric signals not only from the stomach, but also from intestines. An electrogastrogram and a gastroenterogram are similar in principle to an electrocardiogram (ECG) in that sensors on the skin detect electrical signals indicative of muscular activity within, where the electrocardiogram detects muscular activity in various regions of the heart. The electrogastrogram detects the wave like contractions of the stomach (peristalsis) [18]. [52] presents EGG circuit with IA.

(vi) EIT: Electrical impedance tomography is a non-invasive type of medical imaging in which the electrical conductivity, permittivity & impedance of a part of the body is implied from surface electrode measurements & used to form a tomographic image of that part. Electrical conductivity varies considerably among the various biological tissues or the movement of fluids and gases within tissues. The majority of EIT systems apply an alternating currents at a single frequency. However, some EIT systems use multiple frequencies to better differentiate between the normal and suspected abnormal tissue within the same organ [20]. In order to identify & suppress the movement artifacts, the EIT & bio-potential signal should be sensed simultaneously. This requires chopper stabilization technique for the impedance measurement to separate electrophysiological signal from resistive and reactive impedance signals, each occupying different frequency bands [5]. [51] uses IA for its construction.

(vii) ENG: It stand for Electronystagmography. It is a diagnostic test to record involuntary movements of the eye that caused by a condition known as nystagmus (Nystagmus is a condition of involuntary or voluntary eye movement acquired in infancy or later in life, that may result in reduced or limited vision [53]). The ENG signal is centred between 1-5 kHz [38]. It is also used to diagnose the origin of vertigo, dizziness & balance dysfunction by testing the vestibular system [39]. The test of this is performed by connecting the electrodes around the nose and measuring the movements of the eye in reference to the ground electrode. The vestibular system is used to monitor the position & movement of the head to stabilize retinal images and this instruction is integrated with the visual system & spinal afferents in the brain stem to produce vestibulo-ocular reflex. ENG gives fair assessment of the oculomotor & vestibular systems. For testing vertigo by using the caloric reflex test, a similar test is

performed, which can be induced by air or water of specific temperatures i.e., typically ±7 degrees Celsius from body temperature [39]. Table-5 shows the different technological parameter of ENG. [40] shows the ENG based IA.

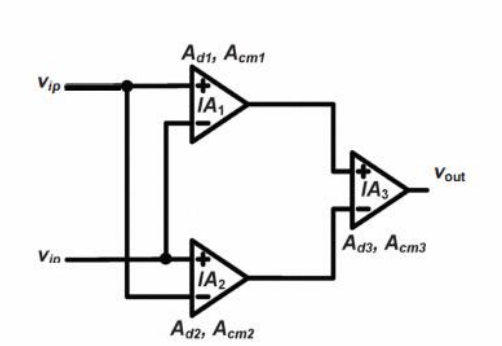

Fig-13: CMRR enhancement technique using three IA's [4].

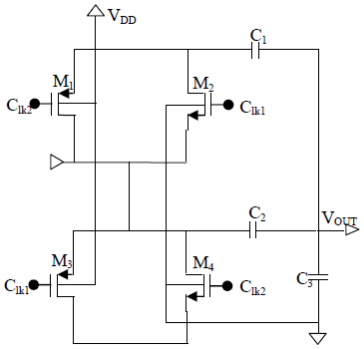

Fig-17: DC offset Removal circuit [7].

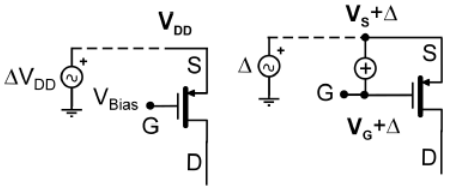

Fig-14

Fig-15

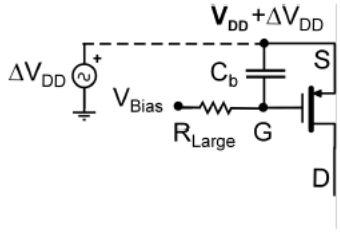

Fig-16

Fig-14: Simple PMOS current source [10],
Fig-15: Proposed Technique [10] &
Fig-16: Implementation with QFG transistors [10].

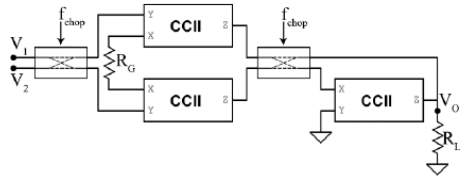

Fig-19: CMIA with Chopping technique [11].

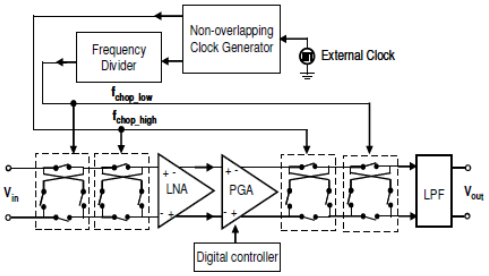

Fig-20: Biomedical readout front-end with spike noise removal circuit [27].

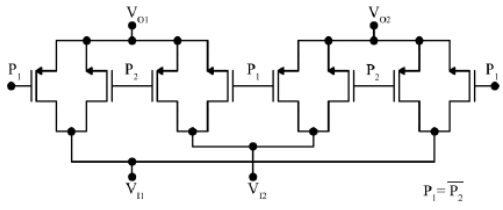

Fig-18: Chopper Circuit [11].

Parameters	[40]	[41]	[2]	[42]
Technology	0.35 µm	0.35 µm	0.35 µm	0.7 µm
Supply voltage	3.3V	3V	2.2V	5V
CMRR(dB)	107	100	120	85
Power consumption	460 µW	0.94 mW	166 µW	1.3 mw
Layout area	0.4 mm^2	1.2 mm^2	350× 150µm^2	2.7 mm^2
Simulator	Spectre	Cadence	Spectre	---
PSRR(dB)	---	85	---	---
DC gain of IA(dB)	63	6-47	81	74
Bandwidth	0.5Hz-13 KHz	100Hz - 12KHz	---	3KHz

Input ref-erred noise (nV/√Hz)	12	12	---	6.6
Total capacitance (pF)	27	>89	---	97
NEF*	---	4.2	---	5.3

*NEF: Noise Efficiency Facto

Table-5: Technological parameters of different ENG circuits.

S. no.	Parameters	[43]	[44]	[45]	[46]	[47]	[48]	[8]
1	Technology	0.35µm	0.18 µm	90nm	65nm	0.25 µm	0.18 µm	0.18 µm
2	Supply voltage	3V	1.2V	0.5V	1V	±0.8V	1V	1V
3	CMRR	>100dB at 0.01-16Hz; >90 dB upto 40Hz	110dB at 50Hz	>91.9dB	>84dB	126.6 dB	90dB	60dB
4	Power consumption	28µW	1.3µW	32.08µW	0.87µw	695µW	---	53.7µW
5	Layout area	---	---	1.21×1.21 mm^2	2.2mm^2	---	---	---
6	Simulator	Spectre	Spectre	---	---	Pspice	---	Virtuoso
7	PSRR	---	105dB at 50 Hz	---	---	---	---	153.71dB
8	DC gain of IA	Variable	40dB	54.4-87.6dB	Variable (59.1/69.8/78) dB	22.23-45.38dB	90dB	96.41dB
9	GB	280kHz	---	---	---	---	50kHz	400kHz
10	IA design	CMIA	CSIA*1	FDIA*2	CCCIA*3	CFIA	CCCIA	Op-amp with active MOS
11	Input referred noise	248 nV/√Hz at 0.01Hz; 197 nV/√Hz at 100 Hz	0.7 μV_{RMS} at 0.15-100Hz	0.358 μV_{RMS}	0.81μV_{RMS}	9.477 µV/√Hz	32 nV/√Hz	610nV/√Hz
12	THD	0.075% at 8Hz, 5mV_{p-p} & 10V/V gain	-68dB at 50Hz & 200 mV_{p-p}	---	---	1.47%	20%	---
13	NEF	---	2.83	2.43	2.97	---	1.7	---

*1: Chopper Stabilized IA, *2: Fully Differential IA, *3: Capacitively Coupled Chopper IA

Table-4: Comparison table of different parameters for EEG processing circuit.

S. no.	Parameters	[3]	[49]	[22]	[50]	[35]
1	Technology	0.5µm	0.35 µm	0.18 µm	0.18µm	0.18µm
2	Supply voltage	2.5V; 7.5V	±1.5V	1.8V	1.8V	1.8V
3	CMRR	>110dB; >112dB	78dB	150dB at 10Hz	127dB	125.3dB
4	Power consumption	152.5µW; 937.5µW	1.23mW	3.9 µW	138 µW	61.504µW
5	Layout area	0.2mm^2	0.94mm^2	0.13mm^2	758×377 μm^2	---
6	Simulator	---	---	---	Hspice	---
7	PSRR	>120dB	---	62dB	65dB	PSRR(+): 125.3dB; PSRR(-): 126dB
8	DC gain of IA	20dB	18.06dB	46dB at 10Hz	45dB	82.4dB
9	GB	---	---	0.9MHz	---	---

10	IA design	Op-amp with active MOS	Op-amp with current mirror	---	Bias circuit, Gm-stage, trans-conductance stage, HPF	---
11	DC offset	26.8mV	---	---	0.3mV	---
12	Input referred noise	$45\mu V_{RMS}$	---	5µV/√Hz At 1Hz	0.278 µV/√Hz	107.7443nV/√Hz

Table-3: Comparison table of different parameters for ECG amplifier.

IV. Conclusion & Future Scope

CMOS IA is a basic building block for most of the physiological signals since, it requires less chip area and less power which is suitable for bio-medical engineering. It also improves the CMRR & DC gain, which amplifies the weak desired signal. All the physiological signals discussed in section-III uses IA in its processing circuit and the rest of the physiological signals discussed in section-I i.e., PPG, fNIRS and ERG still have to use IA in there circuit design.

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