M. Tech (VLSI Design & Embedded System) JAGJEET SINGH 2018

LOW POWER CDBA AND IT'S APPLICATION

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI Design &Embedded System

Submitted by:

JAGJEET SINGH

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Under the supervision of

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Bawana Road, Delhi-110042

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CANDIDATE'S DECLARATION

I **JAGJEET SINGH**, Roll No(s). **2K16/VLS/11** student of M.Tech (VLSI & Embedded System), hereby declare that the project Dissertation titled "**LOW POWER CDBA AND IT'S APPLICATION**" which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology/Bachelor of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi **(JAGJEET SINGH)**
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CERTIFICATE

I hereby certify that the Project Dissertation titled "**LOW POWER CDBA AND IT'S APPLICATION**" which is submitted by **JAGJEET SINGH**, Roll No **2K16/VLS/11** Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology/Bachelor of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

The technology advancements has led to an era of submicron devices/circuit being operated at low power supply which have proper functioning and as reliability. The need of low power supply is also beneficial for increased life time of battery in portable electronic systems. This work investigates the use of dynamic threshold metal oxide semiconductor (DTMOS) transistors in current differencing buffer amplifier (CDBA) an active block. The behavior of DTMOS based CDBA is studied through SPICE simulation using 0.18 μm technology. An application namely CDBA based filter operation is examined used presented DTMOS based CDBA.

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LIST OF SYMBOLS &ABBREVIATIONS:

Abbreviation	Full form
A_V	Voltage Gain
AC	Alternating Current
APF	All Pass Filter
BJT	Bipolar Junction Transistor
BPF	Band Pass Filter
BRF	Band Reject Filter
B.W	Bandwidth
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
CDBA	Current Differencing Buffered Amplifier
CDVB	Current Differencing Voltage Buffer
CDU	CDU
CDTA	Current Differencing Trans-conductance Amplifier
CFOA	Current Feedback Operational Amplifier
CM	Current Mode
CMOS	Complementary Metal Oxide Semiconductor
CNTFET	Carbon Nanotube Field Effect Transistor
DC	Direct Current
DCVC	Differential Current Voltage Conveyor
DDCC	Differential Difference Current Conveyor
DO-OTA	Dual Output Operational Trans-conductance Amplifier
DVCC	Differential Voltage Current Conveyor
ECCII	Electronically Controlled Current-Conveyor
FTFN	Four Terminal Floating Nullor
HPF	High Pass Filter
i/p-o/p	Input-Output
IC	Integrated Circuit
LP	Low Power
LPF	Low Pass Filter
LV	Low Voltage

MISO	Multiple Input Single Output
OTA	Operational Transconductance Amplifier
OTRA	Operational Trans-resistance Amplifier
VM	Voltage Mode
VLSI	Very Large Scale Integration

CHAPTER 1

Introduction

1.1 Background :

Low–power (LP) and low–voltage (LV) analog circuits are receiving appreciable attention and are becoming the first choice in the electronics industry. Therefore, there is need to develop new circuits which can operate on low supply voltage and consume small power. Designing of integrated circuits for a variety of applications has gained significant attention in the industry. It is seen from the trend of the semiconductor industry that with the continuous downsizing of feature size of the transistors, the optimal supply voltage of CMOS integrated circuits has been dramatically declined because the emerging consumer market wants portable devices that needed to be light and must operate for a long duration of time with the small battery. When a MOS transistor size is downsized, the thickness of the oxide is reduced. Therefore, if a MOS transistor has a thinner gate oxide then to safeguard the transistor from a breakdown due to the higher electrical field across the gate oxide, i.e. to ensure its reliability, the supply voltage needed to be reduced [1–5]. Therefore, low–power (LP) and low–voltage (LV) analog circuits are receiving appreciable attention and are becoming the first choice in the electronics industry. Electronic systems that could monitor physiological parameters, or worn by people, or even provide some kind of treatment are made accomplishable by new advance LP LV circuit design [6].

The first utilization of these circuits is low power Systems–on–Chips (SOCs) which is extended over markets such as Mobile Internet Services (Net-books, Smartphones, Laptops, Tablets), Home, Multimedia, Cellular Telecom, and Mobile etc. SOC circuits are having analog circuits and digital circuits co-existing on the same single chip. The idea of SOC came from the fact that the natural signals are mostly analog in nature, consequently, the bandwidth of a signal becomes higher in magnitude if the signal is processed in analog circuits. As a result of this, analog signal processing became inevitable to introduce.

The second application of these circuits is in low power biomedical devices. Lightweight, Small size and extended lifetime battery is a primary need for such devices. For example; fully implanted devices inside the human body must function for 10-20 years without need of replacement to avoid additional surgery. On the other hand, the future trend is taking us to battery-less biomedical devices those are powered by collecting relatively small amounts of energy from the environmental sources or from human body movements. [7-8].

Anyway, when we are moving to a low voltage supply, digital circuits do not suffer degradation in performance, however, the performances of analog circuits; such as speed, bandwidth linearity, dynamic range, gain etc. are overripe by reduced supply voltage [9]. So, there is crucial requirement to develop new design techniques for analog circuits which use the amount of power in the nano-watt range. From the last ten years, CMOS technology has played a great role in the rapid improvement of VLSI systems and the increased integration of VLSI systems. Characteristics of CMOS devices includes extremely low input offset voltage, low switching power consumption, very high input impedance, high packing density, due to these they can be easily scaled. So the requirement of the area for the circuit will be reduced. As a consequence of which, the parasitic capacitances are decreased because of smaller geometry, which in turns leads to more operating speed.

Since battery technologies do not evolve proportionally with the requirement of the applications demand. Therefore the primary challenge is to decrease the power consumption of the circuits.

Average power consumed by any circuit is composed of two components which are static power and dynamic power.

$$P_{avg} = P_{static} + P_{dynamic} \tag{1.1}$$

$$P_{avg} = V_{DD} I_{leakage} + C V_{DD}^2 f \tag{1.2}$$

Where V_{DD} is power supply voltage , $I_{leakage}$ is sub-threshold leakage current of MOS transistor, C represents the total capacitance of a system, and f denotes the frequency at which a circuit operates.

The most essential factors of CMOS VLSI design is the threshold voltage of the MOS device that is V_T.Since, it has been clearly seen that the declining of V_T is not possible as quickly as V_{DD} does in each new process generation and also a MOSFET's sub–threshold leakage current, $I_{leakage}$, has the exponential dependency on the threshold voltage of MOSFET consequences results in concerns over increasing P_{avg} through P_{static}. The example in order to show how disproportionately V_T and V_{DD} have fallen in recent years is shown in Fig. 1.1 where the two parameters are plotted for six standard TSMC bulk CMOS processes [10].

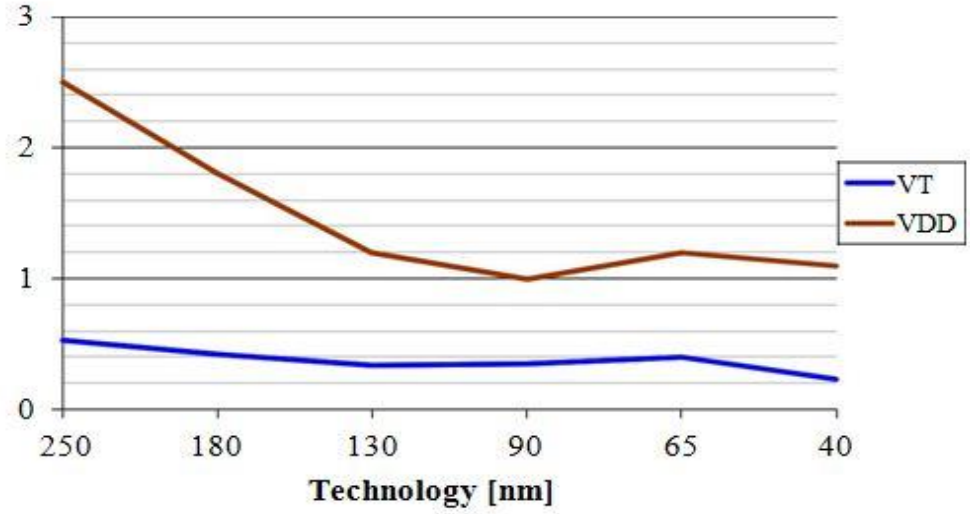

Fig 1.1 A plot of the recent trends seen in V_T and V_{DD} for standard TSMC bulk CMOS processes [10]

On the other hand, the new movement in the design of modern implantable or portable biomedical devices is in the direction of miniaturization and portability for long-term monitoring. Important specifications for these healthcare electronics devices are low power consumption and low supply voltage, which in turns leads to newer biomedical applications having another major target of low–power analog circuits.

1.2 Low–power and Low–voltage techniques :

Low–power and Low–voltage capability could be achieved either by developed technologies or by design techniques [11]. The key technologies used for LP and LV Integrated Chip design are:

- CMOS technology [12]: CMOS technology is a MOS technology in which incorporation of both *N*–channel and *P*–channel MOS transistors are fabricated on the same silicon chip. If in the bulk of the circuit *P*–dopant or acceptor ions has been doped then the MOSFET is labeled as *N*–channel transistors whereas the *P*–channel devices require a well (tube) having N-dopant or donor ions. The technology in which such a well is required is termed *N*–well technology. For an N–type substrate the arrangement is complementary: the *P*–channel transistors are made in the substrate and the *N*–channel transistors sit inside the *P*–well (Fig. 1.2 [13]). In the fabrication of typical microchips, CMOS technology is employed, since it is cheaper than SOI & Bi-

CMOS technologies and offers low–power dissipation, high performance, high density.

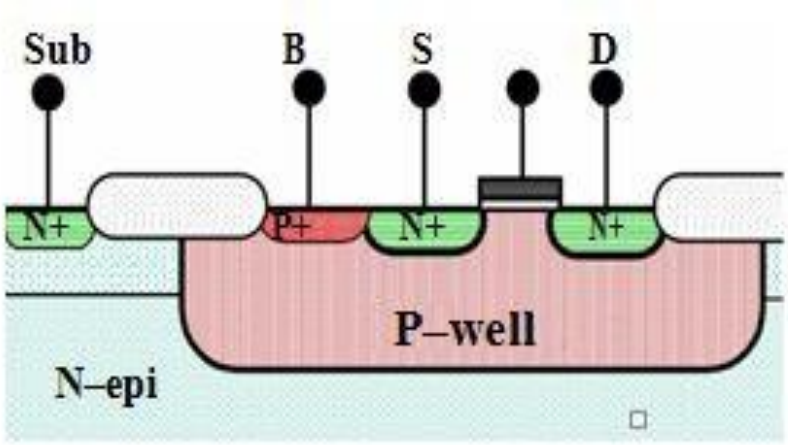

Fig 1.2 Simplified cross-section of an NMOST (*P*–well CMOS technology) [13]

- Bi-CMOS technology [14-15]: In this technology both MOS & BJT transistors are incorporated on a single integrated circuit, therefore this technology comprises the pros of both MOS& BJT transistors. Numerous advantages can be accomplished using this highly developed semiconductor technology such as: reduced value of power dissipation over purely CMOS technology, higher speed over purely bipolar technology, improved current drive over CMOS and obtaining high input impedance, low output impedance, latch-up immunity, high analog performance, low noise, high gain, , flexible I/Os for high performance, smaller IC size and of more reliable IC. However, Bi-CMOS technology requires extra fabrication steps, which makes the technology not cost-effective.
- SOI (Silicon On Insulator) technology [16–18]: In this technology a layer of silicon dioxide is implanted below the surface by oxidation of Si or by oxygen implantation into Si. This implanted silicon dioxide below the surface is called buried oxide (BOX) and helps reducing parasitic capacitances, and as a result of this is improved performance of the device. SOI can be categorized into two types: fully depleted FD and partially depleted PD, the main differences between these two are summarized in Tab. 1.1. Fig. 1.3 shows a starting wafer of FD–SOI.

Table. 1.1. PD–SOI vs. FD–SOI.

PD-SOI	FD-SOI
The channel is doped	The channel is often undoped or lightly doped
The top silicon is 50 to 90nm thick	The top silicon is 5 to 20nm thick
The insulating BOX layer is typically 100 to 200nm thick	The insulating BOX layer may be ultra-thin: 5 to 50nm thick

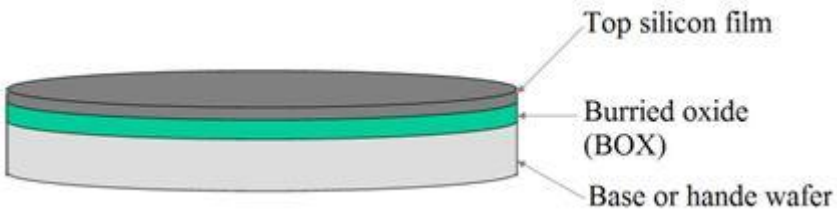

Fig 1.3 FD–SOI starting wafer [17]

SOI technology has numerous merits such as channel effects, capacitance reduction, lower supply voltage, lower device threshold, soft error rate effects, smaller layout area, ideal device isolation, high switching speed and lower–power consumption. However, fabrication of this technology is more expensive featuring also higher self–heating because of poor thermal conductivity of the insulator.

- DTMOS (Dynamic Threshold MOS) (19-20): In this technology the input is applied at gate and bulk terminal of the MOSFET simultaneously or in other words we can say that bulk and gate of the MOSFET are connected. This connection of the device will decrease the V_T of the device and hence we can reduce the supply voltage of the device while maintaining current deriving capability. SOI technique can be use to manufacture the practical DTMOS which combines the pros of SOI technology and DTMOS. The further discussions on DTMOS working was done in chapter 3.

From the above discussed technologies we will utilize DTMOS technology for presenting a DTMOS based current differencing buffer amplifier (CDBA) in this dissertation. The CDBA is a current mode analog circuits which has advantage of high-slew rate, wide bandwidth and simple implementation [21]. The CDBA is a multi-terminal active block having two input port

(i.e. P and N) and two output port (i.e. Z and W). The input current terminals take the current as input and provides the difference of that at one output terminal Z where a voltage is generated because of load present there and that voltage is reflected at other output terminal W. Therefore, the CDBA can be viewed as cascade of CDU and buffer amplifier. A lot of papers were also reported on the applications of CDBA such as voltage mode and current mode filters [22-26].

1.3 Outline of Thesis :

- **Chapter 1:** In this chapter, discussion related to power dissipation is placed along with probable solutions that may help minimizing power dissipation.
- **Chapter 2:** In this chapter, the literature on CDBA implementation is presented and also the implementation of the CDBA has been shown through SPICE simulations.
- **Chapter 3:** In this chapter, working and SPICE modeling of DTMOS is given. It also includes new modified circuit of CDBA has been presented based on DTMOS and characteristics of DTMOS based CDBA are investigated.
- **Chapter 4:** Application of the CDBA based on DTMOS as a VM Universal Biquad has been presented in this chapter to verify the functionality of presented DTMOS based CDBA.
- **Chapter 5:** Further work that can be done in the direction of the low power devices has been presented in this chapter.

CHAPTER-2

CDBA Realization

2.1 Introduction :

In past years, operational amplifier which is an active building block played a prime role and a vast publication comes into existence in the literature. But, op-amp based circuits have limited Bandwidth and slew rate results in drawback of performance. Therefore, because of the merits of current mode analog circuits ,the current mode analog circuits are becoming popular. This results in emergence of various analog block. From last few years, latest current mode active building blocks like second generation current conveyor (CCII), current-feedback op-amps (CFOA) attains substantial attention because of the wider bandwidth & larger dynamic range [27-28]. Additionally, different types of active elements like differential voltage current conveyor (DVCC), electronically controlled current-conveyor (ECCII), differential difference current conveyor (DDCC), third generation current conveyor (CCIII), dual Output operational trans-conductance Amplifier (DO-OTA) and four terminal floating nullor (FTFN) are presented in the literature [29–34].

In this chapter we will discuss a new current mode active building block named as current differencing buffer amplifier (CDBA) which was introduced by Acar and Ozoguz in the year 1999 [35]. Later we will discuss CFOA based realization of CDBA and CMOS based realization of CDBA. The device characteristics of CMOS based realization are also been observed using SPICE simulations.

2.2 CDBA Realization :

As current-mode circuits are becoming popular with advancement of time and because of their applications, a new active block was found in 1999, and this new block is called current differencing buffered amplifier (CDBA) [35]. The electrical symbol of the CDBA is shown in Fig 2.1.

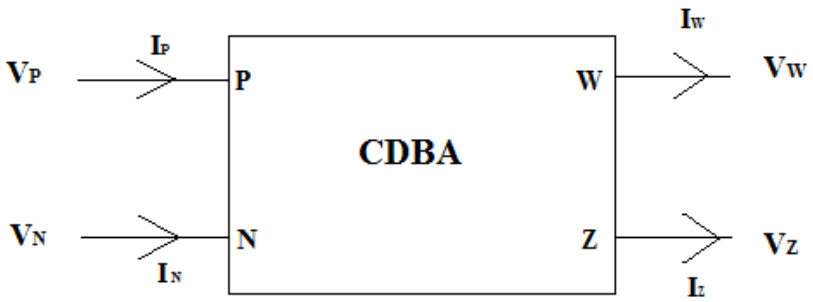

Fig 2.1 CDBA block [35]

The CDBA is characterized by the following relations (2.1):

$$V_P = V_N = 0,$$
$$I_P - I_N = I_Z,$$
$$V_W = V_Z \qquad (2.1)$$

A current differencing buffered amplifier (CDBA) is a multi-terminal active block having two input port and two output port and is developed by Cevdet Acar and Serdar Özoğuz in the year 1999. More appropriately, CDBA can also be called as CDVB (Current Differencing Voltage Buffer) or we can call it as DCVC (Differential Current Voltage Conveyor).

From equation (2.1), it can be inference that a CDBA unit provides the difference of the input current at output terminal Z and provides the voltage at W terminal through an impedance which is connected at the Z terminal of CDBA unit. Therefore, we can view CDBA as the trans-impedance amplifier or transfer- impedance amplifier because it giving output as a voltage by taking difference of current as input to it and therefore from this viewpoint, it is similar to the CFA. Ideally the CDBA has zero impedance at input terminals i.e. P and N current terminal and has high value of impedance at output Z terminal. The W terminal act like a voltage buffer therefore the impedance at W terminal of CDBA has a value of zero ohms.

2.2.1 CFOA Based Realization :

There are many ways to realize the CDBA and many are reported in literature [35-40]. The one of the possible way for implementation of CDBA is by available IC AD844 [36] ,Two AD844 IC can be cascaded as shown in Fig 2.2 for realization of CDBA.

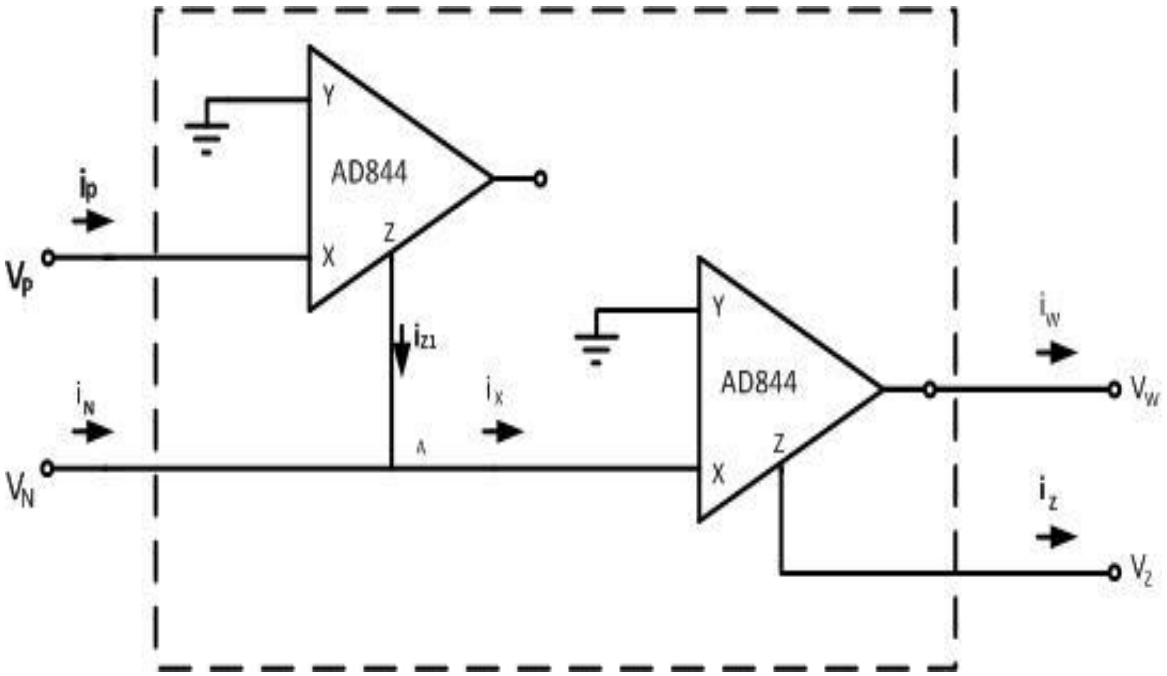

Fig 2.2 CDBA realization using CFOA [36]

The current-voltage characteristics of ideal CFOA can be modeled as :

$$\begin{bmatrix} I_Y \\ I_Z \\ V_X \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \quad (2.2)$$

Using current-voltage characteristics of ideal CFOA from equation (2.2) the current I_{Z1} shown in Fig 2.2 is equal to $-I_P$.

$$I_{Z1} = -I_P$$

Now apply KCL at node A as shown in Fig 2.2 ,we get ;

$$I_X = I_N - I_P$$

Again using current-voltage characteristics of ideal CFOA from equation (2.2)

$$I_Z = I_P - I_N \quad (2.3)$$

$$V_W = V_Z \quad (2.4)$$

By comparing equations of equation (2.1) with equation (2.3) and (2.4) it can be inference that Fig 2.2 represents the CDBA which is realized using two CFOA's.

2.2.2 CMOS Based Realization :

CDBA can also be realized using CMOS devices. There are many topologies reported for realization of CDBA, Among them the topology presented in [35] was popularly used. We are also discussing the same reported topology in our dissertation. Instead of study the CDBA as

whole unit we will divide into two parts one of them is current differencing unit (CDU) and another one is buffer amplifier (BA unit).

2.2.2.1 Current Differencing Unit :

The Current Differencing Unit (CDU) is a basic building block of several active elements for analog signal processing such as CDBA (Current Differencing Buffered Amplifier) [35] ,OTRA (Operational Trans-resistance Amplifier) [41], DCVC (Differential Current Voltage Conveyor) [42], or CDTA (Current Differencing Trans-conductance Amplifier) [43].CDU as shown in Fig 2.3 act as an input block to these circuits. Its primary function is to obtain input signals from P terminal and N terminal in the form of currents I_P and I_N and deliver the difference of these input currents to output terminal Z through high-impedance for subsequent processing of signal. The input terminals P and N must have low-impedance. The low impedance input terminals are required so that conjunction with external circuit could become feasible and CDU input gates can be utilized for direct voltage-to-current conversion. Secondly, the effect of parasitic impedances can be eliminated by low or ideally zero input impedance.

Since, preferred performance of CDU is to act as an ideal current source for supply which should be independent of connected output load impedance Z_L, therefore the high or ideally infinity impedance at the output terminal Z is required. In other words, value of the z-current should not depend on the loading impedance.

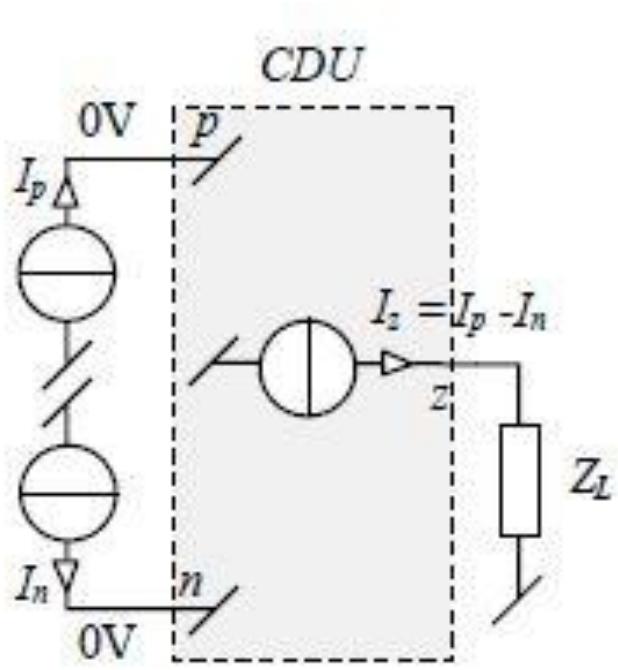

Fig2.3 Ideal CDU unit [21]

In reality, the CDU incorporates internal parasitic impedances Z_p, Z_n, and Z_Z which is shown in Fig 2.4. In combination with external impedances Z_{ip}, Z_{in}, and Z_L, these parasitic impedances i.e. Z_p, Z_n, and Z_z causes a non-ideal behavior of CDU block. The input impedances Z_p and Z_n also have inductive components in them which in turn negatively affect the normal behavior of circuit by increasing the values of impedances at high frequencies [21]. The internal current source is other contributor of error because its current gain β is not equal to unity, it is frequency dependent.

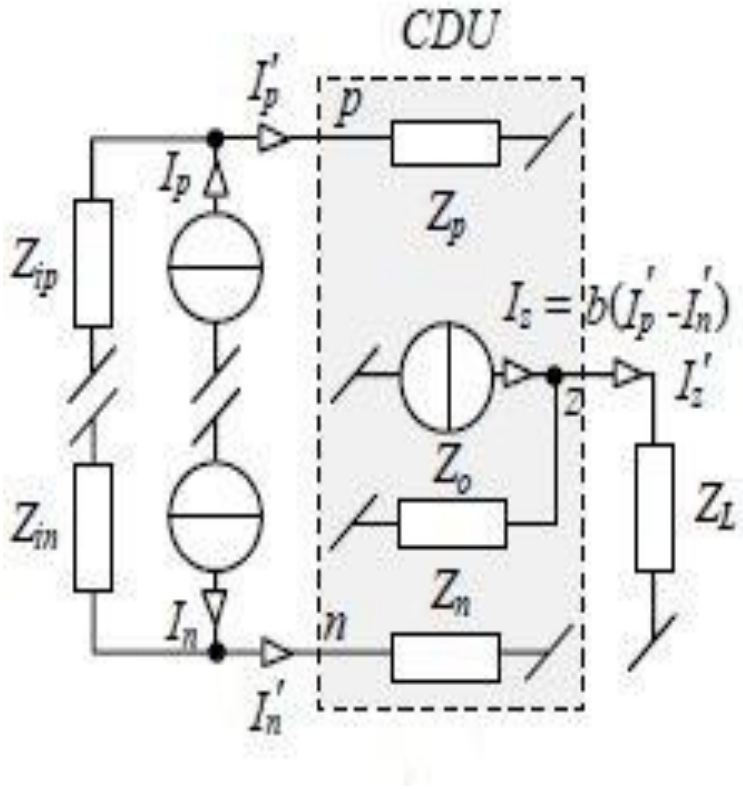

Fig 2.4 CDU with parasitic impedances being considered [21]

2.2.2.2 Buffer Amplifier :

The primary function of a buffer amplifier is to provide excellent isolation between a source of signal and a load. This objective is usually achieved by making the input impedance of the amplifier very high or ideally infinite and the output very low or ideally zero so that that loading effect becomes insignificant on the source. The output signal of buffer amplifier faithfully follows the input signal. If the output voltage which is following the input signal is same as input signal i.e. the voltage gain A_v is 1, then the amplifier is a unity gain buffer amplifier. Another name of buffer amplifier is known as a voltage follower due to reason that the output voltage tracks or follows the input voltage signal. However the voltage gain of a

voltage buffer amplifier can be approximately unity but it usually yields considerable current gain and consequently considerable power gain. However, it is commonplace to say that it has a gain of 1 (or the equivalent 0 dB). The Buffer amplifier can be implemented using OPAMP as shown in Fig 2.5.

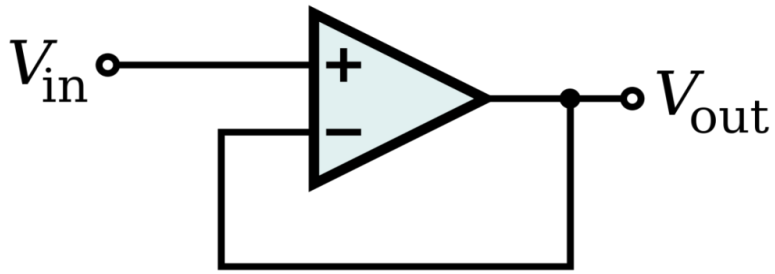

Fig 2.5 op-amp based Voltage follower

2.2.2.3 CDBA Realization :

As discussed earlier CDBA is composed of two units namely current differencing unit (CDU) and another one is buffer amplifier. It is a four terminal device out of which two terminals are input terminal and two are output terminal. The two input terminals P and N takes current as input to it and provides output as difference of two current at Z terminal and also provide a voltage at W terminal which developed across the load which is connected at Z terminal. The CMOS implementation of CBA is shown in Fig 2.6 [35].

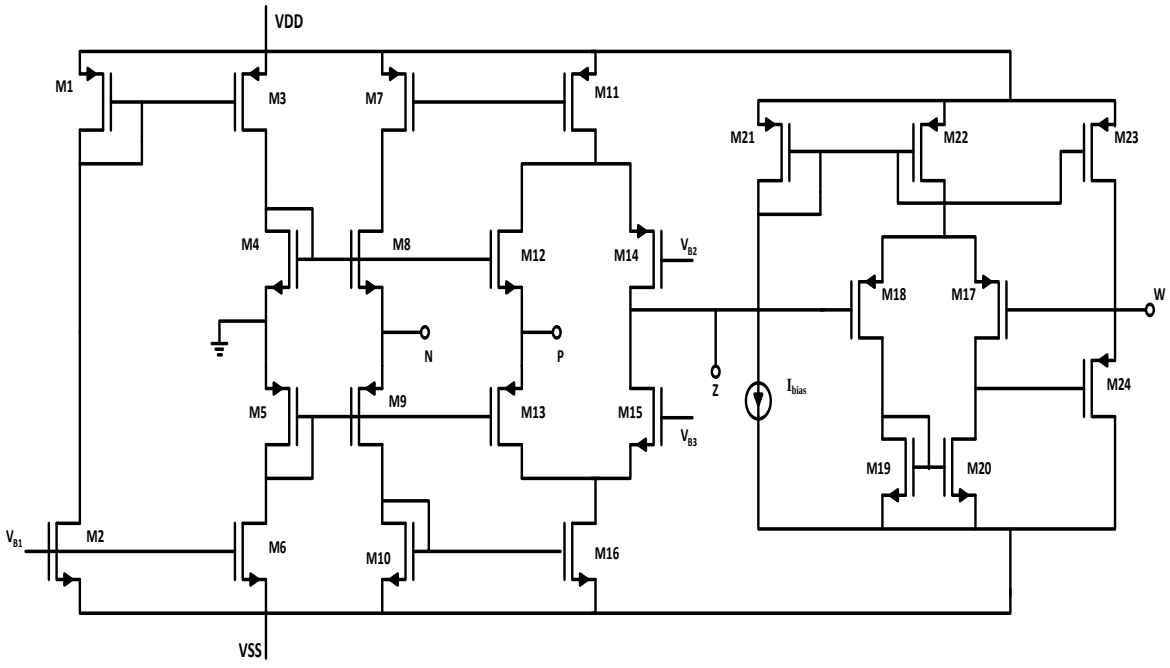

Fig 2.6 CMOS Implementation of CDBA [35]

The W/L ratios of CDBA is shown in table 2.1.

Table 2.1: W/L ratios of CDBA

Transistor	W/L
M1-M13,M16	$36\mu/0.18\mu$
M14-M15	$18\mu/0.18\mu$
M17 – M18, M21-M22	$0.9\mu/0.18\mu$
M19 –M20	$18\mu/0.18\mu$
M23	$3.6\mu/0.18\mu$
M24	$36\mu/0.18\mu$

2.3 CDBA Characterization :

TheSPICE schematic used for CDBA characterization is shown in Fig 2.7. The value of Vb1, Vb2, Vb3 is 0V, -0.9, 0.25V respectively. The Value of bias current I_{bias} is 20µA.The supply voltage used for the device is ±0.9V. The circuit is simulated using 0.18µm technology node.

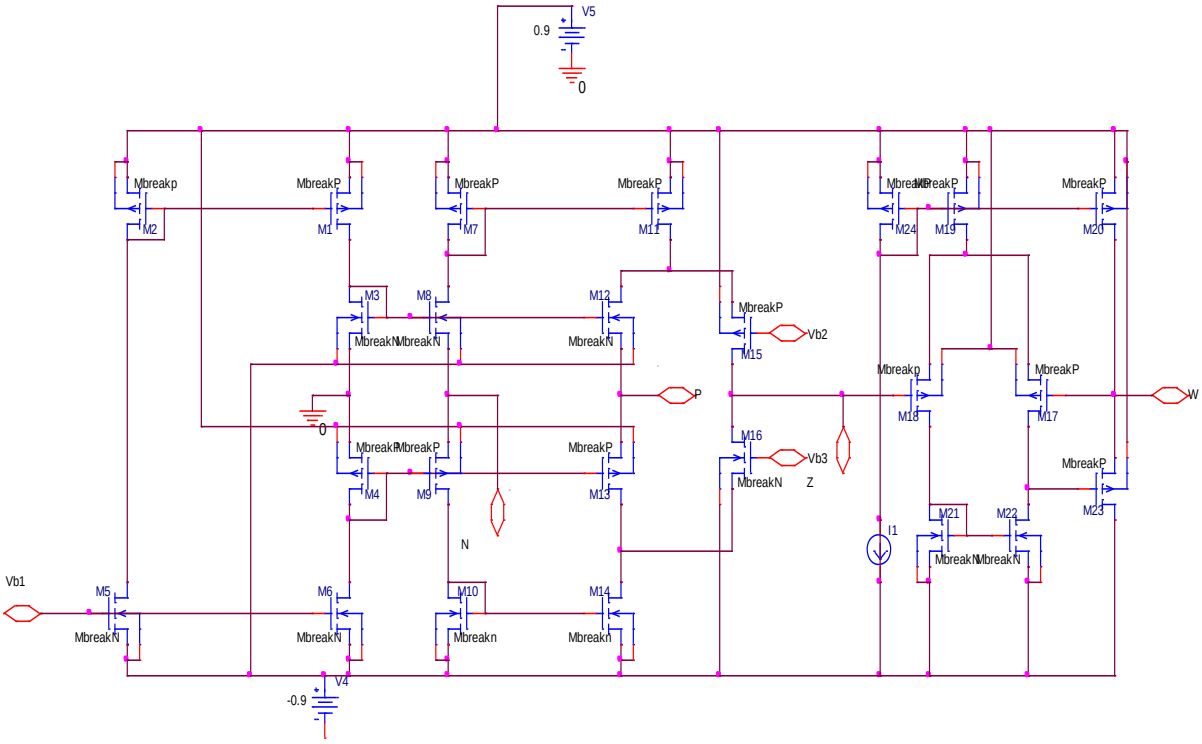

Fig 2.7 Schematic of CDBA characterization

2.3.1 Input Impedance at P and N terminal :

For measurement of impedance at input terminal, the terminals other than input terminal are kept open and then a test AC input signal is applied to the terminal at which the impedance is to be measure. After that the ratio of voltage and current of this test signal is plotted w.r.t. to frequency. From the Fig. 2.8, the impedances seen at these terminal are small. The input impedances Z_p and Z_n also have inductive components in them which in turn negatively affect the normal behavior of circuit by increasing the values of impedances at high frequencies [21] as observed in Fig.2.8. The measured value of these impedances from their corresponding frequency responses are as follows:

$$Z_P = Z_N = 121.977\ \Omega$$

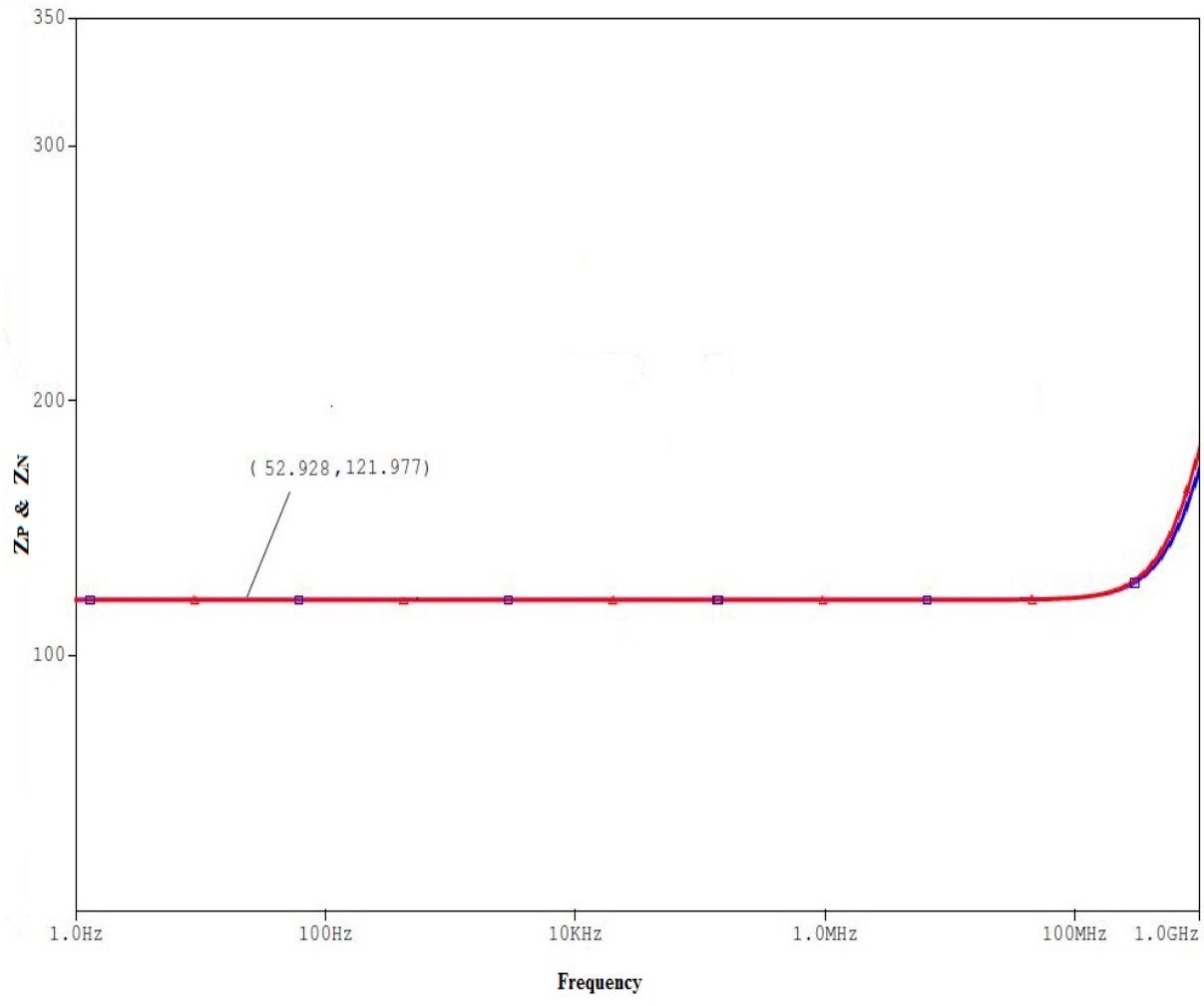

Fig 2.8 Impedance seen from P or N terminal of CDBA

2.3.2 Output Impedance at Z terminal :

For measurement of impedance at output terminal Z, the input terminals are kept grounded and then a test AC input signal is applied to the terminal at which the impedance is to be measured. After that the ratio of voltage and current of this test signal is plotted w.r.t. to frequency. From the Fig. 2.9, the impedance seen at Z terminal is found to be large. The measured values of the impedance from corresponding frequency response is as follows:

$$Z_Z = 548.361\ k\Omega$$

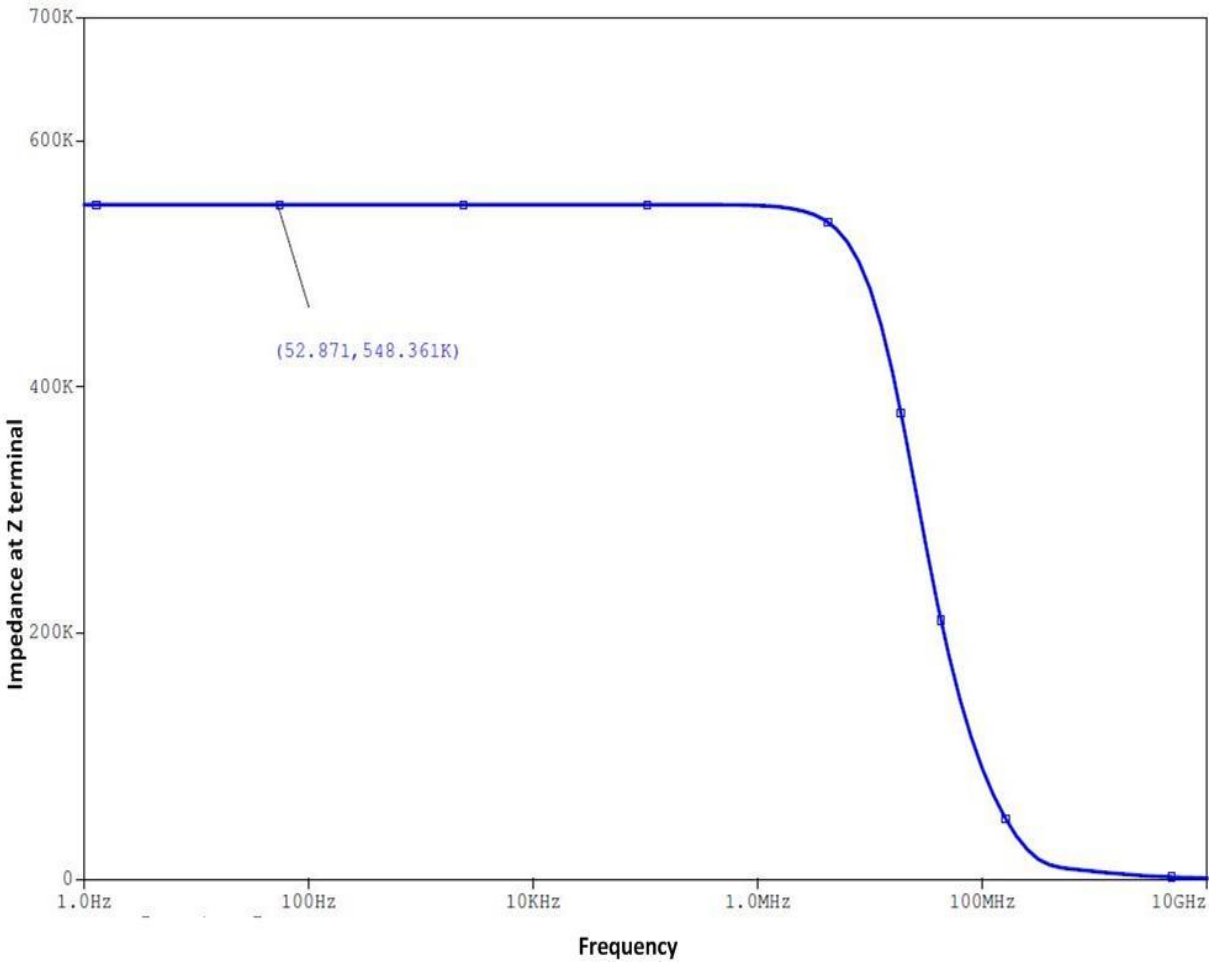

Fig 2.9 Impedance seen from Z terminal of CDBA

2.3.3 Current Transfer Characteristics of Current Differencing Unit :

To verify the current dynamic range along with the verification of current tracking from P to Z, DC curves I_Z v/s I_P (with $I_N = 0$) plotted as shown in Fig. 2.10. To obtain this plots, current at terminal is varied from -100μA to 100μA. The linearity range or the range in which output current follows the input current is from -50 μA to 100 μA.

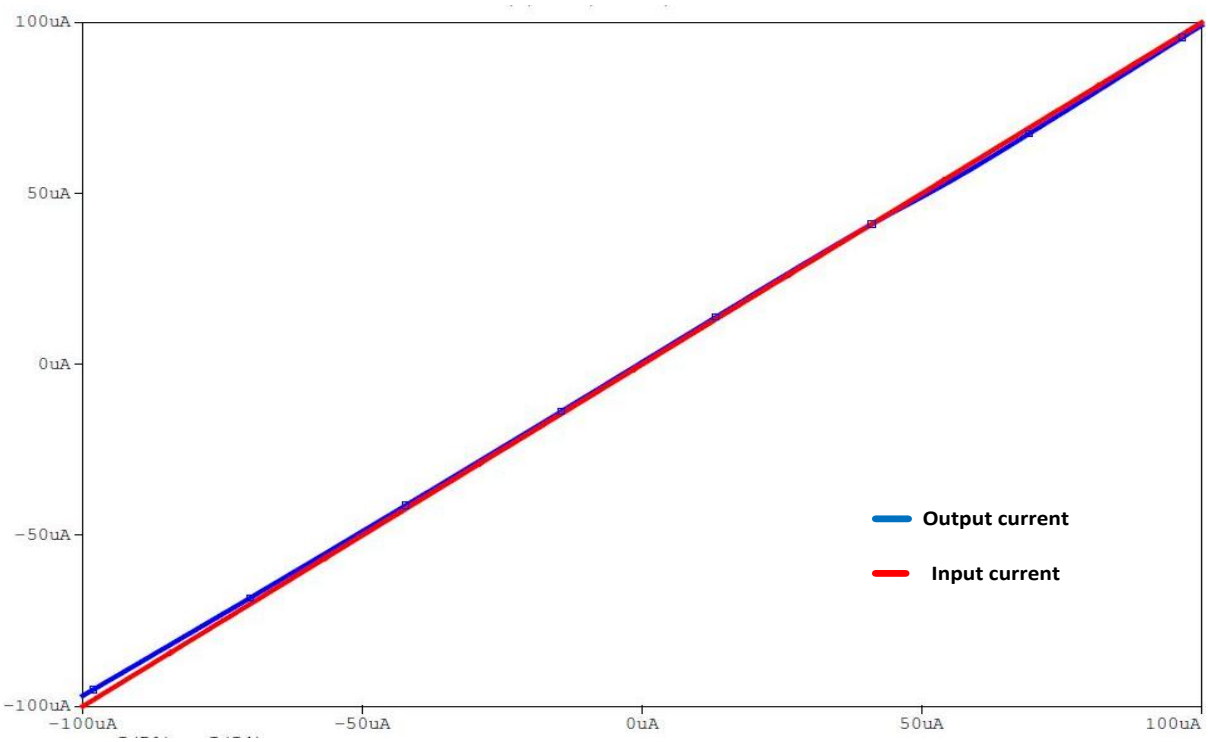

Figure 2.10 Current transfer characteristics from P to Z of CDBA

Current gain is defined as ratio of the output current to input current. To plot variation of the current gain with frequency apply ac source at input terminal and take the ratio of the output and input current w.r.t. frequency. The frequency response of current gain is shown in Fig 2.11. The observed value of current gain β and tracking error is: $\beta = 1.0828$ $\in = 0.0828$ respectively.

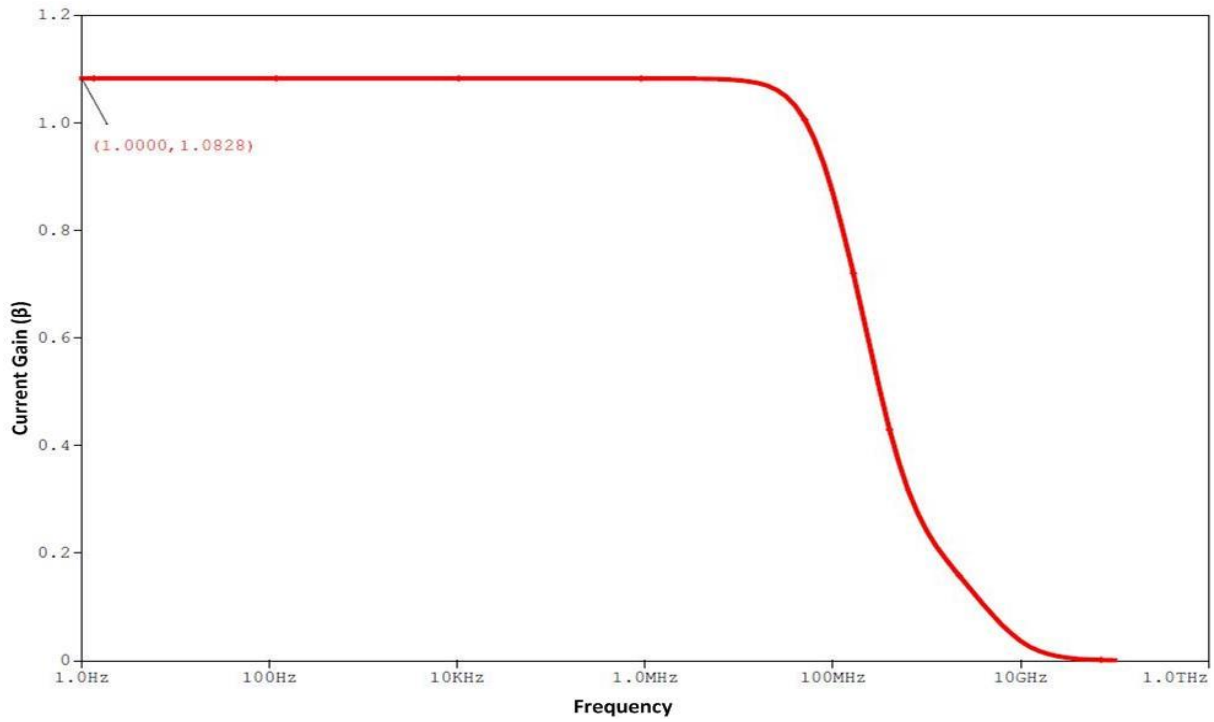

Fig 2.11 Frequency response of current gain

2.3.4 Output Impedance at W terminal :

For measurement of impedance at output terminal W, the input terminal for buffer amplifier i.e. Z is kept grounded and then a test AC input signal is applied to the terminal at which the impedance is to be measured. After that the ratio of voltage and current of this test signal is plotted w.r.t. to frequency. From the Fig. 2.12, the impedance at Z terminal is found out to be large. At higher frequency parasitic comes into role which increases the impedance value.

The values of the measured impedance the corresponding frequency responses is as follows:

$$Z_W = 71.588\ \Omega$$

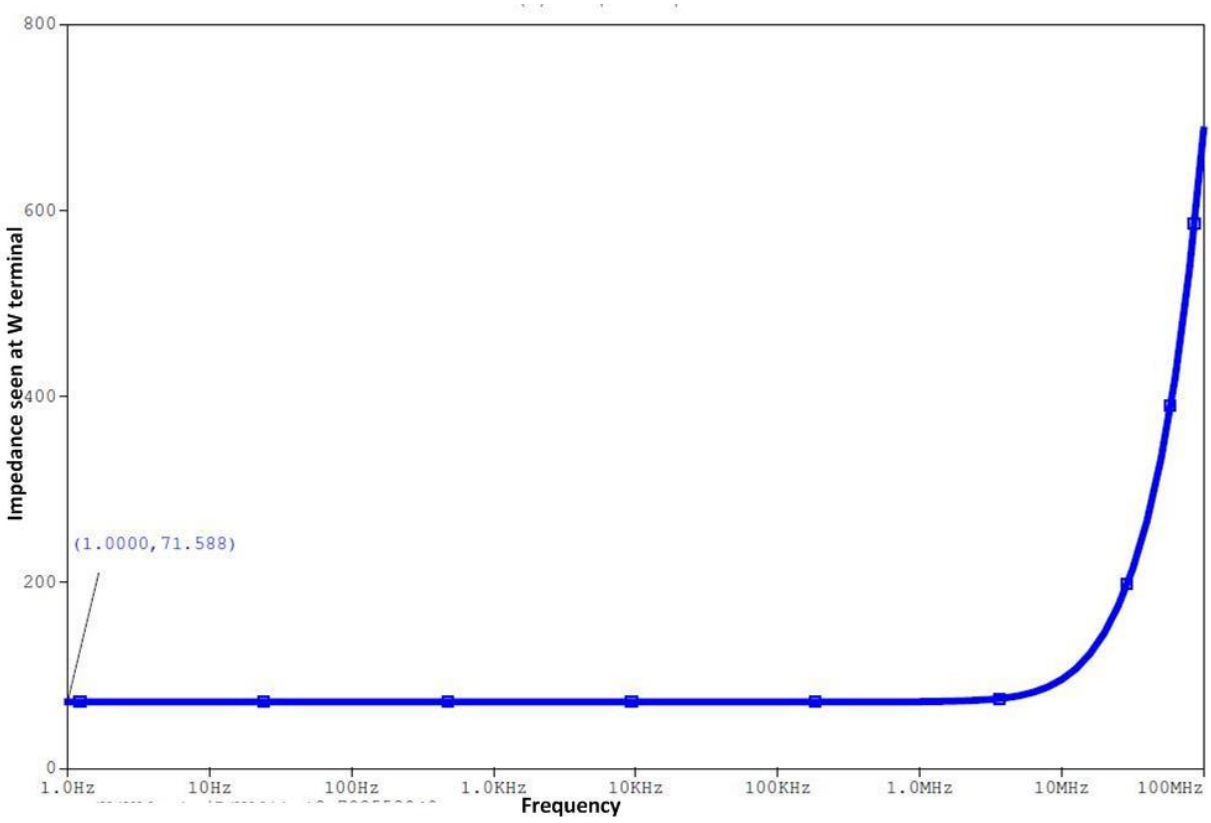

Figure 2.12 Impedance seen from W terminal of CDBA

2.3.5 Voltage transfer Characteristics of Buffer Stage :

The voltage transfer characteristic can be plotted by connecting DC source at input of buffer stage and then by doing DC sweep of that source and measuring voltage at the output. The tracking behavior as shown in Fig 2.13 shows that in buffer stage output voltage follows the input voltage between -0.3V to 0.6V.

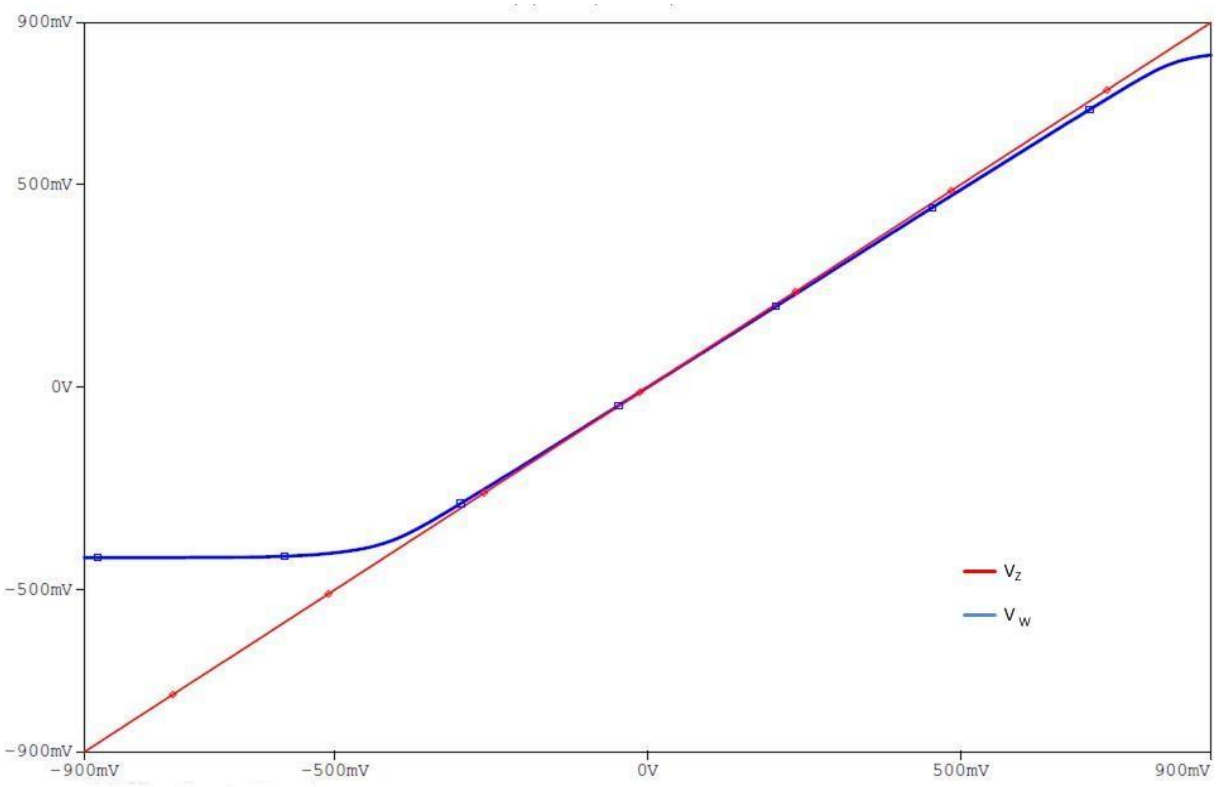

Fig 2.13 Voltage Transfer Characteristics of Buffer stage of CDBA

There is some error in input and output voltage levels in linear range which is known as tracking error. The Plot for tracking error is shown in Fig 2.14 which obtained by subtracting input and output voltage. The range in which tracking error is zero denotes the range in which ouput voltage follows the input voltage.

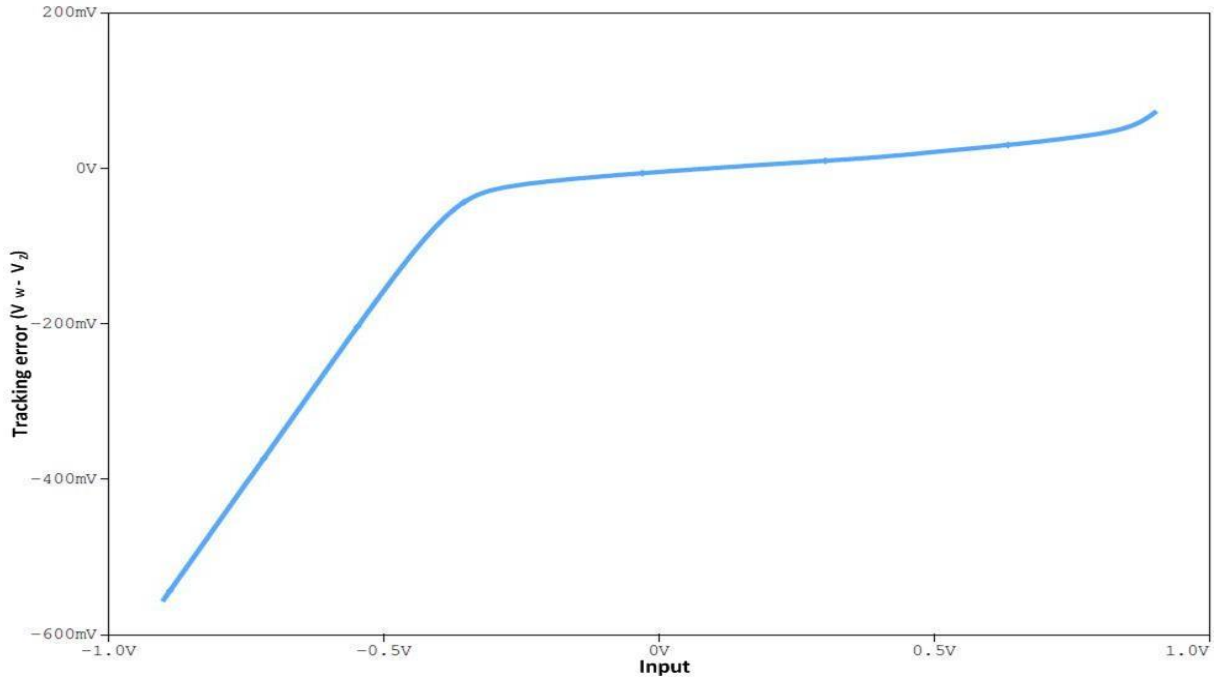

Figure 2.14 Tracking error of Buffer stage of CDBA

2.3.6 Frequency Response of Voltage Transfer Ratio of Buffer Stage :

For plotting the frequency response of voltage transfer ratio of buffer stage the input is applied with ac signal and output voltage is taken. After that ratio of output to input is taken to plot voltage transfer ratio. It is shown in Fig 2.15, and its value is very close to unity (A_v = 0.947856) which is desired value for ideal buffer stage.

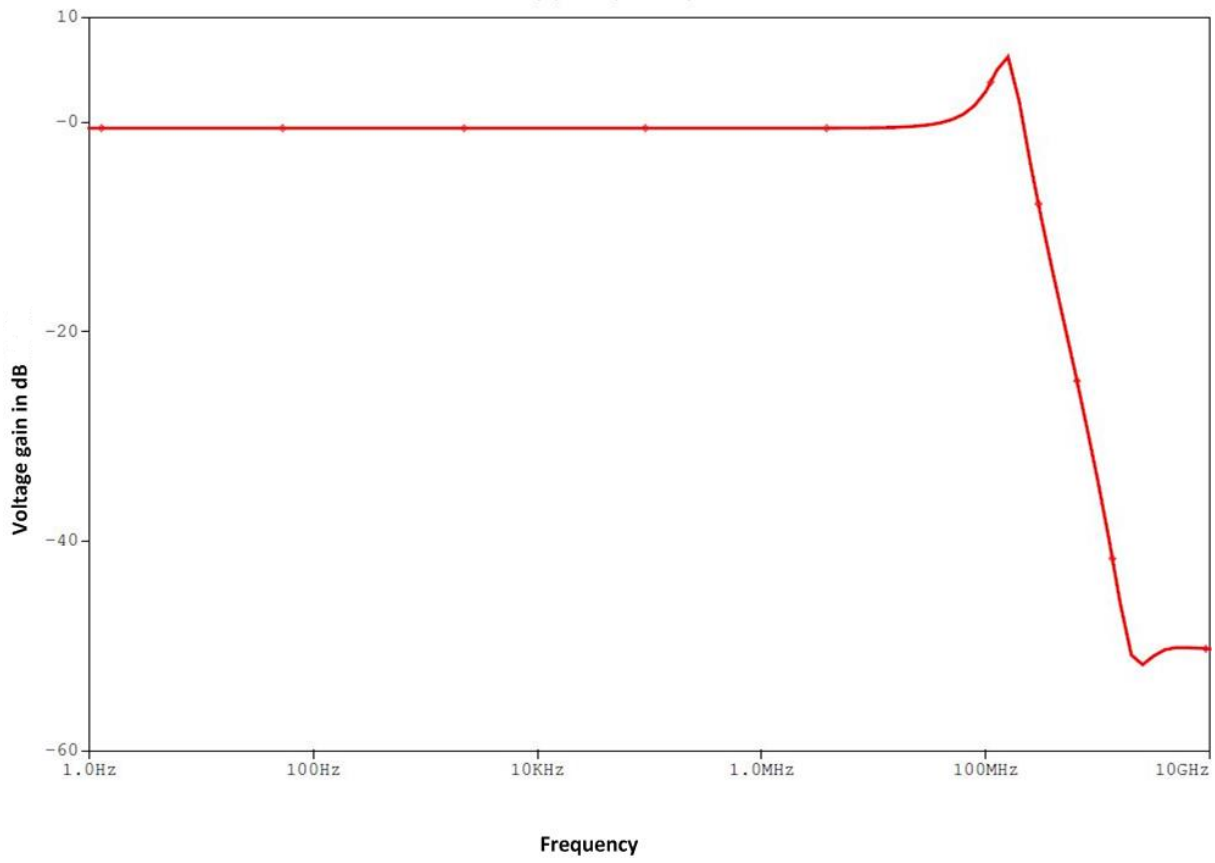

Fig 2.15 Frequency Response of Voltage Transfer Ratio of Buffer Stage of CDBA

2.4 Summary :

In the last, it can be summarized that this chapter presents the CFOA based realization of CDBA and CMOS based CDBA realization . Also, the characteristics of CMOS based CDBA is also observed in this chapter by SPICE simulations.

CHAPTER 3

Modified DTMOS Based CDBA

3.1 Introduction :

In first chapter we had discussed the need of low power technologies to meet the requirement of market and to increase the battery life. There we also discussed different technologies to fulfill this requirement. One such technology i.e. DTMOS (dynamic threshold MOS) is also briefly discussed there. In this chapter we will discuss the DTMOS in detail and after that utilize this technology for implementing the CDBA so that supply voltage of CDBA can be reduced. The characteristics of implemented CDBA is also observed in this chapter by SPICE simulation using 0.18um technology.

3.2 DTMOS :

In the few years need for low-power and high-performance digital systems has increased rapidly. Different circumstances are the reasons for this fast growth. First, computers and laptop, notebook and personal communication systems have gained fame. As a result of which, portable applications those traditionally needs a modest performance (such as calculators & wrist watches), are now dominated by gadgets which demand a very high performance. The demand for these new portable systems limits their battery size and weight which results in severe restriction on their power dissipation. Second, density, speed, and size of non-portable CMOS based systems have increased considerably in recent years. Therefore, power consumption which was not a concern in these systems, now becoming a crucial parameter. The power delivered in CMOS circuit is directly proportional to square of supply voltage as given by equation (3.1):

$$P = CV_{DD}^2 f \tag{3.1}$$

Where C is the total switching capacitance, V_{DD} is the supply voltage or swing across the capacitor and f is the switching fequency.

Though the decreasing of power supply less than three times the threshold voltage i.e. $3V_T$ will result in degradation circuit speed extensively, therefore the scaling of the power supply must be accompanied by threshold voltage reduction [19]. But lower limit of V_T is set by the amount of off state leakage current that can be tolerated. The relation between V_T and lekage current is given in equation (3.2).

$$I_D = I_0 e^{\frac{q}{nk_BT}(V_{gs} - V_T + \gamma V_{bs} + \eta V_{ds})} \left(1 - e^{\frac{-qV_{ds}}{k_BT}}\right) \quad (3.2)$$

It has been seen that if standard MOSFET's are used below a lower bound for power supply voltage then a larger leakage current become unavoidable. Thus to reduce Supply Voltage, DTMOS was proposed. Thus to reduce Supply Voltage to ultra-low voltages (0.6 V and below) a Dynamic Threshold Voltage MOSFET (DTMOS) was introduced, which have a high V_T at zero input bias and a low V_T at high input bias.DTMOS is abbreviation for Dynamic threshold metal oxide semiconductor.

3.2.1 Idea behind DTMOS :

As for ideal operation of any device that it provides excellent performance when it is under operation and gives zero power dissipation when it is in off state. Therefore, for practical MOSFET it can stated as it must provide high current driving capability when it is under operation or in on state and negligible leakage current when it is ideal state or off state. This is the key idea behind origin of DTMOS. In DTMOS when no input is applied in between gate and source terminal i.e. Vgs =0 then the value of V_T remain same as conventional MOSFET and when applied input i.e. Vgs increases then V_T must decreases consequences of which results in larger current driving capability than a standard MOSFET at lower power supply. V_T.

For DTMOS: $V_T = V_{T0}$ at Vgs = 0

V_T= lowest V_T at Vgs = Vdd.

Now let us consider the equation of threshold voltage as given below by equation (3.3)

$$V_T = V_{T0} + \gamma \left(\sqrt{|2\varphi_F| + V_{SB}} + \sqrt{|2\varphi_F|}\right) - \eta V_{DS} \quad (3.3)$$

In equation (3.3),

φ_F is Fermi potential of bulk, V_{SB} is source to bulk voltage,

V_T is the threshold voltage when $V_{SB} \neq 0$ i.e the bulk and source are at different potential,

V_{T0} is threshold voltage when $V_{SB} = 0$ i.e. the bulk and substrate are at same potential.

γ is called Body effect coefficient and is given by:

$$\gamma = \frac{\sqrt{2qN_A \in_{Si}}}{C_{ox}} \quad (3.4)$$

Typical value of γ is 0.4 .

ηV_{DS} represents the effect of DIBL and typical value of η is 0.02 – 0.1 .

From equation (3.3) it is evident that when the Body to source junction is forward biased (at less than 0.6V) causes the threshold voltage to drop. This is due to reason that when bulk potential is increased positively then this results in reduction of junction width and hence depletion region charge density and therefore V_T reduces and when the body to source is reverse biased i.e. the body potential is decreased then it results in Reverse bias of junction consequently increases the depletion region width and hence increases body charge due to which V_T increases. This is the operation of DTMOS. Since threshold voltage of MOSFET is changed dynamically that is why it is called dynamic threshold MOSFET.

This is not with the conventional MOSFET, because in conventional MOSFET bulk is kept at constant potential using a biasing (usually kept at lowest potential in the circuit).

As in case of DTMOS based circuit, when input is high i.e. transistor is on this results on reduction of V_T and therefore higher driving capability when device is ON. and when Vin or Vgs =0 then V_T is high and hence results in low leakage current. Thus DTMOS enables, the circuit to operates under low voltage supply, hence suitable for low voltage, low power application.

3.2.2 Structure of DTMOS :

DTMOS can be built by two techniques.

a. Simply connecting bulk and gate.
b. SOI (Silicon On Insulator)

a. Simply connecting bulk and gate :

DTMOS can be simply by connecting body and bulk of transistor as shown in Fig 3.1. However, the same technique cannot be functional to NMOS transistor in the conventional bulk- CMOS technology this is because of reason that on Integrated circuit all NMOS transistors share the common substrate therefore if it is applied to NMOS then it will affect all devices on chip.It can only be applied to PMOS transistors because every PMOS transistor is fabricated in its own N well.

To extend the application of DTMOS to NMOS we can use triple well technique which is very expensive as the fabrication cost increases.

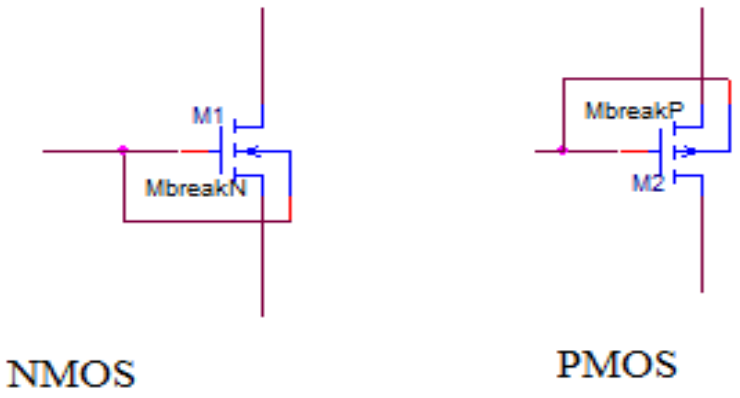

Fig 3.1 DTMOS by Simply connecting bulk and gate

b. SOI (Silicon On Insulator) :

In SOI many author's tried to take advantage of the extra current produced by the lateral bipolar transistor to explain the operation of DTMOS.This requires body voltage to 0.6V or larger. The extra drain current comes at the expense of the large input (base) current which contributes more to leakage current than drain current. Large improvement in I_D is achieved at gate voltage less than 0.6V.Same idea can be achieved in bulk devices but isolation of the MOSFET body can be accomplished more easily in SOI because of very small junction areas and hence the capacitance can be much less than a bulk MOSFET. Also DTMOS technique can be applied to both NMOS and PMOS in the SOI technology. SOI based DTMOS is shown in Fig 3.2 [20].

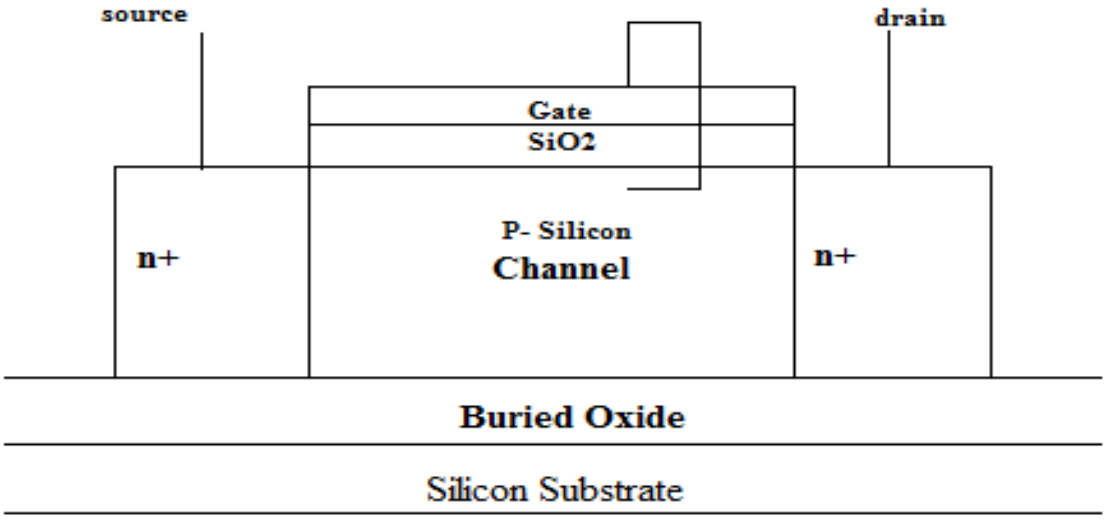

Fig 3.2 SOI-based DTMOS [20]

3.2.3 Characteristic comparison of DTMOS with conventional MOSFET :

The I_D Vs V_{GS} graph i.e. transfer characteristics of DTMOS and conventional MOSFET is shown in Fig 3.3. The graph is simulated using NMOS at 0.18um technology while keeping the drain to source voltage constant at 0.4 V. It is observed from graph that threshold voltage of DTMOS is reduced than conventional MOSFET. It is observed that threshold voltage of DTMOS is reduced to 0.302V from 0.375V.

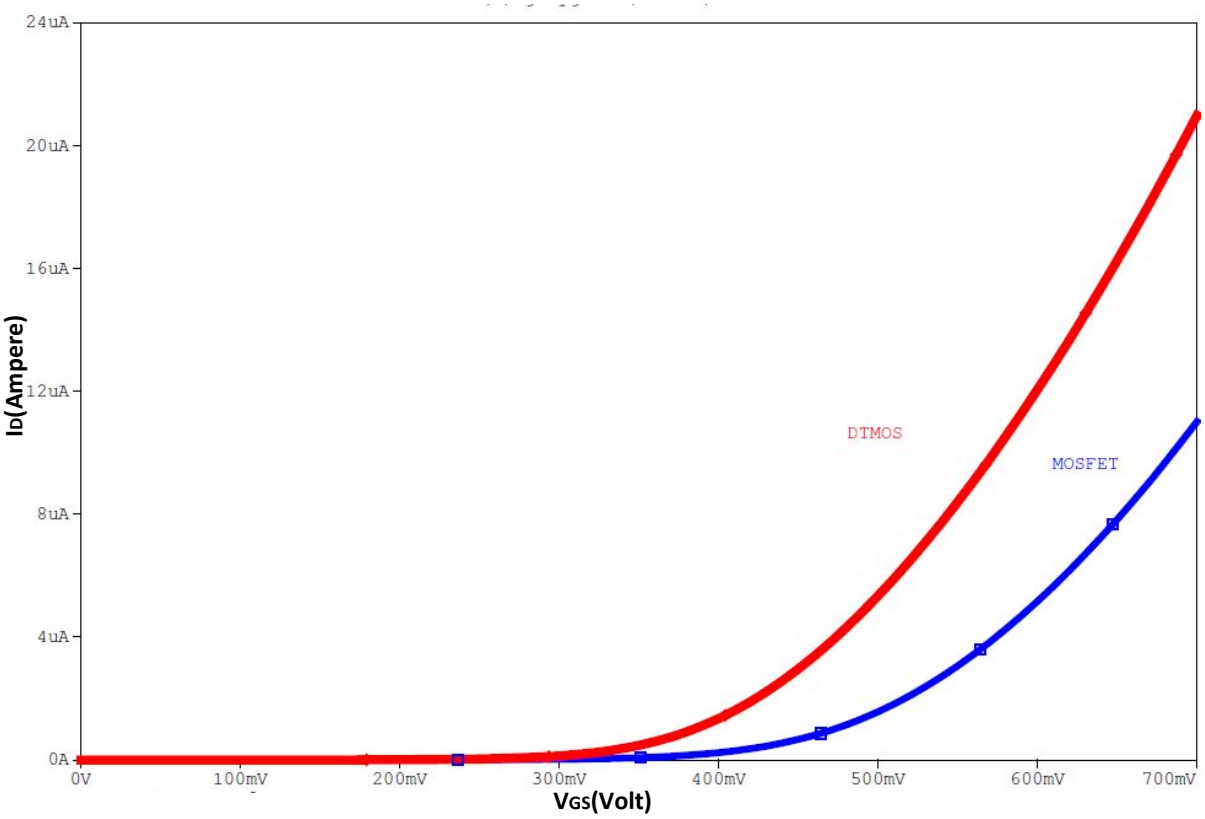

Fig 3.3 Transfer characteristic comparison of DTMOS Vs MOSFET

The plot I_D Vs V_{DS} i.e. output characteristics of DTMOS and conventional MOSFET is shown in Fig3.4. The plot is obtained by keeping V_{GS} at constant voltage of 0.4 volt. It is observed that current driving capability of DTMOS is larger than conventional MOSFET. The current driving capability for a given point i.e at drain to source voltage of 376.744mV is 5.65 times than that of conventional MOSFET.

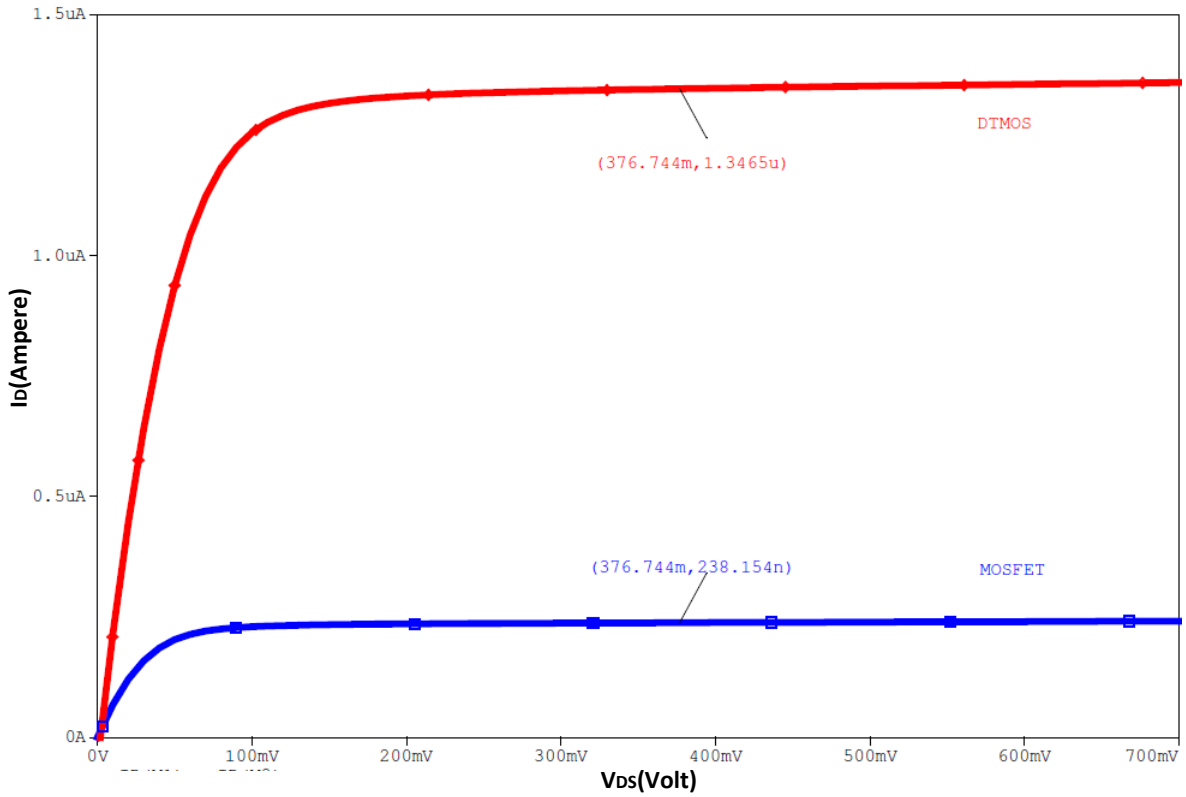

Fig 3.4 Output characteristic comparison of DTMOS Vs MOSFET

3.2.4 Transition frequency :

Transition frequency is the frequency at which the gain of the MOSFET is one or unity. It is called transition because transistor transitions from amplifier to attenuator.It is also called as unity gain bandwidth because at this frequency gain is unity.

Transition frequency of MOSFET is given by equation (3.5):

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{3.5}$$

As transistor is biased in saturation region, Therefore the capacitance, $C_{gs} = \frac{2}{3}C_{ox}WL + C_{ox}WL_D$ is greater than $C_{gd} = C_{ox}WL_D$

Therefore,

$$f_T = \frac{g_m}{2\pi C_{gs}}$$

similarly for DTMOS, transition frequency is given by equation (3.6):

$$f_T = \frac{g_m + g_{mb}}{2\pi C_{gs}} \tag{3.6}$$

Therefore, it is illustrated from the equation (3.5) and equation (3.6) that the transistion frequency or unity gain bandwidth of DTMOS is higher than conventional MOSFET because trans-conductance gain of DTMOS is larger in value than conventional MOSFET.

3.3 Realization of DTMOS Based CDBA :

The DTMOS based CDBA is presented in Fig 3.5. The circuit is derived from previous CDBA circuit presented in Fig 2.7. This DTMOS circuit is achieved by connecting the bulk and gate of PMOS transistors in other word by replacing the PMOS transistors of Fig 2.7 with DTMOS.

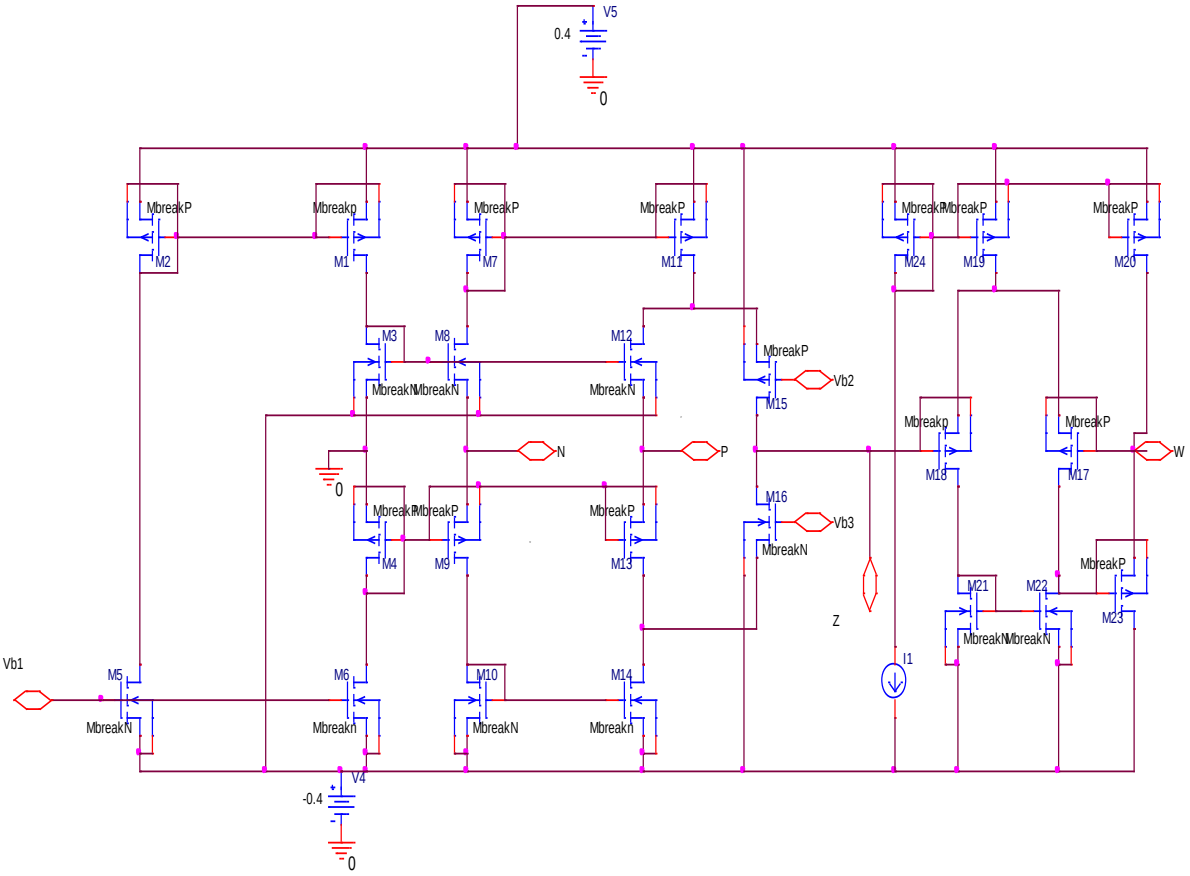

Fig 3.5 DTMOS based CDBA

The W/L ratios of DTMOS based CDBA is shown in table 3.1.

Table 3.1 : W/L ratios of DTMOS based CDBA

Transistor	W/L
M1-M2 , M5-M6	$21.6\mu/0.18\mu$
M3-M4 , M12-M13	$18\mu/0.18\mu$
M7,M10,M11,M14	$90\mu/0.18\mu$
M8-M9	$36\mu/0.18\mu$
M15-M16	$54\mu/0.18\mu$
M17-M20	$1.35\mu/0.18\mu$
M21-M22	$27\mu/0.18\mu$
M23	$54\mu/0.18\mu$
M24	$1.35\mu/0.18\mu$

3.4 Characterization of DTMOS based CDBA :

The DTMOS based CDBA is characterized by using SPICE at 0.18um technology. The value of Vb1, Vb2, Vb3 is 0V, -0.4, 0.1V respectively. The Value of bias current I_{bias} is 20µA.The supply voltage used for the device is ±0.4V.

3.4.1 Current Transfer Characteristics of Current Differencing Unit :

To verify the current dynamic range along with the verification of current tracking from P to Z, DC curves I_Z v/s I_P (with $I_N = 0$) plotted as shown in Fig. 3.6. To obtain this plots, current at terminal is varied from -40µA to 80µA. The linearity range or the range in which output current follows the input current is from -10.579u µA to 52.231µA.

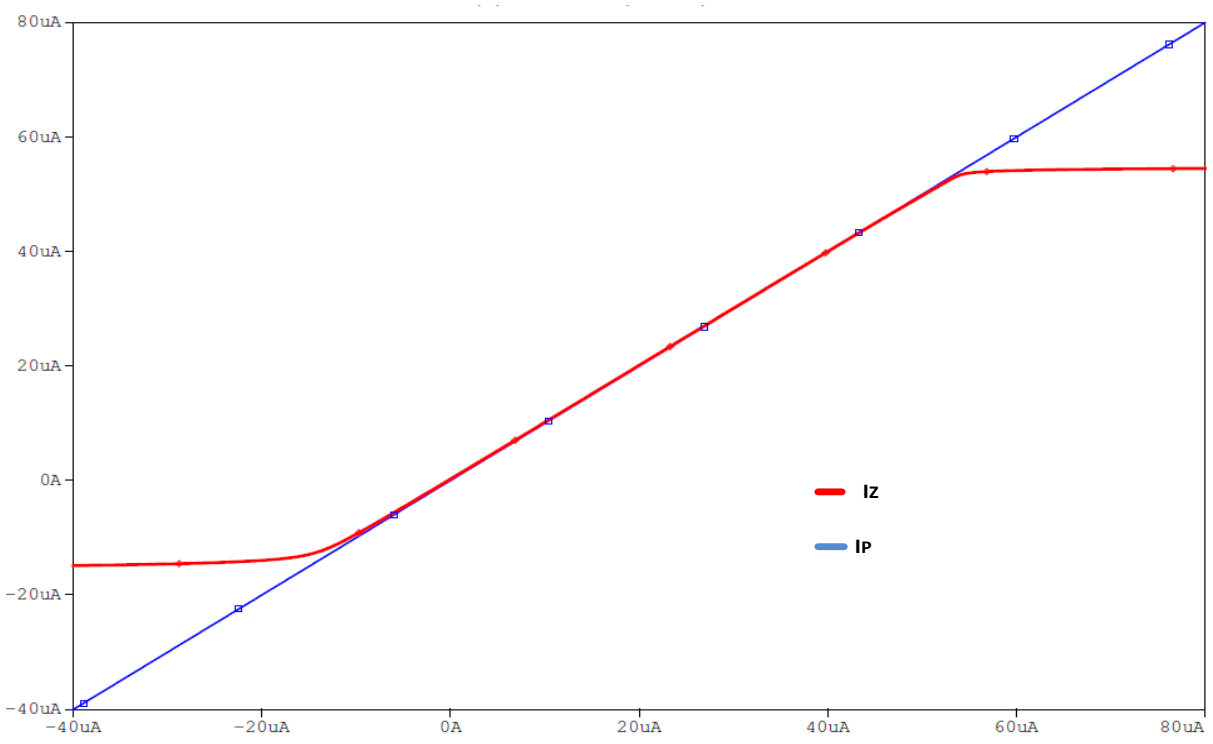

Fig 3.6 Current transfer characteristics from P to Z of CDBA

There is some error in input and output current levels in linear range which is known as tracking error. The Plot for tracking error is shown in Fig 3.7 which obtained by subtracting input and output current. The range in which tracking error is zero denotes the range in which ouput current follows the input current.

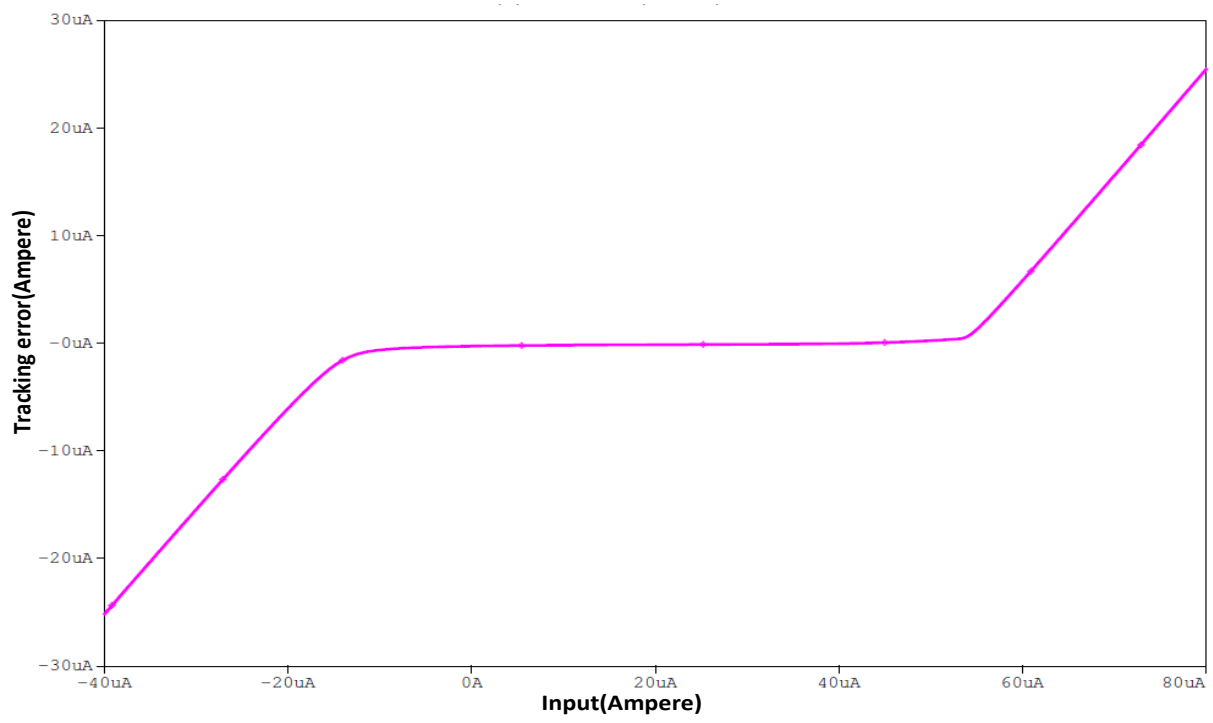

Fig 3.7 Tracking error of current for DTMOS based CDBA

Current gain is defined as ratio of the output current to input current. To plot variation of the current gain with frequency apply ac source at input terminal and take the ratio of the output and input current w.r.t. frequency. The frequency response of current gain is shown in Fig 3.8. The observed value of current gain β and tracking error is: $\beta = 0.969670$ $\in = 0.03033$ respectively**.**

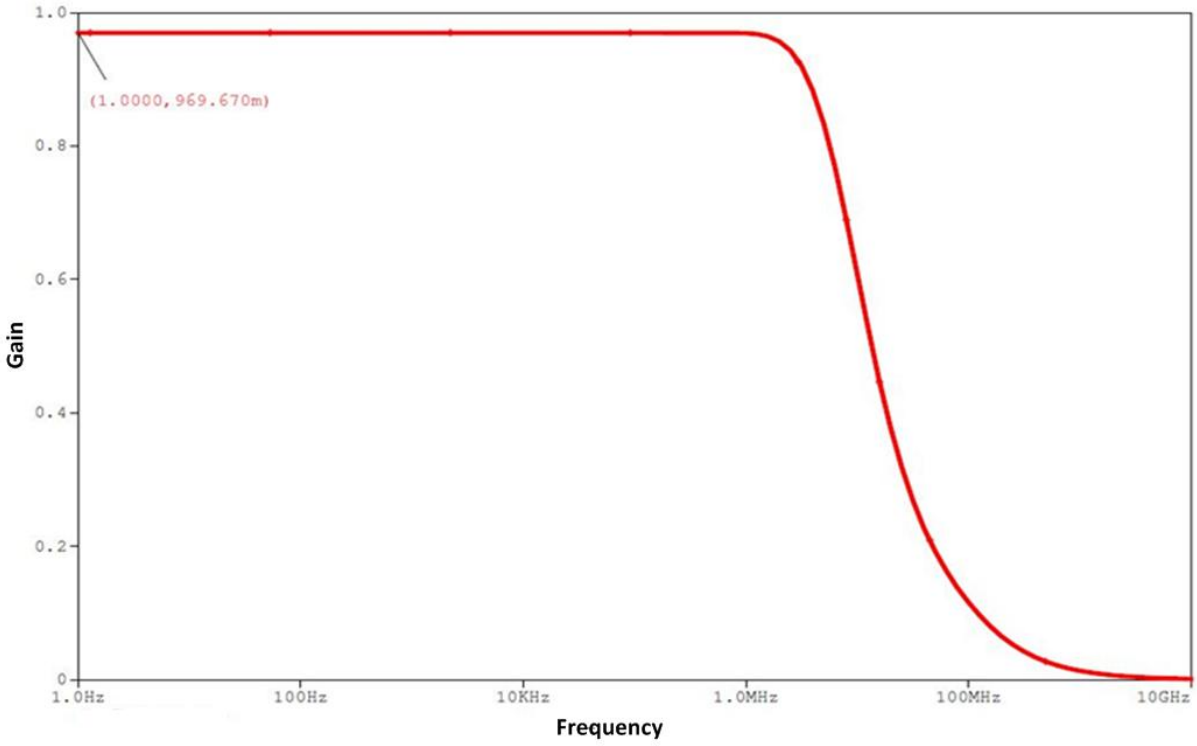

Fig 3.8 Frequency response of I_z/I_p

3.4.2 Voltage transfer Characteristics of Buffer Stage :

The voltage transfer characteristic can be plotted by connecting DC source at input of buffer stage and then by doing DC sweep of that source and measuring voltage the output terminal. It is shown in Figure 3.9.The tracking behavior as shown in Figure 3.10 shows that in buffer stage output voltage follows the input voltage between -0.091V to 0.31V .

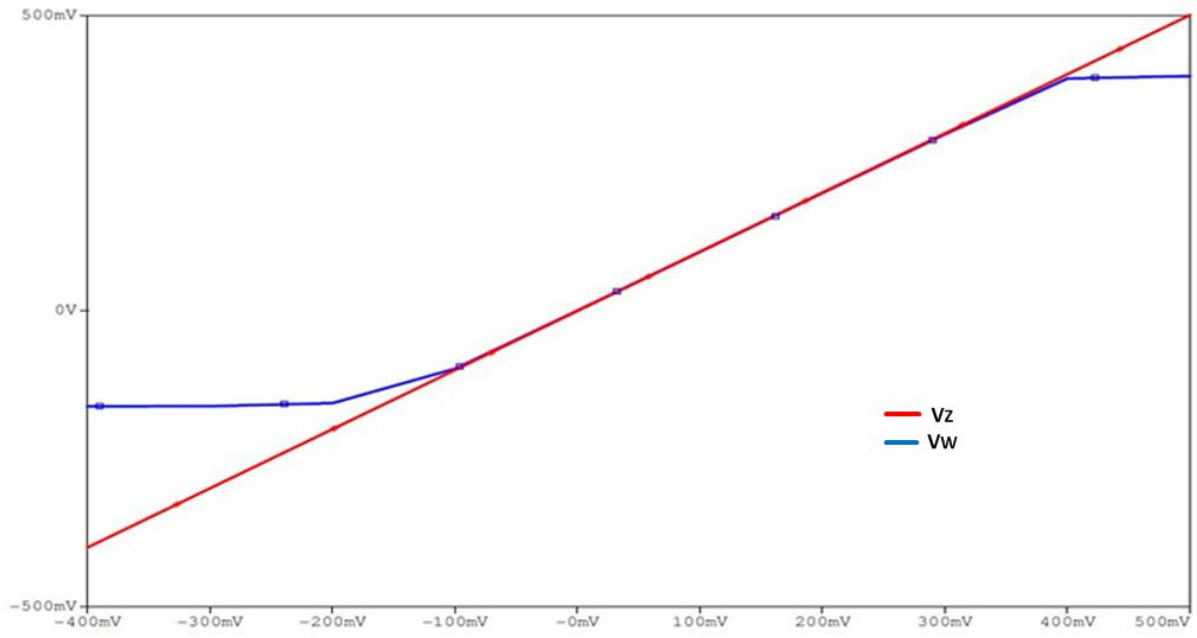

Fig 3.9 voltage transfer characteristics for DTMOS based CDBA

There is some error in input and output voltage levels in linear range which is known as tracking error. The Plot for tracking error is shown in Fig 3.10 which obtained by subtracting input and output voltage. The range in which tracking error is zero denotes the range in which ouput voltage follows the input voltage.

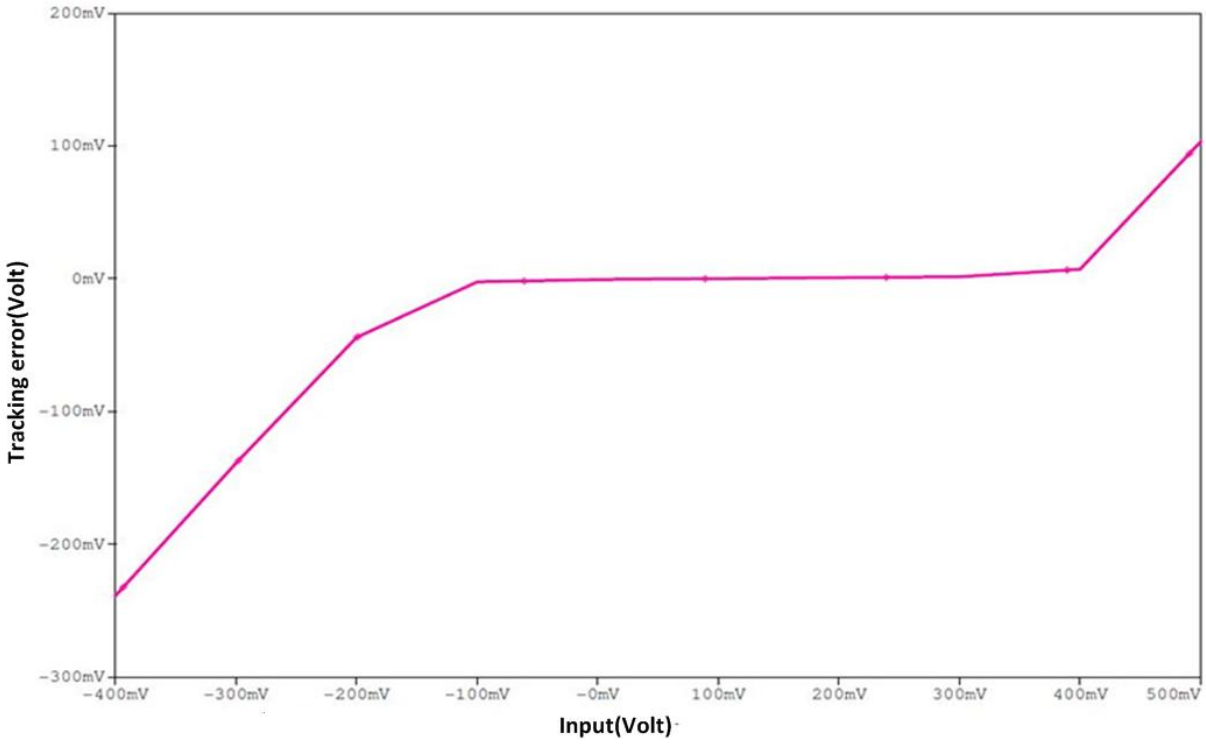

Fig 3.10 Tracking error of voltage transfer characteristics for DTMOS based CDBA

3.4.3 Frequency Response of Buffer Stage :

For plotting the frequency response of voltage transfer ratio of buffer stage the input is applied with ac signal and output voltage is taken. After that ratio of output to input is taken to plot voltage transfer ratio. It is shown in Figure 3.11, and it's value is very close to unity (Av = 0.961912) which is desired value for ideal buffer stage.

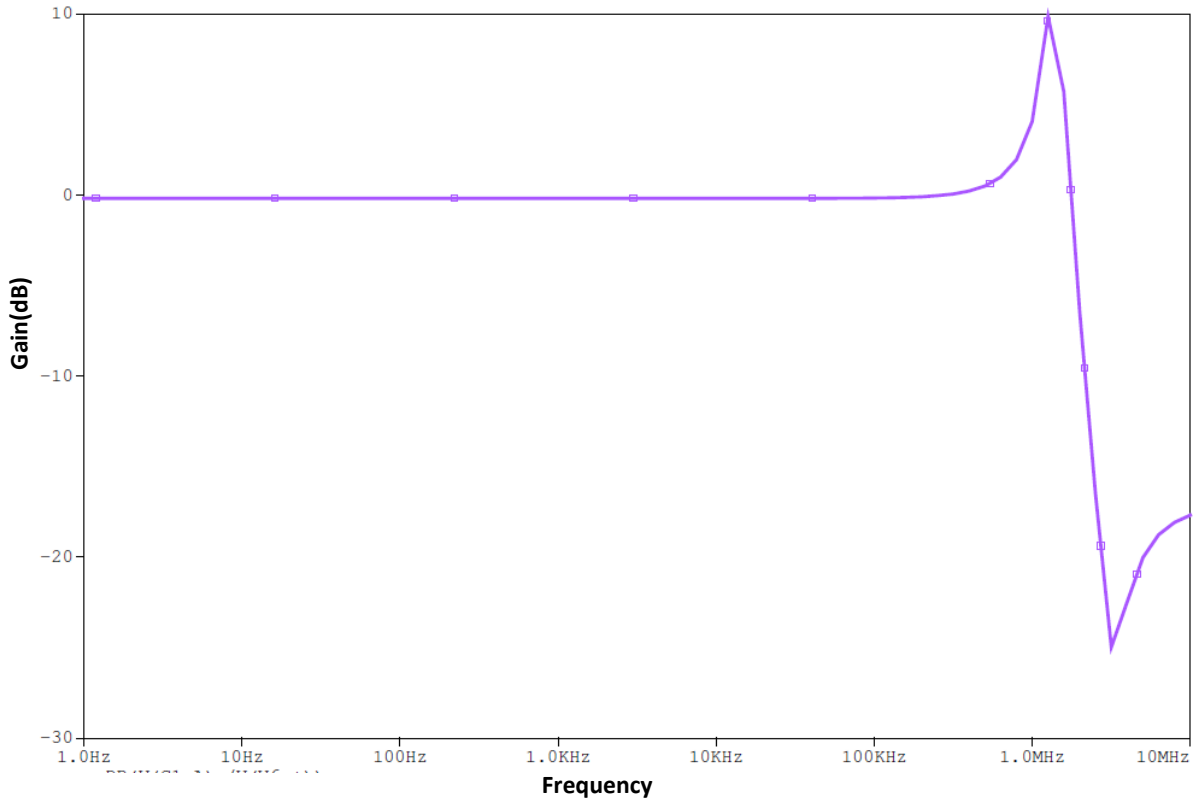

Fig 3.11 Frequency response of Buffer stage

3.5 Summary :

In the last, it can be summarized that this chapter presents the DTMOS technology, later which utilized for realization of CDBA. Therefore, DTMOS based CDBA is presented in this chapter also it's characteristics are observed using SPICE simulation.

CHAPTER-4

APPLICATION

4.1 Introduction :

Universal filters can be classified based on their topology is: variable and fixed topology type. The latter is further divided into voltage mode (VM), current mode (CM) and mixed mode (MM) types, each of which is further subdivided based on how responses are obtained w.r.t. combinations of input's and output's: i) single-input multiple-output (SIMO) type filters, ii) multiple-input single-output (MISO) type filters, and iii) multiple-input multiple-output (MIMO) type filters.

The biquad circuits working in mixed-mode can be operated in voltage, current, transimpedance, and trans-admittance modes. One of the most widely used universal analog filters topology is a MISO type VM filters.

By simply switching on or off the input voltages or by doing the same along with their different combinations, various filter functions is realized simultaneously. One such filter based on CDBA is implemented in this chapter. In this chapter we present MISO type CDBA based voltage mode universal filter which is simulated by utilizing CMOS based CDBA and DTMOS based CDBA which were discussed in earlier chapter and verify the working of DTMOS based CDBA.

4.2 Universal Filter Employing CDBA :

The circuit for universal filter by employing CDBA is shown in Fig 4.1.

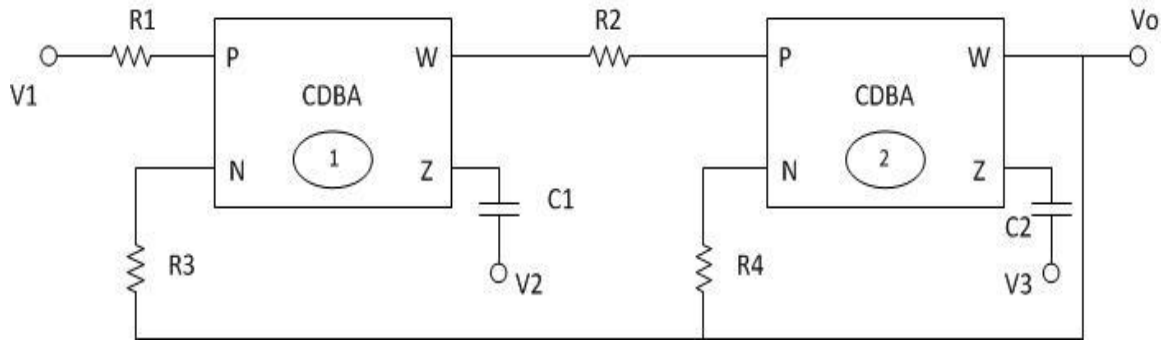

Fig 4.1 Circuit of VM Universal filter using CDBA [44]

Analysing the above circuit by considering the ideal CDBA yields relation between output voltage and input voltages as below :

$$V_O = \frac{s^2V_3 - \left(\frac{s}{R_2C_2}\right)V_2 + \left(\frac{1}{R_1R_2C_1C_2}\right)V_1}{s^2 + \left(\frac{s}{R_4C_2}\right) + \left(\frac{1}{R_3R_2C_1C_2}\right)} \quad (4.1)$$

Above equation can be manipulated for realizing various filters as :

1. **Low Pass Filter (LPF) :**

   Condition for LPF is: $V_2 = V_3 = 0$ and $V_1 = V_{in}$.

   And low pass gain is $H_{LP} = 1$.

   The transfer function is reduced as :

$$V_O = \frac{\left(\frac{1}{R_1R_2C_1C_2}\right)V_1}{s^2 + \left(\frac{s}{R_4C_2}\right) + \left(\frac{1}{R_3R_2C_1C_2}\right)}$$

2. **High Pass Filter (HPF) :**

   Condition for HPF is: $V_1 = V_2 = 0$ and $V_3 = V_{in}$.

   And low pass gain is $H_{HP} = 1$.

   The transfer function is reduced as :

$$V_O = \frac{s^2V_3}{s^2 + \left(\frac{s}{R_4C_2}\right) + \left(\frac{1}{R_3R_2C_1C_2}\right)}$$

3. **Band Pass Filter (BPF) :**

   Condition for BPF is: $V_1 = V_3 = 0$ and $V_2 = -V_{in}$.

   And low pass gain is $H_{BP} = 1$.

   The transfer function is reduced as :

$$V_O = \frac{\left(\frac{s}{R_2C_2}\right)V_2}{s^2 + \left(\frac{s}{R_4C_2}\right) + \left(\frac{1}{R_3R_2C_1C_2}\right)}$$

4. Band Reject Filter (BRF) :

Condition for BRF is: $V_1 = V_3 = V_{in}$ and $V_2 = 0$ and $R_4 = R_2$ and $R_3 = R_1$.

And low pass gain is $H_{BS} = 1$.

The transfer function is reduced as :

$$V_O = \frac{s^2 V_3 + \left(\frac{1}{R_1 R_2 C_1 C_2}\right) V_1}{s^2 + \left(\frac{s}{R_4 C_2}\right) + \left(\frac{1}{R_3 R_2 C_1 C_2}\right)}$$

5. All Pass Filter (APF) :

Condition for APF is: $V_1 = -V_2 = V_3 = V_{in}$ and $R_4 = R_2$ and $R_3 = R_1$.

And low pass gain is $H_{AP} = 1$.

The transfer function is reduced as :

$$V_O = \frac{s^2 V_3 - \left(\frac{s}{R_2 C_2}\right) V_2 + \left(\frac{1}{R_1 R_2 C_1 C_2}\right) V_1}{s^2 + \left(\frac{s}{R_4 C_2}\right) + \left(\frac{1}{R_3 R_2 C_1 C_2}\right)}$$

The natural frequency (ω_0), the bandwidth (BW) and quality factor (Q) for the filter is given by equation (4.2),(4.3) and(4.4) respectively [44].

$$\omega_0 = \frac{1}{\sqrt{R_A R_B C_1 C_2}} \quad (4.2)$$

$$BW = \frac{1}{R_B C_2} \quad (4.3)$$

$$Q = \sqrt{\frac{R_B C_2}{R_A C_1}} \quad (4.4)$$

Where $R_A = R_1 = R_3$ and $R_B = R_2 = R_4$. It can also be noticed that the filter parameter ω_0 and BW are adjustable properly by the virtual- grounded resistor R_A or the capacitor C_1 , and by the virtual- grounded resistor R_B or the capacitor C_2.

4.3 Simulated output :

This filter is designed with natural frequency of 100KHz by considering capacitor values of 1nf and calculating the values of resistors R1,R2,R3,R4 for this which are 4.618K ohms,549.0ohms,4.618K ohms,549.0ohms respectively.

The simulation of filters are done in SPICE using 0.18um technology by using the values of resistors and capacitors as mentioned above and output for both DTMOS based CDBA filters and CMOS based CDBA filters are observed in Fig 4.2 , Fig 4.3 , Fig 4.4 , Fig 4.5 , Fig 4.6 , Fig 4.7.

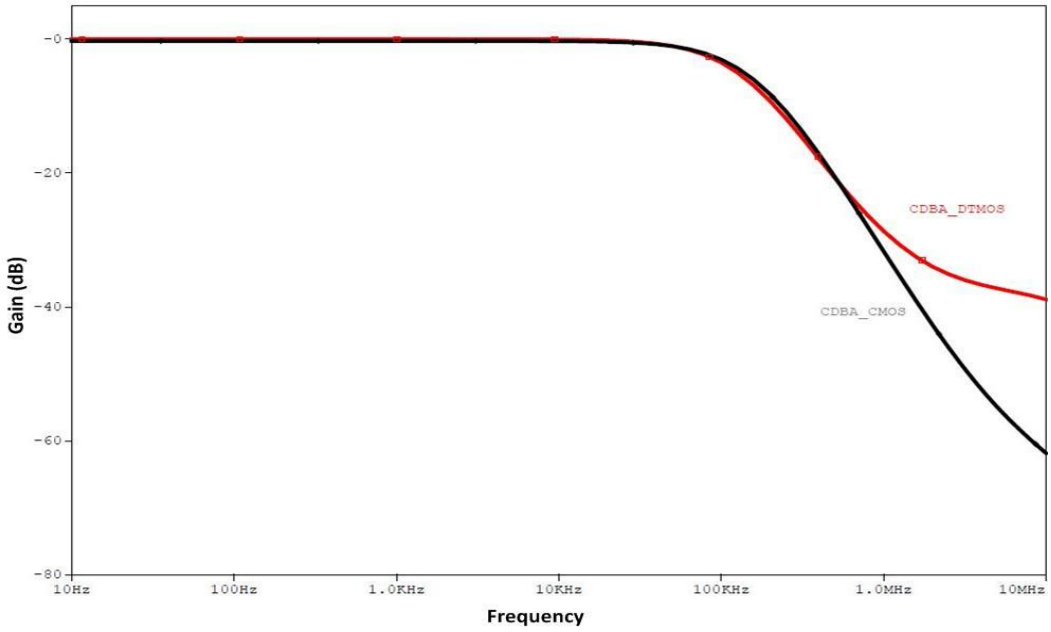

Fig 4.2 Simulated waveform of LPF using DTMOS based CDBA & CMOS based CDBA

From simulated graph the 3dB cut off frequency for CMOS based CDBA and DTMOS based CDBA LPFs are found to be 104.440kHz and 90.803kHz respectively.

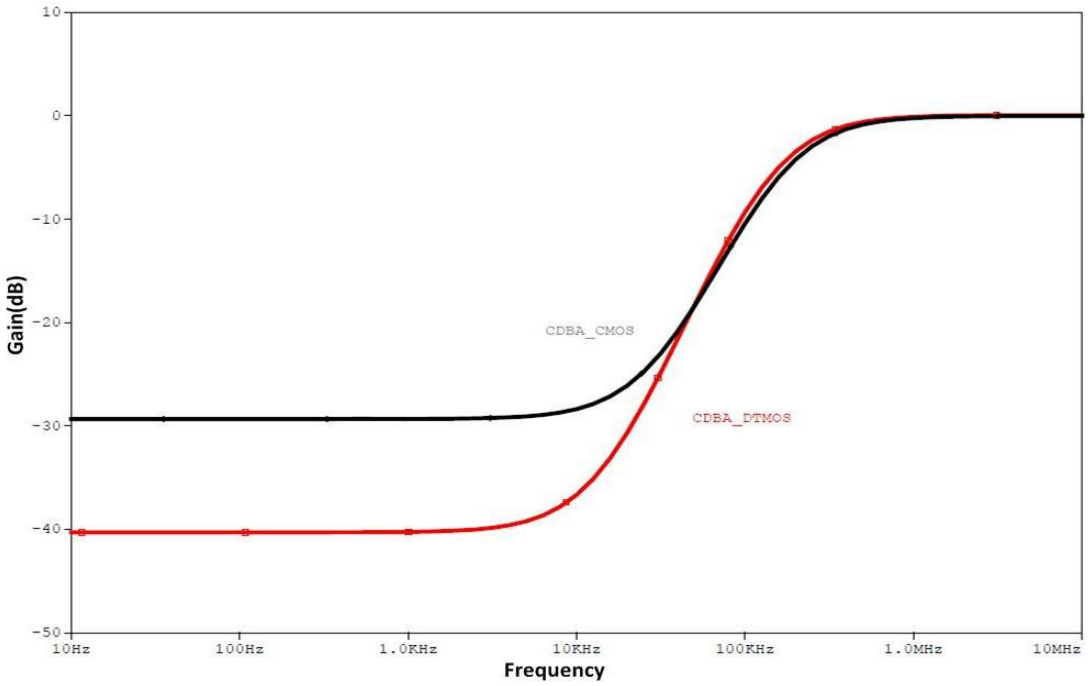

Fig 4.3 Simulated waveform of HPF using DTMOS based CDBA & CMOS based CDBA

From simulated graph the 3dB cut off frequency for CMOS based CDBA and DTMOS based CDBA HPFs are found to be 247.633kHz and 223.190kHz respectively.

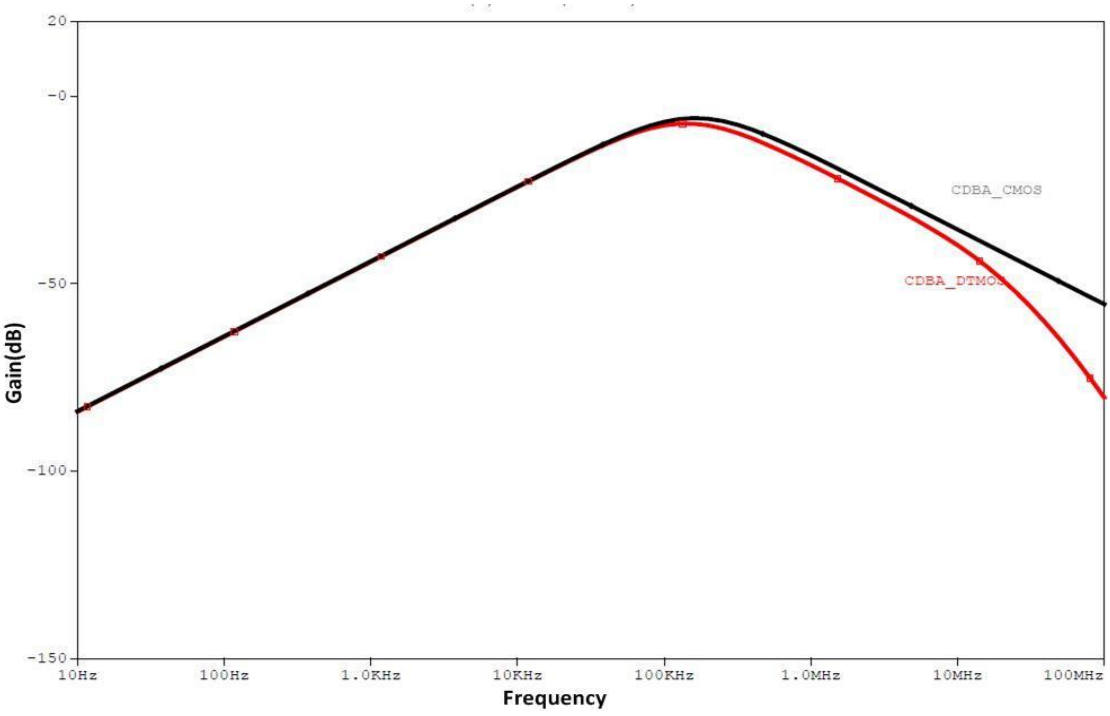

Fig 4.4 Simulated waveform of BPF using DTMOS based CDBA & CMOS based CDBA

From simulated graph the 3dB bandwidth for CMOS based CDBA and DTMOS based CDBA BPFs are found to be 283.738kHz and 224.173kHz respectively.

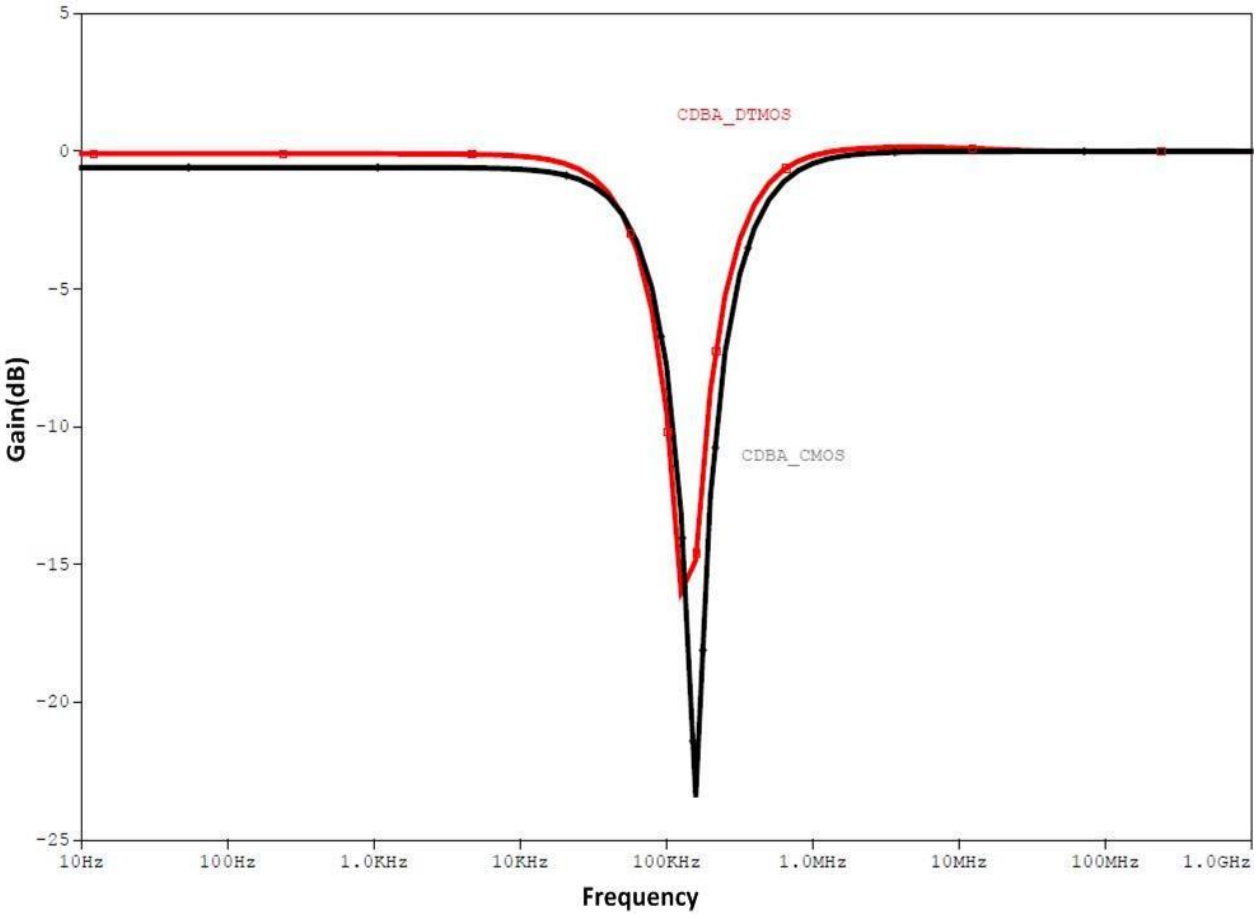

Fig 4.5 Simulated waveform of BRF Filter using DTMOS based CDBA & CMOS based CDBA

From simulated graph the 3dB bandwidth for CMOS based CDBA and DTMOS based CDBA BRFs are found to be 320.774 kHz and 252.176 kHz respectively.

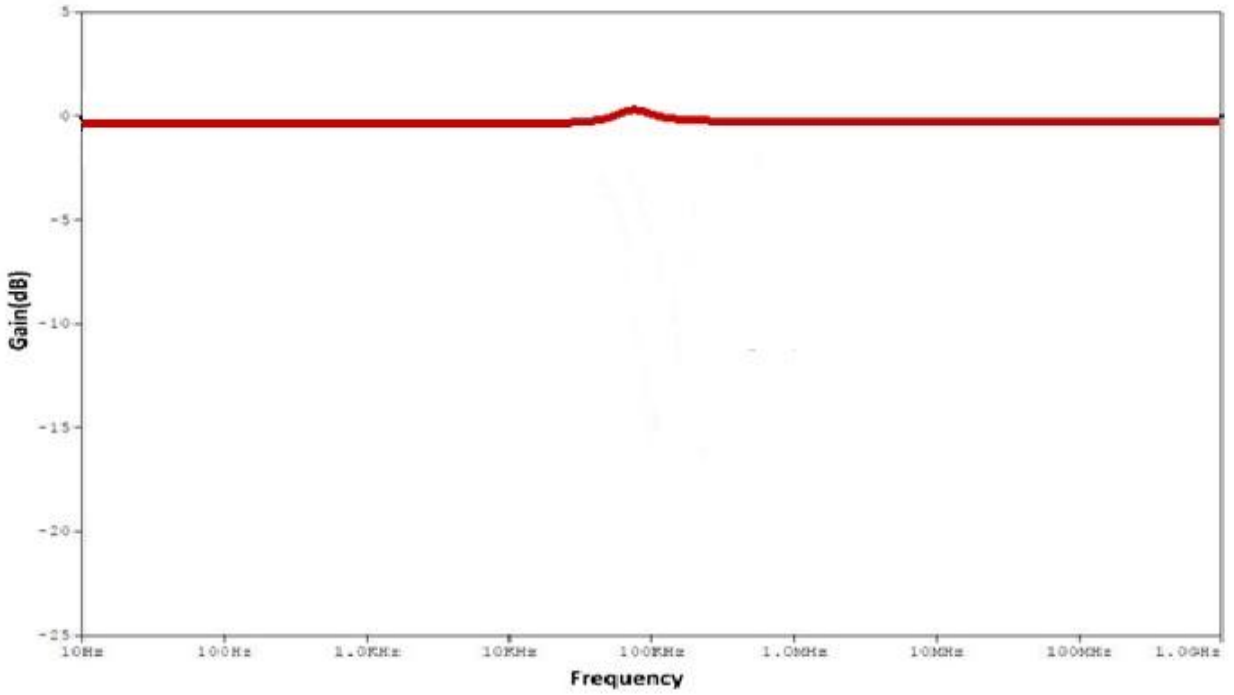

Fig 4.6 Simulated waveform of APF using DTMOS based CDBA

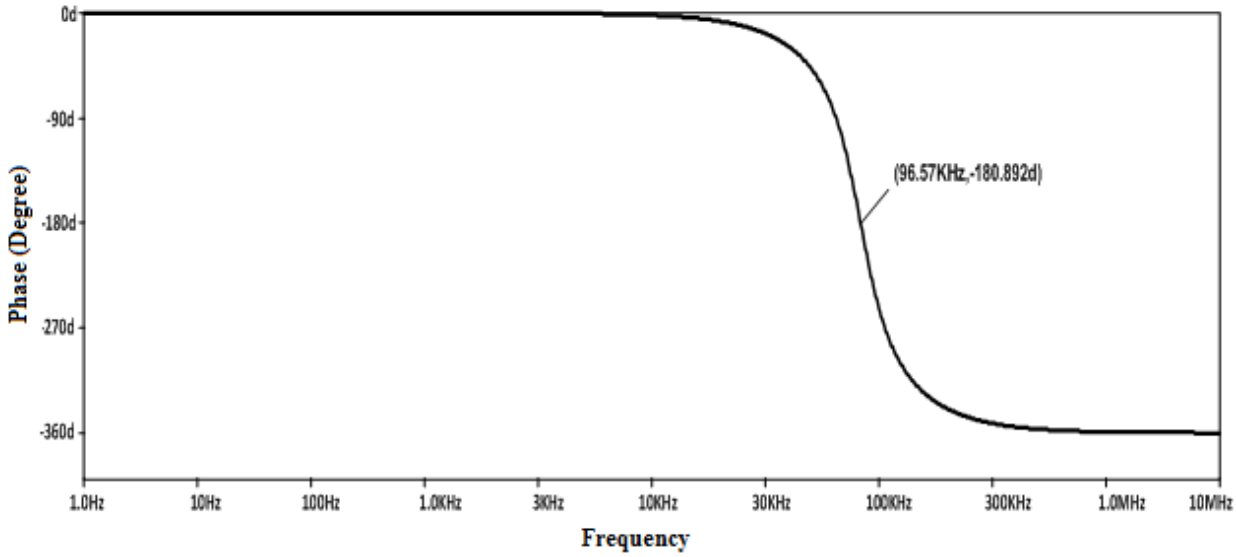

Fig 4.7 Phase response of APF using DTMOS based CDBA

4.4 Bandwidth Comparison Of CMOS CDBA & DTMOS CDBA Filters :

The 3dB cut off frequency and bandwidth for DTMOS based CDBA and CMOS based CDBA filters which are observed from simulated graphs are summarized in table 4.1 as shown below:

Table 4.1 : Bandwidth Comparison Of CMOS CDBA & DTMOS CDBA filters

Filter	CMOS based CDBA Filter	DTMOS based CDBA Filter
LPF	104.440 kHz	90.803 kHz
HPF	247.633 kHz	223.190 kHz
BPF	283.738 kHz	224.173 kHz
BRF	320.774 kHz	252.176 kHz

4.5 Summary :

In the last, it can be summarized that this chapter presents the CDBA based voltage mode universal filter which is modified by replacing the CMOS based CDBA with DTMOS based CDBA . Lastly, the working of DTMOS based CDBA is verified by the simulated output of the filter.

CHAPTER-5

Conclusion & Future Scope

As most of the electronic devices we encounter in our daily life are battery operated, there is huge demand of low power IC's. There are various methods available in literature to reduce the power consumption of integrated circuits. As power consumption is directly proportional to the square of power supply voltage, reduction in power supply voltage is mandatory in order to reduce the power consumption. DTMOS transistor offers the advantage of implementing low power analog circuits by dynamically varying the threshold voltage. In this work we have modified the best available structure of CDBA to obtain low power CDBA by replacing existing PMOS transistors with DTMOS based PMOS transistors.

In this thesis, modified version of CDBA is implemented which has the importance of having only $\pm$ 0.4V supply voltage, thanks to the usage of DTMOS transistors and current mode approach. Since, supply voltage is reduced to great extent therefore power consumption of circuit is also reduced to considerably and hence we are able to increase the battery life. Another advantage of DTMOS is higher trans-conductance and transition frequency.

One of the drawbacks associated with DTMOS based CDBA is that its linear range of operation decreases. The linear range of buffer stage is from -0.091 to 0.3V, also the linear range of CDU units is from -10.579u μA to 52.231μA. Therefore, the further work in low power CDBA deals with increasing linear range of circuit.

REFERENCES

[1] J. E. Chung, M. C. Jeng, J. E. Moon, P. K. Ko, and C. Hu, "Performance and reliability design issue for deep–submicrometer MOSFET's," *IEEE Transactions on Electron Devices*, vol. 38, no. 3, pp. 545–554, Mar. 1991.

[2] T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schuster, and H. N. Yu, "1 um MOSFET VLSI technology: Part IV – hot–electron design constraints," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 2, pp. 268– 275, Apr. 1979.

[3] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, and K. W. Terrill, "Hot–electron–induced MOSFET degradation–model, monitor, and improvement," *IEEE Transactions on Electron Devices*, vol. 35, no. 7, pp. 375–385, Feb. 1985

[4] R. Brodersen, "The network computer and its future," *IEEE International Solids-State Circuits Conference. Digest of Technical Papers*, pp. 32–36, Feb. 1997.

[5] H. Yasuda, "Multimedia impact on devices in the 21st century," *IEEE International Solid–State Circuits Conference Digest of Technical Papers*, pp. 28–31, Feb. 1997.

[6] E. Rodriguez-Villegas, P. Corbishley, C. Lujan-Martinez, and T. Sanchez-Rodriguez, "An ultra-low-power precision rectifier for biomedical sensors interfacing," *Sensors and Actuators A: Physical*, vol. 153, no. 2, pp. 222–229, 2009.

[7] T.-Y. Lo and C.-C. Hung, *1V CMOS Gm-C filters: design and applications*. Dordrecht: Springer, 2009.

[8] "IBM CMOS6SF Model Reference Guide," Nov. 2006

[9] "IBM CMOS7SF Model Reference Guide," Oct. 2008.

[10] TSMC Technology Overview (MPW). Available Online: http://www.europractice–ic.com/technologies_TSMC.php?tech_id=025um.

[11] F. Khateb, S.B. A. Dabbouss, and S. Vlassis, "A Survey of Non–conventional Techniques for Low–voltage Low– power Analog Circuit Design".*Radioengineering*, 2013, vol. 2013 (22), no. 2, IF: 0. 687, pp. 415–427.

[12] F. Maloberti, *Analog design for CMOS VLSI systems*. Dordrecht: Kluwer, 2001.

[13] F. Khateb, "Bulk–driven floating–gate and bulk–driven quasi–floating–gate techniques for low–voltage low–power analog circuits design", *AEU–International Journal of Electronics Communications*, 2013, vol. 68 (1), pp. 64–72.

[14] J. C. Daly and D. P. Galipeau, *Analog BiCMOS design: practices and pitfalls*. Boca Raton, FL: CRC Press, 2000.

[15] BiCMOS Technology Available Online: http://www.scribd.com/doc/184508817/bicmos–technology

[16] T. Sakurai, A. Matsuzawa, and T. Douseki, *Fully-depleted SOI CMOS Circuits and technology for ultralow-power applications*. Dordrecht: Springer, 2006.

[17] A. Marshall and S. Natarajan, *SOI Design: Analog, Memory and Digital Techniques*. Boston: Springer US, 2007.

[18] FULLY DEPLETED (FD) VS. PARTIALLY DEPLETED (PD) SOI. Available online: http://www.advancedsubstratenews.com/2008/05/fully–depleted–fd–vs–partially–depleted–pd–soi.

[19] D. Liu and C. Svensson, "Trading speed for low-power by choice of supply and threshold voltages," *IEEE Journal of Solid-State Circuits*, vol. 28,pp. 10–17, Jan. 1993.

[20] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. Ko, and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for ultra-low voltage vlsi, " *IEEE Transaction on Electron Devices*., vol. 44, no. 3, pp. 414-422, Mar 1997.

[21] S. Özoğuz, A. Toker, C. Acar, "A new current-mode continuous time fully integrated universal filters", *Electronic Letters*, vol. 35, pp. 97-98, 1999.

[22] C. Acar and S. Ozoguz, "A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters," *Microelectronics Journal*, vol. 30, no. 2, pp. 157–160, 1999.

[23] M. Sagbas and M. Koksal, "A new multi-mode multifunction filter using CDBA," *Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005.*

[24] A. Ü. Keskin and E. Hancioglu, "Current mode multifunction filter using two CDBAs," *AEU - International Journal of Electronics and Communications*, vol. 59, no. 8, pp. 495–498, 2005.

[25] A. Ü. Keskin, "Multi-function biquad using single CDBA," *Electrical Engineering*, vol. 88, no. 5, pp. 353–356, Dec. 2005.

[26] A. Ü. Keskin, "Voltage-Mode Notch Filters Using Single CDBA," *Frequenz*, vol. 59, no. 9-10, Jan. 2005.

[27] M. Cheng and C. Toumazou, “3 V MOS current conveyor cell for VLSI technology,” *Electronics Letters*, vol. 29, no. 3, p. 317, 1993.

[28] A. D. Inc., "AD844 current feedback op-amp", Data Sheet.

[29] W. Surakampontorn and P. Thitimajshima, “Integrable electronically tunable current conveyors,” *IEE Proceedings G (Electronic Circuits and Systems)*, vol. 135, no. 2, p. 71, 1988.

[30] H. Elwan and A. Soliman, “Novel CMOS differential voltage current conveyor and its applications,” *IEE Proceedings - Circuits, Devices and Systems*, vol. 144, no. 3, p. 195, 1997.

[31] W. Chiu, S.-I. Liu, H.-W. Tsao, and J.-J. Chen, “CMOS differential difference current conveyors and their applications,” *IEE Proceedings - Circuits, Devices and Systems*, vol. 143, no. 2, p. 91, 1996.

[32] A. Fabre, “Third-generation current conveyor: a new helpful active element,” *Electronics Letters*, vol. 31, no. 5, pp. 338–339, Feb. 1995.

[33] J. Huijsing and J. Korte, “Monolithic nullor-a universal active network element,” *IEEE Journal of Solid-State Circuits*, vol. 12, no. 1, pp. 59–64, 1977.

[34] H. Kuntman and A. Özpinar, “On the realization of DO-OTA-C oscillators,” *Microelectronics Journal*, vol. 29, no. 12, pp. 991–997, 1998.

[35] C. Acar and S. Ozoguz, “A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters,” *Microelectronics Journal*, vol. 30, no. 2, pp. 157–160, 1999.

[36] *Linear products databook 1988*. Norwood, MA: Analog Devices, 1988.

[37] N. Tarim and H. Kuntman, “A high performance current differencing buffered amplifier,” *ICM 2001 Proceedings. The 13th International Conference on Microelectronics.*, 2001.

[38] S. Maheshwari and I. A. Khan, “Current Controlled Current Differencing Buffered Amplifier: Implementation and Applications,” *Active and Passive Electronic Components*, vol. 27, no. 4, pp. 219–227, 2004.

[39] V. Sawangarom, W. Tangsrirat, and W. Surakampontorn, “NPN-based Current Differencing Buffered Amplifier and Its Application,” *2006 SICE-ICASE International Joint Conference*, 2006.

[40] D. Prasad, Mainuddin, Laxya, and S. S. Islam, “Low power low voltage CNTFET-based current differencing buffered amplifier,” *2017 4th International Conference on Signal Processing and Integrated Networks (SPIN)*, 2017.

[41] J.-J. Chen, H.-W. Tsao, and C.-C. Chen, "Operational transresistance amplifier using CMOS technology," *Electronics Letters*, vol. 28, no. 22, p. 2087, 1992.

[42] K. N. Salama, H. O. Elwan, and A. M. Soliman, "Parasitic-capacitance-insensitive voltage-mode mosfet-C filters using differential current voltage conveyor," *Circuits Systems and Signal Processing*, vol. 20, no. 1, pp. 11–26, 2001.

[43] D. Biolek, "CDTA-building block for current-mode analog signal processing," *Proceedings of the ECCTD'03*, vol. 3, pp. 397–400, Krakow, Poland, 2003.

[44] W. Tangsrirat, T. Pukkalanun, and W. Surakampontorn, "CDBA-Based Universal Biquad Filter and Quadrature Oscillator," *Active and Passive Electronic Components*, vol. 2008, pp. 1–6, 2008.