REALIZATION OF CDTA BASED INCREMNETAL/DECREMENTAL TYPE MEMRISTOR EMULATOR CIRCUIT

A PROJECT REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEM

Submitted by:

DAMYANTI SINGH
2K16/VLS/08

Under the supervision of

PROF. NEETA PANDEY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

JUNE, 2018

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Damyanti Singh, Roll No. 2K16/VLS/08 student of M.Tech. (VLSI DESIGN AND EMBEDDED SYSTEM), hereby declare that the project Dissertation titled **"REALIZATION OF CDTA BASED INCREMNETAL / DECREMENTAL TYPE MEMRISTOR EMULATOR CIRCUIT"** which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

Place: Delhi **DAMYANTI SINGH**

Date:

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled **"REALIZATION OF CDTA BASED INCREMNETAL/DECREMENTAL TYPE MEMRISTOR EMULATOR CIRCUIT"** which is submitted by DAMYANTI SINGH, Roll No 2K16/VLS/08 Department of Electronics And Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date:

PROF. NEETA PANDEY

SUPERVISOR

ACKNOWLEDGEMENT

I would like to thank my supervisor, Prof. Neeta Pandey, Department of Electronics and Communication Engineering, DTU for the guidance, encouragement and advice she has provided throughout my time as her student. I have been extremely lucky to have a supervisor who cared so much about my work and who responded to my questions and queries so promptly. I attribute the level of my Masters degree to her encouragement and effort and without her this thesis, too, would not have been completed or written. One simply could not wish for a better or friendlier supervisor.

I am also grateful to Prof. S. Indu, HOD, Department of Electronics and Communication Engineering, DTU for her immense support. I would also acknowledge DTU for providing the right academic resources and environment for this work to be carried out.

Finally, I take this opportunity to extend my deep appreciation to my family and friends, for all that they meant to me during the crucial times of the completion of my project.

Date

Damyanti Singh

2K16/VLS/08

M.Tech (VLSI Design and Embedded System)

ABSTRACT

Memristor is a fourth basic circuit element. It shows the relationship between charge (q) and flux (ϕ). Although memristor is a hypothetical concept, its realization is important for interaction with other circuit element for designers. In this project, a new memristor emulator circuit has been designed using Current Differencing Transconductance Amplifier (CDTA) block. The CDTA block consists of two units: (1) Current Differencing Unit (CDU) and (2) Transconductance Amplifier (TA) unit. The TA unit of CDTA block offers an extra control parameter, transconductance parameter (g_m) in addition to frequency (f) and amplitude value of voltage across emulator (V_m). Since, g_m can be controlled using external voltage/current, the memductance of proposed emulator circuit can be tuned electronically. The proposed emulator circuit provides both type of memductance, incremental and decremental, solely by interchanging the CDTA output terminals controlled by simple switch. The realization of proposed emulator circuit is simple in comparison to the existing emulator circuits and avoids the use of extra circuitry like ADC, DAC, analog multiplier and multiple sub-circuits. The proposed emulator circuit consists of one CDTA block, two resistors and one capacitor. In order to test the functionality of the proposed emulator circuit, a passive component has connected both ways, serial and parallel, than MC circuit is analyzed and results have been included in the end of the report. The simulations have done using SYMICA DE software and technology used is TSMC 250nm.

TABLE OF CONTENTS

List of Figures

List of Tables

LIST OF ABBREVIATIONS

Abbreviation	Full Form
CMOS	Complementary Metal Oxide Semiconductor
ABB	Active Building Block
BJT	Bipolar Junction Transistor
Op-Amp	Operational Amplifier
IC	Integrated Circuit
AC	Alternating Current
DC	Direct Current
VLSI	Very Large Scale Integration
ADC	Analog to Digital Convertor
DAC	Digital to Analog Convertor
ASP	Analog Signal Processing
CM	Current Mode
VM	Voltage Mode
CFOA	Current Feedback Operational Amplifier
CDU	Current Differencing Unit
OTA	Operational Transconductance Amplifier

DO-OTA	Dual Output OTA
TA	Transconductance Amplifier
CDTA	Current Differencing Transconductance Amplifier
CC	Current Conveyor
CCII	2nd generation Current Conveyor
CCTA	Current Conveyor Transconductance Amplifier
DDCC	Differential Difference Current Conveyor
CDBA	Current Differencing Buffered Amplifier
VDTA	Voltage Differencing Transconductance Amplifier
KHN	Kerwin-Huelsman-Newcomb
B.W.	Bandwidth
RC	Resistor Capacitor
MC	Memristor Capacitor
MR	Memristor Resistor
ML	Memristor Inductor
HP	Hewlett Packard

CHAPTER 1

Introduction

Memristor is a basic circuit element postulated by Leon O. Chua in 1971[1]. It presents the relationship between charge (q) and flux (Φ). The article entitled "Memristive Device and Systems" describes about the theory of memristors and memristive systems[2]. This element shows the property of linear and non linear resistance with memory. Memristive devices also plays an important role in the field of both memory and neuromorphic application. For the purpose of memory application, it is non-volatile and has small size of few nanometers. For the neuromorphic application, it contains feature of pulse based operation and adjustable resistance. These features of memristive devices are ideal for tuning the synaptic weights of neuromorphic cells.

Initially, memristor was a theoretical concept. The research was started in 2002 by Williams and his coworkers for the fabrication of memristor and they finally fabricated the memristor structure in HP labs[3] in 2008. They fabricated the first solid state memristor using platinum (Pt) and titanium dioxide (TiO_2). This fabricated memristor exhibit the same mathematical definition and formula as described by Leon O. Chua in [2]. It shows the important electrical and dynamic properties as described in [4]. This property states that the switching time and energy decrease exponentially with increasing applied current. However, the fabrication of such device is difficult for its inventors also and hence the invention of such device took six years i.e from 2002 to 2008 to invent this device.

However, commercial realization of this type of memristor was not possible due to its prohibitively high cost and the fabrication complexities at nano scale level. Therefore,

researchers started working on memristor emulator circuits were introduced which inherit the properties of TiO_2 based memristor circuit.

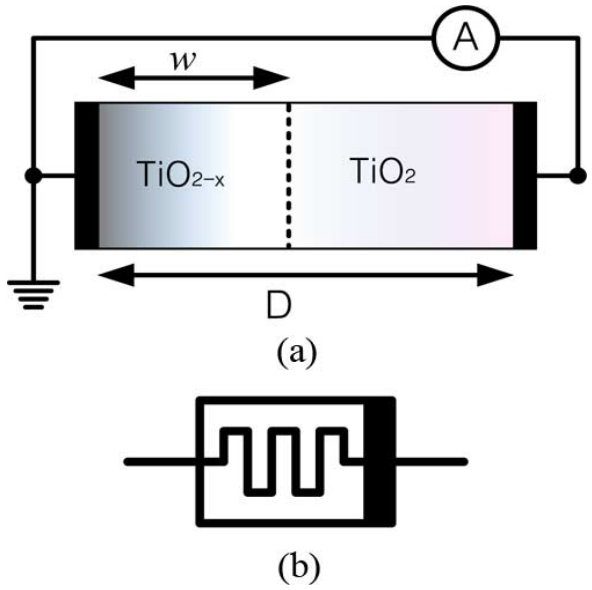


Fig 1.1 (a) Memristor structure (b) Memristor symbol fabricated in HP lab[3]

1.1 Motivation

Memristor is a passive circuit element which shows the relationship between charge (q) and flux (Φ). It shows the property of non linear resistor with memory. Hence, it can store its previous data. Before 2008, memristor was a hypothetical concept. William and his coworker invented the first solid state memristor. But due to the cost problem, its physical realization is not possible. Hence, memristor emulator circuits were introduced. These emulator circuits are available using many active blocks. These blocks have their own advantages and disadvantages.

CDTA is a current mode active block. Current mode (CM) active devices have their own advantages in comparison to their counterpart voltage mode (VM) devices. CM devices

require less external components for realization of circuits and circuits become less complex. They also provide better linearity and higher dynamic range in comparison to VM devices. They also have accuracy in its input output characteristics and higher operating frequency range. Hence, designers have shifted their attention toward current mode devices. The CDTA block has all these properties and its gain is also controllable.

The emulator circuit using CDTA block shows all the advantages of current mode devices as well as its gain can be controlled easily using transconductance (TA) block. By controlling transconductance gain (g_m), the width of hysteresis loop can be controlled. This hysteresis loop shows the memristance value during the frequency response analysis. This hysteresis loop is also known as double valued Lissajous figure. Under the application of periodic input function, memristors give double valued Lissajous function as output because of the values stored in the memristors in its previous state.

1.2 Research Objective

At nanoscale level, memristive devices shows promising attributes. Their small size, low power and simple structure at nano scale level attracts the attention of designers. These memristive devices has been considered as the potential candidate to replace the CMOS technology. However, the physical realization of memristor is not possible, hence their emulators are being designed. In literature, various emulator circuits have been introduced.

The main objective of this thesis is the introduction of emulator circuit using CDTA. This emulator circuit uses single CDTA block, two resistors and one capacitor. The CDTA is an active element consisting of two blocks namely: current differencing unit (CDU) and transconductance amplifier (TA) block. Due to the TA block, transconductance gain (g_m) is

controllable. With the controlling g_m, shape and size of hysteresis loop can be controlled. While plotting the relationship between voltage and current, the hysteresis loop shows the behavior of non linear resistor with memory. By controlling $g_{m,}$ this non linear resistance behavior can be converted into linear resistance behavior.

In this work, a new CMOS structure of CDTA block is also introduced. This CDTA block can be used in different complex circuits. The characteristics of this CDTA block have been described and results of the simulation have been included in this thesis.

1.3 Organization of Thesis

This thesis has been organized in seven chapters. Chapter 1 describes the brief introduction of memristor and memristor emulator circuits. It also includes the motivation and objective of thesis.

In chapter 2, a literature survey on the memristor emulator circuit has been presented. It depicts about the researches done for the memristor emulator circuits.

In chapter 3, a brief introduction about memristor has been given. It also describes about the properties and application of memristor.

In chapter 4, CDTA block has been described. It gives the brief introduction about CDTA block. It also includes the DC and AC analysis of the CDTA block. The simulation results have also been included which verifies the performance of the CDTA. It also provides the introduction about the non ideal behavior of CDTA.

In chapter 5, proposed emulator circuit based on CDTA has been described. All the results of simulation to verify the properties of memristor emulator circuit have been included. It

also describes about the non ideal beahavior of the proposed circuit. It also includes the frequency analysis of the proposed circuit.

In chapter 6, the application of proposed emulator circuit has been described. It describes about the behavior of RC and MC circuits.

In chapter 7, the conclusion and future scope of the proposed emulator circuit has been described.

CHAPTER 2

MEMRISTOR: The Fourth Basic Circuit Element

The history of the circuit theory introduces four fundamental circuit elements. These circuit elements are voltage (v), current (i), charge (q) and flux (Φ). With the help of these four circuit elements, six relationships can be defined. Among these six relationships, five relationships were known until 1971. Out of these five relationships, three of them define the relationship of two port circuit components. These two port circuit components are resistor (R), inductor (L) and capacitor (C) and the relations are as follows:

$$R = \frac{dV}{di}, \qquad C = \frac{dq}{dV} \quad \text{and} \quad L = \frac{d\Phi}{di} \tag{2.1}$$

The other two relations are defined as follows:

$$q = \int_{-\infty}^{t} i(t)dt \quad \text{and} \quad \Phi = \int_{-\infty}^{t} v(\tau)d\tau \tag{2.2}$$

The unknown relationship was between the charge (q) and the flux (Φ). But in 1971, a new passive element was introduced by Leon O. Chua [1] which relates the charge (q) and the flux (Φ) with each other. This new passive element was termed as memristor. This element shows the property of non linear resistor with memory. Fig. 2.1 shows the relationship among all four basic circuit elements which is given on the next page.

2.1 Symbol of memristor and its basic realization

Initially, memristor was a hypothetical concept. It was realizable using mutator[5] only. Fig 2.2 shows the proposed symbol and a hypothetical Φ-q curve of memristor. To realize the memristor with prescribed Φ-q curve, it is connected with an appropriate non linear resistor

or inductor or capacitor across port 2 of an M-R mutator, an M-L mutator and an M-C mutator as shown in fig. 2.3.(a), (b), (c) respectively.

The MR mutator would transform the v_R - i_R curve or i_R - v_R curve of the non linear resistor $f(v_R, i_R) = 0$ or $f(i_R, v_R) = 0$ into the corresponding $\Phi - q$ curve $f(\Phi, q) = 0$ of a memristor. A similar transformation would be observed with ML and MC mutator with respect to the Φ_L-i_L curve or i_L-Φ_L curve of the non linear inductor and v_C – q_C curve or q_C - v_C curve of the non linear capacitor.

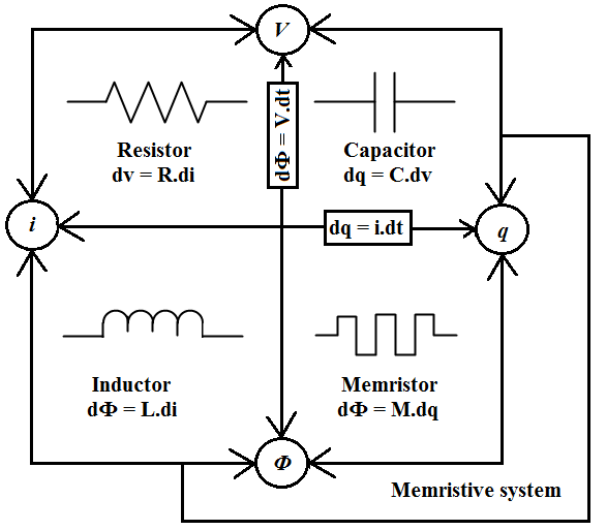


Fig 2.1 Relationship among all four circuit component[3]

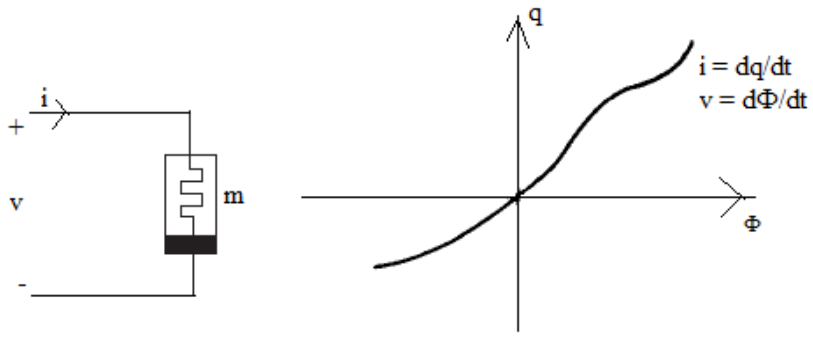


Fig 2.2 Memristor and its Φ-q curve[1]

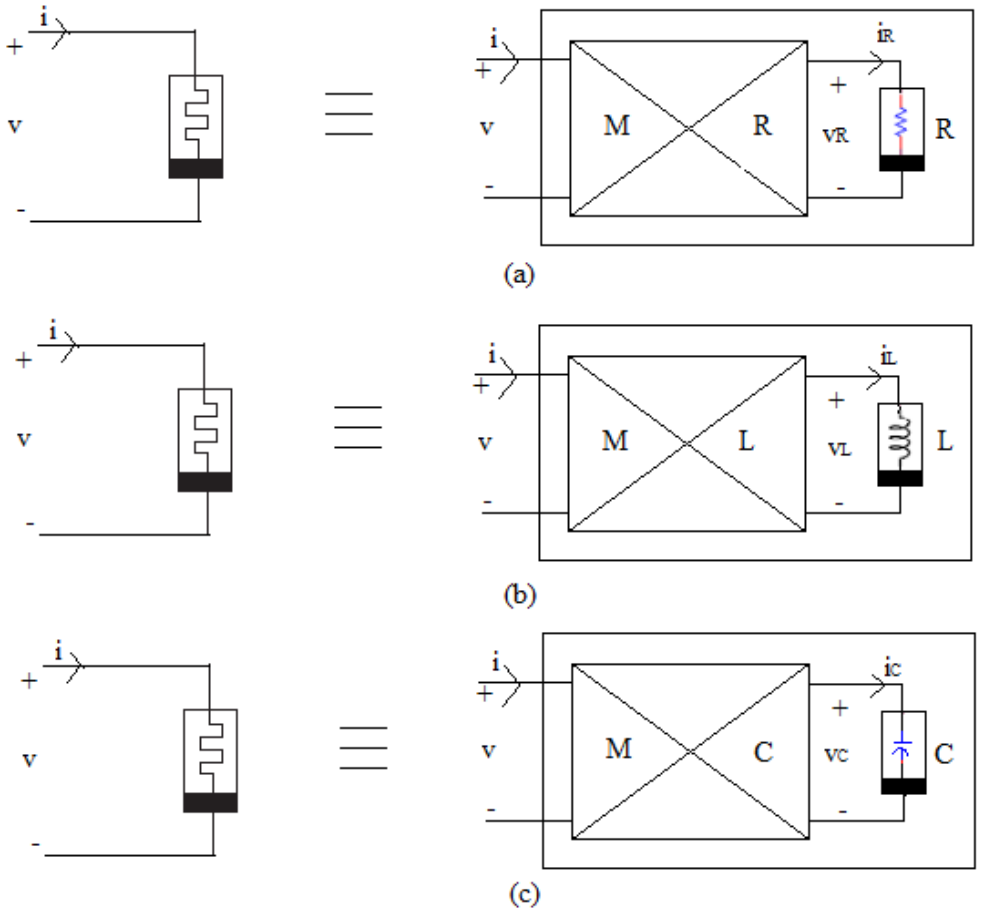


Fig 2.3 Memristor basic realization using mutator[1]

From the Φ – q curve of memristor, it is observed that memristor contain some unique properties, which are not possessed by any of the three existing circuit element. Due to these properties, memristor plays an important role in the area of device modeling and unconventional signal processing applications. Some of these applications have been described in the upcoming chapters.

2.2 Generic Properties of Memristor

According to the definition, memristor is characterized as f(Φ,q) = 0. If this relationship gives a single value of the function in terms of the charge (q) or the flux linkage (Φ), it can

be treated as charge controlled or flux controlled element. The relation between voltage (v) and current (i) across a charge controlled memristor is given as

$$v(t) = M(q(t))\, i(t) \tag{2.3}$$

where,

$$M(q) \equiv d\Phi(q) / dq \tag{2.4}$$

Similarly, the relationship between current and voltage of a flux-controlled memristor is defined as

$$i(t) = W(\Phi(t))\, v(t) \tag{2.5}$$

where

$$W(\Phi) \equiv dq(\Phi) / d\Phi \tag{2.6}$$

Here, M(q) has unit of resistance, hence termed as incremental memristance and W(Φ) has unit of conductance, hence termed as incremental memconductance. To get the value of memristance or memconductance at a particular time t_0, memristor current or voltage is integrated from - ∞ to $t = t_0$. Hence, it can be concluded that at any particular time t_0, memristor behave like an ordinary linear resistor and its resistance or conductance value depends on the previous values of voltage or current. Hence, it justifies its name memory resistor or memristor.

There are many memristives devices which have been classified incorrectly. These generic properties will help in identifying memristive devices and distinguish them from ordinary devices. These properties are as follows:

2.2.1 Passivity Criterion

If an incremental memristance M(q) is non negative, a charge controlled memristor will be treated as a passive element i.e. $M(q) \geq 0$.

Proof: The instantaneous power dissipated by a memristor is given as

$$P(t) = v(t)\, i(t) = M(q(t))\, [i(t)]^2 \qquad (2.7)$$

Hence, if the value of an incremental memristance is non negative i.e. $M(q) \geq 0$, then $P(t) \geq 0$ i.e. power will be dissipated by the memristor and it will act as a passive element. To prove the converse of the above statement, let us consider a point q_0 such that $M(q_0) < 0$. Then on differentiating the $\Phi - q$ curve, it can be implied that there exist an $\epsilon > 0$ such that $M(q_0 + \Delta q) < 0$, $|\Delta q| < \epsilon$.

One should remark that if the differentiability condition is replaced by a continuity condition, provided that the left hand derivative and the right hand derivative at each point on the $\Phi - q$ curve exists then the above criterion remains valid. This criteria shows that monotonically increasing memristor, characterizing the $\Phi - q$ curve, can exist in the device form without internal power supplies and any known physical law does not seem to be violated.

2.2.2 No Energy Discharge Property

If the hypothesis of property 2.2.1 is satisfied by one port current controlled memristive device then it can be stated that the instantaneous power entering into the one port memristive device is always non-negative.

Proof: According to property 2.2.1, $M(q) \geq 0$ for any admissible input signal pair (v,i) and hence the power entering into the one port device i.e $P(t) = v(t).i(t)$ is always non-negative.

Except for the pathological case, stored energy can be discharged from the passive RLC network easily. To extract this stored energy, one has to connect a load across this passive RLC network. However, it is not possible to extract energy from memristive device if it is

satisfying property 2.2.1. To highlight this unique property, it is labeled as “no energy discharge property”.

2.2.3 DC Characteristics

A time invariant current controlled memristive device under dc operation is equivalent to a time invariant current controlled nonlinear resistor if f(x,I) = 0 has a unique solution x = X(I) such that for each value of I $\in \mathcal{R}$, the equilibrium point x = X(I) is globally asymptotically stable.

Proof: An n^{th} order current controlled memristive one port device is represented as

$$\dot{x} = f(x, i, t)$$

$$v = R(x, i, t)\, i \tag{2.8}$$

Similarly, an n^{th} order voltage controlled memristive one port device is represented as

$$\dot{x} = f(x, v, t)$$

$$i = G(x, v, t)\, v \tag{2.9}$$

where v and i are the port voltage and current respectively. Now, on substituting x = X(I) into the output equation in (2.8), we obtain v = R(X(I), I) I $\triangleq \hat{V}(I)$. Since, X(I) is globally asymptotically stable, each value of dc input current (I) gives a stable and hence measurable dc output voltage (V). Hence, the function $\hat{V}(I)$ can be interpreted as the V- I curve of a time invariant nonlinear resistor.

2.2.4 Double Valued Lissajous Figure Property

When periodic input i(t) = I cos ωt is given to memristive one port device, it always give rise to a v-i Lissajous figure whose output voltage v is at most a double valued function of input current i.

Proof: From equation (2.8) and (2.9), the state equation seems to have a unique periodic solution x(t) for all $t \geq t_0$ for some initial state x_0, by assumption. Hence, for any value of current $i \in [-I, I]$, there exist at most two different values of voltage v.

Double valued Lissajous figure property has been illustrated in fig. 2.4. From fig 2.4, it can be observed that 2.4(b) cannot be treated as current controlled memristive one port device because at $i = i_p$, there exist more than two different values of voltage v.

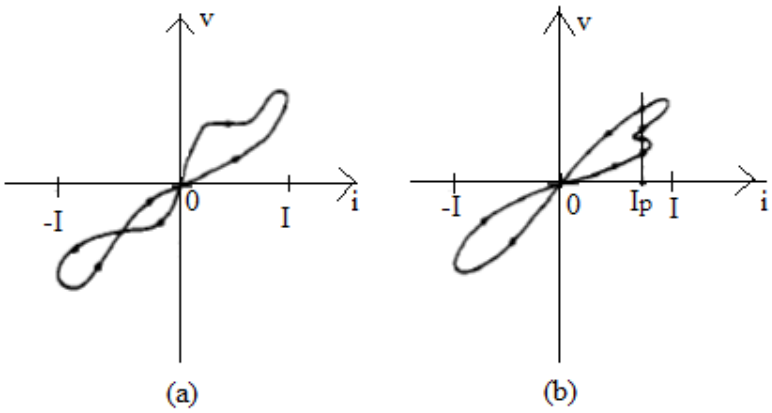


Fig 2.4 Illustration of property 2.2.4 (a) Possible Lissajous pattern (b) Impossible Lissajous pattern[2]

2.2.5 Symmetric Lissajous Figure Property

If a time invariant current controlled memristive one port device is defined as R(x, i) = R(x, -i) then the v-i Lissajous pattern corresponding to the input current i(t) = Icos(ωt) is open i.e. not a closed loop whenever the state x(t) is periodic of the same period as that of the input i(t) and is half wave symmetric. Moreover, Lissajous figure is odd and quarter wave symmetric with respect to the origin whenever the state x(t) is periodic of the same period as that of i(t).

Proof: If both x(t) and i(t) are half wave symmetric then it follows from the output equation v = R(x, i) i that

$$v\left(t + \frac{T}{2}\right) = R\left(x\left(t + \frac{T}{2}\right), i\left(t + \frac{T}{2}\right)\right)\ i\left(t + \frac{T}{2}\right)$$

$$v\left(t + \frac{T}{2}\right) = R\left(x\left(- t + \frac{T}{2}\right), i\left(- t + \frac{T}{2}\right)\right)\ i\left(- t + \frac{T}{2}\right)$$

$$= v\left(- t + \frac{T}{2}\right), \text{ for all } t \in \left[0, \frac{T}{2}\right]$$

where T is the period of both x(t) and i(t). Hence, v-i curve does not form close loop and it is open. If x(t) is quarter wave symmetric then $i\left(t + \frac{T}{4}\right) = -i\left(- t + \frac{T}{4}\right)$ for all $t \in \left[0, \frac{T}{4}\right]$

when $i(t) = I \cos \omega t$, we obtain

$$v\left(t + \frac{T}{4}\right) = R\left(x\left(t + \frac{T}{4}\right), i\left(t + \frac{T}{4}\right)\right)\ i\left(t + \frac{T}{4}\right)$$

$$= - R\left(x\left(- t + \frac{T}{4}\right), i\left(- t + \frac{T}{4}\right)\right)\ i\left(- t + \frac{T}{4}\right)$$

$$= - v\left(- t + \frac{T}{4}\right), \text{ for all } t \in \left[0, \frac{T}{4}\right]$$

Hence, the v-i curve is odd and quarter wave symmetric with respect to the origin.

2.2.6 Limiting Linear Characteristics

If the current controlled time invariant memristive one port device is bounded input bounded state (bibs) stable then under periodic operation it degenerates into a linear time invariant resistor as the frequency of excitation increases toward infinity (∞).

Proof: As the excitation frequency $\omega \rightarrow \infty$, the state vector $x(t) \rightarrow x_0$ where x_0 is some constant vector in $\mathcal{R}^n$. It follows from the bibs stability that for any bounded input i(t), the f(x, i) can be written as

$$f(x,i) = \alpha_0 + \sum_{\substack{k=-N \\ K\neq 0}}^{N} \exp(jk\omega t)\alpha_k \qquad (2.10)$$

where N is some integer and the vectors α_0 and α_k belong to the space ϱ^n of n-tuples of complex numbers. Note that the vectors α_0 and α_k are bounded. And

$$\dot{x} = f(x,i)$$

$$v = R(x)\, i \qquad (2.11)$$

Hence, from equations 2.10 and 2.11, we obtain

$$x(t) = x(t_0) + \int_{t_0}^{t} f\big(x(\tau), i(\tau)\big)d\tau$$

$$= x_0 + \int_{t_0}^{t} (\alpha_0 + \sum_{\substack{k=-N \\ K\neq 0}}^{N} \exp(jk\omega\tau)\alpha_k)d\tau$$

$$= x_0 + \alpha_0(t - t_0) + \sum_{\substack{k=-N \\ K\neq 0}}^{N} \frac{\exp(jk\omega t) - \exp(jk\omega t_0)}{jk\omega}\alpha_k \qquad (2.12)$$

Since x(t) is periodic and bounded by assumption, (2.12) implies $\alpha_0 = 0$ and as $\omega \to \infty$, the state $x(t) \to x_0$.

When the memristive one port device is under periodic operation, different initial states x_0 will have to be selected for different excitation frequencies. However, state x(t) will approach to some constant values as the excitation frequency tends toward infinity (∞). Fig.2.5 illustrates this property of memristor. From fig.2.5, it is observed that when $\omega \to \infty$, the family of Lissajous figure starts to shrink to a straight line.

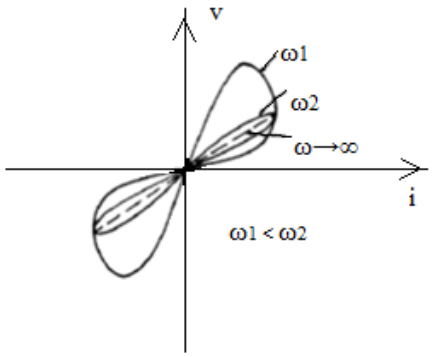


Fig 2.5 Frequency response of a lissajous figures[2]

2.2.7 Small Signal AC Characteristics

If a current controlled time invariant memristive one port device is globally asymptotically stable for all dc input current I then its small signal equivalent circuit about dc operating point will be as shown in fig 2.6.

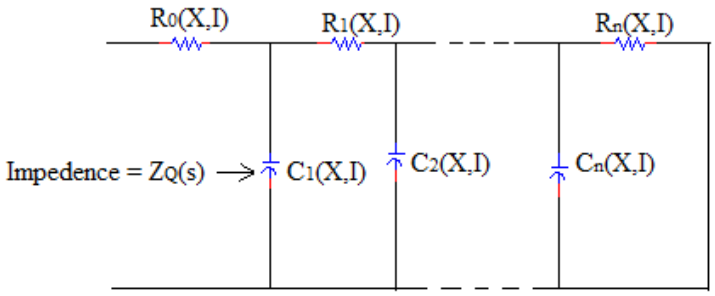


Fig 2.6 Small signal equivalent circuit[2]

The frequency dependence of the small signal Lissajous figure about operating point $I = I_Q$ is depicted in fig 2.7

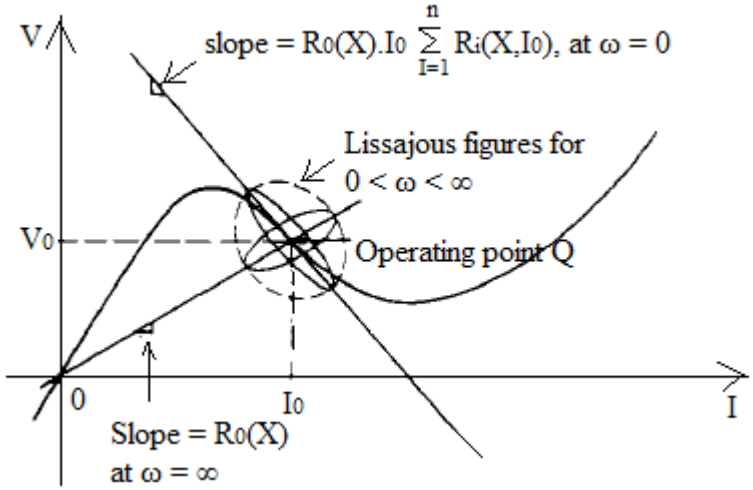


Fig 2.7 The small signal Lissajous figures[2]

This type of behavior has been observed in many physical devices and systems, including thermistors and ionic systems. From fig 2.7, $R_0(x)$ represents the dc resistance at $I = I_Q$ and is equal to the small signal impedance $Z_Q(s)$ as the excitation frequency increases toward infinity (∞).

2.3 Example of memristive devices

As we have discussed previously that there are some physical devices which should be modeled as memristive one port devices, but which have been so far improperly classified. Some of these devices have been described here.

2.3.1 Thermistor

Thermistor is a type of resistor whose resistance varies with ambient temperature[6]. It has a negative temperature coefficient and characterized by

$$v = R_0 (T_0) \exp\left[\beta \left(\frac{1}{T} - \frac{1}{T_0}\right)\right] i \triangleq R(T)\, i \qquad (2.13)$$

where β is called as material constant, T is the thermistor's absolute body temperature and T_0 is the thermistor's ambient temperature in kelvin. The cold temperature resistance is denoted by the constant $R_o(T_o)$ at $T = T_0$. The instantaneous temperature T is known to be a function of the power dissipated in the thermistor and is governed by the heat transfer equation

$$p(t) = v(t)\, i(t) = \delta(T - T_0) + C \frac{dT}{dt} \qquad (2.14)$$

where C is known as heat capacitance and δ is defined as the dissipation constant of the thermistor which is described as the ratio of a change in the body of temperature. Substituting (2.13) into (2.14) and by rearranging terms, we obtain

$$\frac{dT}{dt} = -\frac{\delta}{C}(T - T_0) + \frac{R_0 T_0}{2} \exp\left[\beta \left(\frac{1}{T} - \frac{1}{T_0}\right)\right] i^2 \triangleq f(T, i) \qquad (2.15)$$

We observe from (2.13) and (2.15) that a thermistor is a first-order time invariant current-controlled memristive one-port device which has been treated as memoryless linear resistor whose value varies with temperature.

To describe the property 2.2.3 of memristor, the DC characteristic of thermistor is plotted. Using equation (2.13) and (2.15), values of β, δ, T_0 and $R_0(T_0)$ have been derived and these values are β = 3460 K, δ = 0.1 mW/^{0}C, T_0 = 298 K and $R_0(T_0)$ = 8000Ω. Fig.2.8 represents the DC characteristic of thermistor.

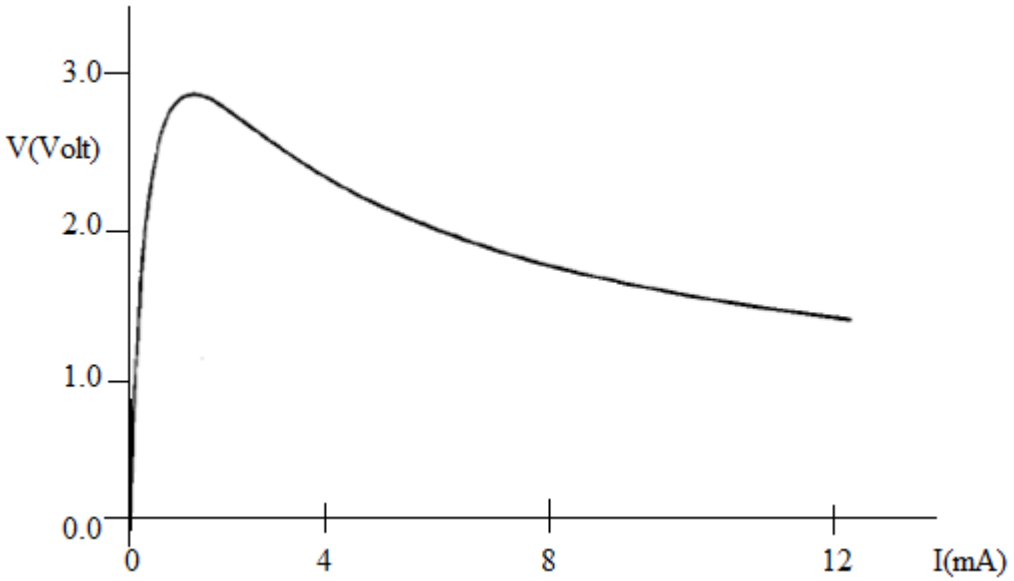


Fig.2.8 The DC V-I characteristic of typical Thermistor[2]

The range of current is $0 \leq I \leq 12.5$ mA. From fig.2.8, it can be noticed that only first quadrant is shown as the DC characteristic is symmetrical with respect to the origin. Hence, from DC curve, it can be observed that under DC operation, time invariant one port memristive device operate as nonlinear resistors.

By using property 2.2.3, one can interpret the use of DC curve of thermistor and its limitations too. The DC V-I curve of thermistor is useful if and only if thermistor is operated under DC supply or slowly varying input signals.

Such V-I characteristics of the thermistors are already specified by the manufacturer with the steady state temperature condition specified along the curve.

2.3.2 Ionic System

Hodgkin – Huxley proposed a circuit model[7] of nerve axon membrane which is shown in fig.2.9.

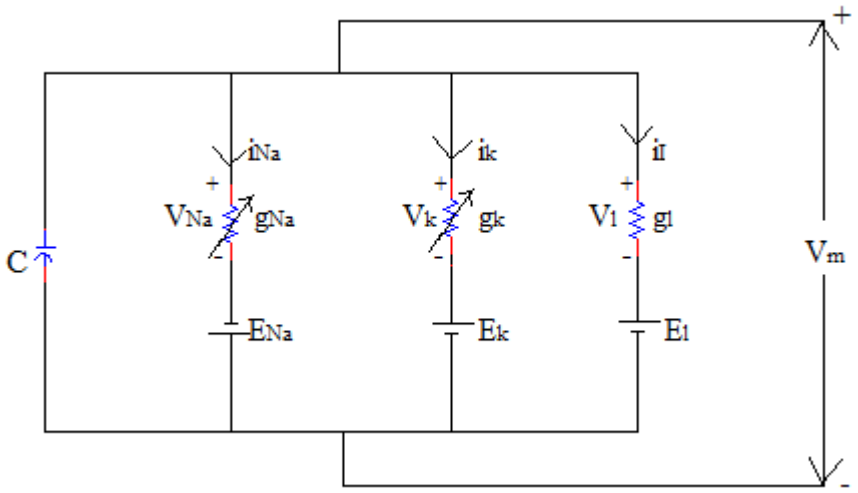


Fig 2.9 The Hodgkin-Huxley Model[7]

This model describes the potassium channel conductance (g_k) and the sodium channel conductance (g_{Na}) as the time varying conductance. The variation of these conductances is a function of solution of first order differential equation. The potassium channel is defined as

$$i_k = \overline{g_k}\, n^4\, v_k \triangleq G_k(n)\, v_k$$

$$\dot{n} = \frac{0.01(v_k+E_k+10)}{\exp\left[\frac{v_k+E_k+10}{10}\right]-1}(1-n) - 0.125\exp\left(\frac{v_k+E_k}{80}\right) n \triangleq f(n,v_k) \qquad (2.16)$$

where $\overline{g_k}$ and v_k are the constant. Similarly, the sodium channel is defined as

$$i_{Na} = \overline{g_{Na}}\, m^3\, h\, v_{Na} \triangleq G_{Na}(m,h)\, v_{Na}$$

$$\dot{m} = \frac{0.1(v_{Na}+E_{Na}+25)}{\exp\left[\frac{v_{Na}-E_{Na}+25}{10}\right]-1}(1-m) - 4\exp\left(\frac{v_{Na}-E_{Na}}{18}\right) m \triangleq f_1(m, v_{Na}) \qquad (2.17)$$

$$\dot{h} = 0.07\exp\left(\frac{v_{Na}-E_{Na}}{20}\right)(1-h) - \frac{1}{\exp\left[\frac{v_{Na}-E_{Na}+30}{10}\right]+1} h \triangleq f_2(h, v_{Na})$$

where, $\overline{g_{Na}}$ and E_{Na} are constants. From equation (2.16) and (2.17), it is observed that the time varying conductance of the system cannot be defined as function of time. They are actually memristive one port devices. Moreover, the potassium channel of the Hodgkin-Huxley system should be treated as first order voltage controlled memristive one port device which is time invariant. Similarly, the sodium channel should be treated as second order voltage controlled memristive one port device which is time invariant.

Fig.2.10 represents the DC characteristic curve of the potassium channel of the Hodgkin-Huxley model. The value of $\overline{g_k}$ = 36 m℧/cm^2 and E_k= 12mV has been derived using equation (2.16).

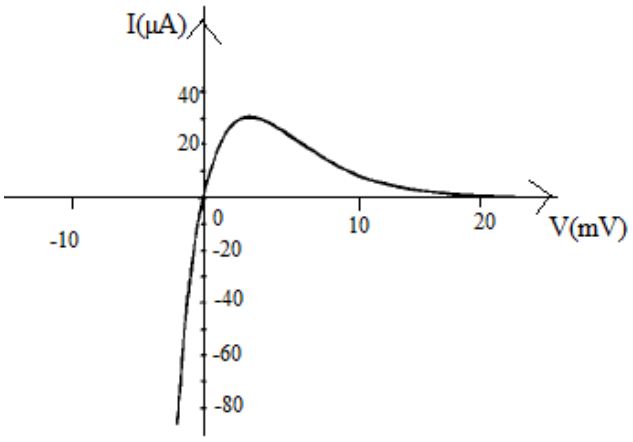


Fig.2.10 The potassium channel DC characteristics[2]

Again, only first quadrant is shown in fig.2.10, as the system is symmetric with respect to the origin.

2.3.3 Discharge Tubes

Francis[8] explained the behavior of the discharge tubes by

$$\dot{n} = \alpha\, i\, v - \beta n \qquad (2.18a)$$

$$v = \frac{F}{n}\, i \triangleq R(n)i \qquad (2.18b)$$

where α, β and F are defined as the constants depending on the dimension size of the tubes and the gas fillings. The variable n represents the electron density of the tubes. Substituting (2.18b) into (2.18a), we get

$$\dot{n} = \frac{\alpha F}{n} i^2 - \beta n \triangleq f(n, i) \qquad (2.18c)$$

From (2.18b) and (2.18c), it is clear that the discharge tubes should be described as the first order time invariant current controlled memristive one port device. But unfortunately, discharge tubes such as neon bulbs and fluorescent lamps has been treated as dynamic devices for a long time. Researchers were failed to identify memristive properties of these devices.

Fig 2.11 shows the DC V-I curve of short neon tube illustrating the generic property 2.2.3 of the memristive one port device.

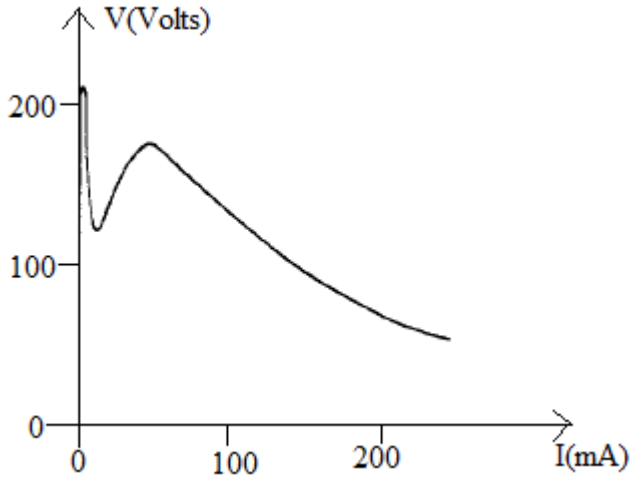


Fig.2.11 The DC characteristic of short neon tube[2]

Again, DC V-I curve in first quadrant only describe the symmetric nature of the device with respect to the origin.

2.4 Applications of Memristors

From previous section, it is clear that the voltage and current waveform of the simple memristor is different from the normal RLC circuit. Due to this reason, it is observed that memristive circuit may give rise to some applications which are not explained by the RLC circuit.

2.4.1 Application of Memristors to device Modeling

There are many unconventional devices that have been invented in the last few tears. However, the principle of operation of these devices have not yet been cleared and fully understood. It will now be shown in this section that using memristors, the properties of these unconventional devices can be understood easily. We will describe two examples of such devices in this section.

2.4.1.1 Modeling an Amorphous "Ovanic" Threshold Switch

An amorphous "Ovanic" threshold switch is a two terminal device. It uses amorphous glass instead of common crystalline semiconductor materials which are used in solid state devices. To show the reasonable model of the amorphous device using memristor, let us consider a memristor circuit shown in fig.2.12 (a) and it Φ-q curve is shown in fig.2.12 (b).

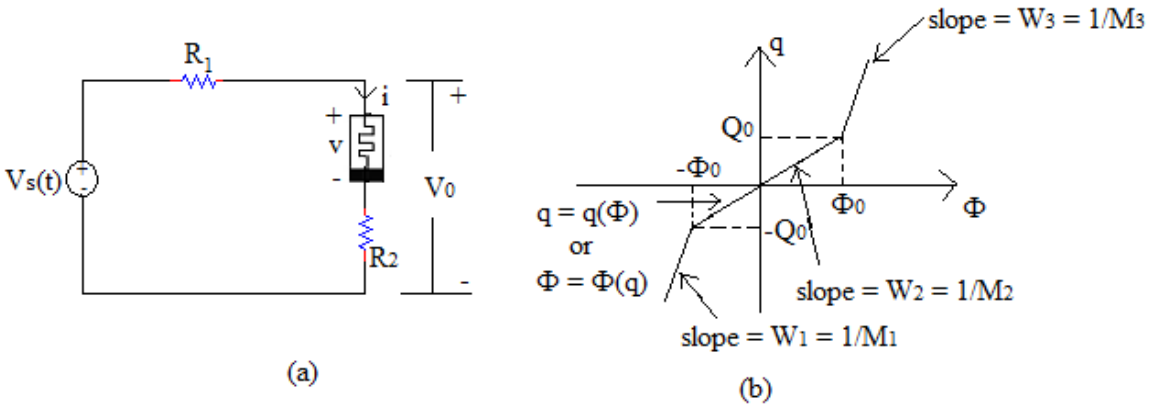


Fig.2.12 (a)Memristor circuit and (b)Φ-q curve to model an amorphous device[1]

The order of complexity of the circuit shown in fig.2.12 (a) is one and its state equation is given by

$$dq/dt = v_s(t)/[R_1 + R_2 + M(q)] \tag{2.19}$$

The solution of equation (2.19) is given as

$$q(t) = h^{-1} \text{ o } (\int_{t_0}^{t} v_s(\tau)d\tau + \Phi(q(t_0))) \tag{2.20}$$

where,
$$h(q) = (R_1 + R_2)q + \Phi(q) \tag{2.21}$$

and $\Phi = \Phi(q)$ represents the memristor's Φ-q curve shown in fig 2.12(b). From equation (2.21), it is observed that h(q) is a strictly monotonically increasing function of charge q and hence its inverse will also exist. The output voltage $v_0(t)$ is found as

$$v_0(t) = v_s(t) - R_1[\frac{dq(t)}{dt}] \tag{2.22}$$

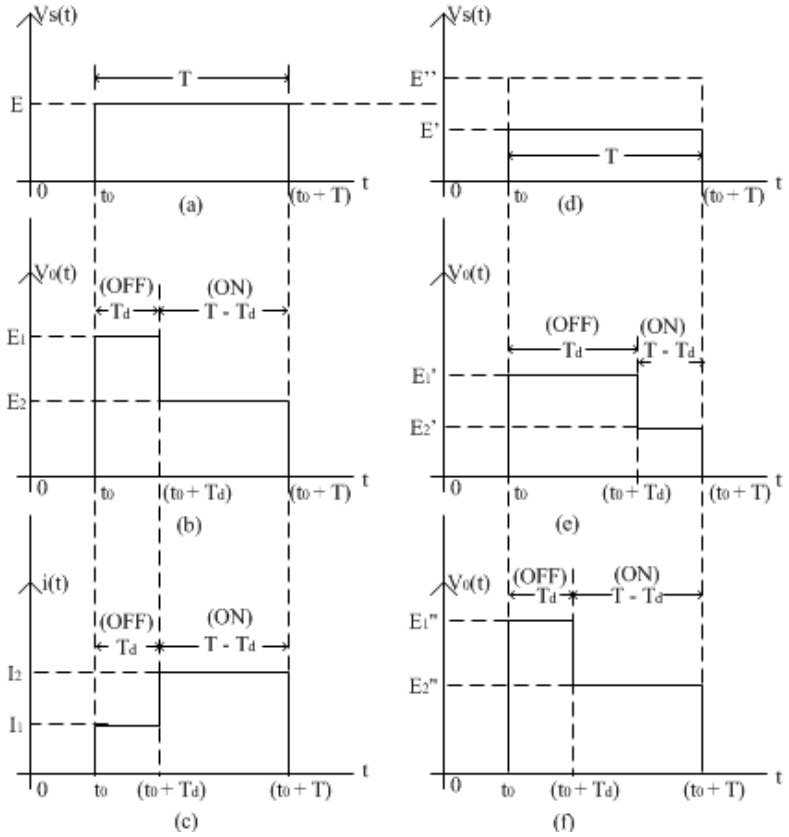


Fig.2.13 Output voltage waveform $v_0(t)$ for simple memristor circuit shown in fig.2.12(a) corresponding to the square wave pulse signal $v_s(t)$[1]

Let $v_s(t)$ is a square wave pulse signal as shown in fig.3.13(a) and $q(t_0) = 0$ at some initial time t_0 then the output waveforms $v_0(t)$ and i(t) can be derived using equations (2.20), (2.21) and (2.22), which are shown in fig2.13(b) and 2.13(c) respectively. These output waveforms can be characterized using following parameters:

$$E_1 = [(M_2 + R_2) / (M_2 + R_1 + R_2)] E \quad (2.23)$$

$$E_2 = [(M_3 + R_2) / (M_3 + R_1 + R_2)] E \quad (2.24)$$

$$I_1 = E / (M_2 + R_1 + R_2) \quad (2.25)$$

$$I_2 = E / (M_3 + R_1 + R_2) \quad (2.26)$$

$$T_d = [\Phi_0 + (R_1 + R_2)Q_0] / E \quad (2.27)$$

where M_2 and M_3 are the memristance of the corresponding line segments 2 and 3 of the Φ-q curve of the memristor shown in fig2.12(b) and coordinates (Q_0, Φ_0) represents the breakpoint between these two segments. From equation (2.27), it is clear that time delay T_d is inversely proportional to the amplitude E of the square pulse wave shown in fig.2.13(a) i.e. on increasing E, T_d will decrease. Hence, to illustrate it three square wave pulse signal having amplitude E, E' and E'' have been plotted in fig.2.13(a) and (d) and their corresponding output voltage has been plotted in fig 2.13(b),(e) and (f). This type of behavior for an amorphous ovanic switch can be observed in [9] and [10]. The memristor with Φ-q curve shown in fig.2.12(b) can simulate not only square wave pulse signal but also describe the phenomena of decrease in time delay T_d with increase in amplitude E.

2.4.1.2 Modeling an Electrolytic E-cell

An electrolytic E- cell is a two terminal electrochemical device, which can produce time delay ranging from few seconds to months. It is also known as a "Coul Cell". E-cell consists of three components namely an anode, a cathode and an electrolyte immersed in an electrolytic plating tank.

Usually, anode is made of gold which is surrounded by silver can which act as cathode also. The initial amount of silver helps in controlling the time delay of E-cell. Within the specified time interval, silver ions will be transferred from anode to cathode. Due to this, E-cell will act as a liner resistor having low value of resistance. However, at the end of the time interval, E- cell will behave as a liner resistor having high value of resistance. Hence, E-cell should be modeled as time varying linear resistor whose resistance can vary from low value to high value after applying DC current for a specified time period equal to the time interval.

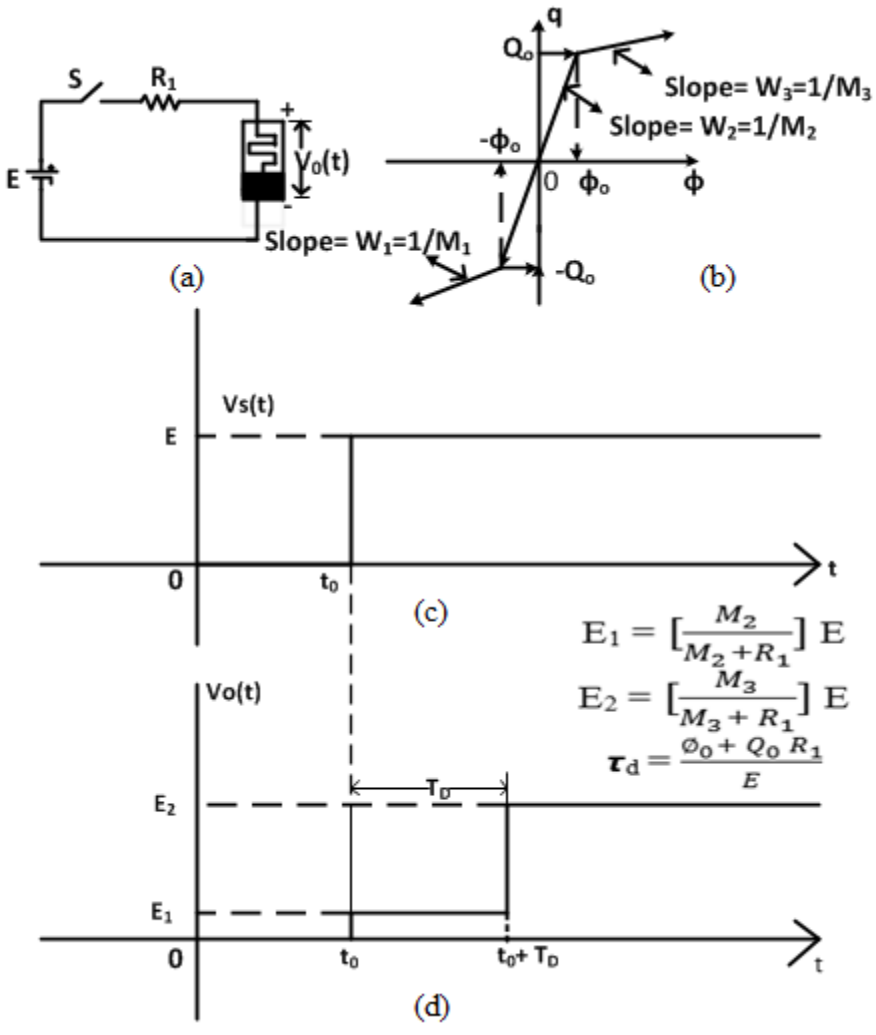


Fig.2.14 (a) E-cell model using memristor (b) its Φ-q curve with timing diagram of input and output shown in (c) and (d) respectively[1]

To show this behavior of E- cell, a memristive model with the Φ-q curve has been shown in fig.2.14(a) and (b) respectively. In this model, E-cell has been replaced by the memristor and its timing diagram has been shown in fig.2.14(c) and (d) to demonstrate the validity of the model shown in 2.14(a). The manufacturer provides the exact quantity of silver so that exact amount of current can be supplied to the E-cell and hence the timing interval. The effect of closing of switch S in fig.2.14(a) is same as giving the step input voltage having amplitude E (in volts) at time $t = t_0$ as shown in fig.2.14(c). From the output waveform shown in fig2.14(d), it is observed that there is an abrupt change in the value of voltage level. It is due to the piecewise linear nature of the Φ-q curve. It also interprets that the change in the resistance from low value to high value is achieved within a small time delay t_d.

2.4.2 Application of Memristor to Signal Processing

Memristors plays an important role in processing different types of signals and in generating various waveforms for practical purposes. In this thesis, an application of memristor for generating staircase waveform has been presented. Staircase waveform plays an important role in different instruments such as the sampling oscilloscope and the transistor curve tracer.

The four step staircase waveform shown in fig.2.14(d) suggests that the E-cell memristor model shown in fig.2.14(a) can be used to generate staircase signal. Another model using memristor to generate staircase signal with its Φ-q curve has been shown in fig.2.15(a) and (b) respectively. This model has been derived by connecting non linear resistor across second port of the M-R mutator. To realize the non linear resistor, two back to back series Zener diodes has been connected with linear resistor in parallel as shown in fig.2.15. For

generating the staircase waveform, the square wave generator v_s has been connected in series with the port 1 of the M-R mutator and with 1Ω resistor as shown in fig.2.15(c). The Φ-q curve and the oscilloscope tracings of both the input signal $v_s(t)$ and the output signal $v_o(t)$ has been shown on fig. 2.15(d) and (e) respectively. The output $v_o(t)$ obtained is a staircase signal. The finite value of the resistance of the Zener diode V-I characteristic gives the finite value of rise time for going from one-step to another step.

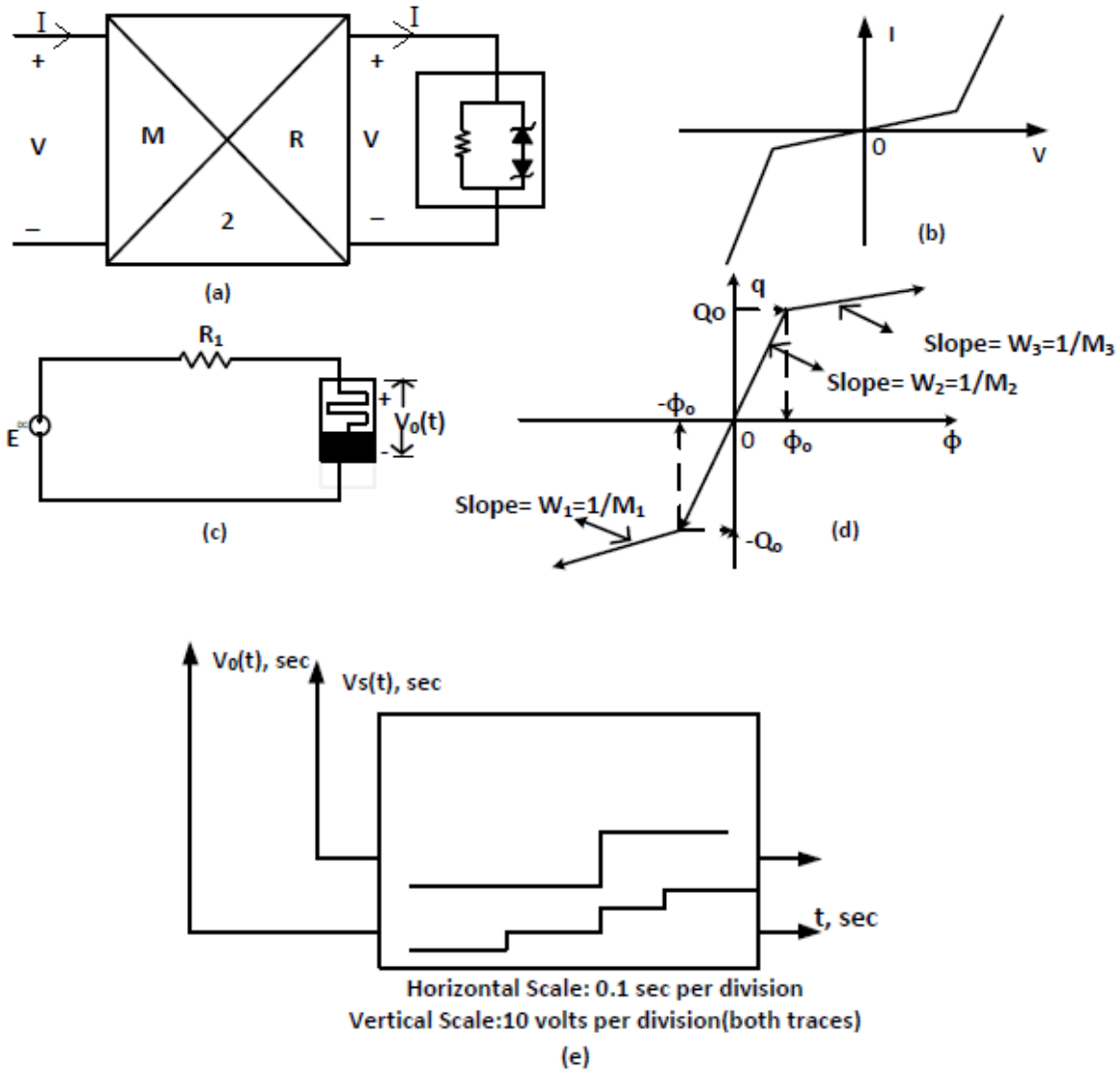


Fig.2.15 (a) Memristor circuit for generating staircase signal and (b) its Φ-q curve (c) signal generator in series with mutator and (d) its Φ-q curve (e) Oscilloscope trace of input signal $v_s(t)$ and output signal $v_o(t)$[1]

With the above circuit, staircase signal waveform with any no. of steps can be generated easily. The circuit for generating ten step staircase signal waveform has been presented in fig.216(a) and its V-I and Φ-q curve has been plotted in fig.2.16(b) and (c) respectively. Its input signal $v_s(t)$ and output signal $v_o(t)$ has been plotted in fig.2.16(d) and (e) respectively.

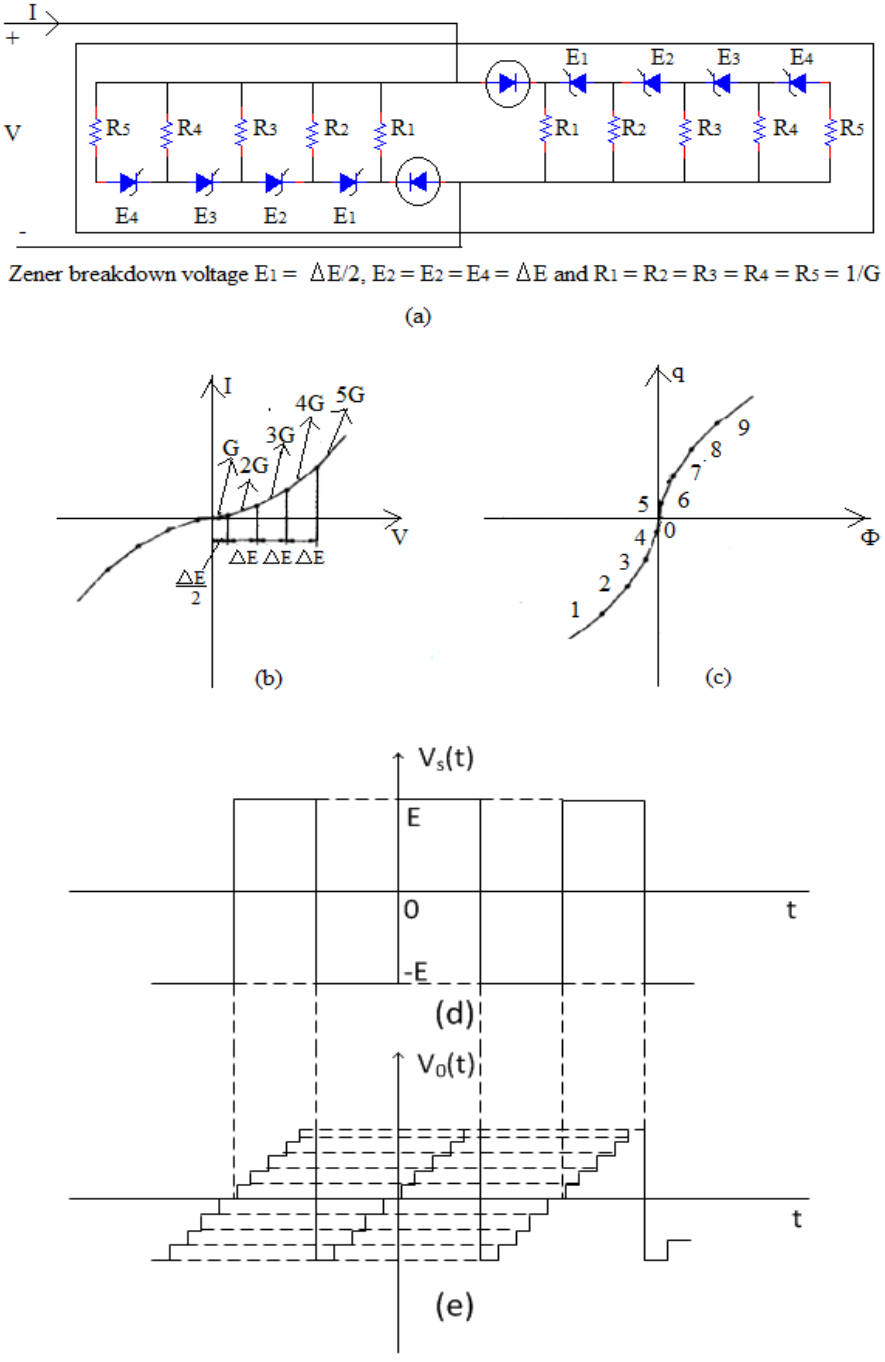


Fig.2.16 Nine segment memristor can be used to generate ten step staircase periodic waveform[1]

Except of the applications discussed in the previous section, memristors also finds application in sensors, cellular networks, different analog circuits, chaotic circuits, non volatile memories and in digital logic neuromorphic systems. Other than this, memristors have already been used in programmable analog circuits, automatic gain control circuits, oscillators and basic arithmetic operators. Memristors also plays an important in the field of nanotechnology and that is why it attracts the attention of many designers.

As the physical realization of memristor is not possible due to cost and technology problem, many emulator circuits has been developed. These emulator circuits act as real memristor i.e. shows the property same as TiO_2 based memristor. A memristor emulator circuit using CDTA has been proposed in this thesis about which we will study in the upcoming chapters.

CHAPTER 3

Memristor Emulator Circuits

In literature, a variety of macromodels and emulator circuits were reported to show the memristive properties [11-20]. In [11], flux controlled memristor circuit was introduced. This circuit can verify the properties of memristor experimentally but hardware realization was not possible. Piecewise linear model [4], spice macromodels [12-19] and cubic non-linear functions [20] were proposed to produce the memristor properties. Some of these models were proposed by HP labs. For memristor simulation, these macromodels were beneficial but hardware realization of these macromodels was not possible. Due to this reason, memristor emulator circuit using active blocks and passive components were introduced in the literature. These emulators show the properties same as actual emulator. These has been developed for real device application. This chapter gives a brief account of active block based memristor emulator circuits.

3.1 Memristor emulator circuits based on active blocks

Due to the complex design and excessive cost, physical realization of memristor is not possible. Hence, memristor emulator circuits were developed as a replacement of memristors. These memristor emulator circuits are designed with various active building blocks (ABB) and are discussed below.

In [20-23,25], op-amp based memristor emulator circuit has been introduced. These circuits operate at low frequency with high speed. In [24], the emulator circuit based on ADC has been introduced. However, due to the sampling frequency of ADC and stepping resolution,

the performance of the circuit is limited. In [26, 27], the emulator circuit based on solid-state device has been introduced. These circuits also operate at low frequency.

In [19, 27-29], CMOS based emulator circuits were introduced. However, these circuits have their own disadvantages. In [19], excessive resistors were used which make the circuit very bulky. In [27], the circuit has a problem of mismatch error on layout. There is no practical evidence for the circuit introduced in [28]. The circuit introduced in [29] uses voltage-controlled resistor, which reduces the linearity of the circuit.

In [30], the emulator circuit based on varactor, diodes and inductor has been introduced, but the presence of inductor make the circuit bulky and costly. In [32], a light dependent resistance (LDR) based emulator circuit has been introduced, but the functionality of the device is limited due to the physical properties of LDR.

In [31, 33-36, 40], current conveyor (CCII+) has been used for designing of the emulator circuit. In [31], emulator circuit uses voltage-controlled resistor as well which causes the reduction of the linearity of the transistor. The circuit introduced in [33] was found unsuitable for the complex circuits. In [35,36], the problem is large input impedance of the device which limits the operation of circuit which are driven by current.

In [37-39], CFOA based emulator circuits were introduced. The circuit introduced in [37] uses OTA as well to show the property of memristive devices. This circuit operates at low frequency. The emulator circuit based on CBTA introduced in [42] also operates at low frequency. In [41, 43] emulator circuits operating at high frequency were introduced. The circuit introduced in [41] uses CCTA while circuit introduced in [43] uses VDTA as active building block.

The salient features of available memristor emulators are summarized in Table 3.1. Following are the observations:

1. The memristor emulator circuits discussed in [21-40,42,43] uses more than one active building block (ABB). Hence, it becomes difficult to design these emulator circuits. Only [41] uses single ABB, which makes the circuit simple.
2. These emulator circuits also require passive elements. With the help of single capacitor, memristor emulator circuits discussed above have been designed except [33]. In [33], two capacitors are used for designing the emulator circuit. However, number of resistor used in the circuits is not same. Two or more than two resistors are required for the designing of emulator circuits. In [25,28,40,42,43], two resistors are required for emulator circuits while rest of the circuits require more than two resistors.
3. Some of the memristor emulator requires multiplier circuits also. The multiplier circuit makes the designing of emulator circuit more complex. [25,28,34-36,39,40,42,43] uses multiplier circuit for designing of emulator circuit.
4. Memristor emulator circuits can be either incremental type or decremental type. With the help of single switch, the emulator circuits can operate in these modes. In [25], emulator circuit uses switch to behave as either incremental type or decremental type. In rest of the circuits, with small change in the circuitry, they can behave as incremental type or decremental type.
5. Some of the emulator circuit uses diodes. These diodes help in maintaining the equivalent resistance of the emulator circuit. [33,38] uses diodes for designing of memristor emulator circuit.

Table 3.1: Comparison of memristor emulator circuits

Ref.	No. and type of ABB used	Single(S)/ Multiple(M) type of ABB	No. of resistor used	No. of capacitor used	Use of multiplier circuit	Type of memristor
[25]	10 MOS, 2 op-amp	M, different type ABB	2	1	Yes	FI, FD
[28]	1 DDCC	S	2	1	Yes	FI, FD
[33]	3 CCII, 1 diode	M, different type ABB	4	1	No	GI, GD
[34]	3 CCII, 1 buffer	M, different type ABB	5	1	Yes	GI, GD
[35]	2 CCII, 2 op-amp	M, different type ABB	7	1	Yes	-
[36]	4 CCII, 1 op-amp	M, different type ABB	8	1	Yes	FI, FD
[37]	2 CFOA, 1 OTA	M, different type ABB	3	1	No	GI
[38]	4 CFOA, 2 diodes	M, different type ABB	4	1	No	FI
[39]	4 AD844,	M, same type ABB	5	1	Yes	FI, FD
[40]	2 CCII	M, same type ABB	2	1	Yes	FI, FD
[41]	1 CCTA	S	3	1	No	FI, FD, GI, GD
[42]	1 CBTA	S	2	1	Yes	GI, GD
[43]	1 VDTA	S	2	1	Yes	FI, FD

FI: Floating Incremental, FD: Floating Decremental, GI: Grounded Incremental, GD: Grounded Decremental

In the last, it can be summarized that this chapter reviews the memristor emulator circuits based on active building blocks. A variety of active blocks are used to design these emulator circuits and the minimum component count is – single active block, one capacitor and three resistors.

CHAPTER 4

Current Differencing Transconductance Amplifier

In field of VLSI design, current mode (CM) devices plays an important role in comparison to their counterpart voltage mode(VM) devices. Some of their advantages have already been discussed in chapter 1. CDTA is an active building block belongs to the family of CM devices. It was invented by D. Biolek[44] in 2005 using current conveyors and dual output operational transconductance amplifier (OTA). CDTA is one of the versatile devices of CM family and therefore, it is being used in the area of Analog Signal Processing (ASP). Afterward, the bipolar implementation of CDTA was reported in 2005[45-47]. Next, the CMOS based CDTA was used in 2006[48] for the designing of KHN filter. Later on in 2008, CMOS based CDTA was introduced having low parasitic impedance and higher speed in comparison to the CDTA existed at that time. These parasitics effect generates the non ideal behavior of CDTA.

4.1 Ideal CDTA

Fig.4.1 shows the circuit symbol of ideal CDTA which was proposed by D. Biolek in 2005. It has a pair of low-impedance current inputs p, n and an auxiliary terminal z, whose outgoing current is the difference of input currents. Here, output terminal currents $I_{x\pm}$ are equal in magnitude, but flow in opposite directions, and the product of transconductance (g_m) and the voltage at the z terminal gives their magnitudes.

From fig 4.1, it can be observed that for the operation of CDTA, there are three possible ways, which are; (1) All currents are flowing into the CDTA, (2) All currents are flowing outside of the CDTA and (3) currents are flowing in different direction.

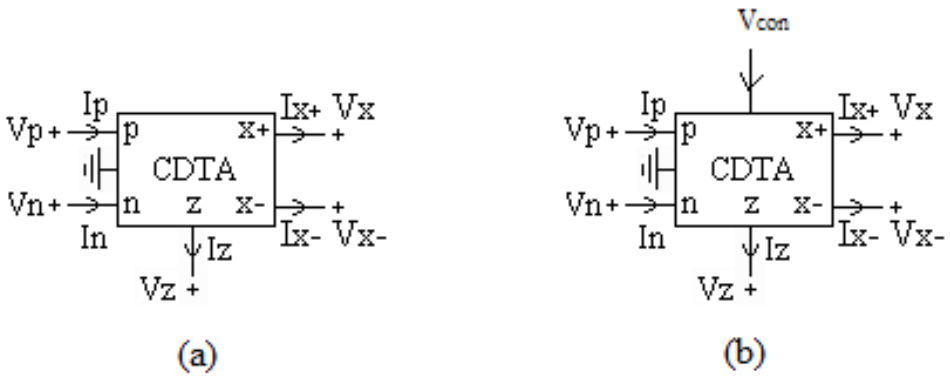


Fig. 4.1 (a) Ideal CDTA block[44] (b) Improved CDTA block

Ideal CDTA is a combination of two blocks: Current Differencing Unit (CDU) at the input stage and dual output Operational Transconductance Amplifier (DO-OTA) block. This model of CDTA has been shown is fig.4.2.

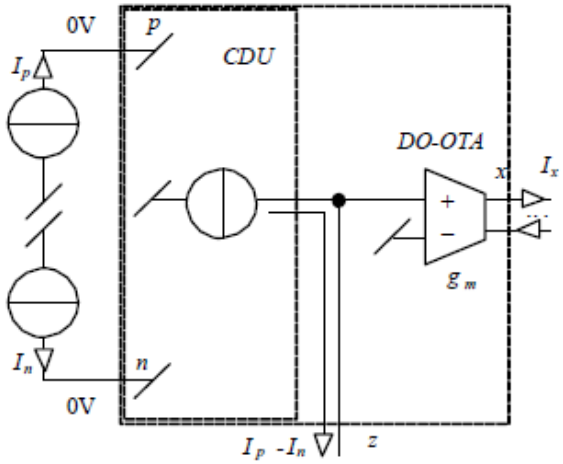


Fig.4.2 Behavioral Model of CDTA

The CDU unit takes current I_p and I_n as input current, sense the difference between these two currents and gives there difference as output to the z-terminal of CDU. The OTA block is connected in series with the CDU block. Hence, the output current I_z is provided to the OTA by converting it into the voltage V_z with the help of the external impedance. This

OTA will give the output current I_{x+} and I_{x-} which are same in magnitude but opposite in direction. Most of the time, the non-inverting terminal of OTA is connected with ground to use it as an amplifier. The equations to depict the behavior of the CDTA are as follows:

$$V_p = V_n = 0 \tag{4.1}$$

$$I_z = I_p - I_n \tag{4.2}$$

$$I_{x\pm} = \pm g_m V_z \tag{4.3}$$

$$V_z = I_z R_z \tag{4.4}$$

where R_z is the external impedance connected with the Z terminal of CDTA and g_m is the transconductance of CDTA, which can be controlled by controlling/biasing voltage V_{con} as shown on fig.4.1(b).

The following equation matrix can describe the overall behavior of ideal CDTA explained by equation (4.1) to (4.4).

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_{x\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \tag{4.7}$$

4.2 Non-ideal CDTA

Practically, CDTA does not follow its ideal equation described in the previous section. There is some non-ideality in the behavior of CDTA due to various reasons. The effect of non-idealities can be categorized into two groups: parasitics and tracking error. CDTA has parasitic low-value series resistors (R_p and R_n) at the input terminals p and n, and also parasitic resistors and capacitors from the terminals z and x to the ground ($R_z \parallel C_z$ and $R_x \parallel C_x$), respectively. Fig 4.3 shows the non ideal structure of CDTA[49].

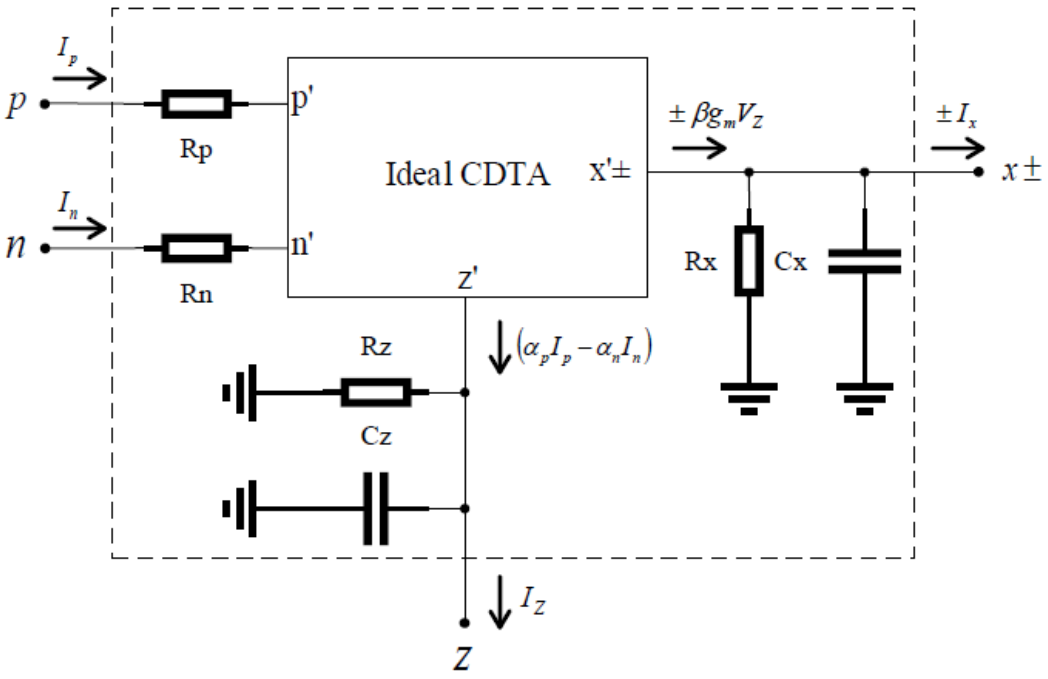


Fig.4.3 Non-ideal structure of CDTA[49]

Taking the effect of non idealities into consideration, the ideal equations of CDTA get change in the following manner:

$$V_p = V_n = 0 \tag{4.8}$$

$$I_z = \alpha_p I_p - \alpha_n I_n \tag{4.9}$$

$$I_{x\pm} = \pm \beta\, g_m V_z \tag{4.10}$$

$$V_z = I_z R_z \tag{4.11}$$

where, $\alpha_p = 1 - \varepsilon_p$, $|\varepsilon_p| << 1$ and $\alpha_n = 1 - \varepsilon_n$, $|\varepsilon_n| << 1$. α_p represents the current transfer error from p to z terminal, α_n represents the current transfer error from n to z terminal and β represents the transconductance inaccuracy factor from z to x terminal. These parasitic values slightly differ from their ideal unit values by the effect of the CDTA tracking errors, those absolute values being much less than unity and ideally taken as unity.

The behavior of the non ideal CDTA described from equation (4.8) to (4.11) has been represented in the matrix form in equation (4.12).

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_{x\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha & -\alpha & 0 & 0 \\ 0 & 0 & 0 & \pm\beta g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \tag{4.12}$$

4.3 Internal Structure of Modified CDTA

The symbol and non ideal structutre of modified CDTA has been presented in fig.4.4(a) and (b) respectively and the internal structure of modified CDTA has been presented in fig.4.5. In the modified structure of CDTA, transistor M1-M20 represents the current differencing unit and transconductance functionality is realized by transistor M21-M37. The circuits for CDU and TA block are adopted from [50] and [35] respectively. A controlling/biasing voltage V_{con} terminal has also been used in this structure. This V_{con} will help in controlling the transconductance gain g_m of the circuit. This behavior of V_{con} has been explained in the equation given below:

$$g_m = 2k(V_{con} + V_{ss} - V_T) \tag{4.13}$$

where k is the device parameter and is given by

$$k = \mu_n C_{ox} \frac{W}{L} \tag{4.14}$$

where W and L are channel width and channel length respectively. μ_n, C_{ox} and V_T are mobility of carrier, oxide thickness and threshold voltage of MOS respectively. Hence, by controlling g_m, the gain of CDTA can be controlled.

The functionality of modified CDTA shown in fig.4.5 is verified through SYMICA DE simulation using 0.25µm TSMC CMOS parameter. The circuit is biased with voltages of V_{DD} = 2.5V, V_{SS} = -2.5V and $I_1 = I_2$ = 20µA. Aspect ratio of MOS transistor is shown in table 4.1. All the MOS transistors are operating in the saturation region.

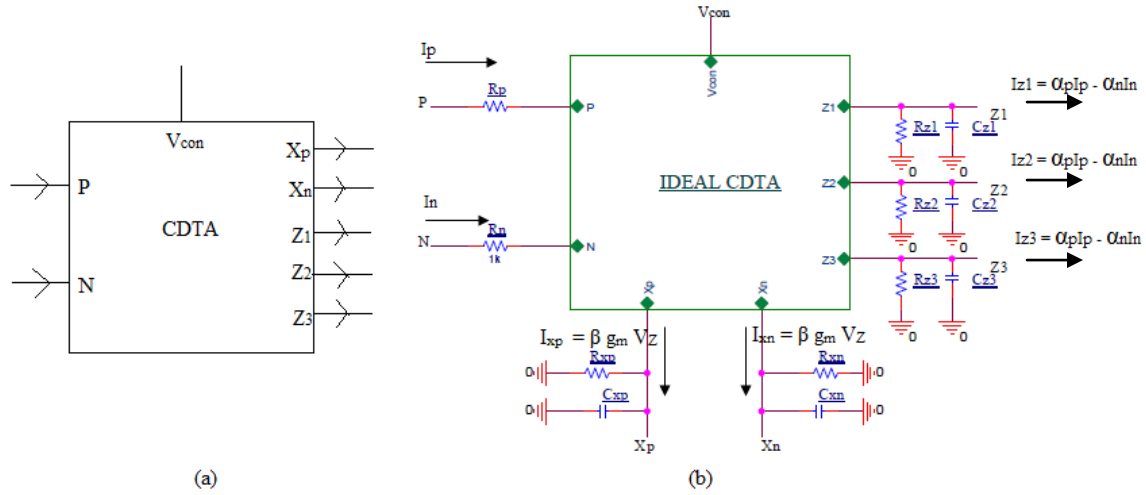


Fig 4.4 (a) Ideal and (b) non-ideal structure of modified CDTA

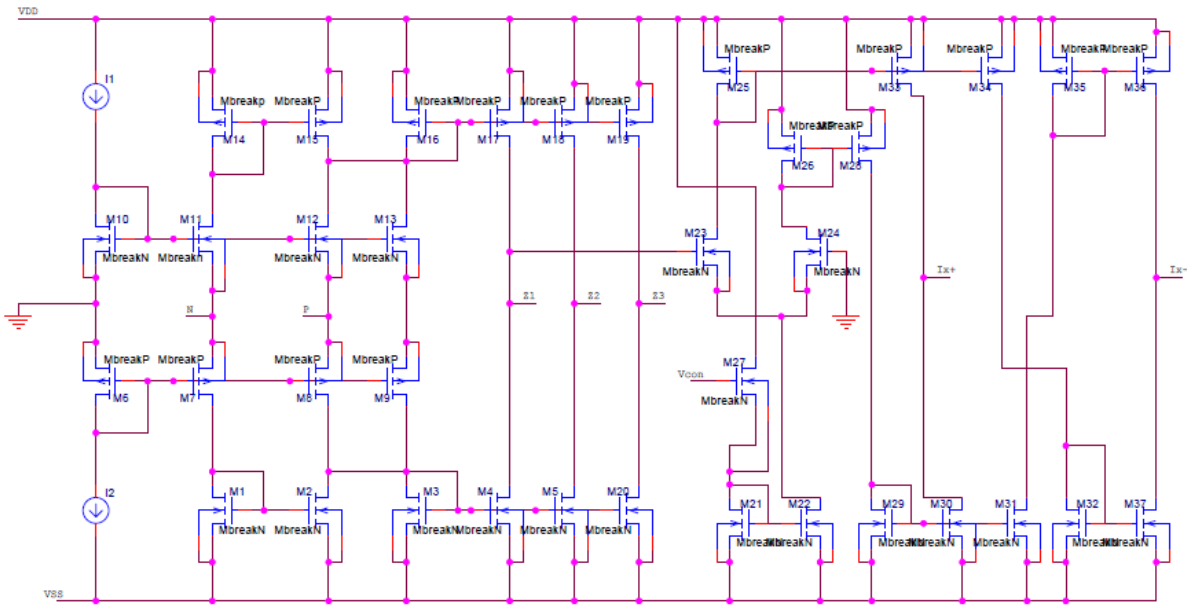


Fig 4.5 Modified Structure of CDTA

Table 4.1 Dimension of MOS Transistors

Transistors	W(µm)/L(µm)
M1,M2	5/0.5
M3,M4,M5,M20	6/1.5
M6,M7,M8,M9	4/0.5
M10,M11,M12,M13	2/0.5
M14,M15	15/0.5
M16,M17,M18,M19	15/1.5
M21-M37	15/0.5

4.4 Simulation Result of Modified CDTA

In order to show the functionality of modified CDTA circuit, simulations using SYMICA DE software have been performed and the technology used is TSMC 0.25µm. The circuit is biased with voltage V_{DD} = 2.5V, V_{ss} = -2.5V and the value of bias current $I_1 = I_2$ = 60µA. The aspect ratio of all transistors is same as shown in table 4.1.

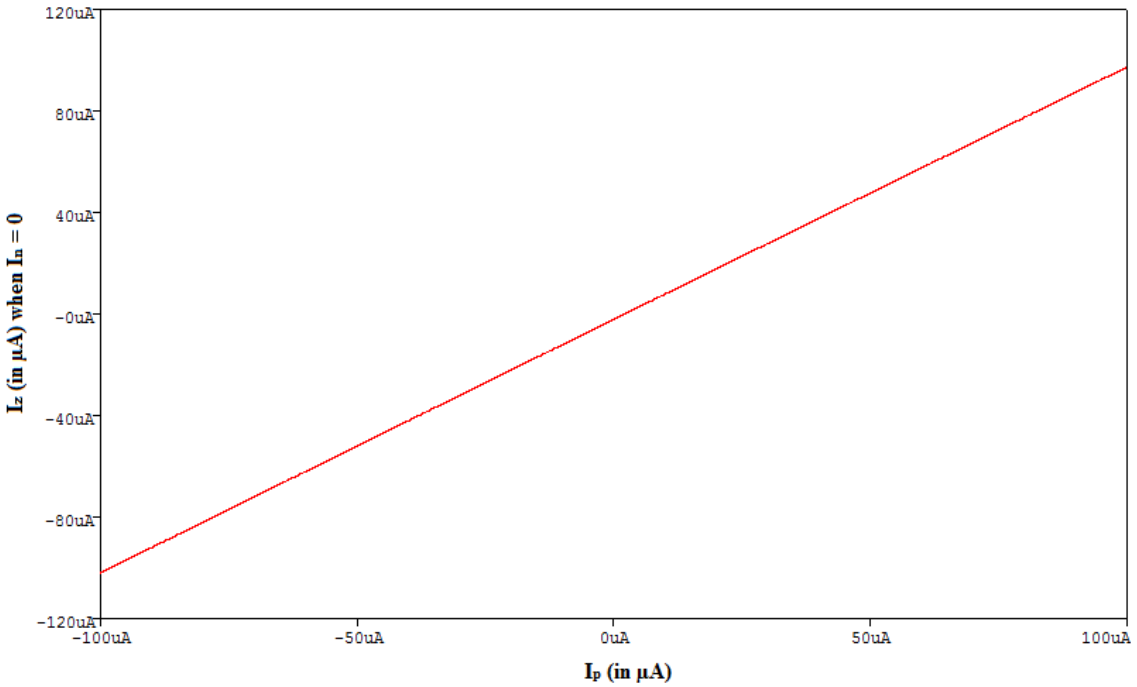


Fig 4.6 Current Transfer from p-terminal to z-terminal with $I_n = 0$ (I_z vs I_p)

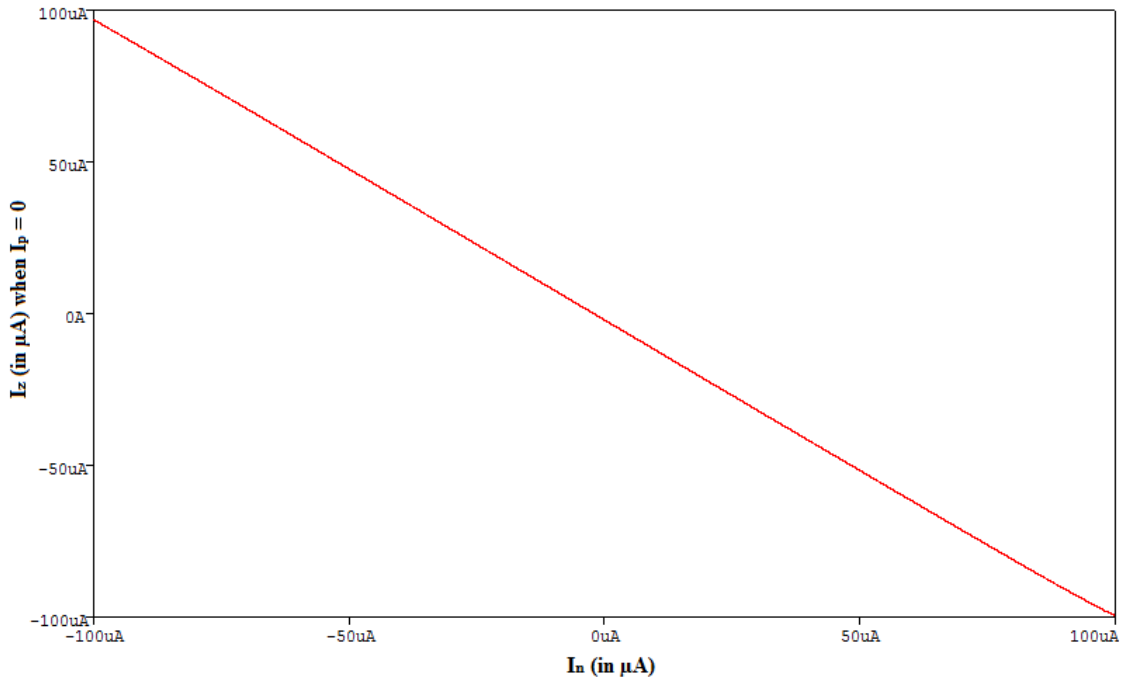


Fig 4.7 Current Transfer from n-terminal to z-terminal with $I_p = 0$ (I_z vs I_n)

Fig.4.6 and 4.7 describe the DC behavior of CDTA. In fig.4.6, the current transfer curve between p-terminal to z-terminal has been plotted keeping $I_n = 0$. Similarly, in fig.4.7, the current transfer curve between n-terminal to z-terminal has been plotted keeping $I_p = 0$. In both plots, I_p and I_n has been varied from -100µA to +-100µA.

According to equation 4.2 of ideal CDTA, $I_z = I_p - I_n$. Hence, if $I_n = 0$ than $I_z = I_p$ i.e. I_z will follow I_p linearly which has been shown by fig.4.6. Similarly, if $I_p = 0$ than $I_z = - I_n$ i.e. I_z will follow I_n linearly but in opposite direction as shown in fig.4.7.

Fig.4.8 shows the variation in the transconductance gain (g_m) of CDTA, when controlling voltage V_{con} is varied from -2V to +2V. From fig.4.8, it is clear that the range of V_{con}, to control g_m is from -1.8V to +1.6V and the range of transconductance g_m, upto which g_m can be varied is from (0 to 2.7)mA/V.

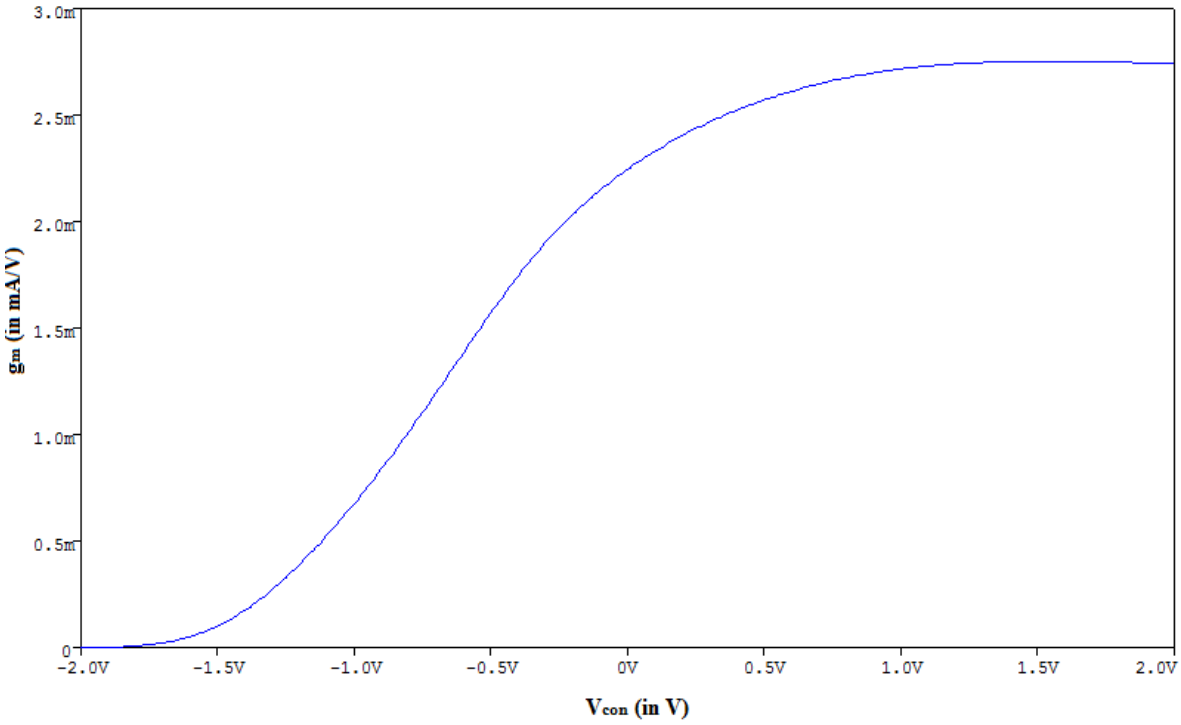


Fig. 4.8 Transconductance gain (g_m) vs. V_{con}

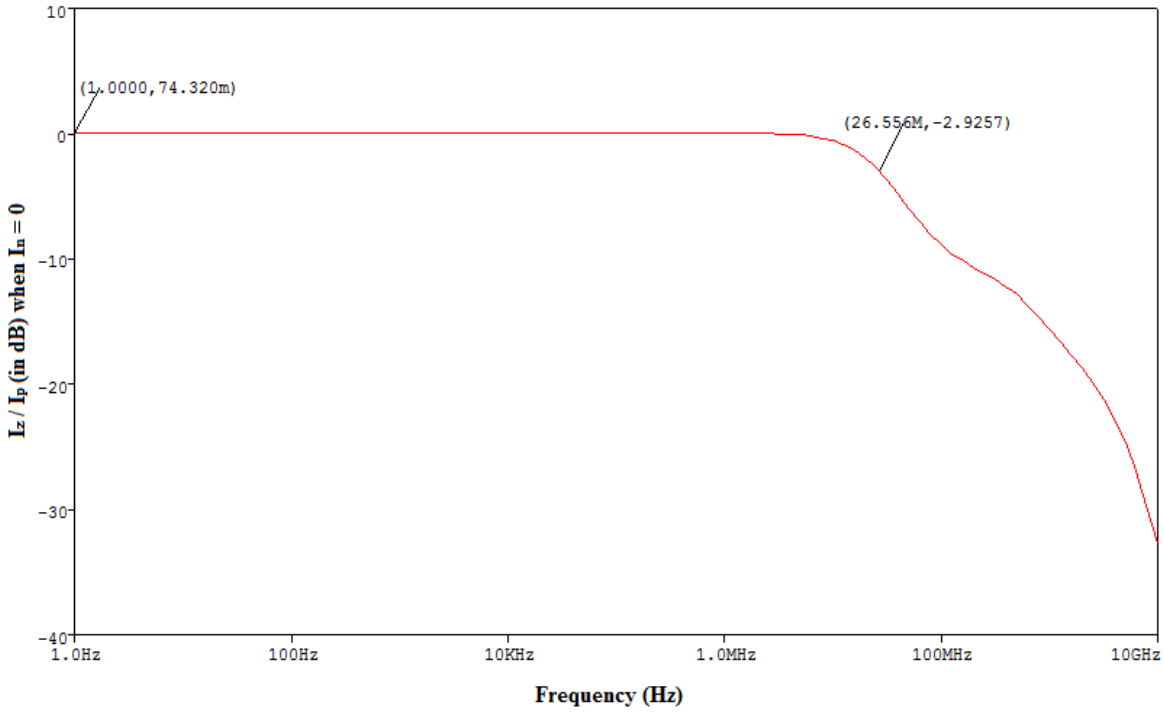


Fig. 4.9 Gain Bandwidth curve from p-terminal to z-terminal with $I_n = 0$ (I_z/I_p vs frequency)

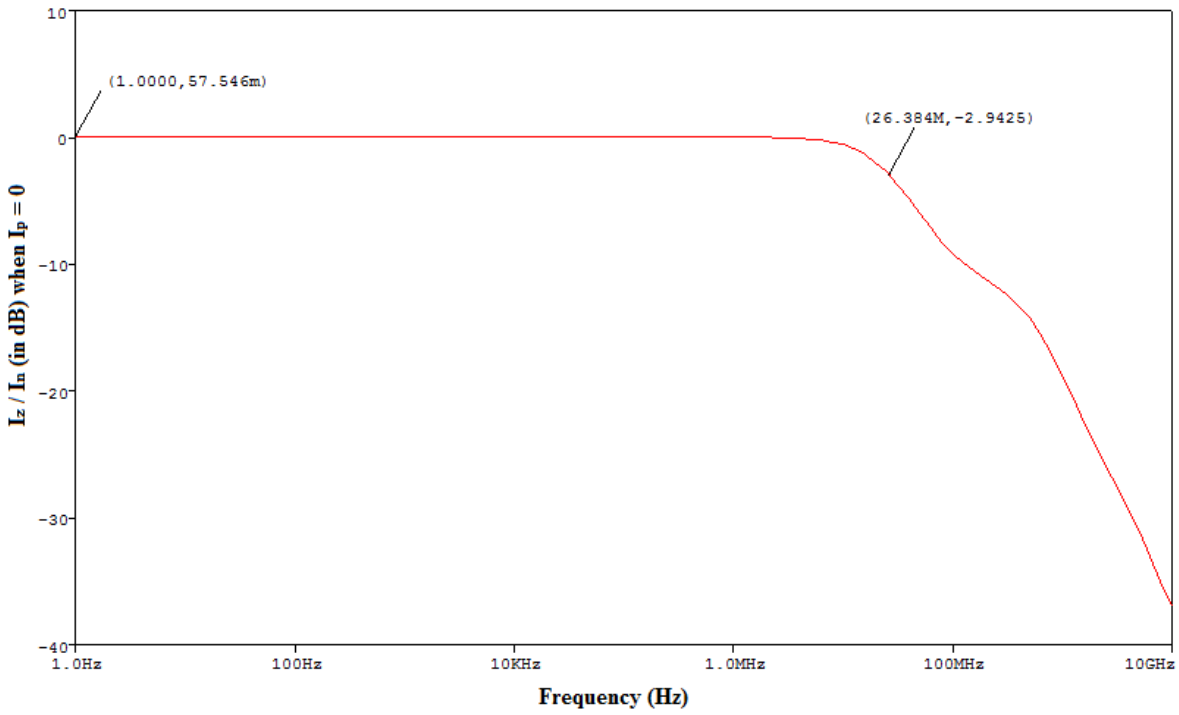


Fig. 4.10 Gain Bandwidth curve from n-terminal to z-terminal with $I_p = 0$ (I_z/I_n vs frequency)

Fig.4.9 and 4.10 shows the AC behaviour of CDTA block. Fig.4.9 is the gain bandwidth curve when z-terminal current varies with respect to change in p-terminal current i.e. I_z/I_p vs frequency keeping n-terminal current equal to zero i.e. $I_n = 0$. The parasitic gain α_p and current tracking error ε_p from p-terminal to z-terminal and its bandwidth are measured from the I_z/I_p vs frequency plot and the values of these parameters are found as follows:

$$\alpha_p = \frac{Iz}{Ip} = 74.320\text{mdB} = 1.0086 \quad (4.15a)$$

$$\varepsilon_p = 1 - \alpha_p = 1 - 1.0086 = -0.0086 \quad (4.15b)$$

$$\text{3-dB bandwidth} = 26.556\ \text{MHz} \quad (4.15c)$$

Similarly, fig.4.10 is the gain bandwidth curve when z-terminal current varies with respect to change in n-terminal current i.e. I_z/I_n vs frequency keeping p-terminal current equal to zero i.e. $I_p = 0$. The parasitic gain α_n and current tracking error ε_n from n-terminal to z-

terminal and its bandwidth are measured from the I_z/I_n vs frequency plot and the values of these parameters are found as follows:

$$\alpha_n = \frac{Iz}{In} = 57.546\text{mdB} = 1.0066 \quad (4.16a)$$

$$\varepsilon_n = 1 - \alpha_n = 1 - 1.0066 = -0.0066 \quad (4.16b)$$

$$\text{3-dB bandwidth} = 26.384\ \text{MHz} \quad (4.16c)$$

Fig.4.11 shows simulated the frequency response of transconductance gain g_m from z-terminal to $x\pm$ terminal. The transconductance gain g_m is obtained from transconducatnce almpifier (TA) block of CDTA. Hence, g_m is obtained by ploting $I_{x\pm}$ when AC voltage supply is given to the z-terminal of CDTA.

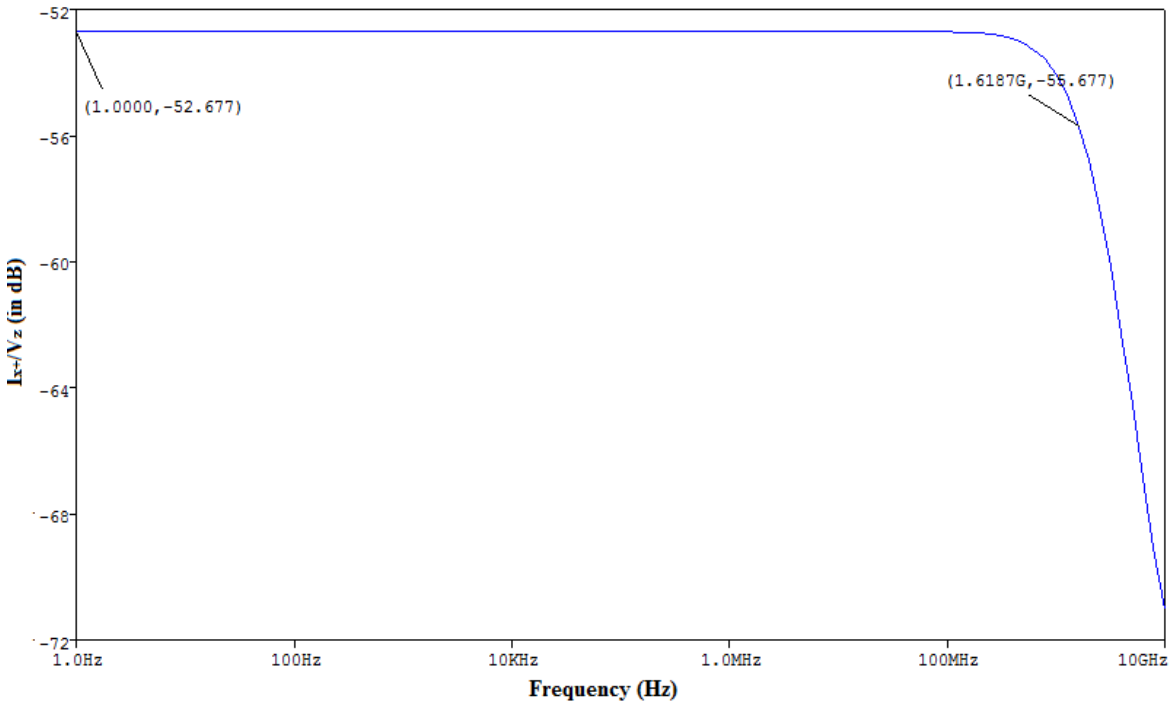


Fig. 4.11 Transconductance gain g_m from z-terminal to x+ terminal ($Ix+/V_z$ vs frequency)

From fig.4.11,

$$g_m = -52.677 = 2.323\text{mA/V} \quad (4.17a)$$

$$\text{3-dB bandwidth} = 1.6187\text{GHz} \quad (4.17b)$$

All the results of simulation presented in this section verify the performance of modified CDTA block. The summary of DC and AC performance of modified CDTA has been listed in table 4.1.

Table 4.2: CDTA parameter

Parameters	Value
Power supply	$\pm$ 2.5V
Process Parameter	TSMC 0.25µm
Parasitic gain	$\alpha_p = 1.0086$ $\alpha_n = 1.0066$
Input Current Dynamic Range	-100µA to +100µA
3-dB bandwidth	26.556MHz (I_z / I_p when I_n= 0) 26.384MHz (I_z / I_n when I_p= 0) 1.6187GHz (I_x / V_{Z1})
Transconductance range	(0 - 2.7) mA/V
V_{con} range for controlling g_m	-1.8V to +1.6 V

This CDTA block finds application in various analog circuits such as current mirror, adder or summing amplifier, subtractor or differencing amplifier, lossless integrator, impedance inverter, CM based Schmitt trigger, CM-KHN biquad filter etc.

CHAPTER 5

Proposed Memristor Emulator Circuit Based on CDTA

Memristor is a fourth basic circuit element introduced by L. O. Chua in 1971[1]. It relates the charge q with flux Φ. Initially, memristor was a hypothetical concept. But, after 37 years of discovery of memristor, Williams and his coworkers invented the physically realizable TiO_2 based solid state memristor in HP labs in 2008. However, due to cost problem and many other complications in fabrication process at nano scale level, it was not possible to build solid state memristor. Hence, its emulator circuits were introduced in literature. These emulator circuits act as real memristors. There are various emulator circuits based on active blocks such as OTA, CCII, CCTA, VDTA etc. This has already been described in chapter 2.

5.1 Introduction of Proposed Emualator Circuit

In this section, the proposed memristor emulator circuit based on CDTA has been introduced. This emulator circuit uses single CDTA block as an active element, two resistors and one capacitor. This proposed emulator has simple circuitry as it does not require any extra circuit like multiplier, ADC, DAC etc. In fig.4.5, the structure of proposed emulator circuit has been demonstrated. This proposed circuit behaves as a floating type incremental/decremental memristor emulator circuit.

Considering, the ideal behavior of the proposed emulator circuit in fig.5.1(a), the input current (I_{in}) is obtained as

$$I_{in} + I_{x\pm} = \frac{V_{in}}{R_1} \quad (5.1)$$

And according to the ideal characteristics of CDTA,

$$I_{x\pm} = \pm g_m V_{Z1} \tag{5.2}$$

and

$$V_{Z1} = I_{Z1} R_2 \tag{5.3}$$

On putting equation (5.2) and (5.3) in equation (5.1), we get

$$I_{in} \pm g_m I_{Z1} R_2 = \frac{V_{in}}{R_1} \tag{5.4}$$

From equation (4.2) describs the ideal characteristics of CDTA. Here putting I_n=0, we get

$$I_{z1} = I_p - I_n = I_p = \frac{V_{in}}{R_1} \tag{5.5}$$

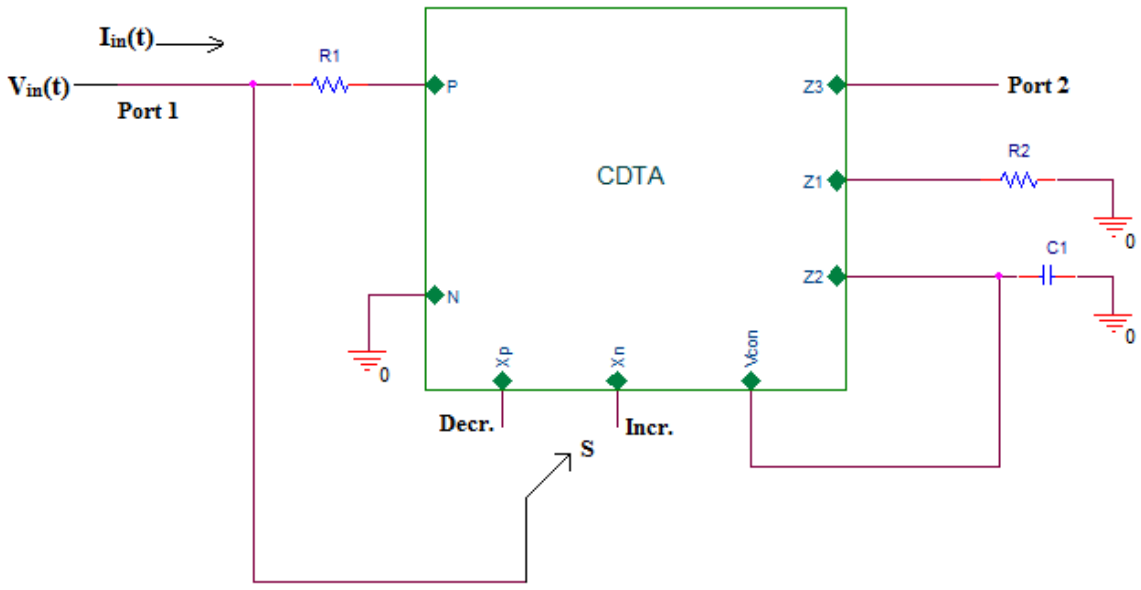


Fig.5.1 Proposed Emulator Circuit when I_n = 0

From equation (4.13),

$$g_m = 2k(V_{con} + V_{ss} - V_T)$$

On substituting equation (4.13) and (5.5) in equation (5.4),

$$I_{in} = \frac{V_{in}}{R_1} \mp 2k(V_{con} + V_{ss} - V_T)\frac{V_{in}}{R_1} R_2 \quad (5.6)$$

And $$V_{con} = \frac{q_c(t)}{C} \quad (5.7)$$

Then the memconductance equation of the proposed emulator circuit is obtained as

$$W = \frac{I_{in}(t)}{V_{in}(t)} = \frac{1}{R_1} \mp 2k(V_{ss} - V_T)\frac{R_2}{R_1} \mp 2k\frac{q_c(t)}{C}\frac{R_2}{R_1} \quad (5.8)$$

Now, if the input is given to the n- terminal of CDTA block and p-terminal is kept at zero i.e $I_p = 0$ as shown in fig 5.2

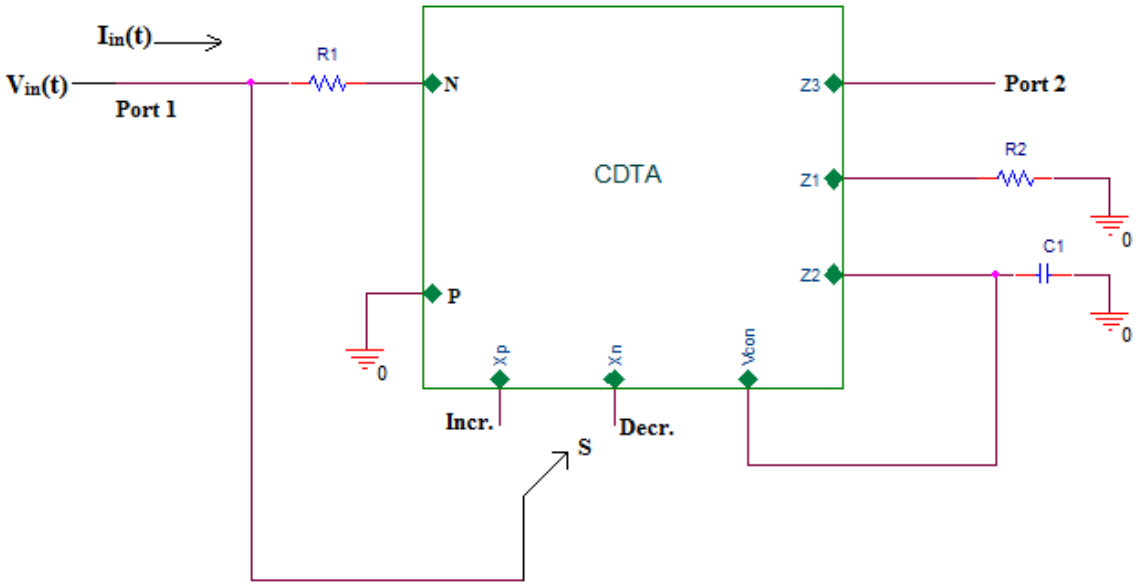


Fig.5.2 Proposed Emulator Circuit when $I_p = 0$

Hence, from fig. 5.2,

$$I_z = I_p - I_n = -I_n = -\frac{V_{in}}{R_1} \quad (5.9)$$

$$I_{in} \pm g_m I_{Z1} R_2 = \frac{V_{in}}{R_1} \quad (5.10)$$

On putting equ.(5.9) in equ.(5.10), we get

$$I_{in} \pm g_m \left(-\frac{V_{in}}{R_1}\right) R_2 = \frac{V_{in}}{R_1} \quad (5.11)$$

On putting the value of g_m and rearranging equ.(5.11), we get

$$I_{in} = \frac{V_{in}}{R_1} \pm \frac{V_{in}}{R_1} 2k(V_{con} + V_{ss} - V_T) R_2 \quad (5.12)$$

On putting the value of $V_{con} = \frac{q_c(t)}{C}$ in above equation, the value of memconductance will be as follows,

$$W = \frac{I_{in}(t)}{V_{in}(t)} = \frac{1}{R_1} \pm 2k(V_{ss} - V_T) \frac{R_2}{R_1} \pm 2k \frac{q_c(t)}{C} \frac{R_2}{R_1} \quad (5.13)$$

Hence, the value of memconductance can be controlled by varying the amplitude of input voltage V_{in} and by varying the value of passive components R and C. The incremental or decremental behavior is decided by X± terminal of CDTA. On providing feedback through +(p) terminal, the proposed emulator circuit will act as incremental circuit and when feedback is given via – (n) terminal, it will act as decremental circuit.

5.2 Non-ideal analysis of Proposed Emulator Circuit

The performance of the CDTA circuit may vary from its ideal characteristics because of the non-idealities. Now, taking into consideration, the effect of non idealities, the modified port relationships of CDTA can be written as

$$V_p = V_n = 0$$

$$I_z = \alpha_p I_p - \alpha_n I_n,$$

$$I_{x\pm} = \pm \beta g_m V_z,$$

$$V_z = I_z R_z$$

where $\alpha_p$and α_n denote the parasitic current gains between p-z and n-z terminals respectively and β represents the transconductance inaccuracy factor between z-x terminals. This non-ideal behavior of CDTA has been already described in section 4.2 of chapter 4.

Now, considering the effect of non idealities and reanalyzing the circuit given in fig 5.1, the memconductance expression for incremental and decemental memristor is modified as

$$W = \frac{I_{in}(t)}{V_{in}(t)} = \frac{1}{R_1} \mp 2k\alpha_p\beta(V_{ss} - V_T)\frac{R_2}{R_1} \mp 2k\alpha_p\beta\frac{q_c(t)}{C}\frac{R_2}{R_1} \quad (5.14)$$

It is clearly seen that the tracking error developed due to non-ideality of CDTA effects the memconductance value.

5.3 Frequency response analysis of Proposed Circuit

For frequency response analysis, let $V_{in}(t) = A_m \sin(\omega t)$, where A_m is the amplitude of the input voltage signal in Volt and ω is the frequency of input signal in radian.

Now, putting time varying part equal to zero in equation (5.8), we get

$$W = \frac{I_{in}(t)}{V_{in}(t)} = \frac{1}{R_1} \mp 2k(V_{ss} - V_T)\frac{R_2}{R_1} \quad (5.15)$$

And

$$q_c(t) = \int I_{in}(t)dt \quad (5.16)$$

From equation (5.15) and (5.16), we get

$$q_c(t) = \frac{A_m}{\omega}\left(\frac{1}{R_1} \mp 2k(V_{ss} - V_T)\frac{R_2}{R_1}\right)\cos(\omega t - \pi) \quad (5.17)$$

On substituting equation (5.17) in equation (5.8), the memconductance of the circuit is obtained as

$$W = \frac{I_{in}(t)}{V_{in}(t)} = \frac{1}{R_1} \mp 2k(V_{ss} - V_T)\frac{R_2}{R_1} \mp \frac{2K}{C}\frac{R_2}{R_1}\frac{A_m}{\omega}\left(\frac{1}{R_1} \mp 2k(V_{ss} - V_T)\frac{R_2}{R_1}\right)\cos(\omega t - \pi) \quad (5.18)$$

From above equation, it can be seen that memconductance contains a linear time variant and linear time invariant part. In equation (5.18), if frequency (ω) tends to infinity, memconductance will behave as time independent conductor, whose value is constant irrespective of time.

The relationship between time variant and time invariant part of mamconductance denotes the frequency dependence of pinched hysteresis loop. This relationship can be obtained by taking ratio of both linear and non-linear the parts which is given below

$$\Phi = \frac{2K}{C}\frac{R_2}{R_1}\frac{A_m}{\omega} = \frac{1}{f\tau} = \frac{T}{\tau} \quad (5.19)$$

where $\boldsymbol{\tau}$ is the time constant of the emulator circuit and it is given as

$$\boldsymbol{\tau} = \frac{\pi R_1 C}{K R_{2} A_m} \quad (5.20)$$

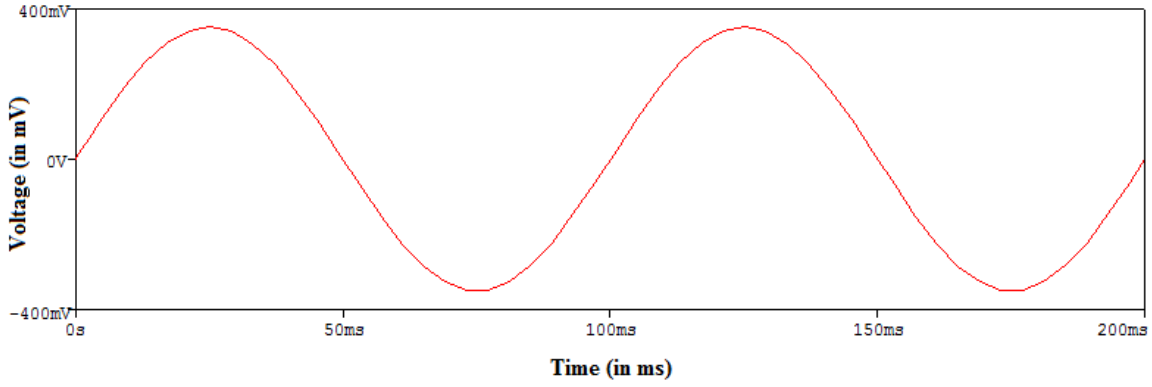
and T is the period of input voltage signal which is given as follows

$$T = \frac{1}{f} = \frac{\pi R_1 C\, \Phi}{K R_{2} A_m} \quad (5.21)$$

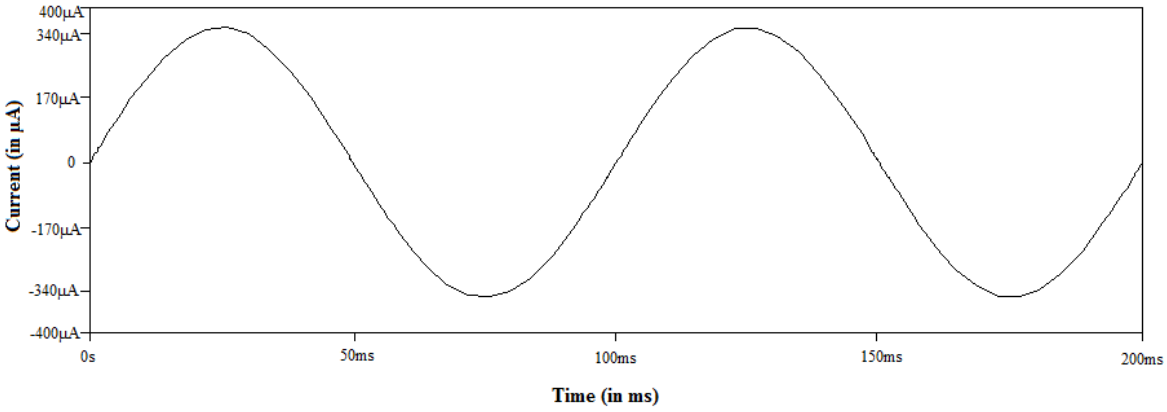
From equation (5.19), it is obvious that Φ is inversely proportional to frequency. Hence, frequency f can be used to hold the pinched hysteresis loop at high frequency.

5.4 Simulation results of Proposed Emulator Circuit

The characteristics and result of CDTA and proposed emulator circuit has been simulated and verified using SYMICA DE and technology used is 0.25µm. For the simulation of proposed emulator circuit, value of R_1 = 2K, R_2 = 4K and A_m = 350mV.



(a)



(b)

Fig. 5.3 (a) voltage time (b) current time characteristic of proposed emulator circuit

Fig 5.3(a) and (b) represents the voltage time and current time characteristic of proposed emulator circuit for A_m = 350mV, R_1 = 2K, R_2 = 4K, C = 10µF and frequency f = 10Hz respectively.

Fig 5.4, 5.5, 5.6, 5.7 illustrates that on changing both frequency(ω) and capacitor(C) value but keeping ωC product constant, the shape of pinched hysteresis loop does not change. It remains constant for both incremental and decremental topology. Hence, one can conclude that if the amplitude of input voltage is constant as well as ωC product is also constant than the value of memristance remains constant. Fig 5.4 and 5.5 shows the pinched hysteresis for incremental topology for $I_n = 0$ and $I_p = 0$ respectively. Similarly, Fig 5.6 and 5.7 shows the pinched hysteresis for decremental topology for $I_n = 0$ and $I_p = 0$ respectively.

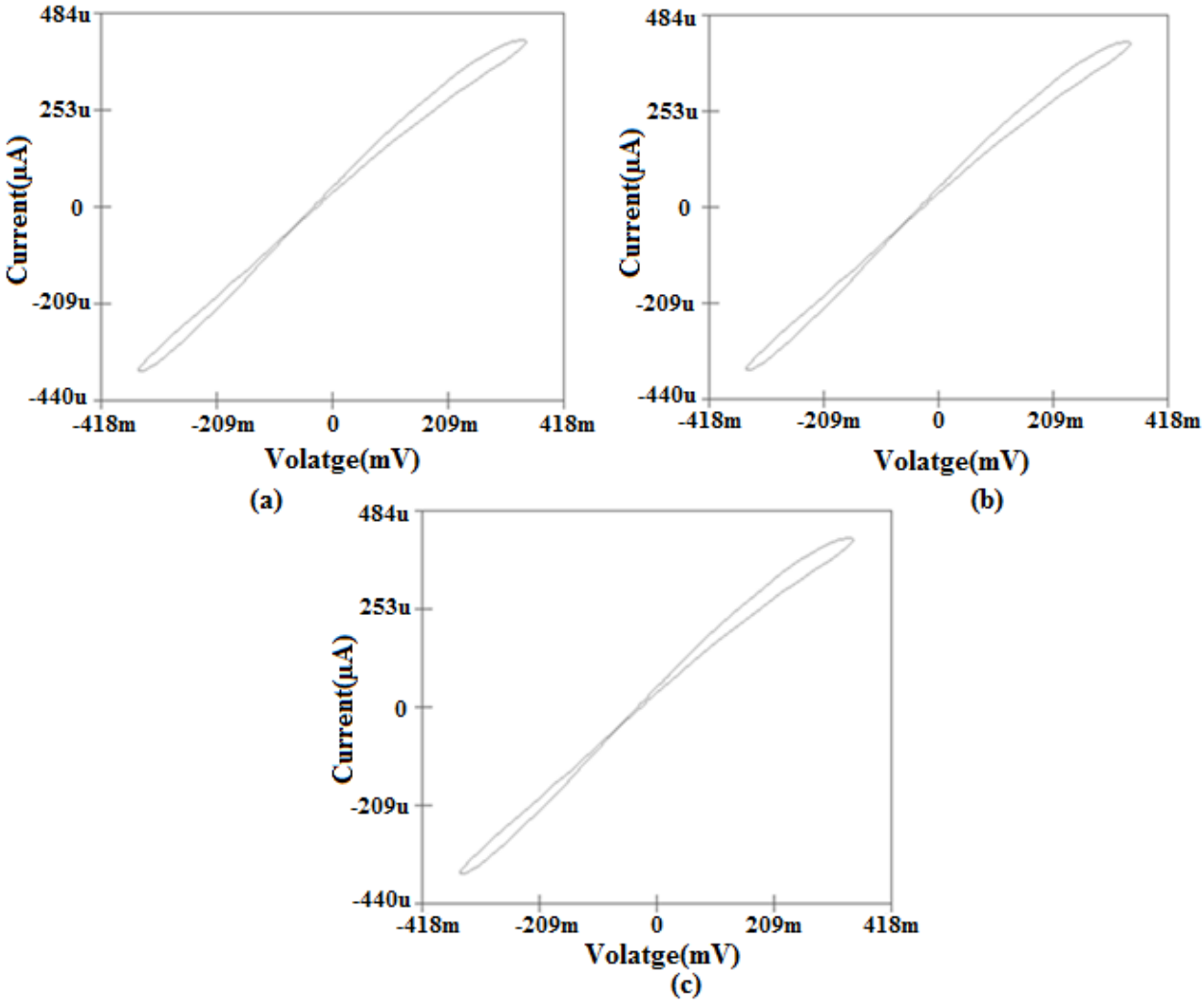


Fig. 5.4 Incremental topology of the proposed emulator circuit for constant ωC when $I_n = 0$ (a) at f = 10Hz and C = 10μF (b) at f = 100Hz and C = 1μF (c) f = 1K and C = 0.1μF

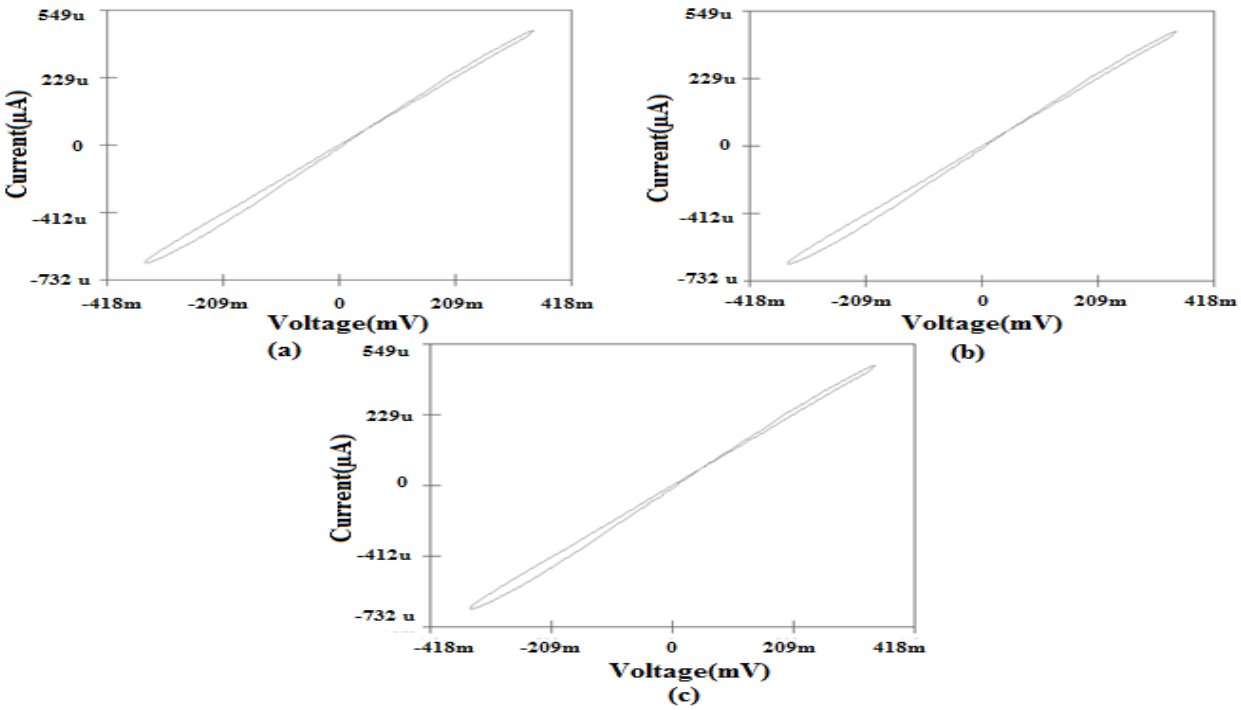


Fig. 5.5 Incremental topology of the proposed emulator circuit for constant ωC when I_p = 0 (a) at f = 10Hz and C = 10µF (b) at f = 100Hz and C = 1µF (c) f = 1K and C = 0.1µF

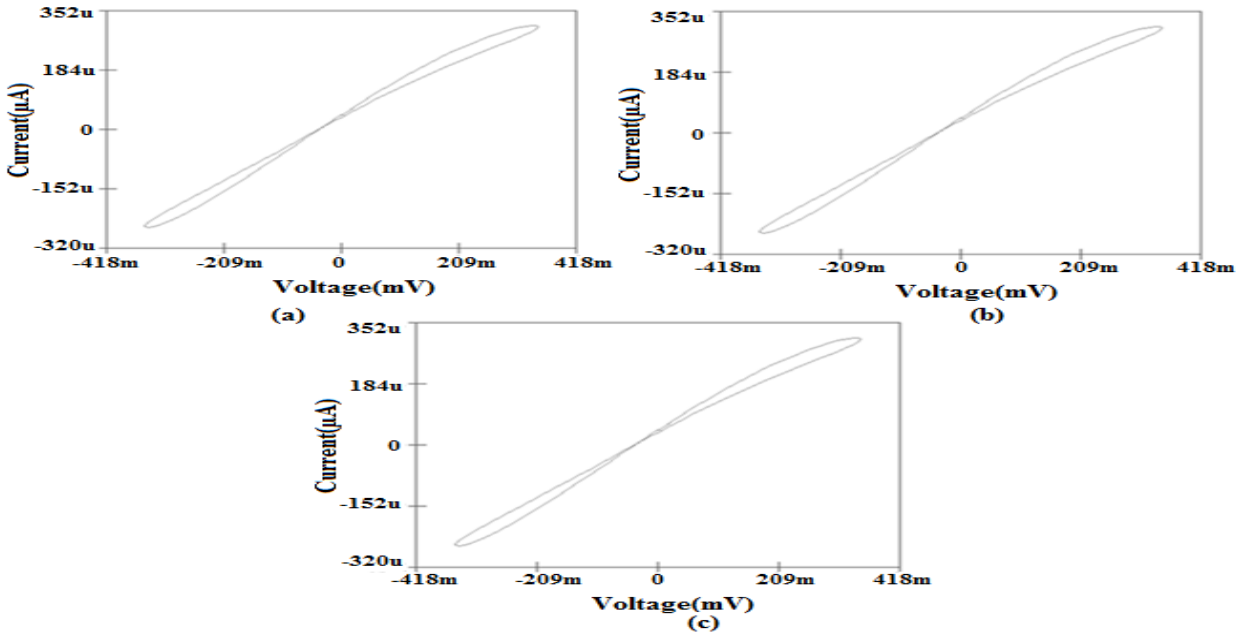


Fig.5.6 Decremental topology of the proposed emulator circuit for constant ωC when I_n = 0 (a) at f = 10Hz and C = 10µF (b) at f = 100Hz and C = 1µF (c) f = 1K and C = 0.1µF

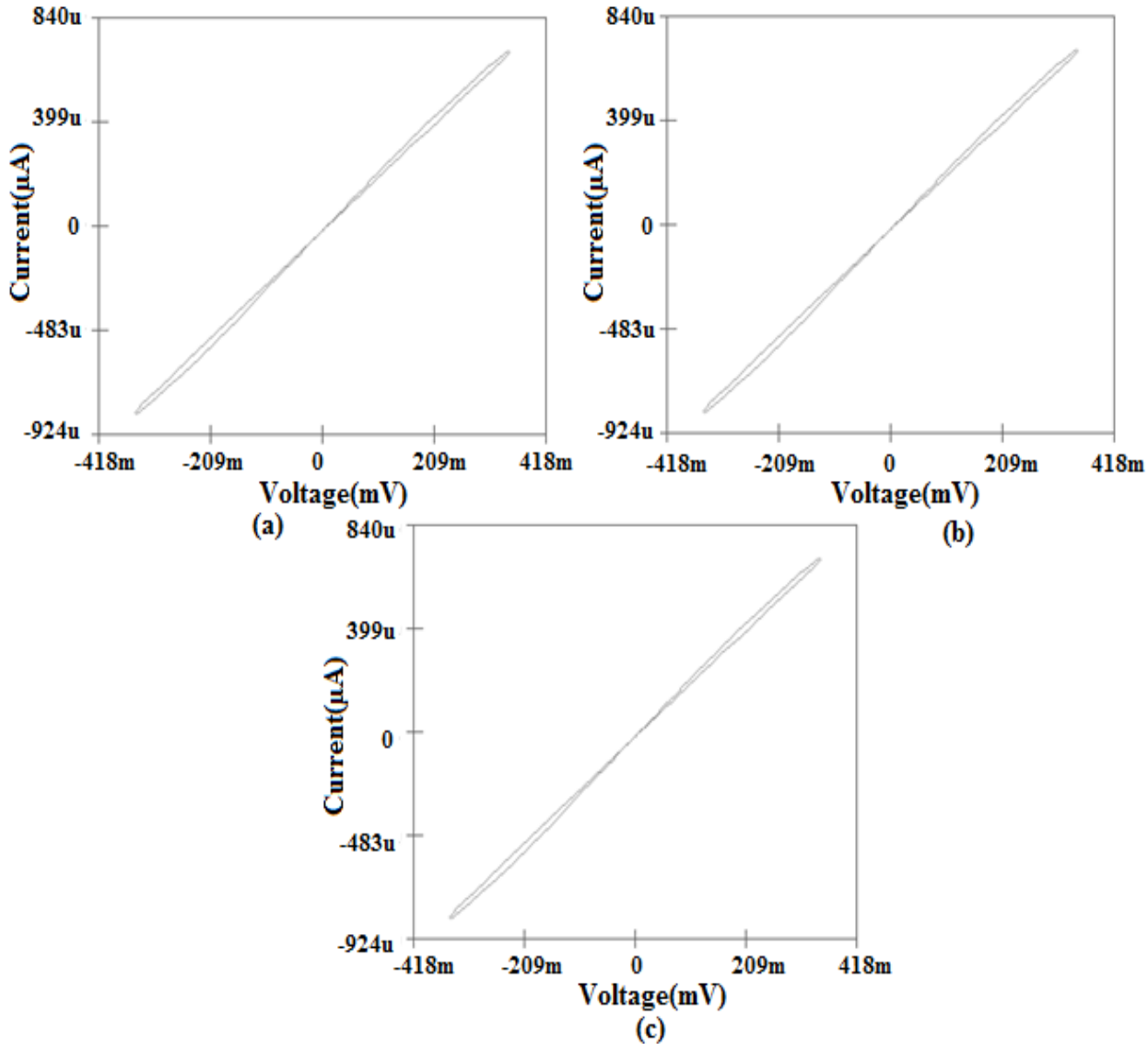


Fig.5.7 Decremental topology of the proposed emulator circuit for constant ωC when I_p = 0 (a) at f = 10Hz and C = 10μF (b) at f = 100Hz and C = 1μF (c) f = 1K and C = 0.1μF

After observing fig.5.4, 5.5, 5.6 and 5.7, one can conclude that memristor emulator circuit shows hysteresis loop of same shape and size if frequency and capacitor product remains constant i.e. ωC = constant. Fig.5.4 and 5.5 shows the I-V curve for incremental topology for I_n = 0 and I_P = 0 respectively. Similarly, Fig.5.6 and 5.7 shows the I-V curve for decremental topology for I_n = 0 and I_P = 0 respectively.

From fig 5.8, 5.9, 5.10 and 5.11, it is illustrated that on keeping capacitor C= 5nF and the amplitude of applied voltage signal A_m = 350mV constant, on the changing the frequency for 10K, 50K and 100K, the width of pinched hysteresis loop decreases. With increase in frequency, time varying part will decrease and consequently memristance converted into linear resistance at higher frequency. At higher frequency, memristance is dominated by linear time invariant part.

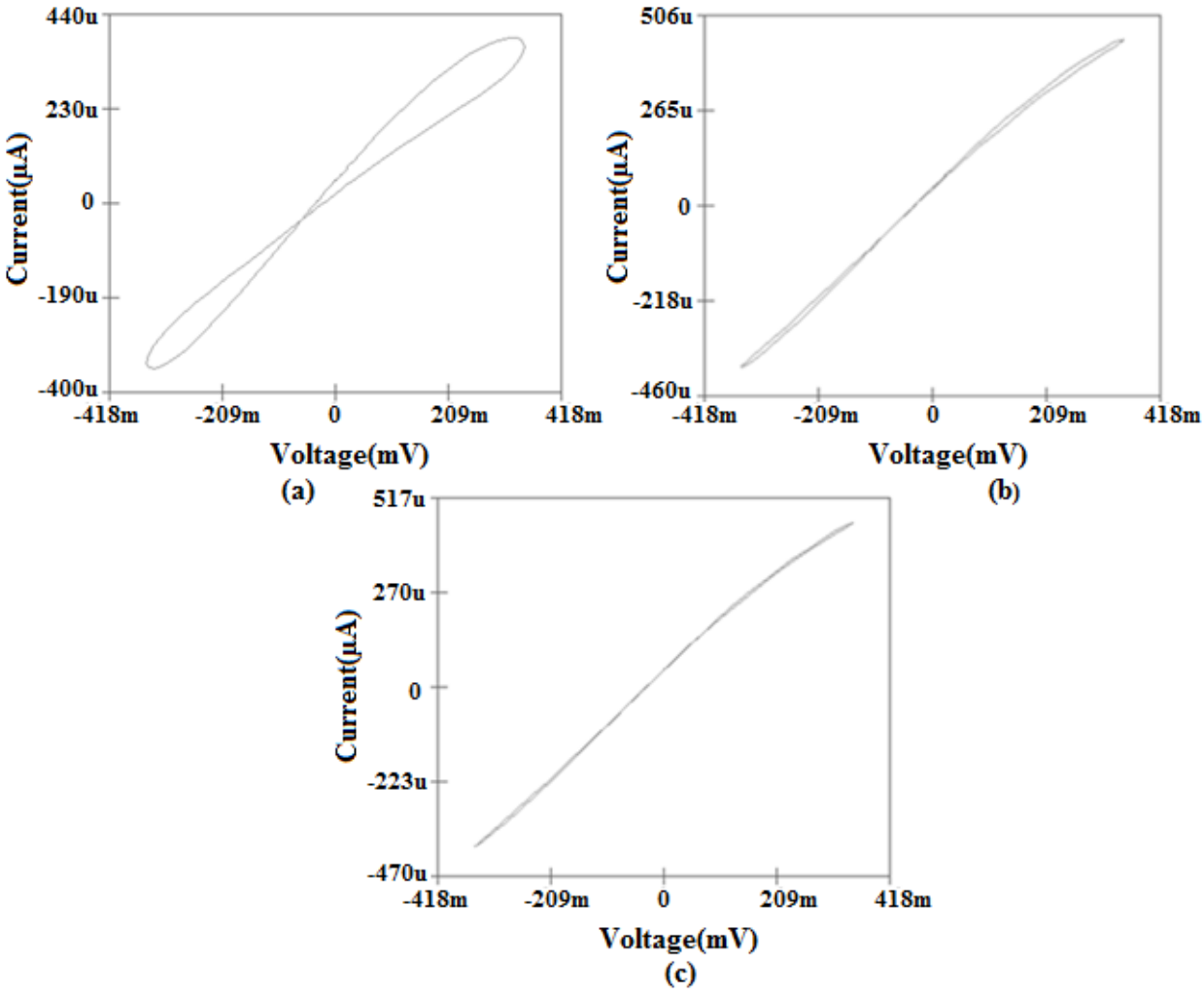


Fig.5.8 Incremental topology of proposed emulator circuit for different frequency but constant C = 5nF when I_n = 0 (a) at f = 10K (b) at f = 50K (c) at f = 100K

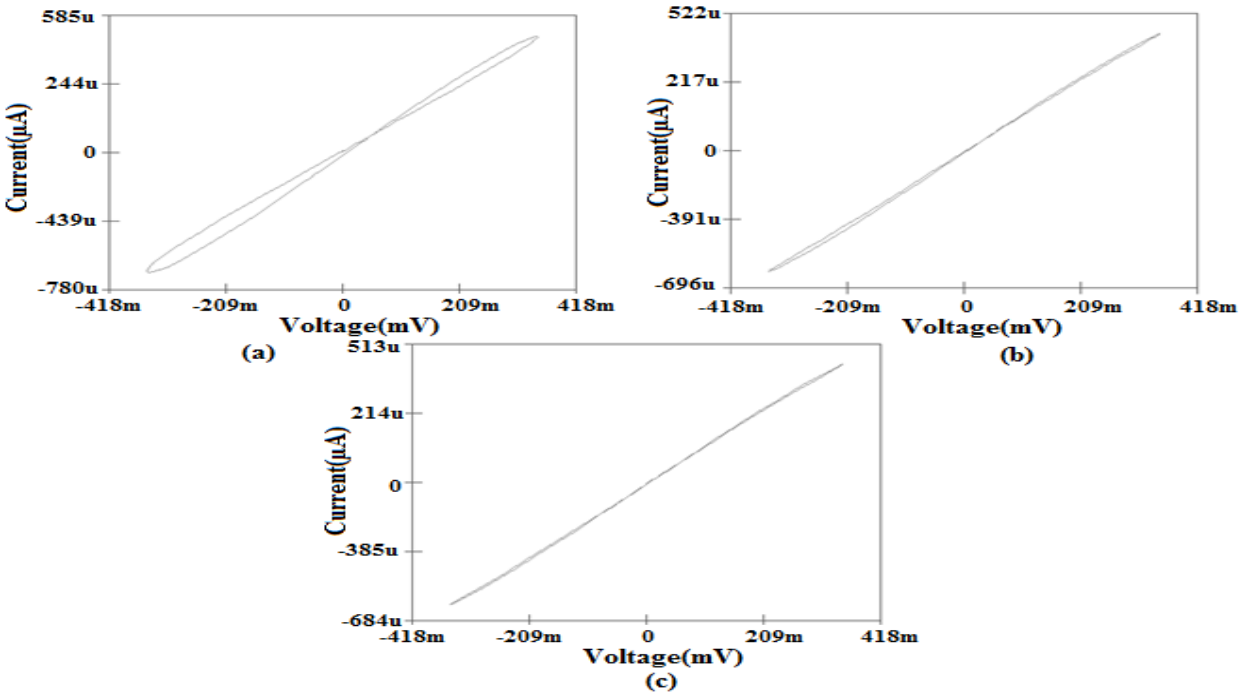


Fig.5.9 Incremental topology of proposed emulator circuit for different frequency but constant C = 5nF when I_p = 0 (a) at f = 10K (b) at f = 50K (c) at f = 100K

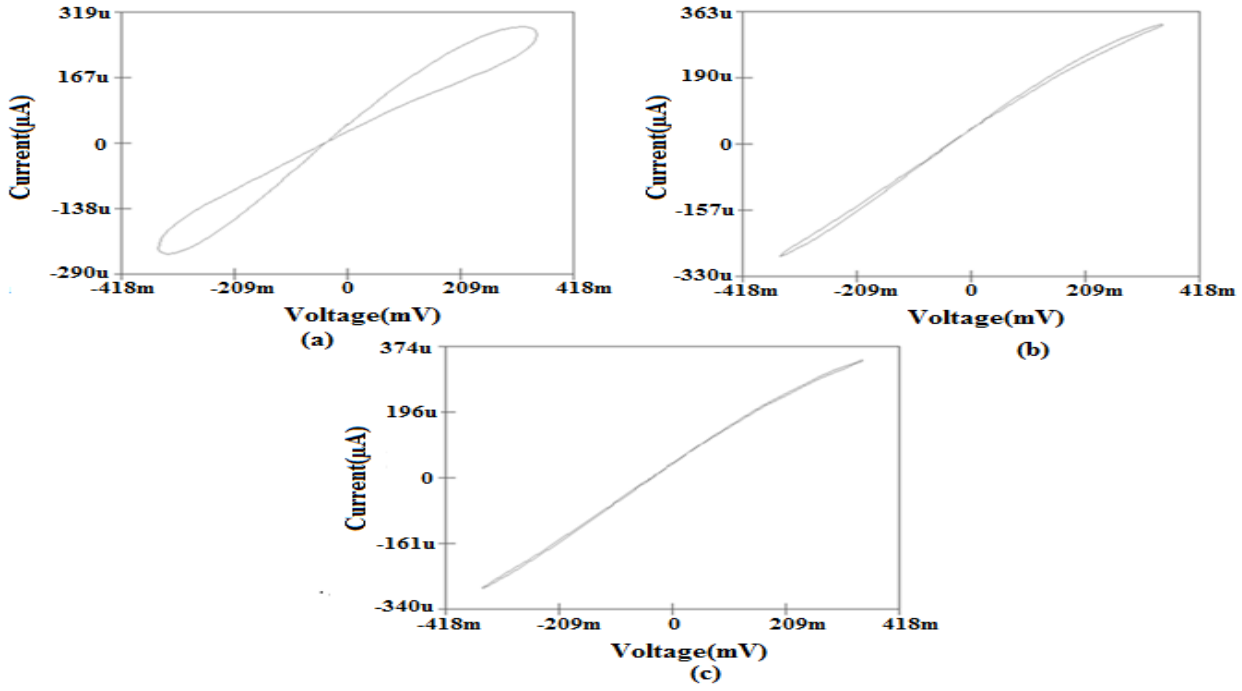


Fig.5.10 Decremental topology of proposed emulator circuit for different frequency but constant C = 5nF when I_n = 0 (a) at f = 10K (b) at f = 50K (c) at f = 100K

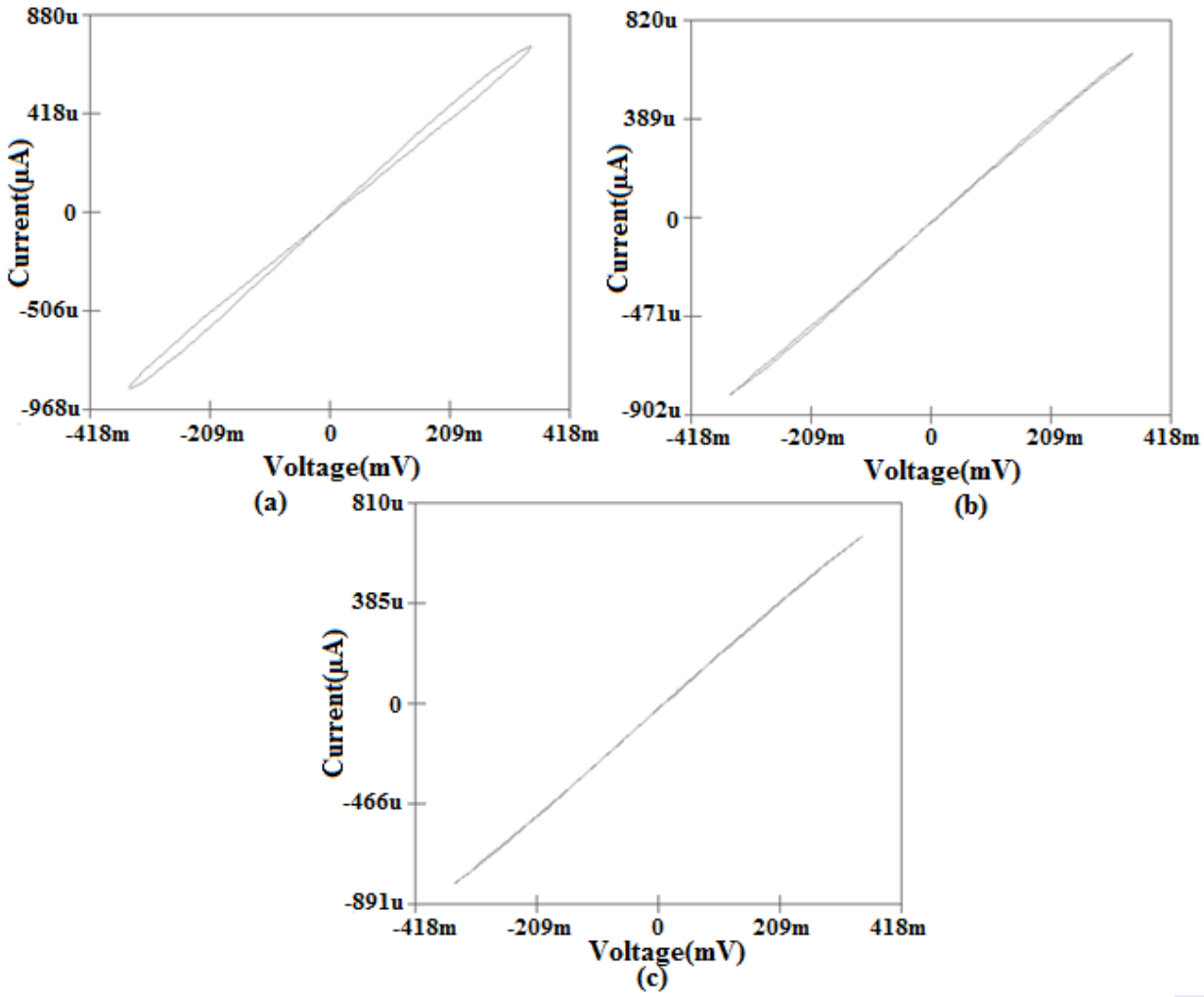


Fig.5.11 Decremental topology of proposed emulator circuit for different frequency but constant C = 5nF when I_p = 0 (a) at f = 10K (b) at f = 50K (c) at f = 100K

From fig.5.8, 5.9, 5.10 and 5.11, one can conclude that if capacitance value is kept fixed and frequency is increasing than I-V plot of memristor emulator circuit losses its nature of hysteresis. At lower frequency, I-V plot shows the hysteresis, which is required while at higher frequency width of hysteresis start to reduce and behave as linear resistor. Fig.5.8 and 5.9 shows the I-V plot for incremental topology for I_n = 0 and I_P = 0 respectively. Similarly, Fig.5.10 and 5.11 shows the I-V plot for decremental topology for I_n = 0 and I_P = 0 respectively.

From equation (5.18), it is clear that on scaling down the capacitor value, the pinched hysteresis loop behavior of both incremental and decremental topology can be pushed for higher frequency. From fig 5.12, 5.13, 5.14 and 5.15, it is clear that on increasing the capacitor value and keeping frequency constant, the width of pinched hysteresis loop start to decrease. It can be seen that for different value of capacitor 5n, 10n and 20n, the memristance will convert to linear resistance with change in capacitor value. Hence, the memristance behavior becomes that of a linear time invariant resistor on monotonically increasing the capacitor value.

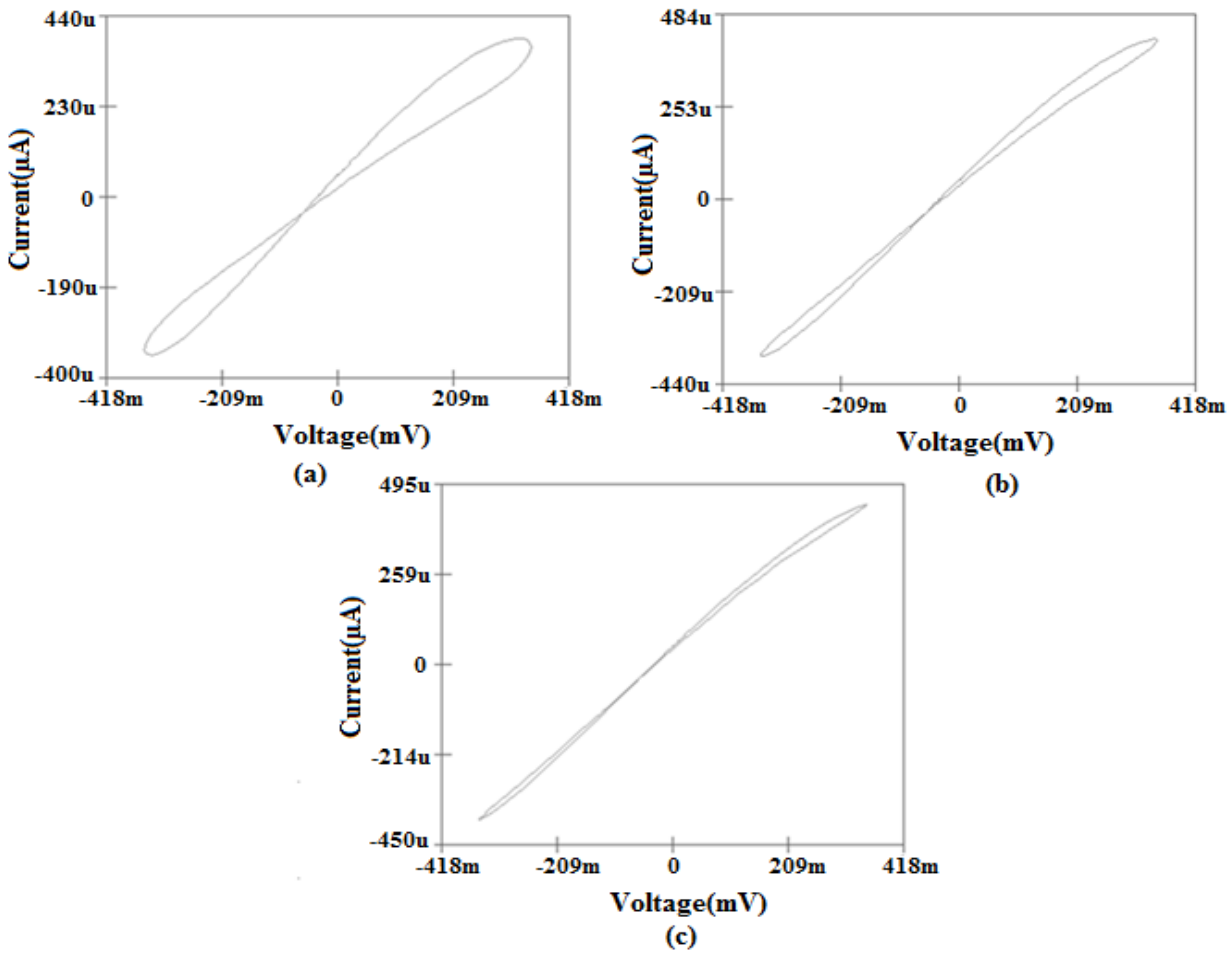


Fig.5.12 Incremental topology of proposed emulator circuit for different capacitance value but at constant f = 10K when I_n = 0 (a) at C = 5n (b) at C = 10n (c) at C = 20n

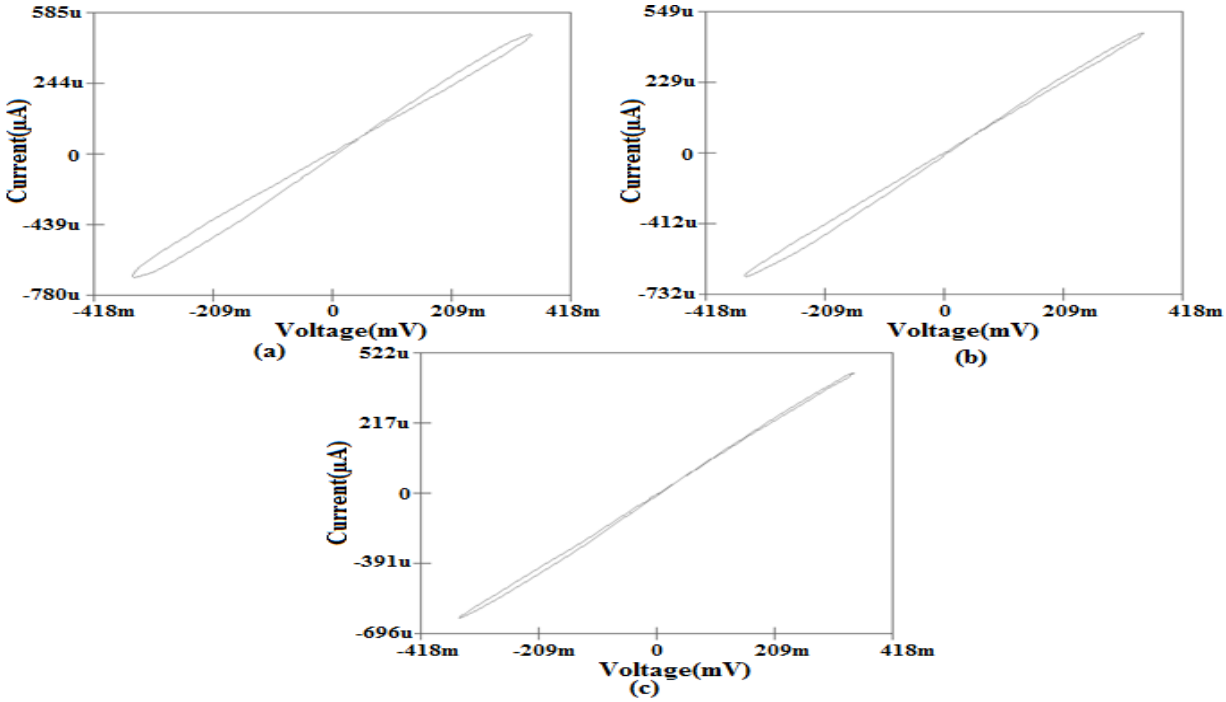


Fig.5.13 Incremental topology of proposed emulator circuit for different capacitance value but at constant f = 10K when I_p = 0 (a) at C = 5n (b) at C = 10n (c) at C = 20n

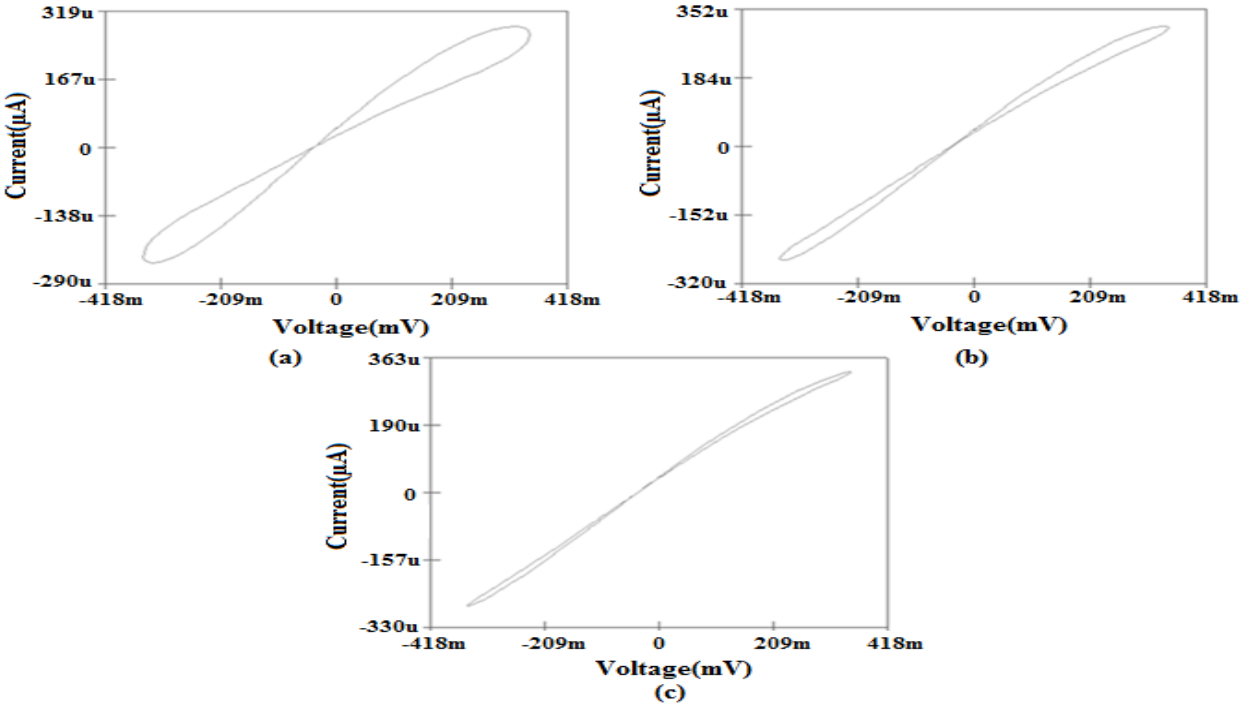


Fig.5.14 Decremental topology of proposed emulator circuit for different capacitance value but at constant f = 10K when I_n = 0 (a) at C = 5n (b) at C = 10n (c) at C = 20n

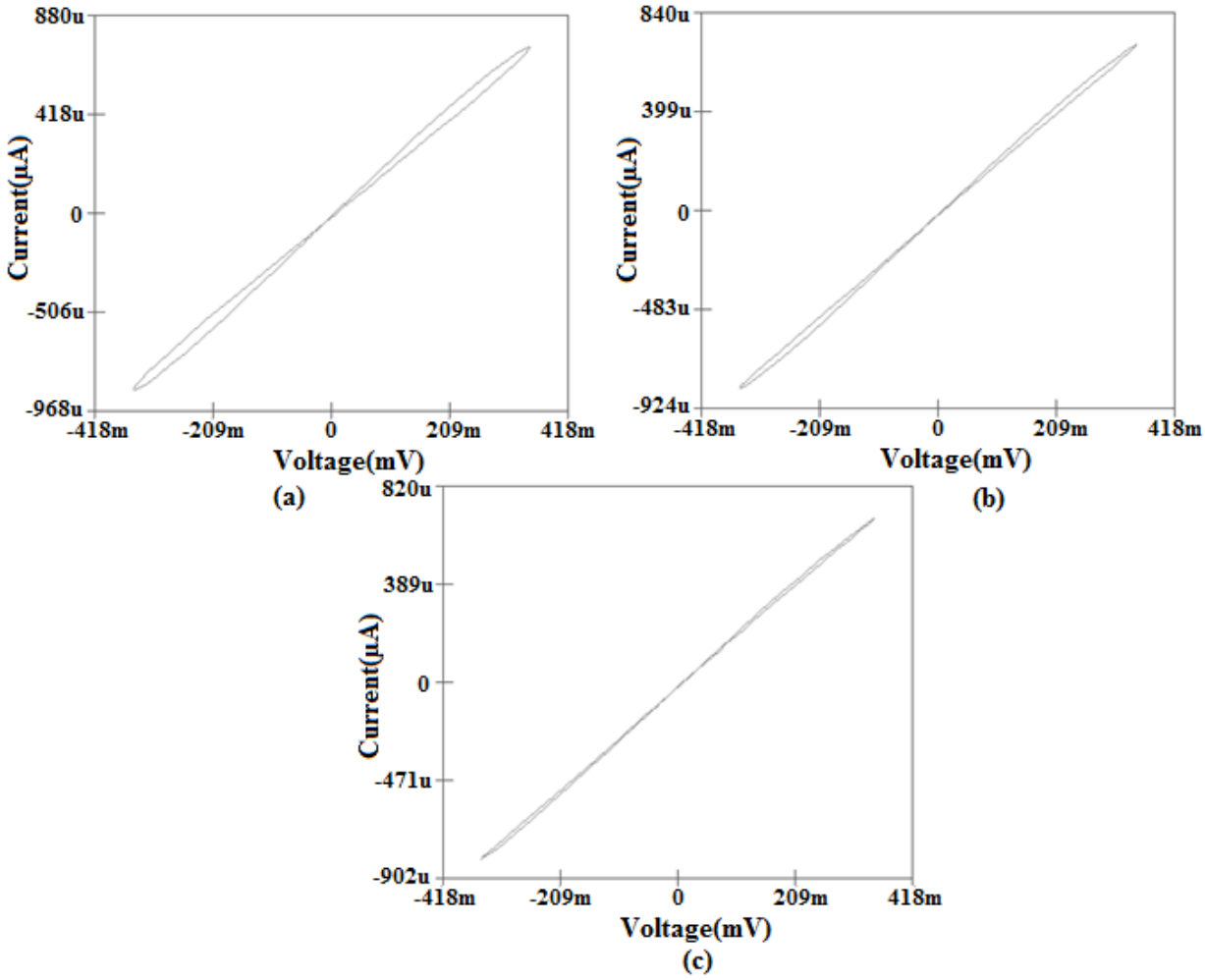


Fig.5.15 Decremental topology of proposed emulator circuit for different capacitance value but at constant f = 10K when I_p = 0 (a) at C = 5n (b) at C = 10n (c) at C = 20n

From fig.5.12, 5.13, 5.14 and 5.15, it can be concluded that if the frequency is kept at some fixed value and capacitance is kept on increasing, the I-V curve of emulator circuit will not show the hysteresis loop at higjer frequency. It will act as linear resistor at higher frequency. Fig.5.12 and 5.13 shows the I-V plot for incremental topology for I_n = 0 and I_P = 0 respectively. Similarly, Fig.5.14 and 5.15 shows the I-V plot for decremental topology for I_n = 0 and I_P = 0 respectively.

Fig.5.16, 5.17, 5.18 and 5.19 shows the pinched hysteresis loop for both incremental and decremental topologies at higher frequency f = 1MHz. At higher frequency, when capacitor value C = 0.02nF, 0.05nF and0.1nF is applied to the proposed emulator circuit, the width of hysteresis loop starts to decrease. Hence, it can be observed that at higher frequency, with increase in capacitor value, memristance starts to behave like a linear time invariant resistance.

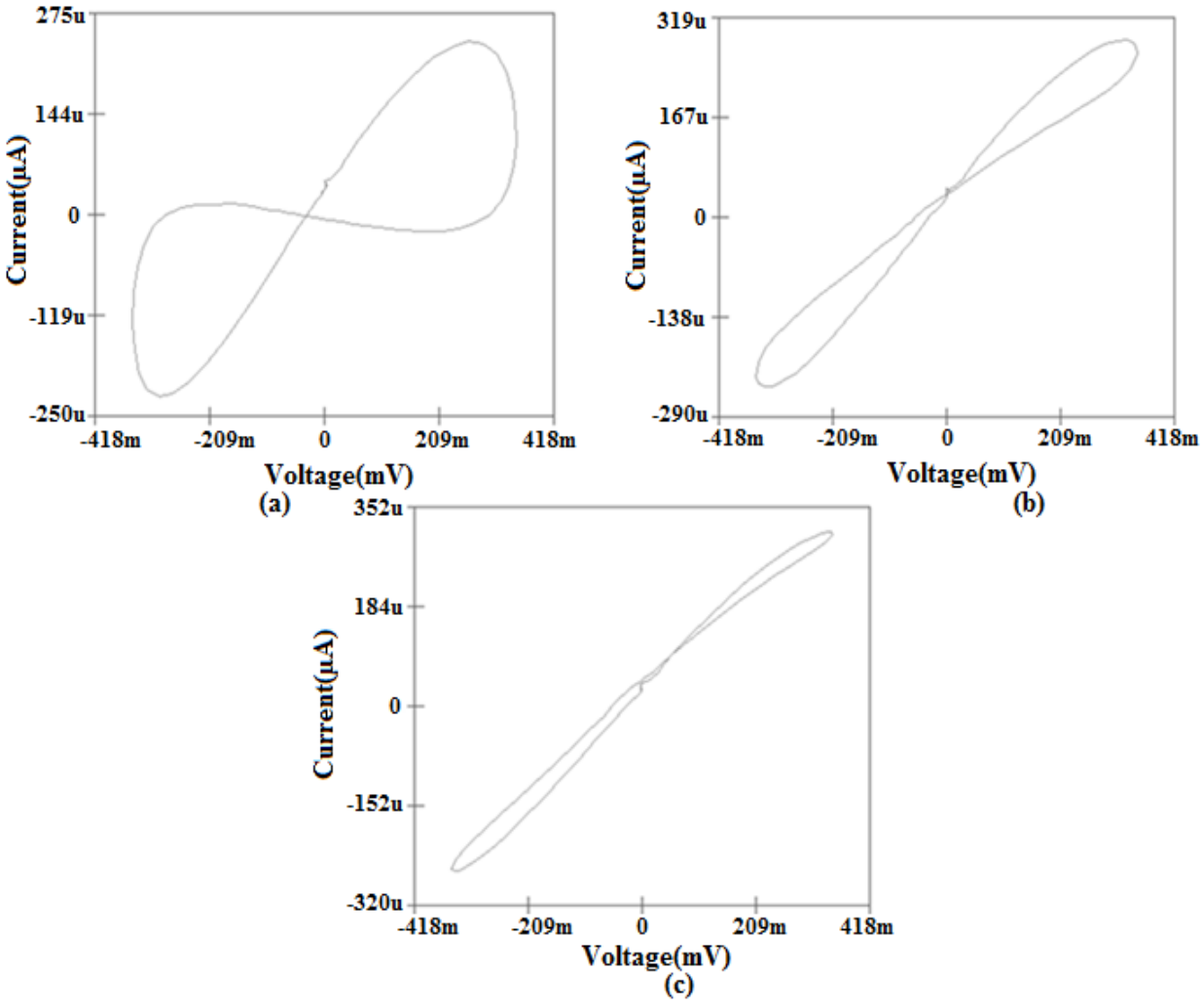


Fig.5.16 Incremental topology of proposed emulator circuit for different value of capacitor but constant f = 1MHz when I_n = 0 (a) at C = 0.02n (b) at C = 0.05n (c) at C = 0.1n

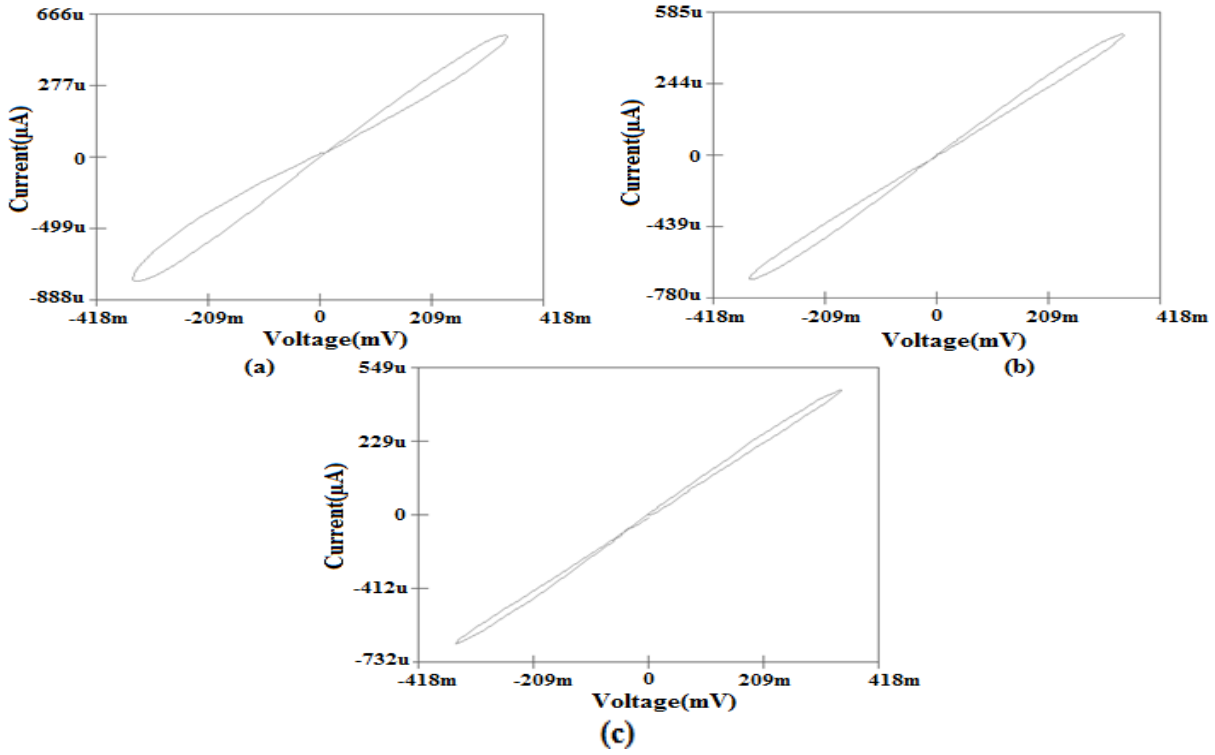


Fig.5.17 Incremental topology of proposed emulator circuit for different value of capacitor but constant f = 1MHz when I_p = 0 (a) at C = 0.02n (b) at C = 0.05n (c) at C = 0.1n

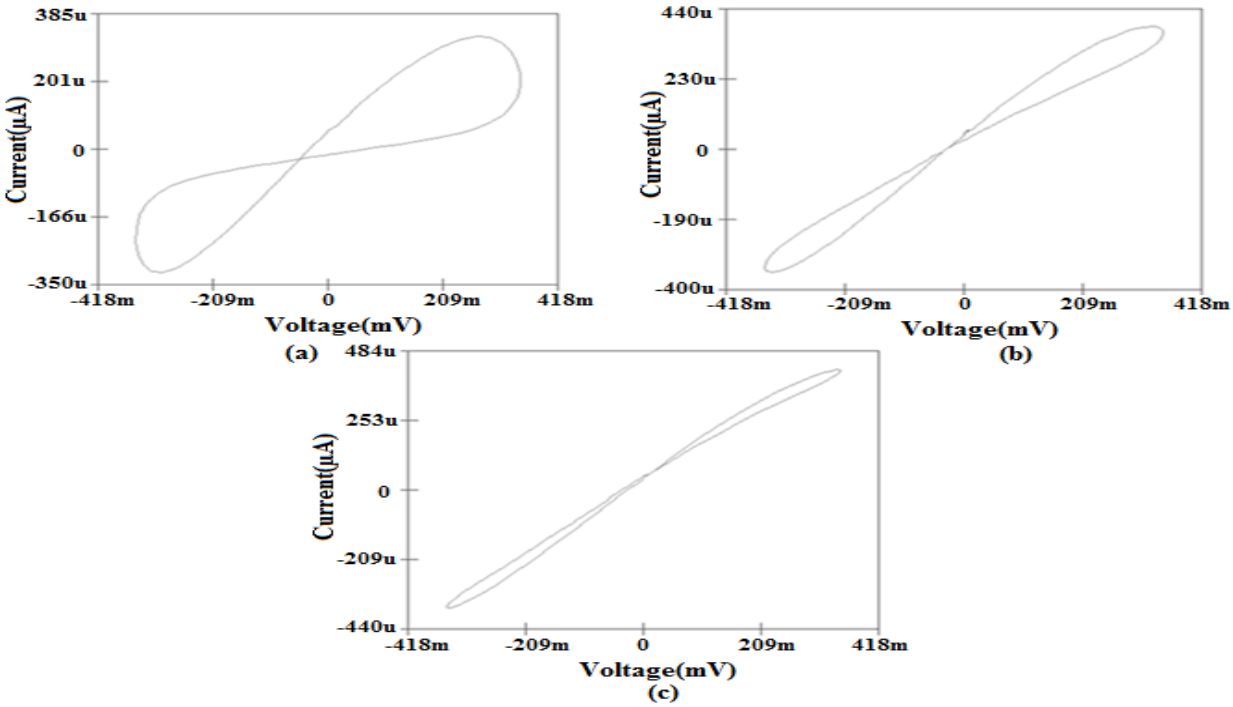


Fig.5.18 Decremental topology of proposed emulator circuit for different value of capacitor but constant f = 1MHz when I_n = 0 (a) at C = 0.02n (b) at C = 0.05n (c) at C = 0.1n

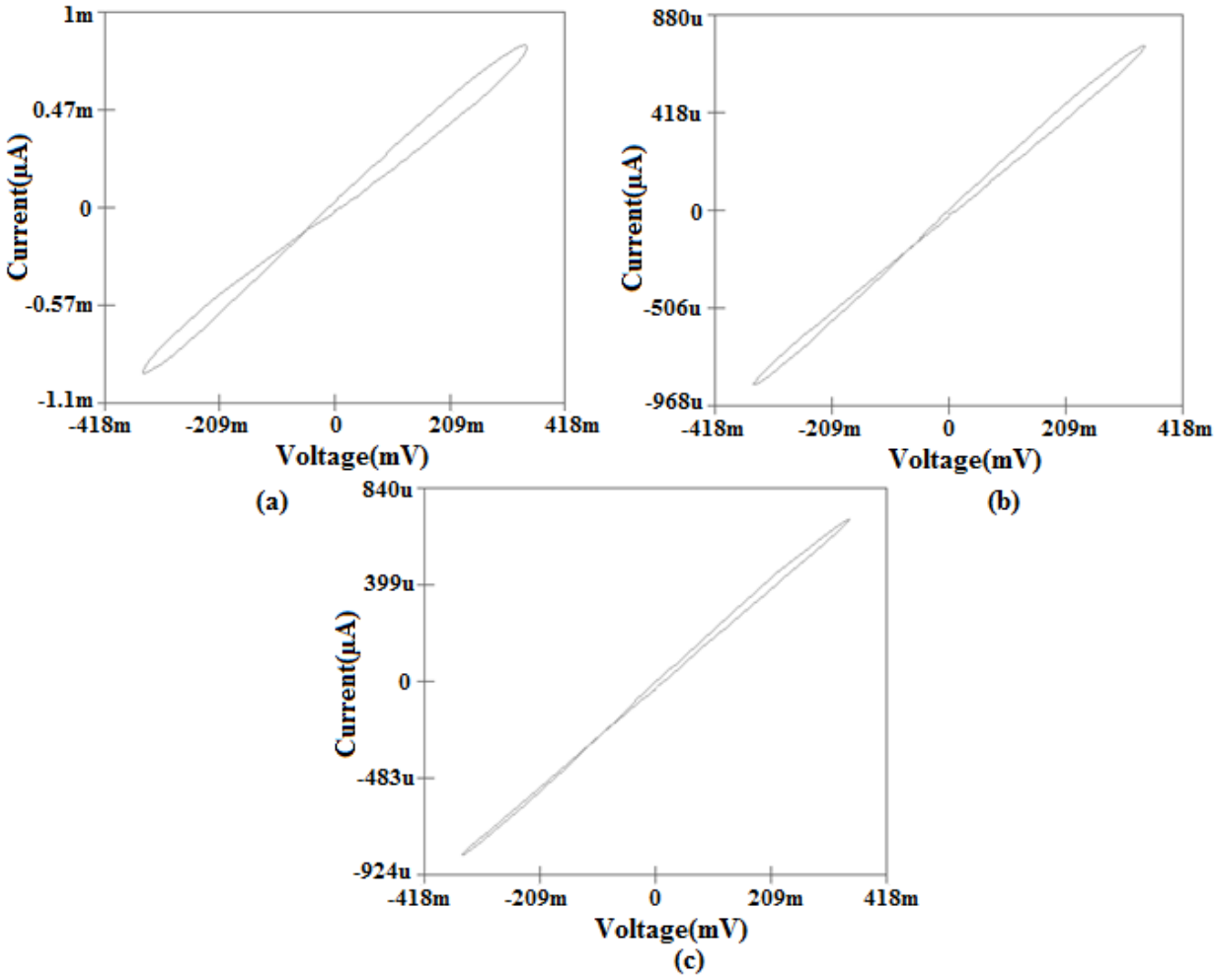


Fig.5.19 Decremental topology of proposed emulator circuit for different value of capacitor but constant f = 1MHz when I_p = 0 (a) at C = 0.02n (b) at C = 0.05n (c) at C = 0.1n

From fig.5.16, 5.17, 5.18 and 5.19, one can observe that if frequency is kept at fixed value and capacitance is kept on increasing, memristor will behave as linear resistor at higher capacitance value. Fig.5.16 and 5.17 shows the I-V plot for incremental topology for I_n = 0 and I_P = 0 respectively. Similarly, Fig.5.18 and 5.19 shows the I-V plot for decremental topology for I_n = 0 and I_P = 0 respectively.

From the fig.5.16 – 5.19, it can be observed that the proposed memristor emulator circuit can operate at higher frequency also.

In the last, it can be summarized that in this chapter proposed emulator circuit has been discussed. This emulator circuit consist of one CDTA block, two resistor and one capacitor. The properties of the proposed circuit are verified at different conditions using SYMICA DE software. And, it was also observed that the proposed emulator circuit can operate at higher frequencies as well.

CHAPTER 6

Conclusion and Future Scope

In this thesis, a new memristor emulator circuit based on CDTA has been proposed. The proposed circuit uses one CDTA block, two resistance and capacitance i.e one active component and three passive components. The advantage of this circuit is that this circuit is quite simple and does not require circuits like multiplier, ADC, DAC, AD844. Hence, the proposed circuit is not complex like other circuits discussed in literature survey. This circuit can work very well at higher frequency also.

The CDTA block used in this thesis is based on CMOS technology. It is a member of CM family. Hence, it provides the advantage of both CMOS technology and CM family. This circuit uses controlling/biasing voltage V_{con} to control the transconductance gain g_m of CDTA. By controlling g_m, the characteristics of the proposed circuit can be controlled.

The simulation results of proposed circuit with different values of frequency and capacitor has been described. With these results, it can be concluded that for higher value of frequency for constant capacitor, the width of hysteresis decreases and memristance converted into linear resistance. Similarly, for constant frequency but on increasing the capacitor value, memristance behave as linear time invariant resistance.

Memristor finds application in memories, neuromorphic cells and in various analog and digital circuits. The proposed emulator circuit can also be used in all these application. One application can be found in AM signal modulation using FM signal as input signal.

REFERENCES

1. L. O. Chua, "**Memristor- the missing circuit element**", IEEE Trans. Circuit Theory 18 (1971) 507–519.
2. L. O. Chua, S. M. Kang, "**Memristive devices and systems**", Proc. IEEE (1976) 209-223.
3. D. B. Strukov, G. S. Snider, D. R. Stewart, R. S.Williams, "**The missing memristor found**", Nature (London) 453 (2008) 80–83.
4. M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, R. S. Williams, "**Switching dynamics in titanium dioxide memristive devices**", J. Appl. Phys. 106 (2009) 106.
5. L. 0. Chua, **"Synthesis of new nonlinear network elements"**, Proc. IEEE, vol. 56, Aug. 1968, pp. 13251340.
6. **L. 0. Chua, "Introduction to Nonlinear Circuit Theory".** New York: McGraw-Hill, **1969.**
7. A. **L.** Hodgkin and A. F. Huxley, **"A quantitative description of membrane current and its application to conduction in nerve''**, J. Physiol, vol. 117, pp 500-544, 1952.
8. V. J. Francis, **"Fundamentals of Discharge Tube Circuits",** London England: Methuen, 1948.
9. S. R. Ovshinsky, **"Reversible electrical switching phenomena in disordered structures",** Phy. Rev. Lett., vol. 21, Nov. 11, 1968, pp.1450-1453.
10. H. K. Henisch, **"Amorphous-semiconductor switching"**,Sci. Amer.,Nov. 1969, pp. 30-41.

11. J. Vasla, D. Biolek, Z. Biolek, "**An Analogue model of memristor**", Int. J. Numer. Model.: Electron. Netw. Devices Fields 24 (4) (2011) 400–408.
12. G. Cserey Adam Rak, "**Macromodeling of the memristor in SPICE**", IEEE Trans. Comput.- Aided Des. Integer. Circuits Syst. 29 (2010) 632–636.
13. D. Batas, H. Fiedler, "**A memristor SPICE implementation and a new approach for magnetic flux – controlled memristor modeling"**, IEEE Trans. Nanotechnol. 10 (2) (2011) 50–255.
14. Z. Biolek, D. Biolek, V. Biolkova, "**SPICE model of memristor with nonlinear dopant drift"**, Radio Eng. 18 (2) (2009) 210–214.
15. S. Benderli, T.A. Wey, "**On SPICE macro modelling of TiO_2 memristor**", Electron. Lett. 45 (7) (2009) 377–379.
16. Y. Zhang, X. Zhang, J. Yu, "**Approximated SPICE model for memristor**", in: Proceeding of International Conference on Communications, Circuits and Systems. ICCCAS, 2009, pp. 928–931
17. A. Delgado, "**Input–Output linearization of memristive systems**", Nanotechnol. Mater. Device Conf. (2009) 154–157.
18. Y. Chen, X. Wang, "**Compact modeling and corner analysis of spintronic memristor**, Int. Symp. Nanoscale Archit. (2009) 7–12.
19. J. Chul-moon, J. Kwan-Hee, M. Kyong-Sik, "**SPICE macro models and CMOS emulator for memristors"**, J. Nanosci. Nanotechnol. 12 (2012) 1487–1491.
20. M.P. Sah, C. Yang, H. Kim, B. Muthuswamy, J. Jevtic, L. Chua, "**A generic model of memristors with parasitic components"**, IEEE Trans. Circuits Syst. I Reg. Pap. 62 (2015) 891–898.

21. C. Sanchez-Lopez, "**A 1.7 MHz Chua's circuit using VMs and CF+s**", Rev. Mex. Fis. 58 (2012) 86–93.
22. E. Ortega-Torres, C. Sanchez-Lopez, J. Mendoza-Lopez, "**Frequency Behaviour of saturated nonlinear function series based on Op Amps"**, Rev. Mex. Fis. 59 (6) (2013) 504–510.
23. E. Ortega-Torres, S. Ruiz-Hernandez, C. Sanchez-Lopez, Behavioral modeling for synthesizing N-scroll attractors, IEICE Electron Express 11 (13) (2014) 1–8.
24. Y.V. Pershin, M. Di Ventra, "**Practical approach to programmable analog circuits with memristors**", IEEE Trans. Circuits Syst.: Regul. 57 (8) (2010) 1857–1864.
25. H. Kim, M.P. Sah, C. Yang, S. Cho, L.O. Chua, "**Memristor emulator for memristor circuit applications**", IEEE Trans. Circuits Syst.- I: Regul. 59 (10) (2012) 2422–2431.
26. M.P. Sah, C. Yang, H. Kim, L.O. Chua, "**A voltage mode memristor bridge synaptic circuit with memristor emulators"**, Sensors 12 (3) (2012) 3587–3604.
27. I. Koymen, E.M. Drakakis, "**CMOS-based nano power memristor dynamics emulator**, Int. Workshops Cell Nanoscale Netw. Appl. (2014) 1–2.
28. A. Yesil, Y. Babacan, F. Kacar, "**A new DDCC based memristor emulator and its Applications"**, Microelectron. J. 45 (2014) 282–287.
29. S. Sanghak, C. Jun-Myung, C. Seongik, K.S. Min, "**Small area and compact CMOS emulator circuit for CMOS/nanoscale memristor co-design"**, Nanoscale Res. Lett. 8 (2013) 454–460.
30. X. Zhang, Y. Yu, Z. Zhang, Z. Huang, "**A simple memristor emulator**", Proc. Chin. Control Conf. (2013) 8718–8721.
31. Al Hussein, M.E. Fouda, "**A simple MOS realization of current controlled memristor Emulator"**, Int. Conf. Microelectron. (2013) 1–4.

32. X.Y. Wang, A.L. Fitch, H.H.C. Iu, W.G. Qi, "**Design of memcapacitor emulator based on memristor**, Phys. Lett. A. 376 (2012) 394–399.
33. M.T. Abuelma'atti, Z.J. Khalifa, "**A new memristor emulator and its application in digital modulation"**, Analog Integr. Circuits Signal Process. 80 (2014) 577–584.
34. A.S. Elwakil, M.E. Fouda, A.G. Radwan, "**A simple model of double loop hysteresis behavior in memristive elements"**, IEEE Trans. Circuits Syst. II Exp. Briefs. 60 (2013) 487–491.
35. Y. Dongsheng, L. Yan, H.H.C. Iu, H. Yi-Hua, "**Mutator for transferring a memristor emulator into meminductive and memcapacitive circuits"**, Chin. Phys. B 23 (7) (2014) 070702–070711.
36. Y. Dongsheng, H.H.C. Iu, A.L. Fitch, Y. Liang, "**A floating memristor emulator based relaxation oscillator"**, IEEE Trans. Circuits Syst. I. Reg. Pap. 61 (10) (2014) 2888–2896.
37. M.T. Abuelma'atti, Z.J. Khalifa, **"A continuous-level memristor emulator and its application in a multivibrator circuit"**, Int. J. Electron. Commun. 69 (2015) 771–779.
38. M.T. Abuelma' atti, Z.J. Khalifa, **"A new floating memristor emulator and its application in frequency-to-voltage conversion"**, Analog Integer Circuit Signal Process. 86 (2016) 141–147.
39. C. Sanchez-Lopez, J. Mendoza-Lopez, M.A. Carrasco-Aguilar, C. Muniz-Montero, **"A floating analog memristor emulator circuit"**, IEEE Trans. Circuits Syst. II Exp. Briefs. 61 (5) (2014) 309–313.
40. C. Sanchez-Lopez, M.A. Carrasco-Aguilar, C. Muniz-Montero, **"A 16Hz-160kHz memristor emulator circuit"**, Int. J. Electron. Commun. 69 (2015) 1208–1219.

41. Rajeev, K. R., Nishtha, R., Ratnadeep, P., Sajal, K. P., & Gaurav, K. (2017). **"Single CCTA based high frequency floating and grounded type of incremental/decremental memristor emulator and its application"**, Microelectronics Journal, 60, 119–128. https://doi.org/10.1016/j.mejo.2016.12.004.
42. Umut, E. A., Shahram, M., & Mehmet, S. (2017). **"Memristor emulator circuits using single CBTA"**, AEU¨ -International Journal of Electronics and Communications, 82, 109–118. https://doi.org/10.1016/j.aeue.2017.08.008.
43. Predrag B. Petrovic **"Floating incremental/decremental flux-controlled memristor emulator circuit based on single VDTA"**, Analog Integrated Circuits and Signal Processing, March 2018. https://doi.org/10.1007/s10470-018-1177-6
44. D. Biolek, "**CDTA-building block for current-mode analog signal processing**", in: Proceedings of the ECCTD'03, Krakow, Poland, vol. III, 2003, pp. 397–400.
45. W. Tanjaroen, T. Dumawipata, S. Unhavanich, W. Tangsrirat, W. Surakampontorn, "**Design of current differencing transconductance amplifier and its application to current-mode KHN biquad filter**", in: Proceedings of the ECTICON, 2006, pp. 497–500.
46. W. Tangsrirat, T. Dumawipata, W. Surakampontorn, "**Multiple-input single-output current-mode multifunction filter using current differencing transconductance amplifiers**", Int. J. Electron. Commun. 61 (4) (2007) 209–214.
47. J. Winai, M. Siripruchyanun, "**Current controlled current differencing transconductance amplifier (CCCDTA): a new building block and its applications**", in: Proceedings of ECTI Conference, 2006, pp. 348–351.

48. A.U. Keskin, D. Biolek, E. Hancioglu, V. Biolkova, "**Current mode KHN filter employing current differencing transconductance amplifier**", Int. J. Electron. Commun. 60 (6) (2006) 443–446.

49. W. Tangsrirat, W. Tanjaroen, and T. Pukkalanun, **"Current mode multiphase sinusoidal oscillator using CDTA-based all-pass sections,"** AEU—International Journal of Electronics and Communications, vol. 63, no. 7, pp. 616–622, 2009.

50. W. Jaikla and M. Siripruchyanan, **"A Versatile Quadrature Oscillator and Universal Biquad Filter Using Dual-Output Current Controlled Current Differencing Transconductance Amplifier"**, International Symposium on Communications and Information Technologies, 2006, DOI: 10.1109/ISCIT.2006.339942