6T SRAM HIGH DENSITY BIT-CELL ANALYSIS FOR 1PPM FAILURE RATE TARGETTING TEMPERATURE (-40,165)

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Submitted by

ANUKRITI SINGH
2K16/SPD/03

Department of Electronics & Communication Engineering

Delhi Technological University, Delhi-110042

DECLARATION

I hereby declare that the dissertation entitled "**6T SRAM HIGH DENSITY BIT-CELL ANALYSIS FOR 1PPM FAILURE RATE TARGETTING TEMPERATURE (-40,165)**" submitted by Anukriti Singh for the degree of Master of Technology in Electronics and Communication Engineering is carried out by me under the guidance and supervision of **Dr. Rajesh Rohilla** at Delhi Technological University, Delhi and **Dr. Anuj Grover** at STMicroelectronics, Greater Noida during the period: Aug, 2017 to June, 2018.

I further declare that the matter embodied in this report has not been submitted for the award of any other degree or diploma.

Date: … July, 2018

Anukriti Singh

2K16/SPD/03

Certified that the above statement made by the student is correct to the best of our knowledge and belief.

Dr. Rajesh Rohilla

Professor

Electronics & Comm. Engg. Department

Delhi Technological University

Dr. Anuj Grover

Principal Engineer

STMicroelectronics Pvt. Ltd.

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2K16/SPD/03

ABSTRACT

Embedded memories occupies up to 70% of systems on a chip area. In SOC's applications embedded SRAM's are often used in order to achieve higher robustness. The main purpose or functionality is to ensure that content of the bitcell are not altered during read operation and bit-cell data could be quickly modified during the write operation. To provide stable read & stable write operation in the SRAM cell, specific conditions are needed to be satisfied. In order to achieve higher robustness there is a need of innovation in the area of SRAM design by scaling SRAM along with CMOS technology. This would help in reducing the variability & increasing the stability while designing the larger SRAM cell.

The stability of SRAM bitcell depends on the Static Noise Margin (SNM), Write Margin (WM), and Write time (WT), Dynamic Noise Margin (DNM), ION, ILEAK etc. In this paper we analyzed SRAM read margin, SRAM write margin on the basis of Static Noise Margin Analysis, Dynamic Noise Margin Analysis & Write Margin Analysis. We present the measured result of modified 6T SRAM cell on 28nm bulk CMOS technology. We calculate the safe design space for SRAM overall allowed voltages, temperature & processes.

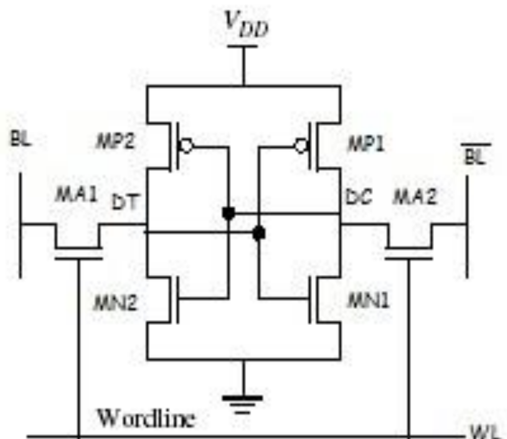
The need of Innovation in the area of SRAM design has been given by scaling the SRAM (Static Random Access Memory) along with CMOS technology in different processors and system-on-chip products rapidly. This would help us in reducing the variability and increasing the stability while designing the larger SRAM cell.

However, it is nearly impossible to guarantee the first silicon success in this advanced technology era. In fact more in high density devices like SRAMs, device variations are common. This is because of continuous scaling down of length, width & threshold voltages of the transistor devices.

In order to increase the stability of the memory cell and achieve a robust read or write operation, multiple assist schemes and design strategies are used. But variations occurring in the devices are

random in nature which degrades the device performance also make it very tedious job to achieve silicon success.

This report presents the complete analysis of the high density bitcell by simulating it using ELDO (Mentor Graphics tool) for all device parameters via sizing of transistors and setting the initial conditions. In this work, we conducted a.comprehensive analysis for detecting the memory cells which exhibits weak Static Noise Margin (SNM), write margin and write time identified by the factors causing these cells to exhibit weak properties. For verification of these methodologies in SRAM, a single port high density STM bitcell was considered in 28nm technology.



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CHAPTER 1

Introduction

ANUKRITI SINGH
Delhi Technological University

1.1 Introduction

Today,the driving factors in the development of efficient and high density static random acce ss memory (SRAMs) memories were the influencial force for the greater development in CMOS techno which was observed in the past few decades. In earlier days first 1Kb Dynamic Random access memory chip was designed & this was done by Intel in 70's nowadays Dynamic Random Access Memories having 1GB capacity or more.The concept of memory virtually inbuilt inside the computers has given the hierarchical flow for different memory which ranged from lower memory capacity, slow but affordable.

The reflection of this flow of memories and its types is on increasing speed & cost per bit on moving to register level from secondary storage.The knowledge of memory flow helped in maintaining the RAM abstraction and limiting its cost & consumption of power.

The increasing difference b/w the Micro Processor Unit (MPU) cycle time and Dynamic Random Access Memory access time compelled for the intro of multiple level of caching in modern data processors. As the difference in speed between Micro Processor Unit, mass storage and memory continued to strengthen, depth in memory hierarchy were defined for high end-server microprocessor. Observing the amount of cache memory, ITRS distinguish the Cost-Performance Micro Processor Unit which needs to be optimize for greater performance, & also the lower marketing cost by reducing the Static Random access memory i.e. cache memory embedded on-chip and the higher performance Micro Processor Unit optimize to get greater system performance by involving a single or multiple Central processing Units cores, and on latest stat's, the on-chip Static Random access memory cache. Logically functional & Static Random access memory cache memory capacity mostly double every techno in every generation by doubling the number of on-chip Central processing units core and memory

There are so many methods to increase the Silicon on chip cache memory size which is to get use of high density dynamic Random access Memory. The embedded dynamic random access memories on Silicon on Chip implemented in the logic flow that can be benefitted by fast LVT transistor.Although, the inherently high sub threshold leakage current complicate implementation of a one Transistor Dynamic Random access Memory cell. Exchnaging one Transistor Dynamic Random access Memory cell with Dynamic Random access Memory cell design having a large no of devices resulted in some area loss & underlined the memory cell size area benefit that embedded Dynamic Random access Memory's usually having over embedded Static Random access memory. Embedded Static Random access memor's have been used for accelerating the performance of higher end MicroProcessor,Switches & NetworkRouterss. The regular fast logic processes were used that done require masking step.

As per the Moore's law , he stated that after every 18 month there will be double the increament in the on chip functionality.This is due to the fact that the transistor size will be reduced by a noticeable factor.The capability of economically manufacturing of chip based on newer technology will determine the advancement.As per the rule, Static Random access memory cell size still continued to scale 0.5 times per generation additionally motivated by the greater need for higher performance rate processor.

1.2 Motivation

Embedded Memory occupies major part of SOC i.e. up to 70%. To target and achieve higher stability and robust memory device embedded memory are often used in SOC application. SRAM cell performance and yield gets limited because of device variations in advanced technology. With the changing technology era, to guarantee stable device on silicon in an IC is nearly impossible. Furthermore in high density devices like SRAMs device variability are very prone to come into picture. This is because of the continuous decrease in device size and also lowering of voltages. This scaling affect the length, width and threshold voltage of the

device transistor. It becomes very tedious job to achieve silicon success if the variation occurring in the devices are random.

Random variation is due to number & location of dopant present inside the channel. This degrades device's performance. It is therefore the growing need after design process, to validate the silicon to detect and fix bugs in the IC. Thus, for research post-silicon validation is becoming an emerging topic for major innovations in electronics design automation.

Also, VLSI industry requires 1ppm qualification of SRAM bitcell to achieve higher yield. The yield of different capacities of SRAM array is calculated for different sigma qualified by designing some statistical model for memory with 28nm FDSOI SMOS techno. This yield or failure rate is to be achieved to fulfill the need of higher density demand for the advanced chip model design.

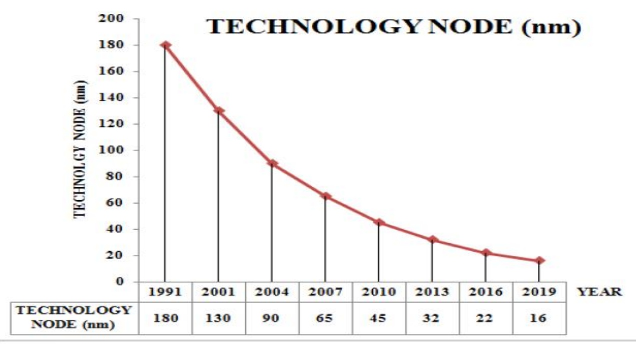


Figure 1.2 : Technology Trend

1.3 Objective of the work

In this work, a comprehensive analysis is conducted for detecting the memory cell stability by calculating static noise margin (SNM), write time, write margin and factors causing device to exhibit weak properties.

My target is to qualify 1ppm failure rate for a high density bitcell at different temperature -40 and 165 for a particular memory capacity. For this there is a requirement to first understand what 1ppm failure rate is. So, my activity began with the study of failure rates. Then I targeted the parameters which are needed to be calculated in order to retain bitcell activity.

In order to achieve the target I varied the beta ratio of the cell and did the simulations of almost 12 cases. By this I tried to analyze the results and look for the best among all.

In the task I finalized 2 cases to be taken into consideration and compared it with the original size of bitcell. This was done by looking into the percentage change between every case with the original one.

After this analysis, I used another tool where Eldo is being interfaced with the MATLAB to qualify the maximum memory capacity with the target keeping in mind of 1ppm. This was done in order to ensure the result achieved by fast fail probability and Monte Carlo simulation.

CHAPTER 2

Technology Introduction

2.1 An overview of FD-SOI technology

The hearts of each digital devices are the Semiconductor Chip that provided the intelligence and power to drive the device. Each chip is made-up of the billions of transistors, the building blocks of digital words. To build better digital devices and enhance the user experience the size of the transistor must be reduced, while increasing performance and reducing the power consumption.

Conventional BULK Technology was the leading and well mature technology with high performance. But as the transistor shrinks, the length of the gate is reduced the control of the gate exercises over the channel region is also reduced which results in lowering the transistor performance. Some unwanted leakage currents flows even when the transistor off and many more problems get introduced like latch up, parasitics across the junction etc. In order to minimize these problems; while continuing to deliver high performance bulk silicon transistors are become more complex adding additional level of manufacturing complexity in an ever increasing technology node (Graphical view for this is shown in Figure 2.1. In technology smaller than 28nm found new solution to reduce complexity was the prime concern.

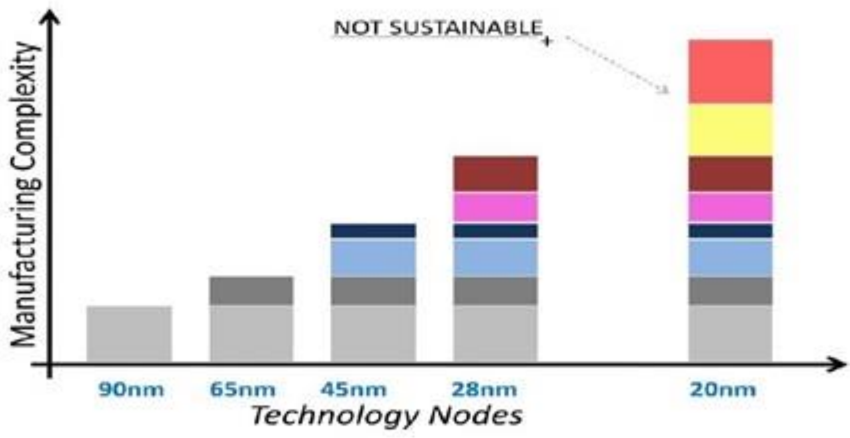


Fig 2.1: Bulk Technology Manufacturing Complexities

SOI innovation is a way which gives us these advantages (performance, improvement, reduction in power and area) while simplifying the manufacturing procedure. Contrasting to few different technology Silicon on Insulator doesn't change basic architecture of transistor.

2.1.1 Silicon on Insulator:

SOI, which show that silicon device, is created over an insulating material, for example, silicon dioxide (additionally known as *Buried Oxide Layer BOX*).The impact of insulation material found in power and speed improvement as decreasing in junction capacitance since junction is isolated from BULK substrate.

The SOI substrate aids in improving performance, reducing power and area and saving for ICs by the use of device architecture and substrate design for the advantages at the IC level. Silicon on Insulator is four terminal device Drain,Source, Gate and the Substrate.The width of the silicon channel tells whether the SOI is fully depleted or partially depleted.

Partially depleted SOI (PDSOI)

The silicon width film is thick that is not used in channel formation then the device is called partially depleted. Partially depleted SOI makes the use of doped channel with silicon film at the top of the thickness of 50 to 90nm while the thickness of insulating layer (BOX) is around 100 to 200nm.

Fully depleted SOI (FDSOI)

The silicon film width used for channel formation is thin therefore, device is known as fully depleted SOI. FDSOI makes use of lightly doped or un-doped channel. The thickness of top silicon film is about 5 to 20nm and for insulating layer is around 5 to 50nm

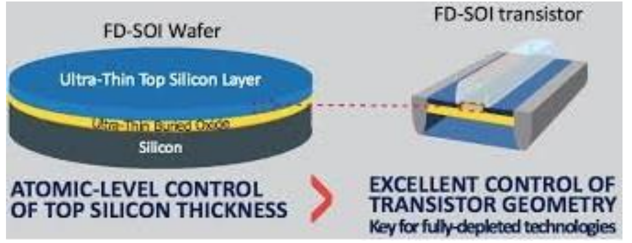


Figure 2.2: FDSOI Transistor

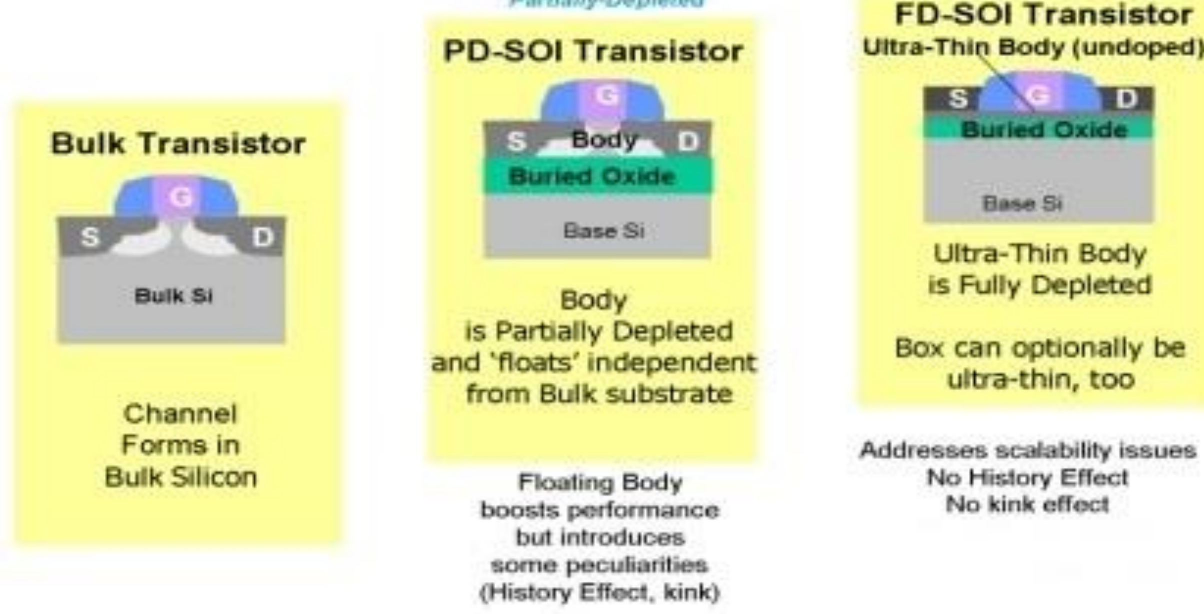


Figure 2.3: BULK, PD-SOI and FD-SOI transistor formation

2.1.2 Advantages of FDSOI over BULK Technology:

Vertical isolation and Excellent lateral of active transistors from substrate.

- Reduction in the leakages and removal of Latch Up in CMOS architechture.
- Elimination of effective interference & cross talk b/w transistors at mixed signal IC's.
- Lessen the soft error present in SRAM from radiation effects of EHP generations.
- Various voltages range can be used for different transistors without any add in processing steps required for triple wells.
- Greater speed device operation in terms of speed and power due to reduction in parasitic capacitances.
- Initially because of reduction in source & drain junction's capacitance, but also from metal to substrate capacitance & gate to substrate capacitance.
- Reduction in power consumption due to lower supply voltage available on device & lower capacitance due to parasitics.

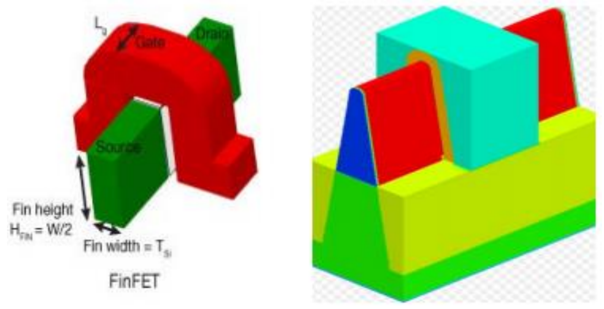
- Greater features/ die area or reduced die area/function ; Silicon on Insulator allow higher integration density meaning tight layout design rules, Performance improvement equivalent to next technology node without scaling.
- Potential to simplify device fabrication steps.

2.1.3 Technology comparison : PDSOI vs FDSOI Technology

- Fully Depleted device operates at faster rate due to the sharp sub threshold slopes, & lower threshold Voltages that benefitted for greater speed in switching of the MOS devices.All these devices also have improved drive current at relative low voltage.
- Many design feature used for designing PullDown transistors can be extracted from Bulk-silicon-devices & used in the SiliconOnInsulator environment with some modest change. This made ckt redesigning for the PullDown transistors easier than for FD Microckt.
- Fully depleted SiliconOnInsulator devices have reduced power requirements ,high gain in ckt speed & high level of soft error-immunity.

FINFET vs FDSOI Technology

3D FINFET is having Ulta low power feature better for Internet of things application whereas FDSOI is having better device performance and greater power efficiency.This advantage of FDSOI has mitigated the process variability and suppressed leakages a lot. Thus in memories leakages are major constraints.So we used FDSOI technology.



Fin (shaped) Field Effect Transistor

CHAPTER 3

Introduction to Memories

ANUKRITI SINGH
Delhi Technological University

3.1 Introduction

The ideal knowledge about holding data in the device can be initialized to provide the quality Eg. Greater Speed and performance ,Lower power consumption,Lowering the cost,greater density occupied,random access priviledge, non-volatile behavior, easy testing & reliability. Before 1970, memory devices were made on magnetic core techno where digital data bits were holded in magnetic wire wound coils. This kind of technology for information storage was having limitations in terms of cost, performance, reliability, area, power and speed. Introduction to memory on the basis of semiconductor device with the small size was the initializaion of a new generation in memory technlogy. Those semiconductor memory were also offered by continuous improvement in termed as speed & reliability by making use of very small-small device.

In today generation of *System on Chip*, majority of components are handled on a single-chip involving the memory. Memories are very important part of the SoC design because they occupy approximately seventy percent of total area of the chip. Semiconductor memories are the electronic circuits which store digital information in large amount, hence are important modules in modern integrated circuits. The increasing demand for low price memory at lower power consumption, higher density ,higher speed operation, & smaller packages sizes This has triggered the fabrication techno and memory designing methodology toward more optimized designing rule and therefore towards high data holding density. Memories manufactured in ST Microelectronics are broadly classified into three categories namely, Read Only Memory (ROM), Single Port Static Random Access Memory (SPSRAM) & Dual Port Static Random Access Memory

3.2 Classification of Semiconductor Memories

The Semiconductor memories are diversified in terms of type of data storage and access.

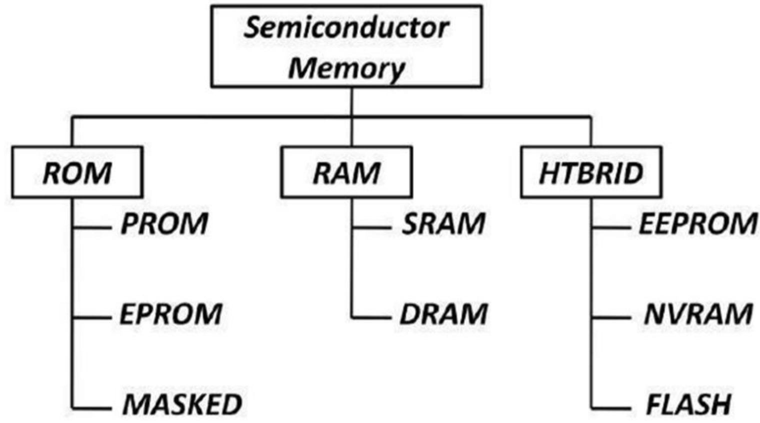


Figure 3.1: Semiconductor Memory categorization

- **ROM (Read Only Memory)**

ROM is permanent memory, doesn't require refresh operation. Even power supply is off the data is not lost. On the basis of programming of new data into the ROM as well the Number of time it can be rewritten, it is distinguished into the following types. Classification shows the generation of ROM device from hardwored to programmable and erasable programmable. Following are the three main categories:

a) PROM (Programmable ROM):

Data can be electrically written after the chip is fabricated. Through applying electrically charged from the input pin of the chip data is written into the ROM (one word at a time).PROM well called as one-time-programmable "(OTP)" since once the data is written in above mentioned way has its content that can never be changed.

b) EPROM (Erasable and Programmable ROM):

Code is programme in EPROM is similar way as in ProgrammableReadOnlyMemory. Although, data written in EPROM's can be easily erased & reprogrammed accordingly. The device is exposed to be a stronger sources of UV light to erase the data. A window is available in the upmost section of the device & this window is provided which allows UV light to reach the silicon.) Initial unprogrammed state of the entire EPROM chip can be achieved by applying the above method.

c) MASKED ROM: A photo mask is used to write the data during chip fabrication. Before chip production the contents to be written into ROM has been specified, so the transistors inside the chip can be arranged according to actual data. Well known as hard wired memories. Low production cost is the major advantage of the masked rom. unfortunately; low cost comes into consideration when mass production of same ROM required.

- **RAM (Random Access Memory)**

RAM is well known as read/write memories. The memory array of RAM provides modification and retrieval of data bits which are stored in memory cell. Any memory bitcell could be access in approximately equal access time, it means read and write cycle nearly same. The data stored is volatile in nature i.e. if the power (operating voltage) supply is switched off the information is lost. RAM can be classified into two main categories.

a) DRAM (Dynamic Random-Access Memory):

In DRAM each data bit is stored in separate capacitor. The capacitor is charged or discharged represent two states, two valued of a single bit data, usually known as high & low. Charge stored in capacitor is refreshed periodically since charge leaks in capacitor due to this information stored get fade. Because of requirement of refresh mechanism, it is a dynamic memory. DRAM requires one transistor and one capacitor to store one bit of information. This is what make its structure simple and allow DRAM to attain high densities. Billions of transistors and capacitors can be fabricated into single memory chip.

b) SRAM (Static Random Access Memory):

In SRAM data can retain till the power is supplied to memory chip. No need to periodically refresh the data for retention as required in flash memory and DRAM. Random access name suggest that data can be retrieve and modify from any SRAM array cell in any order, accessing of new memory cell doesn‘t depend upon the last accessed cell. SRAM attain low

densities since 6Transistors is required to store single bit data.The access time of SRAM is extremely fast but more are costly to manufacture. SRAM memories are used for applications where higher speed makes prime importance.

- **HYBRID**

As memory technology has matured in recent years, the line between RAM and ROM has blurred. Hybrid memories can be read and written as desired, like RAM, but maintain their contents without electrical power, just like ROM. Two of the hybrid devices, EEPROM and flash, are descendants of ROM devices. The third hybrid, NVRAM, is a modified version of SRAM.

a) **EEPROM:** Inner design are quite same as EPReadOnlyMemory, but the erasing operation is completed electrically, not by exposure to UV light. The initial trade off for theses improvement in functions is high cost and longer writes cycle than RAM.

b) **FLASH RAM:** Flash memory device dense, with lower cost, nonvolatile nature, faster operation & electricall reprogrammable. These advantage are beneficial &, as of direct results, its usage has increased dynamically in embedded systems.

c) **NVRAM:** A NonVolatileRAM is usually just as Static Random Access Memory with a power backup. When power turns on, the NonVolatileRAM operates like Static Random Access Memory.When power turns off, the NonVolatileRAM draws enough power from the backup to hold the data.

3.3 SRAM Cell Description

The basic Static Random Access Memory cell depicted by 2 crossly coupled inverter and 2 PassGate transistor, commonly called as the 6T memcell. The 6 transistor static memory cell in *CMOS* techno is used in majority of the designs, today. The crossly coupled inverter, M1 , M5 & M2 , M6, act as storing element. Designers point of view is always directed for

reducing the area of cell and ,lowering power consumption of that million of cell that can be embedded on single chip. The PassGate transistor are routed to the wordline at the gate terminal, and the bitline at the source or drain terminal.

The bitlines are used to perform certain operations as in read and write operation on cell where as word lines are used to select the cell. Basically, the bitcell stores value on one side and its complement on other (Q and Q' as shown in figure 3.2). The 2 complementary bitline are used to improve noise rejection properties & speed. The steadystate power lexploitation of the bitcell is governed by subthreshold leakage current, so in memory circuits larger threshold voltage are few used.

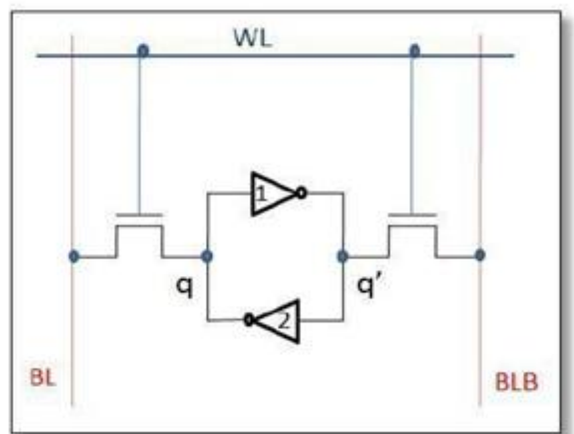


Figure 3.2 Static Memcell

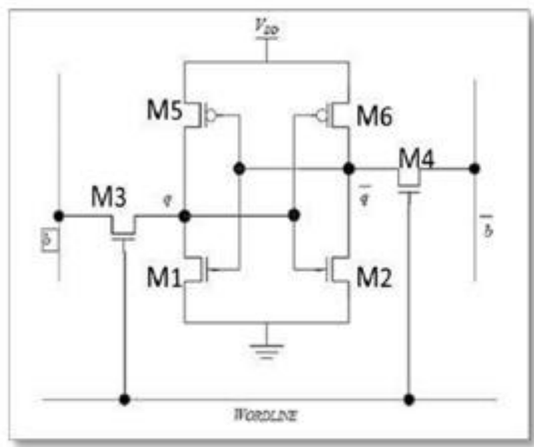


Figure 3.3 6Transistor Memcell

3.4 Voltage Transfer Characteristics

The read and write operations for cell design consideration is conveyed by Voltage Transfer Characteristics (VTC). Two stable states represent the stored value in the VTC of the cross coupled inverters. Till the switching threshold crossed in particular node, it retains its current state. While when the threshold crossed the cell flips current internal state. Therefore, at the time of a read operation, current state won‘t be disturbed, in contrast at the time of write operation internal voltage is forced to alter past vs to change the state.

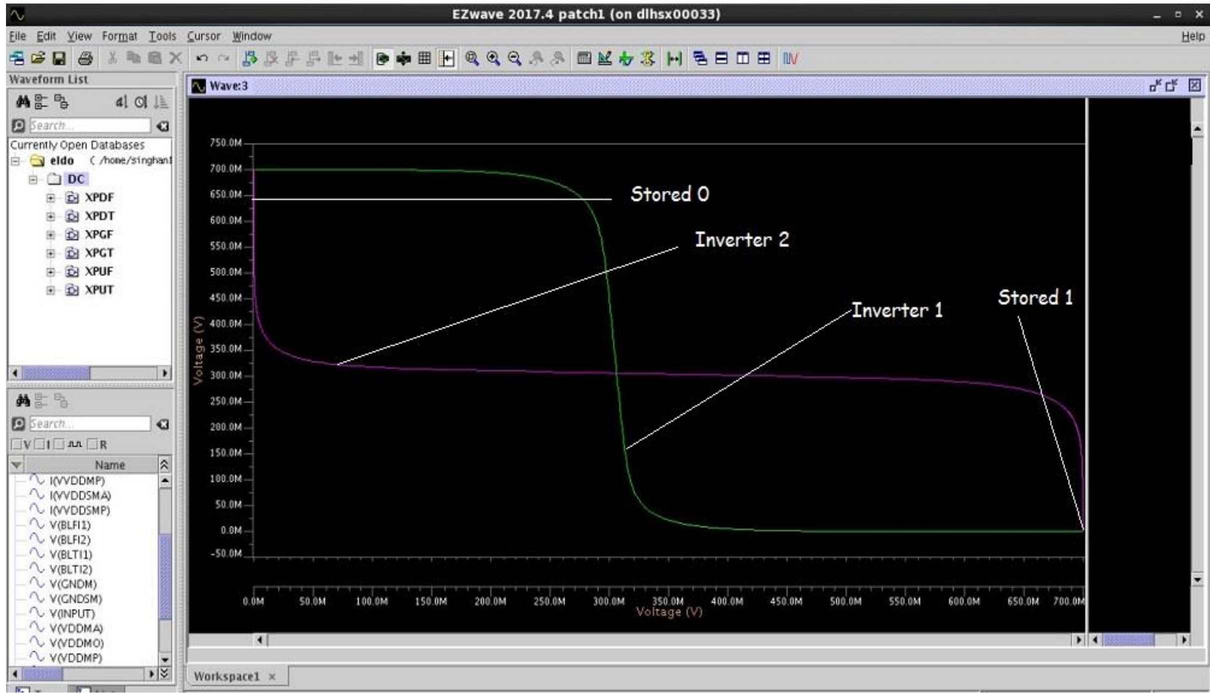


Figure 3.4: Voltage transfer characteristics

3.5 Operational Modes of 6T SRAM

In our memory we have three modes of operation i.e. read mode, write mode and standby mode. Among these three modes we have two modes where we want our bitcell to retain the data and they are read mode & standby mode. In write mode we indeed want the data to be flipped. Data holding of Static Random Access Memory cell, both during read operation & standby mode is an important function in modern technology node. The bitcell become bit unstable with lower VDD,increasing leakages (current) & increasing variability all concluded from lowering gate length.

A. Standby Mode

The wordline (WL) is given lower voltage supply & both BL and $\overline{BL}$ which are bitlines are made away from internal nodes during the Standby operation mode. The word –line is not asserted, so MA1 and MA2 which connects to the bit-lines are turned off .In this mode bit-cell cannot be accessed. Thus, as long as 2 crossly coupled inverter are connected to the supply voltages they feedback each other that are formed by MN1 and MN2.In this mode of operation the latch itself is responsible to hold data.

B. Read Operation

In read mode, all precharge signal is made “1” & thus our bit line BL and $\overline{BL}$ will be left floating at VDD.As soon as WL is made “1” the access transistors goes ON. Since BL=1 and DT=0 i.e. there is potential difference across MOSs, therefore BL discharges to zero through MN2.

If our memory qualifies for retaining data in read mode then it will definitely qualify for retaining data in standby mode & it is this retaining capability of the bitcell we measure as SNM.Thus, we only talk about stability in Read mode.

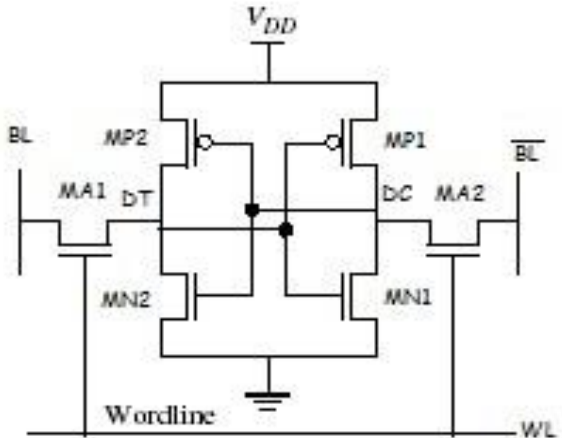


Figure 3.5: 6T SRAM Bitcell

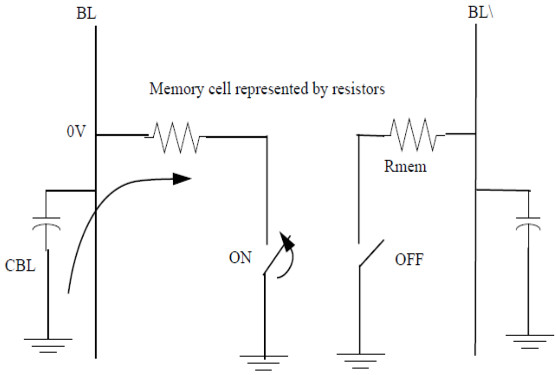


Figure 3.6: Read Operation

C. Write Operation

In write mode, initially if “0” is stored at DT and “1” is stored at DC then corresponding to voltage sources of CMOS SRAM cell, the transistors MN1 & MP2 are turned off, while MP1 and MN2 are operating in linear mode. Thus the internal node voltage DT= “0” and DC= “1” before the access transistors are turned on. Before starting the operation we off the Precharge signal and thus bit line, BL and $\overline{BL}$ will be left floating at VDD.Then, WL is made “1”, which turns on MA1 & MA2. Let data applied be “1”then $\overline{BL}$ is forcefully discharged which in turn discharges node DC. Thus, DC is made “0”.With DC= “0” MP2 goes ON and MN2 goes OFF.DT is pulled up to VDD by MP2. Thus, DT= “1” and DC= “0”and hence data “1” is written in the bitcell with DT= “1”.

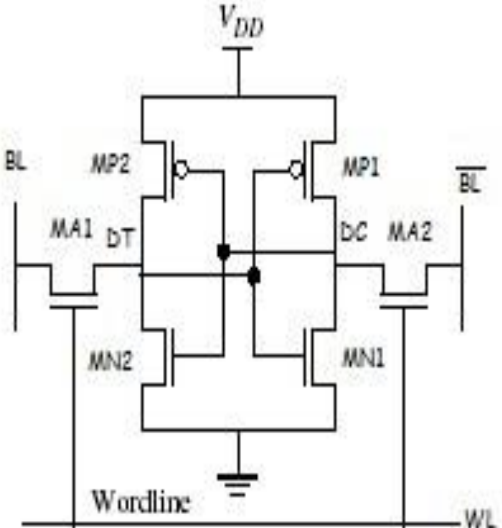


Figure 3.7: 6T SRAM bitcell to understand Read Operation

The transistor pair M6,M4 are involved for the better writing operation to take place in the design of memory cell.They form pseudo nmos inverter during write operation .Two devices allow current to flow which lowers the note volatage from Supply voltage Vdd.The pulling node is responsible for the design of sizing of device to switch through the regeneration action.

3.6 Memory Organization

Random-access architecture is the memory organization for many memory. The name _random access *'is derived from the fact that all the memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing"*. Simple cell circuits are arranged in vertical column(bit lines) and horizontal rows(word lines) to share some connection for storage array or core.

Zero (0) or one (1) can be stored in a memory cell. Data stored in a cell can be responsible or reading or writing by row selecting according word line and column selecting according bit line. Address decoder determines the selection of rows and columns by its decoded binary address data. General memory organization is shown in figure 2.9.

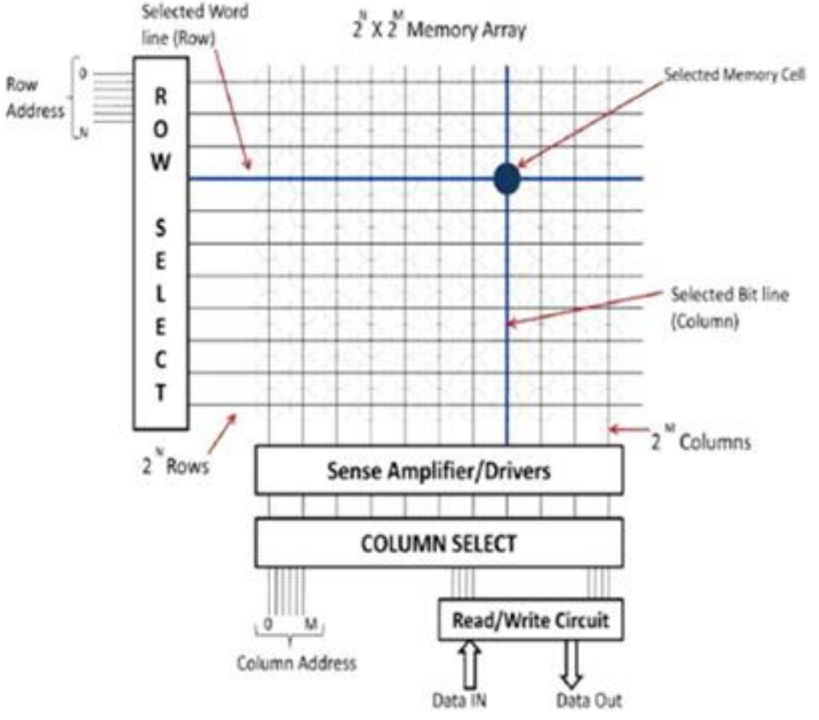


Figure 3.8: Memory Organization

The whole memory block can be divided in 3 major parts as mentioned below:

Memory Arrays: Every individual memcells are kept in such as trend of an array of vertical column and horizontal row in a memory array.One common connection in same column i.e.WordLine and another common connection in same row i.e. RowLine is being made by

each cell.There are 2M columns known as bit line & 2N rows known as word line in 2N×2M memory capacity.Every memcell are capable of storing bits of information.

Row & column decoder: If there is 2N×2M size of memory array, then there will be 2N word lines to address each row and 2M bit lines to access each column. Now to use the specific memcell, according to bit line and word line has enabled. To accomplish this task, N to 2N row decoder and M to 2M column decoder are used which will have N bits of row address and M bits of column address as inputs respectively.

Sense amplifier: As there are lots of devices connected to the bit lines, the capacitive load of bit line is very high. For reading of the memcell, if we allow to discharge the bit lines completely which were pre charged well before the reading operation, it takes too much time to discharge and again to pre charge due to high capacitance. This will limit the speed of the memory. We need to use some mechanism by which the pre charged bit lines can be discharged very fast. This mechanism is called sense amplifier. Its function is to detect the stored data from the selected memcell.

3.7 Different Types of SRAM Architectures

A. Basic Architecture

The dissipation increases whenever the WordLine is set to high because every cell in the row are activated whichever gets connected to the WordLine in previously used architecture.Word line access time & bit line access time are found as important factor for read access in basic Architechture. The cell density increases as we increase the sizes of Static Random Access Memory cell & because of higher WordLine Cap value the WordLine delay gets increases.The above issues needs to be taken care and this can be improved different type of archuitechtures for reducing WordLine cap value and BitLine cap value.

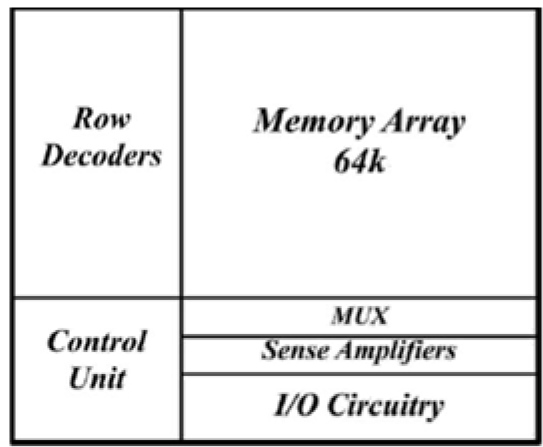


Figure 3.9: Memory Architecture

B. Split Core Architecture

The problem with the basic architecture of memory is that when the memory size is increasing, the load of the word lines in terms of the resistance and capacitance also increases. The increased load will then reduce the speed of the operation of the memory as the worst case memcell which is located at the last part of the word line will violate the timing constraints.

We can control the delay if we can lessen the capacitive loading and Resistive Loading on WordLine and hence more capacity of memory can be practically possible in single memory cut.

A method is proposed to divide the core in 2 part & use the similar WordLine driver in the center to drive the common word line which is running to both the core as shown in figure 2.8. The word lines are driven from the center that is rowdec. Therefore, unlike the case of single core each path will encounter half of capacitive and half of resistive loading among the 2 path which are coming from driver

In this type of architecture, reduction is performed by splitting the memory array in smaller blocks. Reduction in the RC delay is observed because of the split bank, but the activation of a word line activates the entire cell in both of the core areas. So certainly, there is need of a different architecture, which could also provide some advantage in terms of power dissipation.

Figure 3.10: Optimized Memory Architecture

C. Bank Architecture

An improvement in BitLine Cap value & WordLine Cap value can be seen in the Banking Architecture.Here the Input/Output & Control section were separated & because of this number of memory BitCell which were activated degraded at major extent.This is the major contribution of this type of architecture.

There was significant decrease in the value of power cionsumption as discussed earlier.The only disadvantage of this of archtecture is the memory built is lesser dense because area occupied is more.Figure (2.9) showing the block diagram of bank type architecture.

Figure 3.11: Bank Architecture

Redundancy Feature

Redundancy feature is an optional feature added in the memory architecture. This feature is like an on chip repair mechanism. There are two redundant rows provided as shown in Figure with only consecutive row correctability. In case memcells of any row fails, that particular row will be replaced by redundant row.

Figure 3.12: Redundancy Feature

3.8 SRAM Characteristics

3.8.1 High Speed Operation of SRAM

With the improving technology,to extend the increasing edges of design in VLSI system is continued for larger memory storage capacity and efficient memory density.The achievement for faster systems , memories has beeen always BottleNecked for years.For today memory designers needs to keep in mind that to wisen the memory speed they need to think abiout important matching of main memory with the processor speed.Static Random Access Memory has moved into the above area to fasten the lower density Mos transistors.

During read Operation the delay of access path can be classified into 3 parts:

- Maximum Delay from the clock implimentation to activation of WordLine
- Maximum time required from the activation of WordLine inorder to sense the activity of SenseAMP &
- Maximum Time required from the SenseAmp on for data availability @Output

The tradeoff is always b/w speed of memory & density required for array.For this the two parameters are very importent : Access Time for Memory & Time required to store or retrieve the data in specific data bit.The time required to access the memory is very important variable for the PPA(Power | Performance | Area) for the memory BitCell.In order to increase read operation speed ,few Analog Amps can make the effective use.The small diff is fastly translated into logic categories instead the BitLine didn't arrived their final volatges.

3.8.2 A High Density in SRAM

All the other circuits except the memory core are redundant if talk about user point of view.Therefore in order to get higher density BitCell there is a requirement of smaller logics of Control section, RowDec ,ColumnDec as well as Input/Output Buffer.Technology used also govers the density of a Memory BitCell.Every Technology has there own area requirement for designing perspective & they descrive the minimum area required.The available types are 6Transistor SRAM ,8Transistor SRAM, Single port as well as Dual port etc.

Uses of small MemoryCells are effective rather than reducing the number of peripheries.As there effects are lesser instead of former one.So, to get density we need to do trade off with the speed of the cell.For better featured Memory there should maintainance of balance betwen the two i.e density as well as speed.

The change in techno starting from 180nmm,130nm,90nm,65nm,45nm ,28nm,22nm,14nm, 10nm, 7nm etc has altogether played a major role in Semiconductor industry in terms of Sizing ,densities as well as compactness of memory bitcell.This has significantly braught changes in densities & areas of BitCells.Also the periphery circuitaries are also affected.There is also gain in Speed increament of the memory Cells also.

3.8.3 Low Power Approaches in SRAM

This presents the latest development in low power circuit techniques and methods for static Random access memories. The key techniques in power reduction in both Active and standby modes are: capacitance reduction by using divided word line structure, selective recharging scheme, pulse word line, ac Current reduction by multistage decoding, operating voltage reduction coupled with low power sensing with sense amplifier.

3.9 Memory Compilers

Different compilers exist based on primary parameters like bits, words, mux and other parameter like bank, redundancy etc. A different combination of these parameters corresponds to different cuts (memory instance) created, based on different combination of parameters. According to their requirements, customers choose memory instance.

Memory compiler uses leaf cells and connectivity information which are predefined building blocks to compile the user-specified cut ssize. The output of compiler will be behavioral level model , layout, schematic symbols & a layout qualification to route & place .

Figure 3.13 Function of Memory Compiler

CHAPTER 4

BITCELL ANALYSIS

4.1 6T SRAM Introduction

A fully static RAM cell is a bistable circuit, capable of being driven into one of two states. After removing the driving stimulus, the circuit retains its state. Thus we say the cell is **"static"** since it does not need to have its data refreshed as long as the dc power is applied. SRAM memory cells are based on the **latch structure** with two back-to-back connected Inverters & two pass transistors. There are two kinds of SRAM memory cells- the 6T cell & the 4T cell. The Basic 6T SRAM looks like:

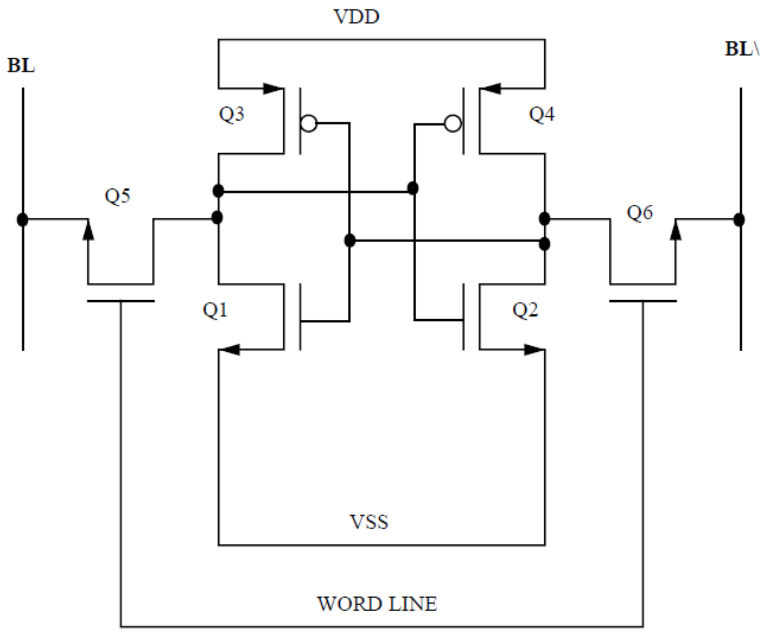


Figure 4.1: 6T SRAM cell

This reduces the power requirements of the cell, except for small leakage current, no power will be dissipated during the time then cell retains the stored logic value. Good static noise margin & stability. Stability is held when VDD is scaled down. The disadvantage of CMOS technology is that it requires more processing steps because of the presence of NMOS & PMOS transistor & requires large area. The changing techno has altogether played a major role in Semiconductor industry in terms of Sizing ,densities as well as compactness of memory bitcell.

4.2 Operational Modes of 6T SRAM

In our memory we have three modes of operation i.e. read mode, write mode and standby mode. Among these three modes we have two modes where we want our bitcell to retain the data and they are read mode & standby mode. In write mode we indeed want the data to be flipped. Data retention of SRAM cell, both in standby mode and during a read access is an important functional constraint in advanced technology nodes. The cell become less stable with lower supply voltage (VDD),increasing Leakage currents & increasing variability all resulting from technology scaling.

4.2.1 Standby Mode

In standby mode, the word line (WL) is set on lower voltage supply & both the internal nodes are isolated from bit lines (BL and $\overline{BL}$) .

4.2.2 Read Operation

Assume that a 1 is stored at DC. We further assume that both bit lines are pre-charged to high before the read operation get started. The read cycle is started by enabling the word line, asserting both the pass transistors MA1 and MA2 after the initial word line delay. During the correct read operation, the values stored in DT & DC are transferred to the bit-line by leaving BL at its Pre_charged value & discharging $\overline{BL}$ through MN2_MA1. A calculative sizing of the transistors is necessary to avoid accidently writing a 1 into the cell. This type of function is frequently called a read_upset .The bitline capacitance for large rmemories is in the pF range. Apparently, the value of $\overline{BL}$ stays at the Pre_charged value VDD upon enabling of the read operation (WL→1). This series combination of the two NMOS's pulls down the $\overline{BL}$ towards the ground .For a small_sized cell, we would like to have these transistor sized as close to minimum as possible, which would result in a very slow discharge of the large bitline capacitance. As the difference between BL

and $\overline{BL}$ builds up, the sense amplifier is activated to accelerate the reading process. Initially, upon the rise of the WL, the intermediate node between these two NMOS transistors , DT is pulled up towards the Pre_charged value of $\overline{BL}$ .This voltage rise of DT must stay low enough not to cause a substantial current through the MN1-MP1 inverter, which in the worst case could flip the data originally stored.It is ultimately precautious to keep the resistance of the transistor MA1 larger than that of MN2 to prevent this flipping of data.

The boundary constraints on the device sizes can be derived by solving the current equation at the maximum allowed values of the voltage ripple ΔV. We ignore the body effect on the transistor MA1 for simplicity and we write

$$\mathbf{\beta n, MA1}\{(\mathbf{VDD} - \mathbf{VQB} - \mathbf{VTn})\mathbf{VDsatn} - \frac{\boldsymbol{VDsatn^2}}{\mathbf{2}}\}$$

$$= \mathbf{\beta n, MA2}\{(\mathbf{VDD} - \mathbf{VTn})\mathbf{VQB} - \frac{\boldsymbol{VQB^2}}{\mathbf{2}}\}$$

which simplifies to

$$\boldsymbol{\Delta V} = \frac{\boldsymbol{VDsatn + CR(VDD - VTn) - \sqrt{VDsatn^2(1 + CR) + CR^2(VDD - VTn)^2}}}{\boldsymbol{CR}}$$

Where, CR is called the cell ratio and is defined as

$$CR = \frac{Wmn2/Lmn2}{Wma1/Lma1}$$

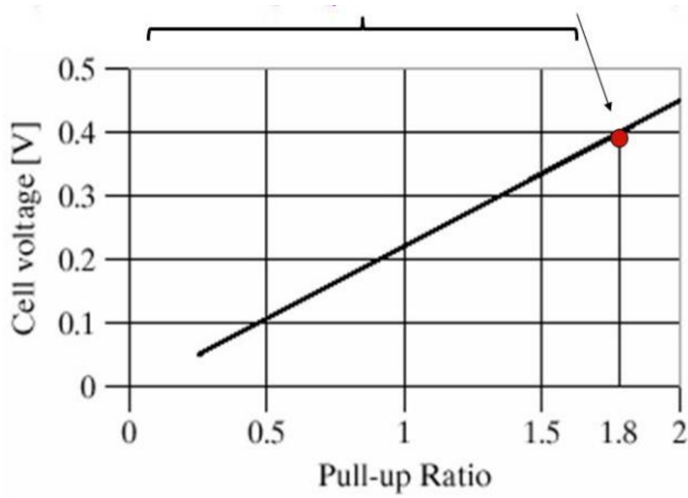


Figure 4.2 Pull-up ratio vs Cell Voltage

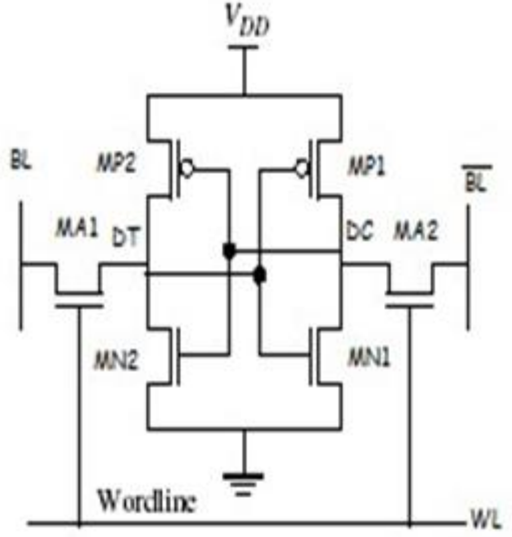


Figure 4.3 Memory Bitcell

In read mode, all precharge signal is made "1" & thus our bit line BL and $\overline{BL}$ will be left floating at VDD.As soon as WL is made "1" the access transistors goes ON. Since BL=1 and DT=0 i.e. there is potential difference across MOSs, therefore BL discharges to zero through MN2.

If our memory qualifies for retaining data in read mode then it will definitely qualify for retaining data in standby mode & it is this retaining capability of the bitcell we measure as SNM.Thus, we only talk about stability in Read mode.

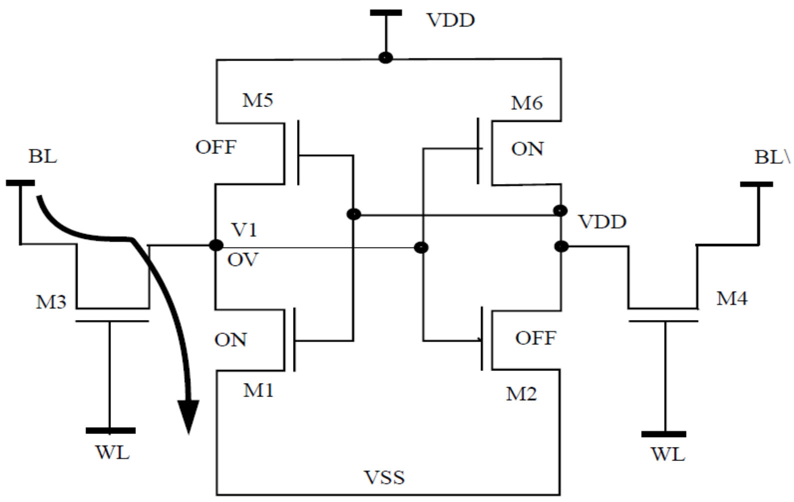


Figure 4.4(a): Write Operation depiction in bit-cell

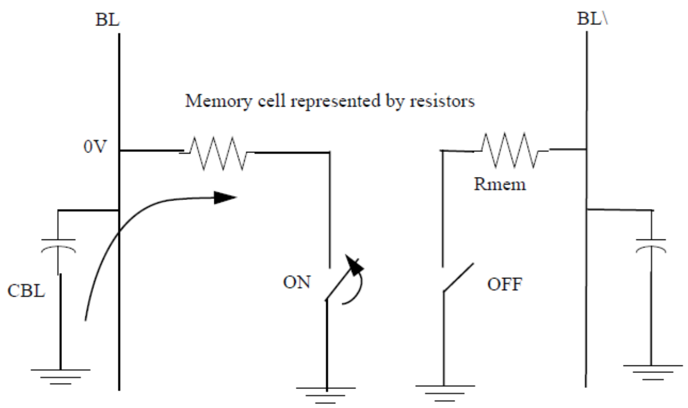


Figure 4.4(b): Write Operation depiction in bit-cell

4.2.3 Write Operation

In write mode, initially if "0" is stored at DT and "1" is stored at DC then corresponding to voltage sources of CMOS SRAM cell, the transistors MN1 & MP2 are turned off, while MP1 and MN2 are operating in linear mode. Thus the internal node voltage DT= "0" & DC= "1" before the access transistors are turned on. Before starting the operation we off the Precharge signal and thus bit line, BL and $\overline{BL}$ will be left floating at VDD.Then, WL is made "1", which turns on MA1 & MA2. Let data applied be "1"then $\overline{BL}$ is forcefully discharged which in turn discharges node DC. Thus, DC is made "0".With DC= "0" MP2

goes ON and MN2 goes OFF.DT is pulled up to VDD by MP2. Thus, DT= “1” and DC= “0”and hence data “1” is written in the bitcell with DT= “1”.

4.3 Stability Parameters

4.3.1 Static Noise Margin

If our memory qualifies for retaining data in read mode then it will definitely qualify for retaining data in standby mode and it is this retaining capability of a bitcell we measure as Static Noise Margin (SNM) .

Static Noise Margin is defined as maximum static spurious noise that the bitcell can tolerate while still maintaining a reliable operation The value of Noise Source where the voltage on the internal nodes of the latch becomes equal is SNM. It is basically the minimum amount of voltage that a bitcell can tolerate at its nodes DT and DC so as not to flip the data, when it is in read mode. Or it may also be defined as the measure of mismatch between both half of the bitcell .It is the measure of the stability of the bitcell in read mode.

It is also termed as *“Read Disturbance margin”*. It is caused due to process mismatch among the MOSs. It determines the readability of a bitcell, higher the SNM higher the retaining capability of the bitcell and vice versa. Bitcell will be efficiently retain the data if the SNM is better. SNM should be high (10% of VDD by some industry standard) so as to make the circuit more immune to noise i.e. mismatches.

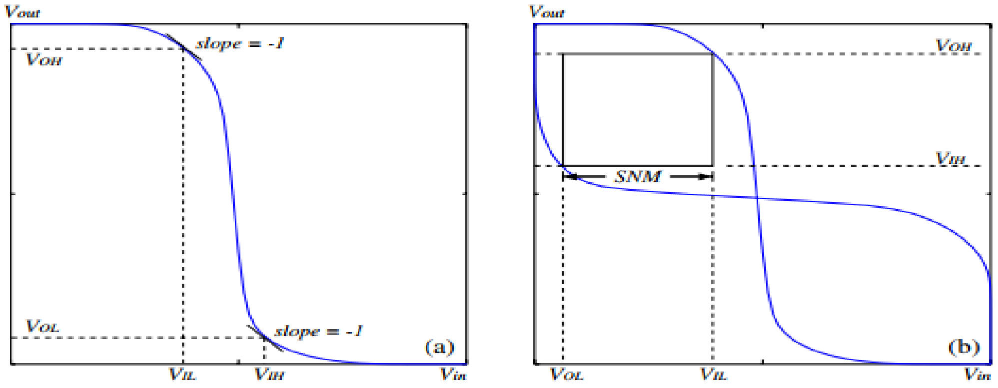


Figure 4.5(a): Static Noise Margin Operation and simulation results

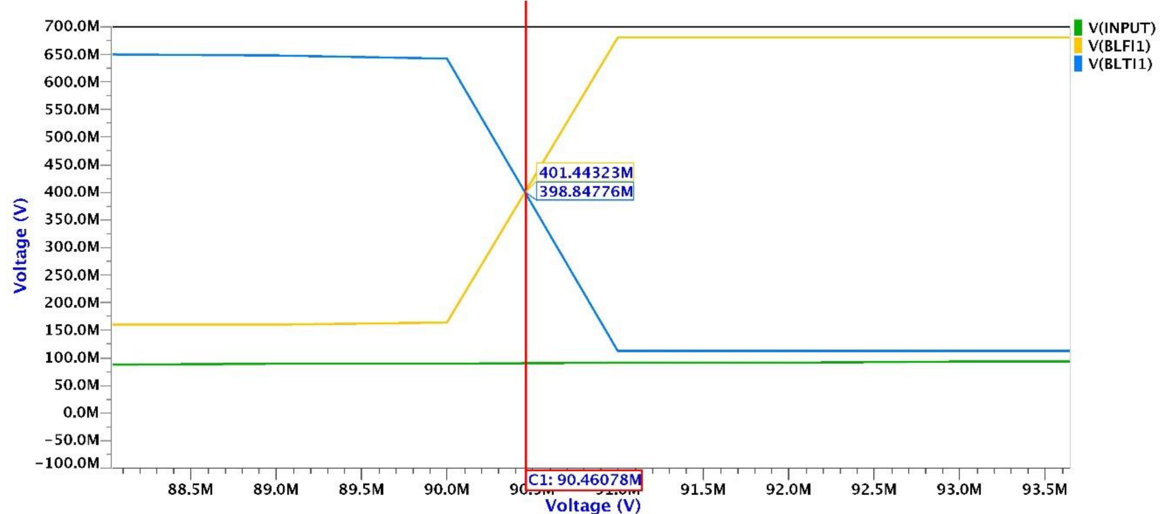


Figure 4.5(b): Static Noise Margin Operation and simulation results

4.3.2 Write Margin

Write Margin is defined as the measure of minimum voltage of BL/$\overline{BL}$ at which the data flips. It determines the writability of a bitcell i.e. how much favorable the bitcell is for write operation. It is also known as *Write-trip Point* .Device sizing may play a major role in calculating the write margin of a bitcell. Besides the read stability of a bitcell, write stability is equally important to be analyzed.

This is done in order to guarantee the writability of the cell without spending too much energy in pulling down the bit line voltage to 0V.

As $\overline{BL}$ will be pulled down, DC will discharge to zero & DT will charged up to VDD. If we increase the strength of MA1 w.r.t. MN2, then due to some charge accumulation at node DT, due to difference in strength, potential will start building up at DT.Thus, if we increase strength of MA1, our writing will be favored.

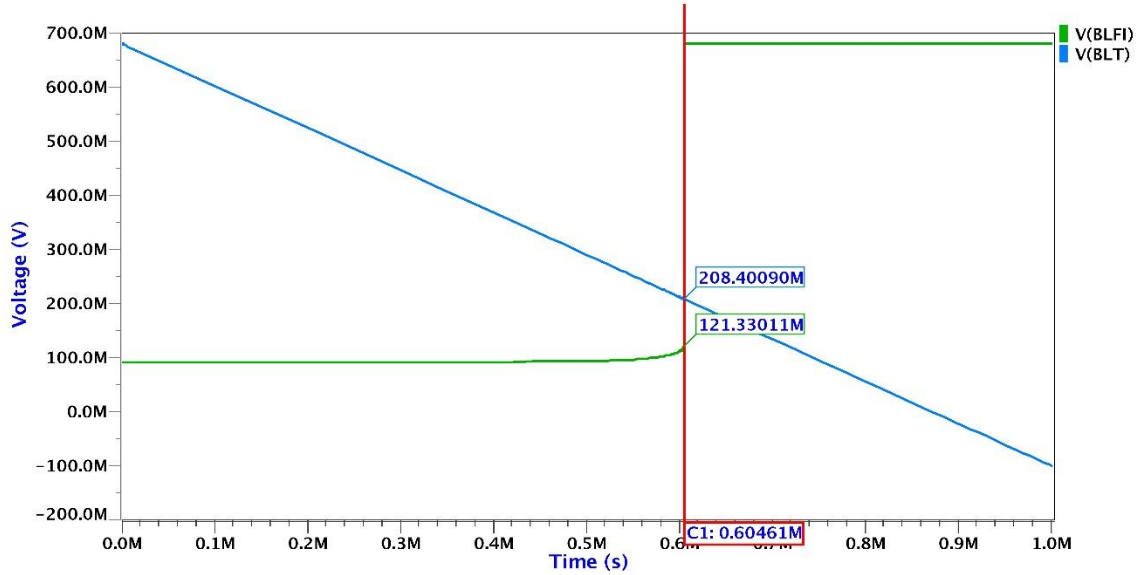


Figure 4.6(a) Write margin Operation and simulation results

4.3.3 Write Time

It is defined as the maximum time required by the transistors (MOS) to perform write operation in the bitcell. The analysis is being made by calculating the time required from 50% Word line slope to the 95% of the write node (initially stored as 0).

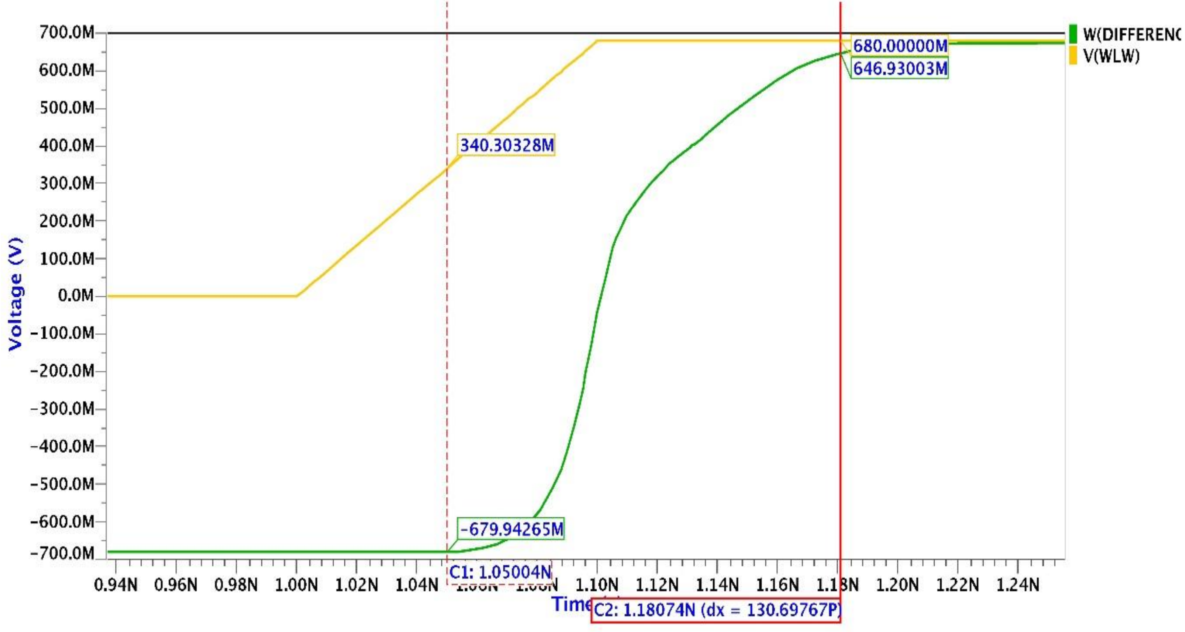


Figure 4.7(a) Write Time Calculation and Simulation results

4.3.4 Read Current (ION)

It is the current flowing through the drain of the pass transistor when bitcell is ON i.e. WL=1. Read current directly effects access time. When nmos & pmos both are slow read current is worst in that case as the drain current of the mos will be low. It will increase access time and thus our memory will be slowest. Read current is best when both nmos and pmos are fast. The read current (READ I), is the summation of two currents namely Dn (I) & Dp (I) flowing through nMOSFET (MN2) & pMOSFET (MA1) of a transmission gate (TG) respectively (see Fig. 3.1). This summation of Currents over two different transistors in parallel is primarily responsible for the lower value of variability in case of 6T SRAM. This averaging is impossible in case of 6T due to the existence of only one access transistor. Moreover, it can also be deduced that the Current through MP1 varies so as to stabilize the total Read Current in case Current through MN2 of TG varies due to RDF induced Vt shift and vice versa.

CHAPTER 5
Stability Analysis of 6T SRAM

ANUKRITI SINGH
Delhi Technological University

5.1 Worst Case Corner Analysis based on Stability Parameters

For analyzing worst case we need to know the behavior of the MOSs in terms of their ON time and threshold voltages. Designing a 6T SRAM cell takes many factors into consideration. The transistor sizes are kept same for PullUp, PullDown and PassGate transistors.

Let,

Pull-up size (PMOS) W/L = 48/38

Pull-down size (NMOS) W/L = 100/38

Pass gate size (NMOS) W/L =86/42

and Supply voltage VDD =0.68.

Temperature = - 40

Threshold Voltage is found as:

Table i. Vthp vs Vthn

Vth (in mv)	PU	PD	PG
	PMOS	NMOS	NMOS
SS	1.045	1.063	1.056
SF	0.983	1.065	1.064
FS	1.017	0.935	0.936
FF	0.954	0.939	0.945
TT	1.000	1.000	1.000

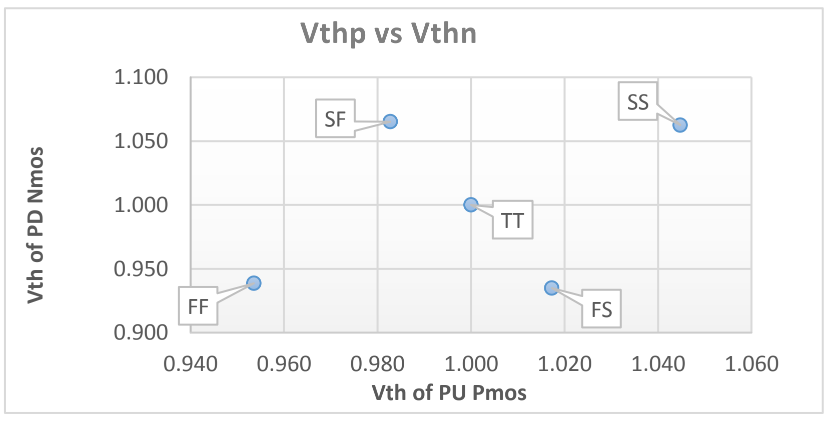


Figure 5.1. Corner analysis depending on Vth

For the similar transistors we calculated the on time and found the result as depicted in table ii. and table iii. corresponding to temperature -40 and 165 respectively. Also mentioned in the three figure (ii. iii. and iv) and three tables (i. ii. iii) about five corners SS, SF, FS, FF and TT.

Table ii. Ion time of different MOSs at temp -40

ION time (in usec)	PU Ion PMOS	PD Ion NMOS	PG Ion NMOS
SS	0.705	0.712	0.800
SF	1.115	0.747	0.736
FS	0.896	1.302	1.317
FF	1.404	1.357	1.353
TT	1.000	1.000	1.000

Table iii. Ion time of different MOSs at temp 165

ION time (in usec)	PU Ion PMOS	PD Ion NMOS	PG Ion NMOS
SS	0.774	0.772	0.772
SF	1.090	0.815	0.810
FS	0.917	1.209	1.217
FF	1.288	1.270	1.273
TT	1.000	1.000	1.000

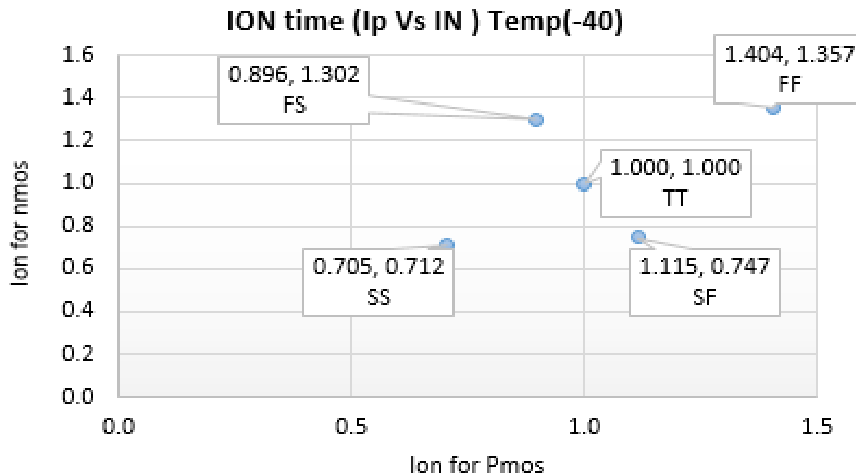


Figure 5.2.Corner analysis depending on Ion for temp. -40

The current flowing through the drain of the pass transistor when bitcell is ON i.e. WL=1. Read current directly effects access time. When nmos & pmos both are slow read current is worst in that case as the drain current of the mos will be low.

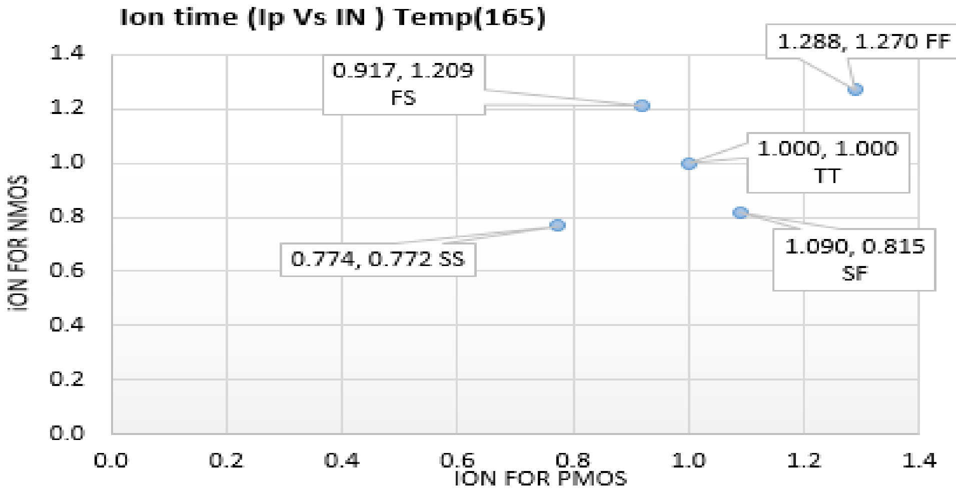


Figure 5.3 Corner analysis depending on Ion for temp.165

Analyzing the above graphs and table, SNM & WM worst corner analysis is done. And the conclusion was

a. FS corner is found worst corner as all the NMOSs will be fast i.e. highly doped and all the PMOSs will be slow i.e. lightly doped. If DT=0 and DC=1.Now, considering only the forward path,MP1 being slow will be holding data loosely and moreover, its VT being higher it will get OFF earlier than it would have been when considered very fast. Moreover, MN1 being fast will have lower VT and will get ON easily. This in turn results in flipping of data.

b. SF is the worst corner for writability as all the NMOSs will be slow i.e. lightly doped and all the PMOSs will be fast i.e. highly doped. If DT=0 and DC=1.Now, considering only the forward path, MP1 being fast will have low VT and thus will OFF late then being slow. Moreover, MN1 being slow will have higher VT and will get ON late. Thus, NMOS and PMOS being slow and fast respectively are not helping in flipping the data earlier.

The above cases gave the approach to analyze the worst corner for both SNM and WM.

6.2 Static Noise Margin Analysis & Write Margin Analysis

Considering Original case with

Pull-up size (PMOS) W/L = 48/43

Pull-down size (NMOS) W/L = 100/43

Pass gate size (NMOS) W/L =86/43

And Supply voltage VDD as 0.7, 0.75 and 1.15 for Temperature = - 40 for WM and Temperature = 125 for SNM, analysis is done for 12 different cases to get the high yield in order to qualify 1ppm failure rate.

The above condition resulted with different cases with different qualifying conditions. This is being shown in the table .

For analyzing a 6T SRAM cell we required to analyze its Static Noise (During read operation) and Write Margin(During write operation). After this we analyze its Current which is On current and Off current (Leakage current).All this figure of merit governs if the bit-cell will be stable in every mode of operation or not.

The analysis of On current and Off current prevails the power required and it also help us to determine the maximum and minimum voltage calculation for bitcell stability. The more the leakage current is, the power is required. So, to be ensured that the bitcell we designed is stable we keep in mind all these factors.

The behavior of SNM and WM is calculated at all possible PVT’s(Process, Voltage and Temperature).So, that in the worst corner analysis we won’t skip any part to be analyzed to ensure the stability analysis. All these variability has so many factors but the most essential one is the dopants behavior which is responsible for Vth shift.

The behavior of SNM is analyzed w.r.t to temperature and Voltages and can be seen in the below graphs.

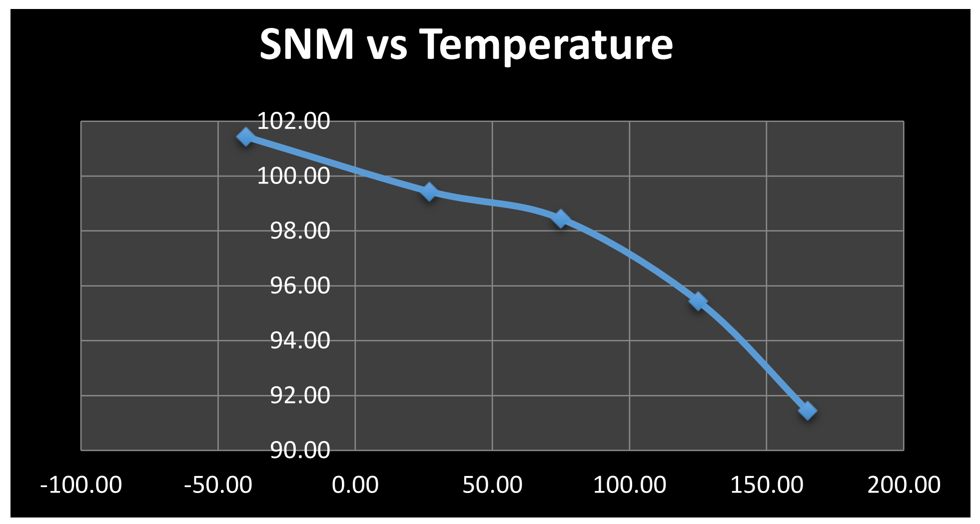


Figure 5.4 SNM variation with Temperature(-40,165)

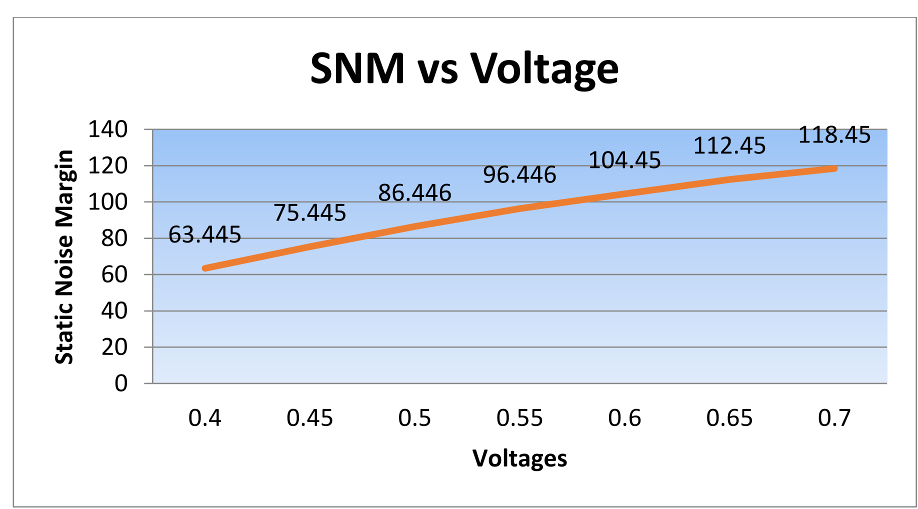


Figure 5.5 SNM variation with Voltage

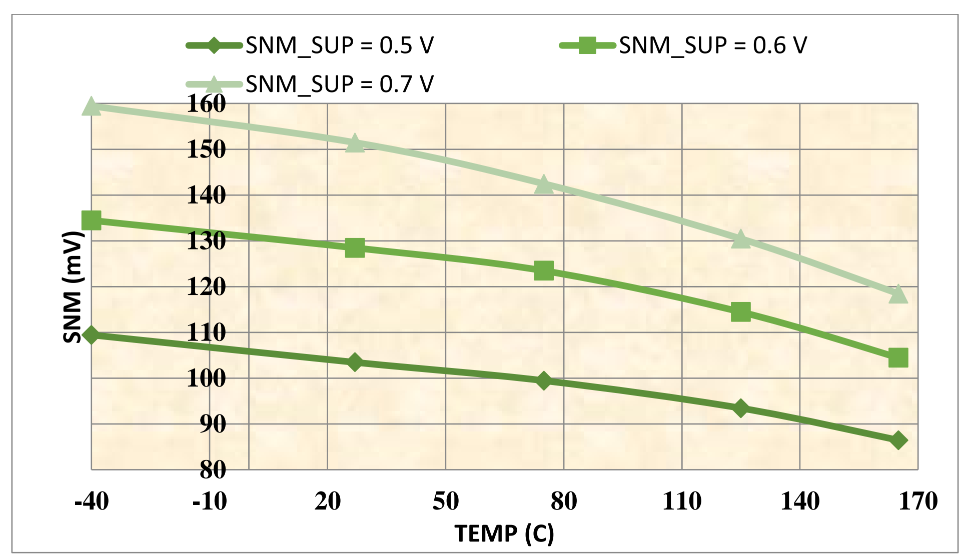


Figure 5.6 SNM variation with temperature with 3 different volatages

Similar Analysis is done for Write Margin Calculation.

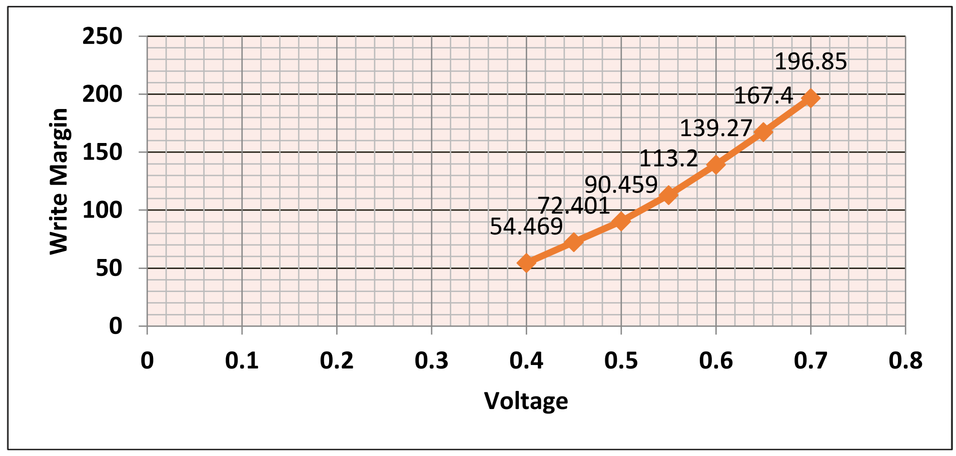


Figure 5.7 Write margin Variation with voltage

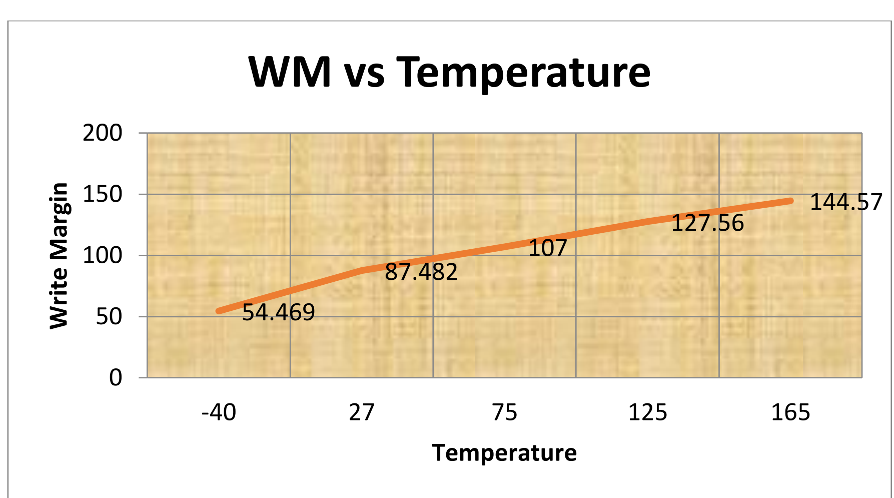


Figure 5.8 Write Margin variation with temperature

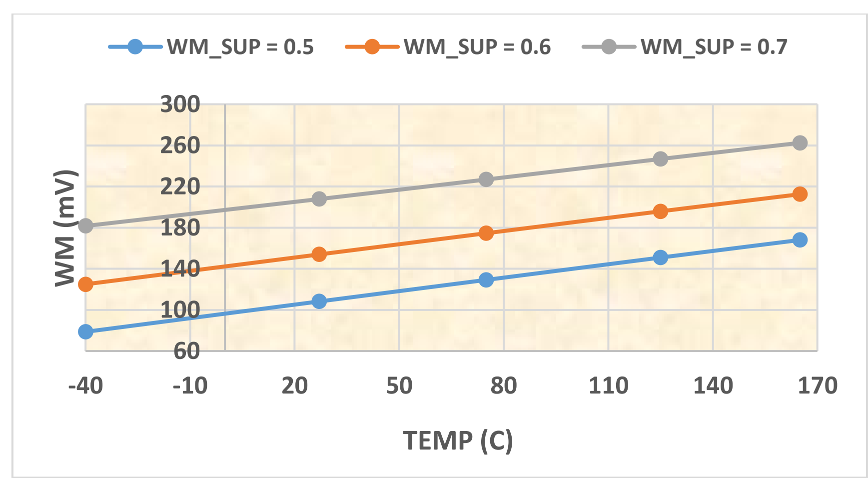


Figure 5.9 Write margin variation with temperature on 3 different voltages

6.3 Methodology

The above analysis was done on keeping W/L for

Pull-up size (PMOS) W/L = 48/43

Pull-down size (NMOS) W/L = 100/43

Pass gate size (NMOS) W/L =86/43

Now, doing further analysis to get the best result in order to get the optimized area with different W/L's of PG, PU and PD.The main thing that comes into picture is the Beta and Gamma ratio.

The primary motivation behind aggressive device scaling is to achieve improved, performance and increased integration .These improvements come at the cost of increased sensitivity to PVT variations and standby leakage, particularly in area-constrained circuit such as SRAM that employs minimum- geometry devices. An attempt is made in this work to mitigate these problems in traditional 6T SRAM cell by incurring minimum area penalty and retaining its fully differential architecture Standard 6T SRAM cell is carefully designed to achieve a balance between conflicting read and write requirements along with minimum silicon area.

However, increasing parametric variation and decreased supply voltage have reduced the cell noise margins, thereby decreasing the reliability of read/write and hold operations. Statistical variability in particular can result in each device of an SRAM cell to behave differently , disturbing the symmetrical balance achieved with device sizing. Large threshold voltage variations can even cause functional failures, thereby, degrading the reliability of SRAM cell. Variability in device characteristics due to RDF (random dopant fluctuation), LER (line-edge-roughness) , OTV (oxide thickness variations) affects the reliability of an SRAM. It increases the timing violations and makes the leakage power dissipation unpredictable. Higher subthreshold and gate

leakage currents in nanoscaled devices prevent further SRAM scaling and also degrade cell stability.

It became tough to differentiate between the cumulative subthreshold leakage current of not used memory cell and the read current of the accessed cell. This may result in read failure and impose a theoretical upper bound on the number of cells sharing a common bitline. The power drawn from the supply source due to leakage currents of several million cells can consume a significant portion of the power budget of a chip. With continued scaling, the capacitance on the internal nodes of a cell decreases. Thus, the amount of charge needed to disturb a cell decreases.

The $I_{(ON\ NMOS)}$ to $I_{(ON\ PMOS)}$, ratio has decreased with scaling, due in large part to the development of strained silicon channels. Strain technologies have improved hole mobility (μ_p) more than electron mobility (μ_n). Although beneficial for speed in logic devices , this can degrad SRAM writeability. If minimum-width pull-up and access devices are retained, the **gamma ratio** of the cell is increased .This may result in write failure. The access device must be made larger to maintain the original gamma ratio, but this requires a proportional increase in the width of pull-down device to maintain the same **beta ratio**. It thus, becomes more difficult to scale cell area at the historical rate.

Beta ratio:

$$\beta = \frac{(\frac{Wpd}{Lpd})}{(\frac{Wpg}{Lpg})}$$

Gamma ratio:

$$\gamma = \frac{(\frac{Wpg}{Lpg})}{(\frac{Wpu}{Lpu})}$$

Variation of SNM and WM w.r.t Beta ratio

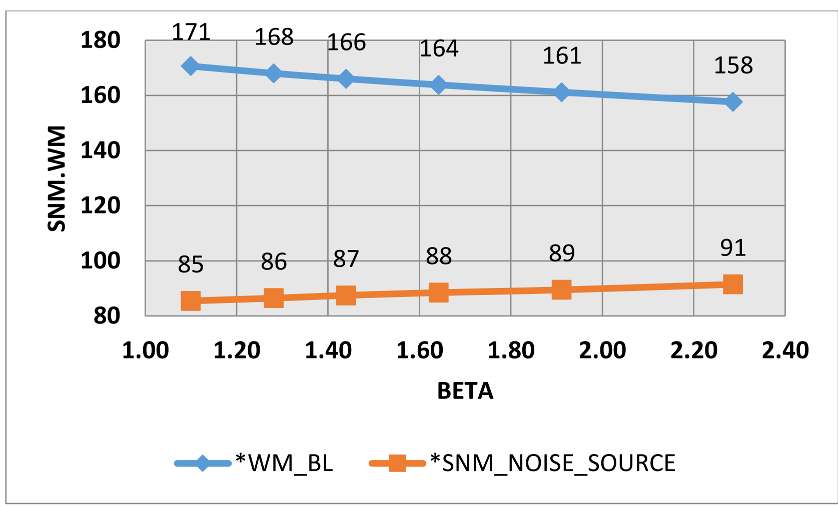


Figure 5.10 SNM and Wm variation with Beta ratio

Variation of SNM and WM w.r.t Gamma ratio

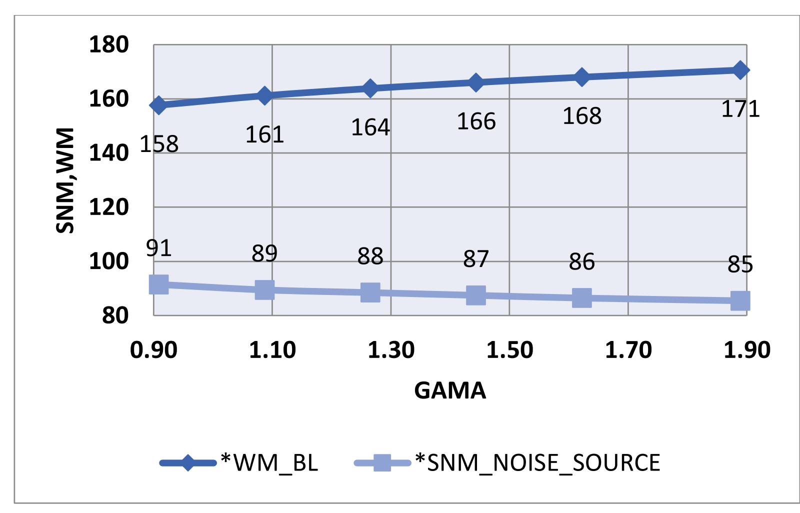


Figure 5.11 SNM and Wm variation with Gamma ratio

These all variability analysis helped in analyzing the bitcell more efficiently and effectively. The variability constrained memory design a lot.Although we have technology benefit of reduction in leakages and lesser power consumption but we have area constraints which needs to be emphasized too.For this the Beta and Gamma ratio are being varied.

The calculations were done by iterating different cases from the original design we took.

Simulation Results of Varying SNM and WM with different Beta and Gamma Ratio

Table iv. Analysis results for SNM and WM corresponding to difference W/L combinations

	PG	PD	PU	PG	PD	PU	WM	WM	WM	SNM	SNM	SNM
Cases:	W	W	W	L	L	L	0.7 , -40 ,SF	0.75 - 40 ,SF	1.15 - 40 ,SF	0.7 ;165;FS	0.75 ;165;FS	1.15 ;165;FS
Original Case	86	100	48	43	43	43	1.18	1.43	>>too high	1.0325	1.06	0.93
Aged										0.9313	0.97	0.89
Case1	86	91	57	43	43	43	1.12	1.36	>>too high	1.0192	1.04	0.90
Aged										0.9950	0.96	0.85
Case2	77	100	48	43	43	43	1.08	1.30	>>too high	1.0770	1.12	1.13
Aged										0.9827	1.09	1.04
Case3	77	91	57	43	43	43	1.02	1.23	>>too high	1.0640	1.10	1.03
Aged										0.9680	1.01	0.99
Case4	86	106	42	43	43	43	1.23	1.49	>>too high	1.0160	1.05	0.94
Aged										0.9202	0.96	0.90
Case5	67	100	48	43	43	43	1.04	1.24	>>too high	1.1297	1.18	1.21
Aged										1.0347	1.10	1.18
Case6	86	106	48	43	43	43	1.25	>>too high	>>too high	1.0727	1.10	1.01
Aged										0.9763	1.02	0.97
Case7	77	106	48	43	43	43	1.15	1.38	>>too high	1.1200	1.16	1.14
Aged										1.0247	1.08	1.11
Case8	86	100	48	45	41	41	1.20	1.46	>>too high	1.0657	1.09	0.98
Aged										0.9660	1.01	0.95
Case9	86	100	48	47	39	39	1.15	1.41	>>too high	1.0967	1.13	1.02
Aged										0.9997	1.05	0.98
Case10	82	100	48	47	39	39	1.11	1.35	>>too high	1.1147	1.15	1.07
Aged										1.0192	1.06	1.03
Case11	86	100	57	43	43	43	1.18	1.42	>>too high	1.0953	1.13	1.03
Aged										1.0263	1.04	0.99
Case12	77	100	57	43	43	43	1.08	1.29	>>too high	1.1408	1.19	1.16
Aged										1.0470	1.10	1.12

The above table gave the conclusion for feasible results which can be definitely extracted from case 2 and case 10.The qualification of 1ppm failure rate for memory bitcell design could be achieved from these two cases for which layout can be easily prepared. Rests of the results were discarded. Case 5 and Case 7 also qualified our requirement but in order to achieve device size only case 2 and case 10 were feasible.

For area advantage bitcell proposed for the automotive use. Automotive product works till very high temperature of 165^{0}C. At such high temperature stability of bit-cell at maximum voltage is issue. This analysis figure out the optimum Beta and Gamma ratio of the bit-cell to achieve higher stability at minimal cost possible of other parameters such as static read stability and write stability measure . Transistor size changes are restricted in order to respect the area .By varying the sizes of bitcell PullUp transistors, PullDown transistors and PassGate transistors , we would achieve mentioned target as discussed. Considering constraints of sizes, voltages and temperature into account we can get achieve the larger yield in terms of memory capacity of the memory bitcell. Further improving the technology would help in future analysis. As today the analysis is done on 28nm FDSOI CMOS technology but this would be improved in upcoming technologies. The simulation results shown have improvement in Write Margin and Static Noise Margin for temperature -40 and 165 respectively. The modification in sizes of bitcell has achieved the target of 1ppm failure rate for high density bitcell. Adding more transistors would also improve the read stability and write stability .The only trade-off is in between gaining Noise Margin with increase in area. Also increasing the voltage would be in favor of increasing memory cell stability during read operation. The modified 6T SRAM can be used as cache memory in internal CPU.The leakage is the most challenging part of this analysis done for SRAM implementing architecture which can be improved by modification in bitcell design of future work.

Also the cases taken into consideration were also analyzed for Icell and Ileak.This is helpful in analyzing the fact about the optimized power requirement.

The results after the simulations are below:

Table v ION percentage variation on different PVT's

	% Loss ION Norm	% Loss ION Norm	% Loss ION Norm	% Loss ION Norm	% Loss ION 6 sigma worst	% Loss ION 6 sigma worst	% Loss ION 6 sigma worst	% Loss ION 6 sigma worst
	0.7V/SS /-40C	0.9V/SS /-40C	0.7V/SS /25C	0.9V/SS /25C	0.7V/SS /-40C	0.9V/SS /-40C	0.7V/SS /25C	0.9V/SS /25C
Case1	6%	6%	6%	6%	4%	5%	4%	5%
Case2	5%	6%	5%	6%	17%	11%	15%	10%
Case3	11%	11%	11%	11%	20%	15%	18%	15%
Case4	-4%	-3%	-3%	-3%	-2%	-3%	-2%	-3%
Case5	11%	13%	11%	13%	35%	23%	32%	22%
Case6	-4%	-3%	-3%	-3%	-2%	-3%	-2%	-3%
Case7	2%	3%	2%	3%	16%	8%	14%	8%
Case8	1%	1%	1%	1%	2%	1%	2%	1%
Case9	2%	2%	2%	2%	3%	1%	3%	1%
Case10	4%	4%	4%	4%	10%	5%	9%	5%
Case11	0%	0%	0%	0%	0%	0%	0%	0%
Case12	5%	6%	5%	6%	17%	11%	15%	10%

Table vi Ileak percentage variation on different PVT's

	% Increase in ILEAK			
PVT	0.9/TT/25C	1.15/TT/165C	0.9/FF/25C	1.15/FF/165C
Case1	1%	8%	-1%	1%
Case2	-1%	-3%	-1%	-3%
Case3	1%	5%	-1%	-2%
Case4	-1%	-5%	0%	-2%
Case5	-1%	-6%	-2%	-6%
Case6	2%	2%	2%	2%
Case7	1%	-1%	1%	-1%
Case8	1%	2%	0%	0%
Case9	4%	11%	3%	9%
Case10	-4%	-10%	-3%	-8%
Case11	-4%	-11%	-3%	-4%
Case12	-4%	-8%	-2%	-1%

Keeping in mind all the analysis we concluded to design a 6T SRAM bit-cell in order to qualify 1ppm failure rate for 2 Mb memory capacity targeting temperature(-40,165).

The case 10 gave the most optimized result after simulation keeping SNM and WM into consideration.

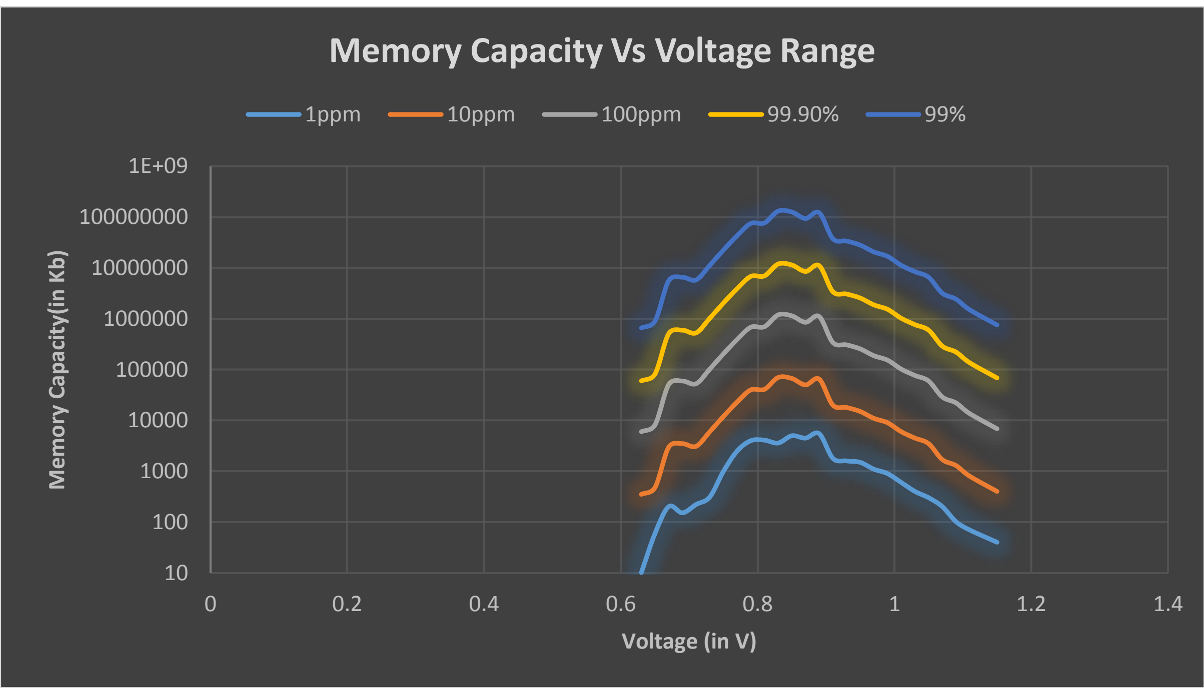


Figure 5.12 Maximum Memory Capacity qualification at different failure rates

The above graph shows the best optimized result as we targeted 2 Mb memory capacities which should qualify 1part per million failure rates at temperature 165.This bitcell with the most optimized result can be effective in proper Read and Write Operation.This is analyzed at all PVT's which can contribute in the worst case analysis. This result showed drastic improvement in device performance for qualification of larger memory capacity which is better than the other design parameters over standard 6T memory SRAM cell focusing on its functionality & robustness . It lessens the impact of Process Voltages and Temperature variations mainly due to Access Transistors involved in our design.This has been possible because of flavoured devices used other than regular Vth device or Lower Vth devices.

CHAPTER 6

Conclusion and Future Work

Conclusion and Future Work

In this work, the efficient generation of high sigma for 1ppm failure rate is aimed. The Static Noise Margin, Write Margin, Icell and Leakage current calculated were selected keeping in mind, the area optimization and qualifying 1ppm failure rate for larger memory capacity. The sensitivity of Read Noise margin and Write Margin is being estimated for different variations on various devices. Static Read Stability and Write Stability variation is being observed at different PVT's corresponding to different temperature and Voltage combinations. It's been observed that Static Noise Margin is worst when Nmos devices are Fast and Pmos devices are slow whereas Write Margin is worst when Nmos devices are slow and Pmos devices are fast. This analysis has helped in analyzing worst cases for this 6T SRAM bit-cell. Then the estimation is made for Static Noise Margin and Write Margin variation with Beta ratio as well as Gamma ratio. This further helped in choosing the best possible case for 6T SRAM bit-cell with the greater stability in terms of higher Static Read stability and Write Stability with the qualification 1ppm failure rate of high density memory bitcell.As shown in previous figures (vi. vii. and viii) it is clear that we can achieve our target i.e. qualifying higher memory with 1ppm failure rate at higher temperature with the discussed cases. Optimization exercise relieve that best design is Case 2 & Case 10 with least penalty on Ion with better SNM and WM. For area advantage bitcell proposed for the automotive use. Automotive product works till very high temperature of 165^0C. At such high temperature stability of bitcell at maximum voltage is issue. This analysis figure out the optimum Beta and Gamma ratio of the bit-cell to achieve higher stability at minimal cost possible of other parameters such as static read noise margin (SNM) and write margin (WM). Transistor size changes are restricted in order to respect the area. By varying the sizes of bitcell PullUp transistors, PullDown transistors and PassGate Transistors, we would reach the target discussed. Considering constraints of sizes, voltages and temperature into account we can get achieve

the larger yield in terms of memory capacity of the memory bitcell. Further improving the technology would help in future analysis. As today the analysis is done on 28nm FDSOI CMOS technology but this would be improved in upcoming technologies. The simulation results shown has improvement in Write Margin and Static Noise Margin for temperature -40 and 165 respectively. The modification in sizes of bitcell has achieved the target of 1ppm failure rate for high density bitcell. Adding more transistors would also improve the read stability and write stability .The only trade-off is in between gaining Noise Margin with increase in area. Also increasing the voltage would be in favor of increasing memory cell stability during read operation. The modified 6T SRAM can be used as cache memory in internal CPU.The leakage is the most challenging part of this analysis done for SRAM implementing architecture which can be improved by modification in bitcell design of future work.

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