

# **DESIGN AND ANALYSIS OF BAND GAP REFERENCE CIRCUITS**

A

DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIRMENTS FOR THE AWARD

OF THE DEGREE OF

**MASTER OF TECHNOLOGY  
IN  
CONTROL & INSTRUMENTATION  
(2015-2017)**

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### **Candidate's Declaration**

I, **Vivek Mittal**, Roll No. **2K15/C&I/21**, student of **M. Tech (Control & Instrumentation)**, herewith declare that the thesis titled “*Design and Analysis of Band Gap Reference Circuits*”, underneath the supervision of Prof. Pragati Kumar of Electrical Engineering Department, Delhi Technological University, in partial fulfilment of the need for the award of the degree of master of technology, has not been submitted elsewhere for the award of any degree.

I herewith solemnly and sincerely confirm that all the particulars declared above by me are true and correct to the best of my knowledge and belief.

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## **Certificate**

This is to certify that the dissertation entitled “*Design and Analysis of Band Gap Reference Circuits*” submitted by **Vivek Mittal** in completion of major project dissertation for the master of Technology degree in **Control & Instrumentation** at Delhi Technological University is an authentic work carried out by him underneath my superintendence and guidance.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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## **Acknowledgement**

It gives me a great pleasure to express my profound gratitude to my supervisor and project guide **Prof. Pragati Kumar**, Department of Electrical Engineering, Delhi Technological University (formerly Delhi College of Engineering), for his invaluable guidance, encouragement and patient reviews throughout the progress of this dissertation. It has been a great experience to get a chance under his rich experience.

I would conjointly wish to extend my heartfelt thanks to Prof. Madhusudan Singh, head of the department and all faculty of department of Electrical Engineering, Delhi Technological University, for keeping the spirits high and clearing the visions to work on the project.

I am conjointly grateful to my family and friends for their constant support and motivation throughout this work.

Finally, I am thankful to the almighty because without his blessing, this work was not possible.

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## **ABSTRACT**

Band Gap Reference circuits are integral part of Analog Integrated Circuits. Their function is to provide a constant reference voltage independent of temperature and supply variations. Two major building blocks of band gap reference circuits are CTAT (Complementary to absolute temperature) and PTAT (Proportional to absolute temperature). The important characteristics of CTAT circuits is the inverse relationship of their output voltage with temperature while the PTAT circuits have proportional dependence. By combining the circuits exhibiting the CTAT and PTAT nature, a constant dependence of voltage on temperature can be achieved which can be used as reference voltage for other analog circuits. Design of CTAT and PTAT circuits and their simulation using the Cadence Design Systems Software have been presented in this dissertation.

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## LIST OF SYMBOLS

S.No	Symbols	Descriptions
1	CMOS	Complementary Metal Oxide Semiconductor
2	NMOS	N-type Metal Oxide Semiconductor
3	PMOS	P-type Metal Oxide Semiconductor
4	BGR	Band Gap Reference
5	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
6	Op-Amp	Operational Amplifiers
7	$V_{ref}$	Reference Voltage
8	$V_{dd}$	Supply Voltage
9	$V_T$	Thermal Voltage
10	w.r.t	with respect to
11	gnd	ground
12	PTAT	Proportional to absolute temperature
13	CTAT	Complementary to absolute temperature
14	k	Boltzmann's constant
15	q	Electric charge
16	T	Temperature
17	$n_i$	Intrinsic carrier concentration
18	$\mu$	Mobility
19	$\epsilon_g$	Energy band gap
20	$I_o$	Diode Current
21	$I_s$	Reverse Saturation Current

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## CHAPTER – 1

# **INTRODUCTION**

## **1.1 HISTORICAL BACKGROUND:**

This dissertation presents design and analysis of Band Gap Reference circuits. Before we present the details of our work, a brief overview of the work done on bandgap references is given below.

The concept of Band gap voltage reference was first published by David Hilbiber in 1964. During his brief tenure at Fairchild semiconductors he found that the potential difference between two diodes can provide a proportional dependence on temperature provided a fairly constant amount of current is passed through them [1].

Later Robert Wildar, Paul Brokaw and others refined the concept given by Hilbiber and implemented commercially successful versions of Band gap Reference (BGR) circuit using bipolar devices [2-3]. The Band gap reference circuit proposed by Robert Wildar became popular as a replacement of Zener diodes to be utilised in data acquisition systems and digital ICs where Zener diodes were not much suitable, since the breakdown voltage of a typical Zener diode is higher than the potential at which the modern circuits operate [4]. With the advent of rise in CMOS technology in late 1970s, several attempts were made to replicate Wildar's design by solely using CMOS devices but due to high mismatch in the threshold voltage of NMOS and PMOS devices it was observed that the designs which were based solely on CMOS devices has significant error as compared to those utilising bipolar devices along with the CMOS devices [5].

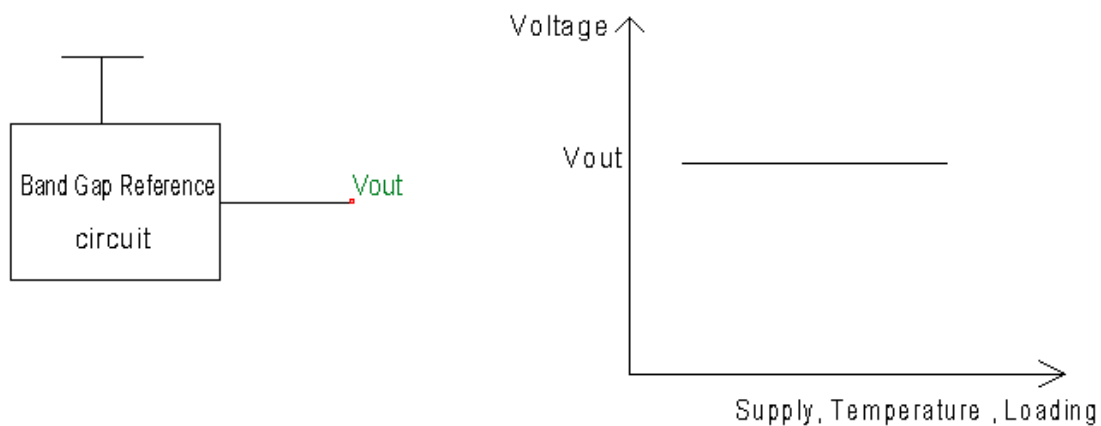
## **1.2 INTRODUCTION TO BAND GAP CIRCUITS:**

The function of Band gap reference circuit is to provide a constant reference voltage independent of supply, temperature and circuit loading. Band gap reference or voltage reference circuits are one of the major building blocks of any modern analog IC so much so that in almost any analog IC one can find at least one BGR [6].

The supply voltage independence of a circuit could be achieved by utilising the threshold voltage  $V_T$  of MOS device as a bandgap reference voltage but due to dependence of the threshold voltage on temperature it is largely avoided.

Since most of the process parameters are dependent on temperature which in turn are the dependence of the basic electrical quantities such as voltage and current, we do not have any circuit which is in itself independent of the temperature.

Thus, in order to achieve the temperature independence of a circuit the negative dependence of the voltage measured across a p-n junction is cancelled with a circuit depicting positive temperature dependence.

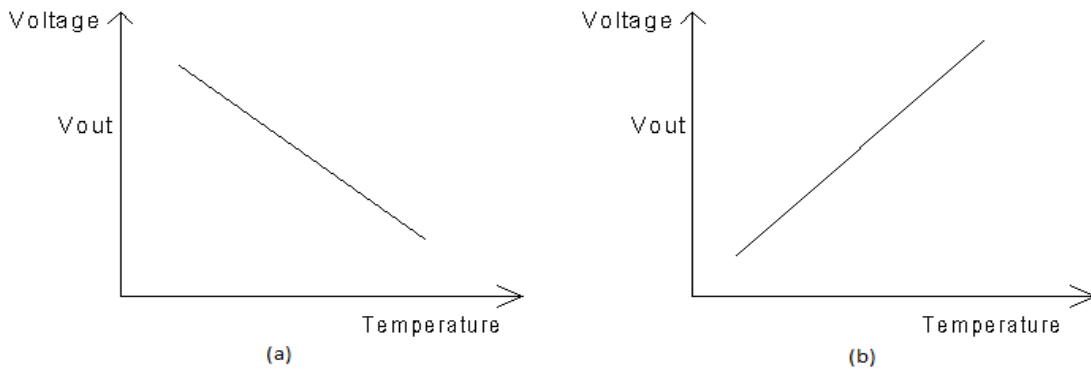


**Figure 1.1** Ideal expected behaviour of Band gap reference voltage circuit

Temperature independence can prove very critical for a circuit since most of the process parameters are inter-dependent on the temperature, so if a circuit can somehow be made temperature independent then the variations in the process parameters will largely be suppressed.

If we analyse the voltage or current dependence of variations of the various circuits on the basis of temperature then we can group those circuits into two categories [9].

1. CTAT (Complementary to absolute temperature)
2. PTAT (Proportional to absolute temperature)



**Figure 1.2** (a) CTAT Behaviour (b) PTAT Behaviour

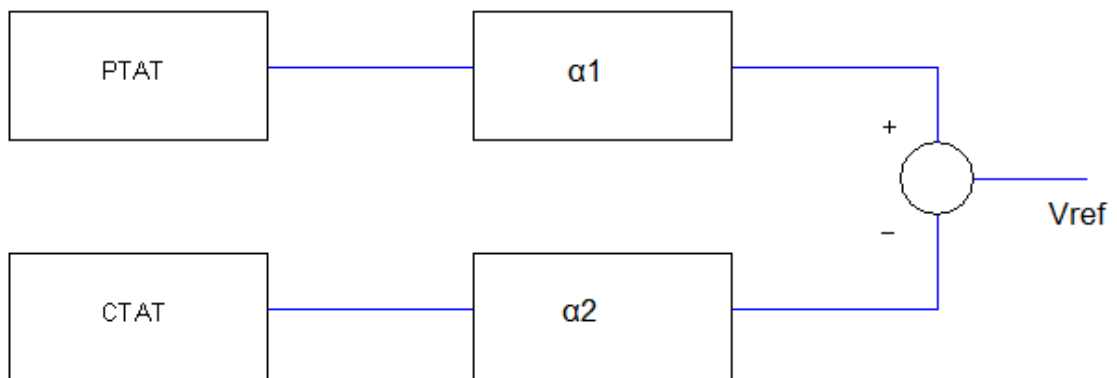
i.e. CTAT having negative temperature coefficient and PTAT having positive temperature coefficient.

In order to achieve zero temperature coefficient (ZC) two circuits each exhibiting PTAT and CTAT behaviour are added.

$$\frac{\partial V_{CTAT}}{\partial T} + \frac{\partial V_{PTAT}}{\partial T} = 0 \quad (1.1)$$

Therefore,

$$V_{Ref} = \alpha_1 V_{CTAT} + \alpha_2 V_{PTAT} \quad (1.2)$$



**Figure 1.3** Block diagram representing the generation of constant reference voltage

### **1.3 CONCLUSIONS**

In chapter 2, CTAT (Complementary to absolute temperature) circuit design is discussed and simulation of those circuits are given.

In chapter 3, PTAT (Proportional to absolute temperature) circuit design is discussed and simulation of those circuits are given.

In chapter 4, how we can go about adding CTAT and PTAT circuits discussed in the above chapters to achieve constant reference voltage independent of temperature and supply voltage is discussed and simulation of those circuits are given.

In chapter 5, Design of band gap reference circuits with cascode current mirrors to achieve better supply rejection is discussed and simulation of those circuits are given.

In chapter 6, the importance of design of start-up circuits in a self-bias circuit such as band gap reference circuits are discussed and simulation of band gap reference circuits are given.

In chapter 7, the future scope of work is discussed.

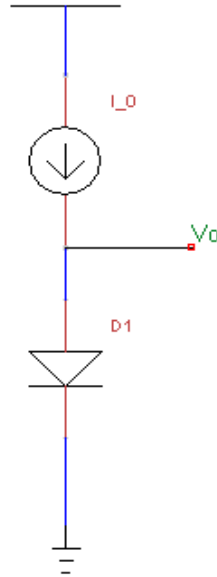


## CHAPTER – 2

# **CTAT DESIGN**

## 2.1 INTRODUCTION:

If we provide a constant current through a diode as shown in the figure 2.1 below then it is observed that the voltage across the diode is CTAT in nature [6].



**Figure 2.1** Simple circuit to generate a CTAT voltage ( $V_o$ ) across diode  $D_1$

We know that the standard equation for the current through the diode is [7].

$$I_o = I_s e^{V_D/V_T} \quad (2.1)$$

Where,  $V_T$  = Thermal Voltage (approximately equal to 26 mV at 300 K)

$V_D$  = Voltage across the diode  $D_1$

$I_o$  = Forward diode current

$I_s$  = Reverse saturation current

Therefore,

$$V_D = V_T \ln\left(\frac{I_o}{I_s}\right) \quad (2.2)$$

The dependence of the voltage  $V_D$  with respect to temperature is CTAT in nature, while the slope of  $\frac{\partial V_D}{\partial V_T}$  is known to be approx.  $-1.6 \text{ mV/K}$  at 300K provided a constant current is passed through the diode [8].

Also,

$$V_T = \frac{kT}{q} \quad (2.3)$$

Where,

k = Boltzmann's constant,  $1.38 \times 10^{-23}$  joules

q = electric charge,  $1.6 \times 10^{-19}$  coulomb

T = temperature

From the above equation we can note that,

$$V_T \propto T \quad (2.4)$$

Thus,  $V_T$  is PTAT in nature.

$$\frac{\partial V_T}{\partial T} = \frac{k}{q} \quad (2.5)$$

We are providing constant current across the diode, therefore

$$\frac{\partial I_o}{\partial T} = 0 \quad (2.6)$$

$$I_s = \mu kT n_i^2 \quad (2.7)$$

$$\mu = \mu_o T^m \quad (2.8)$$

$$n_i^2 \propto T^3 \exp\left(\frac{-\epsilon_g}{KT}\right) \quad (2.9)$$

where,

$\mu$  = mobility

$n_i$  = intrinsic carrier concentration

m = constant (generally taken as -1.5)

$\epsilon_g$  = Energy Band gap for the semiconductor

From equations 2.7, 2.8, 2.9 we get,

$$I_s \propto \mu_o T^m \cdot KT \cdot T^3 \exp\left(\frac{-\epsilon_g}{KT}\right) \quad (2.10)$$

Resolving all the temperature independent quantities as a constant (b) we get,

$$I_s = b T^{(4+m)} \exp\left(\frac{-\varepsilon_g}{KT}\right) \quad (2.11)$$

$$\frac{\partial I_s}{\partial T} = b T^{(4+m)} \exp\left(\frac{-\varepsilon_g}{KT}\right) \left[\frac{\varepsilon_g}{KT^2} + \frac{4+m}{T}\right] \quad (2.12)$$

$$\frac{\partial I_s}{\partial T} = I_s \left(\frac{4+m}{T} + \frac{\varepsilon_g}{KT^2}\right) \quad (2.13)$$

and,

$$\frac{\partial V_D}{\partial T} = \frac{\partial V_T}{\partial T} \ln\left(\frac{I_o}{I_s}\right) - \frac{V_T}{I_s} \frac{\partial I_s}{\partial T} \quad (2.14)$$

Resolving the above equation with 2.5 and 2.13 we get,

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (4+m)V_T - \varepsilon_g/q}{T} \quad (2.15)$$

Putting values in above equation as

$$V_D = 0.7 \text{ V}$$

$$m = -1.5$$

$$V_T = 26 \text{ mV}$$

$$\varepsilon_g = 1.2 \text{ V}$$

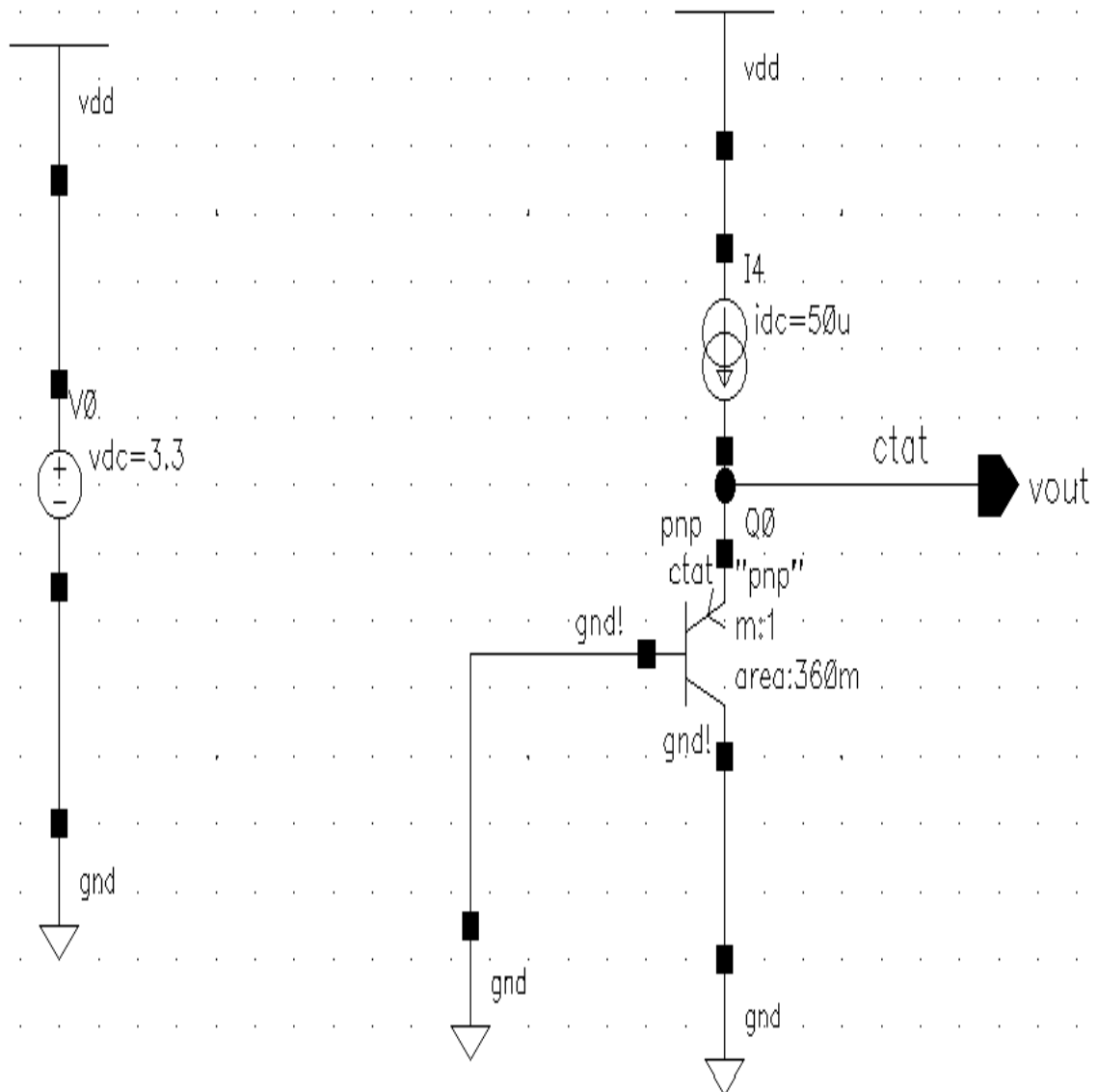
$$T = 300 \text{ K}$$

We get,

$$\frac{\partial V_D}{\partial T} = -1.833 \text{ mV/K} \quad (2.16)$$

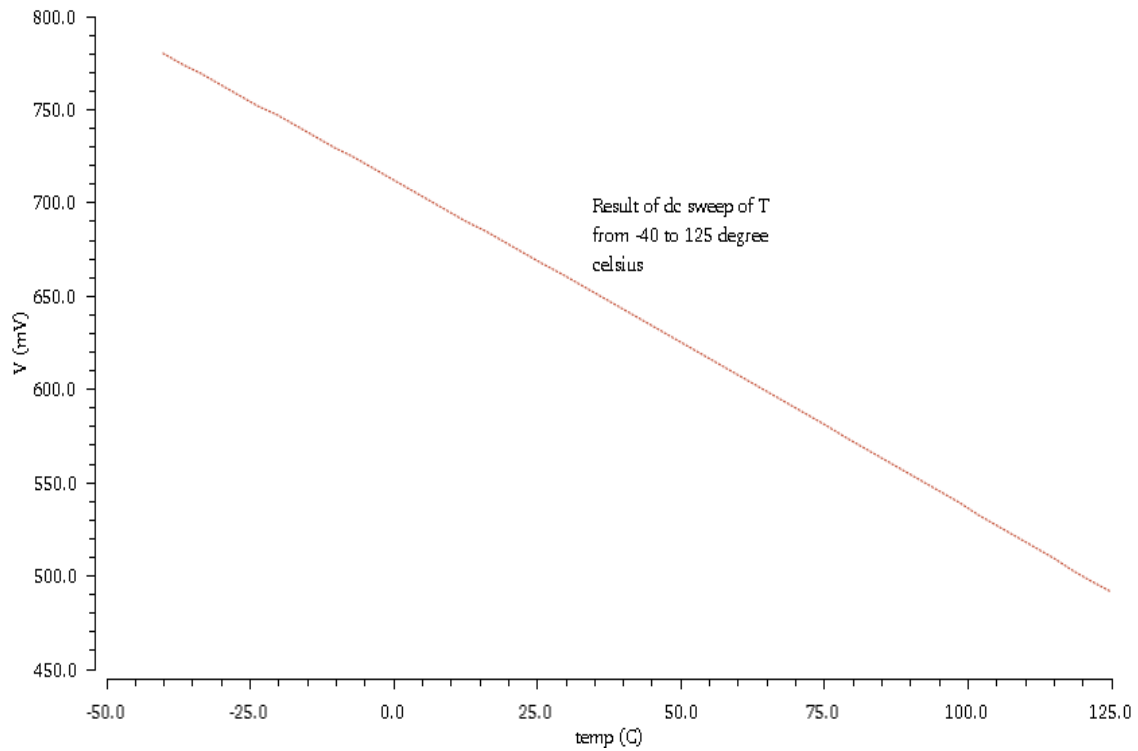
From the above equation 2.16, we can conclude that the voltage across a diode is CTAT in nature, provided a constant current is passed through it.

## 2.2 SIMULATION RESULTS:

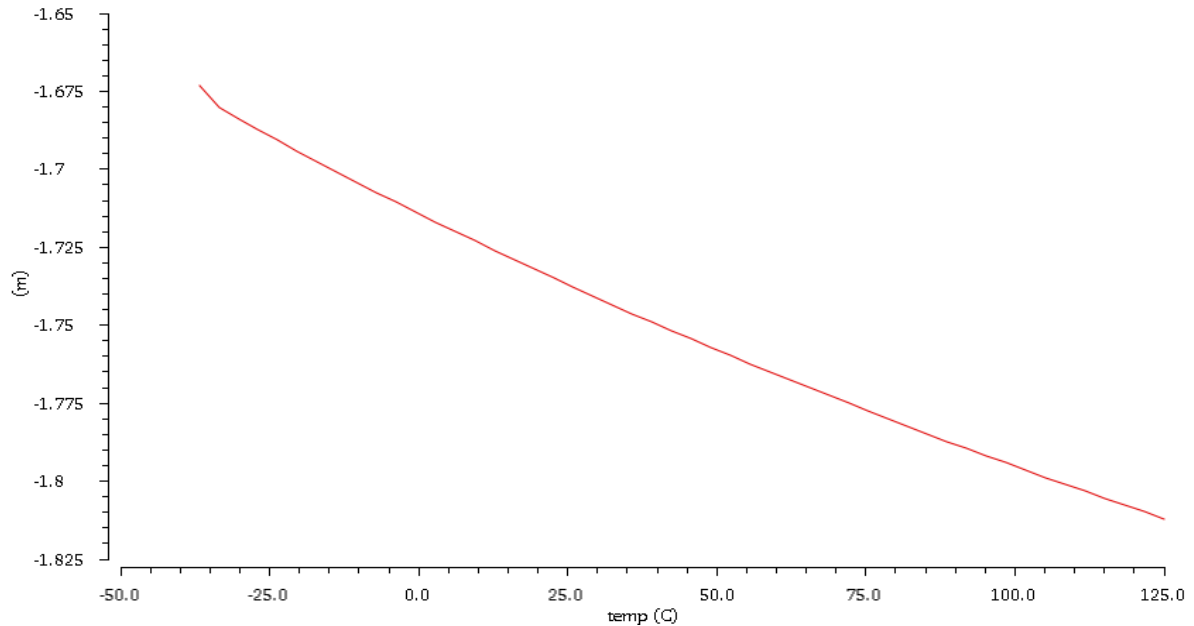


**Figure 2.2** Circuit diagram as drawn in Cadence

The reason the voltage across a diode is CTAT in nature because increasing the temperature results in higher probabilities of collisions between electrons and holes which leads to a significant increase in heat losses [6].



**Figure 2.3** Result of DC sweep of  $V_{out}$  w.r.t T from -40 to 125 °C



**Figure 2.4** Plot showing the variation of  $\frac{\partial V}{\partial T}$  w.r.t. to temperature

From the fig 2.4 we can see that the nature of the  $\frac{\partial V_D}{\partial T}$  is complementary to absolute temperature i.e. the voltage across the diode is CTAT in nature.

## **2.3 CONCLUSIONS:**

In this chapter we discussed the design and analysis of CTAT (Complementary to absolute temperature). We came to conclude that the voltage across a diode provided a constant current is passed through it acts as a CTAT. Later we also simulated in cadence to prove the above observation true.

## CHAPTER – 3

# **PTAT DESIGN**



### 3.1 INTRODUCTION:

When we designed CTAT, we found that  $V_T$  has proportional dependence on the temperature (eq. 2.4). Also, we noticed that the  $V_D$  is CTAT because of the dominating nature of the logarithmic term (eq. 2.2).

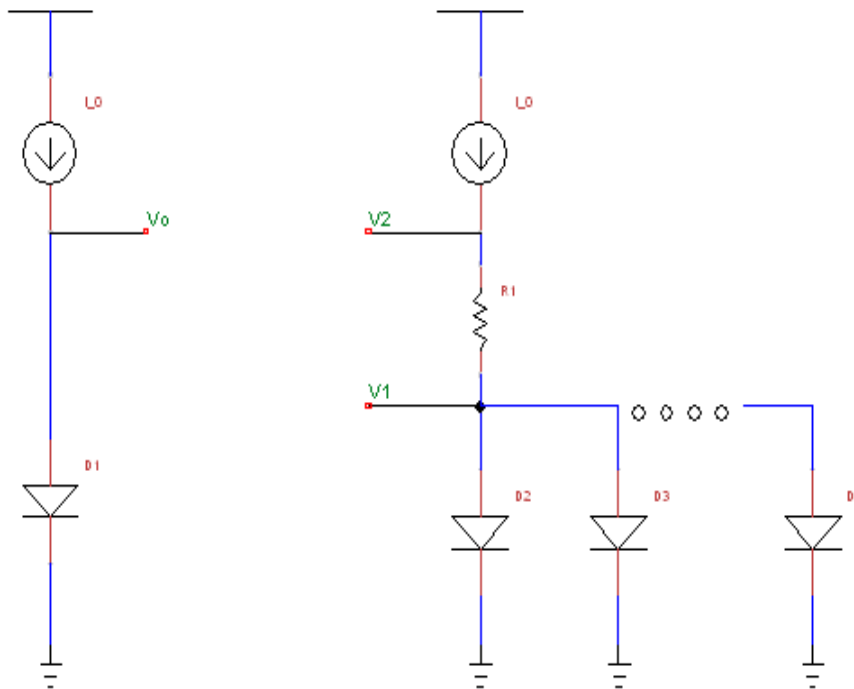
Therefore, in order to get a proportional dependence of voltage on the temperature we need to cancel the logarithmic term [9].

This we can do by subtracting the potential across two diodes.

$$V_d - V_{d1} = V_T \ln\left(\frac{I_o}{I_s}\right) - V_T \ln\left(\frac{I_o}{nI_s}\right) \quad (3.1)$$

$$V_d - V_{d1} = V_T \ln(n) \quad (3.2)$$

Where n is number of diodes in second branch.



**Figure 3.1** Simple circuit to get a PTAT voltage ( $V_2 - V_1$ )

### 3.2 SIMULATION RESULTS:

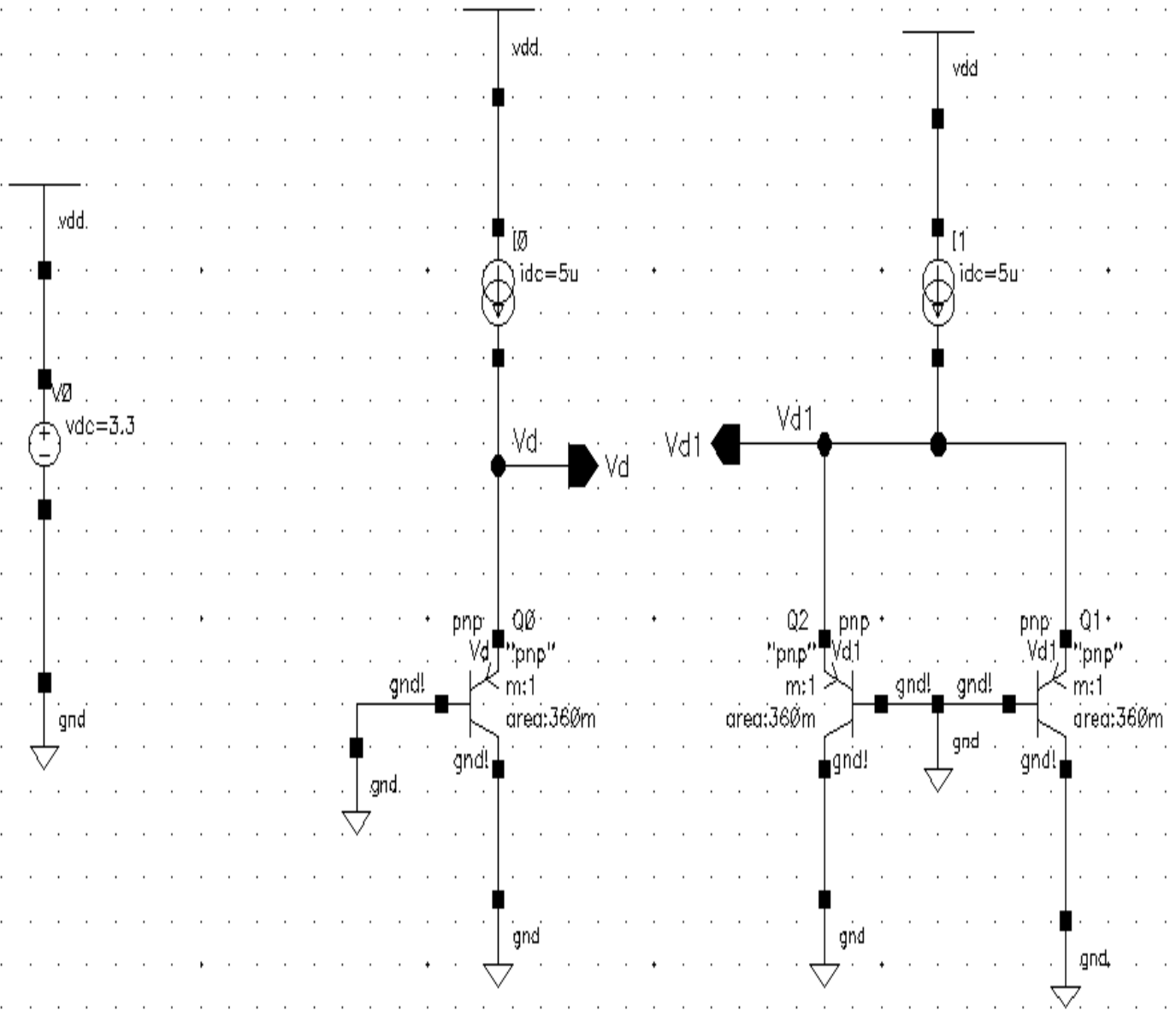


Figure 3.2 Circuit simulated in Cadence to check the nature of  $(V_d - V_{d1})$

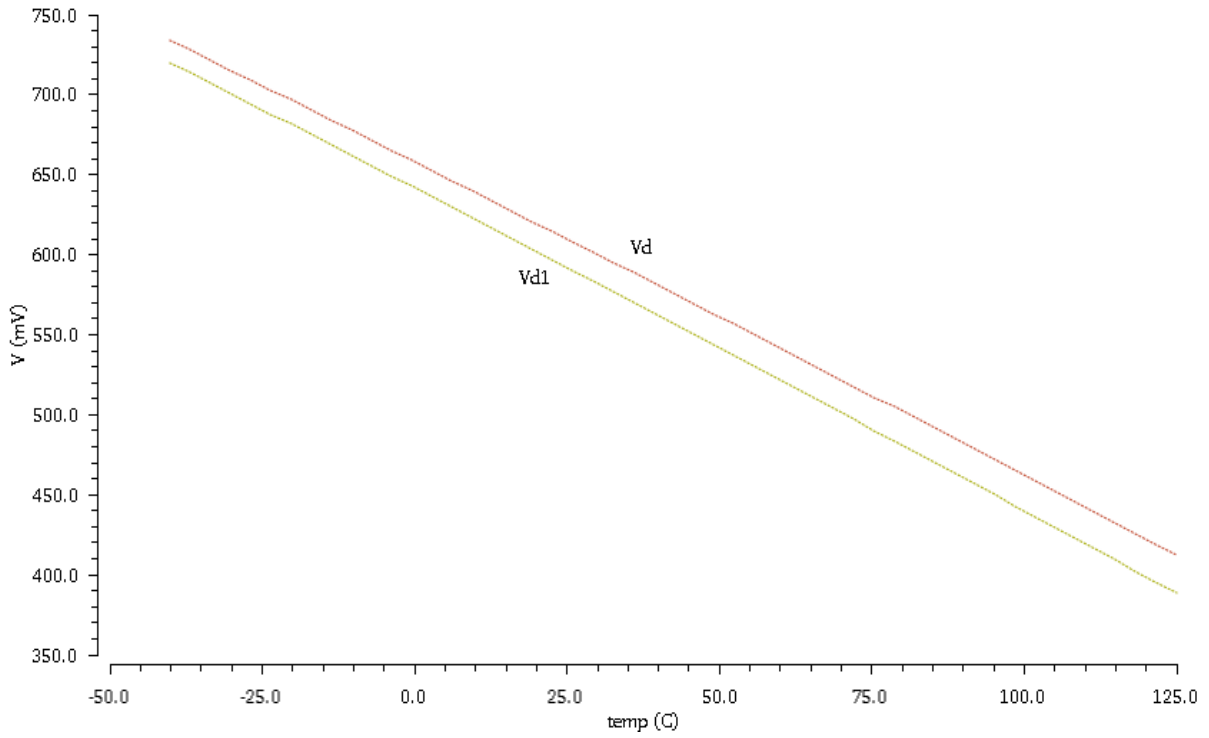


Figure 3.3 Figure showing individual nature of  $V_d$  and  $V_{d1}$

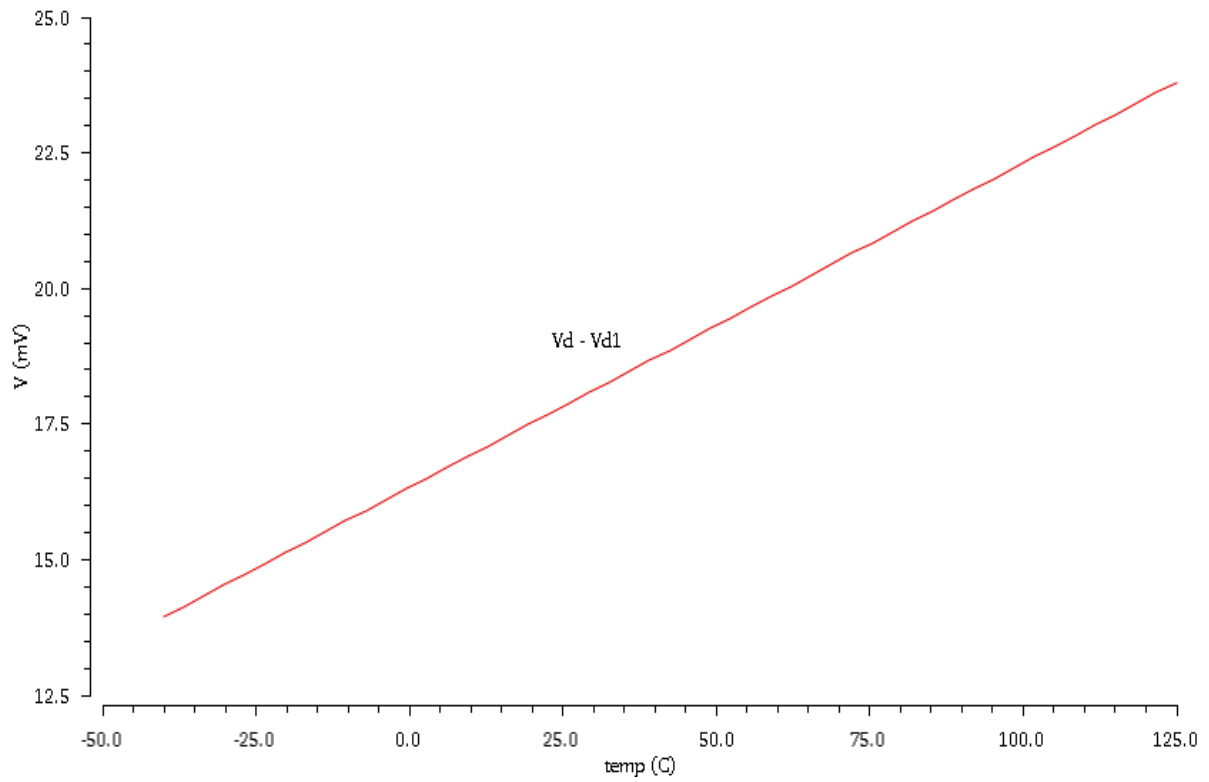
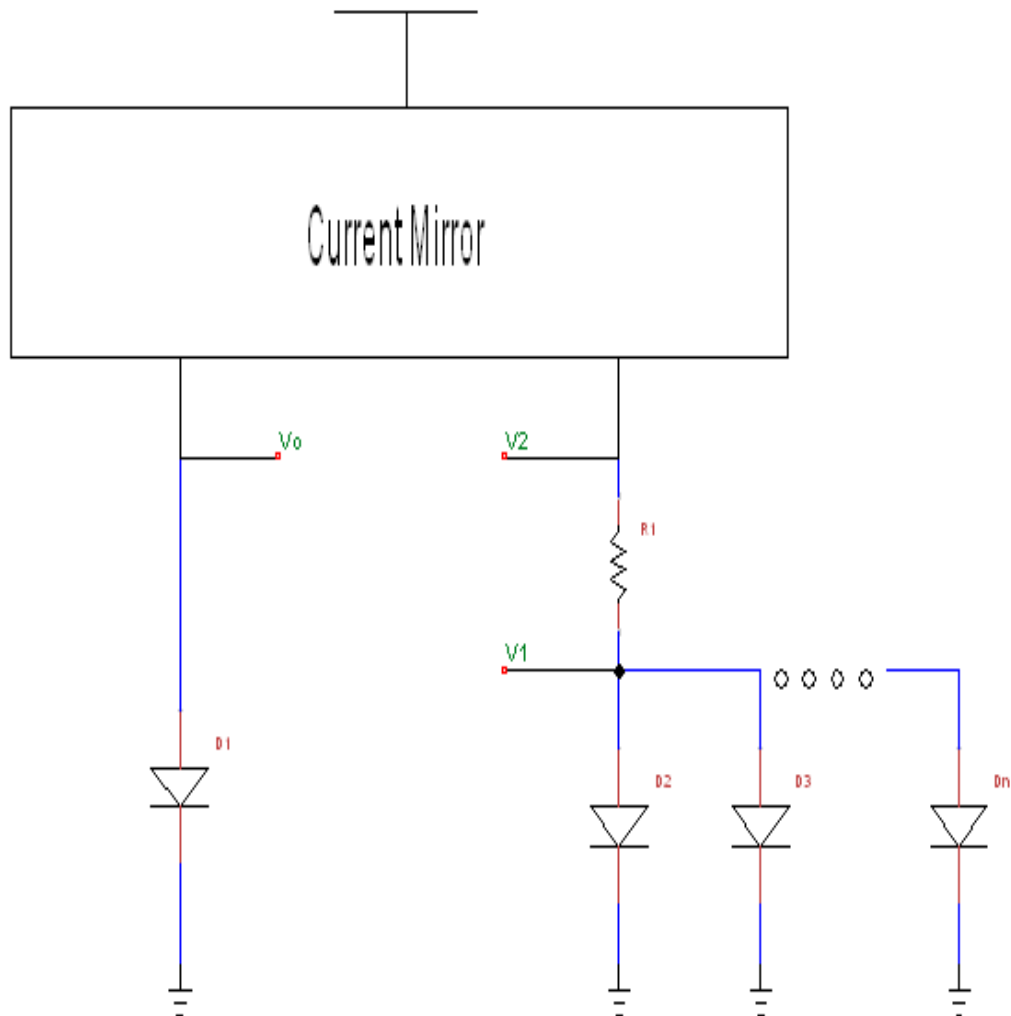


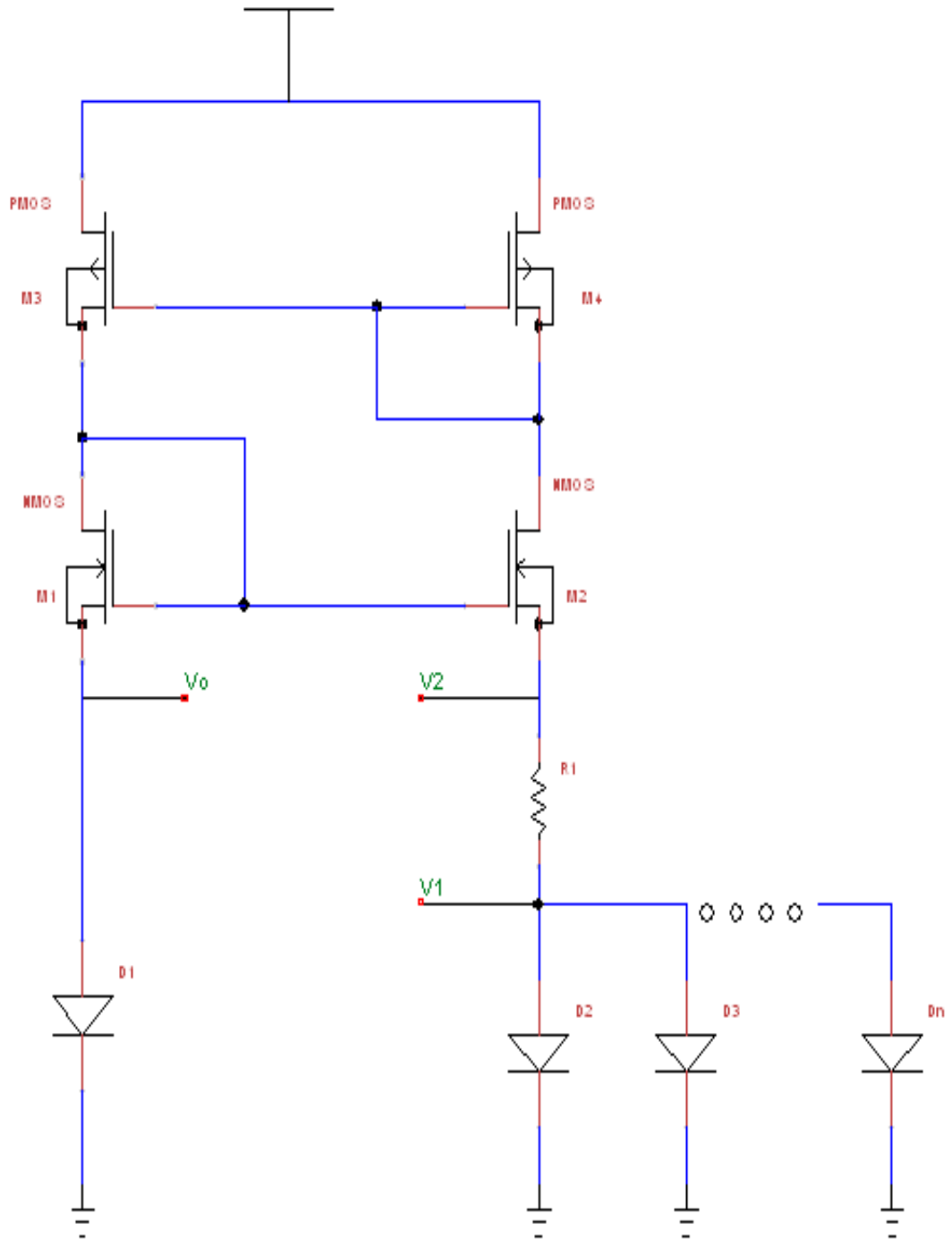
Figure 3.4 Figure showing the nature of  $V_d - V_{d1}$

We can also replace ideal constant dc current source with current mirror in order to obtain the PTAT nature.



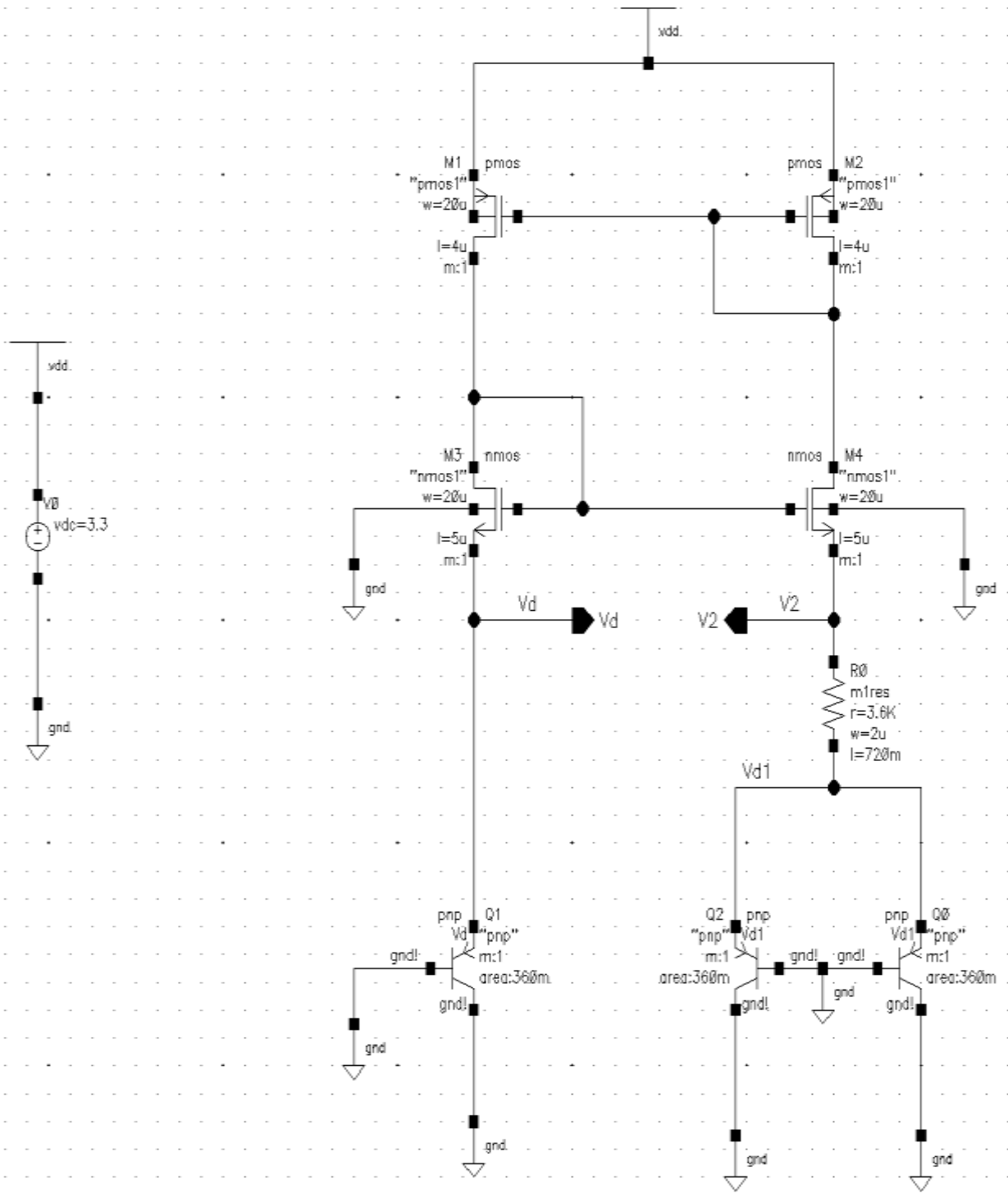
**Figure 3.5** Figure showing the replacement of the ideal current dc source with current mirror

In order to have the same current in both the branches (fig 3.2), and to get the PTAT voltage across the output voltage fig 3.2 is modified as shown in fig 3.5.



**Figure 3.6** Addition of a current Mirror in the figure 3.2

For simulation purpose we are connecting two diodes in parallel i.e taking  $n = 2$ .



**Figure 3.7** PTAT circuit with Simple current mirror drawn in cadence

In the circuit shown in Figure 3.7 the current through M3 and M4 are equal due to the presence of the current mirror across the two branches, this causes the node voltages at Vd and V2 to be equal.

$$V_d = V_2 \quad (3.3)$$

Therefore,

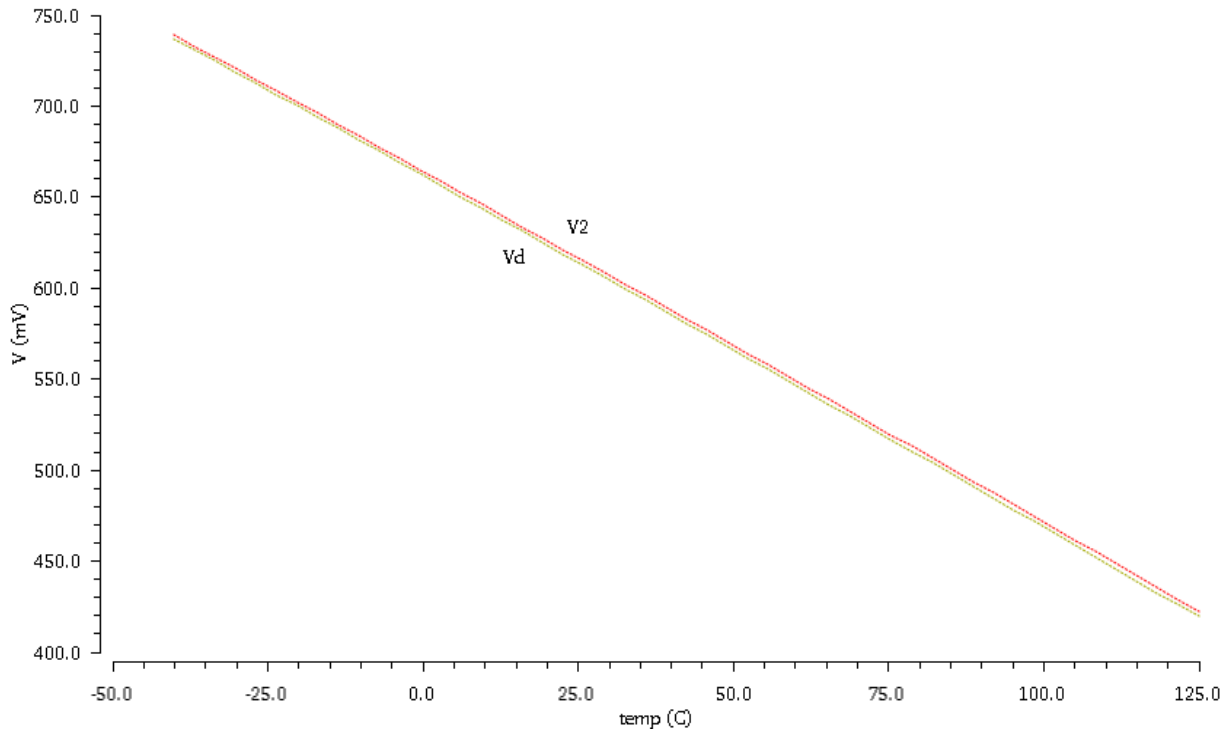
$$V_2 = I_o R + V_{d1} \quad (3.4)$$

$$I_o R = V_d - V_{d1} \quad (3.5)$$

From eq 3.2 and eq 3.5 we get,

$$I_o R = V_T \ln(n) \quad (3.6)$$

Thus eq. 3.6 shows that the voltage across the diode is a PTAT which can be verified from the figure 3.8 and figure 3.9 shown below.



**Figure 3.8** Figure showing the individual nature of the voltage across the diodes in figure 3.7

Notice the closeness of the node potentials  $V_d$  and  $V_2$  as compared to the one plotted in figure 3.3. Thus the PTAT voltage obtained in the figure 3.6 can be controlled to a higher degree of extend as compared to one obtained in figure 3.2.

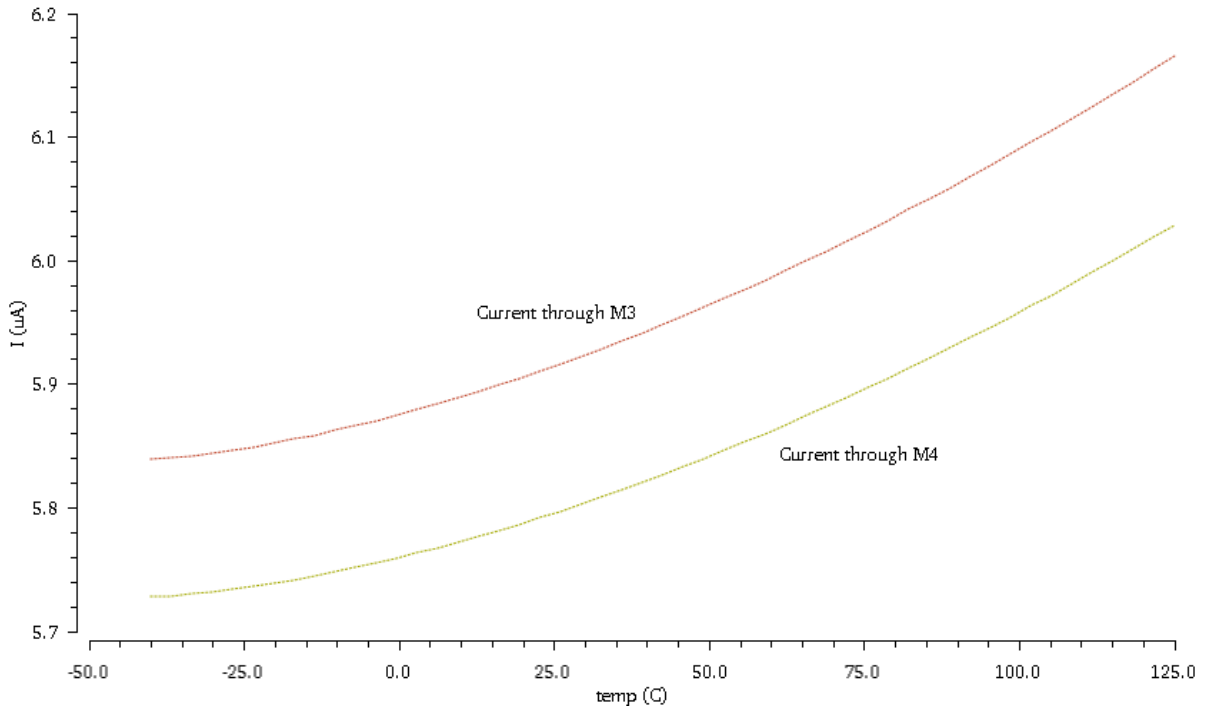


Figure 3.9 Plot showing the variation of current through M<sub>3</sub> and M<sub>4</sub> w.r.t. temperature

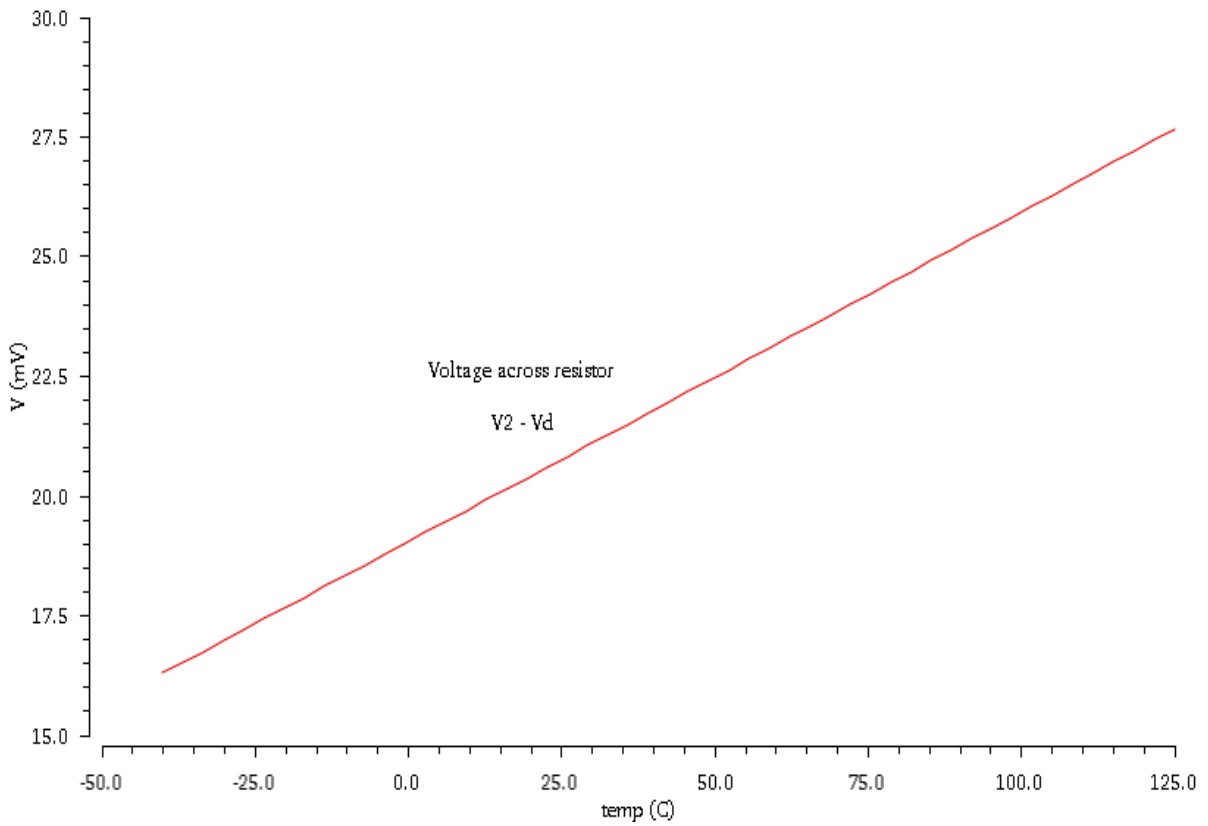


Figure 3.10 Plot showing the variation of PTAT voltage obtained in figure 3.7



### 3.3 FURTHER IMPROVEMENTS:

The disadvantage with the circuit shown in figure 3.7 is that we are obtaining the PTAT voltage across the resistor R, which is present between the diode and MOSFET. The PTAT voltage present across the resistor R can be extracted into a different branch by connecting one more gate connected MOSFET M<sub>5</sub>, since it mirrors the current I<sub>0</sub> which is flowing through M<sub>2</sub> and M<sub>1</sub> [9].

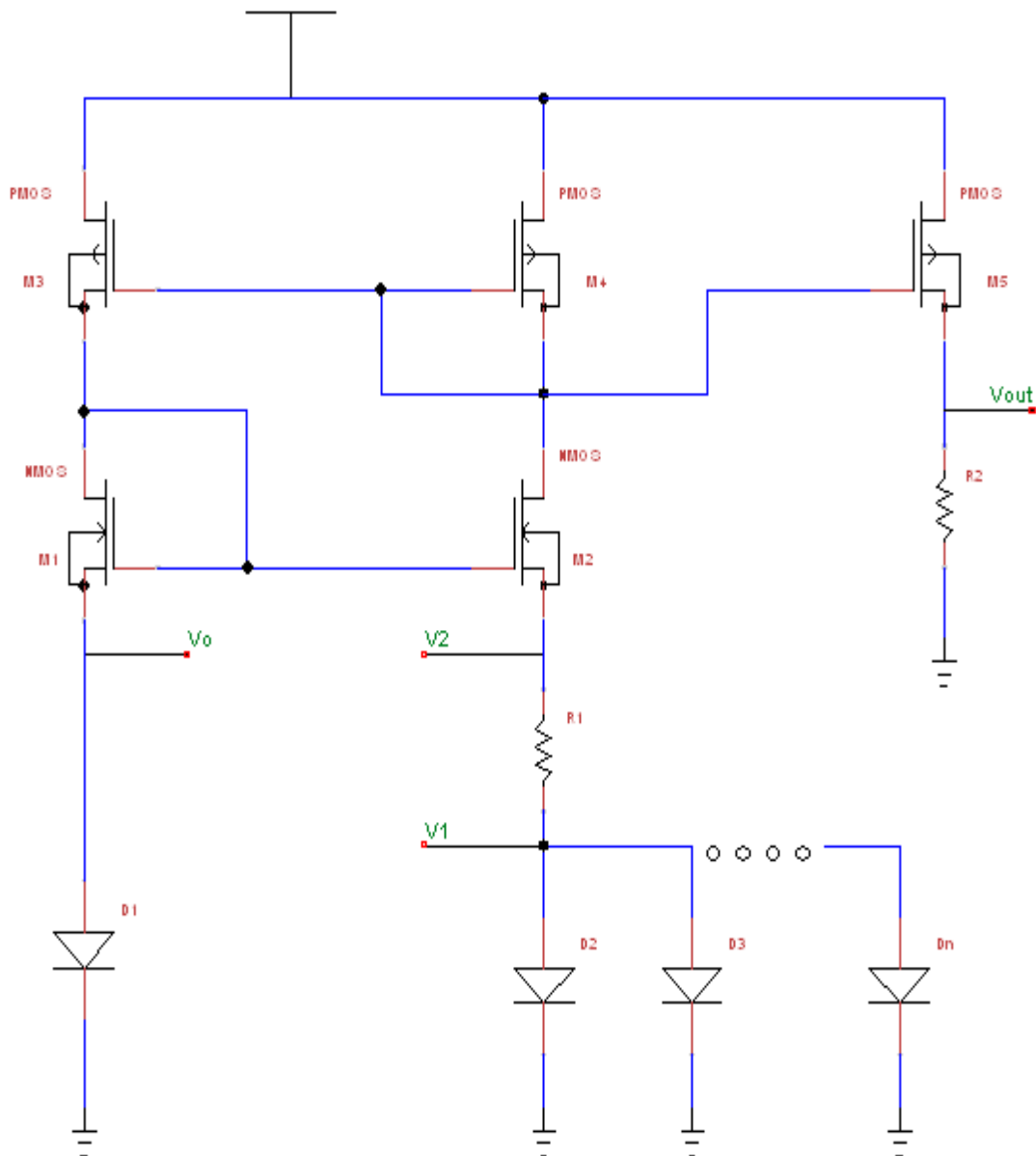


Figure 3.11 Addition of MOSFET M<sub>5</sub> in figure 3.5

The value of resistors  $R_1$  and  $R_2$  to be used for simulation purposes could be determined from equation 3.6 by putting  $I_0 = 5\mu$ ,  $V_T = 26mV$ ,  $n = 2$  which on solving we get  $R_1 = R_2 = 3.6K\Omega$ .

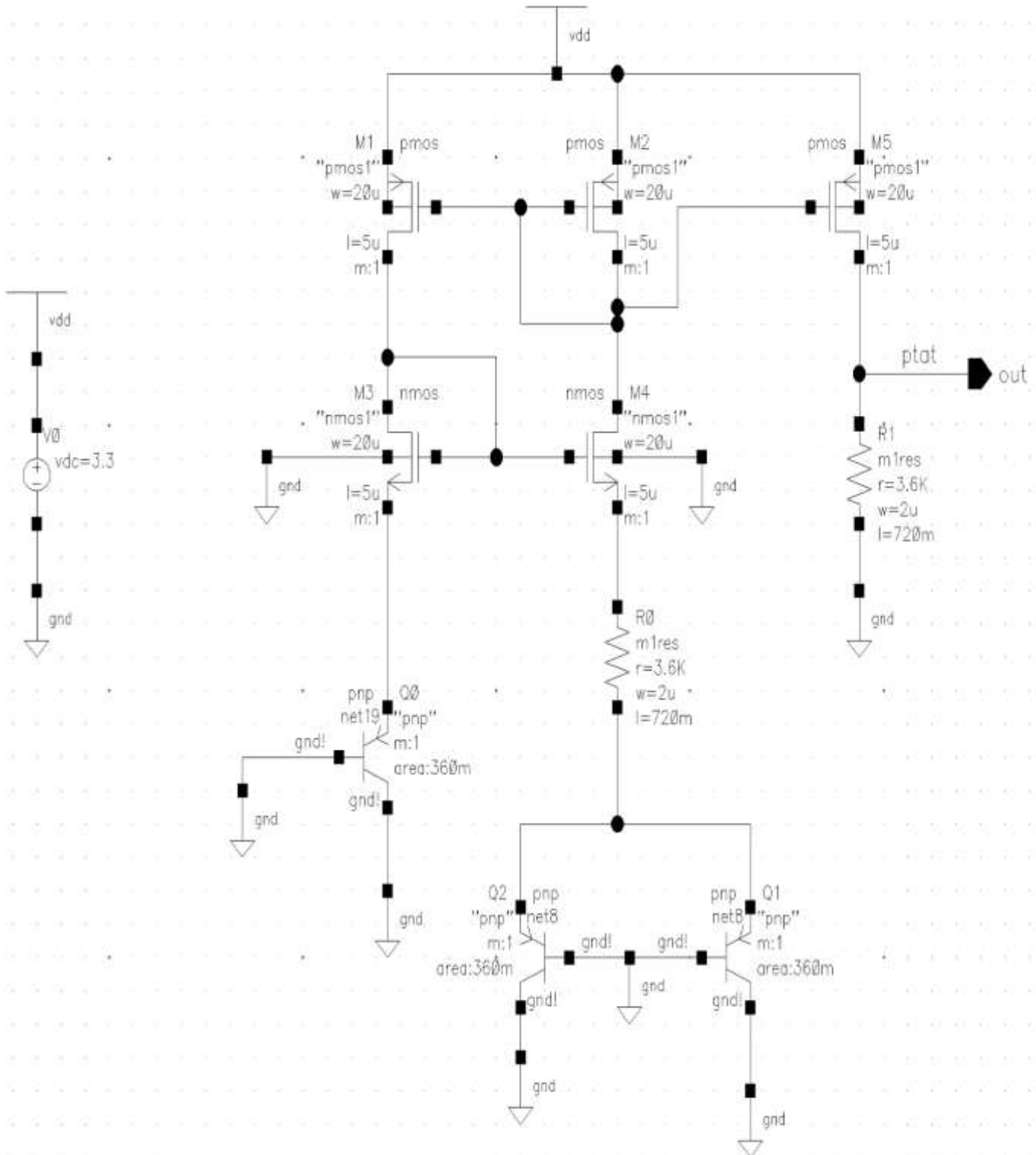


Figure 3.12 Improved PTAT circuit drawn in Cadence for analysis

1.	M1	W = 20 $\mu$ ; L = 5 $\mu$
2.	M2	W = 20 $\mu$ ; L = 5 $\mu$
3.	M3	W = 20 $\mu$ ; L = 5 $\mu$
4.	M4	W = 20 $\mu$ ; L = 5 $\mu$
5.	M5	W = 20 $\mu$ ; L = 5 $\mu$
6.	V <sub>dc</sub>	3.3 V
7.	R <sub>1</sub>	3.6K $\Omega$
8.	R <sub>2</sub>	3.6K $\Omega$

**Table 3.1** Design Parameters used in simulation of circuit in Figure 3.12

From eq. 3.6 we get,

$$I_o = \frac{V_T \ln(n)}{R_1} \quad (3.7)$$

Also,

$$V_{out} = I_o R_2 \quad (3.8)$$

Therefore,

$$V_{out} = \frac{R_2}{R_1} \ln(n) V_T \quad (3.9)$$

From the eq. 3.9 we can conclude that since the term  $\frac{R_2}{R_1} \ln(n)$  is a constant the voltage across the resistor R<sub>2</sub> is PTAT in nature.

$$\alpha_1 = \frac{R_2}{R_1} \ln(n) V_T \quad (3.10)$$

We require to scale PTAT voltage by a factor of  $\alpha_1$  since in BGR design we need to cancel our PTAT nature present in the circuit with the CTAT nature. We can control the value of  $\alpha_1$  by manipulating the values of R<sub>2</sub> and R<sub>1</sub> and thus can alter the slope of the PTAT voltage.

Also,

$$\frac{\partial V_T}{\partial T} = \frac{k}{q} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}} = 86.25 \mu V/K \quad (3.11)$$

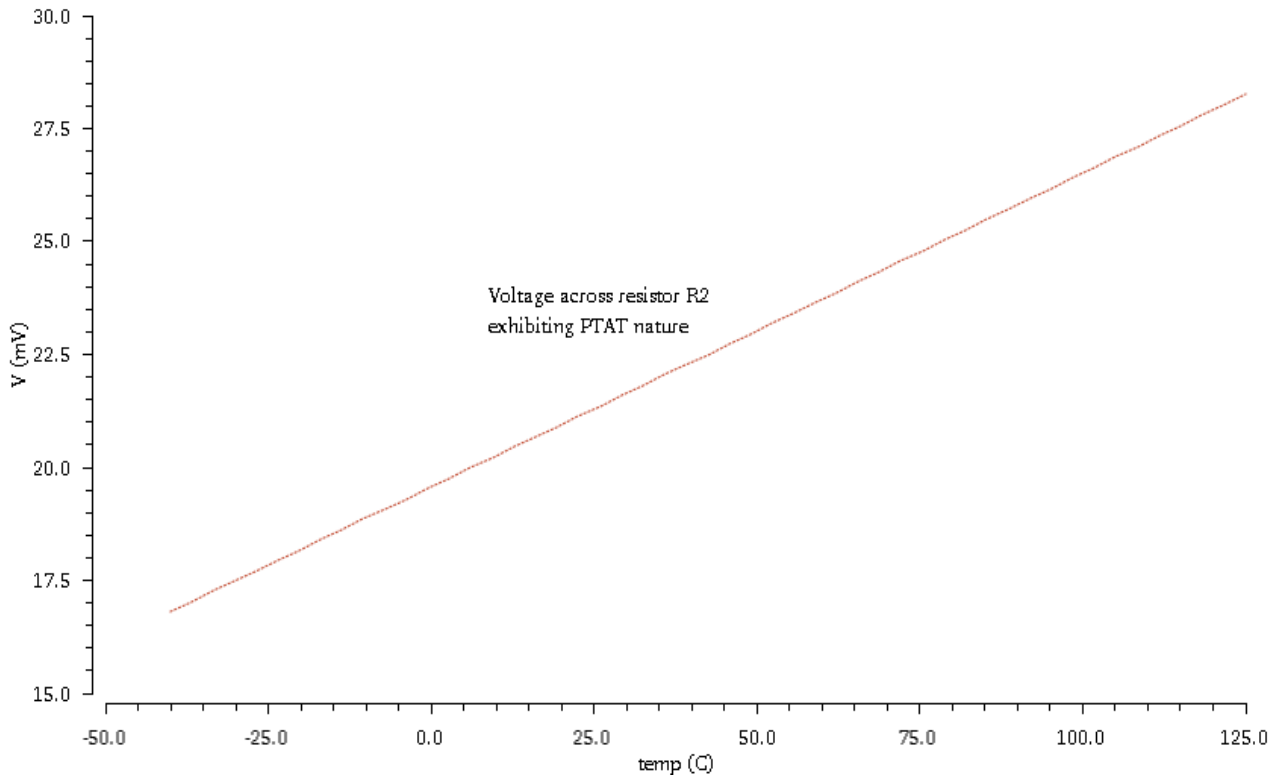


Figure 3.13 Plot showing the variations of the  $V_{out}$  w.r.t to temperature for Figure 3.12

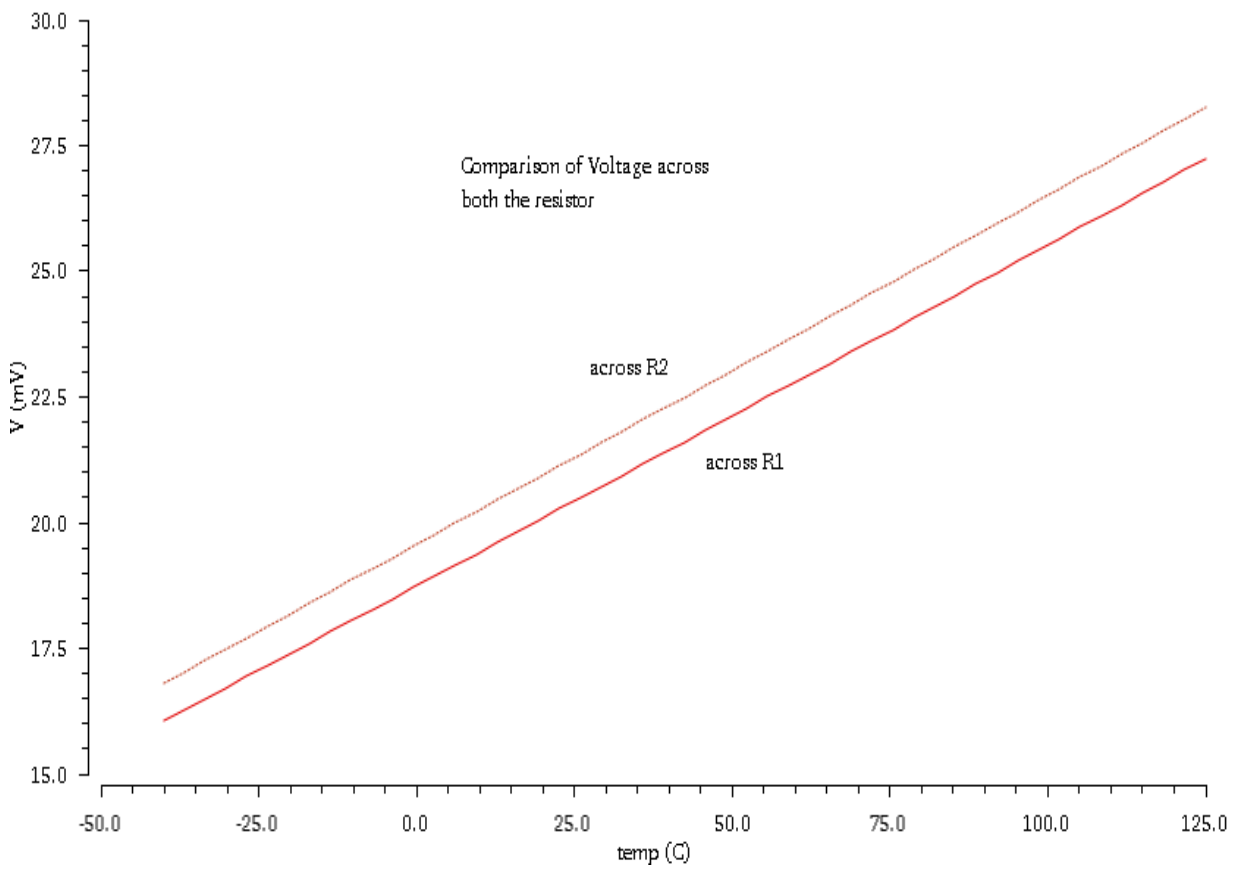


Figure 3.14 Plot showing the comparison of the voltage across R1 and R2 for Figure 3.12

The PTAT design discussed in this chapter can also be achieved by using an op-amp in place of a current mirror which is discussed in the final chapter Future Scope and Work.

Comparing the voltage across the resistors  $R_1$  and  $R_2$  we can notice that they are almost equal, although there is some difference observed due to the divergence of current mirror from its ideal behaviour.

In order to reduce the voltage difference between two resistors observed in Figure 3.14 we can replace the simple current mirror present in Figure 3.12 with a cascode current mirror or any of the other advanced current mirror.

### **3.4 CONCLUSIONS:**

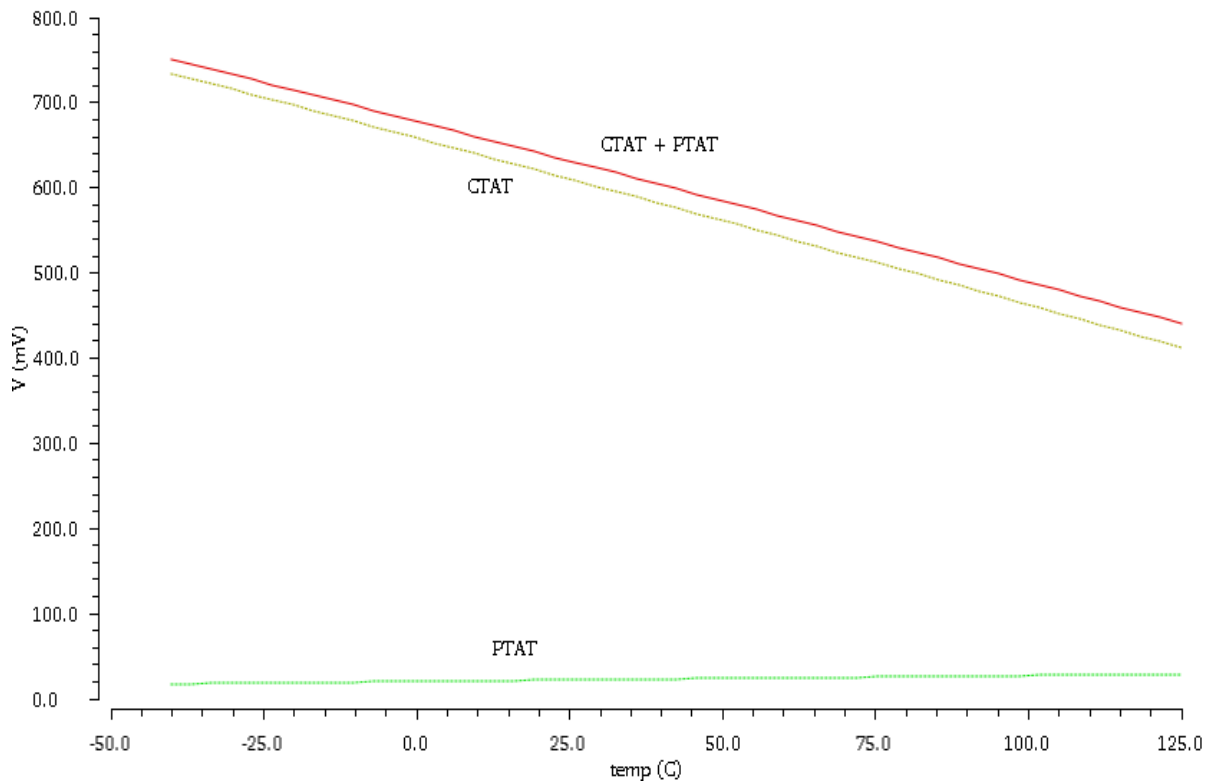
In this chapter we discussed the design and analysis of PTAT (Proportional to absolute temperature) circuits. We conclude in this chapter that the voltage across two diodes is PTAT in nature. We later discussed the improvement in the circuit by adding gate connected PMOS.

## CHAPTER – 4

# **ADDING CTAT and PTAT**



The combined simulation of both the CTAT and PTAT circuit above is done to find the dominating nature among both of them [6].



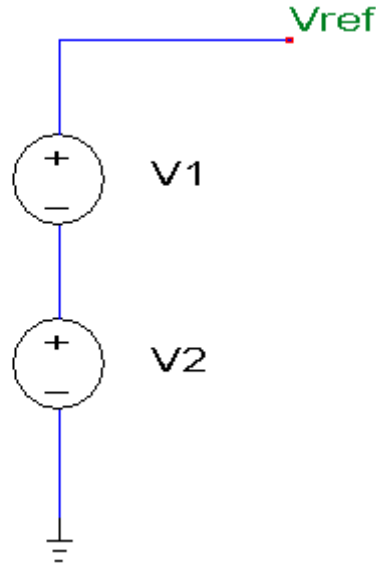
**Figure 4.2** Result of the simulation of the circuit shown in figure 4.1

From the figure 4.1, we can observe that the slope of the PTAT curve i.e.  $\frac{\partial V_{PTAT}}{\partial T}$  is insignificant as compared to the slope of the CTAT curve  $\frac{\partial V_{CTAT}}{\partial T}$ , thus the overall nature of the CTAT and PTAT curve is also CTAT.

Therefore, we need to calibrate the values of  $\alpha_1$  and  $\alpha_2$  which are the coefficients of the slope of the CTAT and PTAT curve such that after combining both the circuits we get a reference voltage independent of the temperature.

In earlier chapters while designing the circuits we took the assumption that  $I_o$  current is constant in nature when it flows through CTAT circuit. But when we add the CTAT and PTAT circuits as shown in figure 2.3, and by eq. 3.7 we can conclude that  $I_o$  is not constant in nature.





**Figure 4.3** Figure showing  $V_1$  as PTAT and  $V_2$  as CTAT connected in series

Therefore, taking the partial derivative w.r.t Temperature  $T$  from eq. 2.2 we get

$$\frac{\partial V_D}{\partial T} = \frac{\partial}{\partial T} \left[ V_T \ln \frac{I_0}{I_s} \right] \quad (4.1)$$

$$= \frac{\partial V_T}{\partial T} [\ln I_0 - \ln I_s] + V_T \left[ \frac{1}{I_0} \cdot \frac{\partial I_0}{\partial T} - \frac{1}{I_s} \cdot \frac{\partial I_s}{\partial T} \right] \quad (4.2)$$

$$\frac{\partial I_0}{\partial T} = \frac{I_0}{T} \quad (4.3)$$

Substituting values from eq. 2.2, eq. 2.5 and eq. 4.5, we get

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (3 + m) - \varepsilon_g/q}{T} \quad (4.4)$$

Substituting standard values in eq. 4.4, we get

$$\frac{\partial V_D}{\partial T} = -1.79 \text{ mV/K} \quad (4.5)$$

By comparing the result obtained in eq. 4.5 and eq. 2.16 we can conclude that the dependence of  $I_0$  on temperature is not significant and we can continue to ignore the effects on temperature on  $I_0$ , since it is miniscule for all practical purposes.

## 4.2 DESIGN OF $\alpha_1$ AND $\alpha_2$ :

Taking the derivative of eq. 1.2 we get,

$$\frac{\partial V_{Ref}}{\partial T} = \alpha_1 \frac{\partial V_{CTAT}}{\partial T} + \alpha_2 \frac{\partial V_{PTAT}}{\partial T} = 0 \quad (4.6)$$

Putting in values from eq. 4.5 and 3.11 in eq. 4.6

$$\alpha_1 \{86.25 \mu V/K\} + \alpha_2 \{-1.79 mV/K\} = 0 \quad (4.7)$$

To decrease the CTAT voltage we need to connect a large number of diodes in parallel which is not a practical solution. Therefore, we keep  $\alpha_2 = 1$  and adjust the value of  $\alpha_1$

Therefore,

$$\alpha_1 = 20.75 \quad (4.8)$$

Calculating the value of  $V_{Ref}$  from eq. 1.2 we get,

$$V_{Ref} = 1.2 V \quad (4.9)$$

From eq. 3.7 we can find the value of  $R_1$  to be equal to

$$R_1 = 3.6 K\Omega \quad (4.10)$$

From eq. 3.10 we can find the value of  $R_2$  to be equal to

$$R_2 = 101.5 K\Omega \quad (4.11)$$

4.3 SIMULATION RESULTS:

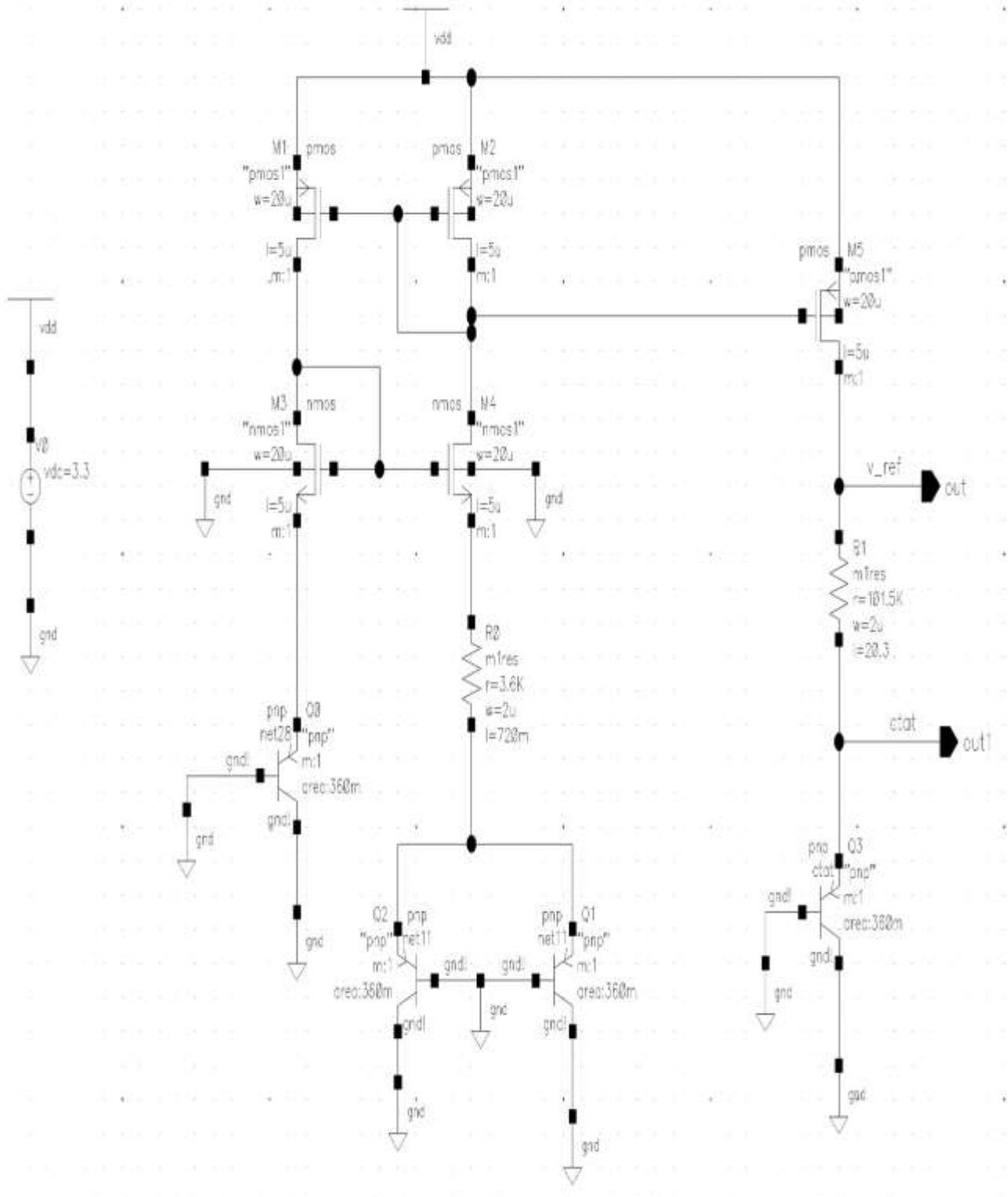
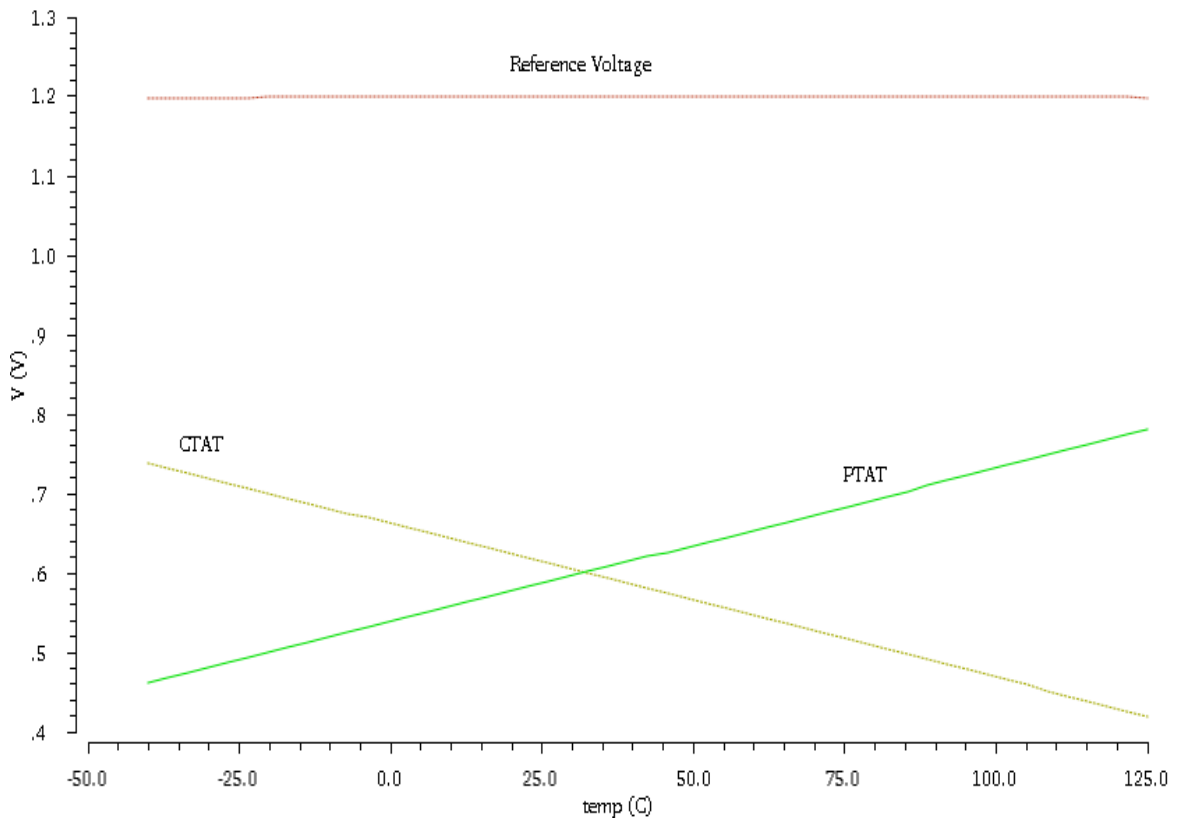


Figure 4.4 Figure showing simulation of BGR circuit with parameters calculated in table 4.1

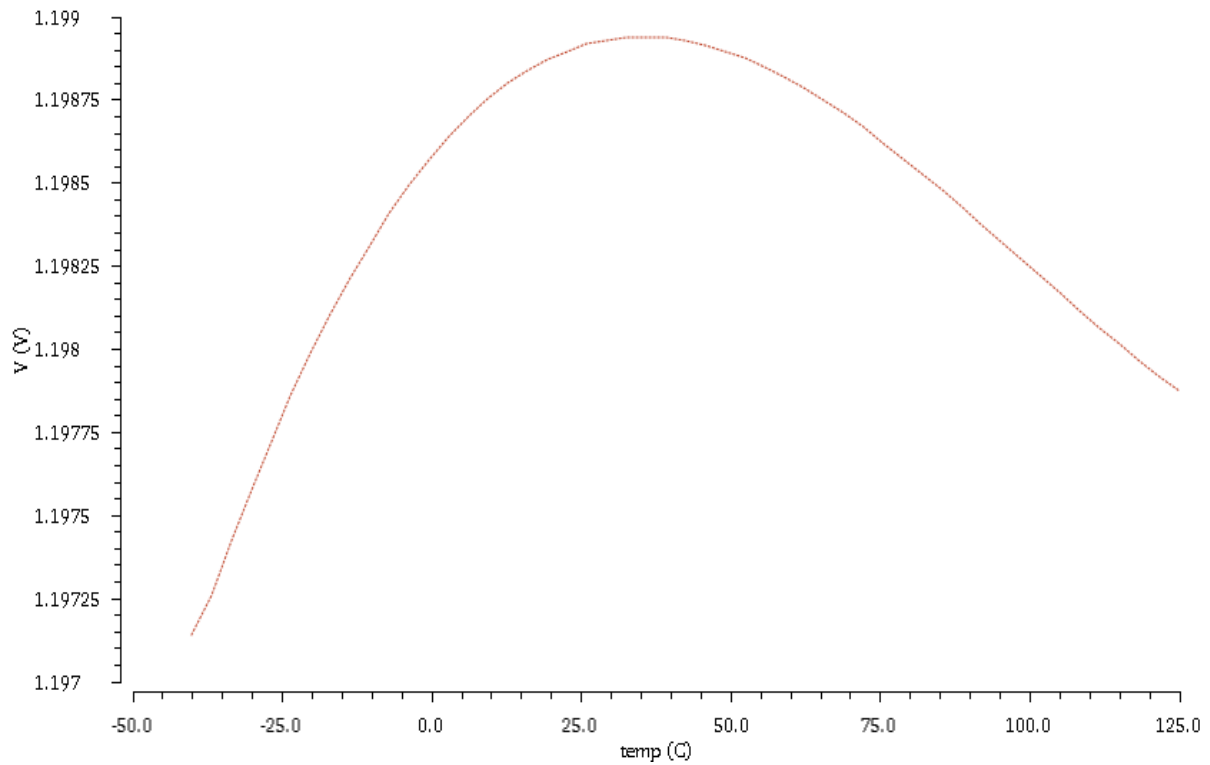
1.	$R_1$	101.5 K $\Omega$
2.	$R_2$	3.6 K $\Omega$
3.	$V_{dc}$	3.3 V
4.	$\alpha_1$	20.75
5.	$\alpha_2$	1
6.	$M_1$	$W = 20 \mu$ ; $L = 5 \mu$
7.	$M_2$	$W = 20 \mu$ ; $L = 5 \mu$
8.	$M_3$	$W = 20 \mu$ ; $L = 5 \mu$
9.	$M_4$	$W = 20 \mu$ ; $L = 5 \mu$
10.	$M_5$	$W = 20 \mu$ ; $L = 5 \mu$

**Table 4.1** Design Parameters used in simulation of circuit in Figure 4.4



**Figure 4.5** Figure showing variation in output voltage ( $V_{ref}$ ) w.r.t temperature (T)

From figure 4.5 we can notice that the  $V_{ref}$  voltage shows an approximated straight-line w.r.t to temperature  $T$  which is basically a combined result of CTAT and PTAT nature of voltages obtained in figure 4.4.



**Figure 4.6** Figure showing that the  $V_{ref}$  is actually a bell-shaped curve as opposed to straight line

We are getting the bell-shaped curve because the CTAT and PTAT curves were not exactly a straight line. However, we did the mathematical analysis assuming that they are straight lines [12].

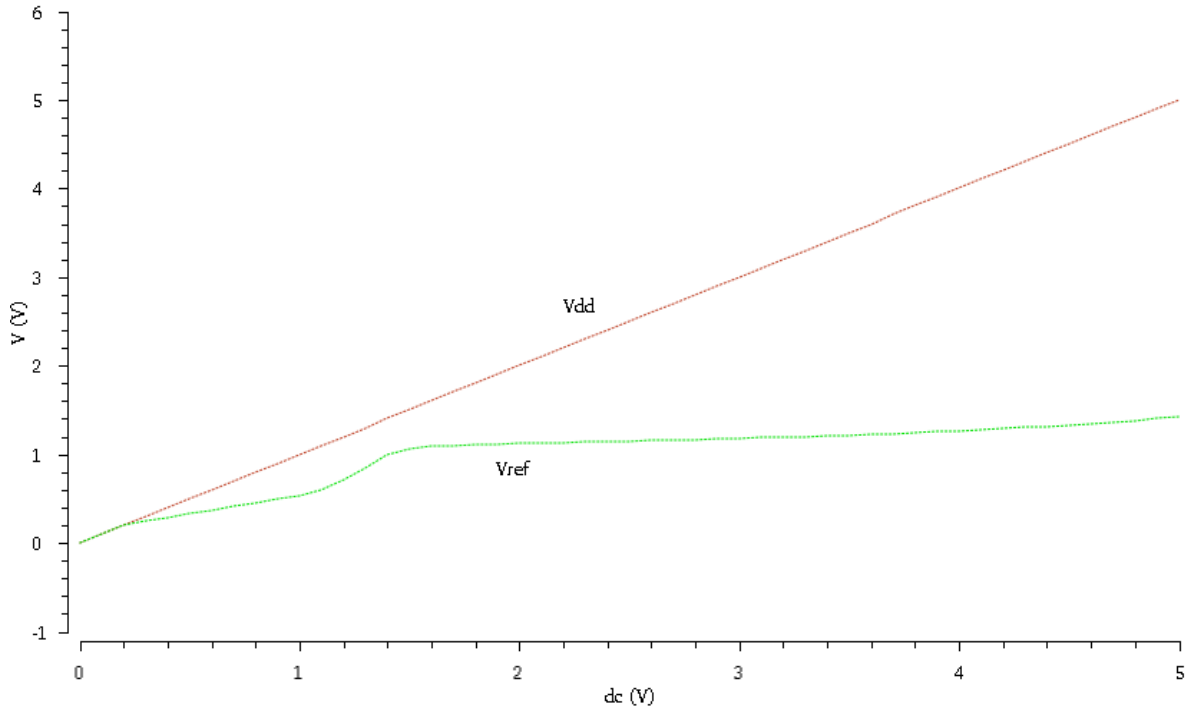


Figure 4.7 Figure showing variations in reference voltage (Vref) w.r.t supply voltage ( $V_{dd}$ ) 0 – 5 V

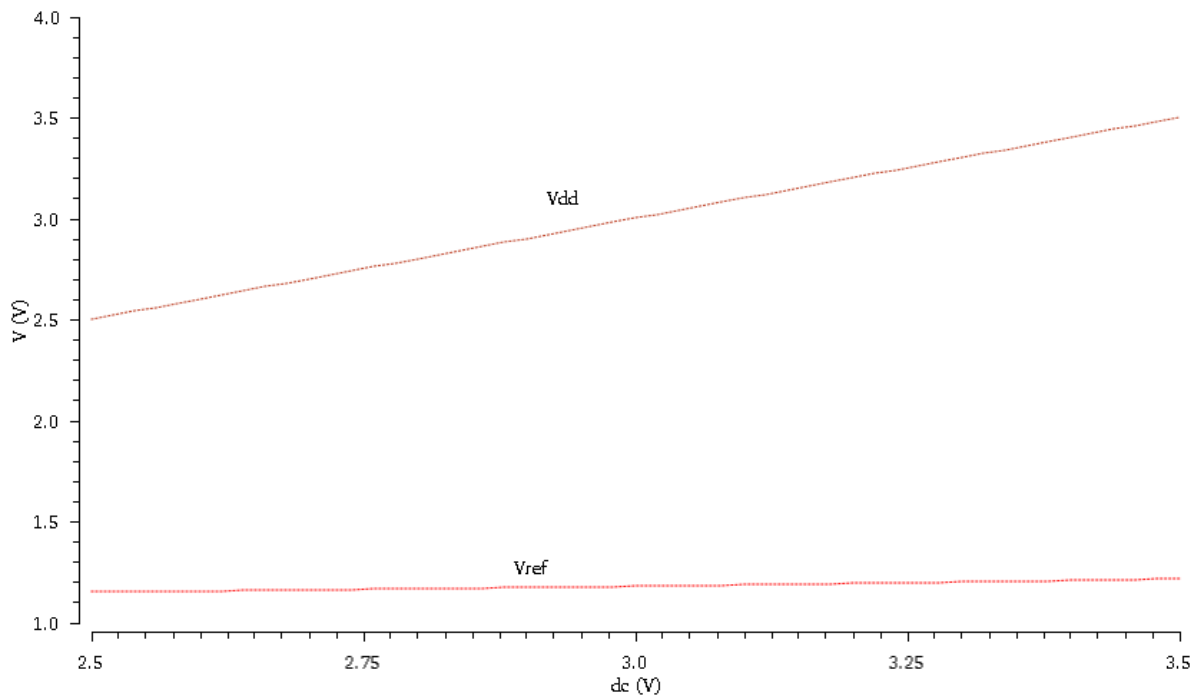


Figure 4.8 Figure showing variations in reference voltage (Vref) w.r.t supply voltage ( $V_{dd}$ ) 2.5 – 3.5 V

Figure 4.7 shows the variation in  $V_{ref}$  voltage for circuit simulated in figure 4.4 w.r.t to supply voltage ( $V_{dd}$ ) over the range of 0 – 5 V.

In practical circuits we do not expect such large variations in supply voltage, typically a 10% variation in supply voltage is expected in practical situations. Hence the variation of 2.5 – 3.5 V is simulated in Figure 4.8.

#### **4.4 CONCLUSIONS:**

In this chapter we combined the circuits designed in chapter 2 (CTAT) with the one designed in chapter 3 (PTAT). Later we calculated the scaling factors in order to combine two circuits in a way such that the output voltage ( $V_{ref}$ ) is constant w.r.t temperature (-40 to 125 degrees Celsius).

## CHAPTER – 5

# **Analysing BGR with Cascode** **Current Mirror**



## 5.1 INTRODUCTION:

As discussed in earlier chapters we know that the current mirror is responsible for the supply rejection in the band gap reference circuit so far discussed. So, if we want better supply rejection we have to improve our current mirror.

We can replace the simple current mirror present in BGR circuit with a cascode current mirror to improve supply rejection [11].

Typically, a variation in supply from 0 – 5 V will never occur in the circuit. Therefore, if our supply voltage is of 3.3 V we can expect a variation of 3 – 3.6 V.

Also, the supply voltage requirement in cascode structure is higher than the simple current mirror because of the  $V_{ds}$  drop across four MOSFETs.

The main advantages of a cascode current mirror as compared to a simple current mirror are:

- It suppresses the effect of channel length modulation.
- It increases the output impedance of current source/sink.

1.	$R_1$	117 K $\Omega$
2.	$R_2$	3.6 K $\Omega$
3.	$V_{dc}$	3.3 V
4.	$M_1$	$W = 20 \mu$ ; $L = 5 \mu$
5.	$M_2$	$W = 20 \mu$ ; $L = 5 \mu$
6.	$M_3$	$W = 20 \mu$ ; $L = 5 \mu$
7.	$M_4$	$W = 20 \mu$ ; $L = 5 \mu$
8.	$M_5$	$W = 20 \mu$ ; $L = 5 \mu$
9.	$NM_0$	$W = 20 \mu$ ; $L = 5 \mu$
10.	$NM_1$	$W = 20 \mu$ ; $L = 5 \mu$
11.	$PM_0$	$W = 20 \mu$ ; $L = 5 \mu$
12.	$PM_1$	$W = 20 \mu$ ; $L = 5 \mu$
13.	$PM_2$	$W = 20 \mu$ ; $L = 5 \mu$

**Table 5.1** Design Parameters used in simulation of circuit in Figure 5.1

## 5.2 SIMULATION RESULTS:

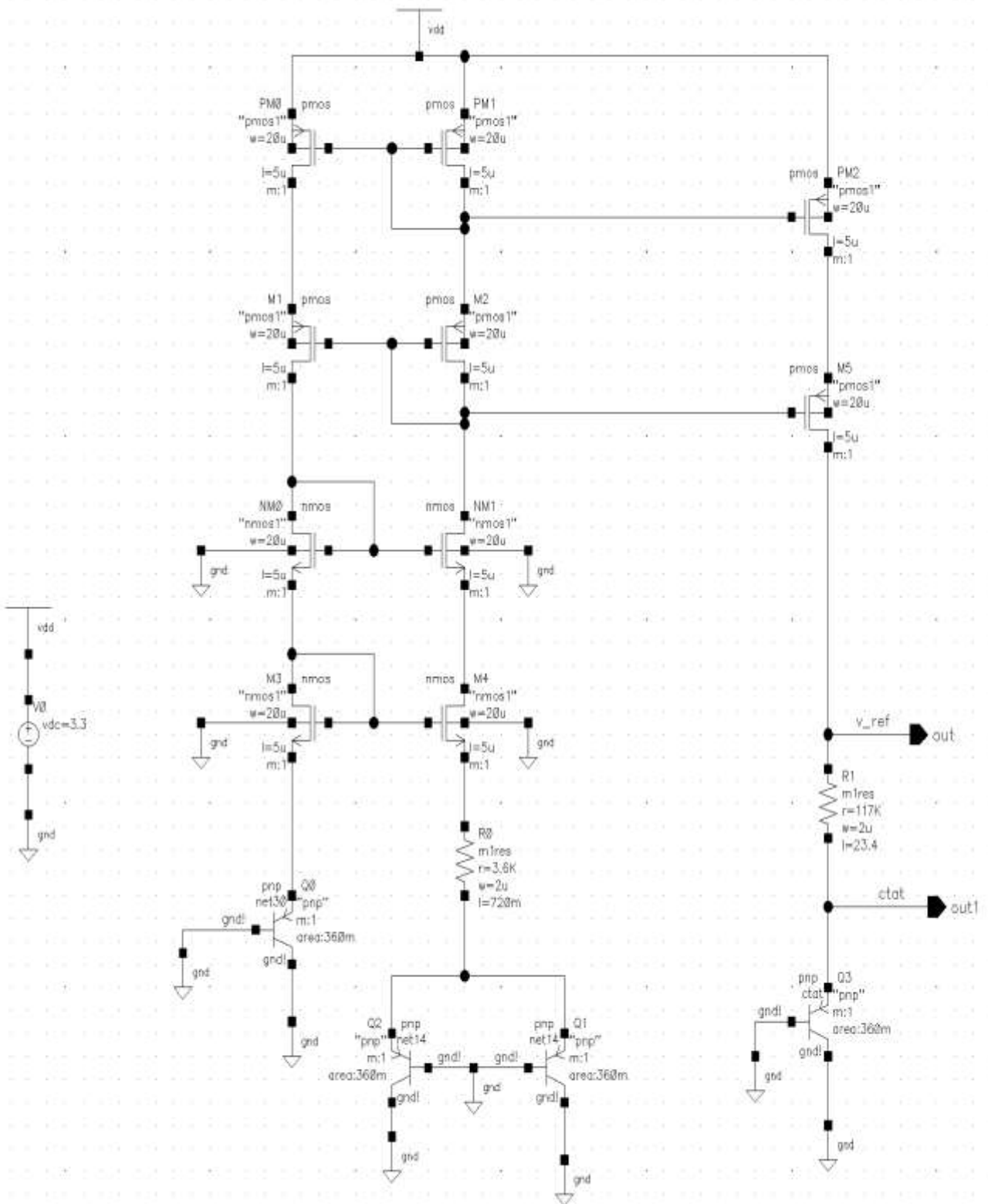


Figure 5.1 Figure showing band gap reference with cascode current mirror for better supply rejection

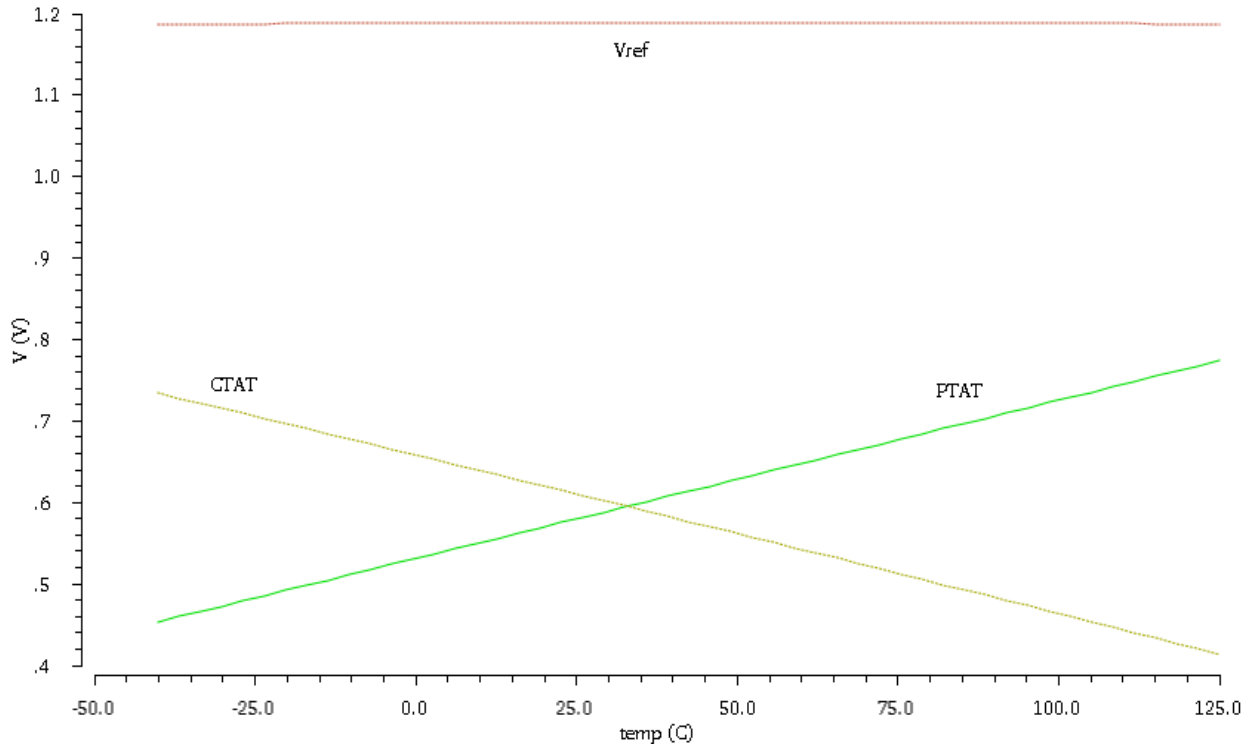


Figure 5.2 Figure showing variations in reference voltage ( $V_{ref}$ ) w.r.t Temperature for figure 5.1

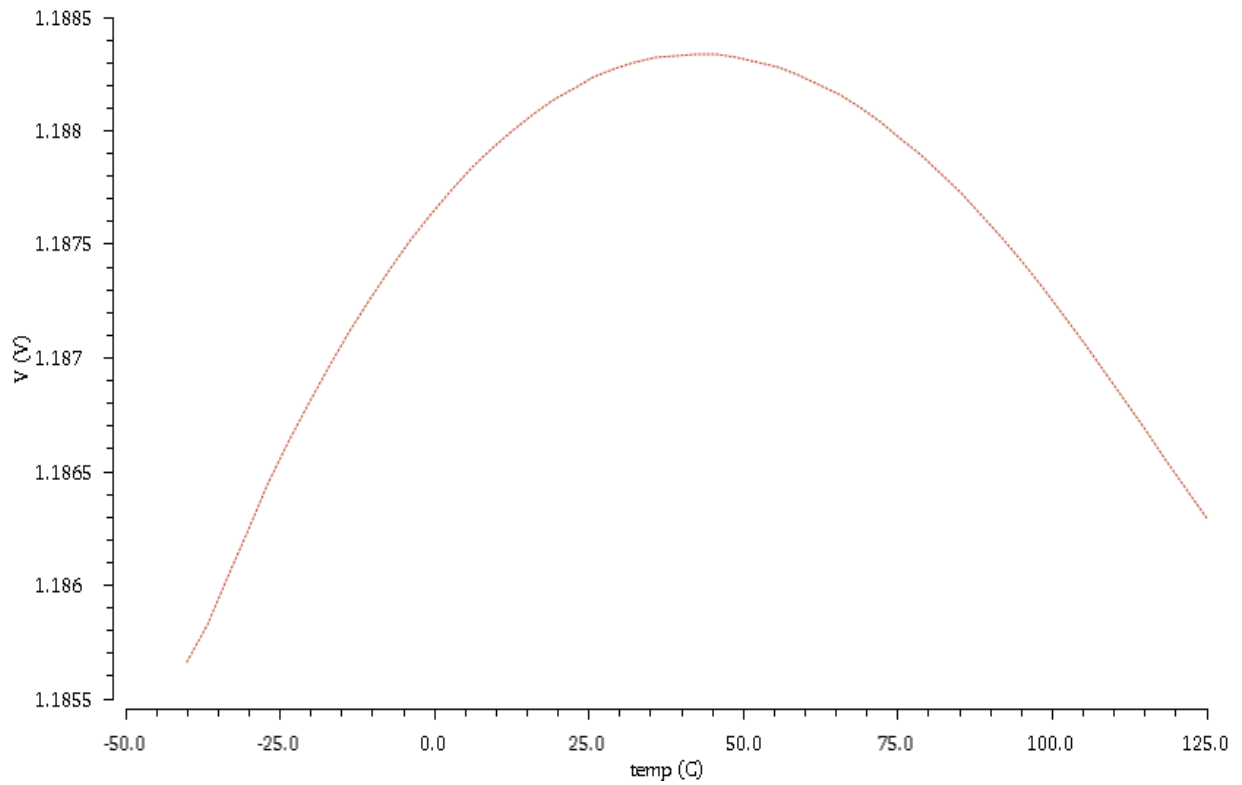


Figure 5.3 Figure showing variations in reference voltage ( $V_{ref}$ ) w.r.t supply voltage ( $V_{dd}$ ) 2.5 – 3.5 V

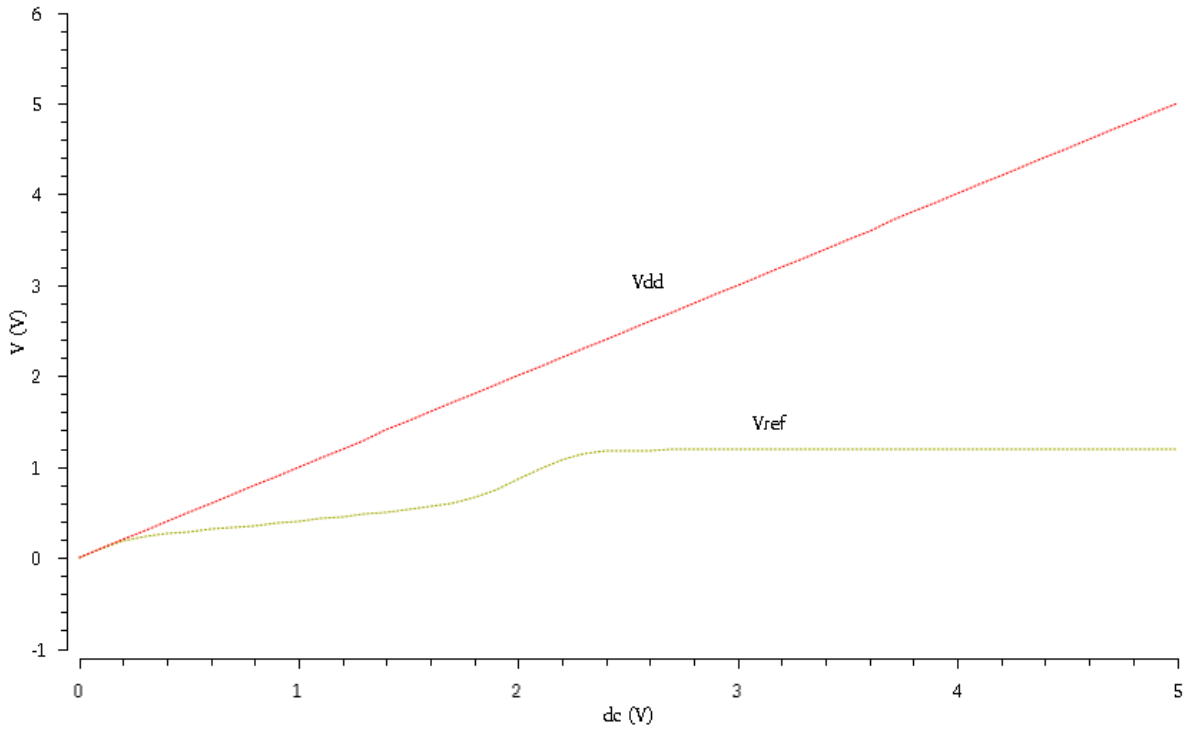


Figure 5.4 Figure showing variations in reference voltage(V<sub>ref</sub>) w.r.t supply voltage( V<sub>dd</sub>) 2.5 – 3.5 V

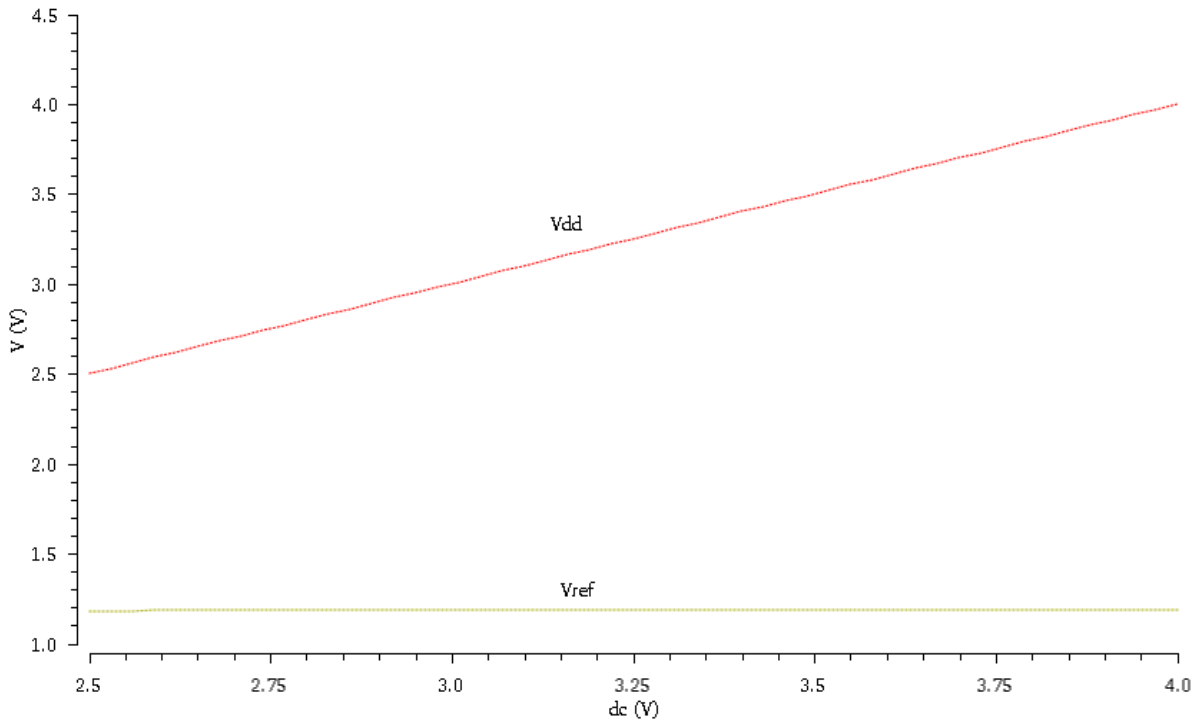


Figure 5.5 Figure showing variations in reference voltage(V<sub>ref</sub>) w.r.t supply voltage( V<sub>dd</sub>) 2.5 – 3.5 V

### **5.3 CONCLUSIONS:**

In this chapter we simulated the band gap reference circuit by replacing the current mirror component with the cascode current mirror. We conclude in this chapter that addition of cascode current mirror provides better supply rejection as compared to a simple current mirror. In the end we also simulated the dc analysis of a band gap reference circuit with a cascode current mirror.

## CHAPTER – 6

### **Start-up Circuits**

## 6.1 INTRODUCTION:

Band gap reference is a self-bias circuit and any self-bias circuit requires a start-up circuit. The band gap reference circuit has two stable regions of operation.

- Normal operating region
- Zero current region

Once the circuit enters the zero current region it will remain in that region forever since it is a stable region and we will not get  $V_{ref}$  at the output.

The function of start-up circuit is to disturb the band gap reference circuit from the zero current region so that it can enter Normal operating region.

While doing dc analysis we will not face this issue, but while doing the transient analysis we can come across this issue of band gap reference circuit getting into its zero-current region, hence we must design a start-up circuit for our band gap reference circuit before performing its transient analysis.

It is hard to detect the necessity of a start-up circuits in the simulation because most simulators like cadence will avoid the zero current state and when we do the analysis everything seems to be fine. But it doesn't guarantee that the circuit will work.

Therefore, even though we cannot see the necessity of start-up circuit in the simulation we should design the start-up circuit for every self-biased circuit such as band gap reference circuit.

To analyse the necessity of start-up circuits we must perform the transient analysis since dc analysis doesn't prove to be of much help in such case scenarios.

If  $V_1$  (node between  $M_3$  and  $M_4$ ) equals to 0 and  $V_2$  (node between  $M_1$  and  $M_2$ ) equals to  $V_{dd}$  then there is no current flow through band gap reference circuit, therefore the functionality of start-up circuit in our case is that it decreases the  $V_2$  and increases  $V_1$  forcefully [5][6].

An NMOS is connected to node  $V_1$  to bring down the voltage of Node  $V_1$  when the BGR is in Zero current state, we want to turn on the NMOS  $N_1$  in order to forcefully pull down the node voltage  $V_1$  this will bring the BGR circuit in Normal region. Once the circuit is in normal operating region we would want to turn-off the NMOS  $N_1$  otherwise the circuit functionality will be disturbed and we will not get good stable state.

1.	$R_1$	101.5 K $\Omega$
2.	$R_2$	3.6 K $\Omega$
3.	$R_0$	10 K $\Omega$
4.	$V_{dc}$	3.3 V
5.	$M_1$	$W = 20 \mu$ ; $L = 5 \mu$
6.	$M_2$	$W = 20 \mu$ ; $L = 5 \mu$
7.	$M_3$	$W = 20 \mu$ ; $L = 5 \mu$
8.	$M_4$	$W = 20 \mu$ ; $L = 5 \mu$
9.	$M_5$	$W = 20 \mu$ ; $L = 5 \mu$
10.	$NM_0$	$W = 2 \mu$ ; $L = 500 \text{ n}$
11.	$NM_1$	$W = 10 \mu$ ; $L = 500 \text{ n}$

**Table 6.1** Design Parameters used in simulation of circuit in Figure 6.1

1.	$V_{pulse}$	0 – 3.3 V
2.	period	1 s
3.	Delay Time	100 $\mu\text{s}$
4.	Rise Time	100 $\mu\text{s}$
5.	Pulse width	0.5 s

**Table 6.2** Parameters for transient analysis used in simulation of circuit in Figure 6.1



### 6.2 SIMULTAION RESULTS:

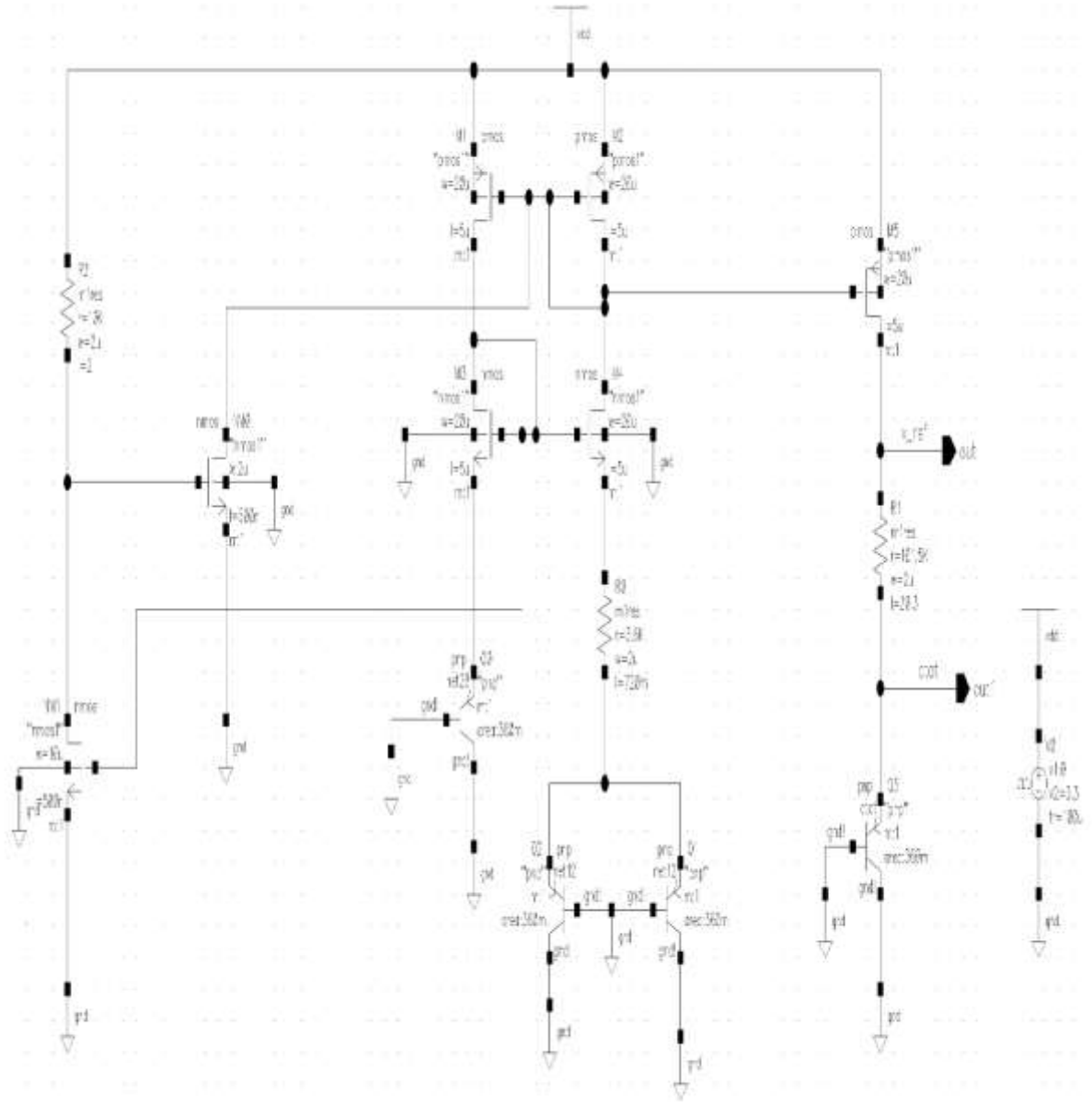


Figure 6.1 Figure showing a simulation of band gap reference circuit with start-up circuit

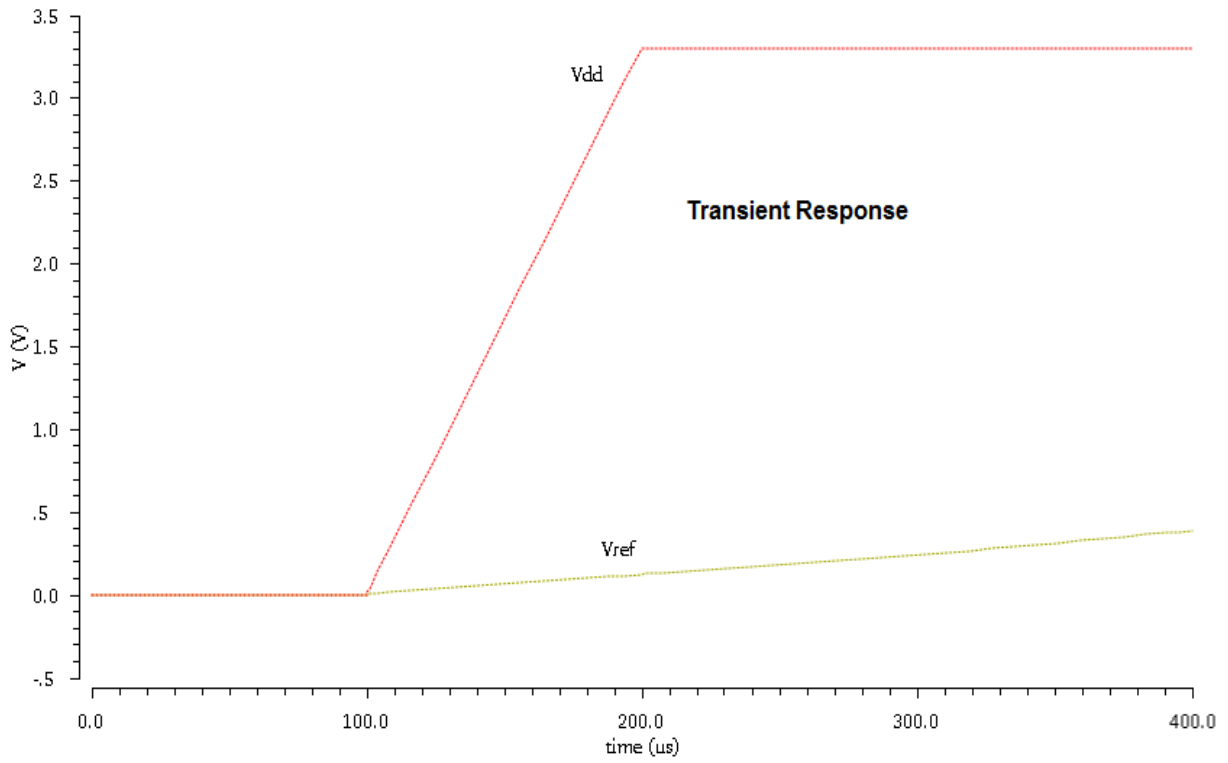


Figure 6.2 Figure showing the transient response of output voltage ( $V_{ref}$ )



Figure 6.3 Figure showing the transient response of gate voltage of  $M_1$ ,  $M_2$ ,  $M_3$ ,  $M_4$

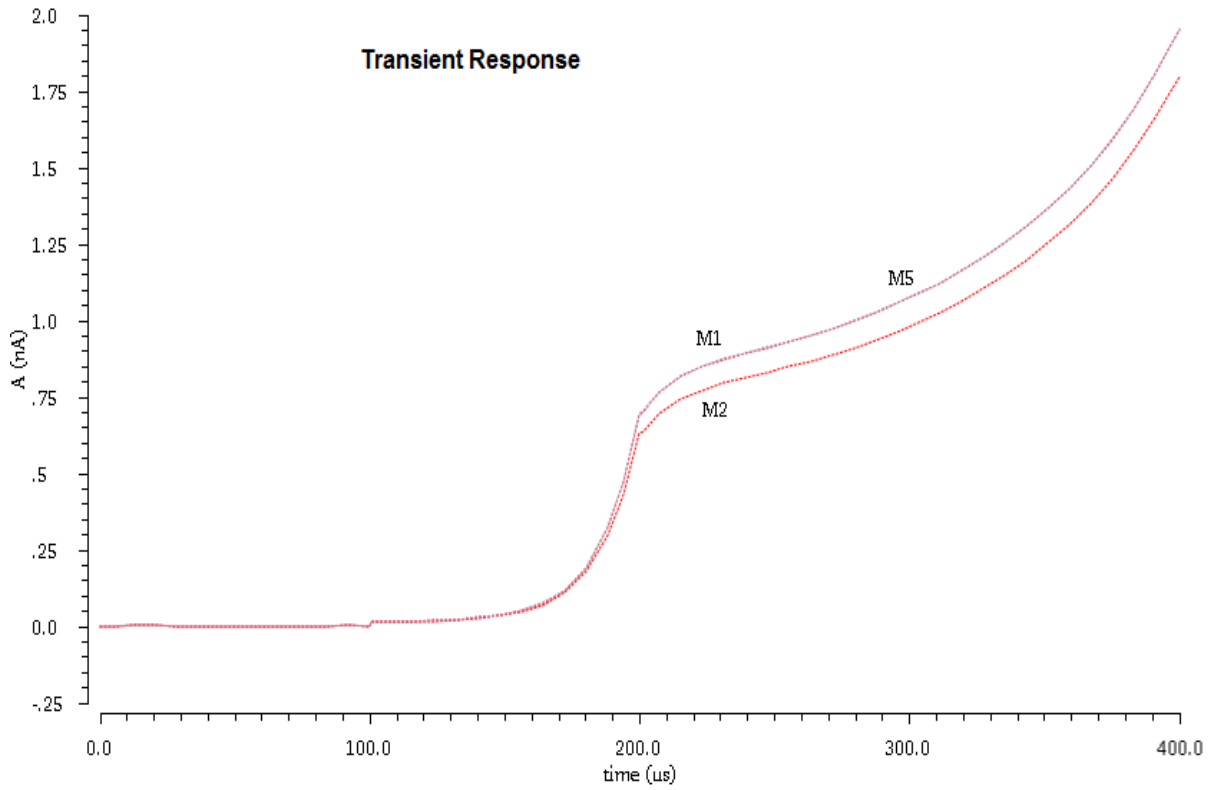


Figure 6.4 Figure showing variations in current for M<sub>1</sub>, M<sub>2</sub>, and M<sub>5</sub>

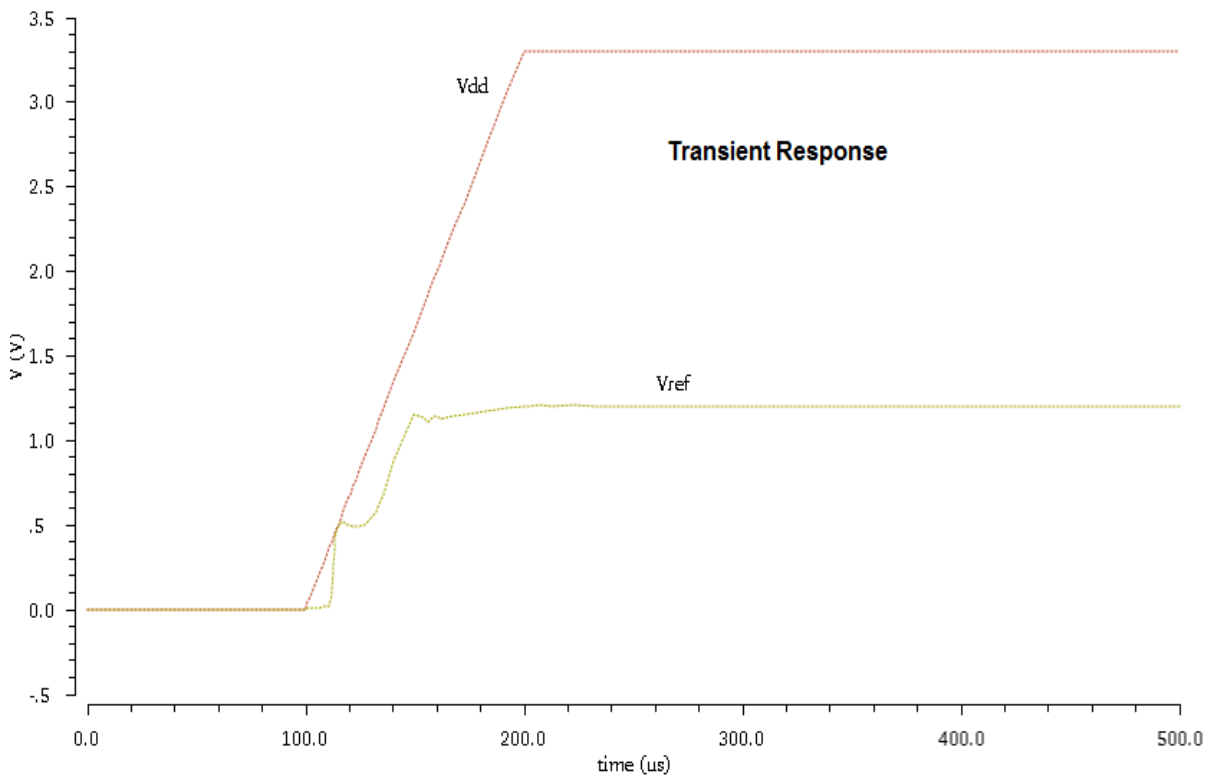
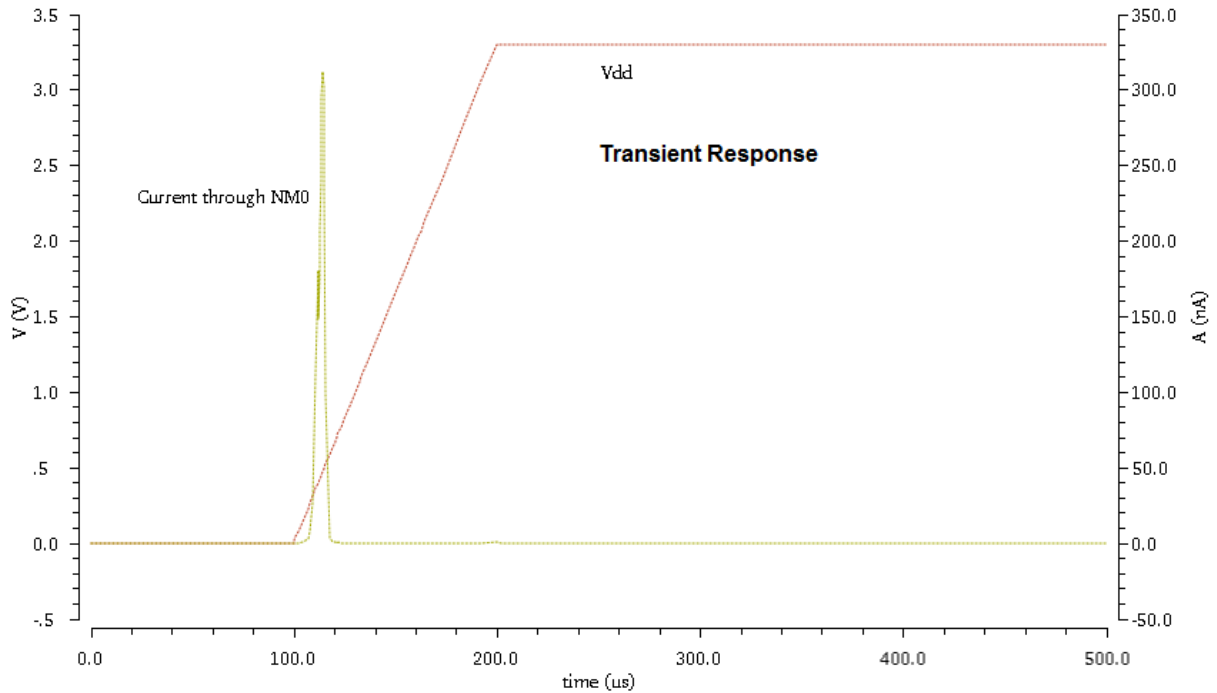


Figure 6.5 Figure shows the effect of start-up circuit on output voltage ( $V_{ref}$ )



**Figure 6.6** Figure shows the variation of current through NM<sub>0</sub> (start-up) in comparison to V<sub>dd</sub>

### 6.3 CONCLUSIONS:

In this chapter we discussed the importance of start-up circuits in a typical self-bias circuit such as band gap reference circuit. We later discussed why the dc analysis alone is not a good test for the functionality of an analog IC and why it is important to perform transient analysis for such circuits. In the end transient analysis for the band gap reference circuit with a start-up circuit is presented.

## CHAPTER – 7

### **Conclusion and Future Scope**

## 7.1 SUMMARY:

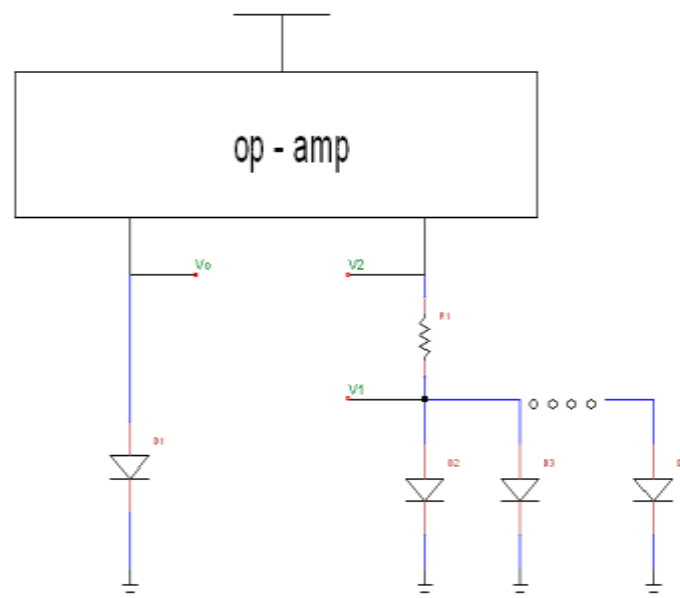
In this dissertation we started with our discussion of CTAT, PTAT design. We later combined both of these circuits in order to achieve a stable band gap reference voltage of 1.2 V. Further in our dissertation we discussed various ways of improving the earlier designs. We also simulated those designs to actually observe that whether or not those design goals have been met or not.

In the end of our dissertation report we discussed the necessity of start-up circuits and critically analysed the transient response of band gap circuits with the inclusion of start-up circuits.

## 7.2 FUTURE SCOPE:

In earlier chapters in design of band gap reference circuit we took the help of current mirror to replicate the current through different branches in order to make the node potential equal across different MOSFETs. We can also use op-amp in negative feedback in place of current mirror to achieve the same result [4][10].

If we replace the current mirror in Figure 3.5 with the op-amp we will get,



**Figure 7.1** Figure shows the modified PTAT with op-amp

While designing the op-amp to be replaced in place of current mirror we should take following points in consideration.

- The current is not directed by the supply voltage in but rather through op-amp therefore op-amp that we are using should be able to supply high current at the output
- The op-amp will be driving resistive load therefore its output impedance should be very low. Therefore, the op-amp required should have low output impedance driving stage in it.

The performance of band gap reference can be further improved by utilising both op-amp and current mirror and in practical cases it is preferred over the one having only current mirror or op-amp.

## REFERENCES

- [1] D. F. Hilbiber, "**A new semiconductor voltage standard**", *ISSCCDig* (International Solid-State Circuits Conference). *Tech. Papers*, pp 32-33: 1964-Feb.
- [2] Widlar, J. Robert, "**New Developments in IC Voltage Regulators**", *IEEE Journal of Solid-State Circuits*, pp 2–7, 1971-Feb.
- [3] Brokaw, Paul, "**A simple three-terminal IC bandgap reference**", *IEEE Journal of Solid-State Circuits*, pp 388–393, 1974-Dec.
- [4] LM113 Data Sheet, National Semiconductor Linear Data Book, 1972, 1976.
- [5] R. A. Blauschild, P. A. Tucci, R. S. Muller and R. G. Meyer, "**A new NMOS temperature stable voltage reference**" *IEEE J. Solid-State Circuits*, vol. 13, pp. 767-774, Dec. 1978.
- [6] Robert A. Pease, Staff Scientist, MS C2500A National Semiconductor Corp, "**The Design of Band-Gap Reference Circuits: Trials and Tribulations**", *IEEE 1990 Bipolar Circuits and Technology Meeting*.
- [7] Behzad Razavi, "**Fundamentals of Microelectronics**", ch-4 Physics of Bipolar Devices, pg 134, Wiley Student Edition, 2007.
- [8] Behzad Razavi, "**Design of Analog CMOS Integrated Circuits**", ch-11 Bandgap References, pg 377, McGrawHill Publication
- [9] Behzad Razavi, "**A circuit for all Seasons: The Bandgap Reference**", *IEEE Solid-State Circuits Magazine*, Summer-2016.
- [10] Yannis P. Tsvividis, Richard W. Ulmer, "**A CMOS Voltage Reference**", *IEEE Journal of Solid-State Circuits*, VOL. SC-13, NO. 6, December 1978
- [11] Karel E. KUIJK, "**A Precision Reference Voltage Source**", *IEEE Journal of Solid-State Circuits*, VOL. SC-8, NO. 3, June 1973.
- [12] Made Gunawan, Gerrard C. M. Meijer, Jeroen Fonderie and John H. Huijsing, "**A Curvature-Corrected Low-Voltage Bandgap Reference**", *IEEE Journal of Solid-State Circuits*, VOL. 28, NO. 6, June 1973.