ON SOME ASPECTS OF GRID SYNCHRONIZATION FOR SINGLE PHASE AND THREE PHASE SYSTEMS

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ABSTRACT

This thesis discusses the design, modeling and performance evaluation of various synchronization techniques. The techniques discussed in the thesis comprises phase locked loop (PLL) techniques applicable to single phase and three phase systems. Additionally, frequency locked loop (FLL) techniques applicable to single phase and three phase systems have also been studied and their performance has been compared. Moreover, experimental results have been obtained for a few single phase PLL techniques. Grid synchronization is a challenging task especially when the utility signal is polluted with disturbances such as harmonics or distorted frequency. Design, modeling and simulation of the complete system along with the controller have been carried out in MATLAB/SIMULINK environment. The focus of this thesis is to review these synchronizing techniques on the basis of frequency variations, voltage amplitude variations, phase angle variations and harmonics particularly for grid integration of renewable distributed power generating systems based on phase locked loop (PLL) and FLL.

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List of abbreviations

1.	PLL	Phase locked loops
2.	FLL	Frequency locked loops
3.	DG	Distributed generators
4.	ZCD	Zero crossing detector
5.	IEEE	Institute of Electrical and Electronics Engineers
6.	PCC	Point of common coupling
7.	DC	Direct current
8.	AC	Alternating current
9.	VCO	Voltage controlled oscillator
10.	PD	Phase detector
11.	pPLL	power Phase locked loops
12.	QSG-PLL	Quadrature signal generator Phase locked loops
13.	LPF	Low pass filter
14.	CBF	Complex band filter
15.	SRF PLL	Synchronous reference frame Phase locked loops
16.	EPLL	Enhanced Phase locked loops
17.	DDSRF PLL	Decoupled double SRF PLL
18.	SOGI PLL	Second order generalized integrator PLL
19.	DSOGI PLL	Dual SOGI PLL
20.	ISC	Instantaneous symmetric components
21.	DSC PLL	Delayed signal cancellation Phase locked loops
22.	DSP	Digital signal processor
23.	PLO	Phase locked oscillator
24.	ANF	Adaptive notch filter
25.	PV	Photo voltaic
26.	OSG	Orthogonal signal generator
27.	DFAC pPLL	Double frequency amplitude compensation pPLL
28.	ATD PLL	Adaptive transport delay Phase locked loops

29. PI	Proportional-Integral
30. GI	Generalized integrator
31. ROGI	Reduced order generalized integrator
32. CBF FLL1	Complex band filter Frequency locked loops 1
33. CBF FLL2	Complex band filter Frequency locked loops 2
34. kVA	kilo volt amperes
35. DSO	Digital scope oscilloscope
36. dq	direct quadrature
37. freq	frequency
38. rms	root mean square
39. Hz	Hertz
40. s	Seconds

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW OF THESIS

Conventionally, the sources of energy consumed for the production of power comprises coal, hydro, diesel and so on. These sources of energy are depleting in nature and therefore, there is an inevitable need to switch to renewable sources of energy such as solar, wind, etc. The power plants in existence are hence being utilized for the generation of green energy (i.e. the energy produced using renewable sources of energy). The integration of power plants such as solar plant with the conventional power plants faces various problems. The major problem faced is of synchronization of the two grids (or plants). Therefore, there was a need to devise suitable synchronization techniques that could synchronize the grids under several disturbances such as harmonics, frequency deviation, etc.

1.1.1 NEED OF SYNCHRONIZATION TECHNIQUES

In recent years, the single-phase power converters have received a considerable attention because of emerging applications/requirements such as the grid integrating of small scale renewable energy sources (particularly rooftop photovoltaic panels), vehicle-to-grid and grid-to-vehicle connections, low-power-rating uninterruptible power supplies, and small-scale power quality conditioners [1]–[5]. Converter interfaced distributed generator (DG) units must be synchronized with the utility system. Grid synchronization is a challenging task especially when the utility signal is polluted with disturbances and harmonics or is of a distorted frequency. A phase detecting technique provides a reference phase signal synchronized with the grid voltage that is required to control and meet the power quality standards. This is critical in converter interfaced DG units where the synchronization scheme should provide a high degree of insensitivity to power system disturbances,

unbalances, harmonics, voltage sags, and other types of pollutions that exist in the grid signal . In general, a good synchronization scheme must i) proficiently detect the phase angle of the utility signal, ii) Track the phase and frequency variations smoothly, and iii) forcefully reject disturbances and harmonics. These factors, together with the implementation simplicity and the cost are all important when examining the credibility of a synchronization scheme.

There are several ways through which synchronization can be implemented. Few of the methods include, but not limited to,

1. Zero Crossing detector (ZCD) method
2. Phase locked loop (PLL)
3. Frequency locked loop (FLL)

1.1.2 GRID CODE REQUIREMENTS:

A grid code is a specification which defines the parameters a facility connected to an electric network has to meet to ensure safe, secure and proper economic functioning of the electric system. These include voltage regulation, reactive power supply and power factor limits, response to a system fault (short-circuit), response to changes in the frequency on the grid, and requirement to "ride through" short interruptions of the connection. The full revision of IEEE Standard 1547 and the corresponding 2030 documents under IEEE SCC21 have established new requirements, recommended practices, and guidance for advanced DER interconnections and interoperability with the grid, now including transmission-level effects in addition to the distribution grid [56].

A few terms associated with the grid code are as follows:

1. Voltage regulation: This means that by the connecting the DG, the voltage at the PCC shall not be outside a specified range.
2. Frequency Deviation: In the same way the frequency deviations shall also not go outside a specified range.

3. Synchronization: While synchronizing a DG with a utility grid it shall not cause a voltage fluctuation of more than ± 5% of the existing voltage level at the Point of Common Coupling (PCC).
4. Monitoring Systems: A DG system of rating 250 kW or more shall have provisions for the monitoring of connection status and real and reactive power outputs at the point of DG connection.
5. Isolation system: Whenever required by utility grid operating practice for making or breaking the connection, an isolation device shall be located between the DG unit and the utility grid.
6. Harmonics: The allowable voltage harmonic distortion is specified at the PCC. It is normally required that the maximum voltage total harmonic distortion is 5% and maximum individual frequency voltage harmonic is 3% of the fundamental component.
7. DC current injection: A DG and its interconnection system shall not inject dc current greater than 0.5% of its rated output current into the utility grid at the PCC.
8. Flicker: A DG must not create objectionable flicker for customers on the Utility grid.

1.1.3 BASICS OF PLL

PLL stands for Phase locked loop. A phase-locked loop is a control system that generates an output signal whose phase is related to the phase of an input signal. Though there are numerous types of PLLs, it is easy to first envisage it as an electronic circuit consisting of a variable frequency oscillator (VCO) and a phase detector (PD). The VCO produce a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, regulating the oscillator to keep the phases harmonized. As the output of VCO is given back to the phase detector, it is called a feedback signal [6].

Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis.

1.1.4 BASIC POINTS ABOUT PLL:

1. PLL is a circuit that locks the phase of the output to the input.
2. PLL is a negative feedback control system where the output frequency tracks the input frequency.
3. PLL is a circuit synchronizing an output signal with a reference or input signal in frequency as well as in phase.
4. In the synchronized or "locked" state, the phase error between the oscillator's output signal and the reference signal is zero, or it remains constant.
5. If a phase error builds up, a control mechanism acts on the oscillator to reduce the phase error to a minimum so that the phase of the output signal is actually locked to the phase of the reference signal. This is why it is called a phase-locked loop.

1.1.5 STRUCTURE OF A PLL

PLL has three basic components [6] i.e.:

1. Phase detector
2. Loop filter
3. A VCO (Voltage controlled oscillator)

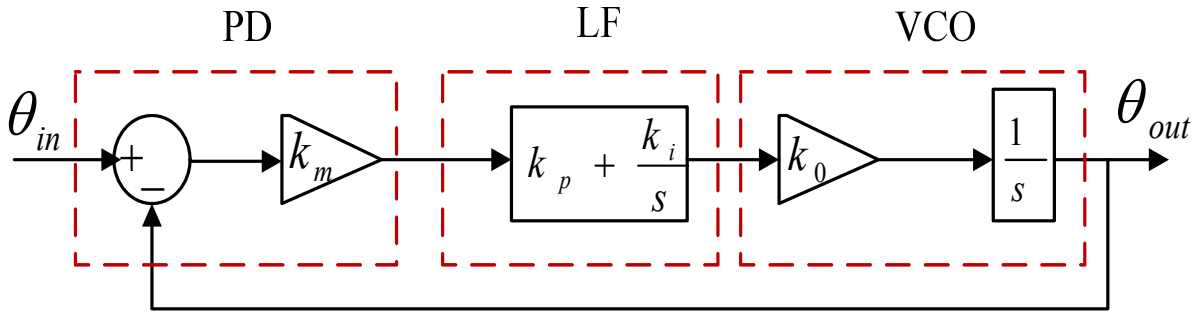

Figure 1.1: Block diagram of a basic Phase locked loop system

Phase, amplitude and frequency of the utility voltage are critical information for the operation of the grid-connected power conditioning and power generating equipment. In such applications, an accurate and fast detection of the phase angle of the utility voltage is essential to assure the correct generation of the reference signals. The phase-locked loop (PLL) structure is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. The purpose of the PLL in a grid connected system is to synchronize the inverter current angle, θ_{out}, with the angle of the grid voltage, θ_{in}, in order to obtain a power factor as close to unity as possible. The angle θ_{out}, is used to calculate the reference current that is compared to the actual output current of the inverter. The main idea in the PLL is that it changes the inverter current frequency, ω_{out}, if the inverter current and the grid voltage are out of phase. If the inverter current lags the grid voltage the PLL will decrease ω_{out}, until the inverter current is in phase with the grid voltage. On the other hand, if the inverter current leads the grid voltage, ω_{out}, is increased until they are in phase. In order to be able to synchronize θ_{out} with θ_{in} it is necessary somehow to measure θ_{in}. This has been done by detecting the zero crossing on the grid voltage. Most recently, there has been an increasing interest in Phase-Locked-Loop (PLL) topologies for grid-connected systems. In order to use a PLL method in single-phase systems an artificial orthogonal voltage system should be created. It is well known that in single-phase systems there are less information than in three-phase systems regarding the grid condition, so more

advanced methods should be considered in order to create an orthogonal voltage system. Also using a PLL structure the grid voltage parameters can be monitored such as grid voltage amplitude and frequency. This grid voltage monitoring is used to ensure that the performances of the investigated methods comply with the standard requirements for operation under common utility distortions such as line notching/harmonics, voltage sags/swells/loss, frequency variations and phase jumps. A large number of single-phase PLLs have been developed and proposed in the literature. Here, they are classified into two major categories: power-based PLLs (pPLLs) [7]–[19] and quadrature signal generation-based PLLs (QSG-PLLs) [20]– [54].

1.1.6 INTRODUCTION TO FREQUENCY LOCKED LOOPS (FLL)

The closed-loop synchronization techniques can be broadly classified into two major categories: phase-locked loops (PLLs) and frequency-locked loops (FLLs). In their standard structures, both PLLs and FLLs have a limited filtering capability [34],[35]. To deal with this problem, many efforts have been made by different researchers. The majority of these efforts have been concentrated on PLLs, and a little work has been conducted on FLLs. The reason behind this probably lies in the reference frame in which PLLs and FLLs are implemented. The PLLs are implemented in the synchronous reference frame. Therefore, their filtering capability can easily and effectively be improved by including additional low-pass filters (LPFs) and/or notch filters into their structure. The FLLs, however, are realized in the stationary reference frame using generalized integrators [36],[37] or complex bandpass filters (CBFs) [51–[54]. Consequently, designing additional filters for incorporating into their structure is more difficult.

An FLL locks the frequency of the grid voltage instead of the phase angle, and the phase angle is calculated outside the loop. Due to inherent differences between the FLL and PLL, where bandpass filtering characteristics are required to extract the fundamental components and attenuate/eliminate the other harmonics in the FLL system, the in-loop low-passing filters (MAF, CDSC filter, repetitive filter, etc.) that are widely used in PLLs, cannot be directly applied to the FLLs. Therefore, in order to adapt FLLs for adverse grid systems,

multiple notch filters are often employed. These FLLs provide good filtering ability, but suffer from heavy computational burden.

1.2 LITERATURE REVIEW

Different synchronization techniques have been proposed in the literature. A popular strategy is using a phase-locked loop (PLL). The PLL can be single phase [7]-[27] or three phase [29]-[33]. The PLL, in simple words, is a closed-loop control system that locks its output to its input with a constant phase error (ideally zero) [6]. All PLLs, regardless of their differences, have three basic parts [6]. The first one is the phase detector (PD), which generates a phase error signal, i.e., a signal that contains the error between real and estimated phases. The second part is the loop filter (LF), which is mainly responsible for suppressing disturbances inside the PLL control loop. The dynamic response, tracking characteristics, and stability properties of the PLL are also mainly dictated by the LF. In energy and power applications, the LF is often a proportional-integral (PI) controller. The third part is the voltage-controlled oscillator (VCO), which is responsible for generating the synchronized signal with the PLL input. A large number of single-phase and three phase PLLs have been developed and proposed in the literature. Here, they are classified into two major categories: power-based PLLs (pPLLs) [22]–[24] and quadrature signal generation-based PLLs (QSG-PLLs) [8]–[21]. This classification is mainly based on the PD of PLLs because the main difference between single-phase PLLs lies in their PD. The pPLLs are characterized by having a product-type PD [22], [23]. A by-product of such PD is a double-frequency disturbance term, which results in double-frequency oscillatory errors and, therefore, an offset error in the estimated quantities by the standard pPLL. To tackle this issue, several advanced pPLLs have been designed in the recent years [22]-[25]. The main difference between them lies in the filtering strategy they use for rejecting the double-frequency disturbance term. The QSG-PLLs can be understood as the single-phase version of the conventional synchronous reference frame PLL (SRF-PLL), which is a standard PLL in three-phase applications. What almost all QSG-PLLs have in common is a unit for creating a fictitious quadrature signal, which is required for transferring the information into the dq frame. This unit can be implemented using different filters/circuits/algorithms [20]–[45]. A

member of this class that looks different from others, at least at first glance, is the enhanced PLL (EPLL) [8]–[13]. This PLL, which has been developed based on an optimization perspective, has a close connection with some QSG-PLLs [11]. For this purpose, it has been subsumed under the category of QSG-PLLs.

The three phase synchronous reference frame phase-locked loops (SRFPLLs) [29]-[33] are the most widely used on synchronization techniques. The SRF-PLL yields a satisfactory performance in terms of the phase/frequency tracking capability and the dynamic response under ideal grid conditions. However, when the grid voltage is unbalanced or harmonically distorted, it presents a degraded performance: high amplitude steady-state oscillations in the estimated phase/frequency arise (Yang et al. 2013). This problem can be mitigated by reducing the SRF-PLL's bandwidth at the expense of the dynamic response; however, this measure may not be an effective solution in some applications. Many advanced PLLs have been proposed in literature. For instance, the decoupled double synchronous reference frame PLL (DDSRF PLL) is proposed in (Rodriguez et al. 2007), it employs two SRFs and a decoupling network to separate the positive and negative sequence components, and extracts the fundamental positive-sequence and negative sequence component of grid voltage. Therefore the approach can prevent the double-frequency detection errors caused by the fundamental frequency negative-sequence component. Because there are four low-pass filters, the system is complex. In (Rodriguez et al. 2006), Rodriguez P et al. proposed a dual second-order generalized integrator based PLL (DSOGI-PLL), which is based on the instantaneous symmetrical components (ISC) theory in the stationary reference frame. The approach achieves frequency self-adaptation, but the orthogonal property of output is sensitive to direct current biasing voltage of input. Delayed signal cancellation-based PLL (DSC-PLL) is applied in order to eliminate the negative sequence component in unbalanced grids and also to cancel any given harmonics (Wang et al. 2011), (Liccardo et al. 2011), but improper sampling rate or system frequency shift could result in estimation deviations and their complexity always require multiple digital signal processors. A three-phase PLL algorithm based on signal reforming is presented by Liu, Baoquan et al. (Liu et al. 2015). It focuses on the reforming of the primary signals before phase estimation, and dedicates to eliminate the negative sequence of the three-phase imbalances. Although the aforementioned PLL methods show good performance, the implementation of these algorithms is quite

complicated, and requires multiple digital signal processors (DSPs) to reduce the execution time of the algorithms (Xu et al. 2007). Several types of PL that can be applied to three phase systems other than the conventional SRF PLL have also been studied in the literature. Few of the prior art includes three phase EPLL [40]-[41] which is categorized under QSG based PLL, three phase power PLL which is quite similar to the single phase power PLL [22]-[25].

1.3 MOTIVATION OF THESIS

The Environmental friendly renewable energy technologies such as wind and solar energy systems are among the fleet of new generating technologies driving the demand for distributed generation of electricity. Power Electronics has initiated the next technological revolution and enables the connection of distributed generation (DG) systems to the grid. Thus the increasing power demand will be met by Distributed Generation (DG) system which are based on renewable energy sources such as solar power, wind power, small hydro power etc. [1]-[2]. These systems need to be controlled properly in order to ensure synchronization of the grid. Grid connected inverter plays a vital role in maintaining voltage at the point of common coupling (PCC) constant. For the reliable operation of utility grid based on DG system, the power plant operators should satisfy the grid code requirements such as fault ride through, grid stability, grid synchronization and power control etc. The major issue associated with DG system is their synchronization with utility voltage vector [4]. Various synchronization methods have therefore been analyzed to meet the synchronization requirements of the grid.

1.4 ORGANIZATION OF THESIS

The thesis is organized into five chapters including the introduction in the Chapter 1. Each of these is summarized below:

CHAPTER 1: Chapter 1 deals with the topics such as need of synchronization techniques, various synchronization techniques, detailed explanation of phase locked loop system, introduction to frequency locked loop system and so forth.

CHAPTER 2: Chapter 2 deals with various single phase phase locked loop systems. Furthermore, the chapter includes the analysis of PLL techniques, the estimation of PLL performance on application of various disturbances such as, frequency change, voltage amplitude change, phase angle change and introduction to harmonics. Additionally, the performance of single phase phase locked loop techniques has been compared with respect to frequency change introduced in the system and formulated in a table.

CHAPTER 3: Chapter 3 deals with various three phase phase locked loop systems. Furthermore, the chapter includes the analysis of PLL techniques, the estimation of PLL performance on application of various disturbances such as, frequency change, voltage amplitude change, phase angle change and introduction to harmonics. Additionally, the performance of three phase phase locked loop techniques has been compared with respect to frequency change introduced in the system and formulated in a table.

CHAPTER 4: Chapter 4 deals with various single phase and three phase frequency locked loop systems. Furthermore, the chapter includes the analysis of FLL techniques, the estimation of FLL performance on application of frequency change. Additionally, the performance of single phase and three phase frequency locked loop techniques has been compared with respect to frequency change introduced in the system and formulated in a table.

CHAPTER 5: Chapter 5 includes experimental results conducted on a few single phase phase locked loop techniques based on frequency change, effect of harmonics and noise. The PLLs were examined for the maintenance of locked state under the mentioned disturbances.

CHAPTER 2

PHASE LOCKED LOOP TECHNIQUES FOR A SINGLE PHASE SYSTEM

2.1 INTRODUCTION

Several techniques such as zero crossing detection (ZCD), phase locked oscillator (PLO), EPLL [14-16] have been mentioned in the literature for implementing grid synchronization. Some newer techniques are also being researched for this purpose which includes PLLs based on adaptive notch filters (ANF), weighted least squares estimation techniques, and artificial neural network based controllers. Moreover, PLL less synchronization is also gaining importance. The use of different PLLs for single phase as well as three phase systems for PV interfaced grid connected systems is gaining high importance and studied thoroughly [28]. High significance is assigned to designing simpler and effective synchronization schemes that will work well in harmonically polluted grid systems. Fast tracking ability should be ensured by the designed PLL under all varied conditions.

Here in this chapter, various synchronization techniques based on phase locked loop applicable to a single phase system have been discussed. Design, modeling and simulation of the complete system along with the controller have been carried out in MATLAB/SIMULINK environment. Simulation results for different cases have been investigated which include the performance of these single phase PLL under (i) Voltage amplitude change, (ii) Frequency change (iii) Phase change and (iv) effect of harmonics. Comparative results have been tabulated for the different PLL schemes. PLL techniques are gaining importance worldwide and the research conducted on synchronization techniques have been mentioned in the literature review in the chapter 1.

2.2 TYPES OF PHASE LOCKED LOOP TECHNIQUES APPLICABLE TO A SINGLE PHASE SYSTEM

In this chapter few of the single phase PLL techniques have been discussed. The most commonly used single phase PLL techniques are based on quadrature signal generation. The quadrature signal generation is used to obtain a signal which is in quadrature with the original signal. There are a few methods which can be used to obtain the quadrature signal. Some of the methods have been discussed below:

2.2.1 TRANSPORT DELAY PLL

The transport delay PLL is one of the easiest methods to obtain a quadrature signal from the grid voltage. The objective of using transport delay block is to generate a signal which is in quadrature with the grid voltage. The signal in quadrature implies that if the grid voltage has a time period of T s, then second signal is generated after the delay block will be (T/4) s.

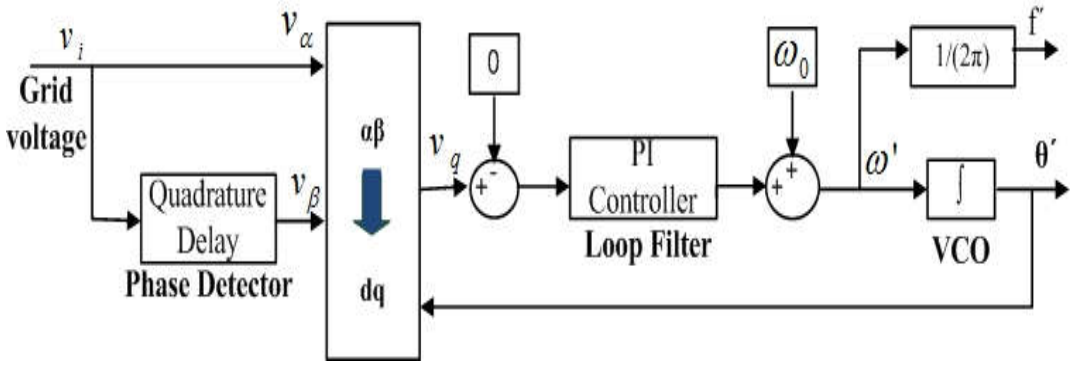

Figure 2.1: Schematic diagram of a Transport Delay PLL

2.2.1.1 ANALYSIS

Figure 2.1 shows the schematic diagram of the transport delay PLL. This is one of the simplest PLLs and uses Park transformation (i.e. αβ to dq) for computation of frequency and phase angle [7]-[11]. To realize this transformation, the β variable is in-quadrature with the grid voltage i.e. shifted from the supply voltage by 90^0.

Let the grid voltage be v_i,

$$v_i(t) = v_i\, cos(\theta) = v_i\, cos(\omega t + \emptyset_o) \tag{2.1}$$

Considering the grid signal frequency is 50 Hz, the time period T will be 1/50 s i.e. 0.02 s. Consequently, there will be a phase shift between v_i and v_β.

The α and β components so obtained are then converted into direct and quadrature (dq) components using Park's transformation described below:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos\,\theta' & sin\,\theta' \\ -sin\,\theta' & cos\,\theta' \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{2.2}$$

The generated signal is now passed through the loop filter which is represented by the PI controller. The further stages include passing it through Voltage controlled Oscillator (VCO). As it a closed loop system, the output of VCO is fed back to the transformation stage as the derived angle. The delay PLL works satisfactorily under normal operating conditions. However, if the input grid voltage is not completely sinusoidal and not at rated frequency, the delayed signal will not be in exact quadrature with the input signal. This will cause problems in the synchronization. Overall, this technique is quite hassle free and can be used to extract phase angle in single phase applications without much distortions.

Due to the problems faced by this method of synchronization, another method was proposed i.e. Adaptive transport Delay PLL technique which has been discussed in the next section.

2.2.1.2 SIMULATION RESULTS

Figure 2.2 shows a simulation model of a transport delay PLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and transport delay PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

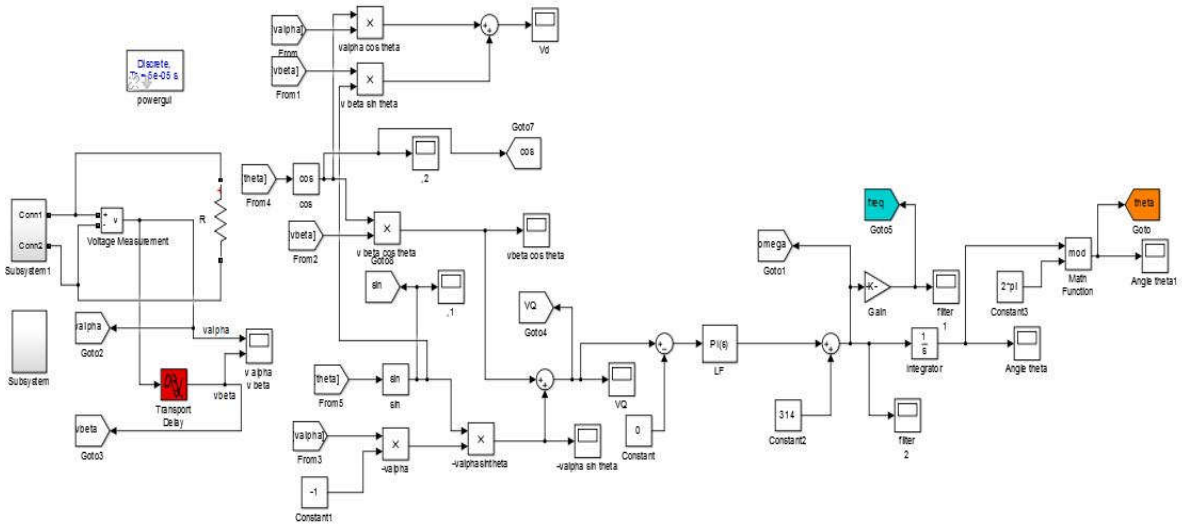

Figure 2.2: Simulation model of a transport delay PLL in MATLAB/SIMULINK environment

The changes have been made at intervals t = 1 s till t = 1.4 s. The working of the PLL has been investigated in case of various disturbances.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It has been observed that the PLL takes nearly 6-7 cycles to settle at 55 Hz and after t = 1.4 s the frequency reaches again to 50 Hz. It can be concluded that in case of frequency deviation, the transport delay PLL is able to maintain synchronism after a few cycles.

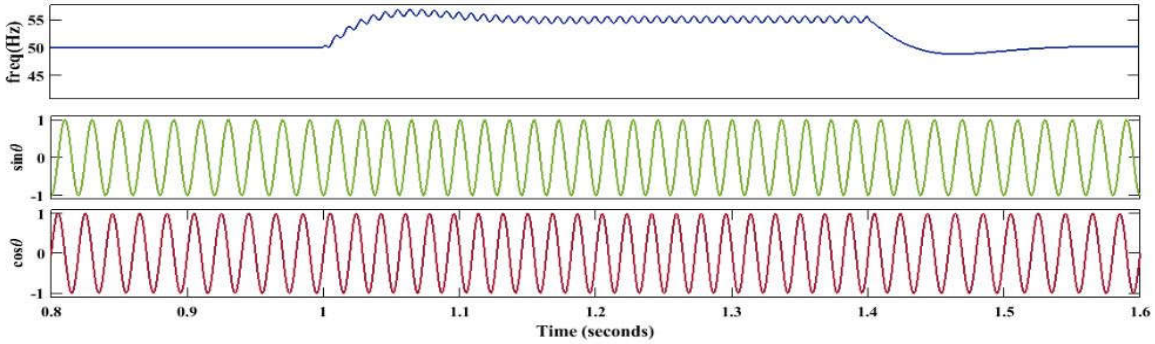

Figure 2.3 Transport Delay PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

The voltage change has been made from 230 V to 110 V between t = 1 s till t = 1.4 s. It can be noted that the PLL tracks voltage and settles to 230 V after t = 1.4 s. It can be observed that the grid voltage is in phase with cosθ.

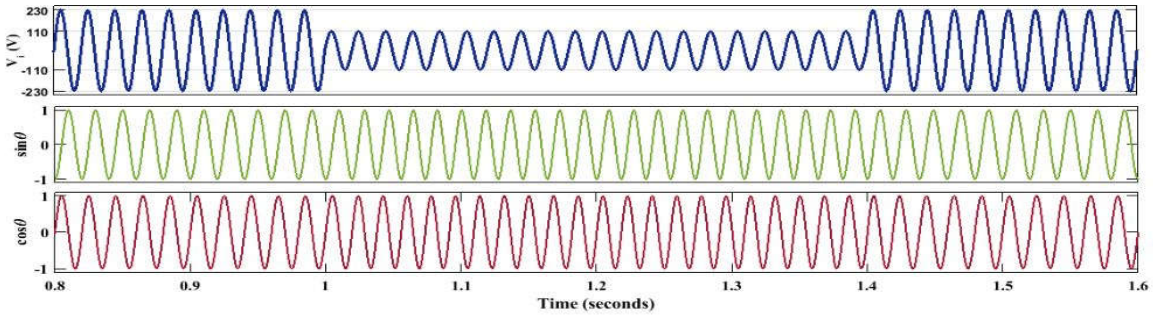

Figure 2.4 Transport Delay PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 second to t = 1.4 s. Phase angle has been changed from 0 radians to pi radians.

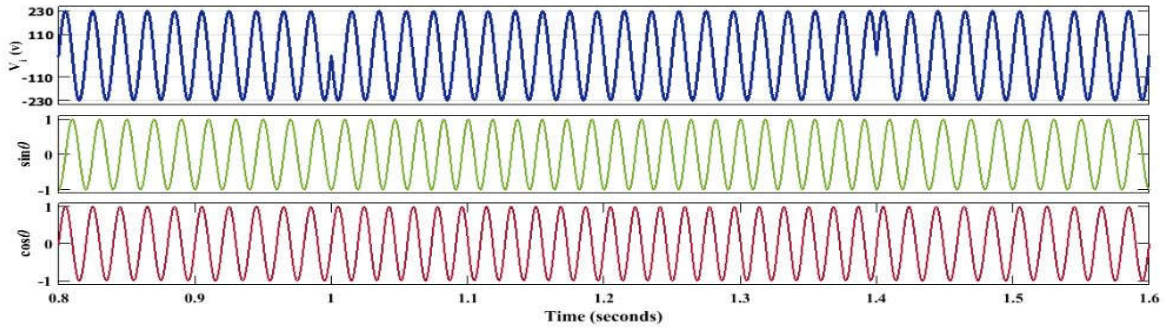

Figure 2.5 Transport Delay PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced between t = 1 s till t = 1.4 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ are maintained in case of harmonics in the system.

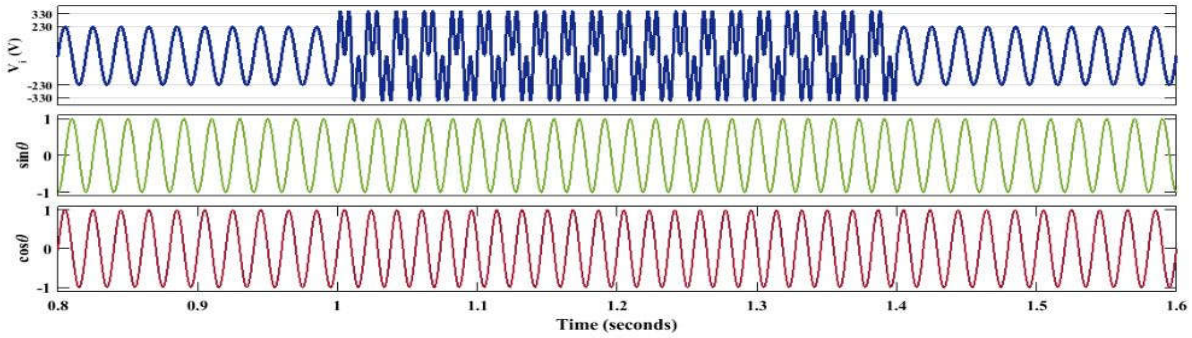

Figure 2.6 Transport Delay PLL (effect of harmonics)

2.2.2 ADAPTIVE TRANSPORT DELAY PLL

Adaptive transport delay PLL is quite similar to the transport delay PLL only with a few modifications. Whenever there is a frequency drift in the system, it results in the lack of orthogonality between v_α and v_β components which causes double-frequency oscillatory errors and offset errors in the predicted quantities of the Transport Delay PLL. Therefore, there was a need to eliminate the abovementioned problem. So a modification to the conventional transport delay PLL was introduced [12]-[13].

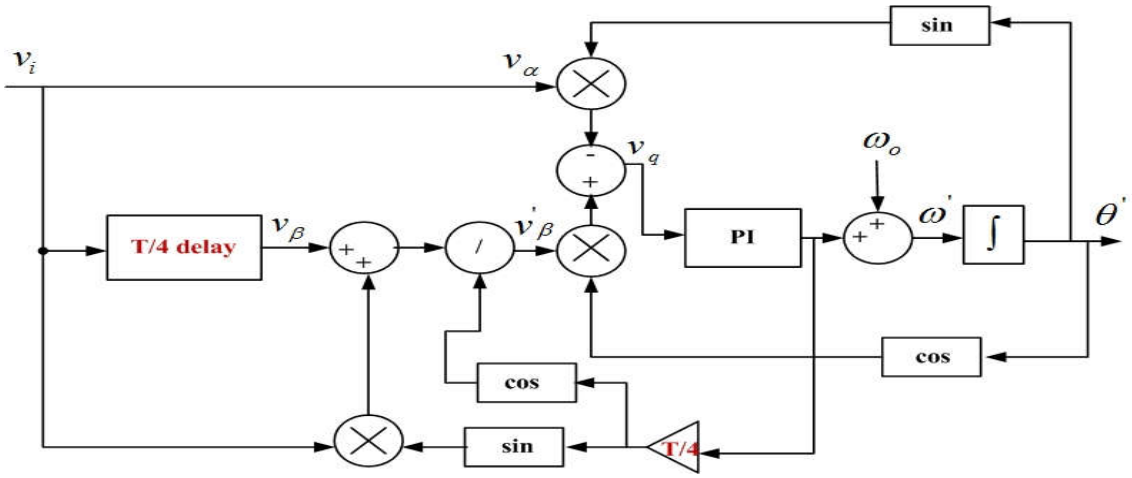

Figure 2.7: Schematic diagram of an Adaptive Transport Delay PLL

2.2.2.1 ANALYSIS

Figure 2.7 shows the schematic diagram of an adaptive transport delay PLL. Mathematical analysis of the Adaptive transport delay PLL has been shown below:

$$v_i(t) = v_\alpha(t) = V_i \cos\theta_i \tag{2.3}$$

$$\theta_i = \omega_i t + \varphi_i \tag{2.4}$$

where,

V_i is the voltage amplitude of the grid,

ω_i is the grid frequency,

φ_i is the initial phase angle of the grid, and

θ_i is the phase angle of the grid.

Let the grid frequency be denoted as:

$$\omega_i = \omega_{nf} + \Delta\omega_i \tag{2.5}$$

where,

ω_{nf} is the actual value of the grid frequency, and

$\Delta\omega_i$ is the deviation of grid frequency from its actual value.

Using equation 2.3 and equation 2.5, the fictitious quadrature signal v_β can be defined as:

$$v_\beta(t) = v_\alpha\left(t - \frac{T}{4}\right) = V_i\, cos(\theta_i - \omega_i \frac{T}{4}) = V_i\, sin(\theta_i - \Delta\omega_i \frac{T}{4}) \tag{2.6}$$

Equations 2.3 and 2.6 demonstrates that v_α and v_β are orthogonal signals only when $\Delta\omega_i$ = 0 (i.e. when there is no deviation of the actual grid frequency in the system). The lack of orthogonality between v_α and v_β components in the case of frequency drifts results in double-frequency oscillatory errors and offset errors in the predicted quantities of the Transport Delay PLL.

By the use of equation 2.6, the quadrature signal produced by the transport delay block can be expressed as:

$$v_\beta(t) = \underbrace{V_i\, sin(\theta_i)}_{v'_\beta} cos\left(\Delta\omega_i \frac{T}{4}\right) - \underbrace{V_i\, cos(\theta_i)}_{v_\alpha} sin\left(\Delta\omega_i \frac{T}{4}\right) \tag{2.7}$$

Using equation 2.7, v_β which is the needed orthogonal signal, can be acquired as:

$$v'_\beta = \frac{v_\beta(t) + v_\alpha(t)\, sin\left(\Delta\omega_i \frac{T}{4}\right)}{cos\left(\Delta\omega_o \frac{T}{4}\right)} \tag{2.8}$$

As equation 2.8 demonstrates, the generation of v_β requires information about the frequency deviation in the system $\Delta\omega_i$. The output of Proportional Integral (PI) controller, imparts an estimation of the change in frequency $\Delta\omega_i$. Therefore, orthogonal signal v_β can be produced as shown in equation 2.9:

$$v'_\beta(t) = \frac{v_\beta(t) + v_\alpha(t) sin\left(\Delta\omega_o \frac{T}{4}\right)}{cos\left(\Delta\omega_o \frac{T}{4}\right)} \tag{2.9}$$

The analysis shows that the adaptive transport delay PLL is an advancement over the conventional transport delay PLL which is basically an SRF PLL employed for a single phase system.

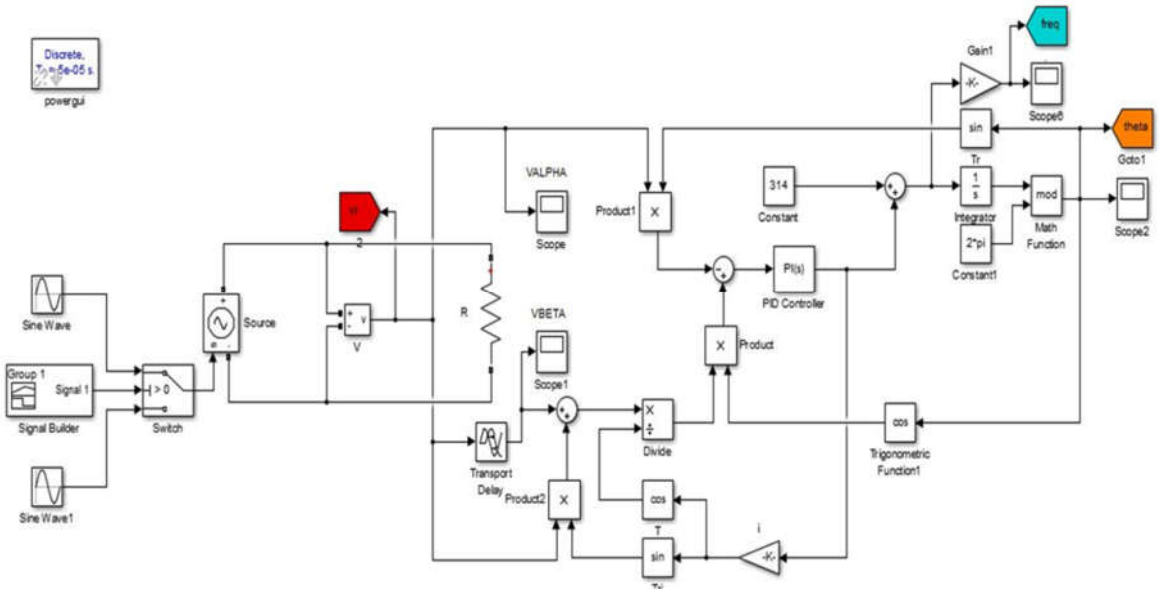

Figure 2.8 Simulation model of an adaptive transport delay PLL in MATLAB/SIMULINK environment

2.2.2.2 SIMULATION RESULTS

Figure 2.8 shows a simulation model of an adaptive transport delay PLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and adaptive transport delay PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances. The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics. The working of the PLL has been investigated in case of various disturbances.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 10-11 cycles to settle at 55 Hz and after t = 1.6 s the frequency reaches again to 50 Hz. It can

be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

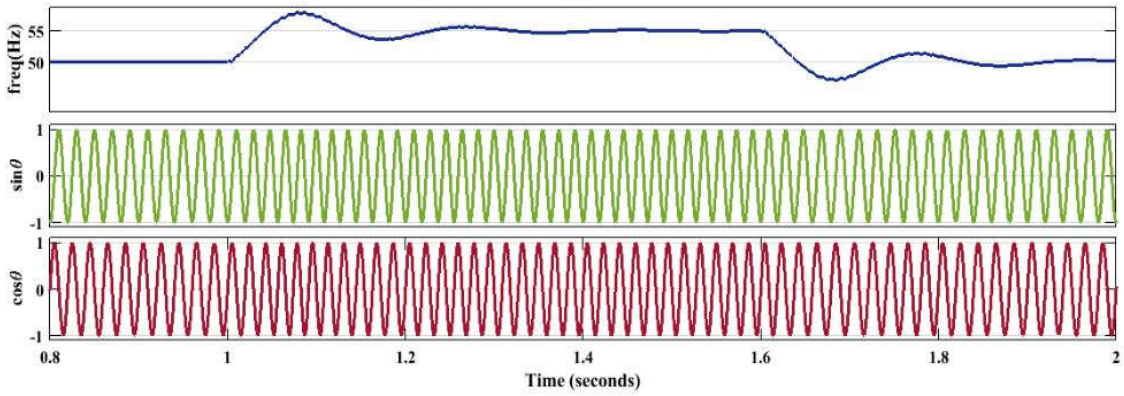

Figure 2.9: Adaptive transport delay PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

The voltage change has been made from 230 V to 110 V between t = 1 s till t = 1.6 s. It can be observed that the PLL tracks voltage and settles to 230 V after t = 1.6 s. Additionally, it can be seen that the grid voltage is in phase with $\cos\theta$.

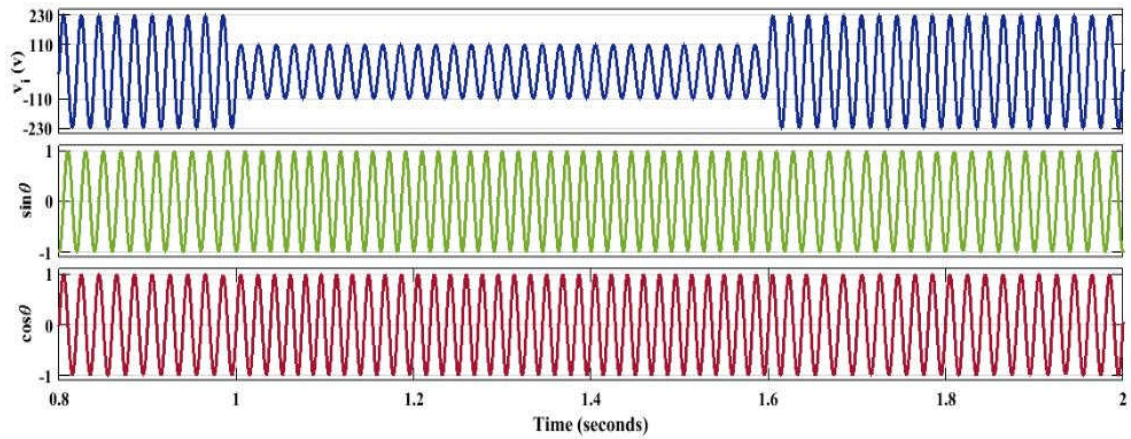

Figure 2.10: Adaptive transport delay PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 second to t = 1.4 s. Phase angle has been changed from 0 rad to pi rad in the 0.4 s interval. The grid voltage maintains synchronism and comes in phase with cos θ when the phase angle is again changed to 0 rad.

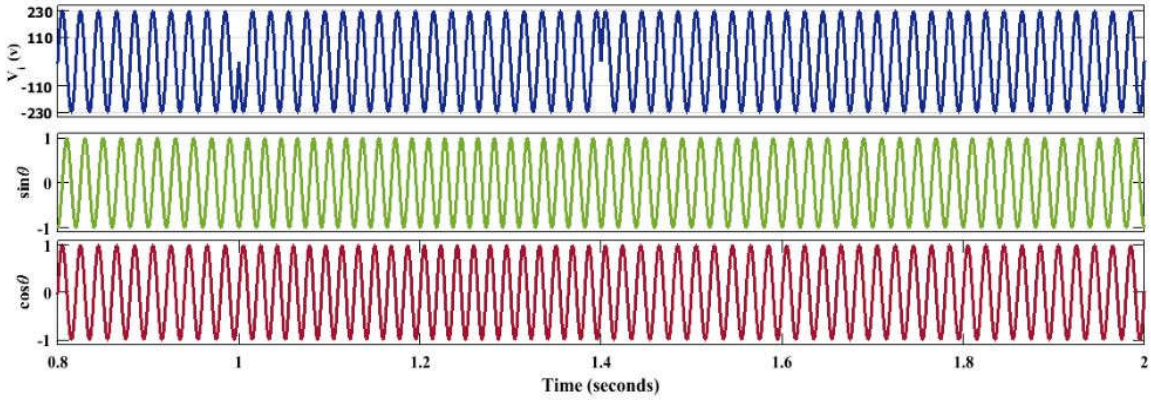

Figure 2.11: Adaptive transport delay PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced between t = 1 second till t = 1.4 s. It can be observed that perfect sin θ and cos θ are maintained in case of harmonics in the system.

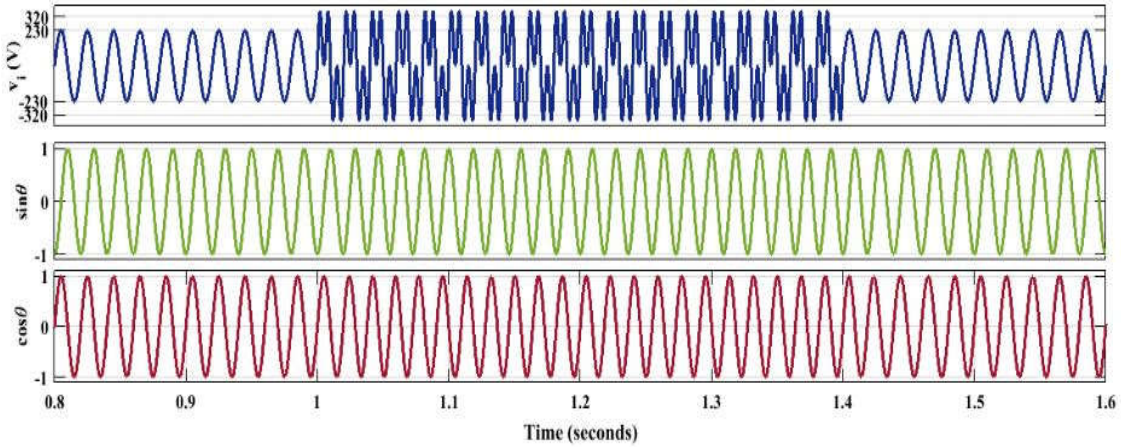

Figure 2.12: Adaptive transport delay PLL (effect of harmonics)

2.2.3 ENHANCED PLL

EPLL is a frequency adaptive non linear synchronization method, which uses an adaptive filter (AF) and a sinusoidal multiplier [14]-[16]. One of the most significant characteristics of an EPLL is that it can be used for locking the grid voltage amplitude and the phase angle both. The EPLL becomes free of any oscillations after a certain time period.

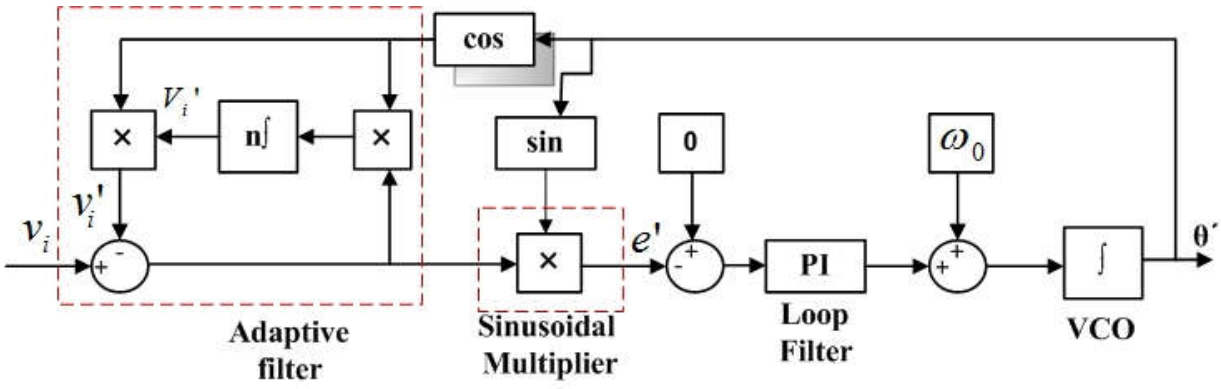

Figure 2.13: Schematic diagram of an Enhanced PLL

2.2.3.1 ANALYSIS

The phase detector of the EPLL is efficient and quite flexible which helps in presenting more information about several attributes of the system vis-à-vis fundamental components, phase components, frequency components, etc. The expected grid voltage amplitude v'_i can be shown as:

$$v_i' = n \int e \cos \theta' \tag{2.10}$$

where n : control parameter and

$$e = v_i - v_i' \tag{2.11}$$

$$e' = e \sin \theta' \tag{2.12}$$

$$V_i' = \cos \theta' = v_i' \tag{2.13}$$

The block diagram for the basic EPLL is shown in Fig.2.13. The input grid voltage v_i' is passed through various stages i.e. Adaptive filter, Loop filter incorporated as a PI controller and a voltage controlled oscillator. The derived angle θ' is fed to cosine and sinusoidal functions which are given to the adaptive filter and the sinusoidal multiplier respectively.

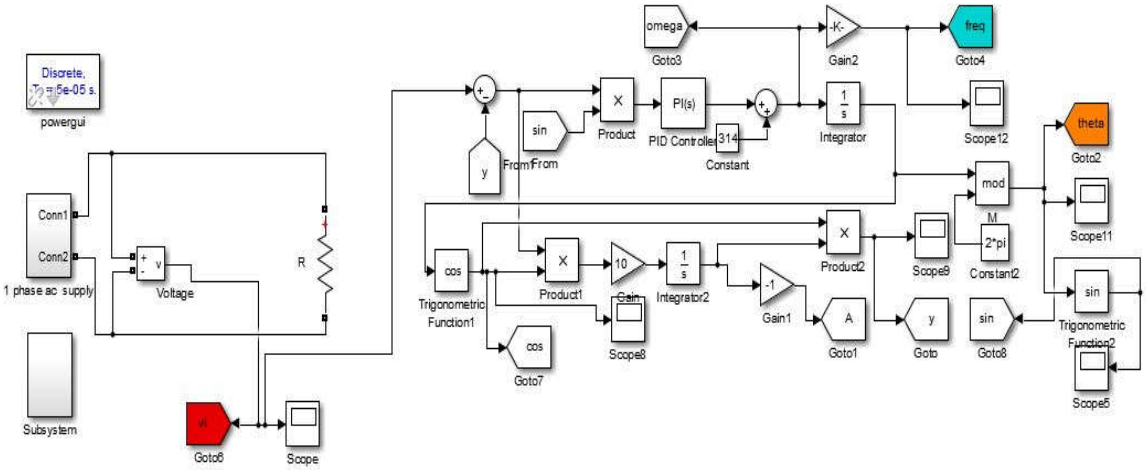

Figure 2.14 Simulation model of enhanced PLL in MATLAB/SIMULINK environment

2.2.3.2 SIMULATION RESULTS

Figure 2.14 shows a simulation model of enhanced PLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and enhanced PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

The changes have been made at intervals t = 1 s till t = 1.4 s.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be observed that the PLL takes nearly 11-12 cycles to settle at 55 Hz along with a few oscillations and after t = 1.4 s the frequency reaches again to 50 Hz.

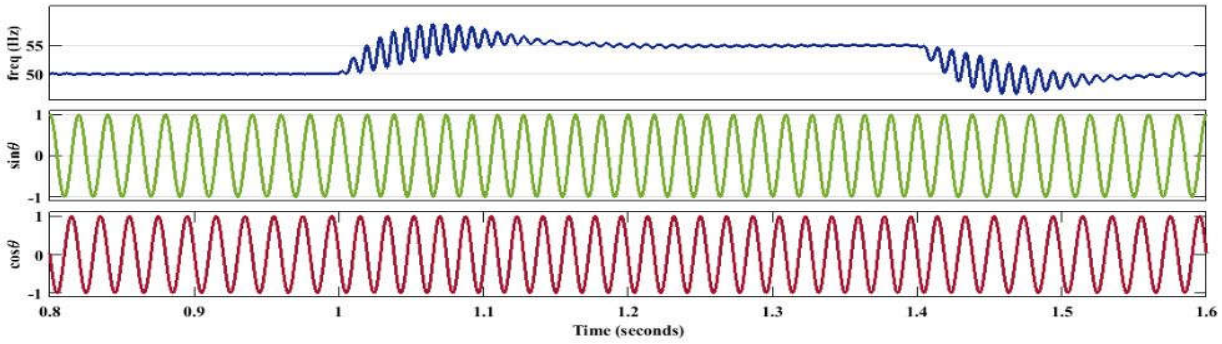

Figure 2.15: Enhanced PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

The voltage change has been made from 230 V to 110 V between t = 1 s till t = 1.4 s. It can be seen that that the PLL tracks voltage and settles to 230 V after t = 1.4 s. Additionally, it can be seen that the grid voltage is in phase with $\cos\theta$.

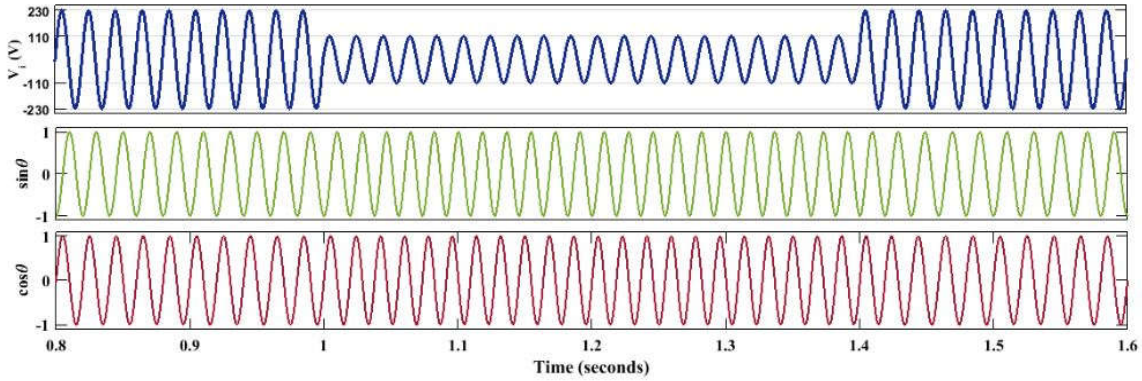

Figure 2.16: Enhanced PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 s to t = 1.4 s. Phase angle has been changed from 0 rad to pi rad. The grid voltage maintains synchronism and comes in phase with $\cos\theta$ when the phase angle is again changed to 0 rad.

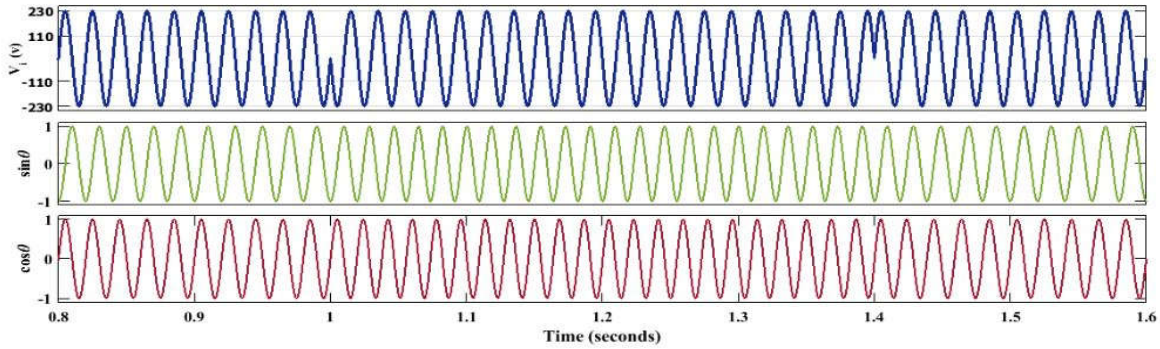

Figure 2.17: Enhanced PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced from t= 1 s till t= 1.4 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ are maintained in case of harmonics in the system.

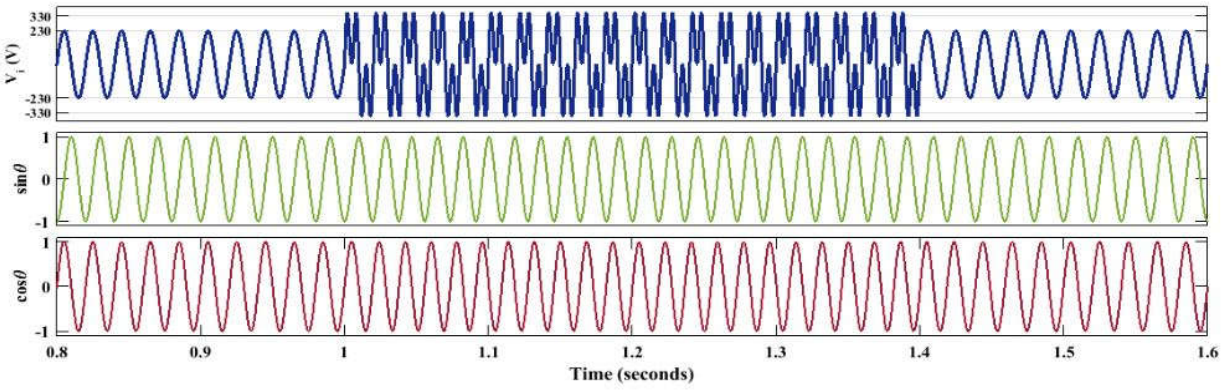

Figure 2.18: Enhanced PLL (effect of harmonics)

2.2.4 SECOND ORDER GENERALIZED INTEGRATOR (SOGI) PLL

SOGI PLL stands for second order generalized integrator PLL. The drawback of using enhanced PLL system is that it uses only one adaptive weight in its realization. Hence, it will take some time period for the transients to die out and the error signal to come into a zero steady state error zone. This zero steady state tracking of the input signal is realized using only one weight adaptive filter. A further improved PLL has been introduced namely SOGI PLL [17-18]. The characteristic feature of SOGI PLL is that it uses a second order adaptive notch filter. The adaptive notch filter in SOGI PLL behaves like a Sinusoidal integrator. Thus, a SOGI PLL behaves like a Sinusoidal integrator whose basic block diagram has been shown in the Fig.2.19.

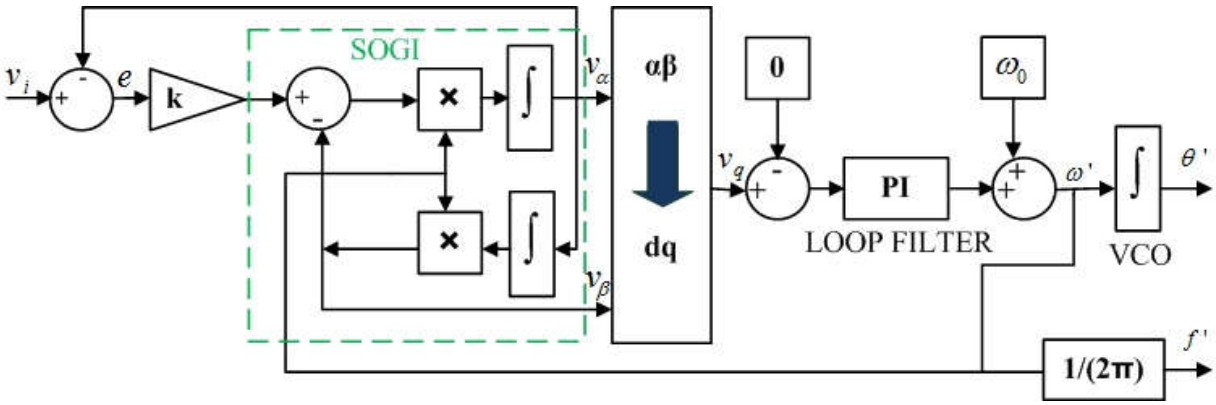

Figure 2.19: Schematic diagram of an SOGI PLL

2.2.4.1 ANALYSIS

It is clear that the SOGI PLL does not employ the typical sin and cosine blocks. This is because it inherently contains the sin and cosine blocks. For an undamped SOGI-PLL system, its transfer function (T.F.) can be defined as:

When in-phase:

$$\text{T. F.} = \frac{\omega_o s}{s^2+\omega_o^2} \tag{2.14}$$

When in quadrature:

$$\text{T. F.} = \frac{\omega_o^2}{s^2+\omega_o^2} \tag{2.15}$$

There is an inherent problem of resonance in using the Equations (2.14-2.15). Hence, the transfer function of the SOGI PLL can be described by adding a feedback control parameter, k as:

$$\begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} = \begin{bmatrix} \frac{k\omega' s}{s^2+k\omega' s+\omega'^2} \\ \frac{k\omega'^2}{s^2+k\omega' s+\omega'^2} \end{bmatrix} V_i(s) \tag{2.16}$$

where k is the control parameter usually taken as $\sqrt{2}$ for accuracy.Now in SOGI PLL, it can be noted that there are two feedback variables. One is the output of the PI controller added to ω_o, let us say ω'. The other one is the output of VCO i.e. θ'. Both the variables are of utmost importance as ω' is used for filteration and θ' for the Park Transform. This leads to the inference that the realization of SOGI PLL is more complicated than the other two schemes discussed in the previous sections. SOGI PLL gives us relatively good results in terms of harmonic rejection capability, therefore it can have added advantage in applications involving distorted single phase systems also.

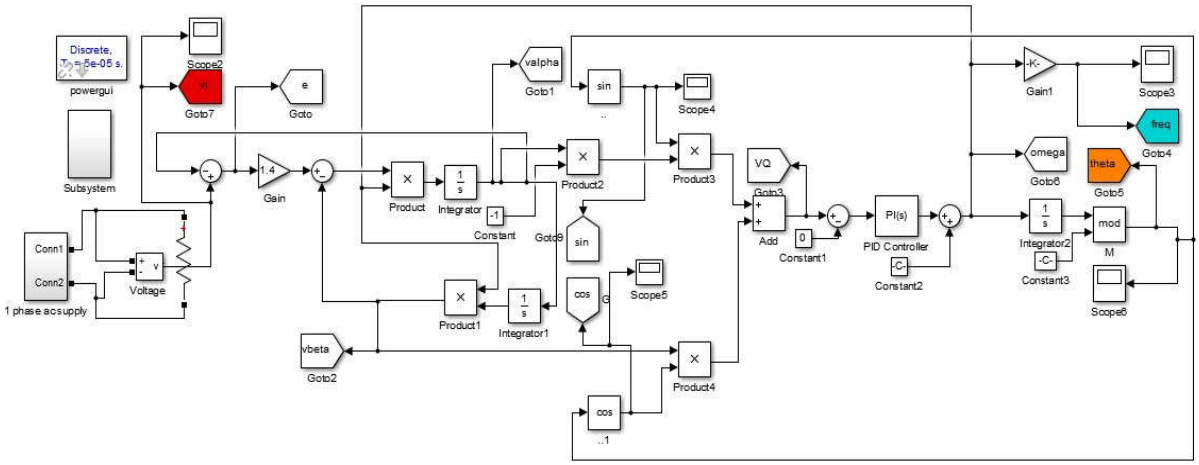

Figure 2.20 Simulation model of SOGI PLL in MATLAB/SIMULINK environment

2.2.4.2 SIMULATION RESULTS

Figure 2.20 shows a simulation model of SOGI PLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and SOGI PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

The changes have been made at intervals t = 1 s till t = 1.4 s.

(a) FREQUENCY CHANGES

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 3-4 cycles to settle at 55 Hz and after t = 1.4 s the frequency reaches again to 50 Hz. It can be concluded that in case of frequency deviation, the SOGI PLL is able to maintain synchronism after a few cycles.

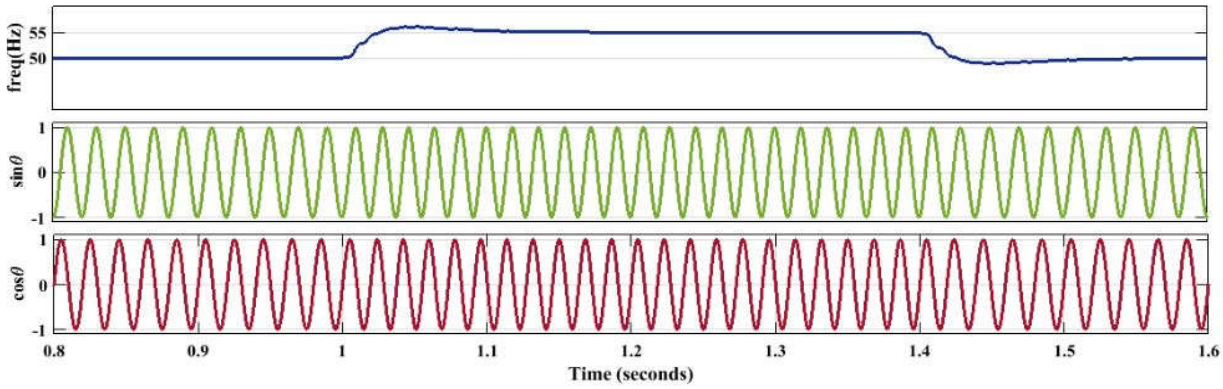

Figure 2.21: SOGI PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

The voltage change has been made from 230 V to 110 V between t = 1 s till t = 1.4 s. It can be noted that the PLL tracks voltage and settles to 230 V after t = 1.4 s. The grid voltage is in phase with $cos\,\theta$.

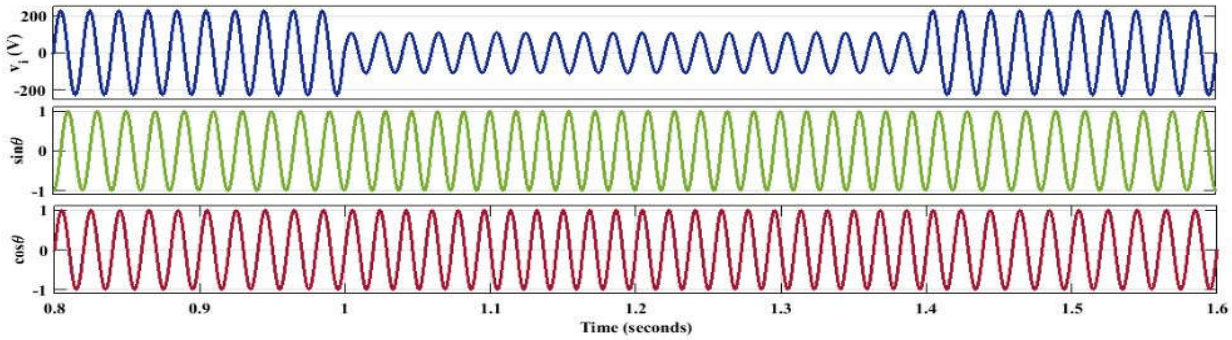

Figure 2.22: SOGI PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 s to t = 1.4 s. The grid voltage maintains synchronism and comes in phase with $\cos\theta$ when the phase angle is again changed to 0 rad.

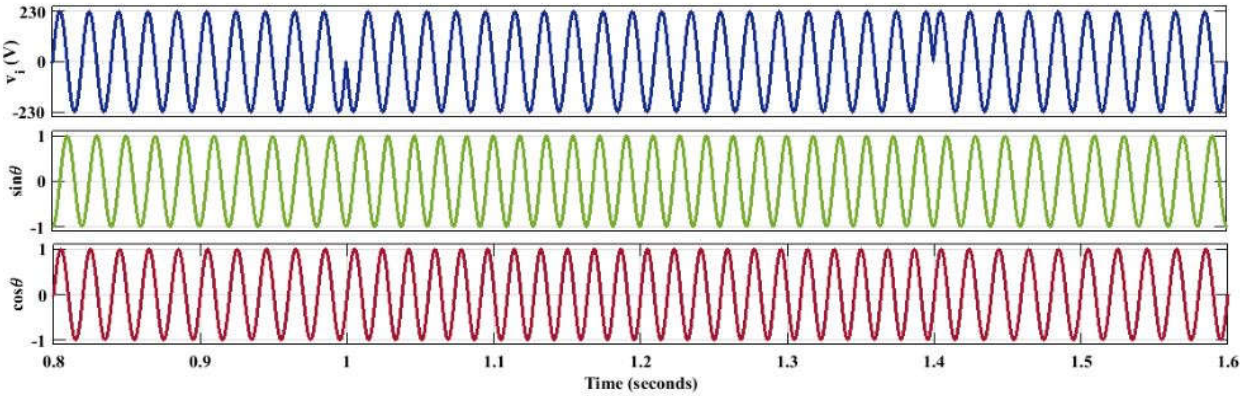

Figure 2.23: SOGI PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced between t= 1 s till t= 1.4 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ are maintained in case of harmonics in the system.

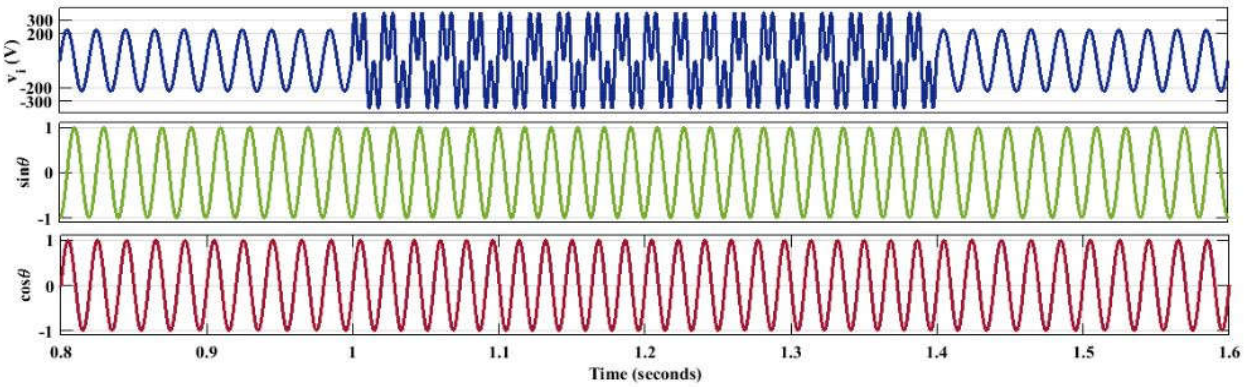

Figure 2.24: SOGI PLL (effect of harmonics)

2.2.5 INVERSE PARK PLL

Inverse park PLL can be employed in single phase systems which is implemented by using park transform. The computational burden of this PLL is quite high as the transformations have to be done twice. Inverse park PLL can be categorized as a QSG based PLL as the motive of using park transform is to generate a component which is in quadrature with the grid voltage.

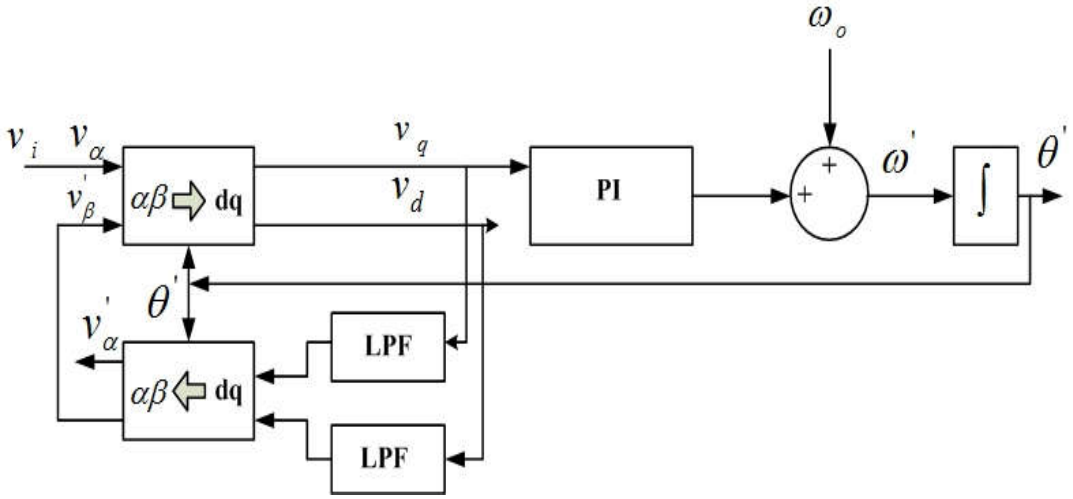

Figure 2.25: Schematic diagram of an Inverse Park PLL

2.2.5.1 ANALYSIS

In this method to build an orthogonal signal generator, which is supposed to generate the 'β' component, a loop consisting of direct as well as indirect Park's transform supported by two low pass filters is created [19]-[21] as shown in Fig.2.25. But here the condition is the PLL should be perfectly tuned to the input frequency to make v_α to be in phase with v_α and in quadrature with v_β . Also the nonlinear inner loop must be fast enough to generate the 'β' component. The whole technique can be described by these set of equations:

$$v_{dq}(s) = \begin{bmatrix} v_d(s) \\ v_q(s) \end{bmatrix} = T_p \begin{bmatrix} v_i(s) \\ v'_\beta(s) \end{bmatrix} \tag{2.17}$$

$$v_{\alpha\beta}(s) = \begin{bmatrix} v'_\alpha(s) \\ v'_\beta(s) \end{bmatrix} = T_p^{-1} \begin{bmatrix} v'_d(s) \\ v'_q(s) \end{bmatrix} \tag{2.18}$$

$$\begin{bmatrix} v'_d(s) \\ v'_q(s) \end{bmatrix} = G_L(s) \begin{bmatrix} v_d(s) \\ v_q(s) \end{bmatrix} = \frac{\omega}{s+\omega_L} \begin{bmatrix} v_d(s) \\ v_q(s) \end{bmatrix} \tag{2.19}$$

where T_p is

$$\begin{bmatrix} cos\,\theta & sin\,\theta \\ -sin\,\theta & cos\,\theta \end{bmatrix} \tag{2.20}$$

Two LPFs are employed to filter out unwanted parts of dq components. The filtered components are used to produce the quadrature signal with respect to the grid signal. The q component is fed to the PI controller and the output of PI controller is fed to the VCO.

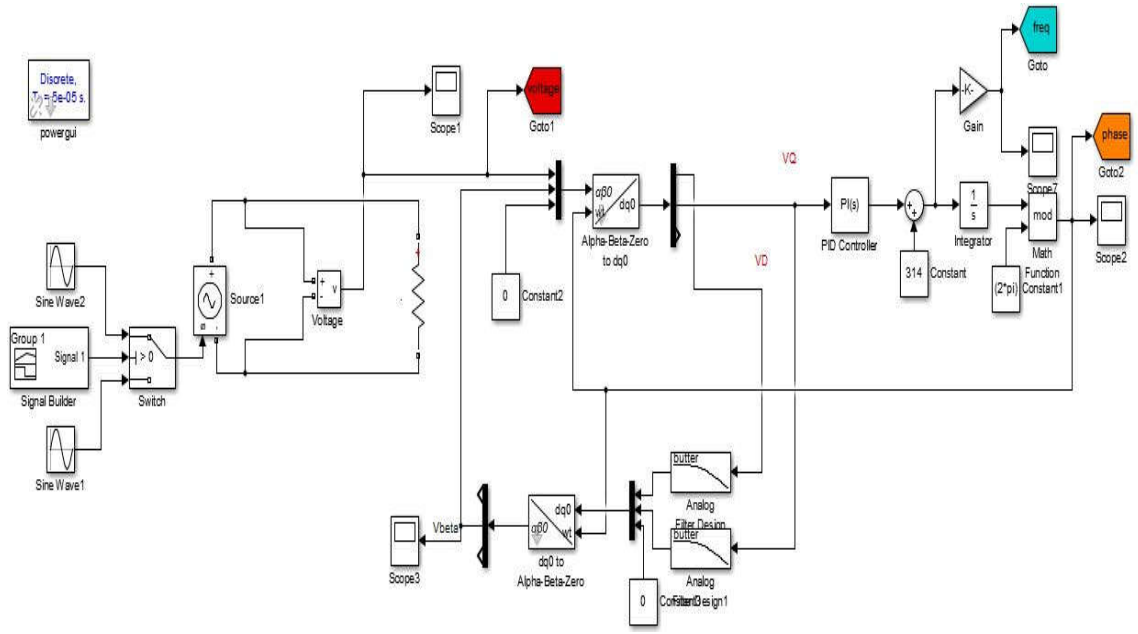

Figure 2.26 Simulation model of Inverse park PLL in MATLAB/SIMULINK environment

2.2.5.2 SIMULATION RESULTS

Figure 2.26 shows a simulation model of inverse park PLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and inverse park PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

The changes have been made at intervals t = 1 s till t = 1.4 s.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be observed that the PLL takes nearly 6-7 cycles to settle at 55 Hz and after t = 1.4 s the frequency reaches again to 50 Hz. It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

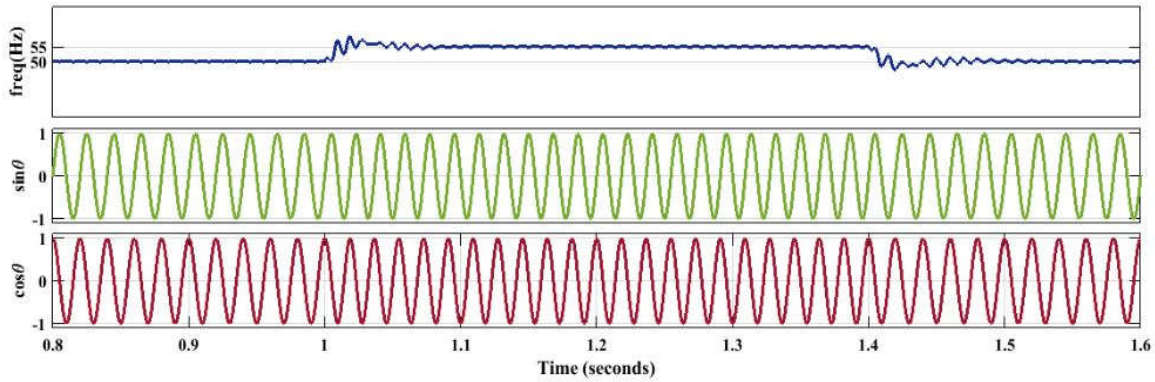

Figure 2.27: Inverse park PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

The voltage change has been made from 230 V to 110 V between t = 1 s till t = 1.4 s. It can be noted that the PLL tracks voltage and settles to 230 V after t = 1.4 s. The grid voltage is in synchronism with $\sin\theta$.

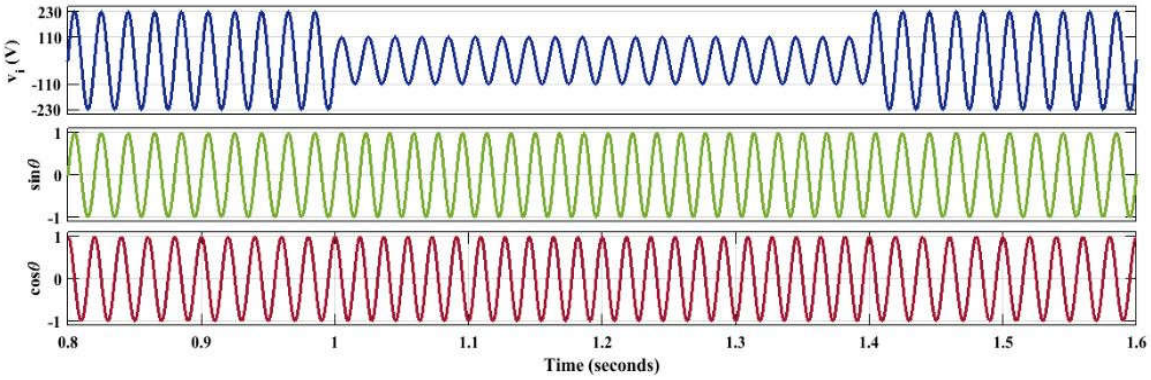

Figure 2.28: Inverse park PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 s to t = 1.4 s. Phase angle has been changed from 0 rad to pi rad. The grid voltage maintains synchronism and comes in phase with $\sin\theta$ when the phase angle is again changed to 0 rad.

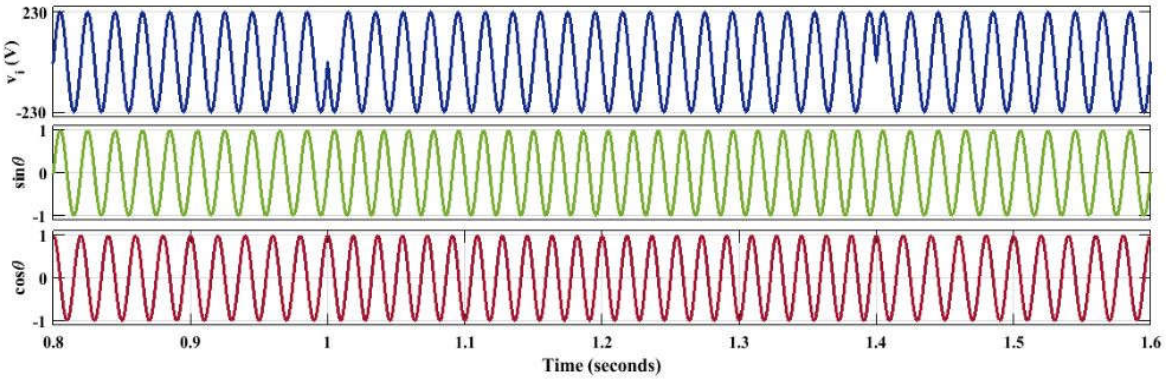

Figure 2.29: Inverse park PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced between t= 1 s till t= 1.4 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ are maintained in case of harmonics in the system.

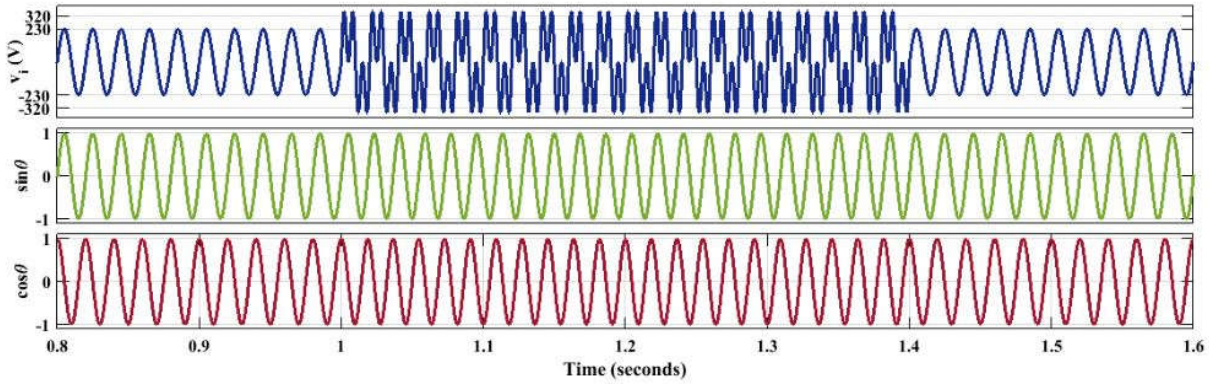

Figure 2.30: Inverse park PLL (effect of harmonics)

2.2.6 POWER PLL (pPLL)

pPLL is one of the simplest PLL techniques for synchronization. There has been ample amount of research on pPLL [22]-[25]. pPLL is one of the oldest methods used for synchronization.

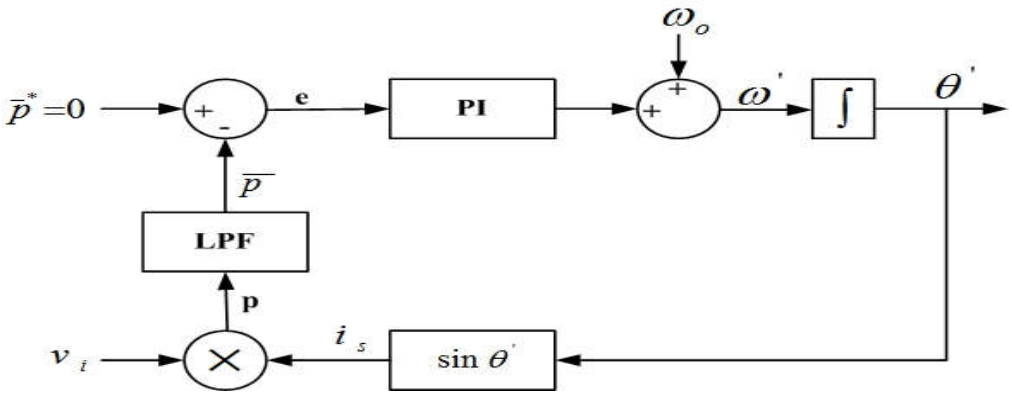

Figure 2.31: Schematic diagram of pPLL

2.2.6.1 ANALYSIS

The input voltage and sin θ are multiplied which gives us the power. This power is fed to a low pass filter which is used to extract mean power ($\overline{p}$), which is the first term of the equation (2.23) i.e. $\bar{p} = \frac{V}{2} sin(\theta' - \theta)$.

Let $v_i = Vcos\theta$ (2.21)

$p = Vcos\theta \, sin\,\theta'$ (2.22)

$p = \frac{V}{2} sin(\theta' - \theta) + \frac{V}{2} sin(\theta' + \theta)$ (2.23)

Suppose $\theta = \omega t + \emptyset$; $\theta' = \omega' t + \emptyset'$ and $\omega' \cong \omega$; for small phase differences $\emptyset - \emptyset'$, $\bar{p}$ can be estimated as:

$\bar{p} = \frac{V}{2}(\emptyset' - \emptyset)$ (2.24)

The above equation demonstrates the small signal static Phase detector gain. If we consider only a slight difference variation between θ and θ', equation (2.23) can be segregated into two parts:

$\frac{V}{2} sin(\theta' - \theta)$ (2.25)

which is a minute dc term and provides information about the phase difference between input signal and the output signal.

and

$$\frac{V}{2} sin(\theta' + \theta) \tag{2.26}$$

which is a double frequency disturbance term comprising of high-amplitude. It is extremely important to filter this double frequency component to keep up the phase jittering within an acceptable range. To cancel out the undesired double-frequency component from the fictitious power p, one can use either a first- (or second-) order LPF with a low cutoff frequency or a high-order LPF with a higher cutoff frequency. In addition to stability problems, using a high-order LPF imposes a high computational load on the control system. On the other hand, using a low-order LPF with a low cutoff frequency, significantly degrades the transient performance of the PLL. Another approach is to use a notch filter tuned at twice the input voltage fundamental frequency. Because of the grid frequency variations, the notch filter should be adaptive, which increases the system cost and complexity. Some improvements to the pPLL have been suggested in [7]-[21]. In these techniques, referred to as orthogonal signal generation (OSG)-based techniques, the fundamental component of the input voltage is shifted by 90° to generate a fictitious phase signal, thus making it possible to represent the single phase system as a pseudo two-phase (αβ) system. Applying the well-known park (αβ → dq) transformation to the two phase (αβ) system, yields the phase error information without generating the undesired double-frequency component. It should be noticed that the main difference among different OSG-based techniques lies in how the fictitious orthogonal signal is generated. In spite of their differences, all OSG-based techniques suffer from some common drawbacks, such as high sensitivity to the grid frequency variations, and relatively high complexity. To filter out the undesired steady-state double-frequency oscillations without degrading the stability and the transient performance of the PLL and, at the same time, to compensate for the input voltage amplitude variations, an effective method, called the DFAC method, is presented in the next section.

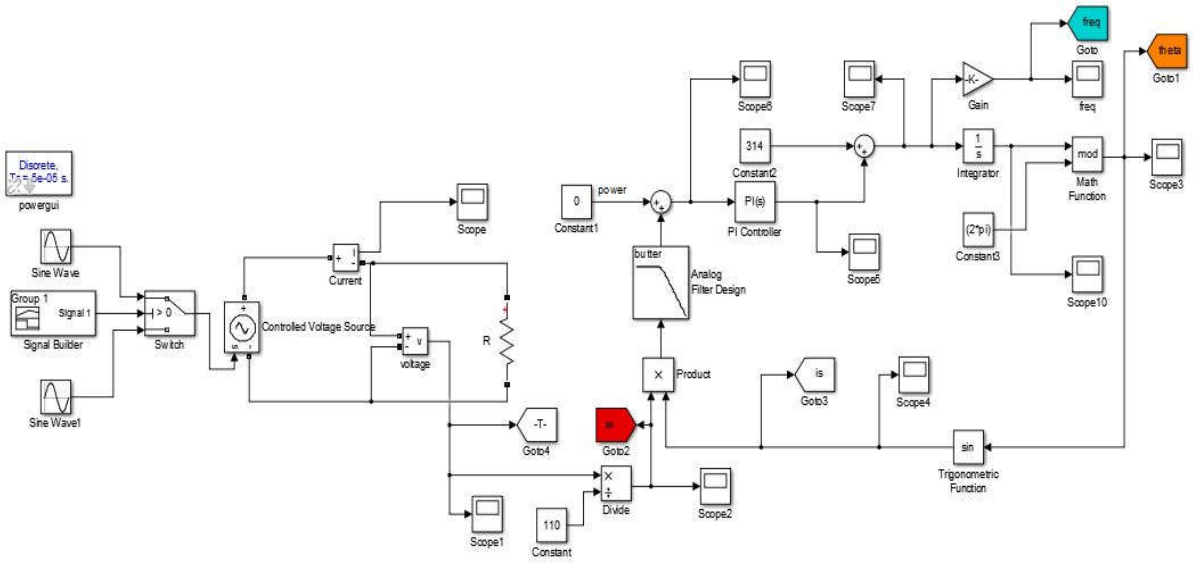

Figure 2.32 Simulation model of pPLL in MATLAB/SIMULINK environment

2.2.6.2 SIMULATION RESULTS

Figure 2.32 shows a simulation model of pPLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and pPLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 6-7 cycles to settle at 55 Hz and after t = 1.4 s the frequency reaches again to 50 Hz. It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

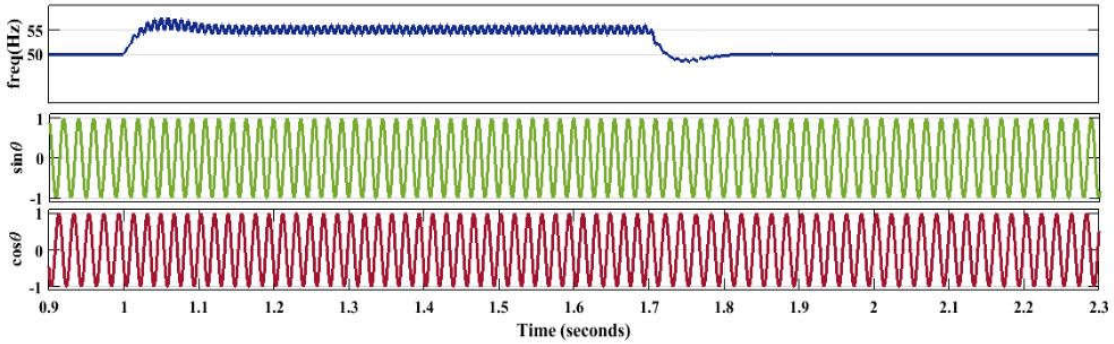

Figure 2.33: pPLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

The voltage change has been made from 230 V to 110 V between t = 1 second till t = 1.4 s. It can be noted that the PLL tracks voltage and settles to 230 V after t = 1.4 s.

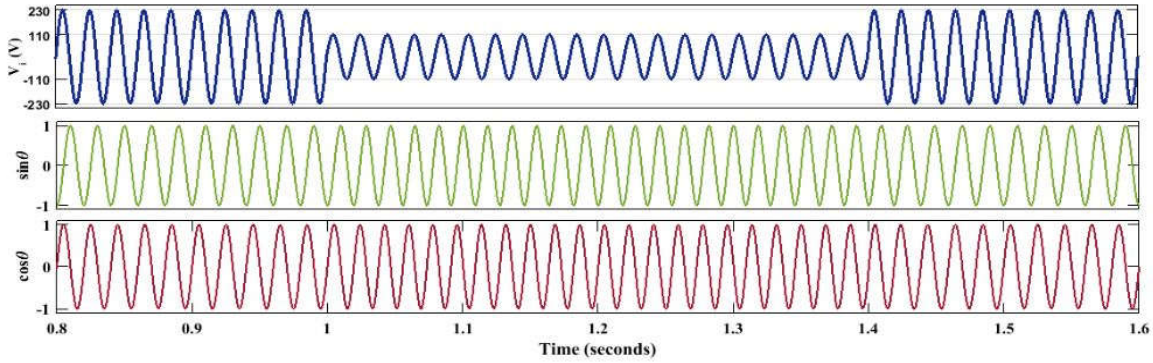

Figure 2.34: pPLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 s to t = 1.4 s. Phase angle has been changed from 0 radians to pi radians. The grid voltage maintains synchronism and comes in phase with $\cos\theta$ when the phase angle is again changed to 0 rad.

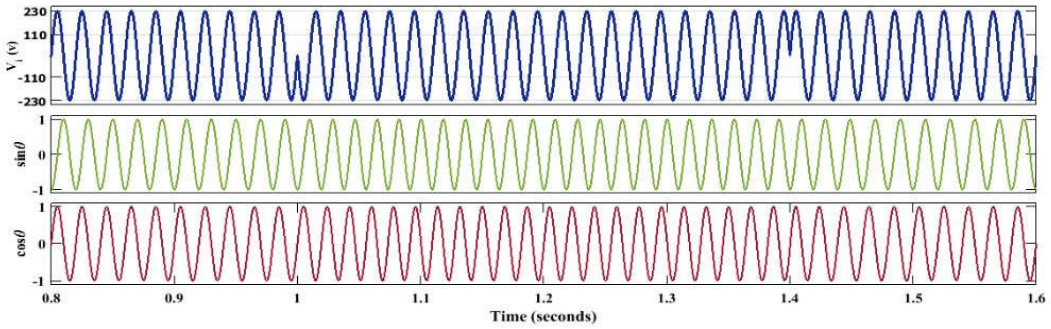

Figure 2.35: pPLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced between t= 1 s till t= 1.4 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ are maintained in case of harmonics in the system.

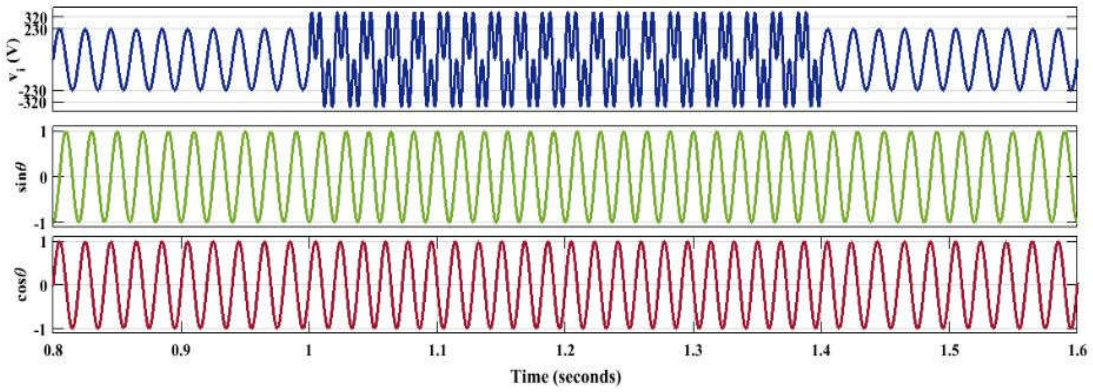

Figure 2.36: pPLL (effect of harmonics)

2.2.7 DOUBLE FREQUENCY AMPLITUDE COMPENSATION (DFAC) PLL

DFAC PLL is an advancement over conventional pPLL. The main advantage of having a DFAC PLL is that is eliminates the double frequency term which is associated with the conventional pPLL technique [26]-[27].

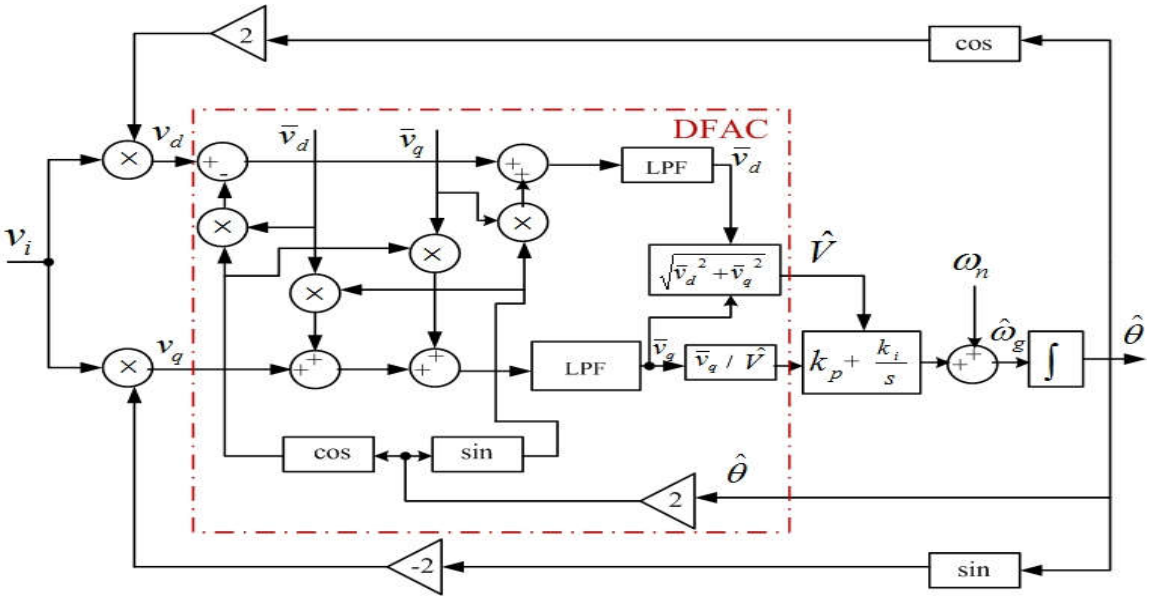

Figure 2.37: Schematic diagram of DFAC PLL

2.2.7.1 ANALYSIS

Fig.2.37 displays the basic scheme of the proposed phase detection unit, where $v_d$and v_q are obtained as expressed in the following equation:

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} cos\theta' & sin\,\theta' \\ -sin\,\theta' & cos\,\theta' \end{bmatrix} \begin{bmatrix} 2v_i(t) \\ 0 \end{bmatrix} \tag{2.27}$$

Substituting $v_i = V\,cos\,\theta$ into equation (2.27)

$$v_d(t) = V\,cos(\theta - \theta') + V\,cos(\theta + \theta') \tag{2.28}$$

$$v_q(t) = V\,sin(\theta - \theta') - V\,sin(\theta + \theta') \tag{2.29}$$

Considering $\theta_e = \theta - \theta'$ and after some simple mathematical manipulations, equations (2.28) and (2.29) can be written as :

$$v_d(t) = Vcos(\theta_e) + Vcos(2\theta' + \theta_e) \tag{2.30}$$

$$v_q(t) = Vsin(\theta_e) - Vsin(2\theta' + \theta_e) \tag{2.31}$$

Expanding the 2nd terms on the right hand side of the equations (2.30) and (2.31), yields:

$$v_d(t) = Vcos(\theta_e) + Vcos(\theta_e)\, cos(2\theta') - Vsin(\theta_e)sin(2\theta') \tag{2.32}$$

$$v_q(t) = Vsin(\theta_e) - Vsin(\theta_e)\, cos(2\theta') - V\, cos(\theta_e)\, sin(2\theta') \tag{2.33}$$

For a small angle difference θ_e , the first terms on the right hand side of the equations (2.32) and (2.33) (i.e., $V\, cos(\theta_e)$, and $Vsin(\theta_e)$ respectively) are almost dc components. It is also clear from the equations (2.32) and (2.33) that the amplitudes of the double-frequency components depend on these dc components. Thus, the perfect cancellation of the undesired double-frequency components can be easily achieved by injecting double-frequency signals with the same amplitude but an opposite angle into v_d and v_q, as shown in Fig 2.37. The proposed DFAC strategy consists of two main parts: a double-frequency cancellation block, and an amplitude compensation block. The low pass filter (LPF) block is considered as a first-order filter.

The LPF is as follows:

$$LPF(s) = \frac{\omega_p}{s+\omega_p} \tag{2.34}$$

where ω_p is the cut off frequency of the LPF.

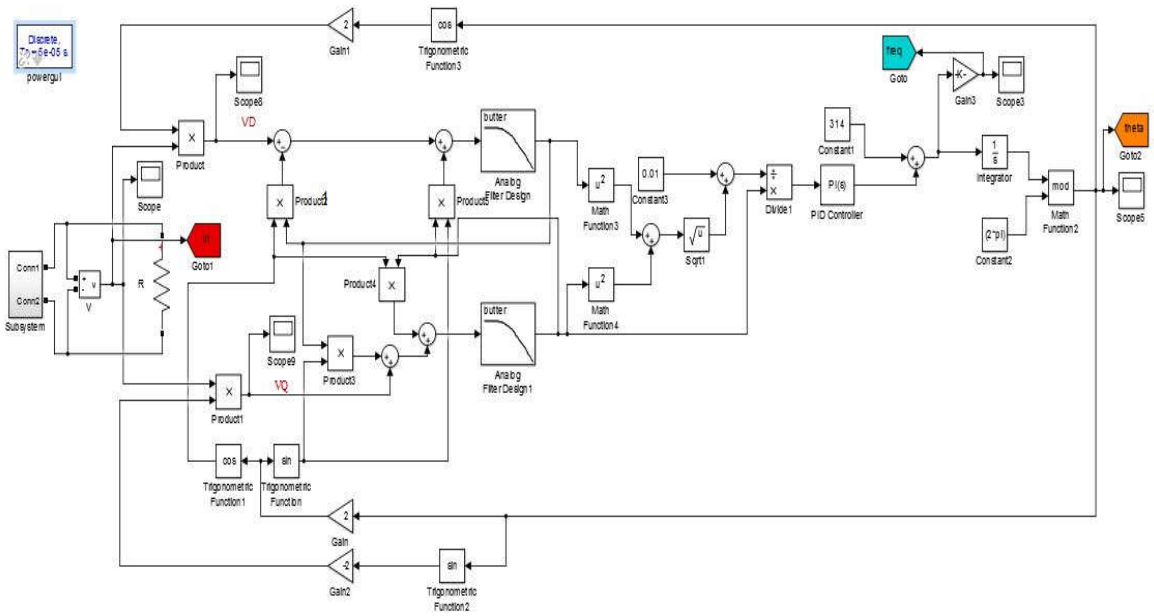

Figure 2.38 Simulation model of DFAC PLL in MATLAB/SIMULINK environment

2.2.7.2 SIMULATION RESULTS

Figure 2.38 shows a simulation model of DFAC PLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and DFAC PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 5-6 cycles to settle at 55 Hz and after t = 1.4 s the frequency reaches again to 50 Hz. It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

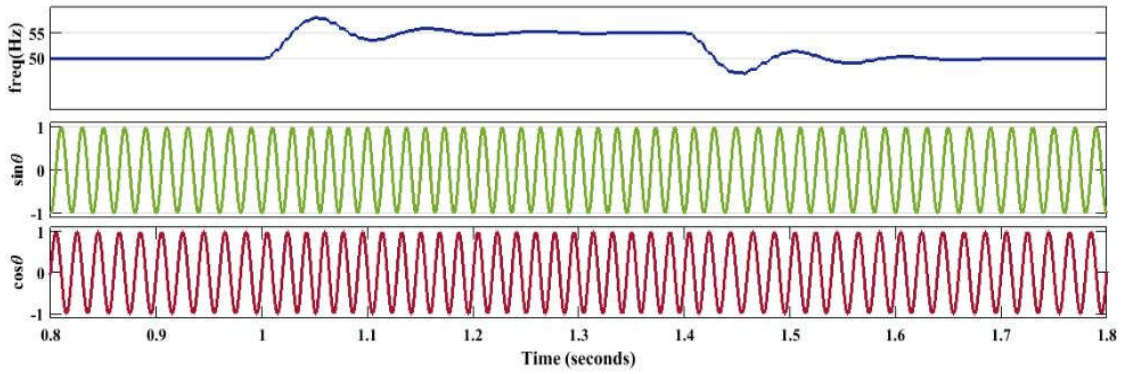

Figure 2.39: DFAC PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

The voltage change has been made from 230 V to 110 V between t = 1 second till t = 1.4 s. It can be noted that the PLL tracks voltage and settles to 230 V after t = 1.4 s.

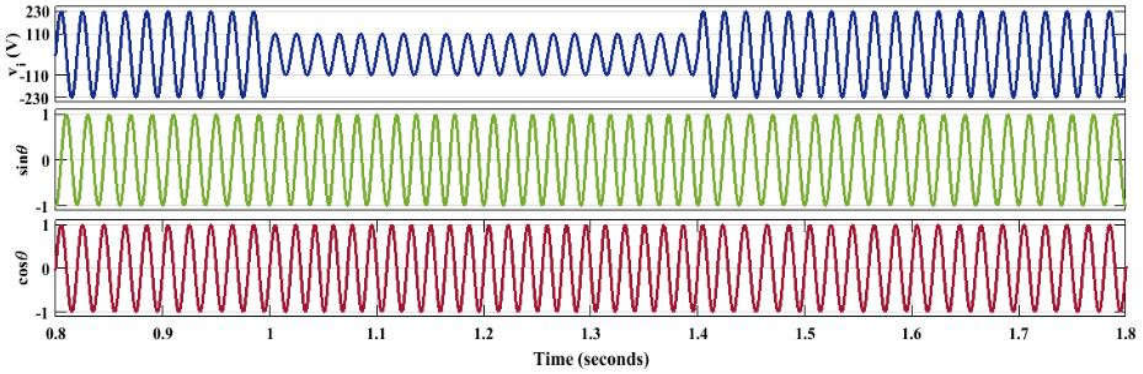

Figure 2.40: DFAC PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 second to t = 1.4 s. Phase angle has been changed from 0 radians to pi radians.

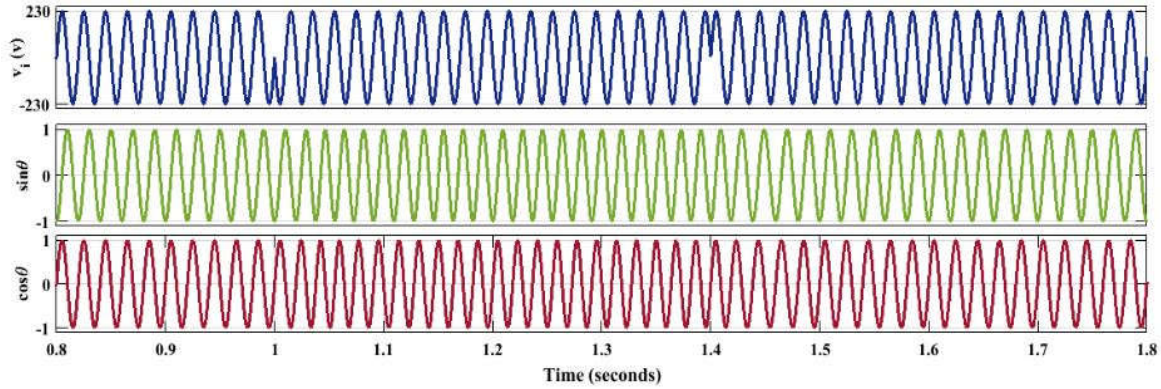

Figure 2.41: DFAC PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced from t= 1 second till t=1.4 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ are maintained in case of harmonics in the system.

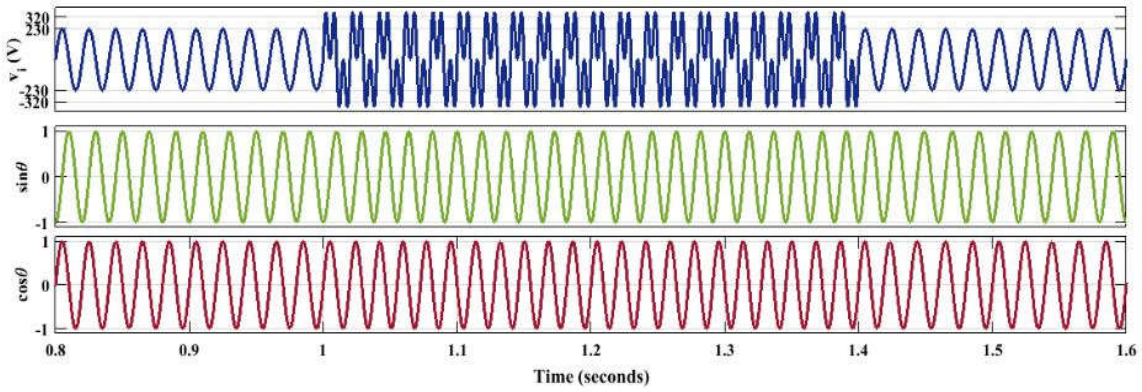

Figure 2.42: DFAC PLL (effect of harmonics)

2.3 COMPARISION

For every single phase PLL scheme, the PI controller is tuned for a certain value for accurate results. The proportional integral (PI) controller has two gains namely, proportional gain k_p and integral gain k_i. The optimum values of the gains is presented in Table-2.1.

TABLE 2.1. PI CONTROLLER GAINS

S.No	Single Phase PLL	k_p	k_i
1	Transport delay PLL	0.286	5.866
2	Adaptive transport delay PLL	0.2	5.7
3	EPLL	0.02	8
4	SOGI PLL	0.26	10
5	Inverse Park PLL	1	7
6	pPLL	0.2	8
7	DFAC PLL	0.2	5.78

For the comparison of different single phase PLL schemes mentioned in this chapter, a single phase system feeding a resistive load has been considered. The single phase PLL models were simulated under the same test conditions in the MATLAB/SIMULINK environment.

Four types of disturbances have been evaluated namely:

1 Frequency change

2 Voltage Amplitude change

3 Phase angle change, and

4 Effect of harmonics

The results of these changes have been thoroughly investigated with the single phase PLLs and a comparison has been made based on these observations. The comparisons have been made on the basis of various factors such as frequency/phase tracking, complexity of the circuit, oscillations, etc. The comparative results have been tabulated in table.2.2:

TABLE 2.2. COMPARISON OF SINGLE PHASE PLL SCHEMES

S.No	Single phase PLLs	Tracking (freq,Voltage,θ)	Complexity of the circuit	No. of cycles	Oscillations	Remarks
1.	Transport delay PLL	yes	low	6-7	yes	Medium settling time, few undamped oscillations
2.	Adaptive transport delay PLL	yes	low	14-15	no	High settling time, oscillations free
3.	EPLL	yes	medium	10-11	yes	High settling time and damped oscillations
4.	SOGI PLL	yes	medium	4-5	no	Low settling time and no oscillations

5.	Inverse park PLL	yes	medium	5-6	yes	Low settling time and very few oscillations
6.	pPLL	yes	low	6-7	yes	settles fast but oscillations undamped
7.	DFAC PLL	yes	high	10-11	no	Oscillation free but settling time large

2.4 CONCLUSIONS

This chapter presents the study of various single phase PLL schemes. The PLLs have been designed and tuned for optimum performance in single phase systems. After this, simulations have been performed to investigate the response under dynamic changes. A comparison has been made on the basis of several factors such as voltage amplitude change, frequency change, phase angle change and effect of harmonics. As can be seen from the figures, practically no oscillations were observed in SOGI-PLL case while tracking the new frequency. Transport Delay PLL is observed to have one of the simplest structure with no control parameter but its settling time is more than SOGI PLL. The performance of transport delay PLL is satisfactory only if the grid distortions are minimal with virtually no harmonics. EPLL has medium complexity and fairly satisfactory performance as its takes approximately 10-11 cycles to settle. The adaptive transport delay PLL has settling time greater than a transport delay PLL but the oscillations in the adaptive transport delay PLL are practically

zero. The inverse park transform PLL also has satisfactory performance as its settling time is quite less as compared to the other PLLs but it shows a few oscillations before it settles down. The pPLL has settling time less than the DFAC PLL but the pPLL shows constant oscillations which do not get damped. Hence, an appropriate PLL can be chosen and designed appropriately for tracking fast grid variations and a compromise can be made between various factors such as settling time, complexity of the circuit, oscillations etc.

CHAPTER 3

PHASE LOCKED LOOP TECHNIQUES FOR A THREE PHASE SYSTEM

3.1 INTRODUCTION

The use of different PLLs for single phase as well as three phase systems for PV interfaced grid connected systems is gaining high importance and studied in [4],[7]-[10]. High significance is assigned to designing simpler and effective synchronization schemes that will work well in harmonically polluted grid systems. Fast tracking ability should be ensured by the designed PLL under all varied conditions.

Here in this chapter various synchronization techniques based on phase locked loop applicable to a three phase system have been discussed. Design, modeling and simulation of the complete system along with the controller have been carried out in MATLAB/SIMULINK environment. Simulation results for different cases have been investigated which include the performance of these PLL under (i) Voltage amplitude change, (ii) Frequency change (iii) Phase change and (iv) Effect of harmonics. Comparative results have been tabulated for the different three phase PLL schemes. PLL techniques are gaining importance worldwide and the research conducted on synchronization techniques have been mentioned in the literature review in the chapter 1.

3.2 TYPES OF PHASE LOCKED LOOP TECHNIQUES APPLICABLE TO A THREE PHASE SYSTEM

In this chapter few of the three phase PLL techniques have been discussed. The most commonly used three phase PLL techniques are based on quadrature signal generation. The

quadrature signal generation is used to obtain a signal which is in quadrature with the original signal. There are a few methods which can be used to obtain the quadrature signal. Some of the methods have been discussed below:

3.2.1 THREE PHASE SYNCHRONOUS REFERENCE FRAME (SRF) PLL

Fig. 3.1 shows the schematic diagram of the conventional synchronous reference frame PLL (SRF-PLL) [29]-[33], which is a standard PLL in three-phase applications and the building block of almost all advanced PLLs.

The Phase detector (PD) in the SRF-PLL is implemented by applying the Clarke's transformation (abc → $\alpha\beta$) and then the Park's transformation ($\alpha\beta \rightarrow dq$)to the three-phase input signals.

The q-axis output of the PD, which contains the phase error information, is passed through the loop filter (i.e. the PI controller). The resultant signal, which is the estimated frequency, is applied to the VCO to provide an estimation of the phase angle.

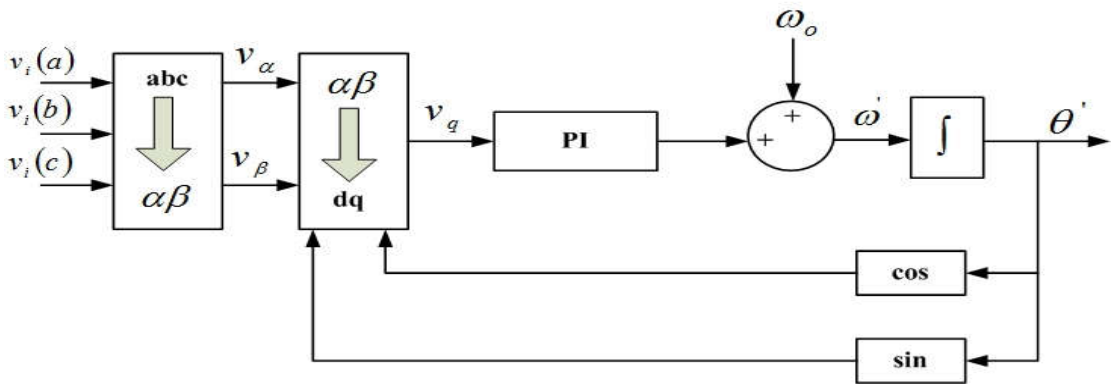

Figure 3.1: Schematic diagram of three phase SRF PLL

3.2.1.1 ANALYSIS

Assuming balanced and harmonic free input voltages, the expression of the *d*-axis component which is feed to the PI controller is:

$$v_d = v_\alpha \sin\theta' + v_\beta \cos\theta' \quad (3.1)$$

$$v_d = V \cos\theta \sin\theta' - V \sin\theta \cos\theta' \quad (3.2)$$

leading to

$$v_d = -V \sin(\theta - \theta') \quad (3.3)$$

where

v_d is the phase detector of the output signal.

V is the amplitude of input signal.

θ is the angle of phase A

θ' is the estimated angle.

Similarly, for q axis:

$$v_q = V \cos(\theta - \theta') \quad (3.4)$$

When θ' approximates θ , v_d component of the equation (3.3) will approximate to zero and the PLL will be in a locked state. In this situation, according to equation (3.4), v_q component will be equal to the input voltage amplitude.

In recent years, there have been many attempts to design more advanced three-phase PLLs. The majority of these efforts have focused on enhancing the disturbance rejection capability of the conventional SRF-PLL and its relatives so that they can deal with the ever increasing power quality issues in power systems. It is worth mentioning that these issues are mainly because of the proliferation of domestic and industrial nonlinear loads and the increased penetration of renewable energy sources to the power grid. Other efforts in the field have been mainly on improving the dynamic behavior and changing the steady-state characteristics of the conventional SRF-PLL and its relatives.

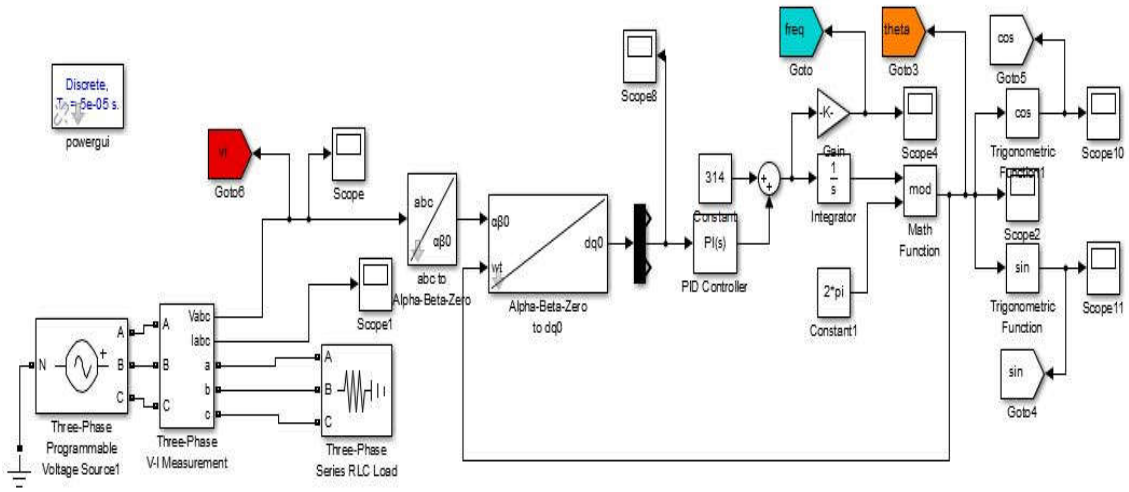

Figure 3.2 Simulation model of three phase SRF PLL in MATLAB/SIMULINK environment

3.2.1.2 SIMULATION RESULTS

Figure 3.2 shows a simulation model of three phase SRF PLL in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and three phase SRF PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 3-4 cycles to settle at 55 Hz and after t = 1.7 s the frequency reaches again to 50 Hz. It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

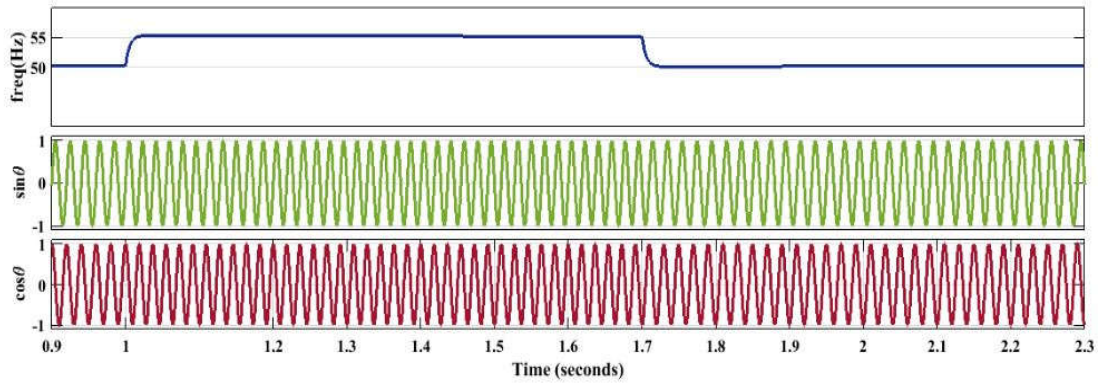

Figure 3.3: Three phase SRF PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

A voltage change has been given by providing a step change of 1 per unit between t = 1 s till t = 1.1 s. It can be noted that the PLL tracks voltage and settles to the original value after t = 1.1 s. Phase A of the grid voltage is in phase with $\sin\theta$.

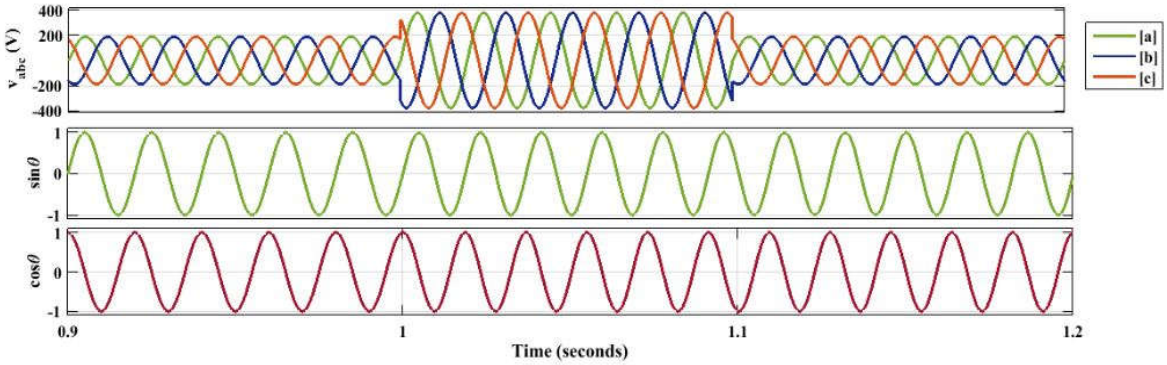

Figure 3.4: Three phase SRF PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 s to t = 1.4 s. Phase angle has been changed from 0 radians to pi radians for all the three phases. The SRF PLL tracks the phase angle change.

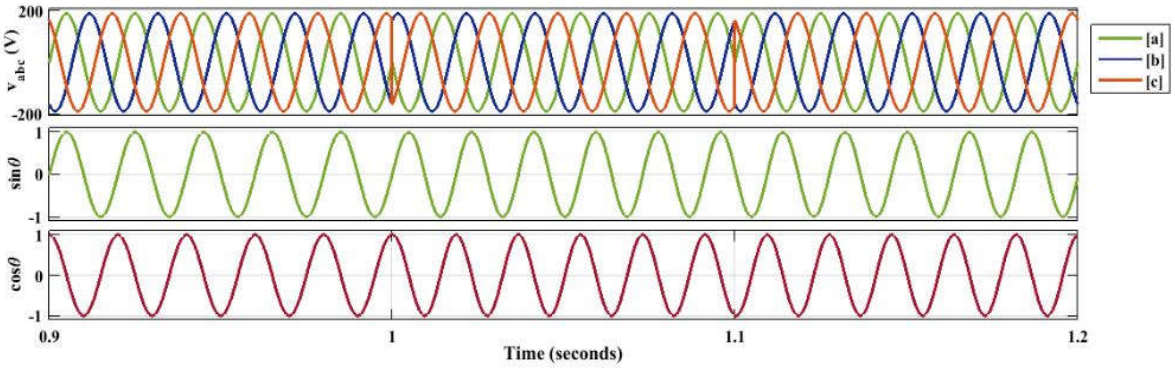

Figure 3.5: Three phase SRF PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced from t= 1 s till t=1.1 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ has been obtained even when the system is polluted with harmonics.

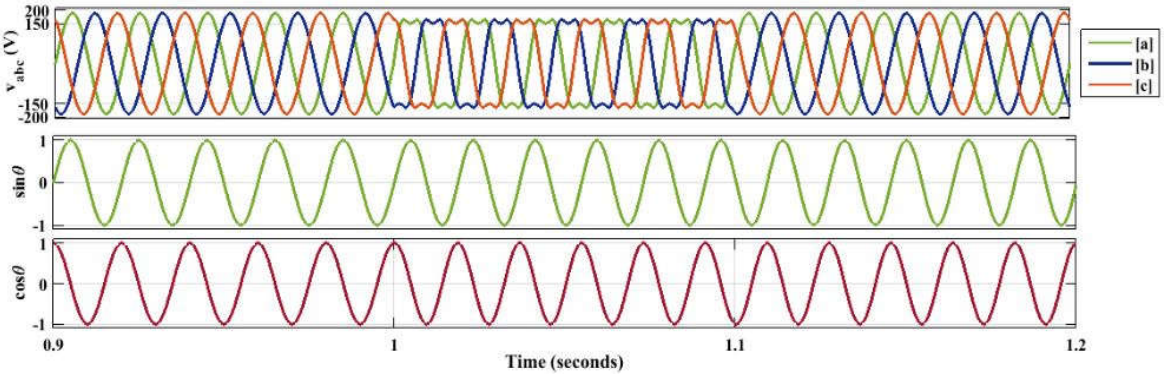

Figure 3.6: Three phase SRF PLL (effect of harmonics)

3.2.2 THREE PHASE ENHANCED PLL (EPLL)

The SRF-PLL as discussed above employs a synchronous rotating frame transformation (Park transformation) to transform the three input signals from a three-phase stationary frame into a two phase SRF. The three-phase inputs converting into two dc components that can be closed-loop controlled to track the phase angle and frequency of the input signals. It should be indicated that the Park transformation increases the calculation burden of the digital controller. Moreover, EPLL adds an amplitude loop into the standard PLL with both the amplitude estimated and a fast dynamic response of the frequency and phase angle achieved. EPLL has found wide acceptance due to its simple structure, robust performance, and ability to estimate signal parameters directly. However, since EPLL is implemented under a three-phase stationary frame, a relatively complex calculation is introduced by the trigonometric and multiplying operation of three phases [40],[41].

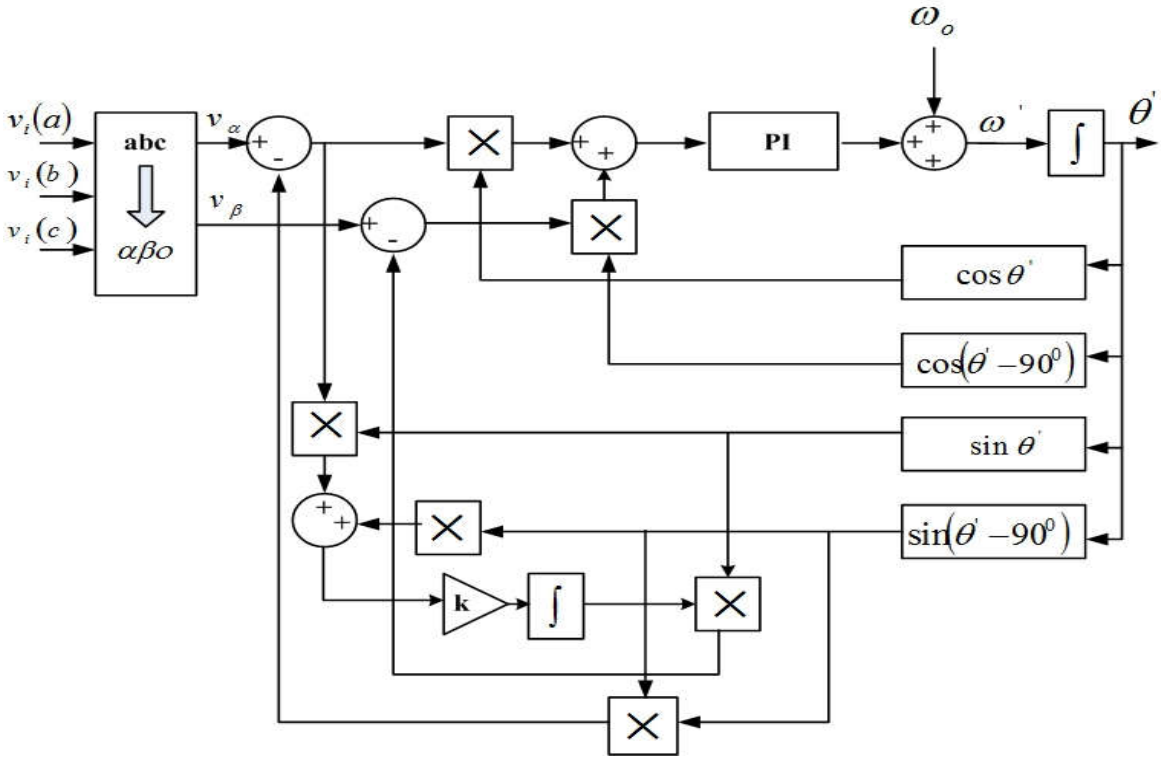

Figure 3.7: Schematic diagram of three phase EPLL

3.2.2.1 ANALYSIS

Figure 3.7 shows a schematic diagram of three phase EPLL. An ideal three-phase set of input signals is given by:

$$v_a = A\,sin(\omega t + \emptyset) \tag{3.5}$$

$$v_b = A\,sin(\omega t + \emptyset - 120^0) \tag{3.6}$$

$$v_c = A\,sin(\omega t + \emptyset + 120^0) \tag{3.7}$$

where A is the amplitude,

ω is the frequency and

$\emptyset$ is the initial phase angle of input signal.

v_{abc} can be converted into $v_{\alpha\beta 0}$ by using transformation:

$$T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.8}$$

After that, signals under the $\alpha\beta$ frame are derived as

$$v_\alpha = A\,sin(\omega t + \emptyset) \tag{3.9}$$

$$v_\beta = A\,sin(\omega t + \emptyset - 90^0) \tag{3.10}$$

The $\alpha\beta$ components so obtained are utilized in the phase detector of the PLL. The output of PD is fed to PI controller which is then fed to the VCO.

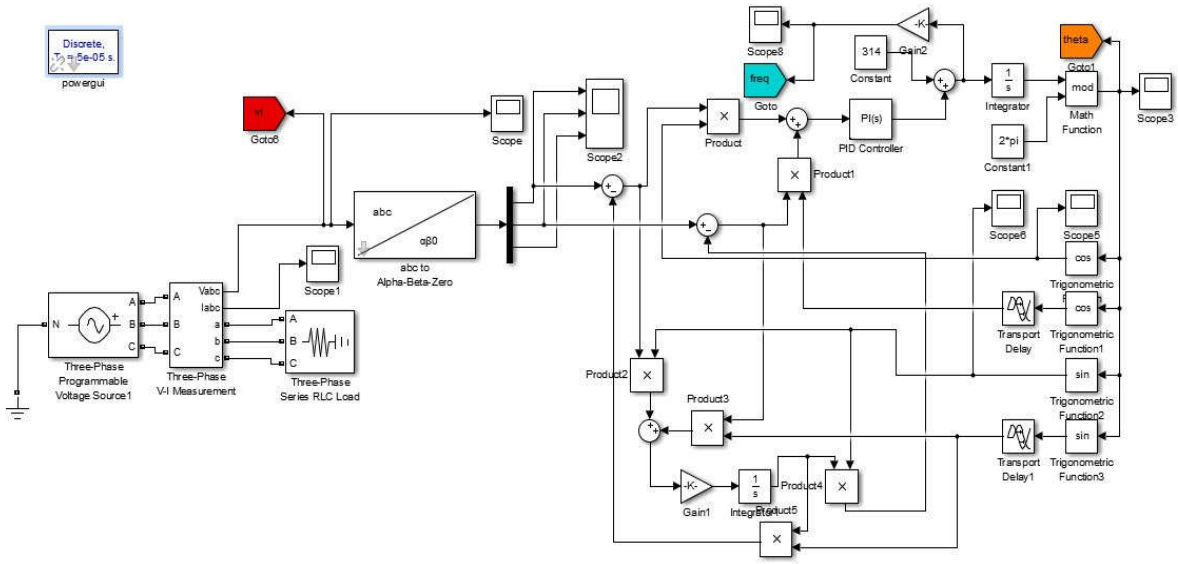

Figure 3.8 Simulation model of three phase EPLL in MATLAB/SIMULINK environment

3.2.2.2 SIMULATION RESULTS

Figure 3.8 shows a simulation model of three phase EPLL in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and three phase EPLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

The results have been taken for frequency change, voltage amplitude change, phase angle change and effect of harmonics.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 18-20 cycles to settle at 55 Hz and after t = 1.7 s the frequency reaches again to 50 Hz. It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

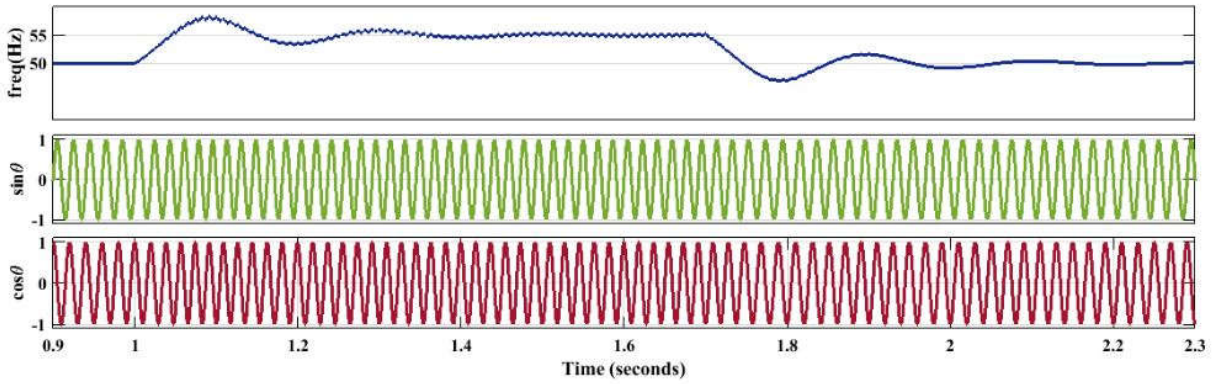

Figure 3.9: Three Phase EPLL (Frequency Change)

(b) VOLTAGE AMPLITUDE CHANGE

A voltage change has been given by providing a step change of 1 per unit between t = 1 s till t = 1.1 s. It can be noted that the PLL tracks voltage and settles to the original value after t = 1.1 s.

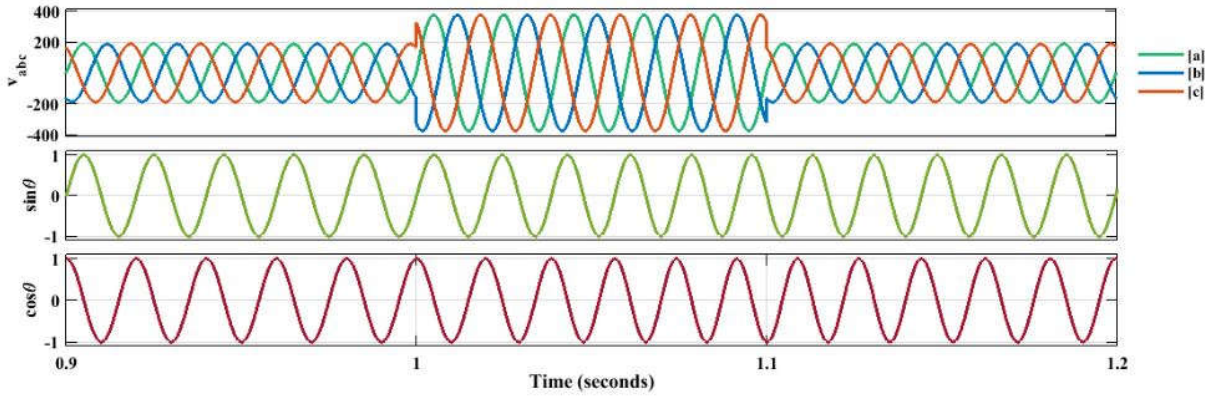

Figure 3.10: Three Phase EPLL (voltage amplitude Change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 s to t = 1.1 s. Phase angle of all the three phases has been changed from 0 radians to pi radians.

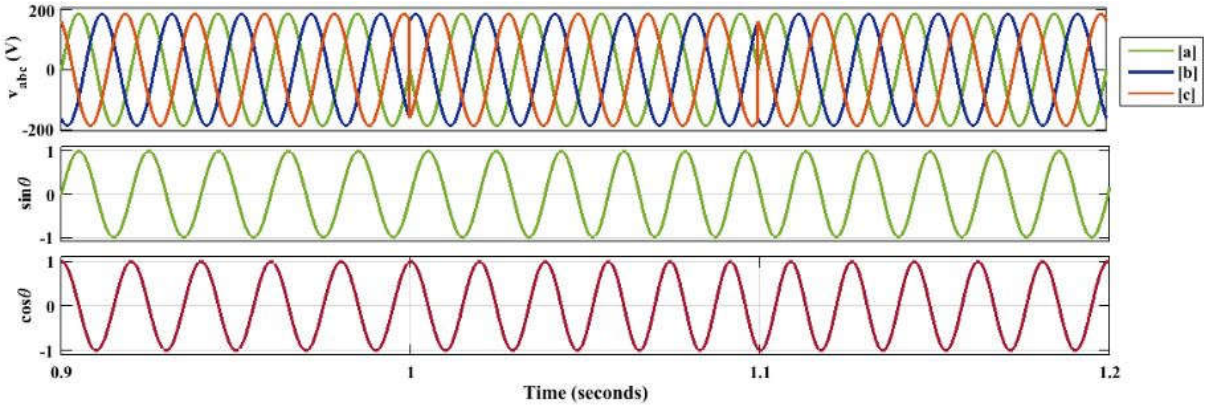

Figure 3.11: Three Phase EPLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced from t= 1 second till t=1.1 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ has been obtained even when the system is polluted with harmonics.

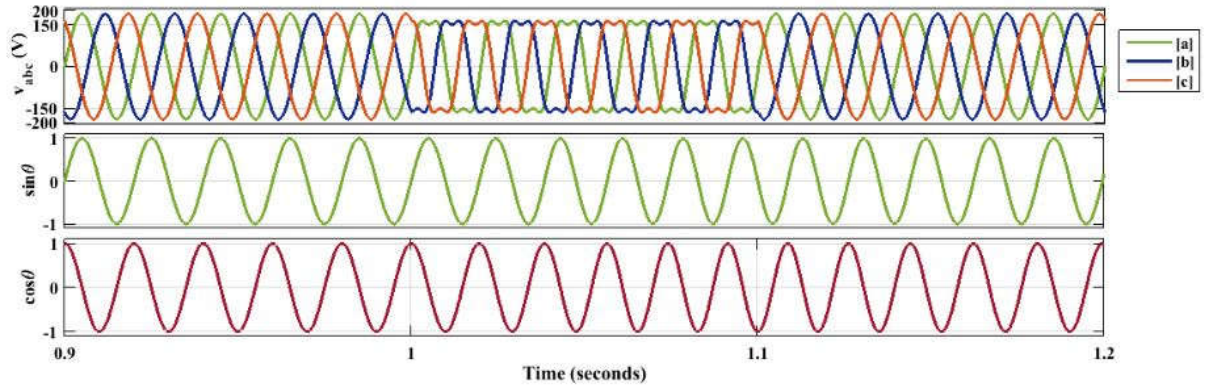

Figure 3.12: Three Phase EPLL (effect of harmonics)

3.2.3 THREE PHASE INVERSE PARK PLL

For the simulation of a three phase inverse park transform PLL, a three phase source is acquired. With the help of Clarke's transformation (abc→ αβ0), the three voltage components of the phase a, b and c are converted into αβ0 components. The αβ components re converted into dq components.

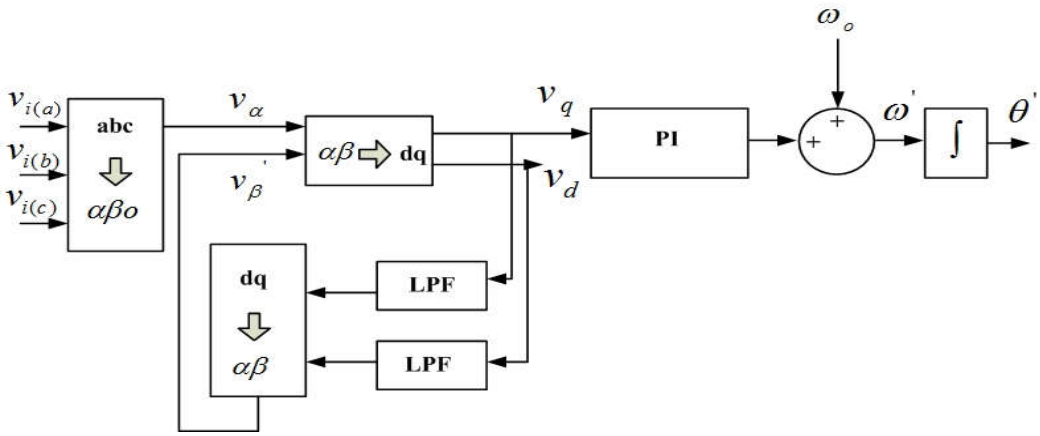

Figure 3.13: Schematic diagram of a three phase Inverse park PLL

3.2.3.1 ANALYSIS

In three phase Inverse park PLL method to build an orthogonal signal generator, which is supposed to generate the 'β' component, a loop consisting of direct as well as indirect Park's transform supported by two low pass filters is created as shown in Fig.3.13. But here the condition is the PLL should be perfectly tuned to the input frequency to make v_α to be in phase with v_α and in quadrature with v_β [19]-[21]. Also, the nonlinear inner loop must be fast enough to generate the 'β' component.

The whole technique can be described by these set of equations:

$$v_{dq}(s) = \begin{bmatrix} v_d(s) \\ v_q(s) \end{bmatrix} = T_p \begin{bmatrix} v_i(s) \\ v'_\beta(s) \end{bmatrix} \tag{3.11}$$

$$v_{\alpha\beta}(s) = \begin{bmatrix} v'_{\alpha}(s) \\ v'_{\beta}(s) \end{bmatrix} = T_p^{-1} \begin{bmatrix} v'_{d}(s) \\ v'_{q}(s) \end{bmatrix} \tag{3.12}$$

$$\begin{bmatrix} v'_{d}(s) \\ v'_{q}(s) \end{bmatrix} = G_L(s) \begin{bmatrix} v_{d}(s) \\ v_{q}(s) \end{bmatrix} = \frac{\omega}{s+\omega_L} \begin{bmatrix} v_{d}(s) \\ v_{q}(s) \end{bmatrix} \tag{3.13}$$

where T_p is

$$\begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{3.14}$$

Two LPFs are employed to filter out unwanted parts of dq components. The filtered components are used to produce the quadrature signal with respect to the grid signal. The q component is fed to the PI controller and the output of PI controller is fed to the VCO.

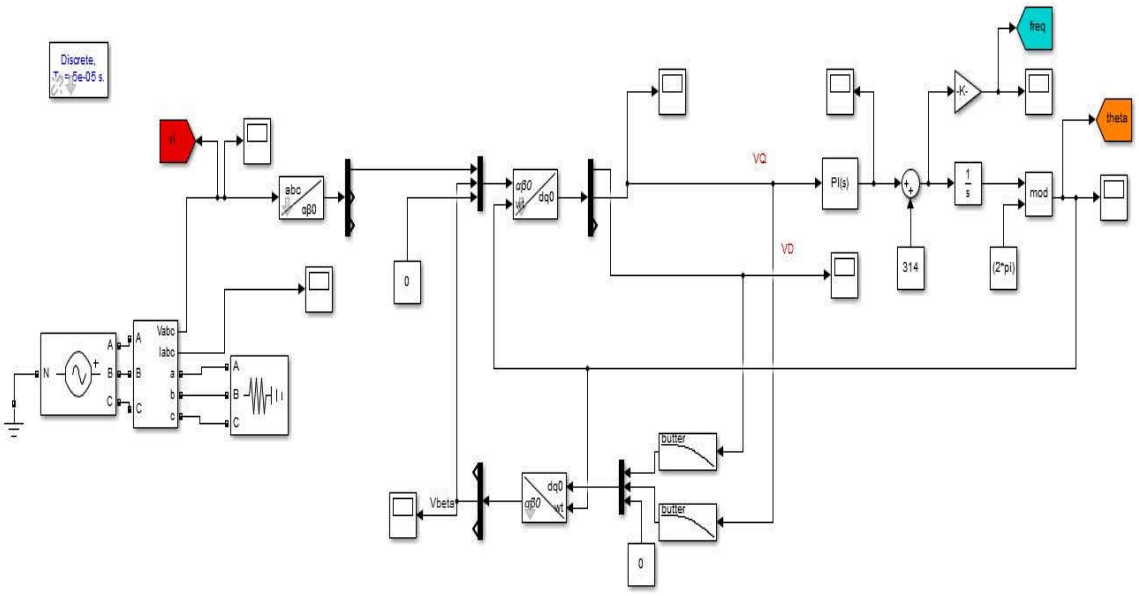

Figure 3.14 Simulation model of a three phase inverse park PLL in MATLAB/SIMULINK environment

3.2.3.2 SIMULATION RESULTS

Figure 3.14 shows a simulation model of a three phase inverse park PLL in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and three phase inverse park PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 6-7 cycles to settle at 55 Hz and after t = 1.7 s the frequency reaches again to 50 Hz. It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

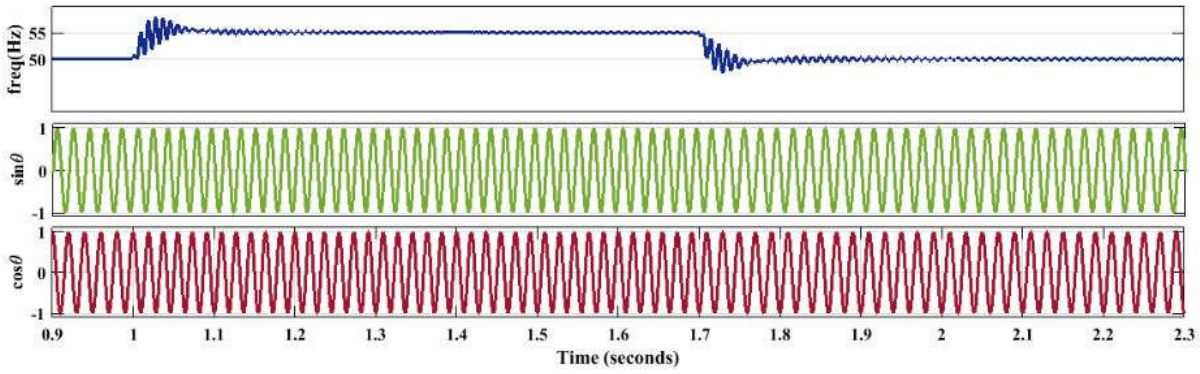

Figure 3.15: Three Phase inverse park PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

A voltage change has been given by providing a step change of 1 per unit between t = 1 second till t = 1.1 s. It can be noted that the PLL tracks voltage and settles to the original value after t = 1.1 s.

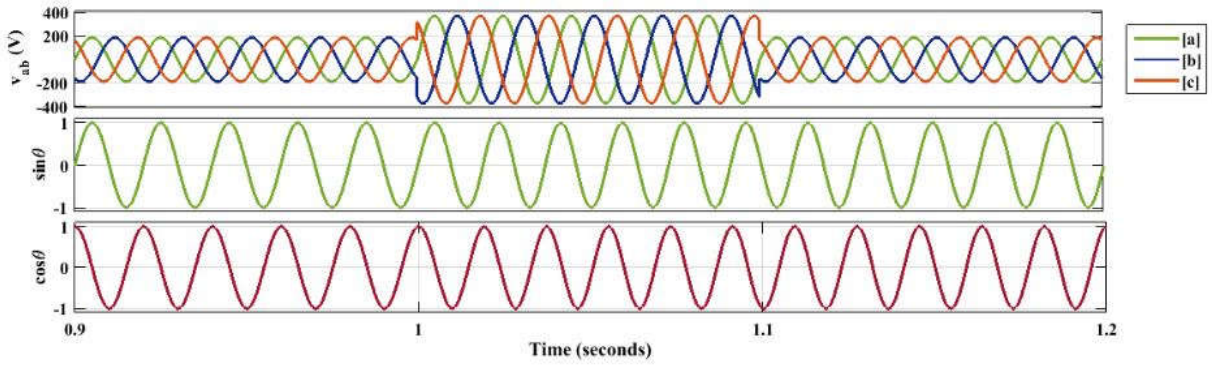

Figure 3.16: Three Phase inverse park PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 second to t = 1.1 s. Phase angle has been changed from 0 radians to pi radians.

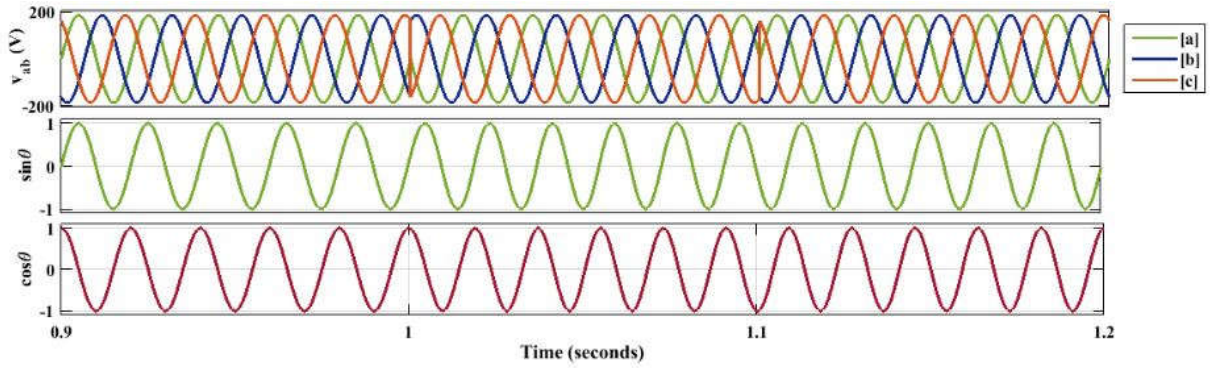

Figure 3.17: Three Phase inverse park PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced from t= 1 second till t=1.1 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ has been obtained even when the system is polluted with harmonics.

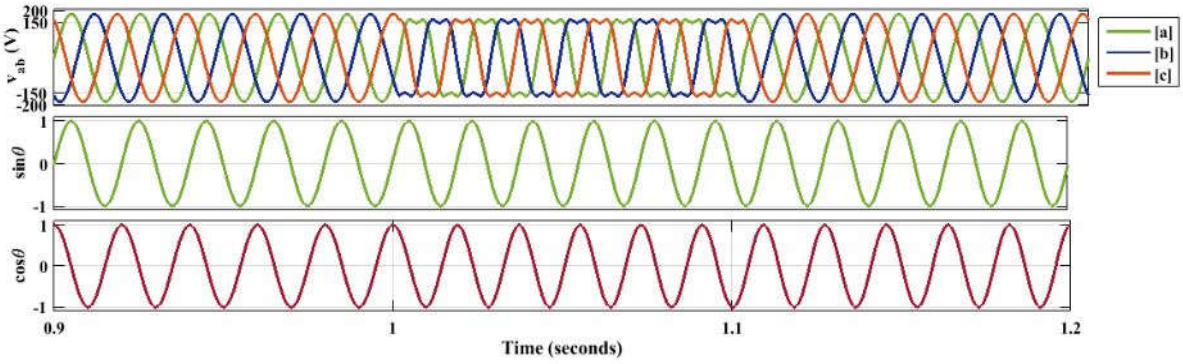

Figure 3.18: Three Phase inverse park PLL (effect of harmonics)

3.2.4 THREE PHASE pPLL

The block diagram of the three-phase pPLL [42]-[44] is shown in Fig. 3.19. The working principle of its phase detector is based on regulating to zero the fictitious instantaneous three phase power.

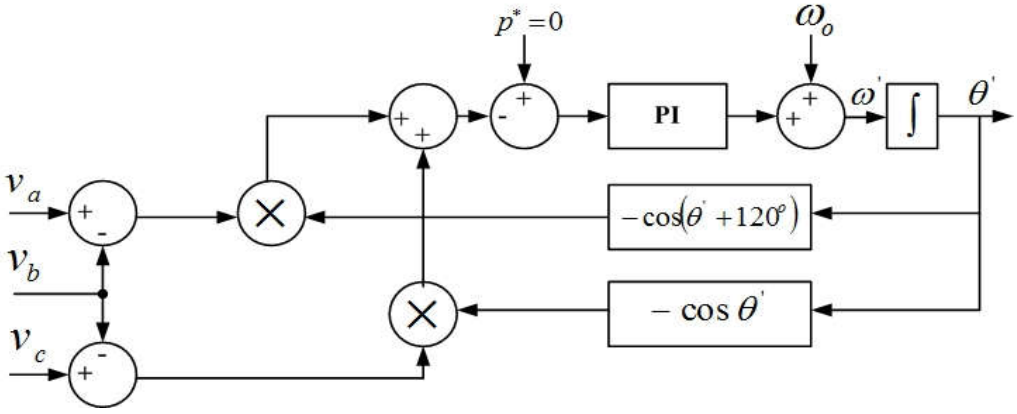

Figure 3.19: Schematic diagram of three phase pPLL

3.2.4.1 ANALYSIS

The fictitious instantaneous three phase power is calculated using the voltages samples and the fictitious currents i_a and i_c depicted in Fig. 3.19 and generated through the estimated angle θ'

It is known that,

$$p = v_a i_a + v_b i_b + v_c i_c \tag{3.15}$$

Since,

$$i_a + i_b + i_c = 0 \tag{3.16}$$

$$p = (v_a - v_b) i_a + (v_c - v_b) i_c \tag{3.17}$$

Substituting:

$$v_a = V \sin\theta, \tag{3.18}$$

$$v_b = V \sin\left(\theta - \frac{2\pi}{3}\right), \tag{3.19}$$

and

$$v_c = V \sin\left(\theta + \frac{2\pi}{3}\right) \tag{3.20}$$

Simplifying the above equations,

$$p = -\frac{3}{2} V \sin(\theta - \theta') \tag{3.21}$$

The k_p and k_i gains determine the speed of response and disturbance rejection of the PLL in a direct relation. However, there is a tradeoff between noise, harmonic and voltage unbalance rejection and speed of response. The higher the gains, the worse the noise, harmonic and line unbalance rejection. The adequate bandwidth will depend on the application purposes.

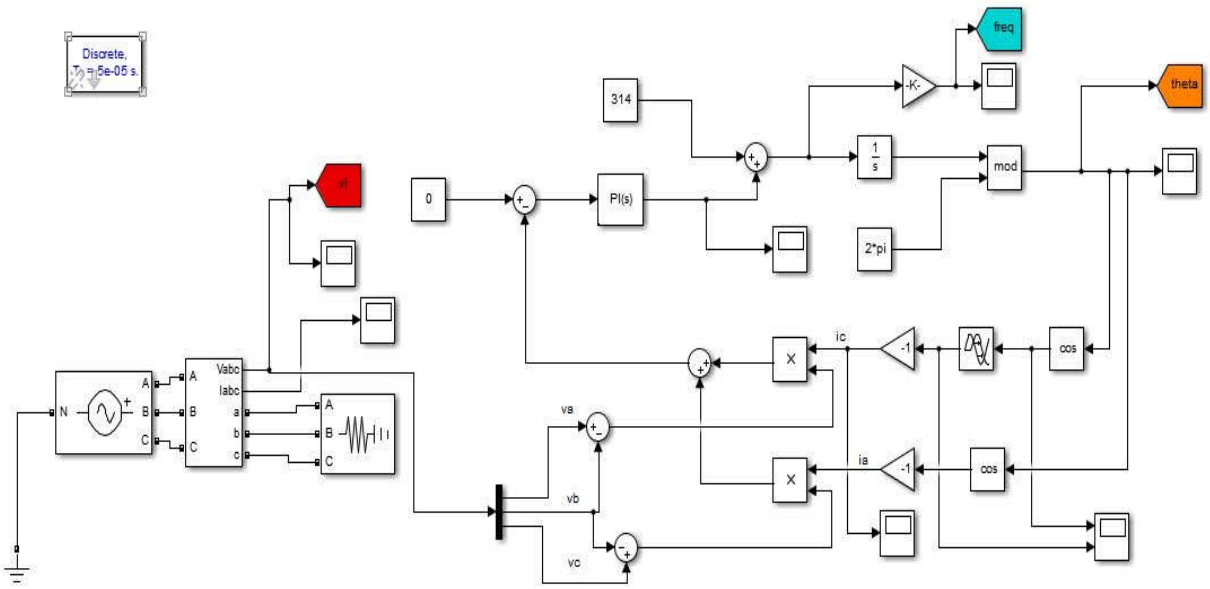

Figure 3.20 Simulation model of three phase pPLL in MATLAB/SIMULINK environment

3.2.4.2 SIMULATION RESULTS

Figure 3.20 shows a simulation model of a three phase pPLL in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and three phase pPLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 4-5 cycles to settle at 55 Hz and after t = 1.7 s the frequency reaches again to 50 Hz. It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

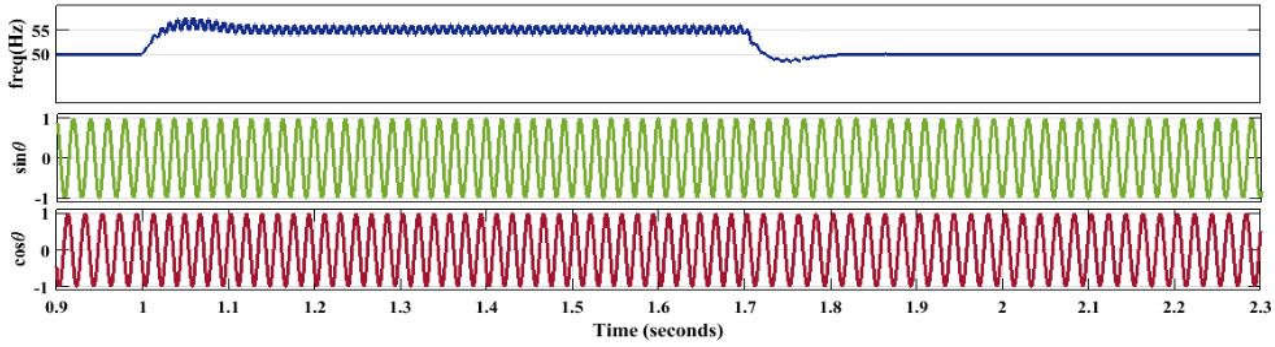

Figure 3.21: Three Phase pPLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

A voltage change has been given by providing a step change of 1 per unit between t = 1 second till t = 1.1 s. It can be noted that the PLL tracks voltage and settles to the original value after t = 1.1 s. Phase A is in phase with $\sin\theta$.

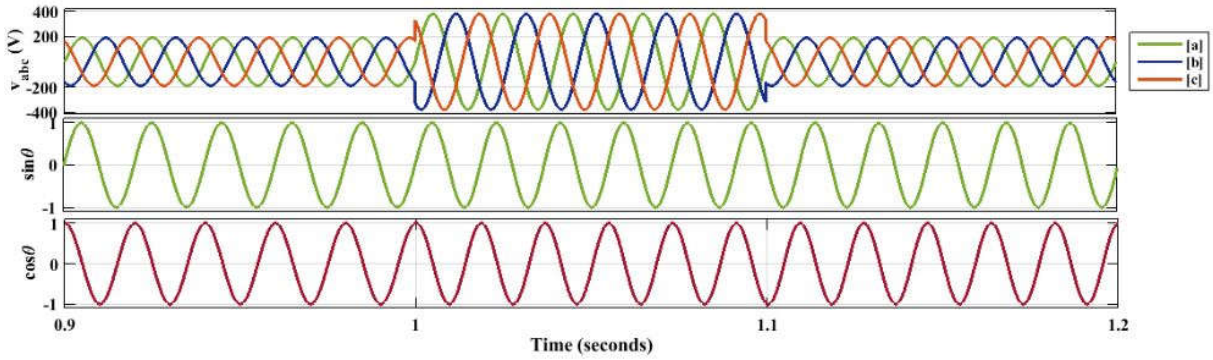

Figure 3.22: Three Phase pPLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 second to t = 1.1 s. Phase angle has been changed from 0 radians to pi radians.

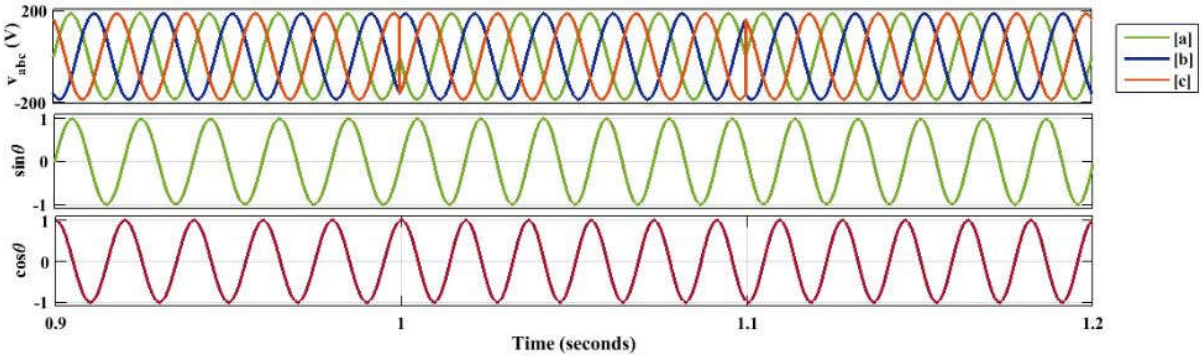

Figure 3.23: Three Phase pPLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced from t= 1 second till t=1.1 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ has been obtained even when the system is polluted with harmonics.

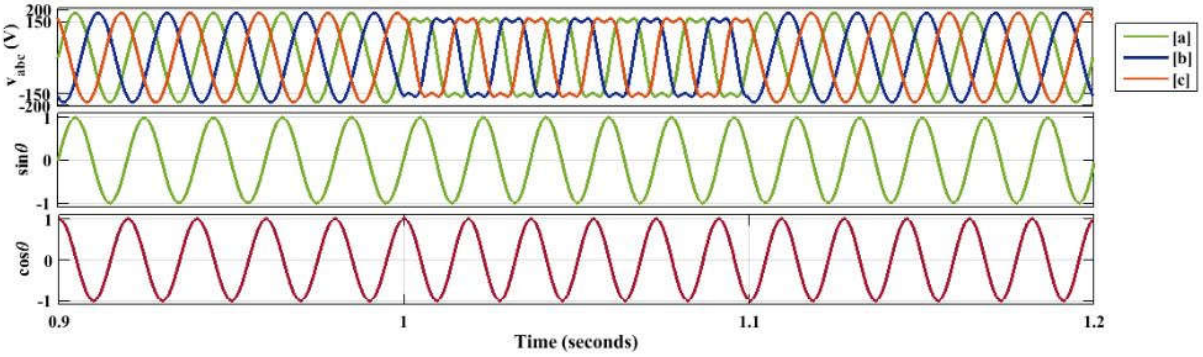

Figure 3.24: Three Phase pPLL (effect of harmonics)

3.2.5 THREE PHASE DFAC PLL

Fig.3.25 displays the basic scheme of the three phase DFAC PLL. For the simulation of a three phase DFAC PLL, a three phase source is acquired. With the help of Clarke's transformation (abc→ $\alpha\beta0$), the three voltage components of the phase a, b and c are converted into $\alpha\beta0$ components.

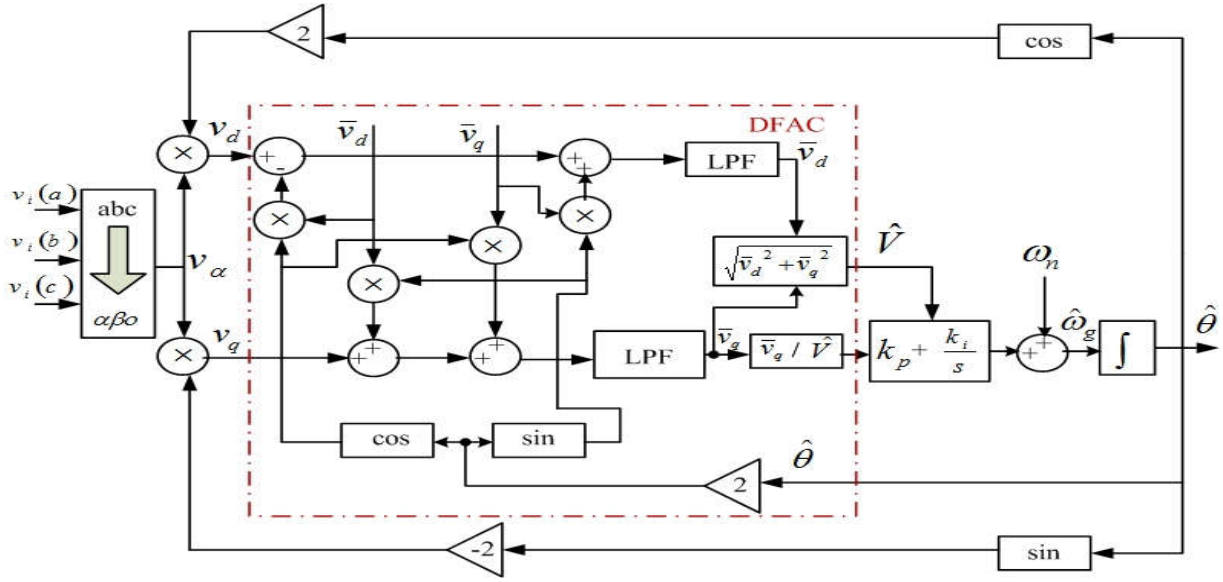

Figure 3.25: Schematic diagram of three phase DFAC PLL

3.2.5.1 ANALYSIS

The phase detection unit, where v_d and v_q are obtained as expressed in the following equation:

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} cos\theta' & sin\,\theta' \\ -sin\,\theta' & cos\,\theta' \end{bmatrix} \begin{bmatrix} 2v_i(t) \\ 0 \end{bmatrix} \tag{3.22}$$

Substituting $v_i = V\,cos\,\theta$ into equation (3.22)

$$v_d(t) = V\,cos(\theta - \theta') + V\,cos(\theta + \theta') \tag{3.23}$$

$$v_q(t) = V\,sin(\theta - \theta') - V\,sin(\theta + \theta') \tag{3.24}$$

Considering $\theta_e = \theta - \theta'$ and after some simple mathematical manipulations, (3.23) and (3.24) can be written as :

$$v_d(t) = Vcos(\theta_e) + Vcos(2\theta' + \theta_e) \tag{3.25}$$

$$v_q(t) = Vsin(\theta_e) - Vsin(2\theta' + \theta_e) \tag{3.26}$$

Expanding the 2nd terms on the right hand side of (3.25) and (3.26), yields:

$$v_d(t) = Vcos(\theta_e) + Vcos(\theta_e)\,cos(2\theta') - Vsin(\theta_e)sin(2\theta') \quad (3.27)$$

$$v_q(t) = Vsin(\theta_e) - Vsin(\theta_e)\,cos(2\theta') - V\,cos(\theta_e)\,sin(2\theta') \quad (3.28)$$

For a small angle difference θ_e , the first terms on the right hand side of the equations (3.27) and (3.28) (i.e., $V\,cos(\theta_e)$, and $Vsin(\theta_e)$ respectively) are almost dc components. It is also clear from the equations (3.27) and (3.28) that the amplitudes of the double-frequency components depend on these dc components. Thus, the perfect cancellation of the undesired double-frequency components can be easily achieved by injecting double-frequency signals with the same amplitude but an opposite angle into v_d and v_q [26]-[27], as shown in Fig 3.25. The three phase DFAC strategy consists of two main parts: a double-frequency cancellation block, and an amplitude compensation block. The LPF block is considered as a first-order filter.

LPF is as follows:

$$LPF(s) = \frac{\omega_p}{s+\omega_p} \quad (3.29)$$

where ω_p is the cut off frequency of the LPF.

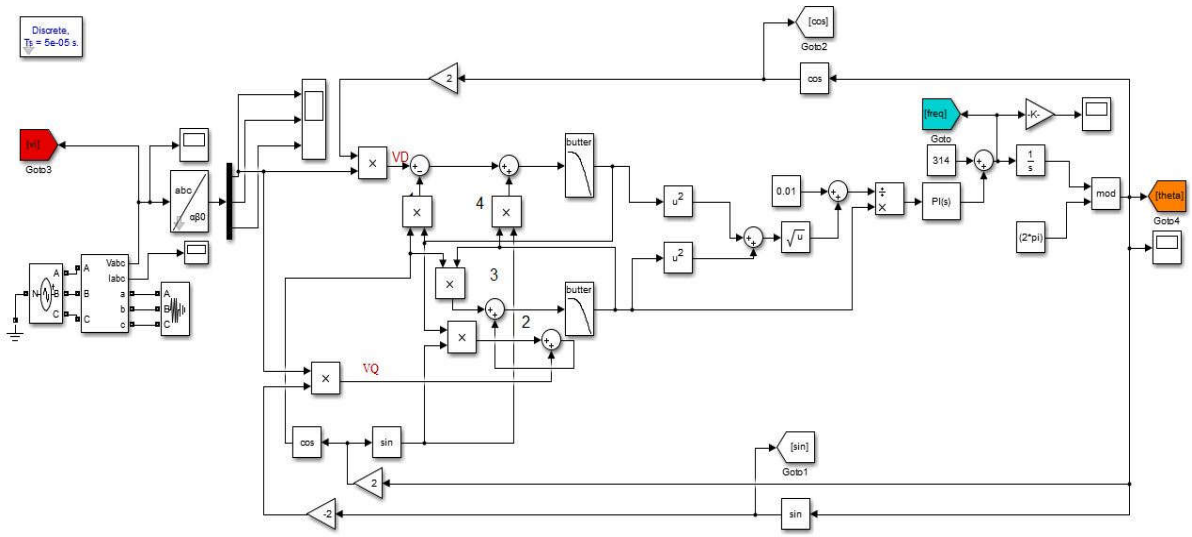

Figure 3.26 Simulation model of three phase DFAC PLL in MATLAB/SIMULINK environment

3.2.5.2 SIMULATION RESULTS

Figure 3.26 shows a simulation model of a three phase DFAC PLL in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and three phase DFAC PLL is implemented. Various changes have been made at an interval to check if the devised model shows synchronism under disturbances.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the PLL takes nearly 9-10 cycles to settle at 55 Hz and after t = 1.7 s the frequency reaches again to 50 Hz. . It can be concluded that the PLL tracks the frequency and remains in synchronism during frequency deviation.

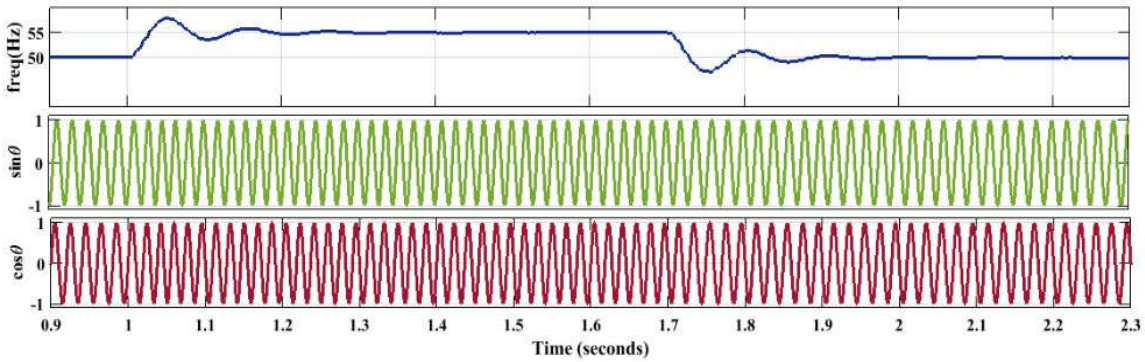

Figure 3.27: Three Phase DFAC PLL (frequency change)

(b) VOLTAGE AMPLITUDE CHANGE

A voltage change has been given by providing a step change of 1 per unit between t = 1 second till t = 1.1 s. It can be noted that the PLL tracks voltage and settles to the original value after t = 1.1 s.

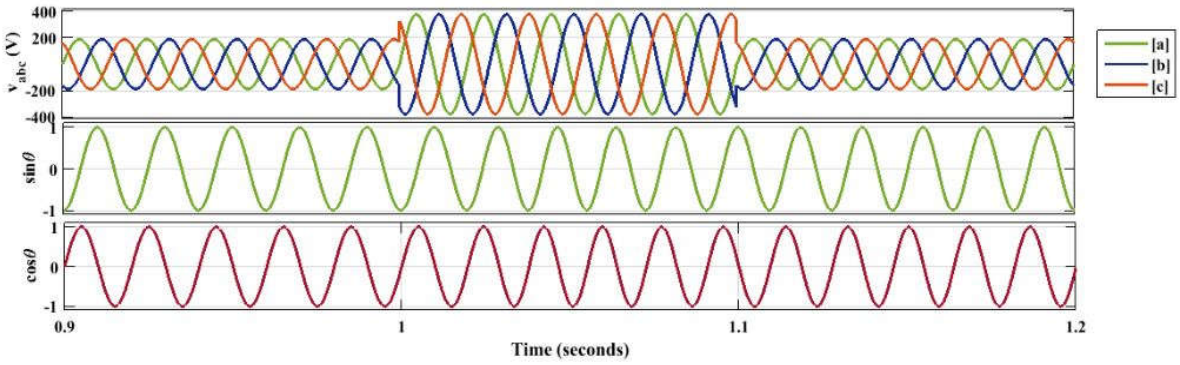

Figure 3.28: Three Phase DFAC PLL (voltage amplitude change)

(c) PHASE ANGLE CHANGE

Phase angle change has been introduced between t = 1 second to t = 1.1 s. Phase angle has been changed from 0 radians to pi radians.

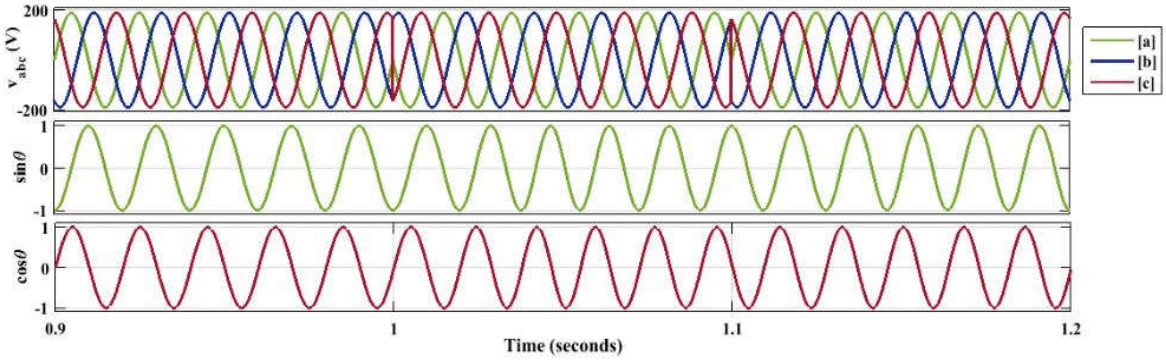

Figure 3.29: Three Phase DFAC PLL (phase angle change)

(d) EFFECT OF HARMONICS

Third harmonics has been introduced from t= 1 second till t=1.1 s. It can be observed that perfect $\sin\theta$ and $\cos\theta$ has been obtained even when the system is polluted with harmonics.

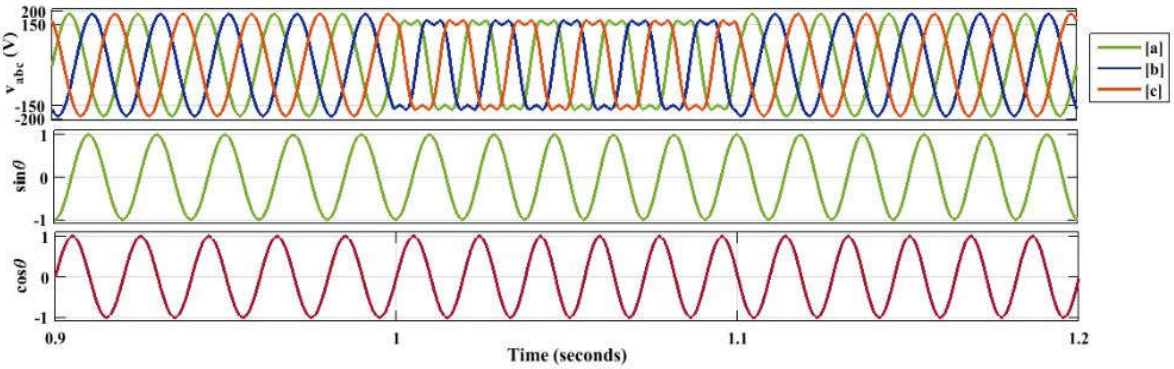

Figure 3.30: Three Phase DFAC PLL (effect of harmonics)

3.3 COMPARISON

For every three phase PLL scheme, the PI controller is tuned for a certain value for accurate results. The proportional integral (PI) controller has two gains namely, proportional gain k_p and integral gain k_i. The optimum values of the gains is presented in Table-3.1.

TABLE 3.1. PI CONTROLLER GAINS FOR A THREE PHASE SYSTEM

S.No	Three Phase PLL	k_p	k_i
1	Three phase SRF PLL	0.02	6.22
2	Three phase EPLL	0.2	5
3	Three phase inverse Park PLL	0.01	10
4	Three phase pPLL	2.1	5.3
5	Three phase DFAC PLL	0.2	9

For the comparison of different three phase PLL schemes mentioned in this chapter, a three phase system feeding a resistive load has been considered. The three phase PLL models were simulated under the same test conditions in the MATLAB/SIMULINK environment.

Four types of disturbances have been evaluated namely:

1 Frequency change

2 Voltage Amplitude change

3 Phase angle change, and

4 Effect of harmonics

The results of these changes have been thoroughly investigated with the three phase PLLs and a comparison has been made based on these observations. The results of these changes have been thoroughly investigated with the three phase PLLs and a comparison has been made based on these observations. The comparisons have been made on the basis of various factors such as frequency/phase tracking, complexity of the circuit, oscillations, etc. The comparative results have been tabulated in table 3.2.

TABLE 3.2. COMPARISON OF THREE PHASE PLL SCHEMES

S.No	**Three phase PLLs**	**Tracking (freq,Voltage,θ)**	**Complexity of the circuit**	**No. of cycles**	**Oscillations**	**Remarks**
1.	Three phase SRF PLL	yes	low	4-5	no	Conventional PLL, unsuitable under harmonics
2.	Three phase EPLL	yes	medium	15-16	yes	High settling time, few oscillations
3.	Three phase inverse	yes	medium	7-8	yes	Medium settling time

	Park PLL					and damped oscillations
4.	Three phase pPLL	yes	medium	5-6	yes	Low settling time and undamped oscillations
5.	Three phase DFAC PLL	yes	high	9-10	no	medium settling time and no oscillations

3.4 CONCLUSIONS

This chapter presents the study of various three phase PLL schemes. The PLLs have been designed and tuned for optimum performance in three phase systems. After this, simulations have been performed to investigate the response under dynamic changes. A comparison has been made on the basis of several factors such as voltage amplitude change, frequency change, phase angle change and effect of harmonics. As can be seen from the figures the three phase SRF PLL takes 4-5 cycles to settle down and practically no oscillations were observed. The three phase EPLL takes approximately 15-16 cycles to settle down but a few oscillations can be observed. The three phase inverse Park PLL takes about 7-8 cycles to settle down and moderate amount of oscillations were observed. The three phase pPLL takes about 5-6 cycles to settle but the amount of oscillations observed in this PLL are the highest. The DFAC PLL takes 9-10 cycles and is almost oscillations free. Hence, an appropriate PLL can be chosen and designed appropriately for tracking fast grid variations and a compromise can be made between various factors such as settling time, complexity of the circuit, oscillations etc.

CHAPTER 4

FREQUENCY LOCKED LOOP TECHNIQUES APPLICABLE TO SINGLE PHASE SYSTEMS AND THREE PHASE SYSTEMS

4.1 INTRODUCTION

A frequency-locked loop (FLL), is an electronic control system that generates a signal that is locked to the frequency of an input or "reference" signal. The main difference between PLL and FLL is explained below:

In the grid connected inverter there is a need to synchronize the output voltage of the inverter with that of the grid to satisfy the coupling condition of the grid. Therefore, the inverter voltage must have the same frequency and phase as that of the grid voltage. The synchronization can be accomplished by the PLL and not by FLL because the PLL minimizes the phase between two periodic wave forms while the FLL minimizes the frequency difference between two periodic wave forms. So, FLL is typically used for frequency tracking unlike PLL which can also be used for phase tracking.

Conventional PLLs/FLLs usually exhibit unacceptable frequency and phase errors when the utility grid is distorted. Therefore, many improved PLLs/FLLs have been proposed [1]-[5],[34],[35]. The PLLs are implemented in the synchronous reference frame. Therefore, their filtering capability can easily and effectively be improved by including additional low-pass filters (LPFs) and/or notch filters into their structure. The FLLs, however, are realized in the stationary reference frame using generalized integrators [36]-[37] or complex bandpass filters (CBFs). Consequently, designing additional filters for incorporating into their structure is more difficult. To enhance the filtering capability of FLLs, some attempts for designing high-order FLLs have been made in recent years. The parallel connection of multiple second-order generalized integrator-based quadrature signal generators (SOGI-QSGs) has also been

suggested. These SOGI-QSGs work in a collaborative way, each of which is responsible for detecting a particular harmonic/disturbance component. This strategy is mainly interesting for applications where the selective extraction/rejection of harmonics is required. Following the same idea, the parallel configuration of multiple CBFs for implementing high-order three-phase FLLs is suggested in [51]-[54]. In this way, all possible harmonics, inter harmonics, and noises in the grid voltage are considerably attenuated. The SOGI-QSG can be seen as a first-order LPF, in which the integrator is replaced by the SOGI. Based on this perspective, a second-order SOGI-QSG is suggested in [34] and [35], which is implemented by replacing two integrators of a second-order LPF by two SOGIs. This second-order SOGI-QSG provides a higher filtering capability than the standard SOGI-QSG. The same idea is used in [51]-[54] for implementing a second-order CBF.

4.2 FREQUENCY LOCKED LOOPS (FLL) TECHNIQUES APPLICABLE TO A SINGLE PHASE SYSTEM

PLLs synchronize with the phase of the input signal, and hence, the accuracy and dynamical response of its estimation under transient conditions are highly influenced by phase angle jumps. On the other hand, a frequency-locked loop (FLL) estimates the frequency of the input signal, which does not experience such sudden changes. As a consequence, the performance of the FLL when the phase angle of the input changes is more advantageous if compared with PLL-based algorithms.

4.2.1 SINGLE PHASE SOGI BASED FLL

The concept of the generalized integrator (GI) for sinusoidal signals was formally presented in [36]-[37]. This integrator stems from the principle that the time-domain convolution product of a sinusoidal function by itself gives rise to the original function multiplied by the time variable.

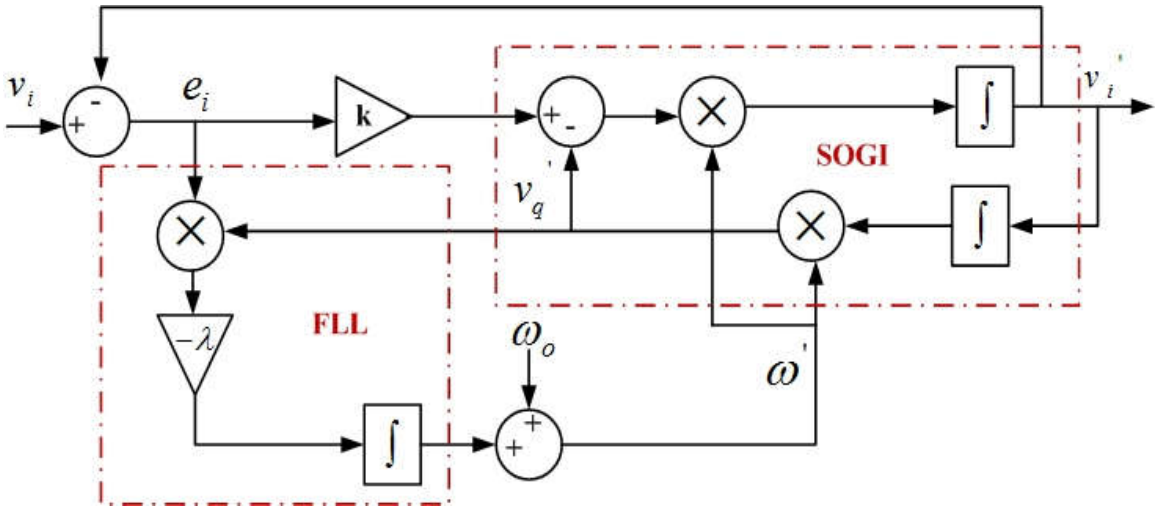

Figure 4.1: Schematic diagram of single phase SOGI based FLL

4.2.1.1 ANALYSIS

A processing block whose transfer function matches with the Laplace transform of a sinusoidal function, i.e., a resonator, will act as an "amplitude integrator" for a sinusoidal signal applied to its input. Moreover, the in-quadrature combination of the sine and cosine transfer functions gives rise to an "ideal integrator" independent of the phase angle of the sinusoidal input signal. In [36], a simplified block was presented as a GI for single sinusoidal signals. The GI is the base of proportional-resonant controllers, and it has also been applied to adaptive filtering applications and PLL implementation. An adaptive filter structure, based on the GI structure, named SOGI was presented in [34],[35] and [38].

The two in-quadrature output signals of the adaptive filter, are defined by the following transfer functions:

$$D(s) = \frac{v_i'(s)}{v_i(s)} = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \tag{4.1}$$

$$Q(s) = \frac{v_q'(s)}{v_i(s)} = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \tag{4.2}$$

The transfer function from the input signal $v_i(s)$ to the error signal $e_i(s)$ i.e., $E(s)$, is given by:

$$E(s) = \frac{e_i(s)}{v_i(s)} = \frac{s^2+\omega'^2}{s^2+k\omega' s+\omega'^2} \tag{4.3}$$

It can be concluded from equation (4.1), the bandwidth of the bandpass filter is exclusively set by the gain k and is independent of the center frequency ω' The same thing happens with the low-pass filter of (4.2), in which the static gain only depends on parameter k. From the bode plots [35], it can be concluded that the v_q' output as shown in figure 4.1 is always 90° lagging from the v_i' output. For this reason, the adaptive filter was named as SOGI quadrature signal generator (SOGI-QSG). This system, together with the FLL presented in this section constitutes the main building blocks of the synchronization algorithm presented. The SOGI equations can be referred from equations (2.14)-(2.16). The values of parameters k and λ can be set accordingly for optimization.

Both Q(s) and E(s) are plotted together in the Bode diagram of [35]. It has been observed from the diagram that the signals v_q' and e_i are in phase when the input frequency is lower than the SOGI resonance frequency ($\omega < \omega'$), and they are in counter phase when $\omega > \omega'$ Therefore, a frequency error variablee_i can be defined as the product of the signals v_q' and e_i. The average value of $e_i$will be positive when $\omega < \omega'$, zero when $\omega = \omega'$,and negative when $\omega > \omega'$. Hence, as shown in Figure. 4.1, an integral controller with a negative gain $-\lambda$ can be used to make zero the dc component of the frequency error by shifting the SOGI resonance frequency ω' until matching the input frequency ω.

The state space analysis of SOGI-FLL [35] concluded that the SOGI FLL behaves as a nonlinear system, whose dynamical response, as well as its own stability, depends on four parameters, namely: the amplitude and frequency of the input signal and the values of parameters k and λ , which are the control parameters of the SOGI and the FLL, respectively. Therefore, SOGI based FLL with gain normalization was implemented.

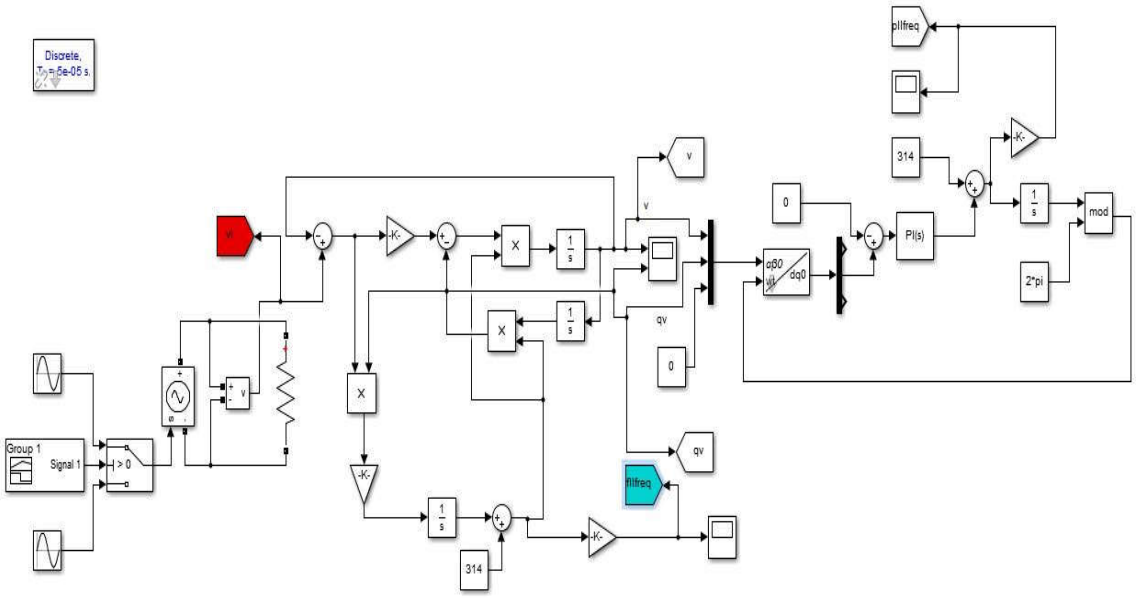

Figure 4.2: Simulation model of a single phase SOGI based FLL in MATLAB/SIMULINK environment

4.2.1.2 SIMULATION RESULTS

Figure 4.2 shows a simulation model of a single phase SOGI based FLL in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and a single phase SOGI based FLL is implemented. Changes have been made at an interval to check if the devised model shows synchronism under varying frequency.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the FLL takes nearly 9-10 cycles to settle at 55 Hz and after t = 1.3 s the frequency reaches again to 50 Hz. Practically, no oscillations were observed.

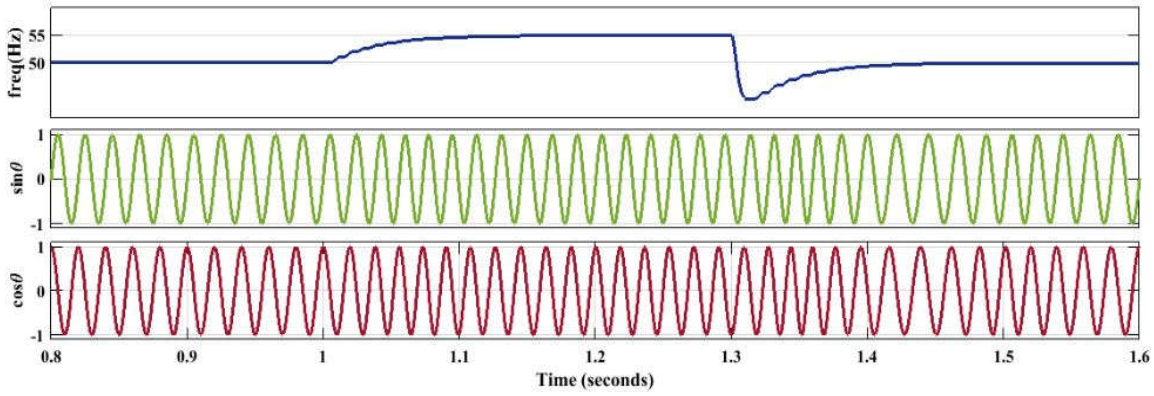

Figure 4.3: Single phase SOGI based FLL (frequency change)

4.2.2 SINGLE PHASE SOGI BASED FLL WITH GAIN NORMALIZATION

The FLL presented in this section is SOGI based FLL with gain normalization. The FLL gain normalization block computes the SOGI control parameter k together with the output variables $\omega'$and $v'^2 + v_q'^2$ to linearize the response of the FLL. On the other hand, the time constant λ is the parameter that permits to set the dynamics of the frequency estimation [34],[39].

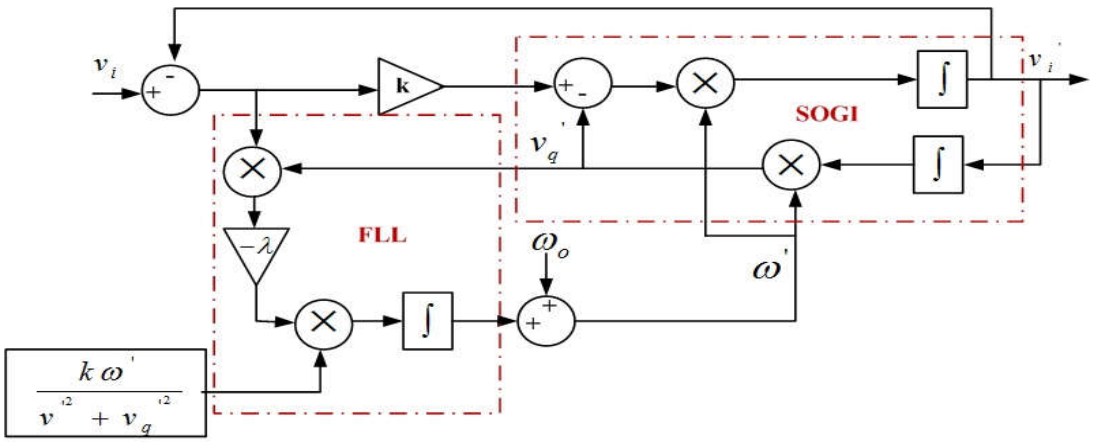

Figure 4.4: Schematic diagram of single phase SOGI based FLL with gain normalization

4.2.2.1 ANALYSIS

The SOGI based equations can be referred from the equations (2.14)-(2.16). The gain normalization block is given below:

$$\frac{k\omega'}{v'^2 + {v_q}'^2}$$

The value of k determines the frequency bandwidth of the SOGI-QSG. A very high value of *k* would make the SOGIQSG performance fast, reducing its immunity to the effects of harmonics in the input signal. On the contrary, a very low value for *k* makes the SOGI-QSG very selective in frequency but gives rise to a long stabilization time. Considering these constrains, the gain of the SOGI-QSG is set to k=$\sqrt{2}$, which results in an optimal tradeoff between settle time, overshooting, and harmonic rejection.

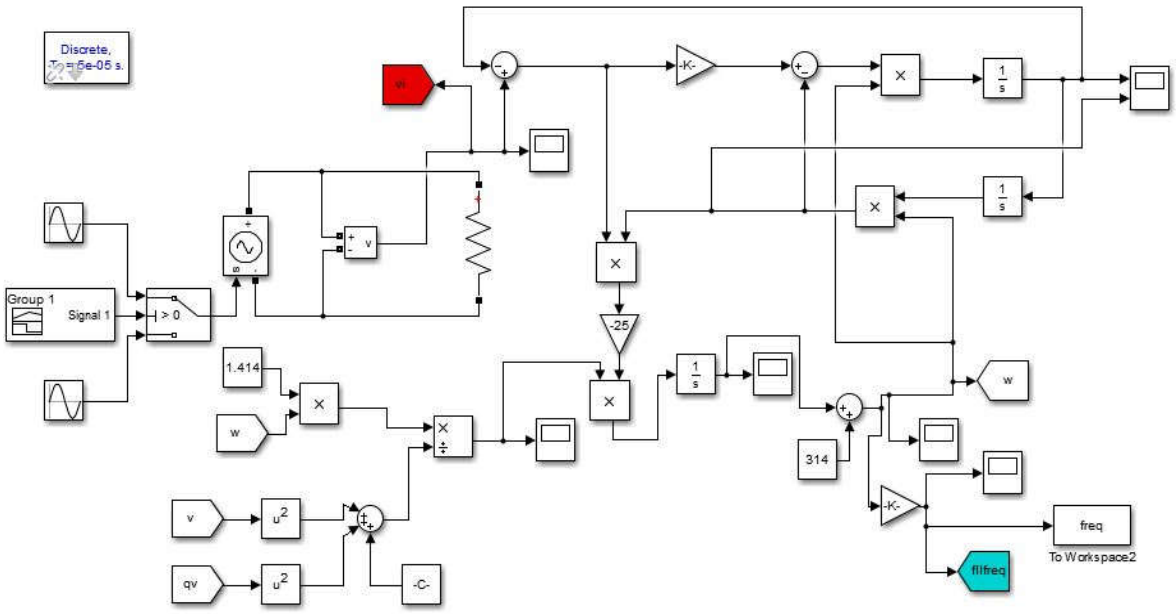

Figure 4.5: Simulation model of a single phase SOGI based FLL with gain normalization in MATLAB/SIMULINK environment

4.2.2.2 SIMULATION RESULTS

Figure 4.5 shows a simulation model of a single phase SOGI based FLL with gain normalization in MATLAB/SIMULINK environment. In the SIMULINK model, single phase system is devised and a single phase SOGI based FLL with gain normalization is implemented. Changes have been made at an interval to check if the devised model shows synchronism under varying frequency.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the FLL takes nearly 3-4 cycles to settle at 55 Hz and after t = 1.3 s the frequency reaches again to 50 Hz.

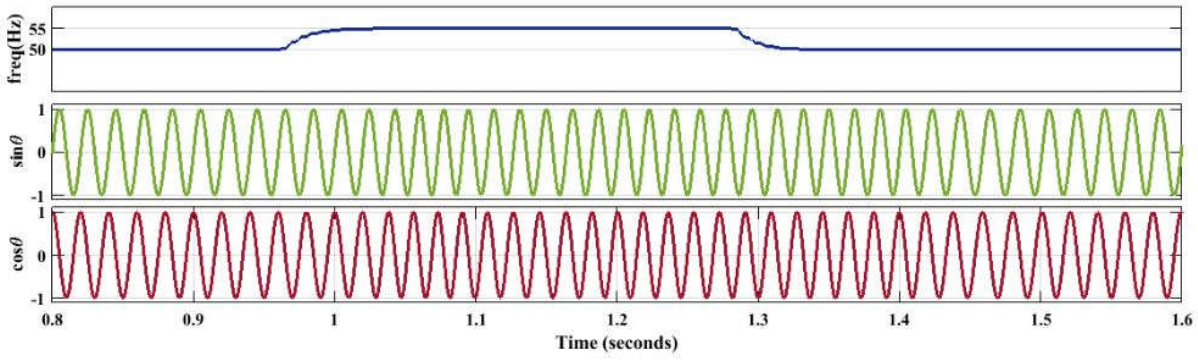

Figure 4.6: Single phase SOGI based FLL with gain normalization (frequency change)

4.3 FREQUENCY LOCKED LOOPS (FLL) TECHNIQUES APPLICABLE TO A THREE PHASE SYSTEM

Three phase FLLs are gaining popularity but are still relatively new as compared to three phase PLLs. Three phase FLLs can be implemented by using reduced order generalized integrator (ROGI) which is analogous to a three phase SRF PLL. Additionally, complex band filter (CBF) FLLs have also been implemented.

4.3.1 THREE PHASE STANDARD FLL

Fig.4.7 illustrates a standard three-phase FLL. The parameters k and λ are the control parameters of this FLL, and $\widehat{\theta_1}, \widehat{\omega'}$, *and* $\widehat{V_1}$, denote the estimated phase, frequency, and amplitude, respectively. The standard FLL is implemented by using a reduced-order generalized integrator (ROGI) [45] in the forward path of a unity feedback control loop for extracting the grid voltage fundamental component and a frequency estimator for adjusting its center frequency. The historical development of this structure has been explained in [46],[47].

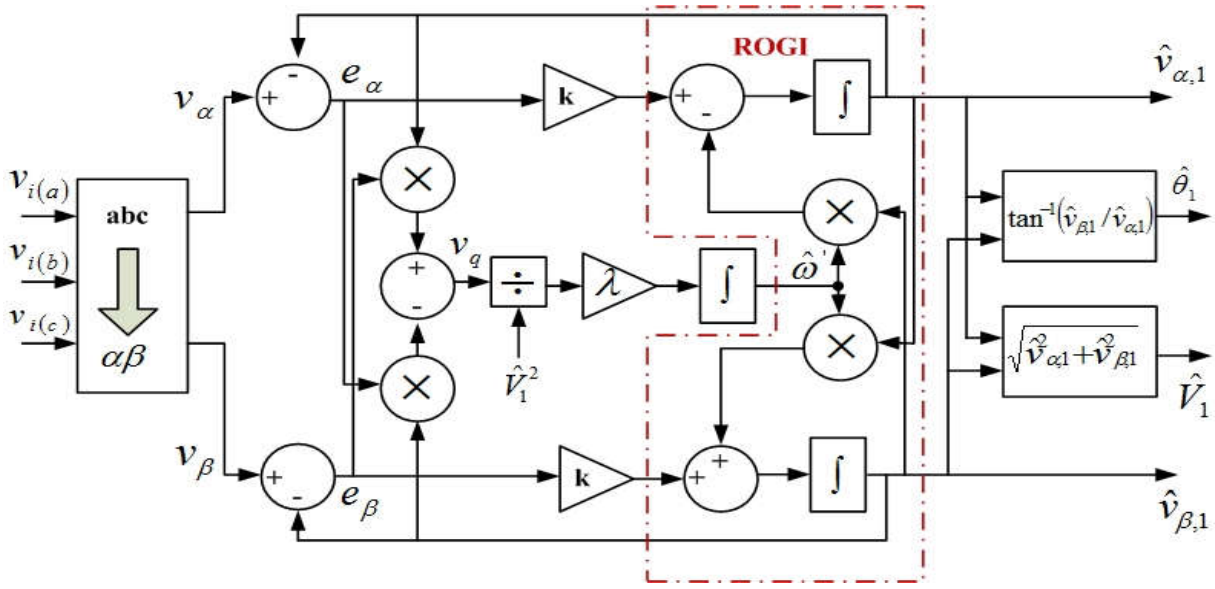

Figure 4.7: Schematic diagram of three phase standard FLL

4.3.1.1 ANALYSIS

The standard FLL and the SRF-PLL are equivalent systems. The assumptions behind this equivalence are $k_p = k_v$ = k and k_i = λ where k_p and $k_i$are the proportional and integral gains of the SRFPLL, respectively, and k_v is the low-pass filter (LPF) cutoff frequency in the SRF-PLL amplitude estimation loop. This equivalence implies that the standard FLL, like a simple SRFPLL, has a very limited filtering capability. To tackle this problem, some

attempts have been made recently. A modification of a standard three phase SRF FLL has been described in the next section.

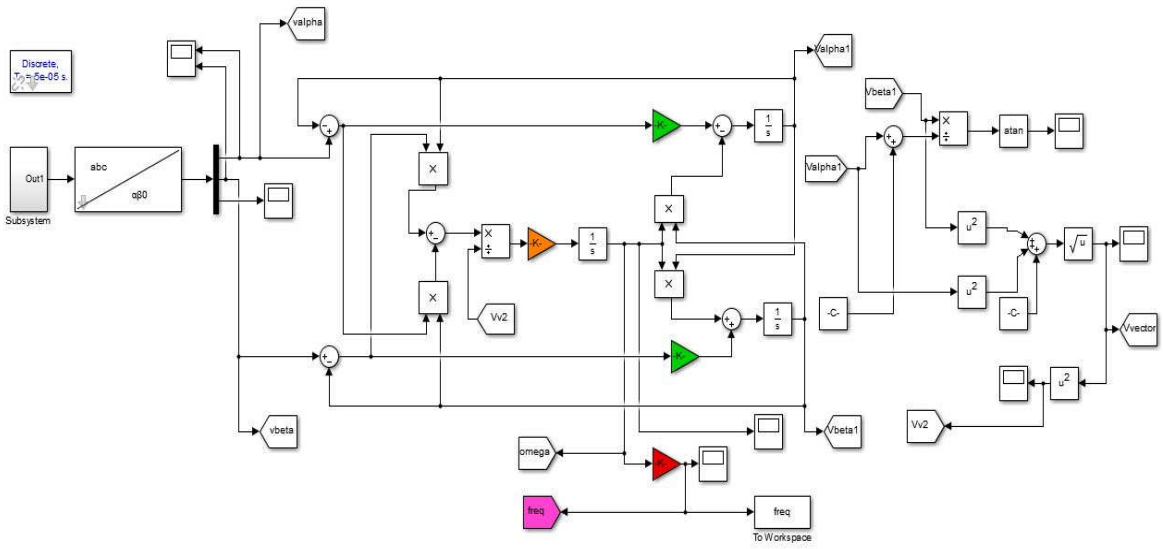

Figure 4.8: Simulation model of a three phase standard FLL in MATLAB/SIMULINK environment

4.3.1.2 SIMULATION RESULTS

Figure 4.8 shows a simulation model of three phase standard FLL in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and a three phase standard FLL is implemented. Changes have been made at an interval to check if the devised model shows synchronism under varying frequency.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the FLL takes nearly 8-9 cycles to settle at 55 Hz and after t = 1.3 s the frequency reaches again to 50 Hz. Practically, no oscillations were observed in the FLL.

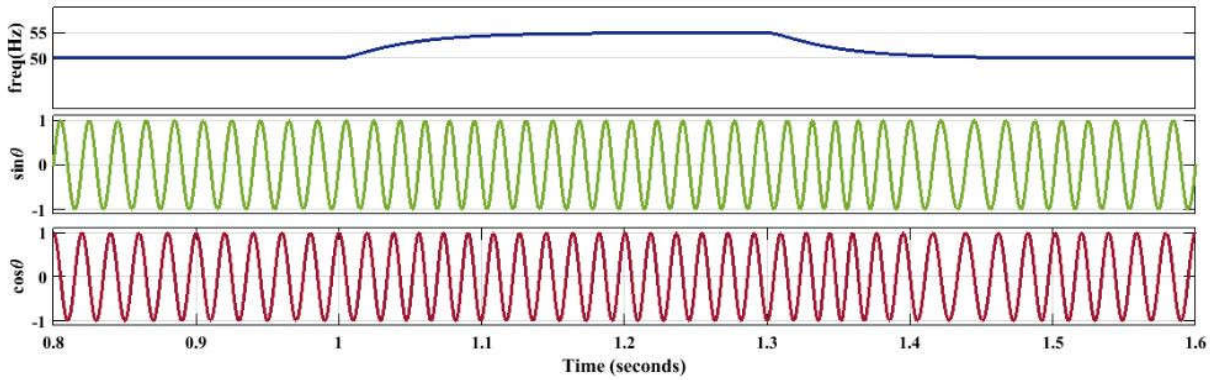

Figure 4.9: Three phase standard FLL (frequency change)

4.3.2 THREE PHASE FLL WITH ENHANCED DC OFFSET REJECTION

Fig.4.10 illustrates a standard three-phase FLL with DC offset rejection. The parameters k and λ are the control parameters of this FLL, and $\widehat{\theta_1}, \widehat{\omega'}$, *and* $\widehat{V_1}$, denote the estimated phase, frequency, and amplitude, respectively. The standard FLL is implemented by using a reduced-order generalized integrator (ROGI) [45] in the forward path of a unity feedback control loop for extracting the grid voltage fundamental component and a frequency estimator for adjusting its center frequency. To enhance the FLL DC-offset rejection capability, two integrators may be included in the standard FLL structure [48]–[50].

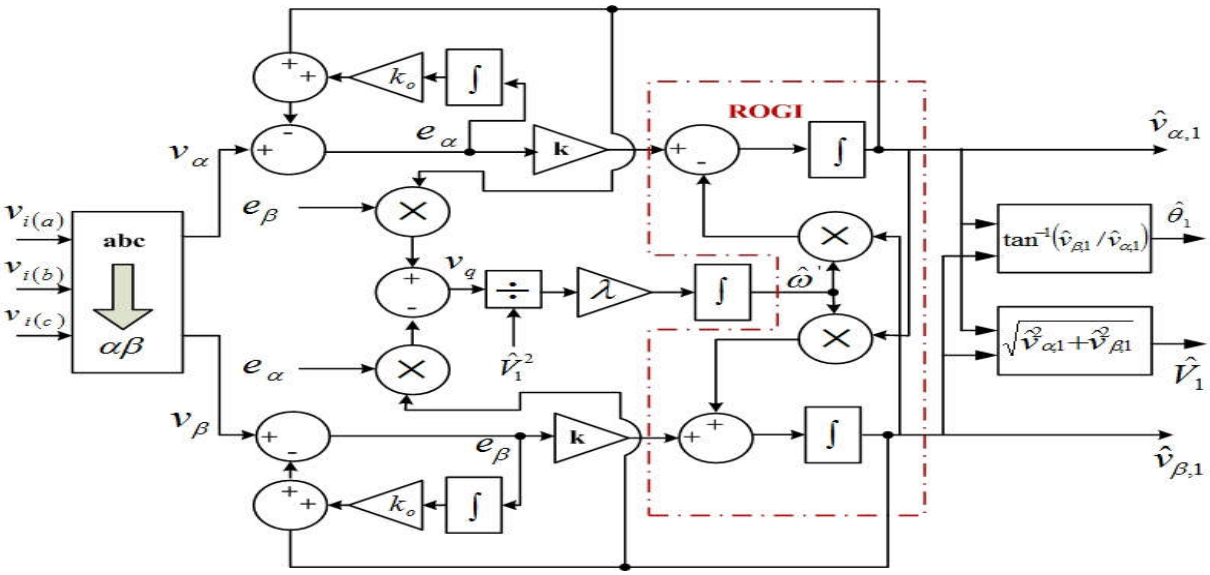

Figure 4.10: Schematic diagram of three phase FLL with DC offset rejection

4.3.2.1 ANALYSIS

The integrators provide an estimation of the grid voltage DC component and, therefore, completely reject its disturbing effect on the FLL performance. They, however, may slightly degrade the FLL harmonic filtering capability and high-frequency noise immunity. Using these integrators mathematically equivalent to including two high-pass filters inside the FLL control loop. The integrators employed for the DC offset rejection can be shown as k_o/s.

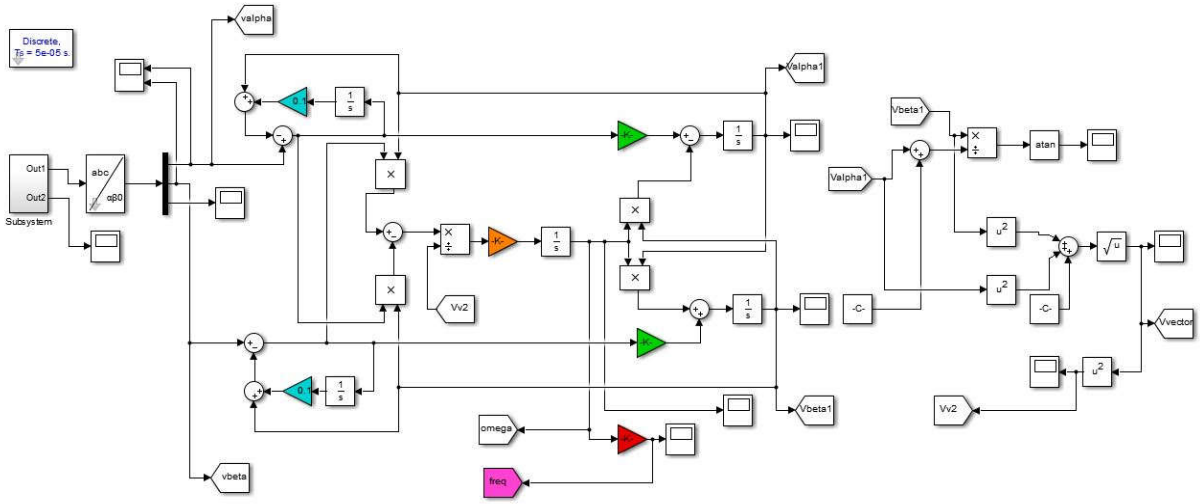

Figure 4.11: Simulation model of a three phase standard FLL with DC offset rejection in MATLAB/SIMULINK environment

4.3.2.2 SIMULATION RESULTS

Figure 4.11 shows a simulation model of three phase standard FLL with DC offset rejection in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and a three phase standard FLL with DC offset rejection is implemented. Changes have been made at an interval to check if the devised model shows synchronism under varying frequency.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the FLL takes nearly 5-6 cycles to settle at 55 Hz and after t = 1.3 s the frequency reaches again to 50 Hz. Practically, no oscillations were observed in the FLL.

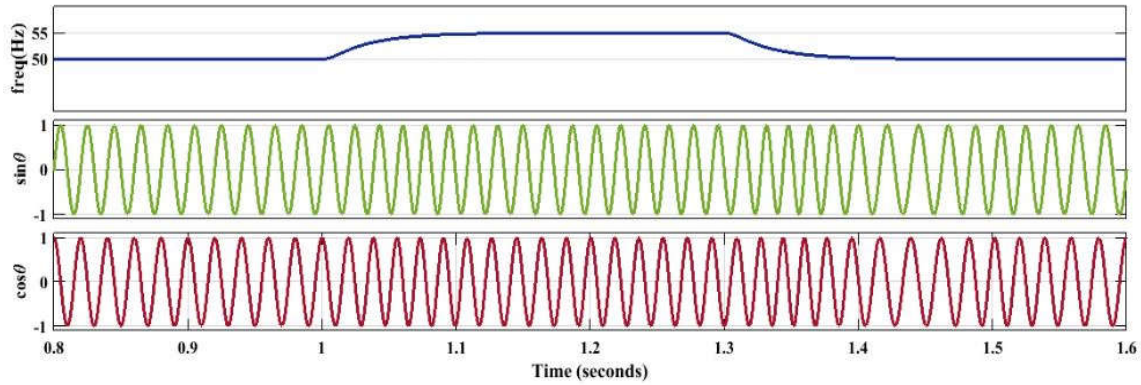

Figure 4.12: Three phase standard FLL with DC offset rejection (frequency change)

4.3.3 THREE PHASE COMPLEX BAND FILTER (CBF) FLL 1

To enhance the filtering capability of FLLs, some attempts for designing high-order FLLs have been made in recent years. In [36]-[37], the parallel connection of multiple second-order generalized integrator-based quadrature signal generators (SOGI QSGs) is suggested. These SOGI-QSGs work in a collaborative way, each of which is responsible for detecting a particular harmonic/ disturbance component. This strategy is mainly interesting for applications where the selective extraction/rejection of harmonics is required. Following the same idea as in, the parallel configuration of multiple CBFs for implementing high-order three-phase FLLs is suggested in [51]-[54]. In this way, all possible harmonics, inter harmonics, and noises in the grid voltage are considerably attenuated.

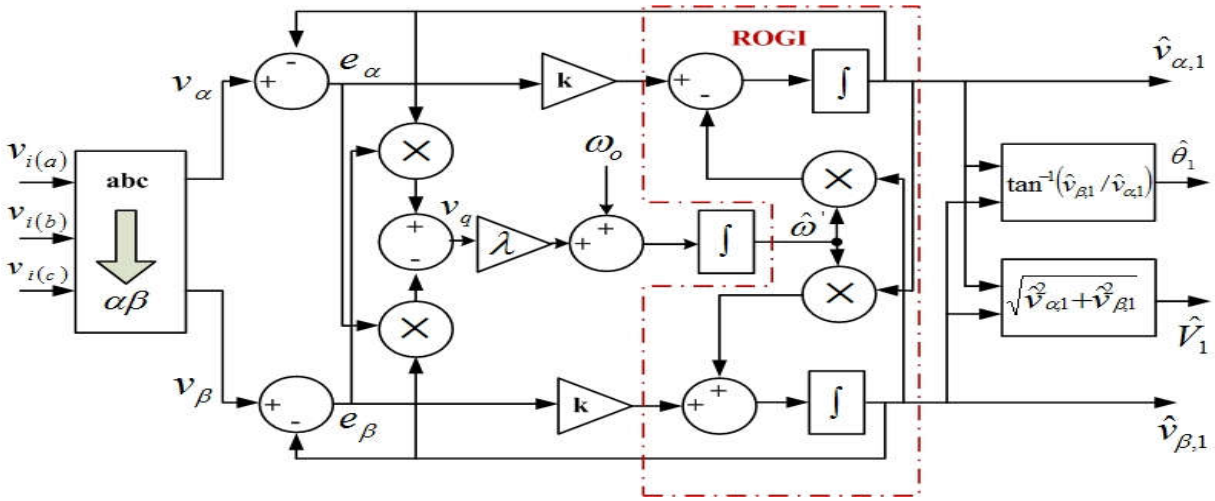

Figure 4.13: Schematic diagram of three phase CBF FLL 1

4.3.3.1 ANALYSIS

The SOGI-QSG can be seen as a first-order LPF, in which the integrator is replaced by the SOGI. Based on this perspective, a second-order SOGI-QSG is suggested in [34] and [35], which is implemented by replacing two integrators of a second-order LPF by two SOGIs. This second-order SOGIQSG provides a higher filtering capability than the standard SOGI-QSG. The same idea is used in [54] for implementing a second-order CBF. The schematic diagram of the CBF-FLL1 can be observed in Fig.4.13. Based on this structure, the characteristic transfer functions of the CBF-FLL1 can be derived as:

$$\hat{\theta}(s) \approx \frac{ks+\lambda V^2}{s^2+ks+\lambda V^2}\theta(s) \tag{4.5}$$

$$\hat{\omega}(s) \approx \frac{\lambda V^2}{s^2+ks+\lambda V^2}\omega(s) \tag{4.6}$$

$$\hat{V}(s) \approx \frac{k}{s+k}V(s) \tag{4.7}$$

The control parameters of the CBF-FLL1 [51]-[52] can be selected using the standard design approach for second-order systems, i.e., defining k =$2\zeta\omega_n$ and $\lambda = (\omega_n/V)2$ and selecting proper values for the natural frequency $\omega_n$and the damping factor ζ.

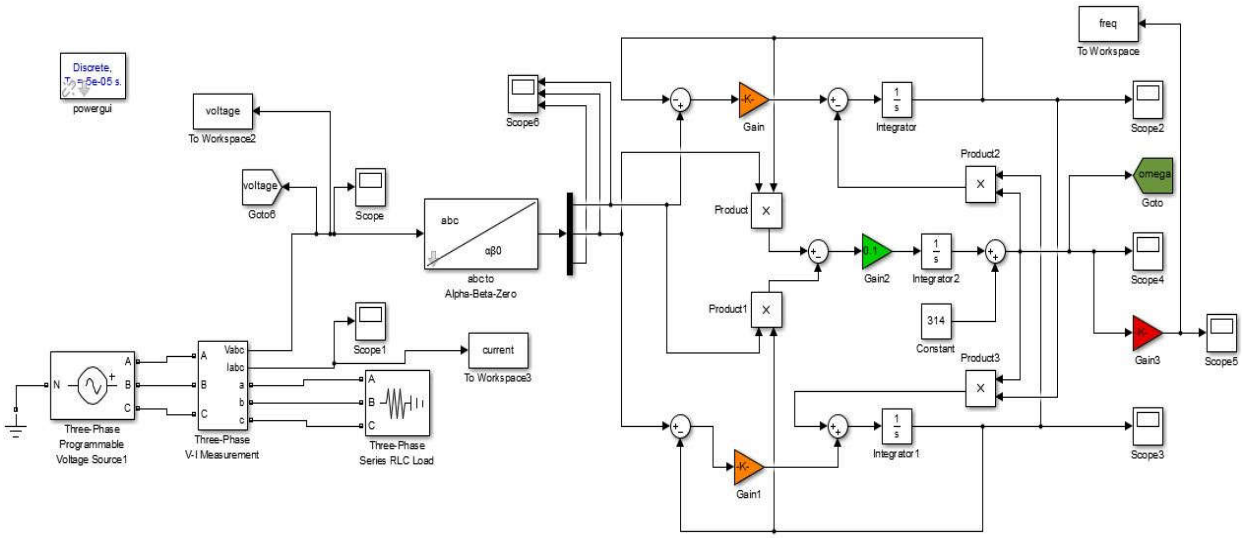

Figure 4.14: Simulation model CBF FLL 1 in MATLAB/SIMULINK environment

4.3.3.2 SIMULATION RESULTS

Figure 4.14 shows a simulation model of CBF FLL 1in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and CBF FLL 1 is implemented. Changes have been made at an interval to check if the devised model shows synchronism under varying frequency.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the FLL takes nearly 4-5 cycles to settle at 55 Hz and after t = 1.3 s the frequency reaches again to 50 Hz. Practically, no oscillations were observed in the FLL.

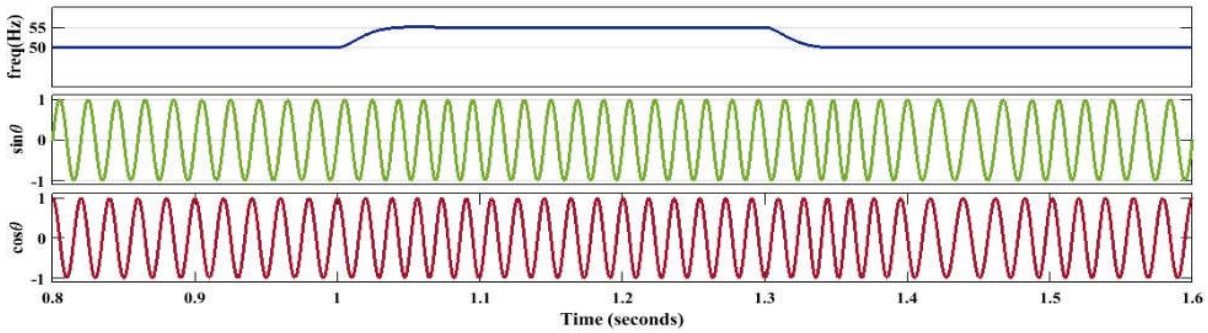

Figure 4.15: Three phase CBF FLL 1

4.3.4 THREE PHASE COMPLEX BAND FILTER (CBF) FLL2

The input signals of the CBF-FLL2 [53]-[54] are considered, where V and $\theta = \int \omega' dt\theta$ are the grid voltage amplitude and angle, respectively, and ω' is the grid frequency. In addition, in obtaining the transfer functions describing the phase and frequency estimation dynamics, it is assumed that the grid voltage amplitude V is constant.

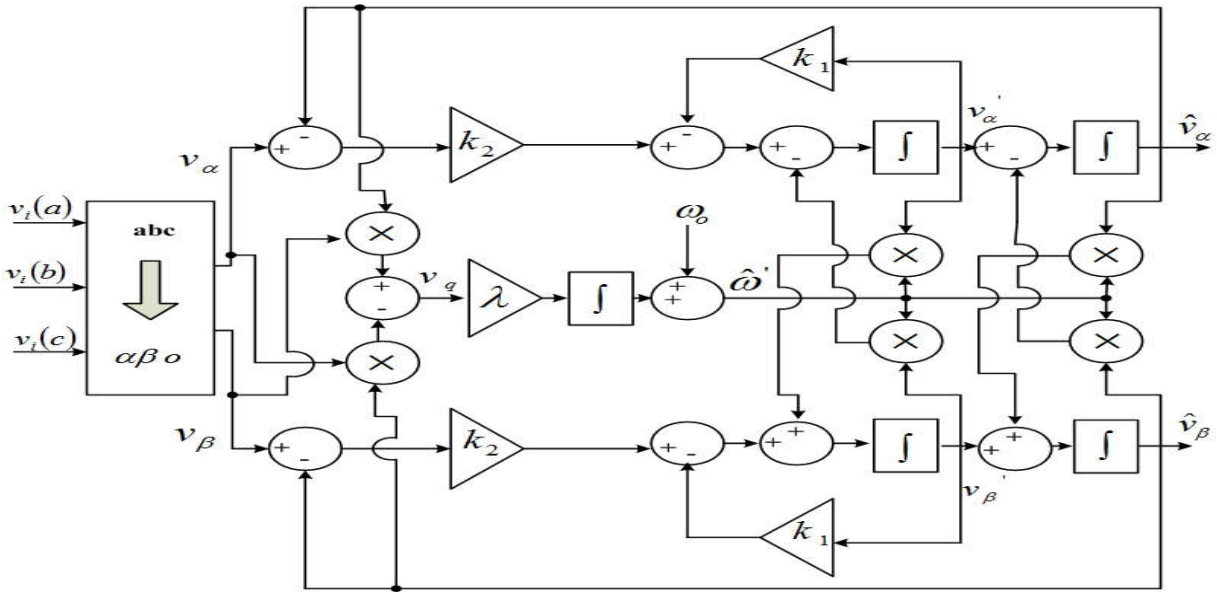

Figure 4.16: Schematic diagram of three phase CBF FLL 2

4.3.4.1 ANALYSIS

The input signals of the CBF-FLL2 are considered as:

$$v_\alpha(t) = V \cos\theta \tag{4.8}$$

$$v_\beta(t) = V \sin\theta \tag{4.9}$$

$$\widehat{\omega'}(s) \approx \frac{\lambda V^2(s+k_1)}{s^3+k_1 s^2+(k_2+\lambda V^2)s+k_1\lambda V^2}\omega'(s) \tag{4.10}$$

$$\hat{\theta}(s) \approx \frac{(\lambda V^2+k_2)s+k_1\lambda V^2}{\lambda V^2 s(s+k_1)}\hat{\omega}(s) \tag{4.11}$$

Substituting $\hat{\omega}(s) = s\theta(s)$

$$\hat{\theta}(s) = \frac{(\lambda V^2+k_2)s+k_1\lambda V^2}{s^3+k_1s^2+(k_2+\lambda V^2)s+k_1\lambda V^2}\theta(s) \tag{4.12}$$

The amplitude estimated by the CBF-FLL2 can be expressed as:

$$\hat{V} = \sqrt{\widehat{v_\alpha^2}(t) + \widehat{v_\beta^2}(t)} \tag{4.13}$$

Using successive differentiation, amplitude estimation dynamics can be approximated by:

$$\hat{V}(s) \approx \frac{k_2}{s^2+k_1s+k_2}V(s) \tag{4.14}$$

The control parameters of the CBF-FLL2 [53]-[54] can be selected using the standard design approach. The performance of the CBF FLL 2 depends on the optimum tuning of the control parameters k_1, k_2 and λ.

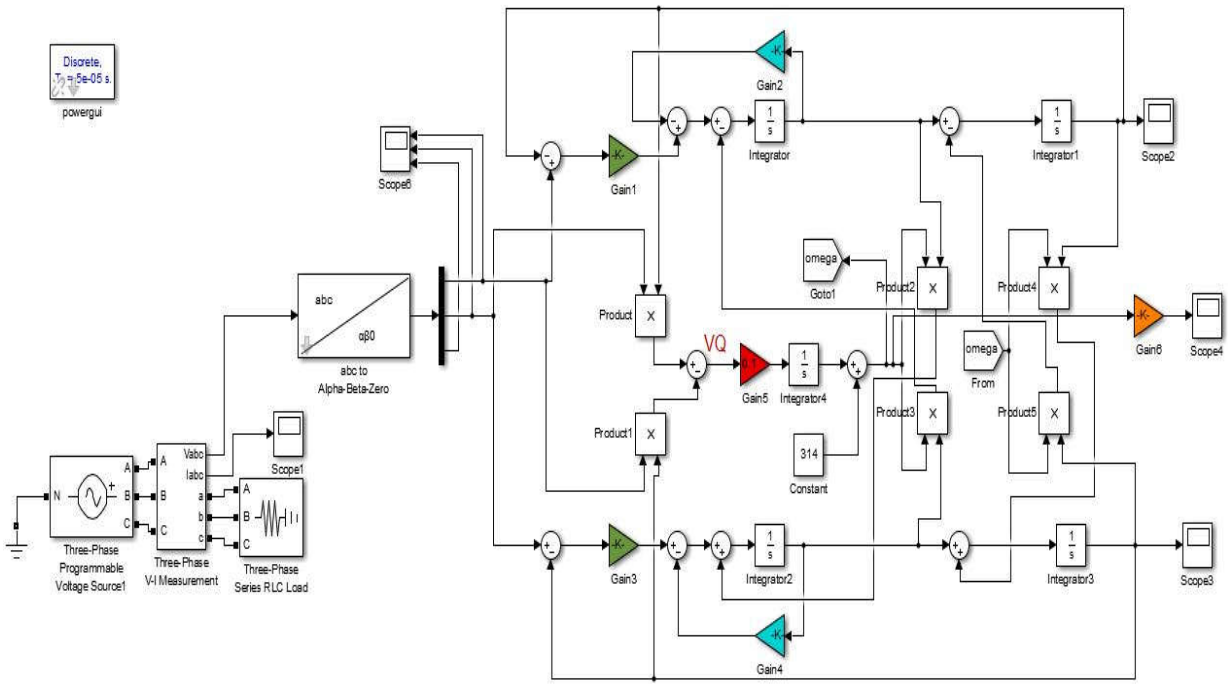

Figure 4.17: Simulation model CBF FLL 2 in MATLAB/SIMULINK environment

4.3.4.2 SIMULATION RESULTS

Figure 4.17 shows a simulation model of CBF FLL 2 in MATLAB/SIMULINK environment. In the SIMULINK model, three phase system is devised and CBF FLL 2 is implemented. Changes have been made at an interval to check if the devised model shows synchronism under varying frequency.

(a) FREQUENCY CHANGE

The frequency is changed from 50 Hz to 55 Hz. It can be noted that the FLL takes nearly 2-3 cycles to settle at 55 Hz and after t = 1.3 s the frequency reaches again to 50 Hz. Practically, no oscillations were observed in the FLL.

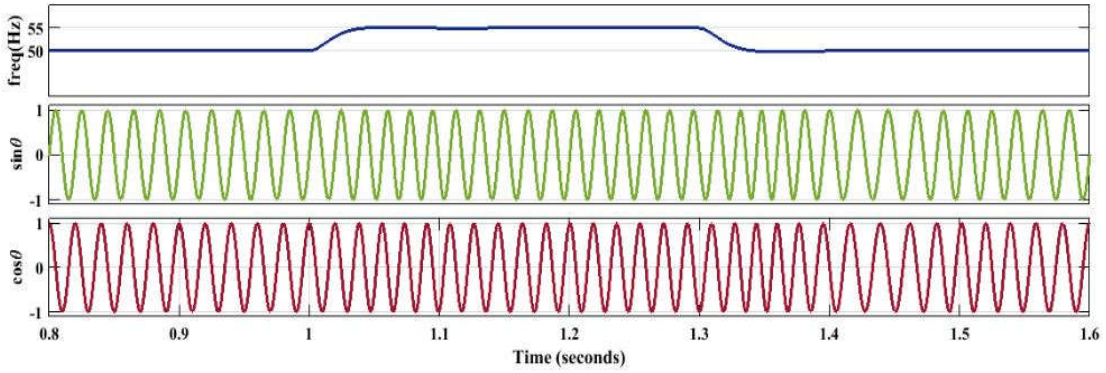

Figure 4.18: Three phase CBF FLL 2 (frequency change)

4.4 COMAPRISON

For every single phase and three phase FLL scheme, there are controlling parameters that needs to be set. The right selection of the values of the controlling parameters ensures optimum operation of the FLLs. For the comparison of different single phase FLL techniques mentioned in this chapter, a single phase system feeding a resistive load has been considered. For the comparison of different three phase FLL techniques mentioned in this chapter, a three phase system feeding a resistive load has been considered. The single phase and three phase

FLL models were simulated under the same test conditions in the MATLAB/SIMULINK environment.

The results of the changes have been thoroughly investigated with the single phase FLLs and a comparison has been made based on these observations. The comparisons have been made on the basis of various factors such as frequency/phase tracking, complexity of the circuit, oscillations, etc. The comparative results have been tabulated in table 4.1.

TABLE 4.1. COMPARISON OF SINGLE PHASE FLL SCHEMES

S.No	**Single phase FLLs**	**Tracking (freq)**	**Complexity of the circuit**	**No. of cycles**	**Oscillations**	**Remarks**
1.	Single phase SOGI based FLL	yes	low	9-10	no	Conventional single phase FLL, low computational burden
2.	Single phase SOGI based FLL with gain normalization	yes	low	3-4	no	Less settling time, oscillations free

The results of the changes have been thoroughly investigated with the three phase FLLs and a comparison has been made based on these observations. The comparisons have been made on the basis of various factors such as frequency/phase tracking, complexity of the circuit, oscillations, etc. The comparative results have been tabulated in table 4.2.

TABLE 4.2. COMPARISON OF THREE PHASE FLL SCHEMES

S.No	Three phase FLLs	Tracking (freq)	Complexity of the circuit	No. of cycles	Oscillations	Remarks
1.	Three phase standard FLL	yes	medium	8-9	no	Conventional three phase FLL, limited filtering capability
2.	Three Phase FLL With Enhanced DC Offset Rejection	yes	medium	5-6	no	Enhances DC offset rejection capability
3.	Three phase CBF FLL 1	yes	high	4-5	no	Enhances filtering capability of FLL
4.	Three phase CBF FLL 2	yes	high	2-3	no	Low settling time, freq free of oscillations

An appropriate FLL can be chosen and designed appropriately for tracking fast grid variations and a compromise can be made between various factors such as settling time, complexity of the circuit etc.

4.5 CONCLUSIONS

This chapter presents the study of various single phase and three phase FLL schemes. The FLLs have been designed and tuned for optimum performance in single phase systems as well as three phase systems. After this, simulations have been performed to investigate the response under dynamic changes. A comparison has been made on the basis of several factors such as frequency change, oscillations, complexity of the circuit, etc. It can be observed from the comparative tables that single phase SOGI based FLL takes approximately 9-10 cycles to settle, whereas the single phase SOGI based FLL with gain normalization takes only 3-4 cycles to get settled. Both the single phase FLLs possess low computational burden and no oscillations. Additionally, three phase FLLs have been compared. It can be observed that the standard three phase FLL takes approximately 8-9 cycles to settle down, its computational burden is medium and it is oscillations free. The three phase FLL with enhanced DC offset rejection shows comparatively less settling time and no oscillations. Moreover, complex bandpass filter (CBF) FLLs have high computational burden and no oscillations. The settling time of CBF FLL 1 was observed to be higher i.e. 4-5 cycles as compared to CBF FLL 2which was observed to be 2-3 cycles. Based on the comparison tabulated in this chapter, it can be concluded that single phase SOGI based FLL with gain normalization is a better option for synchronization in a single phase system whereas in a three phase system, CBF FLL 2 delivers the least settling time therefore, it can be chosen for synchronization in a three phase system.

CHAPTER 5

EXPERIMENTAL RESULTS

5.1 INTRODUCTION

The experiments were performed on a few single phase phase locked loop (PLL) techniques which includes transport delay PLL, EPLL and SOGI PLL. The experiments were performed with the help of the APS-1102 programmable AC/DC power source. The specifications of the the APS-1102 programmable AC/DC power source are given. The APS-1102 programmable AC/DC power source is a power source that can output AC and DC power, features a compact design for convenient desktop use, and provides a wealth of measurement functions. Rated output voltage is 100 Vrms (100 V range) or 200 Vrms (200 V range), with maximum output capacity of 1 kVA (during AC 200 V input). It also features eight output modes, with DC output, external input amplification, and line-synchronized output.

The APS-1102 can be controlled remotely from an external computer via a USB interface. The accompanying software supports use of the following functions.

1. Panel operations
2. Sequence editing and execution
3. Arbitrary waveform editing and transfer
4. Data logger (by capturing measured values)

The Various measurement functions of the APS-1102 programmable AC/DC power source are:

1. Voltage (RMS value, average DC value, peak value)
2. Current (RMS value, average DC value, peak value, peak hold)
3. Power (effective, reactive, apparent)
4. Frequency (only in the external synchronization mode)
5. Load power factor
6. Load crest factor
7. Harmonic current (up to 40th harmonic, 50/60 Hz fundamental only)

5.2 EXPERIMENTAL RESULTS

The single phase PLLs were tested under various disturbances such as harmonics and noise. The effect of disturbances on frequency change and angle θ was noted. Simulated models were developed for single phase PLLs using dspace (DS1104). PLL blocks were processed using DSP 7MS320F2407. The signals i.e. voltage, frequency, θ and $\sin\theta/\cos\theta$ were captured on Digital scope oscilloscope (DSO) for analysis.

5.2.1 TRANSPORT DELAY PLL

The transport delay PLL was developed for experimental results. The disturbances under which the PLL has been studied are frequency change, introduction of 3rd harmonics and introduction of noise signal.

The following signals can be observed on the DSO:

1. Voltage signal
2. Frequency
3. Angle θ
4. Cos θ

(a) Frequency Change

Frequency was changed from 50 Hz to 55 Hz. It can be observed that the tracking of frequency is observed in nearly 6-7 cycles. The frequency signal is almost oscillations free. The voltage signal is synchronized with Cos θ.

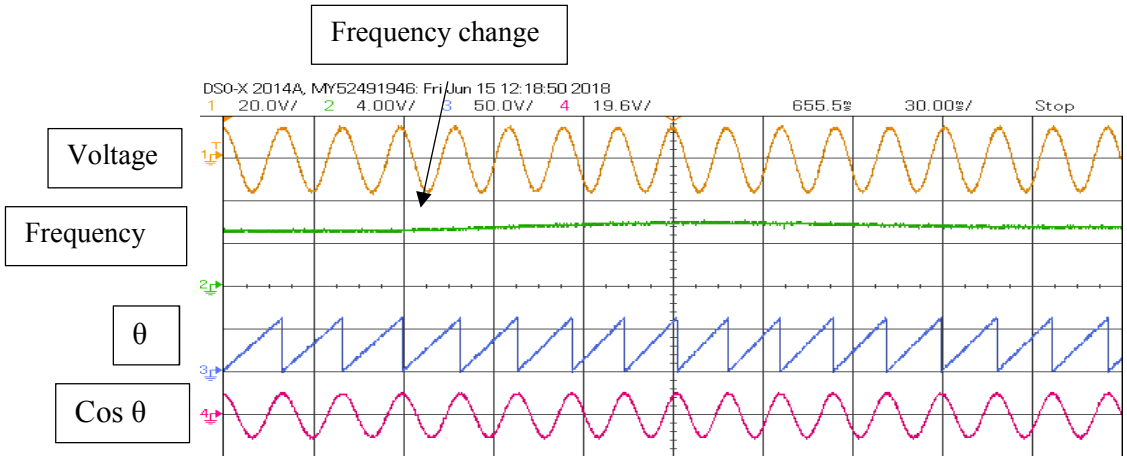

Figure 5.1: Experimental observation of transport delay PLL on DSO (frequency change)

(b) Introduction of 3rd harmonics

The voltage signal has been polluted with 3rd harmonics. It can be observed that the frequency signal develops oscillations during harmonics but the PLL tracks the frequency. The θ and Cos θ shows satisfactory results under harmonics effect.

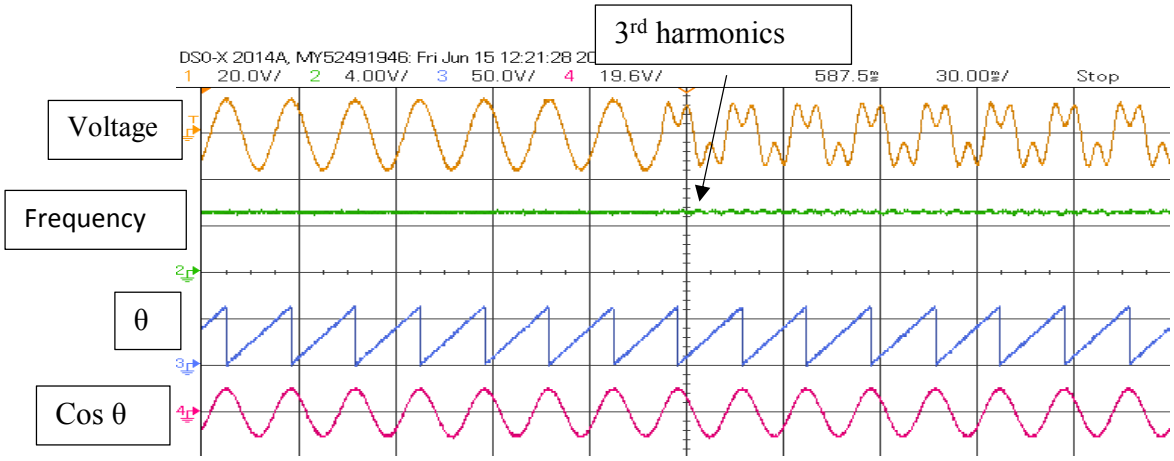

Figure 5.2: Experimental observation of transport delay PLL on DSO (introduction of 3rd harmonics)

(c) Introduction of Noise

The voltage signal was polluted with a noise signal. The frequency signal is maintained almost constant with only a very few oscillations. . The θ and Cos θ shows satisfactory results under noise effect.

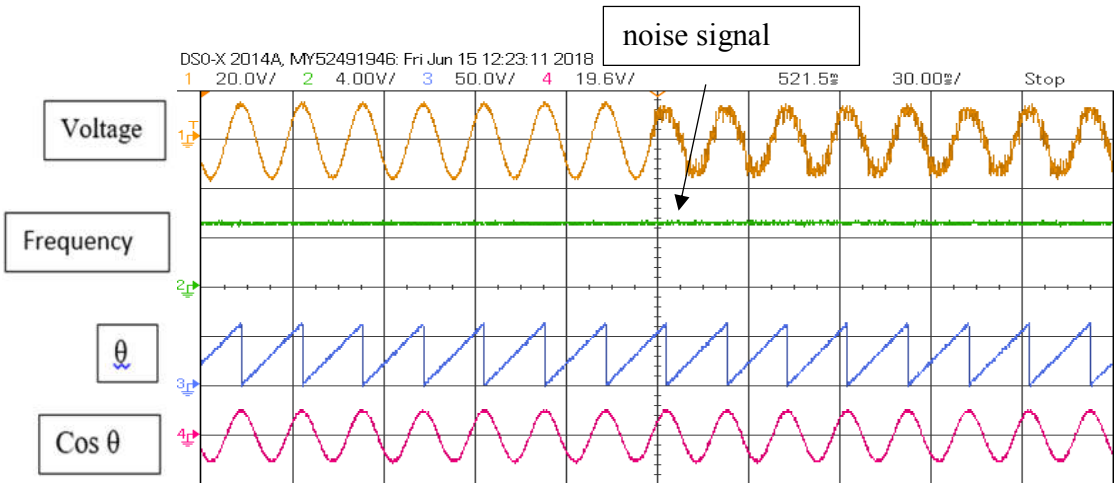

Figure 5.3: Experimental observation of transport delay PLL on DSO (introduction of noise)

5.2.2 EPLL

The EPLL was developed for experimental results. The disturbances under which the PLL has been studied are frequency change, introduction of 3rd harmonics and introduction of noise signal.

The following signals can be observed on the DSO:

1. Voltage signal
2. Frequency
3. Angle θ
4. Cos θ

(a) Frequency Change

Frequency was changed from 50 Hz to 55 Hz. It can be observed that the tracking of frequency is observed in nearly 12-13 cycles. The frequency signal shows oscillations. The voltage signal is synchronized with Cos θ.

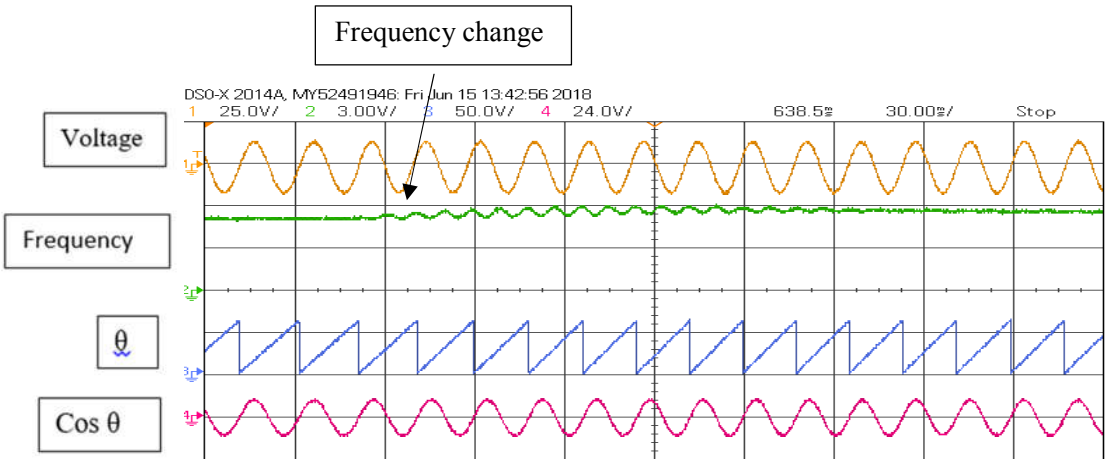

Figure 5.4: Experimental observation of EPLL on DSO (frequency change)

(b) Introduction of 3rd harmonics

The voltage signal has been polluted with 3rd harmonics. It can be observed that the frequency signal develops undamped oscillations during harmonics but the PLL tracks the frequency. The θ and Cos θ shows satisfactory results under harmonics effect.

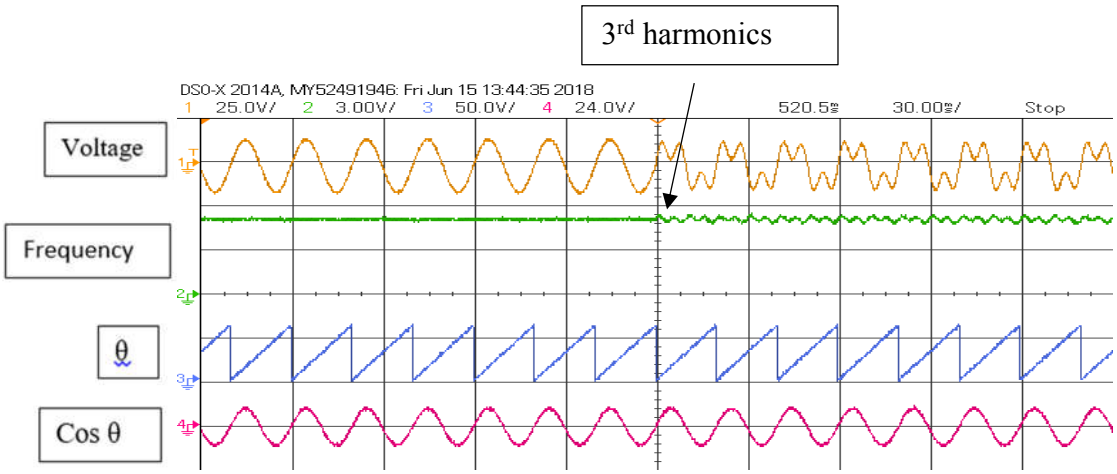

Figure 5.5: Experimental observation of EPLL on DSO (introduction of 3rd harmonics)

(c) Introduction of Noise

The voltage signal was polluted with a noise signal. The frequency signal comprises oscillations. The θ and Cos θ shows satisfactory results under noise effect.

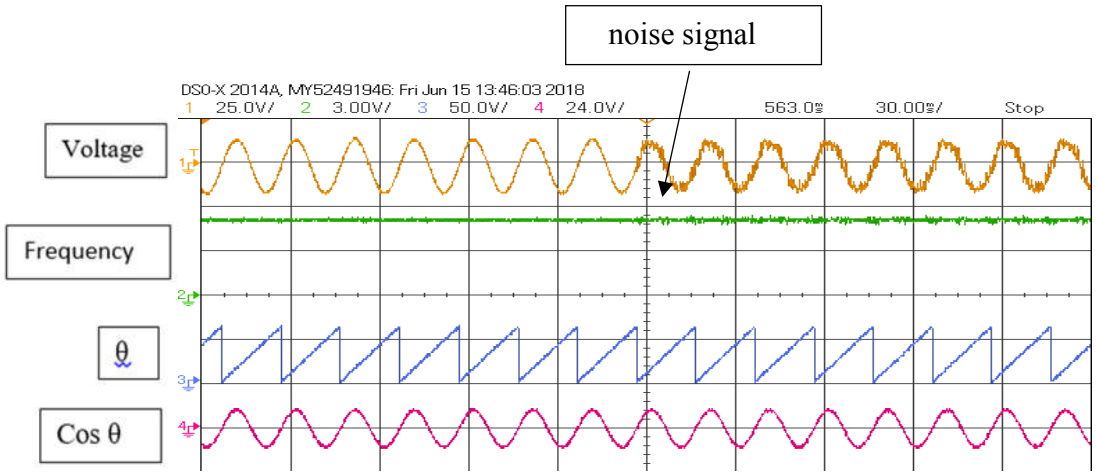

Figure 5.6: Experimental observation of EPLL on DSO (introduction of noise)

5.2.3 SOGI PLL

The SOGI PLL was developed for experimental results. The disturbances under which the PLL has been studied are frequency change, introduction of 3rd harmonics and introduction of noise signal.

The following signals can be observed on the DSO:

1. Voltage signal
2. Frequency
3. Angle θ
4. Cos θ

(a) Frequency Change

Frequency was changed from 50 Hz to 55 Hz. It can be observed that the tracking of frequency is observed in nearly 2-3 cycles. The frequency signal shows no oscillations. The voltage signal is synchronized with Cos θ.

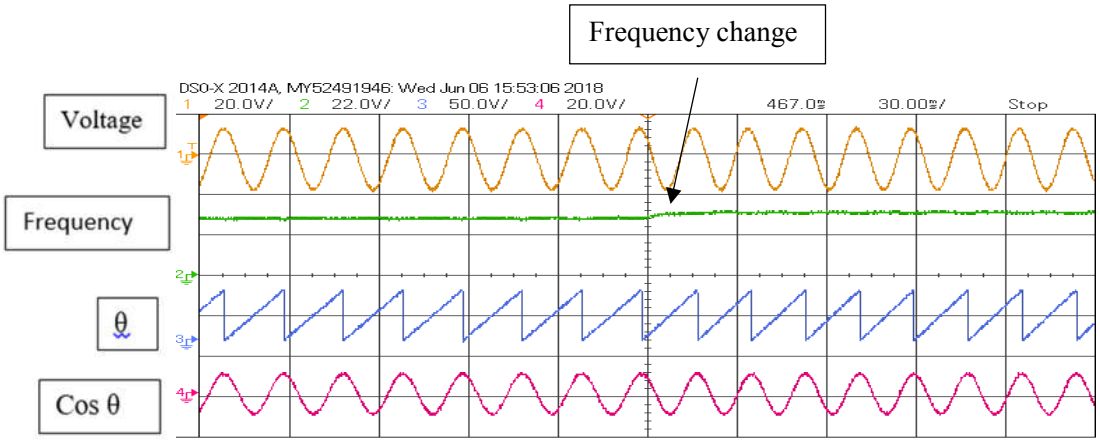

Figure 5.7: Experimental observation of SOGI PLL on DSO (frequency change)

(b) Introduction of 3rd harmonics

The voltage signal has been polluted with 3rd harmonics. It can be observed that the frequency signal develops a few oscillations during harmonics but the PLL tracks the frequency. The θ and Cos θ shows satisfactory results under harmonics effect.

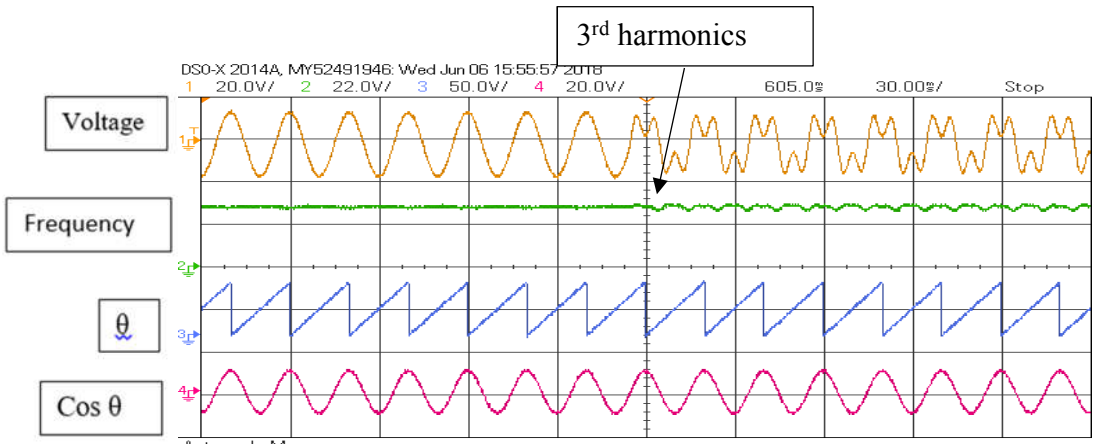

Figure 5.8: Experimental observation of SOGI PLL on DSO (introduction of 3rd harmonics)

(c) Introduction of Noise

The voltage signal was polluted with a noise signal. The frequency signal comprises almost no oscillations. The θ and Cos θ shows satisfactory results under noise effect.

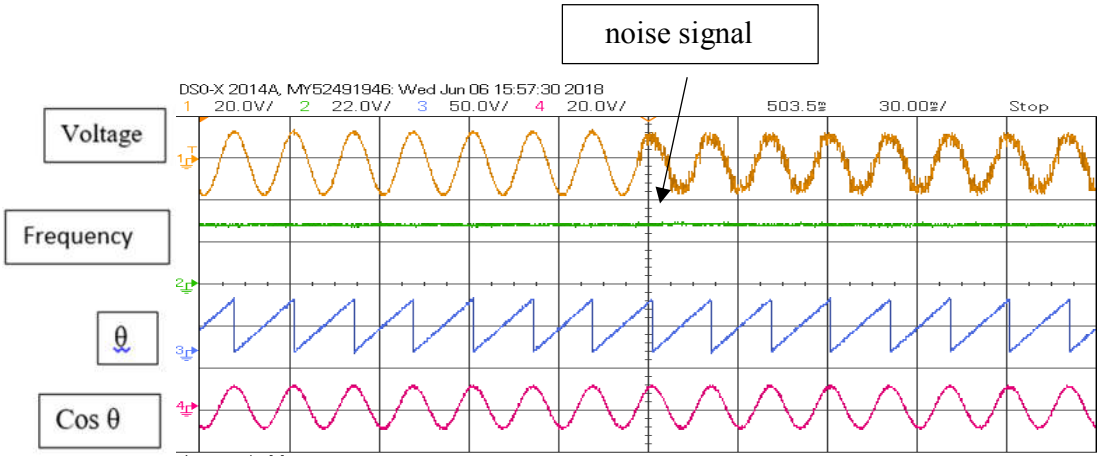

Figure 5.9: Experimental observation of SOGI PLL on DSO (introduction of noise)

5.3 COMPARISON

Based on the experimental results performed, a comparison of the three PLLs has been made in following table. The comparison is based on the settling time and the oscillations observed in the system.

TABLE 5.1: COMAPRISON OF SINGLE PHASE PLL BASED ON EXPERIMENTAL RESULTS

S.No	Single Phase PLL	Frequency tracking (no. of cycles)	Performance under harmonics	Performance under noise
1.	Transport delay PLL	6-7	Few oscillations	good
2.	EPLL	12-13	Large oscillations	satisfactory
3.	SOGI PLL	2-3	Few oscillations	good

5.3 CONCLUSION

The experiments were performed on a few single phase phase locked loop (PLL) techniques which includes transport delay PLL, EPLL and SOGI PLL. The comparison based on the experimental result shows that the SOGI PLL works the best amongst the three PLLs. The SOGI PLL has fast frequency tracking ability as its settling time is only 2-3 cycles. The frequency signal of the SOGI PLL remains oscillations free under effect of disturbances such as harmonics and noise.

CHAPTER 6

CONCLUSIONS

The thesis presents various synchronization methods applicable to both single phase systems and three phase systems. Simulation of the PLL and FLL techniques was performed in MATLAB/SIMULINK environment and the results were studied and compared. The comparison was made considering the two factors i.e. the settling time and the number of oscillations.

Chapter 1: The chapter 1 deals with the overview of the synchronizing techniques, the need of synchronization, motivation of the thesis, basic points about PLL and FLL etc.

Chapter 2: The chapter 2 deals with single phase PLL techniques, the basic points about the PLL techniques, their analysis and the simulation results in MATLAB/SIMULINK environment. The following single phase PLL were simulated and compared:

1. Transport delay PLL
2. Adaptive transport delay PLL
3. EPLL
4. SOGI PLL
5. Inverse park PLL
6. pPLL
7. DFAC PLL

The results of the changes i.e. frequency change, voltage amplitude change, phase angle change and effect of harmonics have been thoroughly investigated with the single phase PLLs and a comparison has been made based on these observations. The time taken to track the new value of frequency/ voltage change and phase angle change are thoroughly studied. The time taken by different single phase PLL schemes after frequency change to reach steady state is tabulated in the chapter.

According to the observations made, SOGI PLL was observed to show the most satisfactory performance on the basis of settling time and the no. of oscillations.

Chapter 3: The chapter 3 deals with three phase PLL techniques, the basic points about the PLL techniques, their analysis and the simulation results in MATLAB/SIMULINK environment. The following three phase PLL were simulated and compared:

1. Three phase SRF PLL
2. Three phase EPLL
3. Three phase Inverse park PLL
4. Three phase pPLL
5. Three phase DFAC PLL

The results of the changes i.e. frequency change, voltage amplitude change, phase angle change and effect of harmonics have been thoroughly investigated with the three phase PLLs and a comparison has been made based on these observations. The time taken to track the new value of frequency/ voltage change and phase angle change are thoroughly studied. The time taken by different three phase PLL schemes after frequency change to reach steady state is tabulated in the chapter.

According to the observations made, three phase SRF PLL was observed to show the most satisfactory performance on the basis of settling time and the no. of oscillations.

Chapter 4: The chapter 4 deals with single phase and three phase FLL techniques, the basic points about the FLL techniques, their analysis and the simulation results in MATLAB/SIMULINK environment. The following single phase and three phase FLL were simulated and compared:

1. Single phase SOGI based FLL
2. Single phase SOGI based FLL with gain normalization
3. Three phase standard FLL
4. Three phase FLL with dc offset rejection
5. Three phase CBF FLL 1
6. Three phase CBF FLL 2

The results of the frequency change has been thoroughly investigated with the single phase and three phase FLLs and a comparison has been made based on these observations. The time taken to track the new value of frequency change is thoroughly studied. The time taken by different single phase and three phase FLL schemes after frequency change to reach steady state is tabulated in the chapter.

According to the observations made, Single phase SOGI based FLL with gain normalization was observed to show the most satisfactory performance on the basis of settling time and the no. of oscillations in a single phase system. CBF FLL 2 was observed to show the most satisfactory performance on the basis of settling time and the no. of oscillations in a three phase system.

Chapter 5: The chapter 5 comprises experimental results performed on single phase transport delay PLL, EPLL and SOGI PL. The observations were made for various disturbances such as frequency change, harmonics and noise. The PLLs were observed to have satisfactory performance i.e. the PLL were maintained in the locked state even when the disturbances were induced. The comparison based on the experimental result shows that the SOGI PLL works the best amongst the three PLLs.

CHAPTER 7

FUTURE SCOPE OF WORK

In recent years, the single-phase power converters have received a considerable attention because of emerging applications/requirements such as the grid integrating of small scale renewable energy sources (particularly rooftop photovoltaic panels), vehicle-to-grid and grid-to-vehicle connections, low-power-rating uninterruptible power supplies, and small-scale power quality conditioners [1]–[5]. Converter interfaced distributed generator (DG) units must be synchronized with the utility system. Therefore, the synchronization of renewable sources of energy with the existing conventional grids require a satisfactory synchronization method. PLL and FLL are the few techniques which can be effectively used for grid integrating of small scale renewable energy sources.

The PLL has three basic components out of which one is the loop filter. The loop filter is incorporated by a PI controller. The tuning of the PI controller is of utmost importance for satisfactory operation of the PLL. The PI tuning depends of two parameters i.e. k_p (proportional gain) and k_i (integral gain). The tuning of these gains ensures optimum operation of the PLL. These gains can be set accordingly to obtain a reasonable sacrifice between the settling time, transients in the systems, oscillations in the system, etc.

There are several PLLs that are being researched upon and a few PLLs have been found out to achieve very less settling time i.e. less than 0.5 s. These PLLs are ROGI based PLL which shows optimum performance in terms of settling time and oscillations. The future of PLL as a synchronization method can be seen holding great advancements.

A few PLLs can be used to extract the load current fundamental component which can further be used for reactive power compensation, power factor improvement etc.

List of publication

1. Shikha Pilania, Alka Singh, Hemant Saxena, "Comparative Evaluation of Different Phase Locked Loop Schemes Applicable to Single Phase Systems" 12th INDIAcom 5th International conference on Computing for sustainable global development, March, 2018.

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