DESIGN AND IMPLEMENTATION OF ANALOG CIRCUITS USING CURRENT MODE BUILDING BLOCKS

A THESIS

SUBMITTED TO THE DELHI TECHNOLOGICAL UNIVERSITY

FOR THE AWARD OF THE DEGREE OF

DOCTOR OF PHILOSOPHY

IN

Electronics and Communication Engineering

SUBMITTED BY

DEVA NAND

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

DELHI- 110042 (INDIA)

2018

DESIGN AND IMPLEMENTATION OF ANALOG CIRCUITS USING CURRENT MODE BUILDING BLOCKS

BY

DEVA NAND

SUBMITTED TO THE DELHI TECHNOLOGICAL UNIVERSITY IN PARTIAL FULFILMENTS OF THE REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
DELHI- 110042 (INDIA)

2018

CANDIDATE DECLARATION

I hereby certify that the research work which is being presented in this thesis entitled **"Design and Implementation of analog circuits using current mode building blocks"** in fulfilment of requirements of the award of degree of Doctor of Philosophy, is an authentic record of my own research work carried out under the supervision of Prof. Neeta Pandey.

The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for award of any degree.

Deva Nand

2K11/PhD/EC/07
Department of Electronics and Communication Engineering
Delhi Technological University
Delhi, India-110042.

CERTIFICATE

This is to certify that the thesis entitled **"Design and Implementation of analog circuits using current mode building blocks"** being submitted by Mr. Deva Nand (Reg. No.: 2K11/PhD/EC/07) for the award of degree of Doctor of Philosophy to the Delhi Technological University is based on the original research work carried out by him. He has worked under my supervision and has fulfilled the requirements that to our knowledge have reached the requisite standard for the submission of this thesis. It is further certified that the work embodied in this thesis has neither partially nor fully submitted to any other university or institution for the award of any degree or diploma.

Prof. Neeta Pandey
(Supervisor)
Department of Electronics and Communication Engineering
Delhi Technological University, Delhi
India-110042

ACKNOWLEDGEMENT

I owe my debt and would like to express deep feelings of gratitude to accomplish the research program with the support and direction of several persons. This challenging and rewarding experience definitely helped me to grow in character as well as academically. It is a pleasant aspect that I have now the opportunity to express my gratitude for all of them.

First and foremost, I would like to thank my supervisor, Prof. Neeta Pandey for insightful advices, conversations and suggestions during PhD work. Her support and trust, together with genuine interest in the research subject, turned my research work into a great experience. Words cannot express my gratitude to her for her patience and support.

Special thanks to DRC chairman/HOD, ECE Prof. S. Indu and Dean academics (PG) Prof. H. C. Taneja for all the administrative support that made the journey smoother. Heartfelt thanks to Prof. Rajeshwari Pandey for her unconditional support, discussions and encouragement all the time. Words cannot express my gratitude to her. I will be thankful to my colleagues for all their helps and comments throughout. I wish to pay high regards to my parents, in-laws, my wife and my children for their invaluable support, best wishes and encouragements.

Last but not least, I would like to thanks my all faculty colleague and friends who supported me during this period directly or indirectly.

Date: (Deva Nand)

Place: Delhi

ABSTRACT

Rapid advancements in semiconductor technology has made integration of millions of transistors on a single die. The analog – digital boundaries are diminishing and integrated solutions for complete system are in vogue where both analog and digital subsystems are placed on single die. Though in last two decades' electronic circuit design has a paradigm shift from analog to digital domain yet analog circuit design is going to remain in mainstay. For signal acquisition and processing, amplifiers, filters, sample and hold circuits, signal comparators, analog to digital converter (ADC) and digital to analog converter (DAC) are required. Further, new applications continue emerging and require high performance analog interface circuits.

There are challenges in designing analog circuits due to continual scaling of device dimensions and also the power supply voltages. The lowering in power supply lead to reduction in input common mode range, linearity and output voltage swing. It is well known that signal processing may be done by manipulating node voltages or branch currents. The analog circuits are termed as voltage mode (VM) or current mode (CM) if the information medium is represented by the nodal voltages or branch currents. The performance parameters of VM circuits such as dynamic range, slew rate and common mode range are severely affected by scaling. The CM circuits show advantageous features such as improved slew rate due to smaller time constant, wider bandwidth, as transistors in current amplifiers may be used till unity gain bandwidth. Further as current depends nonlinearly on voltage, a smaller voltage swing allows larger current change, thus improving dynamic range. Further, these circuits may be compact as addition of current can done by simply joining branches. To exploit the advantages of CM signal processing, a wide variety of analog building blocks have been developed. Operational floating current conveyor (OFCC) is one

among these building block which combines the features of current conveyor and the current feedback operational amplifier along with additional current outputs that adds flexibility in the circuit design. It can readily be used for processing and providing both current and voltage at appropriate impedance levels.

Numerous OFCC based signal processing applications such as basic amplifiers, filters, oscillators, instrumentation amplifiers (IAs), variable/programmable gain amplifiers (VGA/PGA), read out circuits, wheat-stone bridge and logarithmic amplifier, as available in open literature. The main focus of the work presented in this thesis is to develop circuits which are more versatile, modular, integrable and can provide better quality response.

A first order Transadmittance mode (TAM) filters is presented that processes signal from voltage sensor and provide current output for further processing. It provides three responses i.e. low pass, high pass and all pass at high impedance. A feature that is gainfully used for developing an oscillator without using any extra active blocks. Second order CM SIMO filter is put forward that can provide low pass, high pass, band pass and notch responses simultaneously. The filter parameters can be adjusted independently. As an application a CM shadow bandpass filter is developed for controlling filter parameters through an amplifier gain. Electronic tunability of filter parameters is achieved via MOS based resistors.

Instrumentation amplifier (IA) is widely used in applications pertaining to medical instrumentation, sensor read out integrated circuits, data acquisition systems, industrial process control, automotive transducers, bio-potential acquisition systems and linear position sensing. Two generalized structure of IA is put forward and its usefulness is shown through OFCC. These structures are termed as: Structure-I and Structure-II. Each structure is used to generate IA topologies operating in VM, CM, TIM and TAM, thus eight IAs are generated in total. A

modification to Structure I and Structure II are suggested to obtain IA topologies with reduced resistor count. Considering the modifications, six more topologies are put forward. The input and output impedance of all proposed topologies are proper therefore no additional active block is needed for interfacing.

Amplifiers, in particular PGA, find applications in instrumentation, photodiode circuits, ultrasound preamplifiers, sonar, wide dynamic range sensors, driving ADCs and automatic gain control (AGC) loops. A new OFCC based PGA is the key contribution towards such amplifiers which offers programmable gain feature.

The rectifiers are widely used in applications pertaining to telecommunication, instrumentation and measurement. OFCC based CM half wave rectifiers (HWRs) and full wave rectifier (FWR) are put forward. These rectifiers do not use diode and are thus suitable for low voltage rectification. It is pertinent to mention here that all proposed rectifiers use single active block and are resistor-less.

The behavior of all the proposed circuits under the influence of nonidealities of OFCC is also examined. The functionality of proposed circuits is verified through SPICE simulations and/or through experimental observations.

TABLE OF CONTENT

CANDIDATE DECLARATION……..i

CERTIFICATE……ii

ACKNOWLEDGEMENT……..iii

ABSTRACT……...iv

TABLE OF CONTENT…….....vii

LIST OF FIGURES…….....x

LIST OF TABLES……..xiv

CHAPTER 1 INTRODUCTION……1

1.1 Background…….……...3
1.2 Available literature and scope of work……..5
1.3 Thesis organization……..…….11

CHAPTER 2 CURRENT MODE BUILDING BLOCK……13

2.1 Introduction……..15
2.2 Operational floating current conveyor……16
2.3 Effect of nonidealities.……16
2.3.1 Effect of finite transimpedance gain……17
2.3.2 Effect of voltage and current tracking errors……17
2.4 OFCC realization…….……18
2.4.1 CMOS based implementation……...18
2.4.2 CFOA based implementation……21
2.5 Basic applications of OFCC……21
2.5.1 Voltage amplifier…….....22
2.5.2 Current amplifier…….....23
2.5.3 Transadmittance amplifier……25
2.5.4 Transimpedance amplifier……26
2.5.5 Voltage difference amplifier……28
2.6 MOS based resistor implementation……31
2.7 Concluding remarks……32

CHAPTER 3 OFCC BASED TA MODE FIRST ORDER FILTER……33

3.1 Introduction……..35
3.2 Literature review……..36
3.3 Proposed first order TAM filter…….....37
3.3.1 Filter structure…….....37
3.3.2 Non ideal analysis……39
3.3.2.1 Finite transimpedance gain……39
3.3.2.2 Tracking error……41
3.3.3 Filter application……42
3.4 Simulation results……43
3.5 Concluding remarks……48

CHAPTER 4 OFCC BASED CM SECOND ORDER FILTER…..……49

4.1 Introduction……..51
4.2 Literature review of CM SIMO filters……52
4.3 Proposed CM SIMO filter……54
4.3.1 Proposed OFCC based CM SIMO Filter……..54
4.3.2 Non ideal analysis……56
4.3.2.1 Effect of finite transimpedance gain…….....56
4.3.2.2 Effect of tracking errors……57
4.3.2.3 Effect of parasites…….....58
4.4 Proposed OFCC based CM shadow band pass filter…….....60
4.5 Simulation results……63
4.6 Concluding remarks……69

CHAPTER 5 OFCC BASED INSTRUMENTATION AMPLIFIER……...71

5.1 Introduction……..73
5.2 Literature review……..73
5.3 Proposed generalized IA structures……..76
5.3.1 Proposed generalized IA structures……...76
5.3.2 IA topologies derived from Structure I……77
5.3.3 IA topologies derived from Structure II……79
5.3.4 Non ideal analysis……81
5.3.4.1 Effect of the finite transimpedance gain……81
5.3.4.2 Tracking errors……...82
5.3.5 Simulation results……..85
5.3.6 Experimental results……..89
5.4 OFCC based IA topologies with reduced component count…….....90
5.4.1 IA topologies derived from modified Structure I…….....90
5.4.2 IA topologies derived from modified Structure II……92
5.4.3 Non ideal analysis……93
5.4.4 Simulation results……..96

5.5 Performance comparison……..98
5.6 Concluding remarks…….....101

CHAPTER 6 OFCC BASED TRANSIMPEDANCE MODE PGA……103

6.1 Introduction……105
6.2 Literature survey……106
6.3 Proposed OFCC based PGA……..108
6.4 Simulation and Experimental results……112
6.4.1 Simulation results……112
6.4.2 Experimental results……116
6.5 Concluding remarks…….....117

CHAPTER 7 OFCC BASED CM RECTIFIER……...119

7.1 Introduction……121
7.2 Literature survey……121
7.3 Proposed OFCC based rectifiers……123
7.3.1 Proposed CM HWRs…….....123
7.3.2 Proposed CM FWR……124
7.4 Simulation results…….....125
7.5 Concluding remarks…….....131

CHAPTER 8 CONCLUSION AND FUTURE SCOPE……...133

8.1 Conclusion…….135
8.2 Summary of work carried out in this thesis……135
8.3 Future scope…….....137

REFERENCES……...141

LIST OF PUBLICATIONS……....159

AUTHOR'S BIOGRAPHY……161

LIST OF FIGURES

Fig. 2.1 OFCC Circuit symbol……16

Fig. 2.2 Implementation scheme for OFCC block [13]……..19

Fig. 2.3 CMOS schematic of OFCC block [13]……..19

Fig. 2.4 Frequency response of (a) current transfer (b) voltage transfer characteristics of OFCC……...…….20

Fig. 2.5 (a) Circuit symbol of AD844 [170] (b) AD844 based OFCC implementation ……...….21

Fig. 2.6 Voltage amplifier using OFCC…….22

Fig. 2.7 Frequency response of voltage amplifier……..23

Fig. 2.8 Current amplifier using OFCC……..23

Fig. 2.9 Frequency response of current amplifier……...24

Fig. 2.10 Transadmittance amplifier……...25

Fig. 2.11 Frequency response of transadmittance amplifier……..26

Fig. 2.12 Transimpedance amplifier……..26

Fig. 2.13 Frequency response of transimpedance amplifier……27

Fig. 2.14 Voltage Difference Amplifier…….29

Fig. 2.15 Frequency response of voltage difference amplifier with (a) gain=1 (b) gain=5……30

Fig. 2.16 MOS based resistor implementation [169]…..…….31

Fig. 3.1 TA mode first order filter circuit……38

Fig. 3.2 Proposed filter (a) with integrator (b) as an oscillator……..…….43

Fig.3.3 Frequency response of first order (a) LP and HP (b) AP and HP filter……..44

Fig. 3.4 Phase response of first order AP filter…….….44

Fig.3.5 Transient responses for (a) low pass output (I_o) (b) High Pass output (I_{HP})……45

Fig. 3.6 (a) Transient response and (b) corresponding Lissagous figure for all pass filter……...46

Fig. 3.7 Sinusoidal oscillator output (a) simulated (b) experimental……..47

Fig. 4.1 Proposed OFCC based CM SIMO Filter……54

Fig. 4.2 Proposed OFCC based CM SIMO filter with parasites……58

Fig.4.3 (a) Generalized scheme of shadow filter [81], (b) Proposed OFCC based CM shadow band pass filter……..60

Fig. 4.4 Theoretical and simulated responses of CM SIMO filter……63

Fig. 4.5 Simulated magnitude and phase plots of all pass response……64

Fig. 4.6 Tuning of f_o and Q_o……65

Fig. 4.7 Transient responses for Sinusoidal current input of 2μA, 500 KHz……..65

Fig. 4.8 Frequency spectrum of (a) input (b) low pass (c) high pass and (d) band pass output……...66

Fig. 4.9 Simulated and experimental bandpass frequency response…….....66

Fig. 4.10 LP controlled shadow BP response……67

Fig. 4.11 HP controlled shadow BP response……68

Fig. 4.12 BP controlled shadow BP response……68

Fig. 4.13 LP controlled shadow BP response with bandwidth ($BW_{\_LPC}$) independent of ω_{o_LPC} and Q_{o_LPC}……68

Fig. 5.1 Generalized Block Diagrams (a) Structure I (b) Structure II……76

Fig 5.2 Proposed (a) VM (b) TAM (c) CM and (d) TIM IA topologies generated from Structure I……..78

Fig 5.3 Proposed (a) VM (b) TAM (c) CM and (d) TIM IA topologies generated
from Structure II…..……..79
Fig. 5.4 Simulated frequency responses for differential gain and CMRR for
(a) topology 1 (b) topology 2 (c) topology 3 (d) topology 4……..86
Fig. 5.5 Simulated frequency responses for differential gain and CMRR for
(a) topology 5 (b) topology 6 (c) topology 7 (d) topology 8……..87
Fig. 5.6 Observed output responses for input frequencies (a) 100 KHz (b) 1 MHz……..89
Fig. 5.7 Simulated and experimental frequency responses for
(a) differential gain and (b) CMRR……..….89
Fig. 5.8 Generalized block diagram of IAs (a) modified Structure I
(b) modified Structure II……...91
Fig. 5.9 Proposed (a) VM (b) TAM (c) CM and (d) TIM IA topologies generated
from Structure I……...91
Fig. 5.10 Proposed (a) VM (b) TAM IA topologies generated from Structure II……93
Fig. 5.11 Simulated frequency responses for differential gain and CMRR for
(a) topology 9 (b) topology 10 (c) topology 11 (d) topology 12……..96
Fig. 5.12 Simulated frequency responses for differential gain and CMRR for
(a) topology 13 (b) topology 14……..……97
Fig. 6.1 PGAs in data acquisition systems [121]…….….105
Fig. 6.2 Block diagram of proposed Programmable Gain Amplifier……108
Fig. 6.3 (a) Current gain block (b) digitally controlled I-V converter
(c) R-2R ladder network (d) voltage buffer…….....109
Fig. 6.4 Circuit level realization proposed Programmable Gain Amplifier…….110
Fig. 6.5 Schematic of (a) 2x1 multiplexer using transmission gates

(b) 2x4 decoder……..…..111

Fig. 6.6 Frequency response of proposed PGA with coarse gain setting of

(a) 1111 (b) 0001…….112

Fig. 6.7 Variation in gain with respect to control word of the proposed PGA……....…113

Fig. 6.8 Transient responses of proposed PGA with B_3–B_0 = 1111 and B_5B_4 as

(a) 00 (b) 01 (c) 10 (d) 11…….114

Fig. 6.9 Experimental output response……..……...…116

Fig. 7.1 Proposed Half wave rectifiers circuit……..124

Fig. 7.2 Proposed Full wave rectifier circuit……125

Fig. 7.3 (a) Input current (b) Voltage at Z_{2+} port……..126

Fig. 7.4 HW rectified outputs for (a) positive cycle of input current

(b) negative cycle of input current……...127

Fig. 7.5 Ripple factor of HW rectifier under sinusoidal excitation……..127

Fig. 7.6 DC response of the proposed HW rectifiers circuit for

(a) positive current and (b) negative current transfers…….128

Fig.7.7 (a) Input current (b) Voltage at Z_{2+} port (c) FW rectified output…….130

Fig. 7.8 Ripple factor of proposed FWR under sinusoidal excitation……..130

Fig. 7.9 Input and output waveform under triangular excitation for proposed FWR……..130

Fig. 7.10 DC response of the proposed FWR……131

LIST OF TABLES

Table 2.1 Transistor's aspect ratios [13]…….19

Table 2.2 Simulated values of MOS based resistance [169]……..32

Table 3.1 Available TA mode first order filters…….37

Table 4.1 Comparative analysis of CM SIMO Filters……53

Table 4.2 Simulation settings for independent adjustment of filter parameters…….64

Table 4.3 Tuning of shadow filter parameters……....69

Table 5.1 Characteristics of available Instrumentation Amplifiers……..…75

Table 5.2 Stage Description…….……...77

Table 5.3 Differential gain, common mode gain and CMRR with finite transimpedance gain (Z_t)……..84

Table 5.4 Differential gain, common mode gain and CMRR with tracking errors……..85

Table 5.5 Summary of simulation results for IA topologies 1-8……88

Table 5.6 Differential gain, common mode gain and CMRR with finite transimpedance gain (Z_t)…...…….……..94

Table 5.7 Differential gain, common mode gain and CMRR with tracking errors……..95

Table 5.8 Differential gain, common mode gain and CMRR with finite transimpedance gain (Z_t) and tracking errors……..95

Table 5.9 Summary of simulation results for new IA topologies 9-14……....99

Table 5.10 Comparison of performance parameters of available and proposed IAs…….....……100

Table 6.1 Literature Survey on previously reported PGAs……...106

Table 6.2 Truth Table for 2x1 Multiplexer……..……111

Table 6.3 Truth Table for 2 to 4 Decoder…….……..111

Table 6.4 Performance analysis of previously reported PGAs…….115

Table 6.5 Experimental measurement results and error calculation…….117

Table 7.1 Literature survey of available rectifiers……122

CHAPTER - 1

INTRODUCTION

1.1 BACKGROUND

The advancements in VLSI technology has made it possible to integrate millions of transistors on a single die [1]. The analog – digital boundaries are diminishing and integrated solutions for complete system are in vogue where both analog and digital subsystems are placed on single die. Though in last two decades' electronic circuit design has a paradigm shift from analog to digital domain yet analog circuit design is going to remain in mainstay [2]. For signal acquisition and processing, amplifiers, filters, sample and hold circuits, signal comparators, analog to digital converter (ADC) and digital to analog converter (DAC) are required. Further, new applications continue emerging and require high performance analog interface circuits.

The analog circuits are broadly classified as voltage mode (VM) if the information medium is represented by the nodal voltages of the circuits, else as current mode (CM) if the information is represented by time varying currents. The VM circuits are widely employed in applications in comparison to their CM counterparts. This can be attributed to – ease in nodal voltage measurement than branch current (additional circuitry is required); very large input impedance at gate of MOS transistor; and availability of circuit topologies for high voltage gain. The quest for putting more and more circuitry on same die area has led to aggressive scaling of device dimensions, threshold and supply voltage. Some of the after effects of scaling on performance of VM circuits are dynamic range reduction, slew rate, and common mode range. Impact of scaling is less severe in CM circuits as these work on branch currents instead of nodal voltages. Though the performance of any circuit depends on characteristics of the device, current mode circuits may prove advantageous in terms of bandwidth, linearity, slew rate, power consumption and accuracy

for specific applications. Further, these circuits may be compact as addition of current can be done by simply joining branches.

To exploit the advantages of CM signal processing, a wide variety of analog building blocks have been proposed in the literature. Current conveyor (CC) [3, 4, 106, 147] is one among these blocks which is widely explored. It can process both voltage and current signals appropriately and is called voltage/current hybrid circuit. The advantageous features of CC have culminated into development of its extended versions namely first generation current conveyor (CCI) [4], second generation current conveyor (CCII) [5, 35, 65, 96, 102-104, 113, 124, 135, 153, 155, 158, 160, 161, 164, 166] and third generation current conveyor (CCIII) [6, 39, 44, 45, 54, 78]. These blocks share some common port characteristics while other port characteristics slightly differ from one another. Subsequently, extended versions of current conveyors namely differential voltage current conveyor (DVCC) [38, 52, 79, 154, 155, 159], differential difference current conveyor (DDCC) [40], z-copy voltage differencing current conveyor (ZC-VDCC) [49], second generation current controlled current conveyor (CCCII) [56, 70, 71, 76, 107, 111, 150, 162], multiple output current conveyor (MOCC) [57, 62, 63, 66], multiple output second generation current controlled conveyor (MOCCCII) [64], dual output current conveyor (DO-CCII) [58, 67, 74], dual output inverting CCII (DO-ICCII) [75], dual output third generation current conveyor (DO-CCIII) [67], Digitally Programmable CCII (DPCCII) [122], Digitally Controlled Fully Differential CCII (DCFDCCII) [123], Fully Differential CCII (FDCCII) [136], Extra-X second generation current conveyor (EXCCII) [148], dual-X second generation current conveyor (DXCCII) [149, 152] are developed. Operational floating current conveyor (OFCC) [7-33, 50] is another variant of CC family that offer more flexibility and additional current output options. Operational Transconductance Amplifier (OTA) [59, 78, 141, 142, 159, 163] is yet another block that processes

voltage input and provides current output. Its properties are combined with differential input buffer, current conveyor, current follower, current inverter and current difference to result in fully differential input output operational transconductance amplifier (FDIO-OTA) [151], differential input buffered transconductance amplifier (DBTA) [47, 48], current conveyor transconductance amplifier (CCTA) [53, 73], current follower transconductance amplifier (CFTA) [55, 77], Z-copy current follower transconductance amplifier (ZC-CFTA) [60, 72] and Z-copy current inverter transconductance amplifier (ZC-CITA) [61], current difference transconductance amplifier (CDTA) [41, 156, 157] respectively. Few other active blocks are modified current backward transconductance amplifier (MCBTA) [46], multiple output current follower (MO-CF) [69], operational transresistance amplifier (OTRA) [117], operational conveyors (OC) [110], operational amplifier (OPAMP) [97-101, 105, 106, 108, 109, 112, 114, 116, 119, 143-145], current feedback operational amplifier (CFOA) [118, 125] and its variant such as Fully Differential Current Feedback Op Amp (FDCFOA) [126], current difference buffered amplifier (CDBA) [165] and floating current source (FCS) [167]. The topologies [128, 129, 132, 133, 137, 140] employ differential amplifier where along with differential amplifier [128] using current mode feedback (CMFB) and [140] using flipped voltage follower (FVF). A review of available active blocks is presented in [168] along with possible future directions.

1.2 AVAILABLE LITERATURE AND SCOPE OF WORK

Numerous applications such as filters, oscillators, instrumentation amplifiers, programmable gain amplifiers, multivibrators and rectifiers have been developed using active blocks. The circuit topologies, based on the type of input signal processed and output signal provided, are classified as voltage mode (VM), current mode (CM), transimpedance mode (TIM) and transadmittance

mode (TAM). The VM and TAM mode circuits process voltage signal whereas CM and TIM mode circuits process current signal. The voltage output is available in VM and TIM mode circuits while CM and TAM mode provide current output.

There is widespread use of filters in instrumentation and communication systems. The filter comprises of interconnection of passive components (inductors, capacitors and resistors) and active devices such as controlled sources, amplifiers, transistor etc. [34]. Low pass, high pass, bandpass and band reject/notch are typical filter categories when magnitude is of prime concern while all pass filter or delay equalizers is important when phase or delay specifications are to be met while keeping magnitude constant. Other classifications are - first, second or higher order depending upon the roll off characteristics, single input single output (SISO), single input multiple output (SIMO), multiple input single output (MISO) and multiple input multiple output (MIMO) depending upon number of inputs being processed and output provided.

The first order low pass and high pass filters find applications in communication systems while all pass filter is commonly used analog filter offering capability to modify phase of the input signal with unity magnitude for all frequencies. Over the desired frequency range, phase varies from 0˚ to 180˚, due to this frequency dependent time displacement property first order all pass filters may be used in radio systems, communication subsystems such as reconstruction filters and signal generation using multiphase sinusoidal oscillators and quadrature oscillators [35]. First order VM, CM and TAM mode filters are presented in [35-40, 47-49], [39, 41-43, 49, 50] and [44-49] respectively. The structures reported in [38, 39] provide low pass, high pass and all pass responses simultaneously. First order filters with low pass, high pass and all pass functions are reported in VM [38, 39] and CM [39] only. First order TAM filters [44-49] provide all pass response only.

Thus literature survey suggests that no first order TAM filter was present in open literature that provide low pass, high pass and all pass responses simultaneously. This has led to development of TAM filter capable of providing all three responses.

A wide variety of second order CM SIMO filters presented in [29, 30, 52-79] and references cited therein. The features of CM SIMO filters [29, 30, 52-79] differ in terms of number of active blocks and passive elements used; types of active blocks used; input/output impedances; simultaneous availability of output responses; and independent adjustment of the filter parameters. Single active blocks is used in filters reported in [53, 54 (Fig. 2, 3), 77] whereas multiple active blocks of different and similar types are employed in [56, 67, 68, 71, 76, 78] and [55, 60, 65 (Fig. 5a, 9a), 70 (Fig. 3)] respectively. The number of simultaneously available responses are two in [54, 55], three in [29, 52, 53, 57-59, 61-69, 72-75, 77-79], four in [30] and all the five in [56, 60, 70 (Fig.3 & 4), 71, 76]. Few responses are available through components in [30, 53, 54 (Fig.2, 3), 59, 77]. The desired condition of low input impedance in CM filters is not maintained in [29, 52-54, 59, 63, 64, 73, 77, 79]. The configurations [54, 57, 65, 69, 79] use floating passive elements which are not suitable from fabrication viewpoint. Therefore, additional active blocks would be required to process output further. References [29, 30, 52, 54, 55, 59, 61-67, 69, 70, 77] do not support independent adjustment of filter parameters. The parameters adjustment is possible in [55, 56, 60, 68, 71-73, 76] and [53, 58, 65 (sec. 2.2, 3.2), 74, 75, 78, 79] through transconductance (g_m) or internal resistance of active block. It is clear from above discussion that only one SIMO filter [60] is available that uses similar active blocks and provides four or more output responses at high output impedance; and allows independent adjustment of filter parameters. This configuration, however, uses four active blocks.

Thus, single SIMO filter [60] is available that uses similar active blocks and provides four or more output responses at high output impedance. This configuration, however, uses four active blocks. Alternate topology that uses reduced number of similar active blocks may therefore be explored.

The instrumentation amplifier (IA) is used as an input stage in variety of applications such as medical instrumentation [87,88], sensor read out integrated circuits [89], data acquisition systems [2, 90], industrial process control [91], automotive transducers [92], bio-potential acquisition systems [93], [94] and linear position sensing [95]. Numerous IA are available in the literature [14, 96-119] and are classified on the basis of active block employed for implementation. Conventionally the operational amplifier based IAs are termed as voltage mode IAs (VMIA) [97-101, 112, 114, 116, 119] whereas current mode building block based IAs are referred as current mode IAs (CMIA) [14, 96, 102-111, 113, 118]. Most of the available IAs [14, 96-114] can process data sensed by voltage sensor but need current to voltage converter for processing current sensors' data. The IAs [96,115-118] are suitable to process data available from current sensor and provide current [115,118] and voltage outputs [96,116,117]. The IAs may be categorized as VM, CM, TAM and TIM depending on the basis of input and output signals. Accordingly, the IAs presented in [14, 96-114, 119], [107], [115,118] and [96,116,117] are VM, TAM, CM and TIM IAs respectively. Though the input impedance of VM IA topologies [14, 96-114] is high, the output is not available at low impedance [14, 96, 102-104, 106, 107, 110, 111, 113]. It is therefore necessary to place a buffer at the output for isolation. The CM and TAM IA topologies with proper impedance level are put forward in [115] and [107] respectively. The output impedance of TIM IA topologies [116, 117] is proper but former has high input impedance. The IAs [97-101, 112, 114, 116] are designed using operational amplifier and therefore exhibit narrow and gain

dependent bandwidth. The gain is independent of band width in [14, 96, 102-104, 107, 110, 111, 113, 115, 117, 118] as current mode active blocks namely OFCC [14], CCII [96, 102-104, 113], CCCII [107, 111], OC [110], OTRA [117] and CFOA [118] are being used. The IA topologies presented in [105, 106, 108, 109, 119] employ both voltage and current mode active blocks, their bandwidth will be decided by the bandwidth of voltage mode active block.

Though a variety of CM active blocks based VM IA topologies are available, yet none of these provide output at low impedance. Additional active block is required to satisfy impedance requirement. Generalized IA topology is not available. Also, OFCC based CM, TAM and TIM mode IA are not available.

Amplifiers, in particular programmable gain amplifiers (PGAs), find applications in instrumentation, photodiode circuits, ultrasound preamplifiers, sonar, wide dynamic range sensors, driving ADCs (some ADCs have on-chip PGAs), automatic gain control (AGC) loops [120, 121]. Typically, PGA [121] in data acquisition system is placed between a sensor and analog to digital converter (ADC). Additional signal processing circuitry, as per demand of application, may be placed before or after the PGA. Former location is, however, preferred as it allows to condition a larger signal. Typically, operational amplifiers are employed in designing PGAs. The PGA designs [13, 122-143] provide voltage output and process data from voltage sensor. A current to voltage converter is needed if data is sensed from current sensor. The PGA design [122] processes data sensed from current sensor and provides current output. A current to voltage converter is required in case there is a need of interfacing it with circuit having input as voltage. Different active blocks such as CCII [124, 135] and its variants such as DPCCII [122], DCFDCCII [123] and FDCCII [136]; CFA [125] and its variant such as FDCFOA [126]; OFCC is used in [13]; the topologies [128, 132, 133, 137, 140] employ differential amplifier; CMOS based simple single ended and

fully differential gate driven variable gain amplifier (VGA) with programmable gain is also reported in [138, 139]; few topologies with OTA is reported in [141, 142]; whereas [143] employs op-amp for PGA design. The input and output impedances are proper in [13, 125, 127, 129, 130, 133, 138-140, 143] while additional active block is needed in [122-124, 126, 128, 131, 132, 134-137, 141, 142] to satisfy impedance condition. Gain tuning is achieved through current division networks (CDN) [123, 124, 134], weighted transistor arrays [122, 133], potentiometer [125, 126, 132, 136] or switches [13, 127-129, 131]; and digitally controlled exponential function [130] or current mirrors [135]; 4-bit Digitally controlled look up table and pre-calibration method [137]; DAC gain control (dB linear/digital) [138]; 4-bit and 5-bit digitally programmable VGA [139]; source degenerated capacitor array [140]; two stacked transistors [141]; switched capacitor array [142]; and resistor array with MOS switches [143]. Explicit mechanism for fine and coarse gain tuning is applied in [13, 124] and [143].

The discussion of available PGA indicates non-availability of TIM PGA which may be useful when input is sensed in form of current and a voltage output is needed for either further processing or display.

The rectifiers are widely used in applications pertaining to telecommunication, instrumentation and measurement [144-147]. Some of the applications are ac voltmeter, averaging circuits, peak value detectors, clipper circuits, amplitude-modulated signal detectors, signal-polarity detectors etc. Various current mode blocks are also incorporated in rectifiers such as OPAMP [144, 145], CCIICS [146], CC [147], EXCCII [148], DXCCII [149, 152], CCCII [150, 162], FDIO-OTA [151], CCII [153, 155, 158, 160, 161, 164, 166], DVCC [154, 155, 159], CDTA [156, 157], OTA [159], DO-OTA [163], CDBA [165] and FCS [167]. Available rectifiers operate in VM [144 - 147, 149 – 155, 160, 161, 163, 164, 166, 167], CM [148, 156-159, 165] and TAM

[162]. More than one active block is reported in [144 – 147, 152, 154, 155, 158, 161, 162, 164, 166]. VM rectifiers [144-147, 151, 154, 161, 163, 164, 166, 167] and CM rectifiers in [156-159, 165] use diodes to achieve rectification. The input and output impedance of VM rectifier [144, 146, 147, 149-153, 155, 161, 164, 167] and CM rectifier [157] are not proper hence additional active block is required. Resistances and MOS transistors are also used in [144-147, 150-157, 159-163, 166, 167] and [148-150, 152, 153, 155, 164] respectively.

1.3 THESIS ORGANIZATION

The thesis is organized in eight chapters where Chapter 3 to Chapter 7 constitutes the main body of the thesis.

Chapter 1 titled **"Introduction"** presents introduction to current mode approach and current mode signal processing including review of various current mode building blocks. An extensive literature survey is also presented with the scope of work.

Chapter 2 titled **"OFCC current mode building block"** presents description of OFCC and its behavior in presence of nonidealities. Schematic used for verification of proposals through simulations and experimentation are discussed next. The study of basic applications of OFCC such as amplifier configurations are detailed in this thesis and used extensively in this work. The MOS based resistor implementation is also studied and utilized to show electronic tuning in proposed circuits.

Chapter 3 titled **"OFCC based TA mode first order filter"** presents a new first order TA mode filter is put forward in this chapter. Literature survey for TA mode first order filters followed by proposed filter description including filter structure and its routine analysis using nonidealities is presented. One filter application as an oscillator is also developed.

Chapter 4 titled **"OFCC based CM second order filter"** deals with literature review followed by CM SIMO filter description. Proposed CM SIMO filter is also analyzed for nonidealities namely finite transimpedance gain, tracking errors and parasites offered by the OFCC. As an application a CM shadow bandpass filter is developed and both proposals verified through simulations while CM SIMO filter is prototyped for bandpass response.

Chapter 5 titled **"OFCC based Instrumentation Amplifier"** presents generalized structure of IA. This generalized structure is categorized into two structures: Structure-I and Structure-II. Using these structures generalized IA topologies 1-8 are proposed which can operate in VM, CM, TIM and TAM modes. To reduce the number of passive components the structures I and II are modified. Six more IA topologies are derived from modified structures. The effect of non-idealities of OFCC has been analyzed. A thorough comparison of all proposed topologies with existing one is also put forward in a tabulated format for better comparison.

Chapter 6 titled **"OFCC based transimpedance mode PGA"** presents new OFCC based PGA. It operates in TIM i.e. it receives current signal as input and provides voltage as output. It uses four blocks – a current amplifier, digitally controlled transimpedance amplifier, digitally controlled R-2R ladder network and a voltage buffer. Digital coarse and fine gain tuning is the key feature of proposed PGA which is achieved by control bits (B_5-B_0).

Chapter 7 titled **"OFCC based CM rectifier"** presents single OFCC based CM half wave rectifiers (HWRs) and full wave rectifier (FWR). These rectifiers do not use diode and are thus suitable for low voltage rectification. It is pertinent to mention here that all proposed rectifiers use single active block and are resistor-less.

Chapter 8 titled **"Conclusion and Future scope"** presents concluding remarks and future scope of the discussed work.

CHAPTER - 2

OFCC CURRENT MODE BUILDING BLOCK

2.1 INTRODUCTION

The development of current mode circuits has received growing interest over voltage mode circuits due to high frequency limitations of voltage mode circuits just because of constant gain bandwidth product and low slew rate of op-amps. Therefore, current mode approach results in significant improvement in signal linearity, bandwidth and power consumption. It's also in consonance with the trend of operating circuits at lower supply voltages where the current mode concept is more useful. In current mode circuits the operation of the circuit is decided by current which enables the system design having wider dynamic range [1-3]. These circuits are also simple and compact as current addition/subtraction does not require additional circuit blocks. Owing to the advantages of current mode blocks considerable research has directed towards development of active blocks and the realization of current mode signal processing and generation circuits. Current conveyor (CC) [3,4] is one among these CM blocks and CCI [4], CCII [5], CCIII [6] are the basic variants, which is widely explored throughout the literature. The operational floating current conveyor (OFCC) [7,8,10] is yet another variant of CC which combines the features of current conveyor and the current feedback opamp along with additional current outputs that adds flexibility in the circuit design.

This chapter describes OFCC and its behavior in presence of nonidealities. The schematic used for simulation and experimentation verification are discussed next. The VM, CM, TAM and TIM amplifier configurations and difference amplifier are used extensively in this work and are detailed. The MOS based resistor implementation [169] is also presented towards end of this chapter which is utilized to introduce electronic tuning feature in proposed circuits.

2.2 OPERATIONAL FLOATING CURRENT CONVEYOR

The circuit symbol of OFCC [7,8,10] is shown in Fig. 2.1. The port labeled as X is low impedance current input and Y is a high impedance voltage input port. The voltage at port W is multiplication of input current at port X and open loop transimpedance gain Z_t. Ports Z+ and Z- are high impedance current output ports.

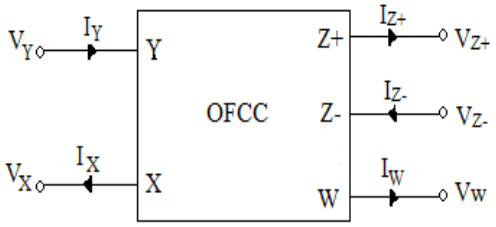


Fig. 2.1 OFCC Circuit symbol

The port X tracks the voltage of Y port and current at port W is copied to ports Z+ and Z- in phase and out of phase respectively. The port relationships of the OFCC are described by matrix given in (2.1).

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{2.1}$$

2.3 EFFECT OF NONIDEALITIES

The behavior of the proposed topologies may deviate from the ideal one due to nonidealities of OFCC which are classified in two categories. The first type of nonidealities is due to the finite transimpedance gain while the second type is due to non-ideal voltage and current transfers. The later type is manifested in terms of voltage and current tracking errors. The following sub sections describe the effect of these two nonidealities.

2.3.1 Effect of finite transimpedance gain

Ideally the transimpedance gain Z_t is assumed to approach infinity. However, in practice Z_t is a frequency dependent finite value. Therefore, using single pole model the transimpedance gain ($Z_t(s)$) can be obtained as

$$Z_t(s) = \frac{Z_{to}}{1+{}^{s}/_{\omega_{tc}}} \tag{2.2}$$

Here Z_{to} is the dc open loop transimpedance gain and ω_{tc} is the transimpedance cut off frequency. For high frequency applications, the transimpedance gain ($Z_t(s)$) is approximated as

$$Z_t(s) \cong \frac{1}{{}^{s}/_{(Z_{to}\omega_{tc})}} = \frac{1}{sC_p} \tag{2.3}$$

where

$$C_p = \frac{1}{Z_{to}\omega_{tc}} \tag{2.4}$$

represents the parasitic capacitance of OFCC.

2.3.2 Effect of voltage and current tracking errors

The port relationship of OFCC in practice, differ from (2.1) due to voltage and current tracking errors and is represented as

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ \beta & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & \alpha & 0 & 0 \\ 0 & 0 & -\gamma & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{2.5}$$

where $\beta = (1-\varepsilon_V)$, $\alpha = (1-\varepsilon_{i+})$ and $\gamma = (1-\varepsilon_{i-})$ are errors in voltage transfer from Y to X port and error in current transfer from W port to Z+ and Z- ports respectively. Here ε_V represents voltage tracking error, whereas ε_{i+} and ε_{i-} are current tracking errors. The effect of tracking errors

is strongly topology dependent, e.g. the voltage tracking error does not affect the response if Y port of OFCC is grounded and the same is true for current tracking errors if Z+ or Z- ports are not used.

2.4 OFCC REALIZATION

The OFCC implementations are based on

- CMOS schematic [13]
- CFOA [170].

2.4.1 CMOS based implementation

The CMOS based implementation of OFCC are given in [13]. This subsection describes the CMOS implementation used to validate different proposals in the work. Simulations are carried out using implementation scheme [13] of Fig. 2.2. It uses a plus type second generation current conveyor (CCII+), a transimpedance amplifier block (Z_t) and a current follower. The CMOS schematic of OFCC [13] based on this implementation scheme is depicted in Fig. 2.3. It uses matched transistor pairs (M1 and M2), (M3 and M4), (M10 and M15) and (M11, M12 and M14). Considering the saturation region operation of all the transistors, the functioning of the circuit may be elucidated as follows. Port X follows voltage of W port through transistors (M1 - M7) which form CCII+. The cross coupled current mirror formed by transistors (M16 - M21) provide negative current transfer from W port to Z- port. Voltage at port W is produced by multiplication of current input at X port with transimpedance gain (Z_t) provided by amplifier formed by transistors M8 - M13. The set of transistors (M10, M12, M14 and M15) forms current follower and provides current tracking between ports W and Z+.

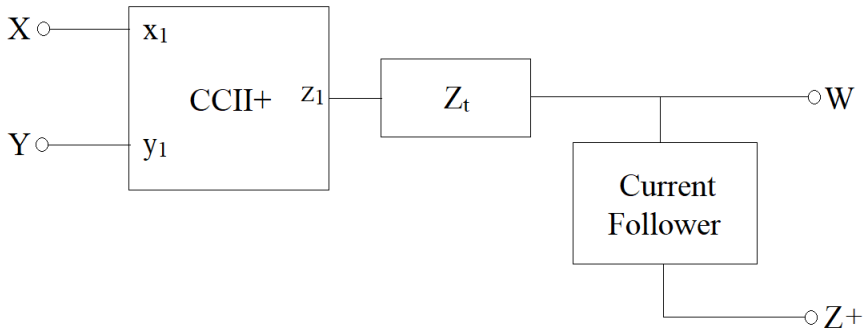


Fig. 2.2 Implementation scheme for OFCC block [13]

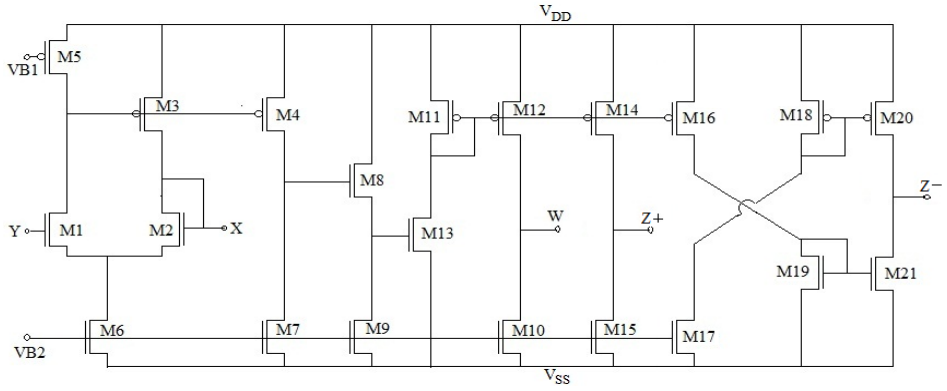


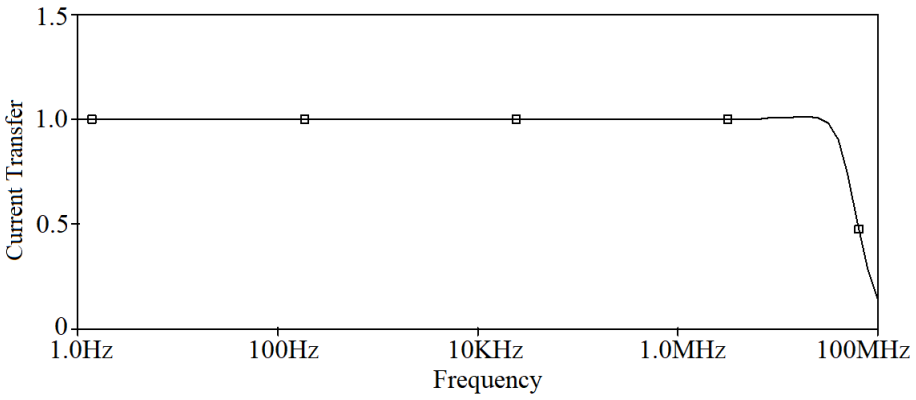
Fig. 2.3 CMOS schematic of OFCC block [13]

To verify the operation of the circuit of Fig. 2.3, SPICE simulations are carried out using MOSIS (AGILENT) 0.5 µm CMOS process technology parameters. The aspect ratios of various transistors are listed in Table 2.1. The power supplies V_{DD} and V_{SS} are taken as 1.5 V and -1.5 V, while bias voltage V_{B1} and V_{B2} of ± 0.8 V are considered.

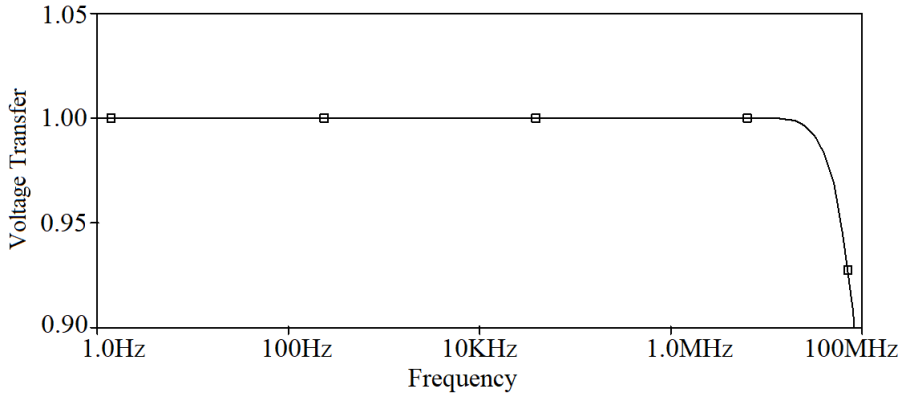
Table 2.1 Transistor's aspect ratios [13]

Transistor	$W(\mu m)/L(\mu m)$
$M1, M2$	50 / 1
$M3, M4, M11, M12, M14,$ $M16, M18, M20$	50 / 2.5
$M5, M7, M10, M15, M17,$ $M19, M21$	20 / 2.5
$M6, M8$	40 / 2.5
$M9, M13$	100 / 2.5

Simulated frequency response for current and voltage transfer characteristics of OFCC is shown in Fig. 2.4 (a) and (b) respectively. These current transfer characteristic is showing current transfer property of OFCC existing in between port Z and W. It is found that current transfer value is 0.998 and is less than unity due to current tracking error (ε_i). Similarly, the voltage transfer characteristic shows voltage transfer property of OFCC existing in between port Y and X. The voltage transfer value is 0.999 and any deviation is represented by voltage tracking error (ε_v).



(a)



(b)

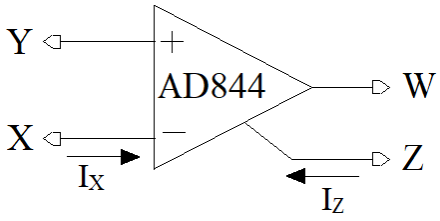
Fig. 2.4 Frequency response of (a) current transfer (b) voltage transfer characteristics of OFCC

2.4.2 CFOA based implementation

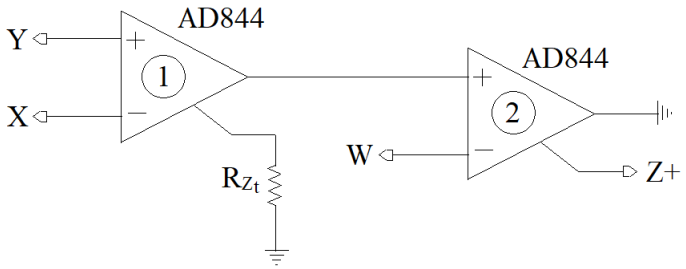
The circuit symbol of AD844 is given in Fig. 2.5 (a). Its port relationship is expressed as

$$I_Y = 0,\ I_Z = I_X,\ V_X = V_Y,\ V_W = V_Z \tag{2.6}$$

The AD844 based implementation of OFCC is given in Fig. 2.5 (b). The experimental verification of various proposals in this work is done using this implementation based on commercially available CFOA AD844 IC. It uses two AD844 ICs. The first IC provides voltage transfer between Y and X ports. The second IC is used for current transfer from W to Z+ port.



(a)



(b)

Fig. 2.5 (a) Circuit symbol of AD844 [170] (b) AD844 based OFCC implementation

2.5 BASIC APPLICATIONS OF OFCC

The OFCC based voltage amplifier, current amplifier, transadmittance amplifier, transimpedance amplifier and voltage difference amplifier are extensively used in this work. These are briefly described in the following subsections.

2.5.1 Voltage Amplifier

The voltage amplifier configuration using OFCC [13] is shown in Fig. 2.6. Assuming transimpedance approaches infinity, the gain of the amplifier (A_V) is computed as

$$A_V = \frac{V_o}{V_{in}} = 1 + \frac{R_2}{R_1} \tag{2.7}$$

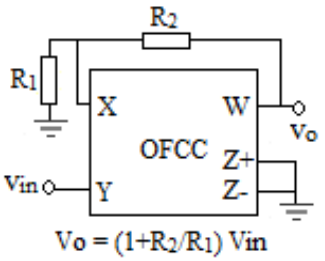


Fig. 2.6 Voltage amplifier using OFCC

Considering the nonidealities described in section 2.3, the gain (A_{v_fz}) in presence of finite Z_t, is recalculated as

$$A_{V\_fz} = \left.\frac{V_o}{V_{in}}\right|_{fz} = \left(1 + \frac{R_2}{R_1}\right)\varepsilon_V(s) \tag{2.8}$$

where, $\varepsilon_v(s)$ is the error function and is given by

$$\varepsilon_V(s) = \frac{1}{1+sC_pR_2} \tag{2.9}$$

Hence, for high frequency application, compensation method is needed to take the error function into account.

Similarly, if tracking errors are taken into consideration then (2.7) modifies to

$$A_{V\_tr} = \left.\frac{V_o}{V_{in}}\right|_{tr} = \beta\left(1 + \frac{R_2}{R_1}\right) \tag{2.10}$$

where A_{v_tr} is voltage gain in presence of tracking errors.

The operation of OFCC based voltage amplifier is examined through simulation using schematic of Fig. 2.3. Fig. 2.7 depicts simulated frequency response of voltage amplifier with

component values R_1 = 1 kΩ and R_2 = 1 kΩ, 5 kΩ, 10 kΩ and 20 kΩ. Simulated gain values are found as 6 dB, 15dB, 20 dB and 26 dB for these settings. Corresponding theoretical gain values are computed as 6.02 dB, 15.56 dB, 20.82 dB and 26.44 dB which verify the functionality of voltage amplifier.

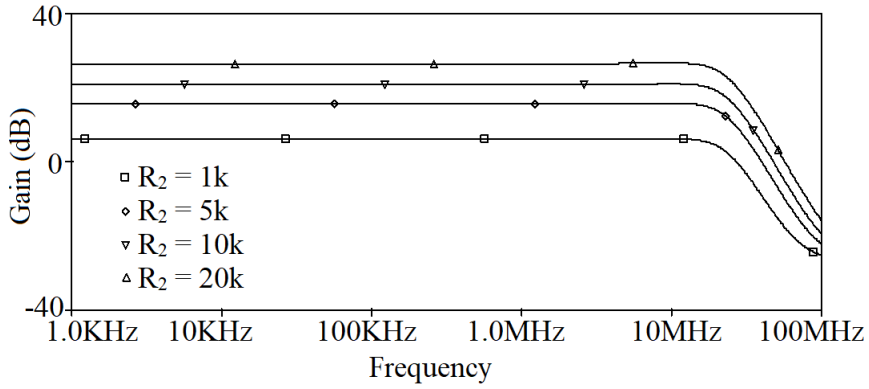


Fig. 2.7 Frequency response of voltage amplifier

2.5.2 Current Amplifier

The current amplifier configuration using OFCC [13] is shown in Fig. 2.8 and using routine analysis, the gain of the amplifier (A_I) can be obtained as

$$A_I = \frac{I_o}{I_{in}} = -\left(1 + \frac{R_2}{R_1}\right) \tag{2.11}$$

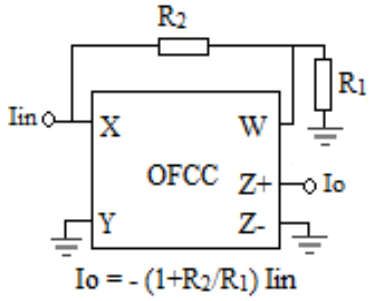


Fig. 2.8 Current amplifier using OFCC

Considering the nonidealities described in section 2.3, the gain (A_{I_fz}) in presence of Z_t, is recalculated as

$$A_{I\_fz} = \left.\frac{I_o}{I_{in}}\right|_{fz} = -\left(1 + \frac{R_2}{R_1}\right)\varepsilon_I(s) \tag{2.12}$$

where, $\varepsilon_I(s)$ is the error function and is given by

$$\varepsilon_I(s) = \frac{1}{1+sC_pR_2} \tag{2.13}$$

Hence, for high frequency application, compensation method is needed to take the error function into account.

Similarly, if tracking errors are taken into consideration then (2.11) modifies to

$$A_{I\_tr} = \left.\frac{I_o}{I_{in}}\right|_{tr} = -\alpha\left(1 + \frac{R_2}{R_1}\right) \tag{2.14}$$

where A_{I_tr} corresponds to current gain in presence of tracking error.

The operation of OFCC based current amplifier is examined through simulation using schematic of Fig. 2.3. Fig. 2.9 depicts simulated frequency response of current amplifier with component values R_1 = 1 kΩ and R_2 = 1 kΩ, 5 kΩ, 10 kΩ and 20 kΩ. Simulated gain values are found as 6 dB, 15dB, 20 dB and 26 dB while theoretical gain values are as 6.02 dB, 15.56 dB, 20.82 dB and 26.44 dB for these settings which verify the functionality of current amplifier.

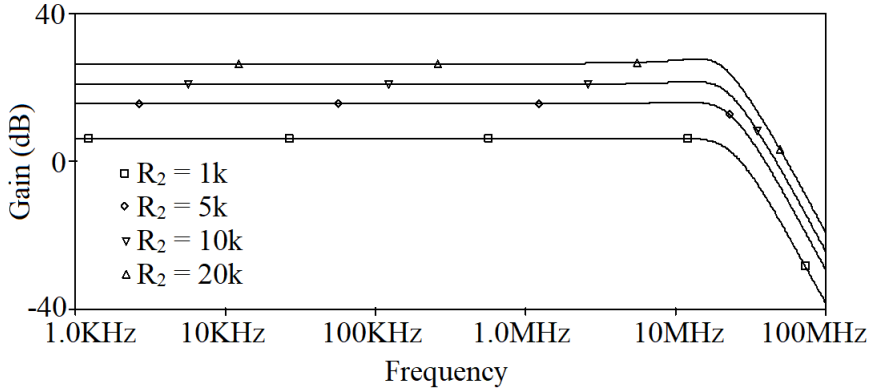


Fig. 2.9 Frequency response of current amplifier

2.5.3 Transadmittance Amplifier

The transadmittance amplifier configuration using OFCC [13] is shown in Fig. 2.10 and using routine analysis, gain of the amplifier (A_{TA}) can be obtained as

$$A_{TA} = \frac{I_o}{V_{in}} = \left(\frac{1}{R_1}\right) \tag{2.15}$$

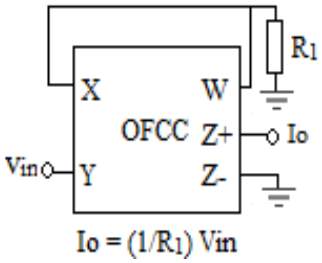


Fig. 2.10 Transadmittance amplifier

Considering the nonidealities described in section 2.3, the gain in presence of Z_t (A_{TA_fz}) is recalculated as

$$A_{TA\_fz} = \left.\frac{I_o}{V_{in}}\right|_{fz} = \left(\frac{1}{R_1}\right)\varepsilon_{TA}(s) \tag{2.16}$$

where, $\varepsilon_{TA}(s)$ is the error function and is given by

$$\varepsilon_{TA}(s) = \frac{1}{1+sC_pR_1} \tag{2.17}$$

Hence, for high frequency application, compensation method is needed to take the error function into account.

Similarly, if tracking errors are taken into consideration then (2.15) modifies to

$$A_{TA\_tr} = \left.\frac{I_o}{V_{in}}\right|_{tr} = \alpha\beta\left(\frac{1}{R_1}\right) \tag{2.18}$$

where (A_{TA_tr}) is transadmittance gain in presence of tracking errors.

The operation of OFCC based transadmittance amplifier is examined through simulation using schematic of Fig. 2.3. Fig. 2.11 depicts simulated frequency response of transadmittance

amplifier with component values R_1 = 0.2 kΩ, 1 kΩ, 10 kΩ, 50 kΩ and 100 kΩ. Simulated gain values are found as 4.99 m-mho, 0.99 m-mho, 100.01 µ-mho, 20.02 µ-mho and 10.02 µ-mho for these settings. Corresponding theoretical gain values are computed as 5 m-mho, 1 m-mho, 100 µ-mho, 20 µ-mho and 10 µ-mho which verify the functionality of transadmittance amplifier.

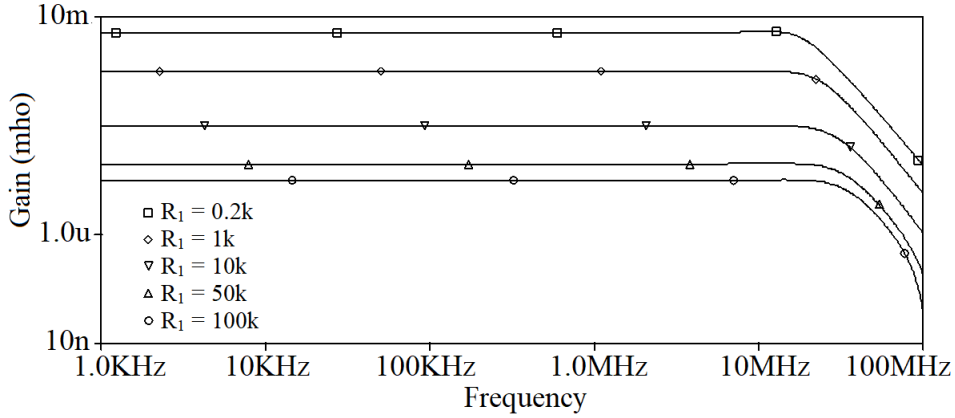


Fig. 2.11 Frequency response of transadmittance amplifier

2.5.4 Transimpedance Amplifier

The transimpedance amplifier configuration using OFCC [13] is shown in Fig. 2.12 and using routine analysis, gain of the amplifier (A_{TI}) can be obtained as

$$A_{TI} = \frac{V_o}{I_{in}} = -(R_1) \tag{2.19}$$

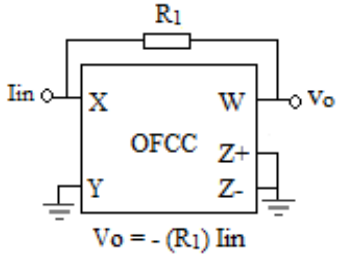


Fig. 2.12 Transimpedance amplifier

Considering the nonidealities described in section 2.3, the gain in presence of Z_t (A_{TI_fz}) is recalculated as

$$A_{TI\_fz} = \frac{V_o}{I_{in}}\Big|_{fz} = -(R_1)\varepsilon_{TI}(s) \tag{2.20}$$

where, $\varepsilon_{TI}(s)$ is the error function and is given by

$$\varepsilon_{TI}(s) = \frac{1}{1+sC_pR_1} \tag{2.21}$$

Hence, for high frequency application, compensation method is needed to take the error function into account.

Similarly, if tracking errors are taken into consideration then gain of transimpedance amplifier remains unchanged and is given as (2.19).

The operation of OFCC based transimpedance amplifier is examined through simulation using schematic of Fig. 2.3. Fig. 2.13 depicts simulated frequency response of transimpedance amplifier with component values R_1 = 1 kΩ, 5 kΩ, 10 kΩ and 20 kΩ. Simulated gain values are found as 1 kΩ, 5 kΩ, 10 kΩ and 20 kΩ for these settings. Corresponding theoretical gain values are computed as 1 kΩ, 5 kΩ, 10 kΩ and 20 kΩ which verify the functionality of transimpedance amplifier.

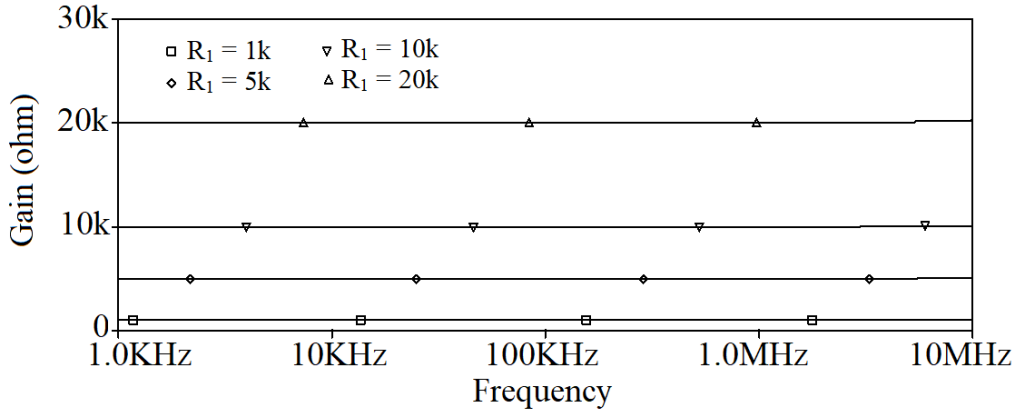


Fig. 2.13 Frequency response of transimpedance amplifier

2.5.5 Voltage difference Amplifier

The voltage differencing principle used in opamp [121] is applied to arrive at OFCC based voltage difference circuit of Fig. 2.14. The voltage difference amplifier configuration using OFCC is shown in Fig. 2.14 and using routine analysis, the currents I_1, I_2 and I_3 in Fig. 2.14 may be written as

$$I_1 = \frac{V_2 - V_X}{R_1},\ I_2 = \frac{V_1 - V_Y}{R_3} \text{ and } I_3 = \frac{V_X - V_o}{R_2} \tag{2.22}$$

where V_X and V_Y are voltages at X and Y ports of OFCC.

As $V_X = V_Y$, then voltage at terminal (V_Y) is computed as

$$V_Y = V_1 \left(\frac{R_4}{R_3 + R_4}\right) \tag{2.23}$$

Now, if $V_1 = 0$ then

$$V_o(V_1 = 0) = -V_2 \left(\frac{R_2}{R_1}\right) \tag{2.24}$$

If $V_2 = 0$, then

$$V_o(V_2 = 0) = V_1 \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) \tag{2.25}$$

and output will be $V_o = V_o\ (V_1 = 0) + V_o\ (V_2 = 0)$ therefore V_o may be obtained as

$$V_o = -V_2 \left(\frac{R_2}{R_1}\right) + V_1 \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) \tag{2.26}$$

If equal resistor values i.e. $R_1 = R_2 = R_3 = R_4$ are taken, then the amplifier will become unity gain voltage difference amplifier and the output expression can be obtained as $V_o = (V_1 - V_2)$. However, if $R_1 = R_3 = R_A$ and $R_2 = R_4 = R_B$ then output voltage is computed as

$$V_o = \left(\frac{R_B}{R_A}\right)(V_1 - V_2) \tag{2.27}$$

and gain of the amplifier (A_{VDA}) can be obtained as

$$A_{VDA} = \frac{V_o}{(V_1 - V_2)} = \left(\frac{R_B}{R_A}\right) \tag{2.28}$$

Thus circuit performs operation of difference amplifier with gain.

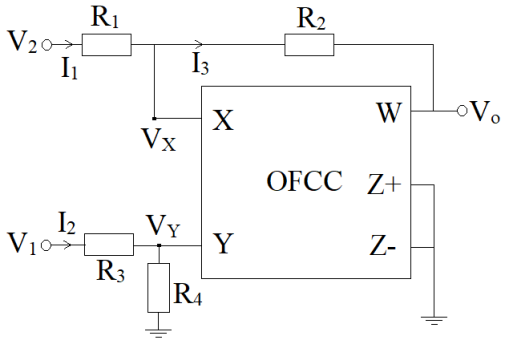


Fig. 2.14 Voltage Difference Amplifier

Considering the nonidealities described in section 2.3, the gain in presence of Z_t, is recalculated as

$$A_{VDA\_fz} = \frac{V_o}{(V_1 - V_2)}\Big|_{fz} = \left(\frac{R_B}{R_A}\right) \varepsilon_{VDA}(s) \tag{2.29}$$

where, $\varepsilon_{VDA}(s)$ is the error function and it is given by

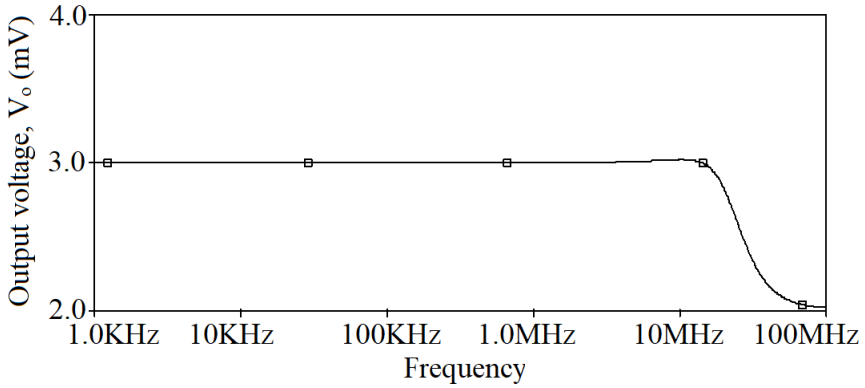
$$\varepsilon_{VDA}(s) = \frac{1}{1 + sC_p R_B} \tag{2.30}$$

Hence, for high frequency application, compensation method is needed for taking the error function into account.

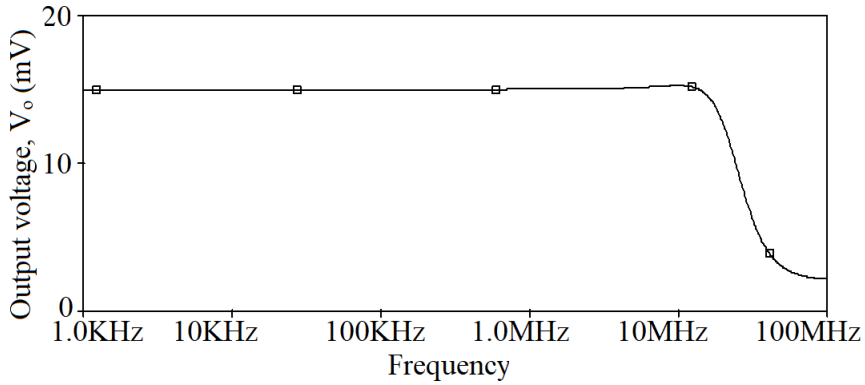
Similarly, if tracking errors are taken into consideration then (2.27) modifies to

$$V_{o\_tr} = \left(\frac{R_B}{R_A}\right)(\beta V_1 - V_2) \tag{2.31}$$

The operation of OFCC based voltage difference amplifier is examined through simulation using schematic of Fig. 2.3. Simulated frequency responses of voltage difference amplifier for input voltage V_1 = 5 mV, V_2 = 2 mV with component values $R_1 = R_2 = R_3 = R_4 = R_A = R_B$ = 1 kΩ to set the unity gain value while $R_1 = R_3 = R_A$ = 1 kΩ and $R_2 = R_4 = R_B$ = 5 kΩ to set the gain value of 5, are depicted in Fig. 2.15 (a) and (b) respectively.



(a)



(b)

Fig. 2.15 Frequency response of voltage difference amplifier with (a) gain=1 (b) gain=5

Simulated values are found as 3 mV and 15 mV respectively for both of these settings. Corresponding theoretical values are computed as 3 mV and 15 mV, which verify the functionality

of voltage difference amplifier. Similarly, by varying R_A and R_B to another values the gain can be varied accordingly and amplified voltage difference output is achieved.

2.6 MOS BASED RESISTOR IMPLEMENTATION

This section briefly describes grounded resistor implementation based on two diode connected MOS transistors as shown in Fig. 2.16 [169].

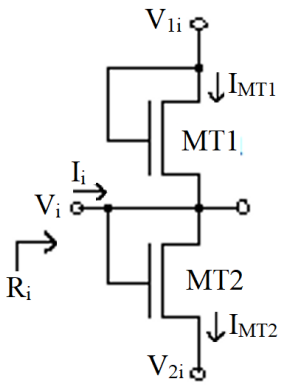


Fig. 2.16 MOS based resistor implementation [169]

Assuming MOS transistor structure operating in saturation region and equal aspect ratios of MT1 and MT2, the KCL at input node may be written as

$$I_i = I_{MT2} - I_{MT1} \tag{2.32}$$

$$I_i = \frac{1}{2}\mu_n C_{ox}\left(W/L\right)(V_i - V_{2i} - V_T)^2 - \frac{1}{2}\mu_n C_{ox}\left(W/L\right)(V_{1i} - V_i - V_T)^2 \tag{2.33}$$

where μ_n, C_{ox} and V_T represent mobility, oxide capacitance and threshold voltage respectively.

Taking $V_{1i} = - V_{2i}$, input resistance (R_i) may be computed by simplifying (2.33) as

$$R_i = \frac{V_i}{I_i} = \frac{1}{2\mu_n C_{ox}\left(W/L\right)(V_{1i} - V_T)} \tag{2.34}$$

So by varying V_{1i} the resistance may be electronically tuned. Simulated values of MOS based resistance are shown in Table 2.2.

Table 2.2 Simulated values of MOS based resistance [169]

Resistance bias voltages		**Resistance value**
V_{1i} (V)	**V_{2i} (V)**	**R_i (kΩ)**
1.310	-1.310	1
0.869	-0.869	2
0.726	-0.726	5
0.711	-0.711	10

2.7 CONCLUDING REMARKS

In this chapter, the description of OFCC as a CM block, its circuit symbol, port matrix and port relationships are given. OFCC implementation using CMOS based schematic and commercially available IC AD844, is provided in next section. It is used for simulation and experimental purpose respectively throughout the complete study. The current and voltage transfer characteristics of OFCC is also verified to check the functionality of the block. The basic amplifier configurations such as voltage, current, transadmittance, transimpedance and voltage difference amplifier followed by their respective responses and derivations are given. These responses confirm the behavior of OFCC as an amplifier. Nonidealities of OFCC is also analyzed and discussed. The MOS based resistor implementation is also studied and utilized wherever required in proposed circuits to provide electronic tunability.

CHAPTER - 3

OFCC BASED TA MODE FIRST ORDER FILTER

This chapter includes various details, analysis and simulated results of following published paper:

1. Deva Nand, Neeta Pandey, **"Transadmittance Mode First Order LP/HP/AP Filter and its Application as an Oscillator"** *IOP Conf. Ser.: Mater. Sci. Eng.* Vol. 225 (012150), 2017. DOI: 10.1088/1757-899X/225/1/012150 **(Scopus indexed)**

3.1 INTRODUCTION

There is widespread use of filters in instrumentation and communication systems. The filter comprises of interconnection of passive components (inductors, capacitors and resistors) and active devices such as controlled sources, amplifiers, transistor etc. [34]. Low pass, high pass, bandpass and band reject/notch are typical filter categories when magnitude is of prime concern while all pass filter or delay equalizers is important when phase or delay specifications are to be met while keeping magnitude constant. Low pass filter passes frequencies (passband) from dc to cut off frequencies while higher frequencies are attenuated. High pass filter attenuates frequencies below cut off frequencies while passing all frequencies above it. Band pass (reject) filter passes (attenuates) passband of frequencies while attenuating (passing) remaining frequencies. In general, the transfer function of first order transfer filter is given by

$$T(s) = \frac{a_1 s + a_o}{s + \omega_o} \tag{3.1}$$

The coefficient selection $a_1 = 0$ and $a_0 = 1$ the numerator of (3.1) give high pass and low pass responses. A first order transfer function may be obtained from (3.1) by making numerator equal to $-\omega_0$ and both a_i's ($i = 0, 1$).

Transadmittance mode filters are class of filters that process voltage input and provide current output. These filters are useful where the system processing filter output is either CM or TIM. A VM or TIM filter in such cases require voltage to current converter. A new first order TA mode filter is put forward in this chapter. The behaviour of proposed filter is examined in presence of nonidealities. To illustrate its usefulness an oscillator structure is also presented.

3.2 LITERATURE REVIEW

Numerous first order filters have been reported in [35-50]. The filters available in [35-40, 47-49] process voltage input while those reported in [39, 41-43, 49, 50] work on current signal. Output of [35-40, 47-49] is voltage signal and [39, 41-43, 49, 50] provide current signal. Therefore, the topologies [35-40, 47-49], [39, 41-43, 49, 50] and [44-49] are classified as first order VM, first order CM and first order TAM filters respectively. First order VM [38, 39] and CM [39] filters provide low pass, high pass and all pass responses respectively. First order TAM filters [44-49] provide all pass response only. Table 3.1 encapsulates the features of available first order TAM filters. It may be observed from Table 3.1 that

- the topologies [44,45,49] use variety of current conveyors namely CCCIII [44, 45] and ZC-VDCC [49]; while those reported in [46-48] use DBTA [47, 48] and MCBTA [46].
- input impedance is low in [44-46] therefore additional active block is needed for interfacing.
- output impedance is low in [47] so additional active block is required for processing.
- the count of passive component is five in [48], highest among the available ones.

Keeping in view the above facts, a new proposal for OFCC based TA mode first order filter is presented next.

Table 3.1 Available TA mode first order filters.

Ref.	Active block count	Passive component count, R/C	Input impedance	Output impedance	No. of simultaneous responses
[44]	1 CCIII	4/1	Low	High	AP
[45]	1 CCIII	3/1	Low	High	AP
[46]	1 MCBTA	1/1	Low	High	AP
[47]	1 DBTA	2/1	High	Low	AP
[48]	1 DBTA	1/1	High	High	AP
[49]	1 ZC-VDCC	0/1	High	High	AP
Proposed	2 OFCC	2/1	High	High	LP, HP or AP, HP

3.3 PROPOSED FIRST ORDER TAM FILTER

The proposed filter structure is presented in the following subsection followed by its behavioral analysis under non ideal conditions. The proposed filter is also used to design a sinusoidal oscillator.

3.3.1 Filter structure

The proposed TA mode first order filter is depicted in Fig. 3.1. It uses two OFCCs, two resistors (one floating and one grounded) and one grounded capacitor.

By applying nodal analysis following filter transfer functions are derived

$$\frac{I_o}{V_{in}} = \frac{1}{R_2}\frac{sC_1(R_2-R_1)-1}{(sC_1R_1+1)} \tag{3.2}$$

$$\frac{I_{HP}}{V_{in}} = -\frac{sC_1}{(sC_1R_1+1)} = T_{HP}\ (say) \tag{3.3}$$

With $R_2 = R_1$ and $R_2 = 2R_1$ the transfer function (3.2) modifies to (3.4) and (3.5) respectively.

$$\frac{I_o}{V_{in}} = -\frac{1}{R_1}\frac{1}{(sC_1R_1+1)} = T_{LP}\ (say) \tag{3.4}$$

$$\frac{I_o}{V_{in}} = \frac{1}{2R_1}\frac{(sC_1R_1-1)}{(sC_1R_1+1)} = T_{AP}\ (say) \tag{3.5}$$

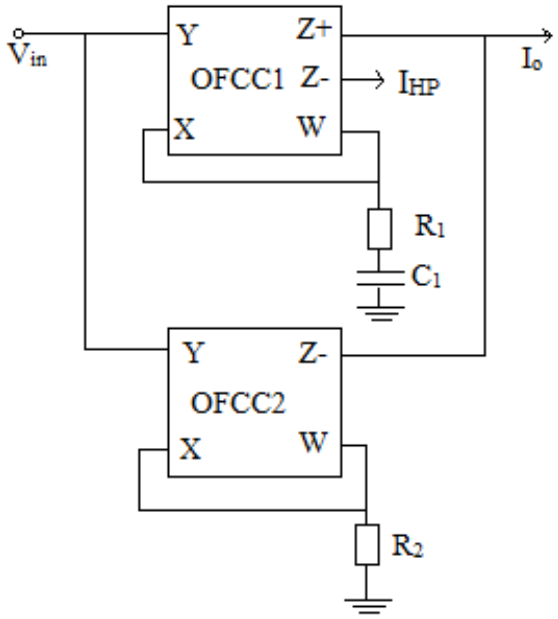


Fig. 3.1 TA mode first order filter circuit

Thus the proposed TA mode filter provides two responses namely high pass and low pass/all pass simultaneously in contrast to availability of single response at a time in available first order TA mode filters [44-49].

The pole frequency for transfer functions T_{HP}, T_{LP} and T_{AP} is given as

$$\omega_o = \frac{1}{C_1R_1} \tag{3.6}$$

and the phase response for T_{AP} is computed as

$$\varphi = 180° - 2tan^{-1}(\omega C_1R_1) \tag{3.7}$$

The sensitivity of the pole frequency with respect to R_1 and C_1 is computed as

$$S_{R_1}^{\omega_o} = S_{C_1}^{\omega_o} = 1 \tag{3.8}$$

3.3.2 Non Ideal Analysis

The behavior of the proposed filter may deviate from the ideal one due to the finite transimpedance gain and due to the presence of voltage and current tracking errors. The following sub sections examines the effect of these two non-idealities on filter performance.

3.3.2.1 Finite transimpedance gain

Considering finite transimpedance gain $Z_t(s)$ given in section 2.3.1 into account, output current I_o modifies to

$$I_o\big|_{fz} = I_1\,\varepsilon_1(s) - I_2\,\varepsilon_2(s) \tag{3.9}$$

where I_1 and I_2 are currents from Z+ port of OFCC1 and Z- port of OFCC2 respectively. The current $I_o\big|_{fz}$ represents I_o in presence of finite $Z_t(s)$.

Expressing I_1 and I_2 in terms of V_{in} and circuit components gives $I_o\big|_{fz}$ as

$$I_o\big|_{fz} = \frac{V_{in}}{R_1 + \dfrac{1}{sC_1}}\varepsilon_1(s) - \frac{V_{in}}{R_2}\varepsilon_2(s) \tag{3.10}$$

where

$$\varepsilon_1(s) = \frac{1}{1 + \left(R_1 + \dfrac{1}{sC_1}\right)sC_{p1}} \tag{3.11}$$

$$\varepsilon_2(s) = \frac{1}{1 + sR_2C_{p2}} \tag{3.12}$$

The output current may be expressed as.

$$\left.\frac{I_o}{V_{in}}\right|_{fz} = \frac{N_1(s) - N_2(s)}{D_1(s)D_2(s)D_3(s)R_2} \tag{3.13}$$

where

$$N_1(s) = s^2 C_1^2 R_2 \left(1 + sC_{p2} R_2\right) \tag{3.14}$$

$$N_2(s) = \left(1 + sC_1 R_1\right)\left(sC_1 + \left(1 + sC_1 R_1\right) sC_{p1}\right) \tag{3.15}$$

$$D_1(s) = \left(1 + sC_1 R_1\right) \tag{3.16}$$

$$D_2(s) = \left(sC_1 + \left(1 + sC_1 R_1\right) sC_{p1}\right) \tag{3.17}$$

$$D_3(s) = \left(1 + sC_{p2} R_2\right) \tag{3.18}$$

Considering $C_{p1} << C_1$ and operating frequencies $\omega << (1/R_1C_{p1}, 1/R_2C_{p2})$, (3.14), (3.15), (3.17) and (3.18) respectively modifies to

$$N_1(s) \approx s^2 C_1^2 R_2 \tag{3.19}$$

$$N_2(s) \approx \left(1 + sC_1 R_1\right) sC_1 \tag{3.20}$$

$$D_2(s) \approx sC_1 \tag{3.21}$$

and

$$D_3(s) = \left(1 + sC_{p2} R_2\right) \approx 1 \tag{3.22}$$

Thus, (3.13) finally simplifies to

$$\left.\frac{I_o}{V_{in}}\right|_{fz} = \frac{1}{R_2} \frac{sC_1\left(R_2 - R_1\right) - 1}{\left(sC_1 R_1 + 1\right)} \tag{3.23}$$

which is same as given in (3.2).

Similar analysis for I_{HP} is also done and it is found that with $C << C_{p1}$ and $\omega << 1/R_1C_p$, $I_{HP}\big|_{fz}$ reduces to (3.3).

3.3.2.2 Tracking error

Now considering the voltage and current tracking errors given in section 2.3.2, the output current I_o is obtained as

$$I_o\big|_{tr} = \alpha I_1 - \gamma I_2 \tag{3.24}$$

Equation (3.24) may be expressed in terms of V_{in} and circuit components as

$$I_o\big|_{tr} = \frac{\alpha\beta V_{in}}{R_1 + \frac{1}{sC_1}} - \frac{\gamma\beta V_{in}}{R_2} \tag{3.25}$$

Thus the transfer function of (3.2) modifies to

$$\left.\frac{I_o}{V_{in}}\right|_{tr} = \frac{\alpha\beta sC_1}{sC_1R_1+1} - \frac{\gamma\beta}{R_2} = \frac{1}{R_2}\frac{\alpha\beta\, sC_1R_2 - \gamma\beta\left(sC_1R_1+1\right)}{\left(sC_1R_1+1\right)} \tag{3.26}$$

in presence of tracking errors.

Solving (3.26) further results in

$$\left.\frac{I_o}{V_{in}}\right|_{tr} = \frac{1}{R_2}\frac{\beta\left(sC_1\left(\alpha R_2 - \gamma R_1\right) - \gamma\right)}{\left(sC_1R_1+1\right)} \tag{3.27}$$

Assuming $\alpha = \gamma$, (3.27) reduces to

$$\left.\frac{I_o}{V_{in}}\right|_{tr} = \frac{1}{R_2}\frac{\alpha\beta\left(sC_1\left(R_2 - R_1\right) - 1\right)}{\left(sC_1R_1+1\right)} \tag{3.28}$$

Further selecting $R_2 = R_1$ in (3.28) will provide low pass function

$$\left.\frac{I_o}{V_{in}}\right|_{tr} = \frac{1}{R_1}\frac{-\alpha\beta}{\left(sC_1R_1+1\right)} = T_{LP\_tr}\,(say) \tag{3.29}$$

Similarly selecting $R_2 = 2R_1$ in (3.28) will provide all pass function

$$\left.\frac{I_o}{V_{in}}\right|_{tr} = \frac{1}{2R_1}\frac{\alpha\beta\left(sC_1R_1-1\right)}{\left(sC_1R_1+1\right)} = T_{AP\_tr}(say) \tag{3.30}$$

Similar analysis for I_{HP} gives the following transfer function

$$\left.\frac{I_{HP}}{V_{in}}\right|_{tr} = -\frac{\gamma\beta sC_1}{\left(sC_1R_1+1\right)} = T_{HP\_tr}(say) \tag{3.31}$$

It is clear from (3.29) – (3.31) that transfer function modify in presence of tracking errors.

3.3.3 Filter application

In this subsection, the proposed filter is used to realize a sinusoidal oscillator. In general, a sinusoidal oscillator may be implemented by connecting output of a first order filter to an integrator and closing the feedback loop. As the proposed filter provides current output at high impedance port, the integration operation may simply be obtained by placing a capacitor at output of filter as shown in Fig. 3.2 (a). The transfer function so obtained is

$$\frac{V_{out}}{V_{in}} = \frac{1}{2R_1}\frac{(sC_1R_1-1)}{(sC_1R_1+1)}\frac{1}{sC_2} \tag{3.32}$$

By connecting output to input, characteristic equation of (3.33) is obtained.

$$2s^2C_1C_2R_1^2 + s(2C_2 - C_1)R_1 + 1 = 0 \tag{3.33}$$

The sinusoidal oscillator so obtained is shown in Fig. 3.2 (b).

The condition of oscillation and frequency of oscillation are derived respectively as

$$C_1 = 2C_2 \tag{3.34}$$

$$f_o = \frac{1}{4\pi R_1C_2} \tag{3.35}$$

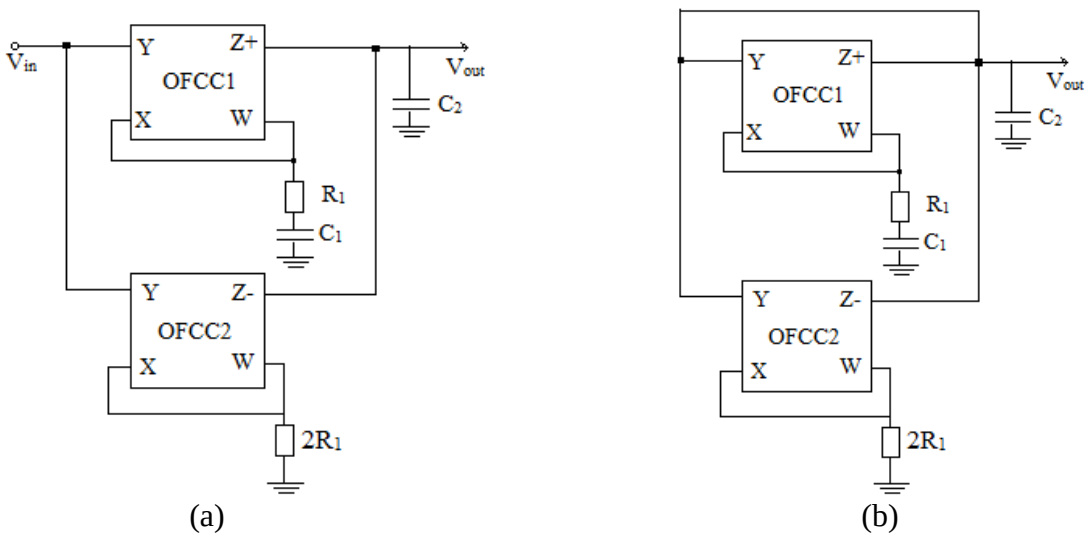
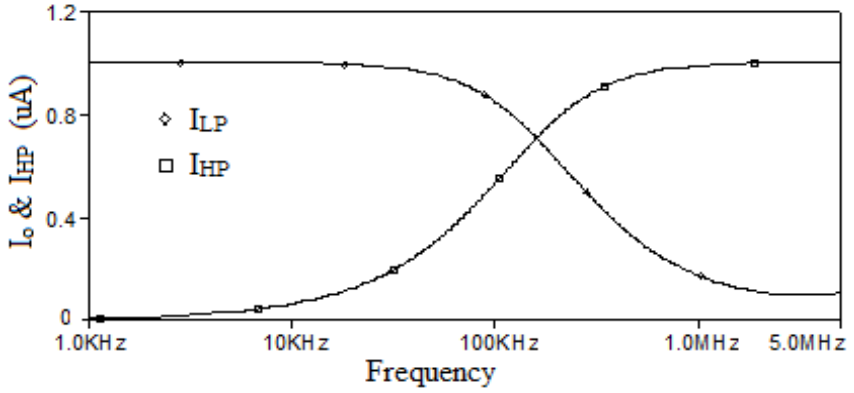


Fig. 3.2 Proposed filter (a) with integrator (b) as an oscillator

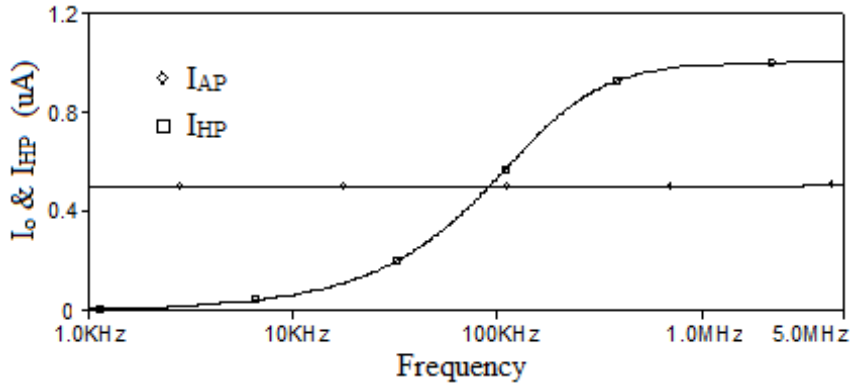
3.4 SIMULATION RESULTS

The functionality of proposed filter topology is verified through SPICE simulation using circuit schematic of OFCC as given in Fig. 2.3 [13]. The pole frequency of 159 KHz is chosen and corresponding component values are computed as, C_1 = 100pF, R_1 = 10 kΩ for all responses. The value of R_2 is taken as 10 kΩ for low pass response and 20 kΩ for all pass response. High pass response is independent of R_2 thus will be available in both conditions and will depend only on R_1 and C_1.

To show simultaneous availability of high pass and low pass responses the frequency domain simulations have been carried out and corresponding responses are shown in Fig. 3.3(a). Similar simulations for high pass and all pass responses are performed and results are shown in Fig. 3.3(b). The simulated pole frequency for both low pass and high pass responses is observed as 159.96 kHz which are in close agreement with theoretical value. Simulated phase response for all pass filter is shown in Fig. 3.4 which comply with theoretical predictions as the simulated frequency for 90° phase is observed as 159.19 KHz against theoretical value of 159 KHz.



(a)



(b)

Fig.3.3 Frequency response of first order (a) LP and HP (b) AP and HP filter

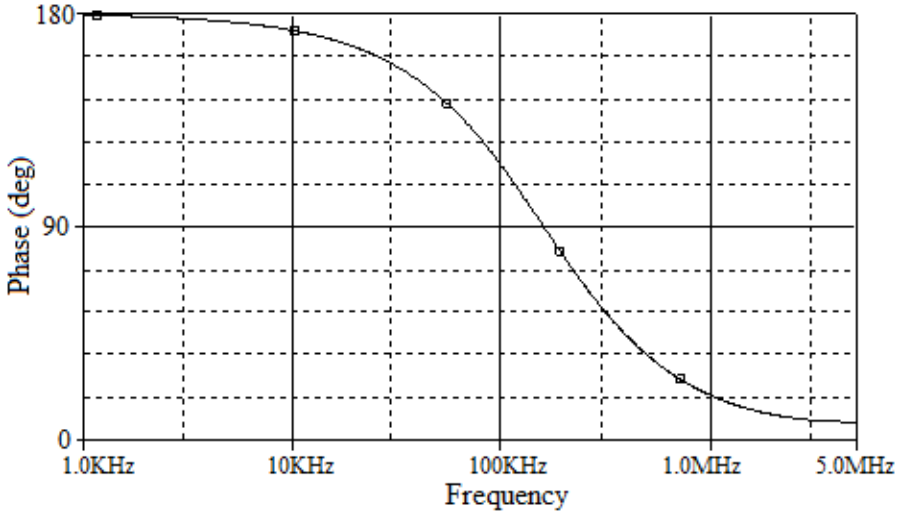
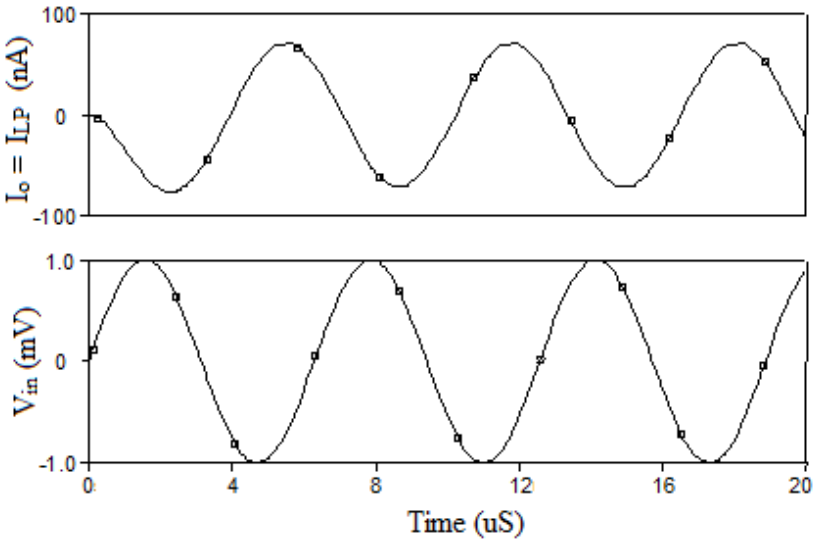
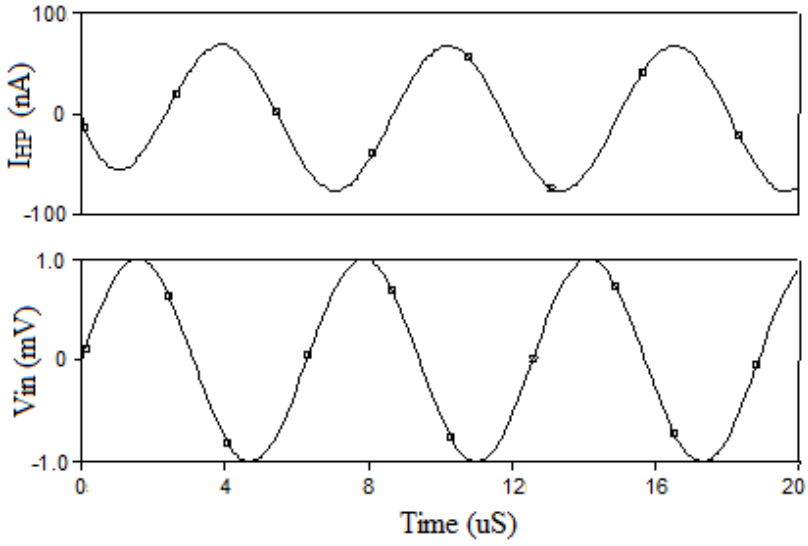


Fig. 3.4 Phase response of first order AP filter

The behavior of proposed filter is also examined in time domain by applying sinusoidal signal of amplitude 1mV, f_o = 159 kHz. The transient responses for low pass, high pass and all pass filter are plotted in Figs. 3.5 (a), 3.5 (b) and 3.6 (a). Simulated Lissagous pattern is shown in Fig. 3.6 (b) which shows 90° phase shift between input and output thus verifies the functionality.

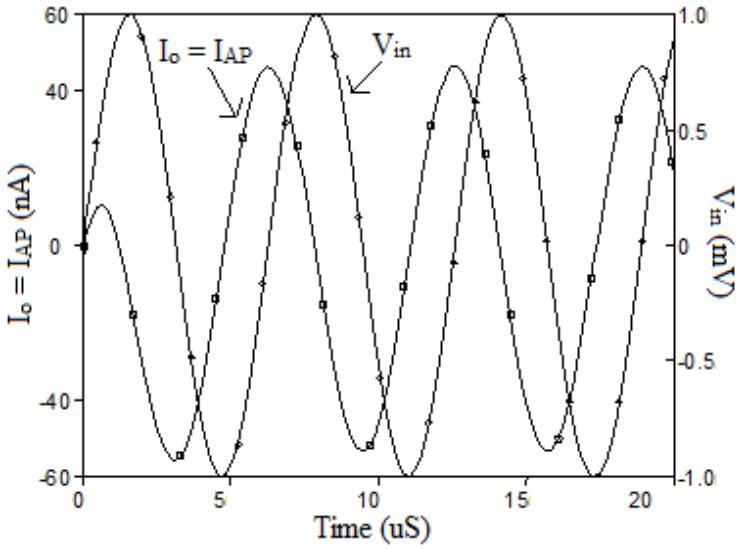


(a)

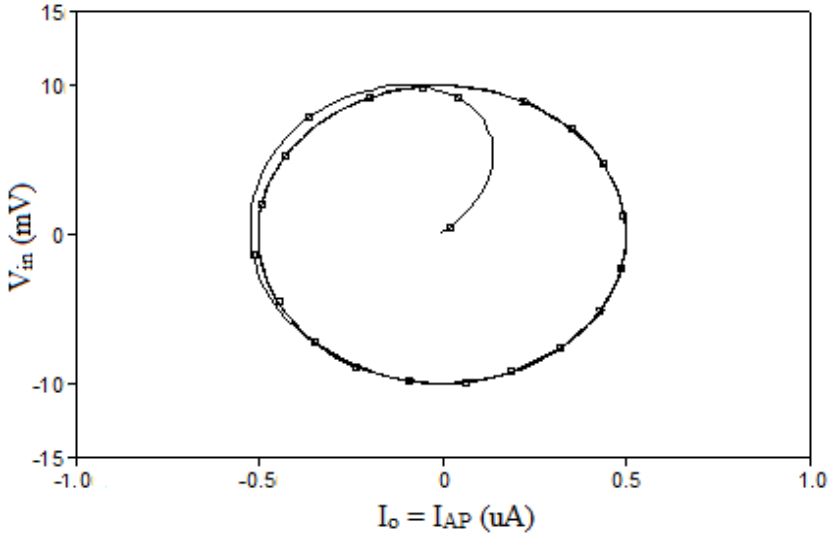


(b)

Fig.3.5 Transient responses for (a) low pass output (I_o) (b) High Pass output (I_{HP})



(a)

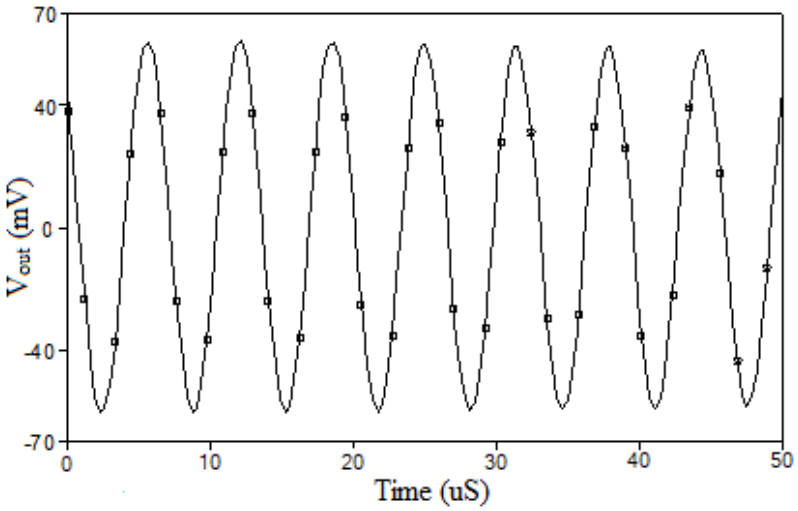


(b)

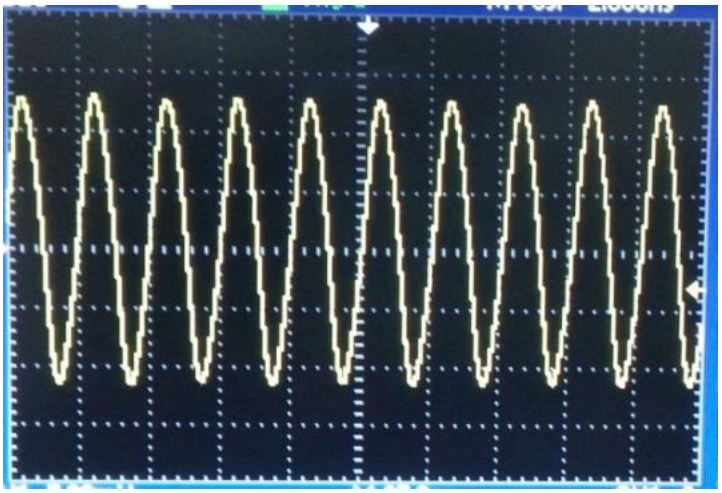
Fig. 3.6 (a) Transient response and (b) corresponding Lissagous figure for all pass filter

The operation of sinusoidal oscillator based on proposed filter is examined using simulations. Oscillator is designed for frequency of 159 KHz and corresponding component values are chosen as R_1 = 10 kΩ, $C_1 = 2C_2$ = 100 pF. The proposed oscillator circuit is also constructed using AD844 based realization of Fig. 2.5 (b) using the component values used in simulation. The

frequency obtained from simulation is 159.15 KHz while experimental values are 163.23 KHz. Simulated and experimental results are shown in Fig. 3.7.



(a)



(b)

Fig. 3.7 Sinusoidal Oscillator Output (a) simulated (b) experimental

3.5 CONCLUDING REMARKS

In this chapter new TA mode first order LP/HP/AP filter using OFCC and its application as an oscillator is proposed. This proposal offers total three filter functions LP/HP/AP in transadmittance mode at high impedance. Only two OFCCs, two resistors and one grounded capacitor are employed for realization. Workability is verified through SPICE simulations and found that simulated results conform the theoretical predictions very well. The proposed circuit is prototyped and tested experimentally for its application as an oscillator.

CHAPTER - 4

OFCC BASED CM SECOND ORDER FILTER

This chapter includes various details, analysis and simulated results of following published paper:

[1] **Deva Nand**, Neeta Pandey, **"New Configuration for OFCC based CM SIMO filter and its application as Shadow filter"** *Arabian Journal for Science and Engineering **(Springer)***, 43, pp. 3011-3022, 2018. **(SCIE)** *DOI: 10.1007/s13369-017-3058-1*

4.1 INTRODUCTION

Ideally, transmission characteristics of a filter should be such that it passes all desirable frequencies and stops remaining frequencies. As this condition is practically not achievable by any practical circuit, so filter specifications allow some transmission over the stop band. The range of frequencies is called transition band, and in a filter, smaller is the transition band, closer would be the filter response to ideal one. The roll off rate determines the width of transition band. The roll off rate of n^{th} order filter is -20n dB/decade e.g. a first order filter has roll off -20 dB/decade, a second order filter roll off rate is -40 dB/decade, and so on. To obtain a desired roll off characteristics, filters of first and second order may be cascaded.

This chapter deals with second order filter which is characterized by following transfer function.

$$T(s) = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + (\omega_o/Q)s + \omega_o^2} \tag{4.1}$$

where ω_o and Q are pole frequency and quality factor. The coefficients a_i (i = 0, 1, 2) decides the filter type. Low pass response is obtained if a_0 is unity while a_i's are zero. The coefficient (a_2, a_1, a_0) of (1, 0, 0), (0, 1, 0), (1, 0, 1), (1, -1, 1) provide high pass, band pass, band reject and all pass responses.

This chapter presents OFCC based CM second order filter. The proposal works on single input and provides multiple outputs, thus falling in SIMO filter category. The behaviour of filter is analyzed for nonidealities namely finite transimpedance gain, tracking errors and parasites. As an application a CM shadow bandpass filter is developed and both proposals verified through simulations while CM SIMO filter is prototyped for bandpass response.

4.2 LITERATURE REVIEW OF CM SIMO FILTERS

Available CM SIMO filters [29, 30, 52-79] differ in terms of number of active blocks and passive elements used; types of active blocks used; input/output impedances; simultaneous availability of output responses; and independent adjustment of the filter parameters. Table 4.1 summarizes the features of available CM SIMO filters. Following points are observed from Table 4.1:

1. Single active block is used in [53, 54 (Fig. 2, 3), 77] whereas multiple active blocks of different and similar types are employed in [56, 67, 68, 71, 76, 78] and [55, 60, 65 (Fig. 5a, 9a), 70 (Fig. 3)] respectively.
2. Number of simultaneously available responses: two in [54, 55], three in [29, 52, 53, 57-59, 61-69, 72-75, 77-79], four in [30] and all the five in [56, 60, 70 (Fig.3 & 4), 71, 76].
3. Some of the responses are available through components in [30, 53, 54 (Fig.2, 3), 59, 77]. Therefore, additional active block would be required to process output further.
4. The desired condition of low input impedance in CM filters is not maintained in [29, 52-54, 59, 63, 64, 73, 77, 79].
5. The configurations [54, 57, 65, 69, 79] use floating passive elements which are not suitable from fabrication viewpoint.
6. References [29, 30, 52, 54, 55, 59, 61-67, 69, 70, 77] do not support independent adjustment of filter parameters. The parameters adjustment is possible in [55, 56, 60, 68, 71-73, 76] and [53, 58, 65 (sec. 2.2, 3.2), 74, 75, 78, 79] through transconductance (g_m) or internal resistance of active block.

Table 4.1 Comparative analysis of CM SIMO Filters

Ref.	Number and type of active block (s)	Number of passive elements -Resistors (R), Capacitors(C), Floating element	I/O impedance, High (H), Low (L)	Available responses[+]	Possible additional responses	Independent adjustment of filter parameters
[29]	2 MO-OFC	2R, 2C	H/H	LP, Notch, BP	HP, AP	No
[30]	3 OFCC	2R, 2C	L/L	LP, HP(C), Notch, BP	AP	No
[52]	3 DVCC	4R, 2C	H/H	LP, HP, BP	Notch, AP	No
[53]	1 CCTA	2R, 2C	H/L	LP, HP(C), BP(R,C)	Notch, AP	Yes
[54]	(i) 1 CCIII+ or – (Fig.2, 3)	1R, 2C, 1R Floating	H/L	LP(R), BP(C).	N.A.	No
	(ii) 3 CCIII+ (Fig.9)	1R, 2C, 1R Floating	H/H	LP, BP	N.A.	No
[55]	4 CFTA	2C	L/H	LP, BP	HP, Notch, AP	Yes
[56]	2 CCCII, 1 MOCCA	2C	L/H	LP, HP, BP, Notch, AP	N.A.	Yes
[57]	3 MOCCII	3R, 2C, 2R Floating	L/H	LP, BP, Notch	HP, AP	No
[58]	3CCII	3R, 2C	L/H	LP, BP, Notch	HP, AP	Yes
[59]	2 OTA	2C	L/L	LP, HP (C), BP	Notch, AP	No
[60]	4 ZC-CFTA	2C	L/H	LP, HP, BP, Notch, AP	N.A.	Yes
[61]	2 ZC-CITA	2C	L/H	LP, HP, BP	Notch, AP	No
[62]	3 MOCC	2R, 2C	L/H	LP, HP, BP	Notch, AP	No
[63]	3 MOCC	4R, 2C	H/H	LP, HP, BP	Notch, AP	No
[64]	3 MOCCCII	1R, 2C	H/H	LP, HP, BP	Notch, AP	No
[65]	Case-I (Sec-2.1, 2.2) & Case-II (Sec-3.1, 3.2). *3 to 5 CCII+/-	Floating R & C (2.1, 2.2) & Grounded R & C (3.1, 3.2). **2 to 5 R, 2 to 3 C	L/H	LP, HP, BP (for all sections)	Notch, AP (for all sections)	No (2.1, 3.1) & Yes (2.2, 3.2)
[66]	3 MOCCII	2R, 2C	L/H	LP, HP, BP	Notch, AP	No
[67]	2 DOCCII, 1 DOCCIII	2R, 2C	L/H	LP, HP, BP	Notch, AP	No
[68]	2 CCII, 1 MOCCCA	2R, 2C	L/H	LP, HP, BP	Notch, AP	Yes
[69]	3 MO-CF	2C, 2R floating	L/H	LP, HP, BP	Notch, AP	No
	(i) 3 DOCCCII (Fig. 2)	2C	L/H	LP, HP, BP	Notch, AP	No
[70]	(ii) 4 CCCII (Fig. 3)	2C	L/H	LP, HP, BP, Notch, AP	N.A.	No
	(iii) 3 CCCII (Fig. 4)	2C	L/H	LP, HP, BP, Notch, AP	N.A.	No
[71]	2 CCCII, 1 CCCII with controlled current gain	2C	L/H	LP, HP, BP, Notch, AP	N.A.	Yes
[72]	3 ZC-CFTA	2C	L/H	LP, HP, BP	Notch, AP	Yes
[73]	2 CCCCTA	2C	H/H	LP, BP, Notch	HP, AP	Yes
[74]	3 DOCCII	3R, 2C	L/H	LP, BP, Notch	HP	Yes
[75]	3 DO-ICCII	3R, 2C	L/H	LP, BP, Notch	HP	Yes
[76]	2 CCCII, 1 CCCII with controlled current gain	2C	L/H	LP, HP, BP, Notch, AP	N.A.	Yes
[77]	1 CFTA	2C	H/L	LP, HP (C), BP	N.A.	No
[78]	2 OTA, 1 ICCIII	1R, 2C	L/H	LP, BP, Notch	HP, AP	Yes
[79]	2 DVCCs	2R, 2C, 1R floating	H/H	LP, BP, Notch	HP, AP	Yes
Proposed	3 OFCC	3R, 2C	L/H	LP, HP, BP, Notch	AP	Yes

N.A.: - Not available, [+]Low pass (LP), High pass (HP), Band pass (BP), Notch and All pass (AP)

[65] *: - 5 CCII+/- in Fig. 5(a), Fig. 9(a) and [65] **: - 4R,2C Fig. 12, 3R,3C Fig. 15, 5R, 2C Fig. 18.

It is clear from above discussion that only one SIMO filter [60] is available that uses similar active blocks and provides four or more output responses at high output impedance; and allows independent adjustment of filter parameters. This configuration, however, uses four active blocks. Therefore, a SIMO filter is presented in this chapter, which uses three active blocks of same type and provides four output responses simultaneously. Further, it possesses independent adjustment of filter parameters and presents output at high impedance. An application of proposed SIMO filter, namely shadow filter is also put forward.

4.3 PROPOSED CM SIMO FILTER

This section put forwards proposed OFCC based CM SIMO filter. The behavior of filter in presence of non-idealities is also analyzed and presented.

4.3.1 Proposed OFCC based CM SIMO Filter

The proposed OFCC based CM SIMO filter is depicted in Fig. 4.1. It uses three OFCCs, three grounded resistors and two grounded capacitors. The filter transfer functions are derived through routine analysis and are obtained as

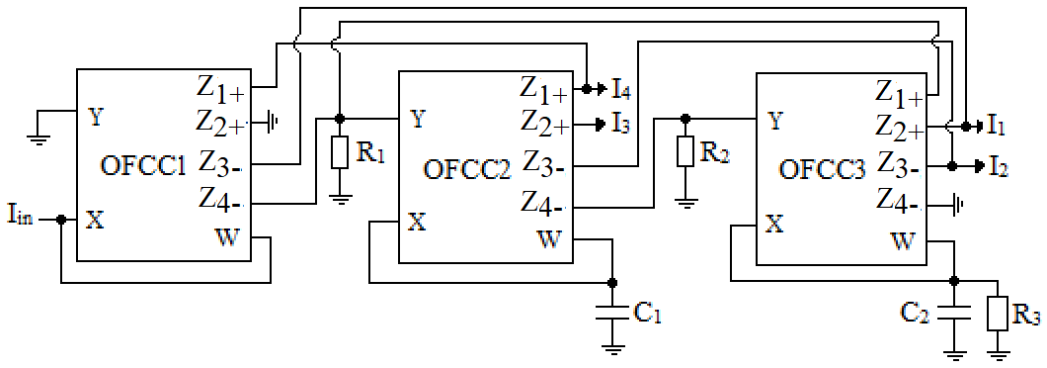


Fig. 4.1 Proposed OFCC based CM SIMO Filter

$$T_{LP} = \frac{I_1}{I_{in}} = \frac{-R_3}{s^2C_1C_2R_1R_2R_3+sC_1R_1R_2+R_3} \quad (4.2)$$

$$T_{HP} = \frac{I_2}{I_{in}} = \frac{-s^2C_1C_2R_1R_2R_3}{s^2C_1C_2R_1R_2R_3+sC_1R_1R_2+R_3} \quad (4.3)$$

$$T_{BP} = \frac{I_3}{I_{in}} = \frac{-sC_1R_1R_3}{s^2C_1C_2R_1R_2R_3+sC_1R_1R_2+R_3} \quad (4.4)$$

$$T_{NF} = \frac{I_4}{I_{in}} = \frac{s^2C_1C_2R_1R_2R_3+R_3}{s^2C_1C_2R_1R_2R_3+sC_1R_1R_2+R_3} \quad (4.5)$$

and

$$T_{AP} = \frac{I_5}{I_{in}} = \frac{s^2C_1C_2R_1R_2R_3-sC_1R_1R_3+R_3}{s^2C_1C_2R_1R_2R_3+sC_1R_1R_2+R_3} \quad (4.6)$$

where $I_5 = I_3 + I_4$.

It is clear from (4.2) to (4.6) that low pass, high pass, band pass and notch responses are available simultaneously at high output impedance therefore these can easily be cascaded. The all pass response may be obtained by simply joining notch and band pass responses together. The filter responses are characterized by pole frequency (ω_o), quality factor (Q_o) and bandwidth ($BW = \omega_o/Q_o$) as given in (4.7) and (4.8)

$$\omega_o = \sqrt{\frac{1}{C_1C_2R_1R_2}} \quad , \quad Q_o = R_3\sqrt{\frac{C_2}{C_1R_1R_2}} \quad (4.7)$$

$$BW = \frac{\omega_o}{Q_o} = \frac{1}{C_2R_3} \quad (4.8)$$

As seen from (4.7), ω_o and Q_o can be tuned by varying R_1 and R_2 without affecting ω_o/Q_o. Further Q_o can be tuned by varying R_3 while keeping ω_o fixed.

The sensitivity of the proposed filter parameters ω_o and Q_o for passive components used is computed as:

$$S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = S_{R_1}^{Q_o} = S_{R_2}^{Q_o} = S_{C_1}^{Q_o} = -\frac{1}{2}, \qquad S_{R_3}^{Q_o} = S_{C_2}^{Q_o} = \frac{1}{2} \quad (4.9)$$

It is clear from (4.9) that all the passive sensitivities are less than unity in magnitude thus the proposed circuit may be termed as insensitive [80].

4.3.2 Non Ideal Analysis

In practice, the filter performance may deviate from the ideal one due to the nonidealities discussed in section 2.3. The effect of transimpedance gain, tracking errors and various parasites is examined in the following subsections.

4.3.2.1 Effect of Finite transimpedance gain

The transfer functions given in section 4.3.1 are obtained by considering ideal value of transimpedance gain. Practically, value of transimpedance gain is frequency dependent and finite. Now considering the effect of finite transimpedance gain ($Z_t(s)$) with single pole model as given in section 2.3.1, the transfer functions (4.2) - (4.6) modify to

$$T_{LP\_fz} = \left.\frac{I_1}{I_{in}}\right|_{fz} = \frac{-R_3}{D_{n\_fz}(s)} \tag{4.10}$$

$$T_{HP\_fz} = \left.\frac{I_2}{I_{in}}\right|_{fz} = \frac{-s^2(C_1+C_p)(C_2+C_p)R_1R_2R_3}{D_{n\_fz}(s)} \tag{4.11}$$

$$T_{BP\_fz} = \left.\frac{I_3}{I_{in}}\right|_{fz} = \frac{-s(C_1+C_p)R_1R_3}{D_{n\_fz}(s)} \tag{4.12}$$

$$T_{NF\_fz} = \left.\frac{I_4}{I_{in}}\right|_{fz} = \frac{s^2(C_1+C_p)(C_2+C_p)R_1R_2R_3+R_3}{D_{n\_fz}(s)} \tag{4.13}$$

and

$$T_{AP\_fz} = \left.\frac{I_5}{I_{in}}\right|_{fz} = \frac{s^2(C_1+C_p)(C_2+C_p)R_1R_2R_3-s(C_1+C_p)R_1R_3+R_3}{D_{n\_fz}(s)} \tag{4.14}$$

where $D_{n\_fz}(s) = s^2(C_1+C_p)(C_2+C_p)R_1R_2R_3 + s(C_1+C_p)R_1R_2 + R_3$ (4.15)

The filter parameters, in presence of finite transimpedance, may be derived from (4.15) as

$$\omega_o|_{fz} = \sqrt{\frac{1}{(C_1+C_p)(C_2+C_p)R_1R_2}} \quad , \qquad Q_o|_{fz} = R_3\sqrt{\frac{C_2+C_p}{(C_1+C_p)R_1R_2}} \tag{4.16}$$

$$BW|_{fz} = \frac{\omega_o}{Q_o}\Big|_{fz} = \frac{1}{(C_2+C_p)R_3} \tag{4.17}$$

It may be observed that the C_p appears in parallel to external capacitors so by choosing C_1, C_2 >> C_p, the effect of $Z_t(s)$ may be accommodated. With this consideration the transfer function and filter parameters given in (4.10) - (4.14) and (4.16), (4.17) reduces to (4.2) - (4.6) and (4.7), (4.8) respectively.

4.3.2.2 Effect of Tracking errors

Now considering the effect of tracking errors given in section 2.3.2, the transfer functions (4.2) - (4.5) modify to

$$T_{LP\_tr} = \frac{I_1}{I_{in}}\Big|_{tr} = \frac{s^2C_1C_2R_1R_2R_3\alpha\beta^2(\gamma^2-1)+sC_1R_1R_2\alpha\beta^2(\gamma^2-1)-R_3}{D_{n\_tr}(s)} \tag{4.18}$$

$$T_{HP\_tr} = \frac{I_2}{I_{in}}\Big|_{tr} = \frac{s^2C_1C_2R_1R_2R_3\alpha\beta^2\gamma^3+sC_1R_1\alpha\beta\gamma^2(\beta\gamma R_2-R_3)}{D_{n\_tr}(s)} \tag{4.19}$$

$$T_{BP\_tr} = \frac{I_3}{I_{in}}\Big|_{tr} = \frac{sC_1R_1R_3\alpha\beta\gamma}{D_{n\_tr}(s)} \tag{4.20}$$

$$T_{NF\_tr} = \frac{I_4}{I_{in}}\Big|_{tr} = \frac{s^2C_1C_2R_1R_2R_3\alpha^2\beta^2+sC_1R_1\alpha\beta(\alpha\beta R_3-\gamma R_3)+\alpha R_3}{D_{n\_tr}(s)} \tag{4.21}$$

where $D_{n\_tr}(s) = s^2C_1C_2R_1R_2R_3\alpha\beta^2 + sC_1R_1R_2\alpha\beta^2 + R_3$ (4.22)

The filter parameters, in presence of finite transimpedance, may be obtained from (4.22) as

$$\omega_o|_{tr} = \sqrt{\frac{1}{C_1C_2R_1R_2\,\alpha\beta^2}} \;\; , \; Q_o|_{tr} = R_3\sqrt{\frac{C_2}{C_1R_1R_2\,\alpha\beta^2}} \tag{4.23}$$

$$BW|_{tr} = \frac{\omega_o}{Q_o}\Big|_{tr} = \frac{1}{C_2R_3} \tag{4.24}$$

It may be observed that if $\alpha = \gamma = 1$, $\beta = 1$ and equal resistances are considered, the transfer functions and filter parameters given in (4.18) - (4.21) and (4.23), (4.24) reduces to (4.2) - (4.5) and (4.7), (4.8) respectively.

4.3.2.3 Effect of Parasites

The effect of parasites on filter behavior is studied in this section to obtain the values of various component used in the circuit from design specifications. The parasites are manifested as parallel combination of resistor and capacitor at ports Y, Z_i (i = 1+,2+,3-,4-) (i.e. R_Y, C_Y, R_{Zi}, C_{Zi}). The proposed filter topology of Fig. 4.1 modifies to Fig. 4.2 in presence of parasites. The parasites appear in parallel at respective ports and show their presence by modifying the values of resistors R_1 as R_{eq1} // C_{para1} and R_2 as R_{eq2} // C_{para2}. Here, $R_{eq1} = R_1//R_{Y2}//R_{Z41}//R_{Z13}$, $R_{eq2} = R_2//R_{Y3}//R_{Z42}$, $C_{para1} = C_{Y2}//C_{Z41}//C_{Z13}$ and $C_{para2} = C_{Y3}//C_{Z42}$. The subscripts i and j with Z port correspond to j^{th} Z port of i^{th} OFCC.

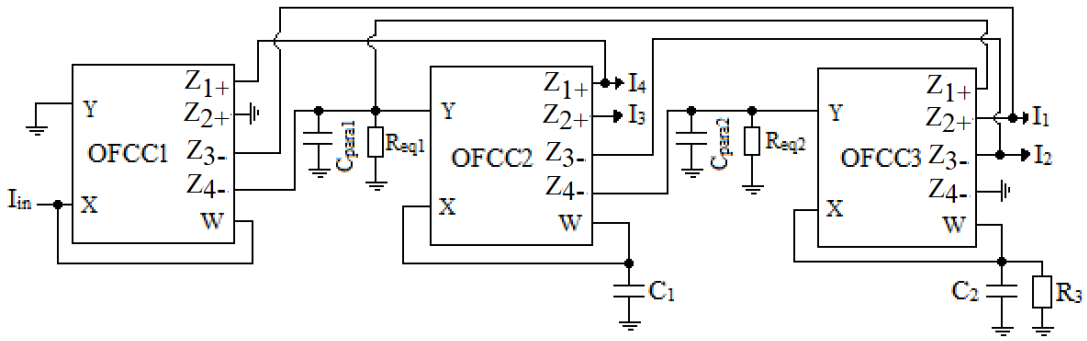


Fig. 4.2 Proposed OFCC based CM SIMO filter with parasites

By taking parasites into account, denominator of transfer functions (4.2) - (4.6) modifies to

$$D_{n\_para}(s) = s^2\left(R_{eq1}R_{eq2}R_3\left(C_1C_2 + C_{para1}C_{para2}\right)\right) + s\left(C_1R_{eq1}R_{eq2} + R_{eq2}R_3C_{para1} + R_{eq2}R_3C_{para2}\right) + R_3 \quad (4.25)$$

where n_para denotes nonideal effect due to parasites only.

So in presence of parasites the pole frequency modifies to

$$\omega_o^2|_{para} = \frac{1}{R_{eq1}R_{eq2}R_3(C_1C_2+C_{para1}C_{para2})} \tag{4.26}$$

$$\omega_o^2|_{para} = \frac{1}{R_{eq1}R_{eq2}R_3C_1C_2}\left[1+\frac{C_{para1}C_{para2}}{C_1C_2}\right]^{-1} \tag{4.27}$$

For C_1, C_2 >> $C_{para1}C_{para2}$, the square bracket term in (4.27) is approximately equal to unity, so

$$\omega_o^2|_{para} = \frac{1}{R_{eq1}R_{eq2}R_3C_1C_2} \tag{4.28}$$

Similarly, the bandwidth in presence of parasites modifies to

$$\left.\frac{\omega_o}{Q}\right|_{para} = \frac{C_1R_{eq1}R_{eq2}+C_{para1}R_{eq2}R_3+C_{para2}R_{eq2}R_3}{R_{eq1}R_{eq2}C_1C_2R_3} \tag{4.29}$$

$$\left.\frac{\omega_o}{Q}\right|_{para} = \frac{1}{C_2R_3}+\frac{C_{para1}}{C_1C_2R_{eq1}}+\frac{C_{para2}}{C_1C_2R_{eq1}} = \frac{1}{C_2R_3}+\frac{1}{R_{eq1}}\left[\frac{C_{para1}}{C_1C_2}+\frac{C_{para2}}{C_1C_2}\right] \tag{4.30}$$

For C_1, C_2 >> C_{para1}, C_{para2}, (4.30) may be written as

$$\left.\frac{\omega_o}{Q}\right|_{para} \approx \frac{1}{C_2R_3} \tag{4.31}$$

The effect of parasites on bandwidth may be ignored if

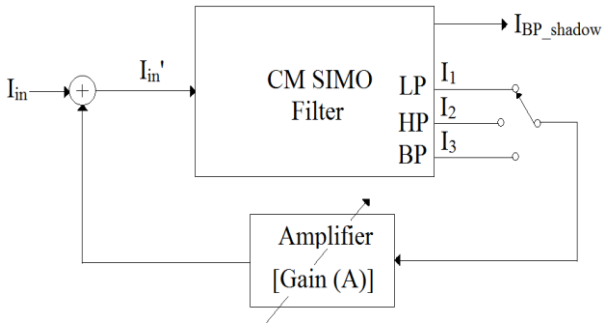
$$\frac{1}{C_2R_3} \gg \frac{1}{R_{eq1}}\left[\frac{C_{para1}}{C_1C_2}+\frac{C_{para2}}{C_1C_2}\right] \tag{4.32}$$

$$C \gg \frac{1}{R_{eq1}}\left(C_{para1}+C_{para2}\right)\frac{Q}{\omega_o} = C_D \tag{4.33}$$

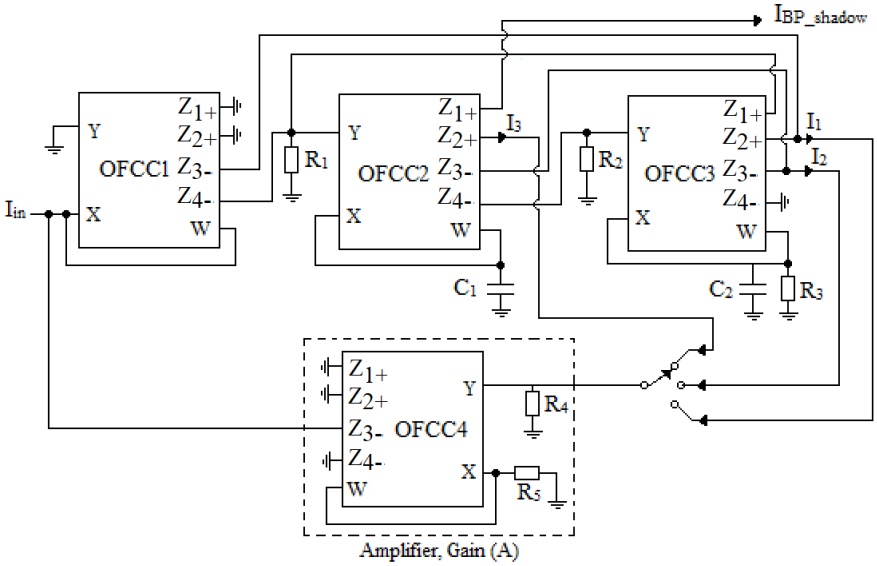
As typical values of parasitic resistors are of the order of hundreds of kΩs, so by selecting external resistors of the order of kΩs and C = C_1 = C_2 >> C_D, the filter may approach towards ideal response as the effect of parasitic impedance can be practically ignored.

4.4 PROPOSED OFCC BASED CM SHADOW BAND PASS FILTER

In this section proposed CM SIMO filter is used to develop an application namely shadow band pass filter. The concept of shadow filter also referred as frequency agile filter [81-86] is based on adding an amplifier in feedback loop and adjusting filter parameters by appropriately changing the amplifier gain.



(a)



(b)

Fig.4.3 (a) Generalized scheme of shadow filter [81],

(b) Proposed OFCC based CM shadow band pass filter

Generalized scheme for CM shadow band pass filter [81] is depicted in Fig. 4.3(a). It uses a CM SIMO filter and one out of LP, BP or HP is applied to input via amplifier.

The proposed filter of Fig. 4.1 is used to construct OFCC based shadow band pass filter and the corresponding proposed circuit is depicted in Fig. 4.3 (b). Here OFCC4 with resistors R_4 and R_5 forms the amplifier of gain ($A = R_4/R_5$). It may be noted that the ports Z_{1+} of OFCC1 and Z_{1+} of OFCC2 are disconnected to obtain an additional band pass response.

Connecting the low pass current (I_1) to the amplifier input, results in low pass controlled shadow band pass response and the governing transfer function is obtained as

$$\left(\frac{I_{BP\_shadow}}{I_{in}}\right)_{BP\_LPC} = \frac{-s/(C_2R_2)}{s^2+\frac{s}{C_2R_3}+\frac{(1+A)}{C_1C_2R_1R_2}} \tag{4.34}$$

where BP_LPC legend represents low pass controlled shadow band pass filter.

The pole frequency, quality factor and bandwidth of the low pass controlled shadow band pass filter are represented by ω_{o_LPC}, Q_{o_LPC} and $BW_{LPC} = \omega_{o\_LPC}/Q_{o\_LPC}$ respectively and are computed from (4.34) as

$$\omega_{o\_LPC} = \sqrt{\frac{(1+A)}{C_1C_2R_1R_2}} \tag{4.35}$$

$$Q_{o\_LPC} = R_3\sqrt{\frac{C_2(1+A)}{C_1R_1R_2}} \tag{4.36}$$

$$BW_{LPC} = \frac{\omega_{o\_LPC}}{Q_{o\_LPC}} = \frac{1}{C_2R_3} \tag{4.37}$$

It is clear from (4.35) to (4.37) that ω_{o_LPC} and quality factor Q_{o_LPC} can be adjusted via amplifier gain while keeping bandwidth BW_{LPC} same as original bandwidth (BW).

Connecting the high pass current (I_2) to the amplifier input, results in high pass controlled shadow band pass response and the governing transfer function is obtained as

$$\left(\frac{I_{BP\_shadow}}{I_{in}}\right)_{BP\_HPC} = \frac{-s/\left(C_2R_2(1+A)\right)}{s^2+\frac{s}{C_2R_3(1+A)}+\frac{1}{C_1C_2R_1R_2(1+A)}} \quad (4.38)$$

where legend BP_HPC represents high pass controlled shadow band pass filter.

From (4.38), pole frequency(ω_{o_HPC}) quality factor (Q_{o_HPC}) and bandwidth BW_{HPC} (= ω_{o_HPC}/Q_{o_HPC}) of the high pass controlled shadow band pass filter are computed as

$$\omega_{o\_HPC} = \sqrt{\frac{1}{C_1C_2R_1R_2(1+A)}} \quad (4.39)$$

$$Q_{o\_HPC} = R_3\sqrt{\frac{C_2(1+A)}{C_1R_1R_2}} \quad (4.40)$$

$$BW_{HPC} = \frac{\omega_{o\_HPC}}{Q_{o\_HPC}} = \frac{1}{C_2R_3(1+A)} \quad (4.41)$$

It is observed from (4.39) to (4.41) that all filter parameters vary with amplifier gain. The change in ω_{o_HPC} and Q_{o_HPC} is opposite in nature i. e. with increase in gain ω_{o_HPC} decreases while Q_{o_HPC} increases.

Connecting the band pass current (I_3) to the amplifier input, results in band pass controlled shadow band pass response and the governing transfer function is obtained as

$$\left(\frac{I_{BP\_shadow}}{I_{in}}\right)_{BP\_BPC} = \frac{-s/(C_2R_2)}{s^2+\frac{s(1+A)}{C_2R_3}+\frac{1}{C_1C_2R_1R_2}} \quad (4.42)$$

where BP_BPC represents band pass controlled shadow band pass filter.

From (4.42), pole frequency(ω_{o_BPC}), quality factor (Q_{o_BPC}) and bandwidth BW_{BPC} (= ω_{o_BPC}/Q_{o_BPC}) of the high pass controlled shadow band pass filter are computed as

$$\omega_{o\_BPC} = \sqrt{\frac{1}{C_1C_2R_1R_2}} \quad (4.43)$$

$$Q_{o\_BPC} = \frac{R_3}{(1+A)}\sqrt{\frac{1}{C_1R_1R_2}} \quad (4.44)$$

$$BW_{BPC} = \frac{\omega_{o\_BPC}}{Q_{o\_BPC}} = \frac{(1+A)}{C_2 R_3} \quad (4.45)$$

It is clear from (4.43) and (4.45) that ω_{o_BPC} remains same as that of original filter. The Q_{o_BPC} may be varied by gain of amplifier.

All the grounded resistors used in circuits of Fig. 4.1 and 4.3 are implemented using the scheme depicted in Fig. 2.16 [169]. So by varying the bias voltages, R_i can be varied to tune the circuit parameters electronically. This allows the resistances to vary with bias voltages, leading to variation of electronic variation of filter parameters.

4.5 SIMULATION RESULTS

The operation of proposed filters is verified through SPICE simulations using CMOS based implementation of OFCC [13] as shown in Fig. 2.3. The proposed CM SIMO filter was simulated for pole frequency of 320 KHz using $C_1 = C_2 = 100$ pF and MOS based resistors of values $R_1 = R_2 = R_3 = 5$ kΩ by selecting bias voltages V_{1i} and V_{2i} in Fig. 2.16 as ± 0.726 V respectively.

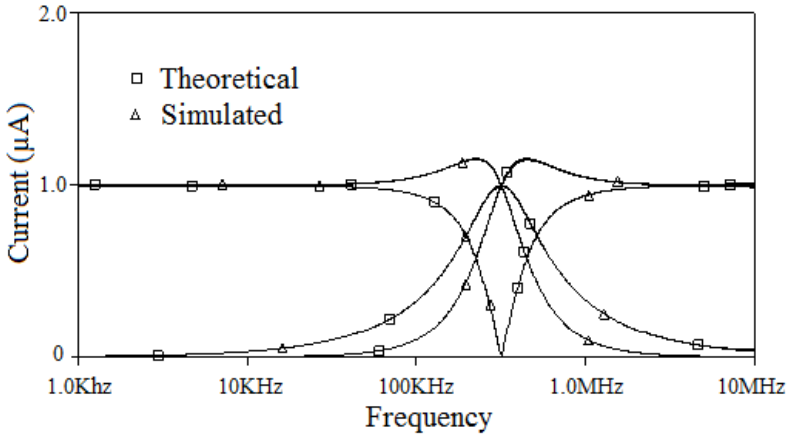


Fig. 4.4 Theoretical and simulated responses of CM SIMO filter

Theoretical and simulated results for low pass, high pass, band pass and notch frequency responses are shown in Fig. 4.4. The simulation results agree quite well with the theoretical analysis. The magnitude and phase plot of all pass response is given in Fig. 4.5.

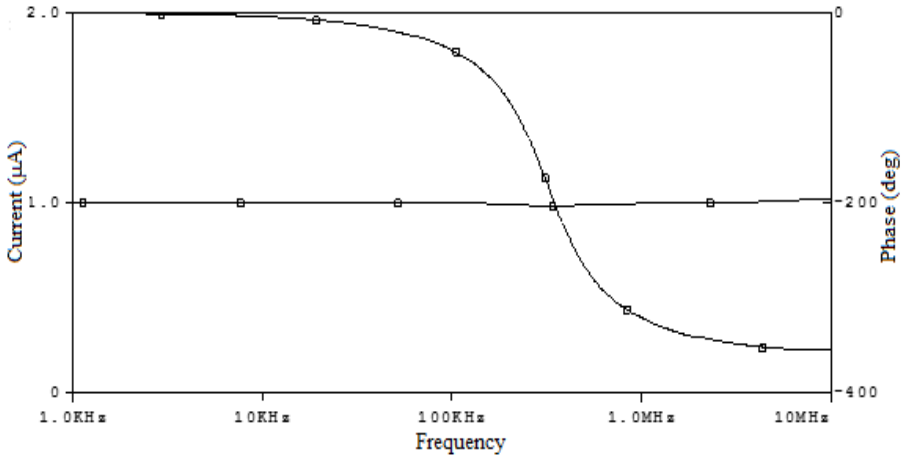


Fig. 4.5 Simulated magnitude and phase plots of all pass response

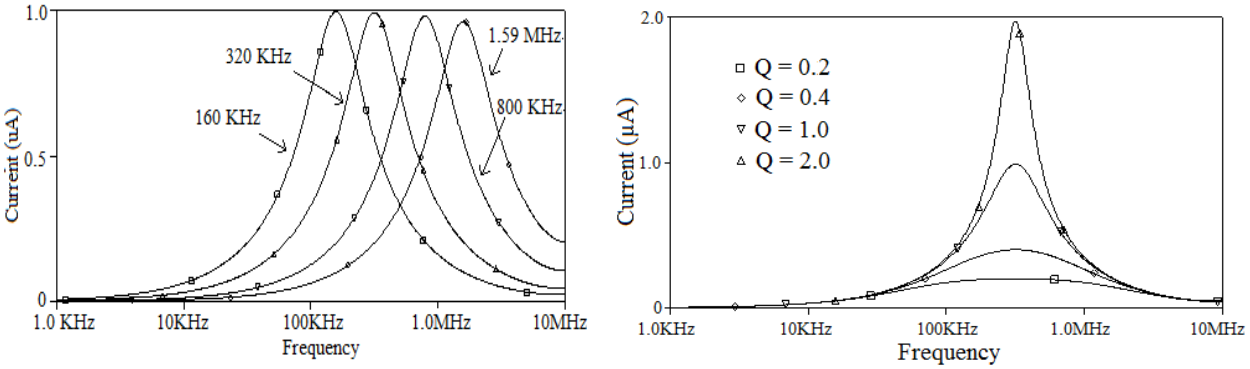
Table 4.2 Simulation settings for independent adjustment of filter parameters

Orthogonal adjustment of f_o with Q_o (Q_o = 1)				**Orthogonal adjustment of Q_o with f_o (f_o = 320 KHz), ($R_1 = R_2$ = 5 kΩ)**			
$V_{11} = V_{12} = V_{13}$ *(V)	**$V_{21} = V_{22} = V_{23}$ *(V)**	**$R_1 = R_2 = R_3$ (kΩ)**	**f_o (KHz)**	**V_{13} *(V)**	**V_{23} *(V)**	**R_3 (kΩ)**	**Q_o**
1.310	-1.310	1	1590	1.310	-1.310	1	0.2
0.869	-0.869	2	800	0.869	-0.869	2	0.4
0.726	-0.726	5	320	0.726	-0.726	5	1
0.711	-0.711	10	160	0.711	-0.711	10	2

*V_{1i} and *V_{2i} refer to bias voltages corresponding to resistance R_i.

Simulation results for independent adjustment of filter parameters are shown in Fig. 4.6 with setting enlisted in Table 4.2. The adjustment of f_o for Q_o fixed at unity is achieved by keeping $R_1 = R_2 = R_3$ and varying these simultaneously. The Q_o adjustment for given f_o is obtained by keeping R_1 and R_2 fixed and varying R_3. Time domain behavior of proposed filter is

verified for sinusoidal current excitation of 2 µA amplitude and 500 KHz frequency and corresponding transient response of low pass, high pass and band pass filter is shown in Fig. 4.7.



(a) Tuning of f_o with R_1 and R_2 (b) Tuning of Q_o with R_3

Fig. 4.6 Tuning of f_o and Q_o

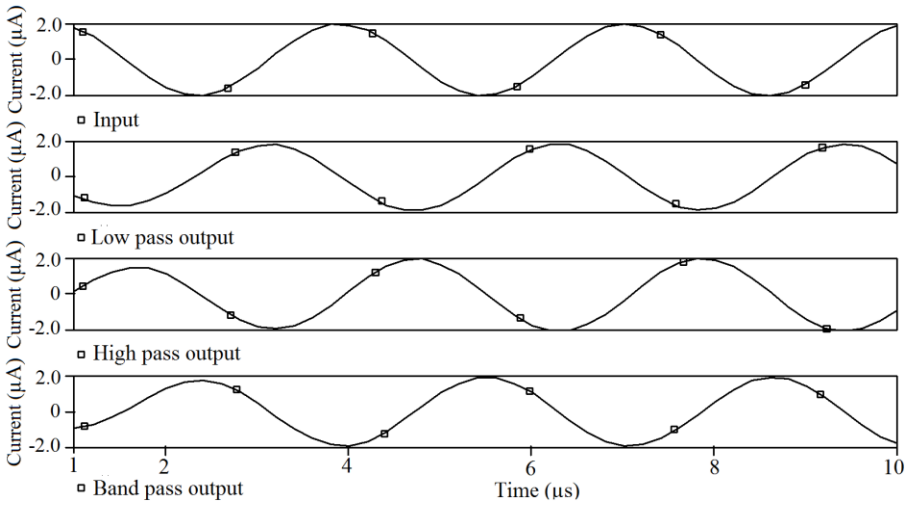


Fig. 4.7 Transient responses for Sinusoidal current input of 2µA, 500 KHz

The frequency spectrum in Fig. 4.8 confirms the effectiveness of the proposed filter for mixed sinusoidal current input of 2 µA amplitude and 50 KHz, 500 KHz, 2.85 MHz frequencies.

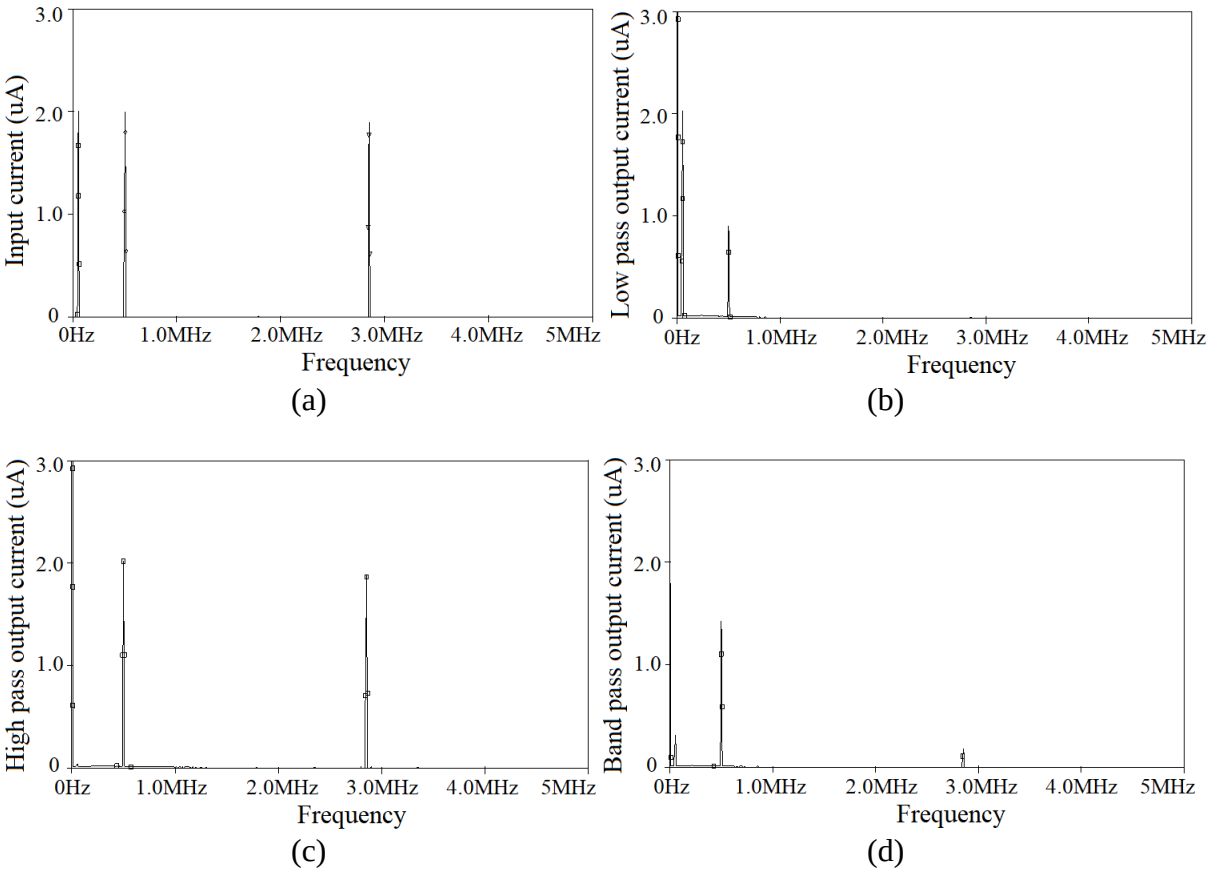


Fig. 4.8 Frequency spectrum of (a) input (b) low pass (c) high pass and (d) band pass output

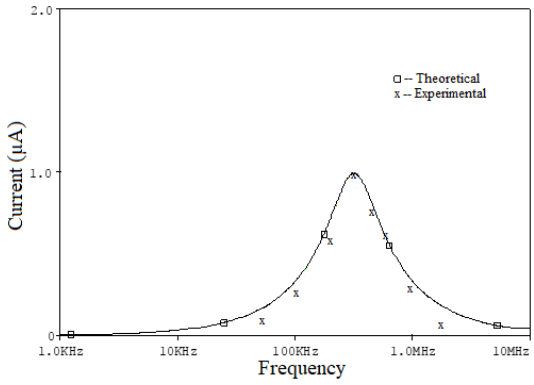


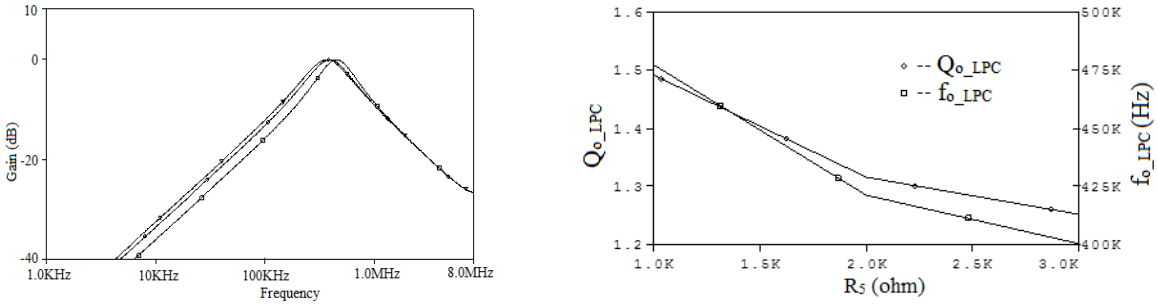
Fig. 4.9 Simulated and experimental bandpass frequency response

The circuit of Fig. 4.1 is prototyped using commercially available IC AD844 based OFCC implementation [170] of Fig. 2.5 (b). The component values are kept same as those used for simulations. The theoretical and experimental frequency response for bandpass output are

depicted in Fig. 4.9. The slight deviation in the responses is observed which is due to nonidealities.

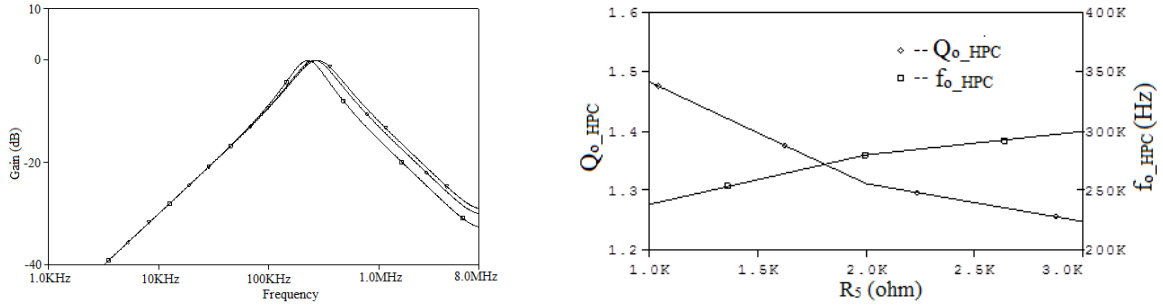
To test the functionality of proposed CM shadow band pass filter of Fig. 4.3(b), the original filter pole frequency is chosen as 320 KHz by employing component values ($C_1 = C_2 =$ 100 pF and $R_1 = R_2 = R_3 = 5$ kΩ). For amplifier block where R_4, R_5 are electronically controlled and keeping $R_4 = 1$ kΩ while R_5 is electronically varied as 1 kΩ, 2 kΩ and 3 kΩ to control the gain of the amplifier. The gain of the amplifier can also be varied using R_4 or R_5 or both. The variation in LP, HP and BP controlled shadow band pass filter parameters with gain is depicted in Fig. 4.10, Fig. 4.11 and Fig. 4.12 respectively. The simulated filter parameters of shadow band pass filter with values of tuning resistor R_4 and R_5 is given in Table 4.3.

It may be noted that the proposed filter and shadow filter have similar characteristics. By examining the expression of ω_o, ω_o/Q_0 and Q_0 it is observed that low pass controlled shadow band pass offers one unique feature of constant bandwidth ($BW_{\_LPC}$) which is independent of ω_{o_LPC} and Q_{o_LPC}. This fact is pictorially represented in Fig. 4.13 by including ω_o/Q_o in Fig. 4.10(b).



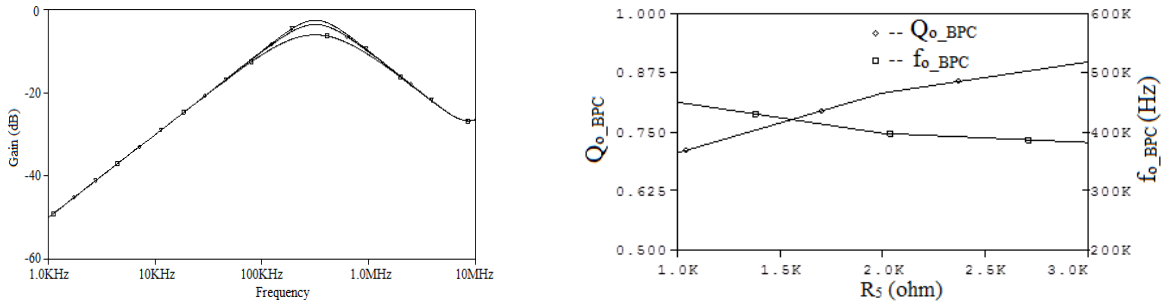
(a) (b)

Fig. 4.10 LP controlled shadow BP response



(a) (b)

Fig. 4.11 HP controlled shadow BP response



(a) (b)

Fig. 4.12 BP controlled shadow BP response

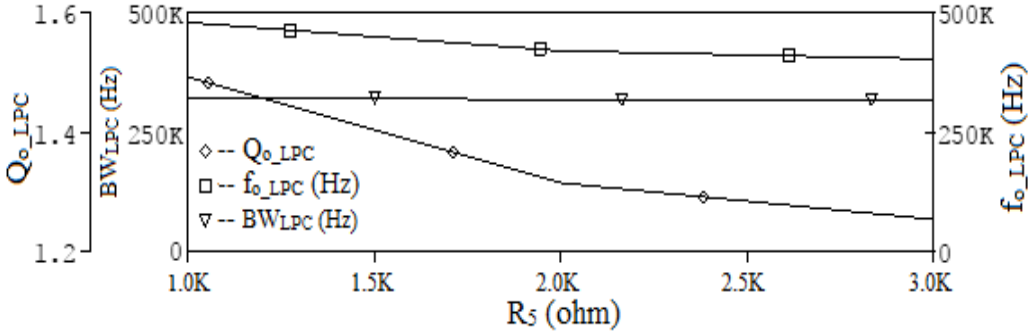


Fig. 4.13 LP controlled shadow BP response with bandwidth ($BW_{\_LPC}$) independent of ω_{o_LPC} and Q_{o_LPC}

Table 4.3 Tuning of shadow filter parameters

					Q_o = 1, f_o = 320 KHz ($R_1=R_2=R_3=5k\Omega$, $C_1=C_2=100pF$)					
V_{14} = - V_{24} *(V)	R_4 (kΩ)	V_{15} = - V_{25} *(V)	R_5 (kΩ)	Gain (A)	LP controlled BP		HP controlled BP		BP controlled BP	
					Q_{o_LPC}	f_{o_LPC} (KHz)	Q_{o_HPC}	f_{o_HPC} (KHz)	Q_{o_BPC}	f_{o_BPC} (KHz)
1.310	1	1.310	1	1	1.49	477.61	1.48	238.56	.706	449.75
1.310	1	0.869	2	0.5	1.31	421.21	1.31	280.44	.831	398.02
1.310	1	0.803	3	0.33	1.25	400.63	1.24	300.12	.898	382.75

*V_{1i} and *V_{2i} refer to bias voltages corresponding to resistance R_i.

4.6 CONCLUDING REMARKS

An OFCC based CM electronically tunable SIMO filter configuration is presented in this chapter. In proposed SIMO filter all the five standard filter responses are available and only three OFCCs, two grounded capacitors and three grounded resistors are used. MOS based implementation of grounded resistors is used for electronic tuning. An application of proposed SIMO filter namely shadow band pass filter is also suggested wherein the filter parameters are controlled by amplifier gain instead of varying components of constituent filter, therefore providing unique electronic tuning feature. The amplifier in shadow band pass filter is realized using an OFCC and two grounded resistors. The proposed configurations are functionally verified through SPICE simulations. The CM SIMO filter is also examined via prototyping it with commercially available IC AD844.

CHAPTER - 5

OFCC BASED INSTRUMENTATION AMPLIFIER

This chapter includes various details, analysis and simulated results of following published papers:

[1] Neeta Pandey, **Deva Nand,** Rajeshwari Pandey, **"Generalized Operational Floating Current Conveyor based Instrumentation Amplifier"** *IET Circuits Devices and Systems*, 10 (3), pp. 209-219, 2016. **(SCI)** *DOI: 10.1049/iet-cds.2015.024*3

[2] **Deva Nand**, Neeta Pandey, Rajeshwari Pandey, Prateek Tripathi, and Prashant Gola, **"OFCC based voltage and transadmittance mode instrumentation amplifier"**, *AIP Conference Proceedings*, 1859 (020109), 2017. **(Scopus)** *DOI: 10.1063/1.4990262*

[3] Neeta Pandey, **Deva Nand,** V. Venkatesh Kumar, Varun Kumar Ahalawat, Chetna Malhotra, "**Realization of OFCC based Transimpedance Mode Instrumentation Amplifier**" *Journal of Advances in Electrical and Electronic Engineering*, 14 (2), pp. 162-167, 2016. **(Scopus)** *DOI*: *10.15598/aeee.v14i2.1551*

[4] **Deva Nand**, Neeta Pandey, **"A new proposal for OFCC based Instrumentation amplifier"** *International Journal of Electrical and Computer Engineering (IJECE)*, 7 (1), pp. 134-143, 2016. **(Scopus)** *DOI: 10.11591/ijece.*v7*i1.pp134-143*

5.1 INTRODUCTION

The instrumentation amplifier (IA) is used as an input stage in variety of applications such as medical instrumentation [87,88], sensor read out integrated circuits [89], data acquisition systems [2, 90], industrial process control [91], automotive transducers [92], bio-potential acquisition systems [93], [94] and linear position sensing [95] to amplify differential signals and to suppress unwanted common mode signals. Numerous IA have been presented in the literature [14, 96-119] and are classified on the basis of active block employed for implementation. Conventionally the operational amplifier based IAs are termed as voltage mode IAs (VMIA) [97-101, 112, 114, 116, 119] whereas current mode building block based IAs are referred as current mode IAs (CMIA) [14, 96, 102-111, 113, 118].

This chapter deals with IA and presents a generalized IA structure. This generalized structure is categorized into two structures: Structure-I and Structure-II. Each structure is used to develop four IA topologies that can operate in VM, CM, TIM and TAM modes. Structures I and Structure II process the input signals separately by two active blocks. To reduce the number of passive components the structures I and II are modified. Six more IA topologies are derived from modified structures. All proposed IA topologies present proper impedances at input and output thereby avoiding extra active blocks. The effect of nonidealities are analyzed on all derived topologies. A thorough comparison of all proposed topologies with existing one is also put forward in a tabulated format for better comparison followed by concluding remarks.

5.2 LITERATURE REVIEW

A variety of IAs [14, 96-119] are available in open literature. The details of available IAs are comprehended in Table 5.1 and after thorough analysis following points are observed:

- Most of the available IAs [14, 96-114] can process data sensed by voltage sensor but need current to voltage converter for processing current sensors' data.
- The IAs [96, 115-118] are suitable to process data available from current sensor and provide current [115, 118] and voltage outputs [96, 116, 117].
- The IAs may be categorized as VM, CM, TAM and TIM on the basis of input and output signals. Accordingly, the IAs presented in [14, 96-114, 119], [107], [115, 118] and [96, 116, 117] are VM, TAM, CM and TIM IAs respectively.
- Though the input impedance of VM IA topologies [14, 96-114] is high, the output is not available at low impedance [14, 96, 102-104, 106, 107, 110, 111, 113]. It is therefore necessary to place a buffer at the output for isolation.
- The CM and TAM IA topologies with proper impedance level are put forward in [115] and [107] respectively.
- The output impedance of TIM IA topologies [116, 117] is proper but former has high input impedance.
- The IAs [97-101, 112, 114, 116] are designed using operational amplifier and therefore exhibit narrow and gain dependent bandwidth. The gain is independent of band width in [14, 96, 102-104, 107, 110, 111, 113, 115, 117, 118] as current mode active blocks namely CCII [96, 102-104, 113], CCCII [107, 111], OFCC [14], OC [110], OTRA [117] and CFOA [118] are being used. The topologies presented in [105, 106, 108, 109, 119] employ both voltage and current mode active blocks, their bandwidth will be decided by the bandwidth of voltage mode active block.

Table 5.1 Characteristics of available Instrumentation Amplifiers

Ref. No.	Type of input	Type of output	Active elements Used	Resistors/ capacitors used	Input impedance	Output impedance
[14]	Voltage	Voltage	2OFCC	4	High	High
[96]	Voltage	Voltage	2 CCII+	3	High	High
[96]	Current	Voltage	2 CCII+	3	Low	High
[97]	Voltage	Voltage	2 opamps 3 opamps 4 opamps	5 7 6	High High High	Low Low Low
[98]	Voltage	Voltage	3 opamps	7/8	High	Low
[99]	Voltage	Voltage	3 opamps	7	High	Low
[100]	Voltage	Voltage	3 opamps	2	High	Low
[101]	Voltage	Voltage	4 opamps	6	High	Low
[102]	Voltage	Voltage	3 CCII+	2	High	High
[103]	Voltage	Voltage	2CCII+	2	High	High
[104]	Voltage	Voltage	2CCII+	2	High	High
[105]	Voltage	Voltage	2CCII+, 1 opamp	3	High	Low
[106]	Voltage	Voltage	2CC, 2opamps	2	High	High
[107]	Voltage	Voltage	3CCCII	Nil	High	High
[107]	Voltage	Current	3CCCII	Nil	High	High
[108]	Voltage	Voltage	6CCII+, 1opamp	3	High	Low
[109]	Voltage	Voltage	6CCII+, 1opamp	3, 1 capacitor	High	Low
[110]	Voltage	Voltage	2 OC	6	High	High
[111]	Voltage	Voltage	2CCCII	1 active resistor	High	High
[112]	Voltage	Voltage	3opamps	7	High	Low
[113]	Voltage	Voltage	2CCII	2	High	High
[114]	Voltage	Voltage	5opamps	5	High	Low
[115]	Current	Current	MOS	Nil	Low	High
[116]	Current	Voltage	3opamps	10	High	Low
[117]	Current	Voltage	3 OTRA	5	Low	Low
[118]	Current	Current	1 CFOA	4	High	Low
[119]	Voltage	Voltage	3 opamps, 2 cm*, 1 cs**	2, 1 capacitor	High	Low

* current mirrors, ** current subtractor

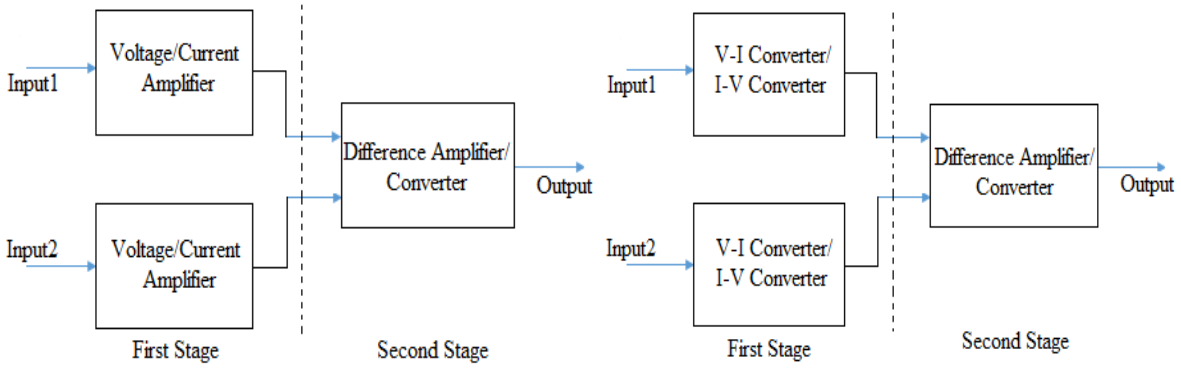
It is clear from the above discussion that though a variety of CM active blocks based VM IA topologies [102-104, 107, 111, 113] are available, yet none of these provide output at low impedance. Further, limited literature is available on TAM, CM and TIM IAs. Therefore, in this chapter two generalized structures are presented which can be used to generate IA topologies operating in all four modes. The active block OFCC is chosen to develop IA topologies as it has both low and high input and output impedance terminals and is thus suitable for amplifying both voltage and current signals at appropriate impedance levels.

5.3 PROPOSED GENERALIZED IA STRUCTURES

Two generalized IA structures are proposed in this section. The section is organized as follows: The OFCC based topologies derived from these configurations, are presented next. Thereafter the behavior of derived IA topologies is examined in presence of OFCC non idealities followed by their functional verification.

5.3.1 Proposed generalized IA structures

The block diagrammatic representation of the generalized IA structures is shown in Fig. 5.1. Each structure consists of two stages to obtain the desired functionality. The first stage of Structure I employs an amplifier whereas Structure II uses a converter as depicted in Fig. 5.1 (a) and (b) respectively.



(a) (b)

Fig. 5.1 Generalized Block Diagrams (a) Structure I (b) Structure II.

A difference amplifier/converter is used as a second stage for both the proposed structures. Appropriate selection of first and second stages for Structures I and II, as detailed in Table 5.2, results in IAs operating in all four modes of operation.

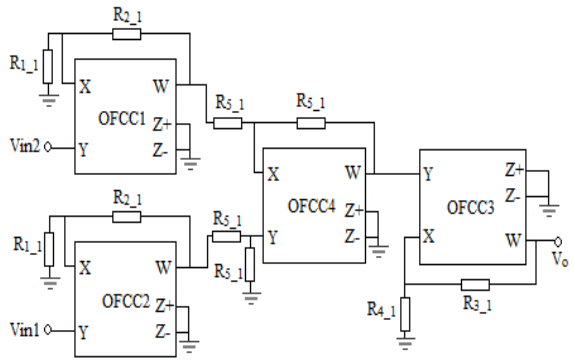
Table 5.2 Stage Description

Structure	Mode	First Stage	Second Stage
Structure I	VM	Voltage Amplifier	Voltage Difference Amplifier
	TAM	Voltage Amplifier	Voltage Difference Current Converter
	CM	Current Amplifier	Current Difference Amplifier
	TIM	Current Amplifier	Current Difference Voltage Converter
Structure II	VM	Voltage to Current converter	Current Difference Voltage Converter
	TAM	Voltage to Current converter	Current Difference amplifier
	CM	Current to Voltage converter	Voltage Difference current converter
	TIM	Current to Voltage converter	Voltage Difference Amplifier

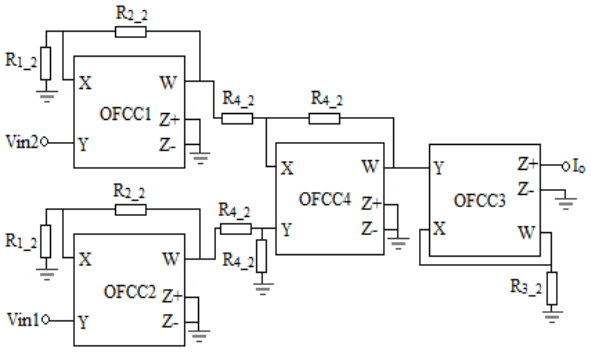
5.3.2 IA topologies derived from Structure I

A close inspection of Table 5.2 entries related to Structure I, reveals that the first stage requires either a voltage or current amplifier whereas the second stage needs voltage/current differencing circuit (for all four modes) followed by a converter (for TAM and TIM modes).

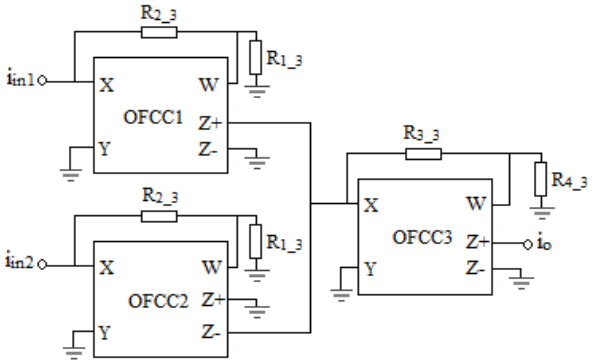
The OFCC based realizations of voltage/current amplifiers, voltage to current/current to voltage converters and voltage difference amplifier as described in section 2.5 are used for obtaining IA topologies. The current difference is performed by simply connecting currents available from Z+ and Z- terminals of two current amplifiers of stage 1. The desired IA topologies derived are given in Fig. 5.2. In stage I, OFCC1 and OFCC2 form voltage amplifiers in topologies 1 and 2 and current amplifiers in topologies 3 and 4. The OFCC3 performs the desired amplification or conversion function and OFCC4 performs voltage differencing as required for proper operation of topologies 1 and 2.



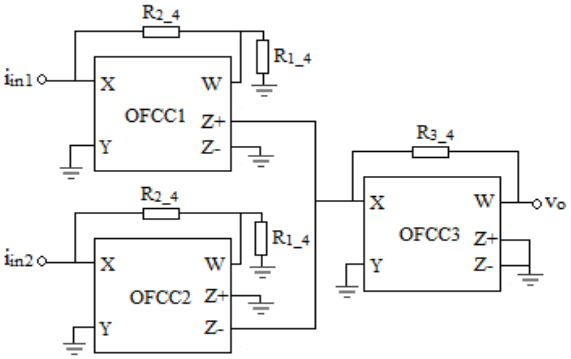
(a) Topology 1



(b) Topology 2



(c) Topology 3



(d) Topology 4

Fig 5.2 Proposed (a) VM (b) TAM (c) CM and (d) TIM IA topologies generated from Structure I

The differential gains of VM, TAM, CM and TIM IAs (topologies 1 - 4) are computed respectively as

For voltage mode:

$$A_{d\_1} = \frac{v_o}{v_{in1} - v_{in2}} = \left(1 + \frac{R_{3\_1}}{R_{4\_1}}\right)\left(1 + \frac{R_{2\_1}}{R_{1\_1}}\right) \tag{5.1}$$

For transadmittance mode:

$$A_{d\_2} = \frac{i_o}{v_{in1} - v_{in2}} = \frac{1}{R_{3\_2}}\left(1 + \frac{R_{2\_2}}{R_{1\_2}}\right) \tag{5.2}$$

For current mode:

$$A_{d\_3} = \frac{i_o}{i_{in1} - i_{in2}} = \left(1 + \frac{R_{3\_3}}{R_{4\_3}}\right)\left(1 + \frac{R_{2\_3}}{R_{1\_3}}\right) \tag{5.3}$$

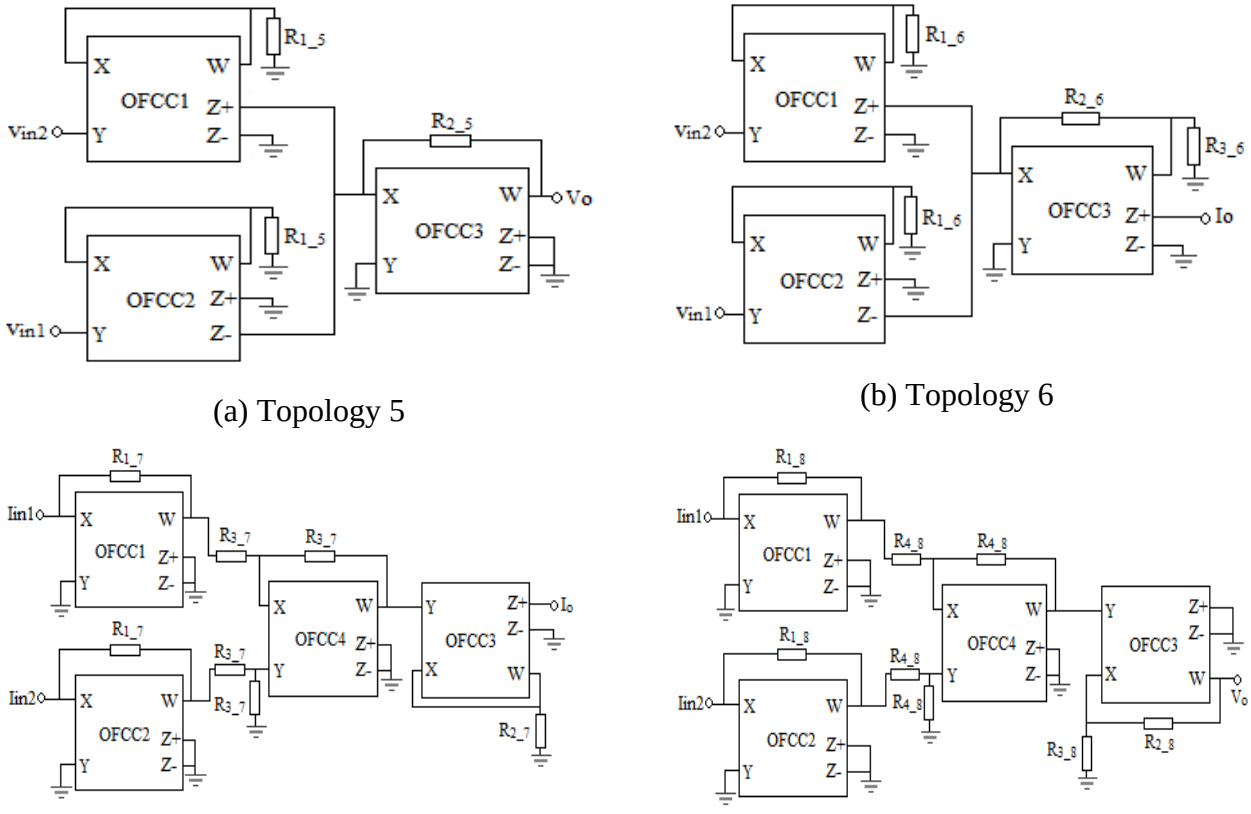
For transimpedance mode:

$$A_{d\_4} = \frac{v_o}{i_{in1} - i_{in2}} = R_{3\_4}\left(1 + \frac{R_{2\_4}}{R_{1\_4}}\right) \tag{5.4}$$

where A_{d_j} and R_{i_j} denote differential gain and i^{th} resistor of j^{th} topology (j=1,2,3,4) respectively.

5.3.3 IA topologies derived from Structure II

The first stage of Structure II is either a voltage to current or a current to voltage converter and is realized using method given in section 2.5. The second stage of Structure II are similar to that of



(a) Topology 5

(b) Topology 6

(c) Topology 7

(d) Topology 8

Fig 5.3 Proposed (a) VM (b) TAM (c) CM and (d) TIM IA topologies generated from Structure II

Structure I and can be designed in an identical manner. Various topologies resulted from Structure II are given in Fig 5.3.

The differential gains for VM, TAM, CM and TIM IAs derived from structure II (topologies 5 - 8) are given respectively as

For voltage mode:

$$A_{d\_5} = \frac{v_o}{v_{in1} - v_{in2}} = \left(\frac{R_{2\_5}}{R_{1\_5}} \right) \tag{5.5}$$

For transadmittance mode:

$$A_{d\_6} = \frac{i_o}{v_{in1} - v_{in2}} = \left(1 + \frac{R_{2\_6}}{R_{3\_6}} \right) \frac{1}{R_{1\_6}} \tag{5.6}$$

For current mode:

$$A_{d\_7} = \frac{i_o}{i_{in1} - i_{in2}} = \frac{R_{1\_7}}{R_{2\_7}} \tag{5.7}$$

For transimpedance mode:

$$A_{d\_8} = \frac{v_o}{i_{in1} - i_{in2}} = R_{1\_8} \left(1 + \frac{R_{2\_8}}{R_{3\_8}} \right) \tag{5.8}$$

where A_{d_j} and R_{i_j} denotes differential gain and i^{th} resistor of j^{th} topology (j = 5,6,7,8) respectively.

A comparison of corresponding VM, TAM, CM and TIM topologies of Figs. 5.2 and 5.3 reveal that:

- VM and TAM topologies derived from structure II (Fig. 5.1 (b)) employ lesser number of active and passive components than those obtained from structure I (Fig. 5.1 (a)).

- CM and TIM topologies derived from structure I (Fig. 5.1 (a)) employ fewer active and passive components than the topologies obtained from structure II (Fig. 5.1 (b)).

5.3.4 Non Ideal Analysis

The behavior of the proposed topologies may deviate from the ideal one due to nonidealities of OFCC which are discussed in section 2.3. The following sub sections describe the effect of these two nonidealities.

5.3.4.1 Effect of the finite transimpedance gain

A detailed analysis of IA of topology 4 is presented here. Keeping single pole model of transimpedance gain $Z_t(s)$ given in section 2.3.1 in view, the output voltage is computed as

$$v_{od\_4}\Big|_{fz} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)\left(i_{in1}\,\varepsilon_1(s) - i_{in2}\,\varepsilon_2(s)\right)\varepsilon_3(s) \tag{5.9}$$

$$v_{od\_4}\Big|_{fz} = \frac{R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)}{1+sC_{p3\_4}R_{3\_4}}\left(\frac{i_{in1}}{1+sC_{p1\_4}R_{2\_4}} - \frac{i_{in2}}{1+sC_{p2\_4}R_{2\_4}}\right) \tag{5.10}$$

where ε_i (i=1,2,3) represents error function for i^{th} OFCC and is given by

$$\varepsilon_i(s) = \frac{1}{1+sC_{pi\_4}R_{i\_4}} \tag{5.11}$$

Assuming $C_{p1\_4} = C_{p2\_4}$, the error functions $\varepsilon_1(s)$ and $\varepsilon_2(s)$ become equal and differential gain in presence of finite Z_t $\left(A_{d_4}\Big|_{fz}\right)$of the circuit of topology 4, is computed as

$$A_{d\_4}\Big|_{fz} = \frac{v_{od\_4}\Big|_{fz}}{i_{in1}-i_{in2}} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)\varepsilon_{uc}(s) \tag{5.12}$$

where $\varepsilon_{uc}(s) = \frac{1}{\left(1+sC_{p3\_4}R_{3\_4}\right)\left(1+sC_{p1\_4}R_{2\_4}\right)}$ (5.13)

and is uncompensated error function.

The frequency dependance of $A_{d\_4}\big|_{fz}$ comes from $\varepsilon_{uc}(s)$ which does not change with R_{1_4}. Therefore the gain may be adjusted by R_{1_4} without affecting the bandwidth.

Considering $i_{in1} = i_{in2} = i_{in}$ the transimpedance common mode gain in presence of finite Z_t ($A_{d\_4}|_{fz}$), is calculated as

$$A_{cm\_4}\big|_{fz} = \frac{v_{ocm\_4}\big|_{fz}}{i_{in}} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)\frac{s\left(C_{p2\_4}-C_{p1\_4}\right)R_{2\_4}}{1+sC_{p2\_4}R_{2\_4}}\varepsilon_{uc}(s) \tag{5.14}$$

Using (5.13) and (5.14), the common mode rejection ratio (CMRR) for this topology, is computed as

$$CMRR_{\_4}\big|_{fz} = \frac{A_{d\_4}\big|_{fz}}{A_{cm\_4}\big|_{fz}} = \frac{2+s\left(C_{p1\_4}+C_{p2\_4}\right)R_{2\_4}}{s(C_{p2\_4}-C_{p1\_4})R_{2\_4}} \tag{5.15}$$

Since $\left(C_{p1\_4} \approx C_{p2\_4}\right)$, a high value of CMRR may be achieved.

Similar analysis for other topologies is also carried out for sake of completeness and the corresponding expressions are given in Table 5.3.

5.3.4.2 Tracking errors

The effect of tracking errors given in section 2.3.2, is strongly topology dependent, e.g. the voltage tracking error does not affect the response if Y terminal of OFCC is grounded and the same is true for current tracking errors if Z+ or Z- terminals are not used.

Now considering the tracking errors, the detailed analysis of the topology 4 gives the output response as

$$v_{od\_4}\big|_{tr} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)\left(\alpha i_{in1}-\gamma i_{in2}\right) \tag{5.16}$$

For ideal OFCC, $\alpha = \gamma = 1$ so (5.16) modifies to

$$v_{od\_4}\Big|_{tr} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)\left(i_{in1}-i_{in2}\right) \tag{5.17}$$

The gain in differential mode ($A_{d\_4}\Big|_{tr}$), is computed as

$$A_{d\_4}\Big|_{tr} = \frac{v_{od\_4}\Big|_{tr}}{\left(i_{in1}-i_{in2}\right)} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right) \tag{5.18}$$

Assuming $i_{in1} = i_{in2} = i_{in}$ for common mode operation, the output voltage is calculated as

$$v_{ocm\_4}\Big|_{tr} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)(\alpha-\gamma)i_{in} \tag{5.19}$$

and common mode gain ($A_{cm\_4}\Big|_{tr}$) is computed as

$$A_{cm\_4}\Big|_{tr} = \frac{v_{ocm\_4}\Big|_{tr}}{i_{in}} = R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)(\alpha-\gamma) \tag{5.20}$$

Thus the CMRR in presence of voltage and current tracking errors becomes

$$CMRR_{\_4}\Big|_{tr} = \frac{A_{d\_4}\Big|_{tr}}{A_{cm\_4}\Big|_{tr}} = \frac{1}{(\alpha-\gamma)} \tag{5.21}$$

Similar analysis of other topologies is also carried out and the results are summarized in Table 5.4.

It may be observed from Tables 5.3 and 5.4 that differential gain of proposed topologies modify from the values given in (5.1) – (5.4). Further there is finite value of common mode gains of proposed topologies which are otherwise zero in ideal case. These modifications in differential and common mode gain lead to finite CMRR values. Further it may be noted that CMRR expressions for both type of nonidealities contain a difference term in denominator which is very small. Therefore a high value of CMRR may be achieved.

Table 5.3 Differential gain, common mode gain and CMRR with finite transimpedance gain (Z_t)

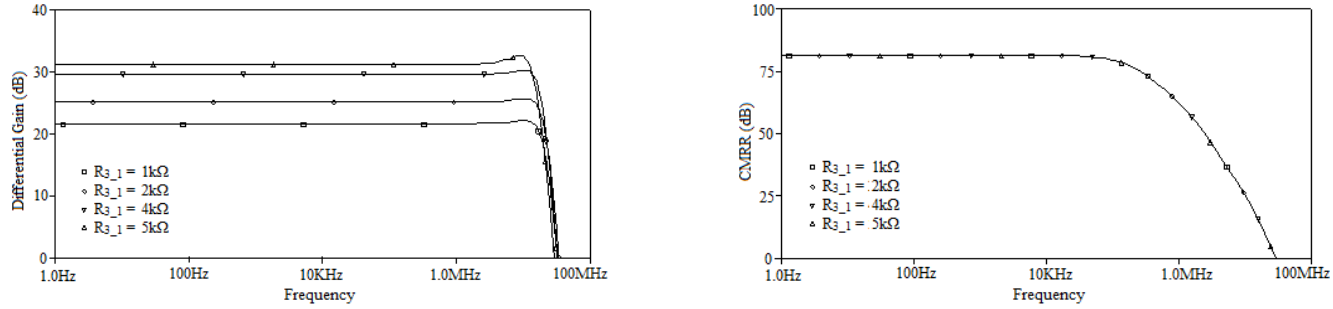
Topo-logy	Differential gain ($C_{p1}=C_{p2}$)	Common mode gain	CMRR
1	$\frac{\left(1+\frac{R_{3\_1}}{R_{4\_1}}\right)\left(1+\frac{R_{2\_1}}{R_{1\_1}}\right)}{(1+sC_{p3\_1}R_{3\_1})(1+sC_{p1\_1}R_{2\_1})(1+sC_{p4\_1}R_{5\_1})}$	$\frac{\left(1+\frac{R_{3\_1}}{R_{4\_1}}\right)\left(1+\frac{R_{2\_1}}{R_{1\_1}}\right)}{(1+sC_{p3\_1}R_{3\_1})(1+sC_{p4\_1}R_{5\_1})}\frac{s(C_{p2\_1}-C_{p1\_1})R_{2\_1}}{(1+sC_{p1\_1}R_{2\_1})(1+sC_{p2\_1}R_{2\_1})}$	$\frac{2+s(C_{p1\_1}+C_{p2\_1})R_{2\_1}}{s(C_{p2\_1}-C_{p1\_1})R_{2\_1}}$
2	$\frac{\left(\frac{1}{R_{3\_2}}\right)\left(1+\frac{R_{2\_2}}{R_{1\_2}}\right)}{(1+sC_{p3\_2}R_{3\_2})(1+sC_{p1\_2}R_{2\_2})(1+sC_{p4\_2}R_{4\_2})}$	$\frac{\left(\frac{1}{R_{3\_2}}\right)\left(1+\frac{R_{2\_2}}{R_{1\_2}}\right)}{(1+sC_{p3\_2}R_{3\_2})(1+sC_{p4\_2}R_{4\_2})}\frac{s(C_{p2\_2}-C_{p1\_2})R_{2\_2}}{(1+sC_{p1\_2}R_{2\_2})(1+sC_{p2\_2}R_{2\_2})}$	$\frac{2+s(C_{p1\_2}+C_{p2\_2})R_{2\_2}}{s(C_{p2\_2}-C_{p1\_2})R_{2\_2}}$
3	$\frac{\left(1+\frac{R_{3\_3}}{R_{4\_3}}\right)\left(1+\frac{R_{2\_3}}{R_{1\_3}}\right)}{(1+sC_{p3\_3}R_{3\_3})(1+sC_{p1\_3}R_{2\_3})}$	$\frac{\left(1+\frac{R_{3\_3}}{R_{4\_3}}\right)\left(1+\frac{R_{2\_3}}{R_{1\_3}}\right)}{(1+sC_{p3\_3}R_{3\_3})}\frac{s(C_{p2\_3}-C_{p1\_3})R_{2\_3}}{(1+sC_{p1\_3}R_{2\_3})(1+sC_{p2\_3}R_{2\_3})}$	$\frac{2+s(C_{p1\_3}+C_{p2\_3})R_{2\_3}}{s(C_{p2\_3}-C_{p1\_3})R_{2\_3}}$
4	$\frac{R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)}{(1+sC_{p3\_4}R_{3\_4})(1+sC_{p1\_4}R_{2\_4})}$	$\frac{R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)}{(1+sC_{p3\_4}R_{3\_4})}\frac{s(C_{p2\_4}-C_{p1\_4})R_{2\_4}}{(1+sC_{p1\_4}R_{2\_4})(1+sC_{p2\_4}R_{2\_4})}$	$\frac{2+s(C_{p1\_4}+C_{p2\_4})R_{2\_4}}{s(C_{p2\_4}-C_{p1\_4})R_{2\_4}}$
5	$\frac{R_{2\_5}}{R_{1\_5}(1+sC_{p3\_5}R_{2\_5})(1+sC_{p1\_5}R_{1\_5})}$	$\frac{R_{2\_5}}{R_{1\_5}(1+sC_{p3\_5}R_{2\_5})}\frac{s(C_{p2\_5}-C_{p1\_5})R_{1\_5}}{(1+sC_{p1\_5}R_{1\_5})(1+sC_{p2\_5}R_{1\_5})}$	$\frac{2+s(C_{p1\_5}+C_{p2\_5})R_{1\_5}}{s(C_{p2\_5}-C_{p1\_5})R_{1\_5}}$
6	$\frac{\left(\frac{1}{R_{1\_6}}\right)\left(1+\frac{R_{2\_6}}{R_{3\_6}}\right)}{(1+sC_{p3\_6}R_{2\_6})(1+sC_{p1\_6}R_{1\_6})}$	$\frac{\left(\frac{1}{R_{1\_6}}\right)\left(1+\frac{R_{2\_6}}{R_{3\_6}}\right)}{(1+sC_{p3\_6}R_{2\_6})}\frac{s(C_{p2\_6}-C_{p1\_6})R_{1\_6}}{(1+sC_{p1\_6}R_{1\_6})(1+sC_{p2\_6}R_{1\_6})}$	$\frac{2+s(C_{p1\_6}+C_{p2\_6})R_{1\_6}}{s(C_{p2\_6}-C_{p1\_6})R_{1\_6}}$
7	$\frac{\left(\frac{R_{1\_7}}{R_{2\_7}}\right)}{(1+sC_{p3\_7}R_{2\_7})(1+sC_{p1\_7}R_{1\_7})(1+sC_{p4\_7}R_{3\_7})}$	$\frac{\left(\frac{R_{1\_7}}{R_{2\_7}}\right)}{(1+sC_{p3\_7}R_{2\_7})(1+sC_{p4\_7}R_{3\_7})}\frac{s(C_{p2\_7}-C_{p1\_7})R_{1\_7}}{(1+sC_{p1\_7}R_{1\_7})(1+sC_{p2\_7}R_{1\_7})}$	$\frac{2+s(C_{p1\_7}+C_{p2\_7})R_{1\_7}}{s(C_{p2\_7}-C_{p1\_7})R_{1\_7}}$
8	$\frac{R_{1\_8}\left(1+\frac{R_{2\_8}}{R_{3\_8}}\right)}{(1+sC_{p3\_8}R_{2\_8})(1+sC_{p1\_8}R_{1\_8})(1+sC_{p4\_8}R_{4\_8})}$	$\frac{R_{1\_8}\left(1+\frac{R_{2\_8}}{R_{3\_8}}\right)}{(1+sC_{p3\_8}R_{2\_8})(1+sC_{p4\_8}R_{4\_8})}\frac{s(C_{p2\_8}-C_{p1\_8})R_{1\_8}}{(1+sC_{p1\_8}R_{1\_8})(1+sC_{p2\_8}R_{1\_8})}$	$\frac{2+s(C_{p1\_8}+C_{p2\_8})R_{1\_8}}{s(C_{p2\_8}-C_{p1\_8})R_{1\_8}}$

Table 5.4 Differential gain, common mode gain and CMRR with tracking errors

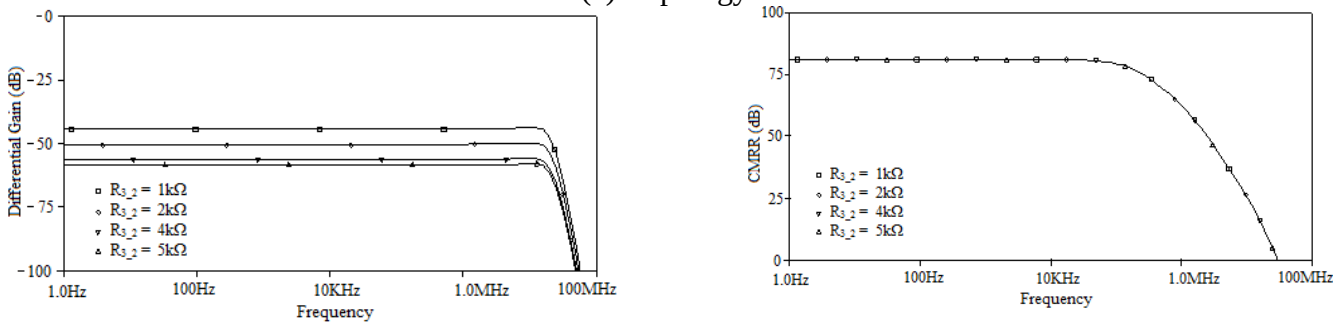
Topology	Differential gain	Common mode gain	CMRR
1	$\left(1+\frac{R_{3\_1}}{R_{4\_1}}\right)\left(1+\frac{R_{2\_1}}{R_{1\_1}}\right)$	$\left(1+\frac{R_{3\_1}}{R_{4\_1}}\right)\left(1+\frac{R_{2\_1}}{R_{1\_1}}\right)\beta(1-\beta)$	$\frac{1}{\beta(1-\beta)}$
2	$\left(\frac{1}{R_{3\_2}}\right)\left(1+\frac{R_{2\_2}}{R_{1\_2}}\right)$	$\left(\frac{1}{R_{3\_2}}\right)\left(1+\frac{R_{2\_2}}{R_{1\_2}}\right)\alpha\beta\ (1-\beta)$	$\frac{1}{\alpha\beta(1-\beta)}$
3	$\left(1+\frac{R_{3\_3}}{R_{4\_3}}\right)\left(1+\frac{R_{2\_3}}{R_{1\_3}}\right)$	$\left(1+\frac{R_{3\_3}}{R_{4\_3}}\right)\left(1+\frac{R_{2\_3}}{R_{1\_3}}\right)\alpha(\alpha-\gamma)$	$\frac{1}{\alpha(\alpha-\gamma)}$
4	$R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)$	$R_{3\_4}\left(1+\frac{R_{2\_4}}{R_{1\_4}}\right)(\alpha-\gamma)$	$\frac{1}{(\alpha-\gamma)}$
5	$\left(\frac{R_{2\_5}}{R_{1\_5}}\right)$	$\left(\frac{R_{2\_5}}{R_{1\_5}}\right)\beta(\alpha-\gamma)$	$\frac{1}{\beta(\alpha-\gamma)}$
6	$\left(1+\frac{R_{2\_6}}{R_{3\_6}}\right)\frac{1}{R_{1\_6}}$	$\left(1+\frac{R_{2\_6}}{R_{3\_6}}\right)\frac{1}{R_{1\_6}}\alpha\beta(\alpha-\gamma)$	$\frac{1}{\alpha\beta(\alpha-\gamma)}$
7	$\left(\frac{R_{1\_7}}{R_{2\_7}}\right)$	$\left(\frac{R_{1\_7}}{R_{2\_7}}\right)\alpha\ (1-\beta)$	$\frac{1}{\alpha(1-\beta)}$
8	$R_{1\_8}\left(1+\frac{R_{2\_8}}{R_{3\_8}}\right)$	$R_{1\_8}\left(1+\frac{R_{2\_8}}{R_{3\_8}}\right)(1-\beta)$	$\frac{1}{(1-\beta)}$

5.3.5 Simulation Results

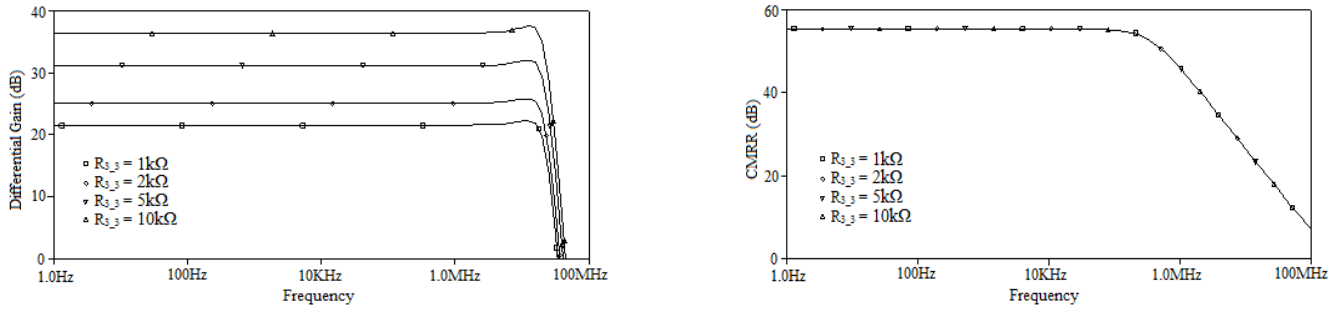
The behavior of proposed topologies is verified through SPICE simulations using CMOS based implementation of OFCC [13] as given in Fig. 2.3. The differential gain and CMRR of topologies derived from Structure I and Structure II are examined by varying R_{3_j} (j = 1,2,3,4) and R_{2_k} (k = 5,6,7,8). The values of various resistors are placed in Table 5.5. For topologies 1,2,5,6 an input of 5 mV is applied and in rest of topologies the input current is 1 µA. The simulated frequency responses for differential gain and CMRR for all derived topologies from Structure I and II are given in Figs. 5.4 and 5.5 respectively. The values of differential gain, CMRR and bandwidth of CMRR is noted for Figs. 5.4 and 5.5 and are placed in Table 5.5.



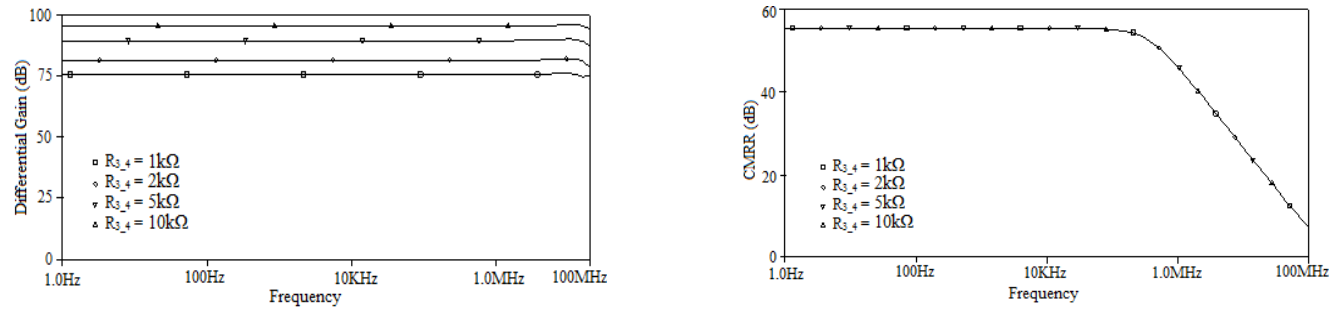
(a) Topology 1



(b) Topology 2

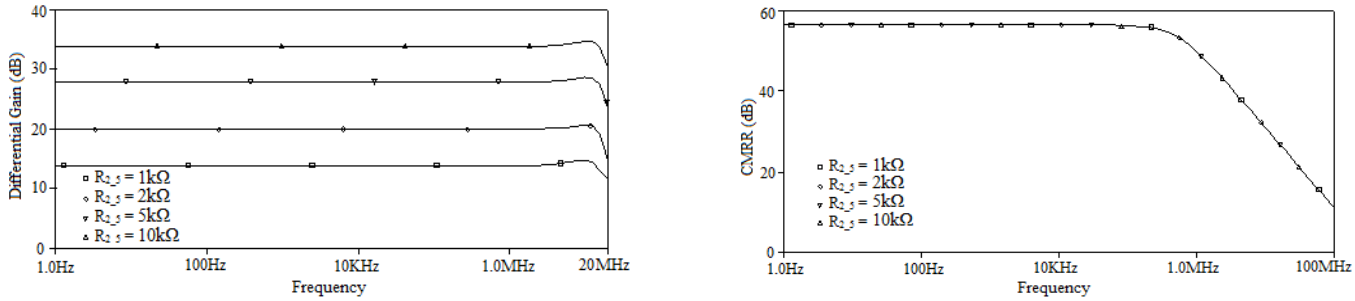


(c) Topology 3

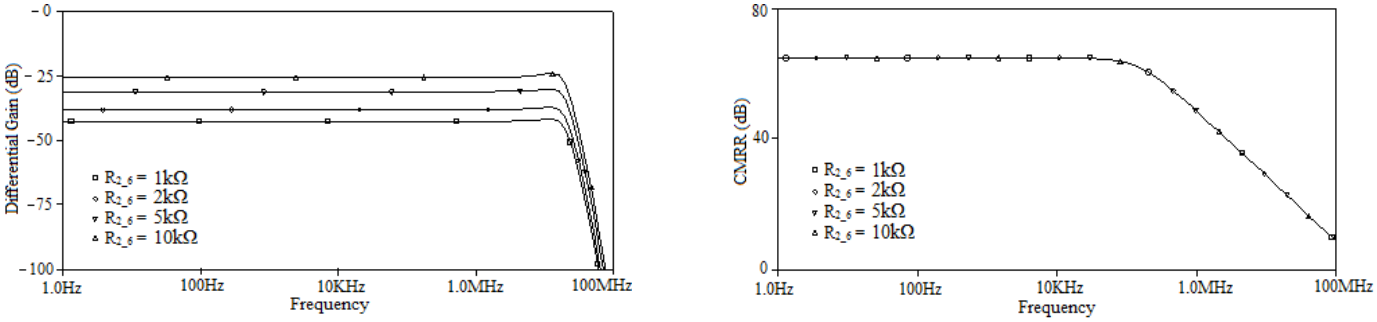


(d) Topology 4

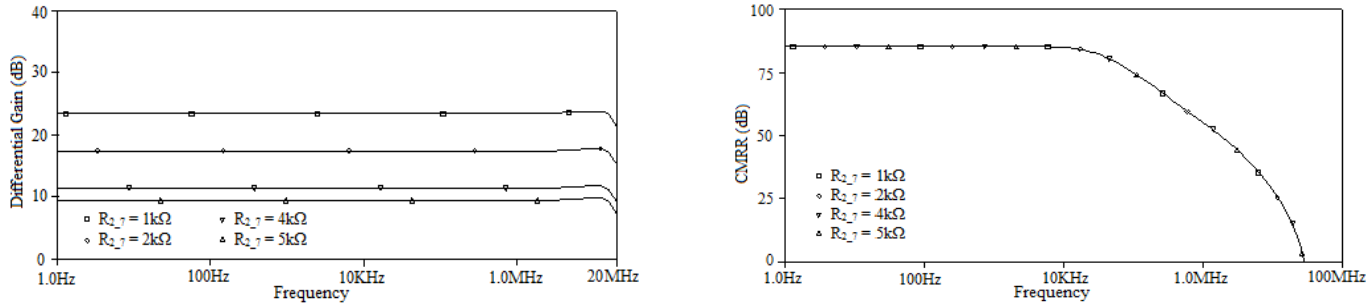
Fig. 5.4 Simulated frequency responses for differential gain and CMRR for (a) topology 1 (b) topology 2 (c) topology 3 (d) topology 4



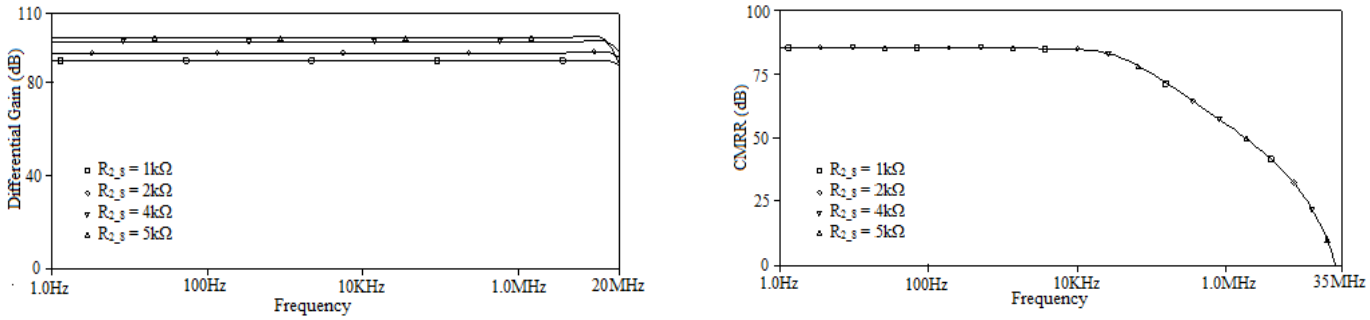
(a) Topology 5



(b) Topology 6



(c) Topology 7



(d) Topology 8

Fig. 5.5 Simulated frequency responses for differential gain and CMRR for (a) topology 5 (b) topology 6 (c) topology 7 (d) topology 8

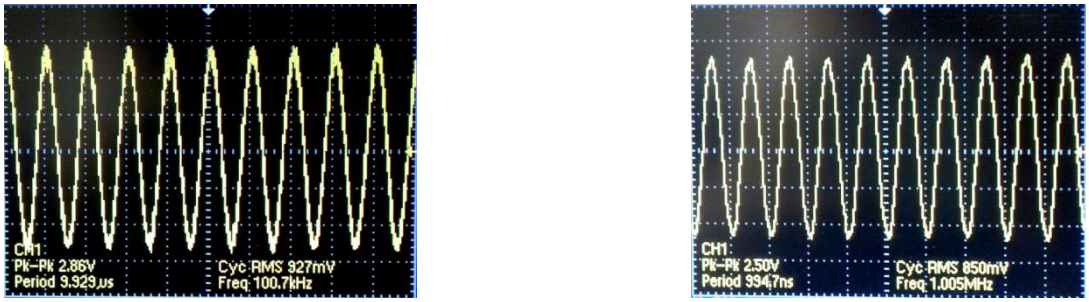
The simulated results verify the functionality of all proposed topologies. It may be noted from Figs. 5.4 and 5.5 that CMRR value is independent of gain.

Table 5.5 Summary of simulation results for IA topologies 1-8

Topology	**Resistor values (kΩ)**		**Differential mode gain (dB)**	**CMRR (dB)**	**CMRR BW (KHz)**
	Fixed resistance	**Variable resistance**			
1	R_{1_1}= 1, R_{2_1}= 5, R_{4_1}= 1, R_{5_1}= 20	R_{3_1} = 1	21	81	148
		R_{3_1} = 2	25		
		R_{3_1} = 4	29		
		R_{3_1} = 5	31		
2	R_{1_2}= 1, R_{2_2}= 5, R_{4_2}= 20	R_{3_2} = 1	-44	81	148
		R_{3_2} = 2	-50		
		R_{3_2} = 4	-56		
		R_{3_2} = 5	-58		
3	R_{1_3}= 1, R_{2_3}= 5, R_{4_3}= 1	R_{3_3} = 1	21	55	349
		R_{3_3} = 2	25		
		R_{3_3} = 5	31		
		R_{3_3} = 10	36		
4	R_{1_4}= 1, R_{2_4}= 5	R_{3_4} = 1	75	55	352
		R_{3_4} = 2	81		
		R_{3_4} = 5	89		
		R_{3_4} = 10	95		
5	R_{1_5}= 0.2	R_{2_5} = 1	14	56	525
		R_{2_5} = 2	20		
		R_{2_5} = 5	28		
		R_{2_5} = 10	34		
6	R_{1_6}= 0.4, R_{3_6}= 0.5	R_{2_6} = 1	-42	64	153
		R_{2_6} = 2	-38		
		R_{2_6} = 5	-31		
		R_{2_6} = 10	-25		
7	R_{1_7}= 15, R_{3_7}= 20	R_{2_7} = 1	23	85	32
		R_{2_7} = 2	17		
		R_{2_7} = 4	11		
		R_{2_7} = 5	9		
8	R_{1_8}= 15, R_{3_8}= 1, R_{4_8}= 20	R_{2_8} = 1	89	85	32
		R_{2_8} = 2	93		
		R_{2_8} = 4	97		
		R_{2_8} = 5	99		

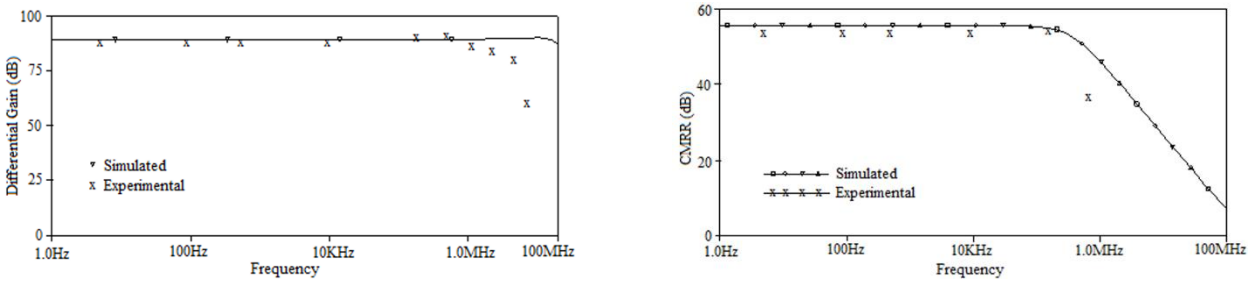
5.3.6 Experimental Results

The proposed TIM IA circuit of Fig. 5.2(d) is also tested experimentally using AD844 [170] based OFCC implementation as shown in Fig. 2.5 (b) with supply voltages of ± 5V. The passive component values for R_{1_4}, R_{2_4}, and R_{3_4} are taken as 1kΩ, 5kΩ and 5kΩ respectively with component tolerance of 5%. The observed output waveforms of the proposed TIM IA at 100 KHz and 1 MHz inputs are depicted in Fig. 5.6(a) and (b) respectively. The functionality of the AD844 based realization is also verified through SPICE simulation for fair comparison. Figure 5.7 shows the simulated and experimental frequency responses for differential gain and CMRR. Slight variation in experimental and simulated results may be attributed to device tracking errors and component tolerances.



(a) (b)

Fig. 5.6 Observed output responses for input frequencies (a) 100 KHz (b) 1 MHz



(a) (b)

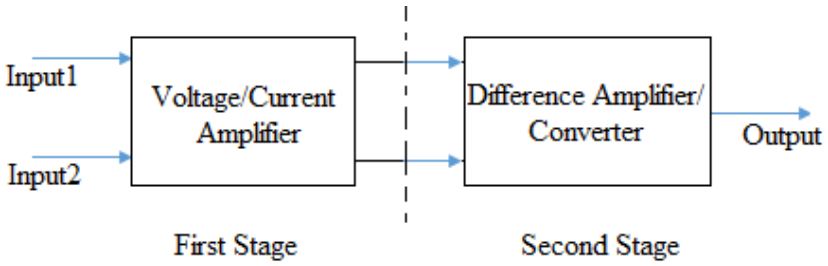
Fig. 5.7 Simulated and experimental frequency responses for (a) differential gain and (b) CMRR

5.4 OFCC BASED IA TOPOLOGIES WITH REDUCED COMPONENT COUNT

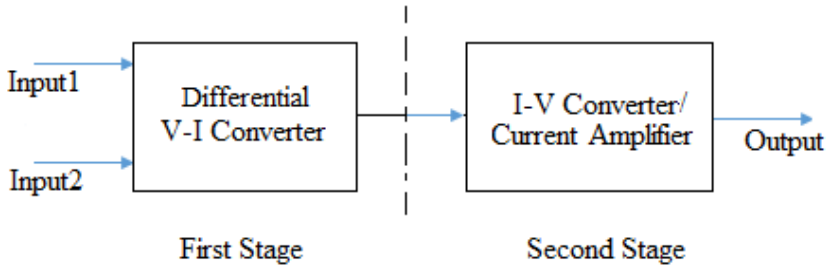
Topologies 1-8 provides independent processing of input signals i.e. inputs are applied to different OFCCs configured as either voltage/current amplifier or voltage to current/current to voltage converter. There is another possibility of sharing of passive component in first stage which may lead to IA topology with fewer passive components. Taking these modifications into consideration the generalized IA structures I and II are modified to Fig. 5.8 (a) and (b) respectively.

5.4.1 IA topologies derived from modified Structure I

The IA topologies derived from modified Structure I are given in Fig. 5.9. The OFCC1 and OFCC2 form voltage amplifiers in topologies 9 and 10 and current amplifiers in topologies 11 and 12. The OFCC3 performs the desired amplification or conversion function for all topologies except topology 9 where OFCC3 performs as a voltage difference amplifier. OFCC4 performs voltage differencing only as required for topologies 10.

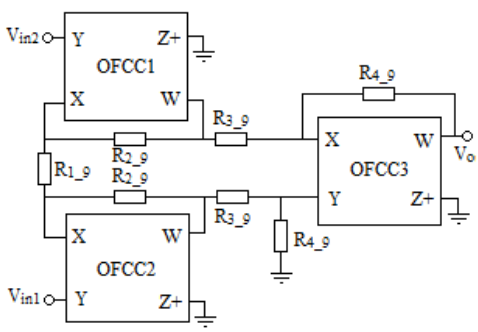


(a)

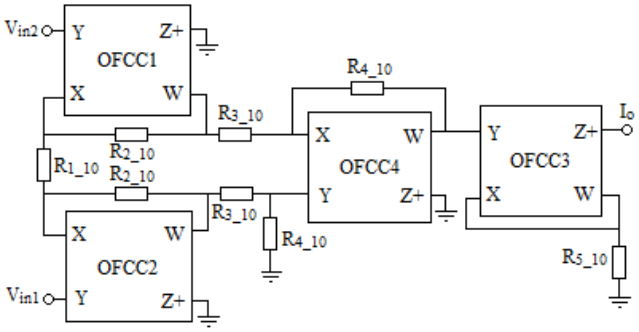


(b)

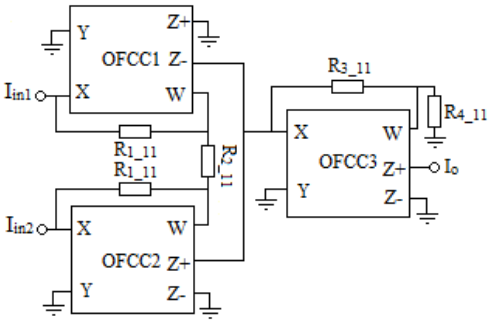
Fig. 5.8 Generalized block diagram of IAs (a) modified Structure I (b) modified Structure II



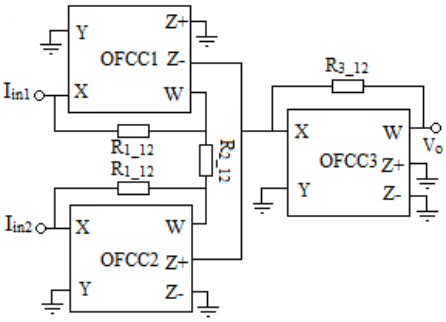
(a) Topology 9



(b) Topology 10



(c) Topology 11



(d) Topology 12

Fig. 5.9 Proposed (a) VM (b) TAM (c) CM and (d) TIM IA topologies generated from Structure I

The differential gains of VM, TAM, CM and TIM IAs (topologies 9 - 12) are computed respectively as

For voltage mode:

$$A_{d\_9} = \frac{v_o}{v_{in1} - v_{in2}} = \left(\frac{R_{4\_9}}{R_{3\_9}}\right)\left(1 + \frac{2R_{2\_9}}{R_{1\_9}}\right) \tag{5.22}$$

For transadmittance mode:

$$A_{d\_10} = \frac{i_o}{v_{in1} - v_{in2}} = \frac{R_{4\_10}}{R_{3\_10}\, R_{5\_10}}\left(1 + \frac{2R_{2\_10}}{R_{1\_10}}\right) \tag{5.23}$$

For current mode:

$$A_{d\_11} = \frac{i_o}{i_{in1} - i_{in2}} = \left(1 + \frac{R_{3\_11}}{R_{4\_11}}\right)\left(1 + \frac{4R_{1\_11}}{R_{2\_11}}\right) \tag{5.24}$$

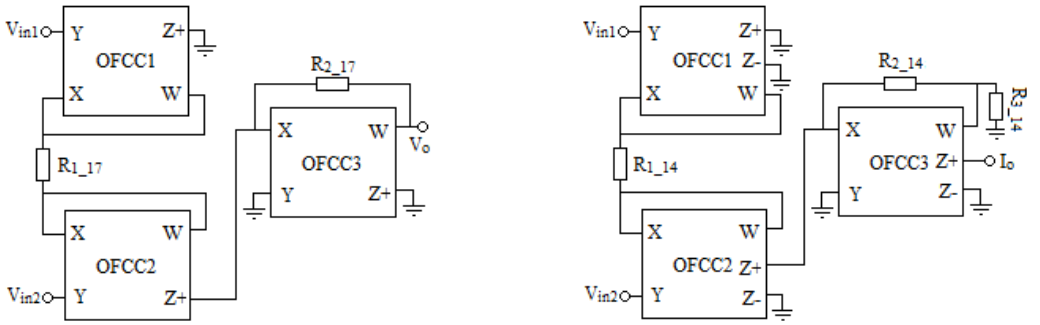
For transimpedance mode:

$$A_{d\_12} = \frac{v_o}{i_{in1} - i_{in2}} = R_{3\_12}\left(1 + \frac{2R_{1\_12}}{R_{2\_12}}\right) \tag{5.25}$$

where A_{d_j} and R_{i_j} denote differential gain and i^{th} resistor of j^{th} topology (j=1,2,3,4) respectively.

5.4.2 IA topologies derived from modified Structure II

The first stage of modified structure II is a differential voltage to current converter while second stage is either a current to voltage converter or a current amplifier. The IA topologies derived from modified Structure II are depicted in Fig. 5.10. Both topologies use a differential voltage to current converter which is followed by current to voltage converter (topology 13) or a current amplifier (topology 14). Topologies 13 and 14 fall under VM and TAM category and corresponding differential gains are obtained as



(a) Topology 13 (b) Topology 14

Fig. 5.10 Proposed (a) VM (b) TAM IA topologies generated from Structure II

For voltage mode:

$$A_{d\_13} = \frac{v_o}{v_{in1} - v_{in2}} = \frac{1}{2}\left(\frac{R_{2\_13}}{R_{1\_13}}\right) \tag{5.26}$$

For transadmittance mode:

$$A_{d\_14} = \frac{i_o}{v_{in1} - v_{in2}} = \left(1 + \frac{R_{2\_14}}{R_{3\_14}}\right)\frac{1}{2R_{1\_14}} \tag{5.27}$$

A comparison of all proposed VM, TAM, CM and TIM IA topologies of Figs. 5.2, 5.3, 5.9 and 5.10 reveal that minimum number of active and passive components are used in:

- VM and TAM IA topologies 13 and 14 respectively.
- CM and TIM IA topologies 11 and 12 respectively.

5.4.3 Non Ideal Analysis

The behaviour of the proposed topologies is also examined in presence of nonidealities of OFCC (section 2.3). The effect of finite Z_t and tracking errors on porposed IA topologies for differential gain, common mode gain and CMRR is analyzed and corresponding expressions are derived and are placed in Tables 5.6 – 5.8.

Table 5.6 Differential gain, common mode gain and CMRR with finite transimpedance gain (Z_t)

Topo-logy	Differential gain (with $C_{p1}=C_{p2}$)	Common mode gain	CMRR
9	$\frac{\left(\frac{R_{4\_9}}{R_{3\_9}}\right)\left(1+\frac{2R_{2\_9}}{R_{1\_9}}\right)}{(1+sC_{p1\_9}R_{2\_9})(1+sC_{p3\_9}R_{4\_9})}$	$\frac{\left(\frac{R_{4\_9}}{R_{3\_9}}\right)\left(1+\frac{2R_{2\_9}}{R_{1\_9}}\right)}{(1+sC_{p3\_9}R_{4\_9})}\frac{s\left(C_{p1\_9}-C_{p2\_9}\right)R_{2\_9}}{(1+sC_{p2\_9}R_{2\_9})(1+sC_{p1\_9}R_{2\_9})}$	$\left(\frac{2+s\left(C_{p1\_9}-C_{p2\_9}\right)R_{2\_9}}{s\left(C_{p2\_9}-C_{p1\_9}\right)R_{2\_9}}\right)$
10	$\frac{\left(\frac{R_{4\_10}}{R_{3\_10}R_{5\_10}}\right)\left(1+\frac{2R_{2\_10}}{R_{1\_10}}\right)}{(1+sC_{p1\_10}R_{2\_10})(1+sC_{p3\_10}R_{4\_10})(1+sC_{p4\_10}R_{5\_10})}$	$\frac{\left(\frac{R_{4\_10}}{R_{3\_10}R_{5\_10}}\right)\left(1+\frac{2R_{2\_10}}{R_{1\_10}}\right)}{(1+sC_{p3}R_{4\_10})}\frac{s\left(C_{p1\_10}-C_{p2\_10}\right)R_{2\_10}}{(1+sC_{p2\_10}R_{2\_10})(1+sC_{p1\_10}R_{2\_10})}$	$\left(\frac{2+s\left(C_{p1\_10}-C_{p2\_10}\right)R_{2\_10}}{s\left(C_{p2\_10}-C_{p1\_10}\right)R_{2\_10}}\right)$
11	$\frac{\left(1+\frac{R_{3\_11}}{R_{4\_11}}\right)\left(1+\frac{2R_{1\_11}}{R_{2\_11}}\right)}{(1+sC_{p1\_11}R_{1\_11})(1+sC_{p3\_11}R_{3\_11})}$	$\frac{sR_{1\_11}\left(1+\frac{R_{3\_11}}{R_{4\_11}}\right)\left(C_{p1\_11}-C_{p2\_11}\right)}{(1+sC_{p1\_11}R_{1\_11})(1+sC_{p2\_11}R_{1\_11})(1+sC_{p3\_11}R_{3\_11})}$	$\left(\frac{2+sR_{1\_11}\left(C_{p1\_11}+C_{p2\_11}\right)}{s\left(C_{p2\_11}-C_{p1\_11}\right)R_{2\_11}}\right)\left(1+\frac{R_{2\_11}}{2R_{1\_11}}\right)$
12	$\frac{R_{3\_12}\left(1+\frac{2R_{1\_12}}{R_{2\_12}}\right)}{(1+sC_{p3\_12}R_{3\_12})(1+sC_{p1\_12}R_{1\_12})}$	$\frac{sR_{1\_12}R_{3\_12}(C_{p1\_12}-C_{p2\_12})}{(1+sC_{p1\_12}R_{1\_12})(1+sC_{p2\_12}R_{1\_12})(1+sC_{p3\_12}R_{3\_12})}$	$\left(\frac{2+sR_{1\_12}(C_{p1\_12}+C_{p2\_12})}{s(C_{p2\_12}-C_{p1\_12})R_{2\_12}}\right)\left(1+\frac{R_{2\_12}}{2R_{1\_12}}\right)$

Table 5.7 Differential gain, common mode gain and CMRR with tracking errors

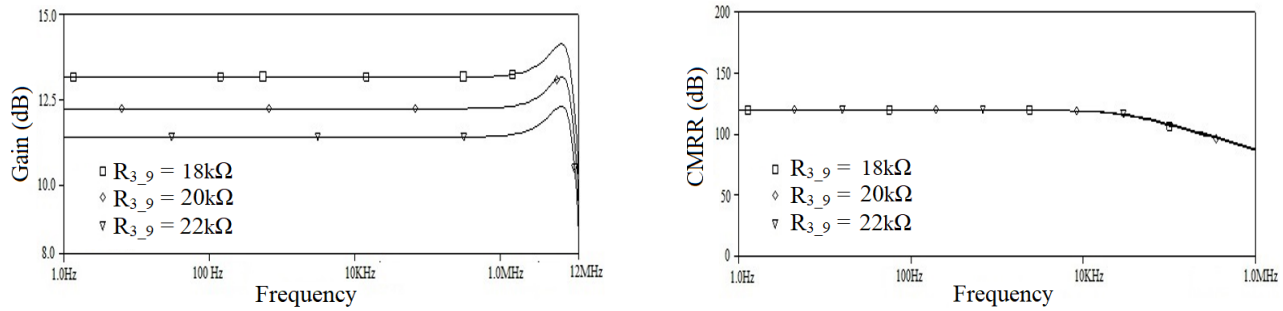
Topo-logy	Differential gain	Common mode gain	CMRR
9	$\frac{R_{4\_9}}{R_{3\_9}}\left(1+\frac{2R_{2\_9}}{R_{1\_9}}\right)$	$\frac{R_{4\_9}}{R_{3\_9}}\left\{\left(\frac{R_{2\_9}}{R_{1\_9}}+1\right)(\beta_2\beta_3-\beta_1)+\frac{R_{2\_9}}{R_{1\_9}}(\beta_2-\beta_1\beta_3)\right\}$	$\frac{\left(1+\frac{R_{2\_9}}{R_{1\_9}}\right)(\beta_3\beta_2+\beta_1)+\frac{R_{2\_9}}{R_{1\_9}}(\beta_3\beta_1+\beta_2)}{\left(1+\frac{R_{2\_9}}{R_{1\_9}}\right)(\beta_3\beta_2-\beta_1)+\frac{R_{2\_9}}{R_{1\_9}}(\beta_2-\beta_3\beta_1)}$
10	$\frac{R_{4\_10}}{R_{5\_10}R_{3\_10}}\left(1+\frac{2R_{2\_10}}{R_{1\_10}}\right)$	$\frac{\alpha_3\beta_3R_{4\_10}}{R_{5\_10}R_{3\_10}}\left\{\left(1+\frac{R_{2\_10}}{R_{1\_10}}\right)(\beta_2\beta_4-\beta_1)+\frac{R_{2\_10}}{R_{1\_10}}(\beta_2-\beta_1\beta_4)\right\}$	$\frac{\left(1+\frac{R_{2\_10}}{R_{1\_10}}\right)(\beta_4\beta_2+\beta_1)+\frac{R_{2\_10}}{R_{1\_10}}(\beta_4\beta_1+\beta_2)}{\left(1+\frac{R_{2\_10}}{R_{1\_10}}\right)(\beta_4\beta_2-\beta_1)+\frac{R_{2\_10}}{R_{1\_10}}(\beta_2-\beta_4\beta_1)}$
11	$\left(1+\frac{R_{3\_11}}{R_{4\_11}}\right)\left(1+\frac{4R_{1\_11}}{R_{2\_11}}\right)$	$\left(1+\frac{R_{3\_11}}{R_{4\_11}}\right)(\alpha-\gamma)$	$\frac{1}{(\alpha-\gamma)}\left(1+\frac{4R_{1\_11}}{R_{2\_11}}\right)$
12	$\left(1+\frac{2R_{1\_12}}{R_{2\_12}}\right)R_{3\_12}$	$(\alpha-\gamma)R_{3\_12}$	$\frac{1}{\alpha-\gamma}\left(1+\frac{2R_{1\_12}}{R_{2\_12}}\right)$

Table 5.8 Differential gain, common mode gain and CMRR with finite transimpedance gain (Z_t) and tracking errors

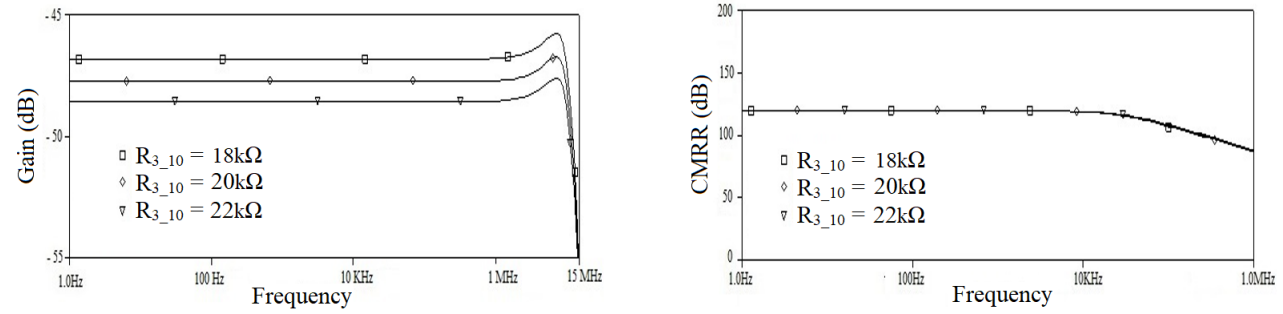
Topo-logy	Differential gain (with $C_{p1}=C_{p2}$)	Common mode gain	CMRR
13	$\frac{1}{2}\frac{R_{2\_13}}{R_{1\_13}}\frac{\alpha(\beta_1+\beta_2)}{(1+sC_{p2\_13}R_{1\_13})(1+sC_{p3\_13}R_{2\_13})}$	$\frac{R_{2\_13}}{R_{1\_13}}\frac{\alpha(\beta_1-\beta_2)}{(1+sC_{p2\_13}R_{1\_13})(1+sC_{p3\_13}R_{2\_13})}$	$\frac{(\beta_1+\beta_2)}{2(\beta_1-\beta_2)}$
14	$\frac{1}{2R_{1\_14}}\left(1+\frac{R_{2\_14}}{R_{3\_14}}\right)\frac{\alpha_2\alpha_3(\beta_1+\beta_2)}{(1+sC_{p2\_14}R_{1\_14})(1+sC_{p3\_14}R_{2\_14})}$	$\frac{1}{R_{1\_14}}\left(1+\frac{R_{2\_14}}{R_{3\_14}}\right)\frac{\alpha_2\alpha_3(\beta_1-\beta_2)}{(1+sC_{p2\_14}R_{1\_14})(1+sC_{p3\_14}R_{2\_14})}$	$\frac{(\beta_1+\beta_2)}{2(\beta_1-\beta_2)}$

5.4.4 Simulation Results

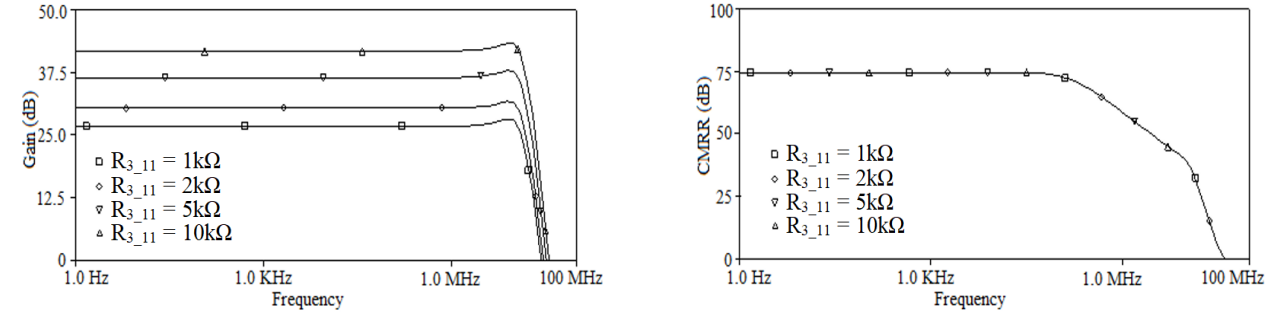
The behavior of proposed topologies is verified through SPICE simulations using CMOS based imple-



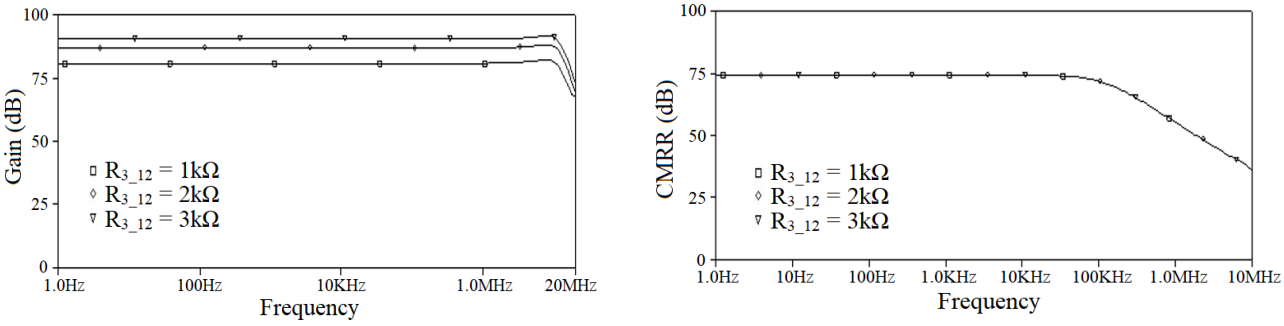
(a) Topology 9



(b) Topology 10



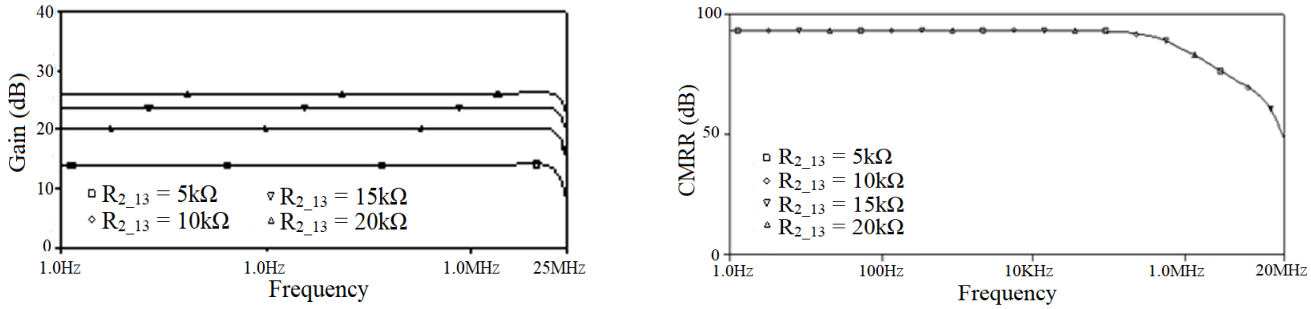
(c) Topology 11



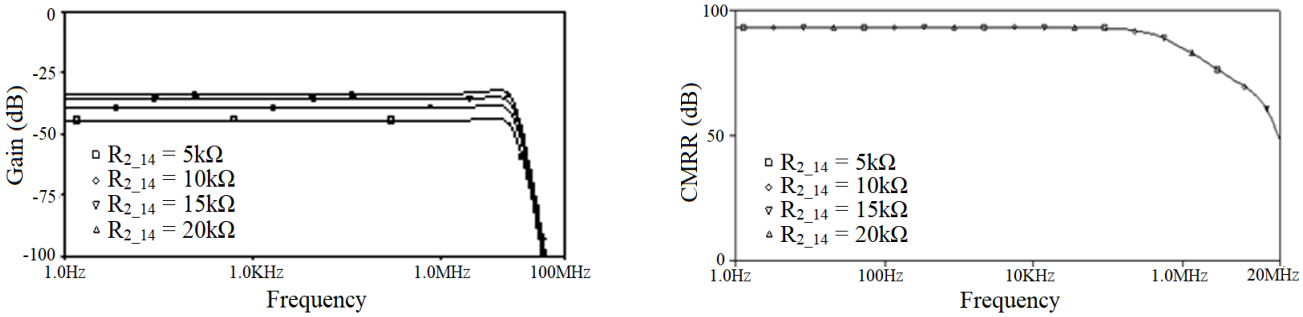
(d) Topology 12

Fig. 5.11 Simulated frequency responses for differential gain and CMRR for (a) topology 9 (b) topology 10 (c) topology 11 (d) topology 12.

mentation of OFCC [13] as given in Fig. 2.3. The differential gain and CMRR of topologies derived from Structure I and Structure II are examined by varying R_{3_j} (j = 9,10,11,12) and R_{2_k} (k = 13,14) respectively. For topologies 9,10,13,14 an input of 5 mV is applied and in rest of topologies the input current is 1 µA. The values of various resistors are placed in Table 5.9. The simulated frequency responses for differential gain and CMRR for all derived topologies from Structure I and II are given in Figs. 5.11 and 5.12 respectively.



(a) Topology 13



(b) Topology 14

Fig. 5.12 Simulated frequency responses for differential gain and CMRR for (a) topology 13 (b) topology 14

The values of differential gain, CMRR and bandwidth of CMRR is noted for Figs. 5.11 and 5.12 and are placed in Table 5.9. The simulated results verify the functionality of all the proposed topologies. It may be noted from Figs. 5.11and 5.12 that CMRR value is independent of gain.

5.5 PERFORMANCE COMPARISON

This section puts forward the comparison of performance parameters such as differential gain (dB) and its -3dB frequency, CMRR (dB) and its -3dB frequency, power supply used and power consumption. The data is also collected about inclusion of experimental results. Table 5.10 enlist all these observations for available IAs and proposed IAs. As the IAs given in [14, 96-119] and the proposed ones have been tested for different differential gains and at different power supply voltages, it is not fair to compare these on the basis of gain and power consumption.

Following are the observations for CMRR, its bandwidth and gain bandwidth product (GBP):

- The proposed VM topology 5 has highest CMRR bandwidth though it has lower CMRR than corresponding VM IAs given in [14, 96, 97, 100-104, 107-112, 114, 119] and that for proposed topology 1, 9 and 13. The proposed VM topology 13 has highest CMRR GBP among all.
- The proposed TAM topology 14 has highest CMRR bandwidth and CMRR GBP.
- The CM IA of [115] gives highest CMRR and the CMRR bandwidth and GBP of this is not available for comparison. Among the proposed CM topologies, the proposed topology 3 outperforms in terms of CMRR bandwidth and gain bandwidth product GBP
- The TIM IA in [96] has best CMRR. As the data for CMRR bandwidth and CMRR GBP is not available for this topology, the results given for the proposed topology 4 are best among those listed in the Table 5.10.

Table 5.9 Summary of simulation results for new IA topologies 9-14

Topology	Resistor values (kΩ)		Differential mode gain (dB)	CMRR (dB)	CMRR BW (KHz)
	Fixed resistance	Variable resistance			
9	R_{1_9}= 1, R_{2_9}= 20, R_{4_9}= 2	R_{3_9} = 18	13	120	28
		R_{3_9} = 20	12		
		R_{3_9} = 22	11		
10	R_{1_10}= 1, R_{2_10}= 20, R_{4_10}= 2, R_{5_10}= 1	R_{3_10} = 18	-46	120	28
		R_{3_10} = 20	-47		
		R_{3_10} = 22	-48		
11	R_{1_11}= 5, R_{2_11}= 1, R_{4_11}= 1	R_{3_11} = 1	26	74.4	165
		R_{3_11} = 2	30		
		R_{3_11} = 5	36		
		R_{3_11} = 10	41		
12	R_{1_12}= 5, R_{2_12}= 1	R_{3_12} = 1	80	74.4	112
		R_{3_12} = 2	86		
		R_{3_12} = 3	90		
13	R_{1_13}= 1	R_{2_13} = 5	14	93	423
		R_{2_13} = 10	20		
		R_{2_13} = 15	23		
		R_{2_13} = 20	26		
14	R_{1_14}= 1, R_{3_14}= 1	R_{2_14} = 5	-44	93	423
		R_{2_14} = 10	-39		
		R_{2_14} = 15	-35		
		R_{2_14} = 20	-33		

Table 5.10 Comparison of performance parameters of available and proposed IAs

Ref. No.	Mode	Differential gain (dB)	- 3dB freq. (diff. gain)	CMRR (dB)	- 3dB freq. (CMRR)	Power supply (V)	Power consumption (max.) (mWatt)	Experimental results available
[14]	VM	40,20,4,2	1.2 MHz	76	185KHz	NA	NA	Yes
[96]	VM	10,20,30,40	1.5-2.3 MHz	100	NA	NA	NA	Yes
[96]	TIM	10,20,30,40	1.5-2.3 MHz	100	NA	NA	NA	Yes
[97]	VM	N.A.	NA	70-90	NA	NA	NA	NA
[98]	VM	N.A.	NA	NA	NA	NA	NA	Yes
[99]	VM	N.A.	NA	NA	NA	NA	NA	NA
[100]	VM	0,20,30	NA	80	NA.	NA	NA	Yes
[101]	VM	Unity	NA	>70 at 100 KHz	NA	NA	NA	Yes
[102]	VM	100,17.8,1.92	1.44 MHz	95	65 KHz	NA	NA	Yes
[103]	VM	10,20,30,40	NA	>70 at100 KHz	NA	NA	NA	NA
[104]	VM	29,24,19	591.6 KHz	95	2 KHz	NA	NA	Yes
[105]	VM	N.A.	NA	50	N.A.	NA	NA	Yes
[106]	VM	40,20,0	1.5-2.97 MHz	55	10 KHz	NA	NA	Yes
[107]	VM	14,19.6,25	10 MHz	147	35 KHz	±2.5	NA	NA
[107]	TAM	14,19.6,25	10 MHz	147	35 KHz	±2.5	NA	NA
[108]	VM	116	UGB 100 MHz	145	NA	±1.5	2.6	NA
[109]	VM	120	UGB 100 MHz	149	NA	±1.5	2.6	NA
[110]	VM	34,26,20	> 1 MHz	120	NA	NA	NA	Yes
[111]	VM	16.7,21,25.4,28.7	70.1 MHz	142	NA	±3.3	.519	NA
[112]	VM	2	NA	62	65 KHz	3.3 (single)	10.5	NA
[113]	VM	DC gain 72 dB	NA	NA	NA	NA	NA	Yes
[114]	VM	Unity	NA	> 60	Up to 200 KHz	NA	N.A.	NA
[115]	CM	19.5, 33.2	>10.18 MHz	91	NA	±0.8	.446	NA
[116]	TIM	10^{11} V/A	NA	NA	NA	NA	NA	Yes
[117]	TIM	48,42,26	NA	64.5	10 KHz	±1.5	4.93	Yes
[118]	CM	40,33.97,20	NA	48	NA	±1	N.A.	Yes
[119]	VM	65	109 Hz	130	NA	±2.5	.104	Yes
Prop.1	VM	21,25,29,31	14.75 MHz	81	148 KHz	±1.5	8.8	NA
Prop.2	TAM	-44,-50,-56,-58	19.67 MHz	81	148 KHz	±1.5	7.38	NA
Prop.3	CM	21,25,31,36	20.85 MHz	55	349 KHz	±1.5	5.04	NA
Prop.4	TIM	75,81,89,95	20.42 MHz	55	352 KHz	±1.5	3.6	Yes
Prop.5	VM	14,20,28,34	18.50 MHz	56	525 KHz	±1.5	.103	NA
Prop.6	TAM	-42,-38,-31,-25	20 MHz	64	153 KHz	±1.5	8.68	NA
Prop.7	CM	23,17,11,9	20 MHz	85	32 KHz	±1.5	3.99	NA
Prop.8	TIM	89,93,97,99	14.85 MHz	85	32 KHz	±1.5	8.33	NA
Prop.9	VM	13, 12, 11	11.9 MHz	120	28 KHz	±1.5	.813	NA
Prop.10	TAM	-46, -47, -48	12.1 MHz	120	28 KHz	±1.5	2.35	NA
Prop.11	CM	26, 30, 36, 41	13.6 MHz	74	165 KHz	±1.5	2.23	NA
Prop.12	TIM	80, 86, 90	12.6 MHz	74	112 KHz	±1.5	1.50	NA
Prop.13	VM	14, 20, 23, 26	21.7 MHz	93	423 KHz	±1.5	.615	NA
Prop.14	TAM	-44, -39, -35, -33	13.79 MHz	93	423 KHz	±1.5	2.59	NA

N.A. – Not Available, Prop. – Proposed IA topology

5.6 CONCLUDING REMARKS

Two generalized IA structures are presented in this chapter. These structures are used to develop eight IA topologies – two each are working in VM, CM, TAM AND TIM. The generalized structures are modified to reduce passive component count and are further used to develop six more IA topologies. The effect of non-idealities such as finite transimpedance gain and tracking error of OFCC, on the performance of all the proposed topologies is analyzed. The corresponding differential gain and CMRR values for all topologies are tabulated for ready reference. The proposed designs are verified through simulations carried out using SPICE 0.5μm model parameters provided by MOSIS AGILENT. These circuits present appropriate input and output impedances for both current and voltage signals. Topology 4 is prototyped to fetch experimental results for better comparison and satisfying the simulated and theoretical predictions very well. The simulated results verify the functionality of all the proposed topologies. The performance parameters of available and proposed IA topologies shows that CMRR and CMRR bandwidth of some of proposed IA topologies outperforms.

CHAPTER - 6

OFCC BASED TRANSIMPEDANCE MODE PGA

This chapter includes various details, analysis and simulated results of following published paper:

1. Prateek Pahalwan, Prateek Tripathi, Prashant Gola, Neeta Pandey, **Deva Nand, "Programmable Gain Amplifier using Operational Floating Current Conveyors"** *Int. Journal of Electronics and Communications, AEU,* ***(Elsevier)***, 90, pp. 163-170, 2018. **(SCI)** *DOI: 10.1016/j.aeue.2018.04.022*

6.1 INTRODUCTION

Amplifiers, in particular programmable gain amplifiers (PGA), find applications in instrumentation, photodiode circuits, ultrasound preamplifiers, sonar, wide dynamic range sensors, driving ADCs (some ADCs have on-chip PGAs), automatic gain control (AGC) loops [120, 121]. Fig. 6.1 [121] depicts a typical use of PGA in data acquisition system wherein it is placed between a sensor and ADC. Additional signal processing circuitry, as per demand of application, may be placed before or after the PGA. Former location is, however, preferred as it allows to condition a larger signal. Typically, operational amplifiers are employed in designing PGAs.

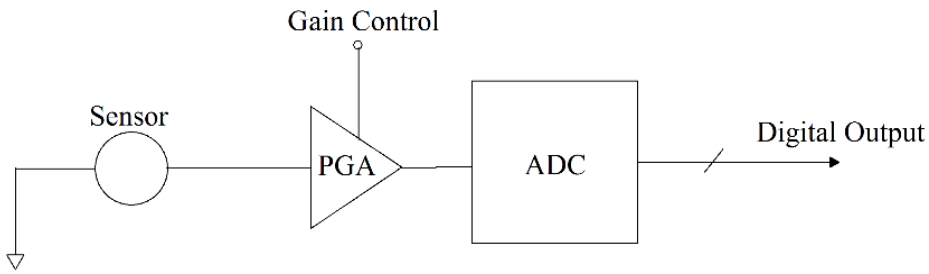


Fig. 6.1 PGAs in data acquisition systems [121]

This chapter presents new OFCC based PGA. It operates in TIM i.e. it receives current signal as input and provides voltage as output. It uses four blocks – a current amplifier, digitally controlled transimpedance amplifier, digitally controlled R-2R ladder network and a voltage buffer. First block amplifies input signal. Second and third blocks of proposed PGA provide control over coarse and fine gain through bits (B_5 – B_0) and a total of 60 different gain values are possible through the arrangement. The last block provides output at low impedance thereby avoiding need of impedance matching circuit.

6.2 LITERATURE SURVEY

The features of available PGAs [13, 122-143] are summarized in Table 6.1 on the basis of type of input being processed and output made available, active block used, input/output impedance and gain controlling mechanism. Following are the observations:

- The PGA designs [13, 122-143] provide voltage output and process data from voltage sensor. A current to voltage converter is needed if data is sensed from current sensor.

Table 6.1 Literature survey on previously reported PGAs

Ref. no.	Input/ output	Active block used	Input/output impedance	Gain control mechanism
[13]	V/V	OFCC	High/Low	Switched Resistor array
[122]	I/I, V/V	DPCCII	Low/High, High/High	Code word controlled transistor arrays by effectively changing the transconductance
[123]	V/V	DCFDCCII	High/High	Code word controlled Current division network (CDN)
[124]	V/V	CCII, Op Amp	Low/Low	Fine Gain- Tuning of external resistors, Coarse Gain- CDN
[125]	V/V	CFA	High/Low	Tuning of feedback resistor
[126]	V/V	FDCFOA	High/High	Resistor tuning
[127]	V/V	Op Amp	High/Low	Switched resistor array
[128]	V/V	Diff. Amp with CMFB	High/High	Source resistor tuning from switch array
[129]	V/V	Diff. Amp with Current Feedback	High/Low	Resistor array
[130]	V/V	Hybrid Exponential Approximation using Diode connected load	High/Low	Bit controlled exponential function
[131]	V/V	MOSFET based differential amplifier array	High/High	Binary weighted switched resistor array
[132]	V/V	FGA with loop amplifier and CMFB	Low/Low	Resistor tuning
[133]	V/V	Diff. Amp with CMFB and DC offset cancellation circuitry	High/Low	Weighted transistor array (trans-conductance control circuitry)
[134]	V/V	CDN and Generic Amplifier	Low/Low	CDN
[135]	V/V	CCII, OTA and Current Mirrors	High/High	Digitally controlled current mirrors
[136]	V/V	FDCCII	High/High	Tuning of resistors
[137]	V/V	Differential Amplifier	High/High	4-bit Digitally controlled look up table and pre-calibration method.
[138]	V/V	CMOS based VGA, 10 bit DAC	High/Low	DAC gain control (dB linear/digital)
[139]	V/V	Single ended gate driven VGA	High/Low	4 bit digitally programmable gain
[139]	V/V	Fully differential gate driven VGA	High/Low	5 bit digitally programmable gain
[140]	V/V	Differential FVF amplifier	High/Low	Source degenerated capacitor array
[141]	V/V	OTA, input negative transconductor	High/High	Two stacked transistors and PMOS bulk driven forward bias
[142]	V/V	OTA, switched capacitor based DAC	High/High	Switched capacitor array (9 bit gain and offset DAC)
[143]	V/V	Op-amp	High/Low	Resistor array with MOS switches
Prop. work	I/V	OFCC	Low/Low	Bit Controlled R-2R ladder network and resistor array

Prop. work: Proposed work

- The PGA design [122] processes data sensed from current sensor and provides current output. A current to voltage converter is required in case there is a need of interfacing it with circuit having input as voltage.
- Different active blocks namely CCII [124, 135] and its variants such as DPCCII [122], DCFDCCII [123] and FDCCII [136]; CFA [125] and its variant such as FDCFOA [126]; OFCC is used in [13]; the topologies [128, 129, 132, 133, 137, 140] employ differential amplifier whereas [128] and [140] using CMFB and FVF along with differential amplifier; CMOS based simple single ended and fully differential gate driven variable gain amplifier (VGA) with programmable gain is also reported in [138, 139]; few topologies with OTA are reported in [141, 142]; whereas [143] employs op-amp for PGA design.
- The input and output impedances are proper in [13, 125, 127, 129, 130, 133, 138-140, 143] while additional active block is needed in [122-124, 126, 128, 131, 132, 134-137, 141, 142] to satisfy impedance condition.
- Gain tuning is achieved through current division networks (CDN) [123, 124, 134], weighted transistor arrays [122, 133], potentiometer [125, 126, 132, 136] or switches [13, 127-129, 131]; and digitally controlled exponential function [130] or current mirrors [135]; 4-bit digitally controlled look up table and pre-calibration method [137]; DAC gain control (dB linear/digital) [138]; 4-bit and 5-bit digitally programmable VGA [139]; source degenerated capacitor array [140]; two stacked transistors [141]; switched capacitor array [142]; and resistor array with MOS switches [143].
- Explicit mechanism for fine and coarse gain tuning is applied in [13, 124] and [143].

It may be observed that no PGA design is available that works in TIM i.e. processes data that is available from current sensor and provides voltage output. Therefore, there is need of PGA topology, operating in TIM.

6.3 PROPOSED OFCC BASED PGA

The block diagram of proposed OFCC based PGA is depicted in Fig. 6.2. The realization of constituent blocks of Fig. 6.2 are shown in Fig. 6.3 (a) - Fig. 6.3 (d). The first block (Fig. 6.3 (a)) of proposed PGA is a current gain block.

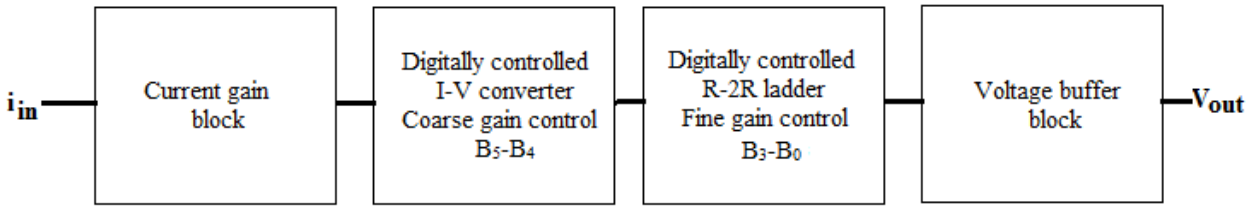


Fig. 6.2 Block diagram of proposed Programmable Gain Amplifier

Considering single pole model transimpedance gain ($Z_t(s)$) (2.3) the output current (i_1) is computed as

$$i_1|_{fz} = -i_{in}\left[1+\frac{R_1}{R_G}\right]\frac{1}{1+\frac{R_1}{Z_t(s)}} \tag{6.1}$$

The second and third blocks of proposed PGA provide control over coarse and fine gain using bits (B_5 - B_4) and (B_3 - B_0) respectively. The second block of Fig. 6.3 (b) converts the current (i_1) to voltage (V_{W_OFCC2}) through resistance R_2. The coarse gain control bits (B_5 - B_4) are applied to a 2 to 4 decoder which outputs bits (D_3 - D_0). The bits (D_3 - D_0) enable one out of the four switches connected between X and W port of OFCC2 providing resistance R_2 of value given in (6.2).

$$R_2 = D_0 \times R + D_1 \times 2R + D_2 \times 4R + D_3 \times 6R \tag{6.2}$$

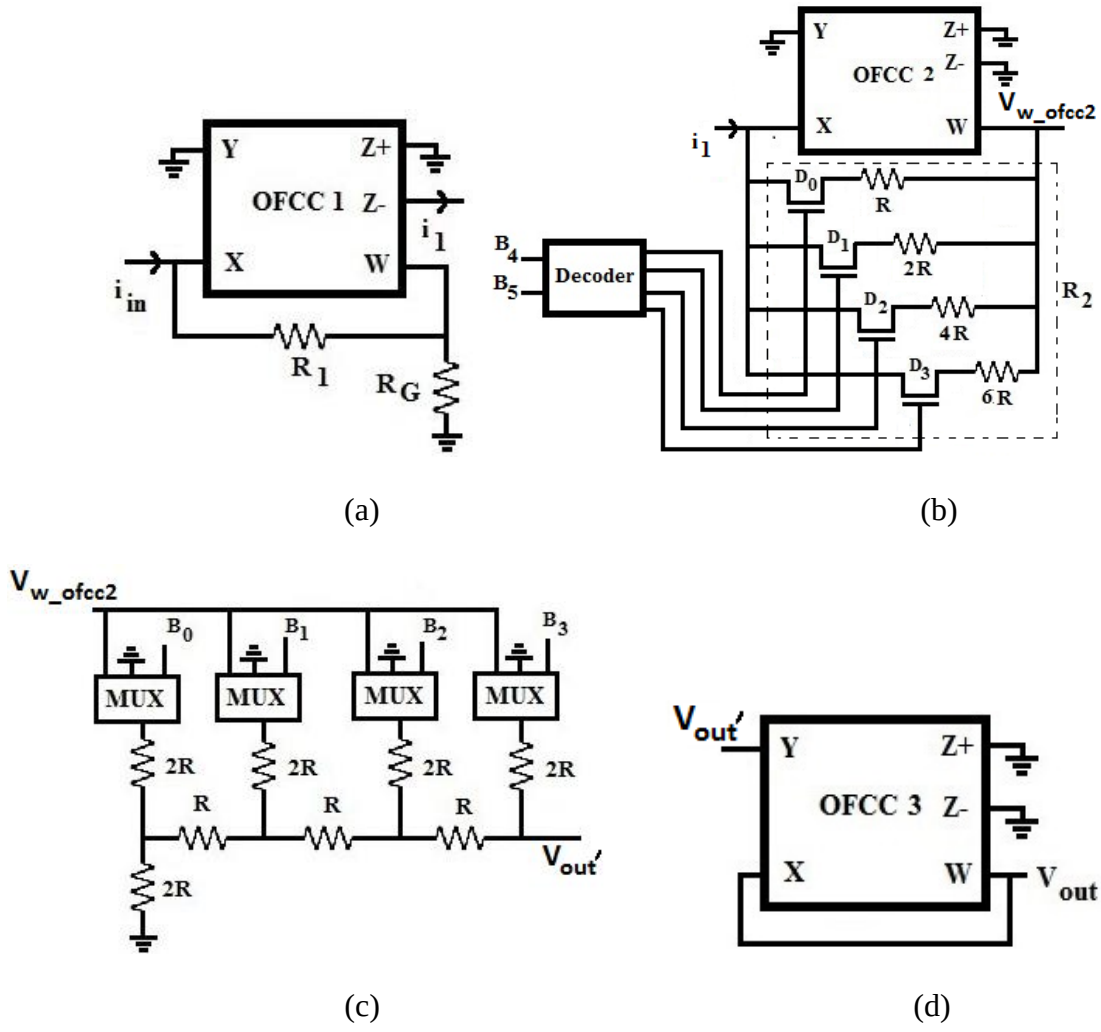


Fig. 6.3 (a) Current gain block (b) digitally controlled I-V converter (c) R-2R ladder network (d) voltage buffer

Considering (2.3), the relation between input and output of second block is obtained as

$$V_{W\_OFCC2}\big|_{fz} = -i_1 \cdot R_2 \frac{1}{1+\frac{R_2}{Z_t(s)}} = i_{in} \cdot R_2 \left[1+\frac{R_1}{R_G}\right] \frac{1}{1+\frac{R_1}{Z_t(s)}} \cdot \frac{1}{1+\frac{R_2}{Z_t(s)}} \tag{6.3}$$

which may be rewritten as

$$V_{W\_OFCC2}\big|_{fz} = i_{in} \cdot R_2 \left[1+\frac{R_1}{R_G}\right] \frac{1}{1+\frac{R_1R_2}{Z_t^2(s)}+\frac{R_1}{Z_t(s)}+\frac{R_2}{Z_t(s)}} \tag{6.4}$$

The second order term ($R_1R_2/Z_t^2(s)$) in denominator of (6.4) may be neglected as $Z_t(s)$ is very high. Therefore (6.4) modifies to

$$V_{W\_OFCC2}\big|_{fz} \approx i_{in} \cdot R_2 \left[1+\frac{R_1}{R_G}\right] \frac{1}{1+\frac{R_1}{Z_t(s)}+\frac{R_2}{Z_t(s)}} \tag{6.5}$$

Taking single pole model and high frequency approximation given in (2.3.1) for $Z_t(s) = 1/(sC_p)$, (6.5) modifies to

$$V_{W\_OFCC2}\big|_{fz} \approx i_{in} \cdot R_2 \left[1 + \frac{R_1}{R_G}\right]\left[\frac{1}{1+(R_1+R_2)sC_p}\right] \tag{6.6}$$

It may be noted that is a pole appears at $s = \left((R_1 + R_2)sC_p\right)^{-1}$ which may affect the processing of high frequency signals.

The third block (Fig. 6.3 (c)) is digitally controlled R-2R ladder network. It adds fine gain control through multiplexers whose operation is controlled by bits (B_3-B_0). The bits (B_3-B_0) can vary from 0001 to 1111 therefore fifteen possible gain combinations exist. Taking the coarse and fine gain variations into account, the proposed PGA can be tuned to 60 possible gain values.

The output of the third block is computed as

$$V_{out'}\big|_{fz} = V_{W\_OFCC2\_fz}\left[\frac{B_0}{16} + \frac{B_1}{8} + \frac{B_2}{4} + \frac{B_3}{2}\right] \tag{6.7}$$

As the output of the third block is not available at low output impedance port, an OFCC based buffer is used as the fourth block (Fig. 6.3 (d)). Thus, the final output can be used for further processing without any impedance matching problem. The overall proposal at the circuit level is presented in Fig. 6.4.

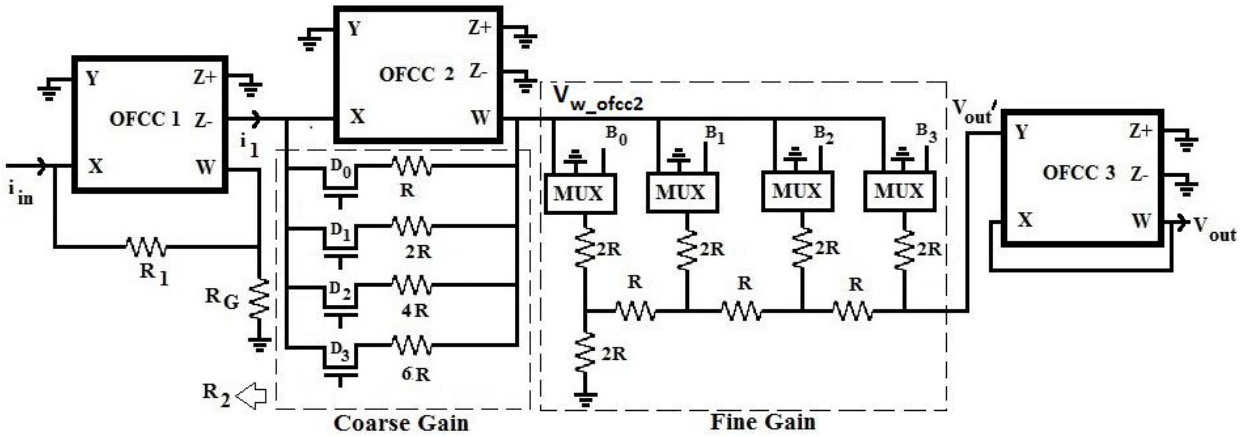
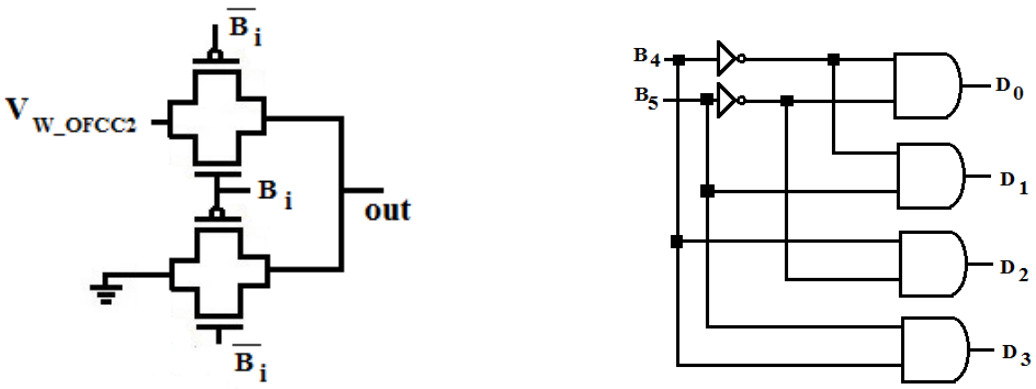


Fig. 6.4 Circuit level realization of proposed Programmable Gain Amplifier

The functionality of 2x1 multiplexer (Fig. 6.3 (b)) and 2x4 decoder (Fig. 6.3 (c)) is described in Tables 6.2 and 6.3 respectively.

Figure 6.5 (a) shows transmission gate based realization of 2x1 multiplexer while Fig. 6.5 (b) depicts static CMOS schematic of 2x4 decoder.



(a) (b)

Fig. 6.5 Schematic of (a) 2x1 multiplexer using transmission gates (b) 2x4 decoder

Table 6.2 Truth Table of 2x1 Multiplexer

B_i	Out
0	0
1	V_{W_OFCC2}

Table 6.3 Truth Table of 2 to 4 Decoder

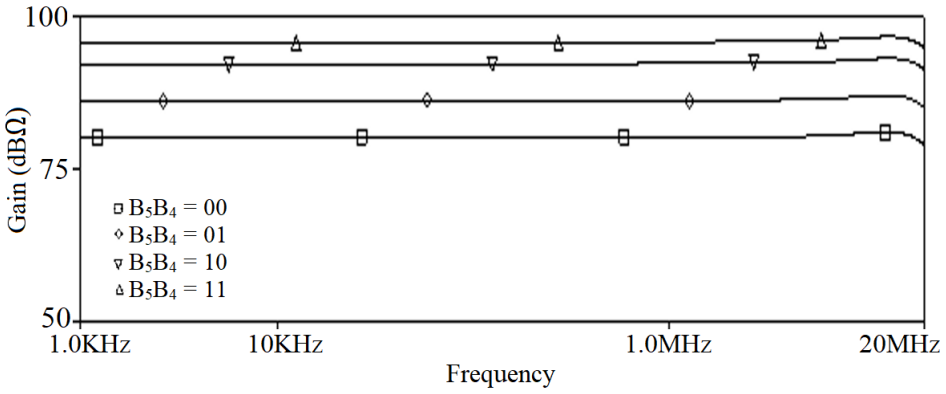
B_5	B_4	D_0	D_1	D_2	D_3	Equivalent resistance at the block, R_2 (kΩ)
0	0	1	0	0	0	1
0	1	0	1	0	0	2
1	0	0	0	1	0	4
1	1	0	0	0	1	6

6.4 SIMULATION AND EXPERIMENTAL RESULTS

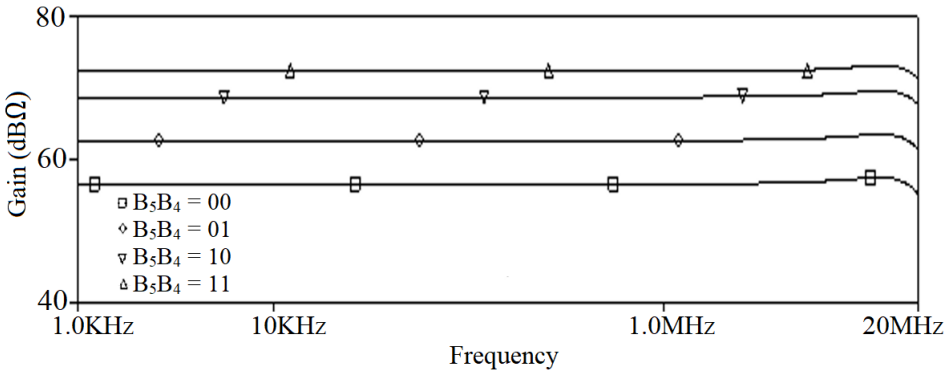
The functionality of the proposed PGA is verified through SPICE simulation and experimentation. The performance parameters of the proposed PGA are compared with those available in literature.

6.4.1 Simulation Results

SPICE simulations are carried out for functional verification using 0.5 µm technology model parameters from MOSIS (AGILENT), wherein OFCC is realized using CMOS based schematic [13] of Fig. 2.3. The resistance R_1 and R_G in current gain block (Fig. 6.3 (a)) are taken as 15 kΩ and 1 kΩ respectively. The value of R in second and third block of proposed PGA (Figs. 6.3 (b) and 6.3 (c)) is 1 kΩ.



(a)



(b)

Fig. 6.6 Frequency response of proposed PGA with coarse gain setting of (a) 1111 (b) 0001

The frequency response of the proposed PGA under maximum coarse gain setting i.e. B_3 - B_0 = 1111 for all the combinations of B_4 and B_5 are found out to be 95.84 dBΩ, 92.32 dBΩ, 86.3 dBΩ and 80.28 dBΩ and are presented in Fig. 6.6 (a). Similarly, the gain variation under minimum coarse gain setting i.e. B_3 - B_0 = 0001 are found as 72.31 dBΩ, 67.79 dBΩ, 62.78 dBΩ, 56.76 dBΩ for all combinations of B_4 and B_5 are presented in Fig. 6.6 (b) with a gain range of 39 dBΩ with a bandwidth of approximately 20 MHz.

The variation in gain setting (dBΩ) with respect to the control word inputs (B_5 - B_0) of the proposed PGA are shown in Fig. 6.7. It may be noted that wide range of gains can be achieved with the amplifier using appropriate control bits tuning thus verifying overall programmability of the proposed PGA while preserving the dB-linear characteristic of the amplifier.

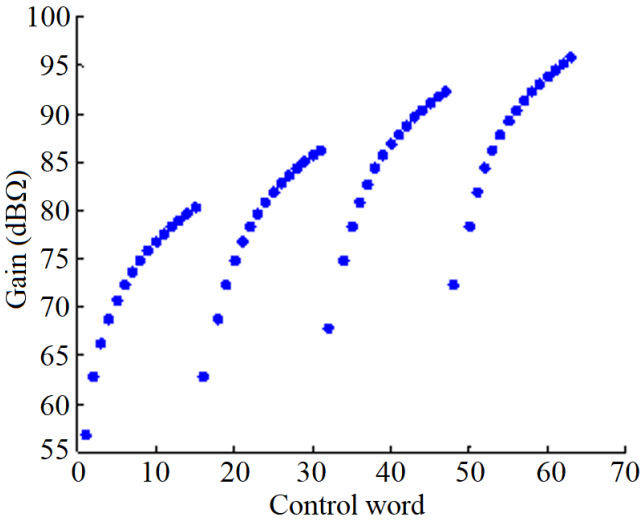


Fig. 6.7 Variation in gain with respect to control word of the proposed PGA

Simulations are also carried out to examine the noise performance of the proposed PGA. The simulated total input referred noise current was found to be 6.9 pA/√Hz. The power dissipation of the overall circuit under maximum gain setting was found to be 3.13mW.

Time domain simulations are also carried out to investigate transient behavior of the proposed PGA. A current sinusoid of 1.5µA, 20 KHz is applied to proposed PGA with maximum coarse gain setting i.e. B_3 - B_0 = 1111 and B_5B_4 are taken as 00, 01,10 and 11. The corresponding outputs are placed at Figs. 6.8 (a) – (d) and respective simulated output values are found as 22.5 mV, 45 mV, 90 mV and 135 mV which are exactly following the theoretical values i.e. 22.5 mV, 45 mV, 90 mV and 135 mV respectively.

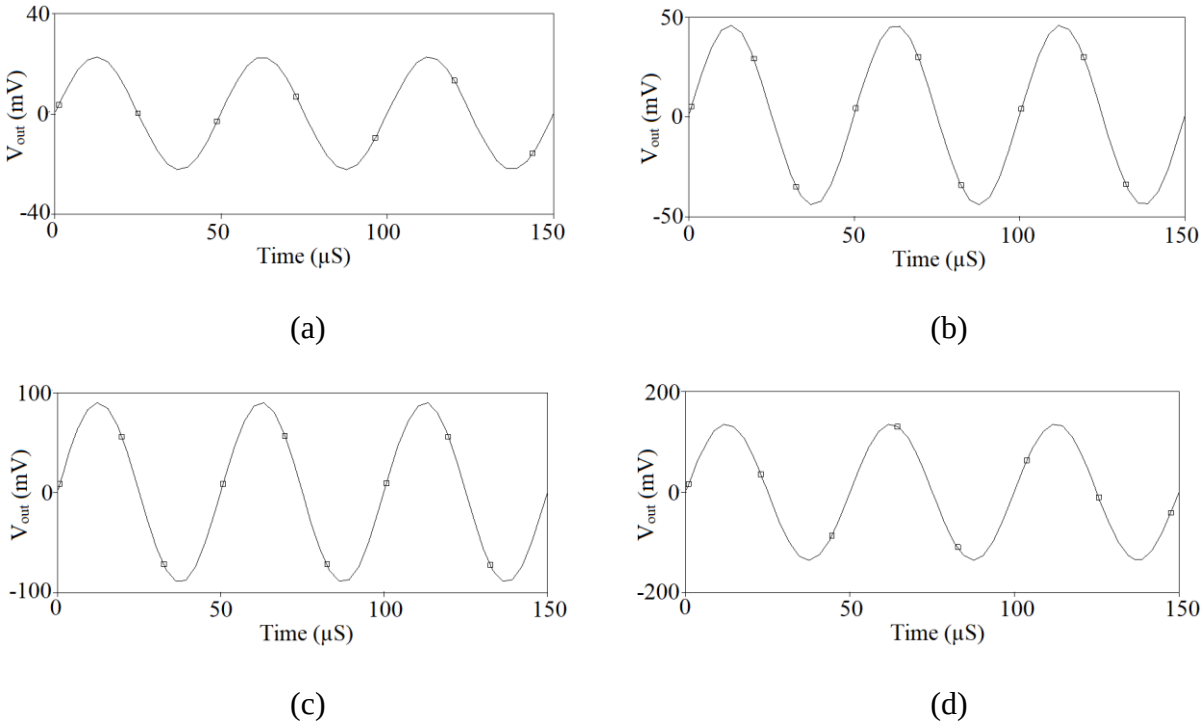


Fig. 6.8 Transient responses of proposed PGA with B_3–B_0 = 1111 and B_5B_4 as (a) 00 (b) 01 (c) 10 (d) 11

The performance comparison of proposed PGA with those available in literature, is done on the basis of parameters such as bandwidth, dynamic range, maximum and minimum gain, input referred noise, power supply used and power consumption and the findings are comprehended in Table 6.4.

Table 6.4 Performance analysis of previously reported PGAs

Ref. No.	Bandwidth	Dynamic range (dB)	(Min. gain - Max gain) (dB)	Input referred noise	Supply (V)	Power consumption
[13]	42 MHz	42	5 to 47	N/A	±1.5	3.12 mW
[122]	35 MHz	33.8	-16.9 to 16.9	N/A	±0.75	2.71 mW
[123]	N/A	24	0 to 24	N/A	±1.5	N/A
[124]	0.05 MHz to 0.8 MHz	41	-5 to 36	N/A	1.5	N/A
[125]	9.48 MHz(at max. gain)	54	6 to 60	N/A	3.3	2.4 mW
[126]	10 MHz	16	0 to 16	N/A	±1.5	1.14 mW
[127]	125 MHz	19	0 to 19	8.63 nV/√Hz	3.3	21 mW
[128]	50 MHz	24	-10 to 14	2.5 nV/√Hz	1.8	11.18 mW
[129]	10 MHz	22.5	13.8 to 36.3	7.41 nV/√Hz	3	12.6 mW
[130]	39 MHz	34.4	4.6 to 39	3.54 nV/√Hz	1.8	6.16 mW
[131]	60 MHz	42	-21 to 21	N/A	1.5	3.12 mW
[132]	30 MHz	30	-10 to 20	11.2 nV/√Hz	1.8	2.43 mW
[133]	60 MHz	48	-16 to 32	N/A	1	1.2 mW
[134]	4.1 MHz	25	0 to 25	21 nV/√Hz	3	N/A
[135]	1 MHz	17	0 to 17	N/A	±10	N/A
[136]	26 MHz	16	0 to 16	65 nV/√Hz	±1.5	N/A
[137]	80 MHz	47	-24 to 23	N/A	1.8	1.42 mW
[138]	3.5 GHz	57	- 33 to 24	N/A	1.2	96 mW
[139]	2 KHz	20	0 to 20	N/A	±0.18	0.15 µW
[139]	8KHz	27	0 to 27	N/A	±0.08	0.07 µW
[140]	6 GHz	20	10 to 30	N/A	1.2	11.78 mW
[141]	0.98 MHz	18.2	0.2 to 18.4	N/A	0.36	15.4 µW
[142]	> 500 MHz	9.53	-1.93 to 7.60	N/A	1.8	18.18 mW
[143]	35 MHz	23	-6 to 17	22 nV/√Hz	1.8	3.96 mW
Proposed work	20 MHz	39	56.8 to 95.8	6.9 pA/√Hz	±1.5	3.13 mW

Following are the observations from Table 6.4:

- The proposed PGA demonstrates a superior dynamic range than the works reported in [122, 123, 126, 127-130, 132, 134-136, 137, 139-143]. While many works claim substantial theoretical dynamic range, it might be misleading as certain works in [122, 124, 128, 131-133, 137, 138, 142, 143] have overall gain values less than 0 dB which have no practical advantage as incoming data is already severely attenuated after passing through skin layers and incurring other losses due to mismatches. Thereby decreasing their effective dynamic range further.

- The proposed work possesses better bandwidth than [124-126, 129, 134, 135, 139, 141], lower input referred noise than [127-130, 132, 134, 136, 143] along with a lower power consumption than [127-130, 138, 140, 142, 143] which further demonstrates the competitive performance of the proposal.
- The proposed PGA provides maximum gain of 95.8 dBΩ which is highest among available ones. The input referred noise is also very small. Therefore, proposed design is capable of processing weaker signals and getting them to an acceptable range.

6.4.2 Experimental Results

Experimental verification of proposed PGA circuit done using commercially available IC AD844 based implementation of OFCC as shown in Fig. 2.5 [170] with supply voltages of ±5V and sinusoidal current input of 10 µA, 20 KHz is applied. The resistance values are kept same as those used in simulations. Experimental results for bit combination (101111) of control word input are shown in Fig. 6.9 for authentication.

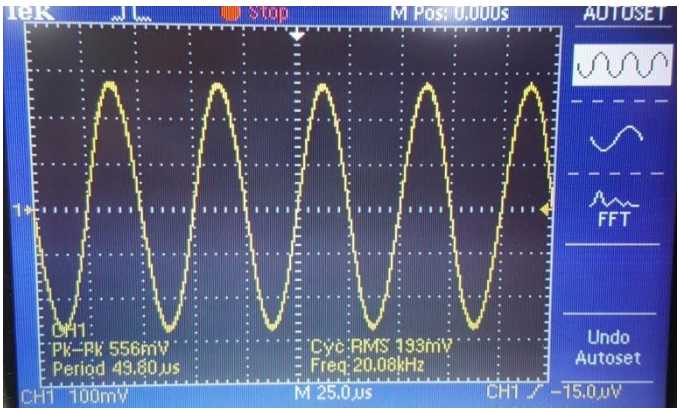


Fig. 6.9 Experimental output response

Measurements for other bit combinations are also performed and the observations are enlisted in Table 6.5 along with the calculated errors. The variation in experimental gain values from the theoretical ones may be attributed to tolerances of resistances used in prototyping and

nonidealities of OFCC. It may be noted that proposed PGA behaves well with a mean error of 6.64% in observation window which demonstrates the fidelity of the circuit. The error in output is attributed to component tolerances and device tracking errors. The precision can be further improved by usage of high impedance current source, precision resistors, higher quality probes and proper insulation of the circuit which cannot be achieved using a breadboard.

Table 6.5 Experimental measurement results and error calculation

Control word input ($B_5B_4B_3B_2B_1B_0$)	**Measured output (mV)**	**Theoretical output (mV)**	**Error (%)**
001111	137	147.9	7.4
000001	10.8	9.86	9.5
001000	73.2	78.9	7.2
000111	63.2	69	8.4
011111	270	295.8	8.7
010001	19.8	19.72	0.4
011000	145	157.8	8.1
010111	126	138	8.71
101111	556	591.6	6
100001	37.2	39.44	5.7
101000	295.3	315.6	6.4
100111	262	276	5.1
111111	816	887.4	8
110001	56	59.16	5.3
111000	441	473.4	6.8
110111	395	414	4.6

6.5 CONCLUDING REMARKS

A novel programmable gain amplifier design working in trans-impedance mode has been presented in this chapter. The design employs variable gain stage using OFCC followed by R-2R ladder network to achieve coarse and fine gain tuning of the amplifier. The presented design provides a wide range of gains 56.76 - 95.84 dBΩ that can be achieved using the control words

with a high degree of precision along with its low input noise current of 6.9 pA/√Hz and low power properties like 3.13mW. The fidelity of the simulated and experimental results with respect to the corresponding theoretical values further demonstrate and exhibit the competitive performance of the proposed design.

CHAPTER - 7

OFCC BASED CM RECTIFIER

This chapter includes various details, analysis and simulated results of following published paper:

1. Neeta Pandey, Rajeshwari Pandey, Deva Nand and Abhishek Kumar, "**Current mode rectifier configuration based on OFCC**" *IEEE International Conference on Signal Propagation and Computer technology (ICSPCT-2014)*, Ajmer, pp. 533-536, 2014. doi**:** 10.1109/ICSPCT.2014.6884960

7.1 INTRODUCTION

The rectifiers are widely used in applications pertaining to telecommunication, instrumentation and measurement [144-147]. Some of the applications are ac voltmeter, averaging circuits, peak value detectors, clipper circuits, amplitude-modulated signal detectors, signal-polarity detectors etc. Conventionally both of the rectifiers are implemented using operational amplifiers which are not capable of operating at higher frequencies because of slew rate and fixed gain-bandwidth product limitations [2]. Another limitation is use of diodes that limits its application in which precision is insignificant in the range of diode cut-in voltage.

In this chapter single OFCC based CM half wave rectifiers (HWRs) and full wave rectifier (FWR) are put forward. These rectifiers do not use diode and are thus suitable for low voltage rectification. It is pertinent to mention here that all proposed rectifiers use single active block and are resistor-less. Available rectifier structures are briefly reviewed prior to presenting the proposed rectifiers.

7.2 LITERATURE SURVEY

A wide variety of active blocks namely OPAMP [144, 145], CCIICS [146], CC [147], EXCCII [148], DXCCII [149, 152], CCCII [150, 162], FDIO-OTA [151], CCII [153, 155, 158, 160, 161, 164, 166], DVCC [154, 155, 159], CDTA [156, 157], OTA [159], DO-OTA [163], CDBA [165] and FCS [167] have been used to realize rectifiers in recent past. Table 7.1 enlist the features of available rectifiers on the basis of type and number of active blocks; passive component count; and diode usage. From Table 7.1 it may be noted that

- available rectifiers operate in VM [144-147, 149-155, 160, 161, 163, 164, 166, 167], CM [148, 156-159, 165] and TAM [162].
- more than one active block is reported in [144-147, 152, 154, 155, 158, 161, 162, 164, 166].

Table 7.1 Literature survey of available rectifiers

Ref.	Name of active block	No. of active blocks	No. of diode/resistance usage	MOS transistor usage	Input/output impedance	Input/output type
[144]	Opamp, CCI	2,1	2/3	0	Low/Low	V/V
[145]	Opamp, CCII+	2,1	2/3	0	High/Low	V/V
[146]	CCIICS	2	4/2	0	High/High	V/V
[147]	CC	2	4/2	0	High/High	V/V
[148]	EXCCII	1	0/0	2	Low/High	I/I
[149]	DXCCII	1	0/0	3	High/High	V/V
[150]	CCCII	1	0/1	2	High/High	V/V
[151]	FDIO-OTA	1	4 active/1 active	0	High/High	V/V
[152]	DXCCII	2	0/1	2	High/High	V/V
[153]	CCII	1	0/1 active	4	High/High	V/V
[154]	DVCC	2	2/2	0	High/Low	V/V
[155]	CCII	2	0/4	1	High/High	V/V
[155]	DVCC	2	0/3	1	High/High	V/V
[156]	CDTA	1	4/1	0	Low/High	I/I
[157]	CDTA	1	2/1	0	Low/Low	I/I
[158]	CCII	2	2/0	0	Low/High	I/I
[159]	OTA	1	2/2	0	Low/High	I/I
[159]	DVCC	1	2/3	0	Low/High	I/I
[160]	CCII and Current mirrors	1,4	0/2	0	High/Low	V/V
[161]	CCII	2	4/1	0	High/High	V/V
[162]	CCCII	3	0/5	0	High/High	V/I
[163]	DO-OTA	1	4/1	0	High/Low	V/V
[164]	CCII	2	0/0	3	High/High	V/V
[165]	CDBA	1	2/0	0	Low/High	I/I
[166]	CCII	2	2/3	0	High/Low	V/V
[167]	FCS	1	4/1 active	0	High/High	V/V

- VM [144-147, 151, 154, 161, 163, 164, 166, 167], CM [156–159, 165] use diodes to achieve rectification.
- the input and output impedance of VM rectifier [144, 146, 147, 149-153, 155, 161, 164, 167] and CM rectifier [157] are not proper hence additional active block is required.
- resistances and MOS transistors are also used in [144-147, 150-157, 159-163, 166, 167] and [148-150, 152, 153, 155, 164] respectively.

It may be noted that no OFCC based HW or FW rectifier is available in open literature. Therefore, OFCC based rectifier topologies are presented in the next section.

7.3 PROPOSED OFCC BASED RECTIFIERS

This section present OFCC based CM HWRs and FWR circuits. All the proposed circuits use single active block and MOS switches.

7.3.1 Proposed CM HWRs

The proposed CM HWRs are depicted in Fig. 7.1. Both the circuits use single OFCC and a MOS switch. As Z_{2+} port is directly connected to gate of MOS transistor which has high resistance, current drops at high resistance therefore, the voltage at Z_{2+} port would be saturating at supply voltage depending upon the value of input current. For instance, if input currents I_{in} (t) > 0, the voltage at Z_{2+} port saturate at V_{DD} and attains value V_{SS} otherwise.

The operation of the circuit of Fig 7.1 (a) may be elucidated as follows

- During positive cycle of input current $I_{in}(t) > 0$ so $V_{Z2+} = V_{DD}$. It makes transistor M_n – ON and output current follows input current i.e.

$$I_{out}(t) = I_{in}(t) \quad (1)$$

and during negative cycle of input current $I_{in}(t) < 0$ so $V_{Z2+} = V_{SS}$. It makes transistor M_n – OFF and gives output current zero i.e.

$$I_{out}(t) = 0 \quad (2)$$

Similar argument for circuit of Fig. 7.1 (b) shows that.

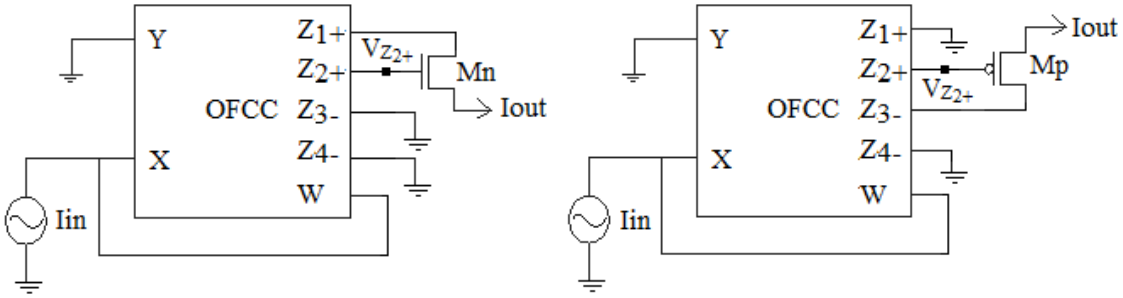
- During positive cycle of input current $I_{in}(t) > 0$ so $V_{Z2+} = V_{DD}$ so transistor M_p is OFF and output current is zero i.e.

$$I_{out}(t) = 0 \quad (3)$$

and during negative cycle of input current $I_{in}(t) < 0$, $V_{Z2+} = V_{SS}$ so transistor M_p is ON and output current follows inverted input current i.e.

$$I_{out}(t) = -I_{in}(t) \quad (4)$$

The above discussion leads to the conclusion that the circuit of Fig. 7.1 (b) also gives functionality of HWR.



(a) (b)

Fig. 7.1 Proposed Half wave rectifiers circuit

7.3.2 Proposed CM FWR

The proposed CM FWR based on single OFCC and two MOS switches (M_n, M_p) is shown in Fig. 7.2. As Z_{2+} port is directly connected to gate of MOS transistor which has high resistance, current drops at high resistance therefore, the voltage at Z_{2+} port would be saturating at supply voltage depending upon the value of input current. For input currents $I_{in}(t) > 0$, the voltage at Z_{2+} port saturate at V_{DD} and attains value V_{SS} otherwise. This will make either transistor M_p or M_n active and allow the current available at Z_{1+} or Z_{3-} port to pass through respectively.

Thus for $I_{in}(t) > 0$

$$V_{Z2+} = V_{DD}, \quad M_n \text{ - ON, } M_p \text{ - OFF, } I_{out}(t) = I_{in}(t) \quad (5)$$

And for $I_{in}(t) < 0$

$$V_{Z2+} = V_{SS}, \quad M_n \text{ - OFF, } M_p \text{ - ON, } I_{out}(t) = -I_{in}(t) \quad (6)$$

Hence the output current may be expressed as

$$I_{out}(t) = |I_{in}(t)| \quad (7)$$

Thus giving functionality of FWR.

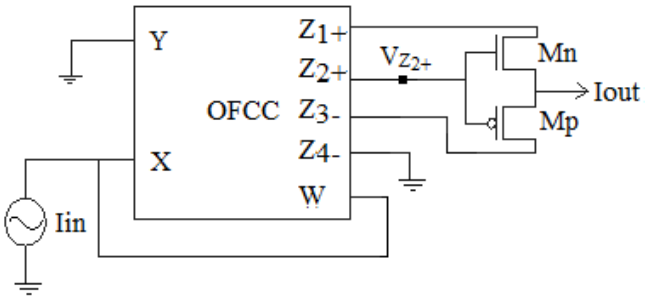
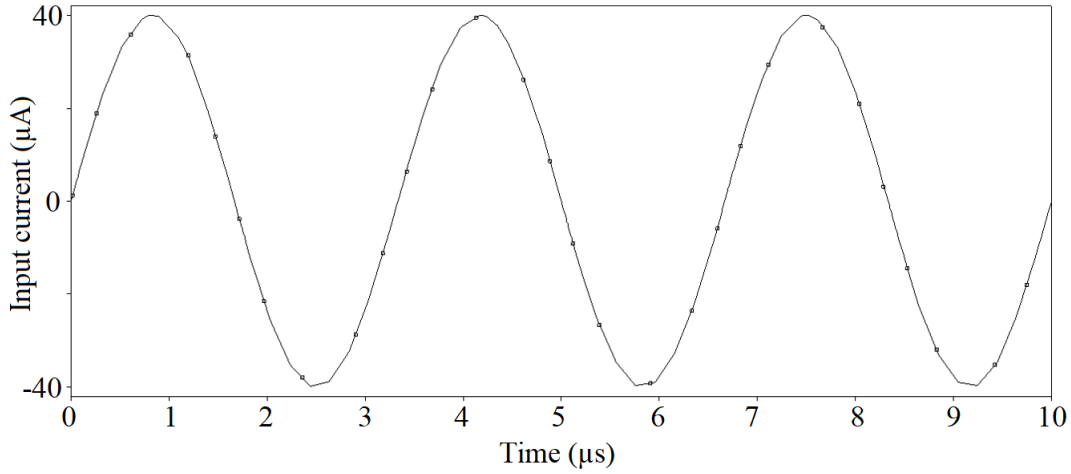


Fig. 7.2 Proposed Full wave rectifier circuit

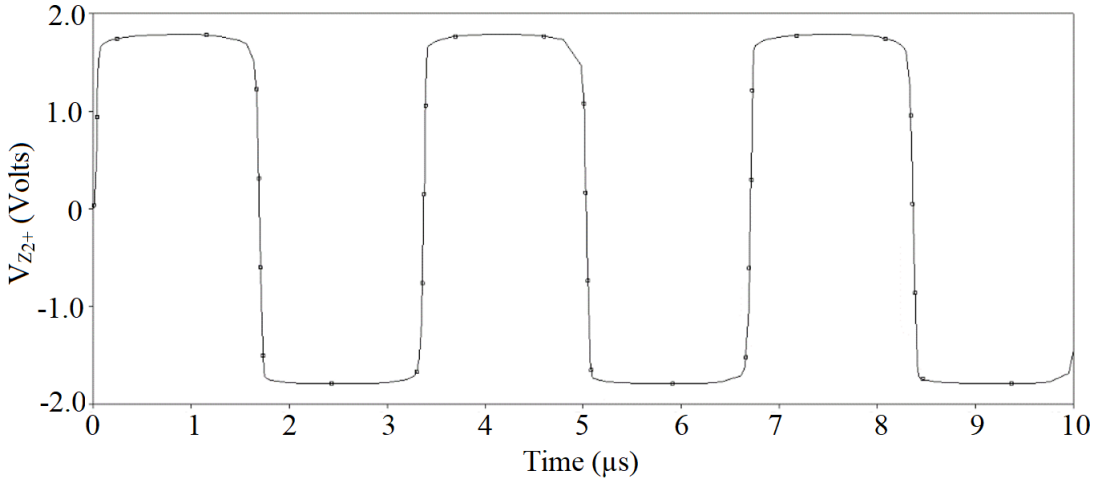
7.4 SIMULATION RESULTS

The functionality of proposed rectifiers is verified through SPICE simulations. Both transient and DC performance are examined. The CMOS based OFCC schematic of Fig. 2.3 is used for all simulations. For transient response of proposed HW rectifier, a current sinusoid of amplitude 40µA and 300 KHz frequency as shown in Fig. 7.3 (a) is applied as input to circuit of Fig. 7.1 (a) and (b). Simulated voltage output (V_{Z2+}) is plotted in Fig. 7.3 (b). It may be noted that V_{Z2+} saturates to V_{DD} therefore transistor M_n (Fig. 7.1 (a)) is ON and transistor M_p (Fig. 7.1 (b)) is OFF. This makes current output to follow input in circuit of Fig. 7.1 (a) and zero in case of circuit of Fig. 7.1 (b).

Similarly, V_{Z2+} saturates to V_{SS} therefore transistor M_n (Fig. 7.1 (a)) is OFF and transistor M_p (Fig. 7.1 (b)) is ON. Thus current output is zero in circuit of Fig. 7.1 (a) and makes current output to follow input with phase same as that of current at Z_{3-} port in case of circuit of Fig. 7.1 (b). Simulated output current waveforms of Fig. 7.4 corroborate with theoretical predictions.

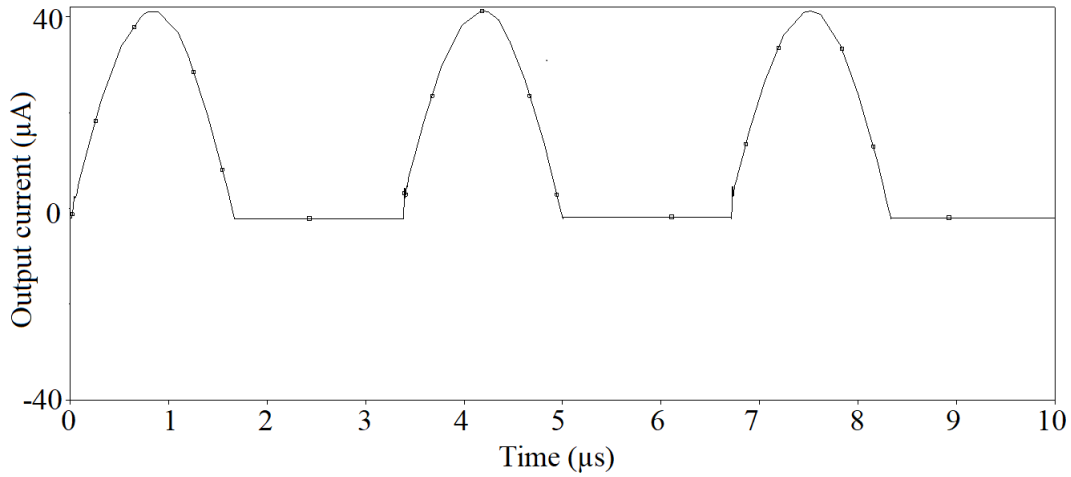


(a)

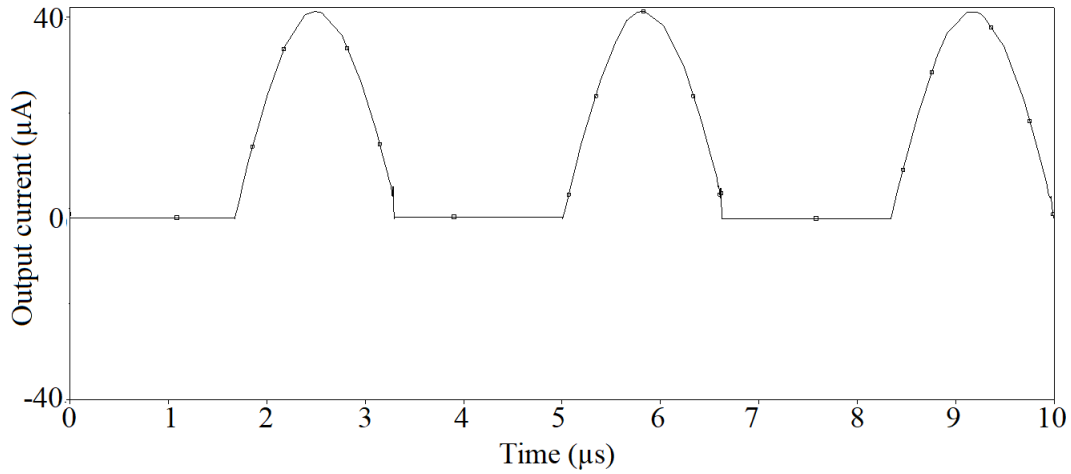


(b)

Fig. 7.3 (a) Input current (b) voltage at Z_{2+} port



(a)



(b)

Fig. 7.4 HW rectified outputs for (a) positive cycle of input current

(b) negative cycle of input current

The ripple factor is also computed from simulated data and the results are placed in Fig. 7.5. The theoretical value of ripple factor for HW rectified output is 1.21 while simulated value is 1.29.

To study DC transfer characteristics of proposed HWRs input current is varied from – 40 µA to + 40 µA and output responses are plotted in Figs. 7.6 (a) and (b). The examination of the responses shows that transfer is linear which follows theoretical prediction.

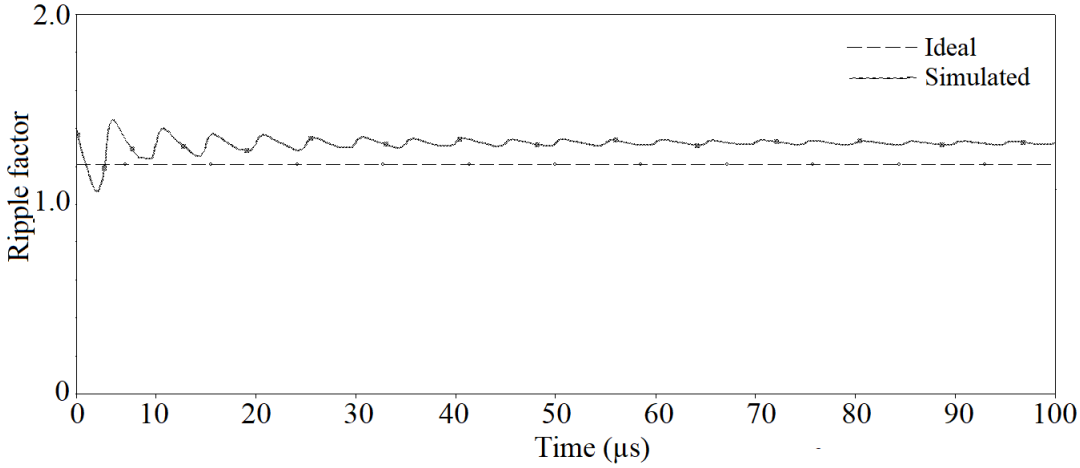
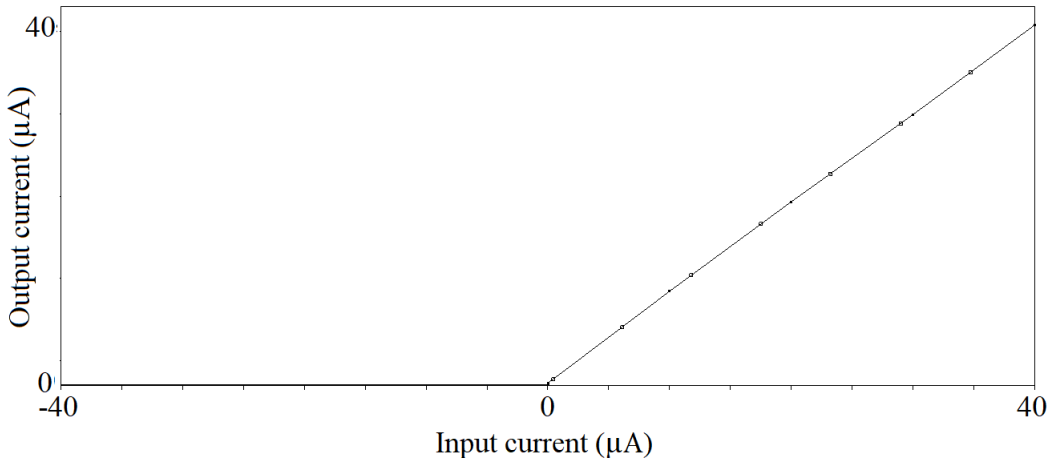
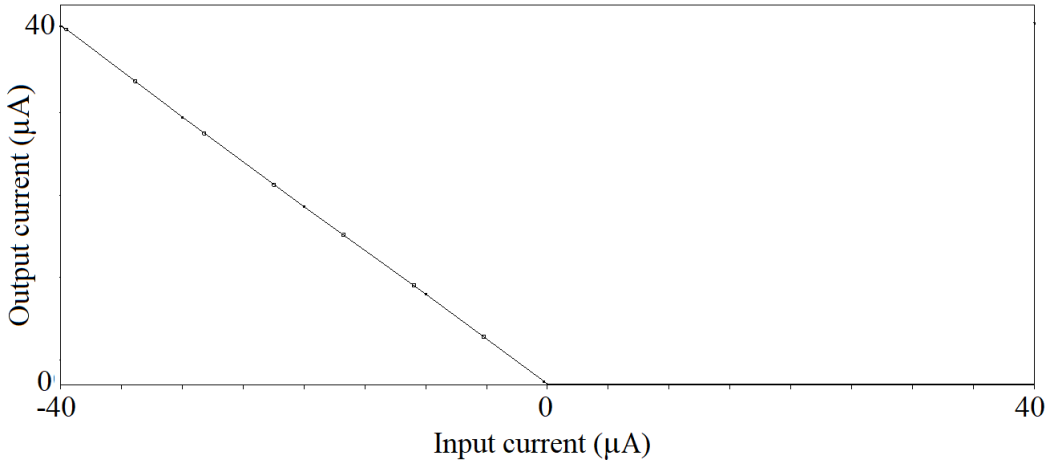


Fig. 7.5 Ripple factor of HW rectifier under sinusoidal excitation



(a)



(b)

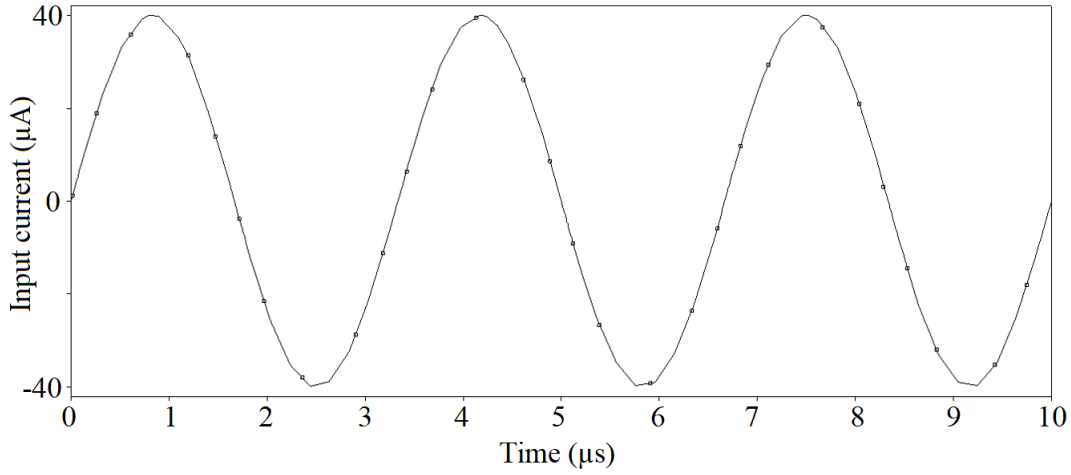
Fig. 7.6 DC response of the proposed HW rectifiers circuit for

(a) positive current and (b) negative current transfers

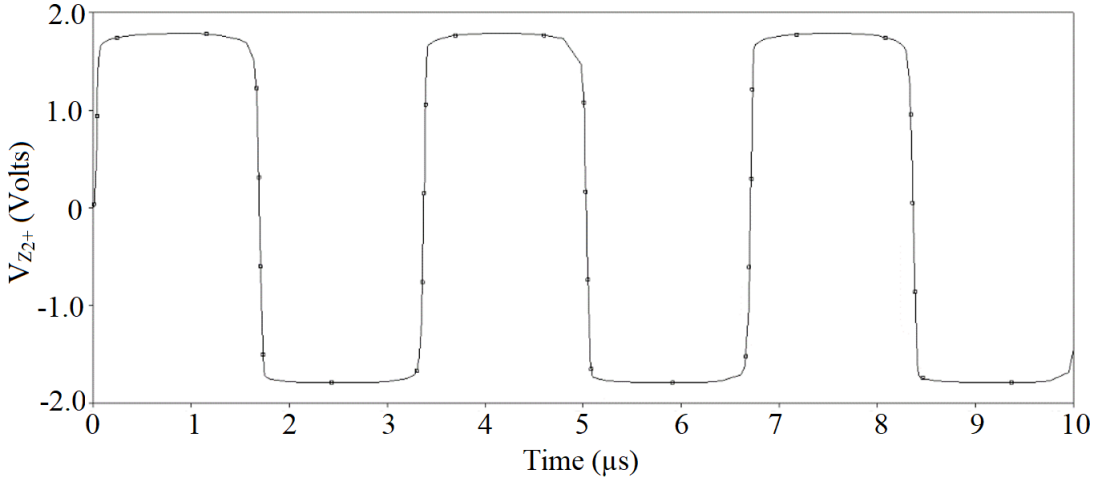
To verify the functionality of proposed FW rectifier, an input sinusoid of 40µA amplitude and 300 KHz frequency as shown in Fig. 7.7 (a) is applied to circuit of Fig. 7.2. Simulated voltage output (V_{Z2+}) is plotted in Fig. 7.7 (b). It may be noted from Fig. 7.2 that during positive cycle of input V_{Z2+} saturates to V_{DD} the transistor M_n is ON and transistor M_p is OFF. This makes current output to follow input while during negative cycle of input V_{Z2+} saturates to V_{SS} then transistor M_n is OFF and transistor M_p is ON thus current output to follow

input with phase same as that of current at Z_{3-} port. Simulated output current waveforms are depicted in Fig. 7.7 (c).

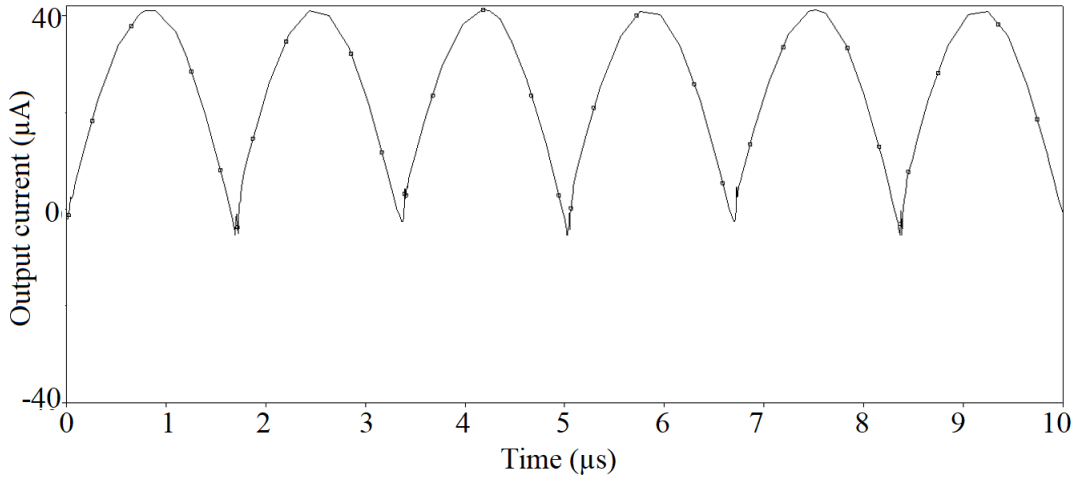
The ripple factor is also computed from simulated data and the results are placed in Fig. 7.8. The theoretical value of ripple factor for FW rectified output is 0.483 while simulated value is 0.562. The functionality of proposed FWR under triangular excitation is also examined and simulation results are placed in Fig. 7.9.



(a)



(b)



(c)

Fig.7.7 (a) Input current (b) Voltage at Z_{2+} port (c) FW rectified output

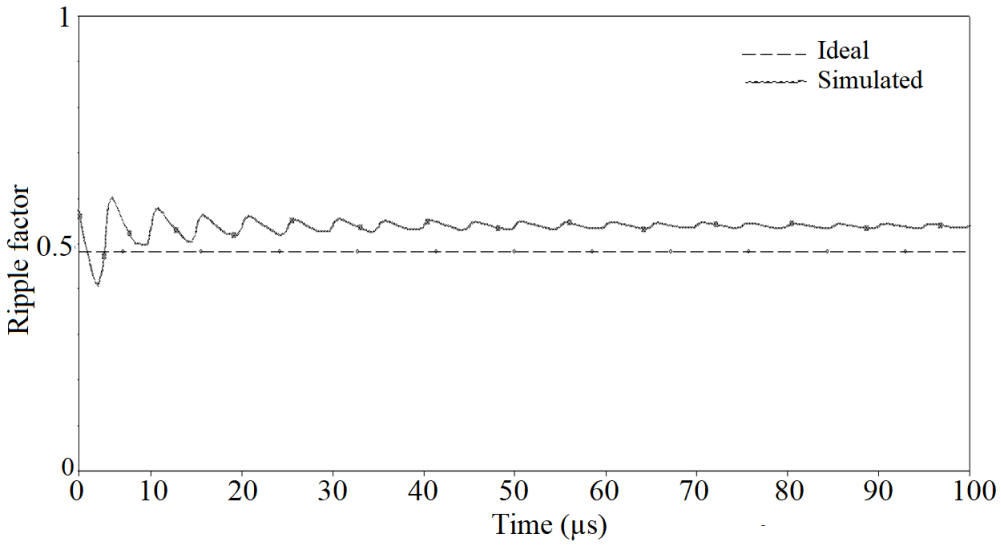


Fig. 7.8 Ripple factor of proposed FWR under sinusoidal excitation

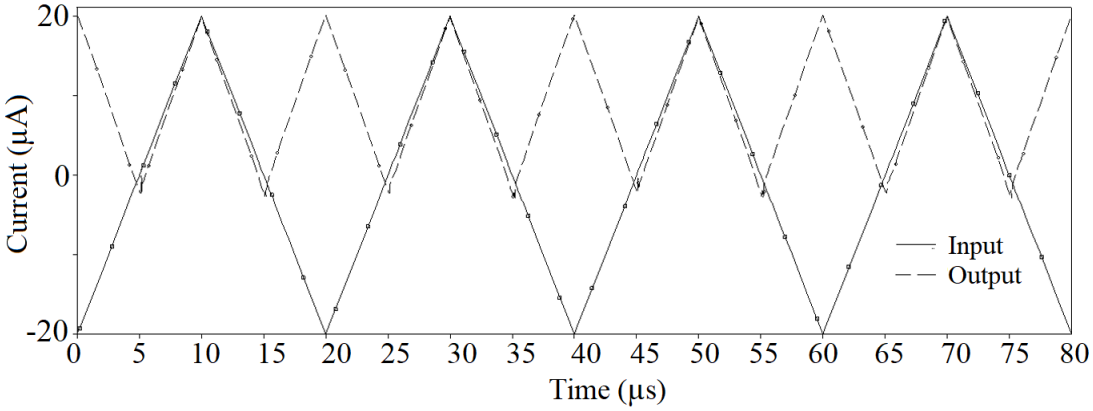


Fig. 7.9 Input and output waveform under triangular excitation for proposed FWR

To study DC transfer characteristics of proposed FWR, the input current is swept from – 40µA to + 40µA and the output is plotted in Fig. 7.10. It is clear that both positive and negative input currents are transferred at the output which will be positive. Thus FWR functionality is confirmed.

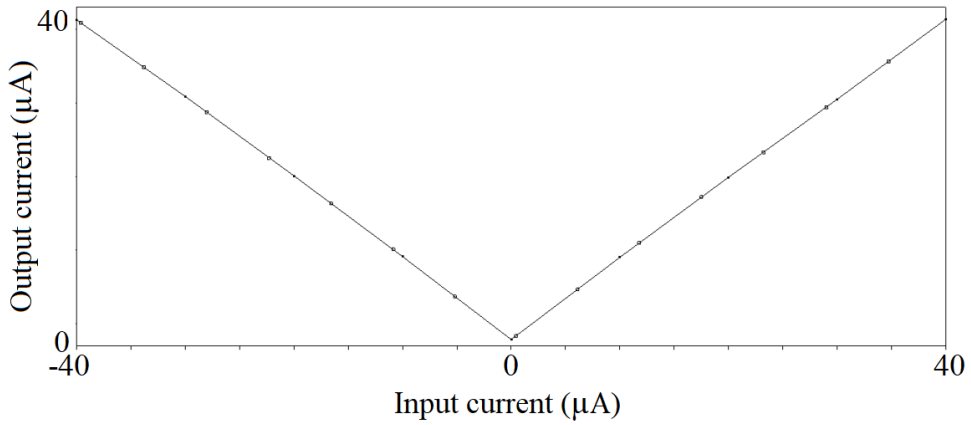


Fig. 7.10 DC response of the proposed FWR

7.5 CONCLUDING REMARKS

CM rectifier configurations of HWRs and FWR using OFCC are presented in this chapter. The HWR uses single OFCC and single MOS transistor, while single OFCC and two MOS transistors are used for FWR which makes it suitable from integration view point. These rectifiers do not use diode and are thus suitable for low voltage rectification. It is pertinent to mention here that all proposed rectifiers use single active block and are resistor-less. SPICE simulations are used to demonstrate the functionality of proposed rectifiers.

CHAPTER - 8

CONCLUSION AND FUTURE SCOPE

8.1 CONCLUSION

Research work carried out in this thesis presents design and implementation of analog circuits using OFCC as a newly emerged CM building block which owns the feature of both CC and CFOA. This chapter summarizes the major conclusions of the work carried out in preceding chapters of this thesis.

8.2 SUMMARY OF WORK CARRIED OUT IN THIS THESIS

The thesis introduction in chapter 1 starts with note on advancements in processing technology and its consequences on circuit design. The evolution of current mode building blocks for analog circuit design is briefly reviewed. Available literature on filters, instrumentation and programmable gain amplifiers; and rectifiers is briefly reviewed and outline of thesis is presented.

Chapter 2 describes OFCC and its behavior in presence of nonidealities. Thereafter OFCC realization based on CMOS and AD844 are placed which are used extensively to validate various proposals. The current and voltage transfer characteristics of OFCC are verified through SPICE simulations. Various OFCC based amplifier configurations such as voltage, current, transadmittance, transimpedance and voltage difference amplifier are used extensively in this work and are detailed. The MOS based resistor implementation [169] is also included which allows to achieve electronic tuning in proposed circuits.

A new first order TA mode filter is put forward in chapter 3. TA mode filters are class of filters that process voltage input and provide current output. These filters are useful where the system processing filter output is either CM or TIM. A VM or TIM filter in such cases require

voltage to current converter. Literature survey for TA mode first order filters is given followed by proposed filter description with its behavior analysis using nonidealities is presented. One filter application as an oscillator is also developed. The proposed filter uses two OFCCs, two resistors and one capacitor while one extra capacitor is used for oscillator. The functional verification of proposed filter and its application is carried out through SPICE simulations while application is also prototyped for experimental observation.

The chapter 4 presents an overview of available works on second order CM SIMO filters. A CM SIMO filter is presented which uses three OFCC, three grounded resistors and two grounded capacitors that makes it suitable from integration view point. This configuration offers all the five standard filter responses and filter parameters ω_o and Q_o can be tuned independently without affecting ω_o/Q_o. The Q_o can be tuned by varying R_3 only while keeping ω_o constant. The effect of nonidealities namely finite transimpedance gain, tracking errors and parasites on filter are analyzed. As an application a CM shadow bandpass filter is developed with introduction of feedback of LP, HP or BP to input through an amplifier. Such filters are used in baseband receivers. Both proposals verified through simulations while CM SIMO filter is prototyped for bandpass response. The observations confirm to the theoretical predictions.

Chapter 5 organization starts with an overview of available IAs followed by proposed generalized structure of IA. This generalized structure is categorized into two structures: Structure-I and Structure-II. Using these structures, eight topologies are derived which can operate in VM, CM, TIM and TAM modes. To reduce the number of passive components the structures I and II are modified. Six more IA topologies are derived from modified structures. All proposed topologies present proper impedances at input and output thereby avoiding extra active

blocks. The effect of nonidealities are analyzed on all derived topologies. A thorough comparison of all proposed IA topologies with existing one is also put forward in a tabulated format for better comparison.

In chapter 6 literature survey of available PGAs is presented followed by description of newly proposed OFCC based PGA. The proposed PGA works in transimpedance mode and processes data that is available from current sensor and provides voltage output for further processing. Digital coarse and fine gain tuning is the key feature of proposed PGA which is achieved by bits (B_5-B_0). The bits (B_5, B_4) provide coarse gain tuning while (B_3-B_0) are used to fine tune gain. A total of 60 gain settings are possible through appropriate control bits tuning. The proposal is verified through simulations and its performance is compared with those in literature available. Experimental verification is also done by bread boarding the entire circuit.

OFCC based CM half wave rectifiers (HWRs) and full wave rectifier (FWR) are put forward in chapter 7. Available rectifier structures are briefly reviewed prior to presenting the proposed rectifiers. These rectifiers do not use diode and are thus suitable for low voltage rectification. It is pertinent to mention here that all proposed rectifiers are resistor-less, use single active block and also offers suitable input and output impedance. MOS transistors are used as switches in both topologies so makes it suitable from integration view point. The workability of all rectifier circuits is confirmed through SPICE simulations.

8.3 FUTURE SCOPE

Technical and scientific research is a very vast field with a possibility to carry out research in multiple directions. A wide variety of research objectives can be formulated in a given specific

research area. However, a researcher is restricted by a variety of constraints such as time, resources and personal interest which makes it feasible to conduct research in a specific narrow area. This leaves a large area unexplored and still available to work upon.

In this thesis, the candidate has worked in the area of design and implementation of analog circuits using current mode building blocks and has directed his focus specific to signal processing circuits based on OFCC, however, as mentioned above, there is a possibility to explore more aspects of this research area. Some of the aspects which may immediately be addressed, are -

- Integration of low-voltage, low-power techniques such as bulk driven MOS, floating gate MOS, quasi floating gates, dynamic threshold MOS etc. can be integrated into the development of OFCC structure to come up with low voltage circuits in order to improve the performance.
- Signal generators are essentially employed in wide range of applications such as communication, measurement and instrumentation systems. Signal generators based on OFCC may be developed.
- Non-linear applications of OFCC may also be explored.

REFERENCES

REFERENCES

[1] Allen, P. E., Holberg, D. R.: CMOS analog circuit design. Oxford University Press, 3rd edition, 2011.

[2] Toumazou, C., Lidgey, F. J., Haigh, D. G.: Analogue IC Design: the current mode approach. IEE Circuits and Systems Series 2. Peter Peregrinus Ltd., 1990.

[3] Ferri, G., Guerrini, N. C.: Low-voltage low-power CMOS current conveyors. Cluwer Academic Publishers, 2003.

[4] Smith, K. C., Sedra, A.: The current conveyor-A new circuit building block. Proceedings of the IEEE, 56(8), pp. 1368-1369, 1968.

[5] Sedra, A., Smith, K. C.: A second-generation current conveyor and its applications. IEEE Transactions on circuit theory, 17(1), pp. 132-134, 1970.

[6] Fabre, A.: Third-generation current conveyor: a new helpful active element. Electronics Letters, 31(5), pp. 338-339, 1995.

[7] Toumazou, C., Payne, A., Lidgey, F. J.: Operational floating conveyor, Electronic letters, 27(8), pp. 651-652, 1991.

[8] Khan, A. A., Al-Turaigi, M. A., El-Ela, M. A.: Operational floating current conveyor: characteristics, modeling and applications. Proc. IEEE Instrum. and Meas. Tech. Conf., Hamamtsu, Japan, pp. 788-790, 1994.

[9] Palmisano, G., Palumbo, G., Pennisi, S.: A CMOS operational floating conveyor. In proceedings of the 37th Midwest Symposium on Circuits and Systems, IEEE, 2, pp. 1289-1292, 1994.

[10] Ghallab, Y. H., El-Ela, M. A., Elsaid, M. H.: Operational floating current conveyor: characteristics, modeling and experimental results. Proc. Int. Con. on Microelectron., Kuwait, pp. 59-62, 1999.

[11] Elsayed, F., Ibrahim, M. F., Ghallab, Y. H., Badawy, W.: A CMOS operational floating current conveyor circuit. In 4th International Design and Test Workshop (IDT), pp. 1-4, 2009.

[12] Edward, N. M., Ghallab, Y. H., Hassan, H. M., Ismail, Y. I.: A CMOS based operational floating current conveyor. In International Conference on Electronics, Circuits, and Systems (ICECS), IEEE, pp. 157-160, 2015.

[13] Hassan, H. M., Soliman, A. M.: Novel CMOS realizations of operational floating current conveyor and applications. J. of Circuits Sys. Comput. (JCSC), 14(6), pp. 1113–1143, 2005.

[14] Ghallab, Y. H., Badawy, W., Kaler, K. V. I. S., Maundy, B. J.: A novel current-mode instrumentation amplifier based on operational floating current conveyor. IEEE Trans. Instrum. Meas., 54(5), pp.1941-1949, 2005.

[15] Edward, N. M., Ghallab, Y. H., Mostafa, H., Ismail, Y. I.: A CMOS based operational floating current conveyor and its applications. In International Conference on Electronics, Circuits, and Systems (ICECS), IEEE, pp. 494-495, 2015.

[16] Ghallab, Y.H., Badawy, W., Kaler, K.V.: A novel pH sensor using differential ISFET current mode read-out circuit. In proc. International Conference on MEMS, NANO and Smart Systems, pp. 255-258, 2003.

[17] Ghallab, Y. H., Badawy, W.: A new differential PH sensor current mode readout circuit using only two operational floating current conveyor, IEEE International workshop on Biomedical Circuits & Systems, pp. 13-16, 2004.

[18] Ghallab, Y. H., Badawy, W.: A new design of a current-mode wheatstone bridge using operational floating current conveyor. International Conference on MEMS, NANO and Smart Systems, pp. 41-44, 2006.

[19] Ducu, D., Manolescu, A.: A continuous time sigma delta modulator with operational floating integrator. In International Semiconductor Conference (CAS-2012), 2, pp. 463-466, 2012.

[20] Ghallab, Y. H., Badawy, W.: The operational floating current conveyor and its applications. J. of Circuits Sys. Comput. (JCSC), 15 (3), pp. 351-372, 2006.

[21] Ghallab, Y. H., El-Ela, M. A., Elsaid, M.: A novel universal voltage-mode filter with three inputs and single output using only two operational floating current conveyor. In Proceedings of the 12th International Conference on Microelectronics, (ICM-2000), IEEE, pp. 95-98, 2000.

[22] Ghallab, Y. H., Badawy, W., Kaler, K. V. I. S., El-Ela, M. A., El-Said, M. H.: A new second order universal filter with single input and three outputs using operational floating current conveyor. Proc. International conference on Microelectronics (ICM-2002), IEEE, pp. 42-45, 2002.

[23] Parveen, T., Ahmed, M. T.: OFC based insensitive voltage mode universal biquadratic filter using minimum components. 4th International Conference on Computer Applications in Electrical Engineering Recent Advances, CERA-09, 2010.

[24] Parveen, T., Ahmed, M. T., Rajput, S. S.: Low voltage high quality multifunctional filter using operational floating conveyor. J. of Active and passive Electronic Devices, 5, pp. 21-28, 2010.

[25] Parveen, T., Ahmed, M. T., Rajput, S. S.: New low voltage high quality OFC based multifunctional filter using FDNR substitution for portable applications. J. of Active and passive Electronic Devices, 5, pp. 71-78, 2010.

[26] Sachan, D., Nand, D., Pandey, N.: Universal biquadratic filter using operational floating current conveyor. In 28th International Conference on Microelectronics (ICM-2016), IEEE, pp. 317-320, 2016.

[27] Parveen, T.: OFC based high input impedance first order and multifunctional biquadratic filter sections with grounded components and their higher order applications. TECHNIA International Journal of Computing Science and Communication Technologies, 4(1), pp. 710-713, 2011.

[28] Parveen, T.: CMOS compatible current mode high output impedance all pass filter using single OFC and grounded passive components. IEEE, International Conference on Multimedia, Signal Processing and Communication Technologies, pp. 107-109, 2011.

[29] Parveen, T.: OFC based high output impedance current mode SIMO universal biquadratic filter. IEEE, International Conference on Multimedia, Signal Processing and Communication Technologies, pp. 134-136, 2011.

[30] Pandey, N., Nand, D., Khan, Z.: Single-input four-output current mode filter using operational floating current conveyor. Active and Passive Electronic Components, 2013.

[31] Pandey, N., Nand, D., Khan, Z.: Operational floating current conveyor-based single-input multiple-output transadmittance mode filter. Arabian Journal for Science and Engineering, 39(11), pp.7991-8000, 2014.

[32] Gola, P., Tripathi, P., Pahalwan, P., Pandey, N., Pandey, R.: OFCC based shadow filter. i-Manager's Journal on Circuits & Systems, 4(2), p.38-44, 2016.

[33] Pandey, N., Tripathi, P., Pandey, R., Batra, R.: OFCC based logarithmic amplifier. International conference on Signal Processing and Integrated Networks (SPIN-2014), pp. 522-525, IEEE, 2014.

[34] Schaumann, R., Ghausi, M.S., Laker, K.R.: Design of analog filters: passive, active rc and switched capacitor, Prentice Hall, 1990.

[35] Maheshwari, S.: Current conveyor all pass sections: Brief review and novel solution. Scientific world Journal, 2013, pp. 1-6, 2013.

[36] Cicekli, H., Gokcen, A.: Synthesis of voltage mode all pass filter employing single current operational amplifier. Int. J. of Comm., 10, pp. 76-79, 2016.

[37] Pandey, N., Pandey, R., Paul, S. K.: A first order all pass filter and its application in a quadrature oscillator. Journal of Electron Devices, 12, pp.-772-777, 2012.

[38] Horng, J. W.: High input impedance first order allpass, highpass and lowpass filters with grounded capacitor using single DVCC. Indian J. of engg. and materials sciences, 17, pp. 175-178, 2009.

[39] Maheshwari, S., Khan, I. A.: Novel first order allpass sections using a single CCIII. Int. J. Electronics, 88(7), pp. 773-778, 2001.

[40] Saied, A. B., Salem, S. B., Masmoudi, D. S.: A quadrature oscillator based on a new Optimized DDCC all pass filter. J. of circuits and systems, 4, pp. 498-503, 2013.

[41] Tangsrirat, W., Tanjaroen, W., Pukkalanum, T.: Current mode multiphase sinusoidal oscillator using CDTA based allpass sections. Int. J. Electron. Commun.(AEU), 63, pp. 616-622, 2009.

[42] Mohan, J.: Single active element based current mode allpass filter. Int. J. of Comp. App., 82(1), pp. 23-27, 2013.

[43] Mohan, J., Maheshwari, S.: Cascadable current mode first order allpass filter based on minimal components. Scientific world Journal, 2013, pp. 1-5, 2013.

[44] Minaei, S.: A new high performance CMOS third generation current conveyor (CCIII) and its application. J. of Electrical engineering, Springer Verlag, 85, pp. 147-153, 2003.

[45] Cam, U.: A new transadmittance type first order allpass filter employing single third generation current conveyor. Analog Int. circuits and signal processing, 43, pp. 97-99, 2005.

[46] Herencsar, N., Lahiri, A., Koton, J., Sagbas, M., Ayten, U. E., Vrba, K.: New MOS-C realization of transadmittance type allpass filter using modified CBTA. In Int. conf. on applied electronics, IEEE, pp. 1-4, 2011.

[47] Herencsar, N., Koton, J., Vrba, K.: Differential input buffered and transconductance amplifier based new transadmittance and voltage mode first order allpass filters. In Int. conf. on Electrical and Electronics Engg., (ELECO-2009), pp. 256-259, 2009.

[48] Herencsar, N., Koton, J., Vrba, K., Metin, B.: Fully cascadable dual mode allpass filter based on single DBTA. 35th Int. conf. on telecomm. And signal processing, pp. 374-377, 2012.

[49] Sotner, R., Herencsar, N., Jerabek, J., Vrba, K., Dostal, T., Jaikla, W., Metin, B.: Novel first order allpass filter applications of z-copy voltage differencing current conveyor. Indian J. of pure and applied physics, 53, pp. 537-545, 2015.

[50] Parveen, T.: CMOS compatible current mode high output impedance allpass filter single OFC and grounded passive components," Int. Conf. on Multimedia, Signal Processing and Comm. Tech., IEEE, pp. 107-109, 2011.

[51] Sedra, A. S., Smith, K. C.: Microelectronic Circuits. Oxford University Press, 2004.

[52] Ibrahim, M. A., Minaei, S., Kuntman, H.: A 22.5 MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements. AEU-Int. J. Electron. Commun. 59(5), pp. 311–318, 2005.

[53] Herencsar, N., Koton, J., Vrba K.: Single CCTA-based universal biquadratic filters employing minimum components. Int. J. Comput. Electr. Eng. 1(3), pp. 307 – 310, 2009.

[54] Yüce E., Metin B., Cicekoglu O.: Current-mode biquadratic filters using single CCIII and minimum numbers of passive elements. Frequenz. 58(9-10), pp. 225-228, 2004.

[55] Tangsrirat, W.: Single-input three-output electronically tunable universal current-mode filter using current follower transconductance amplifiers. (AEU) Int. J. Electron. Commun. 65, pp. 783– 787, 2011.

[56] Wang, C.; Xu, J., Keskin, A.U., Du, S., Zhang, Q.: A new current-mode current-controlled SIMO-type universal filter. AEU Int. J. Electron. Commun. 65, pp. 231–234, 2011.

[57] Horng, J. W.: Current-mode and transimpedance-mode universal biquadratic filter using multiple outputs CCIIs. Indian J. Eng. Materials Sci. 17(3), pp. 169–174, 2010.

[58] Abdalla, K. K., Bhaskar, D. R., Senani, R.: Configuration for realizing a current-mode universal filter and dual-mode quadrature single resistor controlled oscillator. IET Circuits Devices Syst. 6(3), pp. 159–167, 2012.

[59] Qadir, A., Altaf, T.: Current mode canonic OTA-C universal filter with single input and multiple outputs. In: Proceedings of International Conference on Electronic Computer Technology (ICECT-2010), pp. 32–34, 2010.

[60] Satansup, J., Tangsrirat, W.: Single-input five-output electronically tunable current-mode biquad consisting of only ZC-CFTAs and grounded capacitors. Radioengineering. 20(3), pp. 650-656, 2012.

[61] Biolek, D., Biolkova, V., Kolka, Z., Bajer, J.: Single-input multi-output resistorless current-mode biquad. In: Proceedings of IEEE European Conference on Circuit Theory and Design. pp. 225-228, 2009.

[62] Senani, R., Singh, A. K.: A new universal current mode biquad filter. Frequenz. 56, pp. 55-59, 2002.

[63] Senani, R., Singh, A. K., Singh, V. K.: New tunable SIMO type current mode universal biquad using only three MOCCs and all grounded passive elements. Frequenz. 57(7-8), pp. 160–161, 2003.

[64] Senani, R., Singh, V. K., Singh, A. K., Bhaskar, D. R.: Novel electronically controllable current-mode universal biquad filter. IEICE Electronics Express (Japan). 1, pp. 410–415, 2004.

[65] Soliman, A. M.: Current-mode universal filters using current conveyors: classification and review. Circuits Syst. Signal Process. 27, pp. 405-427, 2008.

[66] Sağbaş, M., Köksal, M.: Current-mode state-vriable filter. Frequenz. 62, pp. 37- 42, 2008.

[67] Chunhua, W., Keskin, A. U., Yang, L., Qiujing, Z., Sichun, D.: Minimum configuration insensitive multifunctional currentmode biquad using current conveyors and all-grounded passive components. Radioengineering. 19(1), pp. 178–184, 2010.

[68] Abdalla, K. K.: Universal current-mode biquad employing dual output current conveyors and MO-CCCA with grounded passive elements. Circuits Syst. 4, pp. 83-88, 2013.

[69] Jerabek, J., Sotner, R., Vrba, K.: Comparison of the SITO current-mode universal filters using multiple-output current followers. In: Proceedings of the 35th Int. Con. Telecomm. Signal Process. (TSP-2012). pp. 406– 410, 2012.

[70] Yuce, E.: Current-mode electronically tunable biquadratic filters consisting of only CCCIIs and grounded capacitors. Microelectronics J. 40, pp. 1719-1725, 2009.

[71] Kumngern, M.: A new current-mode universal filter with single-input five-output using trans-linear current conveyors. Aust. J. Electr. Electron. Eng. 9(2), pp. 177-184, 2012.

[72] Senani, R., Singh, B., Singh, A. K.: New universal current-mode biquad using only three ZC-CFTAs. Radioengineering. 21(1), pp. 273-280, 2012.

[73] Singh, S. V., Maheshwari, S., Chauhan, D. S.: Current-processing current-controlled universal biquad filter. Radioengineering. 21(1), pp. 317-323, 2012.

[74] Chen, H.P.: Versatile current-mode universal biquadratic filter using DO-CCIIs. Int. J. Electron. 100(7), pp. 1010-1031, 2013.

[75] Chen, H.P.: Current-mode dual-output ICCII-based tunable universal biquadratic filter with low-input and high-output impedances. Int. J. Circuit Theory Appl. 42(4), pp. 376-393, 2014.

[76] Kumngern, M., Phasukkit, P., Junnapiya, S., Khateb, F., Tungjitkusolmun, S.: ECCCII-Based Current-Mode Universal Filter with Orthogonal Control of ω_o and Q. Radioengineering. 23(2), pp. 687-696, 2014.

[77] Singh, S.V., Tomar, R.S., Chauhan, D.S.: Single CFTA Based Current-Mode Universal Biquad Filter. The J. Eng. Research (TJER). 13(2), pp. 172-186, 2016.

[78] Arora, T.S., Gupta, M., Gupta, S.: Current mode universal filter employing operational transconductance amplifier and third generation current conveyor. In: IEEE Int. Con. on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), IEEE, pp. 1-4, 2016.

[79] Abaci, A., Yuce, E.: A new DVCC+ based second-order current-mode universal filter consisting of only grounded capacitors. J. Circuits Syst. Comput. 26(9), 1750130, 2017.

[80] Fabre, A., Dayoub, F., Duruisseau, L., Kamoun, M.: High input impedance insensitive second-order filters implemented from current conveyors. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 41(12), pp. 918-921, 1994.

[81] Lakys, Y., Fabre, A.: Multistandard transceivers: State of the art and a new versatile implementation for fully active frequency agile filters. Analog Integr. Circuits Signal Process. 74(1), 63-78, 2012.

[82] Pandey, N., Sayal, A., Choudhary, R., Pandey, R.: Design of CDTA and VDTA based frequency agile filters. Advances in Electronics. 2014, 1-15, 2014.

[83] Roy, S. C. D.: 'Shadow' Filters-A new family of electronically tunable filters. IETE J. Education. 51(2-3), 75-78, 2010.

[84] Lakys, Y., Fabre, A.: Shadow filters generalization to nth-class. Electron. Lett. 46(14), 985-986, 2010.

[85] Abuelma'atti, M.T., Almutairi, N.R.: New current-feedback operational-amplifier based shadow filters. Analog Integr. Circuits Signal Process. 86(3), 471-480, 2016.

[86] Lakys, Y., Fabre, A.: Shadow Filters - a new family of second order filters. Electronic Letters, 46(4), 276-277, 2010.

[87] Ghallab, Y. H., Badawy, W.: Lab-on-a-chip: techniques, circuits, and biomedical applications. Artech House, 2010.

[88] Pallas-Areny, R., Webster J. G.: AC instrumentation amplifier for bioimpedance measurements', IEEE Trans. on Biomedical Engineering, 40 (8), pp. 830-833, 1993.

[89] Wu, R., Huijsing, J. H., Makinwa, K. A. A.: 'Precision instrumentation amplifiers and read-out integrated circuits', Springer, 2013.

[90] Redoute, J. M., Steyaert, M.: EMC of analog integrated circuits. Springer, 2010.

[91] Miller, B. D., Sample, R. L.: Instrumentation amplifier IC designed for oxygen sensor interface requirements. IEEE Journal of Solid State Circ., 16(6), pp. 677-681, 1981.

[92] Schaffer, V., Snoeij, M. F., Ivanov, M. V., Trifonov, D. T.: A 36 V programmable instrumentation amplifier with sub-20 V offset and CMRR in excess of 120 dB at all gain settings. IEEE Journal of Solid State Circ., 44(7), pp. 2036-2046, 2009.

[93] Rahal, M., Demosthenous, A.: A synchronous chopping demodulator and implementation for high frequency inductive position sensors. IEEE Trans. Instrum. Meas., 58(10), pp. 3693-3701, 2009.

[94] Steyaert, M. S. J., Sansen, W. M. C., Zhongyuan, C.: A micropower low noise monolithic instrumentation amplifier for medical purposes. IEEE Journal of Solid State Circ., 22(6), pp. 1163-1168, 1987.

[95] Martins, R. Selberherr, S., Vaz, F. A.: A CMOS IC for portable EEG acquisition systems. IEEE Trans. Instrum. Meas., 47(5), pp.1191-1196, 1998.

[96] Wilson, B.: Universal conveyor instrumentation amplifier. Electron. Lett., 25, (7), pp. 470-471, 1989.

[97] Szynowski, J.: CMRR analysis of instrumentation amplifiers. Electron. Lett., 19, (14), pp. 547-549, 1983.

[98] Areny, R. P., Webster, J. G.: Common mode rejection ratio in differential amplifiers. IEEE Trans. Instrum. Meas., 40(4), pp. 669-676, 1991.

[99] Areny, R. P., Webster, J. G.: Common mode rejection ratio for cascaded differential amplifier stages. IEEE Trans. Instrum. Meas., 40(4), pp. 677-681, 1991.

[100] Toumazou, C., Lidgey, F. J.: Novel current mode instrumentation amplifier. Electron. Lett., 25(3), pp. 228-230, 1989.

[101] Zhu, Q. S., Lidgey, F. J., Su, W. J.: High CMRR, second generation current mode instrumentation amplifiers. Int. Symp. on Circuits and Systems (ISCAS-1993), Chicago, 2, pp. 1326-1328, 1993.

[102] Khan, A. A., Al-Turaigi, M. A., Abou El-Ela, M.: An improved current mode instrumentation amplifier with bandwidth independent of gain. IEEE Trans. Instrum. Meas., 44(4), pp. 887-891, 1995.

[103] Galanis, C., Haritantis, I.: An improved current mode instrumentation amplifier', Proc. Int. Conf. Electronics, Circuits, and Systems, Rodos,1, pp. 65-68, 1996.

[104] Azhari, S. J., Fazlalipoor, H.: A novel current mode instrumentation amplifier (CMIA) topology. IEEE Trans. Instrum. Meas., 49(6), pp. 1272-1277, 2000.

[105] Koli, K., Halonen, K. A. I.: CMRR enhancement techniques for current mode instrumentation amplifiers. IEEE Trans. Circuits Syst., 47(5), pp. 622-632, 2000.

[106] Gift, S. J. G.: An enhanced current mode instrumentation amplifier. IEEE Trans. Instrum. Meas., 50(1), pp. 85-88, 2001.

[107] Maheshwari, S.: High CMRR wide bandwidth instrumentation amplifier using current controlled conveyors. Int. J. Electron., 89(12), pp. 889-896, 2002.

[108] Babaei, B., Mirzakuchaki, S.: High CMRR, low power and wideband current mode instrumentation amplifier', 24th Norchip Conf., Linkoping, Sweden, pp. 121-124, 2006.

[109] Babaei, B., Mirzakuchaki, S.: High CMRR and low THD current mode instrumentation amplifier using current inversion technique. 25th Norchip Conf., Aalborg, Denmark, pp. 1-4, 2007.

[110] Gift, S. J. G., Maundy, B., Muddeen, F.: High performance current mode instrumentation amplifier circuit. Int. J. Electron., 94(11), pp. 1015-1024, 2007.

[111] Ercan, H., Tekin, S. A., Alci, M.: Voltage and current controlled high CMRR instrumentation amplifier using CMOS current conveyors. Turk J. Elec. Eng. and Comp. Sci., 20(4), pp. 547- 556, 2012.

[112] Ren, M. Y., Zhang, C. X., Sun, D. S.: Design of CMOS instrumentation amplifier. Int. Workshop on Information and Electronics Engg. (IWIEE), Harbin, China, 29, pp. 4035-4039, March 2012.

[113] Kaulberg, T.: A CMOS Current-mode operational amplifier. IEEE J. of solid-state circuits, 28(7), pp. 849-852, 1993.

[114] Zhu, Q.S., Lidgey, F.J., Vere Hunt, M.A.: Improved wide-band, high CMRR instrumentation amplifier', Clin. Phys. Physiol. Meas., 13, Suppl. A, pp. 51-55, 1992.

[115] Safari, L., Minaei, S.: A novel resistor free electronically adjustable current mode instrumentation amplifier. Circuits Syst. Signal Process, 32, pp. 1025-1038, 2013.

[116] Agouridis, D. C., Fox, R. J.: Transresistance instrumentation amplifier. Proc. of the IEEE, 66(10), pp 1286-1287, Oct. 1978.

[117] Pandey, R., Pandey, N., Paul, S. K.: Electronically tunable transimpedance instrumentation amplifier based on OTRA. J. of Engineering, Article ID 648540, pp 1-5, 2013.

[118] Yuce, E., Minaei, S.: New CCII-based versatile structure for realizing PID controller and Instrumentation amplifier. Microelec. J. (MEJ), 41, pp. 311-316, 2010.

[119] Prior, C. A., Rodrigues, C. R., Aita, A. L., Martins, J. B. D. S., Vieira, F. C. B.: Design of an integrated low power high CMRR instrumentation amplifier for biomedical applications. Analog Integrated Circuit Signal Process., 57, pp. 11-17, 2008.

[120] Mehr, I., Paterson, D., Abaskharoun, N., Lloyd, J., L'Bahy, H., DeSimone, A.: An integrated mixed-signal front-end for broadband modems. IEEE Symp. VLSI Circuits Dig. Tech. Papers, pp. 38–41, 2002.

[121] Jung, W. G.: Op Amp Applications Handbook. Newnes, 2005.

[122] Mahmoud, S. A.: Low voltage current-mode digitally controlled VGA based on digitally programmable current conveyors. 51st IEEE Midwest Symposium on Circuits and Systems, pp. 814-817, 2008.

[123] Mahmoud, S. A.: Low voltage high current gain CMOS digitally controlled fully differential CCII. IEEE International Symposium on Circuits and Systems, pp. 1000-1003, 2005.

[124] Farag, F. A., Khalaf, Y. A.: Digitally controlled variable gain amplifier based on current conveyor with opamp and inverters only. 22nd International Conference on Microelectronics. Pp. 224-227, 2010.

[125] Chao, H. L., Ma, D.: CMOS variable-gain wide-bandwidth CMFB-free differential current feedback amplifier for ultrasound diagnostic applications. IEEE International Symposium on Circuits and Systems, pp. 649–652, 2006.

[126] Mahmoud, S. A., Awad, I. A.: Fully differential CMOS current feedback operational amplifier. Journal of Analog Integrated Circuits and Signal Processing, 43(1), pp. 61–69, 2005.

[127] Hsu, C. C., Wu, J. T.: A highly linear 125 MHz CMOS switched-resistor programmable-gain amplifier. IEEE J. Solid-State Circuits, 38(10), pp. 1663–1670, 2003.

[128] Rahmatian, B., Mirabbasi, S.: A low-power 75-dB digitally programmable variable-gain amplifier in 0.18 μm CMOS. Canadian J. of Electrical and Computer Engineering, 32(4), pp. 181–186, 2007.

[129] Wang, Y., Koen, M., Ma, D.: Low-Noise TGC Amplifier with Adaptive Gain Control for Ultrasound Imaging Receivers. IEEE Trans. Circuits Syst. II: Express Briefs. 58(1), pp. 26-30, 2011.

[130] Tsai, P. K., Ku, P. C., Lu, C. C., Shih, C. M., Lu, L. H.: A precise decibel-linear programmable gain amplifier for ultrasound imaging receivers. Int. Symp. on VLSI Design, Automation and Test. pp. 1-4, 2016.

[131] Nguyen, H. H., Nguyen, H. N., Lee, J. S., Lee, S. G.: A binary-weighted switching and reconfiguration-based programmable gain amplifier. IEEE Trans. Circuits Syst. II, Express Briefs, 56(9), pp. 699-703, 2009.

[132] Tsou, S. C., Li, C.F., Huang, P. C.: A low-power CMOS linear-in-decibel variable gain amplifier with programmable bandwidth and stable group delay IEEE Trans. Circuits Syst. II, Express Briefs, 53(12), pp. 1436-1440, 2006.

[133] Kang, S. Y., Ryu, S. T., Park, C. S.: A precise decibel-linear programmable gain amplifier using a constant current-density function. IEEE Trans. Microwave Theory and Tech, 60(9), pp. 2843-2850, 2012.

[134] Elwan, H., El Adawi, A., Ismail M., Olsson, H. K., Soliman, A.: Digitally controlled dB-linear CMOS variable gain amplifier. Electronics Letters, 35(20), pp. 1725-1727, 1999.

[135] Angkeaw, K., Prommee, P.: Two digitally programmable gain amplifiers based on current conveyors. Analog Int. Cir. Sig. Proc, 67(2), pp. 253-260, 2011.

[136] Mahmoud, S. A.: New fully differential CMOS second generation current conveyor. ETRI Journal, 28(4), pp. 495–501, 2006.

[137] Chen, C-C., Lu, N. K., Zeng, Y. Z.: Low gain error, linear-in-dB variable gain amplifier with programmable gain range and gain steps. Intr. J. Electron. Commun. (AEU), 64, pp. 1203-1206, 2010.

[138] Cheng, X., Zhang, L., Deng, X.: High-dynamic-range programmable gain amplifier with linear-in-dB and DAC gain control. Analog Integrated Circuits and Signal Processing, 94(1), pp. 83-96, 2018.

[139] Pourashraf S., Ramirez-Angulo J., Lopez-Martin A.J., Carvajal R.G., Díaz-Sánchez A.: ±0.18-V supply voltage gate-driven PGA with 0.7-Hz to 2-kHz constant bandwidth and 0.15-μW power dissipation. International Journal of Circuit Theory and Applications., 46(2), pp. 272-279, 2018.

[140] Li, Y.T., Liu, Z.R., Wu, Y.H., Chi, B.Y.. A wideband and high linearity Programmable Gain Amplifier for 60GHz receiver in 65nm CMOS. In 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT) IEEE, pp. 1549-1551, 2016.

[141] Severo L., Van Noije W.: 0.36 V PGA combining single-stage OTA and input negative transconductor for low energy RF receivers. Electronics Letters., 54(5), pp. 319-320, 2018.

[142] Zhang H., Li X., Chen Y., Cheng J.: A switched-capacitor programmable-gain amplifier for high-definition video analog front-ends. In 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT) IEEE, pp. 1-3, 2012.

[143] Shen, X., Yan, T., Lu, Y., Zhou, J.: A 0.25 dB gain step high linear programmable gain amplifier. In 9th International Conference on ASIC (ASICON) IEEE, pp. 1062-1065, 2011.

[144] Gift, S. J. G.: A high performance full-wave rectifier circuit, International Journal of Electronics, 87, pp. 925–930, 2000.

[145] Gift, S. J. G., Maundy, B.: Versatile precision full-wave rectifiers for instrumentation and measurement, IEEE Transaction on Instrumentation and Measurement, 56, pp. 1703–1710, 2007.

[146] Djukic, S. R.: Full-wave current conveyor precision rectifier, Serbian Journal of Electrical Engineering, 5, pp. 263–271, 2008.

[147] Hayatleh, K., Porta, S., Lidgey, F.: Temperature independent circuit conveyor precision rectifier, Electronics Letters, 30, pp. 2091-2093, 1994.

[148] Agarwal, D., Maheshwari, S.: Current-Mode Precision Full-Wave Rectifier Circuits. Circuits Syst. Signal Process, 2017.

[149] Minaei, S., Yuce, E.: A new full-wave rectifier circuit employing single dual-X current conveyor. Int. J. Electron. 95(8), pp. 777–784, 2008.

[150] Maheshwari, S.: Current controlled precision rectifier circuits. J. Circuits Syst. Comput. 16(1), 129–138, 2007.

[151] Kumngern, M., Dejhan, K.: High frequency and high precision CMOS full-wave rectifier. Int. J. Electron.93(3), 185–199, 2006.

[152] Maheshwari, S., Ansari, M.S., Beg, P.: High performance precision rectifier for analog signal processing.Int. J. Comput. Appl. 47(14), 26–29, 2012.

[153] Kumngern, M.: New versatile precision rectifier. IET Circuits Device Syst. 8(2), 141–151, 2014.

[154] Ibrahim, M.A., Yuce, E., Minaei, S.: A new DVCC-based fully cascadable voltage-mode full-wave rectifier. J. Comput. Electron. 15(4), 1440–1449, 2016.

[155] Beg, P., Khan, I.A., Maheshwari, S.: Biphase amplifier based precision rectifiers using current conveyors.Int. J. Comput. Appl. 42(3), 14–18, 2012.

[156] Biolek, D., Hancioglu, E., Keskin, A.Ü.: High-performance current differencing transconductance amplifier and its application in precision current-mode rectification. Int. J. Electron. Commun. 62(2), 92–96, 2008.

[157] Khateb, F., Vavra, J., Biolek, D.: A novel current-mode full-wave rectifier based on one CDTA and two diodes. Radioengineering 19(3), 437–445, 2010.

[158] Koton, J., Herenscar, N., Vrba, K.: Current and voltage conveyors in current and voltage-mode precision full-wave rectifiers. Radioengineering 20(1), 19–24, 2011.

[159] Sagbas, M., Minaei, S., Ayten, U.E.: Component reduced current-mode full-wave rectifier circuits using single active component. IET Circuits Device Syst. 10(1), 1–11, 2016.

[160] Monpapassorn, A., Dejhan, K., Cheevasuvit, F.: A full-wave rectifier using a current conveyor and current mirrors. Int. J. Electron. 88(7), 751–758, 2001.

[161] Toumazou, C., Lidgey, F.J., Chattong, S.: High frequency current conveyor precision full- wave rectifier. Electron. Lett. 30(10), 745–746, 1994.

[162] Anuntahirunrat, K., Tangsrirat,W., Riewruja, V., Surakampontorn, W.: Sinusoidal frequency doubler and full-wave rectifier using translinear current controlled conveyors The IEEE Asia-Pacific Conf. on. Circuits and Systems, (APCCAS), pp. 166–169, 2000.

[163] Kumngern, M.: High frequency and high precision CMOS fullwave rectifier. IEEE International Conference on Communication Systems (ICCS), pp. 5–8, 2010.

[164] Yuce, E., Minaei, S., Cicekoglu, O.: Full-wave rectifier realization using only two CCII+s and NMOS transistors. Int. J. Electron. 93(8), 533–541, 2006.

[165] Erkan, S., Ayten, U.E., Sagbas, M.: Current mode full wave rectifier circuits using current differencing buffered amplifier. 38th Int. Conf. on Telecommunications and Signal Processing (TSP-2015), Prague, Czech Republic, pp. 344-348, 2015.

[166] Monpapassorn, A.: Low output impedance dual CCII full-wave rectifier. Int. J. Electron. 100(5), 648–654, 2013.

[167] Basak, M.E., Kacar, F.: A new fully integrated high frequency fullwave rectifier realization. Inf. Midem J. Microelectron. Electron. Compon. Mater. 45(2), 101–109, 2015.

[168] Biolek, D., Senani, R., Biolkova, V. and Kolka, Z.: Active elements for analog signal processing: classification, review, and new proposals. Radioengg., 17(4), pp.15-32, 2008.

[169] Wang, Z.: 2-MOSFET transresistor with extremely low distortion for output reaching supply voltages. Electron. Lett., 26(13), 951-952, 1990.

[170] “Analog devices, 60 MHz, 2000V/μs, Monolithic Op Amp” Analog Devices Inc., AD844 datasheet, pp. 1-12.

LIST OF PUBLICATIONS

[1] **Deva Nand**, Neeta Pandey, **"Transadmittance Mode First Order LP/HP/AP Filter and its Application as an Oscillator"** *IOP Conf. Ser.: Mater. Sci. Eng.*, 225 (012150), 2017. **(Scopus)** *DOI: 10.1088/1757-899X/225/1/012150*

[2] **Deva Nand**, Neeta Pandey, **"New Configuration for OFCC based CM SIMO filter and its application as Shadow filter"** *Arabian Journal for Science and Engineering **(Springer)***, 43, pp. 3011-3022, 2018. **(SCIE)** *DOI: 10.1007/s13369-017-3058-1*

[3] Neeta Pandey, **Deva Nand,** Rajeshwari Pandey, **"Generalized Operational Floating Current Conveyor based Instrumentation Amplifier"** *IET Circuits Devices and Systems*, 10 (3), pp. 209-219, 2016. **(SCI)** *DOI: 10.1049/iet-cds.2015.024*3

[4] **Deva Nand**, Neeta Pandey, Rajeshwari Pandey, Prateek Tripathi, and Prashant Gola, **"OFCC based voltage and transadmittance mode instrumentation amplifier"**, *AIP Conference Proceedings*, 1859 (020109), 2017. **(Scopus)** *DOI: 10.1063/1.4990262*

[5] Neeta Pandey, **Deva Nand,** V. Venkatesh Kumar, Varun Kumar Ahalawat, Chetna Malhotra, "**Realization of OFCC based Transimpedance Mode Instrumentation Amplifier**" *Journal of Advances in Electrical and Electronic Engineering*, 14 (2), pp. 162-167, 2016. **(Scopus)** *DOI*: *10.15598/aeee.v14i2.1551*

[6] **Deva Nand**, Neeta Pandey, **"A new proposal for OFCC based Instrumentation amplifier"** *International Journal of Electrical and Computer Engineering (IJECE)*, 7 (1), pp. 134-143, 2016. **(Scopus)** *DOI: 10.11591/ijece.v7i1.pp134-143*

[7] Prateek Pahalwan, Prateek Tripathi, Prashant Gola, Neeta Pandey, **Deva Nand, "Programmable Gain Amplifier using Operational Floating Current Conveyors"** *Int. Journal of Electronics and Communications, AEU,* ***(Elsevier)****,* 90, pp. 163-170, 2018. **(SCI)** *DOI: 10.1016/j.aeue.2018.04.022*

[8] Neeta Pandey, Rajeshwari Pandey, **Deva Nand** and Abhishek Kumar, "**Current mode rectifier configuration based on OFCC**" *IEEE International Conference on Signal Propagation and Computer technology (ICSPCT-2014),* Ajmer, pp. 533-536, 2014. *DOI: 10.1109/ICSPCT.2014.6884960*

AUTHOR'S BIOGRAPHY

DEVA NAND

Assistant Professor

Department of Electronics and Communication Engineering

Delhi Technological University, Delhi, India

Email: devanand@dtu.ac.in

Deva Nand received his Bachler of Technology (B.Tech.) in Electronics and Communication Engineering from Kurukshetra University, Kurukshetra, Haryana, India in year 2005 and Master of Technology (M.Tech.) in Microelectronics and VLSI Design from U.I.E.T., Kurukshetra University, Kurukshetra, Haryana, India in year 2007. Presently he is working as an Assistant Professor in the department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India-110042. His research interests are analog circuit design, VLSI design and digital system design.