MICROGRID OPERATION

AND

CONTROL

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MICROGRID OPERATION
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by

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सा विद्या या विमुक्तये !

CERTIFICATE

This is to certify that the thesis entitled **"Microgrid Operation and Control"** being submitted by **Mr. Ashutosh Trivedi** for the award of degree of Doctor of Philosophy in the Department of Electrical Engineering, Delhi Technological University, Delhi, is the record of student's own work carried out by him under my supervision. The contents of this research work have not been submitted in part or full to any other university or institute for award of any degree.

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ABSTRACT

Due to everlasting electricity demand, the worldwide power system networks are under tremendous pressure and there is very strong need of strengthening our infrastructure related to power generation and transmission capabilities. However, with rising concern about the environmental issues of conventional generation and their limited resources, a lot of emphasis is being given to renewable energy sources (RES) based distributed generation (DG). As per the nomenclature the DG'S are to be integrated to main grid at distribution level and this eliminate the need of installing newer centralized power generation facilities and corresponding transmission line infrastructure. The integration of RES at distribution level has its own demerits primarily related to their intermittency and control. Recently, the concept of Microgrid is gaining lot of attention worldwide, as it can be very helpful in controlling the RES both in grid tie mode as well as in island mode. Thus, the microgrid may have its own generation and load, where it can remain grid tie in case of normal operation while it can isolate itself and keeps on feeding the localized load in case of any fault on grid side. However, microgrid has many issues regarding their operation, stability, power quality and protection. Moreover, most of the microgrid technology involves power electronics based interface which makes it almost inertia less system. Thus, the inherent advantage of transient stability by virtue of inertia is lost in case of microgrid. Therefore, to achieve stable operation of microgrid with enhanced power quality under intermittent generation and dynamic load conditions are one of the major issues. In modern distribution system, most of the loads are non-linear in nature and draw harmonic current. The variable load with the non-linear characteristics may distort the output voltage and degrade the power quality. Hence, major requirements of microgrid is to keep on feeding its connected load at regulated voltage and frequency with stable operation in transient condition, which are difficult to achieve especially in inverter based microgrid. The various control methodologies and control layers (Primary, secondary and tertiary etc.) have been used in past literature to overcome these issues. Therefore, the proposed research mainly deals with the two problems, first one is improvement of power quality under harmonic and unbalance load condition

and second is the stable operation of microgrid having reconfigurable architecture which leads to huge variation in grid parameters. For the first problem, a novel repetitive control has been used to enhance power quality of voltage source inverters in droop based microgrid while for second problem a L_1 based droop controller has been proposed. It is well known that variation in grid parameters may not be easily handled by conventional droop controllers which are mainly designed while assuming fixed grid configuration. However, these assumptions become invalid for a microgrid having small mesh network with reconfigurable structure. Therefore, it is most important for a microgrid to remain stable not only during various changes in droop characteristics but also during dynamic topological changes. For validation of methods and control strategy, real world hardware prototype has been developed. The hardware consists of two inverters (3-ph) with battery sources connected via variable transmission line impendences. Various types of load are connected to output of inverters and common points. These inverters are controlled by FPGA development board.

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List of Symbols and Abbreviations

$\alpha\beta$ Direct and Quadrature Axis Transformed Quantities in Fixed Reference Frame

δ Power Angle

ω_c Corner frequency of Filter

ω Frequency in radian / second

θ Phase angle

C_f Capacitance in a Filter

dq Direct and Quadrature Axis Transformed Quantities in Synchronous Reference Frame

E Sending End Voltage

f_s Swtiching Frequency

L_1, L_2, L_∞ Norms in Lebesgue space

n_v, n_f Voltage and Frequency Droop Coeffcient Respectively

P Active Power (if not specified) , Plant Transfer Function

Q Reactive Power

R_c Resistance in Series of Capacitor in a Filter

R_f Equivelent Series Resister of Inductor in a Filter

V Receiving End Voltage

$V_{a,b,c}, I_{a,b,c}$ Three Phase Voltage and Current Quantiteis

X	Reactance (if not specified), States in Variable or Function
Z	Complex Impedance
AC, DC	Alternating Current and Direct Current
ADC	Analog to Digital Converter
AMI	Advance Metering Infrastructure
CERTS	Consortium for Electric Relibility Technology Solutions
CHP	Combined Heat and Power
CIGRE	International Council on Large Electric Systems
CT	Current Transformer
DDS	Direct Digital Synthesis
DEM	Demand Energy Management
DG	Distributed Generators
DR	Distributed Resources
DSP	Digital Signal Processor
FPGA	Field Programble Gate Array
GOI	Governement of India
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-Gate Bipolar Transistor
IMP	Internal Model Principle
LV	Low Voltage
MCB	Miniature Circuit Breaker
MG	Microgrid
MNRE	Ministry of New and Renewable Energy, India

PCC	Point of Comon Coupling
PHC	Primery Health Centre
PI	Proportional plus Integral
PR	Proportional plus Resonant
PT	Potential Transformer
PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Repetitive Controller
REDCO	Renewable Energy Development Cooperative
RES	Renewable Energy Resources
SOC	State of Charge
SPV	Solar Photo Voltaic
SRF	Synchronous Reference Frame
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TPDDL	Tata Power Delhi Distribution
UPS	Unintruptable Power Supply
VHDL	Very high-speed integrated circuit Hardware Description Language
VSI	Voltage Source Inverter
EPS	Electric Power System

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CHAPTER 1

INTRODUCTION

Electricity is the most useful and efficient form of energy amongst various other forms of available energies owing to its various advantages such as, transmittability, controllability, storability, ease of use and clean in use etc. Conventionally, electricity is generated by burning of fossil fuels (e.g. coal, gas or petroleum) in thermal power plants or by water in hydro power plants. In thermal power plants superheated steam produced by combustion of fossil fuels is used to run steam turbines which in turn run the electromagnetic energy conversion devices such as synchronous generators. Whereas, in hydro power plants the potential energy of stored water in the dam is used to run the hydro turbine coupled with the generator. The availability of fossil fuels is the main constraint for the thermal power plant while availability of site with huge water resources or continuous availability of water is the main hindrance in the development of these plants. So, generally these power plants are away from load centers. The generated power from these plants is transported to the distant load centers through an interconnected network of transmission lines known as Electric Power System (EPS) or widely known as grid. The operation of EPS or grid is dynamic and have to continuous control its generation in order to meet the variable load demand. Any mismatch between supply and demand beyond a permissible limit may endanger the healthy state of the grid in terms of voltage and frequency. Rotating mass of generators plays a vital role in stabiliging grid by absorbing small mismatch in demand and supply. The kinetic energy stored in rotating mass may be released quickly to meet the sudden increase in load demand with slight decrease in speed. similarily it can absorb some energy by increasing its speed whenever a big load is suddenly switched off

[1]. So, it is evident that larger the number of interconnected generators, greater is the inertia and hence, greater is the stability provided by cushioning effect of inertia. Moreover, the electric power generated by sources reaches to the load in a unidirectional way which makes the system behaviour more predictive and less complex in terms of operation and control of EPS. Fault detection and protection schemes become more reliable and accurate. Since, conventional generation has been in use over a long time and due to their vast utilization or exploitation, the demerits of conventional generation have almost outweigh their merits. It can better be understood in terms of wide spread threat of global warming and visualizing the global warming and excessive environmental pollution caused by burning of fossil fuels. Depletion of conventional resources is also another matter of concern for the sustainable growth of society while discharging our duty in saving scarce fossil resources for our future generation. Recent technological advancement has made it possible to harness the renewable energy and thereby can provide the substitute of conventionally generated power. Renewable resources are intermittent in nature [2]. Use of energy storage devices such as battery and Combined Heat and Power (CHP) can compensate the intermittency effect of renewable resources. Electric power taped from Solar photo voltaic (SPV) systems and from Wind Conversion Energy Systems can together be used to meet the local load demand. These sources can be interconnected with the conventional grid along with loads. This interconnected network of renewable energy resources and loads is known as microgrid. A microgrid can be used to supply a local load only or can be connected to the conventional grid for the bidirectional transfer of power in case of deficit / excess of power generated from DRs. This bidirectional flow of power makes the EPS operation, protection and control more complex.

1.1 Microgrid and its Requirement

Owing to intermittent nature of renewable resources they fail to provide a reliable power to the load [3]. That is why DRs mainly work in support of main EPS and not as a backup facility. With the advancement of energy storage technologies interconnected DRs can be used to cater the local load demand in the case of

unavailibvilty or failure of main grid. This operation is known as autonomous or stand-alone operation of microgrid. Microgrids are able to serve a load fully or partially thereby reducing power demand from the conventional grid. In case power generated through DRs exceeds the local demand, it can be exported to main grid, when connected to main grid. Thus, the operation of microgrid reduces the demand from the main grid. The reduced power demand from the main grid will certainly reduce the use of conventional resources like fossil fuels. Development of microgrids can empower the society in various aspects. The salient features and future aspects of microgrids towards the development of society could be as follows:

a) **Improved Reach:** Renewable energy resources are available everywhere in abundance. Sunshine is available through the day while wind may be available round the clock. So, a microgrid can be formed near to local load. This can help the rural areas or societies where main grid is still a distant dream. Otherwise also if main grid is available, formation of a microgrid enhances the relaibility of service in addition to meet the local load demand. Therefore, forming a microgrid in a metropolitan or at a far remote place is equally realizable and beneficial in addition to meet the demand locally.

b) **Economics:** The monetary aspects regarding the formation, operation and maintenance of microgrids are equally important. Economics can better be understood by considering the fact that electricity demand is increasing day by day and to meet this increased demand from conventional generation, it needs augmentation in generation capacity and reinforcement of existing transmission lines to transfer the increased amount of power. These additional provisions will require additional capital cost. Whereas the initial cost of forming a microgrid is somewhat high but in fact this cost is very economical because running and maintenance costs are very less. Furthermore, the life span of energy conversion devices is considerable longer, Internal Rate of Return (IRR) becomes high. Consumers can participate in generation

so as they also can manage their economies and practically it results in a flat load demand curve paving the way for establishment of ideal trade based market.

c)   **Social Inclusion and Welfare:** Renewable energies are available freely to all mankind irrespective of rich or poor. The societies living away from main grid can be empowered to develop themselves through operation and management of renewable energy resources through co-operative efforts. Availability of power to such areas will generate sources of living by creating small markets having facilities like ICT, glossary shops with cold or hot preservation systems, vaccine preservation through refrigerators etc. Local people can be encouraged to form and operate microgrids through community based ownership management. In nutshell microgrids can prove a boon for the development of under privileged societies living without access to electricity.

d)   **Future Grid:** Pertaining to the numerous advantages, government agencies are promoting the use of renewable resources to meet energy demands. The most burgeoning issue of environmental and ecology degradation necessitates the use of renewable energies to save the earth. Recently MNRE GOI has proposed setting up of 1000 microgrids across India. With the pace of advancement in the field of energy conversion techniques, power electronics devices and storage energy techniques, it can rightly be said that microgrids have the potential to become a important component of the future grid.

1.2   Role of RES in Microgrid

In Microgrid all type of sources can be incorporated including conventional fossil fuel types and non-conventional renewables. However, inclusion of higher number of RES will increase the efficiency of microgrid and reduce the carbon emission for energy generation. The new trend in electric power generation shows that more number of countries are promoting RES in their distribution system. These countries are also promoting microgrid based on RES to integrate all the sources to

improve reliability and additional benefits. Table 1.1 to Table 1.3 show that RES capacity / generation share in world's major countries. The RES share shows a considerable increase in total electric power generation. China tops in all segment of power generation and has maximum share of RES capacity in the world. India is ranked at 4th position in wind energy generation far behind from USA and China but having growth of 12% per year which is slightly behind from china [4, 5, 6].

Table 1.1 – WIND ENERGY GENERATION -WORLD

S.No.	NAME OF THE COUNTRY	TOTAL CAPACITY(2015)	TOTAL CAPACITY(2016)
1	CHINA	145 GW	168.4 GW
2	UNITED STATES	75 GW	83.2 GW
3	GERMANY	45GW	50 GW
4	INDIA	30 GW	33.6 GW
5	SPAIN	-	23 GW

Table 1.2 – SOLAR PV GENERATION-WORLD

S.No.	NAME OF THE COUNTRY	TOTAL CAPACITY(2015)	TOTAL CAPACITY(2016)
1	CHINA	43 GW	77.5 GW
2	JAPAN	35 GW	43.6 GW
3	GERMANY	40 GW	41.5 GW
4	UNITED STATES	26 GW	40.8 GW
5	ITALY	19 GW	21 GW
6	UK	10 GW	12 GW
7	INDIA	3 GW	7.1 GW

Table 1.3 – HYDRO ELECTRIC GENERATION -WORLD

S.No.	NAME OF THE COUNTRY	TOTAL CAPACITY(2015)	TOTAL CAPACITY(2016)
1	CHINA	300 GW	306.9 GW
2	BRAZIL	238 GW	243.3 GW
3	TURKEY	75 GW	75.8 GW
4	VIETNAM	38 GW	39.1 GW
5	INDIA	41.6 GW-	42.78 GW

Figure 1.1 shows a pie-chart of renewable energy sources capacity. It can be seen from wind source pie-chart that China ranks 1st among all the countries with

wind generation capacity of 168.4 GW in the year 2016. The countries United States, Germany, India and Spain are also in the list of top five countries with wind generation capacity of 83.2GW, 50GW, 33.6GW and 23 GW in 2016. In 2016 solar PV generation, China is again at the first position in worldwide with 77.5 GW capacity. India got the 7th rank worldwide in solar-PV generation with 7.1 GW capacity. Also in hydro power generation, China ranks ahead of all the countries with 308.9 GW capacity . India is on 5th position with 42.78 GW of hydro power capacity. Figure 1.2 shows a pie-chart of power generation capacity share in India. In 2015, only 27% power generation is achieved through renewable energy sources and remaining 73% generation from fossil fuels(like diesel, nuclear, gas, coal). But in 2016,share of renewable energy sources is increased to about 1% and reached at 28% and reduces fossil fuel generation from 73% to 72%. Nowadays ,use of renewable energy sources increases which provide clean energy and these sources are available in abundance. As in 2017,this increase of RES power generation reached to 31% and non-renewable sources generation decreases from 72 % to 69%. So in future, there is a large scope of RES power generation due to their number of advantages. In view of this, Indian government's (MNRE) has targeted to build 10,000 number of microgrid in India for rural electrification using only RES by 2021 [5].

Table 1.4 – HYDRO ELECTRIC GENERATION -WORLD

S.No.	NAME OF THE COUNTRY	TOTAL CAPACITY (2016) HYDRO	TOTAL CAPACITY (2016) WIND	TOTAL CAPACITY(2016) SOLAR PV
	BRAZIL	98.1 GW		
	CANADA	79.3 GW		
	CHINA	331.9 GW	168.4 GW	77.5 GW
	GERMANY		50 GW	41.5 GW
	INDIA	42.7 GW	33.6 GW	7.1 GW
	ITALY			21.0 GW
	JAPAN			43.6 GW
	NORWAY	31.4 GW		
	SPAIN			
	TURKEY	23.66 GW		
	UK			12.0 GW
	USA	265.8 GW	83.2 GW	40.8 GW
	OTHERS	396 GW	111.1 GW	53.7 GW

Wind Power Generation Capacity

CHINA 47%
SPAIN 7%
INDIA 9%
GERMANY 14%
UNITED STATES 23%

(a)

Hydro Power Generation Capacity

OTHERS 31%
CHINA 26%
USA 21%
BRAZIL 8%
CANADA 6%
NORWAY 3%
TURKEY 2%
INDIA 3%

(b)

Solar PV Power Generation Capacity

CHINA 32%
JAPAN 18%
GERMANY 17%
UNITED STATES 17%
ITALY 8%
UK 5%
INDIA 3%

(c)
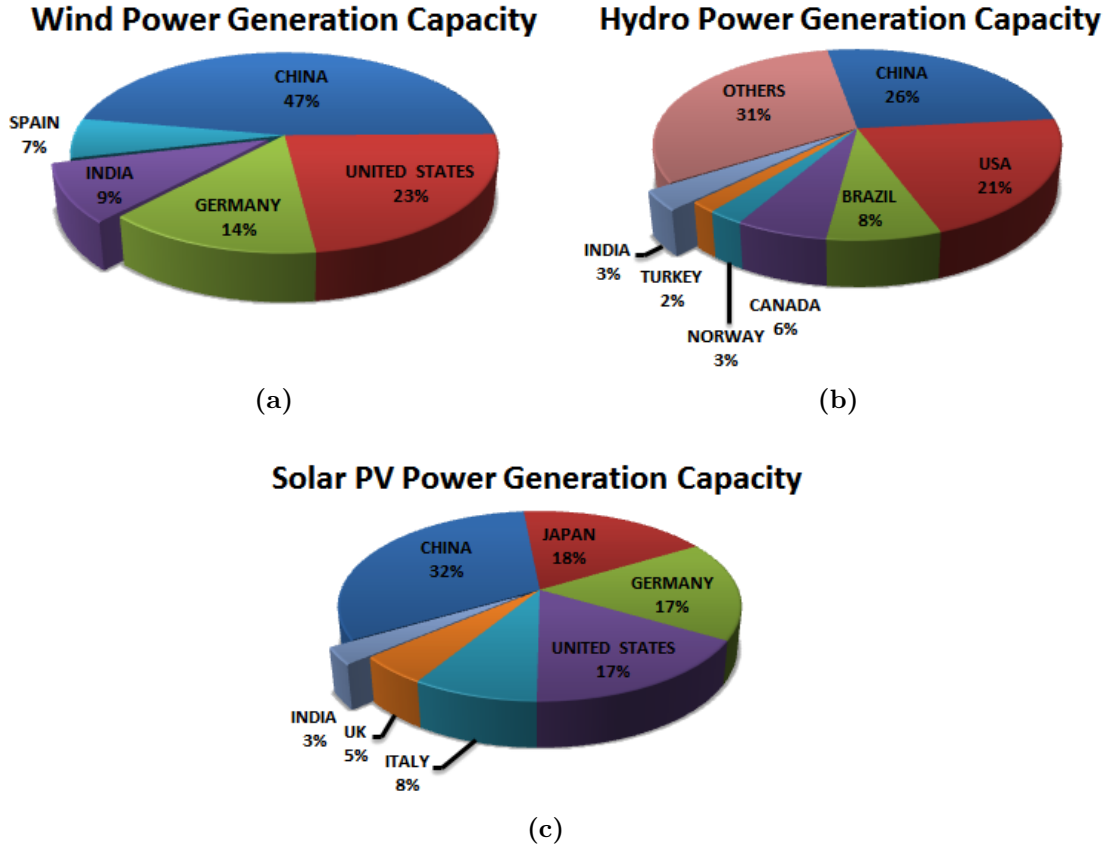
Figure 1.1 – Renewal Power Generation Capacities by Share (World)

1.3 Microgrid Worldwide

With the boost in renewable energy generation and affordable technology, microgrids are becoming more efficient and economically viable. Furthermore, recently a number of major blackouts have occurred in some countries which virtually left the affected areas in a state of chaos [7, 8, 9, 10] .The lack of electric power revealed one common fact that our modern society is highly dependent on electricity. It can be visualized from these blackouts that may cripple the life severely. Electrical transport system, financing activity, academic institutions, industries and health services with no emergency or standby generation, public and residential lighting and even some communication systems may fail to operate. These failures sudden raise the requirement of microgrid to supply electricity to the local area. According to a report of Navigant research, a consulting company, there were 1869 microgrid projects worldwide having a total capacity of 20.7 GW till the year 2017. These projects were analyzed across 123 countries in
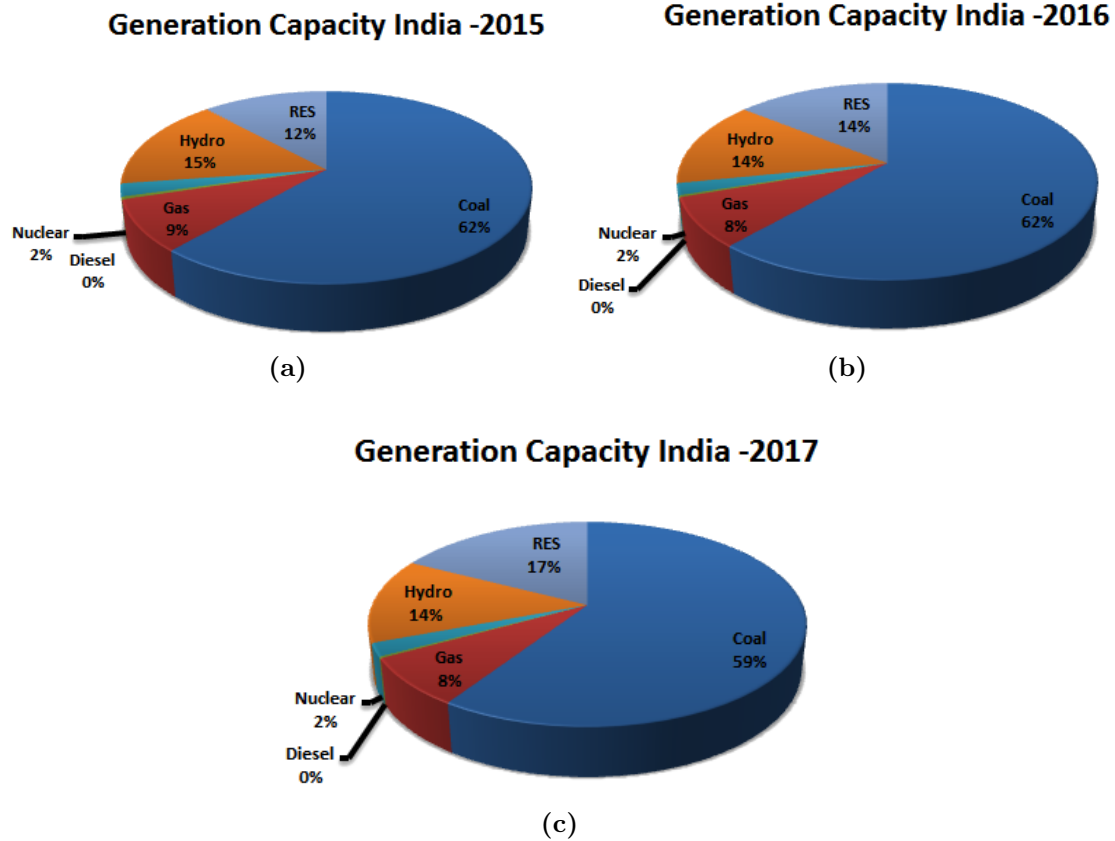
Figure 1.2 – Power Generation Capacity Share in India (by type of source)

which majority of were small-scale with the exception of only one project of 2.2 GW Microgrids installed at Saudi Aramco gas-oil separation plant in Shaybah, Saudi Arabia. In regards to the geographic distribution of microgrid projects, Asia-Pacific and North America followed the way, accounting for almost 75% of all installed microgrid capacity. It is expected that global microgrid capacity will be increased upto 7.6 GW by 2024. In 2013, North America ranks first among all the countries worldwide by taking overall market share with total capacity of 2GW. After that Europe with 384 MW capacities and Asia-pacific with 303 MW capacities take the 2nd and 3rd place. But it is planned that North America will reach upto 5.9 GW and Asia Pacific jump on to 2nd place with 2GW capacity and Europe reached to third place with 694 MW (approx.8% market share) capacity by 2020.The global growth of microgrids has occurred across six key microgrid segments i.e. Commercial and Industrial (C&I), Community, Utility distribution, Institutional / campus, Military and Remote rural areas. Here is brief account of

state of the art microgrid in world:

a) **1.0 MW SOLAR-PV Microgrid, Monolo Island,Fiji:** This, microgrid combines with 1 MW solar –array with 20 Tesla power packs, having a total energy storage capacity of 4MWh.It is installed in Monolo Island, Fiji in 2016 by Tesla.

b) **15.0 KW PV-BASED Microgrid, Ocracoke Island, North Carolina, US**: This microgrid is located in Ocracoke island ,North Carolina,US in 2016 by North Carolina Electric Membership Corp.Tideland Electric Membership Corporation.It includes a PV array of 15 KW, 10 power packs and 150 Ecobee smart thermostats.

c) **4.6 MW Hybrid Microgrid, Marshall Islands:** A 4.6 MW hybrid microgrid installed at Marshall Island by IRENA in 2017.This includes solar-PV assets and lithium-ion batteries as the storage devices.

d) **UC San Diego 42MW Microgrid:** This microgrid is installed in University of California, San Diego consists of 2.8 MW fuel cell, 1.5 MW of photovoltaic array(PV) and a 30KW/30KWh PV fully integrated storage system. Total capacity of this microgrid is 42 MW. This microgrid supplies power to about 45,000 people of university. According to university, this provides approximately 95% of their heating & cooling load and 92% of its annual load.

1.4   Microgrid in India

Conventional microgrids in India have been micro hydroelectric power sources through peltric sets [11, 12, 13]. The oldest microgrid in India is a Sidrapong microhydel power plant, which is at an altitude of about 3600 ft at the base of Arya Tea Estate, around 12km from Darjeeling town in West Bengal. This plant was established in 1897 consisting of two 65-kW single-phase alternators (2,300 V, 83.3 Hz).The plant was later upgraded to 1000KW to fulfill the demand of the residents in the town and nearby tea gardens. Apart from hydel, biomass and wind have also been in use, although, recently, a main focus has been on solar

photovoltaic (PV) plants. These plants are operated as isolated microgrids to supply the local loads. Recently, the oldest monastery (nearly about 2500 year old) in the Ladakh region was powered with solar-PV where approx. 150 monks lived. It was the first time they saw an electric lamp glowing [3]. According to a report in 2010, India had total number of 33 microgrids based on solar-PV. India's first smart microgrid was installed in Upari Babhan, Rajasthan having generation capacity of 15.78 KW.This microgrid supplies power to a village of 200 -300 people having consumption of 10.43 KW.In 2016,MNRE came up with a policy of mini and micro-grids. About 10,000 mini and micro-grids with 500 MW of generation capacity till 2021 are proposed.Tata Power Delhi Distribution (TPDDL) plans to set up two solar MG in two villages(Tayabpur and Behlopur in Baishali District) of Bihar in partnership with Massachusetts Institute of technology Centre for energy and environment policy research,General Electric and Tata Trust. In 2014,first village Dharnai was acclaimed as first fully solar powered village. Microgrids fully based on renewable sources in India are:

a) **Micro-hydro power in Pathanpara village, Kerala:** Pathanpara is a small town of 365 families in the Kannur district of Kerala. As the village had no electricity from the main grid but it also had many permanent and seasonal streams nearby, thus suitable for micro-hydro plants for electricity supply. A plant of 5KW with lean flow of 22 lps,60m head and a diesel backup was setup with the help of village people it developed a sense of resource mobilization, labor, faith in the system .The people took care of the day to day affairs and framed rules together to run the plant . Even when the grid later came into the village, many people still preferred power from micro-hydro plant as the quality of grid supply was poor.

b) **Micro-hydro power in Udmaroo village, Nubra Valley Ladakh:** A plant of 32KVA capacity has been setup in the Udmaroo village, in the Nubra valley of Ladkah.This village has low convenience to market, no mode of employment, and reduction in agriculture interest. The only way of employment in the village is the army with rare gov-

ernment sector jobs. So, this plant has made a positive impact in the people's life. Right now they are only using 20-25KVA out of 32KVA installed capacity, so there is chances to supply the extra load. The citizens are also conscious that the rivers and streams freeze in the Nubra valley for 4 months in a year and during that time, no electricity is generated. So, during this time the EMC (Electrical Maintenance Cell) runs a small diesel gen-set, which is costlier than the micro-hydro electric generators in order to save up for the winter months. They were also aware about the pollution caused by the diesel gen-sets and polluting nature of micro-hydro.

c) **Solar photovoltaic power plant in Durbuk, Changthang, Ladakh:** A 100KW solar plant with 1360 solar photovoltaic panels has been setup in Durbuk, Ladakh region which is far away from the main grid. This uses a 250KVA diesel generator set which cause health issues on account of pollution. Also every year 48,000 liters of diesel had to be purchased at the cost of Rs1.6mn by State Government. Now from this plant, 347 households receive uninterrupted electricity and has enabled heath care with the Primary Health Centre (PHC) which is able to store polio, measles vaccines on site due to refrigeration, and many other medical facilities. Renewable Energy Development Co-operative (REDCo) is a registered society and non-profit entity which is run by the 15 elected members, and a board of directors headed by the councilor.

1.5 Type of Microgrid and their Structures

In literature, a microgrid is defined in three ways i.e. AC, DC and Hybrid microgrid. Brief descriptions of these are given below [14, 15].

1.5.1 AC Microgrid

The network consisting of the DG units and load circuits can form a small isolated AC electric power system i.e. an AC microgrid (as shown in Figure 1.3). AC
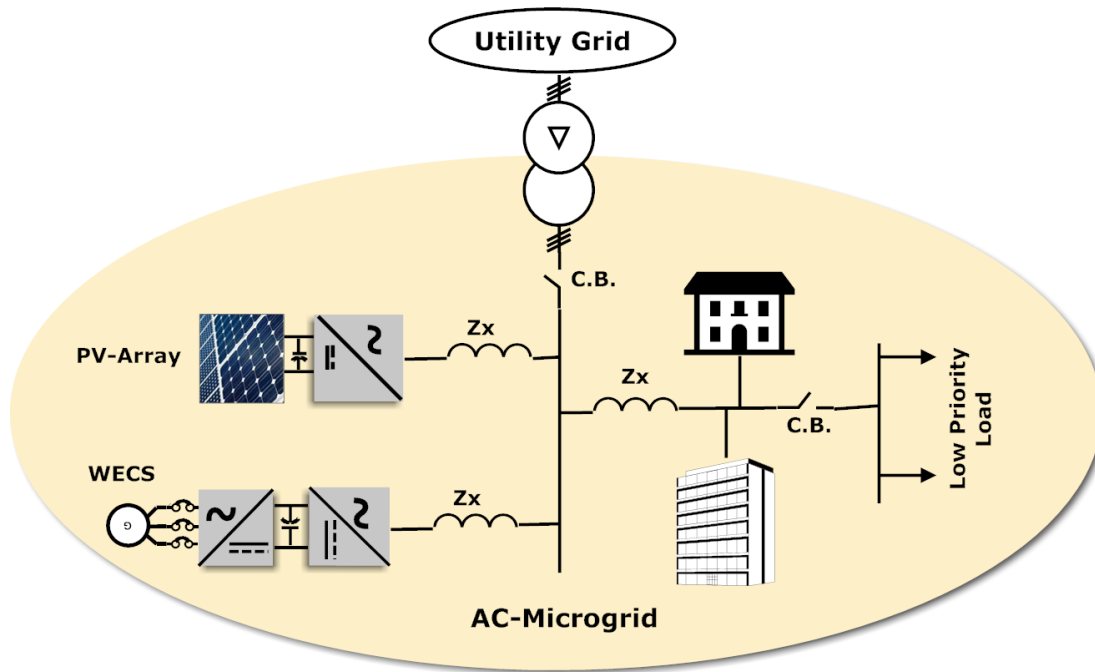
Figure 1.3 – AC Microgrid Schematic

microgrid is more in line to the conventional electric power system therefore any conventional equipment and device can be used in such system. Various demonstrative projects for AC microgrid are under operation worldwide. The Consortium for Electric Reliability Technology Solutions (CERTS) provides a test bed facility to demonstrate the control algorithms developed for microgrids. These algorithms perform well during many transient events and steady state power exchanges. CERTS microgrid also demonstrates the integration of various distributed energy sources into a microgrid and exhibits the stable behavior at critical points with ability to island and reconnect to the grid in an autonomous manner. During normal operating conditions, the two networks are interconnected at the PCC while loads are supplied from the local sources (e.g. RES based DG units) and additional power if needed is drawn from the main grid. If the load demand power is less than the power produced by the DG units, excess power can be exported to the main grid. Joan Rocabert et.al.[1] discussed an overview of different aspects of control and operation of AC microgrids which include various power converter control, detailed analysis of the main operation modes and control structure for power converters which belongs to microgrid.

It provides details on grid-forming, grid-feeding and grid-supporting configur-

ations. This analysis is extended to maximize the reliability and controllability of microgrid and to minimize the operating cost of Microgrid.AC microgrids have various power electronic interfaces which must be controlled adequately for their stable operation. These interfaces can be controlled in centralized or decentralized manners [16]. Although, the main aim for both the strategies is to share power accurately with improved dynamic stability and reliability. Wireless control strategies with autonomous operation are widely accepted and demonstrated by various authors [17, 18].

1.5.2 DC Microgrid

A DC Microgrid is a power network that allows a large amount of solar energy using distributed photovoltaic generation units along with storage devices and traditional electric power systems were designed to provide AC power, via high-voltage AC (HVAC) transmission lines and low voltage distribution lines to house-holds and commercial consumers. Also, DC power systems have been used in industrial power distribution systems, telecommunication infrastructures and point-to-point transmissions over long distances and for interconnecting two areas system with different frequencies. Now a days, all the consumer equipment's and DG units are packed with power electronics devices. These devices (such as computers, fluorescent lights, variable speed drives, households, industrial appliances and equipment's) need the DC power for their operation. Because of this, all these DC devices require conversion of the available AC power into DC for use, and the majority of these conversion stages typically utilize inefficient rectifiers. Moreover, the power from DG units must be converted into AC to tie with the existing AC electric network. In case of DC MG configurations, low voltage DC links are based on bipolar configurations where the loads can be connected either across the positive polarity and the ground or between the two polarities. The LVDC distribution network facilitates the interconnection of more number of DG units [2].Measuring instruments like advanced metering infrastructures (AMIs), demand energy managements (DEMs) and protection systems can also be integrated into the power converters. To achieve this, many researchers stressed for the emphasis on the DC MGs applications such as power supply for the critical loads

in commercial buildings, electronics factories and hospitals. It is concluded that the DC MGs have attractive features in terms of simple configuration, low system cost and the overall improved efficiency because few power converters are needed comparable to the AC MGs.

1.5.3 Hybrid Microgrid
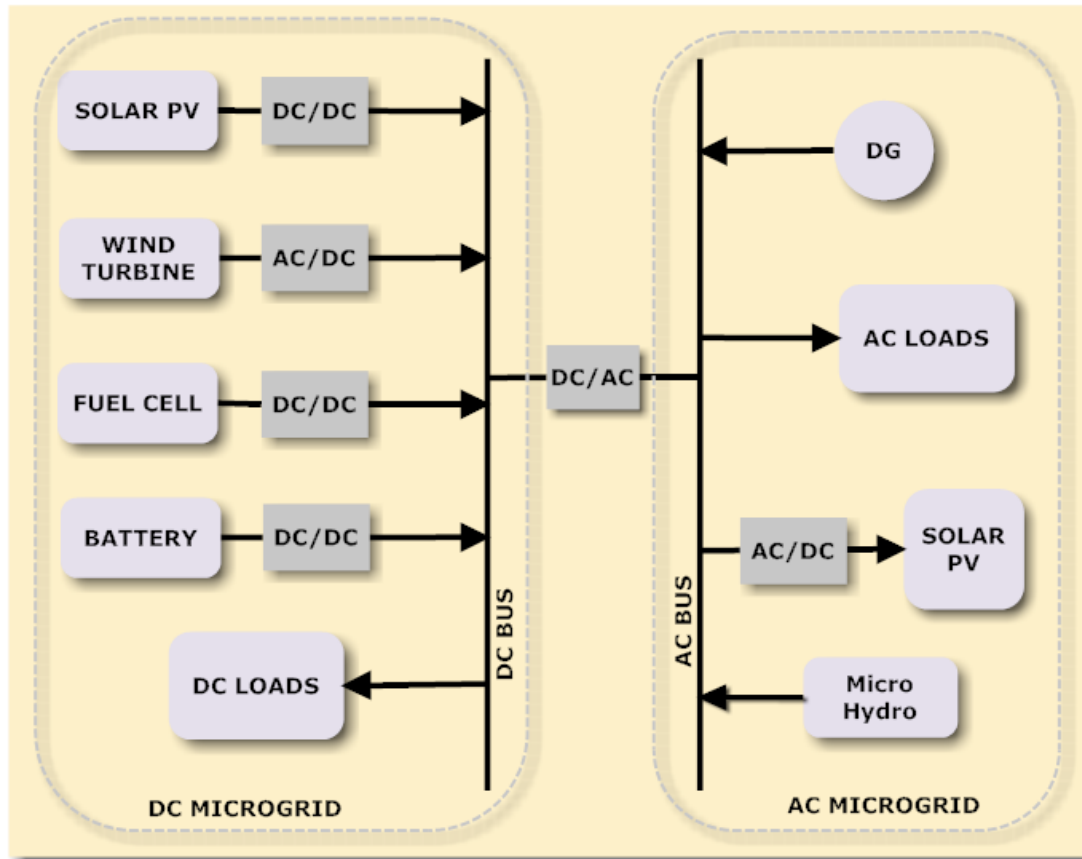
Figure 1.4 – Hybrid Microgrid

Availability of cost-effective electric power to communities and industrial or commercial installations in absence of utility grid has remained a challenge. They have to rely on engine- or turbine-driven generator sets, that are highly reliable but a costly affair on account of cost and environmental pollution. Now a better model is emerging that combine's newly cost-effective renewable energy from wind or solar sources with conventional diesel- or gas-fuelled generation. These configurations are called hybrid microgrids, also employ energy storage devices to enhance economy and reliability. Facilitated by sharp declines in the cost of wind

and solar energy systems, as well as lower energy storage costs relative to the price of fuel, hybrid microgrids are well suited to a host of applications, including individual buildings, resorts, mine sites, remote villages, small islands and others. The most promising applications are those with total power demand from 100 KW to 20 MW. Wind or solar energy reduces reliance on power produced from generator sets, saving fuel and, to a greater extent, maintenance costs. The hybrid microgrid concept is quickly becoming the preferred approach to delivering low-cost, reliable power to the area beyond the reach of larger electric utility infrastructure. These microgrids utilize both AC and DC bus topologies to increase performance and efficiency [14]. The Hybrid microgrid is formed by connecting multiple AC and DC subgrids together using interlink converters as depicted in Figure 1.4. AC frequency and DC voltages are normalized to a common per unit range for comparison and equalization. After equalized, proportional power sharing strategy is able to know precisely the amount of active power transferred among the sub-grids.

1.6   IEEE 1547 Standards and Cigre WG C6.22 for Microgrids

IEEE Standards 1547 and Cigre WG6.22 are closely associated with Microgrid definition. Cigre WG C6.22 technical brochure addresses the main elements and feasibility requirement of microgrid. It provides a basic road map and shows a business perspective to a viable microgrid. The IEEE Standard 1547 provides more detailed definition and technical requirement to form a DR island (Microgrid) over Cigre WG6.22.

The IEEE Standards Association (IEEE-SA) Standards Board has approved the IEEE 1547.4 Guide for Design, Operation and Integration of Distributed Resource Island Systems with Electric Power Systems. The guide includes sections on electric loads, utility equipment and operations, protection, controls and system studies. Testing, communications, contractual and regulatory considerations are additionally cited. The guidelines are organized into three major categories:

a)   Overview covering types of DR islands and the general functionality of each type.

15

b) Planning and Engineering covering the planning and testing of appropriate engineering approaches to encompass a variety of contingencies.

c) Operations covering how a DGs island is formed, and the operational transition scenarios when moving to the island as well as scenarios when transitioning back to the utility grid.

In addition to this, IEEE Standards 1547.4 discuss several types of DR island systems, but they all share the ability to generate their own electric power as well as the ability to connect and disconnect from the electric power system that serves a wider geographic area. Customer facility micro-grids and electric utility distribution circuit micro-grids are two instances of planned DR islands where DRs include both generators and energy-storage technologies. The IEEE 1547.4 guide includes best practices for implementing the various ways in which a DR island can separate from a part of the area electric power system and can reconnect to it while providing power to the islanded local electric power systems. It also explains about the benefits of using DRs by targeting improved electric power system reliability and build upon the interconnection requirements of the IEEE 1547 Standard for Interconnecting Distributed Resources with Electric Power Systems. Additionally, it provides informative background about DRs, interconnection systems and participating electric power systems.

1.7 Scope of the Research Work

The objective of this research work is to study the modeling and control of microgrid under various conditions in order to improve its performance and reliability. In this regards, a Microgrid prototype based on two 3-ph voltage source inverters with FPGA control board have been designed . This Microgrid uses novel repetitive controller for voltage and current control which is capable of sharing accurate power among the inverters under islanded mode of operation with excellent improvement of power quality in terms of lower THD as well as reduced voltage unbalance factor. This particular repetitive controller is designed to achieve robust performance under transient conditions. Further, two different control algorithms have been implemented for the enhanced Microgrid stability under various topo-

logical changes and parameter variations. The variation in transmission line para-
meter has been performed by changing the line resistance using bypass switch.
Due to this variation in line resistance, R/X ratio increased to very high value
emulating topological changes in the Microgrid. Such variation usually causes the
stability issue in the Microgrid. However, the proposed L_1 controller stabilizes the
Microgrid in such conditions by damping out all the low frequency power oscilla-
tions in the Microgrid. This ensures proper operation of Microgrid under various
operating conditions.

1.8   Thesis Structure

Chapter -1: This chapter presents introduction and background to the microgrid
technology. The overview of various microgrids in world is presented. Various
operating condition and control layers have been discussed.

Chapter -2: This chapter discribes the fundamental of microgrid operating
condition, its operation and development of all hardware component required for
an experimental validation.

Chapter -3 :This chapter presents and describe various control for parallel
operation of voltage source inverter in microgrid environment. Primarily droop
based methods have been discussed with their related technologies.

Chapter -4: In this chapter a repetitive controller is proposed and discussed
with their simulation and hardware results.

Chapter -7: This chapter will show unbalance compensation method using PR
& RC add-on controllers. Design and analysis of controller also is presented.

Chapter -8: This chapter will discuss adaptive methods for stable operation
where transmission line impedance get varies. The proposed L_1 control method
will be derived and validated.

Chapter -7: This chapter introduces FPGA and its use in real time implement-
ation. Various methods for DSP operation and their implementation technique is
discussed.

AC MICROGRID OPERATION AND PROTOTYPE DEVELOPMENT

The major aspects of microgrid design and its implementation includes requirement of efficient microgrid devices, control strategies and stable different operating conditions. This involves study of numerous types of economic, technological and environmental aspects. An operating microgrid continuously observes these aspects and works optimally to achieve its goals. The microgrid operation can be categorized to achieve three major goals. The goals include maximum benefits in terms of economic, technological and social benefits [3].

2.1 Operational Goals of Microgrid

2.1.1 Economic Benefits

The most important aspects of any technology are its economic benefits. A microgrid is beneficial if it's operating and capital cost is economical as compared to conventional grid or main grid. The microgrid operation can be optimized in such a manner that it can provide cheaper energy. This requires co-ordination among various energy sources including renewable like solar and wind etc. For e.g., a hybrid wind, solar with BESS system can be operated at lower cost by having co-ordinated use of their generation. The other way to achieve economic benefits is to exchange power with EPS in such a way that it may reduce the microgrid operating cost. Microgrid can store its own energy and receive power from grid in case cost of energy of the grid is high and vice-versa, i.e. it can feed the grid when demand or cost of energy rises on grid side.

2.1.2 Environmental Benefits

RES has small carbon footprint but cannot be used as reliable energy sources due to their intermittency. The microgrid can integrate various RES to form a reliable energy source therefore; can increase the benefit of RES towards the betterment of environmental conditions.

2.1.3 Value Addition

In microgrid, using various power electronics converters and high- end technologies, the other value added ancillary services can be provided. These include charging station for electrical vehicle, different power supply system and higher power quality and allowing microgrid to be managed locally by local operators.

2.2 Microgrid's Renewable Energy Sources

Microgrid can be built by incorporating various RES. The commonly available RES that can be used in distributed system are 1) Solar PV 2) Micro Hydro 3) Wind 4) Fuel Cell and 5) Micro-turbines using Biomass . All these sources can be integrated in microgrid using various control method and power electronic interface.

2.2.1 Solar PV

Solar irradiation is a free source of energy and available in abundance everywhere on the earth. It can be tapped to use in many ways. To convert solar energy in to electric energy, solar PV systems are the most suitable devices. A solar photovoltaic cell (Figure2.1) is made up of semiconductor material where a p-n junction is created by a doping process. In photovoltaic process current flows between p-n junctions on exposing of cells to light photons.

Solar power plant can be established in wide range of their power rating from a few KW (roof top) to concentrated MW plant. Each plant have number of modules connected in series and parallel configuration to generate required voltage and current output whereas each module again is formed by series and parallel
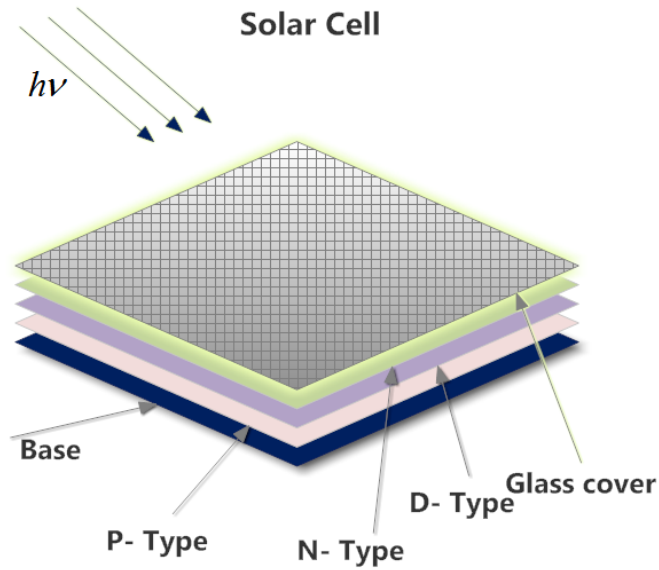
Figure 2.1 – Soler Cell
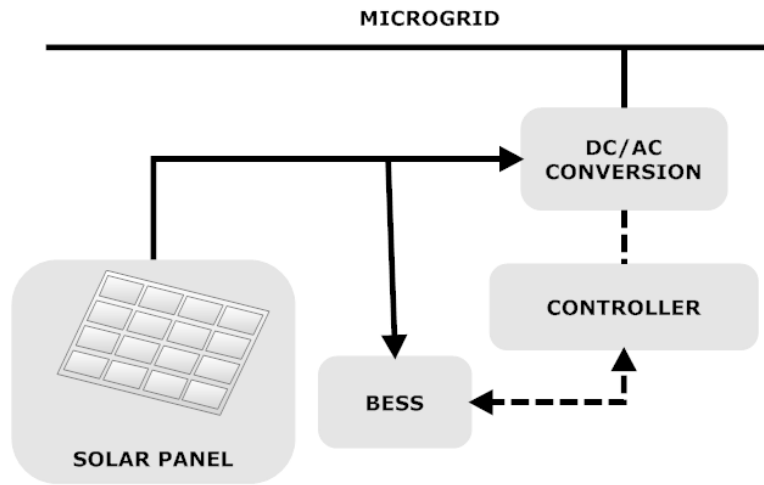
Figure 2.2 – Solar panel connected to microgrid

connection of solar photovoltaic cells. In solar PV electricity generation has minimum number of stages and do not require any mechanical interface. Therefore, solar photovoltaic (SPV) plants are one of the best RES for microgrid. SPV plant can be used in microgrid in different configurations. A basic control scheme and configuration for SPV in microgrid is shown in Figure 2.2. Photovoltaic, fuel cells, micro turbines produce DC voltage which is passed through the inverter to obtain AC for distribution on the grid. The capability of PV system is limited by available sunlight. If power requirement exceeds the available sunlight then storage is required for standalone systems. The main drawbacks are high initial cost and the intermittent nature.

2.2.2 Micro Hydro:
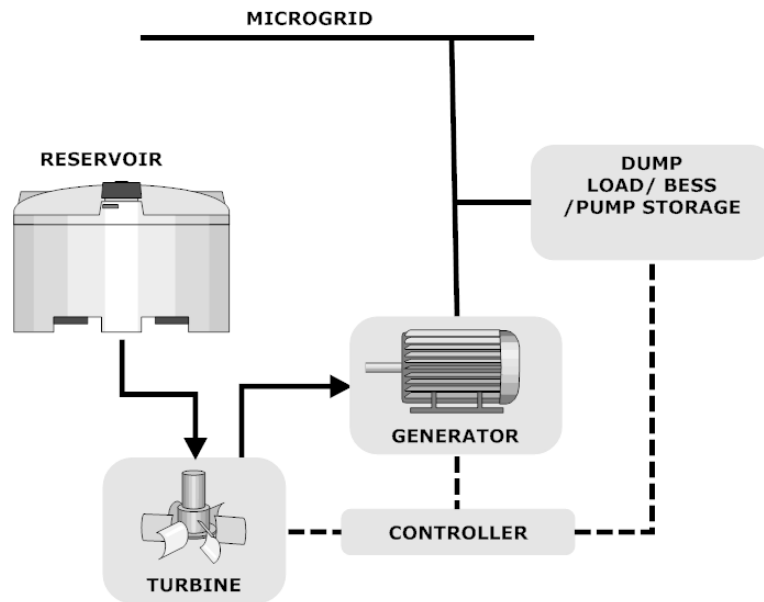
Figure 2.3 – Micro-hydro plant in microgrid

Hydro power plants having generation capability less than 100 KW comes under the category of micro hydro power plants [19]. These plants have number of merits over large hydro power plants. The most important advantages of these power plants are:

a)   Infrastructure and capital cost is low as they do not require any reservoir

b)   These plants can be installed on small stream of water or run-of river.

c)   These can be installed on seasonal water streams. These plants constitute turbine-generator system with controller for voltage, frequency and power output. The dynamics of these turbine-generator set can be controlled in various ways. Figure 2.3 shows the micro-hydro plant controlled by electronic load controller using dump load for power balance. However the dump load can be replaced by pump storage or battery storage with appropriate power electronic converters and machines.

2.2.3 Fuel Cell

Fuel cell acts as a back-bone of microgrid because it provides power from the central grid by converting chemical energy into electrical energy. It consists of number of individual cells known as stack. When a hydrogen-rich fuel i.e. a clean natural gas or renewable biogas enters into the fuel cell stack, then it form electrochemical reaction with oxygen and produce electric current, heat and water. Fuel cells used in microgrid provide high efficiency, high reliability and quieter operation. The only drawback of fuel cell is its high cost.

2.2.4 Biomass

Biomass is a term that includes all organic matter produced by photosynthesis available on the earth's surface. It consists of all water- and land-based vegetation and trees, and all waste biomass such as municipal solid waste (MSW), municipal bio solids (sewage), and animal wastes (manures), forestry and agricultural residues, and certain types of industrial wastes. As we know, world's energy is dependent on fossil-fuels. Then bio-mass is the only option for generating electrical energy naturally due to its large availability[20][21].Biomass-based power plants are good for the area where demand of electricity falls in the range of 10-250 KW.

2.2.5 Wind

Wind energy conversion system is also another renewable option for generating electricity. It converts wind energy into electrical energy using various combinations of turbine and electric generators. Fossil fuels pollute our environment and can cause serious environmental problems, but wind produces clean energy. Fossil fuel based power plants have a limited resources but wind energy has no limit. As the temperature of air is always varying but there will always be wind. Wind farms typically include induction generator to generate electricity where rotor is driven by wind turbine at slightly higher speed then grid frequency. This makes system very simple and robust.

2.3 Operating Modes

Microgrid required to work under various operating modes: Grid-connected mode and island mode. Figure 2.4 shows state –diagram of microgrid operation [22][23].
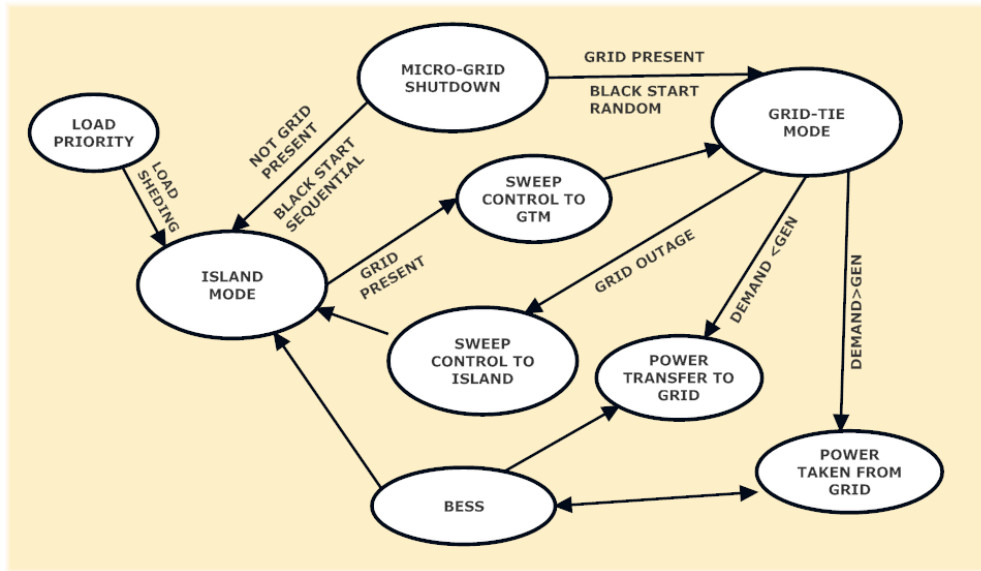
Figure 2.4 – State Diagram of Microgrid Operation

2.3.1 Grid Connected Operations:

Microgrids are majorly connected to grid-tied mode because there are very less possibilities of grid outage [24][25]. In this mode of operation, microgrid can have power transaction to grid and can work as consolidated load or source [26]. If power generation within microgrid is higher than its load demand then microgrid work as a source and surplus power is transfer to grid and similarly if it has more demand than generation then it works as a power sink or consolidated load [27][28]. Microgrids may have battery energy storage system (BESS) to store the surplus generation. So, there are two choices in the case of excess generation. First excess generation is transfer to grid and second generated excess power is stored into BESS for backup supply. By implementing proper economic model, we can make decision to transfer partial of full power to grid or BESS. Figure 2.5shows the conceptual model in this mode [29][30].
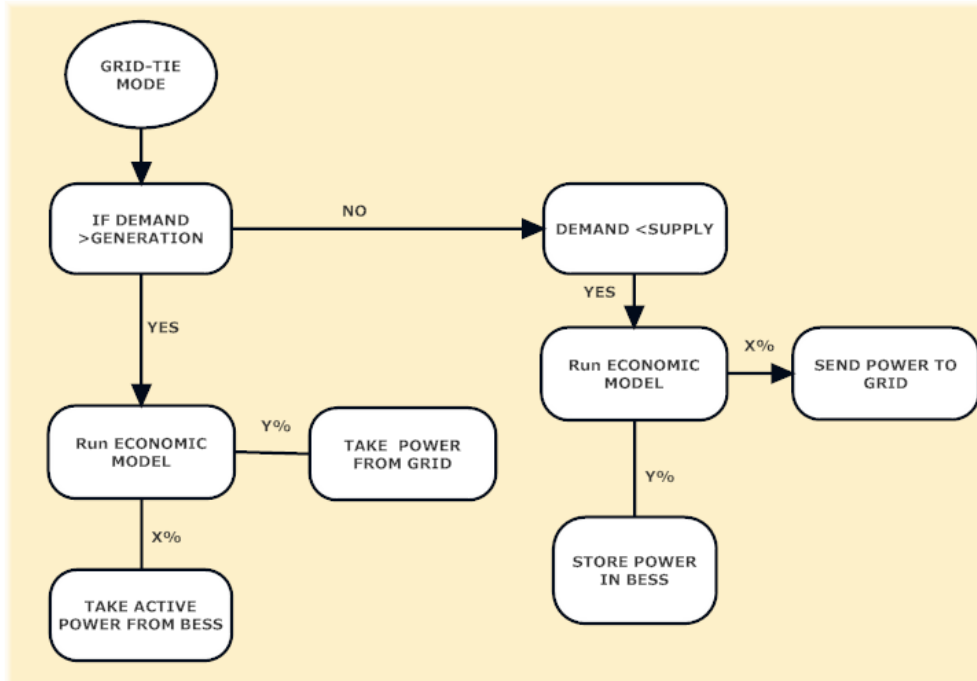
Figure 2.5 – Grid tie mode operation diagram

2.3.2 Island Operations

Island mode operation starts when there is a power outage/failure from grid or microgrid disconnects itself from grid by seeing some grid side fault condition or disturbances [30]. In any condition, microgrid become isolated and serves its all load by its own generation and storage. The main aim in this mode is to supply power to critical loads and minimize the economic damage caused by grid failure. Main issue in this mode is to have stable operation and proper power sharing among the sources [31][32]. As system become very weak, the stability of system also becomes critical.

2.3.3 Black Start & Synchronization

When microgrid is established, each individual source must be synchronized with each other so that they can work as lumped source [25]. Synchronization in the presence of grid is much easier than an islanded condition. The major advantage in presence of grid that of stability. When synchronized with grid, the operating point (voltage & frequency) do not vary and stay stable in whole synchronization process while in islanded condition, system is very weak and cannot sustain the

same operating conditions for long duration [33]. Therefore, in both condition synchronization procedure become different.

2.3.4   Power Quality Improvement

Microgrid can improve power quality by using its power electronics interface in certain way [34]. Microgrid can provide compensative action to various power quality issues like harmonics, voltage sag, unbalance etc.

2.4   Microgrid Control Layers

Micro-grid is formed by various micro sources based on renewable energy sources (RES). These micro-sources must operate in co-ordinated way to ensure reliability and stability [35][36]. These sources are normally interfaced with VSI, further each VSI are interconnected via common transmission line. As our system must operate around tight operating point, so it is required to have a good hierarchical control to maintain stability [[37][38]. There are various control methods available which are applied at various level of the system. Beside inner control method for inverters, there are broadly three basic levels. Figure 2.6 shows the hierarchical control of microgrid. The three basic control methods for microgrid as:
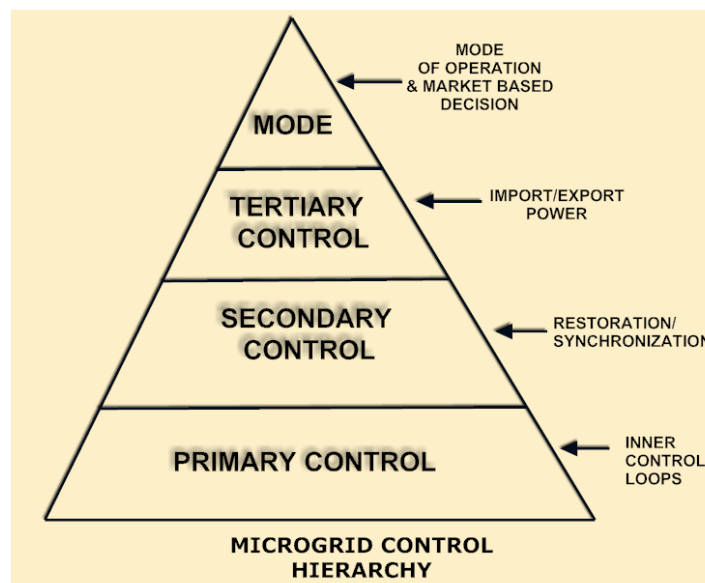
Figure 2.6 – Hierarchical Control of Microgrid

2.4.1 Primary Control (Level 1)

The droop-control method is generally used to match the physical behavior that makes the system stable and more damped. This control constitutes a virtual impedance control loop to match the physical output impedance. This control level alters the frequency and amplitude of the voltage reference of the inner voltage and control loops. The main purpose of this control is to imitate the behavior of a synchronous generator, which reduces the frequency as the active power increases.

2.4.2 Secondary Control (Level 2)

This control is used to compensate the frequency and amplitude deviations [39][40]. It ensures that the electrical levels into the microgrid must be within the required values. In addition, it can comprise a synchronization control loop which ideally connect or disconnect the MG to or from the distribution system. The secondary control also ensures that the frequency and voltage deviations are regulated toward zero after every change of load or change in generation inside the micro grid [41].

2.4.3 Tertiary Control (Level 3)

This controls the power flow between the MG and the grid. When the MG is operating in grid-connected mode, then the power flow can be controlled by altering the frequency (i.e. the phase in steady state) and amplitude of the voltage inside the MG.

2.5 Development of Microgrid Prototype

Power electronic based inverters are used as basic interface in microgrid -63]. Apart from many configuration 3 phase -2 level IGBT converter mostly used in research and development. In this work 3-phase, 2-level inverter is designed and developed for microgrid application.

<div align="center">(a)   (b)</div>
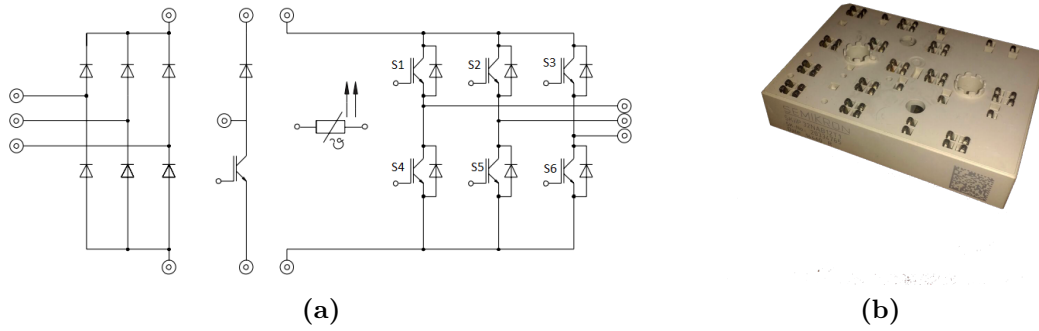
Figure 2.7 – Inverter Module Schematic and a Picture of Physical Device

2.5.1 IGBT Module & Drivers Configuration

The standard three-phase VSI topology is shown in Figure 2.7. The both switches in any of the legs of the inverter (S1 and S4, S3 and S6, or S5 and S2) cannot be switched on simultaneously because this would result in a short circuit across the DC link voltage supply [42][43]. Similarly, in order to avoid undefined states in the VSI, and thus undefined AC output line voltages, the switches in any of the legs of the inverter cannot be switched on/off simultaneously because this will result in voltages that will depend upon the respective line current polarities [44]. Inverters are designed according to prototype requirement. The basic prototype microgrid As per requirement SEMIKRON© (SKIIP32NAB12T1) module has been selected. The module contains integrated chopper and rectifier with 3-ph IGBT 2 level inverter. The picture of designed inverter is given in Figure 2.8.

a)   Drivers: As per requirement SKYPER 32 driver has been selected. These drivers have isolated gate driving circuit with positive and negative polarity gate driving capacity, which diminish the effect of miller capacitance formed in IGBT during turn-on & off. The driver requires only 15 V DC supply and draws 80 mA to 150 mA current per IGBT[45].

b)   VCE observer: When there is any terminal fault (short circuit) at inverter, the output fault current increased rapidly and therefore voltage across IGBT (collector to emitter) terminal increases rapidly. By observing this Voltage Vce, it can be checked that whether there is some

fault (shot through) across terminals or not. SKYPER 32 provides this function internally and can be configured as per rating of IGBT.

(a)   (b)

(c)
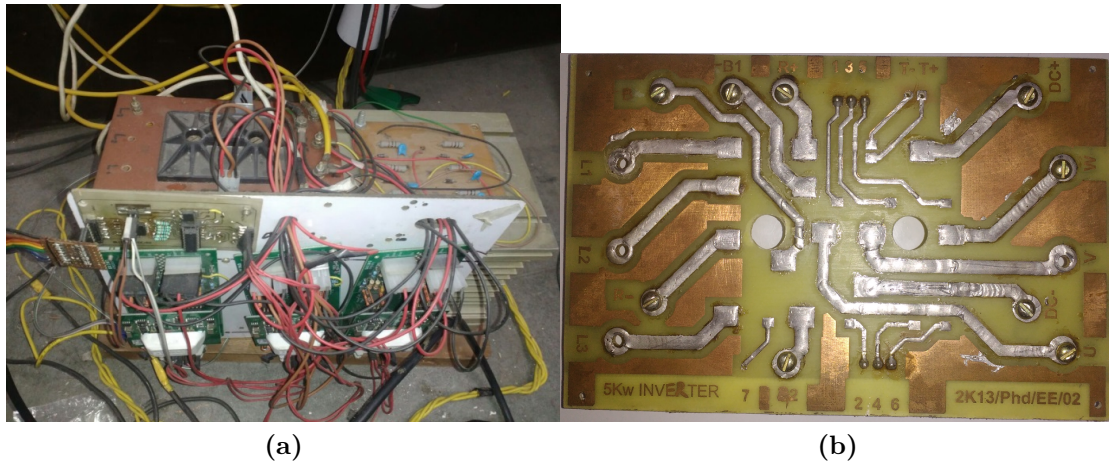
Figure 2.8 – 3-ph Inverter with Driver and other Circuitry

2.6 Output Power Filter for PWM Inverter

In various PWM converters/ inverters based devices low pass passive filters are used at the output of devices so that they can filter out the switching current caused by carrier signal and their harmonic components thereby not allowing them to reach to the load terminals [46]. However, filter requirement is not a compulsion and completely dependent on load and system dynamics. If the system has such dynamics that it can be affected by carrier frequency current harmonics then it become mandatory for converter/inverters to use a well-designed filter at their output. In microgrid a voltage source inverters can serve the different kind of load having different dynamic behavior and frequency responses. Therefore it becomes necessary to use an output filter so that system dynamics remain consistent around fundamental frequency and do not inject high frequency harmonics into system.

The IEEE std. 519 deals and specifies the limitation for all power generators connected to PCC for their harmonic generation. Where it clearly mentions that for low voltage systems (<120 V) source THD & TDD cannot be greater than 8% and 5% respectively. A passive filter for PWM inverter can be designed in different configurations using various combinations of inductors, capacitors and resistors. The most general configuration are L-filter (1st order), LC-filter (2nd order) and LCL- filter (3rd order). An L-type filter is generally used in the inverters, where carrier frequency can vary in broad range and resonance become a major issue. Although these filters are cheap but they only provide low attenuation therefore limited reduction in the current harmonics is possible. LCL filter can drastically reduce the level of current harmonics in output with smaller value of inductance and therefore very much preferred at lower PWM frequencies. However, LCL filters are most suited due to their various advantages but design of these filters are very much complex and many times gives stability issue in closed loop control [47]. LC- type filter are much common type as compared to other two types of filters. These filters provide good attenuation for PWM and their harmonic frequency while having simpler design mechanism. In design of any type of these filters, attenuation is the not only concern but there are many other things to observe. A particular value of attenuation constant (filter cutoff frequency) can be achieved by infinite combination of inductance and capacitance of filters. Lower the cut-off frequency lesser is the amount of harmonics injected into system. To be on safer side one can put higher value of inductance and capacitance to improve the attenuations for high order harmonics but this will not only increase the size of system but a lower filter cutoff frequency will limit the bandwidth of controller. A better choice can be made by analyzing the requirements and design objectives which are as follows:

a)   Filter must not impose uncontrollable bandwidth limitation on overall system. Capacitance should not be too high otherwise it may increases reactive power loading.

b)   Inductance should not be too high otherwise it may give high voltage drop at output on loading.

c)   Filter must be designed for minimum power losses.

d)   Inverter output must remain consistent with IEEE Std. 519-2014 and IEEE Std. 1531-2003. By considering the above mentioned objective we proceeded to design an appropriate (low cost and realizable) LC-filter for VSI.

2.6.1 Design of LC Filter

The transfer function of a 3ph-PWM inverter with a LC filter circuit as shown in Figure 2.8can be described by following equation (2.6.1).

$$G(s) = \frac{V_{out}}{V_{in}} = \frac{R_c C_f s + 1}{L_f C_f s^2 + (R_c + R_f) C_f s + 1} \tag{2.6.1}$$

Where, L_f is inductance in Henry, C_f is Capacitance in Farad and R_c, R_f are series resistance of Capacitor and Inductor.

Now, filter cut-off frequency can be calculated from equation (2.6.2)

$$\omega_c = \frac{2\pi f_s}{10^{(attenuation(dB)/40)}} \tag{2.6.2}$$

where f_s is PWM switching frequency.

2.6.2 Filter Attenuation Constant and Inductance Value

Attenuation provides higher impedance to the frequency for which the filter is designed. For low pass filter the high frequency harmonics must be attenuated significantly. The attenuation generally describes in terms of dB. The 25 dB or higher attenuation is regarded as good. The attenuation at switching frequency can be as high as possible considering the following points:

a)   High attenuation at switching frequency in second order filter may get resonance at any lower order harmonics at corner frequency.

b)   Offers input impedance to the source, so restricted to 5-30% of the rated value.

As per datasheet of IGBT's module, the maximum current must be limited 65 A at 25C. For standard margin, we can take inverter rating limited to 1/3 times of

absolute maximum rating. This will give a good idea of inverter power output rating and required input impedance.

At rated voltage (230 V) and current (22 A) maximum source impedance can be selected between

$$\left(\frac{230}{22} \times 5\%\right) \Omega < Z_{source} < \left(\frac{230}{22} \times 30\%\right) \Omega \qquad (2.6.3)$$

$$0.522\Omega < Z_{source} < 3.136\Omega \qquad (2.6.4)$$

$$\frac{0.522}{2\pi f} < L_{source}|_{f=50Hz,R=0} < \frac{3.136}{2\pi f} \qquad (2.6.5)$$

Therefore, L_f can be selected in between 1.6 mH to 10 mH at 50 Hz power frequency for approximately 5 KVA inverter power rating.

2.6.3 Resonant Peak & Capacitor Selection

Since L_f and C_f can be chosen in wide combination of corner frequency as explained earlier. The resonant peak shows the maximum gain for the resonance frequency. So under dynamic conditions, high value of resonant peak can cause trouble and power flow can occur at resonance frequency other than fundamental frequency. The resonant peak must be low enough while the inductor and capacitor value should not be changed much. Thereby, the damping is the only method to suppress resonant peak. The damping is provided by series filter resistance R_f but this increases the losses in filter at rated current and consequently lowers the overall efficiency. To avoid these losses, equivalent drop in voltage is taken into circuit to have virtual implementation of resistor. This method is called active damping. As in earlier section, it is given that can be selected in particular bound. Similarly we can draw the limits on capacitor value. Here, is an assumption that the voltage and current control loop may have damping ratio in between ($\xi = [0.6 \ 0.9]$) As per [47], the filter ratio L_f/C_f can be calculated by equation (2.6.6) for optimal inrush current and reactive power.

$$\frac{Z_{load}}{\xi} > \sqrt{\frac{L_f}{C_f}} > \frac{Z_{load}}{e^\xi} \qquad (2.6.6)$$

$$13 > \sqrt{\frac{L_f}{C_f}} > 4.75 \Bigg|_{\xi=0.8, Z_{load}=10.45\Omega} \qquad (2.6.7)$$

The inequalities (2.6.6) & (2.6.7)) give us good idea about selection in inductor and capacitor filter design. The final computation of values can be performed with selection of filter cut-off frequency, appropriate frequency response and the bandwidth.

2.6.4 Passive Damping

LC –filter without damping can cause resonance around cut-off frequency. The gain of LC filter at cut-off frequency may go as high as 60 dB (with only parasitic resistance) which is not recommended in practice. However, addition of a small amount of resistance in series with capacitor (not in series with inductor as it increases losses) will increase the damping. It is good practice to provide damping resistance such that the gain at resonance frequency does not go beyond 20 dB so that further damping can be provided by controller (active damping) if required.

LC Filter parameters for 5-kHz Switching Frequency: The filter parameter can be calculated for 30 dB attenuation within the range given by equation(2.6.2) & (2.6.5) Now, from above, we can put forward our choices as:

Attenuation $= [30\ 60]$ dB or $900 > f_c > 160\ Hz$ for $L = [1.6\ 10]\ mH$

Here it can be easily see that for min value of L and lowest value of C computed by ratio $\sqrt{L_f/C_f}$, the cut-off frequency will be 1100 Hz that gives lower attenuation even less than the required minimum value.

For 35 dB (above minimum), attenuation the cut-off frequency ω_c as per equation (2.6.2) is found to be 670 Hz. For this cut-off frequency bode plot of filter with different values of L_f, C_f and with ESR is given in Figure 2.9, Figure 2.10 and Table 2.1respectively.

2.6.5 Inductor Design

The inductor has been designed on the above mentioned parameters. Laminated steal CRNGO (Cold Rolled Non Grain Oriented) core has been used for low cost

Table 2.1 – L & C Values with Different Ratio

Cut-off (ω_c) Hz	$L_f(H)$	$C_f(F)$	Ratio
670	0.0020	2.80e-05	8.42
670	0.0022	2.56e-05	9.26
670	0.0024	2.35e-05	10.10
670	0.0026	2.17e-05	10.945
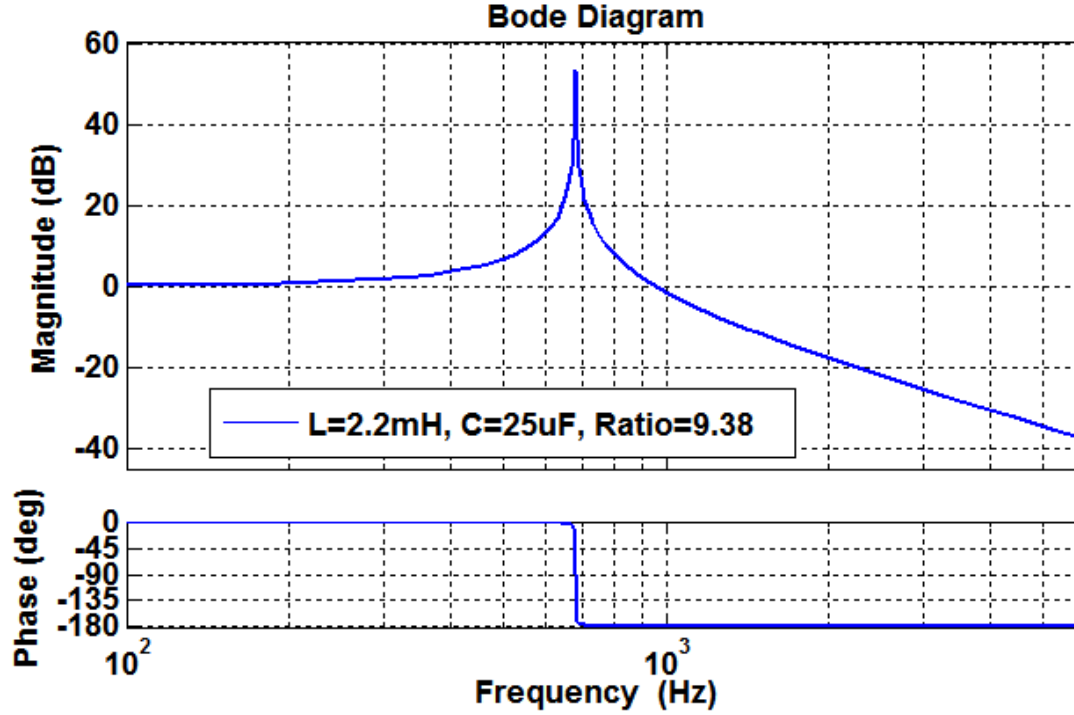
Figure 2.9 – Bode Plot of Designed Filter

of inductor. Lamination of size {85.8} has been chosen as per requirement of A_L value ($inductance/turn^2$). Once A_L value is calculated with small gap (1mm) the required number of turn can be calculated for given value of inductance. A picture of designed physical inductor with capacitors to form LC-filter is given in Figure 2.11.

2.6.6   Transmission Line/ Variable Impedance:

Transmission line prototypes are designed by using inductors and resistances. It is assume that microgrid is a low voltage small network. Therefore, transmission line inductances are mainly very low or negligible and sometimes resistive only. However, using power transformers in transmission line can cause small inductive nature in transmission network. Generally low voltage (415/230 V) transformers
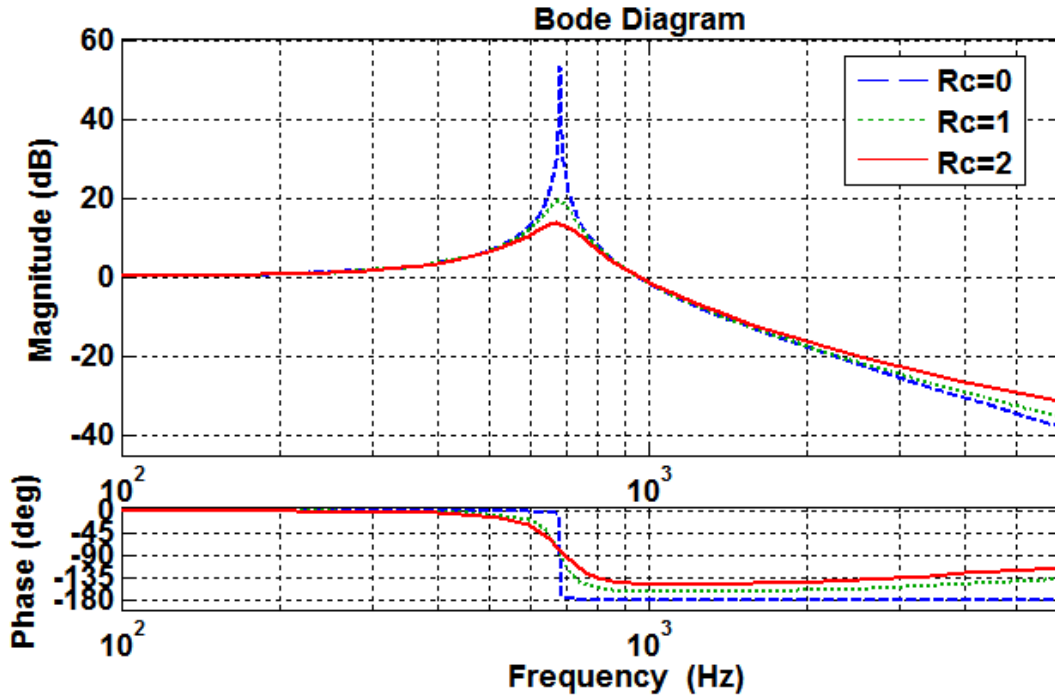
Figure 2.10 – Bode Plot of Filter with Passive Damping

have 4-10% impedance of their rated VA. If we convert these value in absolute impedance (or inductance only), the inductance will be of the order of a few m H. Therefore, transmission line inductor absolute values are taken in range of 2-5mH with low value of (0.1-2.5 ohm) series resistance. To test the variation in these parameters a parallel arrangement has been made to introduce high value resistance into transmission line circuit as shown in Figure 2.12.

2.6.7 Sensors & ADC:

Sensors are most important part of any control system. These devices take physical quantities as inputs and convert them into their equivalent electrical signal as output. To measure high voltage and current Hall Effect, voltage and current sensors are selected. Many other type of sensors are also available in market including conventional current transformer (CT) and Potential Transformer (PT) but Hall Effect sensors are preferred because of many advantage. The main advantage of these sensors is that they can measure both AC and DC quantities without any change in configuration and scaling. Out of many similar sensors the LEM (LEM 25 P-500 V) Voltage and ABB (ABB EL25P1) Current sensors are selected for this work. Both sensors are industrial grade and gives bipolar output current in
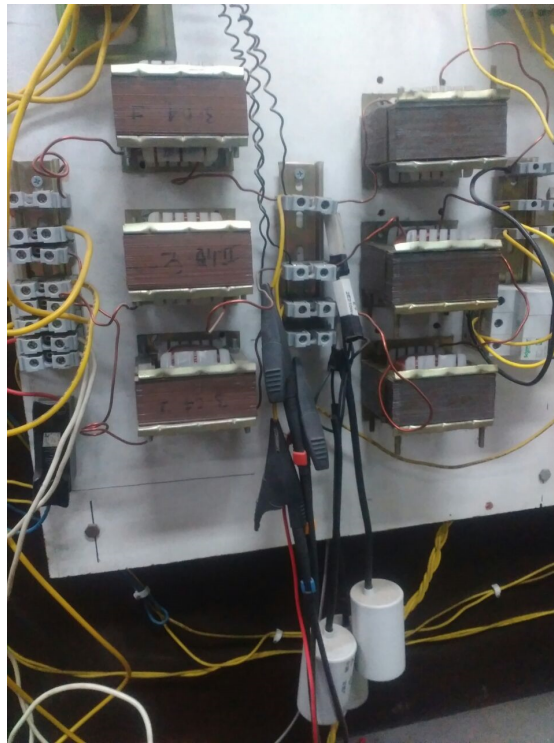
Figure 2.11 – LC Filter in Circuit
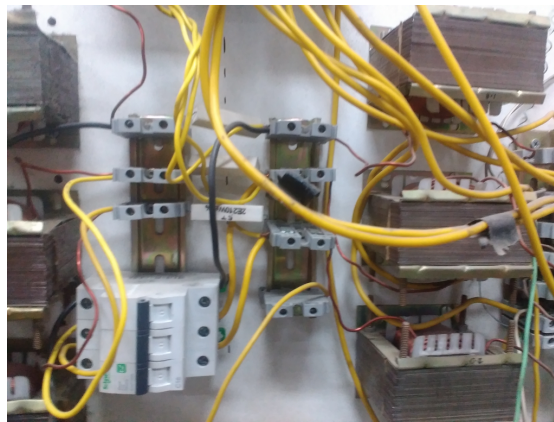
Figure 2.12 – Switchover Circuit for Variable Transmission Line

linear relation with measuring physical quantity (voltage & current). Schematic of voltage and current sensors configuration and physical implementation is given in Figure 2.13& Figure 2.14 respectively.

The sensors output are connected to ADC after 2nd order filter analog filter designed with bipolar op-amp. The ADC has 8 different channels where each channel can sample signal at 50K Sample/sec. All signals are digitized by ADC and serially communicated to FPGA using SPI interface.
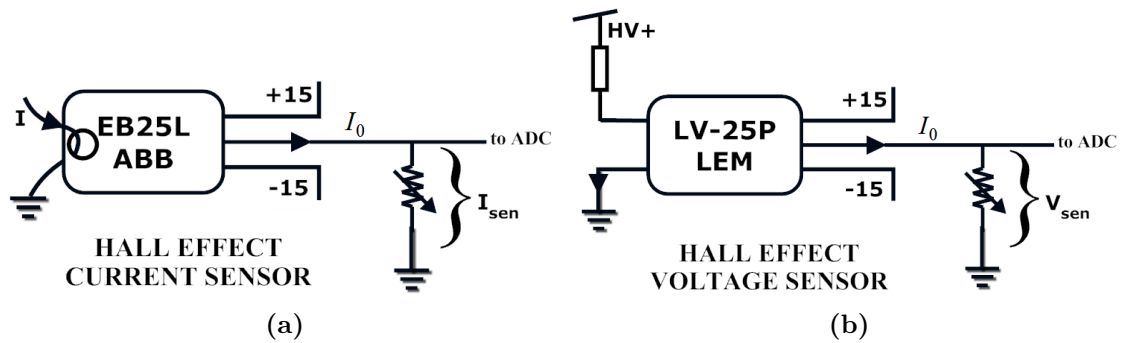
Figure 2.13 – Schematic Diagram of Sensors
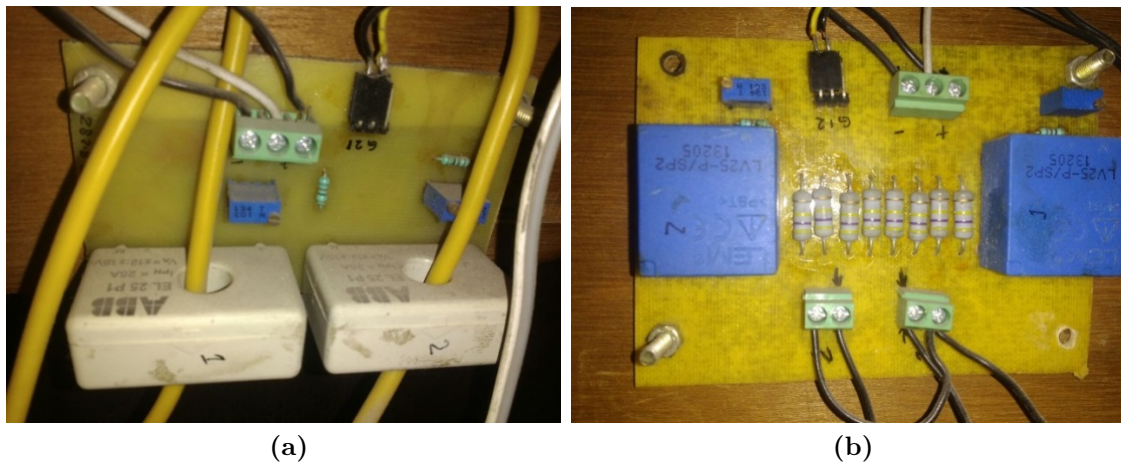
Figure 2.14 – In Circuit Current and Voltage Sensors

2.6.8   Battery Bank

In microgrid prototype it is assume that voltage source inverters has stiff DC link therefore, can be replaced by battery sources. In prototype design to form such kind of low voltage DC link, series connected lead –acid batteries have been used. Therefore, a DC link of nominal 156 V has been designed with 13 series connected batteries where, each battery has nominal rating of 12 V, 7 AH as shown in Figure 2.15.

2.6.9   Linear, Nonlinear and Unbalance Load

To test microgrid dynamics and load sharing capability, small dump load has been designed. The linear loads are made by either purely resistive or combined inductive and resistive components whereas non-linear load are made by rectified RLC circuits.

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Figure 2.15 – Battery Bank

2.6.10 Fuses, Circuit breaker and other Protective Circuits

Each DC link output is connected to DC input of inverter via HRC-fuses. This prevents the short circuit which may occur at DC link. The ratings of fuses are selected 2.5 times lower than maximum instantaneous battery output current. Each inverter output is connected via three poles Miniature Circuit Breaker (MCB). A three phase contactor is also used as isolator to interconnect both inverters after synchronization command. A triac with opto-coupler gate driver has been used as solid state relay for contactor.

2.7 Conclusion

Harnessing energy from renewable ebergy resources through power electronics interface and meeting the load demand through formation of microgrids has social,economic and environmental benifits. Renewable energy resources like solar, micro hydro, wind, biomass, fuel cell can be effectively integrated to form a microgrid. A microgrid can be operated as grid tied mode or in an autonomous (stand alone) mode. Microgrid should have black start and resynchronisation capability. There are three modes of operation such as primary, secondary and tertiary operating mode. In this chapter development of prototype microgrid hardware has been explained, which includes design and development of IGBT based inverter, its driver circuit, LC filter design and passive damping module etc. In the last but

not the least the protection schemes have also been implemented. This chapter highlights the various development stages of prototype hardware setup.

CHAPTER 3

DROOP CONTROL OF MICROGRID

In electric power system, load and generators are interconnected in a network known as grid. In a grid, loads as well as generators are synchronized to each other at a particular frequency in a distributed fashion. Since it is pertinent to mention here that power demand in the grid always keep changing because of very nature of load. Therefore, generators are required to generate the exact amount of power which is demanded by the load to operate in a healthy and efficient manner at any instant. Anytime an increase in power demand causes retardation in rotating speed of the generators at the rate of their inertial response which is reflected in reduced electric power frequency. Restoring the frequency at the previous value needs more mechanical input to the generators. Here it is important to mention that inertia of turbine-generator plays a vital role in instantaneous power balancing. The energy stored and delivered by inertial response of turbine-generator system is proportional to the rate of change of frequency during dynamic change in load and generation. Therefore, higher the inertia (large generator) lower will be the rate of change of frequency with respect to change in load and vice versa. Further, it can be said that at steady state by maintaining frequency at particular value, demanded power can be matched with the generated power. Therefore, a generator is required to continuously match the demand in tune with the control of the turbine power input. At early stage, this control was performed by adjusting the throttle valve opening of turbine by manual operation. Thereafter, the fly-ball speed governor and subsequently different types of electro-hydraulic/ pneumatic and electronic governor were developed to increase the control performance and reliability.

3.1 Droop Control

In conventional power system, by regulating frequency at particular value requires match between demand and supply of active power in a grid. However, the extent at which generator is able to regulate the frequency by its governor action is decided by its generation capacity. The power system is considered by having a number of generators interconnected where each generator has capability to operate at its some maximum output capacity. Therefore, only one generator cannot regulate the frequency by controlling its output and hence, control action must be shared among many generators (but not necessarily all) . In this regards, there are two ways for governor control model:

a)   Flat line or isochronous governor control: In this method, governor always tends to restore the frequency at set value. A huge effort is made by governor to remain at set frequency irrespective of the load level. In such control, smaller generators start oscillating around the set frequency due to their lower inertia constant.

b)   Droop characteristics control: Isochronous governor's strict frequency control tends to overload the smaller generator in transient condition. Therefore, in practice, where multiple different size generating sources participate in frequency control, a droop characteristic followed by each governor according to their capacity. A droop characteristics curve of particular generator is depicted in Figure 3.1. It shows droop curve is a linear relationship between generated power output and its frequency. The generator rotates at a higher frequency and a lower frequency on no-load and full load condition respectively. This, no load to full load condition varies among generator sizes, hence all generator contribute in frequency control in accordance with their sizes.

A droop characteristic gives a good stability in load frequency control but fails to provide many other things such as:

a)   A droop based governor control fails to restore frequency at set value due to its dependency on generation output.
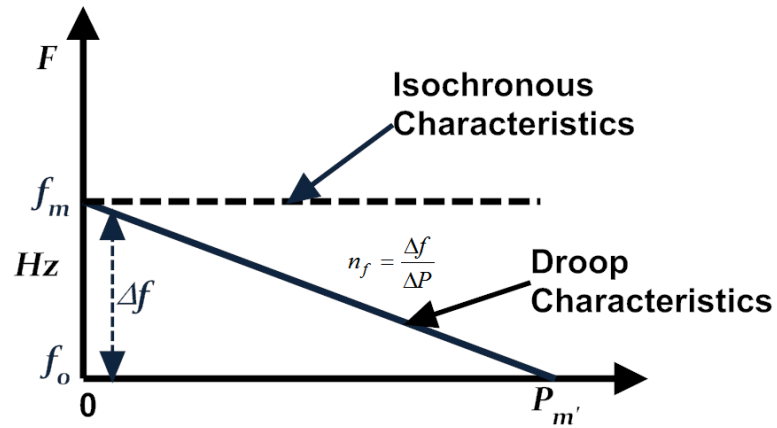
Figure 3.1 – Governor Characteristics Curve

b)   As each droop characteristic of generators is set independently there-
        fore, it becomes difficult to find effective load frequency regulation for
        grid.

c)   Cost of power production is never considered in governor's droop con-
        trol.

Theoretically, with droop control, a generator fails to achieve full load or zero
load condition without changing its droop characteristics according to the grid
condition. Hence, to remove these drawbacks a centralized control is used which is
known as automatic generation control (AGC). This control continuously changes
the frequency set point of droop curve for each generator as per generation cost
and grid condition.

3.1.1   Static Voltage Source Inverter (VSI) vs Synchronous Generator (SG)

The VSI and SG both generate alternating power but have different dynamic
behavior. SG has large rotating mass which stores energy in the form of inertia.
This inertia provides dynamic power balancing through variation in stored kinetic
energy which obtained through change in rotational speed. This power balancing
also persists in multiple interconnected sources where each source shares power
dynamically according to their inertia constant. On the other hand, VSI do not
have such inertia and therefore, no effect occurs on the source frequency due to

load variations. In this case, effects of load variation are compensated by only source impedances.

3.1.2 Power Sharing Parallel VSI

A Source without any inertial system can transfer power to the load at fixed frequency[48]. The similar condition is there for flat line governor control with zero inertia. This type of source can work independently with any type of load dynamics and manage power supply instantly [49]. However, it becomes difficult to balance power dynamically where different inertia less sources have been interconnected to share power in transient and dynamic condition [50]. Thus, it is important to implement a control which can enable the system to share power as per their respective power ratings [51][52].

3.1.3 Power sharing using Dedicated Communication Link:

Multiple VSIs can share common load power demand among each other by knowing dynamic output variables of each others. The reference output power for each inverter can be calculated by radiometric division of total load current according to their rated capacity [53]. However, this required measurement of instantaneous voltage and current of every source and load terminals. This will require a high bandwidth dedicated communication line with high reliability. For short distance between sources, the required bandwidth can be achieved but for long distance, these communication lines become exponentially costly [54, 55].

3.1.4 Power sharing using droop control:

Inter connected VSI's can share common load power demand among each other without any dedicated communication line by incorporating droop characteristics within their control loop. This will work similar to the governor droop control in conventional grid[56].

3.2 Parallel Operation using Droop Control

From the late 80's to early 2000, numerous works had been found on parallel operation of uninterruptible power supplies to share power and efforts [57][58]. These are mainly focused on system configuration and their protection problem [59]. Research shows that parallel operation of voltage source inverters with other similar inverters or with the utility sources are sensitive to disturbances from the load or other sources and can easily be damaged by over current and other transient conditions [45][60]. Therefore, parallel operation of VSI not only requires exact knowledge of types of system configuration, control methods but also needs extremely careful attention about system design [53][61].

Parallel operation of UPS within small area with the concept of a redundant multi-inverter system includes extended monitoring of the status and the operating conditions of all power electronic equipment[59]. These systems require closed high bandwidth communication among inverters [62]. For better operation, further master/slave architectures has been proposed in which one of the inverters acts as master and sets voltage and current reference for the other inverters[63]. This method allows parallel operation of an arbitrary number of inverter modules by a simple control method [64][65][66]. The main problem with Master/slave types of systems is that their lower reliability as they have to rely on high bandwidth communication system. Moreover, whole system fails when master system malfunctions or receives a breakdown. To overcome such problem, droop based scheme for controlling parallel-connected inverters in a stand-alone AC supply system was proposed. These schemes were suitable for control of inverters in distributed source environments such as in isolated AC systems, large and distributed uninterruptible power supply (UPS) systems, photovoltaic systems connected to AC grids, and low-voltage DC power transmission meshes [67][68]. They also considered the emergency and redundant circuit configuration of distributed uninterruptible power supply (UPS) systems [69]. These systems are highly desired to provide high quality and uninterrupted power to critical loads in case of any disturbance or failure.

Few papers discussed about the system configuration issues of distributed UPS.

These can be classified as on-line or line-interactive systems. Many authors addressed the design issue in droop controlled inverters that causes inaccurate power sharing [[70][71][72]. They analyzed and proposed the various schemes with combination of Voltage Controlled and Current-Controlled PWM inverters [73]. In these schemes, each of the units can be designed nearly independent. As a result, the parallel operation of UPS is easy to implement and to expand system capacity[74] [75]. Further, for improved power sharing in droop based DG units operating in LV multi-bus microgrid, a virtual inductor is proposed at the inverter output for proper real and reactive power decoupling[76][67]. Virtual inductors prevent the coupling between the real and reactive powers by introducing inductive impedance in a LV network with resistive line impedances[74][77]. The proposed control can accurately control the DG output, real and reactive powers in both grid-connected and islanding mode without any physical communications among DG units .

3.3   Concept of Droop Control in Microgrid

Active and reactive power expression in steady state interconnected voltage source inverters via impedance represented by (a) can be derived similar to power expression for synchronous generator with its internal impedance connected to infinite bus [105-108]. It is assumed that VSI has stiff internal control so that, power output does not depend on internal loop characteristics[78][79]. The equivalent circuit & phasor diagram of network is shown in Figure 3.2 [108-110].

From the above diagram, active and reactive power (P & Q respectively) at receiving end can be expressed as:

$$P = 3\left(\frac{EV}{Z}\cos(\delta) - \frac{V^2}{Z}\right)\cos(\theta) + 3\frac{EV}{Z}\sin(\delta)\sin(\theta) \qquad (3.3.1)$$

$$Q = 3\left(\frac{EV}{Z}\cos(\delta) - \frac{V^2}{Z}\right)\sin(\theta) - 3\frac{EV}{Z}\sin(\delta)\cos(\theta) \qquad (3.3.2)$$

where R, X,V and E are Line resistance, Line inductance, Source Voltage and Grid Voltage respectively. The impedance angle θ is defined as
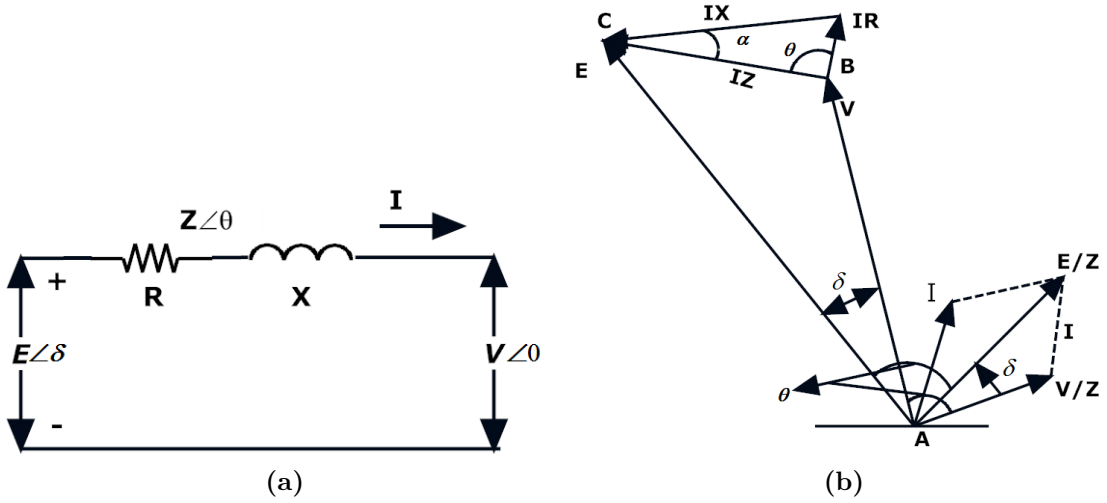
Figure 3.2 – Equivalent Circuit & Phasor Diagram of Network

$$\theta = \cos^{-1}\frac{R}{\sqrt{R^2 + X^2}}$$

Taking assumption that, the line impedance is purely inductive so $Z = X$ and $\theta = 90^0$ Then equation (3.3.1) & (3.3.2) reduced to,

$$P = \frac{EV}{X}sin(\delta) \tag{3.3.3}$$

$$Q = \frac{EV}{X}cos(\delta) - \frac{V^2}{X} \tag{3.3.4}$$

Usually the angle δ is very small so, sin δ ≈ δ and cos δ ≈ 1 can be taken, and consequently,

$$P = \frac{EV}{X}.\delta \tag{3.3.5}$$

$$Q = \left(\frac{EV}{X} - \frac{V^2}{X}\right) \tag{3.3.6}$$

and for small perturbation,

$$\Delta\delta \propto \Delta P \tag{3.3.7}$$

$$\Delta E \propto \Delta Q \tag{3.3.8}$$

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From above deduction, linear droop relation can be established between $f - P$ and $E - Q$, i.e.

$$\omega = \omega * - n_f.P \tag{3.3.9}$$

$$E = E^* - n_v Q \tag{3.3.10}$$
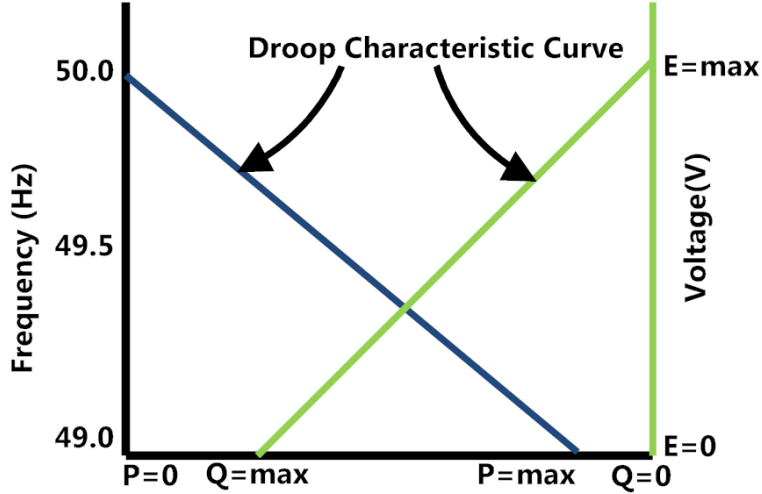
Figure 3.3 – Voltage and Frequency Droop Charactersticss

Where E is the amplitude of the inverter output voltage; ω is the frequency of the inverter; ω* and E* are the frequency and amplitude at no-load, respectively; and n_f and n_v are the proportional droop coefficients of frequency and voltage. Figure 3.3, depict the droop characteristics curve voltage and frequency [80]. The value of droop coefficient defines the slop of $f - P$ and $V - Q$ characteristics curve. As per IEEE Std. 1547.4, frequency and voltage deviation in an islanded microgrid cannot be greater than 2% and 5% from its nominal values respectively. Therefore,

$$n_f < \left. \frac{\Delta f_{\max}}{P \max} \right| \tag{3.3.11}$$

where

$$\Delta f_{\max} = \frac{\Delta f}{f_{nominal}} < 2 \tag{3.3.12}$$

and similarly

48

$$n_v = \frac{\Delta V}{V_{nominal}} \times 100 < 5 \qquad (3.3.13)$$

3.4 Small signal Modeling and Stability analysis of microgrid

The small signal model having two inverters with droop control has been developed to test the characteristics of VSI based microgrid [81][82]. For simplicity, it is assumed that voltage and current loop has sufficiently high bandwidth (ideal) therefore, can be eliminated from analysis with the assumption that the output reference of the droop controller is exactly followed by VSI [83][78].. However, voltage and current controller dynamics (non-ideal case) can affect the microgrid stability and characteristics which may further be investigated by incorporating their inner control loop model in analysis [66-67]. Microgrid in island condition works as isolated system as shown in Figure 3.4 and can be described by homogenous state space equation $\dot{X} = AX$. State Transition matrix A can be derived for two parallel inverter system. Each inverter is assumed to be ideal source under droop characteristics described by equation (3.4.1) & (3.4.2) [84][85][86].
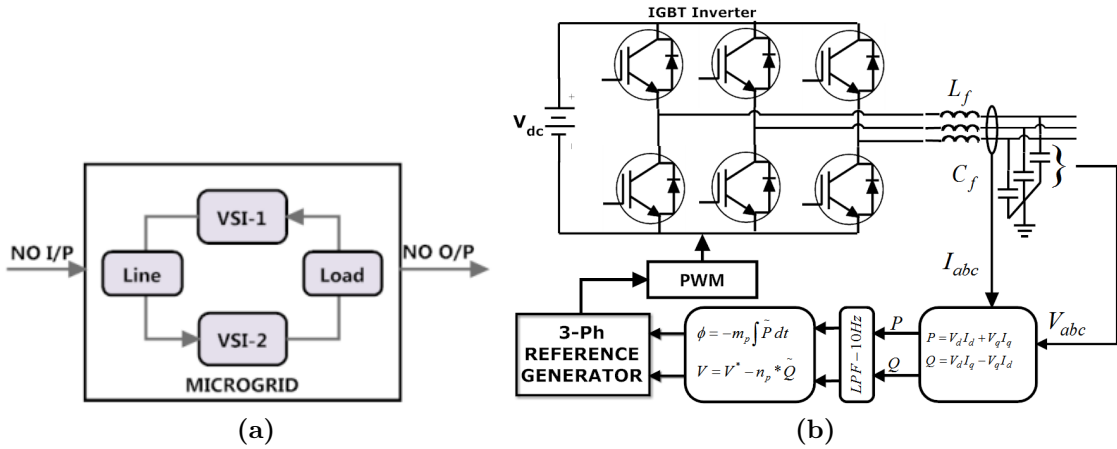
Figure 3.4 – Island Microgrid & Inverter interface

$$\omega = \omega_0 - n_f \bar{P} \qquad (3.4.1)$$

$$E = E_0 - n_v \bar{Q} \qquad (3.4.2)$$

3.4.1 Power controller and Inverter Model

Power P can be computed in D-Q reference frame as

$$\bar{P}(s) = \frac{\omega_c}{s + \omega_c} P(s) \tag{3.4.3}$$

$$\bar{Q}(s) = \frac{\omega_c}{s + \omega_c} Q(s) \tag{3.4.4}$$

Here, ω_c is the cut-off frequency of the filter to remove double harmonic ripple and white noise from calculated power. Linearizing the equations give,

$$\Delta\omega(s) = -\frac{n_f \omega_c}{s + \omega_c} \Delta P(s) \tag{3.4.5}$$

$$\Delta E(s) = \frac{-n_v \omega_c}{s + \omega_c} \Delta Q(s) \tag{3.4.6}$$

and in differential form, we can write

$$\Delta\dot{\omega} = -\omega_c \Delta\omega - n_f \omega_c \Delta P \tag{3.4.7}$$

$$\Delta\dot{E} = -\omega_c \Delta E - n_v \omega_c \Delta Q \tag{3.4.8}$$

Let voltage vector $\vec{E}$ can be represented as:

$$\vec{E} = E_d + j E_q \tag{3.4.9}$$

where $E_d = E\cos(\delta)$ & $E_q = E\cos(\delta)$ are direct and quadrature component of $\vec{E}$ respectively and

$$\delta = \tan^{-1}\left({}^{E_q}/_{E_d}\right)$$

Linearizing equations aroundδ;

$$\Delta\delta = \frac{1}{1 + \left(\frac{E_q}{E_d}\right)^2} \frac{\Delta E_q}{E_d} + \frac{1}{1 + \left(\frac{E_q}{E_d}\right)^2} \left(\frac{-E_q}{E_d^2} \Delta E_d\right) \tag{3.4.10}$$

$$\Delta\delta = \frac{E_d}{E_d^2 + E_q^2} \Delta E_q + \left(\frac{-E_q}{E_d^2 + E_q^2}\right) \Delta E_d \tag{3.4.11}$$

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or

$$\Delta \delta = m_d \Delta E_d + m_q \Delta E_q \tag{3.4.12}$$

where,

$$m_d = -\frac{E_q}{E_d^2 + E_q^2} \ \& \ m_q = \frac{E_d}{E_d^2 + E_q^2}$$

and $\Delta \omega = s \triangle \delta$

$$\Delta \omega = m_d \Delta \dot{E}_d + m_q \Delta \dot{E}_q \tag{3.4.13}$$

The magnitude of voltage can be written as

$$E = \left| \vec{E} \right| = \sqrt{E_d^2 + E_q^2} \tag{3.4.14}$$

Linearize equation will be,

$$\Delta E = n_d \Delta E_d + n_q \Delta E_q \tag{3.4.15}$$

where

$$n_d = \frac{E_d}{\sqrt{E_d^2 + E_q^2}} \ \& \ n_q = \frac{E_q}{\sqrt{E_d^2 + E_q^2}}$$

and first partial derivative ,

$$\Delta \dot{E} = n_d \Delta \dot{E}_d + n_q \Delta \dot{E}_q \tag{3.4.16}$$

Solving equation (3.4.7),(3.4.8) & (3.4.13) gives following linear differential equation:

$$\Delta \dot{E}_d = \frac{n_q}{m_d n_q - m_q n_d} \Delta \omega + \frac{m_q n_d \omega_c}{m_d n_q - m_q n_d} \Delta E_d + \frac{m_q n_q \omega_c}{m_d n_q - m_q n_d} \Delta E_q + \frac{n_v m_q \omega_c}{m_d n_q - m_q n_d} \Delta Q \tag{3.4.17}$$

$$\Delta \dot{E}_q = \frac{n_d}{m_q n_d - m_d n_q} \Delta \omega + \frac{m_d n_d \omega_c}{m_q n_d - m_d n_q} \Delta E_d + \frac{m_d n_q \omega_c}{m_q n_d - m_d n_q} \Delta E_q + \frac{n_v m_d \omega_c}{m_q n_d - m_d n_q} \Delta Q \tag{3.4.18}$$

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and writing in matrix form gives

$$
\begin{bmatrix} \Delta\dot{\omega} \\ \Delta\dot{E}_d \\ \Delta\dot{E}_q \end{bmatrix} = [M] \begin{bmatrix} \Delta\omega \\ \Delta E_d \\ \Delta E_q \end{bmatrix} + [C] \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix}
\tag{3.4.19}
$$

Further, the active and reactive power output can be calculated as

$$
\begin{aligned}
P &= E_d I_d + E_q I_q \\
Q &= E_d I_q - E_q I_d
\end{aligned}
\tag{3.4.20}
$$

In matrix form, the linearized equations will be

$$
\underbrace{\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix}}_{\Delta S_x} = \underbrace{\begin{bmatrix} I_d & I_q \\ I_q & -I_d \end{bmatrix}}_{I_{sx}} \underbrace{\begin{bmatrix} \Delta E_d \\ \Delta E_q \end{bmatrix}}_{\Delta E_x} + \underbrace{\begin{bmatrix} E_d & E_q \\ -E_q & E_d \end{bmatrix}}_{E_{sx}} \underbrace{\begin{bmatrix} \Delta I_d \\ \Delta I_q \end{bmatrix}}_{\Delta I_x}
\tag{3.4.21}
$$

Representing in symbolic form,

$$
\Delta S_x = I_{sx}\Delta E_x + E_{sx}\Delta I_x|_{x=1,2}
\tag{3.4.22}
$$

Now, for two inverters, above equation (3.4.19) can be extended as

$$
\underbrace{\begin{bmatrix} \Delta\dot{\omega}_1 \\ \Delta\dot{E}_{d1} \\ \Delta\dot{E}_{q1} \\ \Delta\dot{\omega}_2 \\ \Delta\dot{E}_{d2} \\ \Delta\dot{E}_{q2} \end{bmatrix}}_{\Delta\dot{X}_N} = \underbrace{\begin{bmatrix} M_1 & 0 \\ 0 & M_2 \end{bmatrix}}_{Ms} \underbrace{\begin{bmatrix} \Delta\omega_1 \\ \Delta E_{d1} \\ \Delta E_{q1} \\ \Delta\omega_2 \\ \Delta E_{d2} \\ \Delta E_{q2} \end{bmatrix}}_{\Delta X_N} + \underbrace{\begin{bmatrix} C_1 & 0 \\ 0 & C2 \end{bmatrix}}_{Cs} \underbrace{\begin{bmatrix} \Delta P_1 \\ \Delta Q_1 \\ \Delta P_2 \\ \Delta Q_2 \end{bmatrix}}_{\Delta S}
\tag{3.4.23}
$$

$$
\Rightarrow \Delta\dot{X}_N = M_s\Delta X_N + C_s\Delta S
\tag{3.4.24}
$$

Where ΔS is complex power output for two inverter system defined as,

$$
\Delta S = \begin{bmatrix} I_{s1} & 0 \\ 0 & I_{s2} \end{bmatrix} \begin{bmatrix} \Delta E_1 \\ \Delta E_2 \end{bmatrix} + \begin{bmatrix} E_{s1} & 0 \\ 0 & E_{s2} \end{bmatrix} \begin{bmatrix} \Delta I_1 \\ \Delta I_2 \end{bmatrix}
\tag{3.4.25}
$$

or in symbolic form as

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$$\Delta S = I_s \Delta E + E_s \Delta I \tag{3.4.26}$$

Putting ΔS into equation (3.4.24) gives

$$\Delta \dot{X}_N = M_s \Delta X + C_s (I_s \Delta E + E_s \Delta I) \tag{3.4.27}$$

$$\Delta \dot{X}_N = [M_s][\Delta X] + [C_s I_s][\Delta E] + [E_s][\Delta I] \tag{3.4.28}$$

3.4.2 Network and Load Model
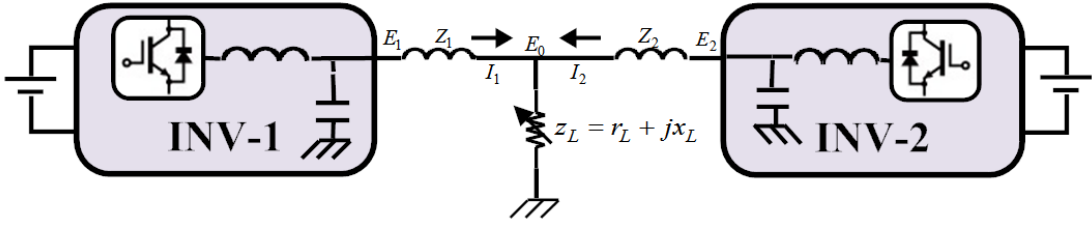
Figure 3.5 – Network and Load Model

Earlier all equations are representing the state-space model of an inverter in the microgrid. If two inverters are interconnected by the transmission line having a common load as shown in Figure 3.5, then the load is shared by each inverter according to the system parameters and controller dynamics. In this case, the inverter's output current in dq can be described by the following differential equations.

$$\frac{di_{1d}}{dt} = \frac{-r_1}{L_1} i_{1d} + \omega_1 i_{1q} + \frac{1}{L_1} E_{1d} - \frac{E_{0d}}{L_1} \tag{3.4.29}$$

$$\frac{di_{1q}}{dt} = \frac{-r_1}{L_1} i_{1q} - \omega_1 i_{1d} + \frac{1}{L_1} E_{1q} - \frac{E_{0q}}{L_1} \tag{3.4.30}$$

$$\frac{di_{2d}}{dt} = \frac{-r_2}{L_2} i_{2d} + \omega_2 i_{2q} + \frac{1}{L_2} E_{2d} - \frac{E_{0d}}{L_2} \tag{3.4.31}$$

$$\frac{di_{2q}}{dt} = \frac{-r_2}{L_2} i_{1q} - \omega_2 i_{2d} + \frac{1}{L_2} E_{2q} - \frac{E_{0q}}{L_2} \tag{3.4.32}$$

From nodal relationship we can write,

$$I_1 + I_2 = \frac{E_0}{Z_L} \tag{3.4.33}$$

$$(I_{1d} + jI_{1q} + I_{2d} + jI_{2q}) = \frac{E_{0d} + jE_{0q}}{R + jX} \tag{3.4.34}$$

$$E_{0d} = R\left(I_{1d} + I_{2d}\right) - \omega L\left(I_{1q} + I_{2q}\right) \tag{3.4.35}$$

$$\underbrace{\begin{bmatrix} \Delta \dot{i}_{1d} \\ \Delta \dot{i}_{1q} \\ \Delta \dot{i}_{2d} \\ \Delta \dot{i}_{2q} \end{bmatrix}}_{\Delta \dot{I}} = [A_{Line}] \underbrace{\begin{bmatrix} \Delta i_{1d} \\ \Delta i_{1q} \\ \Delta i_{2d} \\ \Delta i_{2q} \end{bmatrix}}_{\Delta I} + [B_{Line}] \underbrace{\begin{bmatrix} \Delta E_{1d} \\ \Delta E_{1q} \\ \Delta E_{2d} \\ \Delta E_{2q} \end{bmatrix}}_{\Delta E} \tag{3.4.36}$$

and symbolically can be represented as,

$$\Delta \dot{I} = A_{line}\Delta I + B_{line}\Delta E \tag{3.4.37}$$

where,

$$A_{Line} = \begin{bmatrix} \left(\frac{-r_1}{L_1} - \frac{R}{L_1}\right) & \left(\omega_1 + \frac{\omega L}{L_1}\right) & -\frac{R}{L_1} & \frac{\omega L}{L_1} \\ \left(\omega_1 + \frac{\omega L}{L_1}\right) & \left(\frac{-r_1}{L_1} - \frac{R}{L_1}\right) & -\frac{\omega L}{L_1} & -\frac{R}{L_1} \\ -\frac{R}{L_2} & \frac{\omega L}{L_2} & \left(\frac{-r_2}{L_2} - \frac{R}{L_2}\right) & \left(\omega_2 + \frac{\omega L}{L_2}\right) \\ -\frac{\omega L}{L_2} & -\frac{R}{L_2} & -\left(\omega_2 + \frac{\omega L}{L_2}\right) & \left(\frac{-r_2}{L_2} - \frac{R}{L_2}\right) \end{bmatrix}$$

$$B_{line} = \begin{bmatrix} 1/L_1 & 0 & 0 & 0 \\ 0 & 1/L_1 & 0 & 0 \\ 0 & 0 & 1/L_2 & 0 \\ 0 & 0 & 0 & 1/L_2 \end{bmatrix}$$

Combining equation (3.4.28) and (3.4.37)gives,

$$\begin{bmatrix} \Delta \dot{X}_N \\ \Delta I \end{bmatrix} = \begin{bmatrix} M_s & C_s E_s \\ 0 & A_{Line} \end{bmatrix} \begin{bmatrix} \Delta X_N \\ \Delta I \end{bmatrix} + \begin{bmatrix} C_s I_s \\ B_{Line} \end{bmatrix} [\Delta E] \tag{3.4.38}$$

Here, the voltage input vector in above equation (3.4.37) is the output of the inverters therefore we can write,

$$
\underbrace{\begin{bmatrix} \Delta E_{1d} \\ \Delta E_{1q} \\ \Delta E_{2d} \\ \Delta E_{2q} \end{bmatrix}}_{\Delta E} = \left[\underbrace{\begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{K_s} \;\middle|\; 0 \right]_{4 \times 10} \underbrace{\begin{bmatrix} \Delta \omega \\ \Delta E_{1d} \\ \Delta E_{1q} \\ \Delta E_{2d} \\ \Delta E_{2q} \\ \overline{\Delta I} \end{bmatrix}}_{\Delta X_N \mid \; \Delta I}
\tag{3.4.39}
$$

Incorporating equation (3.4.38) into (3.4.39) gives

$$
\begin{bmatrix} \Delta \dot{X}_N \\ \Delta I \end{bmatrix} = \begin{bmatrix} M_s & C_s E_s \\ 0 & A_{Line} \end{bmatrix} \begin{bmatrix} \Delta X_N \\ \Delta I \end{bmatrix} + \begin{bmatrix} C_s I_s \\ B_{Line} \end{bmatrix} \begin{bmatrix} K_s & 0 \end{bmatrix} \begin{bmatrix} \Delta X_N \\ \Delta I \end{bmatrix}
\tag{3.4.40}
$$

or

$$
\begin{bmatrix} \Delta \dot{X}_N \\ \Delta I \end{bmatrix} = \begin{bmatrix} [M_s + C_s I_s K_s]_{6 \times 6} & [C_s E_s]_{6 \times 4} \\ B_{Line} K_s & A_{Line} \end{bmatrix}_{10 \times 10} \begin{bmatrix} \Delta X_N \\ \Delta I \end{bmatrix}
\tag{3.4.41}
$$

The state space model of two inverter microgrid system can be represented symbolically as:

$$
\dot{X} = [A_{MG}] [X]
\tag{3.4.42}
$$

3.5 Effect of Droop Coefficient in Microgrid

The determination of the droop coefficient values is the critical part in the designing of the microgrid. These values not only determine the minimum and maximum variation in microgrid voltage and frequency but also they shape the transient, dynamic performance and stability of the whole system. The effect of droop coefficient in microgrid can be observed by plotting the modes (Eigen values) of microgrid model for different values of droop coefficient. The Figure 3.6 shows change

in two inverter microgrid's eigen value with change in frequency and voltage droop coefficients of both VSIs respectively under the initial conditions given in Table-3.1. The initial conditions are calculated by solving network for set values of load and line parameters.

Parameters	INV-I	INV-2
Nominal Frequency (ω_0) rad/sec	314	314
Steady state frequency (ω) rad/sec	312.116	312.116
Power Filter Cut-off freqency (ω_c) rad/sec	10	10
Line Resistance (R)	0.12Ω	0.13Ω
Line Inmpedance (X)	0.30 Ω	0.32 Ω
Common Load Resistance (R_L)	11 Ω	
Common Load Impedance (X_L)	1.136 Ω	
Inverter's Currents (d,q)	I_d =2.51, I_q=-3.840 A	I_d =17.77, I_q=1.559 A
Inverter's Voltages	E_d=230, E_q=0	E_d=229.12, E_q=20.05
Droop Coeffient (f,V)	0.005 rad/W, 0.05 V/VAr	0.005 rad/W, 0.05 V/VAr

Table 3.1 – Intitial Condtions

The frequency droop coefficients are changed from $^{0.02}/_{4e3}$ to $^{0.5}/_{4e3}$ at $^{0.1}/_{230}V$ droop in fixed step. It is observable that when there is increase in droop coefficient, few Eigen values which have earlier only real parts, now having imaginary part too and therefore, can create power oscillation at sub synchronous frequency within the microgrid. These Eigen values also move towards imaginary axis with the increase in droop coefficient resulting lower stability margin. Similarly, voltage droop coefficients also have high impact on some Eigen values on real axis near to the origin. These Eigen values moves to the right side of imaginary axis with the increase in voltage droop coefficient depicting voltage instability.

3.6 Primary Control in Microgrid

As discussed earlier, microgrid control structure has different layers. Each layer of control has different dedicated functions. In primary control layer, voltage source inverters are controlled to share the required amount of complex power with other
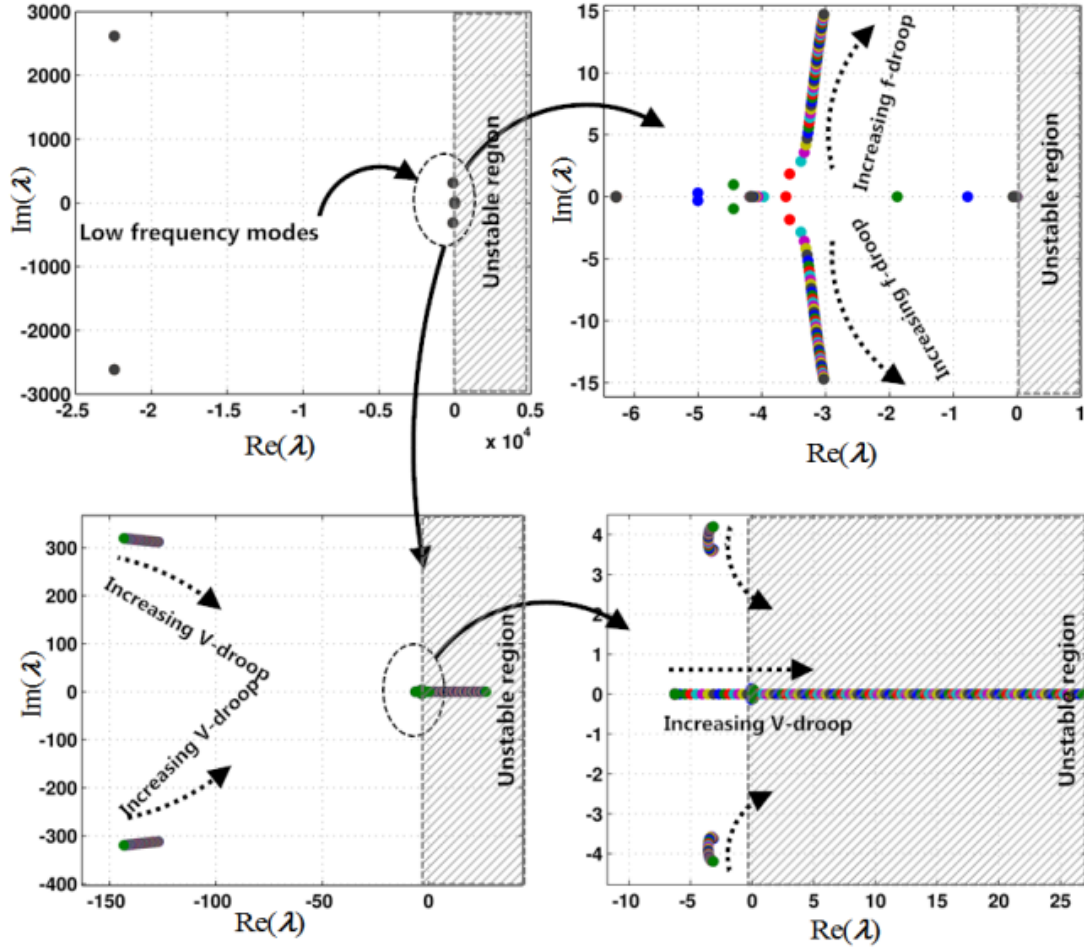
Figure 3.6 – Effect on modes of microgrid due to variation in different droop parameters

* F droop – 0.02/4e3 to 0.5/4e3 at 0.1/230 V-droop
*V droop – 0.02/230 to 2/230 at 0.1/4e3 f-droop

Table 3.2 – Modes of Microgrid at Different f-Droop Values

Modes /F-V Droop	0.2/4000-0.1/230	0.2/4000- 0.2/230	0.2/4000-0.5/230
λ_1	-22445.01 + 2617.17i	-22445.01 + 2617.18i	-22445.019 + 2617.22i
λ_2	-22445.01 - 2617.17i	-22445.01 - 2617.18i	-22445.019 - 2617.22i
λ_3	-127.61 + 312.56i	-128.48 + 312.91i	-131.08 + 313.98i
λ_4	-127.61 - 312.56i	-128.48 - 312.91i	-131.08 - 313.98i
λ_5	-3.25 + 6.0i	-3.42 + 6.07i	-3.51 + 6.42i
λ_6	-3.25 - 6.00i	-3.42 - 6.07i	-3.51 - 6.42i
λ_7	-0.012+ 0.0i	-0.02+ 0.0i	**3.29 + 0.0i**
λ_8	-4.16 + 0.00i	-2.042 + 0.0i	**0.017 + 0.0i**
λ_9	-6.28 + 0.012i	-6.27 + 0.016i	-6.26 + 0.02i
λ_{10}	-6.28 - 0.012i	-6.27 - 0.016i	-6.26 - 0.022i

microgrid sources. The controller also expected to maintain output voltage wave shape nearly sinusoidal under various disturbances. The basic primary control scheme for VSI in microgrid that largely available in literature is shown in Figure 3.7.
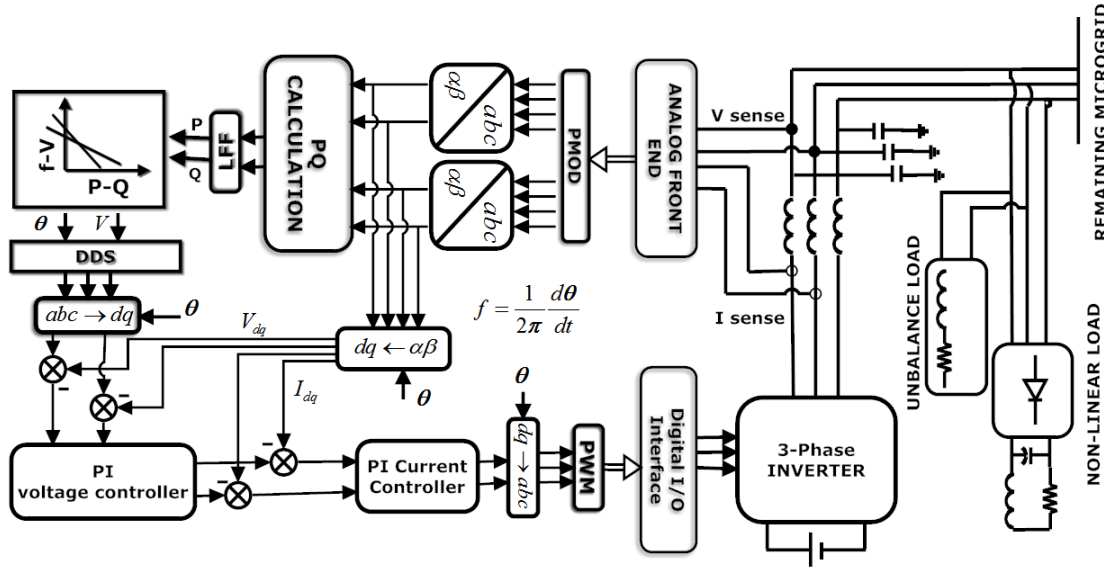
Figure 3.7 – Basic Control Stretegy forVSI in microgrid

3.6.1 Controller design:

Primary control generally requires three control loops. Each control loop dynamics affects dynamics of other control loops. Therefore careful attention is required during design of each control. In basic procedure, bandwidth limitations are imposed in design of each loop so that coupling effect can be mitigated between loops. The most outer loop i.e. power control loop which can be implemented using droop linear controller has slowest dynamics and hence lower bandwidth. The two inner loop i.e. voltage and current control loop as shown in Figure 3.8 have much faster dynamic response than power control loop. Dynamics of these two inner loops closely affect the shape of voltage waveform as well as losses in inverters (due to circulating current). Therefore, it is important to design the voltage and current controller having good performance and operating dynamics.

3.6.2 Design of Voltage and Current Controller:

The purpose of voltage controller is to track reference input voltage and mitigate any effect of disturbance or dynamic changes on output voltage. The design of voltage controller depends upon various arguments. The bandwidth of controller must be sufficiently high so that it can follow higher order harmonics disturbance or noise. For a set of stable controller, gain of PI controller can be easily calculated by Routh-Hurwitz criterion. There are three main considerations which can be taken to find out the gain of stable PI controller with better performance.

1) The stability constrains imposed on Kp and Ki are established by Routh Hurwitz criteria on loop characteristic equation.

2) Gains are selected to increase the bandwidth of controller with appropriate phase Margin and damping ratios.

3) The bandwidth of controllers must follow the increasing order i.e. Power control loop< voltage control loop< current control loop.
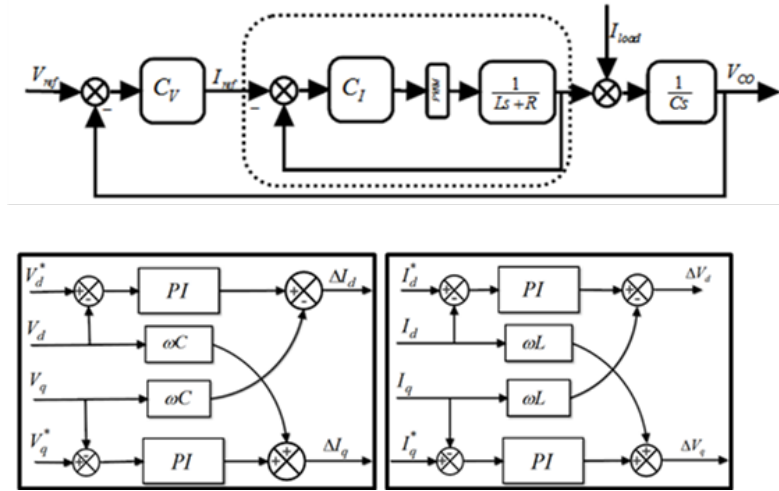
Figure 3.8 – Basic structure of PI voltage and current controllers

For example, simplified voltage loop characteristic equation will be,

$$G(s) = \left(\frac{1}{Ls + R} \right) (K_p + {}^{K_i}/_s) \left(\frac{1}{Cs} \right) \tag{3.6.1}$$

$$(K_p + {}^{K_i}/_s) \left(\frac{1}{Cs(Ls + R)} \right) + 1 = 0 \tag{3.6.2}$$

$$(sK_p + K_i) + Cs^2 (Ls + R) = 0 \tag{3.6.3}$$

$$LCs^3 + RCs^2 + K_ps + K_i = 0 \tag{3.6.4}$$
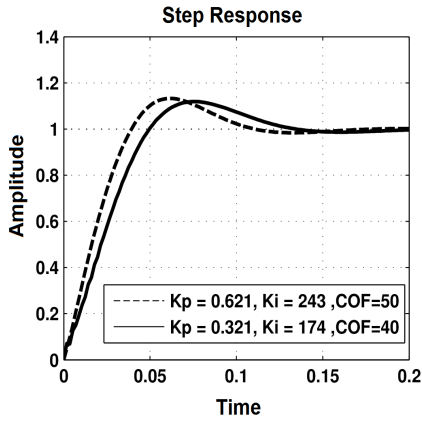
(a) PI gains for Voltage control Loop
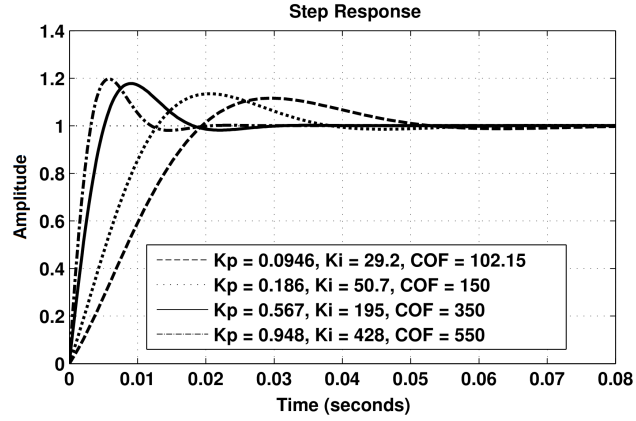
(b) PI gains for current control Loop

*COF=Cross over frequency
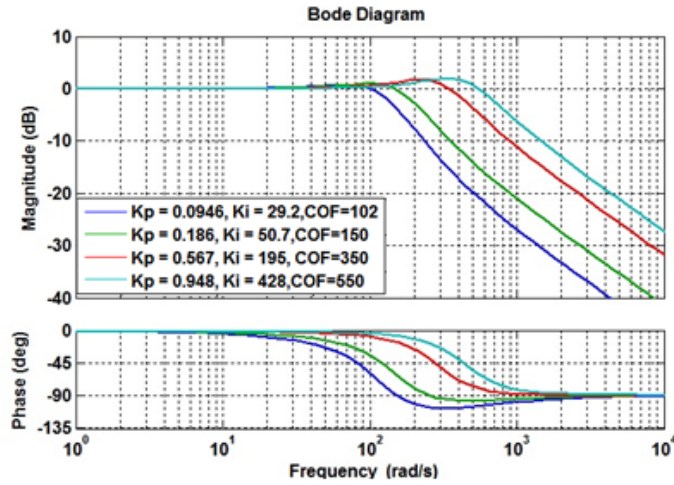
(c) Bode Plot of voltage controller for different Kp & Ki

Figure 3.9 – Controller Responses

Using Routh Hurwitz criteria, we can get following constrain for stable controller

$$K_i > 0 \quad \& \quad K_p < {}^{LK_i}/_R \tag{3.6.5}$$

For suitable value of damping coefficient (0.3-0.7), the value of K_p and K_i can be calculated.

The bandwidth of current loop must be enough high for better regulation and disturbance rejection. The inverter parameters for microgrid are given in Table-I in Appendix (A-1). Based on these parameters, voltage and current controller values can be calculated. The controllers are optimally tuned to give good performance and maximum bandwidth, low overshoot and minimum settling time. The time response for step input has been plotted for different and for both control loop is shown in Figure 3.9. The time response and bode plot shows that, for higher controller bandwidth there is higher overshoot. Therefore, here exists a tradeoff between overshoot and bandwidth in selection of particular parameter.

3.7 Simulation of Droop Control for VSI's in Microgrid

Using droop control, an adequate power sharing can be achieved among the voltage source inverters. The schematic of control system is shown in Figure 3.10.
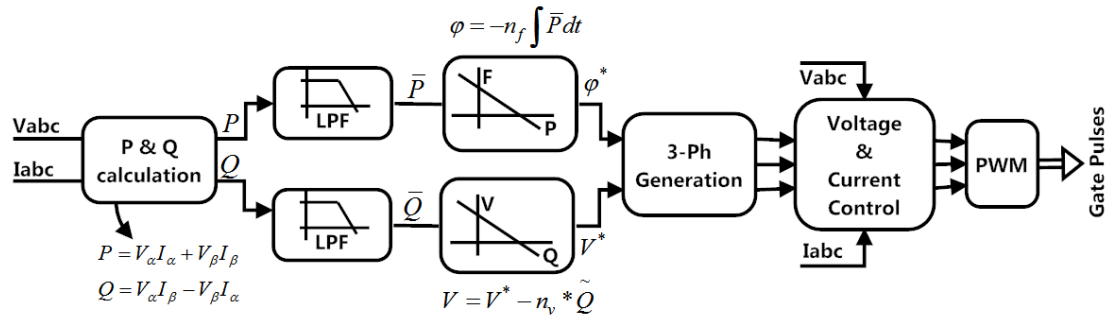
Figure 3.10 – Control Schematic

Droop equation requires knowledge of generated active and reactive output power from VSI. This power can be calculated in reference (see Appendix A-3). The calculated power has double frequency component therefore, average value is obtained using a low pass filter. Once voltage and phase reference is computed using droop equation, then the three phase voltage sinusoid can be generated. These sinusoids are then converted into the direct and quadrature axis voltage component using transformation. The three phase voltage sinusoid generation is not a required part of control as quantities can be calculated directly from voltage

and phase references. However, it makes design flow is more explicit if references are converted into three phase quantities.

3.7.1 Simulation of Parallel Operation of VSI with Linear Droop

The two inverter system can form a minimal AC microgrid when connected in parallel network to share a load. Each inverter will have separate DC battery source which further can be replaced by any renewable energy source [87][88]. In simulation to show the performance of droop control, one of the inverter is first connected to common transmission line and serves the connected load alone. After that the second inverter is connected to same transmission line by synchronizing to network frequency.
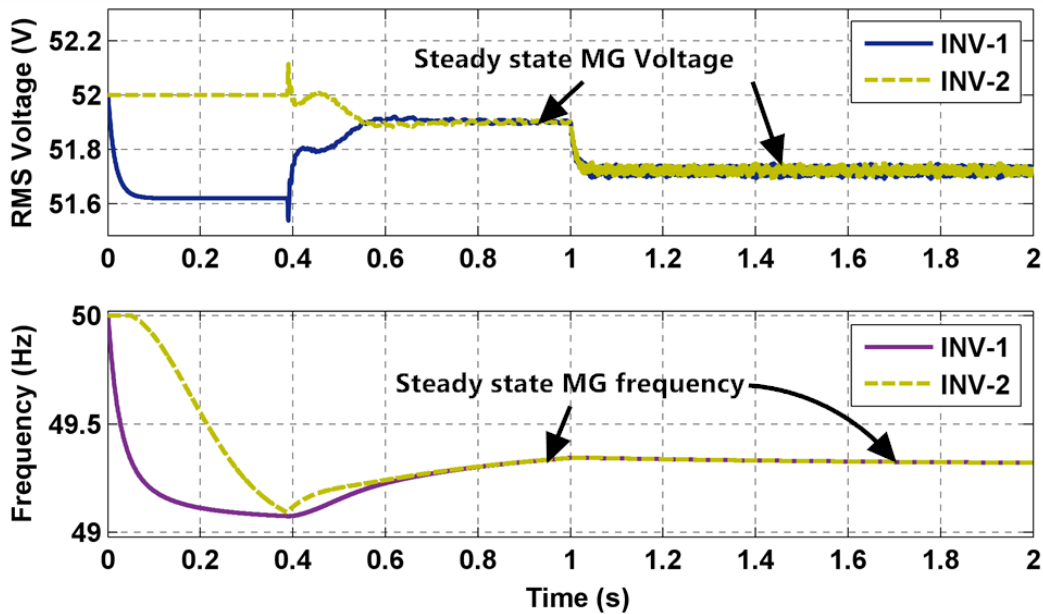
Figure 3.11 – Output Voltage and Frequency in Droop Control

Figure 3.11 & 3.12 shows that when both inverters are under parallel operation, the total load demand is equally shared by them proportional to their respective droop coefficients. The voltage and frequency curve shows the variation in their magnitude according to their power output of inverters. It is also observable that when single inverter is connected to the microgrid, full load on inverter causing much reduced output voltage and frequency. When new inverter is connected to microgrid, it shares power from earlier inverter, hence reducing their power output which raises voltage and frequency of the microgrid.
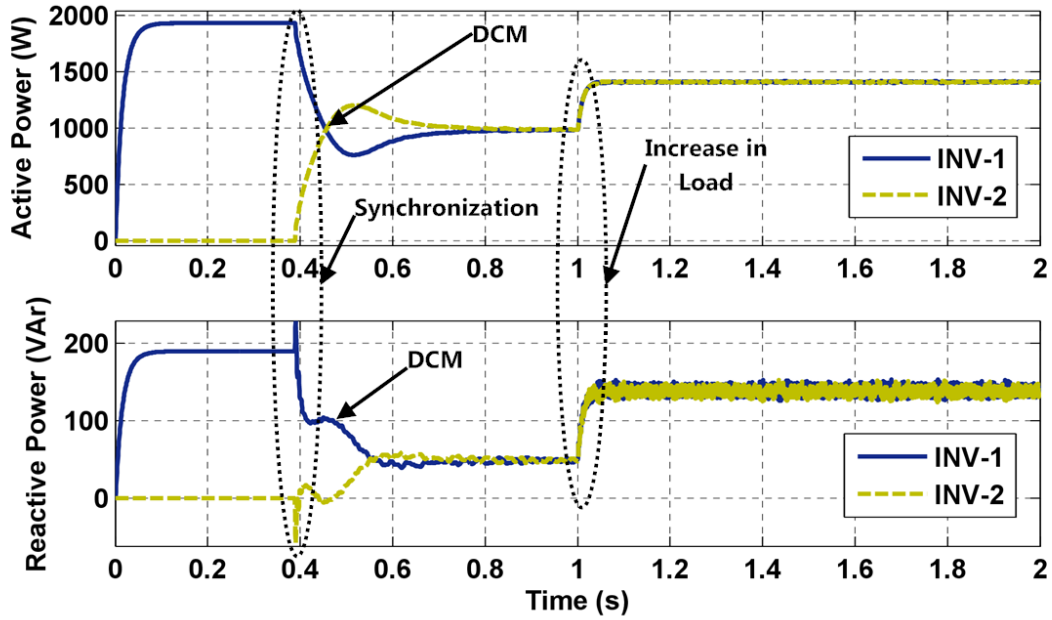
Figure 3.12 – Output Powers in Droop Control
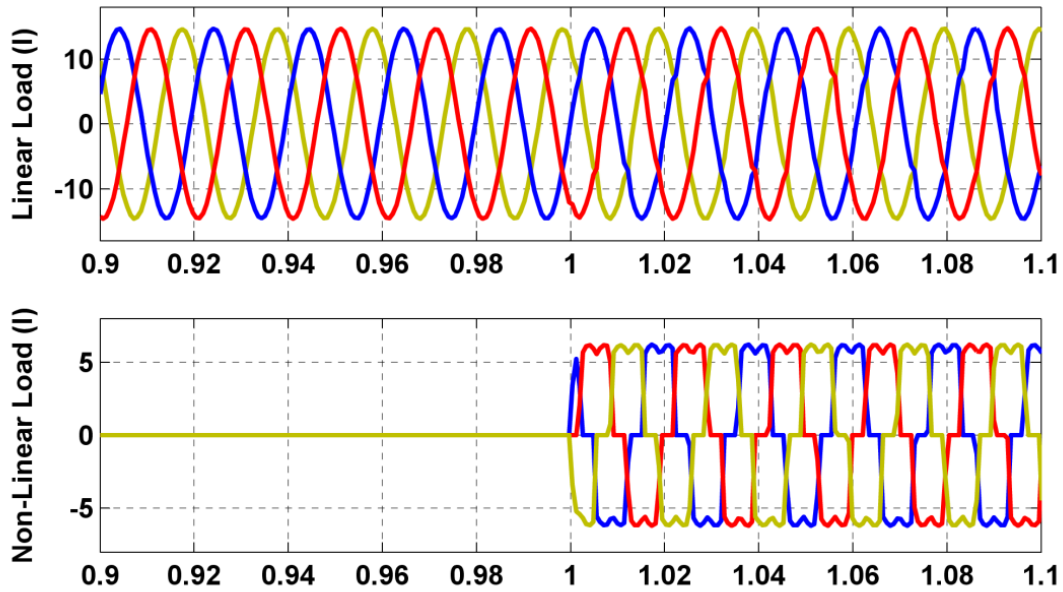
Figure 3.13 – Load Current Profile

Dynamic response can be tested by adding additional load in microgrid as shown in Figure 3.13 & Figure 3.14 where a non-linear load is added to microgrid at t=1sec. The new load is also equally shared by both sources showing good dynamic response. Figure 3.14, shows first phase current of both the inverters. The current profile of both inverters' shows that there is a negligible circulating current among the sources and both inverter also share equal current.
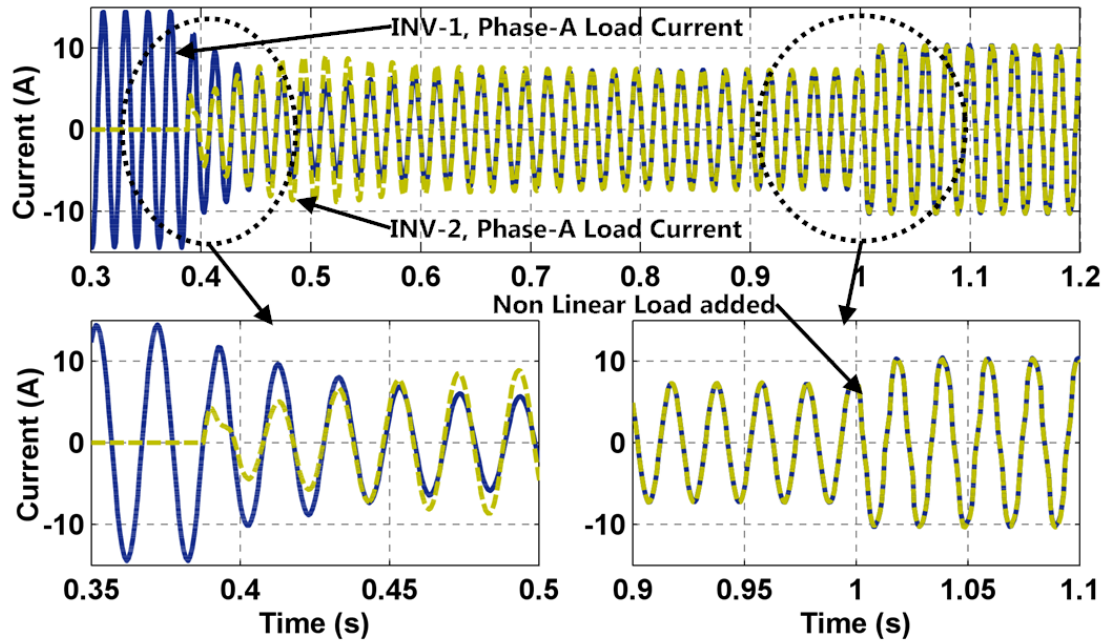
Figure 3.14 – Inverters Output Curernt During Parallel Operation

3.7.2 Effect of Droop Coefficient:

A equal droop coefficient shares equal power among the different sources however, if there are different droop coefficients for each source, then the power sharing will be ratio metric according to their droop coefficient ratio. Figure 3.15 shows the effect of droop coefficient on power sharing. When the frequency droop coefficient of INV-1 is increased to 1.5 times of its initial value, then active power output of the inverter is reduced to almost 75% of its previous value and the frequency of microgrid is also reduced rationally. Although, there is only change in frequency droop coefficient, a small change in reactive power output of inverters can be observed. This shows the existence of a week coupling between frequency and reactive power. This coupling effect becomes more dominant as resistance of the transmission line increases. All of these results not only verify the linear relationship between droop coefficients and the power output of the sources but also verify the dynamic stability in droop control microgrid.

3.7.3 SOC Based Droop Control:

It can be verified by simulation that DC source of each inverter can be replaced by any renewable energy source (RES)[89][90][88]. Figure 3.16 a photovoltaic source
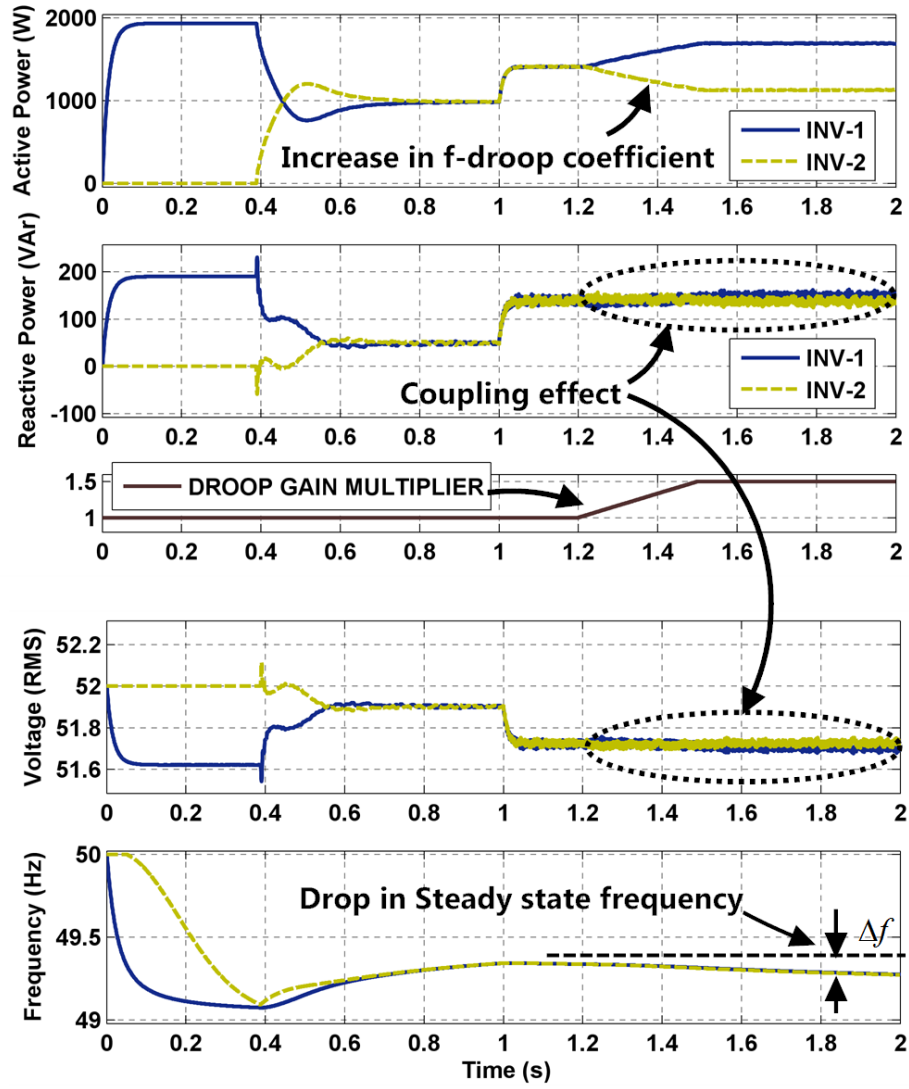
Figure 3.15 – Inverters Output with Varying f-Droop Coefficent
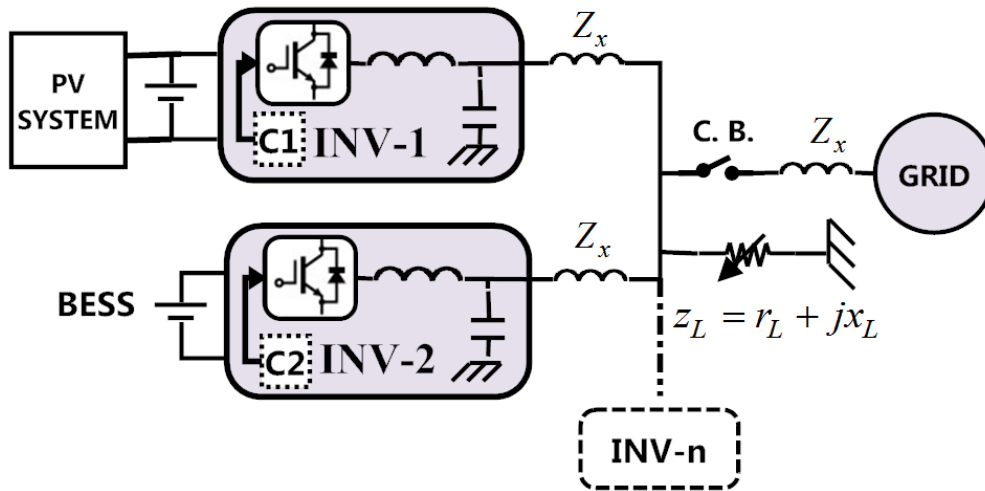
Figure 3.16 – Microgrid with PV System with BESS
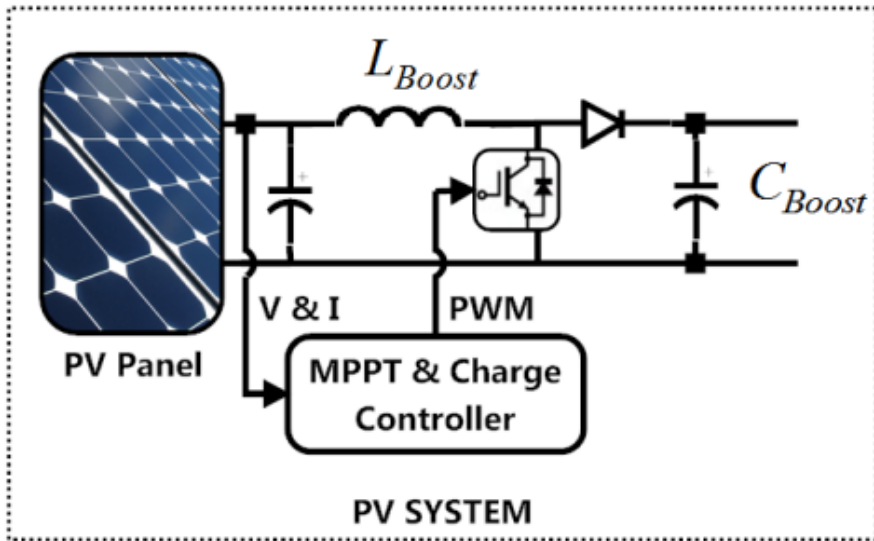
Figure 3.17 – PV System Diagram with MPPT

has been added to one of the VSI at DC side. Photovoltaic system has MPPT controller (Figure 3.17) that transfers maximum power at DC bus as per the solar irradiance[91]. This power either charges battery bank or transferred to the grid on AC side according to the shared load demand of INV-1.
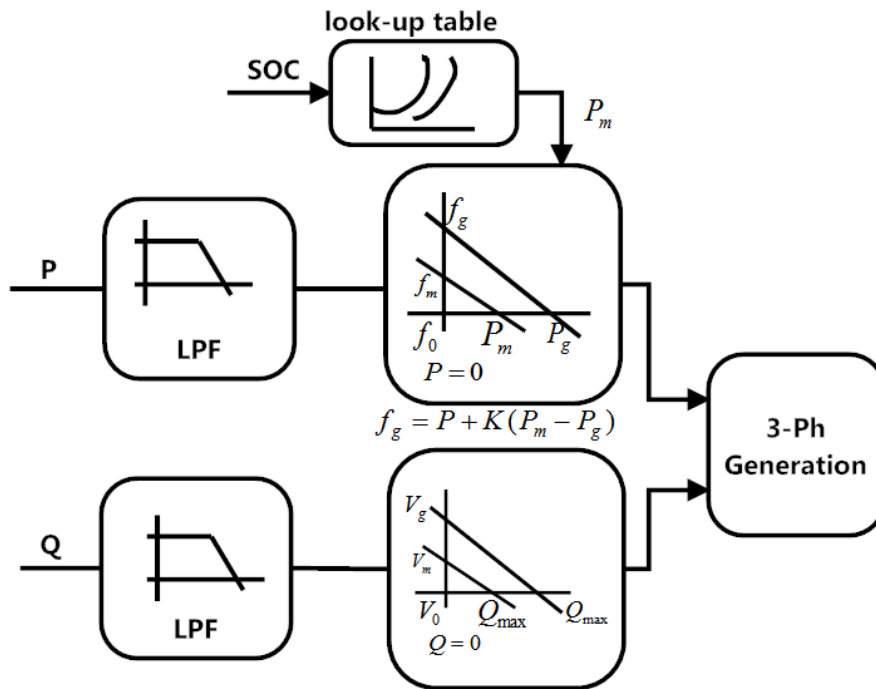
Figure 3.18 – SoC Based Droop Controller

To incorporate the SOC based droop variation a lookup table based controller is designed as shown in Figure 3.18 . The lookup table is providing a map between
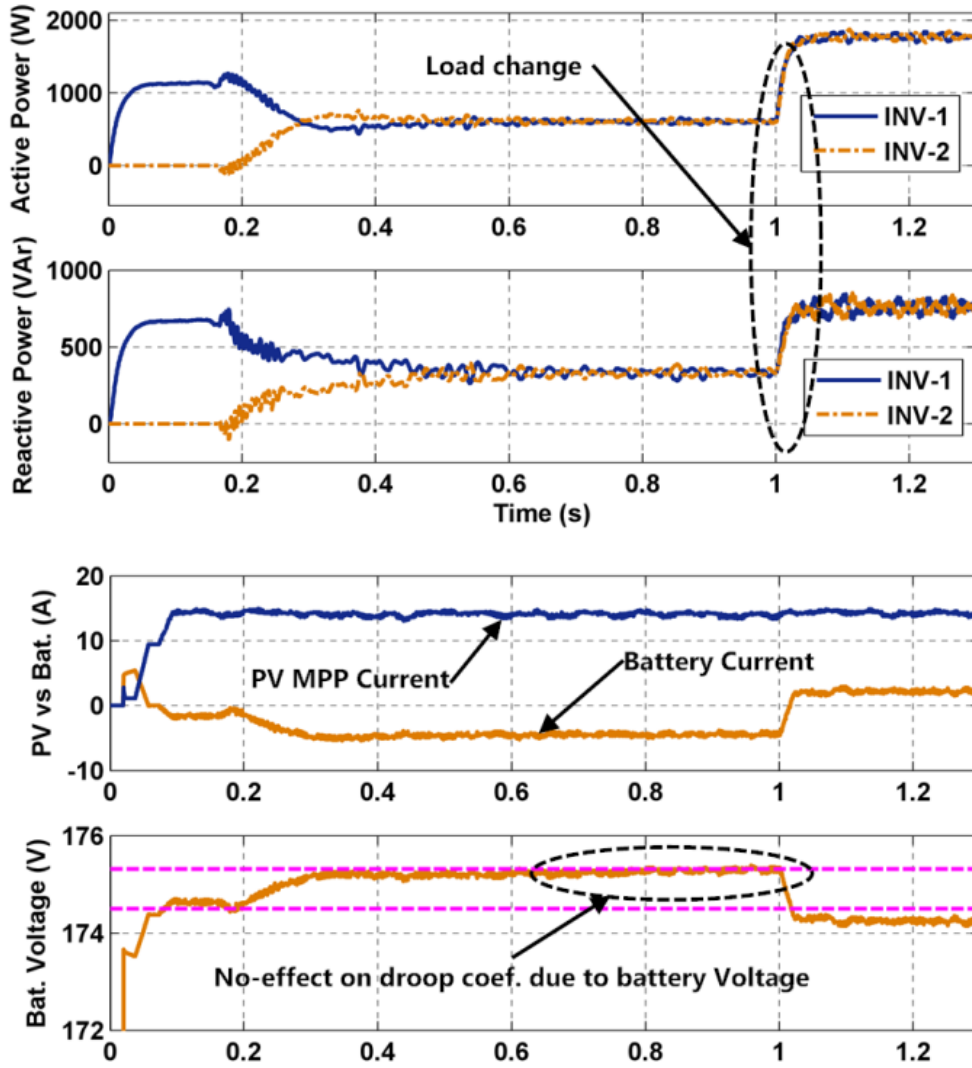
Figure 3.19 – Simulation of PV System without SoC Control in MG

droop coefficient & SOC level. When the SOC level is low, the droop coefficient is set to some higher value. The multiple look-up tables can be formed in similar for different modes of operation. When there is no SOC based control droop coefficient do not change during operation as depicted in Figure 3.19. The simulation shows that both inverters are initially sharing equal power according to their droop control setting, but when PV generation is higher than shared demand of INV-1 and partial power has been used to charge the battery bank of INV-1. This can be observed by negative battery charging current in simulation. Due to charging current, battery's state of charge (SOC) increased to certain limit or full charge level however no effect on droop characteristics occurs in absence of any control. In such case to obtain power balance, PV generation has to be reduced to lower

value which gives lower efficiency of overall system. However, when load demand increases and becomes higher than PV generation then excess power is transferred from the battery bank.
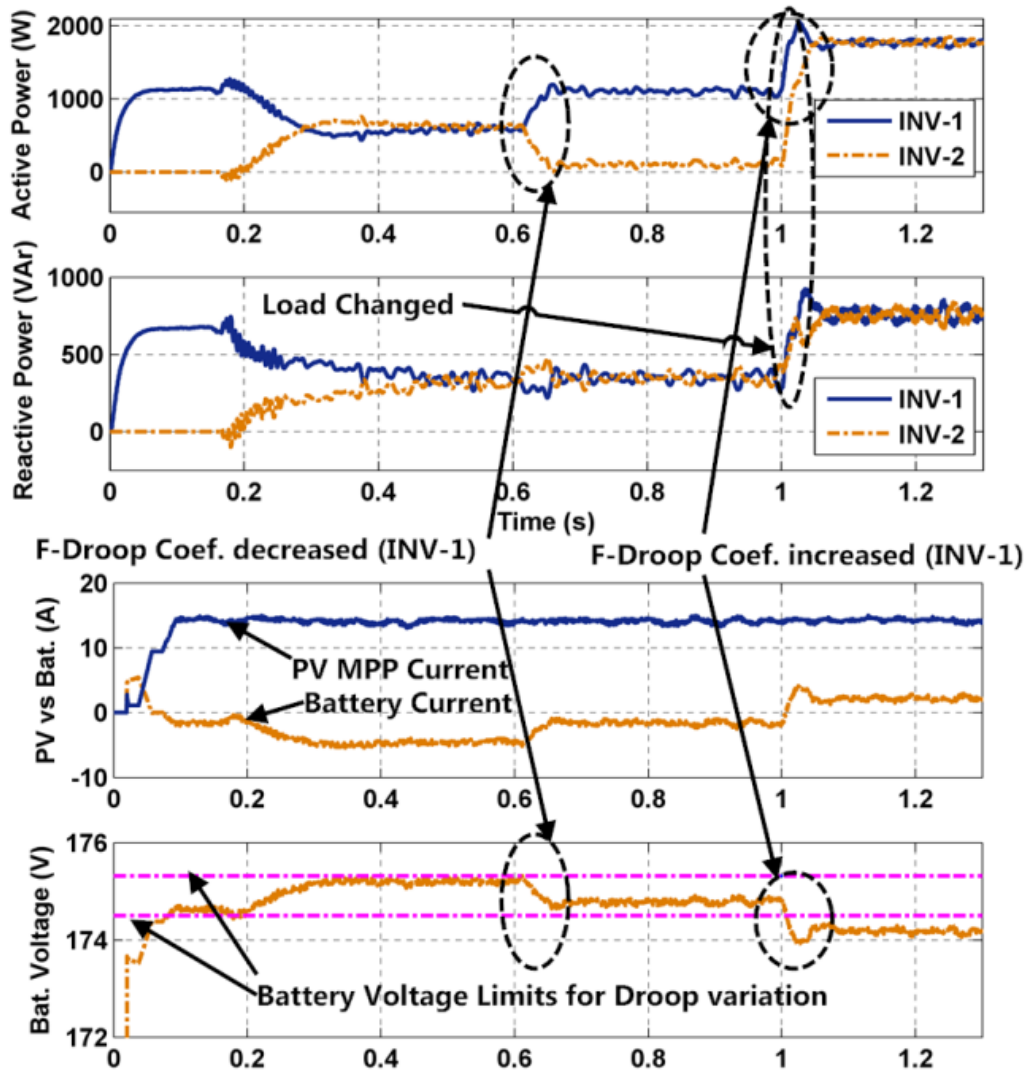
Figure 3.20 – Simulation of PV System with SoC Control in MG

In SOC based control, SOC level of battery is divided in different segment in loop-up table. When battery voltage crosses a segment a corresponding change in droop coefficient are made. When there is no demand of power from grid and battery is fully charged in such case the MPPT control is switched to constant voltage mode. In Figure 3.20 simulation shows similar effect as described earlier. SOC level is divided in only two segment depicted by two dashed horizontal bars. When SOC reached lower bar BESS goes in charging mode by selecting appropriate droop coefficient from look up table as seen at 0.2 sec. When SOC reached upper

limit again new value of droop coefficient are computed from look up table which start discharging the BESS by increasing power sharing by INV-1 as shown at 0.6 sec. However, when total load demand further increased at 1.0 sec SOC of BESS goes below lower limits hence power sharing of INV-1 reduced while output increased.

3.7.4 Grid Tie Mode:
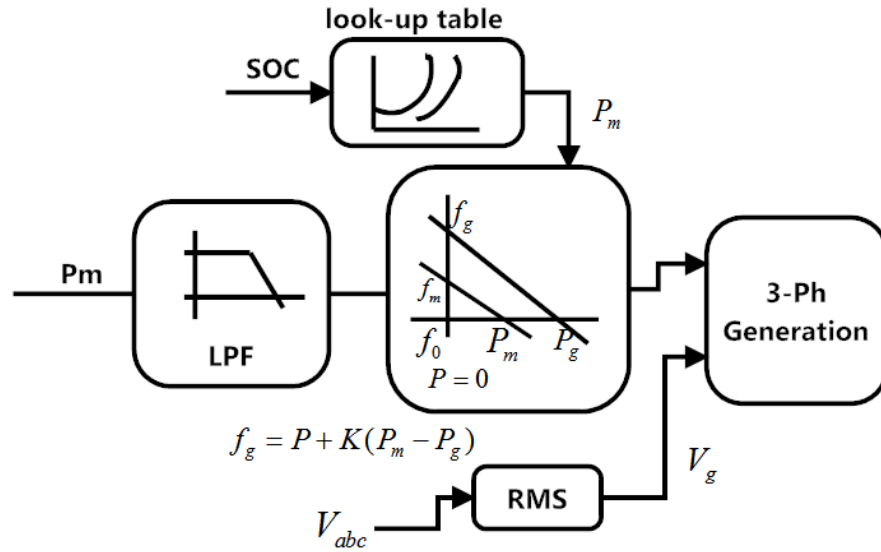
Figure 3.21 – Grid Tie Mode of Control

A microgrid must have ability to work in grid tied as well as in islanded mode of operation. When grid is available, microgrid generates power to reduce total cost of microgrid operation. This can be done by generating the maximum power within the microgrid by renewable energy sources and transfer surplus generation to the main grid. This will reduce the losses in the transmission line of main grid as well as carbon emission caused by fossil fuel on account of reduced demand from main grid. In grid tie mode, microgrid works as consolidated constant power generator or constant load (or PQ bus) and do not participate in voltage or frequency regulation. Figure 3.16 shows DG with VSI based interface connected to the main grid via a circuit breaker (C.B.). The operation of circuit breaker is to connect / disconnect the microgrid with main grid as per operational requirement. If main grid is healthy then microgrid will remain connected to main grid and if there is any disturbance in the main grid, C.B. disconnects the microgrid from

main grid. By this operation, microgrid operates only on its own generation. The control schematic for grid tie mode is given in Figure 3.21.
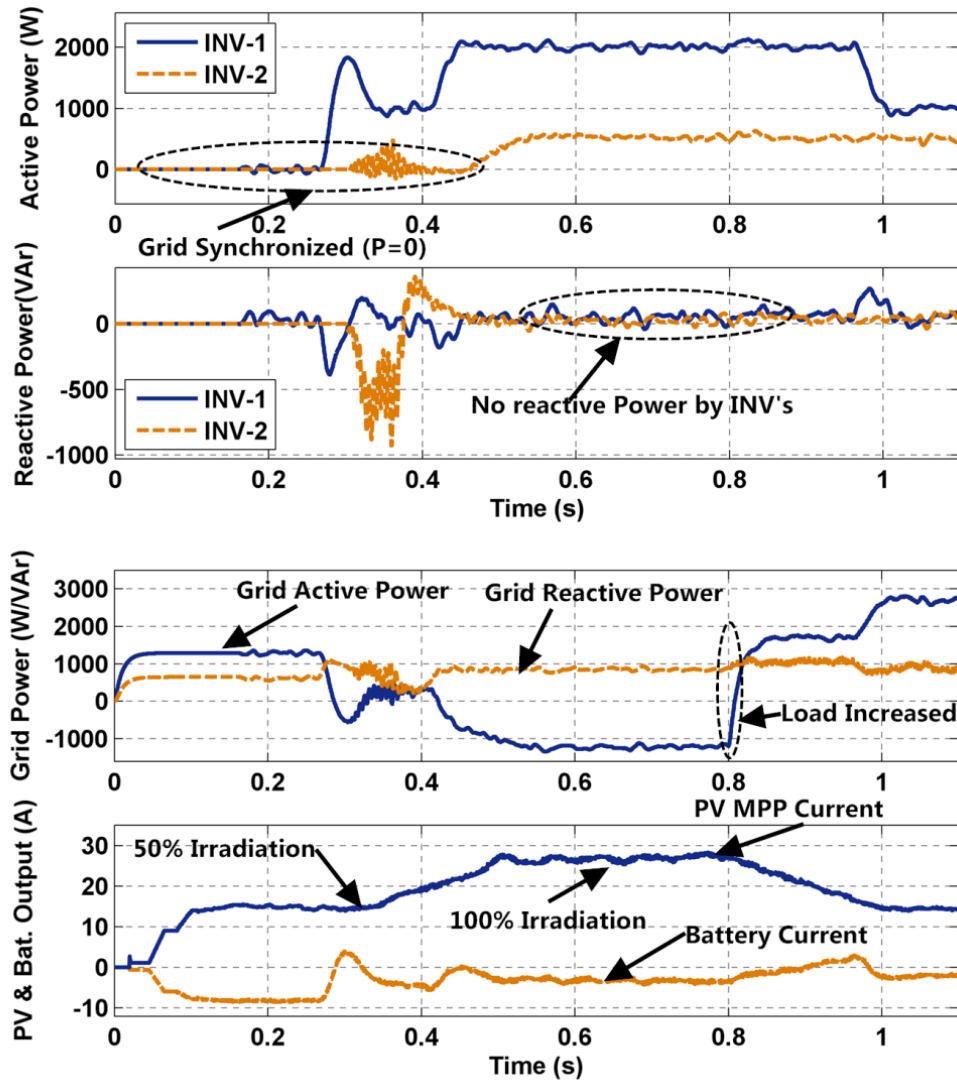
Figure 3.22 – Simulation of PV System in Grid Tie mode

The Figure 3.22 shows that when there is no inverter connected in microgrid, the demanded power is supplied by main grid. At 0.1 sec of simulation time first inverter is synchronized and connected to main grid without any power exchange with grid while at 0.3 sec second VSI is synchronized to grid and remains in standby mode. At 0.25 sec, primary controller of first VSI start transferring power to main grid by setting power reference according to SOC of battery and PV generation. The second VSI has constant DC source therefore, it is set to generate constant power throughout the simulation time. The voltage reference of each VSI is set to follow grid voltage therefore, reactive power generated by each

VSI remains zero and all reactive power is served by main grid. In Figure 3.22 simulations shows that the PV generates power according to the solar irradiation level. Hence, whenever solar irradiance is maximized, PV and battery having higher SOC level and VSI-1 transfer surplus power to grid. But when there is low PV generation and also low battery SOC level in observed, the VSI -1 takes low amount of share of load demand and thus deficit amount of power is taken from the grid.

3.8   A Modified Droop Control

The major problem with linear-droop characteristics is large drop in frequency and voltages at rated shared demand. For example if 80% of time in a microgrid, each inverter is loaded 50% to their rated capacity then due to linear droop characteristics, 80% of time frequency and voltage will be at 50% of droop region. This will need a secondary control to raise frequency or voltage again to nominal value. However, without implementing secondary control a non-linear droop characteristic as shown in Figure 3.23 can be used.
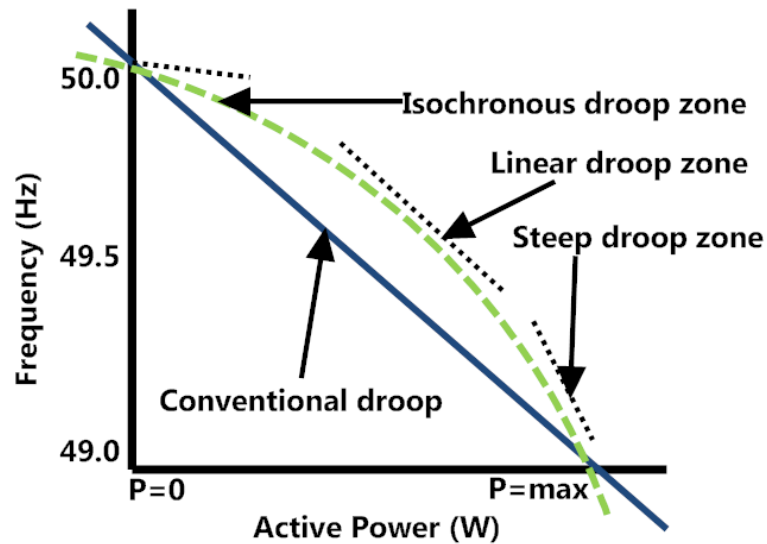
Figure 3.23 – Non-linear Droop Characterstics

The above characteristics can be achieved by making the droop coefficient proportional to power output of inverters, i.e.

$$n_f \propto P \qquad (3.8.1)$$

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Taking new proportionality coefficient n_{fp} such that,

$$n_f = n_{fp}p \tag{3.8.2}$$

The new droop equation now become,

$$\omega = \omega * -n_{fp}P^2 \tag{3.8.3}$$

The value of n_{fp} can take any constant real number, however for simplicity $n_{fp} = n_f/P_{max}$ is taken in simulation.

The simultion result of modified droop control is shown in Figure 3.24, where inverter's-2 droop characteristics have been modified. When both inverters have same droop constant they shares equal power all the time however, when INV-2 droop characteristic is modified, the power output of inverter-2 becomes high at low load condition and reduced relatively when load becomes too high. The grid frequency also remain slightly high at low load condition with modified droop and reduce rapidly when there is overloading. As modified droop characteristics is applied only to droop equations hence reactive power sharing remain same in both the cases.

3.9 Conclusion

In this chapter, a basic control structure of microgrid has been developed. Various aspects of control have been discussed with modeling and simulation results. The real time results have not been provided due to complexity of the complete system. The complexity has been arrived in two ways; first is the time window and second is the multiple numbers of required controllers. To show SOC based results, the real world hardware must run for long duration so that it can show the change in SOC level. On other hand, the control of one PV system and two inverters requires additional hardware and controllers, therefore, it becomes complex and difficult to implement in low cost setup. However, in future, these results can be verified in real time system having long duration run time data acquisition system and powerful distributed controllers.
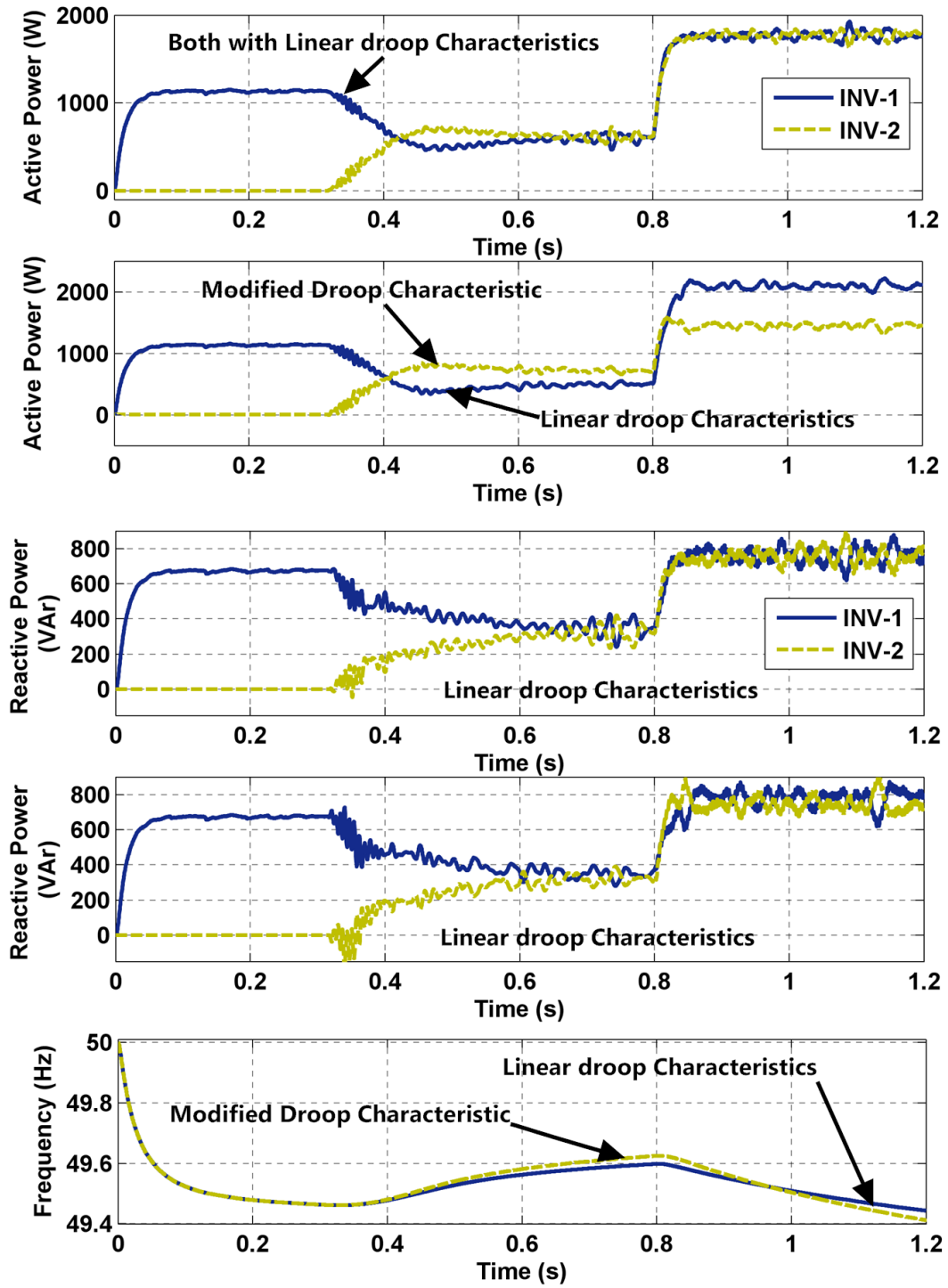
Figure 3.24 – Simulation of Modified Droop Control

REPETITIVE CONTROLLER FOR DROOP BASED MICROGRID

In previous chapter, parallel operation of inverters with droop based control is performed in synchronous reference frame. It uses two step of transformations of three phase voltage and current signals. In the first step all 3-phase signals were transformed in alpha-beta reference and then in the sencond step converted into DQ reference. Proportional plus integral (PI) based voltage and current controller are used in DQ reference frame. These controllers have simple design mechanism with easy implementation in digital processor. The major drawback of these controllers is their low bandwidth and poor performance. When a non-linear load is fed by a VSI, it injects harmonic disturbance of high bandwidth in form current. These harmonics also reflected back into corresponding DQ quantities of current and voltage in control loop. These harmonic current disturbances need to be compensated by controllers so that the effect of non-linear current on terminal voltage waveform of the source can be minimized. This imposes the requirement of a high bandwidth controller which can compensate maximum possible order of harmonic component in the voltage wave. A high bandwidth PI controller can solve this purpose but such PI controller becomes less stable due to its sensitivity to white disturbances (lack of selectivity). Therefore, it becomes mandatory requirement for a high bandwidth controller that selectively compensates all major harmonic components. In the literature majority of voltage control scheme uses proportional plus integral (PI) controller in rotating reference frame, which fails to maintain the desired sinusoidal profile of voltage waveform especially in presence of harmonic current. Many researchers use Proportional plus resonant (PR)

controllers, which deals with harmonic distortion to some extent. However, the strategies based on PR controllers are very complex due to adjustment of gains for each harmonic components of current[92][93]. A perfectly tuned PR controller may exhibit better performance but requires extensive digital hardware (DSP) resources as compared to other controllers. In view of this, a Repetitive controller can be applied to all types of system where disturbances are periodic in nature which is already used in many applications[94]. Some of the researchers have also utilized RC based control approach for VSI in microgrid for Grid tied application[95][96]. Various methodologies have been proposed to design the RC for VSI for different applications. In various litrature, H∞ and frequency adaptive RC has been applied to grid connected VSIs. These control methods uses μ-analysis to minimize H∞ norm to get optimal controller [97][98].

4.1 Multi-loop Control Strategy of Microgrid

In an EPS, active and reactive power outputs from the source are function of voltage and frequency. For a completely decoupled EPS, active and reactive power depends upon either of voltage or frequency. This decoupling depends upon X/R ratio of transmission lines. If lines are purely inductive, the active and reactive power transfer will depend upon the frequency and voltage magnitude respectively whereas it is opposite in the case of resistive lines. Therefore, droop control can be implemented in either of the cases but the conventional droop control may not provide stable operation and proper power sharing among different sources in case of strongly coupled system. In main grid, sources only need to provide the fundamental voltage as it cannot compensate the other high frequency voltage disturbance at long distance. Therefore, harmonic compensations are provided at the distribution end. Microgrid is a small capacity grid confined to small area. It interconnects distributed resources (DR) which already have their local loads. Interconnection of DR generally improves the stability and reliability of the system. The majority of the sources are interfaced via static inverters in ac-microgrid. Inverters are inertia less system, which can give very fast response to the given command. At the same time being inertia less inverter have very short

time overload capacity. Therefore, it is advantageous & major requirement to use a high bandwidth controller where inverters are primarily used as interconnecting interface. Voltage and current control loops regulate the output voltage under various load disturbances within each DR. Block diagram of comprehensive voltage and current controller is shown in Figure (4.1).
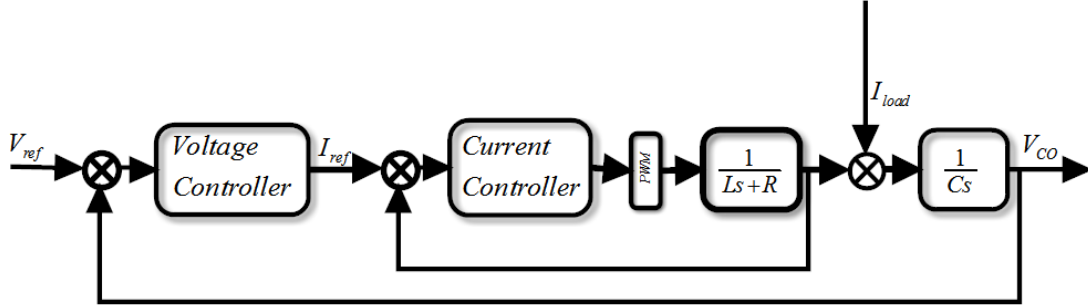
Figure 4.1 – Basic inner loop control

RCs are well known for the rejection of periodic disturbances as it is based on Internal Model Principle (IMP) theory [99, 100, 101, 102]. According to this theory, a controller can reject the entire disturbances for a plant, if it incorporates an internal model of all its disturbances within itself [103]. An Internal model of periodic disturbances can be generated using high order of polynomial, however designing a controller for such system becomes tedious due to complexity involved in the assignment of closed loop poles[104]. Incorporating fixed period time delay (L) in a feedback loop is another way to realize an internal model of a periodic signal as shown in Figure (4.2) [105][106]. The controllers having such time delay consists of large number of poles on imaginary axis. However, such large number of poles may destbilize the system. For the stable operation, these poles must be stabilized in feedback control loop by using appropriate stablilizing controller. However, designing such type of stabilizing controller is very difficult for strictly proper plant just in case of microgrid[107]. To solve this problem many researchers considered using an attenuator or a low pass filter in feedback loop to reduce the complexity in designing a stabilizing controller[108, 109]. This enables in shifting of close loop poles to left hand side in complex plan [110]as shown in Figure 4.4.

(a-1) Without Filter

(a-2) With filter
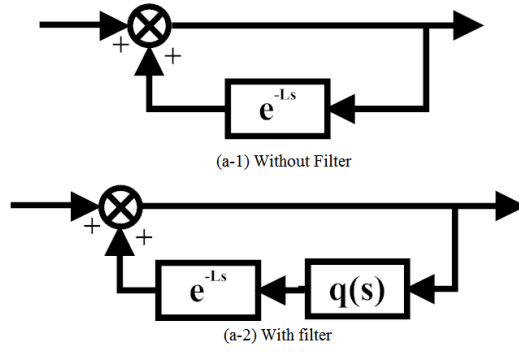
Figure 4.2 – Internal Model of Feedback Time Delay
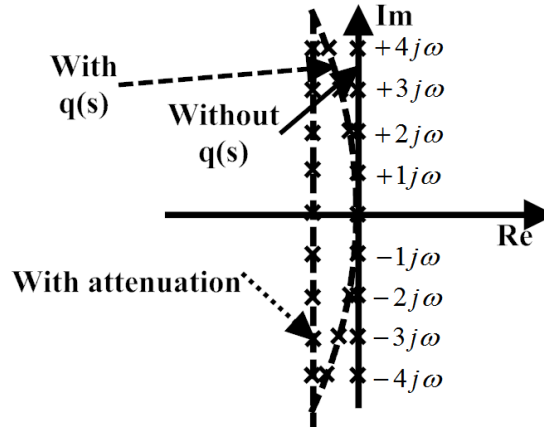
Figure 4.3 – Poles of the Time delay system

4.2 Design of Repetitive Controller

The proposed RC design is implemented in stationary reference frame in order to reduce the number of controllers [111, 112][113]. Hence, Clarke's transformation has been used to convert three phase (abc) quantity into two phases (see Appendix A 2.2). According to [114][115]-133], a generalized RC can attain following form:

$$C\left(s\right) = C_1\left(s\right) + C_2\left(s\right) * C_r\left(s\right) \tag{4.2.1}$$

Where, $C_1(s)$ is an Internally Stabilizing Controller (ISC), $C_2(s)$ is a pre-compensator, and $C_r(s)$ defined as,

$$C_r\left(s\right) = \frac{1}{1 - q\left(s\right)e^{-Ls}} \tag{4.2.2}$$

Where, $q(s)$ is a low pass filter with $q(0) = 1$. Now, A unity feedback system with RC and plant P is reperesented in Figure 4.4. Here, $C_1(s)$ controller is said
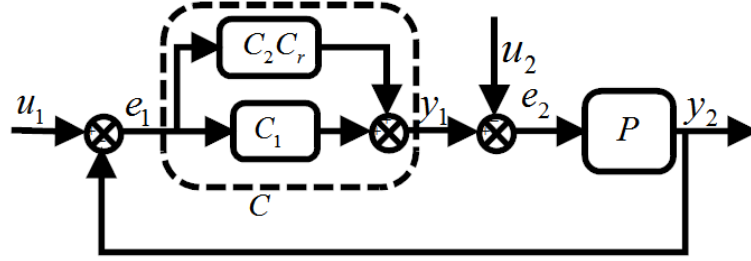
Figure 4.4 – Unity feedback RC

to be an ISC, if and only if all the transfer functions from e to u, as described by (4.2.3), are strictly Hurwitz [103].

$$\begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{1+PC_1} & \frac{-P}{1+PC} \\ \frac{C}{1+PC_1} & \frac{1}{1+PC_1} \end{bmatrix} \begin{bmatrix} u \\ u_2 \end{bmatrix} \tag{4.2.3}$$

Here, u is an input vector and e is an error vector. According to [116][117, 118], set of all controllers $C_1(s)$ that stabilize $P(s)$, can be given by

$$C_1(p) = \frac{X(s) + R(s) * D_P(s)}{Y(s) - R(s) * N(s)} \bigg| \tag{4.2.4}$$

Where, $N_p(s)$ and $D_p(s)$ are the co-prime factors of plant $P(s)$, such that $P(s) = {}^{N_p(s)}/_{D_p(s)}$

and

$$X(s) * N_p(s) + Y(s) * D(s) = 1 \tag{4.2.5}$$

Equation (4.2.5) is known as Bezout's identity[1]. In (4.2.4), $R(s)$ is a free rational function and the value of $R(s)$ is conventionally chosen to maximize the gain of controller $C(s)$ at the fundamental frequency but in this way the impact of the disturbance on the output increases. Therefore, the value of $R(s)$ must be chosen to ensure maximum attenuation to the disturbance and this can be achieved by mixed sensitivity optimization. For this purpose, robust design of the controller can be achieved by mixed sensitivity constraint (4.2.6),

$$\left\| \begin{bmatrix} W_1 S \\ W_2 T \end{bmatrix} \right\|_\infty \leq 1 \tag{4.2.6}$$

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[1]This is also known as Aryabhatta Identity or Diophantine equation [117]

Where, W_1, W_2 are frequency dependent weighting functions, S and T are nominal sensitivity and complimentary sensitivity functions respectively which are defined by:

$$S = \frac{1}{1+PC} \ and \ T = \frac{PC}{1+PC} \qquad (4.2.7)$$

Further, in the absence of suitable controller satisfying (4.2.6), a sub-optimal controller can be designed by minimizing (4.2.6) for a sufficiently large bandwidth. According to [135],[137], for optimal controller , (4.2.6) can be rewritten as:

$$\|W_1 S\| + \|W_2 T\| \ll 1 \qquad (4.2.8)$$

or

$$\|W_1 S\| \ll 1 \ and \ \|W_2 T\| \ll 1 \qquad (4.2.9)$$

or

$$\|S\| \ll \frac{1}{W_1} \ and \ \|T\| \ll \frac{1}{W_2} \qquad (4.2.10)$$

while for $P = \frac{N}{D}$ and $C = \frac{X+RD}{Y-RN}$, (4.2.7) can be written as,

$$S = \frac{1}{1 + \frac{N(X+RD)}{D(Y-RN)}} \qquad (4.2.11)$$

$$S = \frac{D\,(Y-RN)}{XN+DY} \qquad (4.2.12)$$

as $XN + DY = 1$, therefore

$$D\,(Y-RN) < \frac{1}{W_1} \qquad (4.2.13)$$

$$R > \frac{1}{N}\left(Y - \frac{1}{DW_1}\right) \qquad (4.2.14)$$

In inequality (4.2.14), we introduce a free rational function q_r($\|q_r(0) = 1\|$) to make R proper function. However, in (4.2.4) controller can approach to infinite gain at ($\|Y - RN\|_{\omega=\omega_0} = 0$)), this high value of gain can be damped by taking R as

$$R = \frac{q_r}{N_0}\left(Y - \frac{1}{DW_1}\right) \tag{4.2.15}$$

Where, $N_0 = {}^N/_{N_i}$ is the outer function of N.

Similarly, from (4.2.7) and (4.2.14), for complimentary sensitivity T, we can get

$$R < \frac{1}{N_0}\left(Y - \frac{1}{D}\left(1 - \frac{1}{W_2}\right)\right) \tag{4.2.16}$$

Inequality (4.2.16) is complimentary and gives the upper bond for R. The weighing function W_1 is to be selected in order to shape the sensitivity function for any given perturbation bandwidth.

RC requires parameterization of stabilizing controller. The methodology for designing the RC has already been described. Here we use this methodology to design the voltage and current controller for VSI for droop based microgrid.

4.2.1 Design of Voltage Controller:

Figure 4.5 shows the block diagram of control system where, P_1 and P_1 are taken as LC - filter and load transfer functions respectively. Hence, transfer function for P_2 can be written as:

$$P_2 = \frac{K}{(Ls + R_x)} \tag{4.2.17}$$

Where, K is load gain calculated at nominal KVA rating of VSI, L_x & R_x are transmission line parameters. The plant P_1 transfer's function is taken $(1/Cs)$. Then closed loop transfer function (P_1& P_2) will be,

$$\widetilde{P} = \frac{P_1}{1 + P_1 P_2} \tag{4.2.18}$$

$$\widetilde{P} = \frac{K'(s+p)}{s^2 + c_1 s + c_0} \tag{4.2.19}$$

Using parameter from Table-A.1 in appendix-A, (4.2.19) gives following transfer function.

$$\widetilde{P} = \frac{K'(s+166.7)}{s^2 + 166.7s + 1.81e^8} \tag{4.2.20}$$
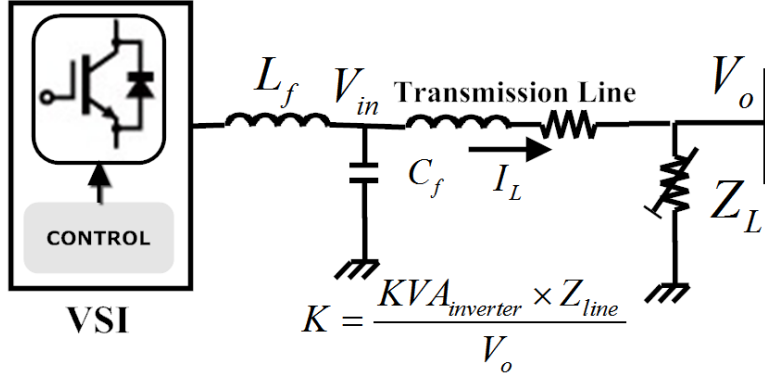
(a) Inverter's interface in microgrid
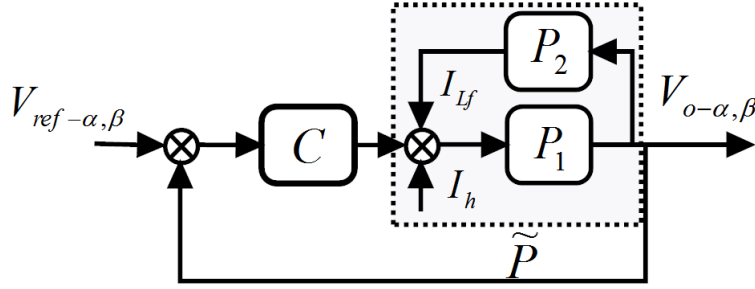
(b) Closed loop diagram of system

Figure 4.5 – Plant Diagram

Where $K' = 1/C_f$

As discussed earlier, $\widetilde{P}$ can be factorized in rational function such that $\widetilde{P} = \frac{\widetilde{N}}{\widetilde{D}}$, where $\widetilde{N}$ and $\widetilde{D}$ are co-prime factors [19], [24]. Weighing function W_1 shapes sensitivity, therefore, taken equal to $\frac{(s+\omega)}{s}$. The corresponding frequency response for sensitivity $\left(S = \left\| \frac{1}{W_1} \right\| \right)$ is shown in Figure 4 6(a), where ω is taken equal to the required bandwidth of controller.

Since plant is strictly proper, it has attenuation for high order frequency and therefore W_2 can be chosen as unity. The value of free variable 'R' is calculated by solving (4.2.15) that gives the parameter of high order ISC ($C_1(s)$). Therefore, the designed controller further reduced by balance truncation method by calculating error bond of Hankel's singular value as:

$$\left\| C_{1V} - \widetilde{C_{1V}} \right\|_\infty \leq 2 \sum_{k+1}^{n} \sigma_i \qquad (4.2.21)$$

Where, k is the order of reduced controller and σ_i is the Hankel's singular values. Hankel's singular values are calculated with separated stable and unstable parts, then transfer function corresponding to relatively higher stable value are

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retained in the controller. The reduced order approximated ISC for voltage controller in 2nd and 1st order transfer function is given in (4.2.22) & (4.2.23).

$$\widetilde{C}_{1V}\left(s\right)^{2nd} = \frac{0.00785s^2 + 1.308s + 1.425e^6}{s^2 + 166.7s + 1.359e^{-14}} \tag{4.2.22}$$

and

$$\widetilde{C}_{1V}\left(s\right)^{1st} = \frac{0.00785s + 8547}{s + 8.154e^{-17}} \tag{4.2.23}$$
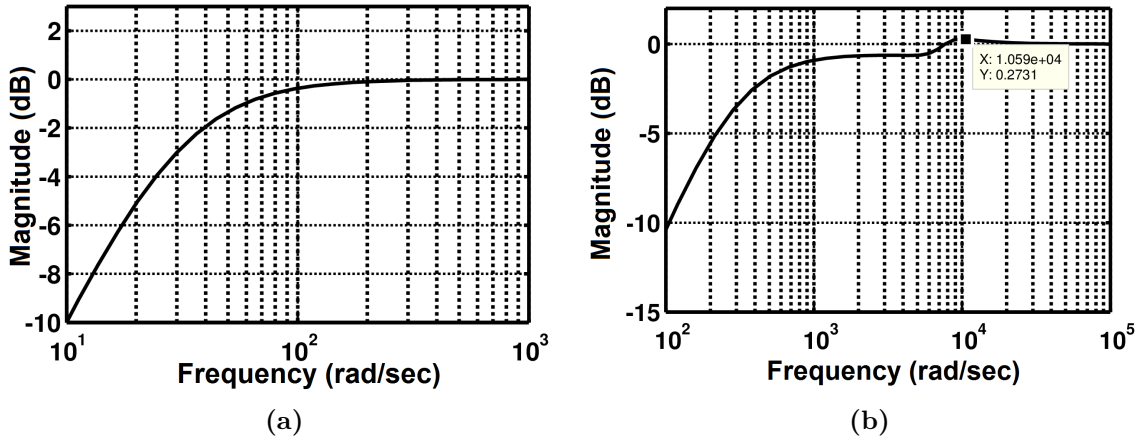
Figure 4.6 – Bode plot of (a) Sensitivity shaping function $1/W_1$ (b) System sensitivity with C_v

Figure 4.6 shows the frequency response of sensitivity with designed controller 4.2.23. It is worthwhile to mention that system attains maximum sensitivity of 0.27dB, hence satisfying (4.2.9).
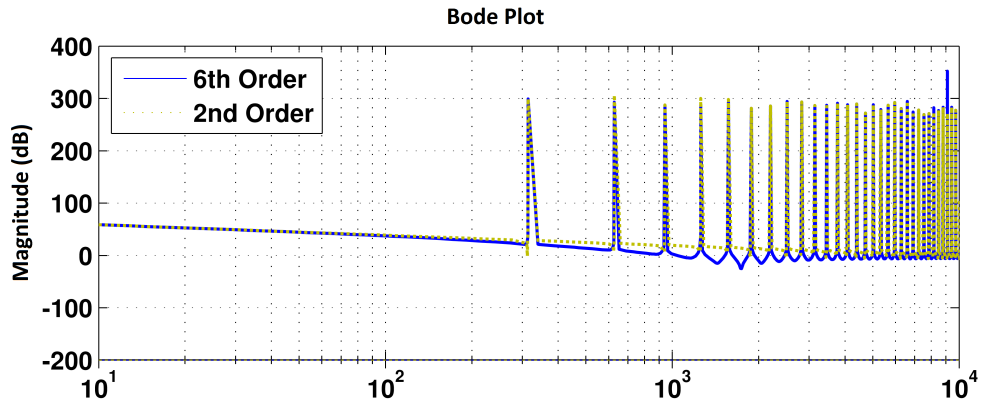
Figure 4.7 – Frequency Response of Voltage RC

The first order low pass filter with corner frequency of 5 KHz is used in time delay loop to implement C_r. The corner frequency is chosen as per bandwidth of feedback of signals i.e. voltage and current. The bode plot of full and approximated voltage controller with unity pre-compensator ($C_2 = 1$) is shown in Figure 4.7. Here, it can be observable that the approximated controller is perfectly matching the characteristics of original controller with minimal error.

4.2.2 Design of Current Controller

The current controller is also designed in similar fashion as the voltage controller one. Here, the plant transfer function is described by series connected filter inductance L_f and resistance R_f. Plant transfer function for current control loop can be written as,

$$P(s) = \frac{1}{L_f s + R_f} \tag{4.2.24}$$

Now, co-prime factors of (4.2.24) is taken as $N(s) = \frac{1/L_f}{s + R_f/L_f}$, and $D(s) = 1$

The value of R(s) as calculated from(4.2.15) is further utilized in (4.2.4) in order to obtain high order controller parameters. Further, reducing the controller order up-to 2nd order with balanced truncation method gives,

$$\widetilde{C_{1C}}(s)^{2nd} = \frac{1.005s^2 + 125.6s + 3925}{s(s + 62.5)} \tag{4.2.25}$$

Frequency response of approximated current controller is shown in Figure 4.8. The value of pre-compensator (C_2) is gain set to unity for simpler configuration. Figure 4.9 shows frequency response of inner current loop with different inverter output impedance. It shows that the loop bandwidth improves when low value of filter inductance is used. Therefore, same controller can perform better when used with high switching frequency that reduces filter inductance requirements. In conventional controllers, the bandwidth is limited by controller, therefore will not perform better with improved hardware configuration.
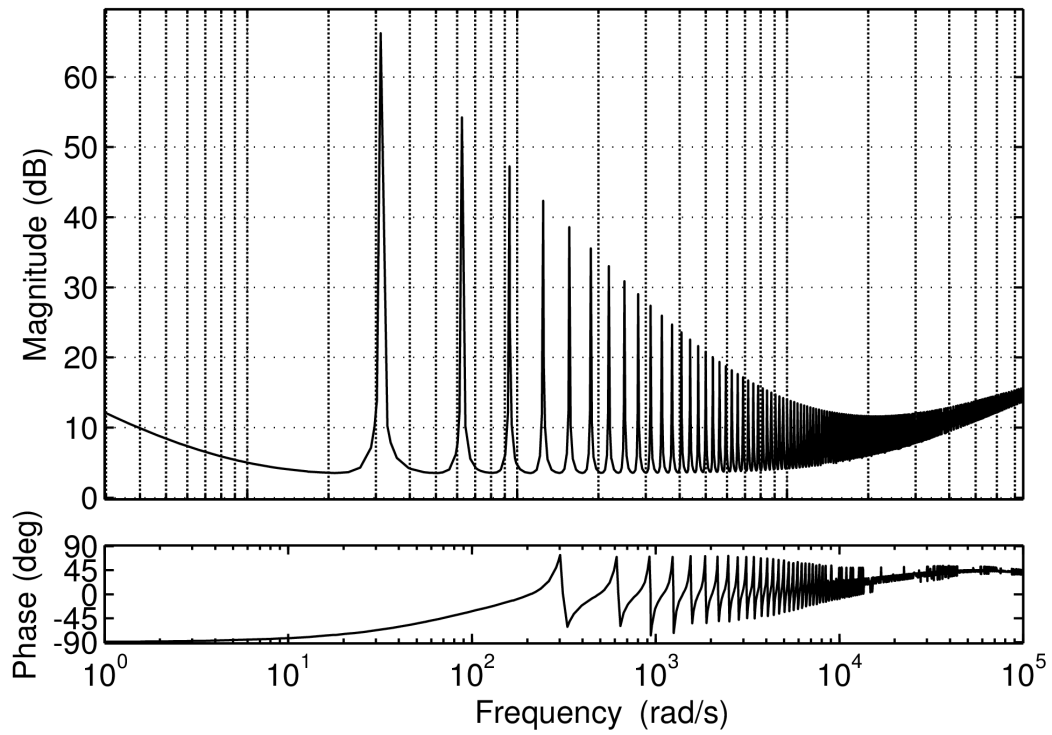
Figure 4.8 – Frequency Response of Currrent RC
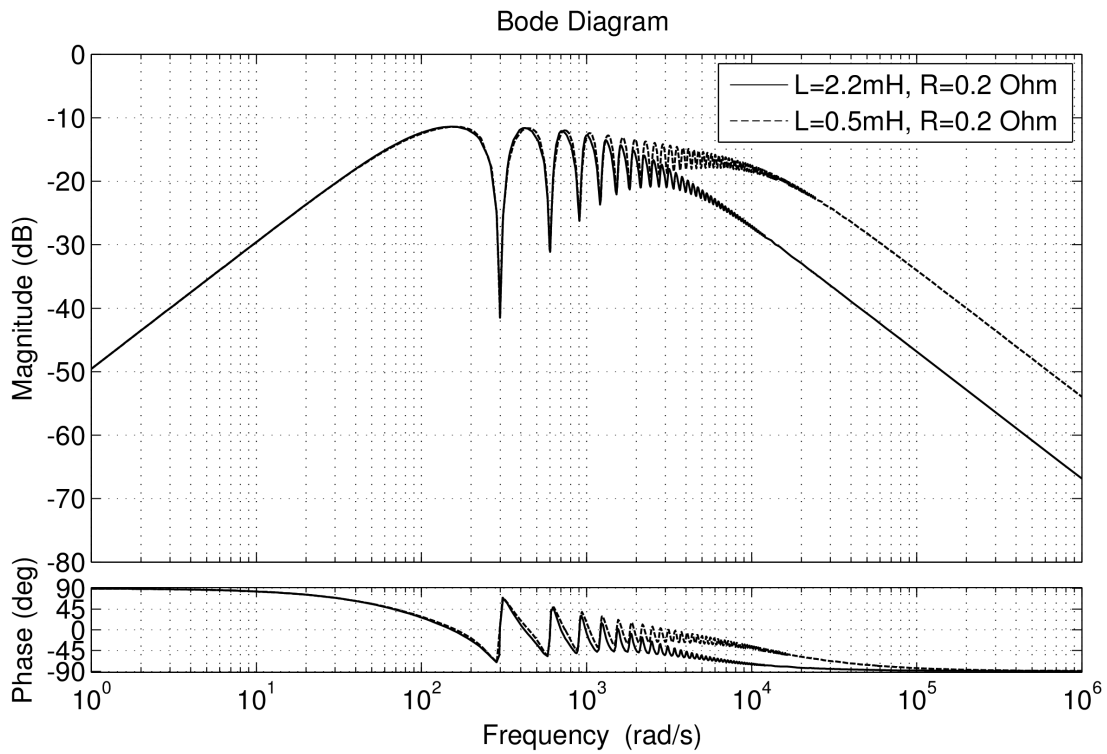
Figure 4.9 – Frequency Response of Current RC with different filter inductance

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4.2.3 Response of Designed Controllers:

Response of designed controller can be verified by simulating their transfer function in close loop of plant transfer function in MATLAB® Simulink as shown in Figure 4.10. A sinusoidal reference signal input is given to closed loop system and harmonic component of output is given as disturbance input to the plant. Reference input and output signal values are collected and plotted in Figure 4.11. It can be easily observed that the error in input signal to output signal is nearly eliminated in few cycles. Harmonic disturbance have negligible impact on output voltage even if its THD is higher than 40% as shown in Figure 4.12.
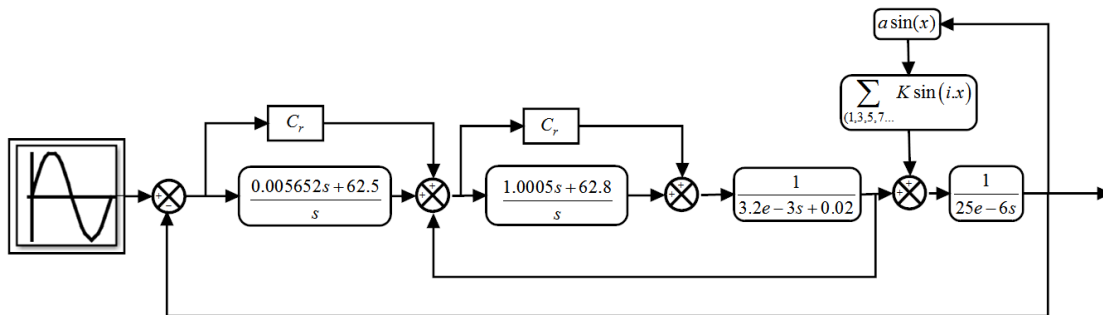
Figure 4.10 – Performance Test Digram of RC
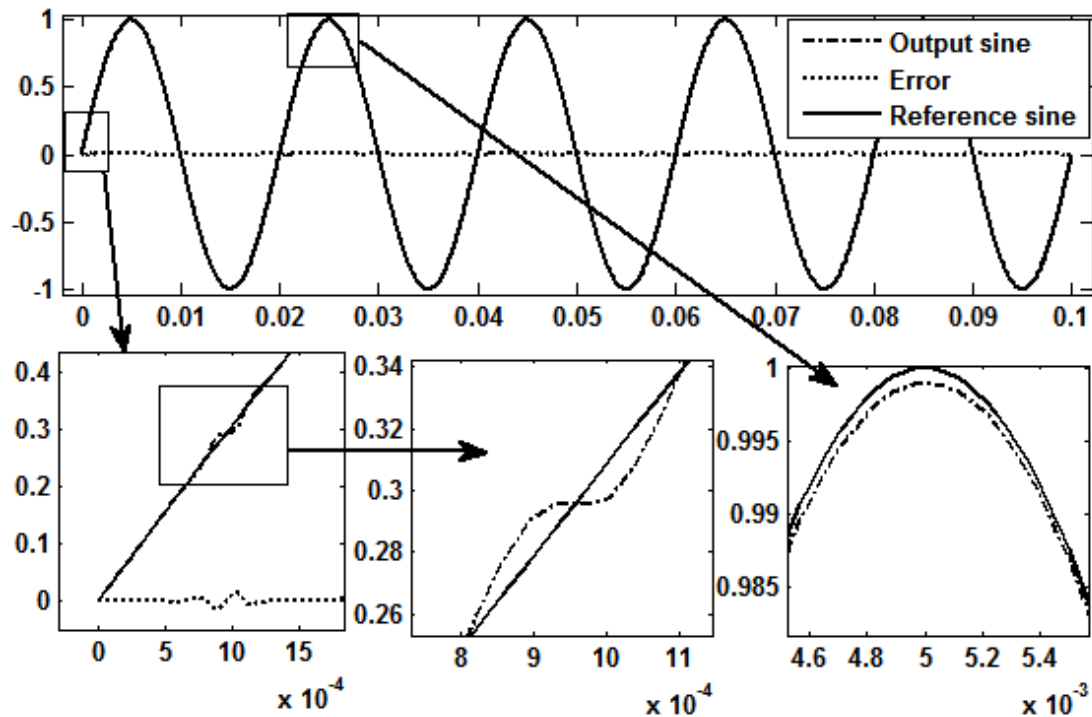
Figure 4.11 – Reference tracking of RC controller with Sin input
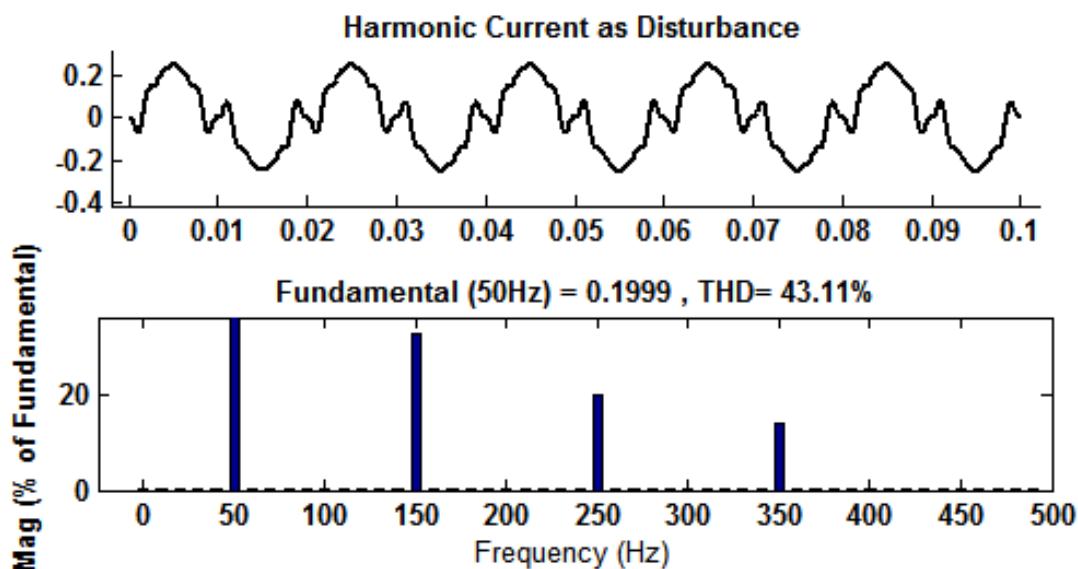
Figure 4.12 – Disturbance input and its THD (Simulating Non-linear Load)

4.3   Implementation in Real Time Hardware

A scaled hardware prototype of microgrid has been developed to test the proposed controller. The prototype consists of two number of three phase VSI having batteries as a constant DC voltage source. Inverters are connected with each other through equivalent network impedance (implemented by inductance). The three phase linear and non-linear loads are connected to common bus via switch. A three phase contactor has been used as C.B. which makes/disconnects the interconnection on low voltage control signal. Each inverter has a LC-filter on its output to filter out PWM carrier frequency and its harmonic component.

The whole control system for both the VSI's is implemented within FPGA (Xilinx-ZYNQ 7000/ZEDBOARD) board as depicted in Figure 4.13. FPGA has various digital I/O port to connect it to external world. All the transfer functions are computed in continuous time domain and discretized by bilinear transformation to make them suitable for real time digital control implementation. Since RC's always have long time delays while implemented for real time control applications and accordingly require large number of logic resource of FPGA. Therefore, in order to have optimal utilizations of logic resources, the delays are generated with dual port RAMs within FPGA. This method reduces the logic count while
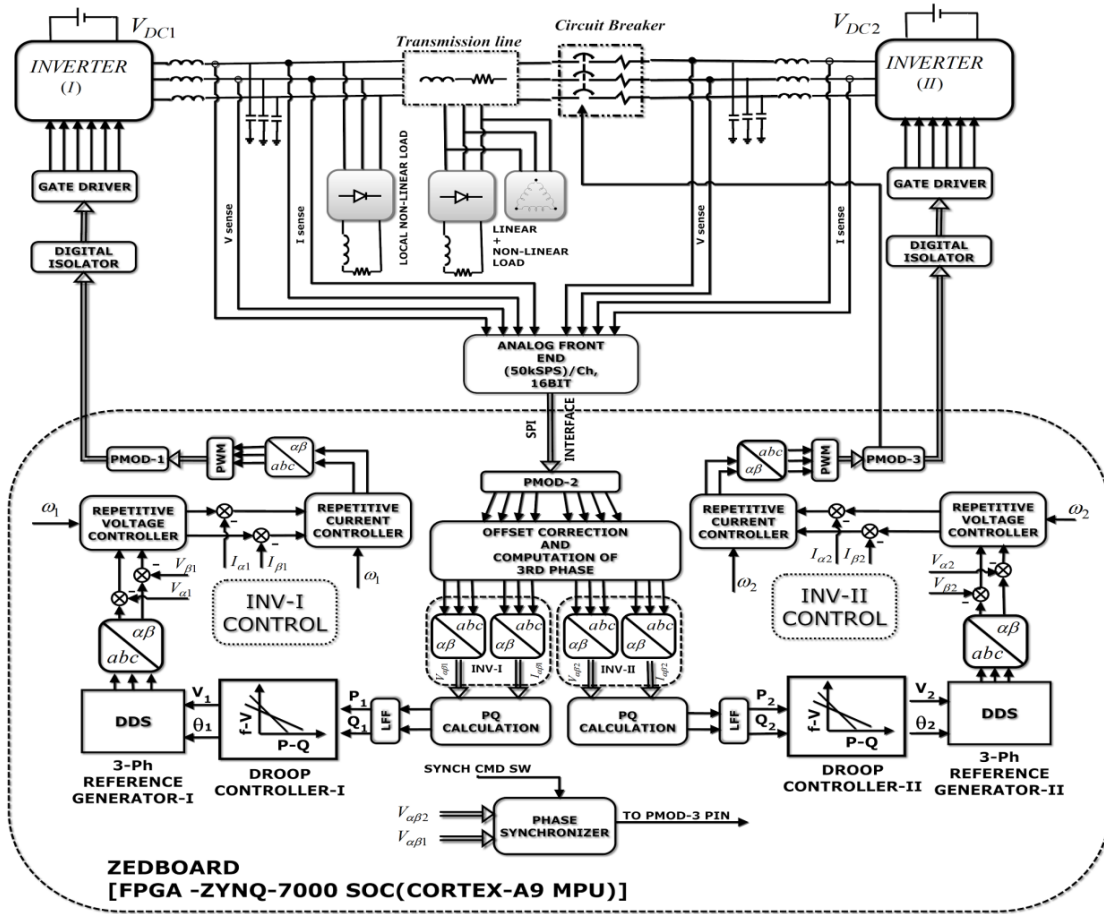
Figure 4.13 – Real Time System Schematic

improving utilization of FPGA.

In addition to this, other resource optimization techniques are also critically required to implement a bigger system within single FPGA chip. Therefore, to reduce logic count for FPGA:

a) All computations are performed in Fixed Point Numbers.

b) Some functions are shared among similar signals using signal multiplexing and overclocking. However, above measures may decrease the control performance and increases complexity of the system in prototyping.

Further, control requires measurment of inductor current and voltage across filter capacitor as a feedback signal. Therefore, Hall effect voltage and current sensors are installed in two phases of each inverter's outputs. The outputs of these sensors are converted into digital signal by analog to digital converter (ADC) which are further communicate to FPGA via digital I/O port. The value of voltage and current of third phase is computed numerically inside the FPGA since it is

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assumed that the system is balanced. Further, all three phase quantities in a stationary reference frame ($\alpha\beta$) using Clarke transformation.

Further, the calculation of inverter's active (P) and reactive powers (Q) are computed using equations (4.3.1)-(4.3.2):

$$P = \frac{\omega_c}{s + \omega_c}(V_\alpha I_\alpha + V_\beta I_\beta) \tag{4.3.1}$$

$$Q = \frac{\omega_c}{s + \omega_c}(V_\alpha I_\beta - V_\beta I_\alpha) \tag{4.3.2}$$

Here, ω_c is power filter cut off frequency in rad / sec.

The calculated values of P and Q is passed to droop controller which gives voltage (V) and rotating phase (ϑ) to generate three phase voltage reference. Three voltage references are then generated by Direct Digital Synthesizer (DDS). DDS is an IP with Xilinx design suite, and used to generate unity sine and cosine signal with FPGA logic.

Reference voltage generated by DDS block is first transformed to ($\alpha\beta$) and subsequently fed to voltage and current RC. The output of RC is transformed back into three phase voltage by Inverse Clarke transformation and fed to the PWM block which generates six gate pulses at output.

For basic comparative study the PI control is implemented in similar fashion except the process of transformation of the quantities which is performed in synchronous reference frame using park transformation (dq) instead ($\alpha\beta$) only. The values of PI gains are calculated with root locus after the plant linearization. The VHDL synthesis shows RC is better suited for FPGA implementation as it better utilize memory than logic slices. This also reduces the logic count as well as other resources in the system . FPGA implementation report has been added in Appendix -C for PI and RC controllers for the reference.

4.4   Simulation and Experimental Results

In this section simulation and experimental studies are presented in two parts. First part shows the performance of proposed RC on the basis of its reference tracking capability under linear and non-linear load condition. A performance

comparison with conventional PI control is also presented. In the second part, performance of the controller is analyzed by connecting both the inverters in parallel under droop control mode to show the stable parallel operation.

4.4.1 Performance of RC with Non-Linear Load:

As already discussed, the RC has an ability to minimize periodic error generated by non-linear load in the form of harmonics. Therefore, to test the tracking performance of RC controller, system is tested in rectified RL load condition. The results are compared with conventional PI controller with same system. At first, model was simulated in MATLAB/ SIMULINK to show the reference tracking capability of inverter. Phase 'A' voltage trajectory for both the controllers have been plotted and it is observed that the RC tracks voltage reference very much precisely in comparison to PI controller. As evident from Figure 4.14 that the PI controller is able to track the voltage reference but unable to avoid the superimposition of harmonics on output voltage. Same time RC controller as shown in Figure 4.15 improve phase 'A' wave shape closely sinusoidal.
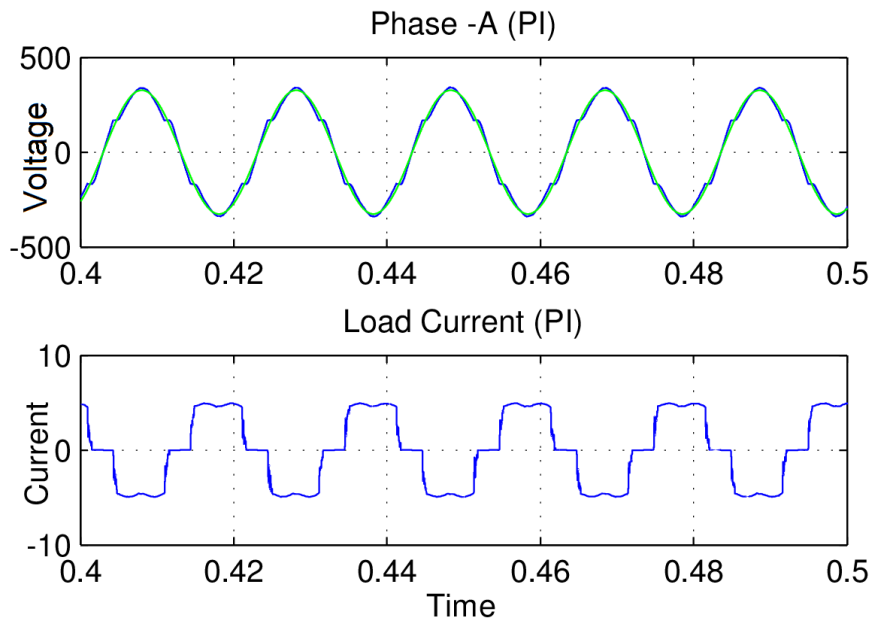
Figure 4.14 – With PI control : Output Voltage, Reference Voltage and load current

The above observations were also verified with scaled down experimental setup. The performance of controller were test-ed with a non-linear load at the output of

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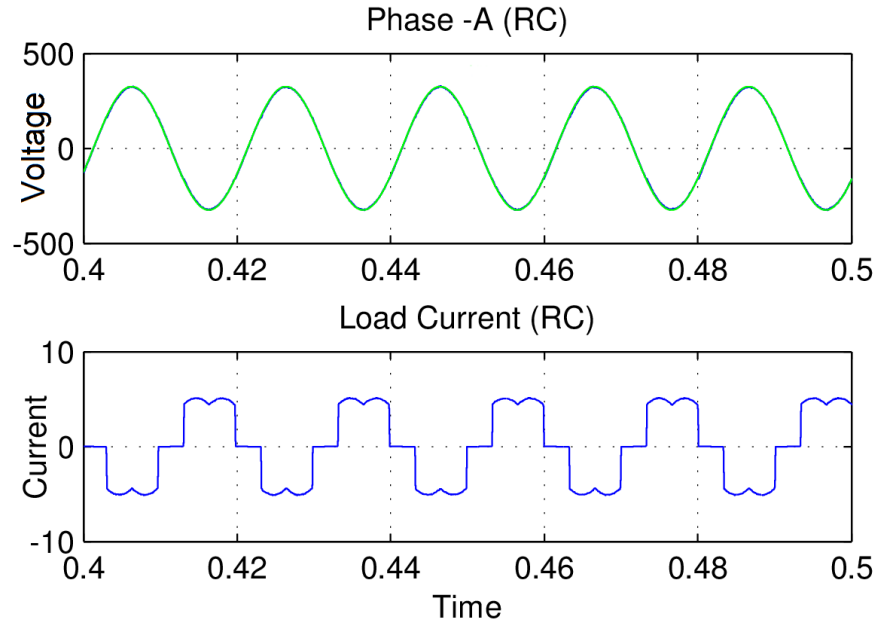
Figure 4.15 – With RC: Output Voltage, Reference Voltage and load current

the VSI, where the non-linear voltage drop across filtering inductance deforms the output voltage waveform in absence of proper control efforts. The performance of perfectly tuned PI controller is shown in Figure 4.16 where the harmonic effect of non-linear current with THD of 29% almost deforms the output voltage with THD of 6.8%. However, this deformation in voltage waveform may be countered by a more capable voltage and current controller. In order to reduce the impact of non-linear load current on output voltage waveform, a RC and current controllers were designed and experimentally validated. The experimental results with RC are shown in Figure 4.17. Here, it can be easily observed that the THD in voltage waveforms are almost negligible (THD = 4.1%) despite of highly non-linear load current with THD of more than 29%.

In Figure 4.18 & Figure 4.19, the dynamic performance with step increase in a non-linear load is demonstrated and compared with PI. Here, it is pertinent to mention here that the PI regulator shows satisfactory performance under linear load. However, the voltage waveforms deteriorate as soon as the non-linear load is introduced as shown in Figure 4.18. Further the voltage profile keep on deteriorating with the increase in non-linear load current.

In Figure 4.19, the voltage and current profiles with RC are shown. Here, it is
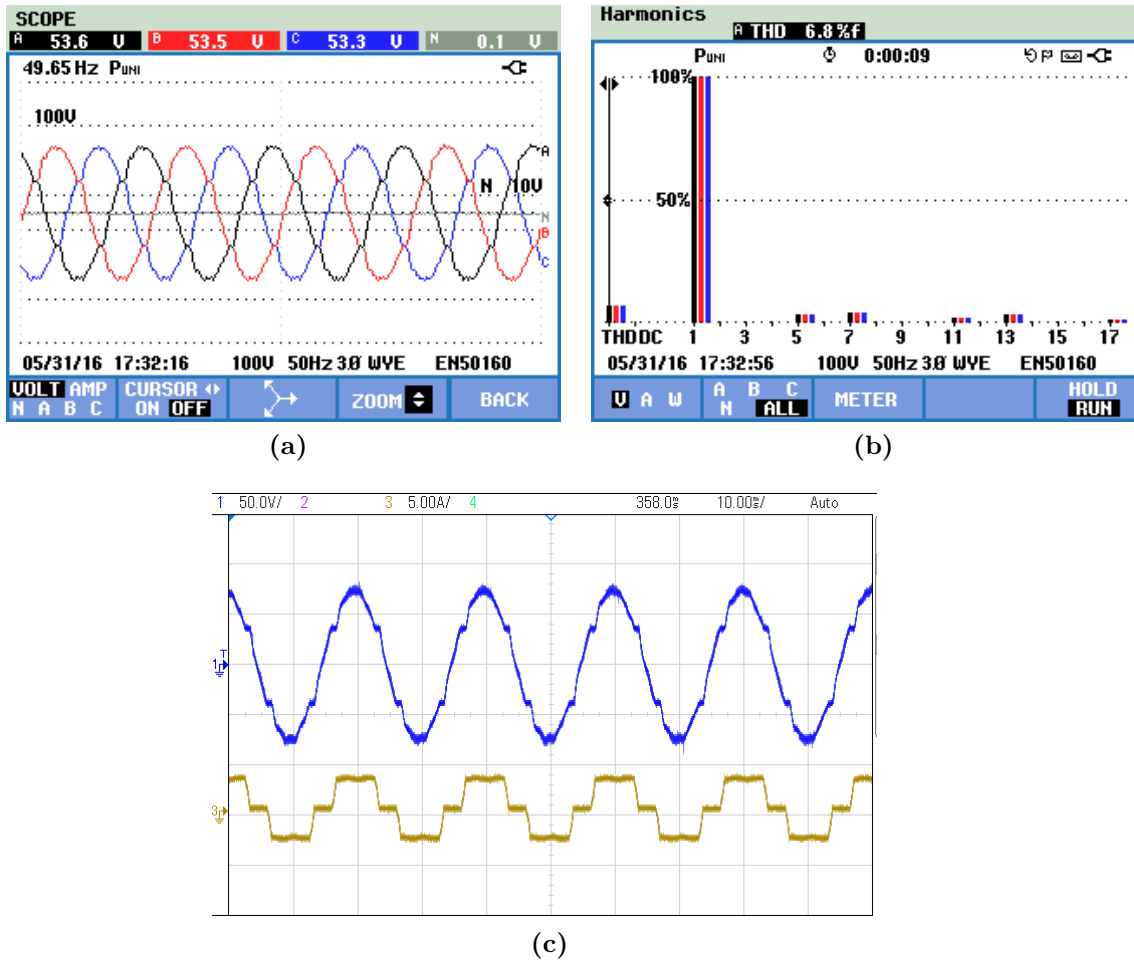
Figure 4.16 – (a) 3-Phase voltage waveform with PI control (b) Harmonics profile of voltage (6.8% THD) (c) Voltage and Non-linear load current profile

shown that the RC is able to handle the dynamic changes in load current without any significant change in output voltage waveform. Moreover, the increase in THD level of load current has very negligible effect on output voltage profile where the THD's of voltage are kept within prescribed limit of 5% of LV system as per IEEE Std. 519.

In Figure 4.20, the effect of increase in nonlinear load current on voltage waveform has been shown. Here, it can be seen that there is abrupt rise in voltage THD level with increase in non-linear loading. However, the percentage change in THD of voltage w.r.t. percentage change in non-linear load current is very low in case of RC based control strategy.
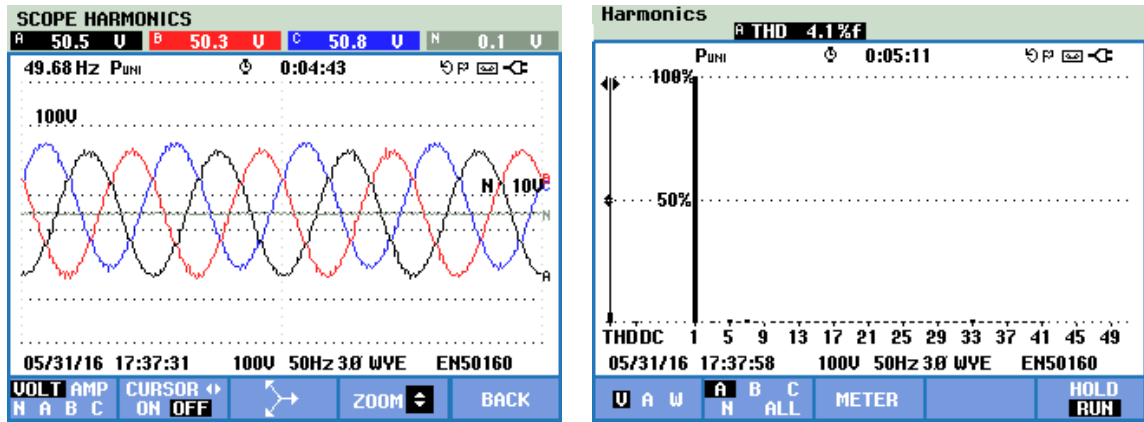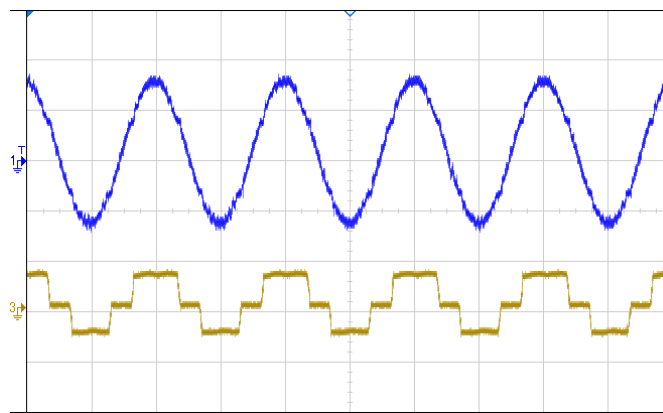
Figure 4.17 – (a) Voltage waveform with RC control (b) Harmonics profile of voltage (4.1% THD) (c) Voltage and Non-linear load current

4.4.2 Performance of RC in power sharing

In droop based microgrid, voltage and current loop must show stability during parallel operation and maintain synchronism with remaining system. Therefore, RC was tested for parallel operation, where INV-II brought to synchronism by phase synchronizer with INV-I and then interconnected by circuit breaker immediately. The sharing of power is in accordance with their droop coefficient as frequency droop is equal for both the inverters. When an additional load (nonlinear in nature) was added to the system, both the inverters increased their power in proportional manner and dropped their frequency and voltage according to their droop coefficients. Initially, only INV-I is connected to a resistive load which is far from inverter and INV-II is running separately at no load. When both the inverters are connected, under droop control active power of INV-I decreased to
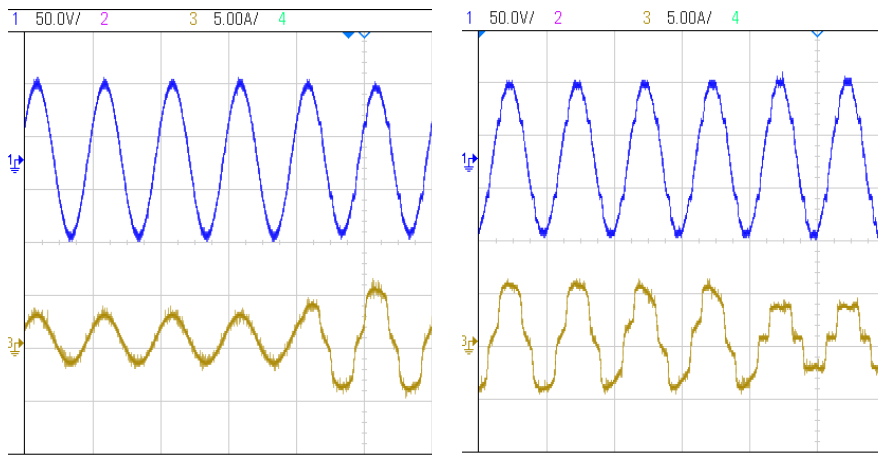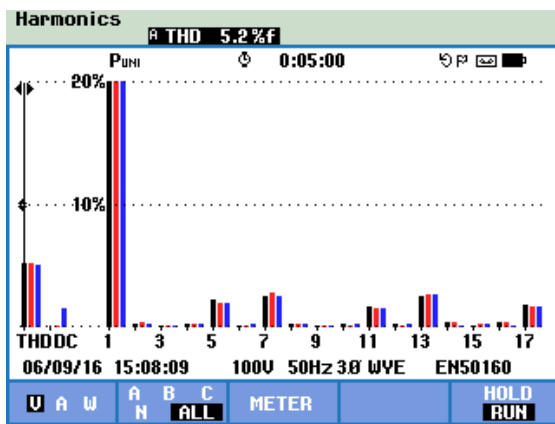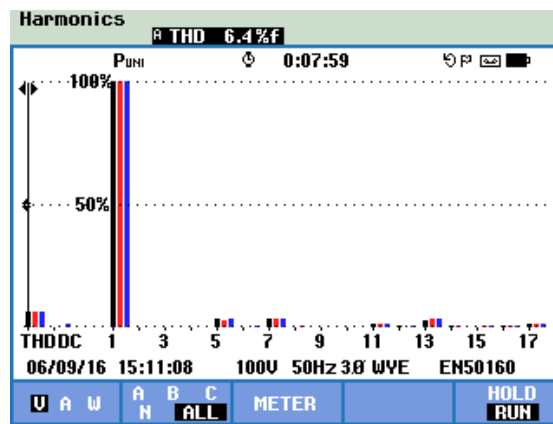
Figure 4.18 – a) Voltage and current under different load condition with PI (b) Harmonic profile of voltage under linear plus non-linear loading(c) Harmonic profile of voltage under non-linear loading

half of its value while remaining half is shared by INV-II as dipicted in Figure 4.21. There is small mismatch in reactive power sharing which occurs probably due to difference between voltage magnitudes of the inverters at the time of interconnection. This effect can be verified in output voltage (RMS) of inverters Figure 4.22. Although, the load is connected far (as per network impedance) from inverter's terminal, the harmonics in inverter's output voltage show a slight improvement with RC 4.23.

4.5 Conclusion

This chapter shows a new simpler RC design methodology for VSI in droop based microgrid. The simulation study as well as experimental validation has been
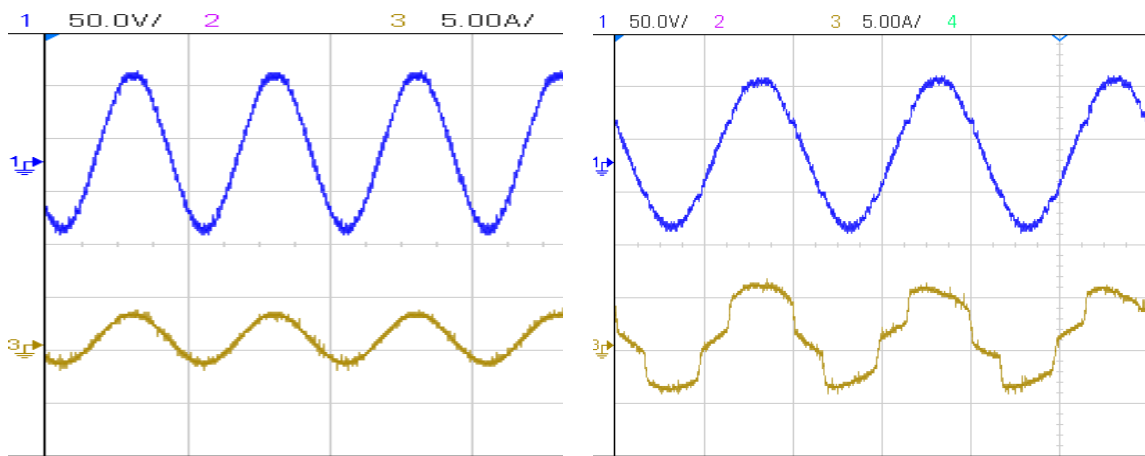
(a)
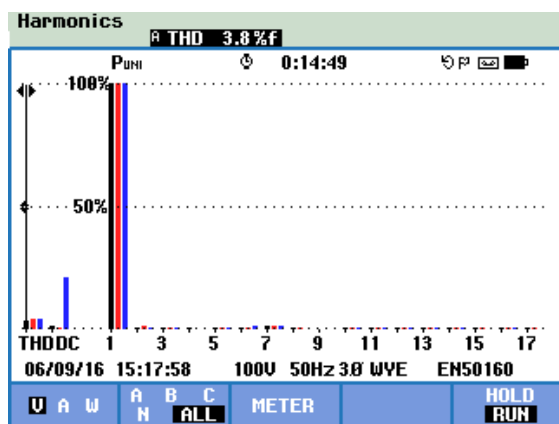
(b)
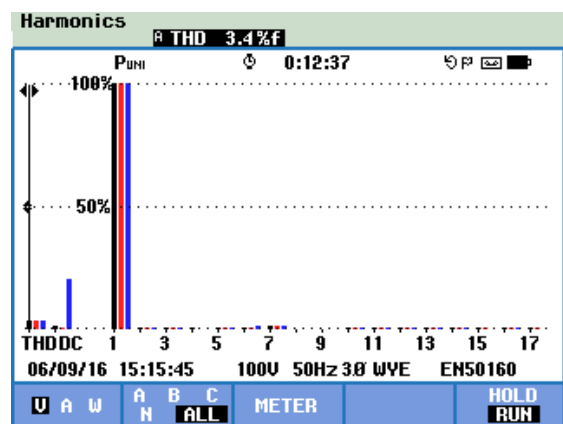
(c)

Figure 4.19 – (a) Voltage and current under different load condition with RC (b) Harmonic profile of voltage under linear plus non-linear loading (c) Harmonic profile of voltage under non-linear loading
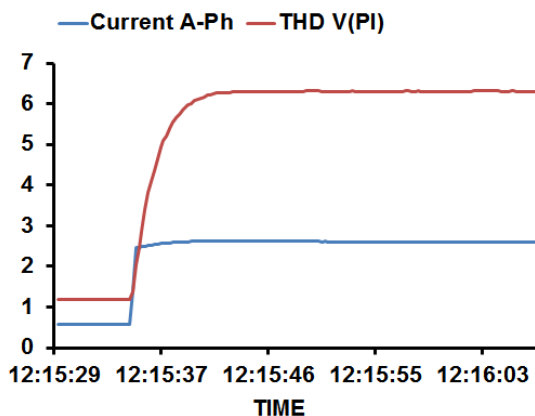
(a) PI control
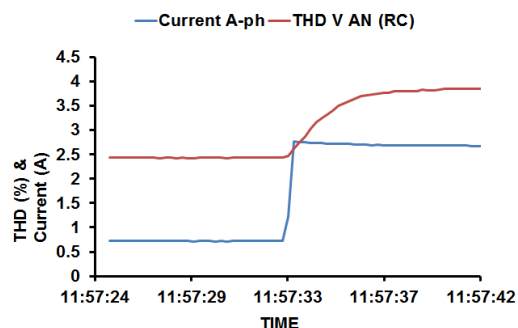
(b) Repetitive Control

Figure 4.20 – THD comparison with Load Current

presented. It has been demonstrated that proposed RC based control strategy shows good performance under steady state and dynamic conditions in comparison
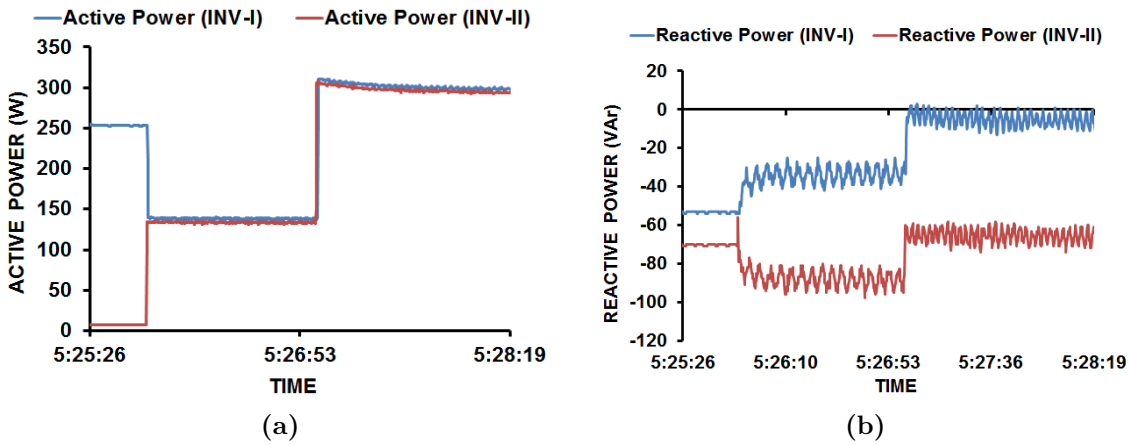
Figure 4.21 – (a) Frequency and (b) Voltage of both inverters
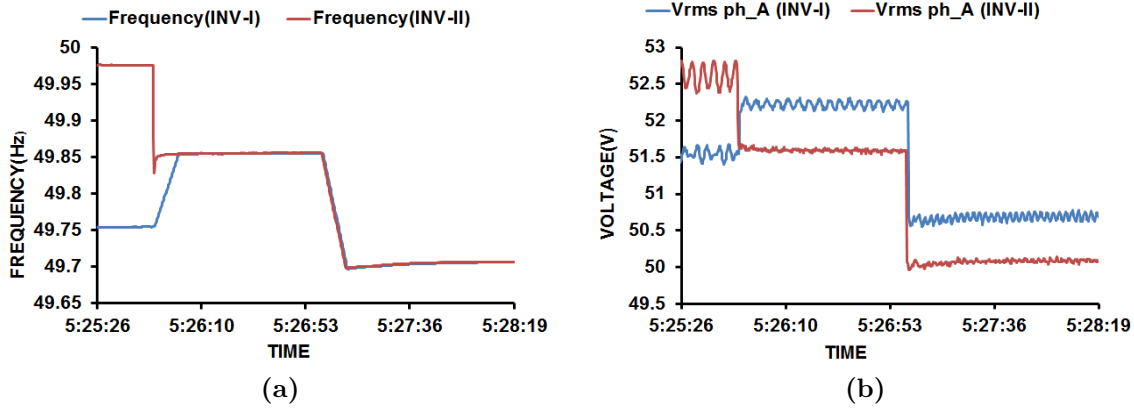
Figure 4.22 – (a) Frequency and (b) Voltage of both inverters

(a) PI control

(b) Repetitive control
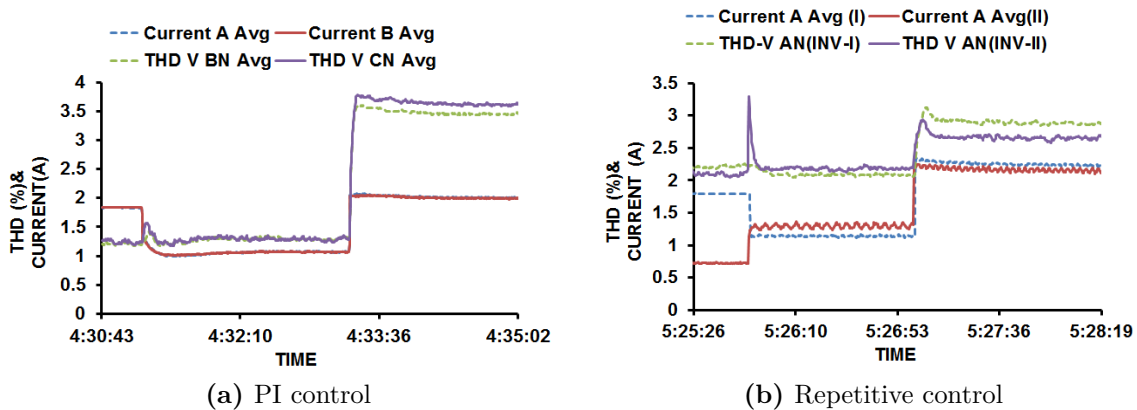
Figure 4.23 – THD vs Load Current diagram during parallel operation of both the inverters

to conventional PI controller. The experimental results for parallel operation of two VSI's in microgrid have been presented where both the inverters are able to handle the linear as well as non-linear varying load demand seamlessly. It is also

shown that the RC has very good control in rejecting the harmonic component on voltage waveform in comparison to its PI counterpart under highly non-linear load conditions.

REPETITIVE ADD-ON CONTROLLER FOR UNBALANCE COMPENSATION IN MICROGRID

AC-Microgrid may be loaded in the same way as the main grid. It may consist of several single phase, three phase and non-linear loads. These types of loads may create severe power quality issues in MG like phase unbalance and voltage harmonics. In presence of any non-linear load, power sharing among different sources may not be appropriate. A VSI having the ability of compensating load harmonics and load unbalance among many interconnected inverters may get overloaded as there may be chances that the rest of inverters connected in MG may also act as nonlinear unbalance load [119][120].

Various control methods have been implemented to mitigate voltage unbalance and harmonics issues in MG. Mostly, voltage unbalance is compensated by feeding negative sequence voltage at point of common coupling (PCC) [121][122]. An additional inverter is used to supply only negative sequence voltage component to mitigate voltage unbalance [123] [124]. However, this compensator increases the component count in MG and may also interfere with normal working of other inverters.

Few methods based on selective virtual impedance loop for positive and negative sequence component have also been reported [125][126]. However, generating reference for harmonics and unbalance components is very complex [127][128]. Based repetitive control has been used to eliminate the harmonics for both grid connected and islanded mode. Being frequency adaptive it ensures stable gain at frequency measured by PLL [129].

In this chapter, RC based add on controller is designed that may be easily

connected in parallel with existing PI controller for unbalance and harmonics compensation. This enables the efficient use of available software resources.

5.1 Voltage Unbalance and Harmonics

Precisely speaking, voltage unbalance is defined as ratio of negative sequence voltage to positive sequence voltage [130][131].The non-linear load connected in system may also introduce distortion in voltage waveform which is generally measured in terms of Total Harmonic Distortion (THD) [132]. While connected on grid it is very difficult to calculate how much effort a controller is making or how much harmonics are being generated or compensated by a source. However, controlling the bandwidth of controller within source's dynamic capabilities, the compensation effort made by individual inverter can be determined.

In synchronous reference frame, the negative sequence component rotates at twice of fundamental frequency $(2f_0)$ with respect to positive sequence component [133][134, 135]. Let, V_1 and V_2 are positive and negative sequence voltages. Then, three phase voltages with harmonic components can be represented as,

$$V_{a12} = V_{m12}\sin(\omega t + \phi) + \sum_{h=3,5,7..} V_{h12}\sin(h\omega t + h\phi) \qquad (5.1.1)$$

$$V_{b12} = V_{m12}\sin(\omega t \mp {}^{2\pi}\!/_3 + \phi) + \sum_{h=3,5,7..} V_{h12}\sin(h\omega t \mp {}^{2h\pi}\!/_3 + h\phi) \qquad (5.1.2)$$

$$V_{c12} = V_{m12}\sin(\omega t \pm {}^{2\pi}\!/_3 + \phi) + \sum_{h=3,5,7..} V_{h12}\sin(h\omega t \pm {}^{2h\pi}\!/_3 + h\phi) \qquad (5.1.3)$$

From above equations, it can be easily observed that the triplen harmonics produce zero sequence $\left({}^{2h\pi}\!/_3 = 0\big|_{h=3,9}\right), (6n-1)\big|_{n=1,2,3..}$ harmonics produce negative sequence $\left(\pm {}^{2(6n-1)\pi}\!/_3 = \mp {}^{2\pi}\!/_3\right)$ and $(6n+1)\big|_{n=1,2,3..}$ produces positive sequence $\left(\pm {}^{2(6n+1)\pi}\!/_3 = \pm {}^{2\pi}\!/_3\right)$ voltages separately.

Performing DQ transformation with respect to the positive sequence component on above voltage equations, where the positive sequence voltage component will rotate at zero frequency ($f - f_+ = 0$) while negative fundamental component

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rotate at double ($f + f_+ = 2f_-$) frequency. Similarly, each positive sequence harmonic voltage components will rotate at frequency of $6nf_+$ w.r.t. positive fundamental, while at the same time negative sequence harmonic voltages will rotate at frequency of $6nf_-$.

5.2   Repetitive Controller for Unbalance and Harmonics

A Repetitive controller can be used to mitigate the effect of unbalance current drawn by unbalance loading. This controller can be implemented adjacent to inner voltage control loop in droop controlled inverter.

5.2.1   Design of controller:

The inner control loops are designed in synchronous reference frame (SRF) [155-158]. Therefore, all the quantities are first converted into DC by using park transformation (dq). The loop transfer function can be derived from following differential equations,

$$\frac{di_d}{dt} = -\frac{r}{L}i_d - \omega i_q + \frac{1}{L}V_d^* - \frac{1}{L}V_d \tag{5.2.1}$$

$$\frac{di_q}{dt} = -\frac{r}{L}i_q + \omega i_d + \frac{1}{L}V_q^* - \frac{1}{L}V_q \tag{5.2.2}$$

$$\frac{dV_d}{dt} = \frac{1}{C}i_d + \omega V_q \tag{5.2.3}$$

$$\frac{dV_q}{dt} = \frac{1}{L}i_q - \omega V_d \tag{5.2.4}$$

Where r, L and C are ESR of filter inductor, filter inductance and filter capacitance.

From equations (5.2.1) to (5.2.4), it is clear that there are some frequency dependent terms (ωI_{dq}), which have to concidered in decoupled control. The simplified current and voltage control loops ignoring coupling effect is shown in Figure 5.1, where the transfer function of current and voltage loop is::
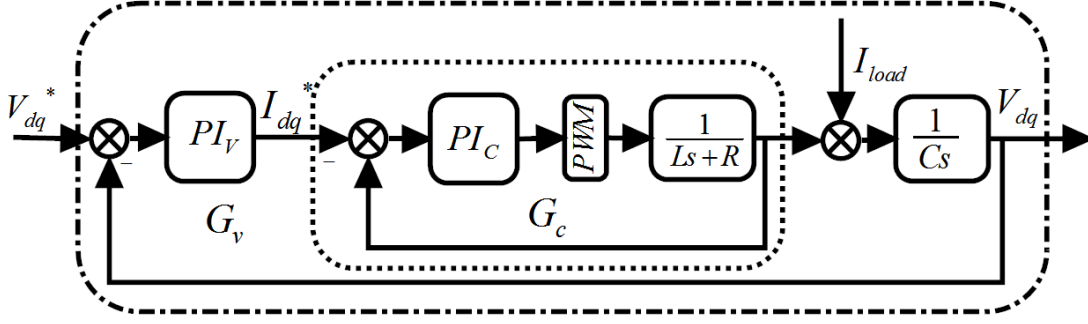
Figure 5.1 – Voltage current control loop
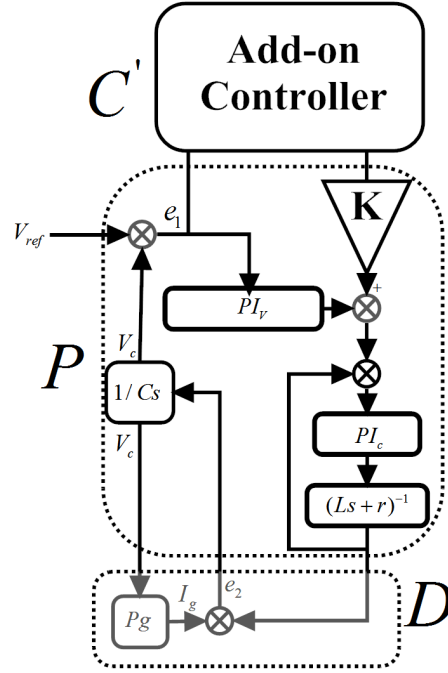
Figure 5.2 – System with Add-on Controller

$$G_c(s) = \frac{PI_c(s) \times G_{pwm}(s) \times (Ls+r)^{-1}}{1 + PI_c(s) \times G_{pwm}(s) \times (Ls+r)} \qquad (5.2.5)$$

$$G_v(s) = \frac{PI_v(s) \times G_c(s) \times (Cs)^{-1}}{1 + PI_v(s) \times G_c(s) \times (Cs)^{-1}}\Bigg|_{I_L=0} \qquad (5.2.6)$$

Here, PI_c and PI_v are proportional and integral controller for current and voltage control loops respectively. The transfer function of PWM generator with saw tooth carrier can be given by $G_{pwm} = 1/(1 + 0.5T_s)$ using first order approximation.

According to [137,133], add-on RC as shown in Figure 5.2 can take following form,

$$C(s) = PI_v(s) + C_2(s).C_r(s) \tag{5.2.7}$$

Where, $C_r(s)$ is internal model for periodic reference input, $C_2(s)$ is precompensator. Here, $C_r(s)$ is represented by feedback time delay (τ , period equals to $1/2f_0$) system with low pass filter $q(s)$.

$$C_r(s) = \frac{1}{1 - q(s)e^{-\tau s}} \tag{5.2.8}$$

PI regulator must be an internally stabilizing controller (C_i) for plant P, i.e., all the transfer function from e to u are strictly Hurwitz.

$$\underbrace{\begin{bmatrix} e_1 \\ e_2 \end{bmatrix}}_{e} = \begin{bmatrix} \frac{1}{1+PC_i} & \frac{-P}{1+PC_i} \\ \frac{C}{1+PC_i} & \frac{1}{1+PC_i} \end{bmatrix} \underbrace{\begin{bmatrix} V_{ref} \\ I_g \end{bmatrix}}_{u} \tag{5.2.9}$$
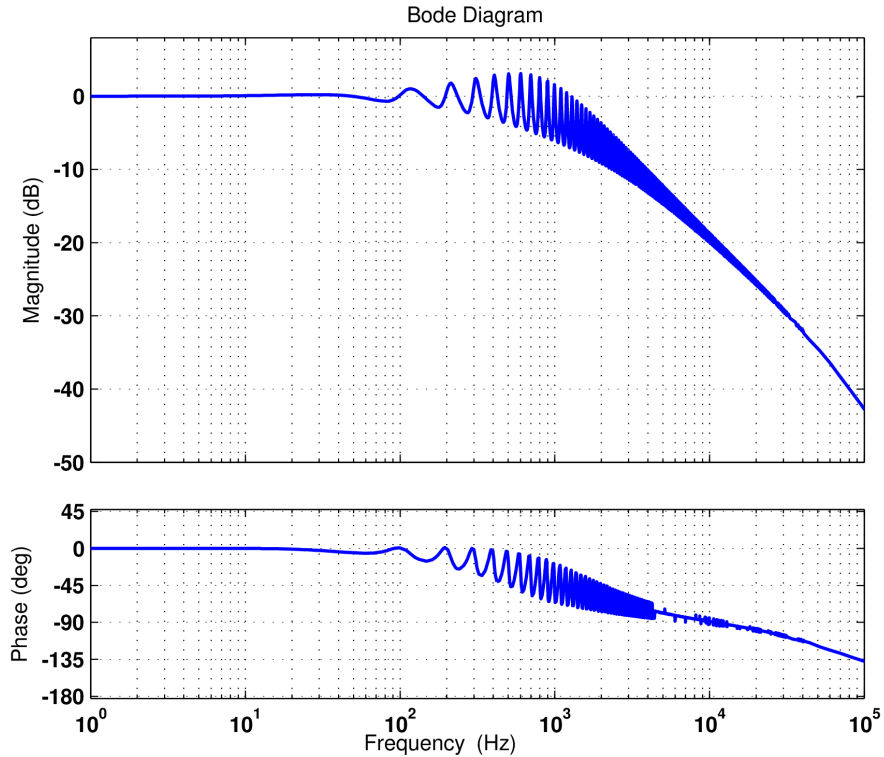
Figure 5.3 – System response with modified RC

Most of the RC's may be designed with assumption of $C_2(s) = 1$ for all frequencies only when internally stabilizing controller ensures adequate stability margin as shown in Figure 5.3. However, stability margin will be compromised using add

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on RC with pre-tuned PI regulator. The closed loop poles with add-on RC tends to give lower phase margin nearby some higher harmonic frequency which must be improved by introducing a pre-compensator $C_2(s)$.

For a given plant P, the pre-compensator can be of any form i.e. lead or leg compensator:

$$C_2(s) = \frac{1 + aTs}{1 + Ts} \tag{5.2.10}$$
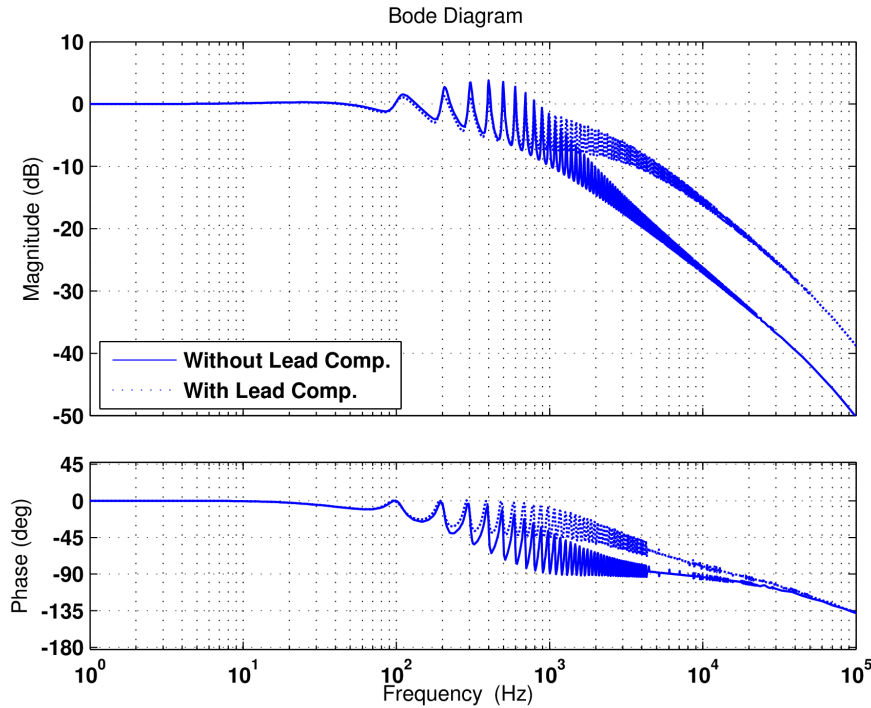
Figure 5.4 – Effect of Lead Compensator

The values of a and T in compensator are selected to manage appropriate phase margin within the bandwidth of controller. Figure 5.4 shows the effect of Compensator $C_2(s)$ with add-on controller giving higher phase margin throughout the bandwidth. The pre-compensator is calculated using closed loop response of system. An appropriate phase margin can be placed either using lead or leg compensator. However computation leads to multiple value of phase margin at different frequencies. Therefore, minimum value of margin should be considered. Hence,

$$PM(sys) = \left.\frac{G_v^*(s)G_c(s)}{1 + G_v^*(s)G_c(s)}\right|_{\phi_m min \forall \omega} \tag{5.2.11}$$

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where,

$$G_v^*(s) = PI_v(s) + C_2(s)C_r(s)$$

As per parameters given in Table-A.1 (Appendix-A), we get minimum phase margin of 38° when $C_2(s) = 1$. However with the suitable choice of lead compensator, the minimum phase margin is increased to 56.77° which will provides better stability.
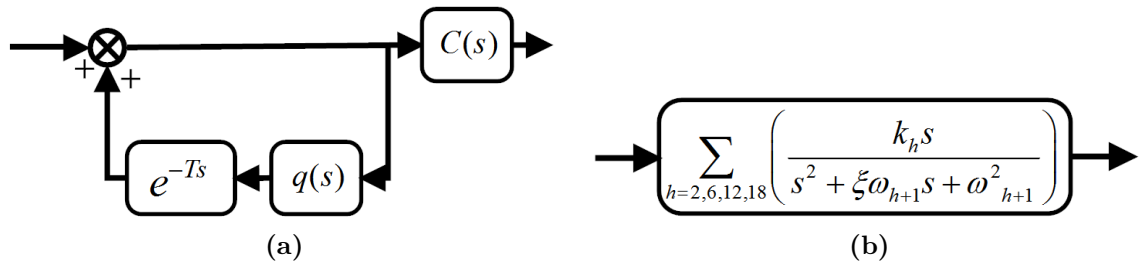
Figure 5.5 – Add-on multi Resonant Controller
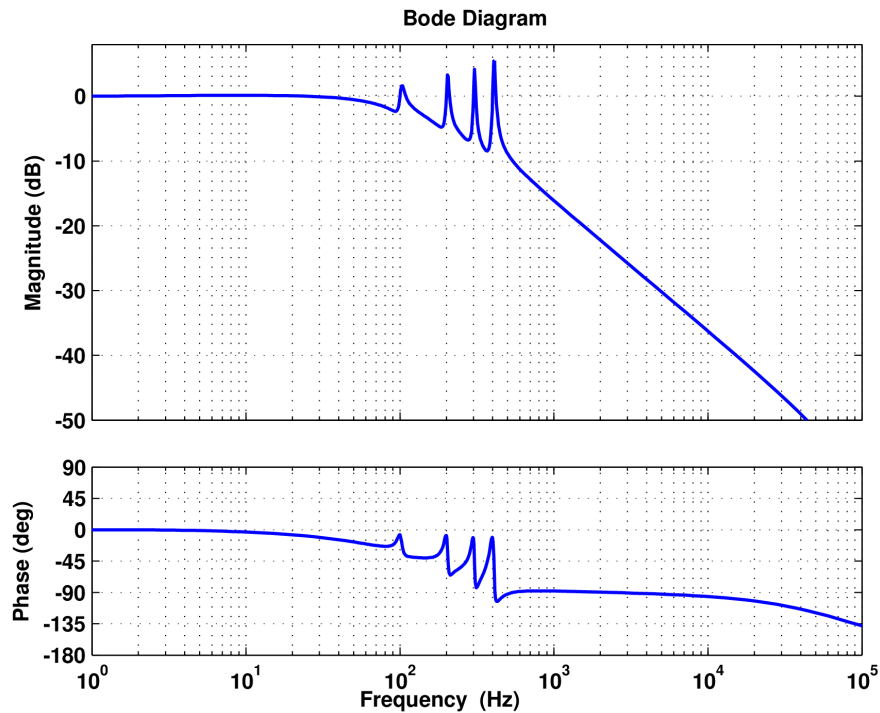
Figure 5.6 – System response with add-on SOGI Resonant controller

The similar add-on controller may also be designed using SOGI loop as shown in Figure 5.5(b). It is also popularly known as multi resonant controller. However, multi resonant controller design is harmonic specific and multi-control loops

corresponding to each harmonic component needs to be added in overall control design. The design of add-on controller having multi control loops itself has lot of inherent complexities related to gain determination. Moreover, add-on resonant controller may be tuned for a given set of harmonics spectrum and may not give satisfactory performance in case of variation in harmonic spectrum, which is line dependent. Further, designing an add-on resonant controller for multiple harmonic frequencies require lot of computational resources which increases the overall cost of hardware. Many authors have presented add-on resonant control loop to damp out harmonic frequency [158][174]. A typical multi resonant controller for 2nd, 6th, 12th, and 18th harmonic components is designed and its frequency response is shown in Figure 5.6.
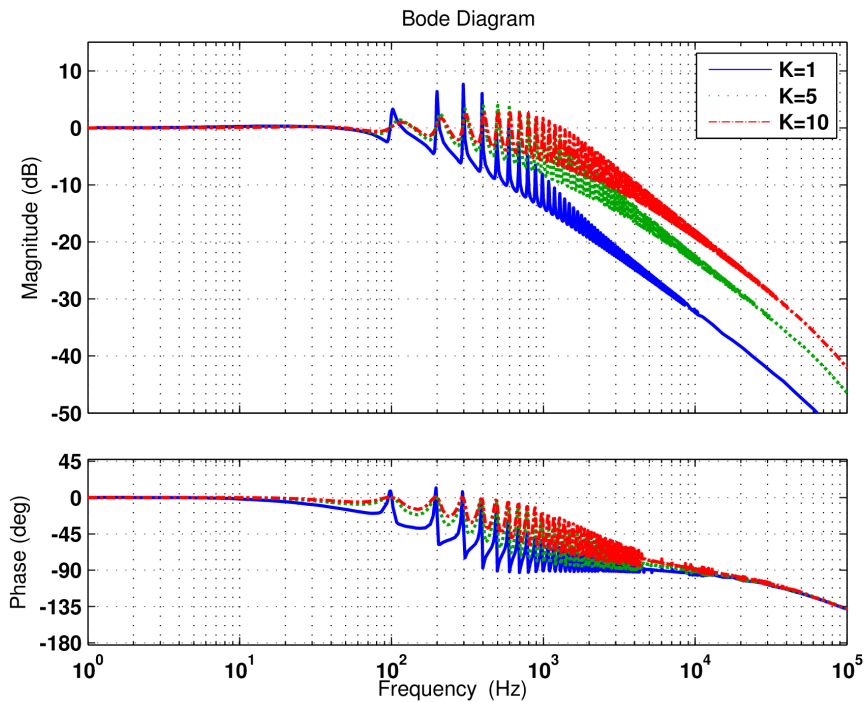
Figure 5.7 – System response with different value of K

Here, it can be easily noticed that the phase margin for each resonant loop has different value, which indicates that the control loop gain for each resonant frequency must be managed separately in order to achieve desired level of stability and performance.

5.2.2 Proportional gain for effort sharing:

A gain K along with RC controller is introduced in the modified controller to have effort sharing in terms of voltage unbalance, harmonics and reactive power to be supplied by the individual inverter connected in a MG.It is clear from Figure 5.2 that add-on RC can be removed from the system by just setting its gain, K to zero. The maximum effort that controller will produce, can be enhanced by increasing the gain K until system remains within stability limit. Therefore, the value of maximum gain K is calculated by small signal stability analysis of system with suitable stability margin. In Figure 5.7, frequency response of system with different values of gain K has been plotted. With increase in gain K the bandwidth of controller also increases proportionally.

5.2.3 RC Implementation in FPGA:
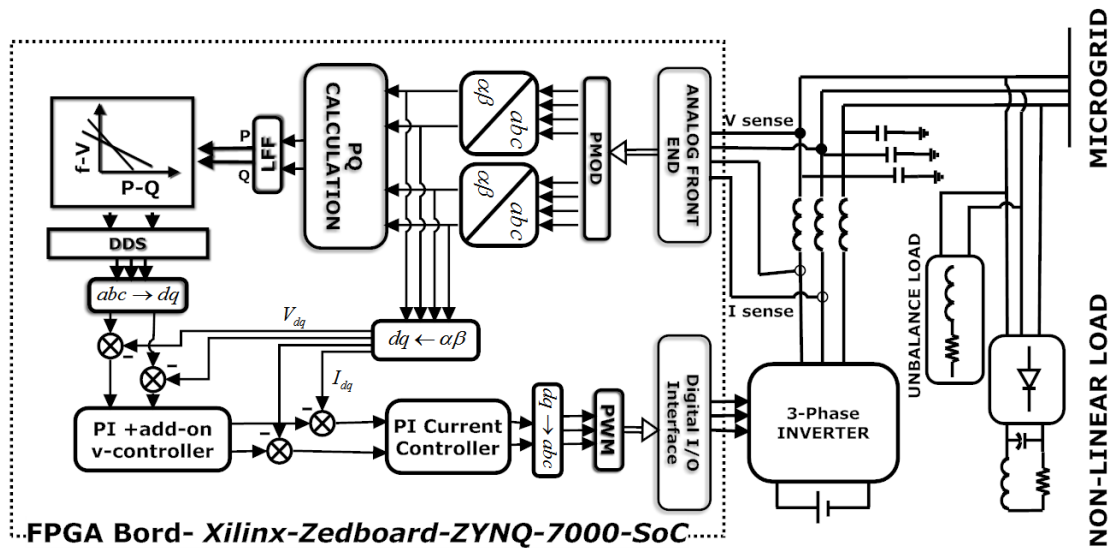
Figure 5.8 – System diagram

The core of Repetitive controller is combination of filters and long variable delay line. A delay generally formed by flip-flop inside FPGA. All filters with unit delay tapped line can be designed in this conventional way. Each CLG/Slice of FPGA contain minimum one memory block formed by flip flop of fixed width (8 bit/16 bit). Whenever, we configure a delay in HDL code where it is synthesized into Flip-flops in most of the case. Flip-flops are one of the important resources of CLG/Slice and are very limited. A repetitive controller requires a delay of

minimum a cycle of fundamental of power frequency. It means it requires delay of 20ms for 50 Hz frequency. For a sampling frequency of 200 KHz we need to have 4000 delay in a line and hence, cannot be implemented conventionally using flip-flops. Therefore, a long variable delay is implemented by using dual port ram. As indicated by the name, it has two ports and can have push and pop operation in various ways. There are two free running counters initialized at different value having difference equal to number of sample required to delay. By this way transfer function with delay T can be implemented (see Chapter-7).

5.3   Experimental and Simulation Results

The hardware prototype of proposed system is developed in laboratory using 2-level 3-phase inverter. Controller for overall system has been implemented using FPGA as shown in Figure 5.8. For optimized performance of FPGA core, whole computational work has been performed in fixed point numbers and other optimization discussed in Chapter-7.
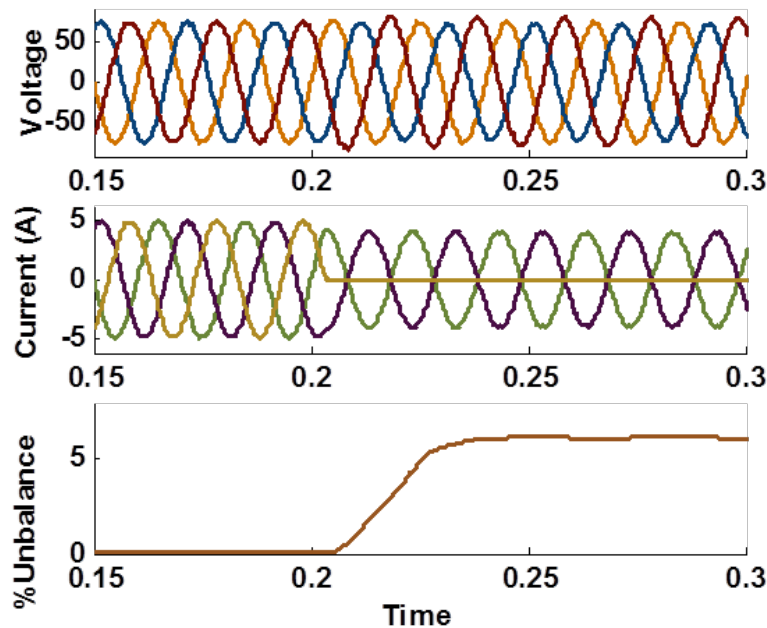
Figure 5.9 – Output Voltage without add-on RC controller (Simulation)

5.3.1 Performance of controller:

The performance of proposed controller has been tested by creating load unbalance at the output of the inverter by disconnecting one of the phases of three phase star connected load. In Figure 5.9 & Figure 5.10 it is shown that the load is perfectly balanced initially and at 0.2 sec, one of the phase is disconnected from circuit to make load unbalance. Since, the system is being controlled by PI controller only, the effect of unbalance load also appears in voltage waveform as evident from the trace of voltage unbalance factor (VUF) which go as high as 7.6% (>7%). At 0.3 sec., add-on RC controller is introduced in voltage control loop. Just after the introduction of add-on RC controller, the VUF start reducing and becomes almost <2% as shown in Figure 5.10.
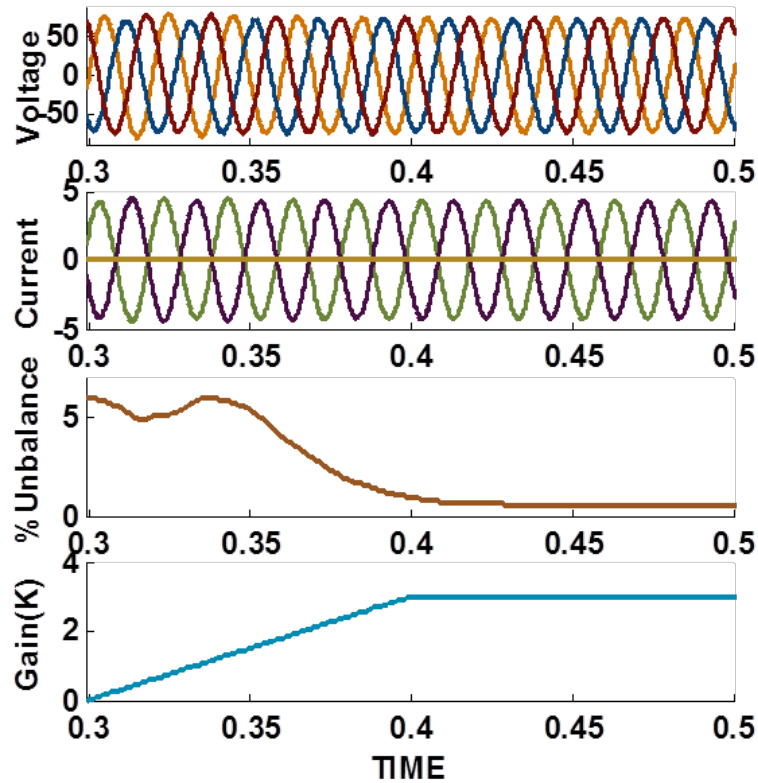
Figure 5.10 – Unbalance mitigation with varying K (Simulation)

Figure 5.10 also shows that unbalance can be mitigated gradually by increasing the value of gain K. The higher value of unbalance cannot be reduced to zero at certain value of K. This is due to the physical bandwidth limitation caused by of inverter's LC-filter, which is difficult to be overcome by the controller. The value

of K can be changed according to required compensation effort. Decreasing the value of gain K according to negative sequence power after computing negative and positive sequence powers separately can ensure a proper effort sharing between the inverters.
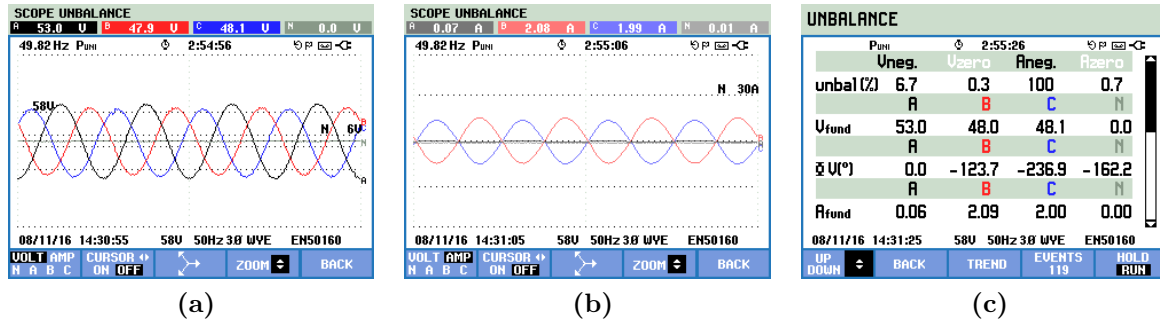
Figure 5.11 – (a) Output Voltage, (b) Load Current (c) Unbalance without add-on controller
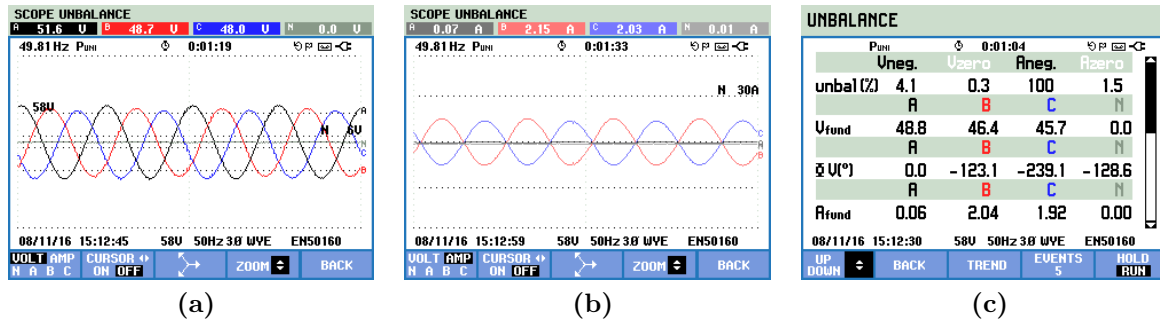
Figure 5.12 – (a) Output Voltage, (b) Load Current (c) Unbalance with add-on resonant controller

The experimental results are shown in Figure 5.11 to Figure 5.13, for unbalance load with PI, add-on resonant controller and add-on RC Controller, respectively. On analysing these results, it is found that the % unbalance voltage is found to be 6.7%, 4.1% and 3.2% with PI, add-on resonant regulator and add-on RC controller, respectively.Therefore, the add-on RC controller shows better performance where unbalance factor has been reduced to almost 40% of its initial value.

In Figure 5.14 to Figure 5.16, the performance of add-on RC controller has been shown with two different non-linear load conditions. In Figure 5.14 when only PI controller is used in the system having a non-linear load with THD level of 28%, the voltage waveform got affected with THD level of 6%. However, the
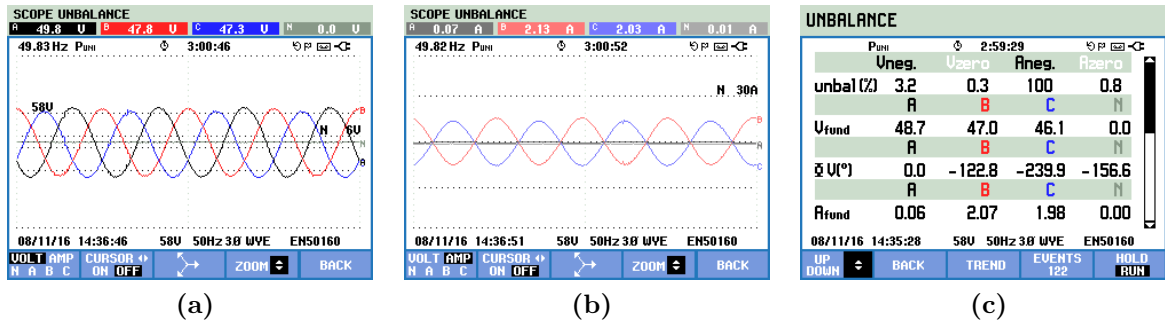
Figure 5.13 – (a) Output Voltage, (b) Load Current (c) Unbalance with add-on Repetitive controller

instant when add-on RC controller is activated under same load conditions, the THD level in voltage have been reduced to 4.1%, as shown in Figure 5.15. Further, the voltage THD level is found to be only 4.2%, even the presence of non-linear load having THD of almost 36%. Therefore, the voltage THD level remains within limit ($<5\%$) even when highly non-linear load (Rectified RLC) is applied as shown in Figure 5.16.
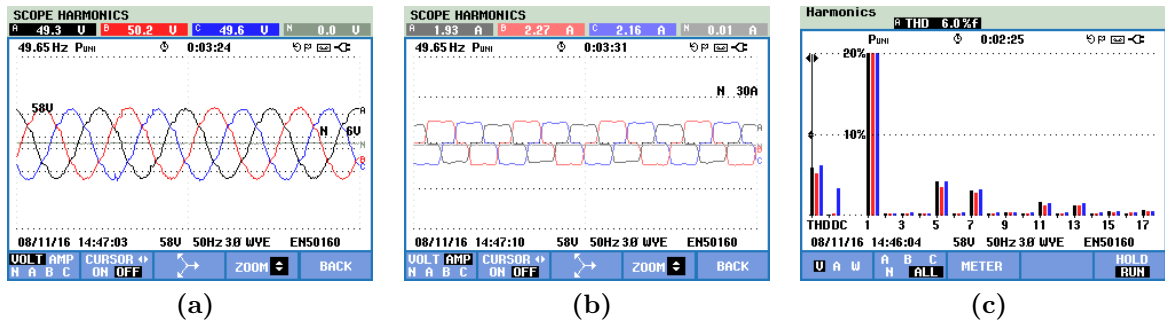
Figure 5.14 – (a) Output Voltage, (b) Load Current (c) THD without add-on controller
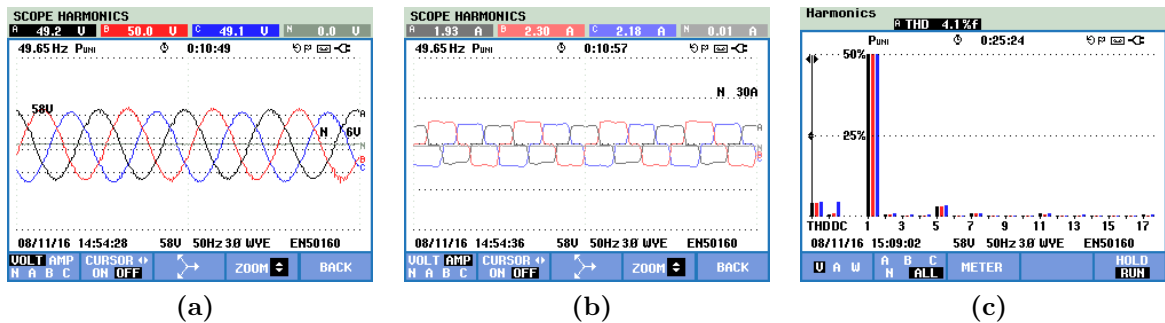
Figure 5.15 – (a) Output Voltage, (b) Load Current -RL(c) THD with add-on RC under Rectifeid RL load

| (a) | (b) | (c) |
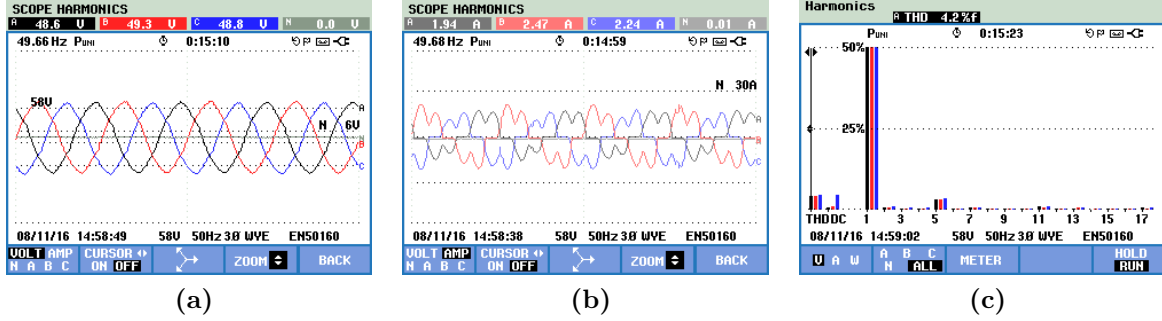
Figure 5.16 – (a) Output Voltage, (b) Load Current -RLC(c) THD with add-on RC under Rectifeid RLC load

5.3.2   Implementation Cost:

The major advantage of add-on RC over add-on multi resonant controller is its lower implementation cost in terms of digital hardware resources. Since, the proposed controllers have been implemented using FPGA, a brief comparison in terms of FPGA resource utilization have been provided in Table-5.1. . FPGA has limited resources in the form of logic cells, registers and multiplexers. FPGA cost increases exponentially with increase in these resources. Therefore, these logic resources must be optimally utilized to minimize total cost of hardware device. Here, it is quite evident that the logic count for add-on RC controller is almost half of the resonant controller which is tuned only for two harmonic frequencies. Resonant controller requires more logic resources for each additional harmonic component in proportional manner. However, RC requires long internal delay chain which must be implemented using dual port block random access memory (BRAM) to save basic logic resources of FPGA.

Table 5.1 – Comparison of FPGA Resources

FPGA Resource Type	PI Control		+Repetitive Control		+Resonant Control	
Slice LUTs as Logic	1326	1326	948	1428	2637	2637
Slice LUT as Memory	0		480		0	
Slice Registers	120		140		160	
Muxes	0		40		20	

5.4 Conclusion

In this chapter, a simple add-on repetitive controller have been designed, simulated and successfully implemented using FPGA for VSI control in MG. The proposed controller shows better performance in comparison to PI controller as well as add-on resonant controller. The add-on Repetitive controller is successfully able to minimize the impact of non-linear unbalance load on system voltage profile. The voltage THD level has been kept to almost 4% despite of non-linear load having THD level of 36%. Moreover, the system voltage remains perfectly balanced despite of sudden loss of one phase under heavily loaded conditions. Further, the proposed controller not only outperforms the conventional controllers but also requires lesser hardware resources.

L_1 ADAPTIVE DROOP CONTROL FOR MESH MICROGRID

In a 'plug and play' microgrid architecture, there occures a huge variation in network parameters when any source, load or part of network is added or removed from grid [136]. The variation in network parameters may not be easily handled by conventional droop controllers which are mainly designed with assumption of fixed network configuration. However, these assumptions become invalid for a microgrid having small mesh network with reconfigurable structure. The most important requirement of the microgrid is to remain stable not only during various dynamical parametric changes but also during dynamic topological changes. It is well established fact that to get required performance where plant parameters are subjected to disturbance or perturbation, the controller must be adaptive in nature. There are many possible ways to design such kind of adaptive controller. These controllers can have various performance measure and bounds to get requires stability and robustness. The most important requirement of controllers is to have good tracking performance in transient dynamical condition, fast adaptation and robust control. L_2 and L_∞ performance bounds can gives good tracking and robust performance respectively [116][137]. However, L_2 lacks robustness under parameter drift and L_∞ lacks in tracking performance with fast adaptation as there is a strong coupling between robustness and adaptation [138]. Various researchers are working towards composite controller to improve the tracking performance and fast adaptation under any parametric drift. These composite controllers many times found to have high adaptation gain and therefore tend to violate physical limits of the system. Most recently, the L_1 controllers are introduced which are

becoming more useful under wide parametric variations. These controllers are designed in such way that the tracking performance can be decoupled from adaptation preformation. Therefore, these controllers not only track reference under dynamic changes but also provide robustness under parametric variations.

In this chapter, a novel L_1 adaptive controller has been designed to achieve enhanced stability of microgrid under the varying network configuration and variable droop controller's characteristics [139]. Appendix is dedicated to provide brief theory of L_1 control with design and computation steps.

Power electronics interface like voltage source inverter (VSI) in AC- microgrid does not have any rotating mass and forms an inertia less system. The conventional control methods used in power system are designed to work with high inertia sources. Therefore, transient power sharing is naturally controlled by the inertia of the system.
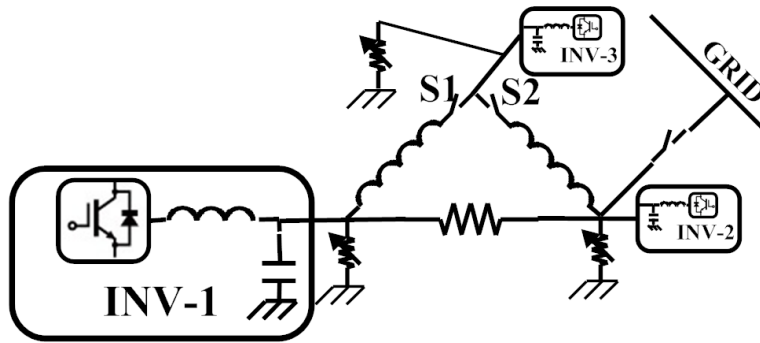
Figure 6.1 – Microgrid with small mesh network

A microgrid network generally works on low voltage level which makes network impedance to be varying in wide range from purely inductive to purely resistive[85]. Many times the sources as well as network may become redundant. This changes the network impedance whenever a branch or source is disconnected in a microgrid as shown in Figure 6.1. Therefore, the active and reactive power cannot be totally decoupled. These changes not only affect thepower sharing accuracy among the sources but also can destablize the full system [140]. However, the power sharing and stability can be improved by incorporating the variations in network parameters (i.e. R/X ratio) within control [141]. However, it requires reliable communication links among the sources to have information about their terminal voltage and current in order to estimate the line parameters.

Many researchers use virtual impedance in voltage control loop to make transmission line virtually inductive[46]. This certainly provides a good mechanism to implement virtual impedance with droop control in a network even having high (>1) R/X ratio to make it virtually inductive [50]. However, selecting a minimum value of virtual impedance is crucial as a larger value of output impedance may decrease output voltage magnitude. Secondly, if there is a local load connected to the source, then additional current sensors will be required for measuring line currents that further increases the cost of the system.

In this chapter a novel L_1 adaptive method for stable operation of a microgrid with wide range of R/X ratio [142]. L_1 adaptive methods are being widely investigated in aircraft control where model parameters vary in a wide range [138]. Therefore, this particular method has been opted for the control of microgrid which is very susceptible to instability with parametric variation.

6.1 Generalized Average Modeling of VSI in Microgrid

The dynamic performance and stability of microgrid operation may be analyzed using small signal modeling of the system as discussed in chapter-2. However, it is not always advisable to model a complete system if the analysis has a particular dynamical concern. Moreover, a full-scale model requires more complex time consuming computation. Incorporating these models into control loop will require high amount of computational resources, hence generally used in the offline analysis. The modeling based on generalized state space averaging method can reduce the complexity of the system significantly [143, 144, 145]. These kinds of modeling have the privilege to choose only those frequency components in the time domain which may have large impact on system dynamics. Therefore, this kind of approach is more suitable for the effective modeling of a given system with reduced complexity.

In the generalized averaging method, the time varying Fourier coefficient $X_\eta(t)$ with time interval $\tau \in [t-T, t]$ constitutes an approximated complex time domain waveform and expressed as:

$$x(\tau) = \sum_{\eta} X_\eta(t) e^{j\eta\omega_s\tau} \tag{6.1.1}$$

where the Fourier coefficient with index η is defined as:

$$X_\eta(t) = \frac{2}{T} \int_{t-T}^{t} x(\tau) e^{-j\eta\omega_s\tau} d\tau \bigg|_{\eta>0} \tag{6.1.2}$$

Here, this important property of the Fourier coefficient as derived in [145], needs special attention for modeling and analysis purpose. As per [145], the time derivation of ηth Fourier coefficient can be described as,

$$\frac{dX(t)}{dt} = \left\langle \frac{dx}{dt} \right\rangle_\eta (t) - jk\omega_s X_\eta(t) \tag{6.1.3}$$

It is important to note that the equation (6.1.3)includes the time varying frequency term ω_s. Therefore, the Fourier coefficient based modeling of microgrid will exhibit better performance where the system frequency fluctuates quite often depending on operating conditions. Further, the derived model can be easily modified to incorporate any number of system harmonics by increasing the number of coefficients.

In this particular study, it is assumed that the VSI's in microgrid are connected to each other via LC-Filter and transmission line impedance. This assumption allows the reconfigurable structure of microgrid, where it may vary from complex mesh to radial network or vice-versa. Here, the transmission line impedance is unknown but remains within finite range. Each VSI has its own inner control with different droop coefficients. Voltage and Current control loops of each VSIs are assumed to be of high bandwidth w.r.t. the droop control loop. This assumption gives way to make inner loop unity whenever analysis has an interest in only slow dynamics of the system.

Now, the voltage drop in inductive line impedance ($R + j\omega L$) can be written as:

$$\frac{d}{dt}\lambda(t) = f[\lambda(t), u(t)] \tag{6.1.4}$$

where is $\lambda(t)$ is flux linkage and $u(t)$ may be any periodic time-dependent function. For a transmission line having inductance L and resistance R with line current i_l at frequency ω, the voltage drop across the line with relevant Fourier Coefficient will be

$$v_z = jk\omega\lambda + \left\langle \frac{d\lambda}{dt} \right\rangle_k + Ri_l \tag{6.1.5}$$

or

$$v_z = jk\omega Li_l + \left\langle L\frac{di_l}{dt} \right\rangle_k + Ri_l \tag{6.1.6}$$

The above formulation can be used in the power flow equation after linearization. Rewriting power transfer equation already described in chapter-2 with conventional symbols,

$$P = 3\left(\frac{EV}{Z}\cos(\delta) - \frac{V^2}{Z}\right)\cos(\theta) + 3\frac{EV}{Z}\sin(\delta)\sin(\theta) \tag{6.1.7}$$

$$Q = 3\left(\frac{EV}{Z}\cos(\delta) - \frac{V^2}{Z}\right)\sin(\theta) - 3\frac{EV}{Z}\sin(\delta)\cos(\theta) \tag{6.1.8}$$

Linearizing equations (6.1.7) & (6.1.8) with assumption of small power angle (δ) i.e. $cos(\delta) = 1$ and $sin(\delta) = \delta$, we get

$$\Delta P = \frac{3RV\Delta E}{R^2 + X^2} + \frac{3\delta XV\Delta E}{R^2 + X^2} + \frac{3EXV\Delta\delta}{R^2 + X^2} \tag{6.1.9}$$

$$\Delta Q = \frac{3XV\Delta E}{R^2 + X^2} + \frac{3V\delta R\Delta E}{R^2 + X^2} + \frac{3ERV\Delta\delta}{R^2 + X^2} \tag{6.1.10}$$

Using equation (6.1.6) in $(((6.1.9)$ & $(6.1.10)))$ at fundamental frequency while ignoring second order perturbations, we get,

$$\frac{X^2}{\omega^2}\frac{d\Delta P}{dt} + 2R\frac{X}{\omega}\frac{d\Delta P}{dt} - \frac{XV}{\omega}\frac{d\Delta E}{dt} +$$
$$(R^2 + X^2)\Delta P - 3VR\Delta E - 3VX\delta\Delta E - 3EVX\Delta\delta = 0 \tag{6.1.11}$$

$$\frac{X^2}{\omega^2}\frac{d\Delta Q}{dt} + 2R\frac{X}{\omega}\frac{d\Delta Q}{dt} - \frac{3XVE}{\omega}\frac{d\Delta\delta}{dt} - \frac{3XV\delta}{\omega}\frac{d\Delta E}{dt} +$$
$$(R^2 + X^2)\Delta Q - \frac{3VX}{\omega}\Delta E - 3VR\delta\Delta E - 3EVR\Delta\delta = 0 \tag{6.1.12}$$

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(a)

(b)
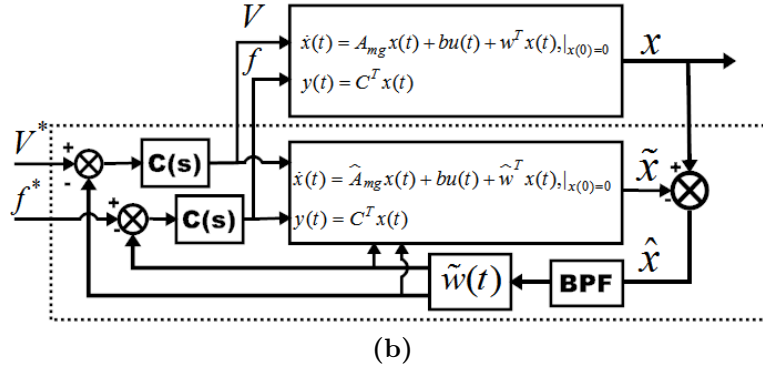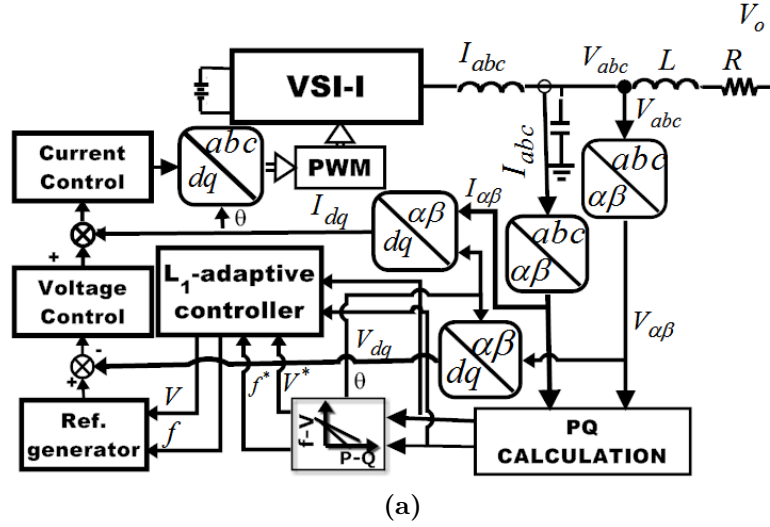
Figure 6.2 – (a) Adaptive control system of an Inverter (b) Adaptive Controller diagram

Furthermore, linear droop equation with low pass filter having cut-off frequency ω_c, the linear droop controller can be defined by equations (6.1.13) and (6.1.14).

$$\Delta\omega = \frac{-m_f\omega_c}{s + \omega_c}\Delta P \tag{6.1.13}$$

$$\Delta E = \frac{-m_e\omega_c}{s + \omega_c}\Delta Q \tag{6.1.14}$$

From equation ((6.1.11)-(6.1.14)) we can get state space model as described by (6.1.15).

$$
\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \\ \dot{x}_5 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 & \frac{-3V\omega m_e\omega_c}{X} & 0 & 0 \\ -(\frac{\omega^2 R^2}{X^2}+\omega^2) & -\frac{2R\omega}{X} & 0 & 0 & 0 \\ 0 & 0 & \frac{3XV\delta m_e\omega_c}{\omega} & 1 & \frac{-3XVE}{\omega} \\ 0 & 0 & -(\frac{\omega^2 R^2}{X^2}+\omega^2) & -\frac{2R\omega}{X} & 0 \\ -m_f\omega_c & 0 & 0 & 0 & -\omega_c \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix}}_{x} +
$$

$$
\underbrace{\begin{bmatrix} \frac{-3V\omega\omega_c}{X} & 0 \\ \frac{3V\omega^2 E(R+X)}{X^2} & \frac{3\omega^2 VE}{X} \\ -\frac{3XV\delta\omega_c}{\omega} & 0 \\ 3V(\frac{X}{\omega}+R\delta) & \frac{3R\omega^2 E^2}{X^2} \\ 0 & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} \Delta E \\ \Delta\delta \end{bmatrix}}_{u} \qquad (6.1.15)
$$

where $x_1 = \Delta P, x_2 = \dot{\Delta P}, x_3 = \Delta Q, x_4 = \dot{\Delta Q}$ and $x_5 = \Delta\omega$ with $\Delta\omega = s\Delta\delta$

6.2 L_1 Adaptive Droop Control

The model derived in previous section is utilized for adaptive control of micro-grid. This model requires less computational resources and therefore gives faster responses in L_1 adaptive controller.

6.2.1 L_1 Adaptive control Theory:

Let consider a microgrid system as:

$$
\dot{x}(t) = Ax(t) + B(u(t) + w^T(t)x(t))\big|_{x(0)=x_0} \qquad (6.2.1)
$$

where, $W(t) \in R^n$ is a vector of the uniformly bounded by varying unknown parameters. Here, we impose the bound on $W(t)$ by considering maximum possible variation in transmission line impedances in the microgrid. Similarly, the system predictor may be defined as,

$$
\dot{\tilde{x}}(t) = A\tilde{x}(t) + B(u(t) + \tilde{w}^T(t)\tilde{x}(t))\big|_{\tilde{x}(0)=\tilde{x}_0} \qquad (6.2.2)
$$

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where $\tilde{x}(t)$ and $\tilde{w}(t)$ are estimated states and parameters of the system. With adaptive control, input can be divided into two components as:

With adaptive control, input can be divided into two components as:

$$u(t) = u_n(t) + u_{ad}(t) \qquad (6.2.3)$$

while, $u_n(t) = -K_{droop}x(t)$ represent nominal droop controller. The adaptive component can be defined as:

$$u_{ad}(s) = -C(s)\left(\xi(s) - r(s)\right) \qquad (6.2.4)$$

where, $r(s)$ and $\xi(s)$ are the Laplac domain vvariable of the input, $r(t)$ and , $\xi(t)$ ($\xi(t) = \tilde{w}^T(t)\tilde{x}(t)$)) respectively. $C(s)$ is strictly proper transfer function with $C(s) = 1$.

On rearranging the equation (6.2.2) and equation (6.2.3), we have,

$$\dot{\tilde{x}}(t) = (A - BK_{droop}u_n(t))x(t) + B(u_{ad}(t) + \tilde{w}^T(t)\tilde{x}(t)) \qquad (6.2.5)$$

or

$$\dot{\tilde{x}}(t) = A_n x(t) + B(u_{ad}(t) + \tilde{w}^T(t)\tilde{x}(t)) \qquad (6.2.6)$$

The coefficients value of nominal droop controller should be such that A_n remain Hurwitz. The non-linear nature of the adaptive controller sometimes gives unbounded output which may lead to instability. This output is made saturated for some values to avoid such situations. However, such coarse saturation of output may decrease the performance of the controller. Therefore, many researchers use the projection operator with predictors to bounds the non-linear output so that adaptive controller confirms the Lyapunov stability rules.

Let, $\hat{x}(t) \triangleq \tilde{x}(t) - x(t)$ estimation error and P solve the Lyapunov equation $A_n P + P A_n = -Q$ for any arbitrary $Q^T > 0$.

The L_1 norm for the adaptive controller for a given $C(s)$ can be defined as:

$$\lambda \triangleq \|(sI - A_n)B(1 - C(s))\|_{L_1} L_n < 1 \qquad (6.2.7)$$

where $L_n \triangleq \underset{w \in W}{max} \, \|w\|_1$ and

$$\dot{\tilde{w}}(t) = \text{Proj}(\tilde{w}(t), -\hat{x}(t)PBx(t)) \tag{6.2.8}$$

6.2.2 Design of L_1 Droop Controller

The configuration of L_1 adaptive controller is shown in Figure 6.2. Let the dynamics of a microgrid is defined by the equation (6.2.1), where state transition matrix A and input matrix B is in accordance with the equation (6.1.15) of the modeled system.

The inner voltage and current loop are of very high bandwidth w.r.t. outer droop control and therefore, may be taken as unity. Here, w^T is unknown time varying line parameter and is bounded by:

$$\begin{aligned}
R &\in [R_{\min} \; R_{\max}] \\
L &\in [L_{\min} \; L_{\max}]|_{L \neq 0} \\
\omega &\in [\omega_{\min} \; \omega_{\max}]|_{\omega \neq 0}
\end{aligned} \tag{6.2.9}$$

For given values as in Table-A.2 of the Appendix-A, we can find the value of L_n accordingly [146][147]. The appropriate value of $C(s)$ for L_1 norm is computed such that it gives desired performance while satisfying equation (6.2.7). The detail calculation norm and controller are provided in appendix-B.3.

Further, a band pass filter can be used to limit the operating bandwidth of adaptive controller so that it could only work for low-frequency modes of the system as they are most sensitive to line impedance variations. Here, $\tilde{w}(t)$ is further can be computed using projection operator. The projection operation requires a continuous differentiable convex function. i.e.

$$f(\tilde{w}) = \frac{\|\tilde{w}\| - \tilde{w}_{\max}^2}{\varepsilon_0 \tilde{w}_{\max}^2} \tag{6.2.10}$$

where $\varepsilon_0 (\approx 0.01)$ is projection tolerance.

For a nominal value of system parameters $V = 54\angle 0, 54\angle 0.05$, (in pu for calculation) and $Q = diag[10, 1, 1, 1, 10]$, P can be computed. Thereafter the bounded value of $\tilde{w}(t)$ can be computed as:

$$\text{Proj}(\tilde{w}(t), -\hat{x}(t)PBx(t)) = \begin{cases} -\hat{x}(t)PBx(t) - \left.\frac{\nabla f(\tilde{w})\nabla f(\tilde{w})^T}{\|\nabla f(\tilde{w})\|^2}\right|_{if\ f(\tilde{w})>0} \\ \\ -\hat{x}(t)PBx(t)|_{if\ f(\tilde{w})\neq 0} \end{cases} \quad (6.2.11)$$

6.2.3 Hardware Description and Results
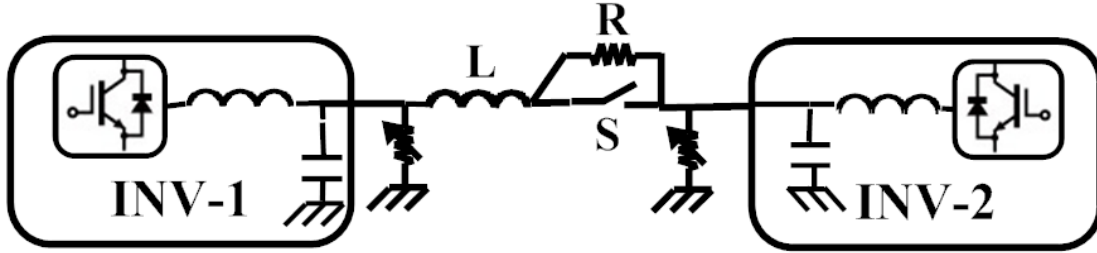
Figure 6.3 – Schematic of Two VSI forming microgrid with Line Changeover Switch

The proposed control algorithm is designed and simulated using MATLAB /Simulink, which is again verified on a low voltage hardware prototype. The hardware consists of two 3-ph, 2-level inverters with output LC-filter, connected in parallel with the provision of variable transmission line parameter using equivalent resistances and inductances. Two separate battery sources are used to feed both the inverters separately. Here, the batteries may be charged externally via any RES like solar or wind using DC/DC or AC/DC converters. The droop coefficient of controller can be changed as per state of charge (SOC) of the batteries. Both inverters are connected by circuit breaker that can be operated under various conditions (i.e. over current, synchronization etc.). There is also provision of changing the transmission line resistance using three phase isolator. The hardware schematic is depicted in Figure 6.3 and which detail description is already provided in chapter-3. The control is fully implemented in discrete using FPGA (Xilinx zynq-7000 SOC, Zedboard) platform. All computations are performed in fixed point numbers with other optimization as given in chapter -7.

6.2.4 Eigen Value Analysis

The effect of various parameters on microgrid can be analyzed using their mathematical model. Small signal stability analysis can be performed by plotting the

eigen values (Modes) of microgrid under its different varying parameters (e.g. droop coefficient, line resistance).

(a) Without adaptation   **(b)** With adaptation
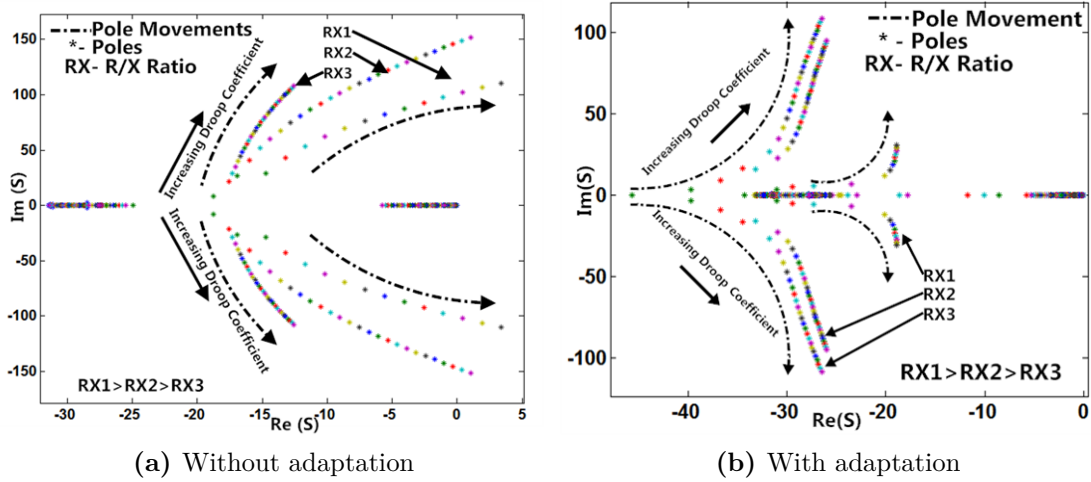
Figure 6.4 – Variation in low frequency modes of two inverter microgrid

In Figure 6.4 eigen values of two inverter microgrid has been plotted with different droop and line impedances. Here, it can be seen that in Figure 6.4 (a) with conventional droop control, few eigen values move towards the RHS of imaginary axis and crossed it when increasing the droop coefficient in high R/X ratio of transmission line, which shows instability in system. It is also observable that higher the R/X ratio gives greater chance of instability. However, with proposed L_1 controller as shown in Figure 6.4 (b), the eigen values are moving in parallel to imaginary axis, which clearly shows that increasing droop with high R/X does not leads to instability in system.

6.2.5 Simulation

The similar observations may be made in simulation results as shown Figure 6.5 and Figure 6.6 where two inverters are synchronized in parallel with high R/X transmission line. Figure 6.5 clearly shows that without adaptive control the system becomes unstable within few cycles after interconnection, where magnitudes of power oscillation keep on increasing exponentially.

However, in Figure 6.6, it is shown that with adaptive control, the power oscillation is damped out rapidly even when droop coefficient of one of the inverters
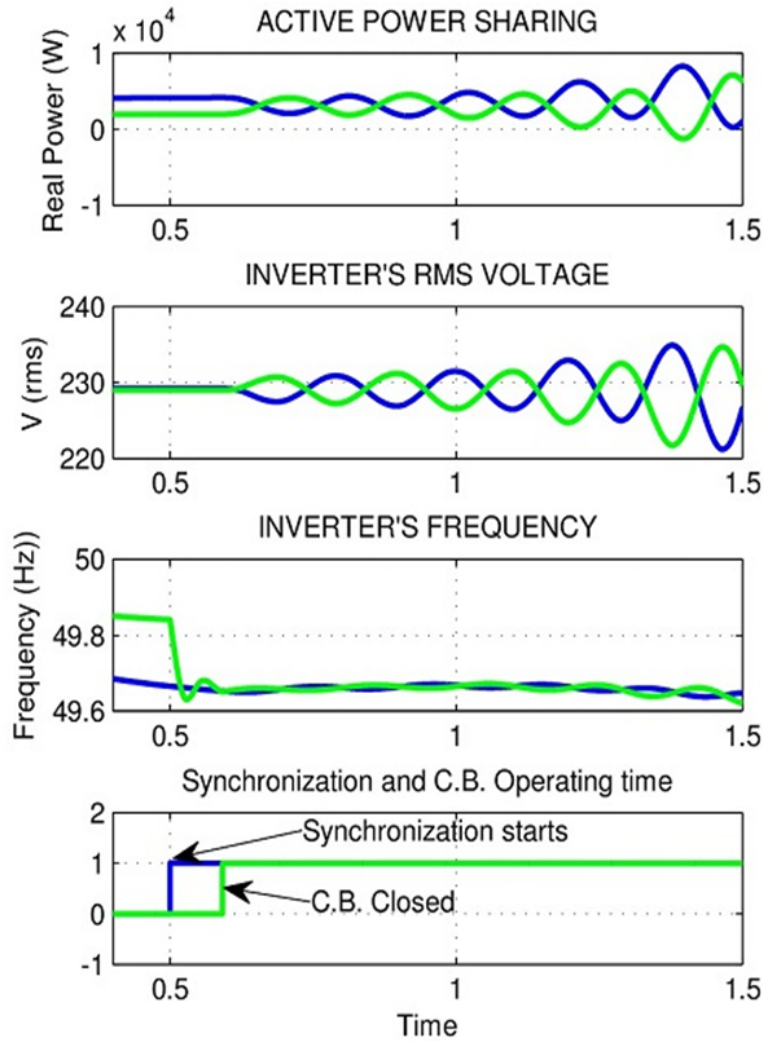
Figure 6.5 – Parallel operation with High R/X (Simulation) without adaptive control

is increased to 200% of its original value. This shows significant improvement in stability of the microgrid.

6.3 Real Time Hardware Verification:

To test performance and robustness of L_1 droop controller, experiment has been conducted for two different cases. In the first case, frequency droop coefficient of one of the inverter is gradually increased up-to 200% of its initial value under high R/X ratio while in second case, R/X ratio of transmission system is increased to more than 7 times of its initial value keeping all droop coefficient values intact. In both these cases L1 controller is compared against conventional droop controller.
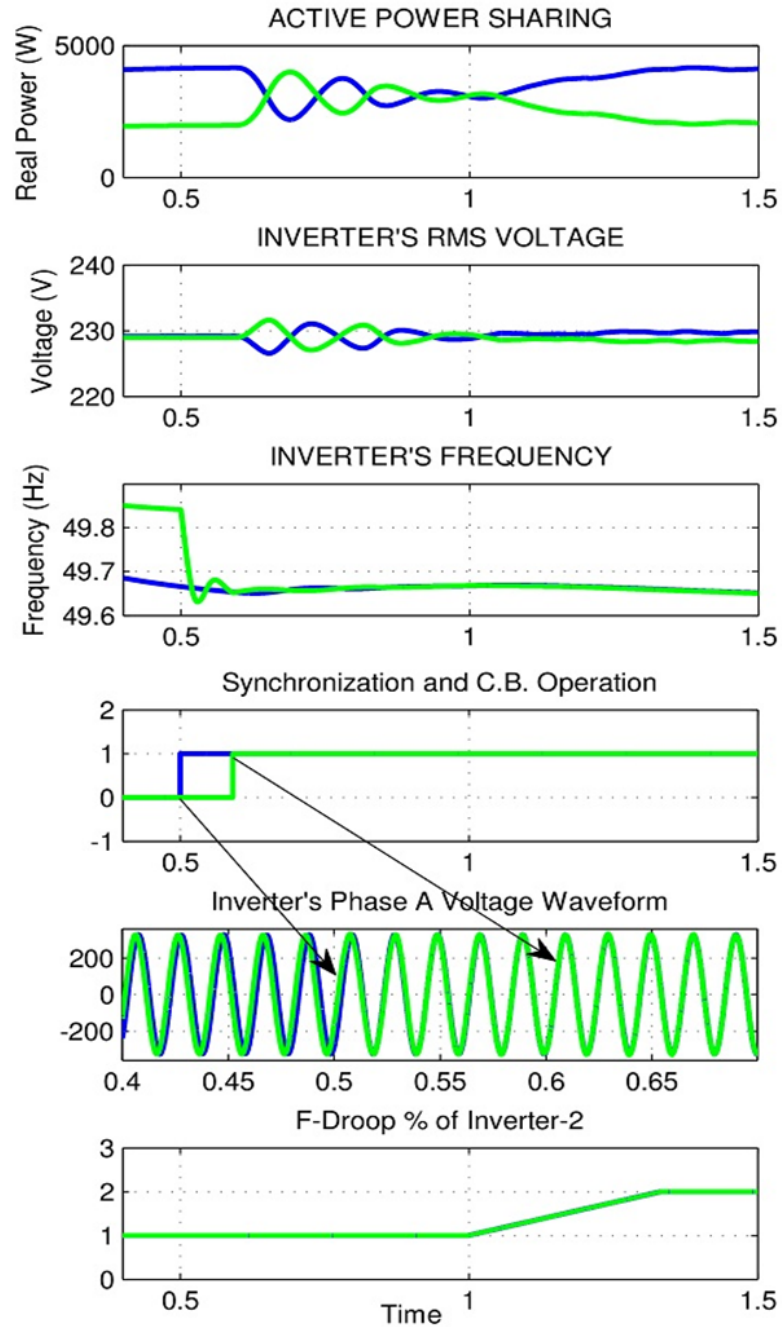
Figure 6.6 – Parallel operation with adaptive control with High R/X (>7) and Increased f-droop coefficient

6.3.1 Case 1: Variation in Droop Coefficients with High R/X

Under similar dynamic conditions as in simulation, real world hardware experiment at low voltage has been performed. Figure 6.8 show the operation of microgrid without adaptive control.

In Figure 6.7 , both VSI's are operated in parallel at high R/X ratio of the

(a) Current waveforms - (1th.VSI-1, 2nd.Load, 3rd. VSI-2) 4th. Load Voltage

(b) Parallel operation with adaptive control with High R/X (>7) and Increased f-droop coefficient
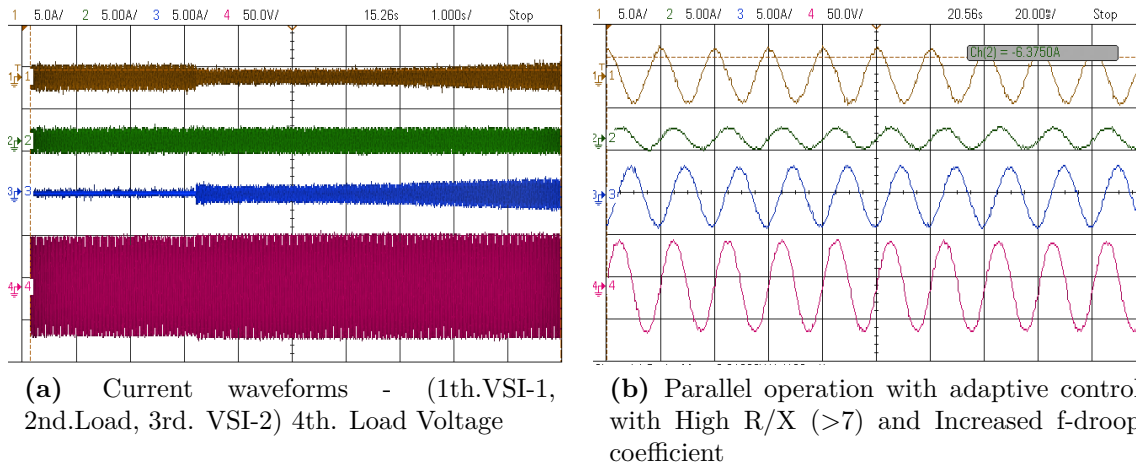
Figure 6.7 – Increasing droop (up-to 200%) with high R/X ratio (>=2) without adaptive control

(a) Current waveform - (1th.VSI-1, 2nd.Load, 3rd. VSI-2) 4th.Voltage across Load

(b) Current waveform - (1th.VSI-1, 2nd.Load, 3rd. VSI-2) 4th.Voltage across Load
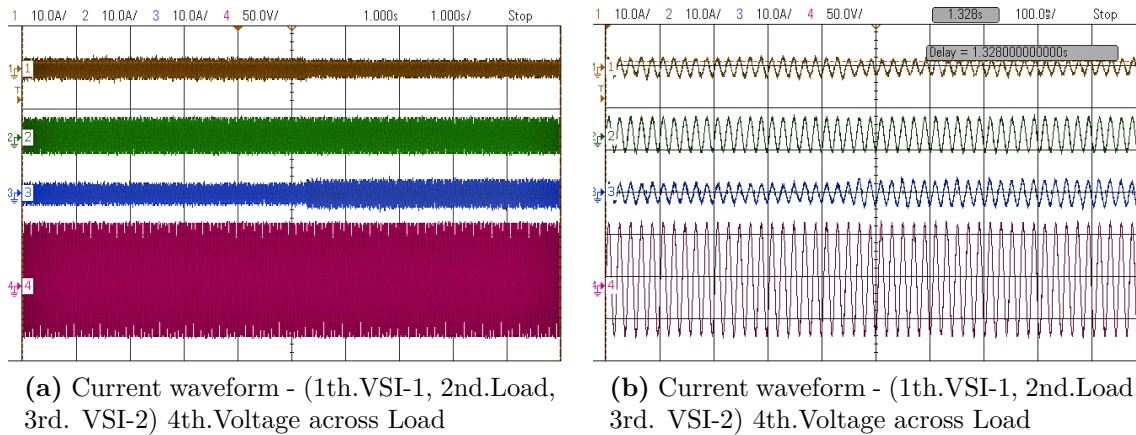
Figure 6.8 – Increasing droop (up-to 200%) with high R/X ratio (>=7) with adaptive control

transmission line with a small frequency-droop coefficient. Both inverters start operating in parallel, but as soon as there is an increase the f-droop coefficient of one of the VSI, the microgrid becomes unstable and both inverter's output currents keep on increasing exponentially while load current remains same. Figure 6.8 (b) shows the later and zoomed version of current where the magnitude of current increases sufficiently to high levels with high reactive power circulation.

Similarly, Figure 6.9 shows the performance of L1 adaptive controller in sharing active power, where even change in droop coefficient under highly resistive transmission line does not have any significant impact on microgrid stability. However, there appears to be some power loss due to increase in line losses and small
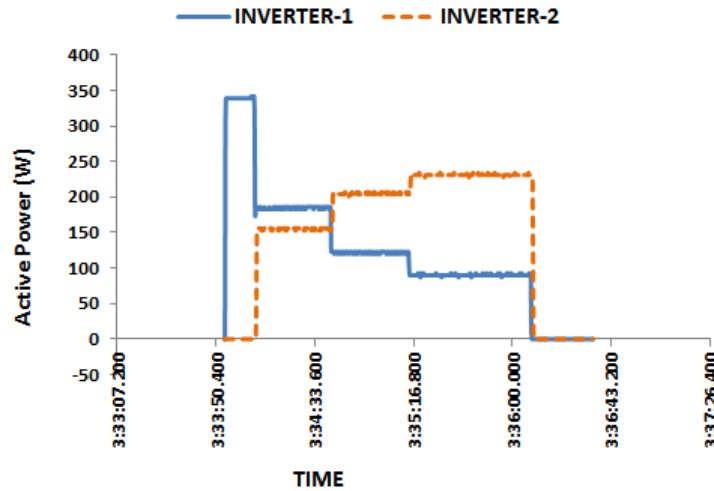
Figure 6.9 – Power sharing while Increasing droop (up-to 200%) with high R/X ratio (>=7) with adaptive control

increase in circulating current but the system remains stable during these fast dynamic changes.

6.3.2 Case 2: Increasing R/X Ratio Instantaneously

In Figure 6.10 both VSIs are operating in parallel using conventional droop controller with inductive transmission line (R=0.1 ohm X=0.32 ohm) sharing almost equal power due to their equal droop coefficient of both the inverters. Robustness of controller can be tested under high parametric variations. In this case these variation in emulated by increasing transmission line resistance by instantly opening bypass switch across resistor in transmission line.
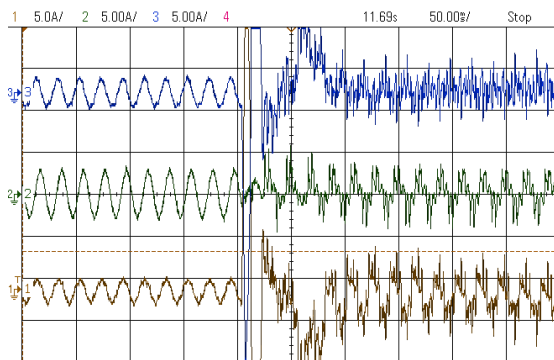
(a) Current waveform - (1th.VSI-1 , 2nd.Load, 3rd. VSI-2)
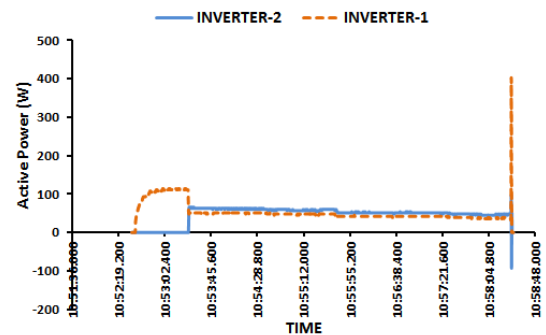
(b) Active power output of VSIs (data logging = 4 sample/sec)

Figure 6.10 – Instantaneous Change of R/X from 0.3 to 7 without adaptation

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However, as soon as the switch is transferred, the transmission line become more resistive (2.2 ohm) and both VSIs shows a rapid rise in their output currents which circulate between the inverters with completely distorted waveform. In Figure 6.10 (b) the active power has been logged, which supports the observation showing a sudden change in power where one of the inverter becomes the source and other becomes a sink.

(a) Current waveforms - (1th.VSI-1 , 2nd.Load, 3rd. VSI-2) 4th. Load Voltage

(b) Current waveforms - (1th.VSI-1, 2nd.Load, 3rd. VSI-2) 4th. Load Voltage
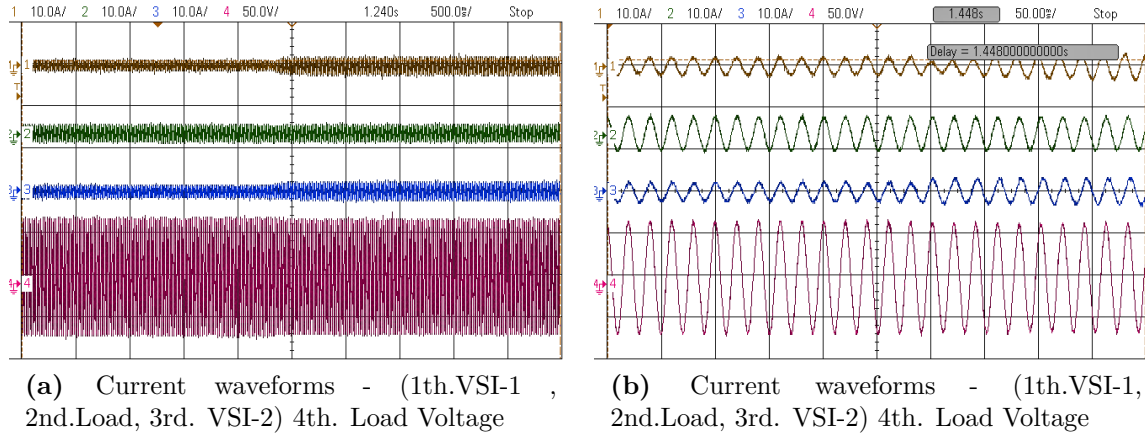
Figure 6.11 – With adaptive Control R/X increased from 0.3 to 7

The similar experiments are performed while incorporating L1-adaptive droop controller, which increases the stability of microgrid significantly high. Figure 6.11 and Figure 6.12 shows the output currents and active power of both the inverters where the transmission line is switched to high resistance mode (2.2 Ohm) during runtime.

It may be easily observed from figures that system remains stable during the transition. However, power sharing of both inverters gets affected by small amount due to lines losses and impedance mismatch.

6.4 Conclusion

In this chapter, a novel L_1 control has been implemented as adaptive droop controller. The performance of L_1 controller is extremely good in respect of its fast adaptation and robustness. The High R/X ratio which is generally found in network of underground cables and short distance transformer- less distribution lines, cause the instability issue in droop control microgrid. This instability issue can
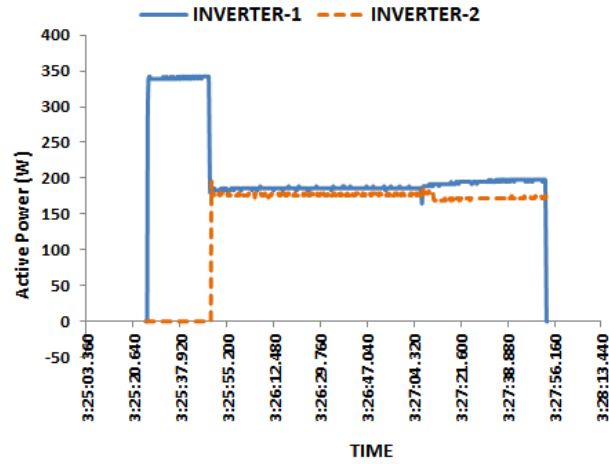
Figure 6.12 – Power sharing with adaptive Control R/X increased from 0.3
to 7

be mitigated by using fast adaptation in droop controller. L_1 controller has best
theoretical properties for fast adaptation hence it shows good results when used
as adaptive droop controller.

The proposed method successfully handled the large variation in network para-
meter along with variable droop characteristics without losing stability. The pro-
posed strategy uses the generalized averaging method to model the inverter opera-
tion in islanded microgrid. On closely observing the controller design methodology,
it can be inference that the same model may be used for any number of inverters.
Moreover, with the increase in number of sources the stability of microgrid may
also increase.

IMPLEMENTATION OF CONTROL WITH FPGA

With technological advancements, a system can be designed in various configurations using various technologies. A controller can be implemented by using basic analog circuits, Microprocessor / Microcontroller, Digital signal processors (DSPs) or most advanced technologies like CPLD[1]s, Field programmable gate arrays (FPGAs) with System on Chip (SOC). All technologies have their own economics, benefits, merits and demeris [148]. In this research work, the FPGA based digital controller has been designed, while DSP and microcontroller based controllers have also been tested and found less useful to carry research on the desired topic.

(a) Xilinx Virtex-II Wafer   **(b)** CLB /Slice
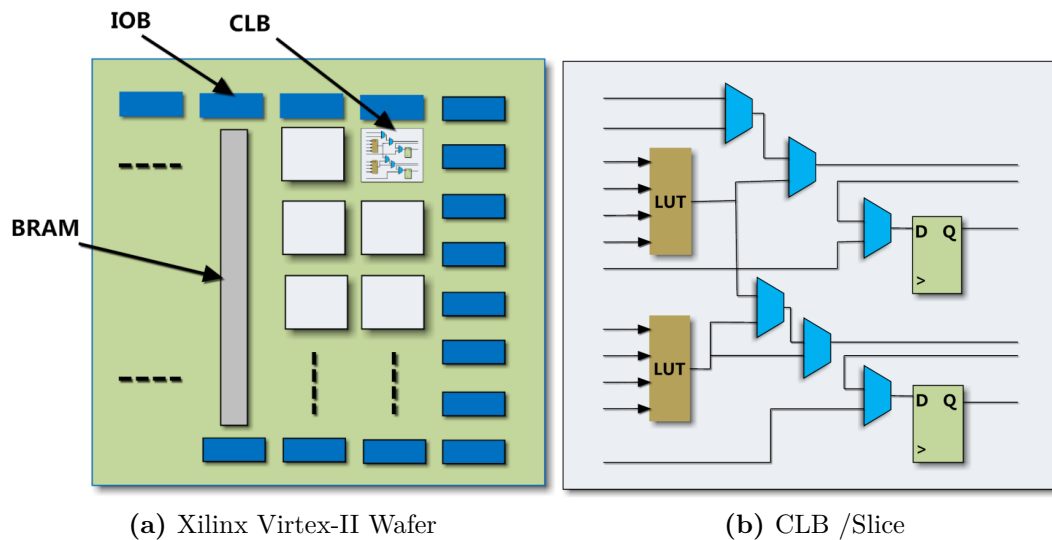
Figure 7.1 – Xlinx FPGA Slice

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[1]CPLD is next generation in programmable logic devices having higher complexity than PAL & PLA

7.1 FPGA Overview

FPGAs are integrated circuits which are able to implement any digital function or logic. Thet give the designer an ability to implement any logic (sequential or combinational) with different input/ output (IO's) in same semiconductor device. Xilinx introduced first commercially viable FPGAs in 1985. These FPGAs have combined functionality of CPLD and PLA[2] and can be programmed many times in the field. Basic FPGA semiconductors consist of many Configurable logic blocks (CLBs) or Slice with I/O routing antifuse and I/O pads. The internal architecture of CLBs is different among the manufacturers but they work almost in a similar fashion, so majority of function that can be used in one FPGA can be used on another FPGA device independently. Figure 7.1shows schematic of a FPGA slice from Xilinx [149]. A FPGA wafer contains multiple unit of CLBs where each CLB have some basic digital circuit containing Look up Tables (LUTs), Multiplexers and memory units (Flip-Flop). LUTs are used to generate any combinational function with multiple inputs which are further connected to various multiplexers which can be configured as adder or subtractor. Every CLB contain few memory elements to perform sequential and other clock synchronized operation. The output of each CLB unit is connected to Input output boundary (IOB) from where they can be routed to anywhere in wafer via antifuse. The advance FPGA contain some more complex slices to perform dedicated operation like multiply plus Accumulate (MAC), Digital Signal processing, Barrel Shifting etc. In addition to all these FPGA contain Random Access Memory (BRAM) distributed in blocks within FPGA wafer to perform high memory and I/O buffer operation . A FPGA can be configured via software environment to perform particular logical operation. Any (Verilog or VHDL) Hardware Descriptive Languages (HDL) can be used to describe the logic operation in a software environment [150, 151]. The number of logic operation which a FPGA can perform depends upon the available resources particularly the FPGA chip. A FPGA can perform more complex task with higher amount of available resources. However, utilization of FPGA resources can be improved by efficient hardware coding. A FPGA manufacturer

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[2]Basically used to implement combinational circuits

gives a bundle of softwares which perform different task with optimization before flashing a FPGA chip. These operation contain I/O planning, Synthesis for optimal resource utilization and Clock & Timing performance. A brief description of these operations is given below for Xilinx FPGA .

a)   I/O planning & design verification: This is the first step, here design is verified against various constrains. The number of I/O, their speed and voltage level are fixed in each FPGA so a designer cannot violate these. Therefore, they are tested and verified.

b)   Synthesis: Each HDL code is compiled and converted into register transistor logic (RTL) netlist. Synthesis test for behavioral model of all component of compiled RTL netlist to generate a gate level structure. It is not always possible to generate gate level structure for every HDL code for a given FPGA technology. However, the HDL code may simulate correctly and logically correct. Synthesis also gives estimation of the required resources like CLB, DSP-Slice, BRAM etc. for given HDL code. It also checks routing possibility for particular net from IOB to I/O pads. A few number of optimizations are also performed in this step in order to reduce gate count. After a successful synthesis gate level structure is ready to be implemented.

c)   Implementation: This is most important and vital step in FPGA design. Optimization is performed for timing and resource management. Mapping of I/O's with optimized routing is performed. Many times a synthesized code or RTL netlist is not implementable due to lack of available resources in FPGA. Moreover, the timing constraint (like two high speed signal must be routed is such a way that they possess acceptable time delay with each other at the termination) must be achieved for proper operation. After implementation software generates bitstream (bitcode/hexcode) for FPGA.

There are various manufacturers which provide FPGA based development platform. These platforms are built to satisfy variety of needs of system designers to

Table 7.1 – FPGA- ZYNQ-7000-SOC (xc7z020clg484-1) Resources

FPGA series	PL cells	LUTs	Flip-Flops	BRAM	DSP Slices (18x25 MAC)	APU
Artix-7	85K	53.2 K	106.4K	4.9 MB	220	Dual Core ARM-Cortex-A9
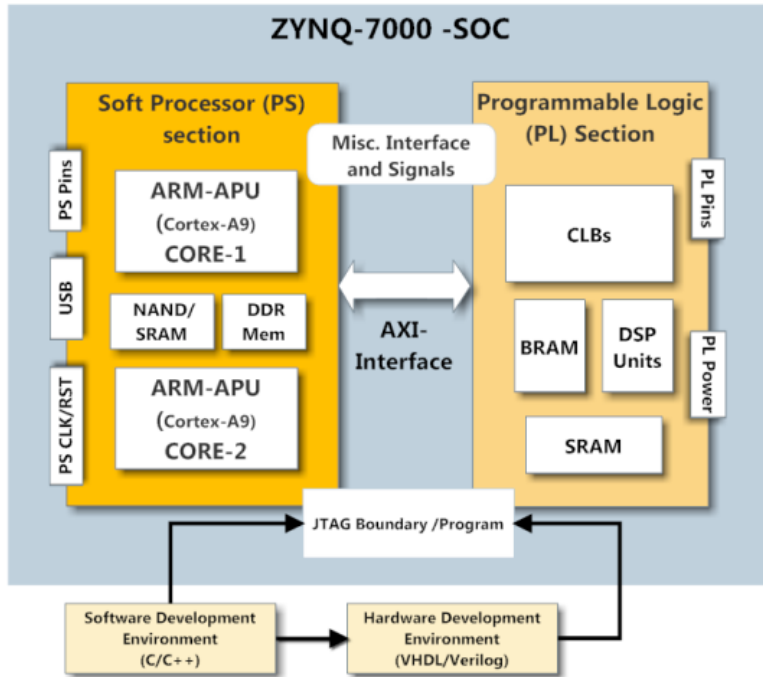
Figure 7.2 – ZYNQ FPGA SOC Design

test their code and develop prototype rapidly. We choose ZYNQ-7000-SOC based development platform ZEDBOARD© produced by digilent™ for the research purpose. The resources of particular FPGA are given in Table-7.1 and architecture is shown in Figure 7.2. In additional to Conventional FPGA elements ZYNQ-7000 contain DSP slices and ARM architecture based Dual core Application Processor Unit [152]. Apart from above resources additional peripherals are required to perform different operation like communication, display and analog to digital or digital to analog conversion etc. These peripherals have to be designed externally by system designer. This work required multichannel ADC to get voltage and current samples which are utilized to perform close loop operation of microgrid in

FPGA.

7.2 ADC Design & Interfacing with FPGA
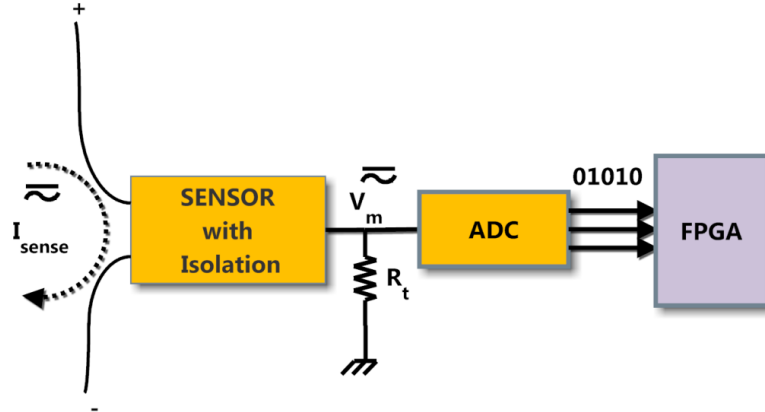
(a) Interfacing of sensor with ADC & FPGA
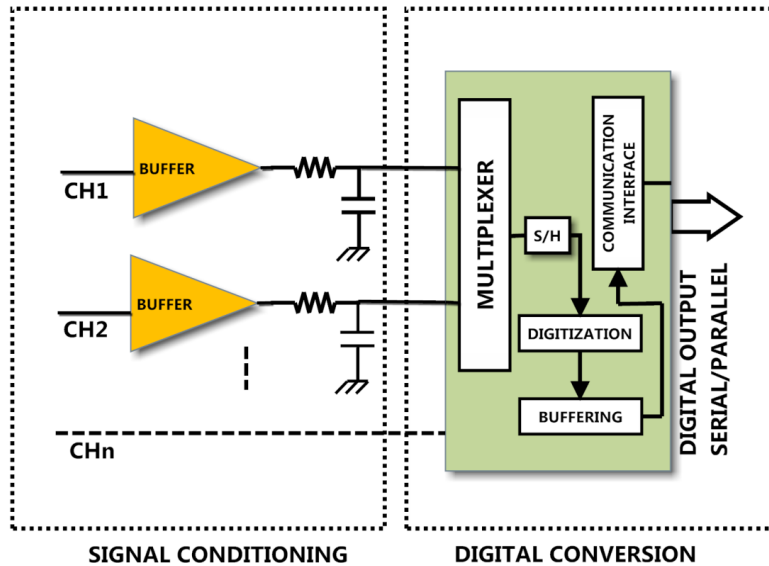
(b) ADC circuit diagram

Figure 7.3 – ADC-FPGA Interface

ADCs are used to convert analog signal into digital signal. Closed loop control of VSI requires the feedback of voltage and current signals. These signals are of high amplitude therefore cannot be used directly in low voltage digital circuitry. Voltage and current sensors are required to convert these high amplitude signals into low amplitude signal with minimum loss in frequency and phase characteristics of the signals. Most industrial high voltage and high current sensors are based on Hall Effect transducer and gives isolated linear current output corres-

ponding to applied signal. By suitable resistive termination this current output is finally converted into low voltage signal and fed to ADC circuitry as shown in Figure 7.3. Digitization of analog signal within IC is done by various methods. Delta-sigma and Successive approximation are the most common methods for medium bandwidth signal conversion. Various semiconductor device manufacturers produce ADC in IC based on these methods. The cost of the IC depends upon the resolution and conversion speed of ADC. A higher resolution and higher bandwidth ADC has higher cost. The cost of ADC cab further be reduced by multiplexing multiple analog inputs with single converter and single sample and hold (S/H) circuit. All channels are polled sequentially and buffer digital data in the dedicated registers from where they can be read by external processor. Digilent zedboard provides a number of digital I/Os at board connector terminal for display, communication and general purpose input/output (GPIO). These I/O are grouped in five 8-bit single ended I/O data port called PMOD™, 10 LED output, 8 input switches, VGA, HDMI and one FMC connector with 34 line of differential I/O. From these, every port is either connected to programmable logic (PL) cells or application processor units. Therefore, selection of a particular port is restricted to a particular use. Before designing an ADC interface for any control, it is required to know the following parameters:

a)   Minimum frequency to be measured: By Nyquist Shannon sampling theorem i.e. a signal can be reconstructed form the samples if sampling frequency is grater than equal to the twice of maximum frequency present in the signal. Therefore, An ADC must sample the signal at double of the frequency of the highest harmonic presents in voltage and current signal. Therefore, sampling frequency of ADC must be adequate.

b)   Input type: Industrial sensors generally require bipolar supply in the range of ±15 V to ±10V and provide full range output at similar rail to rail voltage level. Therefore, ADC input port must be tolerant of minimum ±10 V.

c)   Resolution: The minimum value of amplitude of a signal that can be

measured by ADC is known as resolution. Higher resolution requires higher number of bits to store. Therefore, digital bit length is directly a measure of resolution of the ADC. The General purpose ADCs available in market have resolution in the range of 8-bit to 32 bit. As we go for higher resolution the sampling time gets increased and therefore bandwidth of ADC gets reduced. A 16 bit ADC is sufficient in most of the electrical signal conversion.

d) Output: Once a signal is sampled, it is digitized and stored into ADC's buffer register. This buffer register can be accessed from external world through parallel or serial interface. A parallel interface is faster than serial interface but it requires higher number of data lines while serial interface requires less or only one data line to transfer the data. In parallel interface the higher number of data line are required for higher resolution while in serial interface data line remains same and independent to data width. So interface must be chosen for available data line.

A pseudo code for SPI interface is given in algorithm 7.1. This code can be compiled and simulated in test bench within software environment. After successful testing, code is encapsulated (using software like Core generator) in the form of unit component (IP) so that it can be used with multiple instances and connected to other components by simple interconnection of ports through graphical user interface1 (GUI) as shown in Figure 7.4.

7.3 Droop Control

Block Droop controller generates voltage magnitude and frequency as a linear function of input powers as shown in Figure 7.5. In FPGA implementation droop coefficients and rated voltages are externally set in APU therefore these can be updated at real time. The ARM® -AMBA architecture uses AXI bus protocol to communicate between PL (FPGA logic) and APU. Hence, AXI-LITE Bus port has been created for variable droop coefficient and rated voltage parameters to access from APU. Phase is calculated by time integration using feedback loop and

---

Algorithm 7.1 Pseudo Code for ADC (VHDL

Define Library & Standards [as: ieee.std_logic_1164.all];

Define GENERIC {ALL VARIABLE PARAMETERS} [CLOCK,GAIN,CHANNELS];

Define PORTS {All I/O ports} [clock, chip select, reset, MISO,MOSI, OUTPUT_VECTOR(8)]; *// The output vector is of 8 channel and 16 bit wide can be define by std_logic_vector in VHDL and accessible to outside world//*

Define ARCHITECTURE and STATE MACHINE [all internal signals, buffer registers, temp bits, counters]; *// ARCHITECTURE define all internal connection and signals. These signals are not visible from outside word//*

Write the PROCESS

[IF Reset(Low)

{clear all output registers,internal counters}

set {MOSI Tri-state,CS(high)

set {all Generic parameter to configuration register of ADC}

goto STATE ready;

END IF

IF Clock(high,rising edge] **and Reset**(High)

{check CS, set clock polarity for ADC}

goto STATE Sampling **END IF**

STATE: ready *// In this state ADC parameter are set for number of channel to scan, data format, and channel //number*

STATE: Sampling *// In this state sampling command in given to ADC, scan result are received for from ADC and transfer to specified output channel]*

END of PROCESS
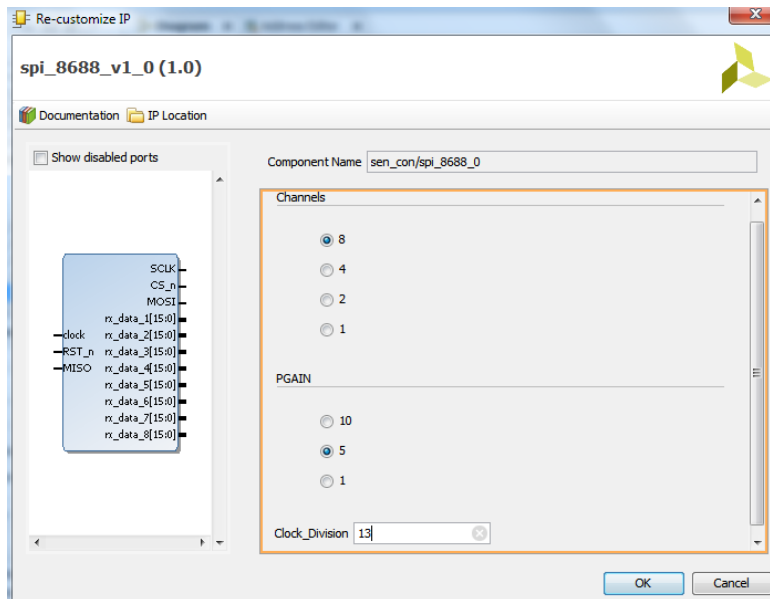
Figure 7.4 – GUI of Component IP ADC

shifted through 120° and 240° to generate three phase references. These three phase references rotate through 360° and speed of rotation reflects the output

frequency. The Active and reactive powers must be passed into droop control block from preceding power computation block.
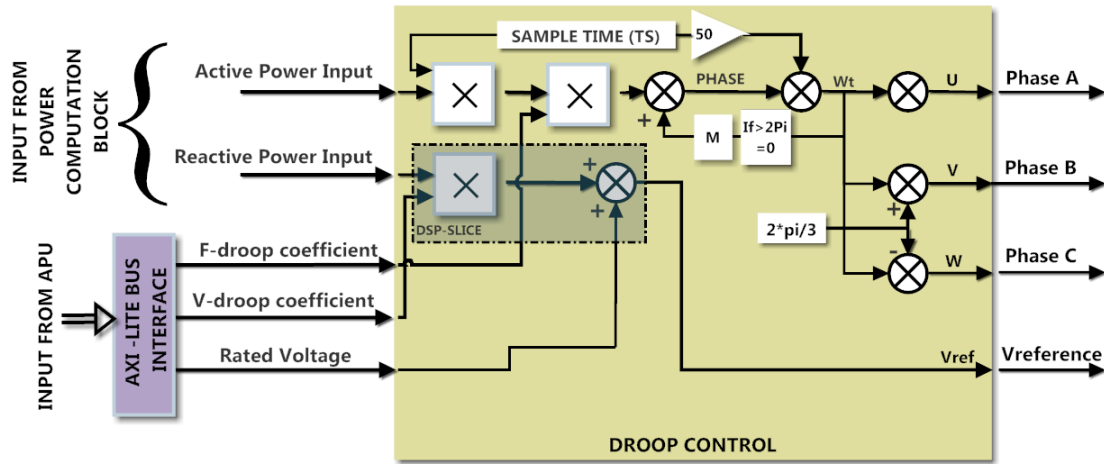
Figure 7.5 – Droop Control Design for FPGA

As per device data sheet, FPGA contain 220 numbers of DSP slices. These DSP slices can perform MAC, Multiply; addition or subtraction operation without using CLBs. Therefore, a DSP slice can be used in V-droop computation which requires only one MAC operation. This strategy will give balance uses of the all resources within FPGA.

7.4 Transformation Block

The two basic transformations, Clarke's and Park's tranformations are used in control system. Clarke's transformation ($\alpha\beta0$) used for Stationary Reference Frame and Park's transformations ($dq0$) is in Synchronous Rotating frame. Both the transformation requires set of computation using multiplication and addition as shown in Figure 7.6. These blocks can be used for multiple times within a single control. The output of these blocks is converted into 16 bit (16, 14) fixed point number.

7.5 Power Calculation and Filters

Block active and reactive power is calculated in stationary reference frame ($\alpha\beta0$). Voltage and current signals are first transformed using Clarke's transformation
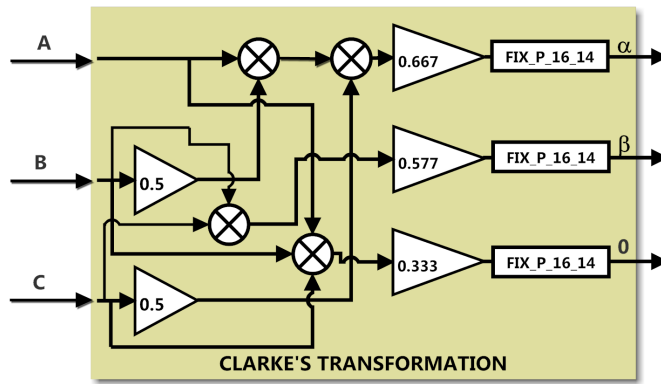
(a)
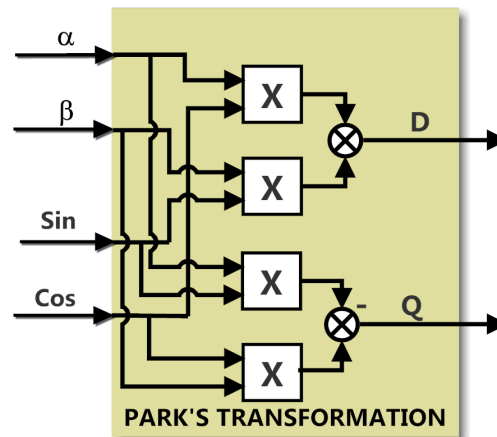
(b)

Figure 7.6 – Transforation block FPGA (3ph- 2ph)

block. Using these signal active power (P) and reactive power (Q) are simply calculated numerically and passed on to the IIR filter. In Figure 7.7 a sample signal similar to power signal is sent to IIR block and response is plotted. Output signal is almost having constant value showing good filtering performance. The filter's coefficient can be changed to any value by software implementation if desired or it can be kept fixed.

7.6   Synchronization Block

The purpose of synchronization block is to match phase of incoming VSI with the instantaneous phase of grid or VSI. The phase must be locked accurately to minimize high circulating current at the time of interconnection. The methodology must be consistent with FPGA design flow and can be implemented in optimal resources. Figure 7.8 shows the implemented synchronization block. Unit template
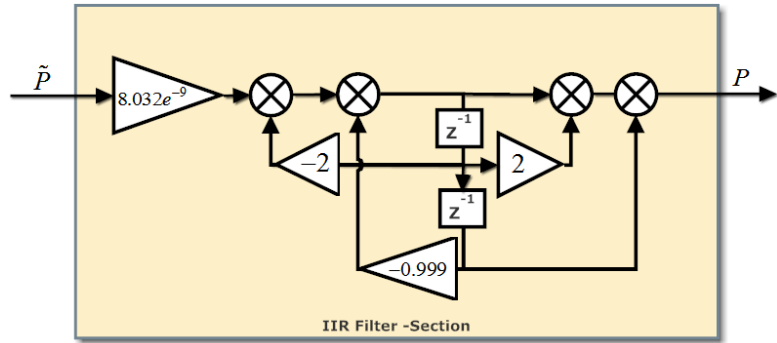
(a) (a) IIR Filter Section-1 (of 3-section filter)
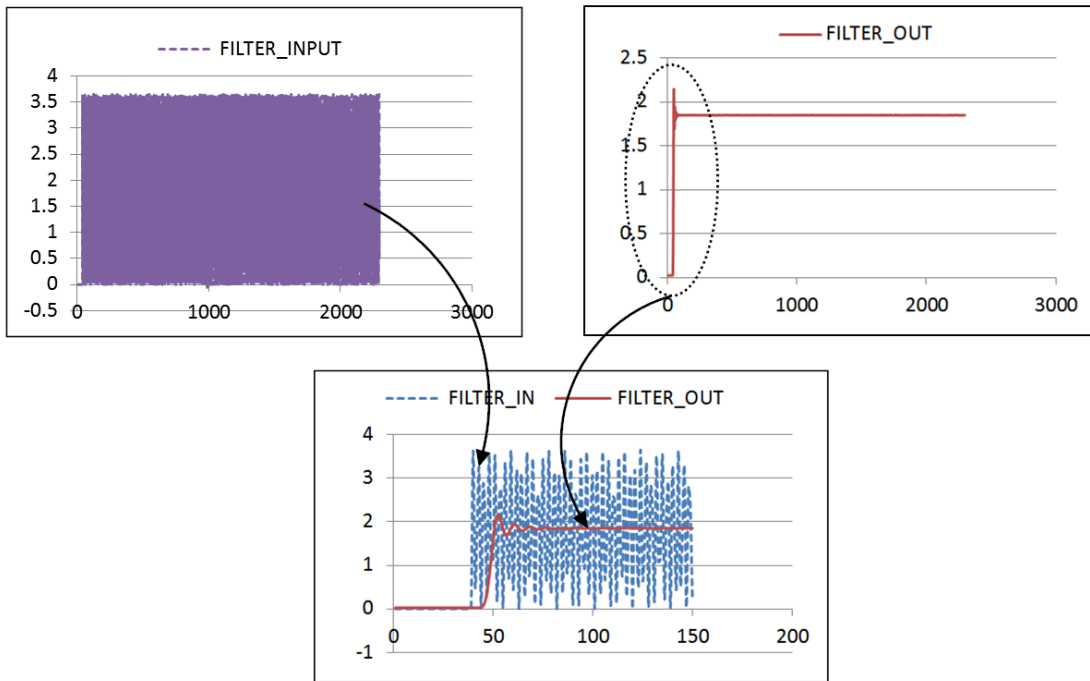
(b) (b) Filter Response

Figure 7.7 – Power filter Block

of both grid voltage and inverter's output voltage has been calculated and fed to Clarke's transformation block. Clarke transformation gives rotating direct axis and quadrature axis components of the three phase signals.

These signals are applied to park's transformation block. Where direct and quadrature components are compared to unity and zero respectively. The generated error is fed to PI controller whose output is multiplied to compute error angle for both the components. Finally, the computed sum of error's square are reduced to a set minimum value. This gives least square minimization of the error signal. Pseudo code of lock function is given in algorithm 7.2. The relay signal is generated when both the phases are stayed locked (errors are minimum) for few
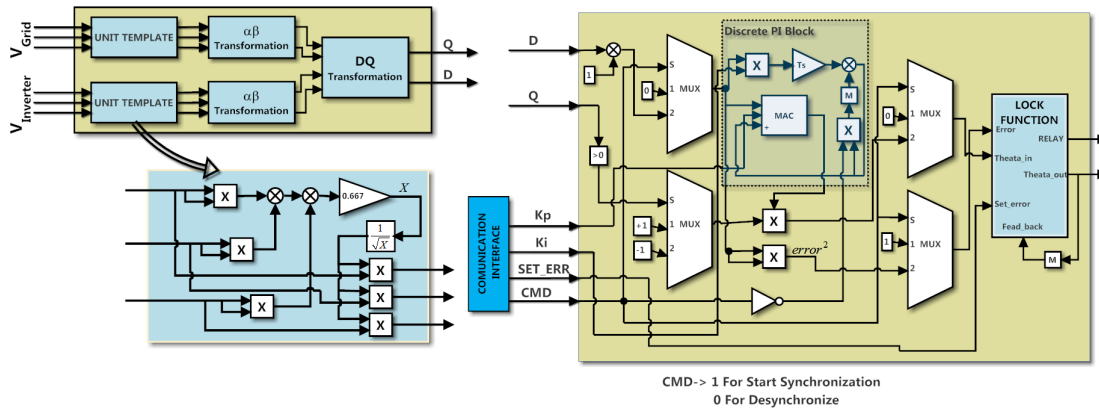
(a) (a) IIR Filter Section-1 (of 3-section filter)

Figure 7.8 – Synchronization Block

Algorithm 7.2 Pseudo Code Lock Function(VHDL

Define Library & Standards [as: ieee.std_logic_1164.all];
LOCK FUNCTION: (VHDL)
PROCESS: Define all temp variable Input (Theta_in,Feedback_Theata,Er)
Sum_er=$\sum_{100}(square.error-in-phase$
If lock=0 Out_theata=Theata_in
Else Out_theata=Feedback_theata/2
End if
If Sum_er<Set_error lock=1 *// RELAY signal can be generated any time after locking//*
End if
END of PROCESS

---

cycle. The trigger once generated is locked and released only when synchronization switch is manually cleared or overcurrent protection is activated.

7.7 Overcurrent Protection Block

In various conditions like fault, out of synchronization or any instability there is flow of overcurrent through inverters. At hardware level there may be other protections activated but protection within controller is also required. This gives us reclosing and restoration facility after clearing the fault. The block compares each fault current magnitude and relay a signal to circuit breaker to open the circuit. After breaking when current goes below the overcurrent limit circuit breaker closes its contacts to restore the circuit. This sequence is counted by an internal counter for 3-10 times and if the same continues for longer duration, the circuit will open permanently.

7.8 Three Phase Reference Voltage Generation

In FPGA, there are various implementations which can generate three phase sine reference. Various IPs can be used to perform this operation. Most simple method is to use look up table for each sine value for 360° output. Look up table can be generated only for a quarter sine wave (90°) while rest of the part can be computed. Other methods are also available and more efficient in the form of resource utilization and precision. Various numerical methods like coordinate rotational digital computer (CORDIC) algorithm or Direct Digital Synthesizer (DDS) algorithm can be used to generate more precise sine wave. DDS algorithm is based on Numerical Control Oscillator (NCO) and also uses Look Up Table. This gives advantage of producing low frequency sine wave with high frequency sampling rate. The present work uses the DDS compiler4.0 to use DDS for variable frequency output of microgrid inverter.

7.9 RC Block

The core of Repetitive Controller is combination of filters and long variable delay line. A delay is generally formed by flip-flops inside the FPGA. Each CLG/Slice of FPGA contain minimum one memory block formed by flip flop of fixed width (8 bit/16 bit). Whenever we configure a delay in HDL code it is synthesized into Flip-flops in most of the cases. Flip-flops are one of the important resources of CLG/Slice. Once a flip-flop is used for a purpose from a slice other resources of that slice cannot be utilized anymore. Further, if it is needed to produce a long delay (for e.g. 1000 samples) for some input then it is required to use high number of CLG/slices. A repetitive controller requires a delay of minimum a cycle of fundamental power frequency. It means it requires delay of 20ms for 50 Hz frequency. For a sampling frequency of 200 KHz we need to have 4000 delay in line. We require minimum of two repetitive controllers for voltage control loop and two for current control loop. It means it will require 16000 delays for four instance of RC. Again if the data size of input signal is increased slightly then same delay may require double number of the slices. Hence, it is clear that a long delay utilize heavy amount of FPGA resources and cannot be used in its
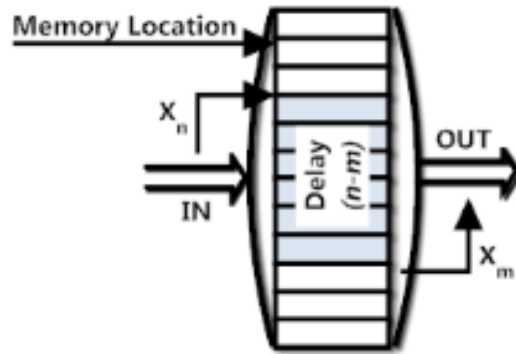
(a) Dual port Ram Structure

$$\frac{1}{1+e^{-Ts}}$$
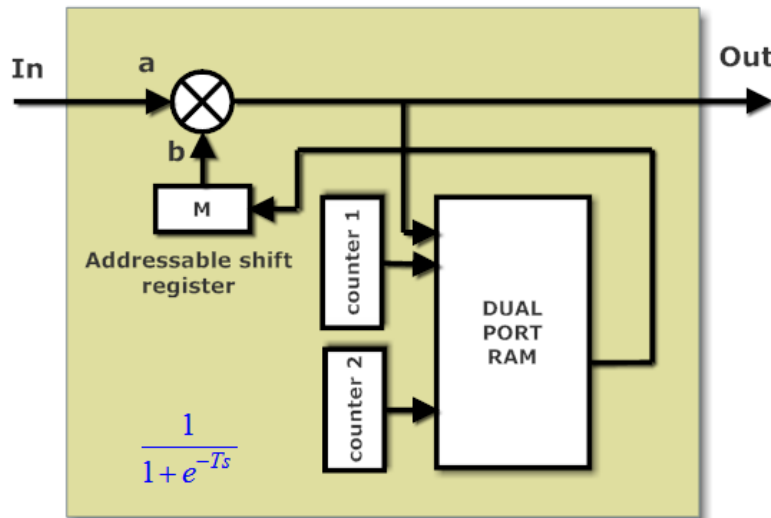
(b) Transfer function Implementation

Figure 7.9 – RC Implementation in FPGA

current form. But observing the requirement and FPGA resources we can find more optimized approach. Therefore two approaches to optimize a RC, a) Down sampling: Down-sampling and reducing sample rate will decreas the number of delay requirement significantly. For example, if we down sample the input signal by two then we need to store half number of data point to cause same time delay. However, reducing sample rate may deteriorate the performance of controller. b) Using Dual Port RAM. The second and better way is to use dual port ram to perform delay of any size. However dual port rams availability is depends on the FPGA class and manufacturer. All FPGA do not contain dual port ram. In dual port RAM data can be pushed through first port and can be taped from second port. There are two free running counters that can be initialized at different value. The counter used for this purpose having difference equal to number of sample

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required to delay as depicted in Figure 7.9(a) Transfer function with delay T can be implemented as shown in Figure 7.9(b).

7.10   PI Regulator Block

PI regulators can simply be designed using MAC and memory operation as shown already in synchronization block. The gain Ts equal to sampling time of system which is internally set. Using fix value of Ts allows us to set data type and width to certain value so that the minimum error can be integrated. However a second way is to implement PI is to compute Ts internally using timer operation.

7.11   Overclocking
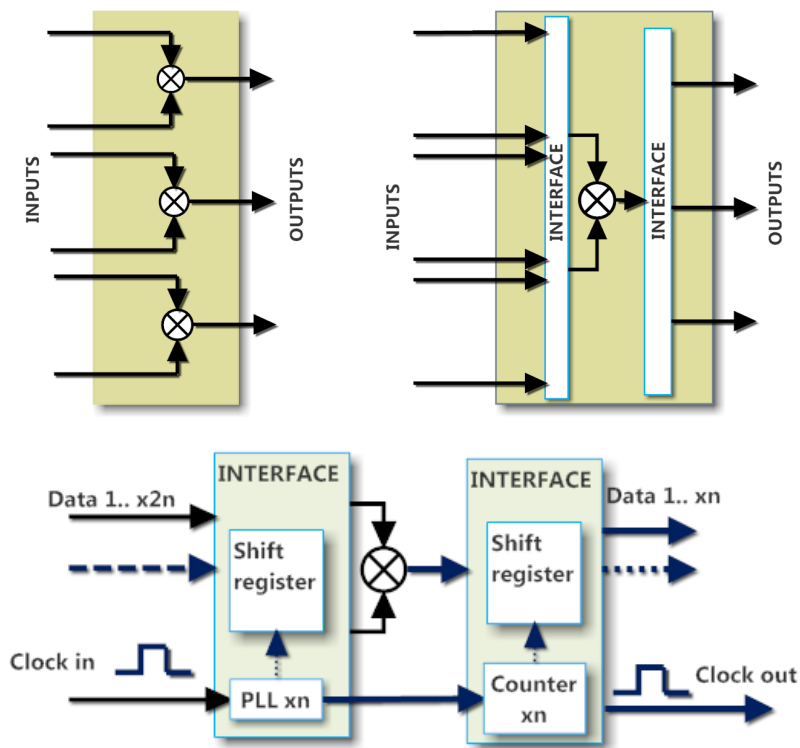
Figure 7.10 – Over clocking (a) Without Overclocking (b) With Overclocking

Once design is coded and tested in VHDL then a valid RTL can be generated in form of component. This component can be used at many times in other designs. However, increasing the instances of component consumes same amount of hardware resources each time it used in a design. For example in Figure 7.10 ,

(a)   Three different instances of summer are used to add six different quantities. This requires three times same resource which requires to build one adder. In second way if we can perform these three additions with single adder as shown in Figure 7.10 which improve the resource utilization in FPGA.

(b)   However, for an adder this may be not a problem as it requires very less resources. But for a large function or combinational logic using their multiple instances may consume large amount of resources for same purpose. For example Park and Clarke Transformation can be used many times in a design and will consume lot of FPGA resources. These transformations are purely combinational logic and do not have any memory state. In such cases we can optimize the resources by using same instance for different quantities. This can be done by poling each input at higher frequency, perform math operation for each group of inputs and transfer output at dedicated port as shown in 7.10 (b). This mechanism always provide higher functional density in FPGA.

Here two basic blocks are used with overclocking to optimize FPGA resources. Using multiplexers and counters we can use single Transformation block to perform this task. However, if there is different latency between different paths from input to output then data can be mixed or overlapped at output. The main reason of latency in any path is computation time (cycle) taken by mathematical operations in that path. Therefore, before doing such arrangement all data path latencies (delays) have to be matched. It means that any data from any input (ABC) to any output ($\alpha\beta$) travel with same time delay. This can be performed by introducing delays (D-Flip Flop) into required path. This will ensure that for any data set output will be at appropriate destination. Clock of counter and other logic will run at double frequency w.r.t. the external world to perform all operation simultaneously.

a)   **Overclocked Clarke/Parks Transform:** 3-phase Voltage and Currents signal are required to be converted into two phase $\alpha\beta$ signal using Clarke transform. Each Clarke transform requires four summers and

five constant multipliers. For the calculation of Active and Reactive power two Block of Clarke transform are required. The transformation can be performed by single transformation block by overclocking and multiplexed inputs. All paths from input to output must have same latency thus additional delay has been added to compensate the delay caused by gain block. A counter is set to count value up to 1 in auto reset mode. We can replace counter by a clock (0/1) for particular operation. One multiplexer and one de-multiplexer is used at input and output respectively. Multiplexer have two input and one selection line similarly de-multiplexer has two output and one selection line. Both selection lines are driven by same clock or counter. The internal clock is set at double of input frequency.

b)   **Overclocked PQ calculation block:** Similar to Clarke's and parks transformation computation of active and reactive power can be optimized. Active and reactive power calculation need simple numerical calculation. Therefore, for two inverter system two P & Q calculation block is required. However, for optimized system one P & Q block can be overclocked at double of the sampling frequency to compute P & Q of both the inverters.

7.12   Time Division Multiplexing
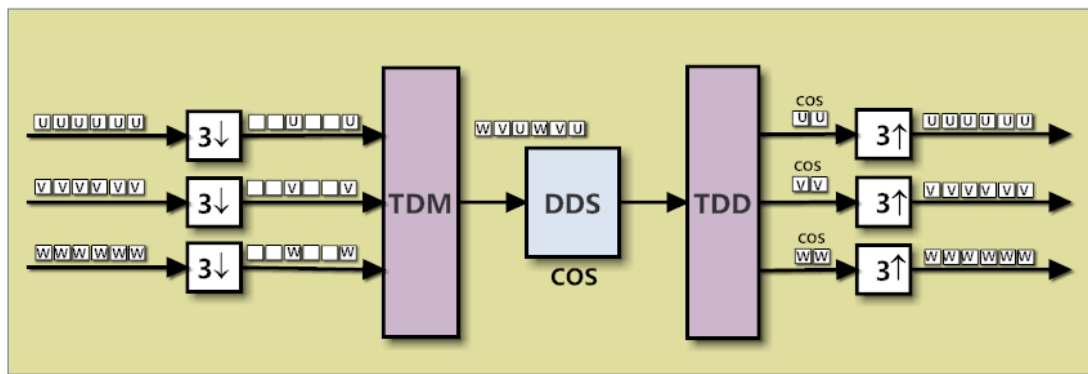
Figure 7.11 – 3-Ph generation using DDS with TDM

In another way optimization can be performed by using time division multi-

plexing (TDM). This method becomes very complex with high number of inputs but gives maximum optimization. A TDM is carefully implemented by mixing samples from two data path into one data path. There are following steps to implement this method:

a.) Match the latency of each path from input to output within component as previously done.

b.) Perform Down sampling of each input path by value equals to numbers of inputs.

c.) Merge all input using TDM.

d.) Process the data using only one instance of component

e.) De-multiplex the output using Time division De-multiplexer (TDD) f.) Perform Up-sampling (copy sample) at each output.

This procedure has loss of samples during down-sampling but does not require extra-clock speed. Sometime we can not generate higher clock speeds but we have chances to operate at lower sampling rate. Here it is important to note that up-sampling and down-sampling physically do not consume any resource in FPGA. Using this procedure one DDS block is shared among all the three phases. First the each input has been down sampled by three (3) and merged by three inputs TDM. This packs all data in single line. The data is passed to DDS block and find the cosine of each data point at output. The process is clearly described in Figure 7.11. However the samples are copied three times at output in each phase but still do not have any impact on inverters output due to very high initial sample rate. If input sample rate of sampling frequency is low then it is good to use interpolation filter at output of each phase during this process.

7.13 Fixed Point Computation

Any data in digital domain is presented or known by two parameters i.e. data width (in bit or byte) and data type (representation method). FPGA resource use is mainly dependent of these parameters. Higher data width always increases the use of FPGA resources (registers, logic gates etc.) while processing time or latency sometimes depend upon data type. For an example the multiplication

of two 32-bit floating point numbers required more resources w.r.t. 32-bit fixed point numbers. However the accuracy of results increase many fold and remains bounded in floating point numbers at same data width while in fixed point numbers accuracy varies at different values. Two basic fixed point numbers namely Q15 and Q16 are widely used to represent fixed point data. A brief description with example in Table 7.2 is given below:

a)   **Q15 Numbers:** These numbers have 16 bit data width. The value presented by the numbers lies between -1 to 1. The radix point is immediate after sign bit. This gives 15bit of fractional value. The maximum resolution by this data type will be $1/215 = 3.0518\text{e-}5$. This data type is suitable for storing the value of filter coefficient, sine and cosine functions.

Table 7.2 – Example of Q15 &Q16 Fixed point number

Sign bit	Fractional Bit														
1	0	1	1	0	1	1	1	0	1	1	0	1	1	0	0

(a) _Q15 Number , Radix at 15th bit, Decimal Value: -0.567

Sign bit	Integer bits														
0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
	Fractional Bit														
0	1	0	0	1	0	0	0	1	0	1	0	1	1	1	1

(b) Q16 Number , Radix at 16th bit, Decimal Value: 56.56787

b)   **Q16 Numbers:** Conversion of value can be performed by MATLAB functions conversion (num2bin() and bin2num()). Q16 fixed point numbers are presented in 32 bit wide field having 16 bit for fractional number, 15 bit for real number and 1 bit for sign.

7.14   Programing Soft Core (Software Development)

There are two general purpose ARM application processors included in ZYNQ FPGA-SOC. This processor's I/O can be routed to programmable logic core via

programmable antifuse. AMBA© ARM AXI bus interface is most reliable method to communicate between processor core and logic core. Each function of droop controller is designed in the form of IP-component block. The input/output of the each block are memory mapped into the APU using AXI interface. Therefore an external program running into processor unit can communicate with PL unit during runtime. For example, if we design an IIR filter of a particular order, then we need to provide coefficients to the filter structure. These coefficients can be initialized into PL logic and can be changed by APU using soft programing at run time. This is one of the best way to change dynamics of the system during runtime. In this work soft core is programmed in C/C++ language using GNU C compiler in Xilinx SDK. In appendix-C code program in C is given to intitlalize, PI based two inverter microgrid for reference.

7.15 Conclusion

In this work, the whole control system is programed in FPGA that runs at the base sample rate (clock) of 200 khz, which is very high sampling frequency with respect to conventional DSP system. This provides flexiblity to perform parallel processing and use of multiple clock rate within single system. Besides this, Application Processor Unit (APU) can be directly interfaced with FPGA hardware logic. This gives oppurtunity to use high level language like C/C++ to perform complex computation like matrix manupulation (L_1controller) in control system. All these features has presented good advantage over conventional DSP controllers.

CHAPTER 8

CONCLUSION & FUTURE WORK

In microgrids, voltage sources inverters (VSIs) can be interfaced in centrally coordinated way to share power among them. Implementation of this coordinated approach requires high bandwidth communication network. But providing a high communication network to the microgrid is not technically viable and economically affordable. So this research is mainly focused on communication independent primary control of microgrid. Various proposed controllers are designed to mitigate different problems in microgrid. In this work, wide variety of operating conditions under different operating modes has been tested and discussed. Further, It is found that power sharing without high bandwidth communication link is the not only concern, but at the same time, depending on loading pattern; the issues of power quality (Harmonics and Unbalance) and stability are also very serious problems. These problems have also been addressed and discussed under primary control of Microgrid.

A microgrid can be formed by minimum of two interconnected inverter source-shaving power sharing capability and one common load. Therefore, the hardware prototype of microgrid has been build using two interconnected VSIs that can work under various modes of operation. The VSIs are designed by using IGBT switches in 3-phase 2-level configuration. The VSIs operate on high frequency PWM, so a proper LC-filter has also been designed. Hardware and software protection schemes has been implemented to VSIs, to protect them against short circuit and shot through fault.

Further, in this work the basic operations of microgrid in grid tied and islanded mode have been discussed. These modes of operation play a pivotal role in en-

ergy management, contingency management and reliability of microgrid. Islanded mode of operation has two main operations as, black start, accurate power sharing. During black start when all sources are operating in isolation and to form a microgrid, each source must be synchronized to the common network without violating source limits. Once all sources have been added to microgrid, then power sharing among these source is required. Accurate power sharing among all sources has been achieved through implementation of droop control in synchronous reference frame theory (SRF). Moreover, in this work various aspects of microgrid control with modelling and simulation have been discussed. Due to the limitation of time window and requirement of multiple controllers it is the real time results have not been provided. However, a different aspect of PV system integration in microgrid has been discussed.

In advance stage of this research work, a high bandwidth repetitive controller is designed to replace conventional PI controller from inner loop of VSI control. This controller is designed, simulated and implemented in real world hardware using FPGA. In addition to this, controllers are compared with conventional PI and PR controller. Further, to mitigate the effect of unbalance loading on source voltage, add-on repetitive controller has been designed. The designed controller can be added to parallel to existing PI controller and can improve bandwidth significantly. It was shown that the add-on Repetitive controller is successful to minimize the impact of non-linear unbalance load on system voltage profile. The voltage THD level has been kept to almost 4% despite of non-linear load having THD level of 36%. Moreover, the system voltage remains perfectly balanced irrespective of sudden loss of one phase under heavily loaded conditions. Further, the proposed controller outperforms the conventional controllers that even with lesser hardware resources.

In last, the major problem of microgrid stability in droop control mode is discussed. It is known that microgrid stability is dependent of network parameters i.e. transmission line resistance and inductance. Hence, a novel method has been used to stabilize VSIs based microgrid by incorporating L1 adaptive droop control under large variation in R/X ratio of the transmission line. The presented methodology has successfully handled the large variation in network parameter

along with variable droop characteristics without losing stability. This strategy uses the generalized averaging method to model the inverter operation in islanded microgrid. The controller has been so designed that the same controller can be used for any number of inverters. Moreover, it has been explained that with the increase in number of sources, the stability of microgrid also increases.

Operating a microgrid with parallel operation of various interfacing converters fed with different DRs in real world condition is still a big technical challenge. It requires rapid technical development to provide commercially viable solutions to the community in near future. The seamless transfer within different operational modes is most potential and challenging task for future work. Surely the microgrids are full of opportunities in terms of socio-economic, environmental and commercial benefits but with technical challenges.

Appendices

APPENDIX A

SYSTEM PARAMETERS AND TRANSFORMATIONS

A.1 SYSTEM PARAMETERS

Table A.1

Parameters	INV-I	INV-II
DC –voltages	160 V	158 V
PWM frequency	5 KHz	6 KHz
Filter Inductance and ESR	2.2 mH,0.1 Ω	1.8 mH,0.1 Ω
Filter capacitance	25 μF	25 μF
Nominal Frequency	50 Hz	50 Hz
Nominal AC voltage*	54 V	54 V
Transmission line Inductance and Resistance	1.2 mH, 0.2 Ω	1.5 mH, 0.2 Ω
Droop coefficient frequency (m_f)	1.0 Hz/1Kw	1.0 Hz/1Kw
Droop coefficient voltage (m_e)	2V/QKVar*	2V/QKVar*
Power filter cut-off frequency (ω_c)	15 rad/sec	15 rad/sec
Non-linear Load, Gain K	Resistance=22 Ω (Cold) , Inductance=120 mH , 7.5	
Kpv & Kiv (PI V- controller)	0.40 / 186	0.42 / 184
Kpc & Kic (PI current controller)	0.30 / 67	0.34 / 73

A.2 REFERENCE FRAME THEORY

A.2.1 $dq0$ Transformation

Transformation: The transform (often called the Park transform) is a space vector transformation of three phase time-domain signals from a stationary phase

Table A.2

Parameters	INV-I	INV-II
DC –voltages	168 V	165 V
PWM frequency	5 KHz	6 KHz
Filter Inductance and ESR	2.2 mH, 0.1 Ω	1.8 mH,0.1 Ω
Filter capacitance	25 μF, 1.0 Ω	25 μF, 1.0 Ω
Nominal Frequency	50 Hz	50 Hz
Nominal AC voltage*	54	54
Transmission line Inductance and Resistance	Lmin=1 mH, Rmin =0.1 Ω Lmax=3.0 mH, Rmax =2.2 Ω	
Droop coefficient frequency (m_f)	0.1-1.0 Hz/Kw	0.1-1.0 Hz/Kw
Droop coefficient voltage (m_e)	2.0 V/KVA_r	2.0 V/KVA_r
Power filter cut-off frequency (ω_c)	30 rad/sec	30 rad/sec
Band Pass Filter Cut-off frequency (BPF)	1.0 -12.0 rad/sec	1.0 -12.0 rad/sec

coordinate system (ABC) to a rotating coordinate system ($dq0$). The transform applied to time-domain voltages in the natural frame (i.e. v_a, v_b, v_c) is as follows:

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - {}^{2\pi}/_3) & \cos(\theta + {}^{2\pi}/_3) \\ \sin(\theta) & \sin(\theta - {}^{2\pi}/_3) & \sin(\theta + {}^{2\pi}/_3) \\ {}^1/_2 & {}^1/_2 & {}^1/_2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad \text{(A.2.1)}$$

Where $\theta = \omega t + \delta$ the angle between the rotating and fixed coordinate system at each is time t and δ is an initial phase shift of the voltage. The inverse transformation from the dq_0 frame to the natural abc frame:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta - {}^{2\pi}/_3) & \sin(\theta - {}^{2\pi}/_3) & 1 \\ \cos(\theta + {}^{2\pi}/_3) & \sin(\theta + {}^{2\pi}/_3) & 1 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \quad \text{(A.2.2)}$$

It can be observed that since the synchronous frame is aligned to rotate with the voltage, the d-component corresponds to the magnitude of the voltage and the q-component is zero. Figure A.1 shows a balance three phase input vector where Figure A.2shows corresponding d-q transform output.
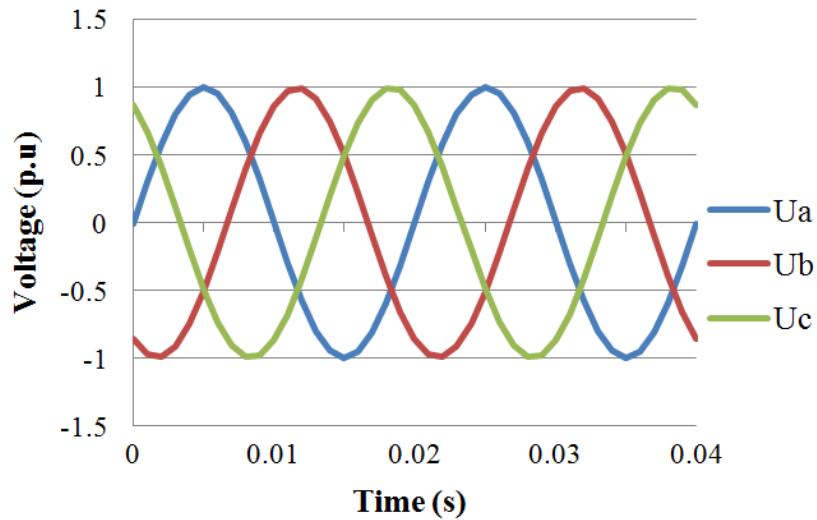
Figure A.1 – 3-phase AC source waveform
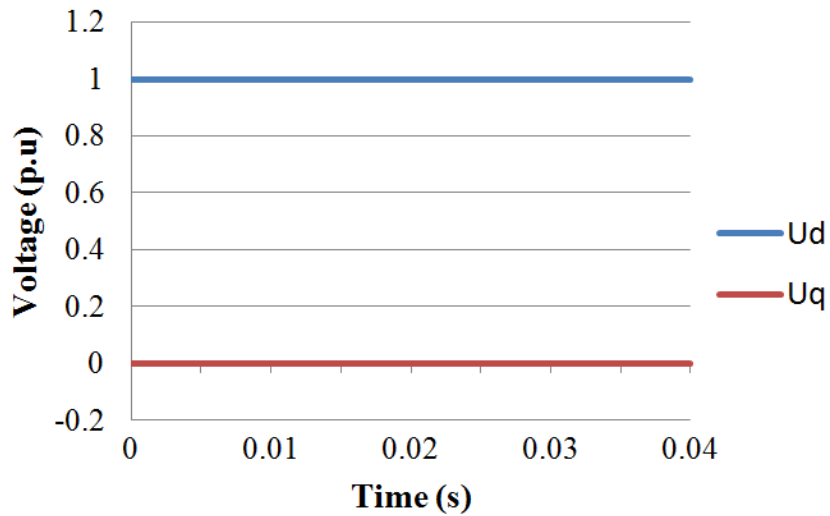
Figure A.2 – Output waveform after dq_0 transformation

A.2.2 $\alpha\beta0$ **Transformation**

The Clarke or $\alpha\beta0$ transform is a space vector transformation of time-domain signals (e.g. voltage, current, flux, etc) from a natural three-phase coordinate system (ABC) into a stationary two-phase reference frame $\alpha\beta0$. It is named after electrical engineer Edith Clarke. By this transformation, Three-phase voltages varying in time along the axes a, b, and c, can be algebraically transformed into two-phase voltages, varying in time along the axes α and β by the following transformation matrix:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \qquad (A.2.3)$$

Figure A.3 shows the Clarke transformation of thee phase balance vector shown in Figure-A.1 . Similarly the Inverse Clark transform will be,
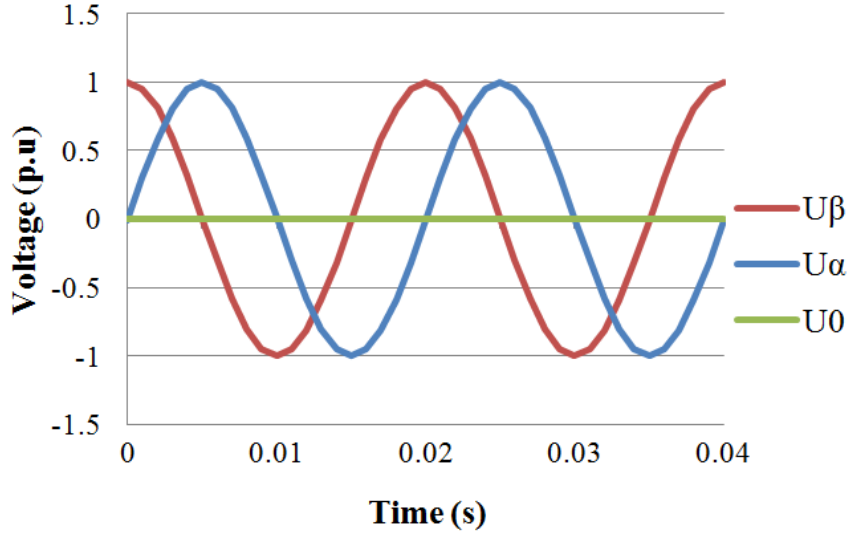
Figure A.3 – Output of waveform of $\alpha\beta$ transformation

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3/2} & 1 \\ -1/2 & -\sqrt{3/2} & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} \qquad (A.2.4)$$

It is important to note that the 0-component in the Clarke transform is the same as the zero sequence components in the symmetrical components transform.

A.2.3 Instantaneous Power Calculation

In the conventional method, we use a voltage phasor and conjugate of current phasor to calculate the complex power $'s'$ which is valid only in steady-state condition. But in this method, instantaneous complex power is calculated by instantaneous vectors of v' and i, which is defined as the product of voltage vector e and conjugate of current vector , given by the following equation:

$$s = e.i^* = (v_\alpha + jv_\beta)(i_\alpha - ji_\beta) \qquad (A.2.5)$$

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$$p + jq = (v_\alpha i_\alpha + v_\beta i_\beta) + j(v_\beta i_\alpha - v_\alpha i_\beta) \qquad \text{(A.2.6)}$$

The above equation can be applied for both steady-state conditions and transient conditions. In matrix form,

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \qquad \text{(A.2.7)}$$

COMPUTATION OF L_1 NORM

B.1 L_P Spaces

The L_p spaces are the function spaces that can be define by p-norm for finite vector spaces. This is named after great mathematician Henri L. Lebesgue. The most general Lebesgue space are L_1, L_2 & L_∞ for P=1,2 and ∞. L_∞ spaces are the basically normed vector spaces. The function space f in L_p spaces are normed by p-can be described as:

$$\|f\|_{L_p} = \left(\int_{\mathbb{Z}} |f(x)|\, dx \right)^{1/p} \tag{B.1.1}$$

For discrete system $f = \{a_n\}_{n \in \mathbb{Z}}$,

$$\|f\|_{L_p} = \left(\sum_{n=-\infty}^{\infty} |a_n|^p \right)^{1/p} \tag{B.1.2}$$

B.2   Computation of L_1–Norm

The performance and robustness of the linear dynamical system can be measured by system norms. Out of infinite number of norms, most important are the H∞-, H2-, and L1-norms. Therefore, various algorithms have been used in literature to compute these three norms. The H2-norm is easiest to compute using appropriate computing Lyapunov equations. The H∞-norm can be determined by analyzing the eigenvalues of an associated Hamiltonian matrix of system, and a careful implementation of corresponding algorithms works fine in most cases.

In case of L1 norm various methods has been used to compute of LTI system.

For SISO system:

$$G: \quad \dot{X} = AX + BU$$
$$Y = CX \tag{B.2.1}$$

L1 norm is given by :

$$\|G\|_1 = \int\limits_0^\infty \left| Ce^{At}B \right| dt \tag{B.2.2}$$

To compute an estimate of the L1-norm, the impulse response of LTI system numerically integrate over a finite interval, where the discrete function values are obtained by simulating the differential equation. However, the faster algorithms for higher order system are also available like Rauland and Lane algorithm. These algorithms are fast and provide good accuracy within a given tolerance. In these algorithms upper and lower bounds are computed in iteration until calculated value converges to within given error tolerance limits. In this thesis computed the L1 norm by conventionally by numerical integration of impulse response in matlab. The algorithm is given bellow:

Algorithm B.1 Computation of L1-norm using impulse response
***
Start: Input: A,B,C,D Matrix of system in State –space.
Step-1: Compute number of Column(C) in Matrix B.
Step-2: Compute number of Row(R) in Matrix C.
Step-3: Create matrix 'G_s' with R-rows and C- column.
Step-4: Create system 'G_s' equal to $C * (Is - A)^{-1} + D$
Step-5: Compute Impulse Response using matlab function 'impulse' (Gs) and save time series in Y:T.
Step-6: Run loop for C time, R times for G= $\sum\limits_{i=1}^{C}\sum\limits_{j=1}^{R} |Y_{ij}| . \Delta T_{ij}$

Step-7: Compute L1 Norm i.e. L1= max(G)
End

Example-1: L1-norm computation:

$$A = \begin{bmatrix} 0 & 1 & 0 & 0 \\ -2 & -2 & 1 & 1 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & -1 & -1 \end{bmatrix}, B = \begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix}, C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{B.2.3}$$

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Computing norm using impulse response,

$$G = \begin{bmatrix} 1.8112 & 2.3121 \\ 2.3121 & 4.1233 \end{bmatrix} \tag{B.2.4}$$

Hence, L1 norm=max (1.8112+2.3121, 2.3121+4.1233) =6.4354

Example-2: SISO system:

$$A = \begin{bmatrix} -0.2 & -1 & 0 \\ 1 & 0 & 0 \\ -1 & 1 & -1 \end{bmatrix}, B = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}, C = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \tag{B.2.5}$$

computing $\|G\|_1 = \int_0^\infty |Ce^{At}B| \, dt$ gives

G=6.4660 with (Y=622 sample,)

Hence, L1 Norm=6.4660;

And by using Rauland & Lane's algorithm with Error Tolerance=1e-4, Iteration max=10;

L1 Norm=6.4660;

B.3 Computation for L_1–Controller Parameters

For given system variation matrix can be calculated by computing the difference between minimum and maximum value of state-transition matrix with variation in different parameter. For two inverter system this is calculated in Matlab and written bellow:

$$\Theta = \begin{bmatrix} 0 & 0 & 615.49 & 0 & 0 \\ -564678.24 & -1326.53 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -0.0056 \\ & & -564678.24 & -1326.53 & 0 \\ & & & & 615.49 \end{bmatrix} \tag{B.3.1}$$

The calculated L1 norm of this matrix will be,

L_n=8.659372516942356e+05;

Now Computing the L1 norm for all transfer function representing whole system,

$$G_s = C * (sI - A)^{-1}B \qquad \text{(B.3.2)}$$

From all input to output is

$$I/O = \begin{bmatrix} 23.51 & 5.96e^{-9} \\ 0.36 & 1.24 \end{bmatrix} \qquad \text{(B.3.3)}$$

Selecting first order filter cut off frequency such that;

$$Gs * (I - Cs) * L_n < 1 \qquad \text{(B.3.4)}$$

Where, Cs is low pass filter with Cs (0) =1, therefore simply can be taken of the form of $\omega/s+\omega$

Hence, with iterative calculation for various cut-off frequencies we get

$$Cs = \begin{bmatrix} \frac{10^6}{s+10^6} & \frac{10^2}{s+10^2} \\ \frac{10^9}{s+10^9} & \frac{10^9}{s+10^9} \end{bmatrix} \qquad \text{(B.3.5)}$$

This gives

$$\lambda \triangleq 0.87 < 1 \qquad \text{(B.3.6)}$$

Now predictor can be calculated by solving lyapnov equation for A_n i.e. $A_nP + PA_n = -Q$.

Where Q is positive definite matrix as $Q = diag[10, 1, 1, 1, 10]$

By solving lyapnov equation the value of P is

$$P = \begin{bmatrix} 0.0112 & -5.00 & -1.47e-05 & 0.0096 & -6.33e-07 \\ -5.00 & 2832.89 & 0.0062 & -4.48 & 0.00047 \\ -1.48e-05 & 0.0064 & 0.00112 & -0.500 & -5.57e-06 \\ 0.00968 & -4.48 & -0.500 & 283.27 & 0.00314 \\ -6.33e-07 & 0.00048 & -5.57e-06 & 0.00314 & 0.500 \end{bmatrix} \qquad \text{(B.3.7)}$$

SYSTEM DIAGRAMS & SOURCE CODE

C.1   FPGA UTTILIZATION REPORTS

In the Synthesis and Implementation stage, the inbuilt design software computes the amount of FPGA resources that are utilized for the successful implementation of system in the FPGA device. If the value these resource is higher then available resources in a perticular FPGA device then software generates the error report.So to accomodate the program within available FPGA resources control progrms are coded most efficiently. Here, the whole control system for microgrid is implemented in FPGA using PI or RC based controllers. These FPGA resource utilization report for both system is attached here for references. The schematic using VIVADO^{TM} is also attached herewith.

```
Utilization Report of PI Control based System

Utilization Design Information

Table of Contents
-----------------
1. Slice Logic
1.1 Summary of Registers by Type
2. Memory
3. DSP
4. IO and GT Specific
5. Clocking

1. Slice Logic
--------------


+---------------------------+-------+-------+-----------+-------+
|         Site Type         |  Used | Fixed | Available | Util% |
+---------------------------+-------+-------+-----------+-------+
| Slice LUTs*               | 38846 |     0 |     53200 | 73.01 |
|   LUT as Logic            | 37007 |     0 |     53200 | 69.56 |
|   LUT as Memory           |  1839 |     0 |     17400 | 10.56 |
|     LUT as Distributed RAM|   816 |     0 |           |       |
|     LUT as Shift Register |  1023 |     0 |           |       |
| Slice Registers           | 24746 |     0 |    106400 | 23.25 |
|   Register as Flip Flop   | 24746 |     0 |    106400 | 23.25 |
|   Register as Latch       |     0 |     0 |    106400 |  0.00 |
| F7 Muxes                  |    65 |     0 |     26600 |  0.24 |
| F8 Muxes                  |    15 |     0 |     13300 |  0.11 |
+---------------------------+-------+-------+-----------+-------+
* Warning! The Final LUT count, after physical optimizations and full implementation, is
typically lower. Run opt_design after synthesis, if not already completed, for a more realistic
count.


1.1 Summary of Registers by Type
--------------------------------


+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 974   |          Yes |           - |          Set |
| 3752  |          Yes |           - |        Reset |
| 1246  |          Yes |         Set |            - |
| 18774 |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+


2. Memory
---------


+-------------------+------+-------+-----------+-------+
|     Site Type     | Used | Fixed | Available | Util% |
+-------------------+------+-------+-----------+-------+
| Block RAM Tile    |   24 |     0 |       140 | 17.14 |
|   RAMB36/FIFO*    |   14 |     0 |       140 | 10.00 |
|     RAMB36E1 only |   14 |       |           |       |
|   RAMB18          |   20 |     0 |       280 |  7.14 |
|     RAMB18E1 only |   20 |       |           |       |
+-------------------+------+-------+-----------+-------+
```

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate
only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile
can still accommodate a RAMB18E1

3. DSP

```
+----------------+------+-------+-----------+--------+
|   Site Type    | Used | Fixed | Available | Util%  |
+----------------+------+-------+-----------+--------+
| DSPs           |  220 |     0 |       220 | 100.00 |
|   DSP48E1 only |  220 |       |           |        |
+----------------+------+-------+-----------+--------+
```


4. IO and GT Specific

```
+----------------------------+------+-------+-----------+-------+
|          Site Type         | Used | Fixed | Available | Util% |
+----------------------------+------+-------+-----------+-------+
| Bonded IOB                 |   22 |     0 |       200 | 11.00 |
| Bonded IPADs               |    0 |     0 |         2 |  0.00 |
| Bonded IOPADs              |   57 |     0 |       130 | 43.84 |
| PHY_CONTROL                |    0 |     0 |         4 |  0.00 |
| PHASER_REF                 |    0 |     0 |         4 |  0.00 |
| OUT_FIFO                   |    0 |     0 |        16 |  0.00 |
| IN_FIFO                    |    0 |     0 |        16 |  0.00 |
| IDELAYCTRL                 |    0 |     0 |         4 |  0.00 |
| IBUFGDS                    |    0 |     0 |       192 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY  |    0 |     0 |        16 |  0.00 |
| PHASER_IN/PHASER_IN_PHY    |    0 |     0 |        16 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |   0 |     0 |       200 |  0.00 |
| ILOGIC                     |    0 |     0 |       200 |  0.00 |
| OLOGIC                     |    0 |     0 |       200 |  0.00 |
+----------------------------+------+-------+-----------+-------+
```


5. Clocking

```
+------------+------+-------+-----------+-------+
| Site Type  | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    2 |     0 |        32 |  6.25 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |        72 |  0.00 |
| BUFR       |    0 |     0 |        16 |  0.00 |
+------------+------+-------+-----------+-------+
```

Utilization Report of Repetitive Control based System

Utilization Design Information

Table of Contents
----

1. Slice Logic

```
+----------------------------+-------+-------+-----------+-------+
|          Site Type         |  Used | Fixed | Available | Util% |
+----------------------------+-------+-------+-----------+-------+
| Slice LUTs*                | 42843 |     0 |     53200 | 80.53 |
|   LUT as Logic             | 36380 |     0 |     53200 | 68.38 |
|   LUT as Memory            |  6463 |     0 |     17400 | 37.14 |
|     LUT as Distributed RAM |   612 |     0 |           |       |
|     LUT as Shift Register  |  5851 |     0 |           |       |
| Slice Registers            | 18447 |     0 |    106400 | 17.33 |
|   Register as Flip Flop    | 18447 |     0 |    106400 | 17.33 |
|   Register as Latch        |     0 |     0 |    106400 |  0.00 |
| F7 Muxes                   |  2659 |     0 |     26600 |  9.99 |
| F8 Muxes                   |  1298 |     0 |     13300 |  9.75 |
+----------------------------+-------+-------+-----------+-------+
```
* Warning! The Final LUT count, after physical optimizations and full implementation, is
typically lower. Run opt_design after synthesis, if not already completed, for a more realistic
count.

1.1 Summary of Registers by Type

```
+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 731   |          Yes |           - |          Set |
| 2861  |          Yes |           - |        Reset |
| 1363  |          Yes |         Set |            - |
| 13492 |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+
```


2. Memory

```
+-------------------+------+-------+-----------+-------+
|     Site Type     | Used | Fixed | Available | Util% |
+-------------------+------+-------+-----------+-------+
| Block RAM Tile    |  118 |     0 |       140 | 84.28 |
|   RAMB36/FIFO*    |   94 |     0 |       140 | 67.14 |
|     RAMB36E1 only |   94 |       |           |       |
|   RAMB18          |   48 |     0 |       280 | 17.14 |
|     RAMB18E1 only |   48 |       |           |       |
+-------------------+------+-------+-----------+-------+
```

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate
only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile
can still accommodate a RAMB18E1

3. DSP

```
+----------------+------+-------+-----------+-------+
|   Site Type    | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
| DSPs           |  190 |     0 |       220 | 86.36 |
|   DSP48E1 only |  190 |       |           |       |
+----------------+------+-------+-----------+-------+
```


4. IO and GT Specific

```
+----------------------------+------+-------+-----------+-------+
|          Site Type         | Used | Fixed | Available | Util% |
+----------------------------+------+-------+-----------+-------+
| Bonded IOB                 |   22 |     0 |       200 | 11.00 |
| Bonded IPADs               |    0 |     0 |         2 |  0.00 |
| Bonded IOPADs              |   57 |     0 |       130 | 43.84 |
| PHY_CONTROL                |    0 |     0 |         4 |  0.00 |
| PHASER_REF                 |    0 |     0 |         4 |  0.00 |
| OUT_FIFO                   |    0 |     0 |        16 |  0.00 |
| IN_FIFO                    |    0 |     0 |        16 |  0.00 |
| IDELAYCTRL                 |    0 |     0 |         4 |  0.00 |
| IBUFGDS                    |    0 |     0 |       192 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY  |    0 |     0 |        16 |  0.00 |
| PHASER_IN/PHASER_IN_PHY    |    0 |     0 |        16 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY|    0 |     0 |       200 |  0.00 |
| ILOGIC                     |    0 |     0 |       200 |  0.00 |
| OLOGIC                     |    0 |     0 |       200 |  0.00 |
+----------------------------+------+-------+-----------+-------+
```


5. Clocking

```
+------------+------+-------+-----------+-------+
| Site Type  | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL   |    2 |     0 |        32 |  6.25 |
| BUFIO      |    0 |     0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |        72 |  0.00 |
| BUFR       |    0 |     0 |        16 |  0.00 |
+------------+------+-------+-----------+-------+
```

C.2 HARDWARE PICTURES AND DESCRIPTION
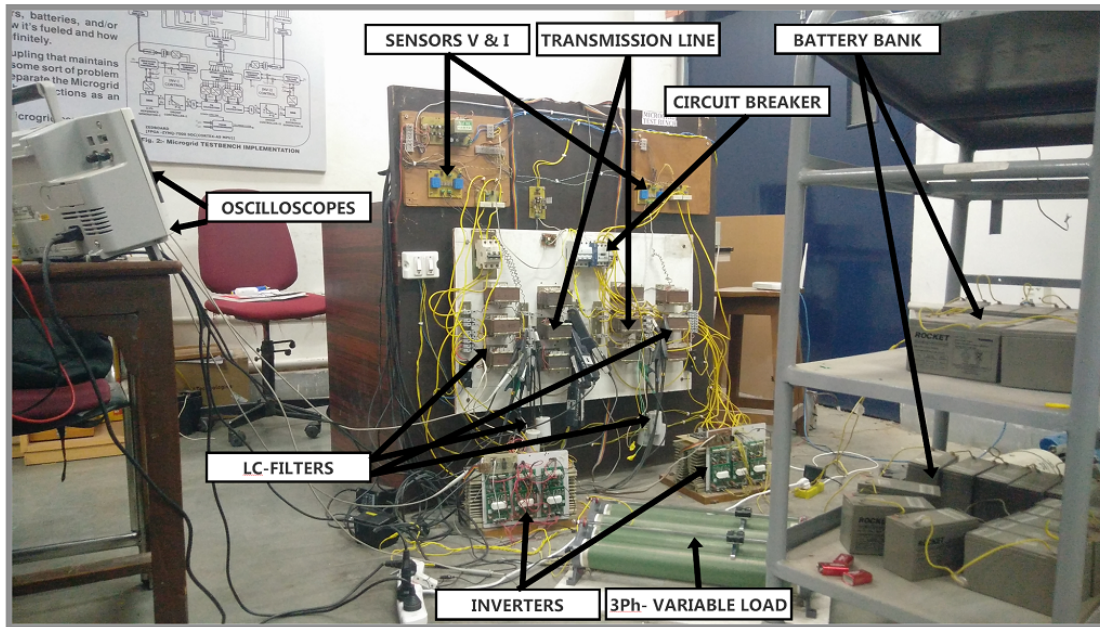
Figure C.1 – Complete Hardware Setup
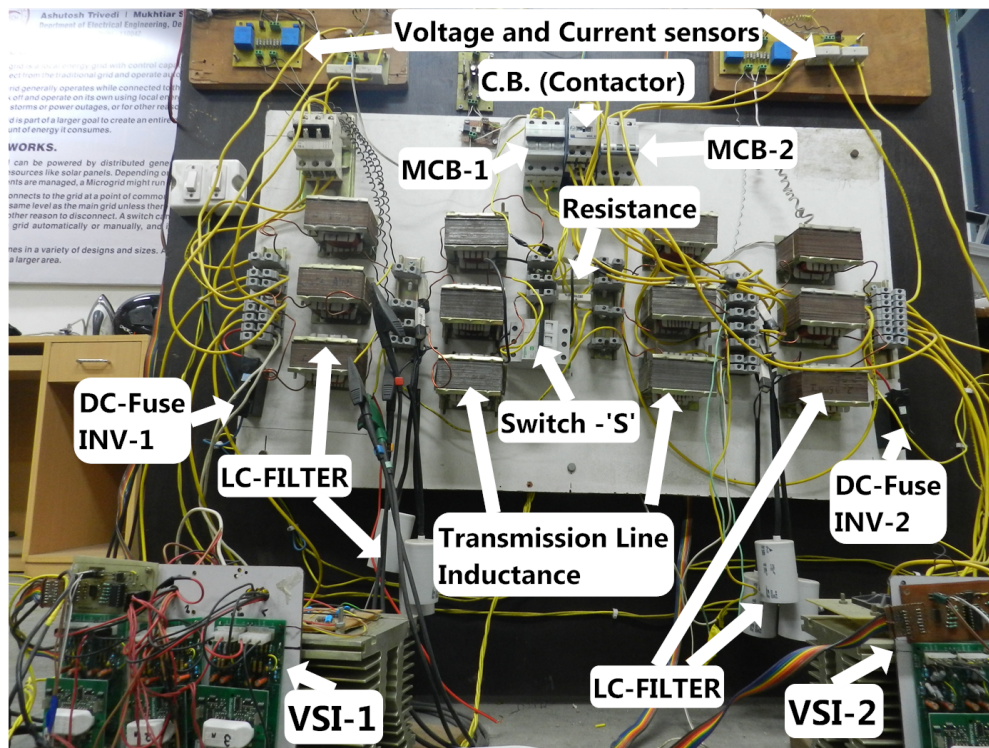
Figure C.2 – Hardware Description
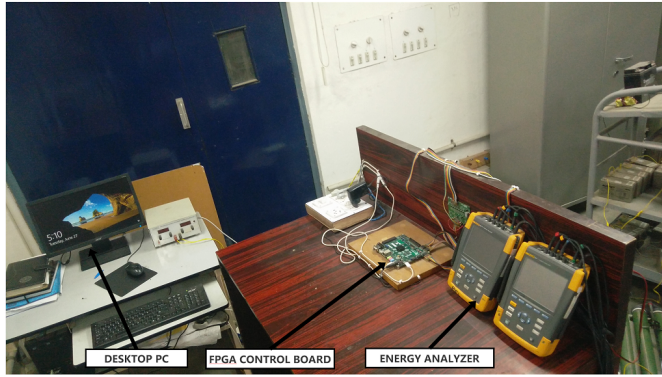
(a) Controller's desk
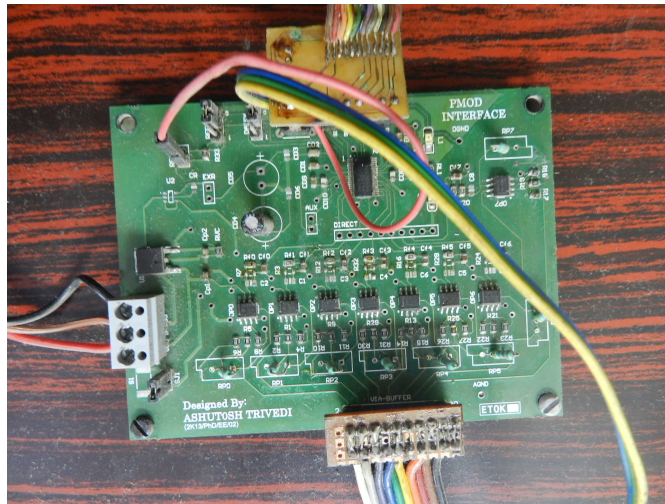
(b) Analoge Front End

Figure C.3 – Setup Component

C-3: SOFTWARE IN C
```
-----C-Source Code for run time configuration of parameters------

#include "xparameters.h"    /* EDK generated parameters */
#include "xgpio.h"
//#include "xspips.h"        /* SPI device driver */
#include "xscugic.h"         /* Interrupt controller device driver
*/
#include "xil_exception.h"
#include "xil_io.h"
#include "system_pi.h"
#include "vcloop_pi_f.h"
#include "xuartps.h"
#include "stdio.h"

#define DEVICE_ID_0 XPAR_AXI_GPIO_0_DEVICE_ID
#define DEVICE_ID_1 XPAR_AXI_GPIO_1_DEVICE_ID
#define DEVICE_ID_2 XPAR_AXI_GPIO_2_DEVICE_ID
#define DEVICE_ID_3 XPAR_AXI_GPIO_3_DEVICE_ID
#define DEVICE_ID_4 XPAR_AXI_GPIO_4_DEVICE_ID
#define DEVICE_ID_5 XPAR_AXI_GPIO_5_DEVICE_ID
#define DEVICE_ID_6 XPAR_AXI_GPIO_6_DEVICE_ID
#define DEVICE_ID_7 XPAR_AXI_GPIO_7_DEVICE_ID
#define DEVICE_ID_8 XPAR_AXI_GPIO_8_DEVICE_ID

#define GPIO_BA_0 XPAR_AXI_GPIO_0_BASEADDR
#define GPIO_BA_1 XPAR_AXI_GPIO_1_BASEADDR
#define GPIO_BA_2 XPAR_AXI_GPIO_2_BASEADDR
#define GPIO_BA_3 XPAR_AXI_GPIO_3_BASEADDR

#define DIN XPAR_PS7_UART_1_BASEADDR
static u8 recv_buf;
XGpio
Gpio_0,Gpio_1,Gpio_2,Gpio_3,Gpio_4,Gpio_5,Gpio_6,Gpio_7,Gpio_8;
XGpio_Config
*Config0;//*Config1,*Config2,*Config3,*Config4,*Config5;
//XUartPs Uart_Ps;
//XUartPs_Config *Config;
void droop_coeff_write(system_pi*,float[6],float[2]); //my dec
void offset_corr_write(system_pi*,float[10]);
void piv_control_write(vcloop_pi_f*, float, float,float);
void pic_control_write(vcloop_pi_f*, float,float);
void update_kp(vcloop_pi_f*);
```

```c
int main()
{
                int Status;
            float    code_flt1,code_flt2,code_flt3,code_flt4;
            float ain_valu1,ain_valu2,ain_valu3,ain_valu4;
            char
buffer1[10],buffer2[10],buffer3[10],buffer4[10];
            char *recv_buf[4];
            int16_t
data1,data2,data3,data4;//,data2,data3,data4; //int16_t

            Status = XGpio_Initialize(&Gpio_0, DEVICE_ID_0);
            xil_printf("GPIO status1 is as 1:  %d\r\n",
Status);

            XGpio_SetDataDirection(&Gpio_0, 1,0xFFFF);
            XGpio_SetDataDirection(&Gpio_0, 2,0xFFFF);
            Status = XGpio_Initialize(&Gpio_1, DEVICE_ID_1);
            xil_printf("GPIO status2 is as 2:  %d\r\n",
Status);

              XGpio_SetDataDirection(&Gpio_1, 1,0xFFFF);
              XGpio_SetDataDirection(&Gpio_1, 2,0xFFFF);
              Status = XGpio_Initialize(&Gpio_2, DEVICE_ID_2);
              xil_printf("GPIO status is as 3:  %d\r\n",
Status);
              XGpio_SetDataDirection(&Gpio_2, 1,0xFFFF);
              XGpio_SetDataDirection(&Gpio_2, 2,0xFFFF);
              Status = XGpio_Initialize(&Gpio_3, DEVICE_ID_3);
              xil_printf("GPIO status is as 4:  %d\r\n",
Status);
              XGpio_SetDataDirection(&Gpio_3, 1,0xFFFF);
              XGpio_SetDataDirection(&Gpio_3, 2,0xFFFF);
              Status = XGpio_Initialize(&Gpio_4, DEVICE_ID_4);
              xil_printf("GPIO status is as 5:  %d\r\n",
Status);
              XGpio_SetDataDirection(&Gpio_4, 1,0xFFFF);
              XGpio_SetDataDirection(&Gpio_4, 2,0xFFFF);
              Status = XGpio_Initialize(&Gpio_5, DEVICE_ID_5);
              xil_printf("GPIO status is as 5:  %d\r\n",
Status);
              XGpio_SetDataDirection(&Gpio_5, 1,0xFFFF);
              XGpio_SetDataDirection(&Gpio_5, 2,0xFFFF);
              Status = XGpio_Initialize(&Gpio_6, DEVICE_ID_6);
              xil_printf("GPIO status is as 6:  %d\r\n",
Status);
              XGpio_SetDataDirection(&Gpio_6, 1,0xFFFF);
```

```c
                XGpio_SetDataDirection(&Gpio_6, 2,0xFFFF);
                Status = XGpio_Initialize(&Gpio_7, DEVICE_ID_7);
                xil_printf("GPIO status is as 7:  %d\r\n",
Status);

                XGpio_SetDataDirection(&Gpio_7, 1,0xFFFF);
                XGpio_SetDataDirection(&Gpio_7, 2,0xFFFF);
                Status = XGpio_Initialize(&Gpio_8, DEVICE_ID_8);
                XGpio_SetDataDirection(&Gpio_8, 1,0xFFFF);
                XGpio_SetDataDirection(&Gpio_8, 2,0xFFFF);


        system_pi* IP_syste=malloc(sizeof(system_pi));
        int status0=system_pi_Initialize(IP_syste,
XPAR_SYSTEM_PI_0_DEVICE_ID);
        vcloop_pi_f* IP_vc1=malloc(sizeof(vcloop_pi_f));
        vcloop_pi_f* IP_vc2=malloc(sizeof(vcloop_pi_f));
        int status1=vcloop_pi_f_Initialize(IP_vc1,
XPAR_VCLOOP_PI_F_0_DEVICE_ID);
        int status2=vcloop_pi_f_Initialize(IP_vc2,
XPAR_VCLOOP_PI_F_1_DEVICE_ID);


        }

        //int droop_coef[6] ={-322123,-214749,-858994,-
1073system_pi742,7360,7360 }; // {F1, F2, VD1,Vd2,Vr1,Vr2}
//      float droop_coef[6] ={-0.0003,-0.0002,-0.0008,-
0.0001,12,12};
//      float droop_coef[6] ={0.001,0,0,0,35,35};
        float droop_coef[6] ={-0.002,-0.002,-0.002,-
0.002,70,70};//
//      float droop_coef[6] ={0,0,0,0,76.2,80.8};//

    float vga=0.011;
    float vgb=0.011;

//
    float Kpi [2]={0,60};
    float kpv[2]={0.6,0.6};
    float kiv[2]={0.5,0.5};
//     float kpv[2]={0.1,0.1};
//     float kiv[2]={0.2,0.2};
    float kpc[2]={2,2};
    float kic[2]={0,0};
//     float offset_all[8]={1.88,2.70,0,0,0.062,0.1,0,0};
//     float offset_all[8]={3.3,4.50,0,0,0.062,0.1,0,0};
```

```c
        Float offset_all[10]={7.5,7.5,5.4,5.4,0.128,0.136,0.128,0.04,45,45};//INV2
//      float offset_all[8]={4.65,4.93,5.125,5.125,0.132,0.062,-0.0117,0.0703};//INV2
        droop_coeff_write(IP_syste,droop_coef,Kpi);
        offset_corr_write(IP_syste,offset_all);
        piv_control_write(IP_vc1, kpv[0], kiv[0],vga);     // tf=[b2,b1,b0]/[a2,a1,a0] == a0=1/a0
        pic_control_write(IP_vc1,  kpc[0], kic[0]);     // tf=[b2,b1,b0]/[a2,a1,a0] == a0=1/a0
        piv_control_write(IP_vc2, kpv[1], kiv[1],vgb);     // tf=[b2,b1,b0]/[a2,a1,a0] == a0=1/a0
        pic_control_write(IP_vc2, kpc[1], kic[1]);     // tf=[b2,b1,b0]/[a2,a1,a0] == a0=1/a0


//           xil_printf("SPI status is as 4:  %d\r\n", Status);
//
int c_sig=0;float count=0;
        while (1)
            {
             c_sig=c_sig+1;
//                 update_kp(IP_vc1);
//                 update_kp(IP_vc2);
             Gpio_2: Vxa,Vxb;  Gpio_3: Ixa, Ixb , Gpio_7: Vya,Vyb; Gpio_8:Iya, Iyb
                 xil_printf("In LOOP for Reading Data\r\n");
                 data1=XGpio_DiscreteRead(&Gpio_2,1);
                 data2=XGpio_DiscreteRead(&Gpio_2,2);
                 data1=XGpio_DiscreteRead(&Gpio_7,1);
                 data2=XGpio_DiscreteRead(&Gpio_7,2);
             -----power_out gpi0-5= P1,P2, gpio-6=Q1,Q2
                 data1=XGpio_DiscreteRead(&Gpio_5,1);
                 data2=XGpio_DiscreteRead(&Gpio_5,2);
                 data3=XGpio_DiscreteRead(&Gpio_6,1);
                 data4=XGpio_DiscreteRead(&Gpio_6,2);
             -----power_out_end
             ---------V_oltage_current_
                 data1=XGpio_DiscreteRead(&Gpio_2,1);
             data2=XGpio_DiscreteRead(&Gpio_2,2);
                 data3=XGpio_DiscreteRead(&Gpio_3,1);
                 data4=XGpio_DiscreteRead(&Gpio_3,2);
```

```c
                        data3=XGpio_DiscreteRead(&Gpio_8,1);
                         data4=XGpio_DiscreteRead(&Gpio_8,2);

            //--------voltage_current_end

                        data3=XGpio_DiscreteRead(&Gpio_6,1);
                        data4=XGpio_DiscreteRead(&Gpio_6,2);
                    //      -------------------------------------
---//gpi0-5= P1,P2, gpio-6=Q1,Q2
                        code_flt1=(float)data1;
                        code_flt2=(float)data2;
                        code_flt3=(float)data3;
                        code_flt4=(float)data4;
//                      ain_valu1 = (code_flt1/16.0F);   //16_5
fix
//                      ain_valu2 = (code_flt2/16.0F);
                        ain_valu1 = (code_flt1/ 32.0F);
//16_5 fix
                        ain_valu2 = (code_flt2/ 32.0F);
//                      ain_valu3 = (code_flt3/ 16.0F); //16_8
fix
//                      ain_valu4 = (code_flt4/ 16.0F);
                        ain_valu3 = (code_flt3/256.0F); //16_8
fix
                        ain_valu4 = (code_flt4/256.0F);
//                      xil_printf("I am in loop %d\r\n");
                        sprintf(buffer1,"%f",ain_valu1);
                        sprintf(buffer2,"%f",ain_valu2);
                        sprintf(buffer3,"%f",ain_valu3);
                        sprintf(buffer4,"%f",ain_valu4);
//                      xil_printf("Signal %d:  %d %d
%d\r\n",data1);

                        xil_printf("%s,
%s,\r\n",droop_coef[0],droop_coef[1]);
//                      xil_printf("Signal:, %s,
%s,\r\n",buffer1,buffer2); c_sig,buffer1,buffer2,buffer3,buffer4,
                        Sprint(buffer8,"%f",code_flt5);//%d,
%s, %s, %s, %s
                         xil_printf("In LOOP for Reading Data
%s\r\n",buffer1);

                        if(count>10000)
                        {
                             count=0;

        droop_coef[0]=droop_coef[0]+0.01/1000;
```

```c
        droop_coef[1]=droop_coef[1]+0.01/1000;

        droop_coeff_write(IP_syste,droop_coef,Kpi);

                        }
                        count=count+1;
                }


//                      if(count>10000)
//                      {
//                              count=0;
//                              droop_coef[0]=-0.004;
//=droop_coef[0]+0.01/1000;
//                              droop_coef[1]=-0.004;
//                              getchar();
//
        droop_coef[1]=droop_coef[1]+0.01/1000;

        droop_coeff_write(IP_syste,droop_coef,Kpi);
//                              droop_coef[1]=-0.006;
//                              droop_coef[0]=-0.006;
//=droop_coef[0]+0.01/1000;
//                              getchar();

        droop_coeff_write(IP_syste,droop_coef,Kpi);
//                              droop_coef[1]=-0.008;
//                              droop_coef[0]=-0.008;
//=droop_coef[0]+0.01/1000;
//                              getchar();

        droop_coeff_write(IP_syste,droop_coef,Kpi);
//                              droop_coef[1]=-0.010;
//                              droop_coef[0]=-0.010;
//=droop_coef[0]+0.01/1000;
//                              getchar();

        droop_coeff_write(IP_syste,droop_coef,Kpi);

//                      }

                return 0;
}

void update_kp(vcloop_pi_f* IP_vc)
```

```c
{
    float kpvx,kivx;
    int i;
    float vgax=0.02;
    for (i=0;i<=1;i++)
    {
        if (i==0)
        {
            xil_printf("Enter Kpvx :");
            read(0,recv_buf, 4);
            kpvx=(float)(recv_buf);
            xil_printf("\r\n");
        }
        else if(i==1)
        {
            xil_printf("Enter Kpvi: ");
            read(0,recv_buf, 4);
            kpvx=(float)(recv_buf);
            xil_printf("\r\n");
        }

    }

}


void droop_coeff_write(system_pi* IP_s,float droop_coef[6],float
Kpi[2])
{
    int temp;
    temp=(int)(droop_coef[0]*1073741824);
    system_pi_f_droop_1_write(IP_s, temp); // -1.5/5000= -322123
// 32_30 , 2^30=1073741824
    temp=(int)(droop_coef[1]*1073741824);
    system_pi_f_droop_2_write(IP_s, temp); // -1/5000 = -214749
    temp=(int)(droop_coef[2]*1073741824);
    system_pi_v_droop_1_write(IP_s, temp); // -4/5000= -858994
    temp=(int)(droop_coef[3]*1073741824);
    system_pi_v_droop_2_write(IP_s, temp);// -5/5000 = -1073742
    temp=(int)(droop_coef[4]*32);
    system_pi_vrated_1_write(IP_s,  temp); // 230 =7360
    temp=(int)(droop_coef[5]*32);
    system_pi_vrated_2_write(IP_s,  temp); // 230 =7360
    xil_printf("Droop coeff configured !\r\n");
    temp=(int)(Kpi[0]*512);
    system_pi_kps_write(IP_s, temp);
```

```c
        temp=(int)(Kpi[1]*64);
        system_pi_kis_write(IP_s, temp);
        temp=(int)(25*32);
        system_pi_imax_write(IP_s,temp);
        temp=(int)(0.000001*268435456);
        system_pi_set_er_write(IP_s,temp);
        temp=(int)(10);
        system_pi_cnt_write(IP_s,temp);

}


void offset_corr_write(system_pi*IP_o,float offset[10])
{
        int temp;
        temp=(int)(offset[0]*32);
        system_pi_offvxa_write(IP_o, temp);
        temp=(int)(offset[1]*32);
        system_pi_offvxb_write(IP_o, temp);
        temp=(int)(offset[2]*32);
        system_pi_offvya_write(IP_o, temp);
        temp=(int)(offset[3]*32);
        system_pi_offvyb_write(IP_o, temp);
        //------------------
        temp=(int)(offset[4]*256);
        system_pi_offcxa_write(IP_o, temp);
        temp=(int)(offset[5]*256);
        system_pi_offcxb_write(IP_o, temp);
        temp=(int)(offset[6]*256);
        system_pi_offcya_write(IP_o, temp);
        temp=(int)(offset[7]*256);
        system_pi_offcyb_write(IP_o, temp);
        temp=(int)(offset[8]*16);
        system_pi_q_off_1_write(IP_o, temp);
        temp=(int)(offset[9]*16);
        system_pi_q_off_1_write(IP_o, temp);
        xil_printf("offset adjusted !\r\n");



}


void piv_control_write(vcloop_pi_f* IP_vc,float kpv,float
kiv,float rgain)
```

```c
{
        int temp;
        temp=(int)(kpv*512);
        vcloop_pi_f_kpv_write(IP_vc, temp); //0.13 = 532ss
        temp=(int)(kiv*32);
        vcloop_pi_f_kiv_write(IP_vc, temp); // -0.2604 =-1067
        temp=(int)(rgain*16384);
        vcloop_pi_f_ref_gain_write(IP_vc, temp);// 0.1304 =534
        xil_printf("v control coeff configured!\r\n");
        temp=(int)(12e-6*32768);
        vcloop_pi_f_xlcon_write(IP_vc, temp);    // virtual
impedance




}
void pic_control_write(vcloop_pi_f* IP_vc,float kpc,float kic)
{
        int temp;
          temp=(int)(kpc*512);
          vcloop_pi_f_kpc_write(IP_vc, temp); //16x12
multiyfact=2^12
                temp=(int)(kic*32);
                vcloop_pi_f_kic_write(IP_vc, temp);
                xil_printf("c control coeff configured! \r\n");

}

//////if there is problem in generation of xparameter device Id
then, check local repository. Also regenerate output product from
Vivado .
```

List of Publication from Thesis

[1]   A. Trivedi, D. K. Jain and M. Singh, "A Modified Droop Control Method for Parallel Operation of VSI's in Microgrid," 2013 IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia), Bangalore, 2013, pp. 1-5.

[2]   A. Trivedi and M. Singh, "Repetitive Controller for VSIs in Droop-Based AC-Microgrid," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6595-6604, Aug. 2017.

[3]   A. Trivedi and M. Singh, "L_1 Adaptive Droop Control for AC Microgrid With Small Mesh Network," in IEEE Transactions on Industrial Electronics, vol. 65, no. 6, pp. 4781-4789, June 2018.

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