GaAs JUNCTIONLESS FinFET for High Performance Analog Application in sub-25 nm Regime

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MASTER OF TECHNOLOGY
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NANOSCIENCE AND TECHNOLOGY

Submitted by:

Anuj Chhabra 2K16/NST/01

Under the supervision of

DR. Rishu Chaujar
Assistant Professor
Department of APPLIED PHYSICS

DEPARTMENT OF APPLIED PHYSICS
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

JUNE, 2018

DEPARTMENT OF APPLIED PHYSICS
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi - 110042

CANDIDATE'S DECLARATION

I, ANUJ CHHABRA, Roll No. 2K16/NST/01, student of M. Tech. Applied Physics, hereby declare that the project Dissertation titled "**GaAs JUNCTIONLESS FinFET for High-Performance Analog Application in sub-25 nm Regime"** which is submitted by me to the Department of APPLIED PHYSICS, Delhi Technological University, Delhi in the partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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Date:

DEPARTMENT OF APPLIED PHYSICS
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi - 110042

CERTIFICATE

I hereby certify that the Project Dissertation titled "**GaAs JUNCTIONLESS FinFET for High-Performance Analog Application in sub-25 nm regime**" which is submitted by Anuj Chhabra, Roll No. 2K16/NST/01 of Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi
Date:

Dr. RISHU CHAUJAR
SUPERVISOR
Assistant Professor
Department of Applied Physics
Delhi Technological University

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During the time of my project, several people support my work and I would like to take this opportunity to acknowledge them.

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I am thankful to Delhi Technological University for generous support and providing ample infrastructure to carry out my research work.

ABSTRACT

When a conventional MOSFET is decreased in size many short channel effects come into play. These short channel effects include Drain Induced Barrier Lowering, Tunneling into and through gate oxide, Threshold Voltage Roll-Off, Drain Punch Through. To reduce these effects a new device has been proposed named GaAs Junctionless FinFET using high-κ dielectric. Junctionless device can help reduce these effects but it suffers from lower switching ratio. To maintain the switching ratio to an optimal level new techniques have been introduced like use of metal gate and high-κ material.

In this Work GaAs Junctionless FinFET is designed in Sub-25 nm regime. Firstly, GaAs Junctionless SOI FinFET is designed using high-k spacer. This is compared with two other fin material (Si and Ge). Proposed device is found to provide a higher switching ratio. Charge density in the device is compared for three different fin materials.

Further SOI is replaced with HfO_2 which leads to increase in switching ratio. Change in Fermi level is noted for the device, which is compared with JL FinFET. When device is off, difference between Fermi level and conduction band is more in the proposed device which is a reason for lower off current.

Further, temperature analysis is done on the device. At high temperature on current shows 18% increase when compared to JL device. When device is in on state current is depended on mobility of the device and at off state current flow is found to be depended on charge density. As mobility is decreased with increase in temperature, so on state current decreases and due to increase in charge density with temperature, device is found to have an increase in leakage current. As device shows higher switching ratio even at high temperature so device can be used as a good alternative for conventional device.

Further, a grove can be introduced in place of spacer; biomolecules can settle in that grove. Change in dielectric of the grove region can lead to change in current of the device. This device can be used as a protein sensor.

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CHAPTER 1

INTRODUCTION

1.1 CONVENTIONAL MOSFET:

Conventional MOSFET is a planar three terminal device. It consists of source, drain and gate. Gate controls the flow of current in the device. Fig. 1.1 shows the schematic diagram of the conventional MOSFET. It consists of Si substrate with different doped regions. Gate forms an inversion region when the voltage applied is above the threshold voltage. This region acts as a conduction region for the device. Conventional MOSFET is made using polysilicon as the gate material and SiO_2 as gate oxide. Polysilicon and SiO_2 is used because formation of layer of SiO_2 and polysilicon is easy and well established in the industry. Conventional MOSFET is a bulk type structure. Current flow in the device is mainly constrained to the inversion region of the device; bulk part is mainly a supporting structure. Conventional MOSFET is very small in size. It generally has a channel length of around 1 to 100 µm. Gate oxide is in the range to 2 to 100 nm. Because of the small size millions of MOSFET can be placed in a single chip. MOSFET provide a better switching ratio and are faster when compared to Bipolar Junction Transistor. MOSFET are also a low power device. MOSFET is mainly used a switch, as switching circuitry is very important part of logic devices making MOSFET a fairly useful device.[1, 2]

1.2 SCALING

Efforts are being made to decrease feature size. Technology is moving towards miniaturization. To keep Moore’s law alive scaling down of the MOSFET’s is down. Scaling refers to decreasing the size of MOSFET’s. Scaling is done in such a way that ratio of the geometry is same as that of the larger device.

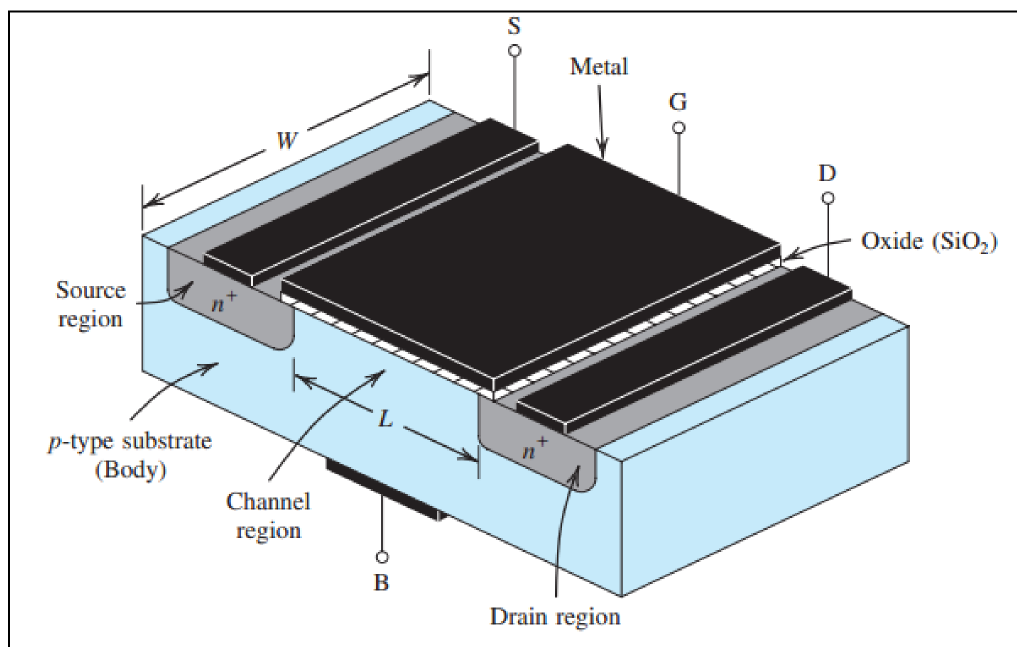


Fig. 1.1 Schematic diagram of Conventional MOSFET[1].

There are two types of scaling are common:

1) Constant field scaling

2) Constant voltage scaling.

1.2.1 Constant field is scaling: It refers to scaling in such a way that all the potentials inside the device are scaled down in proportion. Charge density has to be multiplied by the factor of S > 1 in order to maintain the electric field inside the device. It yields the largest reduction in the power-delay product of a single transistor. However, it requires a reduction in the power supply voltage as one decreases the minimum feature size.

1.2.2 Constant voltage scaling: It refers to scaling in such a way that all the voltage inside the device remains the same. The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length are reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages.[3]

1.3 SHORT CHANNEL EFFECTS:

Due to miniaturization, many new effects come into play these effects disturb the conventional setup of the device. Some of the short channel effects are Drain Induced Barrier lowering (DIBL), threshold voltage roll-off, Drain Punch through, tunneling into and through the gate oxide.

1.3.1 DIBL: When the device is a short channel device, and the device is heavily doped at the source and drain region there can be interactions between a source and drain which can lead to loss of control by the gate on the device. Drain Induced barrier lowering leads to increase of leakage current in the device which cause the switching ratio to decrease in the device. In long channel, device drain does not affect the channel region as it is far away from the region but in short channel devices as the channel length is really small drain voltage starts to act as the gate voltage, and it starts to control the device. This reduces the electron potential energy in the channel region.[3]

1.3.2 Threshold Voltage Roll-Off: When the device is reduced in size leakage current in the device is increased as DIBL takes place in the device. Due to increase in leakage current and because of punch through, the threshold voltage of the device decreases. It gets worse when a device is reduced to nanometre range. This reduction in the threshold voltage can lead to loss of control of the gate on the device. Because of threshold voltage roll-off threshold can decrease to such a level the noise present in the circuit can set the device in on state. Use of high doped polysilicon can help in maintaining the threshold voltage, but the use of higher doping can lead to tunneling into and through the gate oxide.[2, 3]

1.3.3 Tunnelling into and through gate oxide: When polysilicon is used with higher doping SiO_2 which is a low-κ dielectric because of reduced gate oxide charge can tunnel through gate oxide to the depletion region and can lead to increase leakage current. This can be reduced by using the high-κ stack. Because of use of high-κ material, polysilicon cannot be used instead metal gate is used.

1.3.4 Drain Punch through: When the device has reduced the distance between source and drain is reduced to a significant ratio. A junction is formed between drain or source and the channel region. At higher voltage junction between source or drain and channel can punch through restricting the amount of voltage that can be applied to

source and drain. This can be reduced by using the higher doping which can reduce the junction width.[3]

1.4: FinFET:

FinFET is a three-dimensional device. Its working is same as that of MOSFET, but the key difference between MOSFET and FinFET is that MOSFET is a planar device whereas FinFET is a 3D device. FinFET gets its name from the fin-like structure. Fig 1.2 shows the schematic diagram of the FinFET. FinFET is found to show less DIBL, better control over the channel region. Because of the fin structure gate can control the channel region from three sides. FinFET has three main dimensions i.e. the height of fin, length of channel length, the width of the channel length. Gate control is (2×height of fin + width) times that of the conventional device. Since the fin is so thin and generally Silicon on oxide type FinFET is used so source and drain contacts can be extended to the insulation region which reduces the device capacitance. Different types of FinFET include Tri-Gate (TG) FinFET[4], Tri-Independent Gate (TIG) FinFET[5], Dual-Gate (DG) FinFET[6], Silicon on oxide (SOI) FinFET and Bulk FinFET[7, 8].

1.4.1 Tri-Gate FinFET: It is a basic type of FinFET in which gate is surrounded by gate material from all three sides. Fig. 1.2 shows the schematic diagram of the TG FinFET Doping is done on the fin region to create source and drain regions. This device has better control when compared to conventional MOSFET because of its three-dimensional structure.

1.4.2 Tri-Independent Gate FinFET: This is modified version of TG FinFET. It has three independent gates. Fig. 1.3 shows TIG FinFET. The threshold can be controlled by applying voltage on three gates accordingly. Fig. This type of FinFET works in 5 modes.

- TIG FinFET with only top gate turns on;
- TIG FinFET with only bottom gate1/gate2 turns on;
- TIG FinFET with both bottom gate1/gate2 and top gate turn on;
- TIG FinFET with both bottom gate1 and bottom gate2 turn on;
- TIG FinFET with all of the gates turns on.

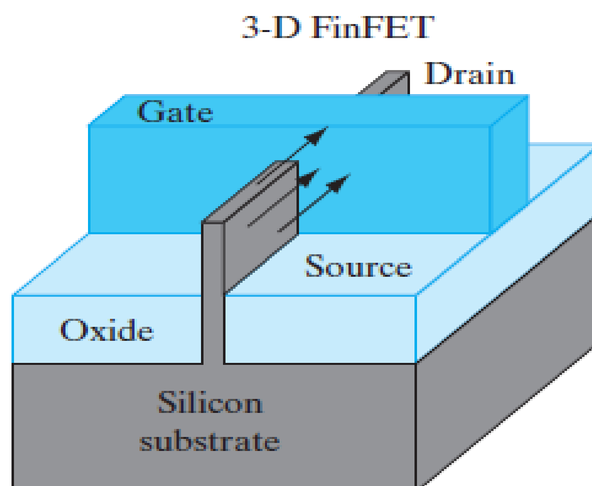


Fig. 1.2 Schematic diagram of Tri-Gate FinFET[2].

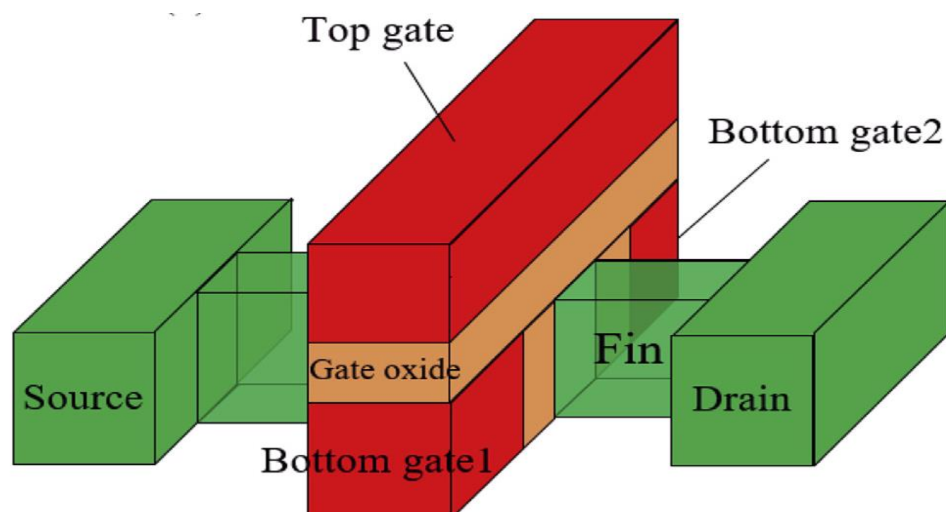


Fig 1.3 schematic diagram of TGI FinFET[5].

1.4.3 Dual Gate FinFET: In this type of FinFET two independent gates are formed which can help control the channel in a better way. The threshold can be adjusted by applying different voltage on respective gates. If in Fig. 1.3 top gate is removed it will form a dual gate FinFET.

1.4.4 SOI FinFET: Silicon on Insulator is a type of technique in which fin region is grown on insulator region. Fig. 1.4 a shows the schematic diagram of the SOI type FinFET. Most of the current flow is restricted to the inversion region only, so there is no need of the bulk region. In SOI type FinFET Silicon oxide layer is grown on the substrate region. On this oxide region, a fin-like structure is created. SOI type structures are found to provide with better switching ratio. This type of devices tends to have a

problem of lattice heating as it does not provide with a way for the heat created in the device region to escape to bulk region.

1.4.5 Bulk FinFET: Bulk FinFET is a type of FinFET in which fin is directly connected to the bulk region. It helps in providing better transfer of the heat inside the device, thus helping to maintain a constant temperature throughout the device. Fig 1.4 b shows the basic Bulk FinFET structure. Major disadvantage of this type of FinFET is that it suffers from lower switching ratio and higher parasitic capacitance.

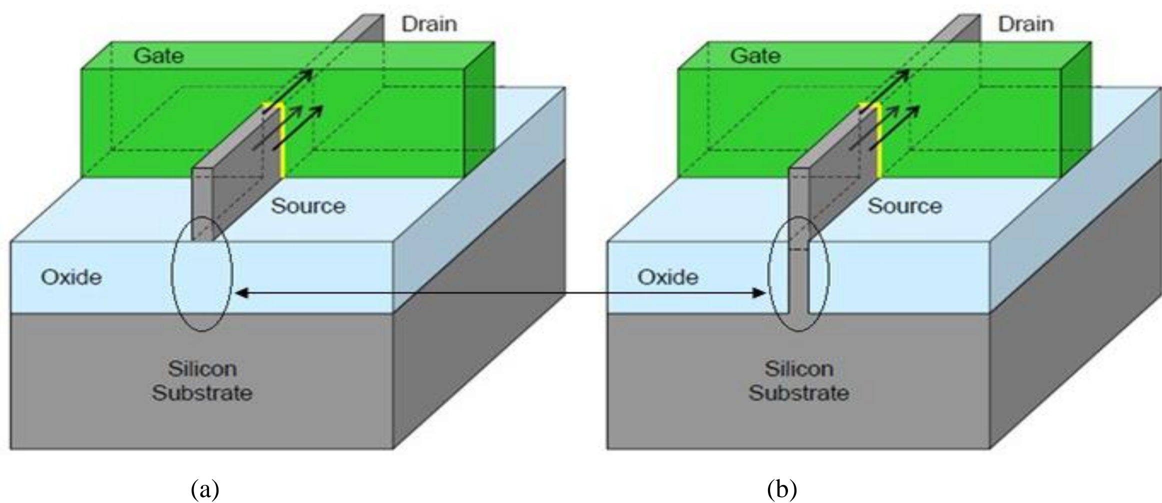


Fig. 1.4: (a) Schematic diagram of SOI FinFET. (b) Schematic diagram of Bulk FinFET.

CHAPTER 2

GaAs JUNCTIONLESS FinFET USING Si_3N_4

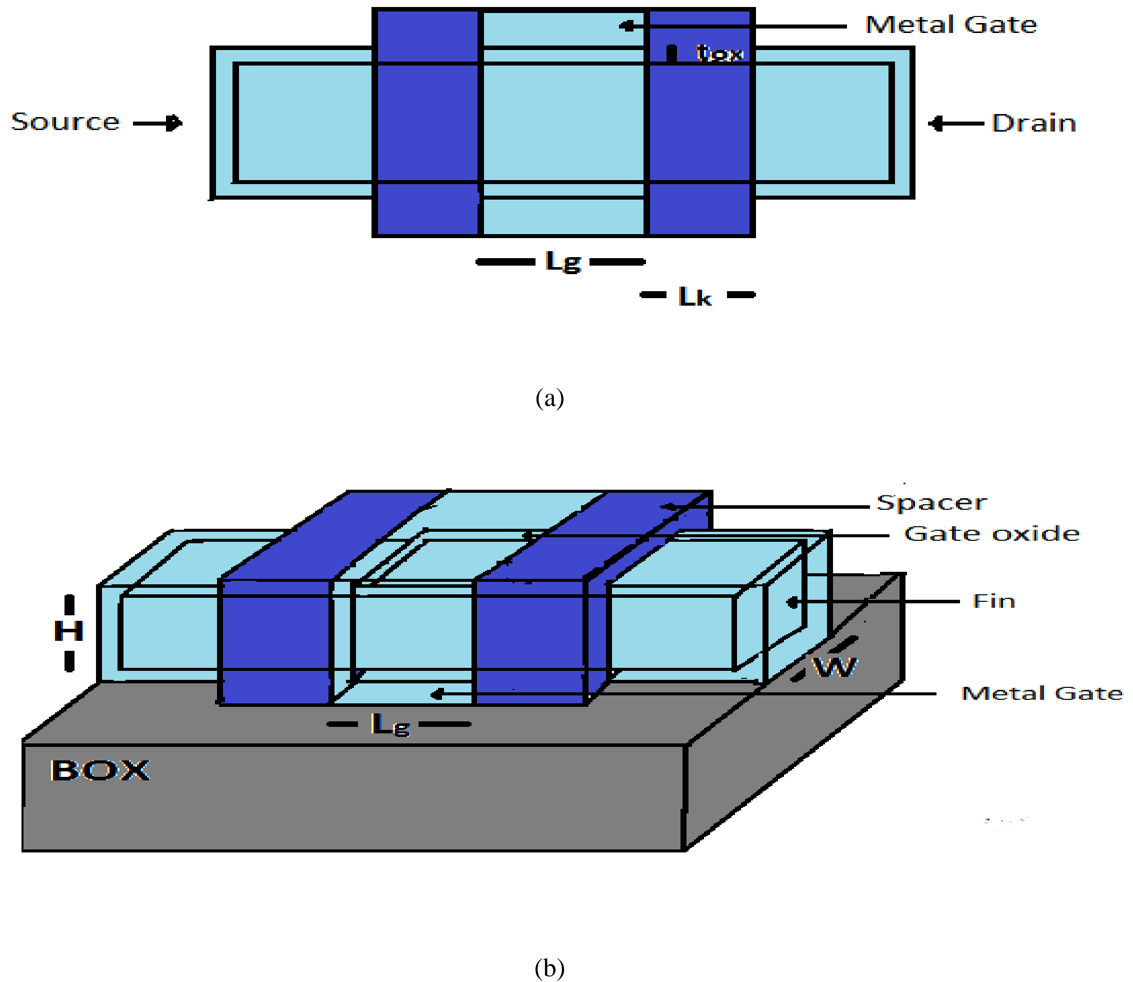
2.1 INTRODUCTION:

As the size of conventional FETs is decreased beyond a feature size, many short channel effects (SCE) like drain induced barrier lowering (DIBL), threshold voltage roll-off, degradation of off current start to play an important role. To reduce these effects, many new alternative structures are being offered to keep the Moore's law intact. Many structures like Dual gate (DG)-FinFET, Tri Gate (TG)-FinFET, non-rectangular FinFET, novel tri-independent-gate FinFET are proposed[5, 9]. Junctionless FinFET is one such device. Junctionless device can be compared to a gated resistor in which we control the current flow by varying the conductivity using the gate voltage. Junctionless device can be considered as a low resistance device in which gate voltage allows the semiconductor film of carriers to be depleted which modulates the conductivity of the charge. Junctionless devices are found to have the lower off (higher) current compared to the conventional FinFET[10]. SOI FinFET is used as it is found to have better threshold voltage roll-off and sub-threshold voltage swing values as compared to bulk FinFET. In bulk, higher value of body doping does not always give better I_{on}/I_{off} ratio. The 3D nature of bulk FinFET's gives rise to additional device parasitic[7]. FinFET provide a better control over the channel as compared to the conventional FETs and show decrease in short channel effects. Metal gate are being used these days[2, 11]. In this chapter, different parameters of FinFET using different materials (Si, Ge and GaAs) are compared.

2.2 DEVICE STRUCTURE:

Fig. 2.1 (a) and (b) show the basic structure of Junctionless FinFET used for simulation. VisualTCAD is used to create a 3D structure of the FinFET[12]. Si_3N_4 is used a spacer between gate and source/drain as well as gate oxide for each simulation. Si_3N_4 is not compatible with polysilicon gate so metal gate is used instead[13]. Si_3N_4 of thickness 8nm

is used. Gate oxide is kept at 2nm constant thickness around the fin. Gold (Au) as metal gate contact is used. Work function of metal contact is adjusted to give optimal results. Metal contact should be made of different materials for compatibility but for fair comparison, same metal contact has been used. Thickness of gate metal contact is kept at 6 nm length. Gate length (Lg) is kept constant at 20 nm length. 2nm thick source and drain metal contact are used, made of Au. Fin of height (H) and width (W) of 10nm each is used for each simulation. Fin is made of three different materials; Si, Ge and GaAs. Fin extension lengths (L_k) are kept at 20nm distance from the channel. In junctionless device, a higher doping of range of 10^{19} cm^{-3} is kept to increase the I_{on} to an optimal level. Device is made n-type by using donor doping of N_d= 3.25×10^{19} cm^{-3} in each device. Since this is a junctionless device, so source and drain are also doped as Fin i.e 3.25×10^{19} cm^{-3}.



(a)

(b)

Fig. 2.1 : (a) FinFET device top view (b) FinFET device 3D view.

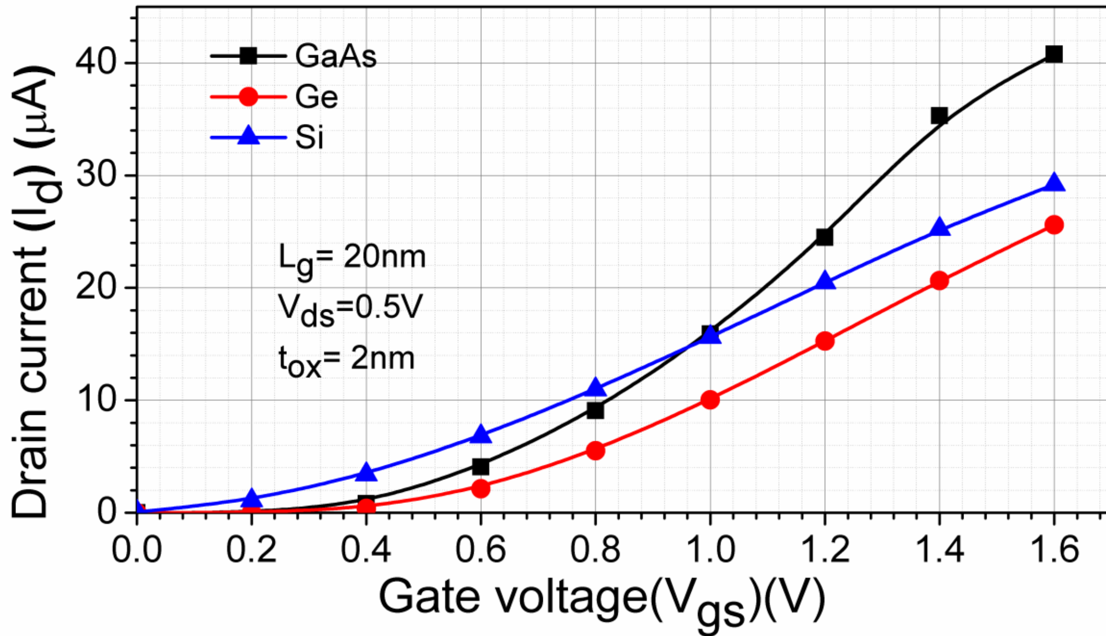
2.3 SIMULATION RESULTS:

Si, Ge and GaAs are used to make 3 different devices which are compared. Fig. 2.2 (a, b) compares the change of drain current with the change in gate voltage at constant drain voltage. All the calculation are done at a constant drain voltage, V_{ds} =0.5V. GaAs is found to have more I_{on} which is 4.07×10^{-5} A and I_{on} for Si and Ge are found to be 2.99×10^{-5} A and 2.559×10^{-5} A respectively. I_{on} is calculated at gate voltage (V_{gs}) of 1.6V and drain voltage of V_{ds}=0.5V for each device. I_{off} is found to be in the range of 10^{-12} and for Si and Ge, I_{off} is found in the range of 10^{-8} A and 10^{-9} A respectively. Fig. 2.2 (a) shows that increase of drain current is steep and shows less variation once threshold is reached but for Ge and Si, it shows more variation. Difference in I_{on} and I_{off} is because of the difference in bandgap and difference in mobility of each material. GaAs has higher bandgap and higher mobility as compared to Si and Ge. Metal gate shows more control in GaAs device.

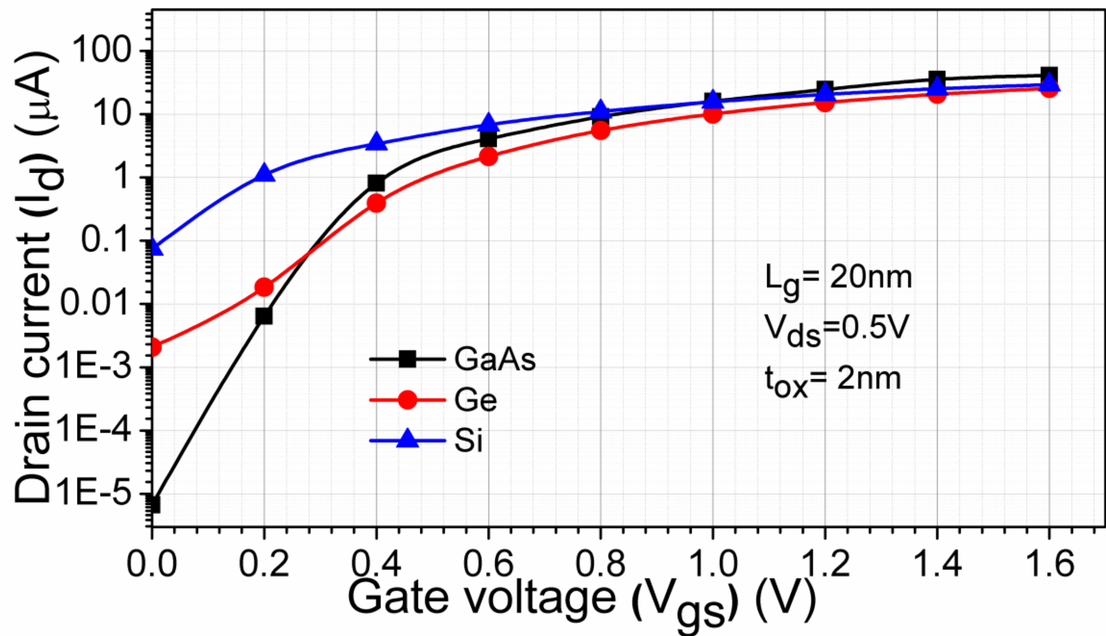
Fig. 2.3 gives the variation of drain current as the drain voltage is increased. Gate voltage is kept constant at 1V for each of the material. GaAs show the steep rise in drain current after which it saturates in the range of 10^{-5} A but Si and Ge shows gradual increase in drain current with the increase in drain voltage. This is because of large bandgap difference and higher mobility of electrons in GaAs. When device is in off state bandgap difference is dominating and when device is in on state mobility is the dominating factor, as device is in saturation. At off state in-case of GaAs FinFET more inversion charge carrier are present near the channel region which leads to decrease of leakage current.

Fig. 2.4 shows transconductance calculated for different gate voltages. Transconductance is calculated at V_{ds}=0.5 V. GaAs shows much variation in the transconductance as voltage is increased compared to Si and Ge FinFET. I_{on}/I_{off} values are calculated for Si, Ge and GaAs FinFET.

I_{on}/I_{off} for these three materials is shown in Fig. 5. GaAs provides the value of 0.607×10^{7} μA/V which is better than that of Si and Ge which gives the value of 0.39×10^{3} μA/V and 1.24×10^{4} μA/V respectively. Transconductance variation in GaAs is more because of the higher change in I_{on}/I_{off} in the device.



(a)



(b)

Fig. 2.2 (a) Variation of drain current as gate voltage is increased for Si, Ge and GaAs finFET with drain current in linear scale. (b) Variation of drain current as gate voltage is increased for Si, Ge and GaAs with drain current in log scale.

In Fig. 2.6, potential change along the channel length is observed. In between the gate length i.e. from 32nm to 52nm, we observe steep change in potential. Potential is

calculated at drain voltage of 0.5 V and gate voltage of 1V. For GaAs, this change is steep when compared to change in potential for Ge and Si.

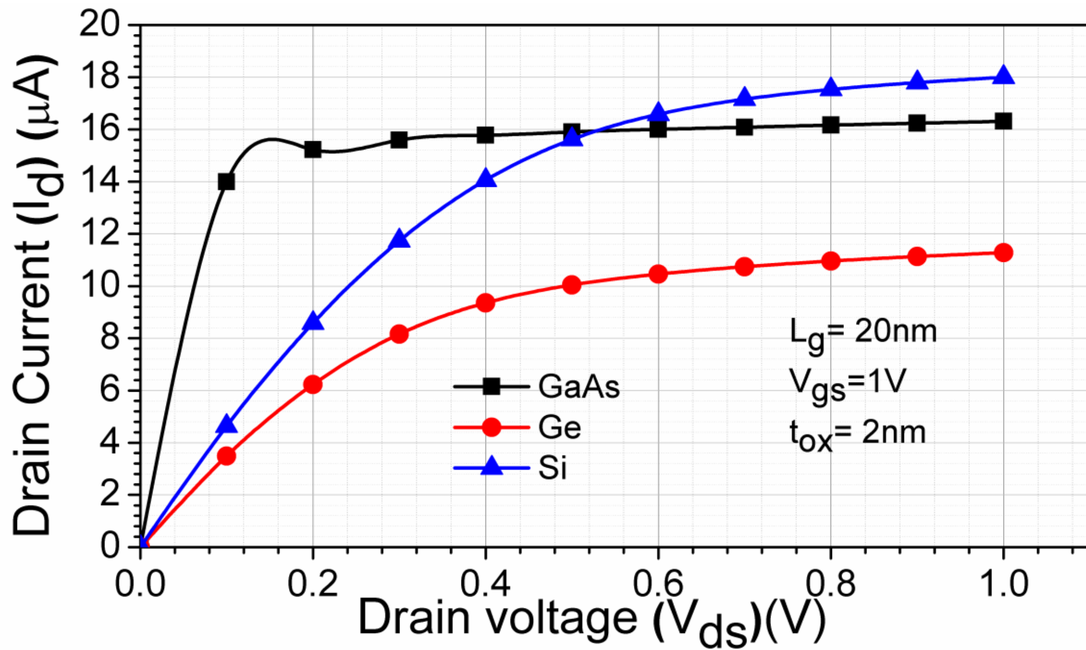


Fig. 2.3: Change in drain current Id w.r.t to change in drain voltage for Si, Ge and GaAs

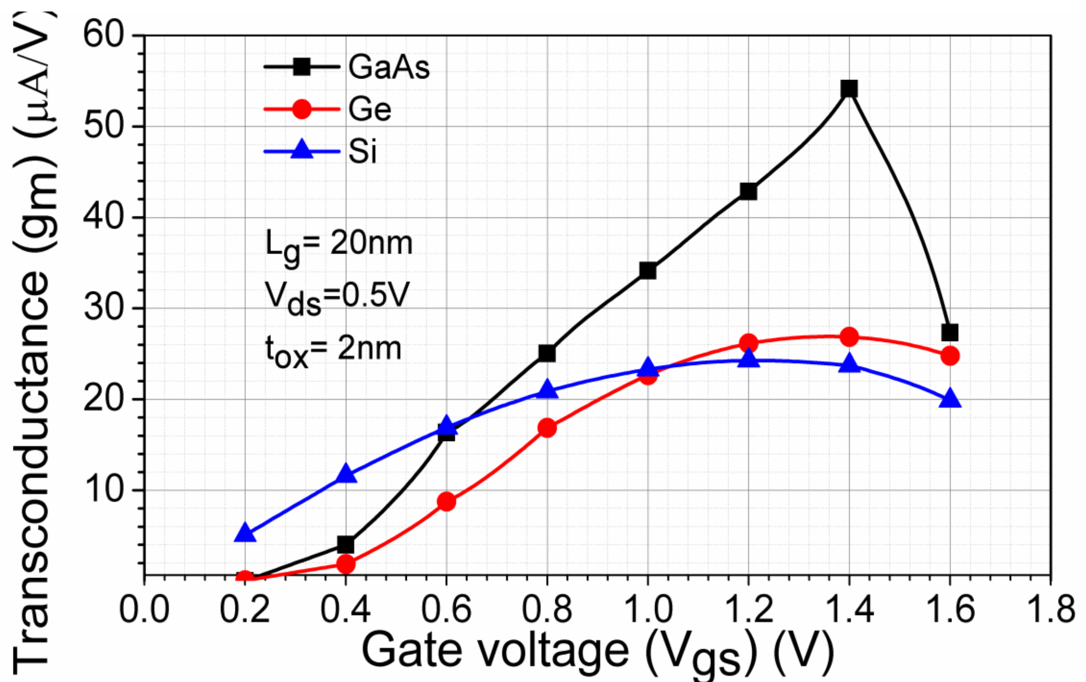


Fig. 2.4 : Transconductance variation with change of gate voltage.

Fig. 2.7 (a, b and c) shows the potential of different region of the FinFET at gate voltage (V_{gs}) of 1 V and drain voltage (V_{ds}) of 0.5 V for GaAs, Ge and Si. GaAs show more potential difference because of more control of gate on the device for same gate voltage. Because of higher potential difference in the GaAs Fin region, it shows more current when device is on.

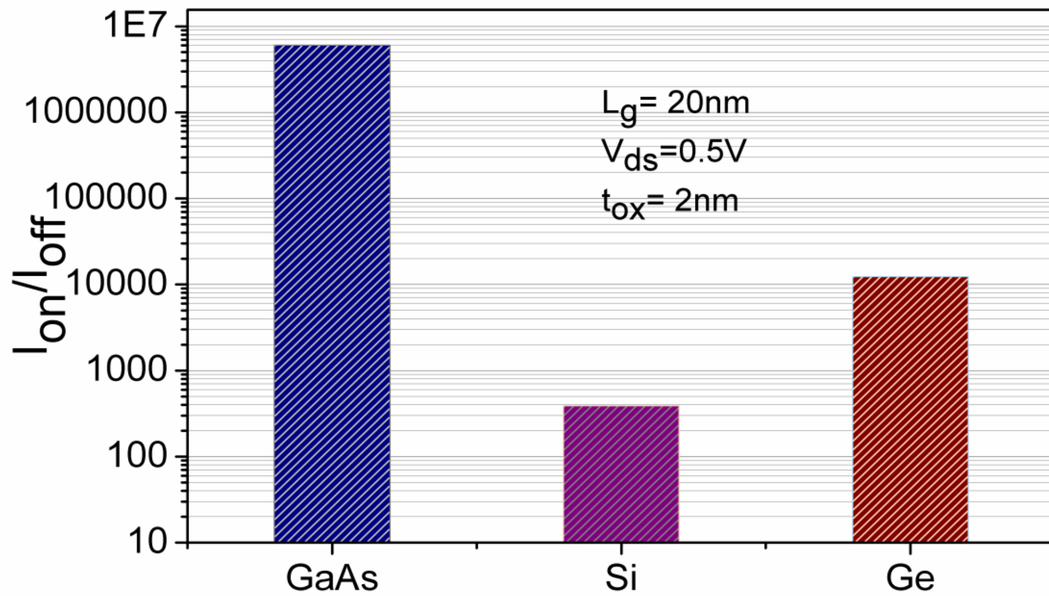


Fig. 2.5: Ion/Ioff for different materials.

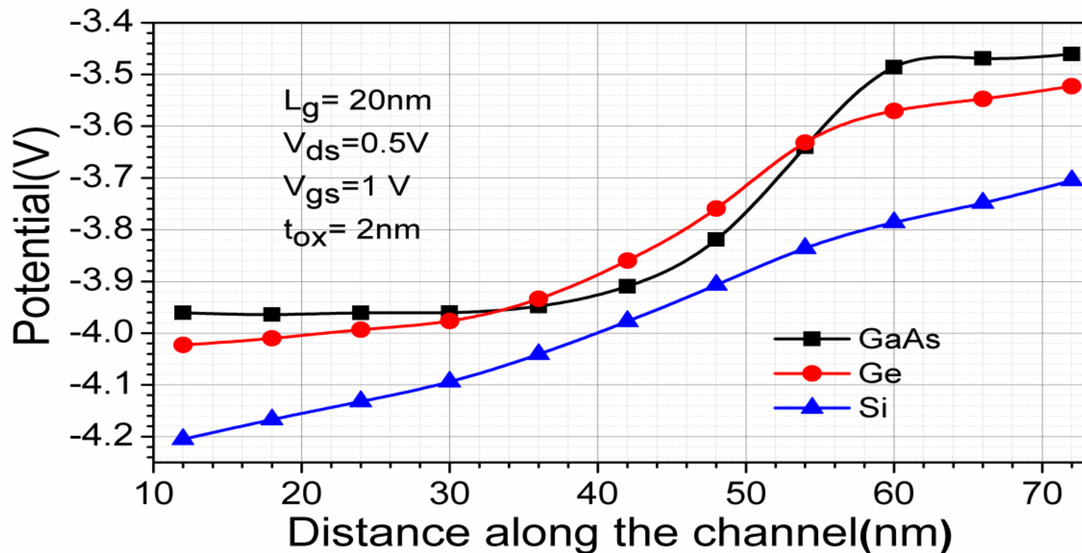


Fig 2.6: Potential variation along the channel length.

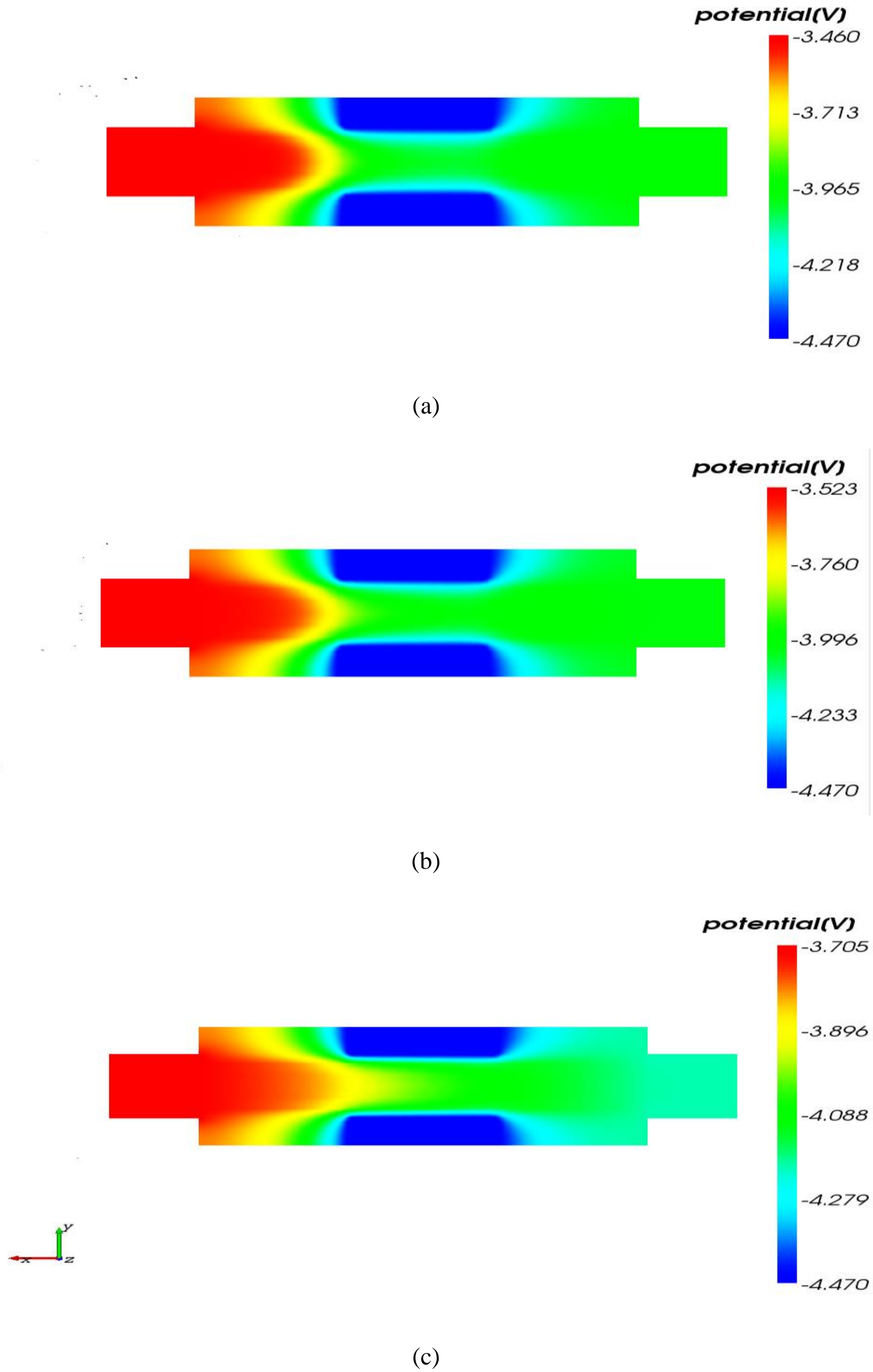


Fig 2.7: (a) potential along the device for GaAs. (b) potential along the device for Ge. (c) potential along the device for Si.

CHAPTER 3

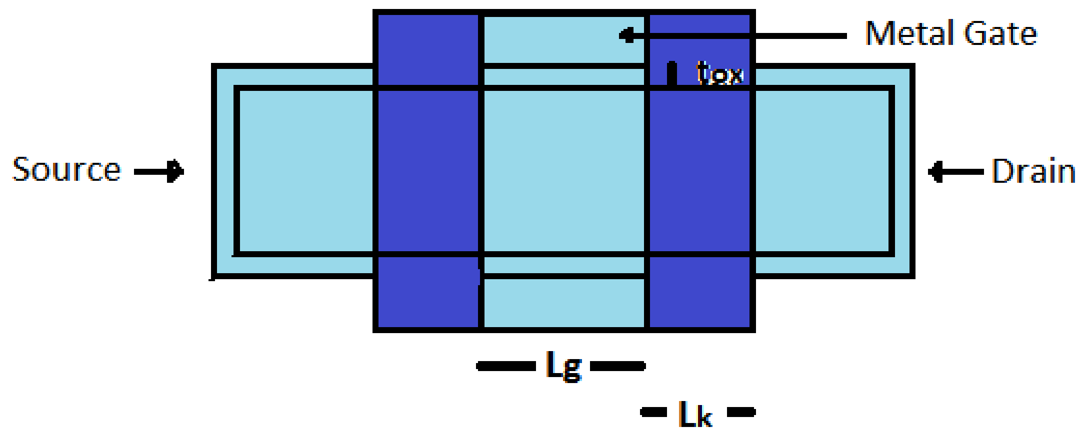
GaAs JUNCTIONLESS FinFET using high-κ dielectric material

3.1 INTRODUCTION:

This chapter proposes GaAs junctionless (JL)-FinFET for high-performance applications. Results are so obtained and compared with conventional JL-FinFET. FinFET is designed using the metal gate and using Si_3N_4 as a spacer between gate and source/drain and using high-κ BOX. Output and input characteristics are compared. GaAs JL-FinFET is found to provide lower leakage current. Further, potential inside the device is studied which show decrease in potential in the channel region in off state. In energy band diagram, higher difference is observed between Fermi and conduction level showing less conduction in off state. Electron charge density inside the device is also studied which shows the depletion of majority charge carrier concentration in off state. FinFET is being used to design SRAM as it is found to bring read stability and is found to have less parasitic capacitance, less leakage current and higher switching speed. Use of high κ-spacer increases the $I_{on}\backslash I_{off}$ ratio drastically but it is found to have increased delay time in the circuits.

3.2 DEVICE STRUCTURE:

Fig. 3.1 shows the structure of JL-FinFET with a spacer and the high-κ box is used for simulation. The 3D structure is simulated using VisualTCAD. Boltzmann statistics and drift-diffusion models are used for simulation. For the proposed device fin is made of GaAs semiconductor and for conventional FinFET, it is made of Si. Si_3N_4 is used a spacer between gate and source/drain as it shows gate capacitance comparable to that of SiO_2 and shows less delay when compared to the high-κ spacer. Si_3N_4 is not compatible with a polysilicon gate, so the metal gate is used instead[11, 13]. The thickness of Si_3N_4 spacer is kept constant at 8 nm. For fair comparison, gate oxide material is chosen to be Si_3N_4 of thickness of



(a)

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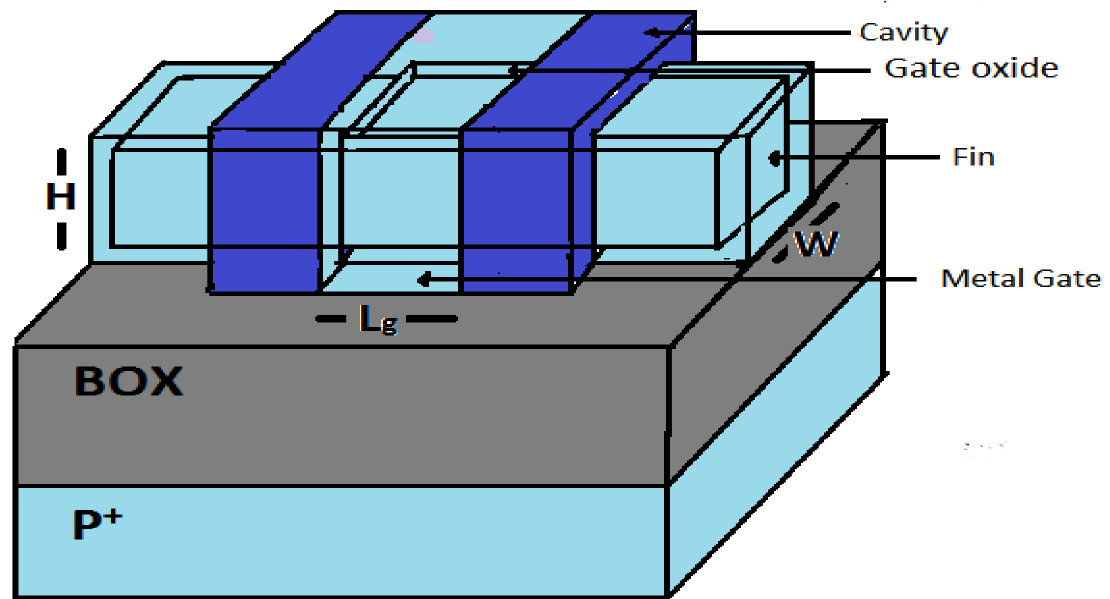


(b)

Fig.1 : (a) FinFET device top view (b) FinFET device 3D view.

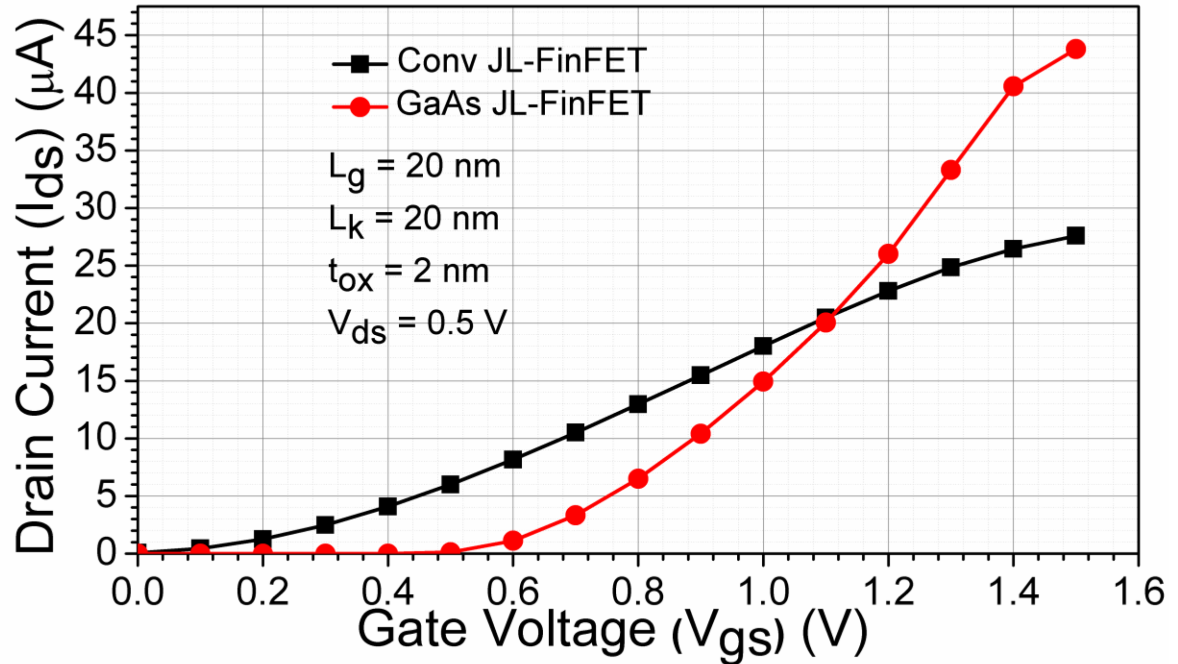
- 2 nm for conventional Junctionless FinFET as well as for the GaAs JL-FinFET using a spacer and high-k BOX. Au is used as a gate material for each simulation with the work function of 5.31 eV. For compatibility, the metal gate should be of different material, but for comparison, same metal is used. All the parameters were kept same for both the devices so

that a clear comparison can be made. Gate length (L_g) was kept constant at 20 nm as well as gate extensions (L_k), i.e., the distance between gate and source/drain was also kept constant at 20 nm. Higher donor doping of $N_d = 10^{19}$ cm^{-3} is used for junctionless devices to get appreciable I_{on}. Source and drain are also doped with $N_d = 10^{19}$ cm^{-3}. Source and drain metal contacts of thickness 2 nm are used. BOX of thickness 20 nm is used. For conventional JL-FinFET BOX is of SiO_2 while for GaAs JL-FinFET BOX is made of HfO_2 which has high dielectric constant. The heavily doped ground plane is used of thickness 20 nm with acceptor doping of 3.25×10^{18} cm^{-3}.

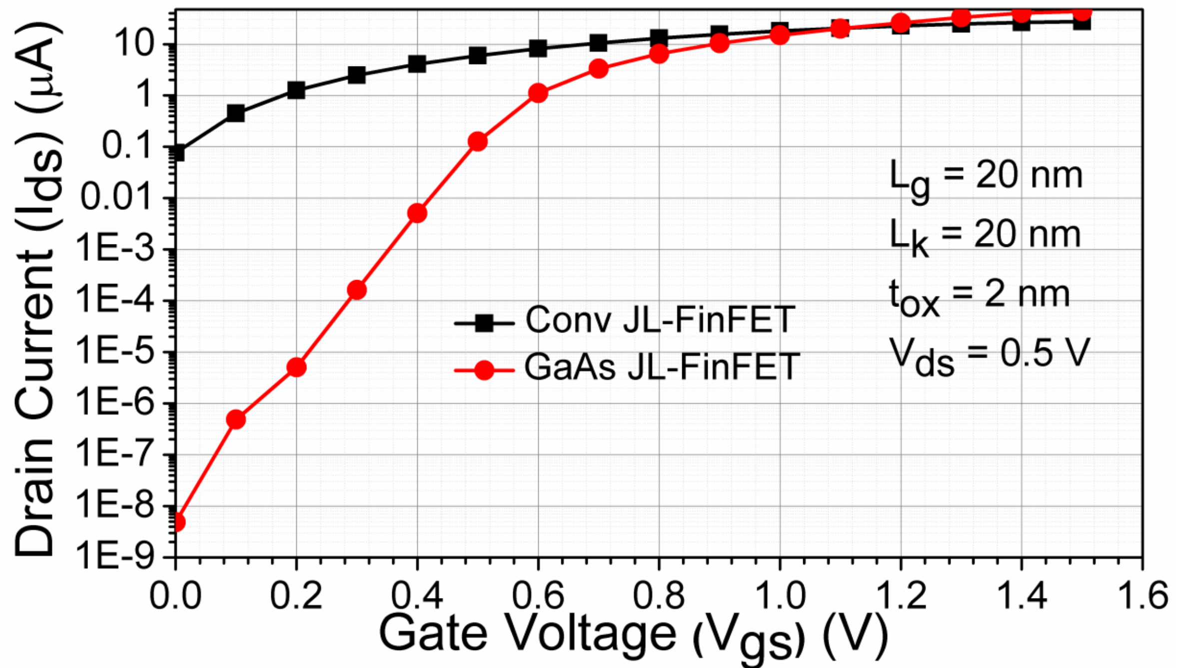
3.3 SIMULATION RESULTS AND DISCUSSION:

GaAs JL-FinFET and conventional JL-FinFET is compared. Fig. 3.2 (a, b) shows the variation of drain current (I_{ds}) with the change in gate voltage (V_{gs}) at a constant drain voltage (V_{ds}) of 0.5 V. In conventional device, threshold voltage is achieved at a very low gate voltage of about 0.1 V as compared to GaAs JL-FinFET, for which it is close to 0.5 V. At saturation i.e Vgs = 1 V, both devices show almost same current in the range of 10^{-5}. For GaAs JL-FinFET, it is found to be 1.49×10^{-5} A and for the conventional device, it is found to be 1.8×10^{-5} A. I_{off} shows the major difference in both the devices. For proposed device, it is found to be in the range of 10^{-15} whereas for a conventional device, it is 10^{-8}. Fig. 3.3 shows the I_{on}/I_{off} for both devices. For conventional device, it is 2.36×10^{2} but for GaAs JL-FinFET it is 3.08×10^{9}.

Fig. 3.4 reflects the variation of drain current with the change in V_{ds} at two constant gate voltages, i.e. V_{gs} = 0.5 and V_{gs} =0.1 V. It can be observed that for a for lower gate voltage, the leakage current is very less for GaAs JL-FinFET as compared to the conventional device. Subthreshold current is in the range of 10^{-13} A and 10^{-7} A for GaAs JL-FinFET and conventional JL-FinFET respectively.



(a)



(b)

Fig. 3.2 (a) Variation of drain current as the gate voltage is increased for conventional JL-FinFET and GaAs JL-FinFET with drain current. (b) Variation of drain current as the gate voltage is increased for conventional JL-FinFET and GaAs JL-FinFET with drain current.

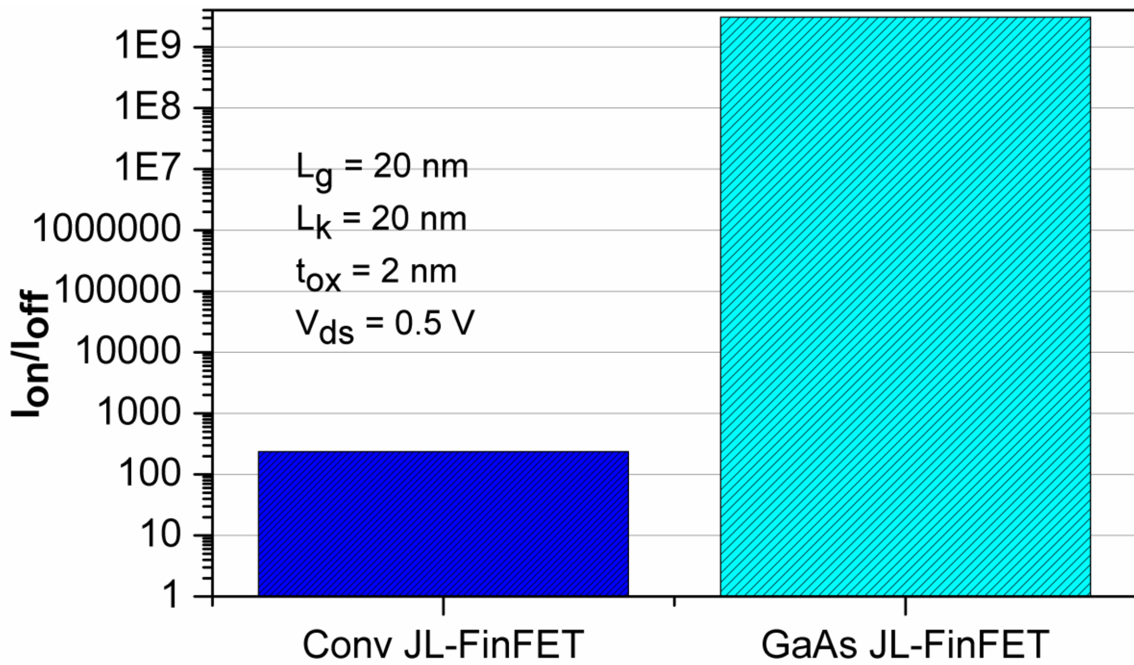


Fig. 3.3: I_{on}/I_{off} for conventional and GaAs JL-FinFET.

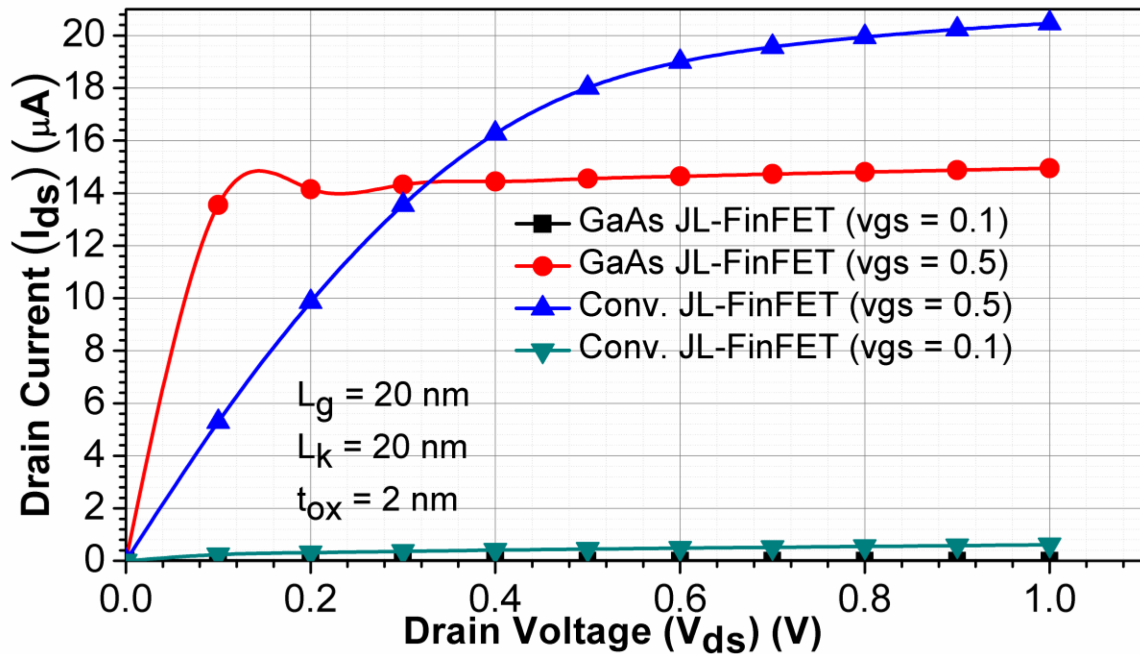


Fig. 3.4: Change in drain current Id w.r.t to change in drain voltage for conventional and GaAs JL-FinFET.

Fig. 3.5 Show the variation of potential along the channel for two devices. When the devices are in off state i.e. when $V_{gs} = 0$ V, potential barrier is formed in the channel region, i.e., between 32 nm to 52 nm. Dip in potential is almost six times for GaAs JL-FinFET as compared to the conventional device. Because of increased potential lowering in case of GaAs JL-FinFET, leakage current is less as compared to the conventional device. In saturation region, potential in the channel region is almost linear for conventional device showing little higher current.

Fig. 3.6 (a, b) show the band diagram of the devices. In channel region, difference in case of GaAs JL-FinFET between the Fermi level and conduction is more when compared to the conventional device. Because of higher difference in between Fermi level and conduction level, less charge is present in the conduction band which reduces the drain leakage current. In Fig. 3.7 (a, b), when $V_{gs} = 1$V the difference in Fermi level and conduction band is constant in the channel region and is comparable to the difference in Fermi level and conduction level in source and drain region showing the device is in saturation region for both the devices.

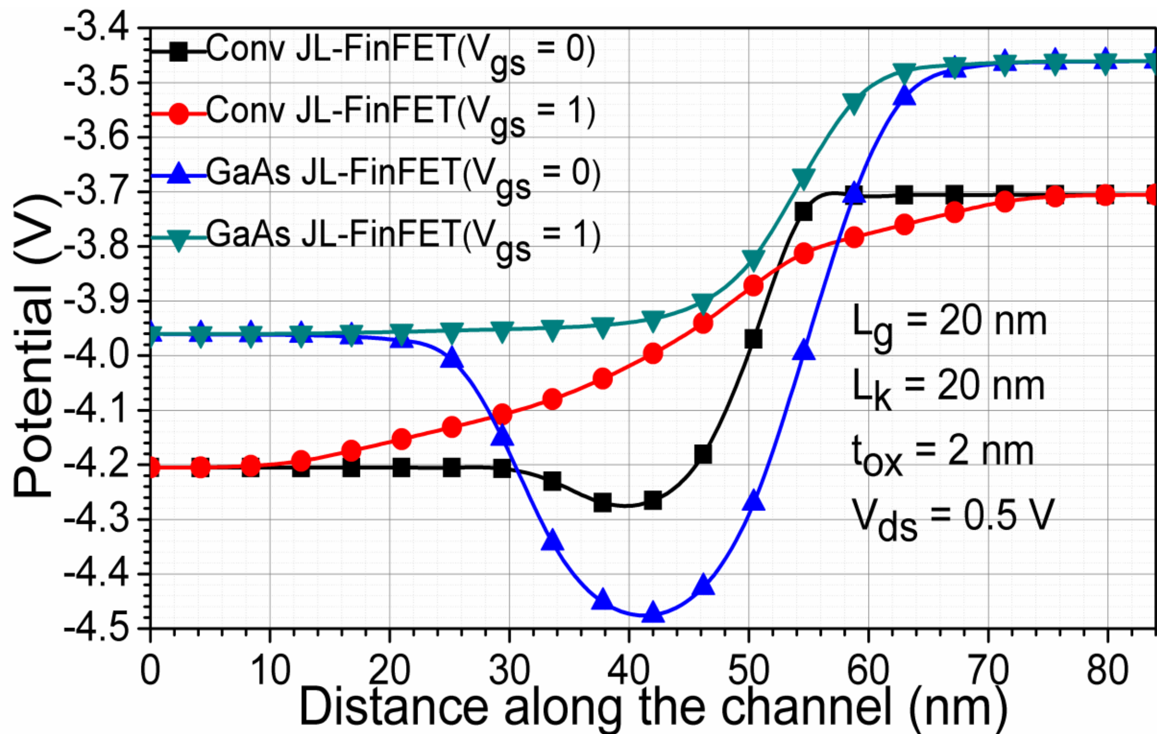
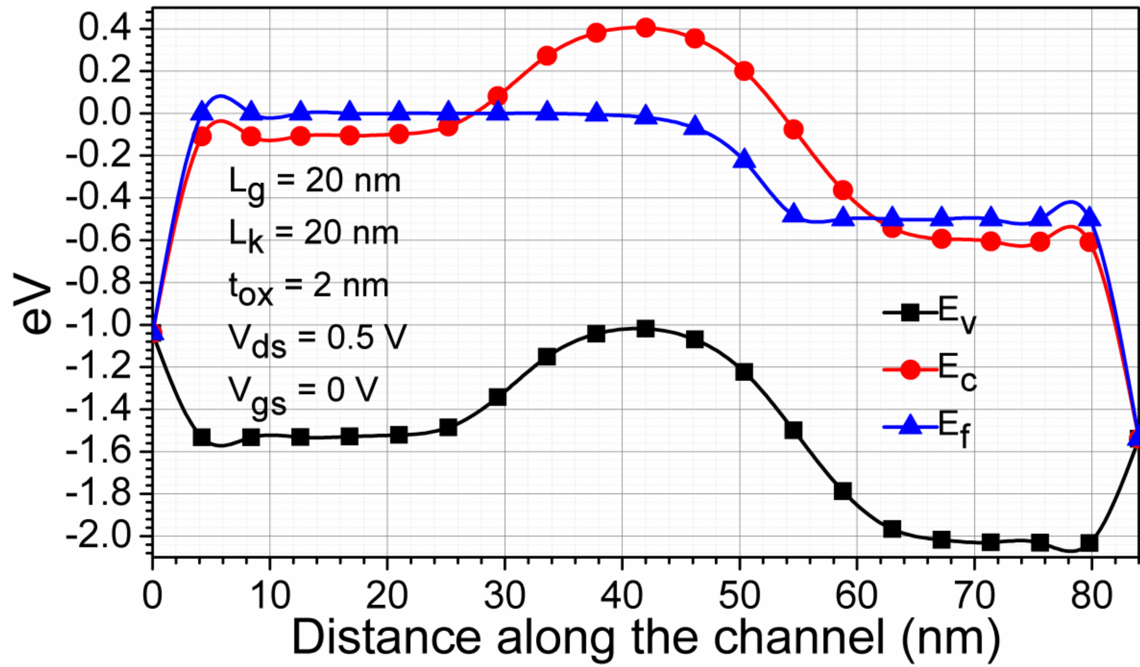
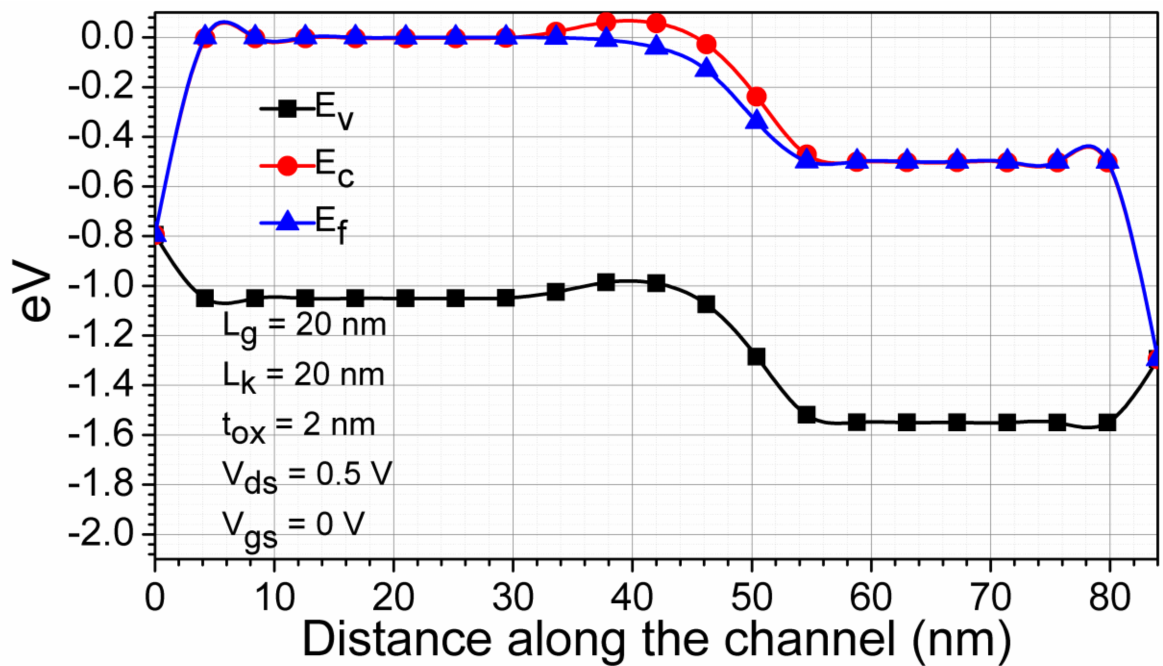


Fig 3.5: Potential variation along the channel length.

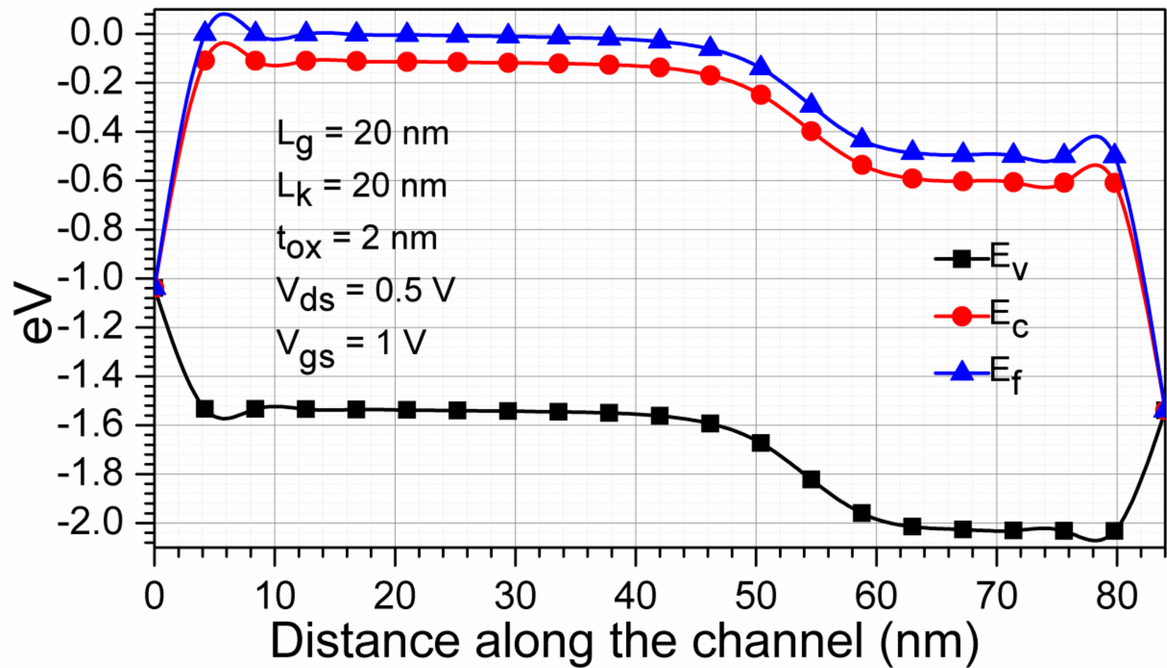


(a)

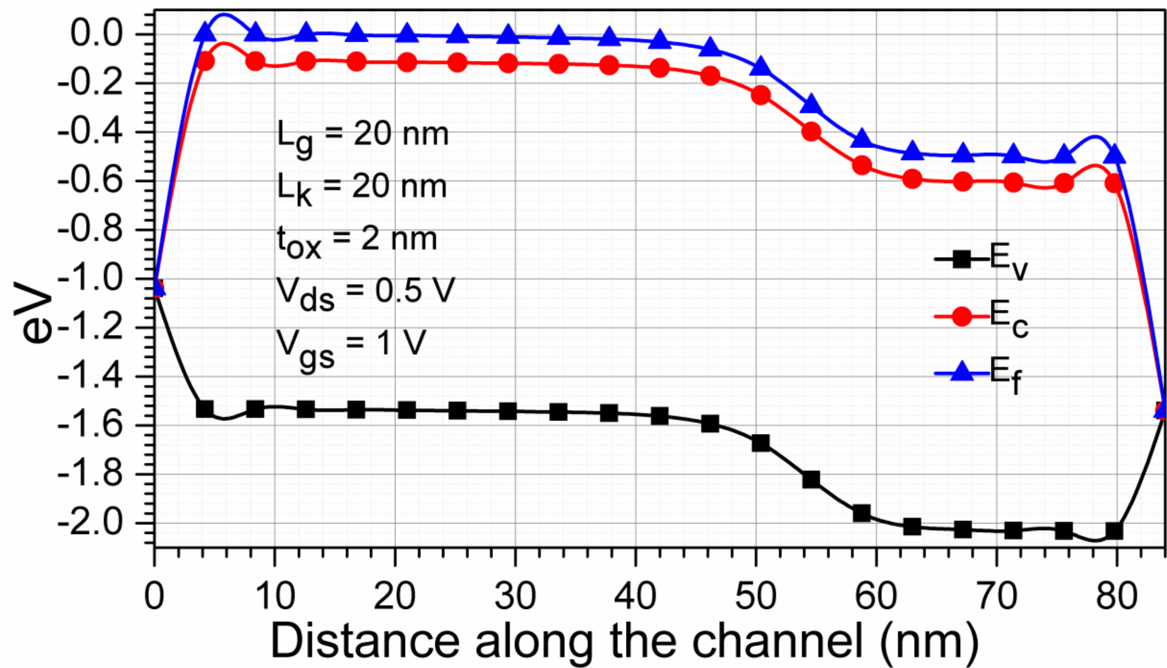


(b)

Fig. 3.6 (a) Band diagram of GaAs JL-FinFET when device is in off state (b) Band diagram of Conventional JL-FinFET when device is in off state



(a)



(b)

Fig. 3.7 (a) Band diagram of GaAs JL-FinFET when the device is in on state (b) Band diagram of Conventional JL-FinFET when the device is in on state

Fig. 3.8 (a, b) show the electron concentration when the device is OFF, or V_{gs} = 0 V at constant V_{ds} = 0.5 V. In case of GaAs JL-FinFET, higher density is near the source and drain

region only. When zero bias is applied, the channel region is depleted of majority charge carriers. Holes are attracted towards channel region as metal gate has majority electrons, so opposite charges are attracted in the channel region. Because of higher majority charge depletion in case of GaAs JL-FinFET, it shows lower leakage current. Fig. 3.8 (c, d) show electron concentration when the device is ON or V_{gs} = 1 V. When the gate voltage is positive, electrons are attracted towards the gate material in the channel region showing a decrease in minority charge carrier and increase in majority charge carriers near the channel region which increase the conductivity of the device.

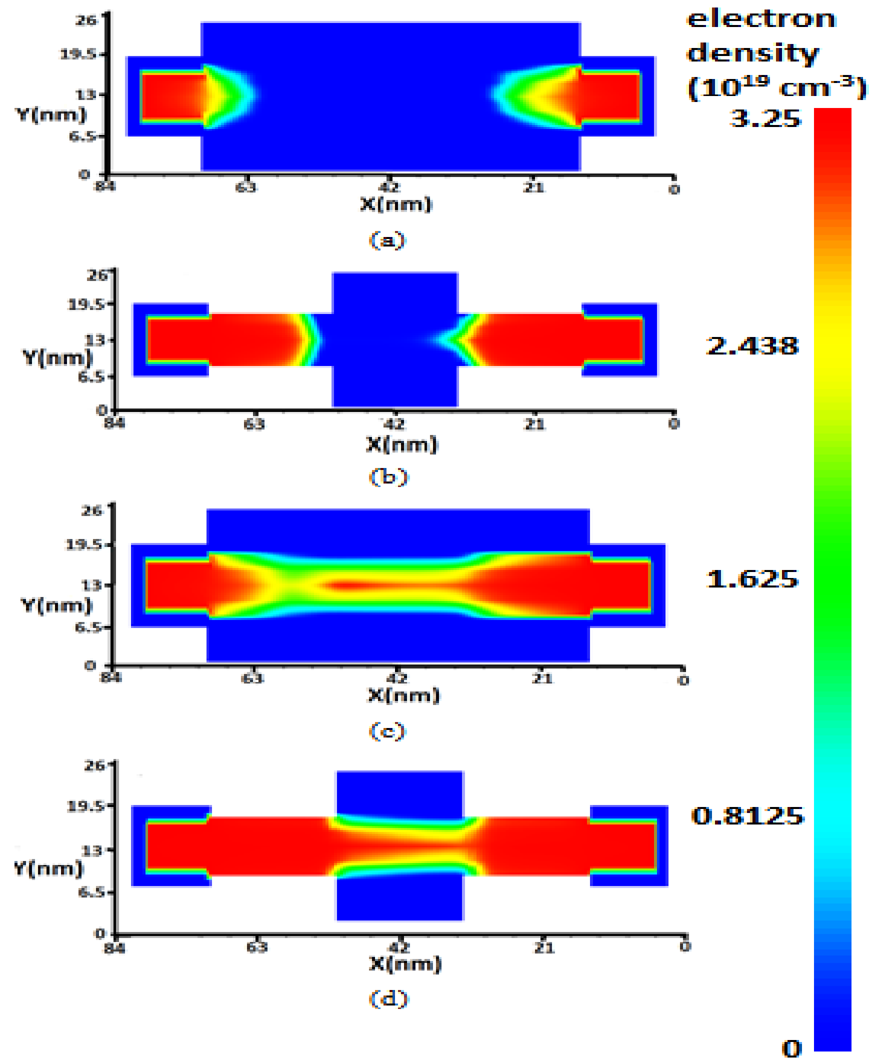


Fig. 3.8 Contours plots of (a) Electron charge density variation in GaAs JL-FinFET in off state. (b) Electron charge density variation in conventional JL-FinFET in off state. (c) Electron charge density variation in GaAs JL-FinFET in on state. (d) Electron charge density variation in conventional JL-FinFET in on state

CHAPTER 4

EFFECT OF TEMPERATURE ON GaAs JUNCTIONLESS FinFET

4.1 INTRODUCTION:

In this paper, the effect of temperature on GaAs Junctionless (JL) FinFET using high-κ dielectric has been studied at 200K, 300K, and 400K. JL FinFET, a sub-20nm device is designed using GaAs as Fin material. High-κ material is used as BOX and as a spacer. Drain current is compared with the conventional JL device. Switching ratio is enhanced by 2.58×10^7 times and I_{on} is also increased by 70% in the proposed device as compared to JL FinFET at low temperature (200K). I_{on} is found to decrease for GaAs JL FinFET with increasing temperature (200K to 400K), which is opposite to that of the conventional device. Even with the decrease of on current with temperature, I_{on} shows 18% increase as compared to JL FinFET. Further, the effect of temperature on band gap, electron mobility, and charge density is studied along the channel length. It is found that mobility plays an important role in the GaAs JL device when the device is on, and charge density plays an important role when the device is off. Higher switching ratio can be used in SRAM and as the high-κ material is used, the device can be a good alternative for RF and microwave application in sub-25 nm regime.

4.2: DEVICE STRUCTURE AND SIMULATION METHODOLOGY:

VisualTcad is used to create the 3D model of the device. Fig 4.1 shows the calibration of the software with [14]. In this simulation drift-diffusion model and Boltzmann statistics is used. Since junctionless device use higher doping to achieve higher on current, so band gap narrowing model has been used. As FinFET is a three-dimensional device so high transverse and lateral electric field models are included.

Recombination rate is calculated using the sum of auger and Shockley read hall recombination [12]. Channel doping of N_d of 3.25×10^{19} cm^{-3} is done. As the device is a JL device source and drain doping is same as a channel. Gate length (L_g) is kept at 20 nm. Source and drain extension of 20 nm is used. Gold is used as gate material. Work Function of 5.31 is used. In junctionless device higher work function has to be used to get an optimal result. HfO_2 and substrate doping of 20 nm thickness each is used. Substrate doping of N_a = 1×10^{19} cm^{-3} is done, this helps in achieving less leakage current with the use of substrate bias. Si_3N_4 is used as spacer of height 8 nm and width 20 nm.

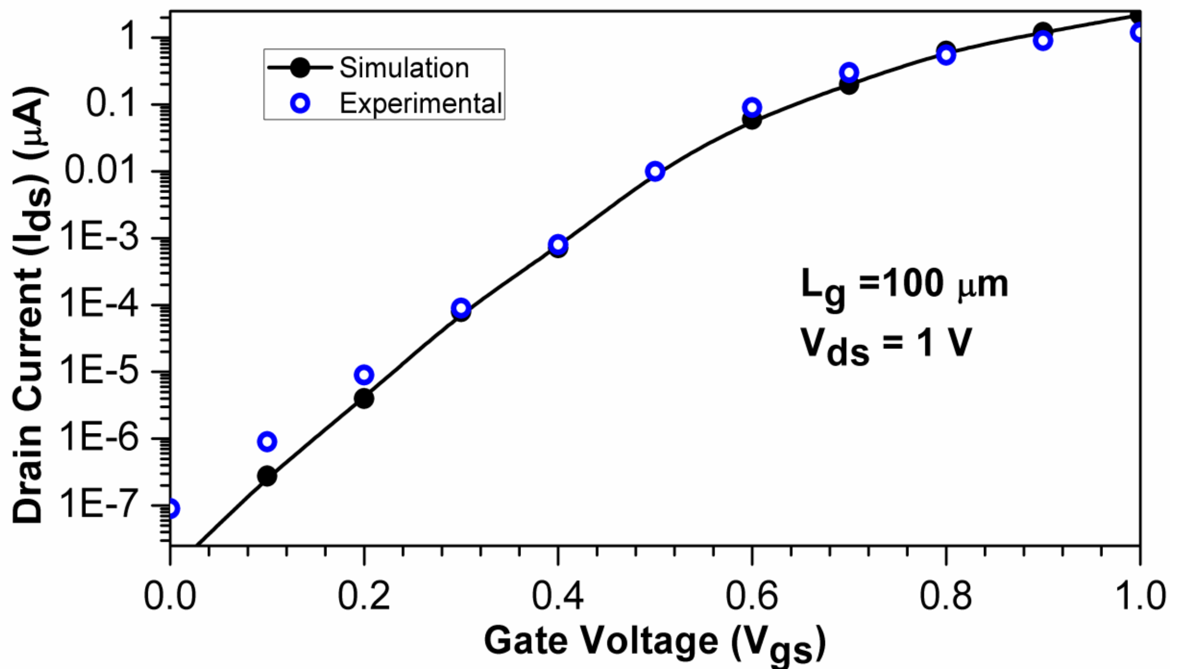
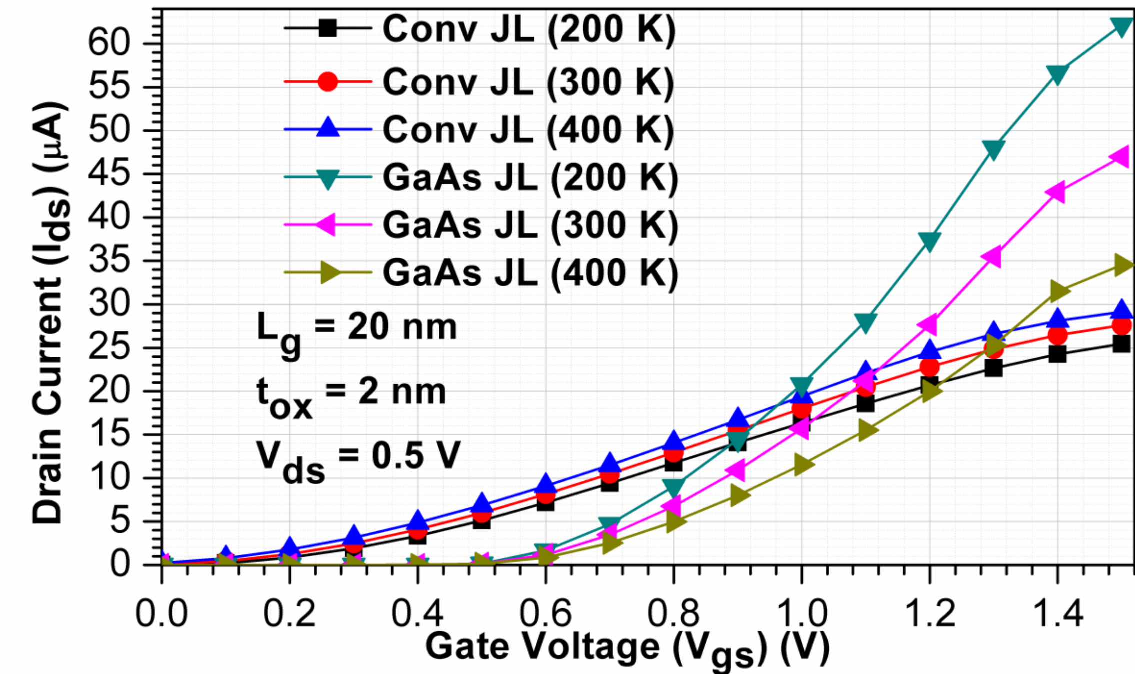


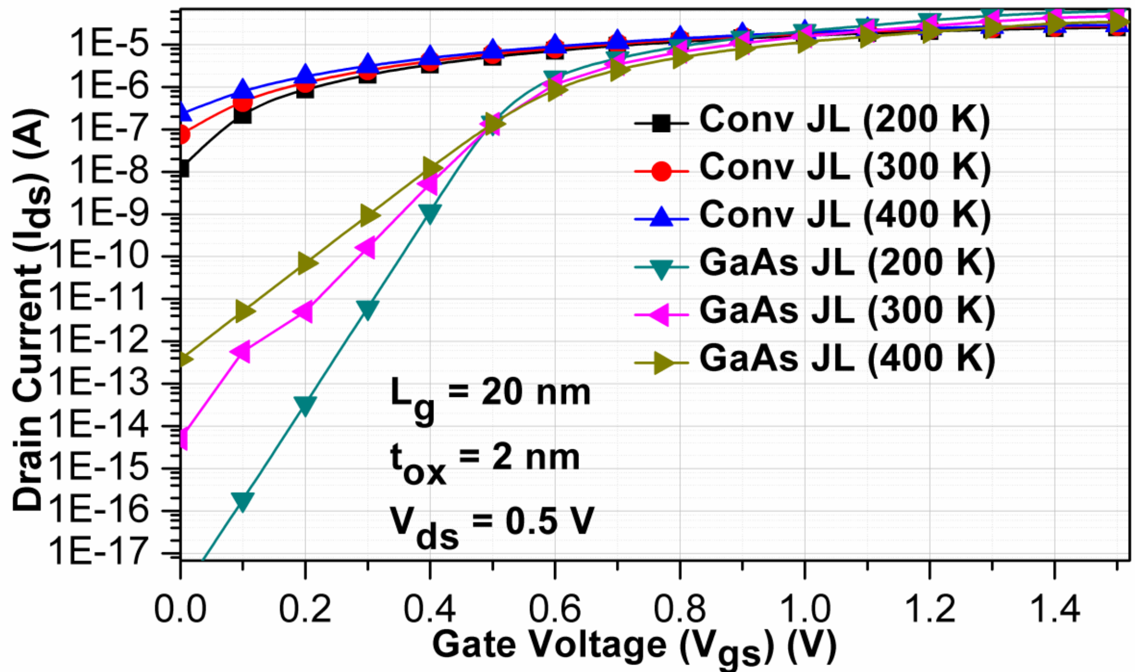
Fig. 4.1: Calibration of software with experimental data.

4.3: SIMULATION RESULTS AND DISCUSSIONS:

GaAs junctionless device is compared with the Conventional junctionless device. All the parameters are kept same for both the devices to get a fare comparison in both the devices. Fig. 4.2 (a,b) compares the drain current with change in gate voltage at different temperatures at a constant drain voltage V_{ds}= 0.5 V. For conventional device at T=300 K switching ratio is in close relation as given in the [15] at 20 nm. It is observed that for almost same on current there is a large increase in off current for both the devices. Even at-



(a)



(b)

Fig. 4.2: (a, b) Variation of drain current at constant drain voltage at a different temperature.

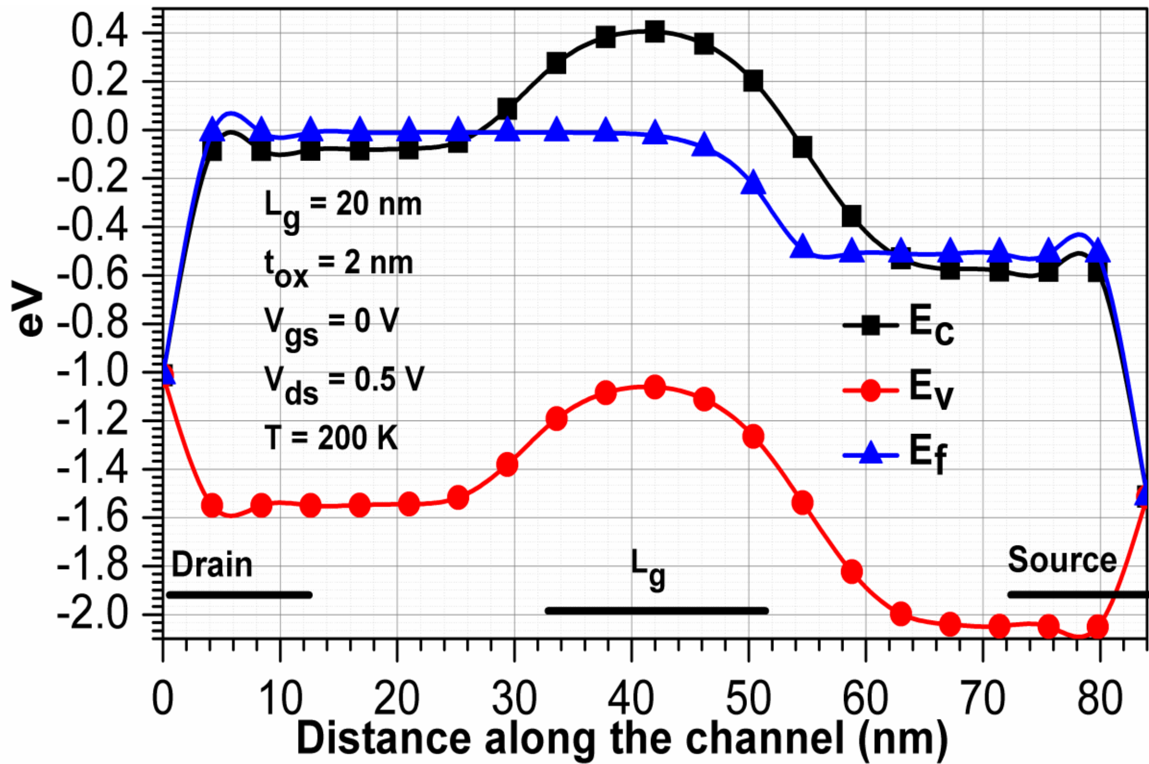
-high-temperature GaAs JL FinFET provides with better switching ratio as compared to Conventional JL FinFET. GaAs JL FinFET. GaAs JL device has increased in leakage

current with the increase in temperature but at higher voltage current decreases for GaAs JL device. Because of the use of high-κ materials prediction of various temperature effects is difficult. It was observed that percentage change in time delay was constant with reduction of temperature, opposite to that of conventional devices. [16].

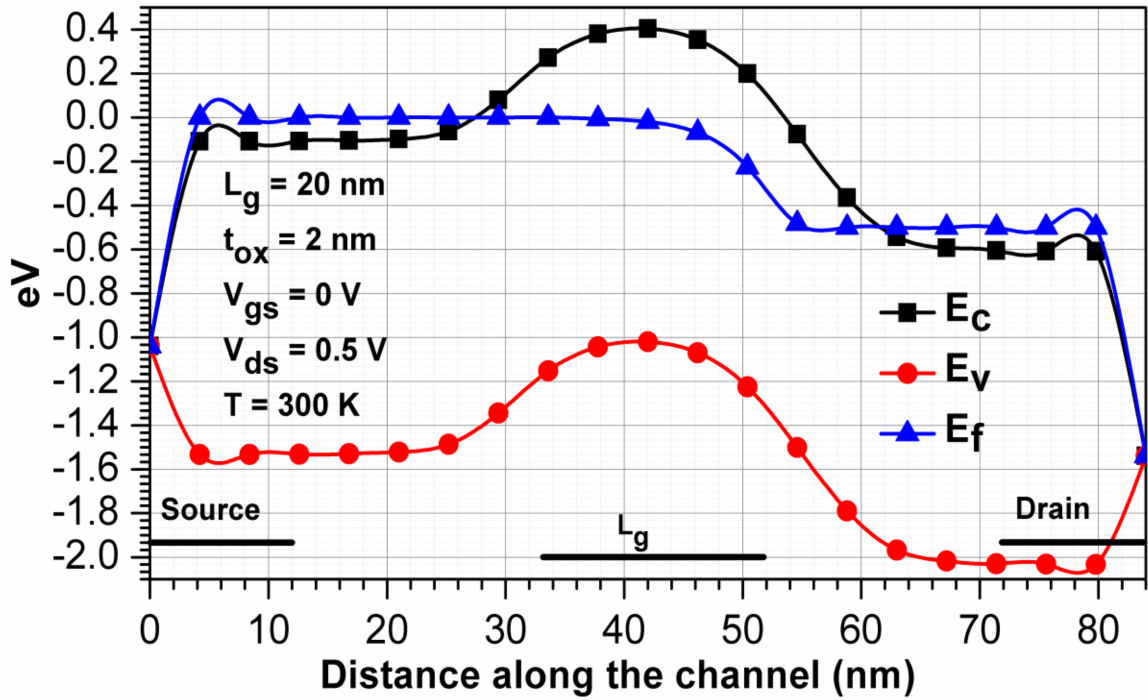
Fig 4.3 (a, b and c) compares the change in variation of band diagram inside the device at different temperature at V_{ds} = 0.5 V and when the device is in off state. With the increase of temperature difference in Fermi level and conduction band increases in source and gate region which shows the higher off-current with increasing temperature. The relation between band gap and temperature can be given by (1)[16].

$$E_g(T) = E_g(0) - \alpha_E T^2/(T + \beta_E) \quad (1)$$

Where, α for GaAs = 5.41×10^{-4} eV/K, β = 204 K and E_g = 1.519 eV.



(a)



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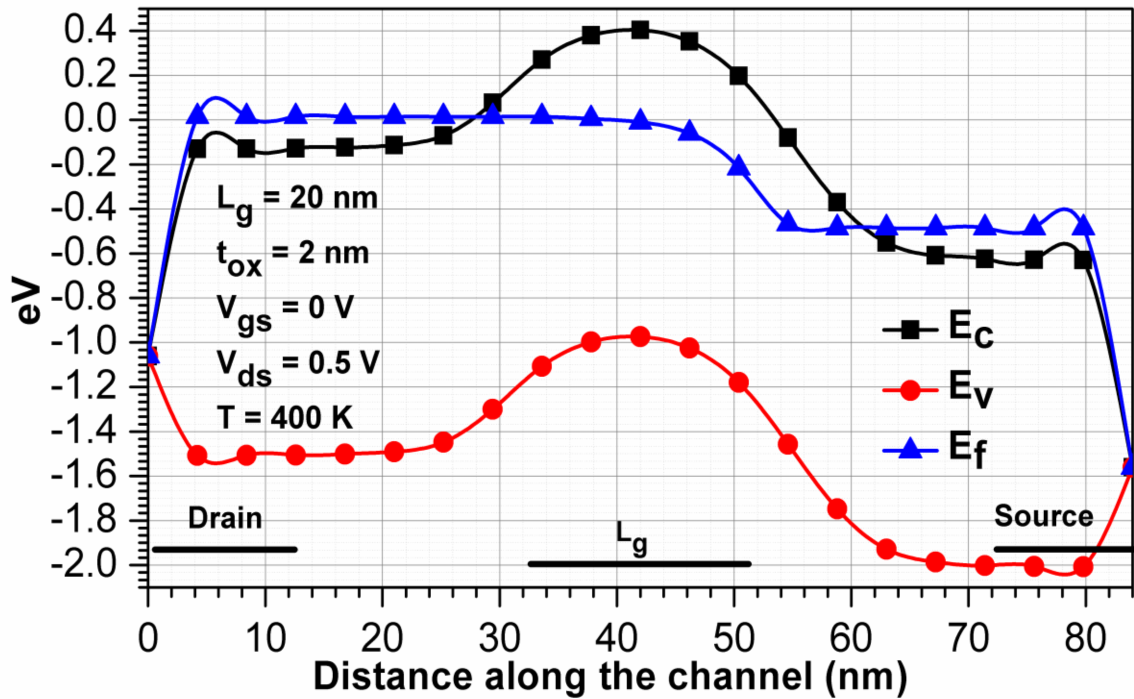


(c)

Fig. 4.3: Variation of band diagram with temperature when the device is in off state (a) T=200K (b) T=300K (c)T=400K.

In channel region, a decrease in the difference in Fermi level and conduction band can be related to the increase of charge carrier with the increasing temperature. As the temperature increase majority charge carrier increases and this is shown in Fig. 4.4 when the device is off. Temperature and charge carrier can be related by (2)[16].

$$n_i = 5.2\times10^{15}\times T^{3/2}\times\exp(-E_g/2kT) \qquad (2)$$

Where E_g is bandgap, T is the given temperature.

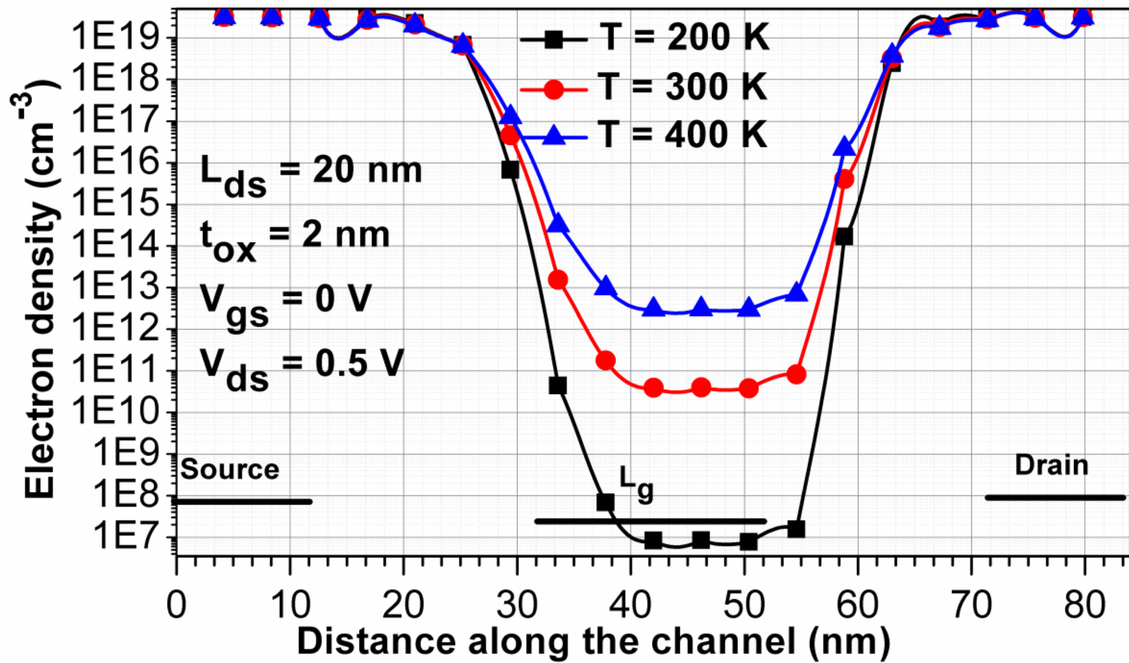


Fig. 4.4: variation of charge density when the device is in off state.

The temperature at which analysis is done, phonon scattering is more dominating and so mobility decreases with increasing temperature. This can be given by the equation (3)[17].

$$\mu_{eff} = \mu_{eff\,0}\,(T/T_0)^{-2} \qquad (3)$$

Where μ_{eff} is effective mobility, $\mu_{eff\,0}$ is effective mobility at 300 K, T_0 at 300 K and T is the temperature of the lattice.

Fig. 4.5 show the variation of electron mobility in the device with the temperature variation when the device is in off state. At off state charge density in the channel region

increases by a factor of 10^2 when the temperature is increased by 100 K. Charge density becomes a dominating factor in off state which results in an increase of leakage current.

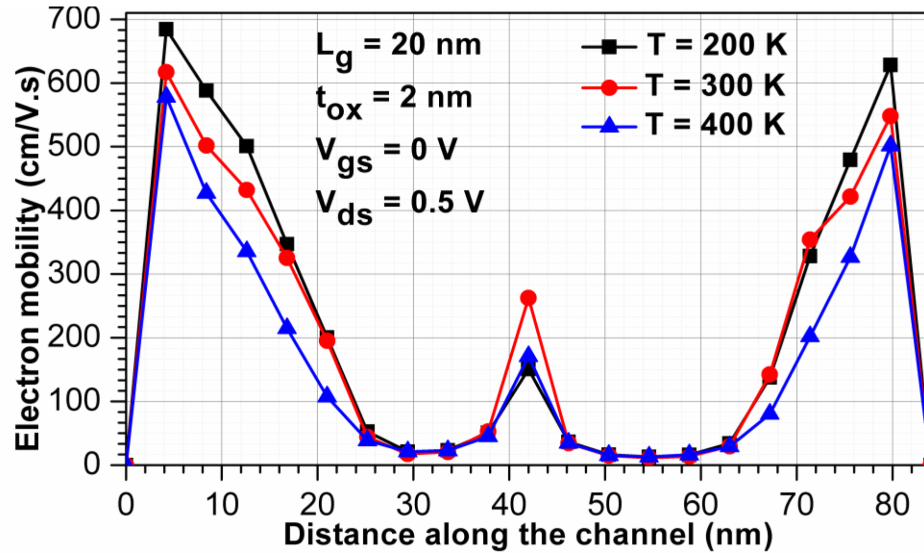
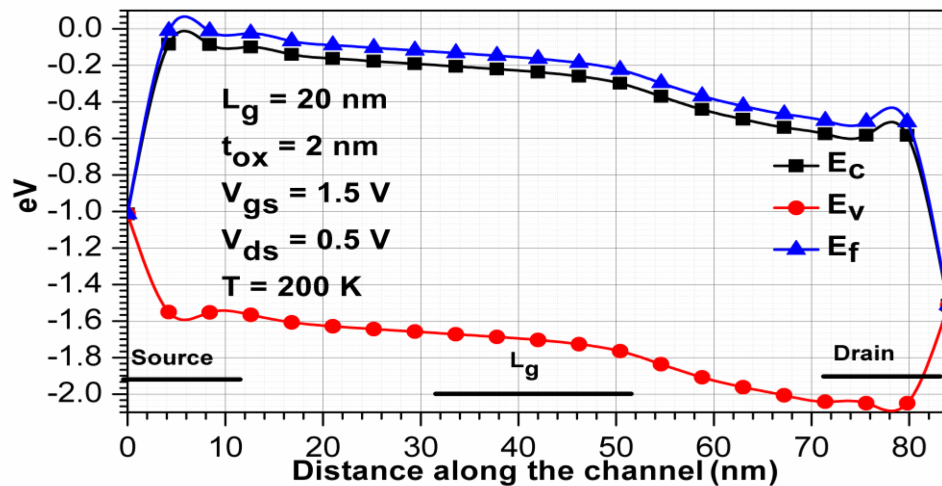


Fig. 4.5: Variation of mobility with temperature when the device is in off state.

Fig. 4.6 (a, b and c) shows the variation of the band diagram when the device is in on state. Fermi level goes into the conduction band due to higher doping in the Fin region. As the device is in saturation region difference in between the conduction band and Fermi level is constant for constant temperature. This difference increases with the increase in temperature.



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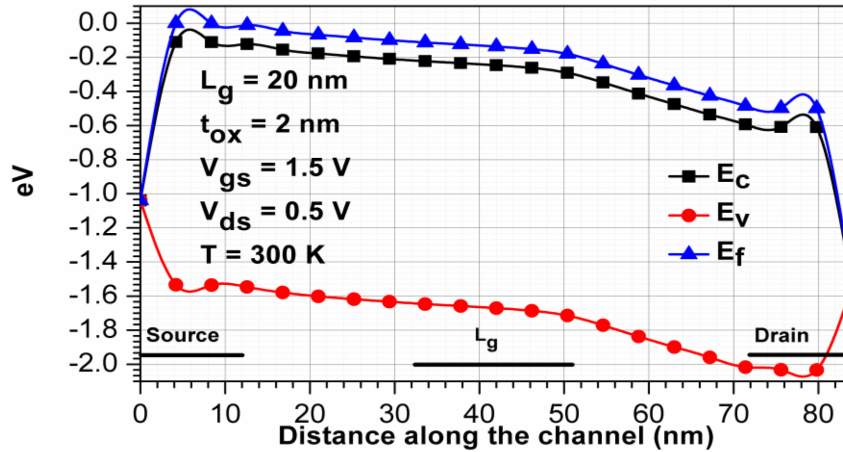

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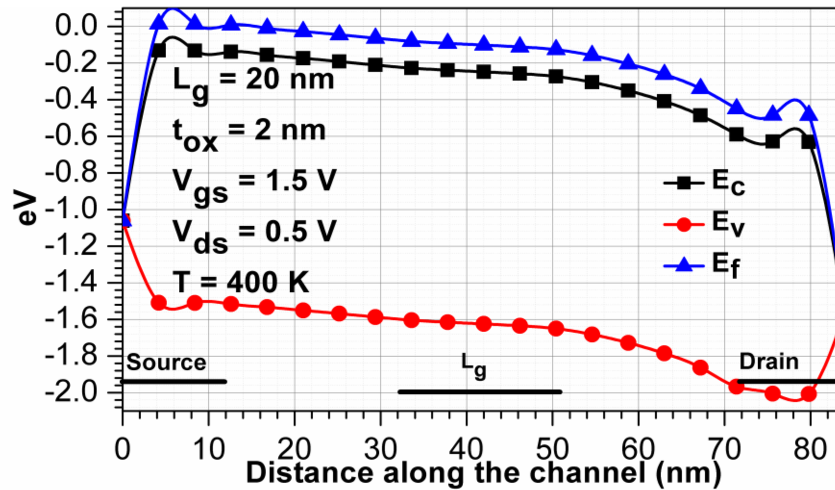


(c)

Fig. 4.6: variation of band diagram with temperature when device is in on state (a) T=200K (b) T=300K (c)T=400K

Fig. 4.7 shows the variation of charge density along the channel length. It is almost same in the channel region, but near the drain, region charge density decreases so less charge is collected at drain leading to less current. This is because at strong inversion, it is weakly dependent on temperature and at weak inversion; it is highly dependent on temperature. At on state, V_{gs} = 1.5 and V_{ds} = 0.5 V, as the gate voltage is at a higher voltage, so temperature dependence is less, but at lower drain voltage, the temperature dependence is more.

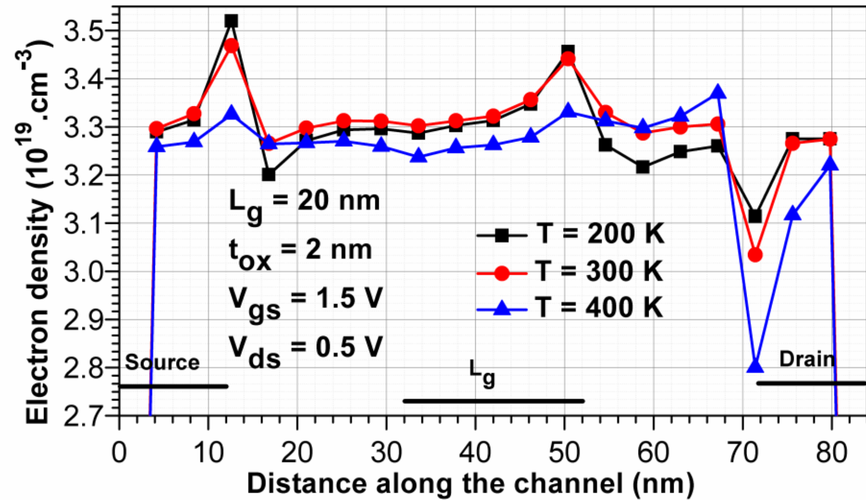


Fig. 4.7: Variation of electron charge density with the variation of temperature when the device is in on the state.

Fig. 4.8 shows the variation of mobility with temperature along the channel length. Mobility decreases slightly near the drain region, as the device is saturation region so charge density is almost same along the channel so current flow is majorly dependent on mobility, as mobility is reduced with temperature so overall there is slight decrease in current flow.

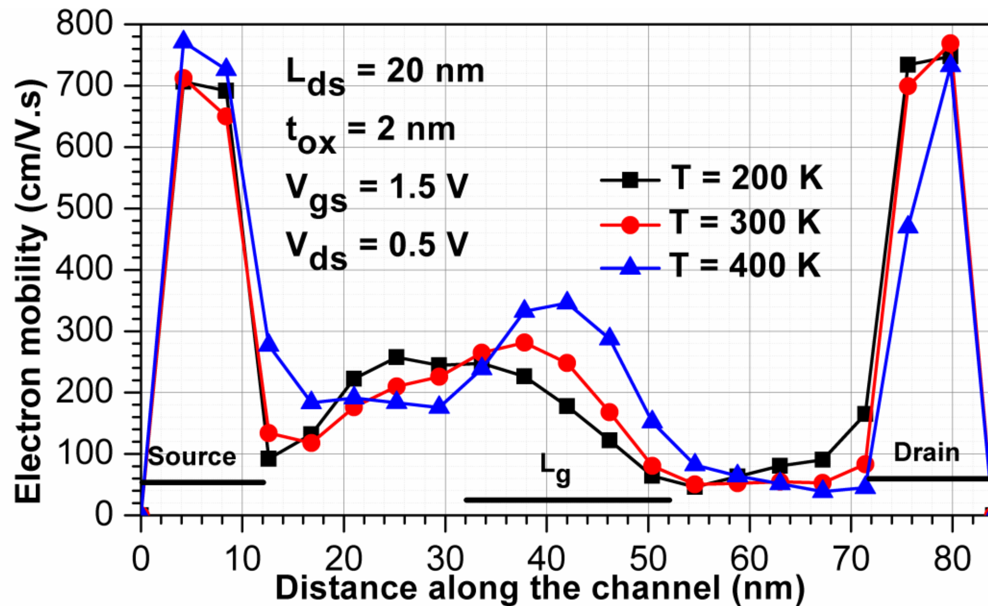


Fig. 4.8: Variation of electron mobility with the variation of temperature when the device is in on state.

CHAPTER 5

CONCLUSION

5.1 SUMMARY

MOSFET Scaling is done to keep Moore's law alive. Scaling increases the number of transistors on a single chip. But this decrease in size leads to many short channel effects. In this work, many short channel effects are summarized, and some of the methods are given to reduce them. To reduce these short channel effects, a new type of device was introduced named FinFET, which gets its name from the fin-like structure. Few types of FinFET's are explained.

Firstly, In this work a 3D JL SOI FinFET is designed using three different materials GaAs, Si and Ge using Silicon Nitride as a spacer and as a gate oxide. I_{on} is found to converge in range of 10^{-5} A for each of the material, but the difference is being observed in I_{off} among FinFETs. For GaAs, it is in the range of 10^{-12} A, and for Si and Ge, it is in the range of 10^{-8} A and 10^{-9} A respectively. Transconductance also shows much variation in the case of GaAs when compared to that of Si and Ge FinFET. GaAs based FinFET also changes quickly when the drain voltage is increased. The potential variation of GaAs FinFET is also found to be much more along the channel length in the Fin region.

Next, the 3D structure of GaAs JL-FinFET is designed using silicon nitride spacer and high-κ BOX and compared with conventional JL-FinFET. When Silicon Oxide box was replaced with a HfO_2 decrease in off current was noted. The device was compared with JL FinFET. I_{on} is found to be in the same range of 10^{-5} A, but the huge difference is found in case of I_{off} for both the devices. For GaAs, it is in the range of 10^{-15}, and for the conventional device, it is in the range of 10^{-8}. The higher potential difference in the channel region and higher depletion of majority charge carrier when no gate voltage is applied leads to lowering of sub-threshold current in the GaAs JL-FinFET. The proposed device can thus be used in designing the SRAM which requires higher switching speed and lower leakage current.

Further temperature analysis was done on this device. Drain current of the proposed device is compared with Conventional JL device at a different temperature and proposed device is found to have better switching ratio even with variation of temperature so that it can be considered as an alternative for SRAM. Effect of variation of temperature on charge density, band gap, and electron mobility is studied. At off state device current is found to depend on the charge density and at a higher voltage when the device is in on state device current is found to depend upon the mobility of the device.

5.2 FUTURE SCOPE:

- As switching ratio is one of the big criteria for SRAM. As SRAM are switching devices, they tend to heat up, and this heating effect can cause the increase in leakage current. The proposed device is found to have a good switching ratio, which remains in the appreciable range even at high temperature. It can be a considered as a good alternative, to be used in place of the conventional device. Also, as the channel length is nanometer range packing fraction will increase leading to more number of FinFETs in a single chip.

- As in the device high-κ materials are, it will increase the capacitance of the device. It can be used in various RF and microwave applications. Capacitance can increase the time delay of the device, so this device can be used where time delay does not have much effect on the overall circuitry.

- This device can be used as a temperature sensor. As switching ratio was found to decrease with the increase in temperature, it can be considered as one of the parameters.

- It can further be used as a protein biosensor. A grove can be formed in place of the spacer. On introduction of the nano-biomolecules, it can change the current flow. As protein has a dielectric constant of 8.1, it will provide with higher sensitivity when compared to APTES and streptavidin which has a dielectric constant of 3.57 and 2.1 respectively.

REFERENCES

[1] A. s. a. C. Smith, *Microelectronics circuits* vol. SEVENTH.

[2] G. S. a. S. K. Banerjee, *Solid state devices* vol. SEVENTH.

[3] I. Banglore. (31-August-2016). *nptel.ac.in/courses/117108047/3#*.

[4] R. R. e. al, "Comparison of Junctionless and Conventional Trigate Transistors With L_g down to 26 nm," *IEEE Electron Device Letters,* vol. 32, no. 9, pp. 1170-1172, Sept. 2011.

[5] C. Liu, F. Zheng, Y. Sun, X. Li, and Y. Shi, "Novel tri-independent-gate FinFET for multi-current modes control," *Superlattices and Microstructures,* 2017.

[6] M. Rostami and K. Mohanram, "Dual-$ V_ {th} $ independent-gate FinFETs for low power logic circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 30, pp. 337-349, 2011.

[7] C. Manoj, N. Meenakshi, V. Dhanya, and V. R. Rao, "Device optimization of bulk FinFETs and its comparison with SOI FinFETs," in *Physics of Semiconductor Devices, 2007. IWPSD 2007. International Workshop on*, 2007, pp. 134-137.

[8] R. Deshmukh, A. Khanzode, S. Kakde, and N. Shah, "Compairing FinFETs: SOI Vs Bulk: Process variability, process cost, and device performance," in *Computer, Communication and Control (IC4), 2015 International Conference on*, 2015, pp. 1-4.

[9] F. Karimi and A. A. Orouji, "Electro-thermal analysis of non-rectangular FinFET and modeling of fin shape effect on thermal resistance," *Physica E: Low-dimensional Systems and Nanostructures,* vol. 90, pp. 218-227, 2017.

[10] M.-H. Han, C.-Y. Chang, H.-B. Chen, Y.-C. Cheng, and Y.-C. Wu, "Device and circuit performance estimation of junctionless bulk FinFETs," *IEEE Transactions on Electron Devices,* vol. 60, pp. 1807-1813, 2013.

[11] R. Saha, B. Bhowmick, and S. Baishya, "Si and Ge step-FinFETs: Work function variability, optimization and electrical parameters," *Superlattices and Microstructures,* vol. 107, pp. 5-16, 2017.

[12] *Genius Semiconductor Device Simulator Version 1.7.4 Genius User's Guide*.

[13] N. Vinodhkumar, Y. Bhuvaneshwari, K. Nagarajan, and R. Srinivasan, "Heavy-ion irradiation study in SOI-based and bulk-based junctionless FinFETs using 3D-TCAD simulation," *Microelectronics Reliability,* vol. 55, pp. 2647-2653, 2015.

[14] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain*, et al.*, "Nanowire transistors without junctions," *Nature nanotechnology,* vol. 5, p. 225, 2010.

[15] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling," *IEEE Electron Device Letters,* vol. 32, pp. 261-263, 2011.

[16] D. Wolpert and P. Ampadu, "Managing temperature effects in nanoscale adaptive systems. 2011," *Google Scholar,* pp. 15-34.

[17] B. B. a. S. B. R. Saha, ""Effects of temperature on electrical parameters in GaAs SOI FinFET and application as digital inverter,"" presented at the 2017 Devices for Integrated Circuit (DevIC),, Kalyani,, 2017.

GaAs Junctionless FinFET Using Si3N4 Spacer for High performance Analog Application

Anuj Chhabra[1], Ajay Kumar[2] and Rishu Chaujar[1*]
[1*]*Applied Physics Department,* [2]*Electrical Engineering Department, Delhi Technological University, Delhi, India*
*[1]anuj.chhabra30@gmail.com, [2]ajaykumar@dtu.ac.in, [3]rishu.phy@dce.edu

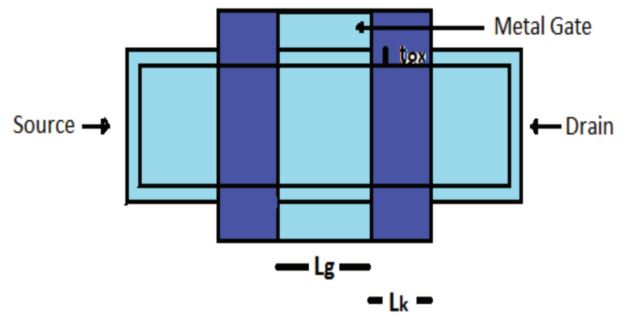
***Abstract*—This paper proposes GaAs junctionless FinFET which is compared with Si and Ge based junctionless FinFET and shows significant improvement. It is designed using metal gate and using Si3N4 as a spacer between gate and source/drain. Improved switching is observed for GaAs Junctionless FinFET as compared to Si and Ge devices. GaAs shows more variation of transconductance compared to Si and Ge FinFET which reflects the proposed device can be used to design SRAM as it is found to bring read stability and have less parasitic capacitance, less leakage current and higher switching speed.**

Keywords*—*FinFET, Junctionless, GaAs, spacer, Si, Ge.

I. Introduction

Effort is made to keep the Moore's law from reaching the saturation point. As the size of conventional FETs is decreased beyond a feature size, many short channel effects (SCE) [1-6] like drain induced barrier lowering (DIBL), threshold voltage roll-off, degradation of off current start to play an important role. To reduce these effects, many new alternative structures are being offered to keep the Moore's law intact. Many structures like Dual gate (DG)-FinFET, Tri Gate (TG)-FinFET, non-rectangular FinFET, novel tri-independent-gate FinFET are proposed [7, 8]. Junctionless FinFET is one such device. Junctionless device can be compared to a gated resistor in which we control the current flow by varying the conductivity using the gate voltage [9].

Junctionless device can be considered as a low resistance device in which gate voltage allows the semiconductor film of carriers to be depleted which modulates the conductivity of the charge. Junctionless devices are found to have the lower off (higher) current compared to the conventional FinFET [10]. In Silicon on insulator (SOI) FinFET, junction is isolated from the substrate while in case of bulk fin, it is directly connected to the substrate through an oxide layer. Oxide layer provides isolation from the bulk. Oxide provides the isolation between the different fins so different fins can be connected underneath the layer. SOI FinFET is found to have better threshold voltage roll-off and sub-threshold voltage swing values as compared to bulk FinFET [11]. In bulk, higher value of body doping does not always give better I_{on}/I_{off} ratio. The 3D nature of bulk FinFET's gives rise to additional device parasitic [12]. FinFET provide a better control over the channel as compared to the conventional FETs and show decrease in short channel effects. Metal gate are being used these days [13]. In this paper, we have compared different parameters of FinFET using different materials (Si, Ge and GaAs) based on VisualTCAD software.



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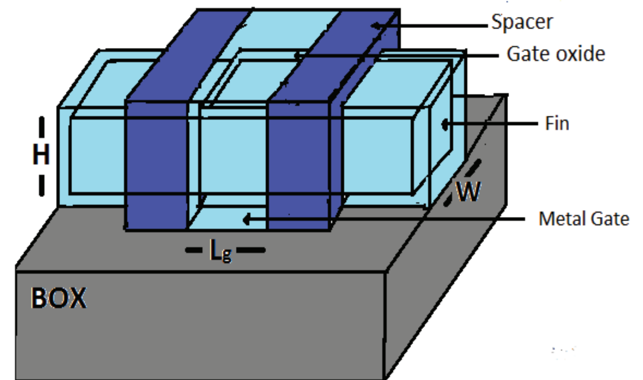


(b)

Fig.1 : (a) FinFET device top view (b) FinFET device 3D view.

II. Device Structure and Simulation Methodology

Fig. 1(a) and (b) show the basic structure of Junctionless FinFET used for simulation. VisualTCAD is used to create a 3D structure of the FinFET. Si_3N_4 is used a spacer between gate and source/drain as well as gate oxide for each simulation. Si_3N_4 is not compatible with polysilicon gate so metal gate is used instead [12, 14]. Si_3N_4 of thickness 8nm is used. Gate oxide is kept at 2nm constant thickness around the fin. Gold (Au) as metal gate contact is used. Work function of metal contact is adjusted to give optimal results. Metal contact should be made of different materials for compatibility but for fair comparison, same metal contact has been used. Thickness of gate metal contact is kept at 6 nm

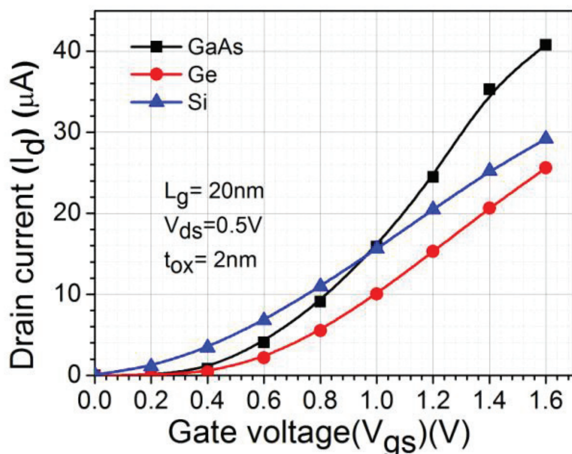
length. Gate length (Lg) is kept constant at 20 nm length. 2nm thick source and drain metal contact are used, made of Au. Fin of height (H) and width (W) of 10nm each is used for each simulation. Fin is made of three different materials; Si, Ge and GaAs. Fin extension lengths (L_k) are kept at 20nm distance from the channel. In junctionless device, a higher doping of range of 10^{19} cm^{-3} is kept to increase the I_{on} to an optimal level. Device is made n-type by using donor doping of N_d= 3.25×10^{19} cm^{-3} in each device. Since this is a junctionless device, so source and drain are also doped as Fin i.e 3.25×10^{19} cm^{-3}.

III. Simulation Results and Discussion

Si, Ge and GaAs are used to make 3 different devices which are compared. Fig. 2 (a, b) compares the change of drain current with the change in gate voltage at constant drain voltage. All the calculation are done at a constant drain voltage, V_{ds} =0.5V. GaAs is found to have more I_{on} which is 4.07×10^{-5} A and I_{on} for Si and Ge are found to be 2.99×10^{-5} A and 2.559×10^{-5} A respectively. I_{on} is calculated at gate voltage (V_{gs}) of 1.6V and drain voltage of V_{ds}=0.5V for each device. I_{off} is found to be in the range of 10^{-12} and for Si and Ge, I_{off} is found in the range of 10^{-8} A and 10^{-9} A respectively. Fig. 2(a) shows that increase of drain current is steep and shows less variation once threshold is reached but for Ge and Si, it shows more variation. Difference in I_{on} and I_{off} is because of the difference in bandgap and difference in mobility of each material. GaAs has higher bandgap and higher mobility as compared to Si and Ge. Metal gate shows more control in GaAs device.

Fig. 3 gives the variation of drain current as the drain voltage is increased. Gate voltage is kept constant at 1V for each of the material. GaAs show the steep rise in drain current after which it saturates in the range of 10^{-5} A but Si and Ge shows gradual increase in drain current with the increase in drain voltage.

Fig. 4 shows transconductance calculated for different gate voltages. Transconductance is calculated at V_{ds}=0.5 V. GaAs shows much variation in the transconductance as voltage is increased compared to Si and Ge FinFET. I_{on}/I_{off} values are calculated for Si, Ge and GaAs FinFET.



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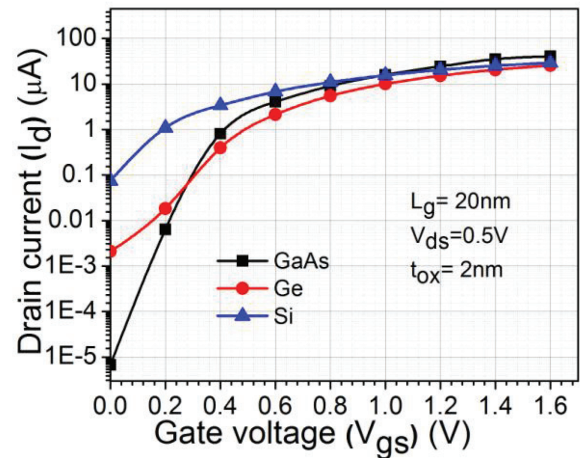


(b)

Fig. 2 (a) Variation of drain current as gate voltage is increased for Si, Ge and GaAs finFET with drain current in linear scale. (b) Variation of drain current as gate voltage is increased for Si, Ge and GaAs with drain current..

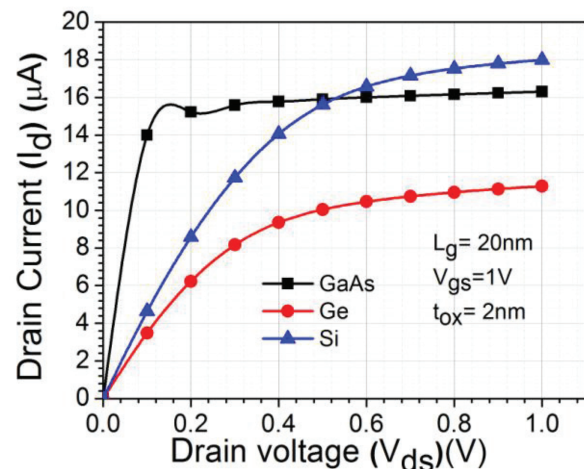


Fig. 3: Change in drain current Id w.r.t to change in drain voltage for Si, Ge and GaAs

I_{on}/I_{off} for these three materials is shown in Fig. 5. GaAs provides the value of 0.607×10^{7} μA/V which is better than that of Si and Ge which gives the value of 0.39×10^{3} μA/V and 1.24×10^{4} μA/V respectively. Transconductance variation in GaAs is more because of the higher change in I_{on}/I_{off} in the device.

In Fig. 6, potential change along the channel length is observed. In between the gate length i.e. from 32nm to 52nm, we observe steep change in potential. Potential is calculated at drain voltage of 0.5 V and gate voltage of 1V. For GaAs, this change is steep when compared to change in potential for Ge and Si. Fig. 7(a, b and c) shows the potential of different region of the FinFET at gate voltage (V_{gs}) of 1 V and drain voltage (V_{ds}) of 0.5 V for GaAs, Ge and Si. GaAs show more potential difference because of more control of gate on the device for same gate voltage. Because of higher potential difference in the GaAs Fin region, it shows more current when device is on.

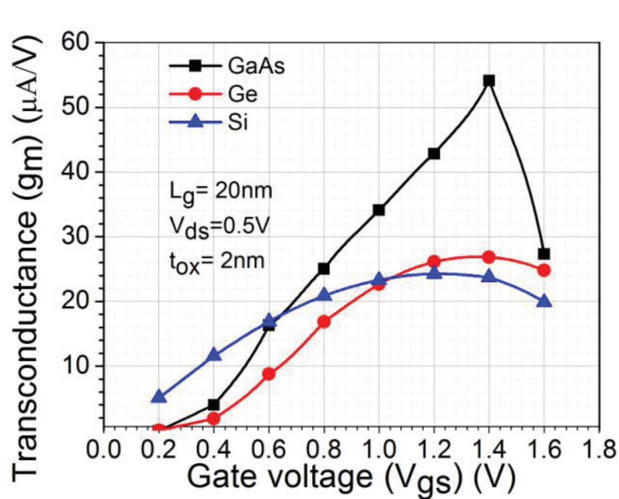


Fig. 4: Transconductance variation with change of gate voltage.

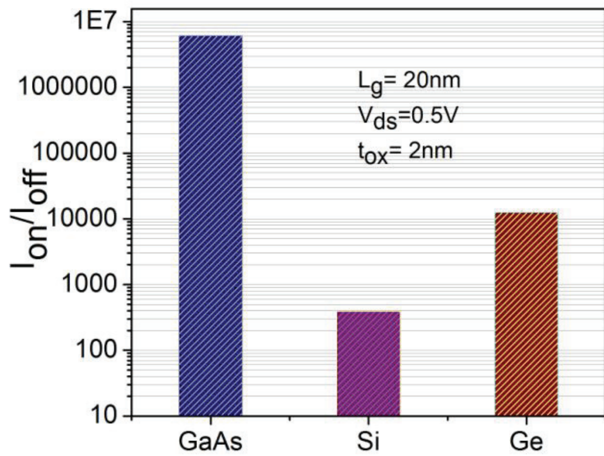


Fig. 5: Ion/Ioff for different materials.

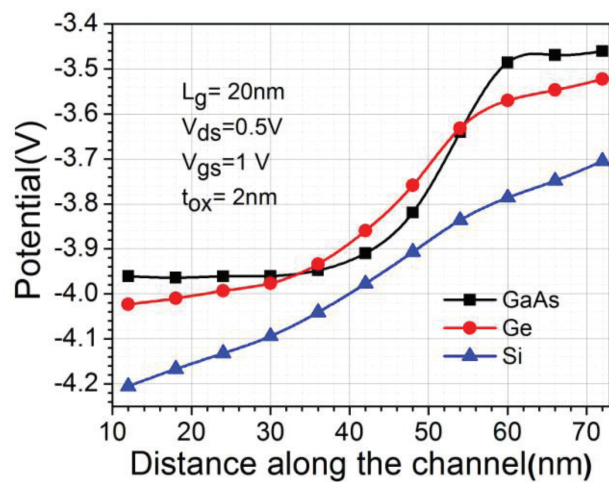
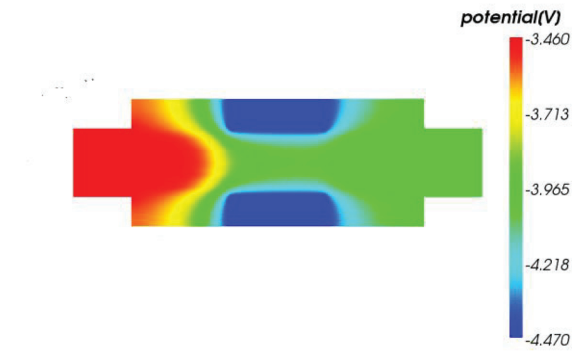


Fig 6: Potential variation along the channel length.



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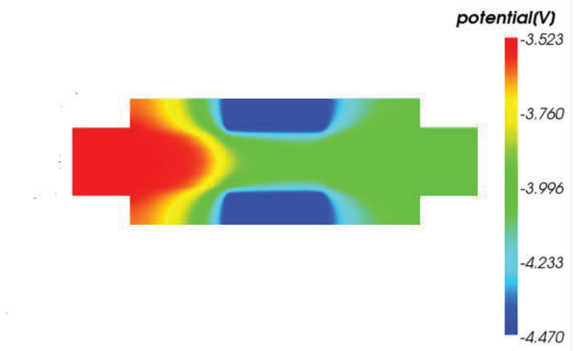

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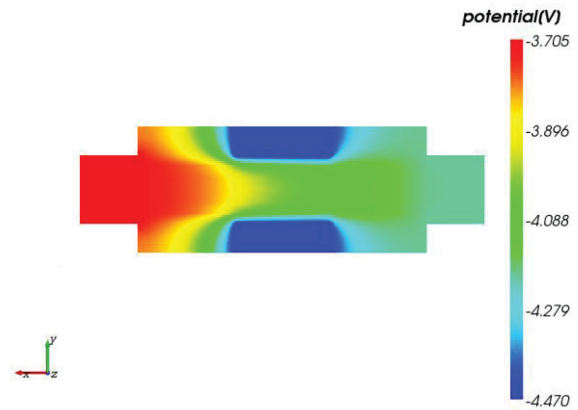

(c)

Fig 7: (a) potential along the device for GaAs. (b) potential along the device for Ge. (c) potential along the device for Si.

IV. Conclusion

3D structure of FinFET is designed using three different materials GaAS, Si and Ge. I_{on} is found to converge in range of 10^{-5} A for each of the material but difference is being observed in I_{off} among FinFETs. For GaAs, it is in the range of 10^{-12} A and for Si and Ge it is in the range of 10^{-8} A and 10^{-9} A respectively. Transconductance also shows much variation in the case of GaAs when compared to that of Si and Ge FinFET. GaAs based FinFET also changes quickly when drain voltage is increased. Potential variation of GaAs

FinFET is also found to be much more along the channel length in the Fin region. FinFET is used to design SRAM these days as it provides with higher switching speed, less leakage current, less parasitic capacitance compared to bulk structures.

ACKNOWLEDGEMENTS

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REFRENCES

[1] A. Kumar, N. Gupta, and R. Chaujar, "Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications," *Superlattices and Microstructures,* vol. 91, pp. 290-301, 3// 2016.

[2] A. Kumar, N. Gupta, and R. Chaujar, "TCAD RF performance investigation of Transparent Gate Recessed Channel MOSFET," *Microelectronics Journal,* vol. 49, pp. 36-42, 2016.

[3] A. Kumar, N. Gupta, and R. Chaujar, "Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET," *Microsystem Technologies,* pp. 1-8, 2016.

[4] A. Kumar, N. Gupta, and R. Chaujar, "Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour," *Microsystem Technologies,* vol. 22, pp. 2665-2671, 2016.

[5] A. Kumar, M. Tripathi, and R. Chaujar, "Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications," *Microsystem Technologies,* pp. 1-8.

[6] A. Kumar, "Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET," *Superlattices and Microstructures,* 2017.

[7] F. Karimi and A. A. Orouji, "Electro-thermal analysis of non-rectangular FinFET and modeling of fin shape effect on thermal resistance," *Physica E: Low-dimensional Systems and Nanostructures,* vol. 90, pp. 218-227, 2017.

[8] C. Liu, F. Zheng, Y. Sun, X. Li, and Y. Shi, "Novel tri-independent-gate FinFET for multi-current modes control," *Superlattices and Microstructures,* 2017.

[9] M. Poljak, V. Jovanović, and T. Suligoj, "Improving bulk FinFET DC performance in comparison to SOI FinFET," *Microelectronic Engineering,* vol. 86, pp. 2078-2085, 2009.

[10] M.-H. Han, C.-Y. Chang, H.-B. Chen, Y.-C. Cheng, and Y.-C. Wu, "Device and circuit performance estimation of junctionless bulk FinFETs," *IEEE Transactions on Electron Devices,* vol. 60, pp. 1807-1813, 2013.

[11] R. Deshmukh, A. Khanzode, S. Kakde, and N. Shah, "Compairing FinFETs: SOI Vs Bulk: Process variability, process cost, and device performance," in *Computer, Communication and Control (IC4), 2015 International Conference on*, 2015, pp. 1-4.

[12] C. Manoj, N. Meenakshi, V. Dhanya, and V. R. Rao, "Device optimization of bulk FinFETs and its comparison with SOI FinFETs," in *Physics of Semiconductor Devices, 2007. IWPSD 2007. International Workshop on*, 2007, pp. 134-137.

[13] R. Saha, B. Bhowmick, and S. Baishya, "Si and Ge step-FinFETs: Work function variability, optimization and electrical parameters," *Superlattices and Microstructures,* vol. 107, pp. 5-16, 2017.

[14] N. Vinodhkumar, Y. Bhuvaneshwari, K. Nagarajan, and R. Srinivasan, "Heavy-ion irradiation study in SOI-based and bulk-based junctionless FinFETs using 3D-TCAD simulation," *Microelectronics Reliability,* vol. 55, pp. 2647-2653, 2015.

GaAs Junctionless FinFET Using High-κ Dielectric for High-Performance Applications

Ajay Kumar[1], Anuj Chhabra[2] and Rishu Chaujar[2*]
[1]Department of Electrical Engineering
[2]Department of Applied Physics
Delhi Technological University,
Delhi, India

***Abstract*—This paper proposes GaAs junctionless (JL)-FinFET for high-performance applications. Results are so obtained and compared with conventional JL-FinFET. FinFET is designed using the metal gate and using Si_3N_4 as a spacer between gate and source/drain and using high-κ BOX. Output and input characteristics are compared. GaAs JL-FinFET is found to provide lower leakage current. Further, potential inside the device is studied which show decrease in potential in the channel region in off state. In energy band diagram, higher difference is observed between Fermi and conduction level showing less conduction in off state. Electron charge density inside the device is also studied which shows the depletion of majority charge carrier concentration in off state. FinFET is being used to design SRAM as it is found to bring read stability and is found to have less parasitic capacitance, less leakage current and higher switching speed.**

Keywords—FinFET; Junctionless; GaAs; spacer; High-κ dielectric

I. Introduction

With the advancement in technology, size of the devices is decreasing by Moore's law but as the size of the device is decreased, many new effects come into play which is called short channel effects. These short channel effects hinder Moore's law. These short channel effects include drain induced barrier lowering (DIBL) [1], threshold voltage roll-off and degradation of off current. Many structures like Dual gate (DG)-FinFET, Junctionless (JL)-FinFET, Tri-Gate (TG)-FinFET, non-rectangular FinFET, nanowire structures, novel tri-independent-gate FinFET are proposed[2-4]. FinFET helps in providing with better control over the channel region as compared to conventional devices[4]. Junctionless device acts as gated resistor in which gate voltage allows the semiconductor film of carriers to be depleted which modulates the conductivity of the charge. Junctionless devices deal with an issue of lower off current[5, 6]. In bulk devices, fin is directly connected with the substrate while in case of Silicon on insulator (SOI) fin and substrate layer are not connected directly, instead a layer of oxide is grown between fin and substrate. Oxide layer helps in providing better isolation as compared to bulk [5]. Silicon oxide can be replaced with high-k BOX and it helps in providing better I_{on}/I_{off} ratio [7] as compared to SOI device and the reduction in gate capacitance [8, 9]. Use of high κ-spacer increases the $I_{on}\backslash I_{off}$ ratio drastically but it is found to have increased delay time in the circuits [10]. Instead of using polysilicon as gate material, metal gate is being used. The work function of metal gates can be adjusted accordingly to give better results.

II. Device Structure and Simulation Methodology

Fig. 1 shows the structure of JL-FinFET with a spacer and the high-κ box is used for simulation. The 3D structure is simulated using VisualTCAD. Boltzmann statistics and drift-diffusion models are used for simulation [11]. For the proposed device fin is made of GaAs semiconductor and for conventional FinFET, it is made of Si. Si_3N_4 is used a spacer between gate and source/drain as it shows gate capacitance comparable to that of SiO_2 and shows less delay when compared to the high-κ spacer. Si_3N_4 is not compatible with a polysilicon gate, so the metal gate is used instead [12, 13].

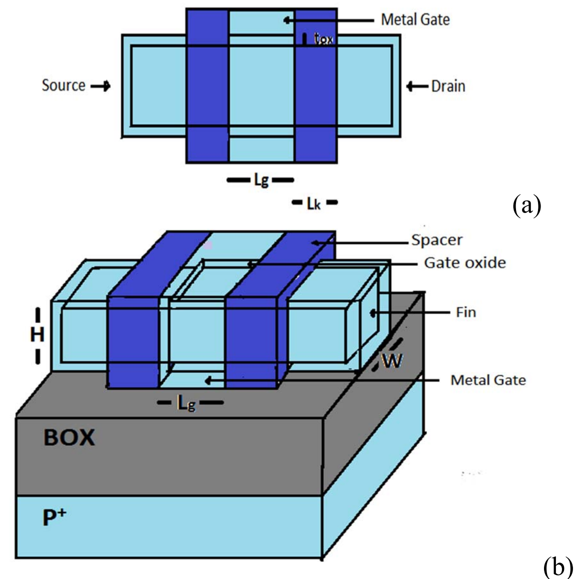

Fig. 1. (a) FinFET device top view; (b) FinFET device 3D view.

The thickness of Si_3N_4 spacer is kept constant at 8 nm. For fair comparison, gate oxide material is chosen to be Si_3N_4 of thickness 2 nm for conventional Junctionless FinFET as well as for the GaAs JL-FinFET using a spacer and high-k BOX. Au is used as a gate material for each simulation with the work function of 5.31 eV. For compatibility, the metal gate should be of different material, but for comparison, same metal is used. All the parameters were kept same for both the devices so that a

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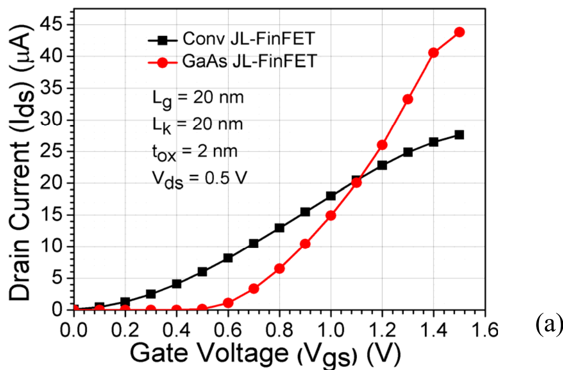
clear comparison can be made. Gate length (L_g) was kept constant at 20 nm as well as gate extensions (L_k), i.e., the distance between gate and source/drain was also kept constant at 20 nm. Higher donor doping of $N_d = 10^{19}$ cm^{-3} is used for junctionless devices to get appreciable I_{on}. Source and drain are also doped with $N_d = 10^{19}$ cm^{-3}. Source and drain metal contacts of thickness 2 nm are used. BOX of thickness 20 nm is used. For conventional JL-FinFET BOX is of SiO_2 while for GaAs JL-FinFET BOX is made of HfO_2 which has high dielectric constant. The heavily doped ground plane is used of thickness 20 nm with acceptor doping of 3.25×10^{18} cm^{-3}.

III. Simulation Results and Discussion

GaAs JL-FinFET and conventional JL-FinFET is compared. Fig. 2 (a, b) shows the variation of drain current (I_{ds}) with the change in gate voltage (V_{gs}) at a constant drain voltage (V_{ds}) of 0.5 V. In conventional device, threshold voltage is achieved at a very low gate voltage of about 0.1 V as compared to GaAs JL-FinFET, for which it is close to 0.5 V. At saturation i.e Vgs = 1 V, both devices show almost same current in the range of 10^{-5}. For GaAs JL-FinFET, it is found to be 1.49×10^{-5} A and for the conventional device, it is found to be 1.8×10^{-5} A. I_{off} shows the major difference in both the devices. For proposed device, it is found to be in the range of 10^{-15} whereas for a conventional device, it is 10^{-8}. Fig. 3 shows the I_{on}/I_{off} for both devices. For conventional device, it is 2.36×10^{2} but for GaAs JL- FinFET it is 3.08×10^{9}.



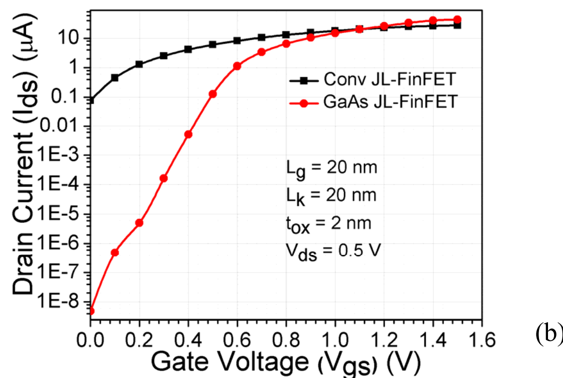


Fig. 2. (a) Variation of drain current as the gate voltage is increased for conventional JL-FinFET and GaAs JL-FinFET with drain current; (b) Variation of drain current as the gate voltage is increased for conventional JL-FinFET and GaAs JL-FinFET with drain current.

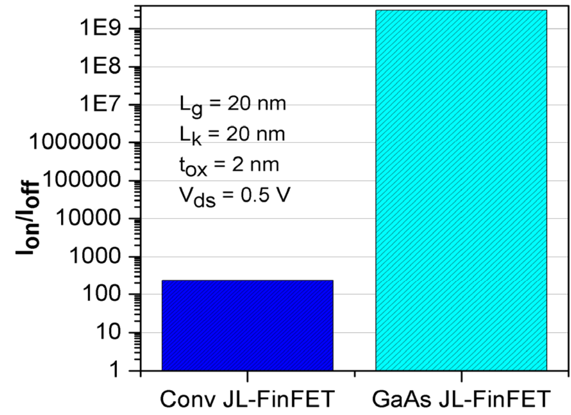


Fig. 3. I_{on}/I_{off} for conventional and GaAs JL-FinFET.

Fig. 4 reflects the variation of drain current with the change in V_{ds} at two constant gate voltages, i.e. $V_{gs} = 0.5$ and $V_{gs} = 0.1$ V. It can be observed that for a for lower gate voltage, the leakage current is very less for GaAs JL-FinFET as compared to the conventional device. Subthreshold current is in the range of 10^{-13} A and 10^{-7} A for GaAs JL-FinFET and conventional JL-FinFET respectively.

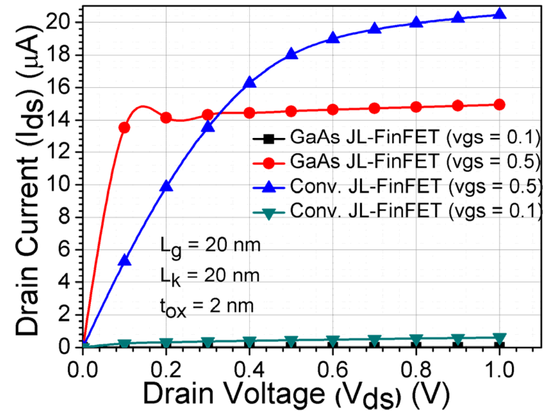


Fig. 4. Change in drain current Id w.r.t to change in drain voltage for conventional and GaAs JL-FinFET.

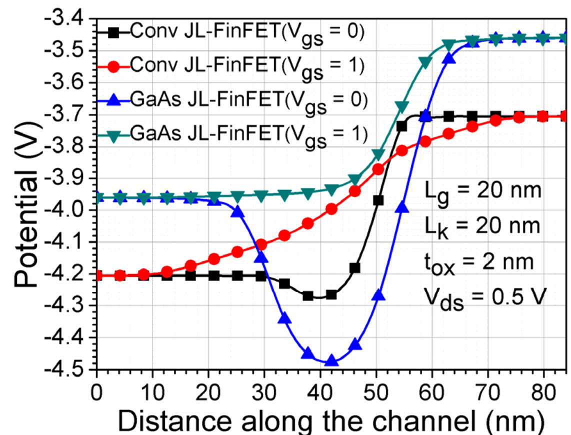
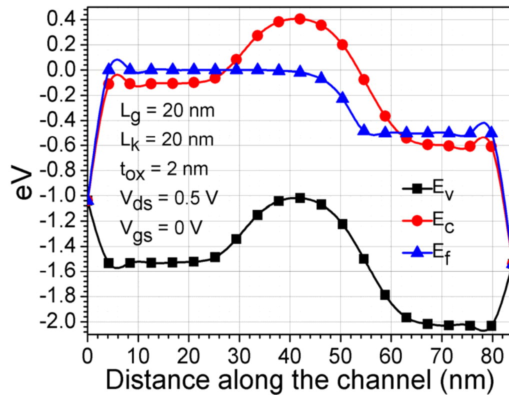


Fig. 5. Potential variation along the channel length.

Fig. 5 Show the variation of potential along the channel for two devices. When devices are in off state i.e. when V_{gs} is 0 V, a potential barrier is formed in the channel region, i.e., between 32 nm to 52 nm. Dip in potential is almost six times for GaAs JL-FinFET as compared to the conventional device. Because of increased potential lowering in case of GaAs JL-FinFET, leakage current is less as compared to the conventional device. In saturation region, potential in the channel region is almost linear for conventional device showing little higher current.

Fig. 6 (a, b) show the band diagram of the devices. In channel region, difference in case of GaAs JL-FinFET between the Fermi level and conduction is more when compared to the conventional device. Because of higher difference in between Fermi level and conduction level, less charge is present in the conduction band which reduces the drain leakage current. In Fig. 7 (a, b), when V_{gs} = 1V the difference in Fermi level and conduction band is constant in the channel region and is comparable to the difference in Fermi level and conduction level in source and drain region showing the device is in saturation region for both the devices.



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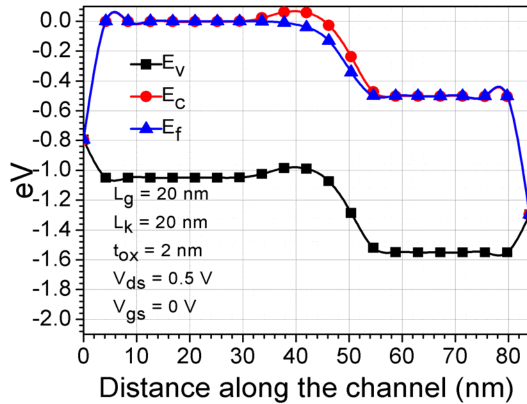
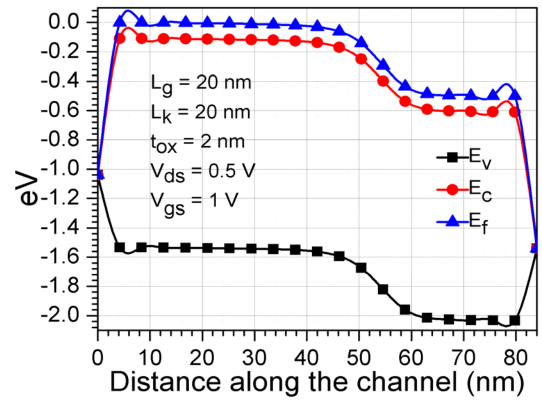


(b)

Fig. 6. (a) Band diagram of GaAs JL-FinFET when device is in off state; (b) Band diagram of Conventional JL-FinFET when device is in off state



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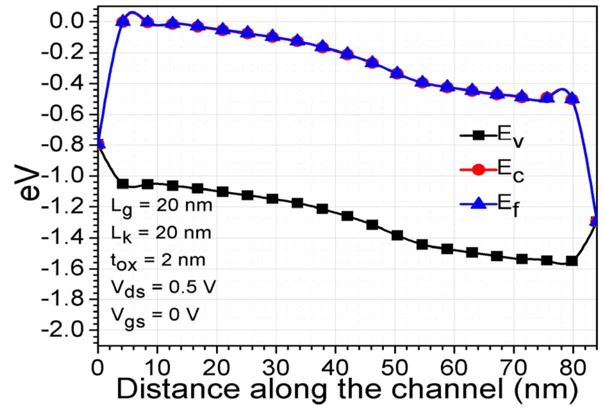

(b)

Fig. 7. (a) Band diagram of GaAs JL-FinFET when the device is in on state; (b) Band diagram of Conventional JL-FinFET when the device is in on state.

Fig. 8 (a, b) show the electron concentration when the device is OFF, or V_{gs} = 0 V at constant V_{ds} = 0.5 V. In case of GaAs JL-FinFET, higher density is near the source and drain region only. When zero bias is applied, the channel region is depleted of majority charge carriers. Holes are attracted towards channel region as metal gate has majority electrons, so opposite charges are attracted in the channel region. Because of higher majority charge depletion in case of GaAs JL-FinFET, it shows lower leakage current. Fig. 8 (c, d) show electron concentration when the device is ON or V_{gs} = 1 V. When the gate voltage is positive, electrons are attracted towards the gate material in the channel region showing a decrease in minority charge carrier and increase in majority charge carriers near the channel region which increase the conductivity of the device.

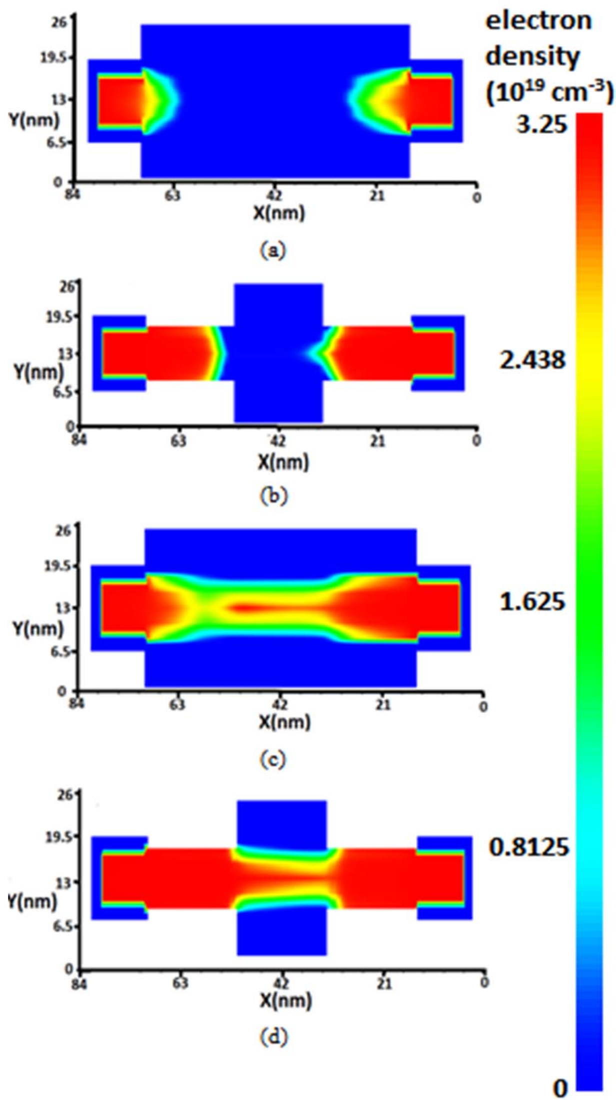

Fig. 8. Contours plots of (a) Electron charge density variation in GaAs JL-FinFET in off state. (b) Electron charge density variation in conventional JL-FinFET in off state. (c) Electron charge density variation in GaAs JL-FinFET in on state. (d) Electron charge density variation in conventional JL-FinFET in on state.

IV. Conclusion

In this work, the 3D structure of GaAs JL-FinFET is designed using silicon nitride spacer and high-κ BOX and compared with conventional JL-FinFET. I_{on} is found to be in the same range of 10^{-5} A, but huge difference is found in case of I_{off} for both the devices.. For GaAs, it is in the range of 10^{-15}, and for the conventional device, it is in the range of 10^{-8}. The higher potential difference in the channel region and higher depletion of majority charge carrier when no gate voltage is applied leads to lowering of sub-threshold current in the GaAs JL-FinFET. The proposed device can thus be used in designing the SRAM which requires higher switching speed and lower leakage current.

Acknowledgements

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References

[1] A. Kumar, N. Gupta, and R. Chaujar, "Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour," *Microsystem Technologies,* vol. 22, pp. 2665-2671, 2016.

[2] F. Karimi and A. A. Orouji, "Electro-thermal analysis of non-rectangular FinFET and modeling of fin shape effect on thermal resistance," *Physica E: Low-dimensional Systems and Nanostructures,* vol. 90, pp. 218-227, 2017.

[3] C. Liu, F. Zheng, Y. Sun, X. Li, and Y. Shi, "Novel tri-independent-gate FinFET for multi-current modes control," *Superlattices and Microstructures,* 2017.

[4] C. Manoj, N. Meenakshi, V. Dhanya, and V. R. Rao, "Device optimization of bulk FinFETs and its comparison with SOI FinFETs," in *Physics of Semiconductor Devices, 2007. IWPSD 2007. International Workshop on*, 2007, pp. 134-137.

[5] R. Deshmukh, A. Khanzode, S. Kakde, and N. Shah, "Compairing FinFETs: SOI Vs Bulk: Process variability, process cost, and device performance," in *Computer, Communication and Control (IC4), 2015 International Conference on*, 2015, pp. 1-4.

[6] M.-H. Han, C.-Y. Chang, H.-B. Chen, Y.-C. Cheng, and Y.-C. Wu, "Device and circuit performance estimation of junctionless bulk FinFETs," *IEEE Transactions on Electron Devices,* vol. 60, pp. 1807-1813, 2013.

[7] A. Kumar, M. Tripathi, and R. Chaujar, "Reliability Issues of In2O5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature," *IEEE Transactions on Electron Devices,* vol. 65, pp. 860-866, 2018.

[8] S. Sahay and M. J. Kumar, "Realizing efficient volume depletion in SOI junctionless FETs," *IEEE Journal of the Electron Devices Society,* vol. 4, pp. 110-115, 2016.

[9] A. Kumar, M. Tripathi, and R. Chaujar, "Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications," *Microsystem Technologies,* vol. 23, pp. 5867-5874, 2017.

[10] N. Surana, J. Mekie, and N. Ranjan Mohapatra, *Impact of high-κ spacer on circuit level performance of junctionless FinFET*, 2017.

[11] *Genius Semiconductor Device Simulator Version 1.7.4 Genius User's Guide*.

[12] R. Saha, B. Bhowmick, and S. Baishya, "Si and Ge step-FinFETs: Work function variability, optimization and electrical parameters," *Superlattices and Microstructures,* vol. 107, pp. 5-16, 2017.

[13] N. Vinodhkumar, Y. Bhuvaneshwari, K. Nagarajan, and R. Srinivasan, "Heavy-ion irradiation study in SOI-based and bulk-based junctionless FinFETs using 3D-TCAD simulation," *Microelectronics Reliability,* vol. 55, pp. 2647-2653, 2015.

Effect of Temperature on GaAs Junctionless FinFET Using High-κ Dielectric

Anuj Chhabra
Applied Physics Department
Delhi Technological University
Delhi, India
anuj.chhabra30@gmail.com

Ajay Kumar
Electrical Engineering Department
Delhi Technological University
Delhi, India
ajaykumar@dtu.ac.in

Rishu Chaujar
Applied Physics Department
Delhi Technological University
Delhi, India
chaujar.rishu@dtu.ac.in

***Abstract*— In this paper, the effect of temperature on GaAs Junctionless (JL) FinFET using high-κ dielectric has been studied at 200K, 300K, and 400K. JL FinFET, a sub-20nm device is designed using GaAs as Fin material. High-κ material is used as BOX and as a spacer. Drain current is compared with the conventional JL device. Switching ratio is enhanced by 2.58×10^7 times and I_{on} is also increased by 70% in the proposed device as compared to JL FinFET at low temperature (200K). I_{on} is found to decrease for GaAs JL FinFET with increasing temperature (200K to 400K), which is opposite to that of the conventional device. Even with the decrease of on current with temperature, I_{on} shows 18% increase as compared to JL FinFET. Further, the effect of temperature on band gap, electron mobility, and charge density is studied along the channel length. It is found that mobility plays an important role in the GaAs JL device when the device is on, and charge density plays an important role when the device is off. Higher switching ratio can be used in SRAM and as the high-κ material is used, the device can be a good alternative for RF and microwave application in the sub-20nm regime.**

Keywords*— *FinFET, Junctionless, GaAs, spacer, High-κ dielectric.

I. Introduction

Scaling is done on the devices to decrease the size of the devices to keep up with Moore's law. But when scaling is done on the conventional devices, off current increases and short channel effects come into play. Short channel effects (SCE) is one of the major issues in the semiconductor MOSFET's, with the increase in temperature this issue gets worse due to increasing off current. To reduce SCEs, many new devices are proposed such as Dual- gate (DG) FinFET, Trigate (TG) FinFET, Tri-independent gate, Junctionless (JL) FinFET[1-3] Junctionless Devices are the devices in which no junction is formed, and uniform doping is done in the device. It acts as a gated resistor in which current flow is maintained by applying different voltages at the gate. With the change in voltage, charge accumulation or charge inversion inside the gate region is achieved which controls the flow inside the device[4-6] Generally there is two type of FinFETs; SOI and Bulk FinFET. In SOI type FinFET, Fin is not connected with the substrate, but in Bulk FinFET, Fin is directly connected with the substrate. SOI type provides better insulation between the substrate and Fin, and it reduces the leakage current, but SOI devices suffer from self-heating effect, so it becomes extremely important to find the effect of temperature on the device. On replacing-

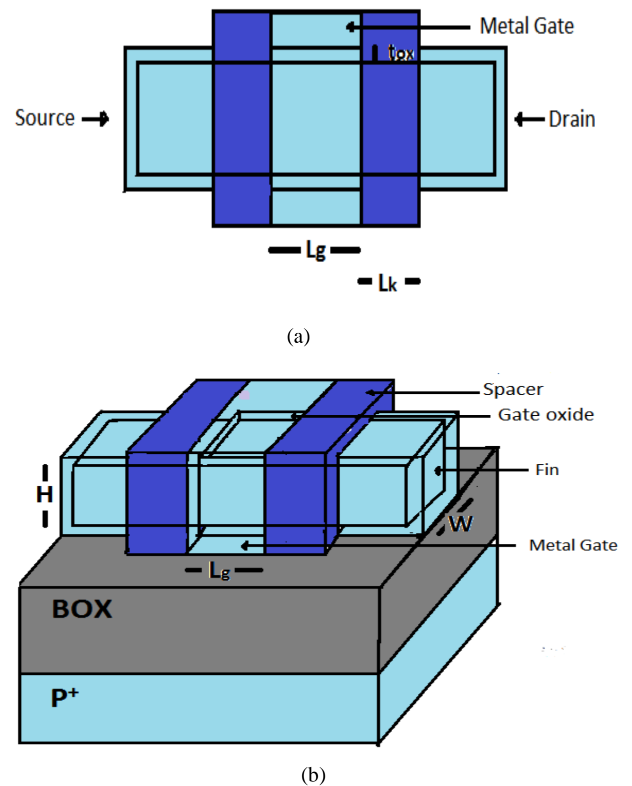


Fig.1 : (a) FinFET device top view (b) FinFET device 3D view.

Silicon-oxide with HfO_2 (high-κ material), off current or leakage current, is decreased[7]. Including high-κ material makes it difficult to find the effect of temperature on the device[8]. Including spacer also decreases the off current and helps to reduce the short channel effects in the device. Instead of using polysilicon, metal gate contacts are used[9] and GaAs is used as a fin material instead of silicon which reduces the short channel effects [10].

II. Device Structure and Simulation Methodology

VisualTcad is used to create the 3D model of the device. Fig 2 shows the calibration of the software with [11]. In this simulation drift-diffusion model and Boltzmann statistics is

used. Since junctionless device use higher doping to achieve higher on current, so band gap narrowing model has been -

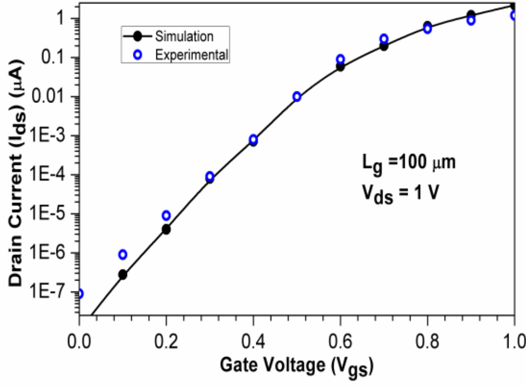


Fig. 2: calibration of software with the experimental data.

-used. As FinFET is a three-dimensional device so high transverse and lateral electric field models are included.

Recombination rate is calculated using the sum of auger and Shockley read hall recombination [12]. Channel doping of N_d of 3.25×10^{19} cm^{-3} is done. As the device is a JL device source and drain doping is same as a channel. Gate length (L_g) is kept at 20 nm. Source and drain extension of 20 nm is used. Gold is used as gate material. Work Function of 5.31 is used. In junctionless device higher work function has to be used to get an optimal result. HfO_2 and substrate doping of 20 nm thickness each is used. Substrate doping of $N_a = 1\times10^{19}$ cm^{-3} is done, this helps in achieving less leakage current with the use of substrate bias. Si_3N_4 is used as spacer of height 8 nm and width 20 nm.

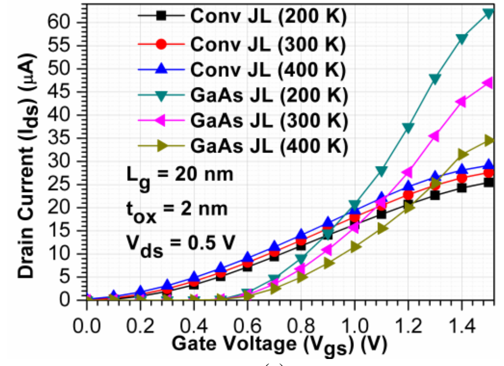
III. Simulation Results and Discussion

GaAs junctionless device is compared with the Conventional junctionless device. All the parameters are kept same for both the devices to get a fare comparison in both the devices. Fig 3 (a, b)compares the drain current with change in gate voltage at different temperatures at a constant drain voltage V_{ds}= 0.5 V. For conventional device at T=300 K switching ratio is in close relation as given in the [13] at 20 nm. It is observed that for almost same on current there is a large increase in off current for both the devices. Even at high-temperature GaAs JL FinFET provides with better switching ratio as compared to Conventional JL FinFET. GaAs JL FinFET. GaAs JL device has increased in leakage current with the increase in temperature but at higher voltage current decreases for GaAs JL device. Because of the use of high-κ materials prediction of various temperature effects is difficult. It was observed that percentage change in time delay was constant with reduction of temperature, opposite to that of conventional devices. [8].

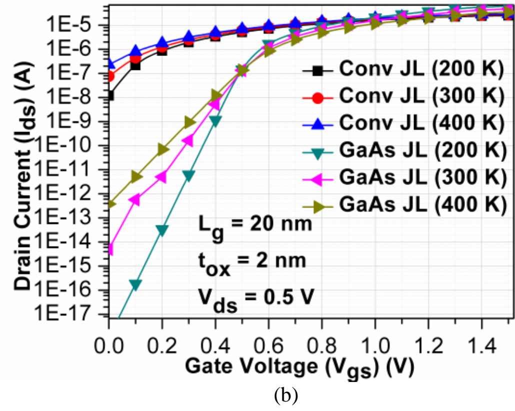
Fig 4 (a, b and c) compares the change in variation of band diagram inside the device at different temperature at V_{ds} = 0.5 V and when the device is in off state. With the increase of temperature difference in Fermi level and conduction band increases in source and gate region which shows the higher off-current with increasing temperature. The relation between band gap and temperature can be given by (1)[8].

$$E_g(T) = E_g(0) - \alpha_E T^2/(T + \beta_E) \quad (1)$$

Where, α for GaAs = 5.41×10^{-4} eV/K, β = 204 K and E_g = 1.519 eV.



(a)



(b)

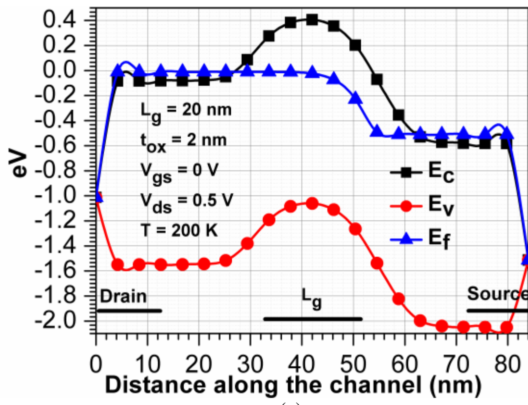
Fig. 3: (a, b) Variation of drain current at constant drain voltage at a different temperature.

In channel region, a decrease in the difference in Fermi level and conduction band can be related to the increase of charge carrier with the increasing temperature. As the temperature increase majority charge carrier increases and this is shown in Fig. 5 when the device is off. Temperature and charge carrier can be related by (2)[8].

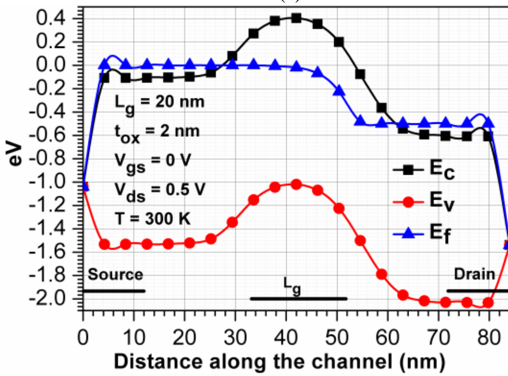
$$n_i = 5.2\times10^{15}\times T^{3/2}\times\exp(-E_g/2kT) \quad (2)$$

Where E_g is bandgap, T is the given temperature.

The temperature at which analysis is done, phonon scattering is more dominating and so mobility decreases with increasing temperature. This can be given by the equation (3)[10].



(a)



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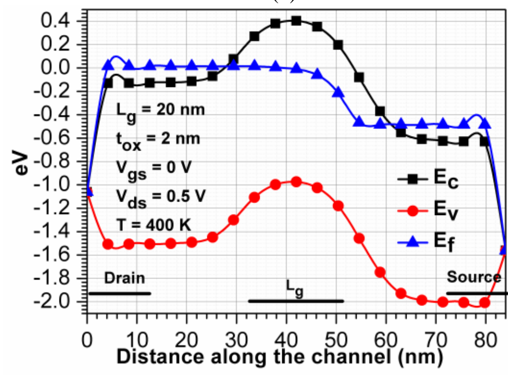

(c)

Fig. 4: variation of band diagram with temperature when the device is in off state (a) T=200K (b) T=300K (c)T=400K.

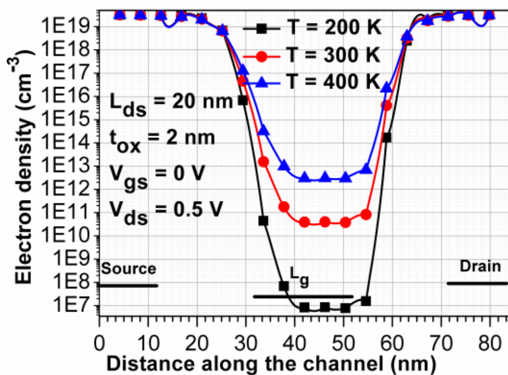

Fig. 5: variation of charge density when the device is in off state.

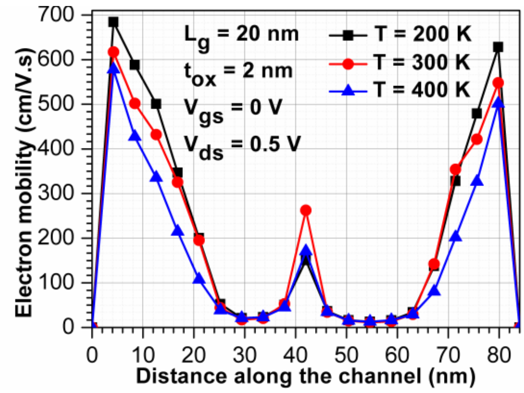

Fig. 6: Variation of mobility with temperature when the device is in off state.

$$\mu_{eff} = \mu_{eff\,0}\left(T/T_0\right)^{-2} \quad (3)$$

Where μ_{eff} is effective mobility, $\mu_{eff\,0}$ is effective mobility at 300 K, T_0 at 300 K and T is the temperature of the lattice.

Fig. 6 show the variation of electron mobility in the device with the temperature variation when the device is in off state. At off state charge density in the channel region increases by a factor of 10^2 when the temperature is increased by 100 K. Charge density becomes a dominating factor in off state which results in an increase of leakage current.

Fig. 7 (a, b and c) shows the variation of the band diagram when the device is in on state. Fermi level goes into the conduction band due to higher doping in the Fin region. As the device is in saturation region difference in between the conduction band and Fermi level is constant for constant temperature. This difference increases with the increase in temperature.

Fig. 8 shows the variation of charge density along the channel length. It is almost same in the channel region, but near the drain, region charge density decreases so less charge is collected at drain leading to less current. This is because at strong inversion, it is weakly dependent on temperature and at weak inversion; it is highly dependent on temperature. At on state, V_{gs} = 1.5 and V_{ds} = 0.5 V, as the gate voltage is at a higher voltage, so temperature dependence is less, but at lower drain voltage, the temperature dependence is more. Fig. 9 shows the variation of mobility with temperature along the channel length. Mobility decreases slightly near the drain region, as the device is saturation region so charge density is almost same along the channel so current flow is majorly dependent on mobility, as mobility is reduced with temperature so overall there is slight decrease in current flow.

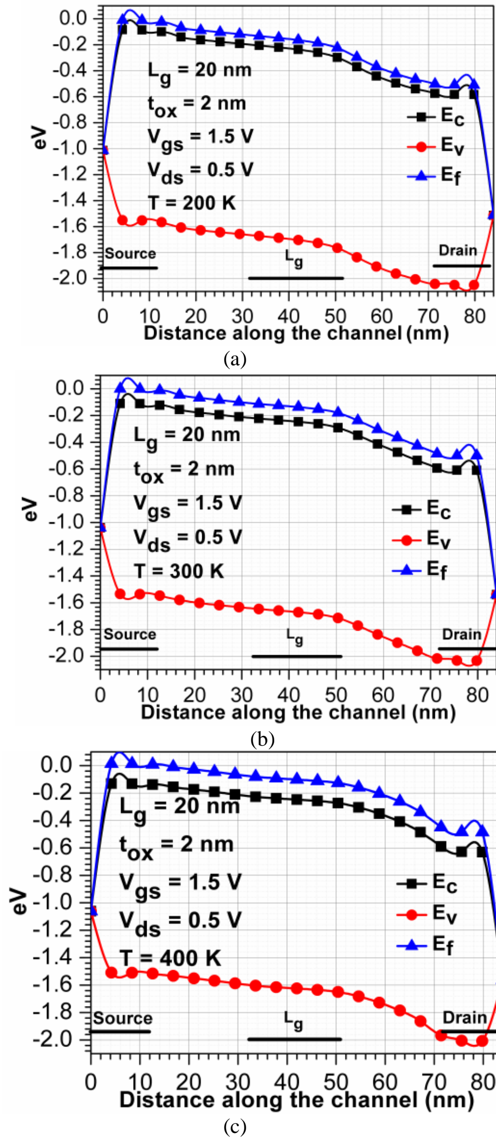

Fig. 7: variation of band diagram with temperature when device is in on state (a) T=200K (b) T=300K (c)T=400K

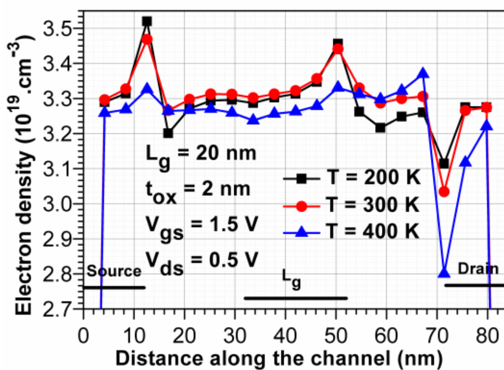

Fig. 8: Variation of electron charge density with the variation of temperature when the device is in on the state

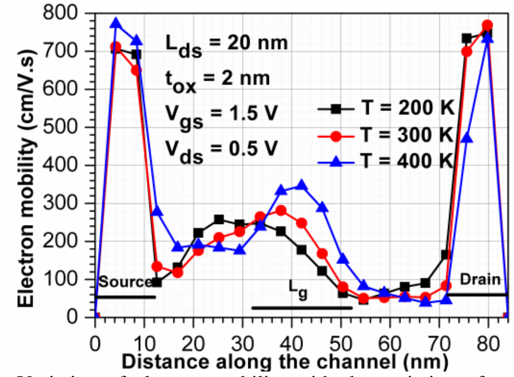

Fig. 9: Variation of electron mobility with the variation of temperature when the device is in on state.

IV. CONCLUSION

In this work, the 3D structure of GaAs JL-FinFET is designed using silicon nitride spacer and high-κ BOX and compared with conventional JL-FinFET. Drain current of the proposed device is compared with Conventional JL device at different voltages and proposed device is found to have better switching ratio even with variation of temperature so that it can be considered as an alternative for SRAM. Use of high-κ material increases the device capacitance so it can be used for RF and microwave applications as well. Effect of variation of temperature on charge density, band gap, and electron mobility is studied. This device can be used as a temperature sensor by considering switching ratio an important parameter.

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REFERENCES

[1] F. Karimi and A. A. Orouji, "Electro-thermal analysis of non-rectangular FinFET and modeling of fin shape effect on thermal resistance," *Physica E: Low-dimensional Systems and Nanostructures,* vol. 90, pp. 218-227, 2017.

[2] C. Liu, F. Zheng, Y. Sun, X. Li, and Y. Shi, "Novel tri-independent-gate FinFET for multi-current modes control," *Superlattices and Microstructures,* 2017.

[3] C. Manoj, N. Meenakshi, V. Dhanya, and V. R. Rao, "Device optimization of bulk FinFETs and its comparison with SOI FinFETs," in *Physics of Semiconductor Devices, 2007. IWPSD 2007. International Workshop on*, 2007, pp. 134-137.

[4] " Semiconductor on Insulator Materials for Nanoelectronics Applications," pp. 187-200.

[5] R. Deshmukh, A. Khanzode, S. Kakde, and N. Shah, "Compairing FinFETs: SOI Vs Bulk: Process variability, process cost, and device performance," in *Computer, Communication and Control (IC4), 2015 International Conference on*, 2015, pp. 1-4.

[6] M.-H. Han, C.-Y. Chang, H.-B. Chen, Y.-C. Cheng, and Y.-C. Wu, "Device and circuit performance estimation of junctionless bulk FinFETs," *IEEE Transactions on Electron Devices,* vol. 60, pp. 1807-1813, 2013.

[7] S. Sahay and M. J. Kumar, "Realizing efficient volume depletion in SOI junctionless FETs," *IEEE Journal of the Electron Devices Society,* vol. 4, pp. 110-115, 2016.

[8] D. Wolpert and P. Ampadu, "Managing temperature effects in nanoscale adaptive systems. 2011," *Google Scholar,* pp. 15-34.

[9] N. Surana, J. Mekie, and N. Ranjan Mohapatra, *Impact of high-κ spacer on circuit level performance of junctionless FinFET*, 2017.

[10] B. B. a. S. B. R. Saha, ""Effects of temperature on electrical parameters in GaAs SOI FinFET and application as digital inverter,"" presented at the 2017 Devices for Integrated Circuit (DevIC),, Kalyani,, 2017.

[11] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain*, et al.*, "Nanowire transistors without junctions," *Nature nanotechnology,* vol. 5, p. 225, 2010.

[12] *Genius Semiconductor Device Simulator Version 1.7.4 Genius User's Guide*.

[13] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling," *IEEE Electron Device Letters,* vol. 32, pp. 261-263, 2011.