M. Tech (VLSI AND EMBEDDED SYSTEMS) CHETAN ASTHANA 2018

A DISSERTATION
ON
TRANSMITTER USING GROUNDED COMPLEX CAPACITOR
SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI and Embedded Systems

Submitted by:

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CONTENTS

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CANDIDATE'S DECLARATION

I, Chetan Asthana, Roll No. 2K16/VLS/06 student of M.Tech. (VLSI and Embedded Systems), hereby declare that the project Dissertation titled "TRANSMITTER USING GROUNDED COMPLEX CAPACITOR " which is submitted by me to the Department of Electronics and Communications, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "TRANSMITTER USING GROUNDED COMPLEX CAPACITOR " which is submitted by Chetan Asthana, Roll No 2K16/VLS/06 Electronics and Communications, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi **Prof. Dr. Rajeshwari Pandey**

Date: **SUPERVISOR**

ACKNOWLEDGEMENT

I would like to thank my supervisor Prof. Dr. Rajeshwari Pandey for giving me this opportunity to learn the topic and simulate one of its applications, and always motivating me throughout the project and providing me her guidance without which this project completion would not have been possible.

Secondly, I would like to thank my parents and my friends who kept encouraging me and the ECE department of Delhi Technological University for being my support.

Chetan Asthana

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ABSTRACT

The project deals with simulation of grounded complex capacitor ,using which as a low pass filter a time varying signal is band limited and the band limited signal is given to a signal processing block which removes the DC offsets from the complex filter output and an amplifier which converts few milli volt signal to a 10 volt peak signal. This was done because the next stage (analog to digital converter) was not compatible to milli volt signal; therefore the signal had to be amplitude amplified. Then the signal is sampled and converted into digital equivalent by using a counter type analog to digital converter. The analog to digital converter used in the project also uses a digital to analog converter. The opamp based weighted digital to analog converter is used in the project for this purpose. The digital bits when converted back to analog voltage is then compared to the input analog voltage and accordingly the digital bits are upgraded. The upgradation of the digital bits is done by the digital counter. Here 4 bit up counter is used for the same. The results were verified using Spice simulation which came out to be in line with the theoretical expectations

List Of Tables

List Of Abbreviations

Abbreviation	Meaning
MOS	Metal Oxide Semiconductor
N-MOS	N Channel MOS
P-MOS	P channel MOS
A/D	Analog To Digital Converter
D/A	Digital To Analog Converter
TG	Transmission Gate
CMRR	Common Mode Rejection Ratio
PM	Phase Margin
GM	Gain Margin
IC	Integrated Circuit
g_m	Transconductance
KHz	Kilo Hertz
R	Resistor
Vin	Input Voltage
Clk	Clock
I/O	Input/Output
u(unit)	Micro(unit)
Kn	MOS Parameter
Vtn	NMOS Threshold Voltage
Vtp	PMOS Threshold Voltage
Opamp	Operational Amplifier
Vo	Output Voltage
KCL	Krichhoff's Current Law
KVL	Krichhoff's Voltage Law

CHAPTER 1

Literature Survey And Motivation For The Project

1.1 Motivation

The motivation for the project came from the benefits of the complex filter that it can handle 2 signals one in phase and the other quadrature phase signal. Complex filters and systems are even able to eliminate the image signal problem faced in super hetrodyne receiver. Quadrature phase multiplexing of signals also was one of the motivating factors to go for the project. If in the transmission line both in phase and quadrature signals are sent, even though they occupy the same frequency spectrum, they won't interfere due to the 90 degree phase difference between them .This will reduce the bandwidth requirement of the transmission line and one can use the channel economically.

In these complex filters or more generally complex system, the transfer function is complex in nature which means that it has 2 components in phase and quadrature part.

1.2 Literature survey

1.2.1 Complex signal

It is a signal which has 2 signals in it, one is in phase and the other is out of phase

$X= x1 + jx2$

Complex signal processing is not a new concept theoretically … it has been studied since the time of Fourier analysis.

As Fourier said that **any** periodic signal can be represented in the form of sum of weighted complex exponentials …. which later had a correction that it was not **any** but it was applicable for only those periodic signals which satisfy Dritchlet conditions.

1.2.2 Why complex signal processing?

1. Even though its realization does the same work as real signal processing, still complex signal processing leads to simple and compact signal flow graphs of the system.

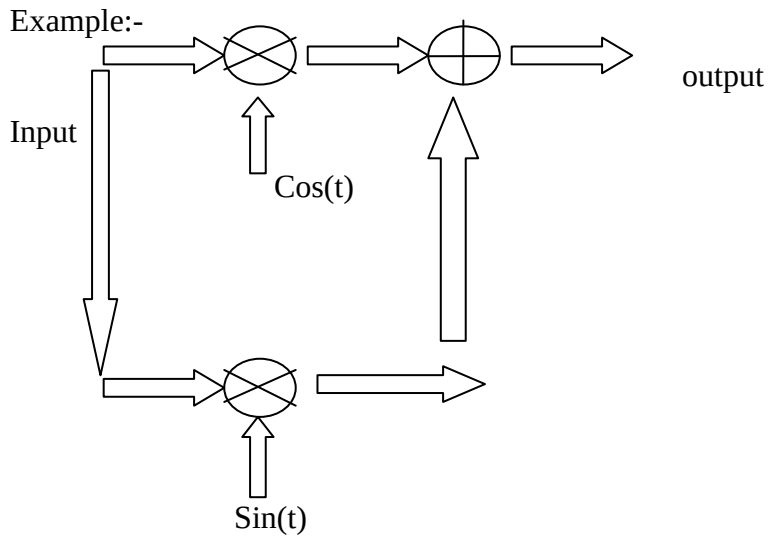


Figure 1.1 a) Complex Multiplication

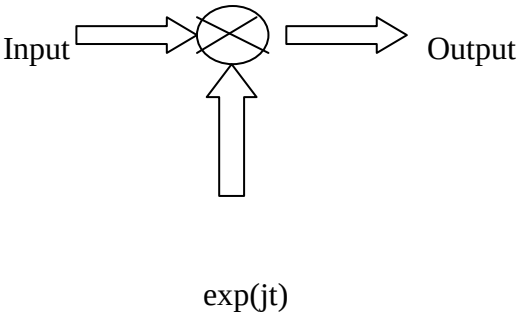


Figure 1.1b) complex exponential multiplication

2. In super heterodyne receiver the problem of images occurs because when we multiply with cos() or sin() the frequency spectrum is shifted 2 sided and not just one side, but in complex signal processing :-

   X(t)exp(jWot)=X(W-Wo)

   The spectrum X(W) will shift only in 1 side thereby the problem of images is gone .

1.2.3 Meaning of Complex

In mathematics complex numbers are defined with reference to a complex plane.

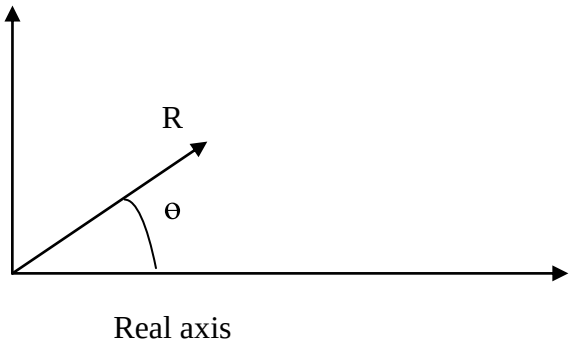


Figure1.2 complex plain [7]

The above figure represents the rectangular coordinate system in complex plane.

But if the y axis is imaginary, how it is visible?

In electrical engineering complex numbers have a very practical meaning. The real axis represents the in phase or the reference signal and the imaginary axis represents the quadrature component … any signal can be represented using these to orthogonal signals, which is nothing but the rectangular representation of a complex signal. So the electrical engineering does not start with $j = \sqrt{-1}$ but it specifies that j represents 90 degree phase shift with respect to the reference signal.

1.2.4 Complex operations

As in real signals complex signals also have multiplication, addition, subtraction, integrations, etc. with additional property of conjugation.

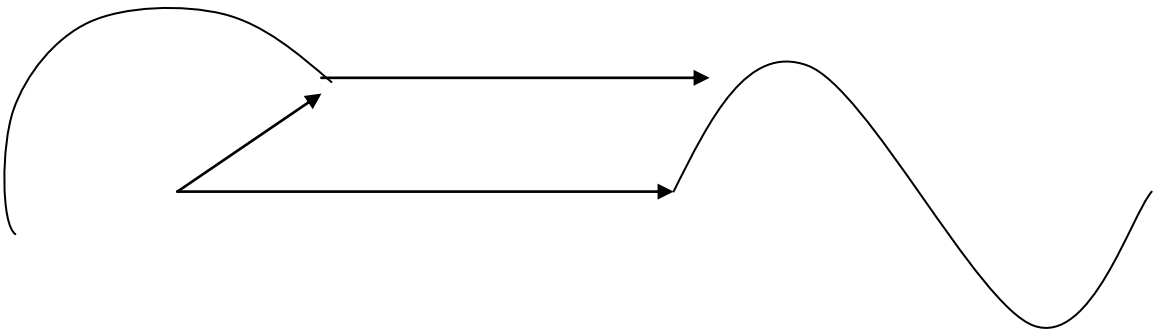
Conjugation represents changing the sign of quadrature signal component and keeping the in phase component intact. Moreover, the complex signals can be represented in the polar as well as rectangular form also.

1.2.4.1 Changing of rectangular to polar representation

Rectangular representation of a complex signal= a + bj

Polar form=R(Ɵ)

Where R is the magnitude of the resultant signal and Ɵ is the phase of the same.



Rotating magnitude rectangular signal

Figure1.3 Polar to Rectangular

The projections of polar system result in the instantaneous wave forms which is nothing but the rectangular system to represent the complex signals.

1.2.5 Explaining the negative frequencies

-10 Hz seems to be a wrong information as it has a negative frequency which may have no physical significance. Even though it has not got any physical significance because as far as definition of frequency is concerned it says the number of cycles covered in one second represents the frequency of the signal. There is no physical significance of the negative frequency, but without representing the negative frequencies theoretically one cannot justify the power sectrum of a signal.

Example:-

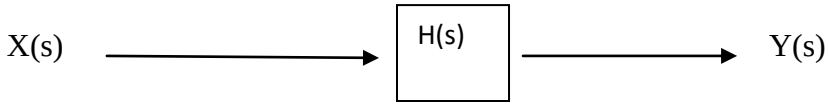
Figure 1.4 Understanding Negative Frequency

The above is the spectrum representation of the signal $A_c\cos(wot)$ which has power = $\frac{Ac^2}{2}$, if we calculate the power by using Parsavel's theorem without negative frequency

component we get only half power , and my multiplying the signal by a sin(w_1t) and passing through the spectrum analyzer, the scientists observed that there exists frequencies w_1-w_0 also in the spectrum of the resultant signal which was not possible without having the negative frequency $-w_0$.

1.2.6 Complex filters

These filters do not have complex symmetry like the real filters .



If H(s) = R(s)+jQ(s)

And X(s) = Xi(s)+jXq(s)

Therefore, Y(s) = H(s)X(s)

= [Xi(s)R(s)-Xq(s)Q(s)]+j[XqR+Q(s)Xi(s)]

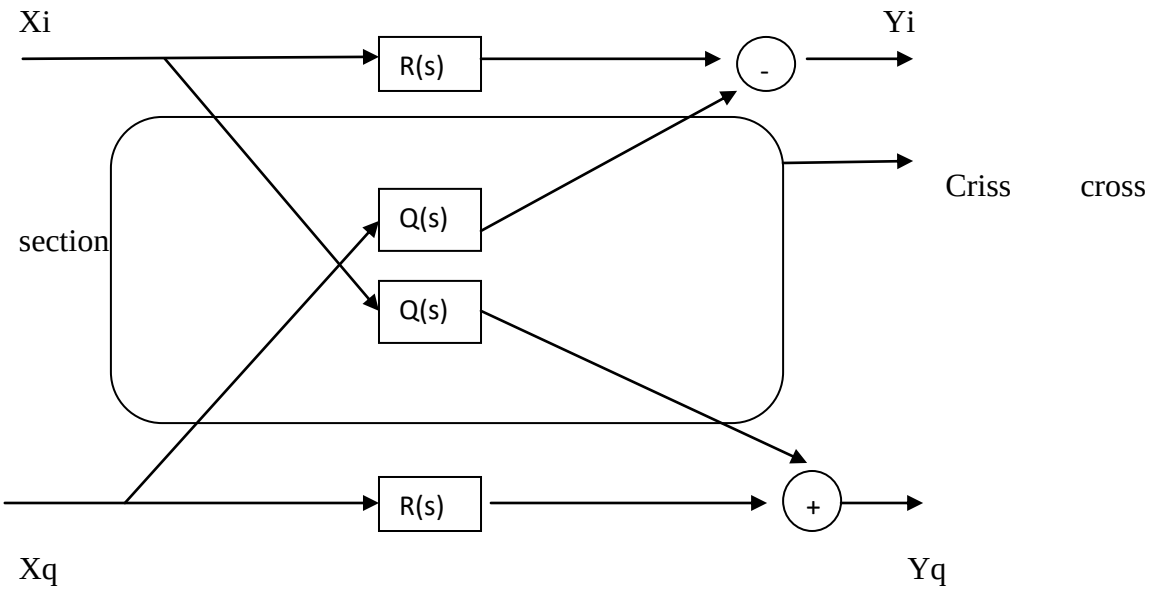


Figure 1.5 Complex System

The criss cross block as shown in the figure is common in all the complex filters.These can process 2 signals at a time.

The problem of images will vanish only when the balanced complex multiplication that is:-

a1=a2 (here =R(s)) in figure shown above

b1=b2(here=Q(s)) in above figure

If they are not equal and balanced they will result in signal components with the unwanted frequency spectrum which can be eliminated by using notches at that particular frequency.

1.2.7 Shifting the frequency

Considering a capacitor of admittance = sC now shifting s we have (s-jwo)C we can have a complex filter of the form :-

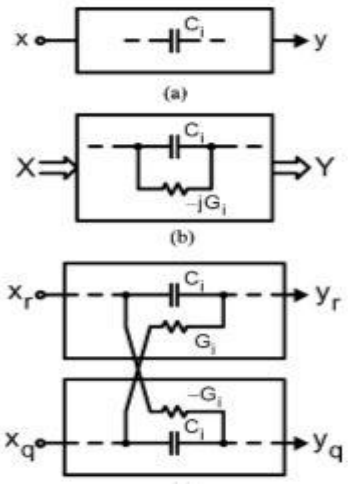


Figure 1.6 Frequency Shift In Capacitor[1]

CHAPTER 2

Simulating Complex filters

2.1 Example of complex lossy integrator

Here the project has simulated a lossy complex integrator and realized the complex low pass filter using 1.5u m technology CMOS implementation .

Symbolic circuit:-

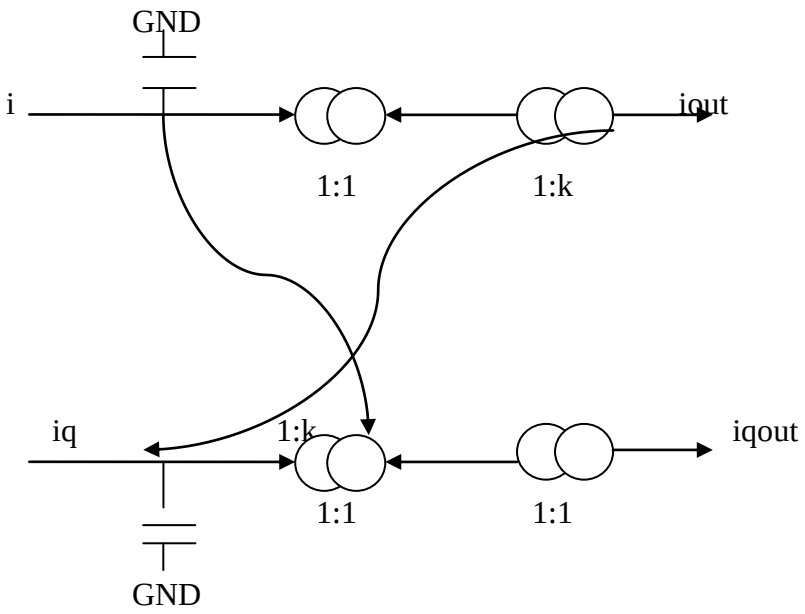


Figure2.1 Complex Lossy Integrator [2]

The above figure shows complex Lossy Integrator. The bubbles show a current mirror with the given W/L ratios, iq and i are the quadrature and inphase components of the current. Iout and Iqout are the output in phase and quadrature currents. The arrows shown in the figure show the criss cross section which is always present in a complex system. The iout is taken out from the current mirror transistor but if a MOS is considered, the necessary amount of drain to source voltage is to be supplied to the transistor to keep it in saturation and mirror the exact current.

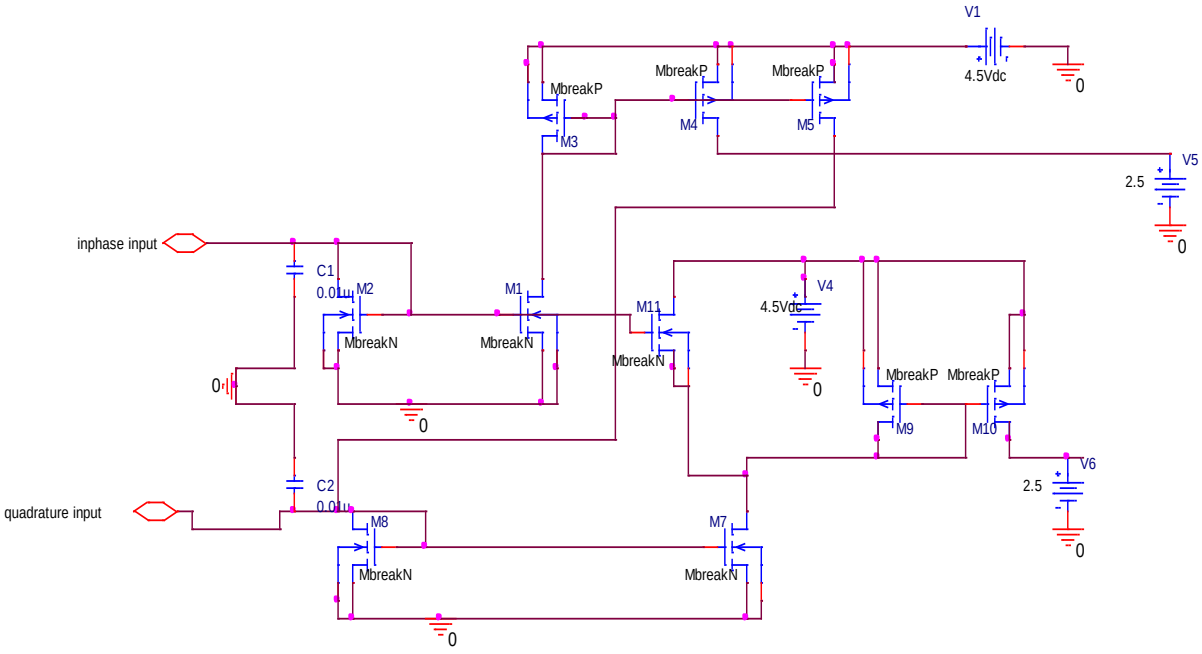


Figure 2.2 Actual circuit of lossy integrator

The project uses chosen length of all transistors to be 1.5u m and width is varied according to N-MOS and P-MOS taking care that width of P-MOS is 2.5 times width of N-MOS so that same current is flown through it with equal amount of voltage as in N-MOS .

$$\text{Iout} = \frac{\omega o}{s - j\omega if + \omega o}\text{Iin} \quad [2]$$

$$\omega o = \frac{gm}{c}$$

$$\omega if = \frac{k\omega o}{c}$$

The K value has been chosen to be 2 , i.e., the width of the feed back transistor is twice the other transistor . One can choose any value of K depending on which frequency the pole needs to be shifted . ωo is set by biasing of transistor and the value of capacitance used in the project. In the project pole is chosen at 10KHz to clip off the voice signal if exceeding that frequency.

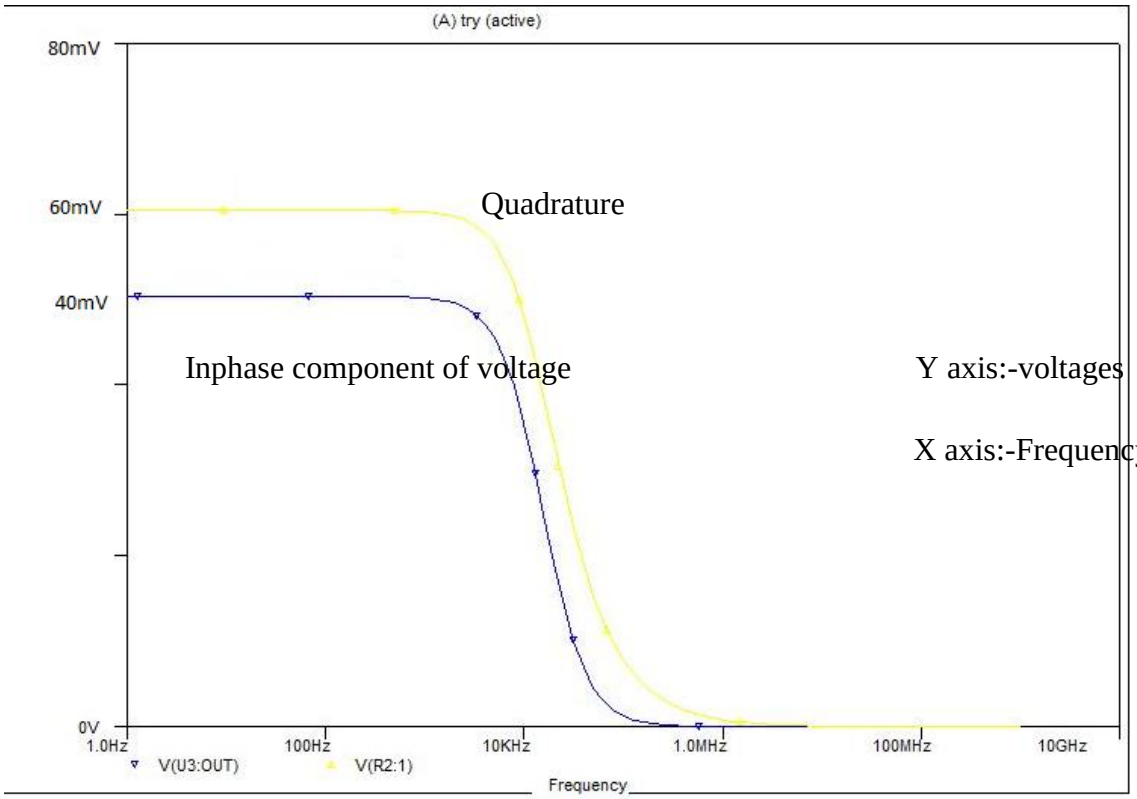


Figure 2.3 Frequency response of lossy integrator

The above figure shows the in phase and quadrature phase voltages after passing through lossy integrator. The in phase and quadrature phase components are unequal in magnitude as seen in the figure; this is due to the criss cross section positive and negative feedback of current in quadrature and in phase component respectively. The cutoff frequency of both can be set the same .LPF plays an important role in communication system as in band limits the signal which in-tern reduces the bandwidth required for its transmission also it reduces the white noise which is proportional to the frequency of the signal (this is the reason to avoid High pass filter in communications) .

Note that as it is lossy integrator one cannot have pole at origin, there is always a finite frequency other than 0 to give -20dB/dec slope to the voltage.

2.2 Complex Grounded Capacitor

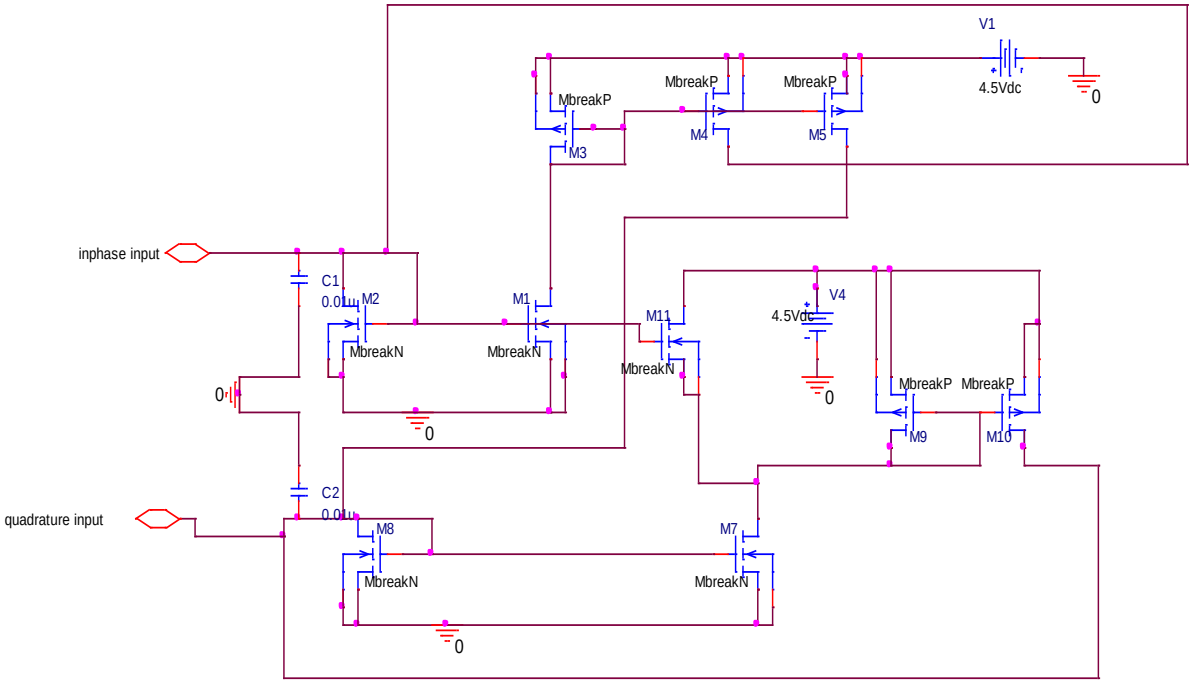


Figure 2.4 Grounded complex capacitor

The feedback taken in the figure ensures that the lossy integrator is converted into a lossless integrator, i.e,, ideal integrator, the above is used as a grounded complex capacitor and its frequency is shifted to give the in phase and quadrature part of the system.

2.2.1 Circuit diagram of LPF using grounded complex capacitor

A simple 2^{nd} order LPF is realized using opamp as the interfacing stage. Taking an RC circuit in mind a simple one pole system can be realized , using such system in cascade in non interfacing condition (no loading) a 2^{nd} order LPF having pole at the same cutoff frequency was simulated.

Using grounded capacitor simulating 2nd order low pass filter

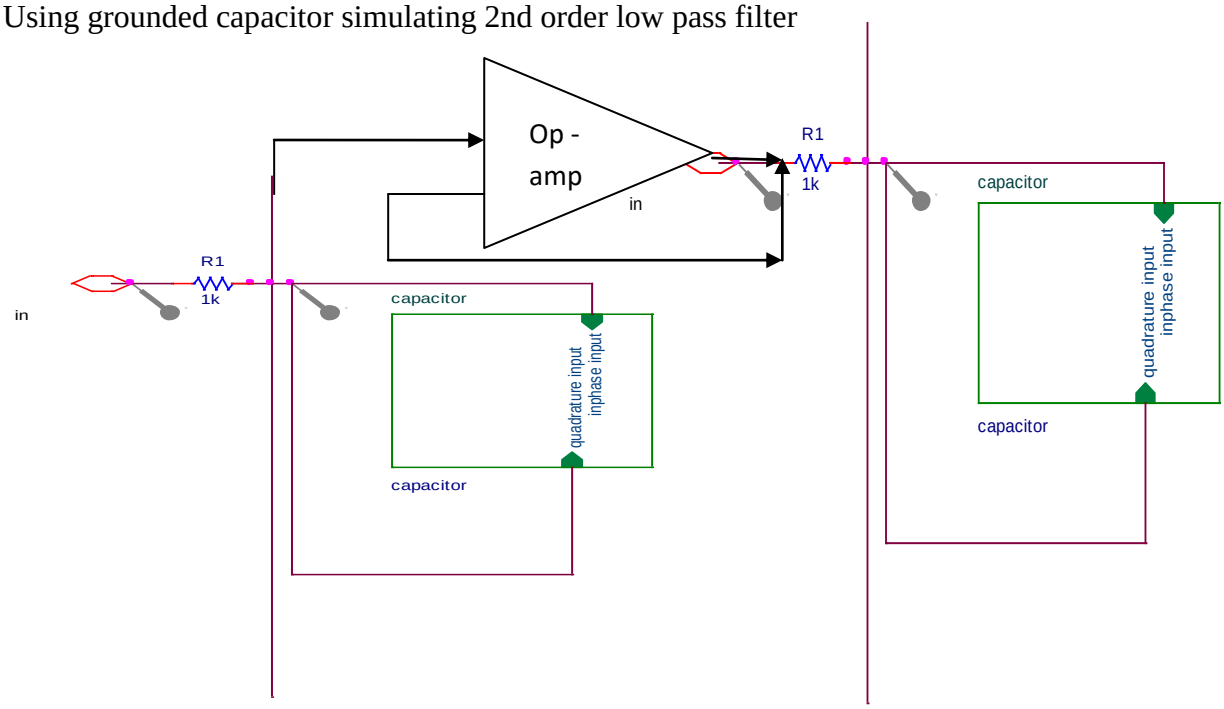


Figure 2.5 LPF

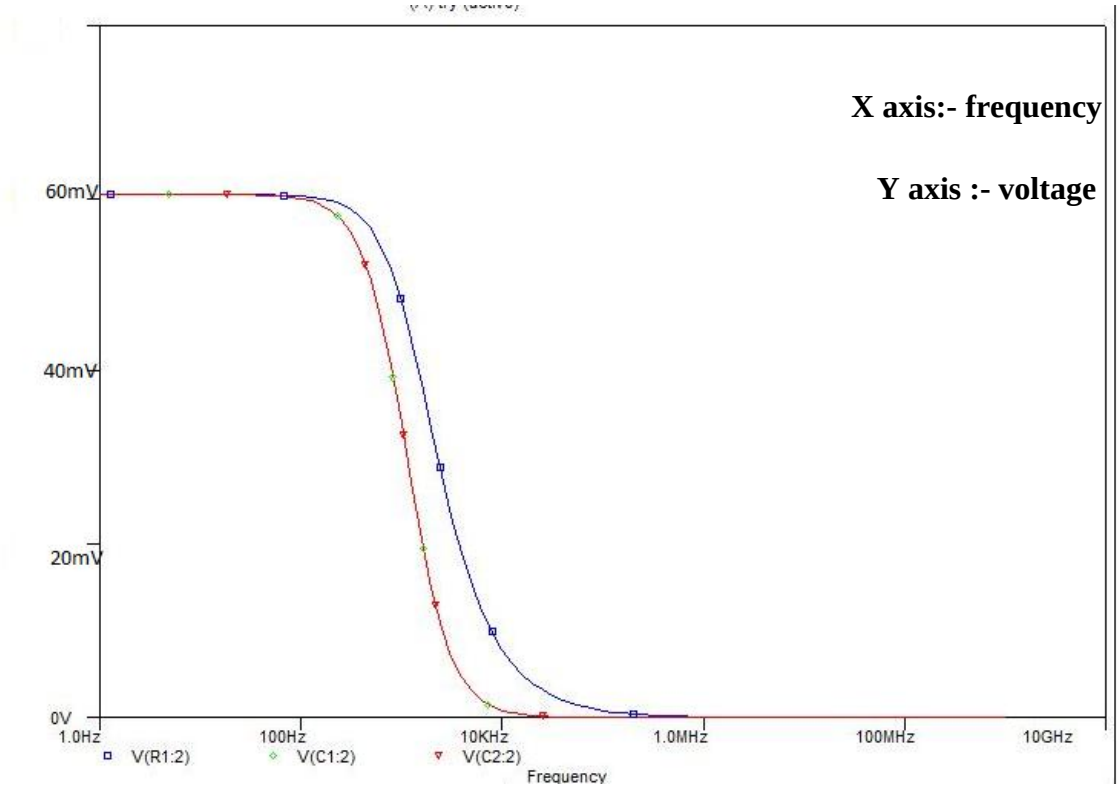


Figure 2.6 Frequency response of LPF

2.3 Example of a complex Inductor

a grounded inductor which can be simulated by gyrator

A Gyrator is a positive impedance inverter which is explained in chapter 3 using which a complex inductor with variable zero of the transfer function can be realized, even though there is a direct implementation of a complex inductor using current mirrors but in the project inductor is simulated using a gyrator, if pole of a complex load capacitor is varied the inductor simulated it the input side will also have its zero varied. The currents and voltages of load and the input side are verified as shown in Figure 2.8

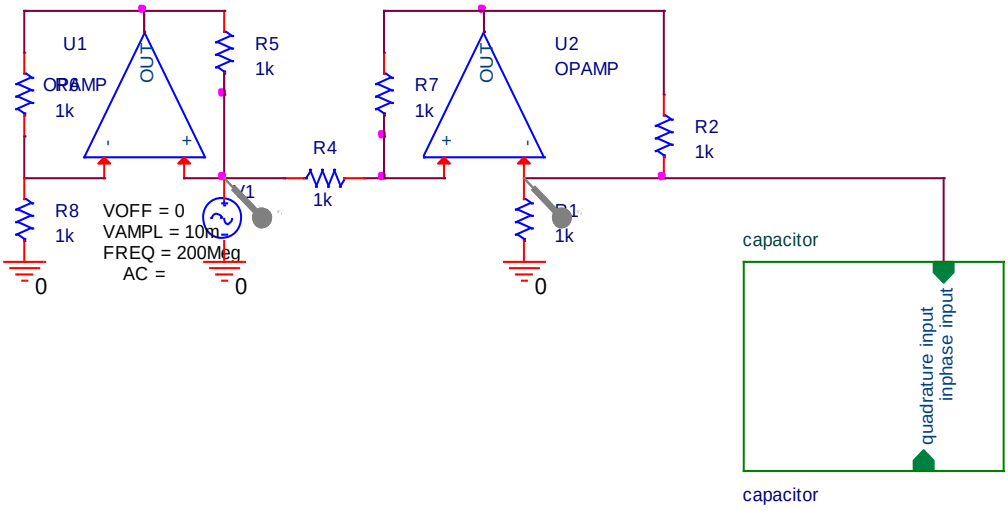
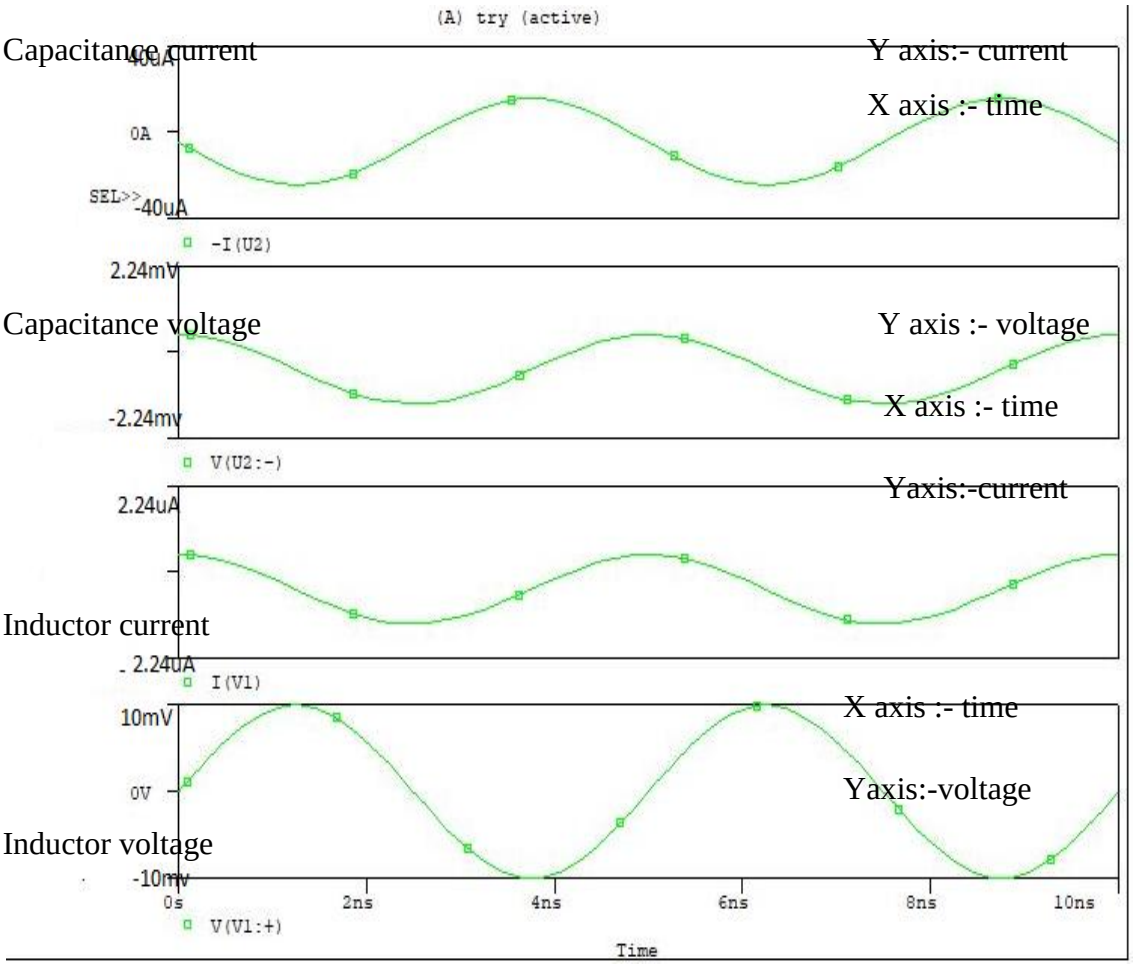


Figure 2.7 Inductor using gyrator

The above figure shows an inductor being simulated using a capacitor. If we place a capacitor at the load side of the gyrator, it is easily observed by applying KVL and KCL equations, we are able to realize an impedance inversion at the input port. That means if a resistor is placed at load side, we get admittance, also if an inductor is at load it will be inverted to a capacitor at input terminal. This element Gyrator was then realized by many other analog blocks like OTA other than opamp but to keep the design simple the project has used an opamp based gyrator only.

Output of inductor:-



Capacitance current

Y axis:- current

X axis :- time

Capacitance voltage

Y axis :- voltage

X axis :- time

Yaxis:-current

Inductor current

X axis :- time

Yaxis:-voltage

Inductor voltage

Figure 2.8 Inductor Output

It is very clear that the voltage and currents of the inductor and capacitor are out of phase , not exactly 90 deg because of the complex nature of the grounded capacitor but the above graphs confirm that the inductor is successfully simulated by using grounded complex capacitor therefore confirming the Gyrator nature of positive impedance inverter. For ease one does not even need to know the magnitude of the currents and voltages in the above graph just the phases are enough to say that inductor and capacitor is simulated. Here 90 degree phase shift is not seen because complex capacitor is taken at load not the ideal one.

CHAPTER 3

GYRATOR

3.1Introduction

Gyrator is a passive device which is also known as positive impedance inverter. Due to the non integrative nature of inductor in an IC the gyrator is used to realize an inductor in an IC where required.

A capacitor can easily be implemented using a varactar diode or a MOS or where ever a PN junction is formed but to simulate an inductor we require to have a positive impedance inverting element which can invert the capacitor connected on one terminal and give an inductor realization on the other .

To do this Bernard D. H. Tellegen who was an electrical engineer and who also invented pentode , gave well known Tellegen's theorem also gave the invention of a gyrator

3.2 Port Equation and symbol

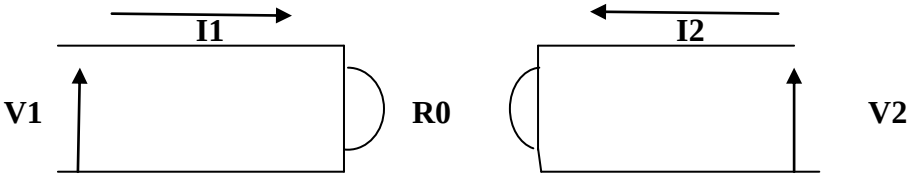


Figure 3.1 Gyrator [3]

Ro is constant

I1=Ro(V2)

I2=-Ro(V1)

So connecting a capacitor on 2nd terminal will give an inductor in 1st terminal

$$Zin = \frac{Ro^2}{Zout}$$

3.3 Implementation of gyrator using OPAMP

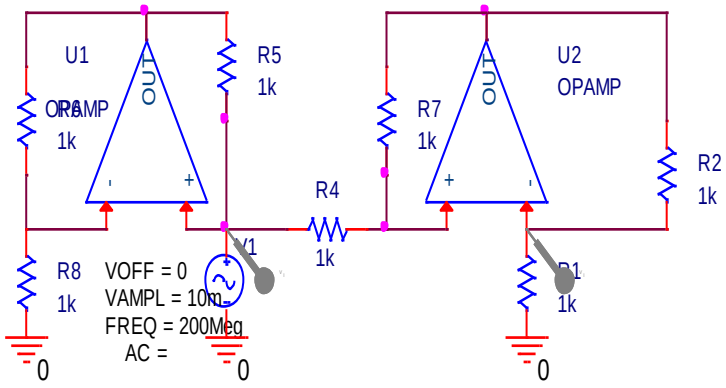


Figure 3.2 Opamp based Gyrator

Here 1 gyrator is used as shown in the above figure. The project uses 2 gyrators one for the quadrature and other for the in phase component of the signal. At the load side one complex capacitor kept whose pole is converted to a zero in the input side. Even though gyrator seems to be a very useful impedance inverter but its demerit is the number of transistors used to manufacture a positive impedance inverter. An opamp takes 22 to 25 BJTs and here 4 opamps are used which makes fabrication costly.

CHAPTER 4

UNDERSTANDING LOGIC GATES AND OPAMP

4.1 Introduction

Gates in digital can be realized using

1. N-MOS technology
2. P-MOS technology
3. C-MOS
4. TG gate technology

Each has their advantages and disadvantages respectively like N-Mos has strong 0 whereas P-Mos has strong 1 so C-Mos combines them both to have a strong 1 and a strong 0 with least leakage current and highest fan out.

One of the basic logic gate to realize is AND gate:-

4.1.1 Characteristic table of and gate

Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Tabel 4.1 AND Gate Truth Table

The above table is made taking ‘1’ as higher voltage level and ‘0’ as lower voltage Level. There is another logic also followed in digital called negative logic which treats ‘0’ as higher voltage level and ‘1’ as lower voltage level.

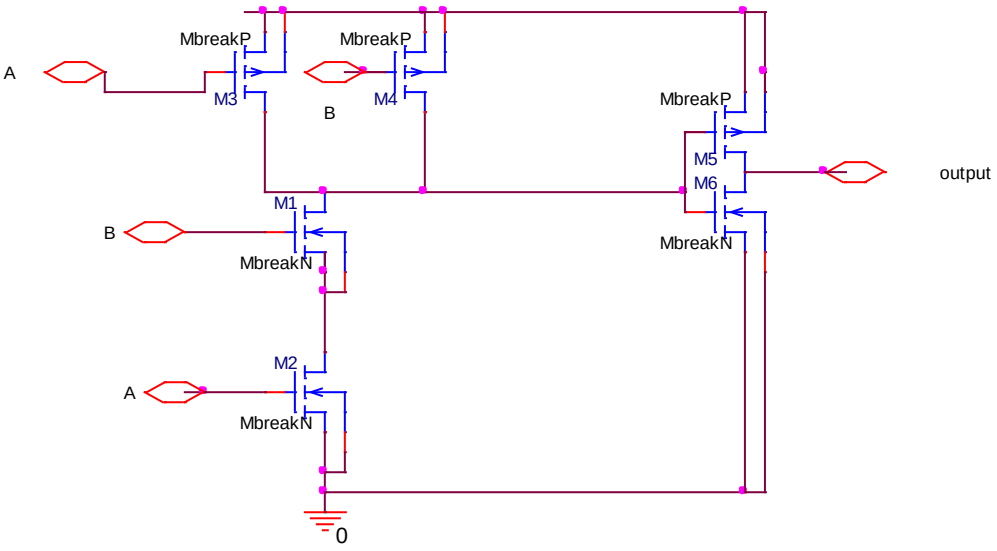


Figure 4.1 And gate logic [8]

The concept of the digital logics is to switch between on and off condition of the transistor for N-MOS the basic concept is if $V_{GS}>V_{th}$ therefore the transistor is on, that is, it can be treated as a short ideally but practically it acts like a resistor.

The same thing is applicable with P-MOS but with reverse sign of voltage

The above gave an idea of CMOS logic now considering NMOS logic

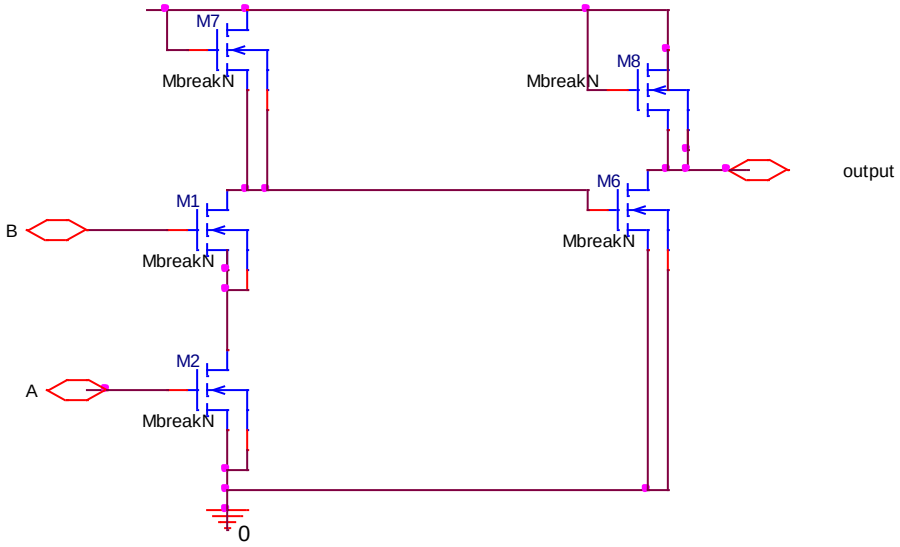


Figure 4.2 NMOS logic [9]

It has a problem of weak 1 and leakage current from V_{dd} to ground

Similarly using P-MOS too one can implement logics,

Instead of using MOS even BJT can be used to implement a logic family the very famous Emitter coupled logic can be implemented to have fastest operation, but BJT has less input resistance compared to MOS and is better suited for amplifier operations , till now BJT is used in industries because it offers higher power rating.

4.2 Opamp IC 741

4.2.1 Some important points on Op amp:-

1. It is a linear amplifier, therefore we can apply superposition on its output
2. It is designed to do mathematical calculations like sum , integration ,etc.
3. Its input stage is a differential amplifier and has got high input resistance and low output resistance.
4. Ideally it has infinite voltage gain but practically its value is very high, therefore giving rise to virtual short concept.
5. In +ve feedback its output is either +Vsat or –Vsat.
6. Opamps are also used in signal generator and oscillators.

Symbolic diagram:-

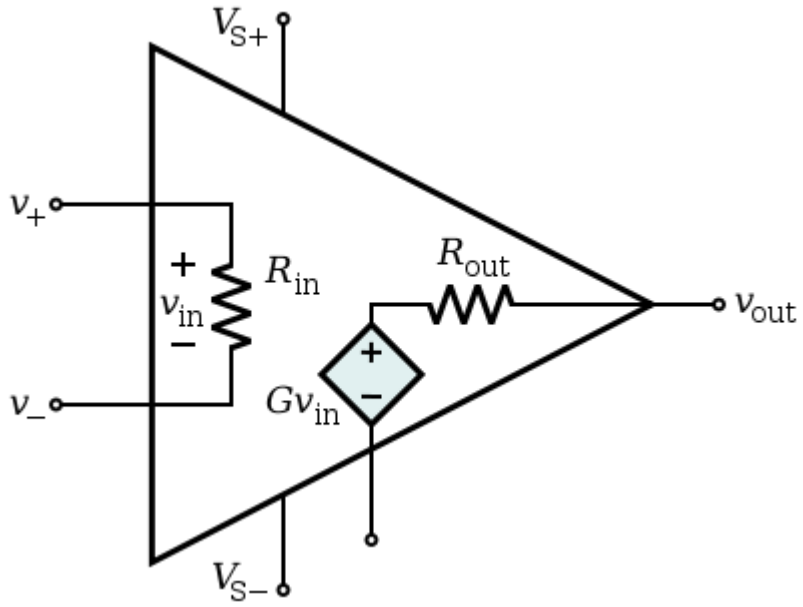


Figure 4.3 Opamp [10]

4.2.2 Some applications of opamp

1. Astable mutivibrator circuit:-

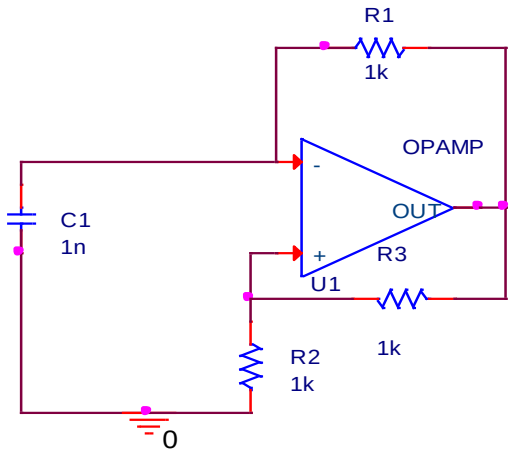


Figure 4.4 Astable mutivibrator circuit

It generates a square wave with time period:-

$$T = 2RCln\frac{1+\beta}{1-\beta}$$

$$\beta = \frac{R3}{(R3+R4)}$$

working of above circuit :-

1. Initially if output voltage is $+V_{sat}$
2. Capacitor charges till $\beta Vsat$ voltage level
3. As soon as the capacitor voltage reaches > βV_{sat} the output of Opamp triggers to –Vat
4. The capacitor starts to discharge to $-\beta V_{sat}$, again the output of opamp changes when this voltage is reached by the capacitor
5. The above process continues…..

2. Filters and integrators

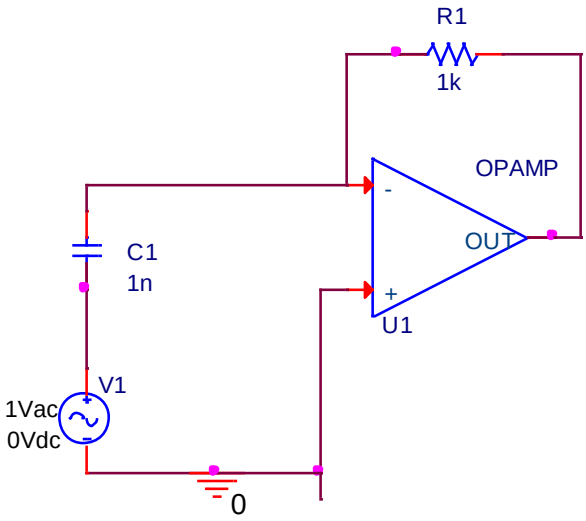


Figure 4.5 High Pass Filter

Opamp working as a filter is a very widely used application of opamp , in the above circuit , a high pass filter is simulated using opamp .Due to negative feedback the positive and negative terminals of opamp are shorted virtually and a simple KCL equation can give the relation between the output and the input voltages.

The transfer function comes to be = -RCS.

The above circuit is also called a differentiator, as it differentiates the input voltage with amplitude scaling. There are many applications of high pass filter in control system, but these are avoided in communications because they add more white noise to the signal therefore for communication system we use more low pass filters so that the noise added to the signal is as minimum as possible.

Figure 4.6 shows a low pass filter using opamp, also known as integrator circuit. Here also the virtual short concept of the opamp is valid due to negative feedback of Opamp and one can easily get the transfer function.

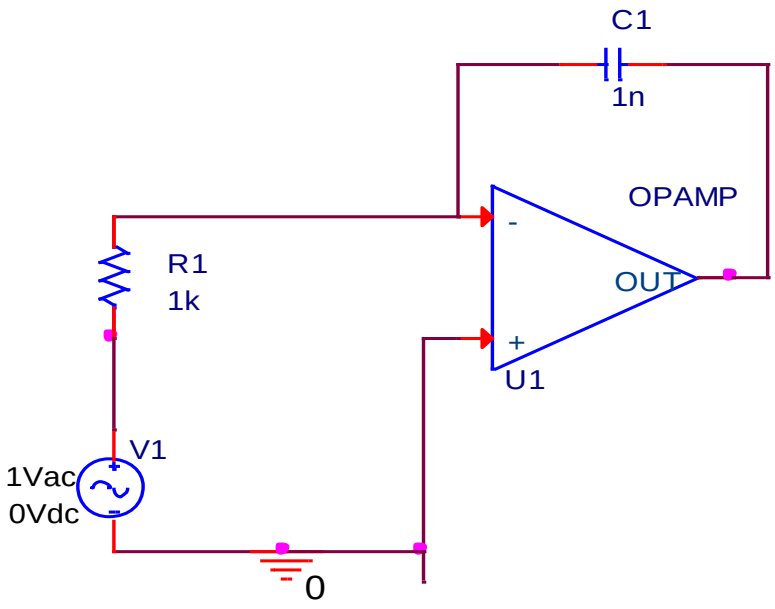


Figure 4.6 LPF using Opamp

Opamps are also used in controllers and compensators in control system in which frequency and transient response of the system is improved using these blocks

Realizing an opamp: - there are many ways to improve opamp performance like adding a compensation capacitor, a feedback amplifier, etc. won't go in these details because the project uses opamp as a comparator and a non interacting stage in implementation of 2^{nd} order filter as well as in digital to analog.

4.3 An example of Opamp design

Specifications:-

Supply= 1.65V (+,-)

Ibias=200uA

Kn=200 uA/V^2

Kp=80 uA/V^2

Vtn=|vtp|=0.5 (threshold voltage of N, PMOS)

0.2<Vov<0.4

Voltage Gain 12000

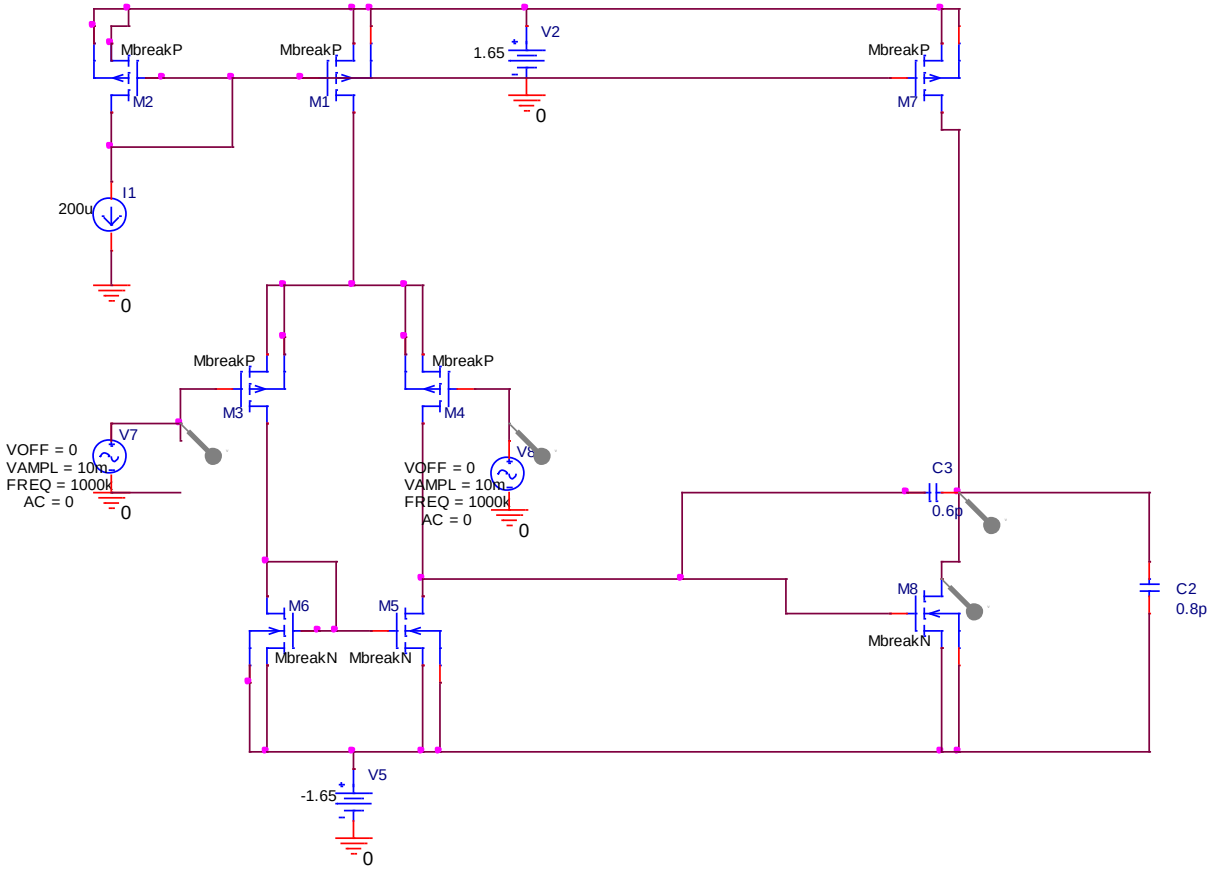


Figure 4.7 opamp design

Here in the above circuit an opamp with a given gain specification is designed and the difference in the stability is observed.

The primary motive of biasing the above circuit is that the transistors should remain in saturation region so that amplification action can happen. The biasing current is adjusted and trans conductance of 1st stage is calculated, the gain of the amplifier is simply the trans conductance multiplied with the impedance seen at the output node. Because there are 2 stages both the gains are multiplied and equated to 12k, therefore the width and length of each transistor can be calculated.

Dc bias:-

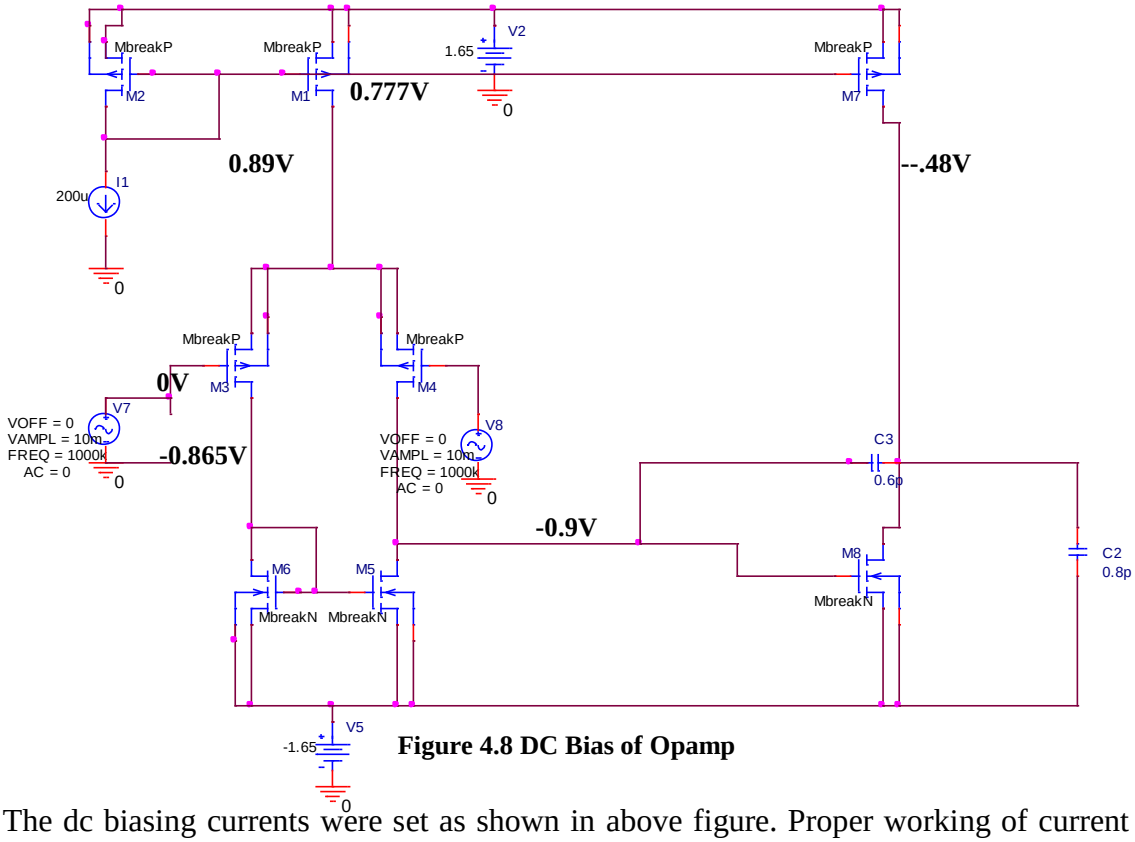


Figure 4.8 DC Bias of Opamp

The dc biasing currents were set as shown in above figure. Proper working of current mirrors was verified and assured that all the MOS s were in saturation region.

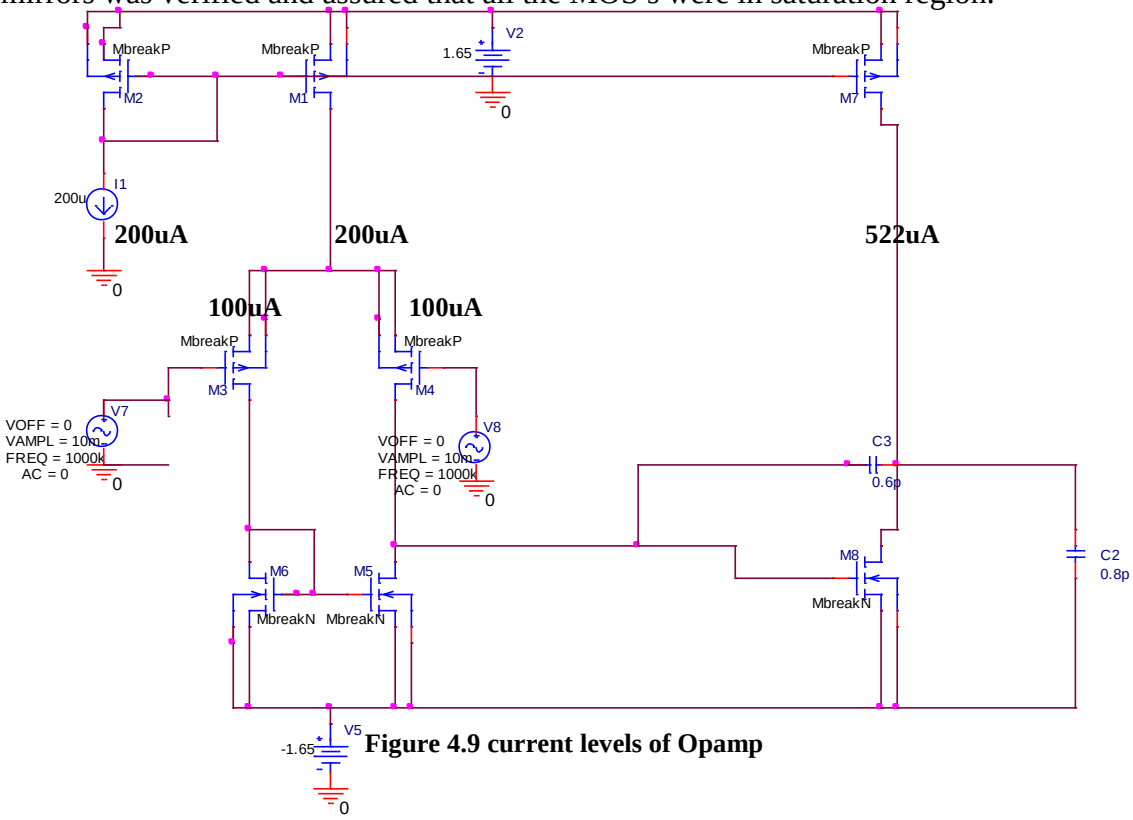


Figure 4.9 current levels of Opamp

The above figure shows the voltage levels at different nodes of the 2 stage opamp. The results were verified with theoretical calculations and then the Opamp was ready to process an AC signal with proper DC biasing .Note that the bias voltage level of the MOS is important as it tells about the voltage swing of the input and output waveform, because if one exceeds the overdrive voltage of the MOS the AC signal would clip.

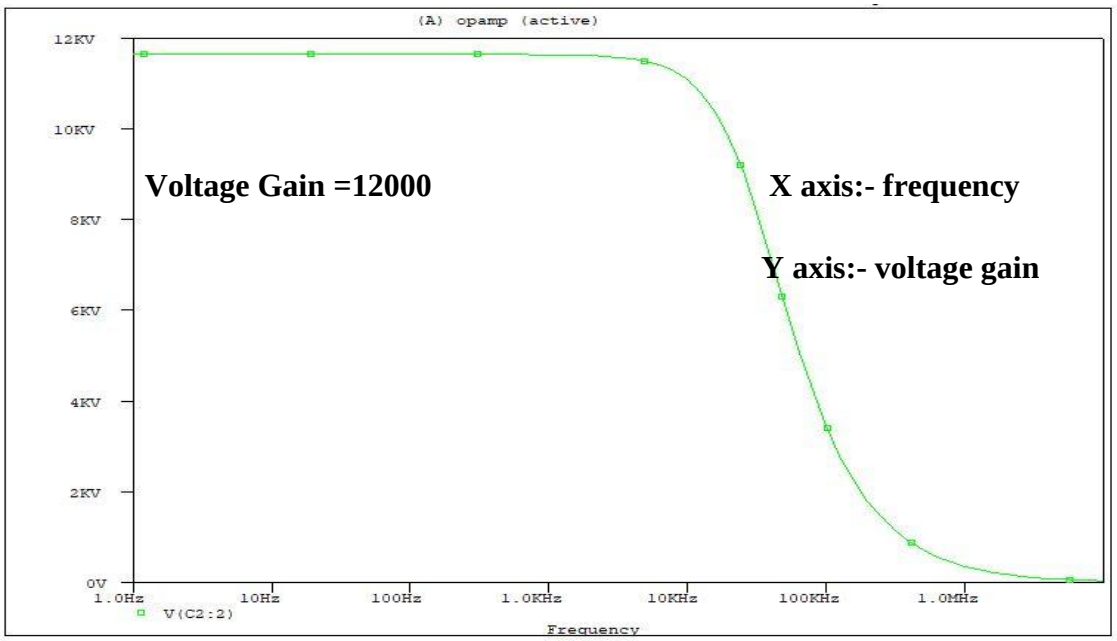


Figure 4.10 Differential gain

As shown in the graph above, the voltage gain of the Opamp was set to 12000. This was differential gain, the common mode voltage gain was also calculated to get the CMRR.

$$\text{CMRR} = \frac{\text{differential voltage gain}}{common\ mode\ voltage\ gain} = 24000$$

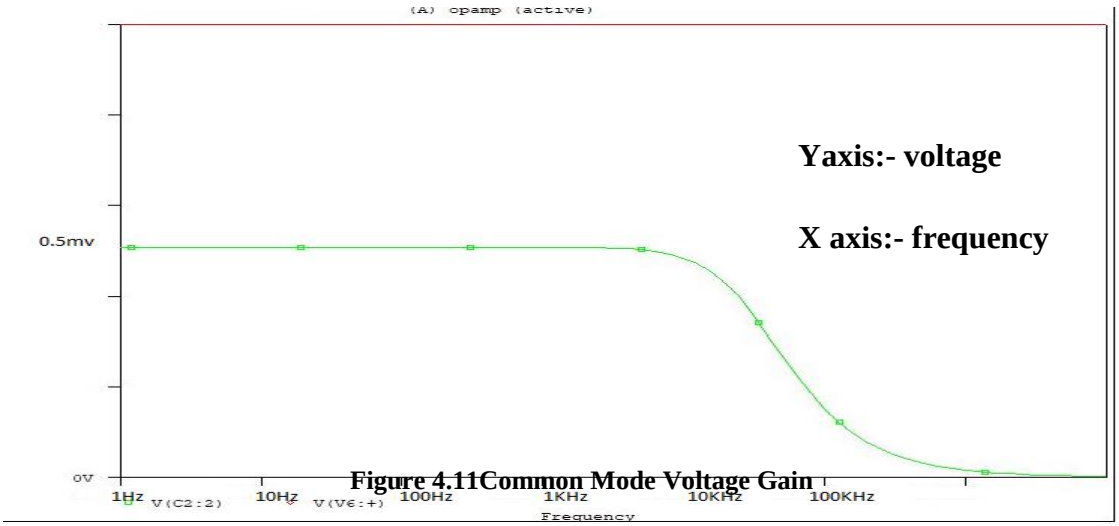


Figure 4.11Common Mode Voltage Gain

After setting the gain, the frequency response of the opamp with and without compensation capacitor was verified

Phase margin = 180+ the phase of the system at gain crossover frequency. Having a positive phase margin indicates that more phase lag can be added to the system to make it reach on the verge of instability. There is also one more measure of stability, i.e,, the gain margin which is defined as the inverse of the gain of the system at phase crossover frequency.

In the above graph it is very clear that without compensating capacitor the system had negative phase margin, whereas in the below figure the phase margin changed to 33 deg

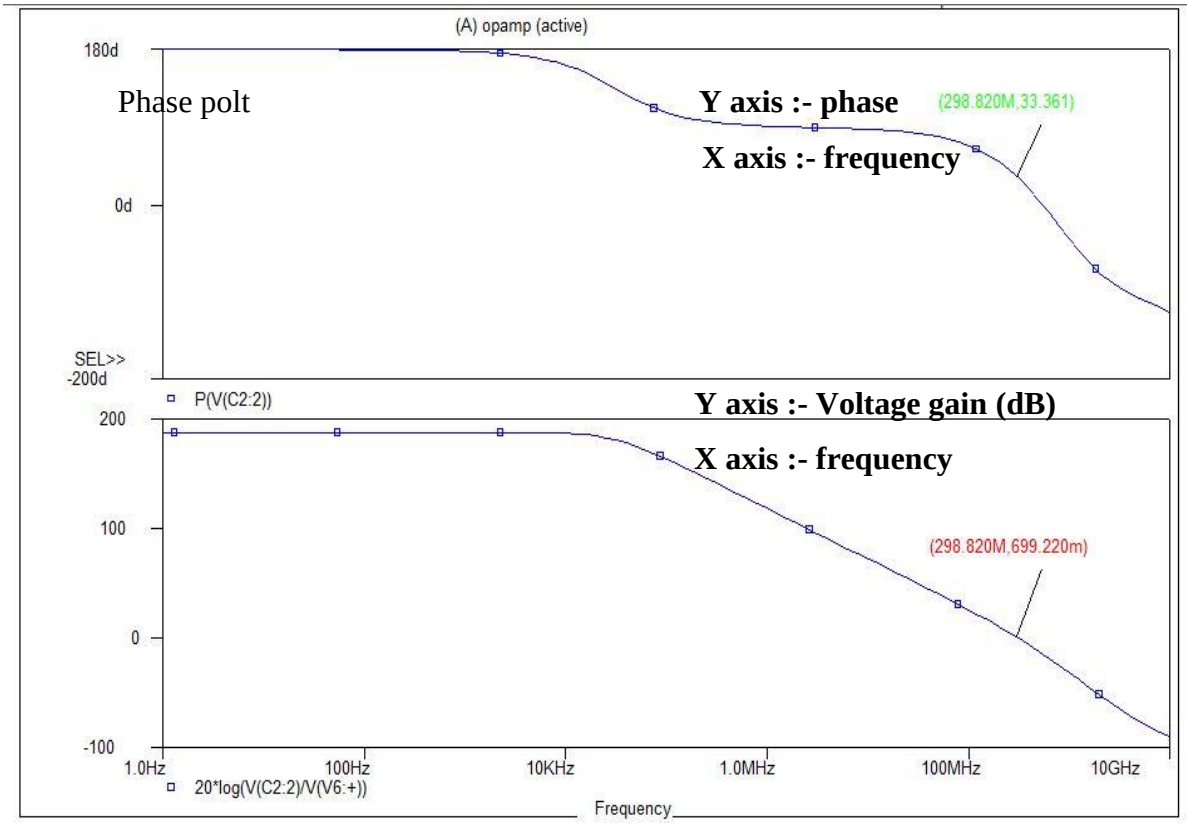


Figure 4.12 Frequency response of Opamp designed

Phase margin= 33deg

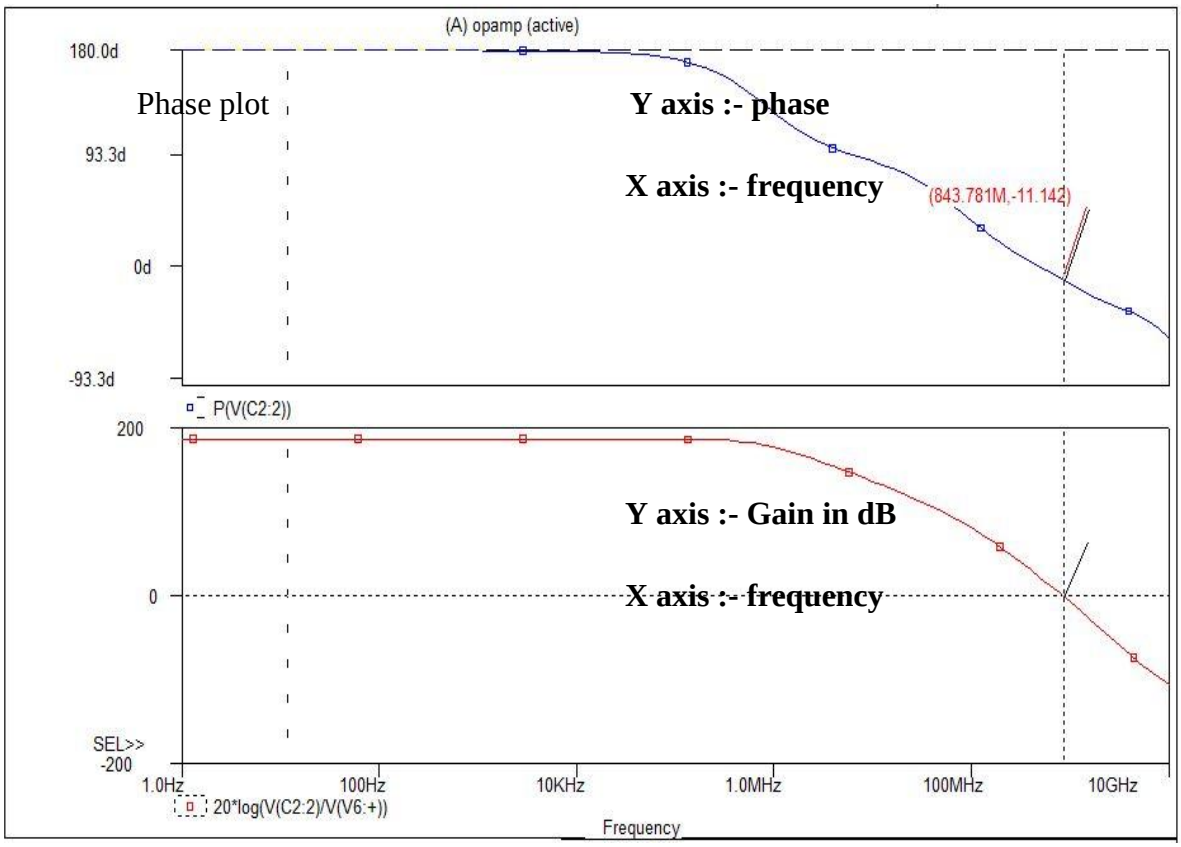


Figure 4.13Frequency response of opamp without compensating capacitor

Gain margin =-11dB without compensation capacitor

Having negative gain margin in dB indicates that system is unstable, that is, there is no margin of the gain we can have to make the system at the verge of instability. To avoid such situations we use a low pass filter or an attenuator which decreases the overall gain of the system and brings it to stable condition

Chapter -5

Counter Design Using D FLIP FLOP

Counter design starts with sequential circuit and flip flops as a building block, the same has been explained below:

5.1 Sequential circuit

The combinational circuits do not have the ability to store a bit, only sequential circuits have the ability to store,

Basic element to prove above statement:-

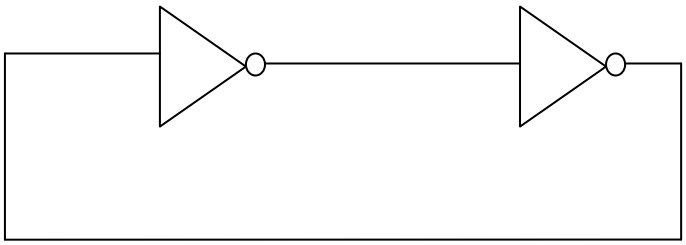


Figure 5.1 Basic memory element

Whatever the input is given to the above circuit ideally, it will never decay till the power supply to the inverters in ON. So the bit stored in the above circuit is stored infinitely.

This gives rise to sequential circuits whose value depends on past as well as present input but unfortunately we can't give another input to the above circuit as we need to have a stronger input pulse to overcome the previous stored data. There are latches (level triggered) and flip flop (edge triggered) which serve the purpose of storing a bit in the sequential circuit as well as gating the input by a clock pulse. Having a clock pulse gating is very important because it avoids race around condition and trigger the sequential circuit only when required. In practical situation if there was no clock , any noise signal could trigger the circuit which can be very dangerous if that sequential circuit is a part of an aircraft or simply a computer memory

Thus we go for :-

1. SR latch

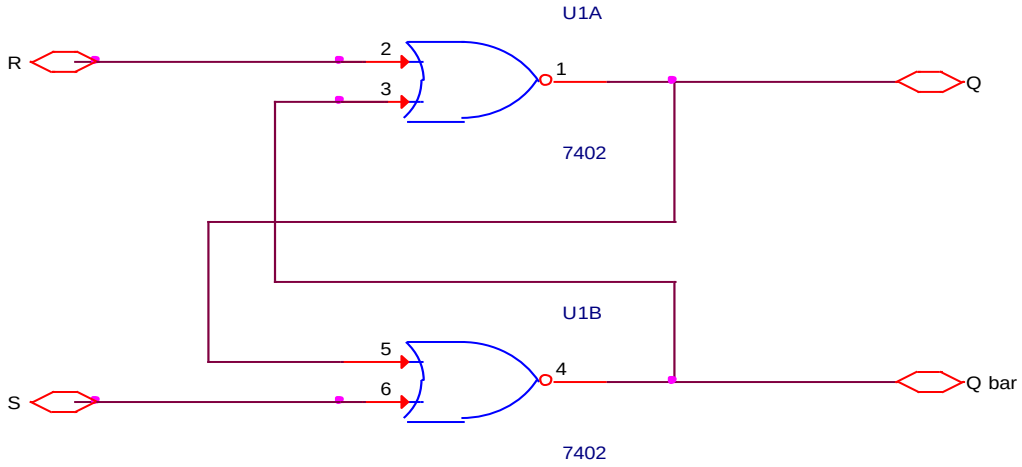


Figure 5.2 SR latch

S	R	Q
0	0	Q
0	1	0
1	0	1
1	1	X

Table 5.1 Truth Table of SR Latch

To avoid transient triggering we use clocked circuit:-

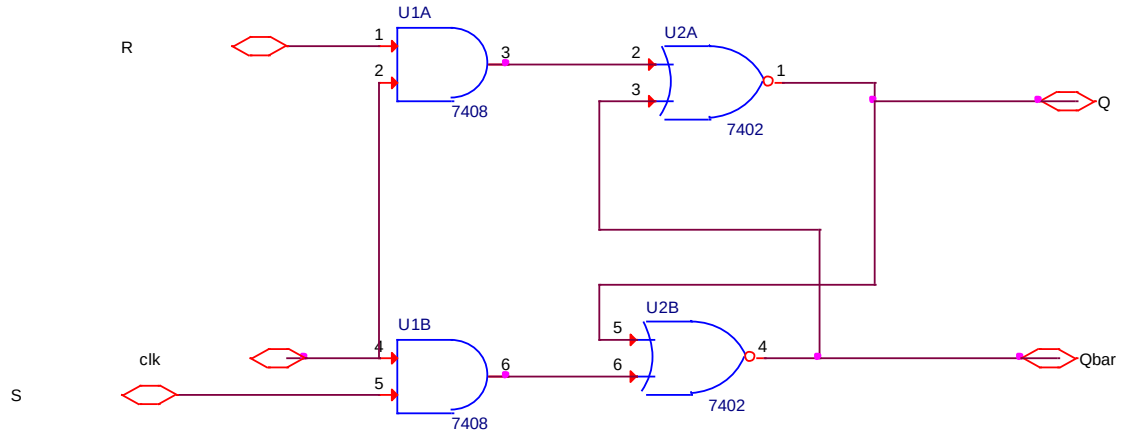


Figure 5.3 Clocked SR

2. D latch:-

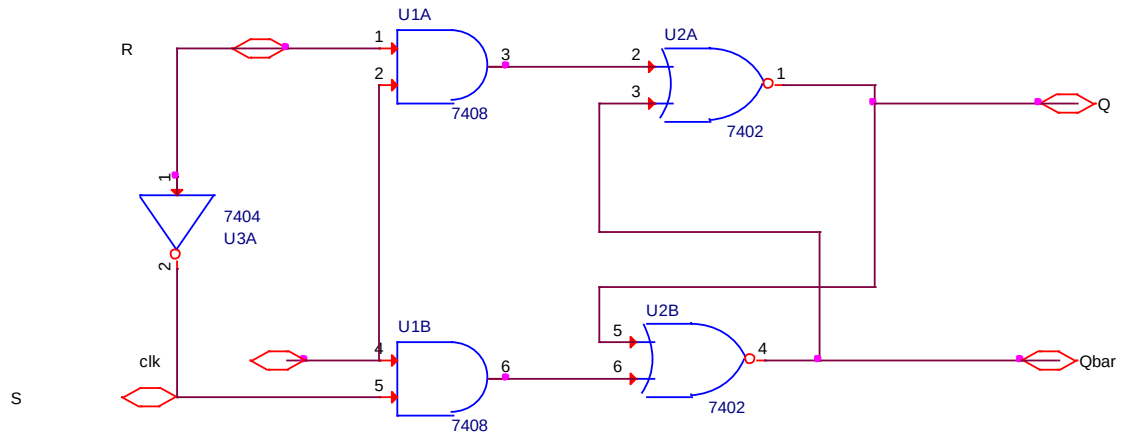


Figure 5.4 D latch

D	Q	Q+
0	0	0
0	1	0
1	0	1
1	1	1

Table 5.2 Truth Table of D latch

3. Jk latch:-

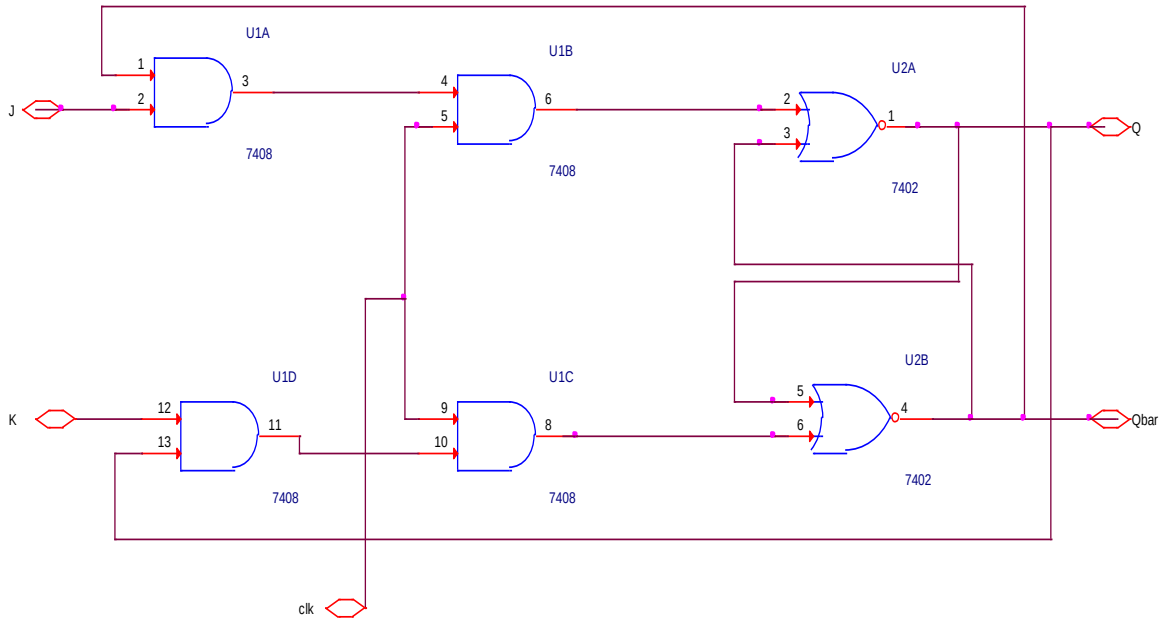


Figure 5.5 Jk latch

J	K	Q+
0	0	Q
0	1	0
1	0	1
1	1	Q’

Table 5.3 Truth Table of JK Latch

3. T latch:-

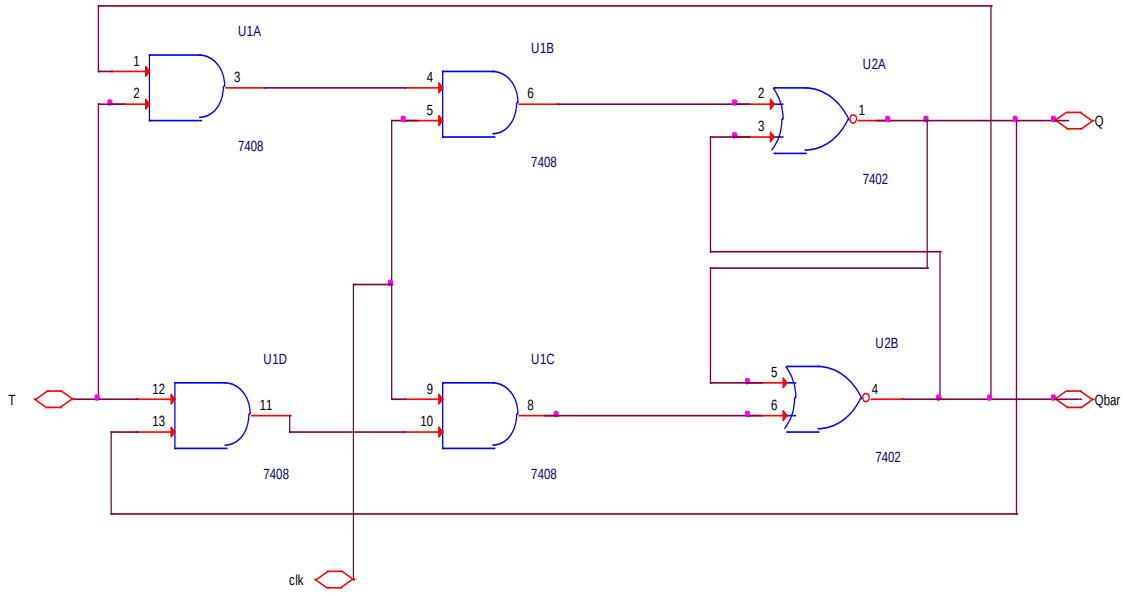


Figure 5.5 T latch

T	**Q+**
0	**Q**
1	**Q’**

Table 5.4 Truth Table of T Latch

Whichever sequential circuit has toggle mode has got a problem of getting into race around condition therefore this gave rise to

1. Master slave circuit
2. Limitations on clock on time

5.2 Counters

These are digital circuits which count up to as designed .

For a 4 bit counter we can make it change sate from 0000 to 1111 that is 16 states also called as mod 16 up counter.

TRUTH TABLE:-

Q3	Q2	Q1	Q0	(Q3+)	(Q2+)	(Q1+)	(Q0+)
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0						
…….							
1	1	1	1	0	0	0	0

We get the expressions of D:-

D3=Q3(Q1')+Q3Q0'+Q3'Q2Q1Q0

D2=Q2Q1'+Q2Q0'+Q2'Q1Q0

D1=Q1'Q0+Q1Q0'

D0=Q0'

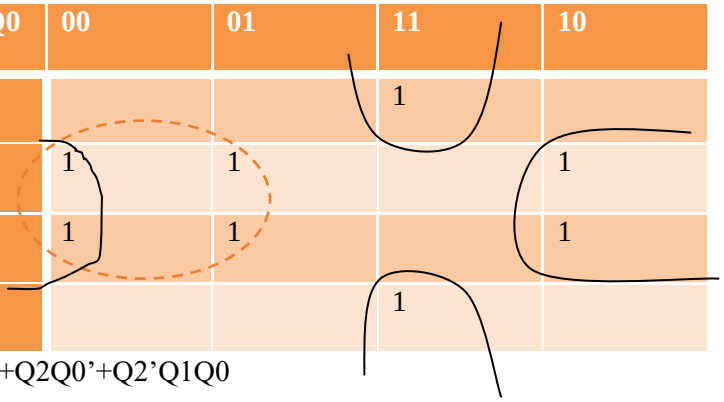
By using d flip flop

The project has used 4 bit up counter using D flip flops

Q3Q2|Q1Q0	00	01	11	10
00				
01			1	
10	1	1		1
11	1	1		1

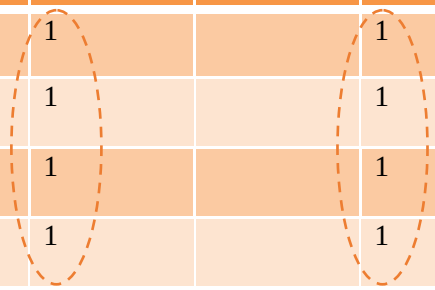
D3=Q3(Q1')+Q3Q0'+Q3'Q2Q1Q0

Q3Q2|Q1Q0	00	01	11	10
00			1	
01	1	1		1
10	1	1		1
11			1	



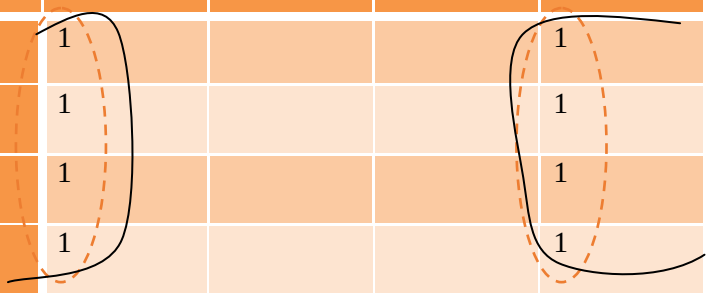
D2=Q2Q1'+Q2Q0'+Q2'Q1Q0

Q3Q2|Q1Q0	00	01	11	10
00		1		1
01		1		1
10		1		1
11		1		1



D1=Q1'Q0+Q1Q0'

Q3Q2|Q1Q0	00	01	11	10
00	1			1
01	1			1
10	1			1
11	1			1



D0 =Q0'

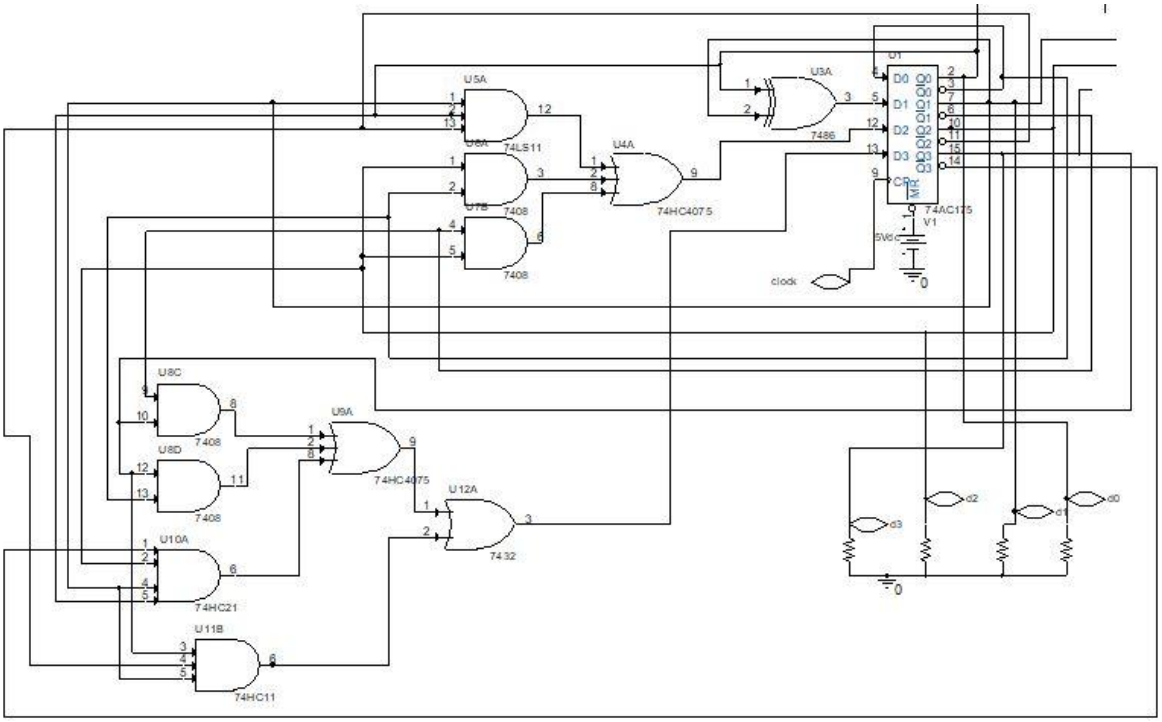


Figure 5.7 Upcounter

Even though counter can be made by other flip flops too but the project uses D ff as a 4 bit up counter.

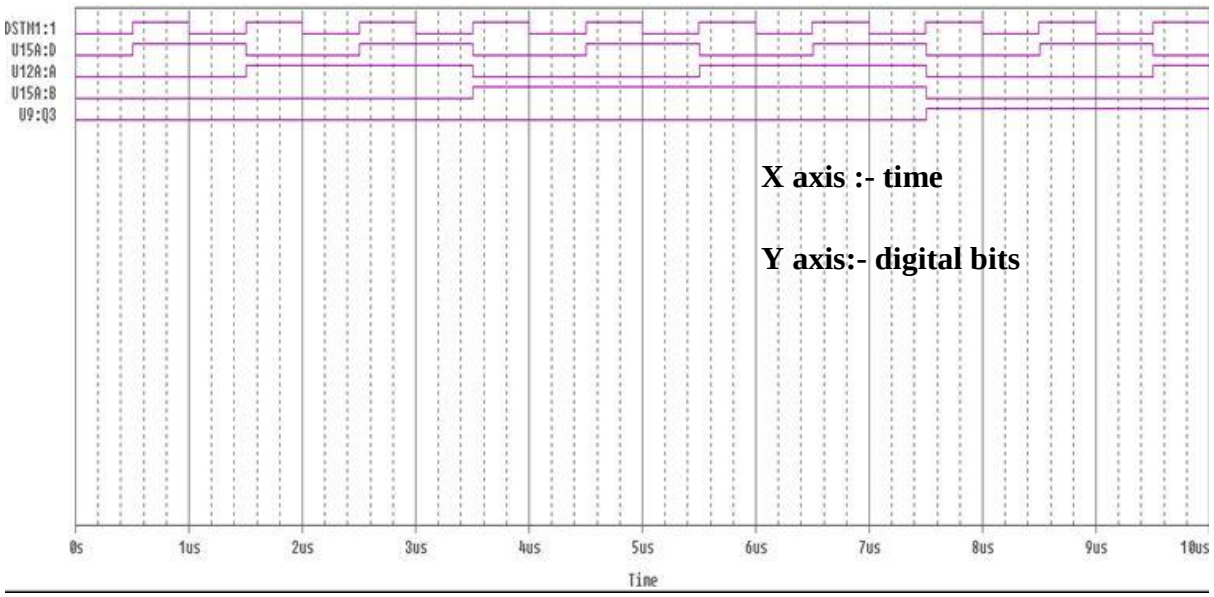


Figure 5.8 Results of up counter

The above graph shows the up counting process of the designed counter here:-

DSTM1:1 is the clock signal supplied with period 1usecond

U15A:D is the least significant bit (d0)

U12A:A is 1st significant bit (d1)

U15A:B is 2nd significant bit (d2)

U9:Q3 is the most significant bit (d3)

It can be easily seen that on 1st edge triggering the counter starts to count as follows:-

d3 d2 d1 d0

0 0 0 0

0 0 0 1

0 0 1 0

……and so on. The basic idea for A/D is controlling these counts with a comparator

5.3Analog to digital converter

Taking 5 v sample

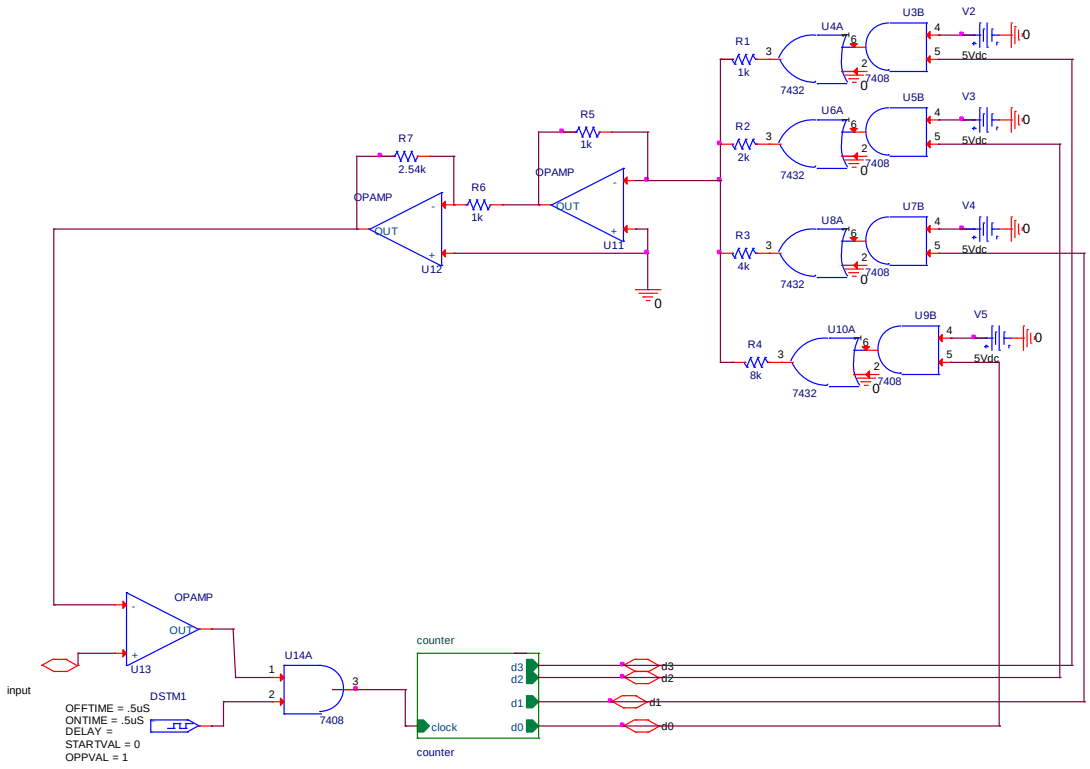


Figure 5.9 analog sample to digital conversion

In the above figure, 2 voltages are fed to the comparator and because initially the output from the digital to analog converter is coming 0V , the comparator gives positive output to the AND gate thereby the clock is passed to the counter .The counter starts counting and 1st count becomes “0001” these digital bits are fed to the digital to analog converter which gives 1V as its analog equivalent. This 1 V is then compared to input signal by the comparator and the process repeats till the output of the digital to analog converter is greater than or equal to the input applied signal. Once this is achieved the counter is not able to get further clock signal and the counting stops, the digital bits of the counter are the digital equivalent of the analog sample provided.

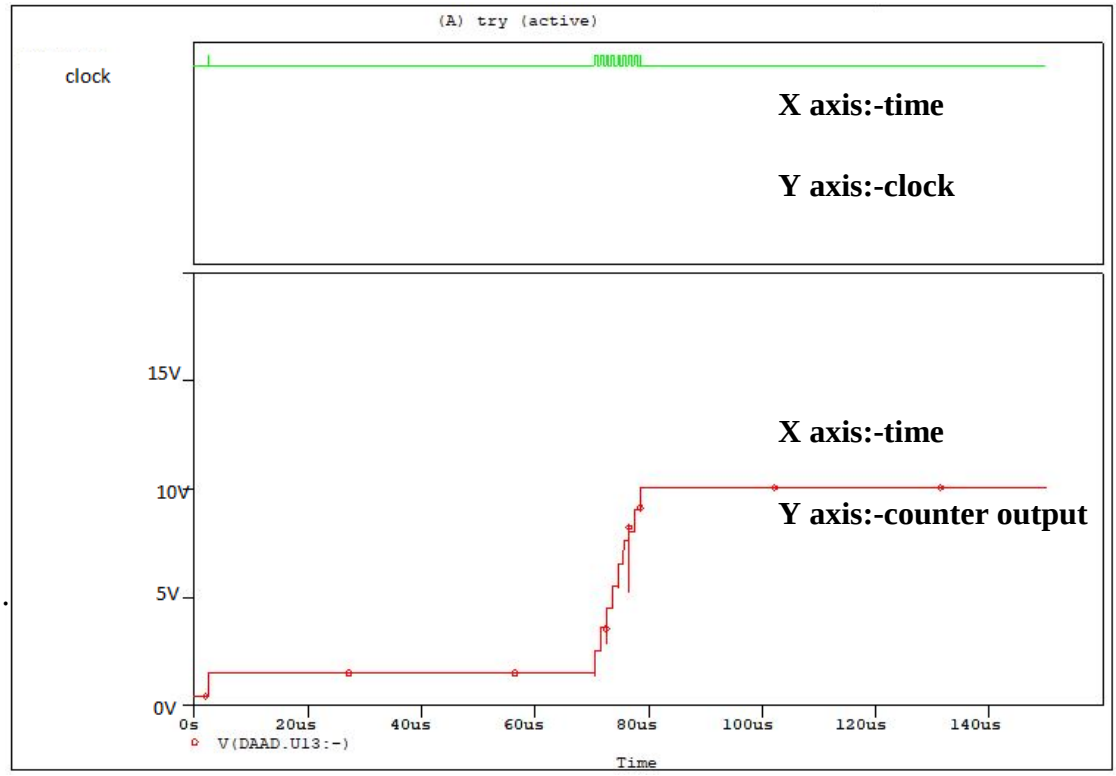


Figure 5.10 Result of Digital counter

It is very clear from Figure 5.9 that the counter takes time to reach the required voltage level. That is the drawback of counter type A/D converter; the best A/D converter is flash type A/D which does not have such delay. The project uses counter type A/D because it is easy to implement and the quantization can easily be varied in this process. The maximum delay provided by the counter is 2^n times the time period of the clock signal where n= number of bits (flip flops) used in counter. In practical situations if the

cost of manufacturing is a concern then also flash type A/D converter is not used because it uses 2^n -1 number of opamp comparators which requires 22 to 25 transistors each . More usable A/D in that case would be either successive approximation type or the dual slope type A/D converter which is very accurate due to which it is used in digital voltmeters too.

Chapter -6

Final Project And Its Modules

6.1 Comparator circuit

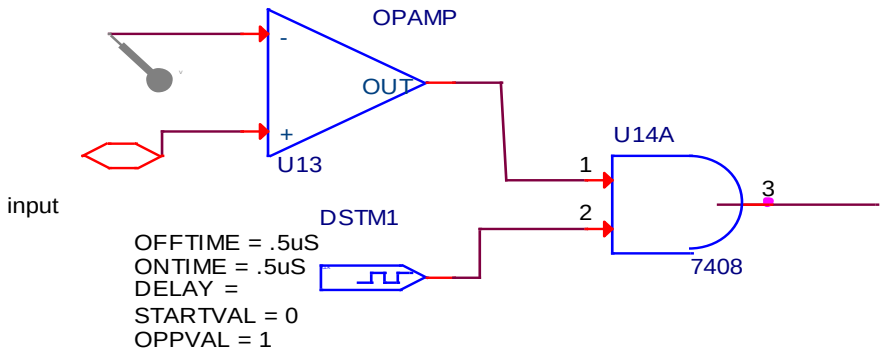


Figure 6.1 comparator

Here opamp is used as a comparator as shown in the figure, the sample voltage is kept on the +ve terminal of opamp and the voltage from the Digital to analog converter is kept on the –ve side of the terminal, the output of opamp is set to be +5 and 0 V and is given to a AND gate circuit. The other terminal of the AND gate is connected to the clock of the counter which is passed only till the opamp output is high. As soon as the opamp output is 0 the clock is gated by the AND gate and the counter stops .The respective digital bits produced by the counter represents the digital representation of the analog signal.

6.2 Message spectrum

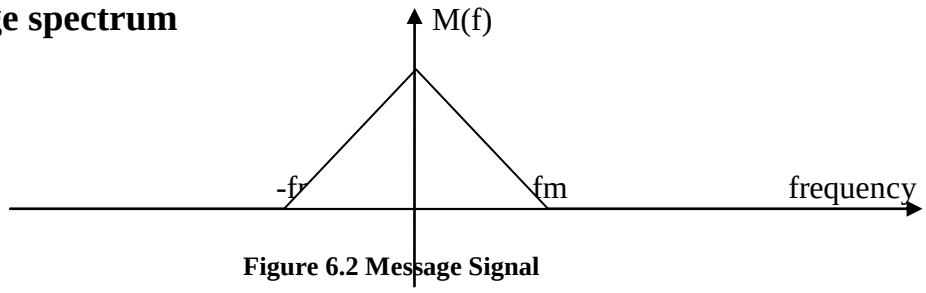


Figure 6.2 Message Signal

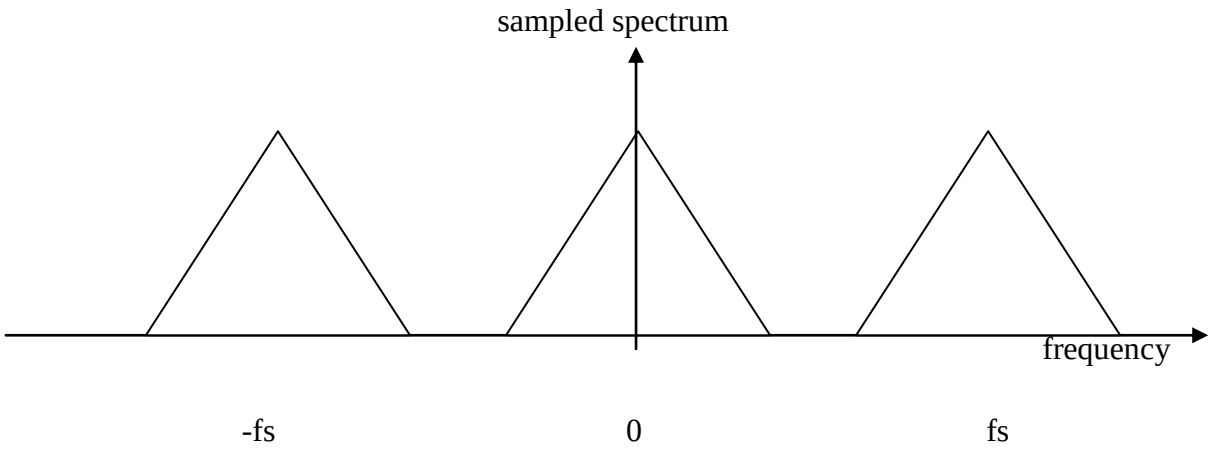


Figure 6.3 Sampling Output

The sampled spectrum results from convolution of impulses shifted by fs (sampling frequency) therefore, we get a periodic spectrum of the message signal

Nyquist rate :- the rate fs should be at least 2fm , i.e., the sampling frequency should be 2 times the highest message signal frequency, which in other words implies that we have to take 2 samples of the message signal in 1 time period so that we can recover the message signal faithfully from the samples chosen. If the condition is not satisfied the spectrum would superimpose on each other and the message would be lost forever, that is the reason that spectrum allocation is such an important task when done by the government for commercial purpose.

Fs=2fm

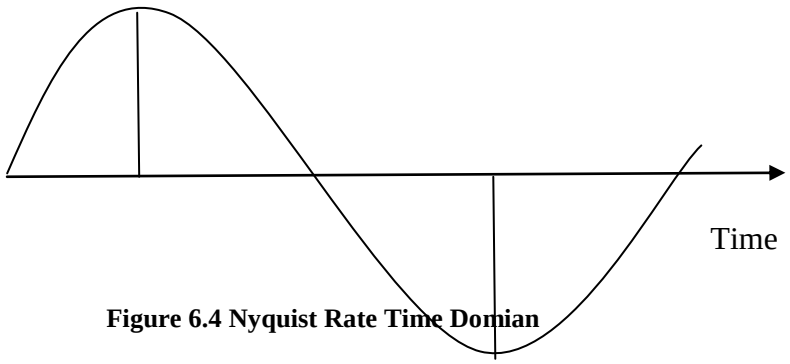


Figure 6.4 Nyquist Rate Time Domian

6.2.1 Sample and hold circuit

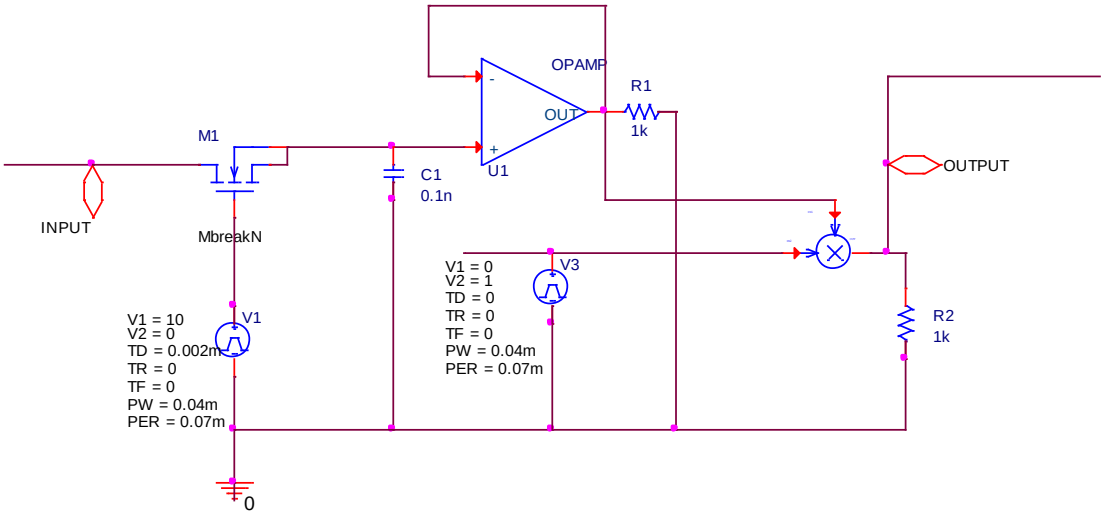


Figure 6.5 Sample and hold circuit

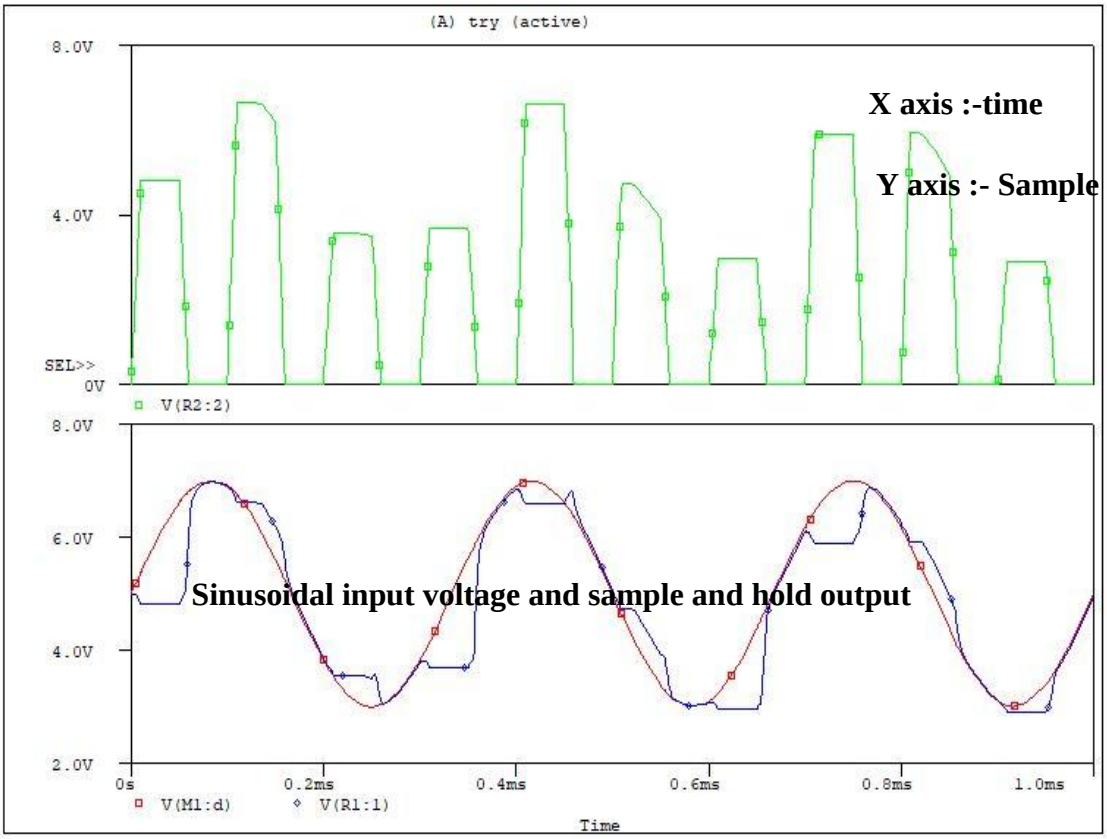


Figure 6.6 Result of sample and hold

Sample and hold output is shown above in the project; the held samples are further multiplied by unit amplitude pulses just to remove the fluctuations by the MOS and to get a constant output of the sample.

6.3 Grounded Complex Low pass filter out put

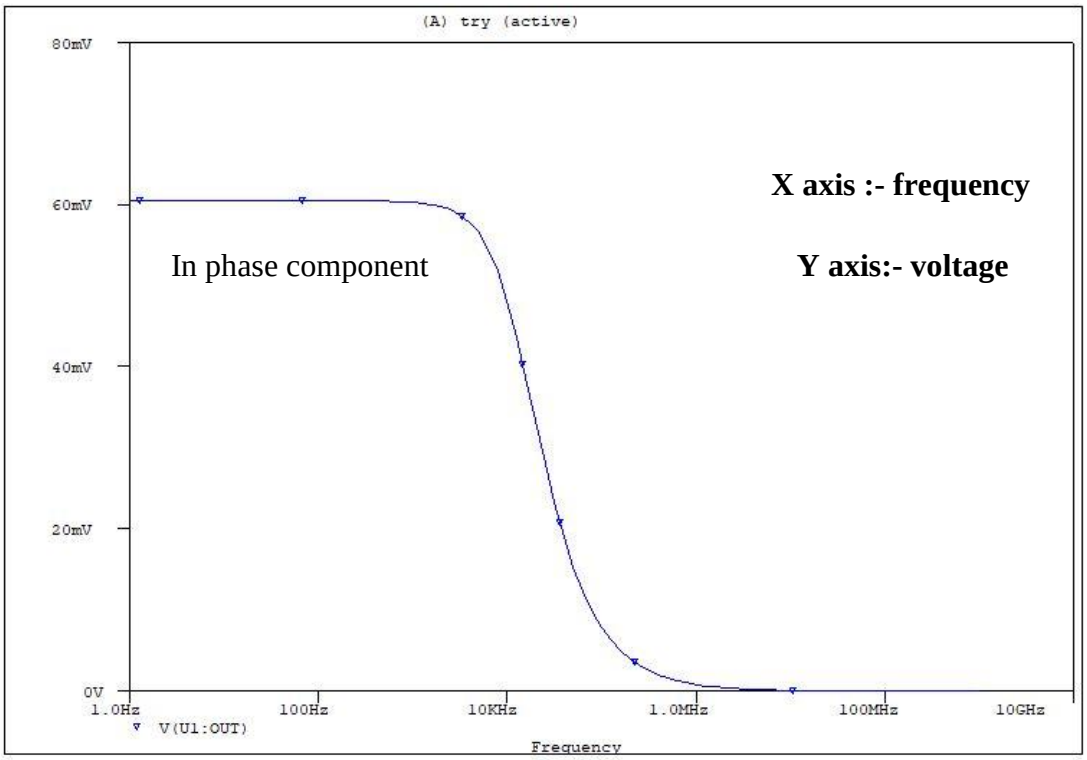


Figure 6.7 Complex Low pass filter frequency Response

As it can be seen from the figure that the complex filter will not allow frequency more than 10 kHz from the message signal, (circuit diagram is same as explained in chapter 1).

6.4 Signal processing block

The project has used a signal processing block as shown in the figure; the small signal generated by speech in mV is converted into 20 Vpp

The below block has:

1. Complex capacitor to band limit the signal
2. Opamp buffer
3. Dc bias elimination circuit
4. Amplifier and inverter

Each block uses opamp because it does not have the band width problem till the speech signal frequency range and provides good gain.

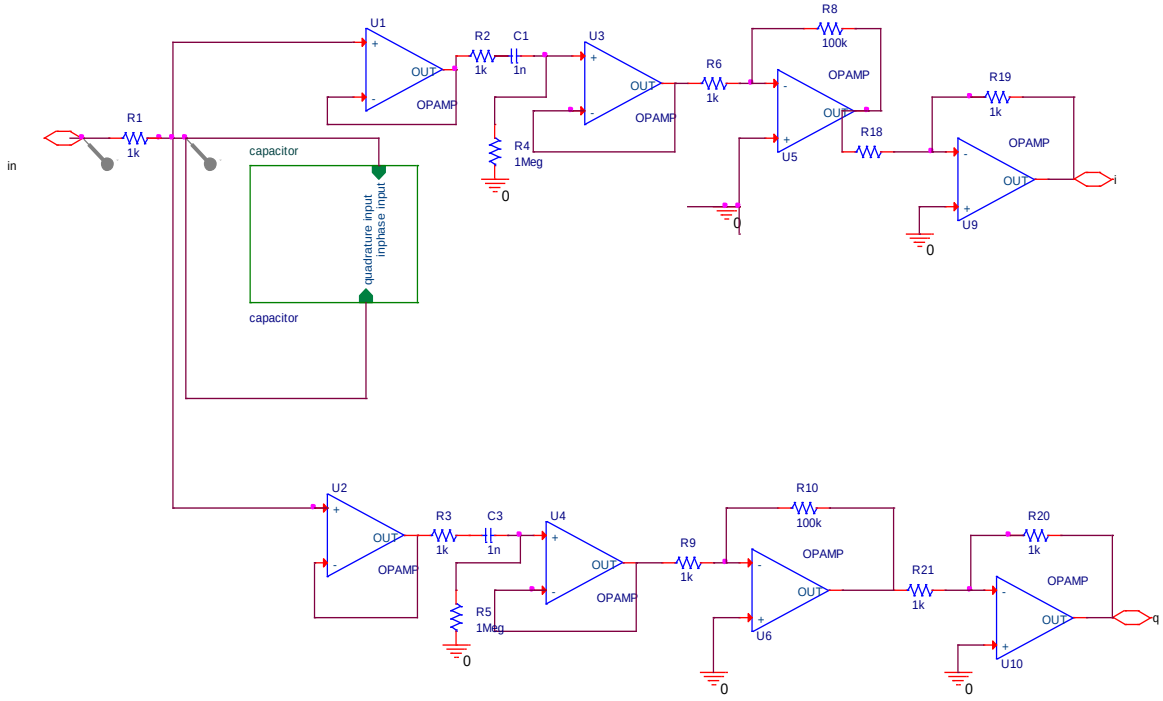


Figure 6.8 Signal processing block

The Dc eliminating block uses a capacitor to avoid DC and eliminate the DC which was required to Bias the complex capacitor circuit. Further the amplifier stage amplifies and the inverter is used to eliminate the 180 degree phase shift provided by the inverting amplifier.

6.5 Final project

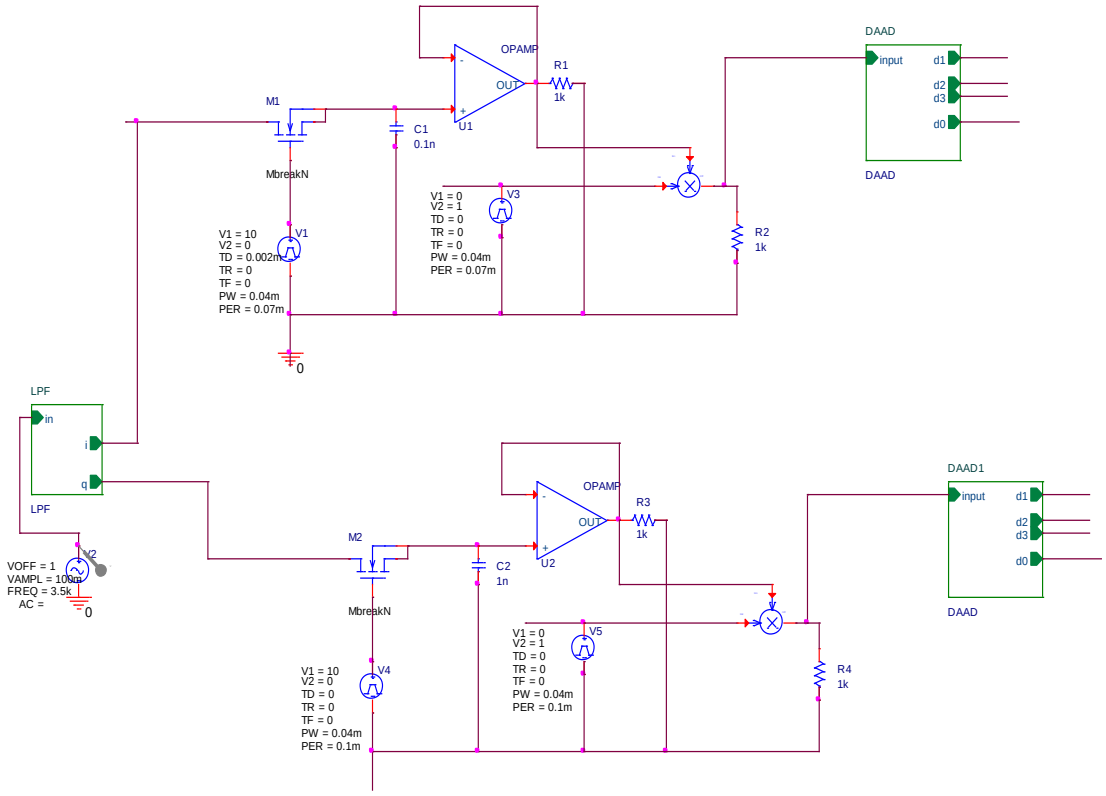


Figure 6.9 Final project

The final project circuit diagram is shown above which consists of signal processing block , sample and hold circuit and the encoder circuit which converts analog to digital signal,the encoder includes the quantizer, the step size of the quantizer can be varied by changing gain of the amplifier connected at the output stage of the D/A.

The output of the D/A

Vo = (step size)×(gain of amplifier cascaded)×(decimal equivalent of the bits at input)

This gives the voltage which is to be compared with input signal sample by the opamp whose output is required by the counter to update accordingly.

6.6 Output of some sample input

This part of the graph shows how the sample is taken and held till it is traced by to digital counter.

This part of the graph shows how digital bits are tracing an Analog input sample

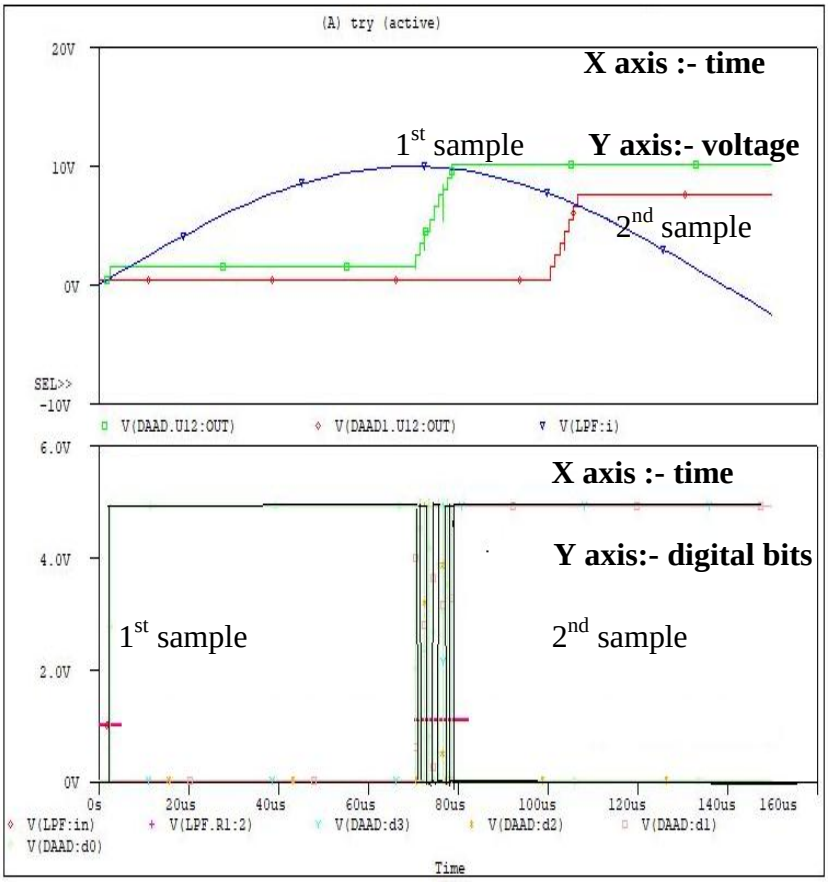


Figure 6.10 Output of Project

The time varying signal from the signal processing block is sent to the sample and hold circuit. The sample and hold circuit samples and holds the voltage till the A/D converter converts the held analog sample to digital equivalent. The sample must be taken at a rate greater than the Nyquist rate so the message signal can be recovered from the sample at the receiver end. The Nyquist sampling theorem is very useful in communication system because it decides the bandwidth required to send the signal via transmission line (air, copper wire, optical fiber, etc,). The higher is the sampling rate the more accurately the signal will be reconstructed at the receiver but the more bandwidth will be required to transmit or store the signal.

Counter tracks the same Analog Input

This shows the tracking of D/A

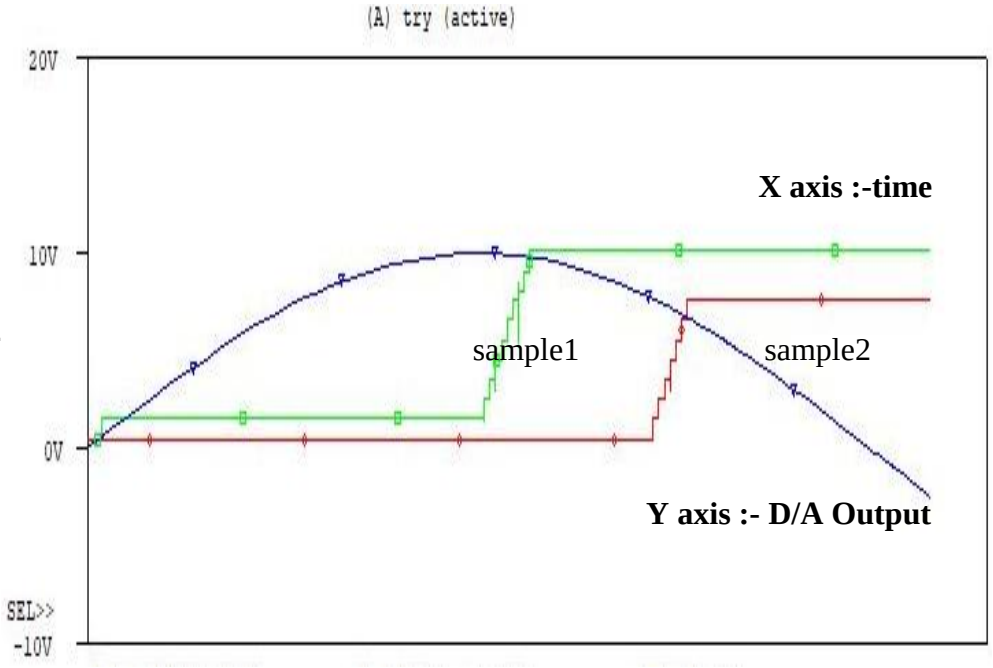


Figure 6.11 Counter Final Output with sampling of input wave

From the above figure it is clear that, the D/A output voltage changes with the changing bits of the counter. As the counter bits increase in digital counts the voltage level of the D/A converter also increases till the analog sample is traced. The transient faced by the Digital bits of the counter should be avoided before the transmission because these won't have any relation with message signal once sent in the transmission line. Such situation is avoided by a latch placed at the output of the counter which only gives output when the steady state is reached by the counter. Thus it results in another constraint on the Bandwidth of the transmission.

6.7 Future scope of the project

Once the digital bits are generated for the in phase and the quadrature phase component of the signal, these bits can be converted into Amplitude shift keying or phase shift keying or frequency shift keying modulation and then they can be transmitted via an antenna.

6.7.1 Amplitude Shift Keying

It is a modulation technique in which if a bit is '1' the pulse signal is multiplied with a carrier signal of high frequency to generate band pass modulation, whereas if the bit is '0' no signal is sent. The probability of error in this comes out to be as follows:

$$P_e = Q\sqrt{\frac{E}{2N}}$$

Where E is the bit energy, N is the power density of white noise and Q is the standard function

$$Q(x) = \frac{\int_x^{\infty} e^{-\frac{y^2}{2}} dy}{\sqrt{2\pi}}$$

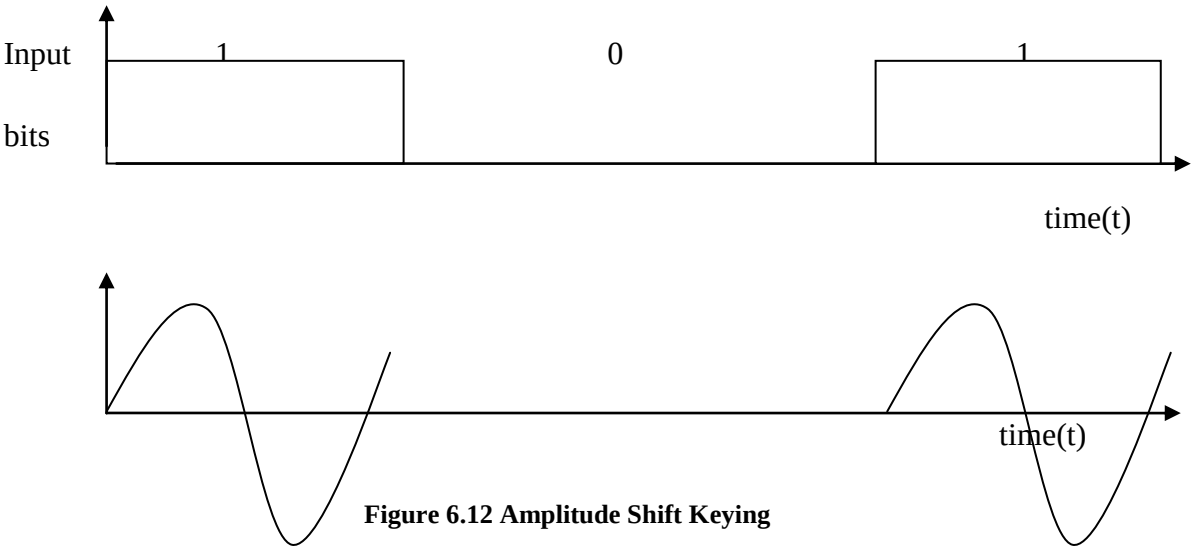


Figure 6.12 Amplitude Shift Keying

6.7.2 Frequency Shift Keying

It is a band pass modulation technique in which if bit is '1' one frequency signal is sent via antenna and if bit is '0' another frequency is sent via antenna.

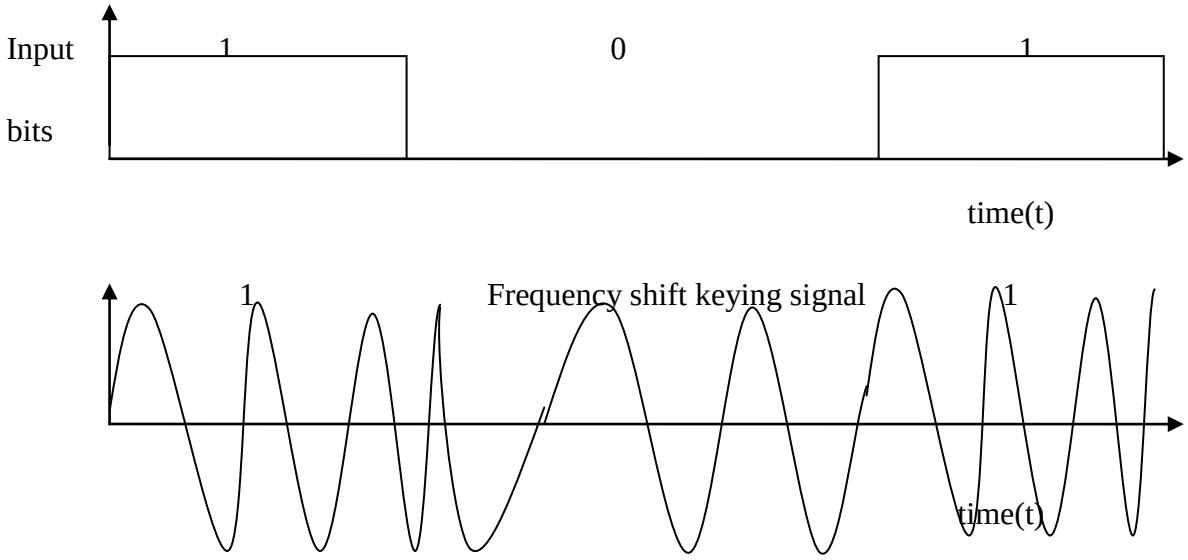


Figure 6.13 Frequency Shift Keying

$P_e = Q\sqrt{\frac{E}{N}}$

6.7.3 Phase Shift Keying

It is a band pass modulation technique in which if the bit is '1' one phase is transmitted and if the bit is '0' another phase signal is transmitted via antenna. This is the best scheme in terms of probability of error as it offers least probability of error.

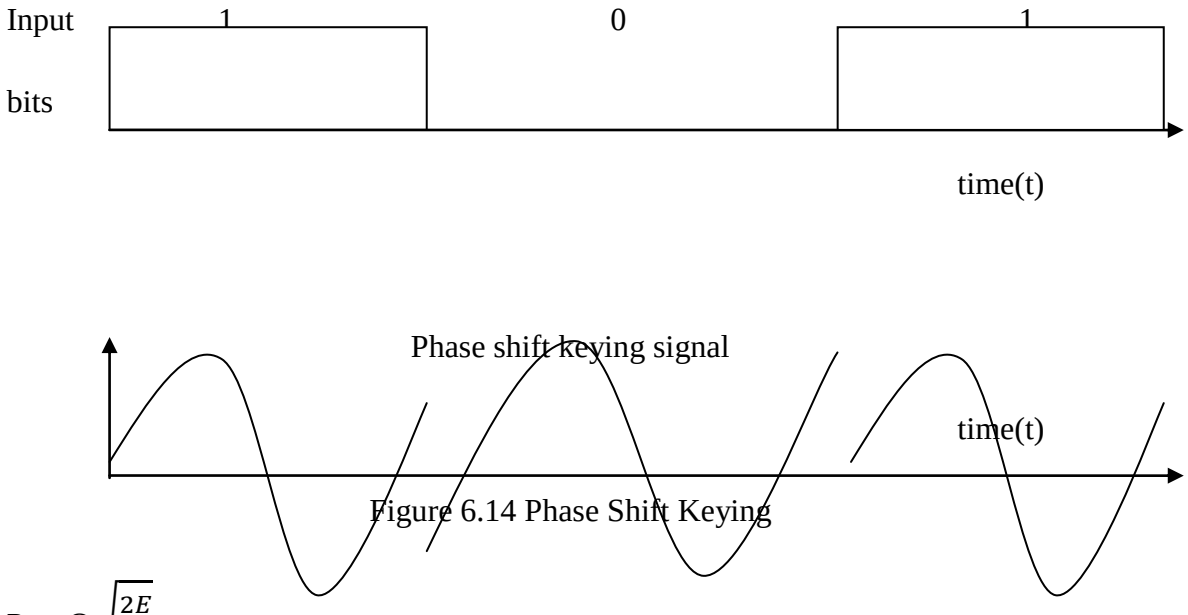


Figure 6.14 Phase Shift Keying

$P_e = Q\sqrt{\frac{2E}{N}}$

6.8 Merits of the project

The project deals with sending 2 sets of bits into the transmission line, the 1st one is in phase signal and the 2nd one is the complemented signal. Therefore, if this in phase and quadrature phase signal component is sent in the transmission line then one is able to send 2 signals at a time encouraging multiplexing. Even though the project is about generating in phase and qudrature signal multiplexing and does not employ the complex filter upto its full potential, it has a great future scope when one can easily remove the image signal problem from the super hetrodyne receiver and encourage multiplexing of 2 signals.

6.9 Limitations of the project

1. The D/A and A/D module of the project does not deal with negative voltages. Therefore, the negative signals cannot be processed by the project.
2. The benefits of the complex filter are not employed to full potential.
3. Using counter type A/D converter makes the system slow.
4. The analog sample must be held at the input of A/D converter till the conversion is in process.
5. Instead of using counter type A/D converter one can use successive approximation type A/D which is more faster.

References:-

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[9] https://www.electrical4u.com/nmos-and-pmos-logic

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Mos parameter used:-

.model MbreakP PMOS (LEVEL= 1

+VTO = -0.7 GAMMA= 0.4 PHI= 0.8

+NSUB = 5e+14 LD = 0.09e-6 uo = 100

+LAMBDA= 0.2 TOX = 9e-9 PB= 0.9

+CJ= 0.94e-3 CJSW = 0.32e-11 MJ =0.5

+MJSW=0.3 CGDO = 0.3e-9 JS= 0.5e-8)

.model MbreakN NMOS (LEVEL = 1

+VTO = 0.7 GAMMA = 0.45 PHI = 0.9

+NSUB = 9e+14 LD = 0.08e-6 UO = 350

+LAMBDA = 0.1 TOX = 9e-9 PB = 0.9

+CJ = 0.56e-3 CJSW = 0.35e-11 MJ = 0.45

+MJSW = 0.2 CGDO = 0.4e-9 JS = 1.0e-8)