IMPLEMENTATION OF ANALOG SIGNAL PROCESSING CIRCUITS USING EXCCII

A DISSERTATION

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FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN & EMBEDDED SYSTEMS

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I, (Radha Kalyani Ruppa), Roll No. 2K16/VLS/16 student of M.Tech (Vlsi & Embedded systems), hereby declare that the project Dissertation titled "Implementation of Analog Signal Processing circuits using EXCCII" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "Implementation of Analog Signal Processing circuits using EXCCII" which is submitted by Radha Kalyani Ruppa, 2k16/vls/16, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Analog signal processing (ASP) is any type of signal processing conducted on continuous analog signals by some analog means as set of continuous values (as opposed to the discrete digital Signal Processing (DSP) where the signal processing is carried out by a digital process). DSP suffers of fundamental drawbacks, such as high cost analog-digital conversion, high power consumption and poor performance at high frequencies. To overcome these drawbacks, ASP is preferred.

Current mode (CM) blocks offers advantages over voltage mode (VM) blocks, such as performance improvement, low power consumption, controlled gain without feedback components, better linearity and improved bandwidth. This gives the motivation to use CM block to implement various ASP applications and to review already existing literatures available using CM blocks. Current conveyor is used as it is a high-performance active element and it ensures high accuracy, wide bandwidth and exceptionally high slew rates combined with low voltage and low power implementations under small or large signal conditions. As compared to op-amp based circuits, the conveyor based circuits offers a higher gain-bandwidth product which makes it an ideal choice for modern applications in analog signal processing. Extra X- second generation current conveyor (EXCCII) is one of the new emerging CM block. In the process, an EXCCII with buffered output is used which is a modified second generation current conveyor that provides an extra input terminal. The block EXCCII has been verified and its applications on electronic functions like amplitude shift keying (ASK), binary phase shift keying (BPSK), current mode half wave and full wave rectifiers have also been verified. All pass filter, current mode universal and biquad filter have been explored.

From literature survey done it is found that, instrumentation amplifier, oscillators, multivibrators have not been explored using EXCCII. This inspires me to do work on applications mentioned above. The new topology of instrumentation amplifier (IA) using EXCCII is proposed and analyzed which is working in current mode (CM) and has high input impedance, low output impedance, high differential mode gain and high CMRR. Another application using EXCCII is mixed mode three phase oscillator may also be proposed and is under analysis. A feedback scheme consisting of two lossy integrators followed by a lossless inverting integrator is employed to obtain three voltage-mode and three current-mode sinusoidal signals simultaneously. The functionality of the two proposed circuits are analyzed through PSPICE simulation using 250 nm (0.25μm) TSMC technology parameters.

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LIST OF ABBREVIATIONS AND SYMBOLS

ASP	:	Analog Signal Processing
DSP	:	Digital Signal Processing
CM	:	Current Mode
VM	:	Voltage Mode
CC	:	Current Conveyor
CCI	:	First generation current conveyor
CCII	:	Second generation current conveyor
CCIII	:	Third generation current conveyor
DX-CCII	:	Dual X second-generation current conveyor
EX-CCII	:	Extra –X second generation current conveyor
IA	:	Instrumentation amplifier
OTA	:	Operational transconductance amplifier
CMOS	:	Complementary MOSFET
CMRR	:	Common mode rejection ratio
CRO	:	Cathode ray oscilloscope
THD	:	Total harmonic distortion
MTSO	:	Mixed mode three-phase sinusoidal oscillator
FO	:	Frequency oscillations
CO	:	Condition of oscillations

CHAPTER 1

1.1 Introduction

Signal processing finds many applications in communication systems, biomedical engineering, instrumentation, control systems, etc. can be implemented in two different ways:

1. Analog (continuous) method.
2. Digital (discrete) method.

The analog approach to signal processing was dominant for many years. This uses analog circuit elements such as resistors, capacitors, diodes, transistors, etc. Analog signal processing (ASP) is based on the natural ability of analog systems to solve the differential equations that describe a physical system. The solutions are obtained in real time. In contrast digital signal processing (DSP) relies on numerical calculations, this method may or may not give results in real time. DSP suffers from significant drawbacks, such as high-cost analog-digital conversion, high power consumption and poor performance at high frequencies. To overcome these drawbacks, ASP is preferred.

Nowadays current mode (CM) blocks are widely using in the analog platform because of its broad dynamic range, more bandwidth, linearity, simple analog circuit design and parasitic components effect less in current mode circuit while in voltage mode (VM) blocks limited dynamic range because of the frequency dependency of its gain.

The current conveyor is used as it is a high-performance active element and it ensures high accuracy, exceptionally high slew rates combined with low voltage and low power implementations under small or large signal conditions and wide bandwidth. As compared to op-amp based circuits, the conveyor based circuits offer a higher gain-bandwidth product which makes it an ideal choice for modern applications in analog signal processing (ASP).

1.1.1 Voltage Mode and Current Mode

When signals, depicts the information being processed, are in form of electric voltages. In contrast to current mode which employs electric currents. The analog circuits where the circuit performance is determined in terms of a voltage levels at various nodes including input and output nodes are named as voltage-mode (VM) circuits. The VM circuits are required to provide large output swing while diminishing the total power consumption. This leads to high impedance node architecture of the VM circuits. Yet, the parasitic capacitances present in the circuits need to be charged and discharged with high voltage swing, thereby limiting the slew rate and speed of the VM circuits. Although, BJTs and FETs are current devices, but generally configured into voltage oriented networks [1]. The current signal is moved into voltage domain causing system bandwidth to reduce, and create dominant pole at low frequency as parasitic capacitances with high valued node resistances. Thus simultaneous low power, low voltage and wide bandwidth operations are difficult to accomplish in VM circuits.

Over the last few decades CM processing circuits have been established as an unconventional design technique using current signals for signal processing [2]. The CM circuits are low impedance node networks, and therefore low time constant circuits, too. This improves system performance in terms of speed and slew rate. In current amplifiers the transistors are useful almost up to their unity gain bandwidth f_T, so resulting in wider bandwidth. Yet another advantage of CM circuits results from the nonlinear characteristic of transistors. In FETs the volatge is proportional to square root of current in saturation region of operation, similarly in BJTs the voltage depends logrithmically on current. If current instead of voltage is used as signal, the output swing reduces and hence the CM circuits can operate under low supply voltage [3]. Hence for a fixed supply voltage the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. Furthermore, in CM circuits the addition and subtraction operation can be performed by connecting the terminals at a single point resulting in simple architecture as compared to VM circuits. This may result in chip area and power saving.

CM blocks also offers advantages such as controlled gain without feedback components, performance improvement, better linearity over VM blocks. This gives the motivation to use CM block to implement various ASP applications [4-41]. Literature survey suggests that there are

neumerous CM blocks are alreadily available. The details of some of CM blocks are listed below.

Current- mode signal processing has resulted in emergence of numerous analog building blocks [42-57] which are used for realization of various signal processing and generation circuits. The current conveyor (CC) [45], a voltage/current hybrid circuit, is the most extensively explored block. The three generations of CC namely CCI, CCII [42], and CCIII [46], were introduced way back in 1968, 1970 and 1995 respectively and are differ in terms of port characteristics. Variety of alterations in the basic conveyor structure, for more effective operation, led to introduction of various CC based newer elements [47] – [57]. Very recently, the second generation current conveyor was further extended to Extra-X second-generation current conveyor (EXCCII)[7]. Chapter 2 describes the device characteristics of EXCCII.

CHAPTER 2

2.1 Extra-X second generation current conveyor (EXCCII)

The idea of the extra-X terminal in second generation current conveyor (EXCCII) was recently given in [7]. The EX-CCII macro model contains the extra X-terminal with the additional feature of the voltage generated at output Z terminal is buffered to the W terminal. Which is a modified version of the second-generation current conveyor that provides an extra input terminal concerning former Dual X second-generation current conveyor (DXCCII). The potential of the Y terminal is copied to the X_1, and X_2 terminals and similarly the current at X_1 and X_2 is copied to the Z_1 and Z_2 terminals respectively. Its circuit symbol is shown in Fig. 1.

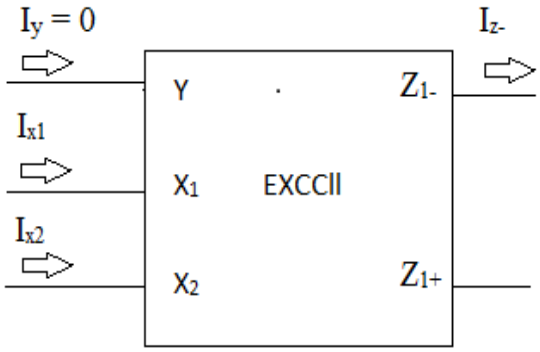

Fig 1. Symbol of EX-CCII with buffered output[8].

The relationship between port voltages and currents can be characterized by the following matrix.

$$\begin{bmatrix} I_y \\ V_{x1} \\ V_{x2} \\ I_{z1} \\ I_{z2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & R_{x1} & 0 & 0 & 0 \\ 1 & 0 & R_{x2} & 0 & 0 \\ 0 & P_1 & 0 & 0 & 0 \\ 0 & 0 & P_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_{x1} \\ I_{x2} \\ V_{z1} \\ V_{z2} \end{bmatrix}$$

The above matrix gives the following equations

$I_y = 0$, $V_{x1} = V_y + R_{x1}I_{x1}$,$V_{x2} = V_y + R_{x2}I_{x2}$, $I_{z1} = P_1I_{x1}$, $I_{z2} = P_2I_{x2}$

Here, Rx_1 and Rx_2 are intrinsic resistances at terminal X_1 and X_2.

$R_{x1} = R_{x2} = \frac{1}{\sqrt{8\mu C_{ox} W/L I_o}}$, where Io is biasing current. And p1 and p2 are current copy factor from X_i to Z_i.we have used p_1 = -1,1 and p_2 = -1,1 .

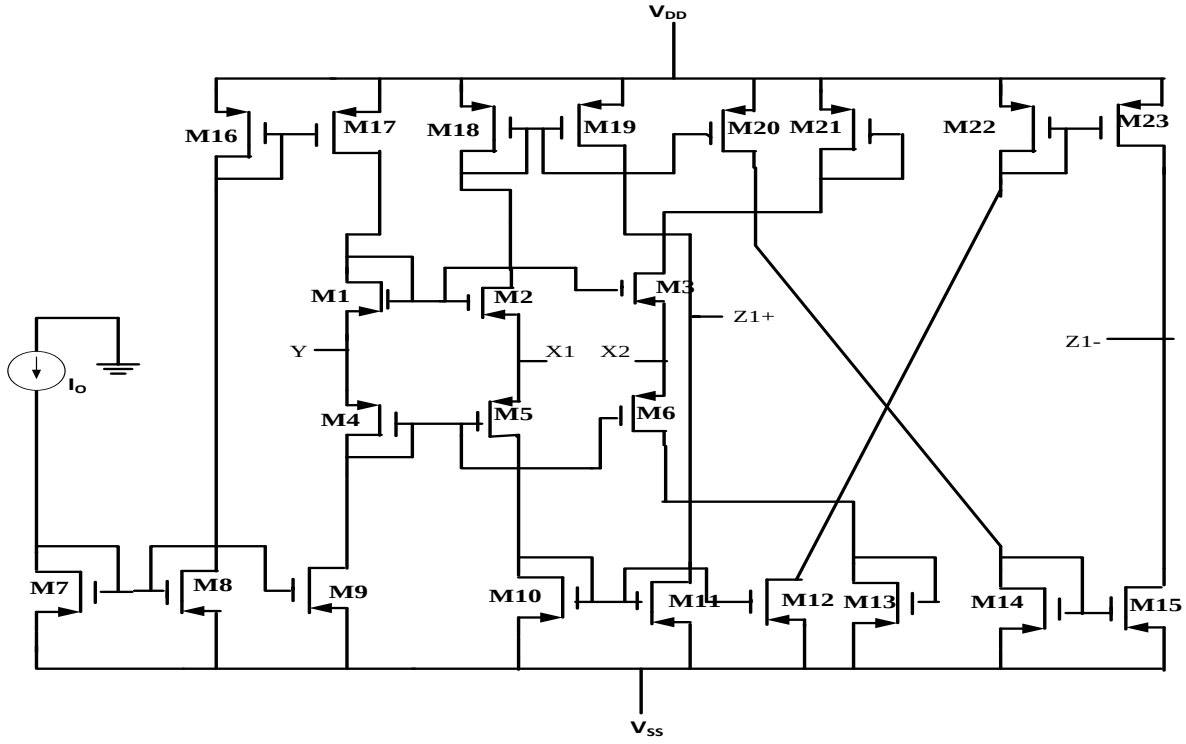

Fig 2. CMOS implementation of EXCCII [8]

The port relation of EXCCII has been verified using PSPICE simulation with 250nm process parameters. In Fig 2. the supply voltage V_{DD} = 1.25 V and V_{SS} = -1.25 V and bias current Io = 10 μA is used.

The aspect ratio of the transistors is given in Table 1.

Table1. Aspect ratios of transistors

MOS	W(µm)	L(µm)
M1,M2,M3,M16,M17,M18 M19,M20,M21,M22,M23	10	0.5
M4, M5, M6	16	0.5
M7,M8,M9,M10,M11,M12 M13,M14,M15	6	0.5

2.2 Device Characteristics

The EXCCII block is tested as shown in Fig 3, to check the port relationship. A voltage source is applied at terminal Y and copied voltage at X1 and X2 is traced as in Fig 4. A voltage source (V) is varied from -5V to +5V. From Fig 4 it is clear that EXCCII follows the voltage at Y in the range -2.33V to 2.33V.

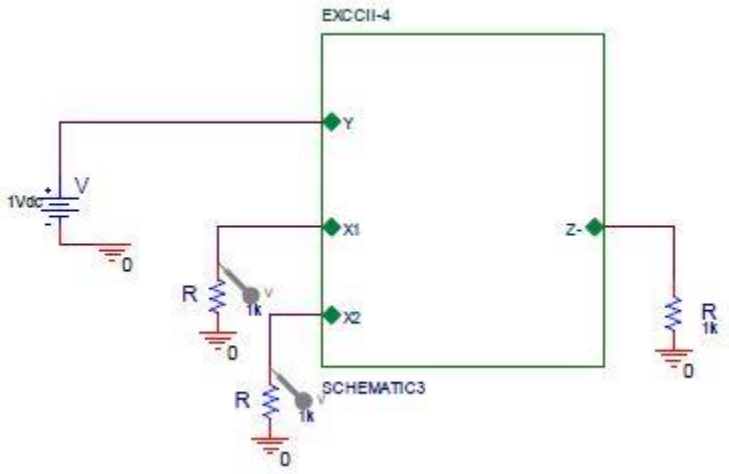

Fig 3 Circuit for testing voltage transfer characteristic of EXCCII

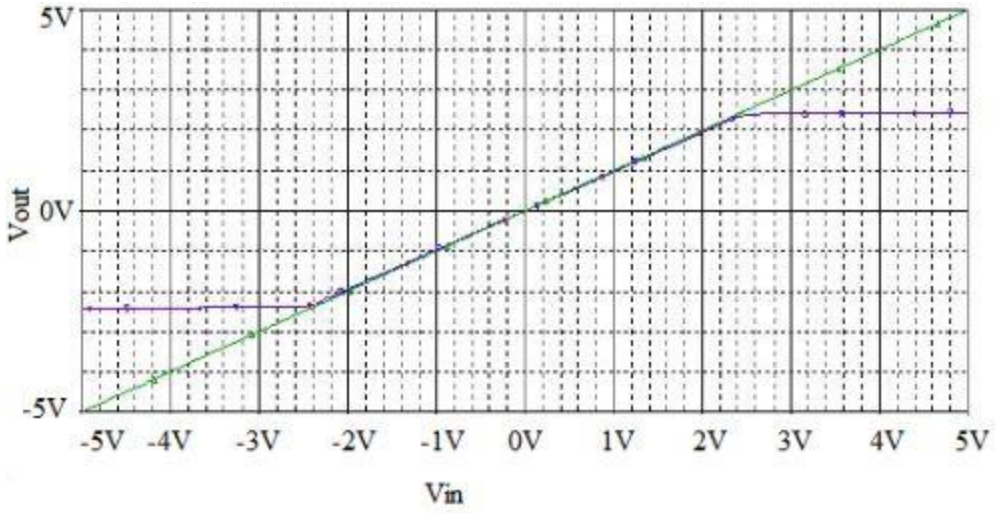

Fig 4. Voltage transfer characteristic of EXCCII.

The current relationship is also tested by applying a current source (I_{28}) in Fig 5. Current source I_{28} is varied from -10mA to +10mA. From Fig 6 it is clear that EXCCII follows the current at X1 hence it also follows at Z- ranging -1.26mA to 1.26mA

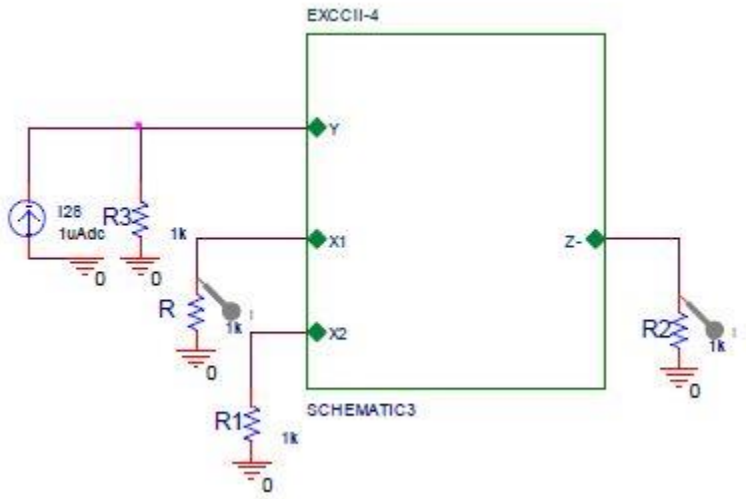

Fig 5. Circuit for testing current transfer characteristic of EXCCII

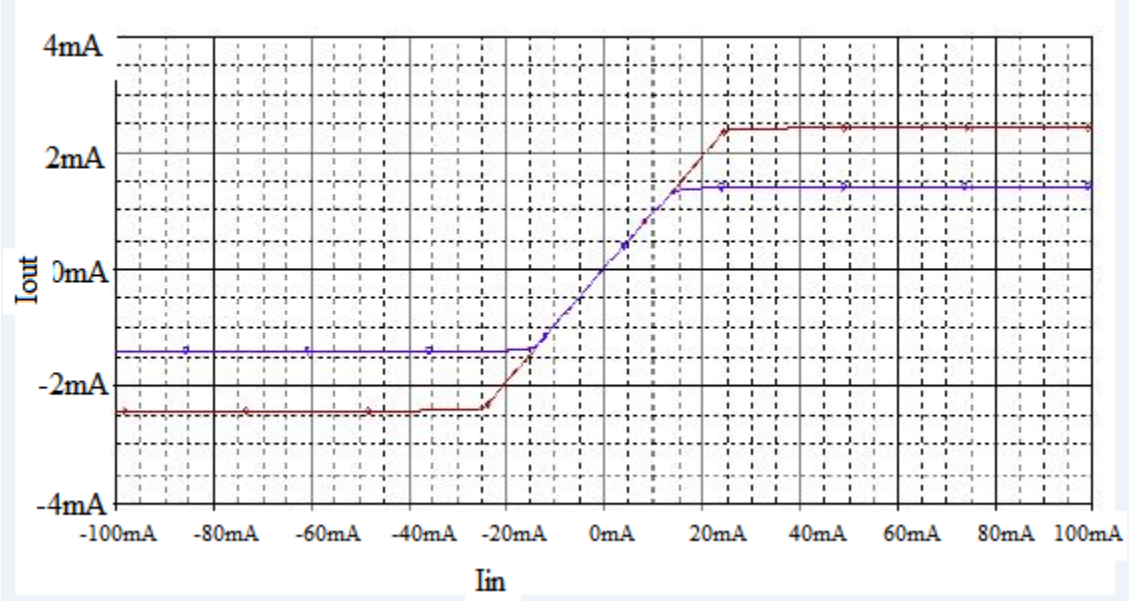

Figure 6. Current transfer characteristic of EXCCII.

The two analog applications using EXCCII have been proposed. One is the Instrumentation amplifier (IA). Another is Mixed-mode three phase oscillator.

CHAPTER 3

3.1 Instrumentation amplifier (IA)

An instrumentation amplifier is a type of differential amplifier which consists of input buffer amplifiers, which eliminates the need for input impedance matching and thus make the amplifier predominantly suitable for use in measurement and test equipment. Additional characteristics include very high input impedance, low drift, very low DC offset, low noise, very high open-loop gain, and very high common-mode rejection ratio. Instrumentation amplifiers are used where high accuracy and stability of the circuit both short and long-term are required.

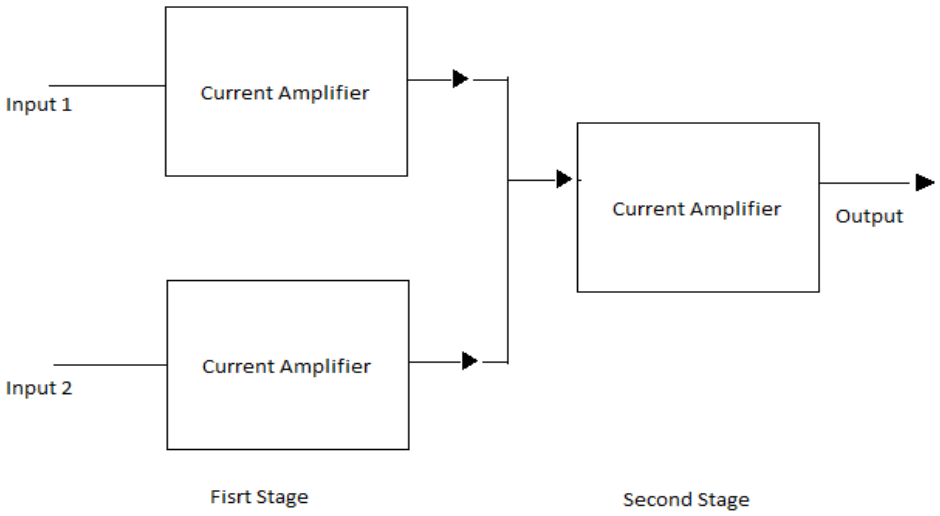

Fig 7: Instrumentation amplifier

In instrumentation amplifier (IA), two inputs are applied to separate current amplifiers and then amplified the output of both the amplifiers are then differenced and then applied to another current amplifier which gives the final output of the IA. The advange is, it doesn't require input impedance matching, This makes the amplifier ideal for testing and measuring various equipment. Instrumentation amplifier has a low DC offset. It doesn't generate any noticeable noise, and the drift is considerably low. IA is very stable and hence best for long-term

as well as short-term use. IA has a controlled circuit, but it can be simply varied or adjusted by functioning on the gain value. There is no need to change the circuit or its structure.

IA works with the input and therefore doesn't really depend much on the various factors that effect the output at the final stages. We can understand more about an instrument's output ability only if we know the input very well. The outputs will anyway depend on many associated and disassociated factors. Using IA we can amplify small input to a greater extent. With amplification of outputs, there is still a need for considerable input, only then can you amplify to a desired extent. The only concern with instrumentation amplifier is the super imposing of the original wave when the noise or sound gets transmitted over a long range. The system will depend on special cables that can cancel this noise or super imposition.

3.2 LITERATURE SURVEY

IAs are of supreme importance in the overall performance of a signal acquisition system. They play a dynamic role in extracting low-value differential signals from unwanted common mode ones which tend to corrupt them. The traditional method of implementing IA based on 3 op-amps and 7 resistors is not striking anymore because of its high power consumption, gain-dependent bandwidth and strict matching requirement between resistors. To overcome the requirement of matched resistors, recently many unconventional ways to implement IAs are explored using both VM and CM, based on OTA, Current Conveyors and other building blocks. IA have also been implemented using many different type of components and techniques like second generation controlled current conveyor (CCCII) [9] , CMOS nested chopping technique [10] , instrumentation amplifier with improved gain and CMRR for low power sensor applications [11] , low power CMOS subthreshold current mode instrumentation amplifier based on CCII [12] , operational floating current conveyor based instrumentation amplifier [13], micropower CMOS instrumentation amplifier [14], low-noise CMOS instrumentation amplifier for thermoelectric infrared detectors [15] and many more.

Hence as per literature survey and best to my knowledge it is found that there is no implementation of instrumentation amplifier using EXCCII in recent past.

3.3 Proposed Instrumentation amplifier

The EXCCII discussed in Fig 2 is used in the realization of an instrumentation amplifier. The proposed circuit uses six resistors. The circuit uses 3 EXCCII blocks with both negative and positive output at Z1 which is shown in Fig 8.

From the port matrix of EXCCII, we get

$$V_{x1} = V_y + I_{x1}R_{x1}; V_{x2} = V_y + I_{x2}R_{x2}; \tag{1}$$

From circuit analysis, we get

$$V_y = I_{in}R_1, I_{x1} = \frac{-V_{x1}}{R_2} \tag{2}$$

$$V_{x1} = I_{in}R_1 + (-V_{x1})\frac{R_{x1}}{R_2} \tag{3}$$

$$I_{in}R_1 = V_{x1}\left(1+\frac{R_{x1}}{R_{x2}}\right) \tag{4}$$

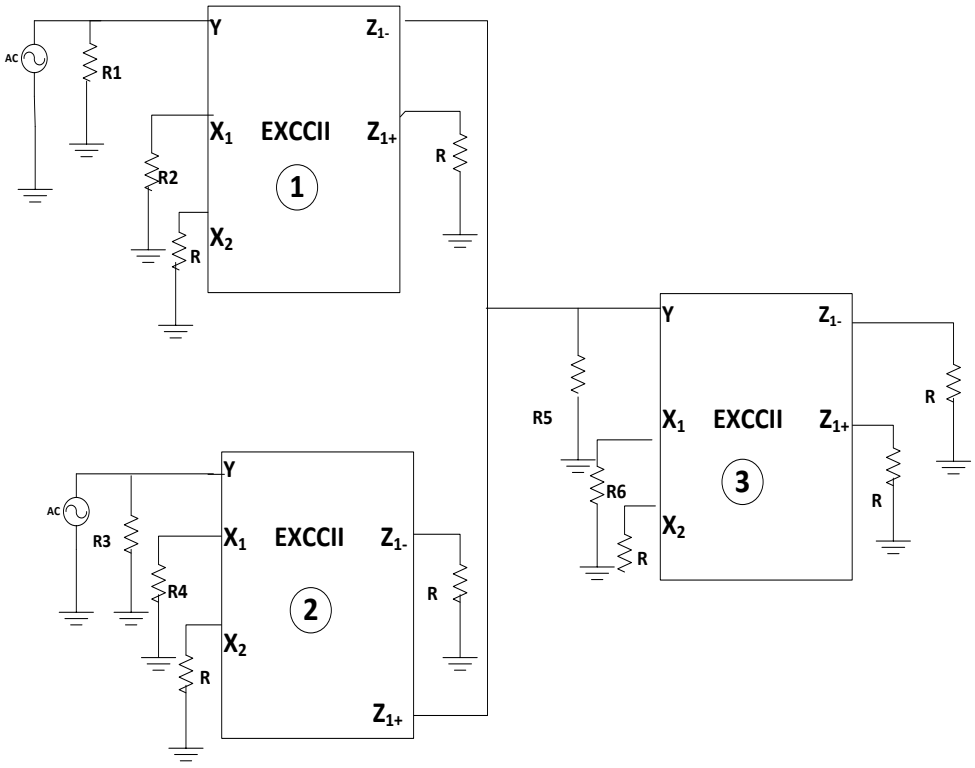

Fig 8. Proposed circuit amplifier using EXCCII

$$I_{z1-} = \frac{-I_{in1}R_1}{\left(1+\frac{R_{x1}}{R_2}\right)R_2}, \quad I_{z1+} = \frac{I_{in2}R_3}{\left(1+\frac{R_{x1}}{R_4}\right)R_4} \tag{5}$$

$$Io = I_{z1-} + I_{z1+} \tag{6}$$

$$I_{out} = \frac{-I_o R_5}{\left(1+\frac{R_{x1}}{R_6}\right)R_6} \tag{7}$$

$$I_{out} = \frac{-\left(\frac{I_{in2}R_3}{\left(1+\frac{R_{x1}}{R_4}\right)R_4} - \frac{I_{in1}R_1}{\left(1+\frac{R_{x1}}{R_2}\right)R_2}\right)R_5}{\left(1+\frac{R_{x1}}{R_6}\right)R_5} \quad (8)$$

So, we get the final output current equation as :

$$I_{out} = \frac{-\left[\left[\frac{R_3}{\left(1+\frac{R_{x1}}{R_4}\right)R_4} - \frac{R_1}{\left(1+\frac{R_{x1}}{R_2}\right)R_2}\right]I_{cm} + \left[\frac{R_3}{\left(1+\frac{R_{x1}}{R_4}\right)R_4} + \frac{R_1}{\left(1+\frac{R_{x1}}{R_2}\right)R_2}\right]\frac{\Delta}{2}\right]R_5}{\left(1+\frac{R_{x1}}{R_6}\right)R_6} \quad (9)$$

$$\text{Differential Mode Gain} = \frac{1}{2}\frac{-\left(\frac{R_3}{\left(1+\frac{R_{x1}}{R_4}\right)R_4} + \frac{R_1}{\left(1+\frac{R_{x1}}{R_2}\right)R_2}\right)R_5}{\left(1+\frac{R_{x1}}{R_6}\right)R_6} \quad (10)$$

$$\text{Common Mode Rejection Ratio(CMRR)} = \frac{1}{2}\frac{\frac{R_3}{\left(1+\frac{R_{x1}}{R_4}\right)R_4} + \frac{R_1}{\left(1+\frac{R_{x1}}{R_2}\right)R_2}}{\frac{R_3}{\left(1+\frac{R_{x1}}{R_4}\right)R_4} - \frac{R_1}{\left(1+\frac{R_{x1}}{R_2}\right)R_2}} \quad (11)$$

This CMRR is calculated while taking in account the intrinsic resistance at port X_1 and X_2.

3.4 Nonideal and Parasitic effects

3.4.1 Tracking errors

The response of the proposed circuit deviates from the ideal one due to nonidealities of the active elements. The nonideal EXCCII is described by the following relationship:

$$V_{x1} = \beta_1 V_y + I_{x1} R_{x1};\ V_{x2} = \beta_2 V_y\ +\ I_{x2} R_{x2} \tag{12}$$

Where β_1, β_2 is the voltage transfer gains from the Y terminal to the X_1 and X_2 terminals respectively.

$$I_y = 0;$$
$$I_{z1-} = -\alpha_1 I_{x1},\ I_{z1+} = \alpha_2 I_{x1} \tag{13}$$

Where α_1, α_2 is the current transfer gains from the X1 terminal to the Z1- and Z1+ respectively. More specifically $\beta = (1-\varepsilon)$ and $\alpha = (1-\delta)$ where $|\varepsilon| << 1$ is the voltage tracking error and $|\delta| << 1$ is the current tracking error of the EXCCII.

From circuit analysis, we get :

$$V_y = I_{in} R_1;\ I_{x1} = \frac{-V_{x1}}{R_2} \tag{14}$$

$$V_{x1} = \beta_1 I_{in} R_1 + \frac{-V_{x1}}{R_2} R_{x1}\ \ V_{x1} = \beta 1 I_{in} R_1 + \frac{-V_{x1}}{R_2} R_{x1} \tag{15}$$

$$Vx1 = \frac{\beta_1 I_{in1} R_1}{1 + \frac{R_{x1}}{R_2}} \tag{16}$$

$$I_{x1} = \frac{\beta_1 I_{in1} R_1}{\left(1 + \frac{R_{x1}}{R_2}\right) R_2} \tag{17}$$

$$I_{z1-} = \frac{-\alpha_1 \beta_1 I_{in1} R_1}{\left(1 + \frac{R_{x1}}{R_2}\right) R_2},\ I_{z1+} = \frac{-\alpha_2 \beta_1 I_{in2} R_3}{\left(1 + \frac{R_{x1}}{R_4}\right) R_4}, \tag{18}$$

$$I_o = I_{z1-} + I_{z1+}$$

$$I_{out} = \frac{-I_0 \beta_1 I_{in1} R_5}{\left(1+\frac{R_{x1}}{R_6}\right) R_6} \tag{19}$$

$$I_{out} = \frac{\beta_1 R_5}{\left(1+\frac{R_{x1}}{R_6}\right) R_6} \left(\left(\frac{\alpha_2 \beta_1 R_3}{\left(1+\frac{R_{x1}}{R_4}\right) R_4} - \frac{\alpha_1 \beta_1 R_1}{\left(1+\frac{R_{x1}}{R_2}\right) R_2} \right) I_{cm} + \left(\frac{\alpha_2 \beta_1 R_3}{\left(1+\frac{R_{x1}}{R_4}\right) R_4} + \frac{\alpha_1 \beta_1 R_1}{\left(1+\frac{R_{x1}}{R_2}\right) R_2} \right) \frac{\Delta}{2} \right) \tag{20}$$

$$\text{Differential Mode Gain} = \frac{1}{2} \frac{\beta_1 R_5}{\left(1+\frac{R_{x1}}{R_6}\right) R_6} \left(\frac{\alpha_2 \beta_1 R_3}{\left(1+\frac{R_{x1}}{R_4}\right) R_4} + \frac{\alpha_1 \beta_1 R_1}{\left(1+\frac{R_{x1}}{R_2}\right) R_2} \right) \tag{21}$$

$$\text{CMRR} = \frac{1}{2} \frac{\frac{\alpha_2 R_3}{\left(1+\frac{R_{x1}}{R_4}\right) R_4} + \frac{\alpha_1 R_1}{\left(1+\frac{R_{x1}}{R_2}\right) R_2}}{\frac{\alpha_2 R_3}{\left(1+\frac{R_{x1}}{R_4}\right) R_4} - \frac{\alpha_1 R_1}{\left(1+\frac{R_{x1}}{R_2}\right) R_2}} \tag{22}$$

3.4.2 Parasitic effect

The performance of the proposed circuit is affected by the presence of various parasitics at the terminal of the active device. The various parasitics are the high resistance Ry parallel with low parasitic capacitor C_y at the Y terminal, series parasitic resistances R_{x1} and R_{x2} at the terminal X_1 and X_2 respectively which can be varied by the bias current Io as shown in Fig 2. The terminal Z exhibit a high resistance R_{z1} in parallel with low parasitic capacitor C_{z1} shown in Fig 9.

From the port relationship of EXCCII

$$V_{x1} = V_y \; + \; I_{x1}R_{x1}; V_{x2} \; = \; V_y + I_{x2}R_{x2} \tag{23}$$

$$I_{x1} = \frac{-V_{x1}}{R_2}; \; I_{z1-} \; = -I_{x1} \tag{24}$$

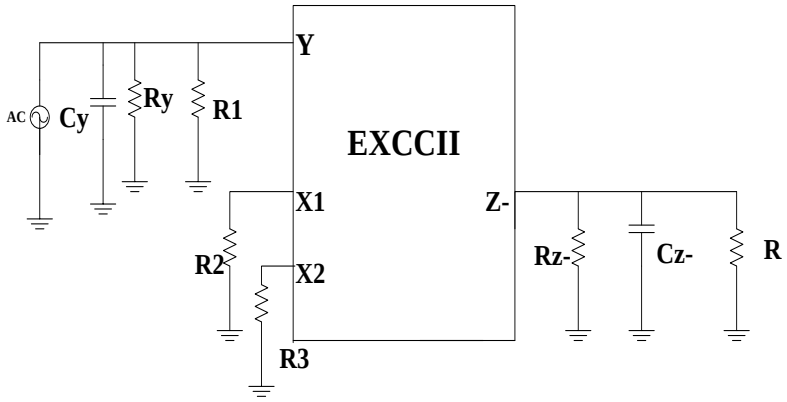

Fig 9. EXCCII with parasitic effect

From the routine analysis of Fig 5, we get :

$$V_y = \; I_{in1}R_1 \left| \right| \; R_y \left| \right| \; C_y = \frac{I_{in1}R_1R_y}{sC_yR_1R_y + R_1 + R_y} \tag{25}$$

$$V_{x1}\left(1 + \frac{R_{x1}}{R_2}\right) = \frac{I_{in1}R_1R_y}{sC_yR_1R_y + R_1 + R_y} \tag{26}$$

$$I_{z1-} = \frac{-I_{in1}R_1R_y}{\left(sC_yR_1R_y + R_1 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_2}}\right)\mathrm{R_2}} \; ; \; I_{z1+} = \frac{-I_{in2}R_3R_y}{\left(sC_yR_3R_y + R_3 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_4}}\right)\mathrm{R_4}} \tag{27}$$

$$I_o = \; I_{o-} + \; I_{o+}$$

$$I_{out} = \frac{-I_0R_5R_y}{\left(sC_yR_5R_y + R_5 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_6}}\right)\mathrm{R_6}} \tag{28}$$

$$I_{o-} = \frac{Z_z I_{z1-}}{Z_z + R} = \frac{-Z_z}{Z_z + R}\left[\frac{I_{in1} R_1 R_y}{\left(sC_y R_1 R_y + R_1 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_2}}\right)\mathrm{R_2}}\right]$$

(29)

$$I_{o+} = \frac{Z_z I_{z1+}}{Z_z + R} = \frac{-Z_z}{Z_z + R}\left[\frac{I_{in2} R_3 R_y}{\left(sC_y R_3 R_y + R_3 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_4}}\right)\mathrm{R_4}}\right] \quad (30)$$

where $Z_z = \frac{R_z}{1 + sC_z R_z}$

$$I_{out} = \frac{Z_z}{Z_z + R}\left(\frac{R_3 R_y}{\left(sC_y R_3 R_y + R_3 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_4}}\right)\mathrm{R_4}} - \frac{R_1 R_y}{\left(sC_y R_1 R_y + R_1 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_2}}\right)\mathrm{R_2}}\right) I_{cm} + \frac{Z_z}{Z_z + R} \quad (31)$$

$$\left(\frac{R_3 R_y}{\left(sC_y R_3 R_y + R_3 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_4}}\right)\mathrm{R_4}} + \frac{R_1 R_y}{\left(sC_y R_1 R_y + R_1 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_2}}\right)\mathrm{R_2}}\right)\frac{\Delta}{2}$$

Differential Mode Gain =

$$\frac{Z_z}{Z_z + R}\left(\frac{R_3 R_y}{\left(sC_y R_3 R_y + R_3 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_4}}\right)\mathrm{R_4}} + \frac{R_1 R_y}{\left(sC_y R_1 R_y + R_1 + R_y\right)\left(1 + \frac{\mathrm{R_{x1}}}{\mathrm{R_2}}\right)\mathrm{R_2}}\right) \quad (32)$$

$$\text{CMRR} = \frac{1}{2}\frac{\dfrac{R_3R_y}{\left(sC_yR_3R_y+R_3+R_y\right)\left(1+\dfrac{\mathrm{R_{x1}}}{\mathrm{R_4}}\right)\mathrm{R_4}} + \dfrac{R_1R_y}{\left(sC_yR_1R_y+R_1+R_y\right)\left(1+\dfrac{\mathrm{R_{x1}}}{\mathrm{R_2}}\right)\mathrm{R_2}}}{\dfrac{R_3R_y}{\left(sC_yR_3R_y+R_3+R_y\right)\left(1+\dfrac{\mathrm{R_{x1}}}{\mathrm{R_4}}\right)\mathrm{R_4}} - \dfrac{R_1R_y}{\left(sC_yR_1R_y+R_1+R_y\right)\left(1+\dfrac{\mathrm{R_{x1}}}{\mathrm{R_2}}\right)\mathrm{R_2}}} \tag{33}$$

3.5 Simulation results

3.5.1 Differential gain plot for proposed circuit

The plot for the differential gain of the instrumentation amplifier is shown in Fig 10. The plot is taken by applying the input value of 1µA at Y terminal of one EXCCII block, and 0µA at the Y terminal of other EXCCII block for different gains and corresponding resistance values are shown in the plot.

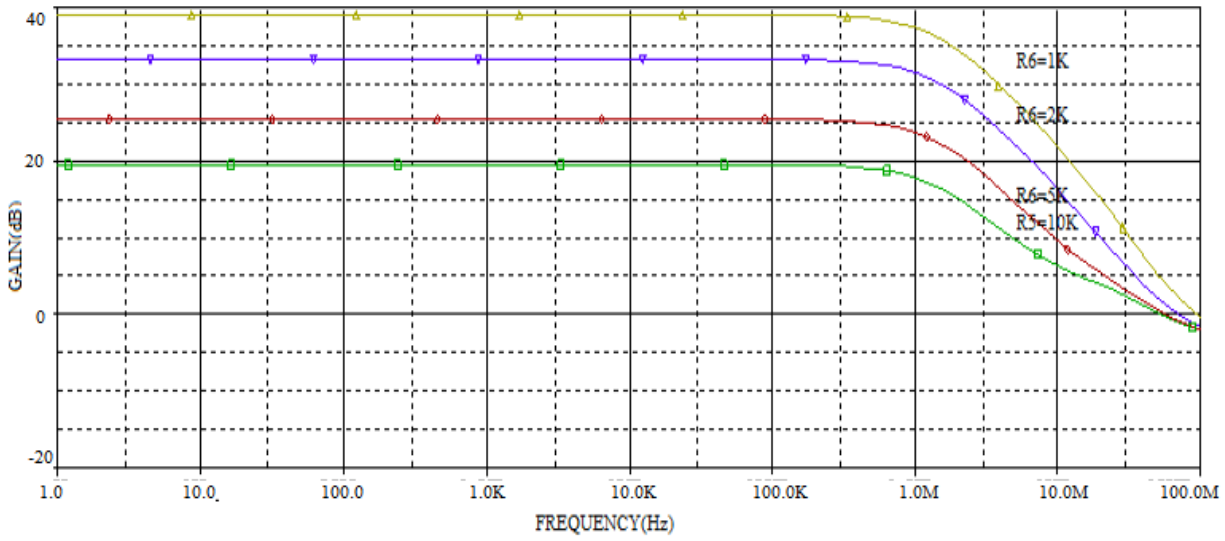

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Figure 10. Differential gain plot for proposed circuit

The differential gain is plotted for output stage gains of 1, 2, 5 and 10 by varying the value of resistance R_6 in Fig 9. The differential gain increases with an increase in the output stage gain, and the input stage gain is fixed at $R_1/R_2 = 10$.

3.5.2 CMRR plot for proposed circuit

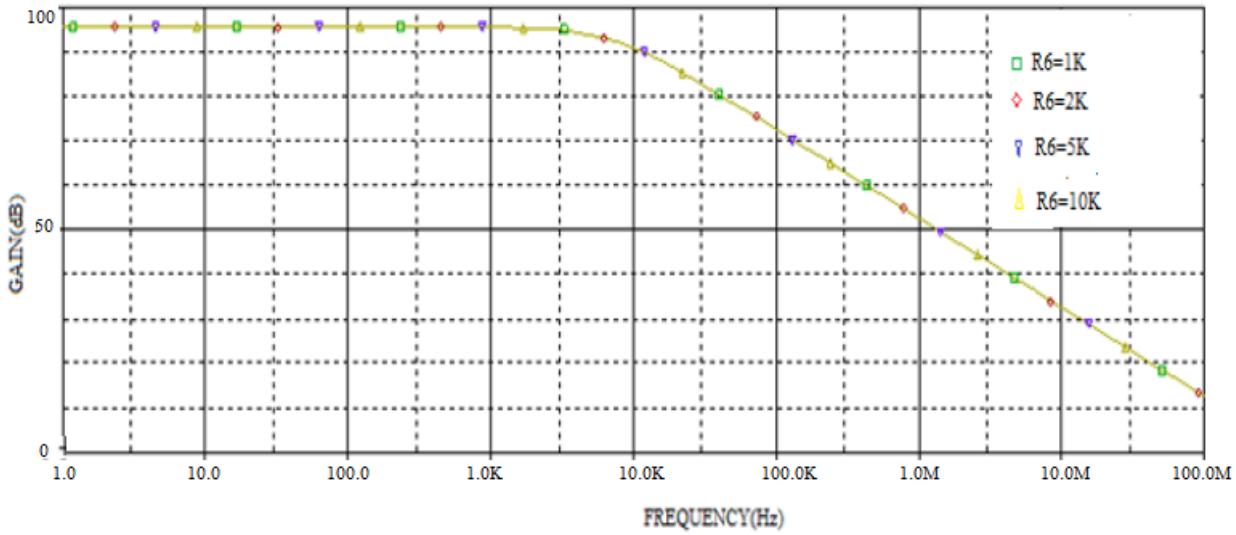

Figure 11. CMRR plot for proposed circuit

The CMRR is plotted for output stage gains of 1, 2, 5 and 10 by varying the value of resistance R_6 and the input stage gain is fixed at $R_1/R_2 = 10$ in Fig 11. The input stage gain is kept the same for both the input blocks.

The common mode gain is taFken by applying 1μA current source at the Y terminals of both the EXCCII blocks. The CMRR plot is constant, i.e., independent of the output stage gain.

CHAPTER 4

4.1 Proposed Circuit with improved CMRR

The CMRR is enhanced by using a common resistor between the two X1 terminals of both the input stage EXCCII blocks.

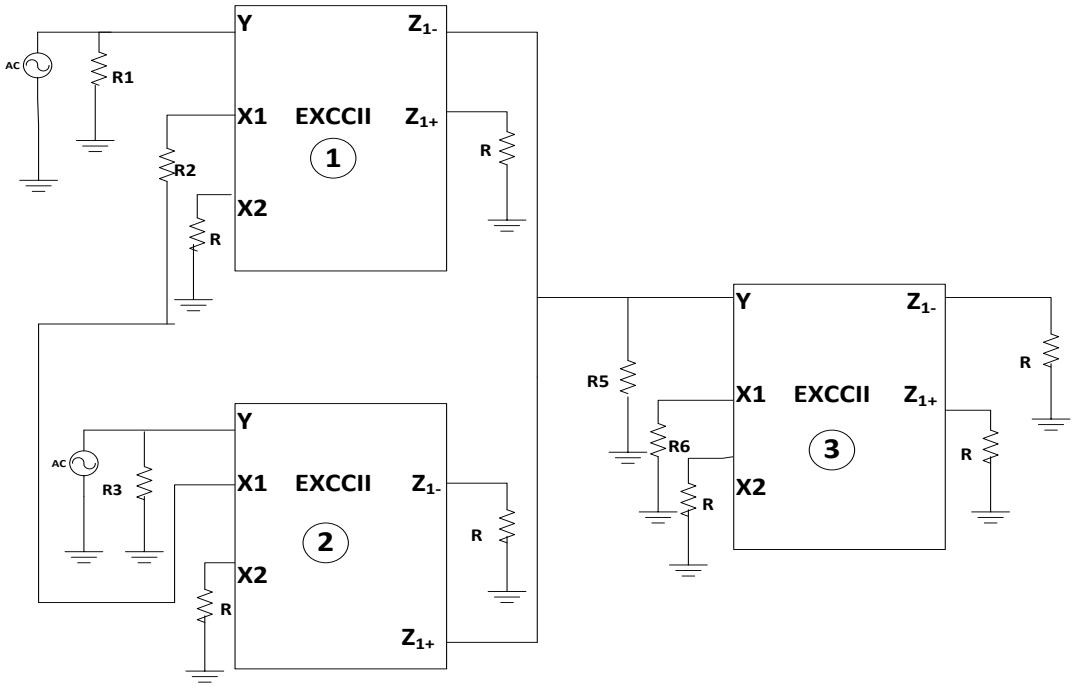

Fig 12. Proposed instrumentation amplifier with improved CMRR

This proposed circuit has a common resistance to make sure that the same current flows through the X_1 terminals of both the EXCCII blocks. `

The same current at both the X_1 terminals at least eliminates the current difference at X_1 terminals due to tracking errors in the block. Further tracking errors follow the same course and hence CMRR of the proposed circuit with improved CMRR.

4.2 Simulation results

4.2.1 Differential gain plot for a proposed circuit with improved CMRR

The plot for the differential gain of the proposed instrumentation amplifier with improved CMRR is shown in Fig 13. The plot is taken by applying the input value of 1μA at Y terminal of one EXCCII block, and 0μA at the Y terminal of other EXCCII block for different gains and corresponding resistance values are shown in the plot. The differential gain is plotted for output stage gains of 1, 2, 5 and 10 by varying the value of resistance R_6 in Fig 13.

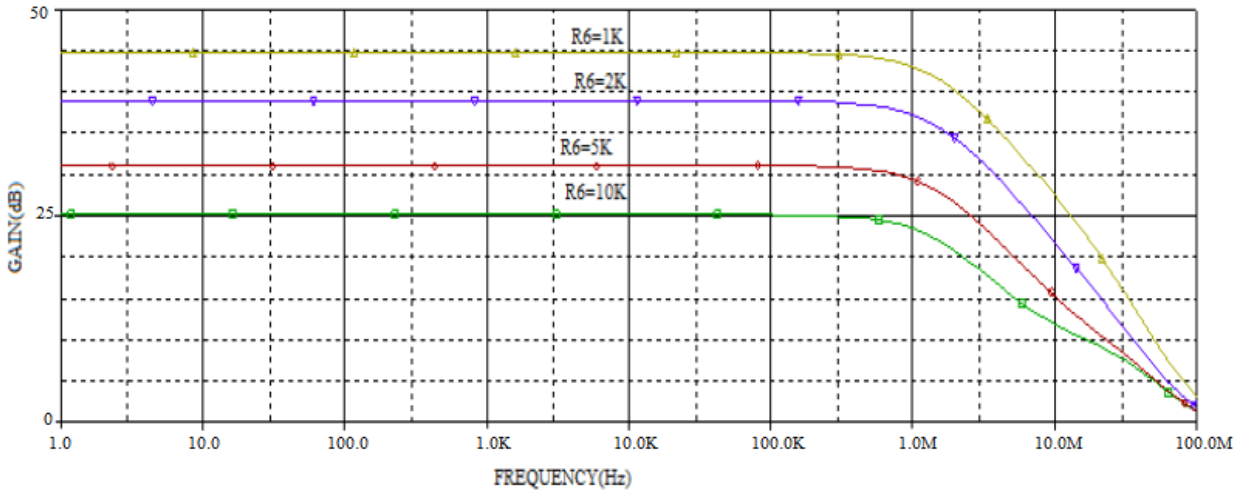

Fig 13. The differential gain plot for a proposed circuit with improved CMRR

The differential gain increases with an increase in the output stage gain, and the input stage gain is fixed at $R_1/R_2 = 10$.

4.2.2 CMRR plot for a proposed circuit with improved CMRR

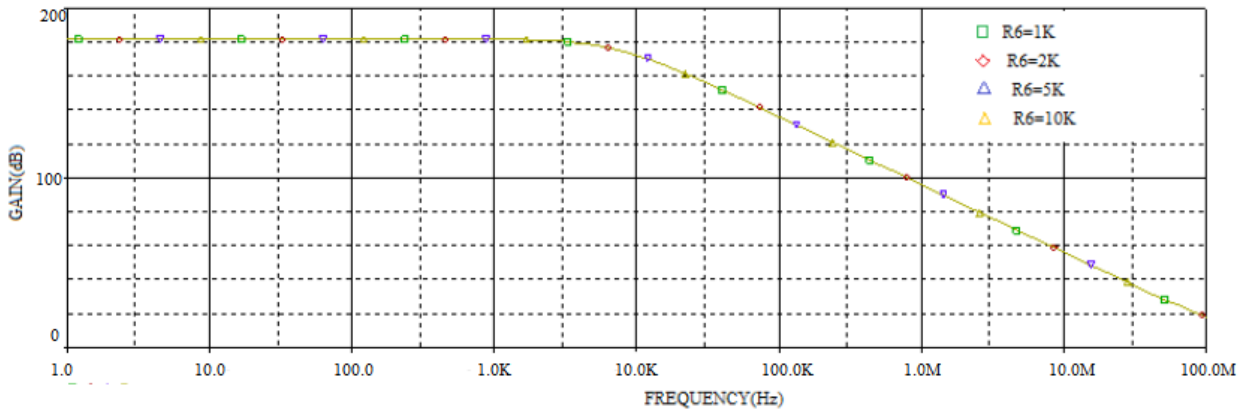

Fig 14. CMRR plot for a proposed circuit with improved CMRR

The CMRR is plotted for output stage gains of 1, 2, 5 and 10 by varying the value of resistance R6 and the input stage gain is fixed at $R_1/R_2 = 10$ in Fig 14. The input stage gain is kept the same for both the input blocks. The common mode gain is taken by applying 1μA current source at the Y terminals of both the EXCCII blocks. The CMRR plot for a proposed circuit with improved CMRR is constant, i.e., independent of the output stage gain.

4.3 Conclusion

All the values of Differential gain and CMRR are shown in the Table 3 along with bandwidth and components used. The value of CMRR is approximately 181 dB which is pretty high as compared to other instrumentation amplifiers.

The comparison Table 2 shows the different blocks used to implement the instrumentation amplifier and the CMRR associated with them also it shows the number of resistors used. Amongst them, the proposed circuit with improved CMRR has highest CMRR. Although the bandwidth is less for the both the proposed circuits 4.55 kHz and 7.001 kHz with improvement, but it exhibits higher CMRR.

Table 2: Comparative study of instrumentation amplifier circuits

Ref. no.	Type of input	Type of output	Active elements Used	Resistors used	CMRR (in dB)
[13]	Current	Current	3 OFCCs	6	55
[13]	Current	Current	4 OFCCs	7	85
[16]	Current	Current	Current mirror	Nil	91
[17]	Current	Current	1 CFOA	4	48
[37]	Current	Current	2 CCIIs	1	95
[38]	Current	Current	2 OFCCs	3	76
[39]	Current	Current	2 CCIIs and 2 Op-amps	1	55
[40]	Current	Current	5 OTAs	1	95
[41]	Current	Current	3 OTRAs	5	64.5

Proposed	Current	Current	3 EXCCII	6	95.54
Proposed with improved CMRR	Current	Current	3 EXCCII	5	181.64

Table 3. Parameters of the proposed circuit and proposed circuit with improved CMRR

Input Value (μA)	Resistor Value (in kΩ)		Differential mode gain (in dB)		Differential gain bandwidth (in MHz)	CMRR (in dB)		CMRR bandwidth (in kHz)	
	Fixed Resistors	Variable Resistor	Proposed	Proposed with improved CMRR		Proposed	Proposed with improved CMRR	Proposed	Proposed with improved CMRR
1	$R_1=R_3=R_5=10$; $R_2=R_4=1$	$R_6 = 1$	39.119	44.73	1.447	95.540	181.646	7.001	4.55
		$R_6 = 2$	33.307	38.924	1.459	95.540	181.646	7.001	4.55
		$R_6 = 5$	24.475	31.091	1.449	95.540	181.646	7.001	4.55
		$R_6 = 10$	19.493	25.109	1.498	95.540	181.646	7.001	4.55

This work presents the study of a new building block, i.e., Extra – X Second Generation Current Conveyor (EXCCII). Moreover, proposes two current-mode instrumentation amplifier topologies. The secondly proposed topology has improved CMRR. The circuit exhibits high CMRR as compared to existing CM instrumentation amplifiers in the literature. Since CMRR is a valid and reasonable parameter for the comparison of any circuit, we have worked on improving the CMRR, although we get a low bandwidth. The proposed circuit can also be tested experimentally and by simulation by another implementation of EXCCII using AD844 as given in [7].

4.4 Future Scope

Since the bandwidth of the proposed circuit is low, the bandwidth can be improved in the future by using bandwidth enhancement techniques. Also, the voltage to current Instrumentation Amplifier can be developed using this block.

CHAPTER 5

5.1 Oscillators

Oscillators are an important class of circuits and finds many applications in communication, instrumentation, measurement, and control systems. Oscillation is an effect that frequently repeated and regularly fluctuates about the mean value and the Oscillator is a circuit that produces oscillation The electrical oscillations whose amplitude remains constant with time are called undamped oscillations. Oscillators are used to generate signals, for example used as a local oscillator to transform the RF signals to IF signals in a receiver, used to generate RF carrier in a transmitter, as sweep circuits in TV sets and CRO, used to generate clocks in digital systems. Op amp oscillators are restricted to the lower end of the frequency spectrum because op amps do not have the required bandwidth to achieve low phase shift at high frequencies. Voltage-feedback op amps are limited to low kHz range since their dominant, open loop pole may be as low as 10 Hz. The new current-feedback op-amps have a much wider bandwidth, but they are inflexible to use in oscillator circuits because they are sensitive to feedback capacitance. Oscillators are useful for creating uniform signals that are used as a reference in applications such as audio, function generators, digital systems, and communication systems. For these applications low value of total harmonic distortion (THD) is an crucial requirement as higher harmonics have detrimental effects on electrical equipment. These higher order harmonics can also interfere with communication transmission lines since they oscillate at the same frequencies as the transmit frequency. If left unchecked, increased temperature and interference can greatly reduce the life of electronic equipment and cause damage to power systems.

5.2 Multi phase sinusoidal oscillator

Sinusoidal oscillators can be classified based on generated output such as single, quadrature and multiphase. Particularly multi phase sinusoidal oscillators finds many applications in the field of control, communication systems. Multiphase oscillators are capable of producing multiple signals that are equally separated in phase, used as an essential functional

block in many communication networks, power electronics, measurement and instrumentation systems. The examples of commonly used multiphase oscillator circuits included control schemes for 5-φ induction motor drives [18] and decoupled dynamic control of a six-phase two-motor drive system. This literature has numerous realizations of such oscillators. Whereas some earlier systems are complex circuitry, contemporary multiphase oscillating systems have relatively simpler structures presented in [18,19]. The latter systems have generally utilized first-order low-pass sections to produce the necessary phase shifts. Such networks have a gain that rolls off beyond the corner frequency with produce phase shifts of up to 90º. Three phase sinewave oscillators are used as references for modern ac power converters [20,21]. The oscillator is employed for frequency control in cyclometer converters, for phase control, and for determining the whole switching sequence of the converter [18], [19]. Among the different versions of current conveyors, why the second-generation current conveyor (CCII) used is discussed above in the introduction part. Oscillators using CCII and exhibiting resistor-less realizations are reported in the literature.

5.2.1 Literature survey

The oscillator circuits presented in [22]–[25] exhibit good performance, they suffer from the use of large number of active and passive components and complex structure. The simple structure operational transconductance amplifier based realization [26] enjoys electronic tunability but suffers from limited output voltage swing and temperature sensitivity. Although the active-R realization [27], [28] are a simple structure, it lacks the electronic tunability. The basic second-generation current-conveyor based structures [29], [30] use a single current conveyor per phase. However, to achieve electronic tunability a junction field-effect transistor (JFET) and three current-conveyors are required for each phase. The current feedback operational amplifier-based realization [31] is simple. It exploits the internal pole of the amplifier to advantage and can operate at relatively high frequencies. However, this requires a current feedback operational amplifier with accessible compensation terminal. Thus its application is limited to current feedback operational amplifiers (AD844) which is no more than a second-generation current conveyor and a buffer on the same chip. Moreover, while electronic tunability is feasible, each phase requires the simulation of a dc supply-dependent capacitor using the

internal pole of a voltage feedback operational amplifier. The current follower based structure [32] requires two current followers, one floating resistor, one floating capacitor for each phase, and does not enjoy electronic tunability. Finally, most of these circuits can realize either odd or even-phase signals [22]–[32]. The circuit present in [33] exploited the parasitic resistance of the current conveyors which make electronic tunability possible through the bias current. So, in [34] only grounded passive components used. In the field of multiphase oscillator design, these circuits offer varied desirable functionalities like current-mode outputs, quadrature outputs, multiphase outputs, etc. Other features for such circuits are the condition of oscillation and frequency of oscillation, low component count and the use of grounded passive components from the viewpoint of monolithic integration. In 2011 Parveen Beg, Mohd. Samar Ansari and M.A. Siddiqi presented the paper on mixed mode 3-phase oscillator using DXCCII [35] have the advantage of CMOS compatible It has the complexity of CMOS structure and the circuit would require two voltage followers (one of them with two outputs) and one current follower. Now, a lot of circuit complexity of DXCCII with buffered output becomes redundant for realizing the goal.

A simpler approach would only demand an extra-*X* stage, resulting in a new active element, named EX-CCII (with buffered output), introduced in [7]. and therefore opens up avenues for simpler circuits [35,36]. Now, recently reported building block the Extra-X Current Conveyor (EXCCII), its device characteristics and its CMOS implementation was discussed in chapter 2. Mixed-mode, three phase sinusoidal oscillator using three EXCCIIs, two grounded resistors and three grounded capacitors. The proposed circuit enjoys independent control of the frequency of oscillation. And verified with PSPICE using 0.25µm CMOS technology simulation results are.a lso presented.

5.3 PROPOSED CIRCUIT

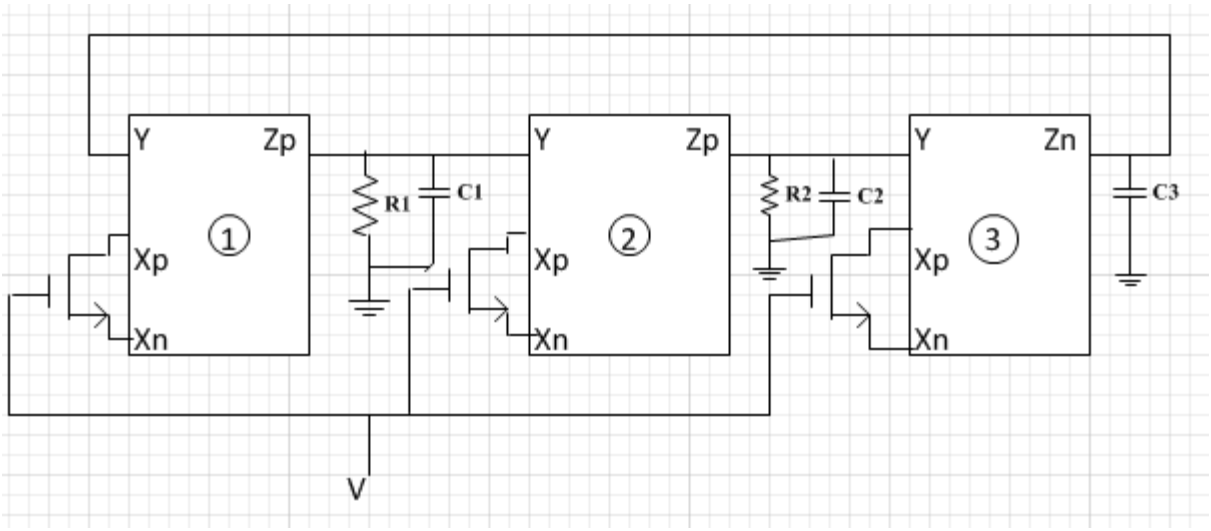

Fig 15: Proposed Mixed mode 3-phase oscillator using EXCCII

The design of mixed mode three-phase sinusoidal oscillator (MTSO) is presented. The basic building blocks for the MTSO are an inverting lossless integrator and two lossy integrators. Each of these sections is realized using a single EXCCII, grounded resistor, grounded capacitors and a MOSFET biased in the triode region acting as a resistor. The transconductance (g_m) value for MOSFET operated in triode region is

$$g_m = 2\mu_n c_{ox}\left(\frac{w}{L}\right)_i \left(V_{Gi} - V_{Ti}\right) \qquad i = 1,2,3 \tag{34}$$

The characteristic equation for the third order oscillator show in fig.15 is given by

$$s^3 + s^2\left(\frac{1}{R_2C_2} + \frac{1}{R_1C_1}\right) + s\left(\frac{1}{R_1C_1R_2C_2}\right) + \frac{8g_{m1}g_{m2}g_{m3}}{C_1C_2C_3} = 0 \tag{35}$$

From the above equation, by putting S= jω and solve for ω which is the frequency of oscillations (FO) and condition of oscillations (CO) is given by

$$\text{The frequency of oscillations } (\omega) = \frac{1}{\sqrt{R_1C_1R_2C_2}} \tag{36}$$

$$\text{Condition for oscillations (CO)} \Rightarrow 8 g_{m1} g_{m2} g_{m3} R_1 R_2 = \frac{R_1 C_1 C_3 + R_2 C_2 C_3}{R_1 R_2 C_1 C_2} \quad (37)$$

If assume all resistor values are equal i.e $R_1 = R_2 = R_3$ and capacitors $C_1 = C_2 = C_3$. Then above two expressions simplifies to

$$\text{The frequencycillations } (\omega) = \frac{1}{RC} \quad (38)$$

$$\text{Condition for oscillations} \Rightarrow R = \sqrt[3]{\frac{1}{g_{m1} g_{m2} g_{m3}}} \quad (39)$$

The inverted lossy integrator provides 3Π/2 phase shift and two lossy integrators provide Π/2 Phaseshift each. The feedback loop gives 2Π, which is in compliance with the standard barkhausen criterion for sustained oscillations.

5.4 Simulation results

The proposed mixed-mode sinusoidal oscillator was verified using the PSPICE simulation. Simulations were conceded out using 0.25μm TSMC device model parameters. The circuit was simulated using V_{DD} = -V_{SS} = 1.25 V and the aspect ratios of the triode MOSFETs (M1 to M3) are W_1/L_1= W_2/L_2 = W_3/L_3 = 1.25μm/0.25μm and the gate voltages were kept at 1.1 V. The values of the passive elements were kept as C1 = C2 = 50 pF and R1 = R2 = 500Ω. The frequency of oscillation obtained in PSPICE simulations is found to be 6.2 MHz shown in fig 18, which is very close to the designed value of 6.32 MHz and the obtained three-phase voltage and current waveforms are shown in Fig 16 and 17 respectively.

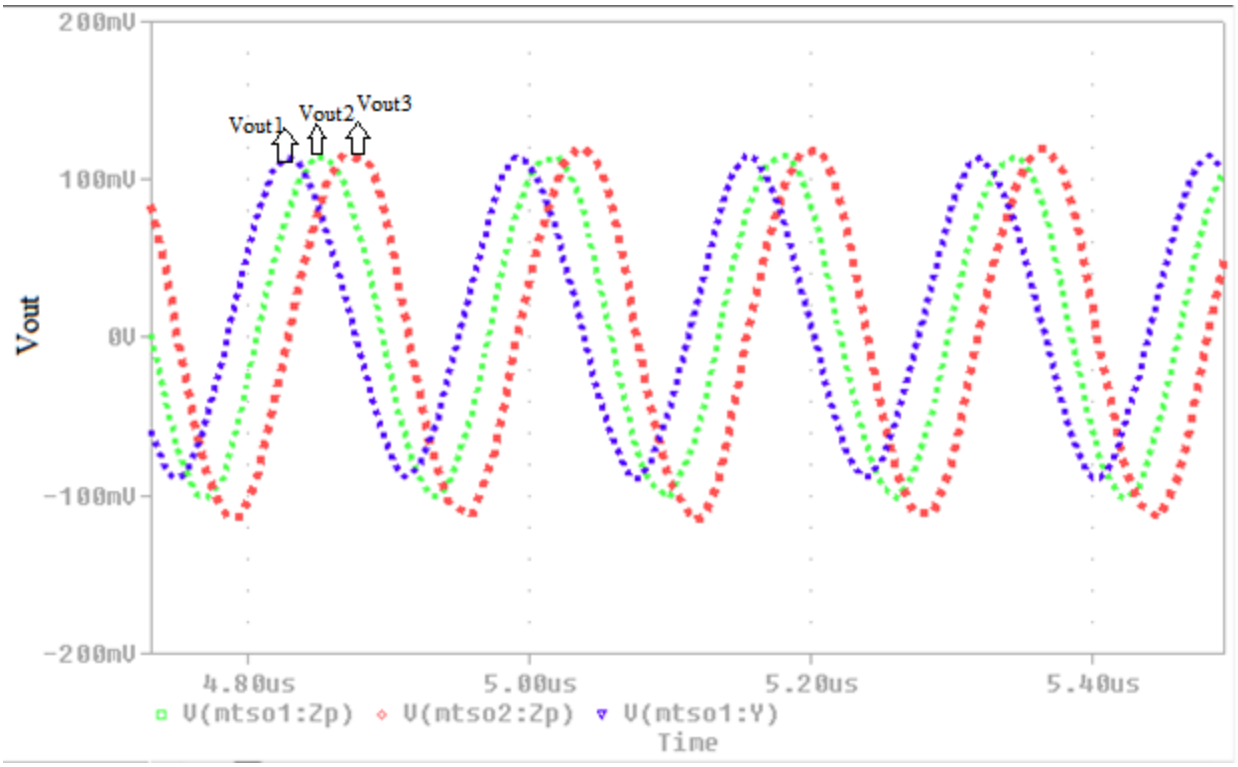

Fig 16: Three phase voltage outputs

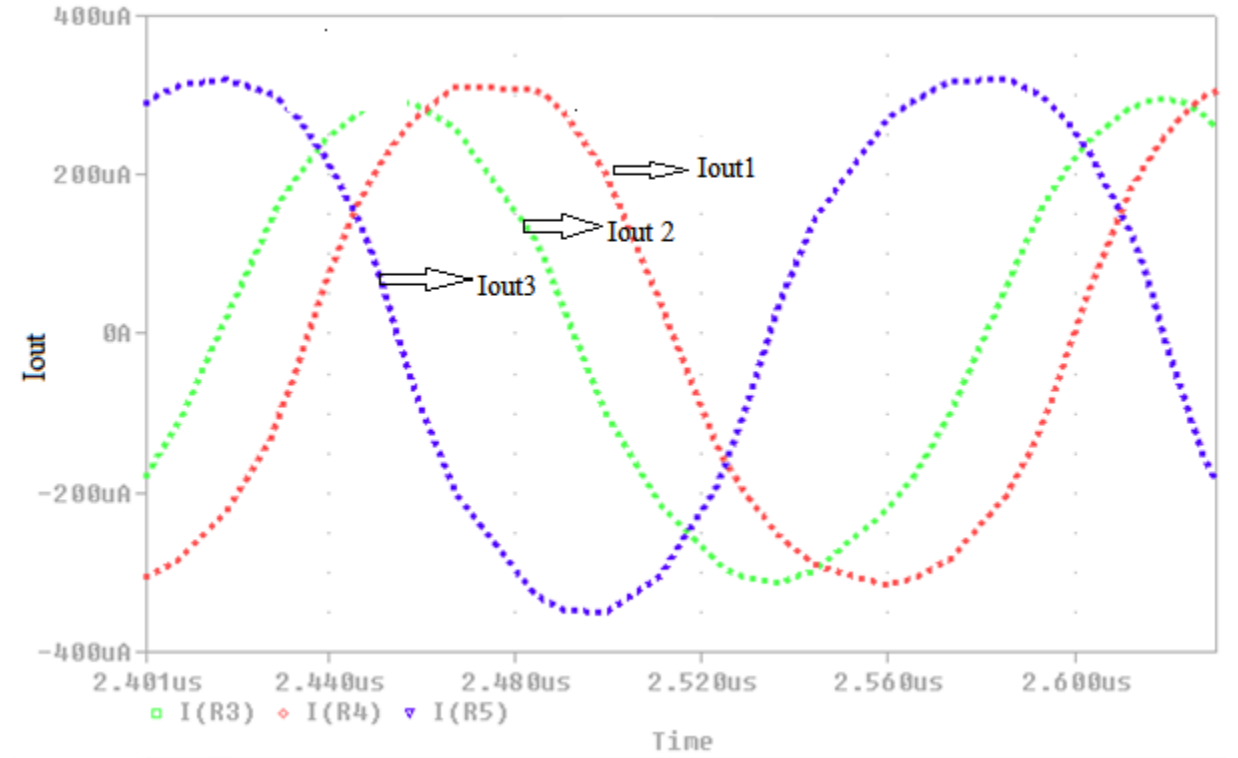

Fig 17: Three phase current outputs

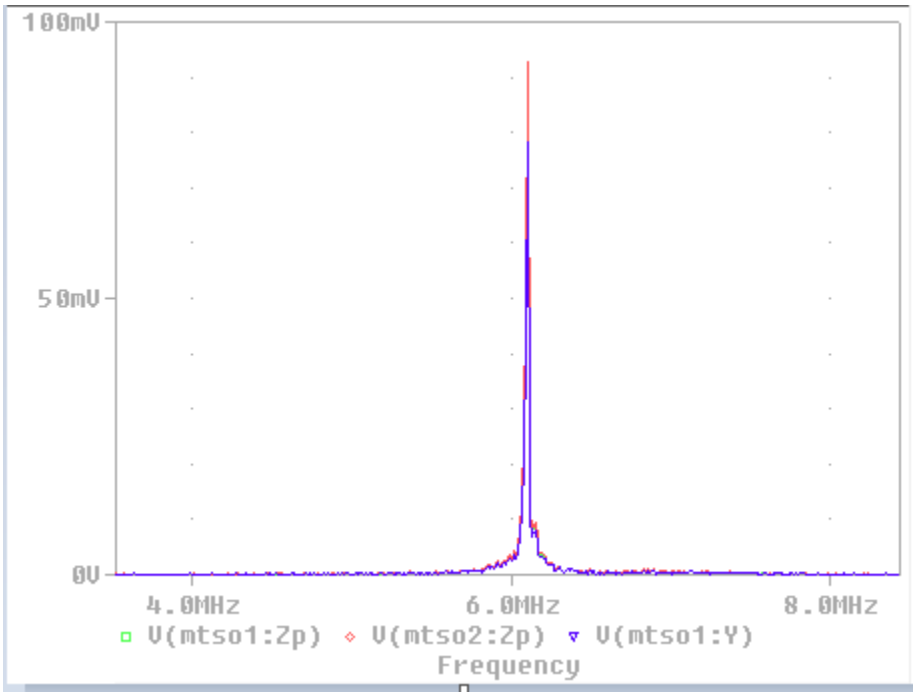

Fig 18: FFT spectrum

5.5 Conclusion

A new mixed-mode three-phase sinusoidal oscillator employing three EXCCIIs, two resistors and three capacitors and three MOSFET's are presented. The circuit is CMOS compatible and suitable for monolithic implementation by use of all grounded passive elements. Other attractive features are low sensitivities of the frequency of oscillation with respect to the passive elements and independent control of the FO and CO. The generated three-phase voltage and current waveforms exhibited low harmonic distortion.

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