ABSTRACT

Designing ADC is a new challenge these days owing to the rapid growth of digital technology. Digital signals impart several inherent advantages and are most preferred these days than their analog counterpart. The conversion of analog signal to digital signal is done by ADC. Flash ADC is fastest of all other ADCs and is used for high speed purposes. Comparator is the main building block of ADC. Dynamic comparators provide high speed, low power dissipation and are more area efficient as compared to pre-amplifier comparators.

In this thesis, comparison of flash ADC using different dynamic comparators with and without adiabatic logic is done. The circuits are simulated using SymicaDE and LTspice software at 90nm PTM model. It has been concluded that power dissipation can be reduced to great extent by using adiabatic logic without much affecting the propagating delay.

CHAPTER 1: INTRODUCTION

These days, the increases demand of portable electronic devices has led to the requirement of very high speed and low power consuming devices which is a challenge as the technology node is advancing. In nature, only analog signals exist but the processing of analog signals is very difficult and hence is operated directly only for limited applications. Moreover, not only the effect of noise is prominent on analog signals but also they are less secured as compared to their digital counterpart. Therefore, to improve the overall performance of the system, analog signals should be converted into digital signals for most of the processing. For any digital device, ADC is the primary requirement.

Both pre-amplifier and comparator play a significant role in the performance of a flash ADC. Several enhancements are reported in the literature for these components recently. These include dynamic latch comparator with inverter buffer [1], comparator with high accuracy switched-capacitors [2], low power preamplifier latch based comparator [3]. The main disadvantages of inter-stage amplifier are its less speed and constant power dissipation. Dynamic comparators with adiabatic logic have overcome this problem. The idea of dynamic comparator is to increase the speed of latch by increasing the intermediate voltage. Because of dynamic comparators, it has become possible to design low power consuming and high speed flash ADC.

1.1 MOTIVATION

As technology is scaling down, the requirement of low voltage supply is also increasing. It is challenging to design an ADC at such a low supply voltage. Comparator plays a major role in the designing of an ADC. A flash ADC using dynamic comparator can be designed at low supply voltages. Power, speed and accuracy are the major features of an ADC. A flash ADC using dynamic comparator with adiabatic logic will also reduce the power dissipation.

Clocked regenerative comparators have improved the speed of ADC because of fast decision making with the help of regenerative latch. The main idea of adiabatic logic is that if a slowly increasing voltage across RC will dissipate less power than immediate increasing voltage. So an adiabatic logic can be applied with dynamic comparator for fast and less power consuming circuit.

1.2 LITERATURE REVIEW

Design and implementation of different comparators is reported recently [10]. The implementation of comparator using CMOS technology imparts high speed, low noise and low power dissipation [11]. To further increase the speed of a CMOS comparator, a latching comparator using dynamic topology has been designed [12]. The conventional CMOS comparator has been extremely successful in the industries. The lower limit of power dissipation for these devices is $C_L V_{DD}^2/2$ which is limited by the power supply voltage V_{DD}. Adiabatic switching circuits push the power dissipation below this limit. Reduction of power dissipation occurs at the cost of slow speed. The basic principle of adiabatic logic is the recycling of energy so that the total energy consumed from the source is reduced [17]. The main disadvantages of inter-stage amplifier are its less speed and constant power dissipation. Different methods for designing adiabatic logics i.e. CMOS adiabatic circuits is also reported in the literature [18]. Design and analysis of double tail comparator using adiabatic logic for high speed applications has also been proposed [22]. In this thesis, simulation and analysis of flash ADC using different dynamic comparators with and without adiabatic logic has been done.

1.3 ORGANISATION OF THESIS

This thesis has been organised as follow: Chapter1 has described the importance of comparator in an ADC and the work which has already been done to improve the performance of comparator and the need of dynamic comparator. Chapter2 has described different types of analog to digital converters, their comparison and their static and dynamic characteristics. Chapter3 has described static and dynamic characteristics of the comparator and has described various dynamic comparators. Chapter 4 is describing the logic of adiabatic circuits and how its work and in which circuits it can be applied. Chapter 5 represents the simulation and analysis of power dissipation, propagation delay and frequency of flash ADC using different dynamic comparators. Chapter 6 contains the conclusion and future scope of this work.

CHAPTER 2: ANALOG TO DIGITAL CONVERTER

2.1 INTRODUCTION TO ANALOG TO DIGITAL CONVERTER

Due to its simpler analysis, processing and storage, digital signal has become popular. According to Moore's Law, the number of transistors per square inch on integrated circuits had doubled every year resulting in a significant decrease in transistor size with a much higher speed. Over the years, the technology gap between the analog and its digital counterpart has been increasing continuously. Though the digital systems have gained immense popularity due to their high speed, efficient processing and noise immunity, most of the real world signals are analog in nature. Also, the processes like amplification, tuning and different modulation schemes are operated on analog signals. Analog interface circuits, thus is a prime factor in an electronic system. Therefore, there is the necessity of merging the merit of digital systems with the analog system which is performed by analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). These converters provide interface between the analog and digital subsystems and their performance plays a critical role in determining the performance of the complete system. Designing of high speed converters with low power consumption in a small chip area is a new challenge these days.

Fig. 1 shows the basic block diagram of an analog-to-digital converter. An analog signal generally after amplification is fed to the input of the ADC. It converts the analog signal into the digital signal which is then used for further processing. On the basis various performance parameters, ADCs can be classified into different types [4].

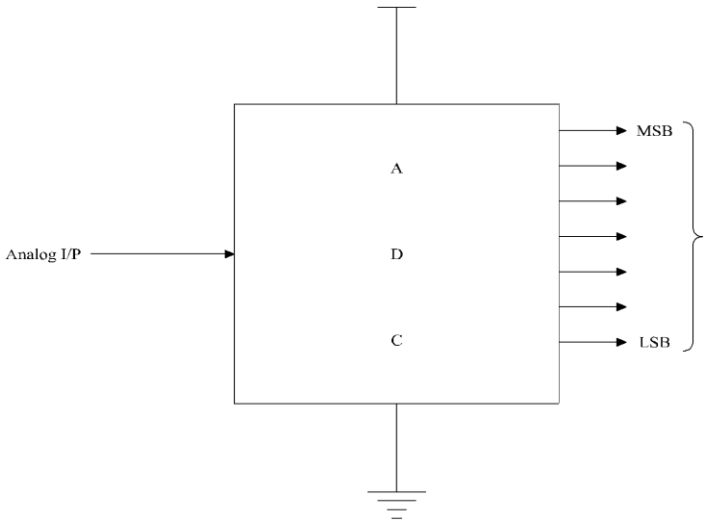

Figure 1: Block diagram of analog to digital converter

There are different types of ADCs are as follows:

- Successive Approximation Register (SAR) ADC
- Dual slope type ADC
- Pipeline ADC
- Sigma delta ADC
- Flash ADC

In this chapter, various analog-to-digital converter architectures are discussed.

2.1.1 SUCCESSIVE APPROXIMATION REGISTER ADC

Successive approximation register (SAR) analog-to-digital converters (ADCs) are usually used in moderate to high resolution and low sampling rate applications. The resolution of SAR ADC is in the range of 8 to 16 bits as pipeline ADC and it also offers low power consumption. Because of its low power consumption, it is used in low power applications such as portable/battery powered devices, data acquisition systems, pen digitizers and industrial controls. For an N bit SAR ADC, N number of comparisons is required for the complete conversion as compared to flash type ADC which requires 2^{N-1} comparisons. Therefore, in SAR ADC, the power consumption can be reduced by a large amount [5].

Fig. 2 shows the block diagram of SAR ADC. The SAR architecture mainly use the binary search algorithm. The SAR ADC consists of fewer blocks such as one DAC (Digital to Analog Converter), one comparator and one control logic known as SAR. At the start, the input of the shift register is applied with logic high. The logic one is shifted to the right position by one bit for each bit conversion. Initially, B_{N-1} is logic high i.e. one and the rest of the bits are zeroes. In the same manner, SAR bit D_{N-1} is initially set to one and rest of the bits are set to zeroes. DAC output which is controlled by the SAR output is set to $V_{REF}/2$. If the analog input is less than $V_{REF}/2$, the comparator resets D_{N-1} to logic low ("0"). If analog input voltage is greater than $V_{REF}/2$, D_{N-1} remains in logic high. The logic high which is enforced to shift register is shifted by one position in the next clock as a result D_{N-2} is set to logic high and rest of the bits are zeroes. The output of DAC is either $3V_{REF}/4$ (D_{N-1}=1) or $V_{REF}/4$ (D_{N-1}=0). The DAC output is compared with analog input. If output of DAC is less than analog input, D_{N-2} remains high otherwise it is set to low. The process is goes further until the output of the DAC converges.

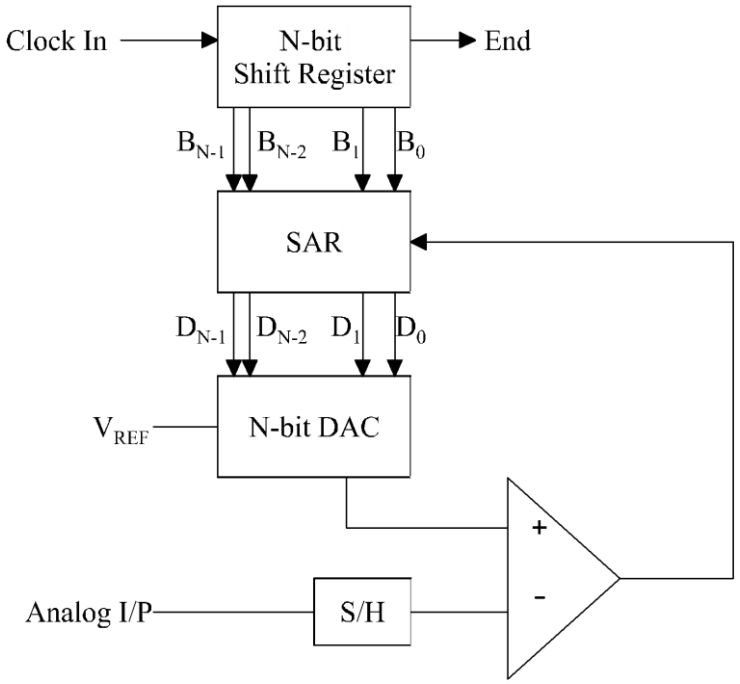

Figure 2: Block Diagram of SAR ADC

2.1.2 DUAL SLOPE ADC

Dual slope ADCs are also called Integrating ADCs. They comprise of an integrator, a comparator and a counter [6]. The basic block diagram of dual slope ADC is shown in Fig.3

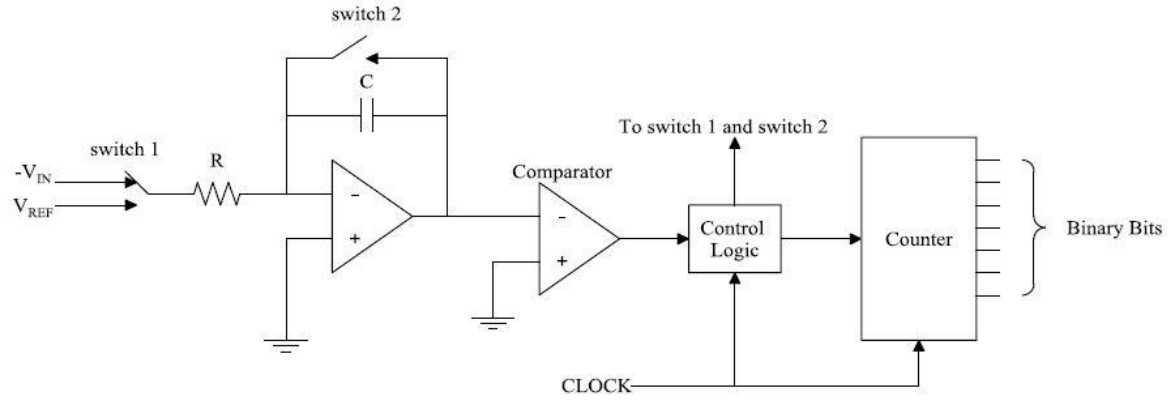

Figure 3: Block diagram of Dual slope ADC

The operation is based on the principle that firstly the unknown voltage i.e. the analog input is integrated for a known or fixed time and then it is equated with the known voltage i.e. reference voltage which is integrated for the time which is to be determined. Here, the opamp works as an integrator which can be used to generate a reference ramp signal that will compare it with input signal by a comparator. The integration of input voltage (V_{IN}) for a fixed time interval which is the highest count in the internal counter. When the counter counts

to its maximum, the system reset the counter and opposite polarity applies to the integrator input (V_{REF}). When opposite polarity reference signal is integrated the counter counts until the output becomes zero. At this instance, the counter stops and the integrator is reset. Charge stored in the capacitor during integrating interval must be equal to the charge which is lost during the de-integrating interval. Therefore, the digital output is directly proportional to the ratio of time durations ($T_{INT}/_{TDE-INT}$). The timing diagram of dual slope ADC has been shown in Fig.4 Output of the ADC is governed by the Eq.1.

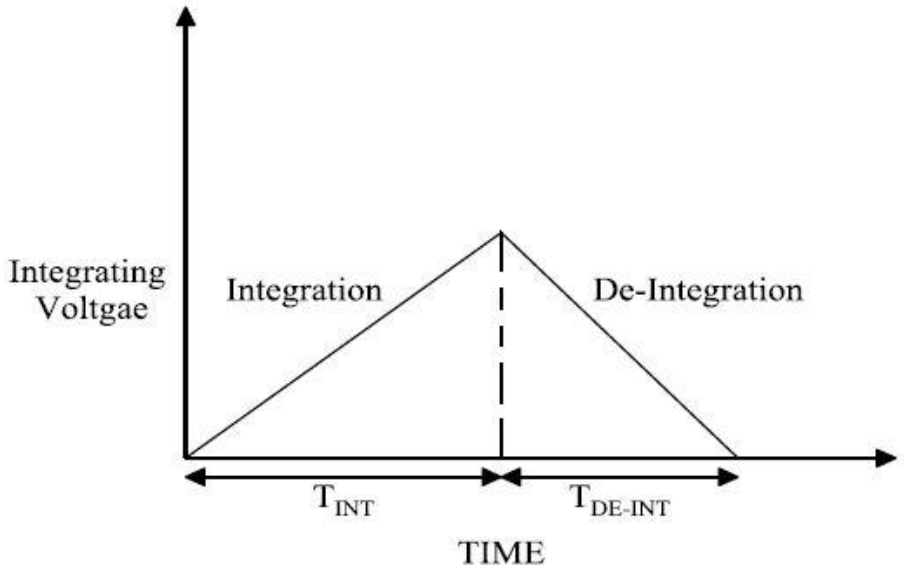

Figure 4: Timing diagram of dual slope ADC

These converters are commonly used in high accuracy applications and have good noise immunity. Unlike all other topologies, flash and dual slope topologies do not require digital to analog converters which reduces the design complexity. These ADCs are suitable for low bandwidth input signals only and which is the major demerit of dual slope ADC.

$$\frac{V_{IN}}{V_{REF}} = \frac{T_{INT}}{T_{DE-INT}} \quad (1)$$

2.1.3 PIPELINE ADC

Pipeline ADC is the one of the widely used ADC architectures. The exponential increase in the number of comparators with the resolution is the major drawback of flash type ADC. In pipeline ADC the circuit complexity increases linearly with the resolution due to which it can be used from 8 bits to 16 bits resolution. Also, it works up to hundreds of mega samples. Due to its moderate sampling rate and high resolution, it is commonly used in communication and

medical applications such as, digital video (HDTV), fast Ethernet, CCD imaging, digital receiver, cable modem and ultrasonic medical imaging. Pipeline ADCs due to their good time and frequency domain performance, are widely used in data acquisition systems[7].

The basic diagram of pipelined ADC has been shown in Fig.5. The pipeline ADC is consisted N stages of connected in series comparator networks where N is the number of bits [6]. Each network consists of a comparator, an amplifier and a sample and hold circuit with a voltage gain of two. The applied analog signal is first sampled and is compared with the voltage equal to VREF/2 where VREF is the reference voltage. The output of each comparator generates a binary bit. If the input analog voltage is less than VREF, the signal is transferred to the amplifier where is it amplified and fed to the next stage and the comparator output is logic low. However, if the input is larger than VREF/2, the comparator output is logic one and VREF/2 is subtracted from the incoming voltage signal and is fed it to the amplifier. As the signal is transmitted serially, the total time taken for the analog to digital conversion is the time of N number of clock cycles. The disadvantage of pipeline ADC is that the decreased circuit complexity and power consumption comes at the cost of higher conversion time. Also, the small error in a prior stage transmits through the converter and a large error results at the end of conversion. Another drawback of pipeline ADCs is the latency and hence they are not used in the applications where latency is critical and flash ADCs are used instead.

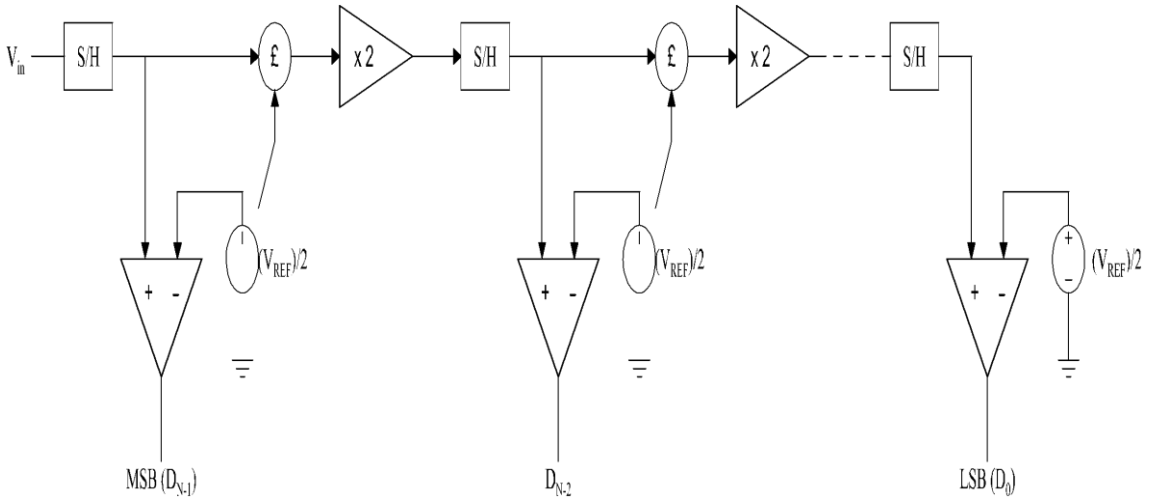

Figure 5: Basic diagram of pipeline ADC

2.1.4 SIGMA DELTA ADC

Sigma delta ADC is immensely used in industries where requirement is better accuracy. The three main advantages of sigma delta ADC:

- High performance conversion with low cost
- Digital Signal Processor (DSP) compatibility for system integration
- Integrated digital filter

Sigma-Delta analog-to-digital converters can be used where high accuracy and high precision is required. This ADC comprises a comparator, an integrating circuit and Digital Filter [6]. Also, 1-bit digital-to-analog converter is used which acts as a switch. Sigma-delta ADC functions on the principle of over sampling ratio at margin and highly accurate conversions is performed. The basic diagram has been shown in Fig.6

The functioning of a converter is understood by the application of a low frequency signal at the input. The digital-to-analog converter samples and quantizes the input at high sampling rate. The comparator compares the output and which is then passed onto the decimation filter where the sampling rate and noise components are reduced. Due to this the overall accuracy and the resolution is increased. The accuracy of the converter can be enhanced by the use of the reference circuitry and over-sampled clocking mechanism. Sigma-delta ADC has the advantage of better noise performance as compared to flash ADC as the resistors used in the later are susceptible to noise. Owing to its noise shaping capability, sigma delta ADC finds use in low bandwidth and high resolution applications.

On contrary, the major demerit of sigma delta ADC is its very low speed as this topology is the slowest of all other ADC topologies. The reason being, the oversampling mechanism actually converts the input signal to take quite a few clock cycles to perform. Also, design of the decimation filter is complex and so is a challenge which comes as the other bottleneck of these converters.

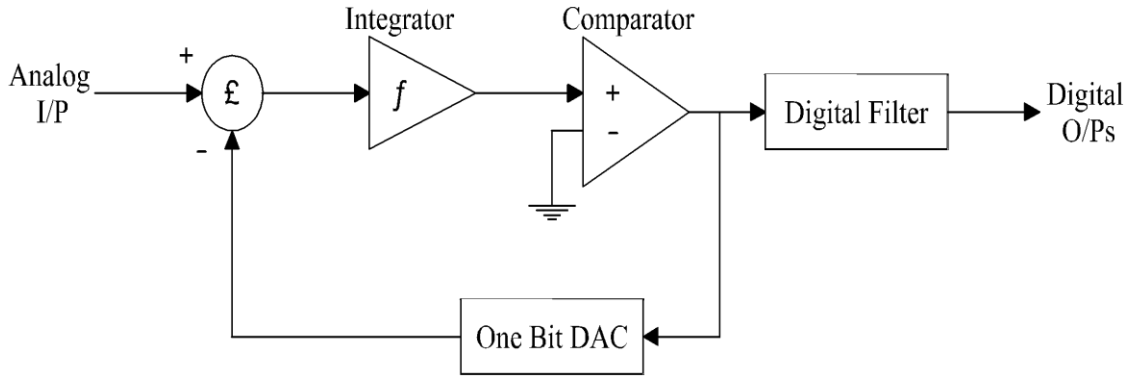

Figure 6: Block Diagram of Sigma delta ADC

2.1.5 FLASH ADC

Flash analog-to-digital converters are also called as parallel ADCs as they utilize parallel architecture. It is the fastest technique to convert an analog signal to a digital signal as the results of the conversion are available in the output at the end of only one clock cycle. Flash ADCs, however, have the demerits of limited resolution of maximum eight bits due to the fact that the number of comparators required depend exponentially on the number of bits i.e. resolution. Further increase in the number of bits increases the power requirement and the cost drastically. Flash ADCs find application in large bandwidth systems such as radar processing, data acquisition, satellite communication, real time oscilloscopes, data communications and high density disk drives. It is also used in various other types of ADCs such as pipeline ADC and sigma delta ADC [5].

Fig.7 shows the block diagram of flash ADC. As shown in figure, for N bit flash ADC, the number of comparators required is 2^N-1. The non-inverting terminal of each comparator is connected to the analog input and the inverting terminal is fed by the reference voltage. The reference voltage of the comparator can be obtained with the help of a resistance divider network known as resistor ladder. For an N bit flash ADC, the number of resistors required is 2^N. The reference voltages can be uniformly spaced by least significant voltage which is resolution and is equal to V_{ref} /2^N. When the input voltage is not more than the reference voltage of comparator it will produces logic low otherwise, the comparator output is logic high. The comparators having the inputs voltages greater than the reference voltages will all produce a string of logic high at the outputs whereas all the other upper comparators will give a string of logic low. This string of consecutive zeroes followed by consecutive ones is also known as thermometer code. In a mercury thermometer, the presence of mercury below a certain temperature and its absence beyond that temperature calls for the name thermometer code. This thermometer code is translated into a binary data with the help of a thermometer to binary code converter which is usually a priority encoder. A priority encoder produces the output which is the binary equivalent of the highest logic high input.

Flash ADC requires comparators large in number when the resolution is increased. For example, an 8 bit flash ADC requires 255 comparators and a 10 bit flash ADC requires 1023 comparators. This exponential increase in the number comparators requires a large area and also the power consumption increases drastically.

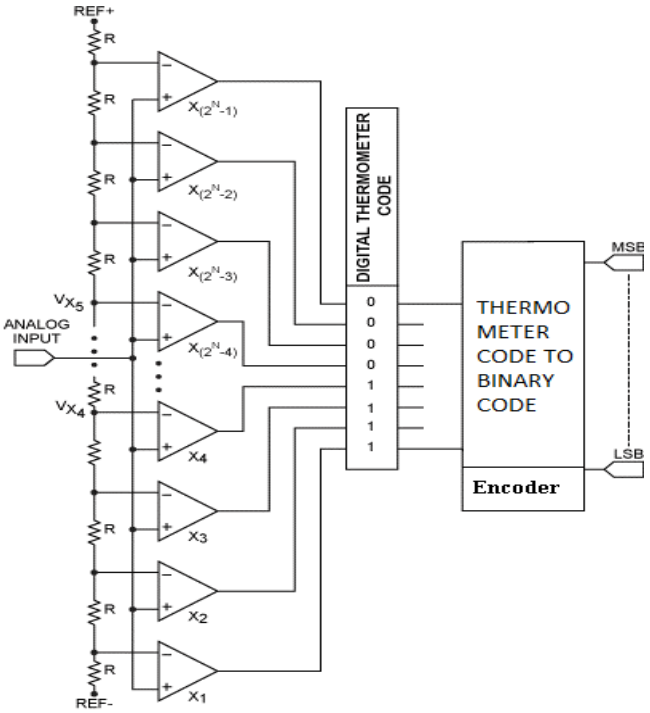

Figure 7: Generic block diagram of flash ADC

2.2 COMPARISON OF ADC TOPOLOGIES

Different ADC topologies have different specifications such as resolution, conversion time, sampling frequency which is based on their conversion and encoding method and are chosen for the specific application accordingly [4]. Table1 gives the comparison of the different types of ADCs.

Architecture of ADC	SAR ADC	Dual slope ADC	Pipeline ADC	Sigma-Delta ADC	Flash ADC
Application	Low speed and moderate resolution	High resolution and low speed	Medium speed and moderate resolution	Medium speed and high resolution	High speed and low resolution
Encoding method	Successive approximation	Analog integration	Digital correction logic	Digital filter	Thermometer to binary code encoder
Conversion method	Binary search algorithm	Voltage to time conversion	Serial conversion	Over sampling technique	Parallel conversion
Conversion time	Increases linearly with	Increases exponentially	Increases linearly with	Depends on noise and	Independent on resolution

	resolution	with resolution	resolution	output data rate	
Optimum Resolution	10-16 bits	16 bits	12-16 bits	14-20 bits	4-8 bits
Sampling frequency	50kHz-500kHz	40kHz-100kHz	10MHz-100MHz	100kHz-500MHz	100MHz-5GHz
Demerit	Anti-aliasing filter needed	Slow conversion rate	Only for low speed application	High order DAC required	High power and large die size needed

Table 1: Comparison of ADC topologies

2.3 ADC CHARACTERISATION PARAMETERS

Analog signals can have any value on the real number axis whereas a digital signal can take only a predefined value. Analog to digital converter transforms the analog signal to a suitable digital output code.

To analyse the performance of the any ADC, various performance parameters have to be discussed. ADC parameters are broadly classified into two categories.

- Static (DC) parameters
- Dynamic (AC) parameters

DC parameters describe static transfer function of the ADC and AC parameters relates with the dynamic performance of the converter [6].

2.3.1 STATIC CHARACTERISTICS

It mainly includes quantization error, conversion speed, offset error, resolution, gain error, integral non linearity and differential non linearity.

2.3.1.1 RESOLUTION

It is defined as the number of bits in the digital output of an ADC. The resolution of an ADC depends on the number of bits that an ADC requires to represent the analog input. The resolution just indicates the number of output bits and does not signify the accuracy of the converter.

Generally, dual slope type and sigma delta ADCs have highest resolution followed by SAR and pipeline ADCs with moderate resolution. Flash ADC has the lowest resolution of all other

ADCs.

2.3.1.2 QUANTIZATION ERROR

The analog signal which can take any value from the set of infinite values has to be converted into digital signal which takes only predefined values. The sampled analog signal is transformed from having continuous levels to discrete levels which is called quantization and is done with the aid of a quantizer. By quantization, the sampled signal gets a definite level. Because the digital signal is confined to definite values, there is always a difference in values of the sampled analog signal and the value assigned to the digital signal. This difference results in an error which is named as the quantization error. This is a truncating error resulting from the deviation between the analog signal and its digital counterpart. Eq.2 represents the formula for calculation of the step size; V_{ref} is the full scale voltage hence $\pm V_{ref}$ i.e. $2V_{ref}$ is the full voltage swing. N represents the number of bits of the output of ADC and Δ is the step size.

$$\Delta = \frac{2V_{ref}}{2^N} \qquad (2)$$

Step size is the smallest value with which the input is quantized or it is the difference between two consecutive values of digital levels. Step size is also the least significant bit or the resolution of a quantizer. Therefore, every assigned value can deviate within ±Δ/2 from an analog input sample which implies that the quantization error is always in the range of -Δ/2 to +Δ/2 volts. Also, Δ/2 is the maximum quantization error for a quantizing a sampled analog input.

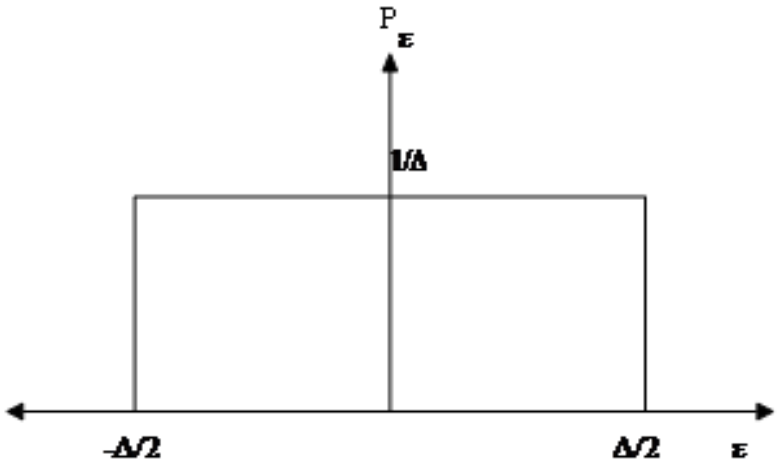

Figure 8: Probability density function of the quantization noise

Since, at each sampling instant, the analog input value is known and so, the quantization error

can be determined. However mathematically, the analog input may take any value with the same probability thus making a uniform probability density function for the quantization error as shown in Fig.8. The mean square value of this quantization error denotes the quantization noise power and shown in Eq.3.

$$\sigma^2 = \int_{-\Delta/2}^{\Delta/2} \mathcal{E}^2 \frac{1}{\Delta}\, d\mathcal{E} = \frac{\Delta^2}{12} \qquad (3)$$

2.3.1.3 OFFSET ERROR

Offset error represents the deviation in the performance of an ADC at zero volts or zero count. Fig.9 shows the offset error of a practical ADC as compared to an ideal ADC. The ideal ADC transits exactly at LSB/2 whereas the practical ADC transits at voltage equivalent to one LSB. This deviation of the practical transition voltage from the ideal transition voltage is the offset error. Offset error is a fixed and can be eliminated by calibration.

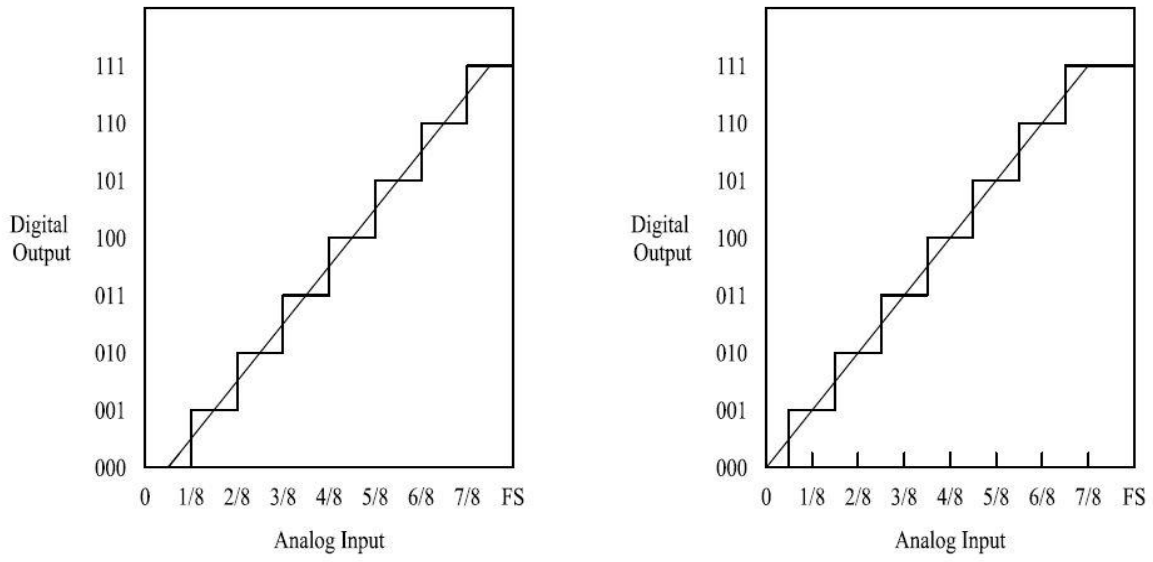

Figure 9: a) Practical ADC with offset b) Ideal ADC characteristics

2.3.1.4 CONVERSION SPEED

Conversion speed has been defined as the quantity of analog data that is converted by an ADC per second. Selection of an ADC is mostly done on the basis of speed requirements for the desired application. Flash ADC is the fastest ADC as it based on parallel conversion.

2.3.2 DYNAMIC CHARACTERSTICS

Dynamic performance of the ADC represents the imperfections caused by random processes like distortion and noise sources and results in performance degradation of the ADC. Distortion is measured done by applying a sine wave to the test system. The analog response is calculated and then evaluated in the frequency domain performance is evaluated and the FFT spectrum is analysed.

2.3.2.1 SIGNAL TO QUANTIZATION RATIO (SQR)

SNR is the ratio of the input signal power and the total quantization noise power. Eq.4 shows the maximum signal power. Eq.5 and Eq.6 shows the calculation of SQNR.

Quantization noise power as calculated in above section is $\Delta^2/12$

Let the analog input signal be Asinωt, then, the input signal power is $A^2/2$

Also, $\Delta = \frac{2A}{2^N}$, therefore

$$Maximum \text{ signal power} = \frac{\left(2^{N-1}\,\Delta\right)^2}{2} \quad (4)$$

$$Peak\ SQNR = \frac{\frac{\left(2^{N-1}\,\Delta\right)^2}{2}}{\frac{\Delta^2}{12}} = 3 \times 2^{2N-1} \quad (5)$$

$$SQNR\ (dB) = 10\ log_{10}\ (3 \times 2^{2N-1}) = 6.02N + 1.76 \quad (6)$$

2.3.2.2 SIGNAL TO NOISE DISTORTION RATIO

Signal to noise and distortion ratio SNDR is SNR with the non-linear distortion components taken into account as well. The distortion produced by higher harmonics is calculated as the root mean square value of the harmonics.

2.3.2.3 EFFECTIVE NUMBER OF BITS

For a given SNDR, the lowest tolerable resolution is termed as the effective number of bits (ENOB)

As calculated in the previous section, SQNR = (6.02 N+1.76) dB, where N is the number of bits of ADC. From this equation substituting SNQR with SNDR we get the expression for ENOB in Eq.7

$$ENOB = \frac{SNDR-1.76}{6.02} \quad (7)$$

ENOB is a used to check the performance of an ADC under noise and distortion conditions for any given input signal.

CHAPTER 3: COMPARATORS

3.1 INTRODUCTION TO COMPARATOR

Comparator is an electronic device which does the comparison between two input analog signals and output gets switched to one of the saturation state indicating which one is greater. Figure 10 is showing the symbol of comparator [8]. Comparator is main building block of an ADC. It is mainly used in open loop configurations which makes it second most widely used device in the electronics after Opamp.

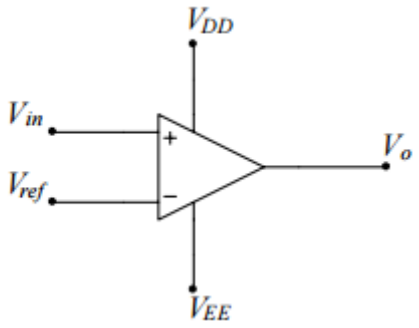

Figure 10: Comparator Symbol

If Vin is greater than Vref, then Vout will be switched to higher saturation state and it indicate binary logic '1'.

If Vref is greater than Vin, then Vout will be switched to lower saturation state and it indicate binary logic '0'.

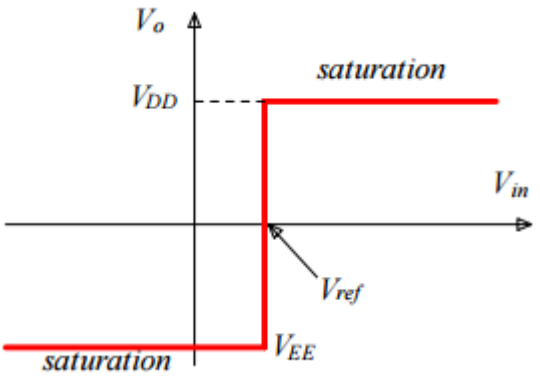

Figure 11: Ideal Characteristics of a comparator

In ideal state, it should not have two values at any point. Figure 11 is showing the ideal characteristics of a comparator [9]. But there is always a transition region between two

saturation states. The transition region should be very small for better performance of the comparator.

3.2 CHARACTERISTICS OF COMPARATOR

3.2.1 STATIC CHARACTERSTICS

It mainly includes gain, offset, input resolution, noise and input common mode range [10].

3.2.1.1 GAIN

Gain of a comparator is defined as ratio of difference of saturation level voltages and range of input voltage. It can be expressed as:

$$\text{Gain (Av)} = \lim_{\Delta V \to 0} \frac{V_{DD} - V_{EE}}{\Delta V} \quad (8)$$

ΔV= range of input voltage

3.2.1.2 OFFSET

The main reason of offset is the mismatch between the transistors [3]. Input offset voltage is applied between the input terminals to balance the amplifier and output offset voltage is applied at the output terminal when both inputs are grounded.

3.2.1.3 INPUT RESOLUTION

It is difference in input signals which is required to make output to go to one of the saturation state.

3.2.1.4 NOISE

During transition region, the effect of noise is maximum as it can lead to output to different saturation state which will cause jitter in the circuit.

3.2.1.5 INPUT COMMON MODE RANGE

This is minimum input voltage which is required for normal functioning of a comparator.

3.2.2 DYNAMIC CHARACTERSTICS

3.2.2.1 PROPAGATION DELAY

It is defined as time difference between response of the comparator and applied input signal. Propagation is calculated by taking average of rising propagation delay time and falling propagation delay time.

3.2.2.2 SPEED

It is reverse of propagation delay. It defines how fast the output switches the saturation state when the input of the comparator changes.

3.3 DIFFERENT TYPES OF COMPARATOR

3.3.1 CONVENTIONAL DYNAMIC COMPARATOR

It is a clock regenerative comparator which makes it widely used in high speed ADC. It makes fast decision due to the internal positive feedback in the regenerative latches [11]. Figure is showing conventional dynamic comparator.

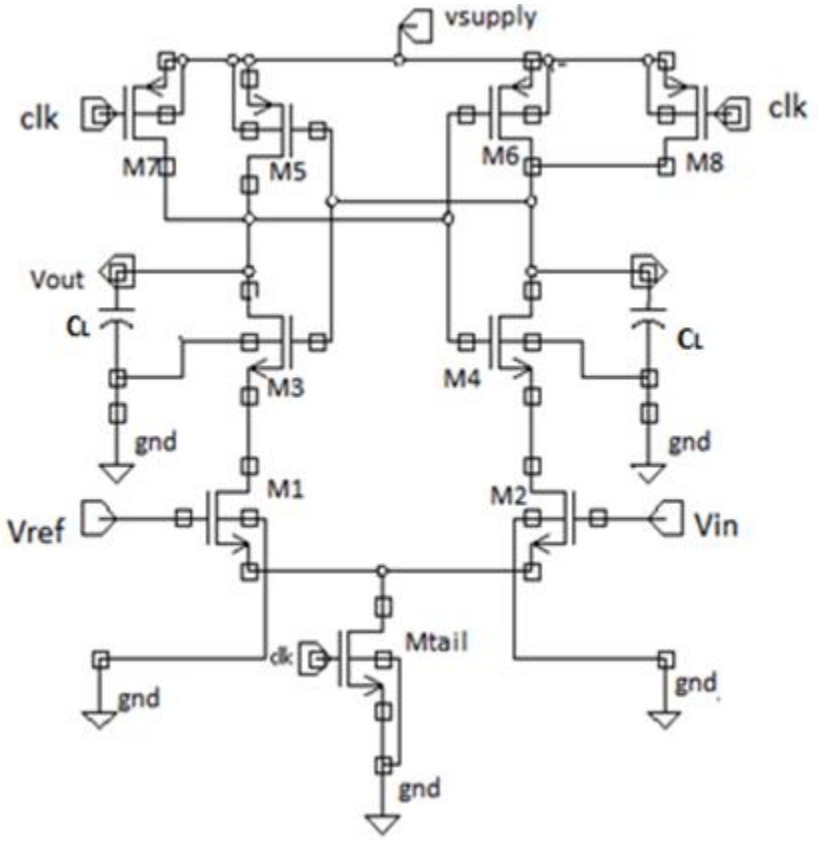

Figure 12: Conventional Dynamic Comparator

WORKING

Dynamic comparator works in two phases, one is reset phase and other is comparison phase. In the reset phase, when clk= ‘0’ and Mtail is off, Transistors M7 and M8 charge load capacitors to

V_{DD} to define a valid logic. In the comparison phase, when clk= 'V_{DD}', Mtail is on and transistors M7 and M8 are off. Both capacitors are pre-charged to V_{DD}, depending upon the input voltage, both capacitors start discharging at different rate. If Vin is greater than Vref, outp will discharge faster than outn and when voltage at outp reaches V_{DD}-Vtp, M5 will on and will start the latch generation caused by back to back inverter. Thus, Vout will charge to V_{DD} which indicate the binary logic '1'. When Vin is less than Vref, Vout will discharge to ground which indicate the binary logic '0'.

The delay of comparator consists of two time delays, t0 and tlatch. The value of t0 represents the discharging of load capacitor until it reaches V_{DD}-Vtp and turns on one of the transistor M5 or M6. I1 and I2 are the discharging current and when Vin is greater than Vref, I2 is greater than I1 which leads to faster discharging of C1 [11]. So, the value of t0 is

$$t_0 = \frac{C_L \left|V_{thp}\right|}{I_2} \cong 2\frac{C_L \left|V_{thp}\right|}{I_{tail}}. \tag{9}$$

The value of tlatch depends on the time, latch takes so that the voltage difference between the values of capacitor is V_{DD}/2. The latch delay is given by

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \tag{10}$$

Where gm,eff is the net trans conductance of latch. The value of ΔV is given by

$$\begin{aligned} \Delta V_0 &= \left|V_{outp}(t = t_0) - V_{outn}(t = t_0)\right| \\ &= \left|V_{thp}\right| - \frac{I_2 t_0}{C_L} = \left|V_{thp}\right| \left(1 - \frac{I_2}{I_1}\right) \end{aligned} \tag{11}$$

The difference between discharging current is very less so I1 can be approximated to Itail/2. So the propagation of the comparator is given by

$$\begin{aligned} t_{delay} &= t_0 + t_{latch} \\ &= 2\frac{C_L \left|V_{thp}\right|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4\left|V_{thp}\right| \Delta V_{in}} \sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \end{aligned} \tag{12}$$

From the equation 12, it can be observed that delay of comparator depends indirectly on the difference of input voltage and directly on the output capacitance.

The advantages of dynamic comparator are its high input impedance, less effect of noise and mismatch on the output and low power dissipation [12]. The parasitic capacitances of the transistors do not effect the switching speed of the output nodes.

The major disadvantage is high stacking between the power supply and ground because of which high power supply is required for proper delay of the comparator.

3.3.2 CONVENTIONAL DOUBLE TAIL COMPARATOR

This comparator has less stacking and can work on low supply voltage as compared to conventional dynamic comparator. It has two tail transistors, Mtail2 because of wider width enables large current in the latching stage which leads to fast latching and other is small Mtail1 which enables small current at the input stage for low offset [11].

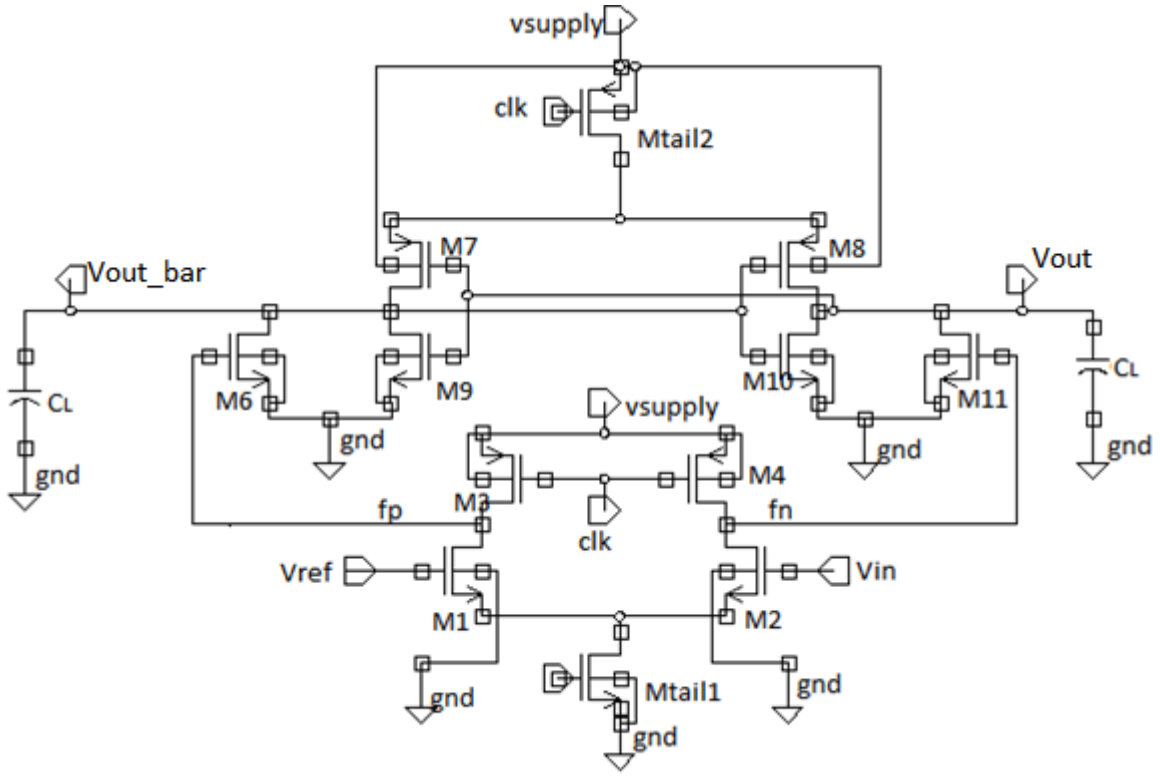

Figure 13: Conventional Double Tail Comparator

WORKING

In the reset phase, when clk= '0' Mtail1 and Mtail2 are off and transistors M3 and M4 are on which will pre-charge the nodes fn and fp to V_{DD}. In the decision making phase, when clk= '1' Mtail1 and Mtail2 are on and M3 and M4 are off which will lead to voltage drop of nodes fn and fp. Because of discharging a differential voltage will be developed. An intermediate stage is

formed by M6 and M11 transistors which will transfer the intermediate voltage to the cross-coupled inverters.

The delay of comparator consists of two time delays, t0 and tlatch. The value of t0 represents the time load capacitor takes to charge to Vthn which will initiate the latch regeneration process, so value of t0 is

$$t_0 = \frac{V_{\mathrm{Thn}} C_{L\mathrm{out}}}{I_{\mathrm{B1}}} \approx 2\frac{V_{\mathrm{Thn}} C_{L\mathrm{out}}}{I_{\mathrm{tail2}}} \tag{13}$$

I_{B1} represents the drain current of M9 which is half of the tail current.

After the initiation of latch process, one of the nmos transistor will turns on which will lead to discharge of corresponding output up to ground and will turn on the pmos of another inverter and charge the another output to the V_{DD}. The time tlatch can be derived by

$$\begin{aligned} \Delta V_0 &= \left|V_{\mathrm{out}p}(t = t_0) - V_{\mathrm{out}n}(t = t_0)\right| = V_{\mathrm{Thn}} - \frac{I_{\mathrm{B2}} t_0}{C_{L\mathrm{out}}} \\ &= V_{\mathrm{Thn}}\left(1 - \frac{I_{\mathrm{B2}}}{I_{\mathrm{B1}}}\right) \end{aligned} \tag{14}$$

ΔV0 is the difference of output voltage at t0. $I_{B1}$and $I_{B2}$are the latch current of side branches. The difference between the latch currents can also be written as

$$\Delta I_{\mathrm{latch}} = |I_{\mathrm{B1}} - I_{\mathrm{B2}}| = g_{mR1,2}\Delta V_{\mathrm{fn/fp}} \tag{15}$$

$g_{mR1,2}$ is the effective trans conductance of transistors MR1 and MR2.

$\Delta V_{fn/fp}$ is the difference of voltage at node fn and fp at time t0

$$\Delta V_0 = V_{\mathrm{Thn}}\frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{B1}}} \approx 2V_{\mathrm{Thn}}\frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{tail2}}} = 2V_{\mathrm{Thn}}\frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}}\Delta V_{\mathrm{fn/fp}} \tag{16}$$

It can be noticed that intermediate stage is amplifying the voltage difference at fn anf fp node.

$\Delta V_{fn/fp}$ can be derived from

$$\begin{aligned}\Delta V_{\text{fn/fp}} &= \left|V_{\text{fn}}(t=t_0) - V_{\text{fp}}(t=t_0)\right| \\ &= t_0 \cdot \frac{I_{\text{N1}} - I_{\text{N2}}}{C_{L,\text{fn(p)}}} \\ &= t_0 \cdot \frac{g_{\text{m1,2}}\Delta V_{\text{in}}}{C_{L,\text{fn(p)}}}\end{aligned} \tag{17}$$

$I_{N1}$and I_{N2} are the discharging current from transistor M1 and M2. So, ΔV0 can be expressed as

$$\begin{aligned}\Delta V_0 &= 2V_{\text{Thn}}\frac{g_{\text{mR1,2}}}{I_{\text{tail2}}}\Delta V_{\text{fn/fp}} \\ &= \left(\frac{2V_{\text{Thn}}}{I_{\text{tail2}}}\right)^2 \cdot \frac{C_{L\text{out}}}{C_{L,\text{fn(p)}}} \cdot g_{\text{mR1,2}}g_{\text{m1,2}}\Delta V_{\text{in}}\end{aligned} \tag{18}$$

So, the total delay can be expressed as

$$t_{\text{delay}} = t_0 + t_{\text{latch}} = 2\frac{V_{\text{Thn}}C_{L\text{out}}}{I_{\text{tail2}}} + \frac{C_{L\text{out}}}{g_{m,\text{eff}}} \cdot \ln\left(\frac{V_{\text{DD}}/2}{\Delta V_0}\right)$$

$$\begin{aligned}t_{\text{delay}} &= 2\frac{V_{\text{Thn}}C_{L\text{out}}}{I_{\text{tail2}}} + \frac{C_{L\text{out}}}{g_{m,\text{eff}}} \\ &\quad \cdot \ln\left(\frac{V_{\text{DD}} \cdot I_{\text{tail2}}^2 \cdot C_{L,\text{fn(p)}}}{8V_{\text{Thn}}^2 \cdot C_{L\text{out}}g_{\text{mR1,2}}g_{\text{m1,2}}\Delta V_{\text{in}}}\right)\end{aligned} \tag{19}$$

It has been noticed that the delay of comparator is depending on the difference of node voltage of fn and fp at time t0. So, increasing the difference of voltages at node will reduce the delay time of the comparator.

After the initiation of latch, the voltage at node fn and fp will discharge to ground so intermediate stage doesn't perform any role in improving the trans conductance of latch regeneration [12]. In reset phase, the voltage at node fn and fp again pulls up to V_{DD} which means power consumption.

3.3.3 MODIFIED DOUBLE TAIL COMPARATOR

In conventional double tail comparator, it has been noticed that difference in node voltage at fn and fp at time t0 effect the speed of latch regeneration. If the difference between node voltages

is more, it will increase the speed of the comparator. To achieve this two control transistors have been added in parallel to M3 and M4 in a cross coupled manner [11].

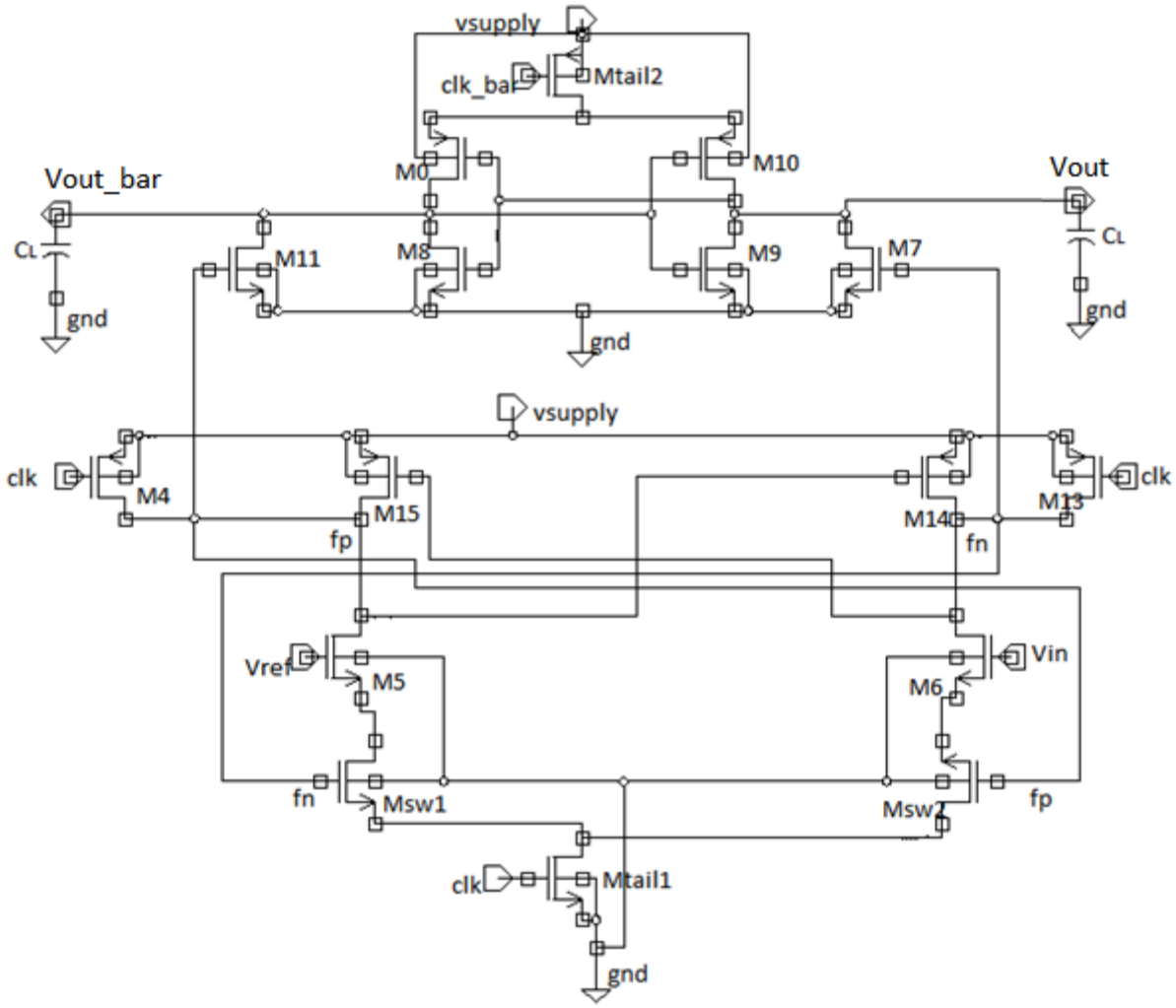

Figure 14: Modified Double Tail Comparator

WORKING

In the reset phase, clk= '0' , Mtail1 and Mtail2 are off and M4 and M13 are on which will pull up the node fn and fp to supply voltage which will lead to discharge of both latch outputs to ground.

In the decision making, clk= '1', Mtail1 and Mtail2 are on and M4 and M13 are turn off. In the beginning, control transistors M15 and M14 are off as fn and fp are still charged upto V_{DD}. Depending on the input voltage one the node starts discharging faster than other and the faster discharging node will turn on the corresponding pmos which will lead to pulling up the another node to V_{DD}. In the modified double tail comparator, fn and fp will charge or discharge

exponentially which will reduce the latch regeneration time. In the modified structure, one of the control transistor is always turns on which will lead to static power dissipation. To overcome this problem, two switching transistors have been used.

Similar to the previous discussed dynamic comparator, the delay of the comparator consists of two time delay, t0 and tlatch, where t0 is considered as the time which comparator takes for initiation of latch regeneration. The latch regeneration time (tlatch) depends on the difference of the output voltages at time t0. More is the difference in output voltage (ΔV0) less will be the regeneration time. ΔV0 can be expressed as

$$\begin{aligned}\Delta V_0 &= V_{\text{Thn}} \frac{\Delta I_{\text{latch}}}{I_{\text{B1}}} \\ &\approx 2V_{\text{Thn}} \frac{\Delta I_{\text{latch}}}{I_{\text{tail2}}} \\ &= 2V_{\text{Thn}} \frac{g_{\text{mR1,2}}}{I_{\text{tail2}}} \Delta V_{\text{fn/fp}}\end{aligned} \tag{20}$$

ΔVfn/fp represents the voltage difference between the node fn and fp at time t0. It can be derived by the equation

$$\Delta V_{\text{fn/fp}} = \Delta V_{\text{fn(p)0}} \exp((A_{\text{v}} - 1)t/\tau) \tag{21}$$

where $\frac{\tau}{A_{\text{v}}-1} \cong \frac{C_{\text{L,fn(p)}}}{G_{\text{m,eff1}}}$

$\Delta V_{fn(p)0}$ represents the voltage difference when the corresponding pmos turns on. Therefore, $\Delta V_{fn(p)0}$ can be expressed as

$$\Delta V_{\text{fn(p)0}} = 2\left|V_{\text{Thp}}\right| \frac{g_{\text{m1,2}} \Delta V_{\text{in}}}{I_{\text{tail1}}} \tag{22}$$

After substitution, ΔV0 can be expressed as

$$\begin{aligned}\Delta V_0 &= 2V_{\text{Thn}} \frac{g_{\text{mR1,2}}}{I_{\text{tail2}}} \Delta V_{\text{fn/fp}} \\ &= 4V_{\text{Thn}} \left|V_{\text{Thp}}\right| \frac{g_{\text{mR1,2}}}{I_{\text{tail2}}} \frac{g_{\text{m1,2}} \Delta V_{\text{in}}}{I_{\text{tail1}}} \exp\left(\frac{G_{\text{m,eff1}} \cdot t_0}{C_{\text{L,fn(p)}}}\right)\end{aligned} \tag{23}$$

It can be noticed that ΔV0 has been increased impressively as compared to conventional dynamic comparator.

In the conventional double tail comparator both nodes fn and fp discharge to ground so they don't play any role in the improvement of trans conductance. But in the modified comparator one of the node will remain charge to power supply which will increase the trans conductance of the latch. Therefore, tlatch can be given by

$$t_{\text{latch}} = \frac{C_{L\text{out}}}{g_{\text{m,eff}} + g_{\text{mR1,2}}} \cdot \ln\left(\frac{\Delta V_{\text{out}}}{\Delta V_0}\right) = \frac{C_{L\text{out}}}{g_{\text{m,eff}} + g_{\text{mR1,2}}} \cdot \ln\left(\frac{V_{\text{DD}}/2}{\Delta V_0}\right) \tag{24}$$

The total delay time of the modified comparator can be expressed as

$$\begin{aligned} t_{\text{delay}} &= t_0 + t_{\text{latch}} \\ &= 2\frac{V_{\text{Thn}} C_{L\text{out}}}{I_{\text{tail2}}} + \frac{C_{L\text{out}}}{g_{\text{m,eff}} + g_{\text{mr1,2}}} \cdot \ln\left(\frac{V_{\text{DD}}/2}{\Delta V_0}\right) \\ &= 2\frac{V_{\text{Thn}} C_{L\text{out}}}{I_{\text{tail2}}} + \frac{C_{L\text{out}}}{g_{\text{m,eff}} + g_{\text{mR1,2}}} \\ &\quad \times \ln\left(\frac{V_{\text{DD}}/2}{4V_{\text{Thn}}\left|V_{\text{Thp}}\right| \frac{g_{\text{mR1,2}}}{I_{\text{tail2}}} \frac{g_{\text{m1,2}}\Delta V_{\text{in}}}{I_{\text{tail1}}} \exp\left(\frac{G_{\text{m,eff1}} \cdot t_0}{C_{\text{L,fn(p)}}}\right)}\right) \end{aligned} \tag{25}$$

From the comparison of time delay equations it can be noticed that the modified comparator has taken the advantage of inner positive feedback to improve the latch regeneration.

It has also reduced the power dissipation. In the conventional double tail comparator both fn and fp nodes discharge to ground in the latch regeneration phase and pull back to power supply during reset phase. But in the modified comparator, one of the node remain to power supply which will lead to less power dissipation.

CHAPTER 4: PRIORITY ENCODER

4.1 INTRODUCTION

It is a logic device that converts 2^N input signals to N-bit coded outputs. A priority encoder provides the binary coded output corresponding to the highest order active input. If more than one input is active at the same time, the input having highest priority will take precedence. If input n is active, all lower inputs (0 to n-1) are ignored and the binary representation of 'n' is available at the output. The priority encoders are widely used in flash ADCs and interrupt controllers to select the most critical out of multiple interrupt requests. The outputs of the comparator are fed to the priority encoder shown in fig.15. D_0, D_1, D_2 are the inputs to the encoder and O_0, O_1 are the outputs. Table.2 shows the truth table of a 4-to-2 priority encoder[19].

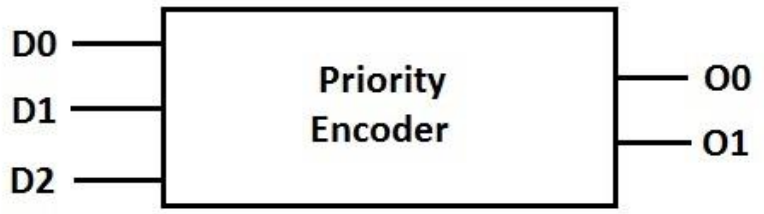

Figure 15: Inputs and Outputs of used priority encoder

D0	D1	D2	O0	O1
1	×	×	1	1
0	1	×	1	0
0	0	1	0	1
0	0	0	0	0

Table 2: Truth table of 3-to-2 priority encoder

	$D'_1D'_2$	D'_1D_2	D_1D_2	$D_1D'_2$
D'_0	0	0	1	1
D_0	1	1	1	1

Table 3: K-Map for the expression of O_0

	$D'_1D'_2$	D'_1D_2	D_1D_2	$D_1D'_2$
D'_0	0	1	0	0
D_0	1	1	1	1

Table 4: K-Map for the expression of O_1

Table.3 and Table.4 show the K-maps used for obtaining the expressions for O_0 and O_1 respectively which are shown in Eq.1 and Eq.2. The priority encoder circuit is realised using CMOS topology as shown in Fig.16.

$$O_o = D_0 + D_1 \tag{26}$$

$$O_1 = D_0 + D_1' D_2 \tag{27}$$

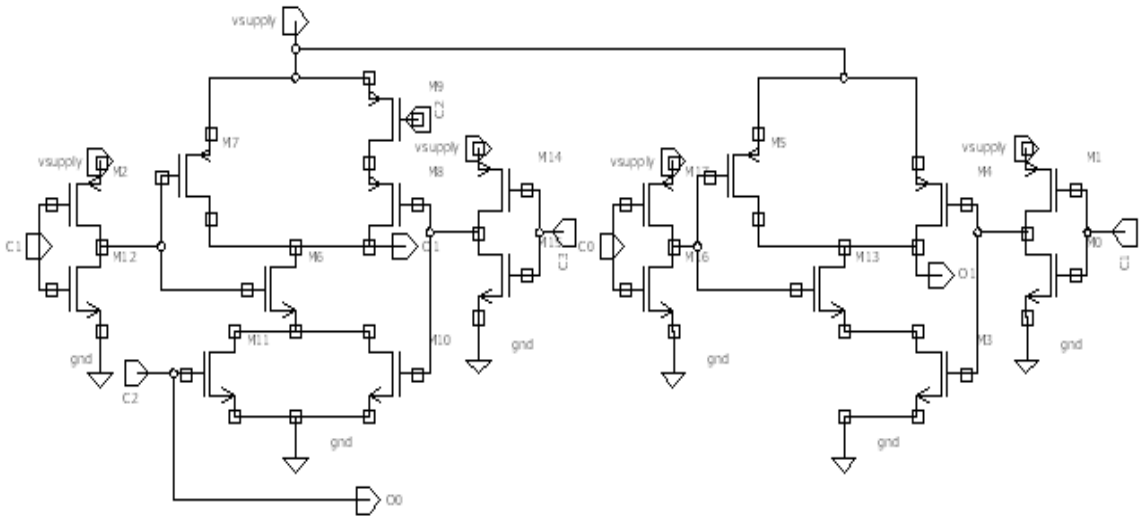

Figure 16: CMOS implementation of priority encoder circuit

CHPATER 5: ADIABATIC LOGIC CIRCUITS

5.1 INTRODUCTION

Adiabatic is a Greek word which means no energy will be transferred from the system to the environment and from the environment to the system. There are two type of power dissipation in the VLSI circuits: static power dissipation and dynamic power dissipation. Static power dissipation occurs due to leakage current and dynamic power dissipation occurs during switching. Power dissipation due to switching has a lower limit of $f_{clk}C_LVdd^2/2$ where C_L is the load capacitance. Adiabatic switching circuits take the power dissipation below this lower limit. It also recycles the energy which reduces the total energy from the power source [20].

The main idea of adiabatic logic circuit is to provide slow constant charging current to the load capacitance which requires a time varying power supply and it is called pulsed power supplies. During charging of a capacitor, power dissipation in the circuit depends on the difference of supply voltage and capacitor voltage. If the difference is small then power dissipation will be less. So, instead of giving constant power supplies, voltage increasing with time will reduce the power dissipation.

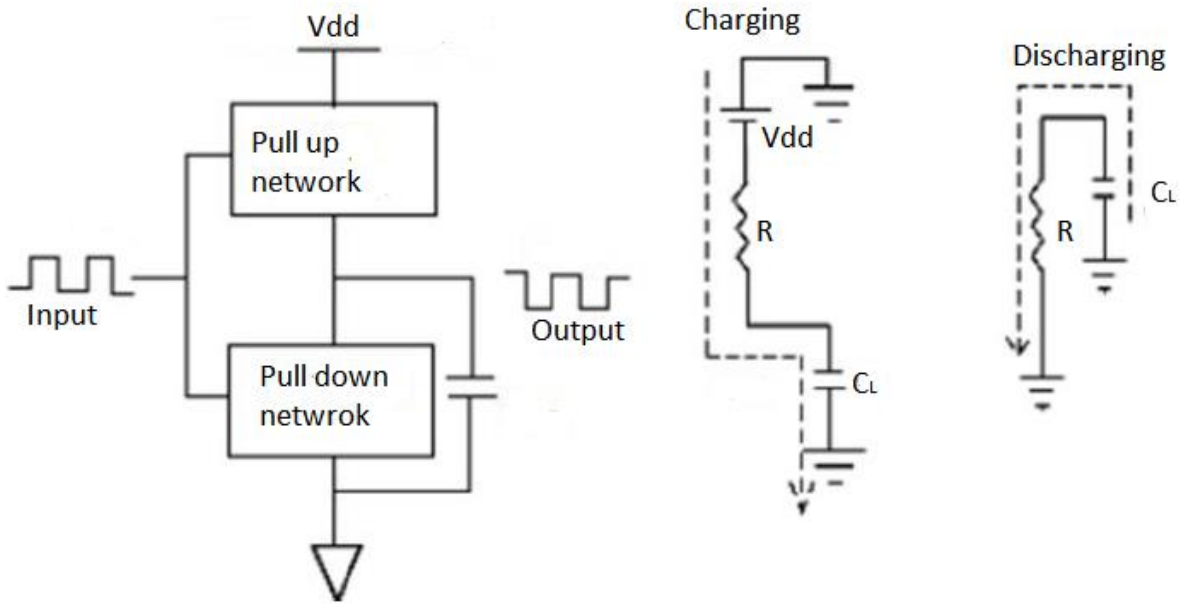

Figure 17: Charging and discharging of load capacitance using constant voltage supply

During charging of capacitor the voltage of capacitor will increase from 0 to Vdd which leads to power dissipation of $f_{clk}C_L Vdd^2/2$. There are many ways to reduce power dissipation such as decrease load capacitance, reduce voltage swing, reduces switching frequency and many more but in all this cases power supply is used only once.

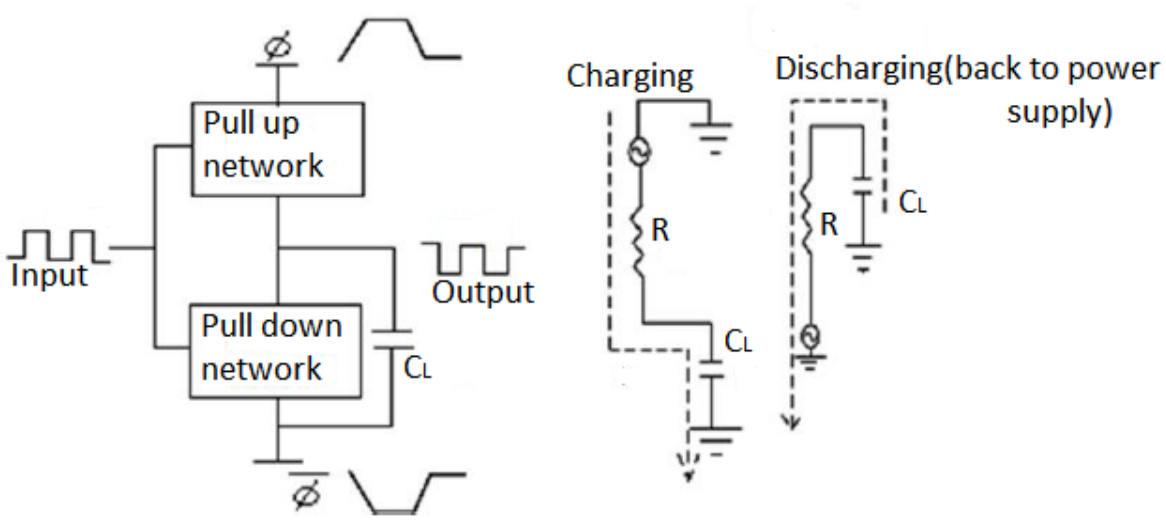

Figure 18: Charging and discharging of load capacitance using adiabatic logic

In adiabatic logic constant current is provided instead of constant power supply. The constant current is given by i(t)= $C_L.\frac{dV}{dt}$, so energy dissipation by using adiabatic logic can be given by

$$E_{adiabatic} = \text{R. } C_L{}^2.V_{dd}^2/\ T_{ramp} \qquad (28)$$

Where, $E_{adiabatic}$ is energy dissipated, C_L is load capacitance, R is resistance of MOS, V_{dd} is final output voltage and T_{ramp} is the rising time. The rising time should be more than 2RC for less power dissipation than conventional logic switching.

Adiabatic logic circuits are of two types:

1) Fully adiabatic logic
2) Partially adiabatic logic

In fully adiabatic logic circuits, number of transistors requires for implementation is much more than conventional circuit so there is need of partially adiabatic logic circuit. There are many ways to implement partially adiabatic logic circuits [21].

5.1.1 EFFICIENT CHARGE RECOVERY LOGIC(ECRL)

In ECRL, two cross coupled PMOS transistors are used which gives complimentary outputs.

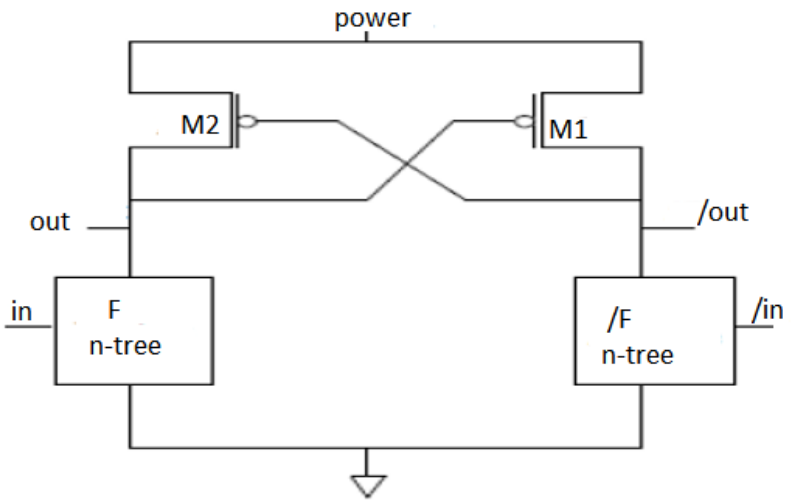

Figure 19: Block Diagram of ECRL

When power supply is raising from 0 to Vdd, one of the output is zero and other output charge to Vdd and when power clock reaches Vdd, outputs will hold in that state. When power supply falls from Vdd to zero, then the output which is charged to Vdd will return the energy back to power supply.

5.1.2 POSITIVE FEEDBACK ADIABATIC LOGIC(PFAL)

In PFAL, there are 2 PMOS and 2 NMOS and the logic function is decided by NMOS which are connected parallel to PMOS devices.

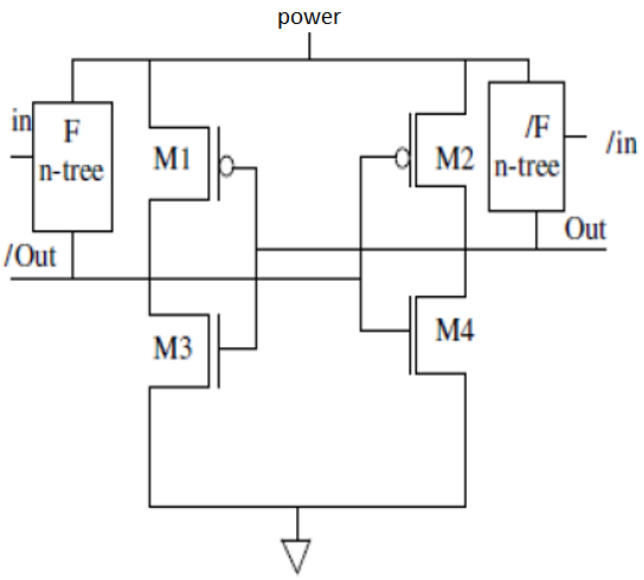

Figure 20: Block Diagram of PFAL

The advantage of PFAL is that output will never be in floating state. In ECRL, before power clock reaches Vth there is non-adiabatic power loss which will not occur in PFAL.

5.1.3 2N-2N2P

In 2N-2N2P, two inverters are cross coupled and inputs are connected to NMOS devices which are parallel to NMOS.

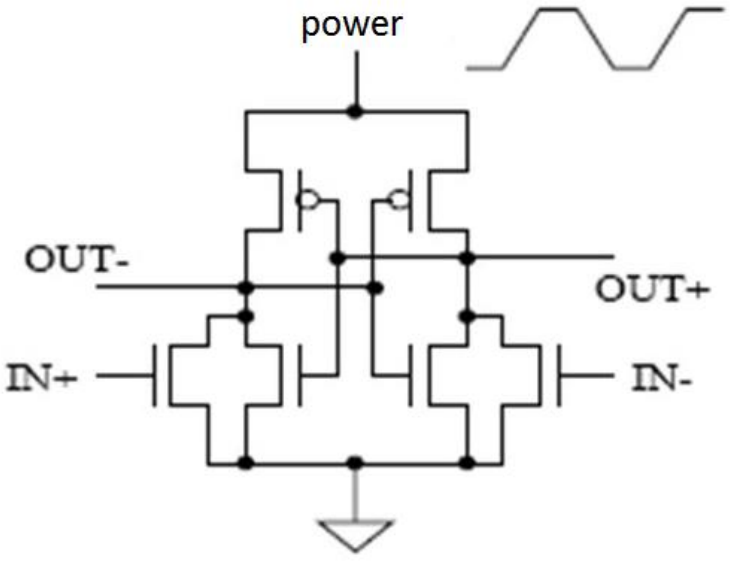

Figure 21: 2N-2N2P

Because of cross-coupling of NMOS transistors the output will never be in floating state and energy will get recycled in the recovery state.

CHAPTER 6: SIMULATION AND ANALYSIS

Flash ADC using different dynamic comparators which are explained in chapter 3 has been simulated with and without adiabatic logic at 90nm PTM technology parameter. Analysis of delay, power dissipation and frequency of flash ADC has been done. The output of priority encoder is O0 O1. The output values of 00, 01, 10 and 11 represents 0.5V, 0.6V, 0.7V and 0.8V respectively.

6.1 SCHEMATIC AND RESULTS OF FLASH ADC USING VARIOUS DYNAMIC COMPARATORS WITHOUT ADIABATIC LOGIC

Fig.22 is showing the value of input and reference voltages to the comparators and the clock signal at which circuit is working. The input voltage is 0.645V.

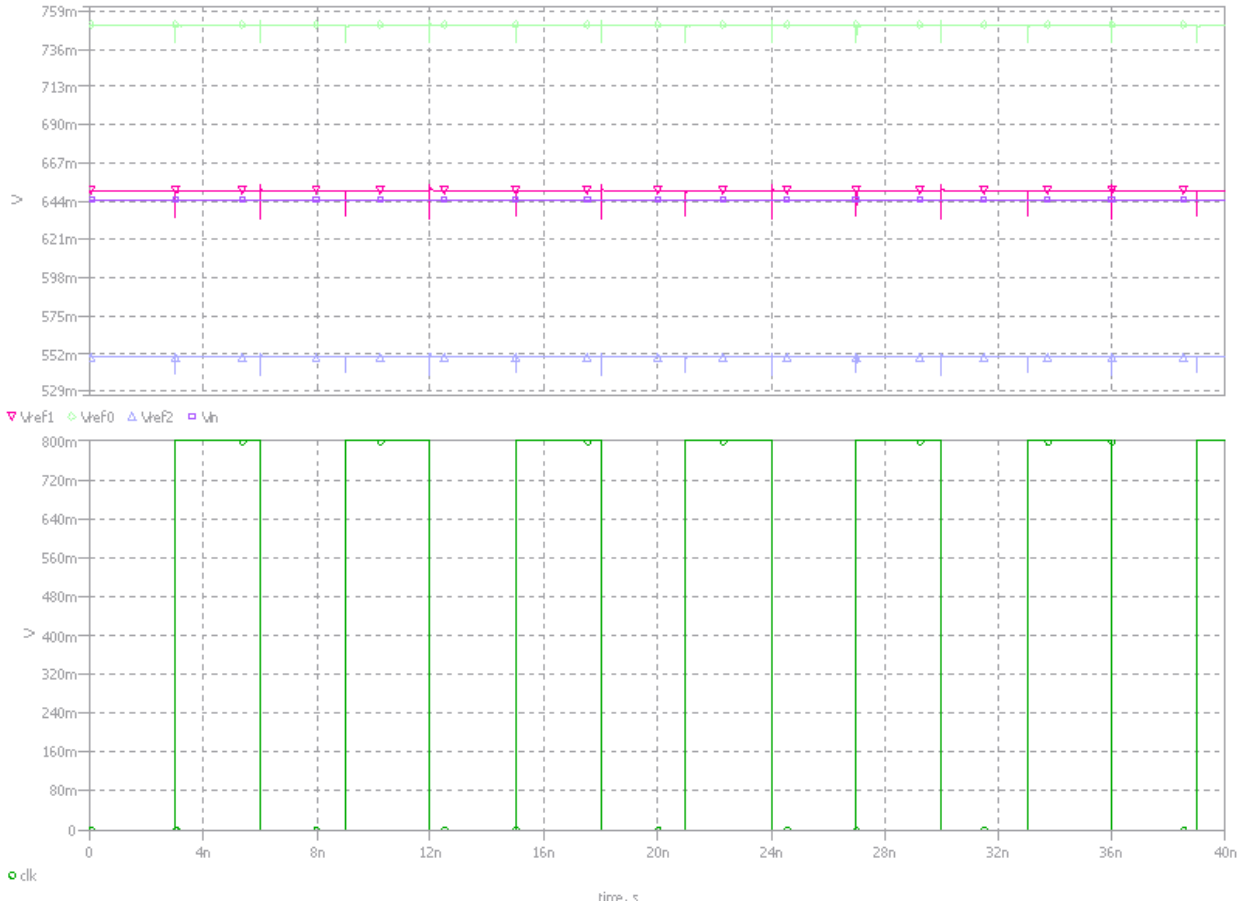

Figure 22: Value of input and reference voltages and clock signal

6.1.1 FLASH ADC USING CONVENTIONAL DYNAMIC COMPARATOR

Schematic of 4-bit flash ADC using conventional dynamic comparator is shown in Figure 23. Figure 24 is showing the output of conventional dynamic comparator at supply voltage of 0.8V with input voltage of 0.645V. Figure 25 represents the output of priority encoder.

The output of priority encoder is 01 which represents 0.6V.

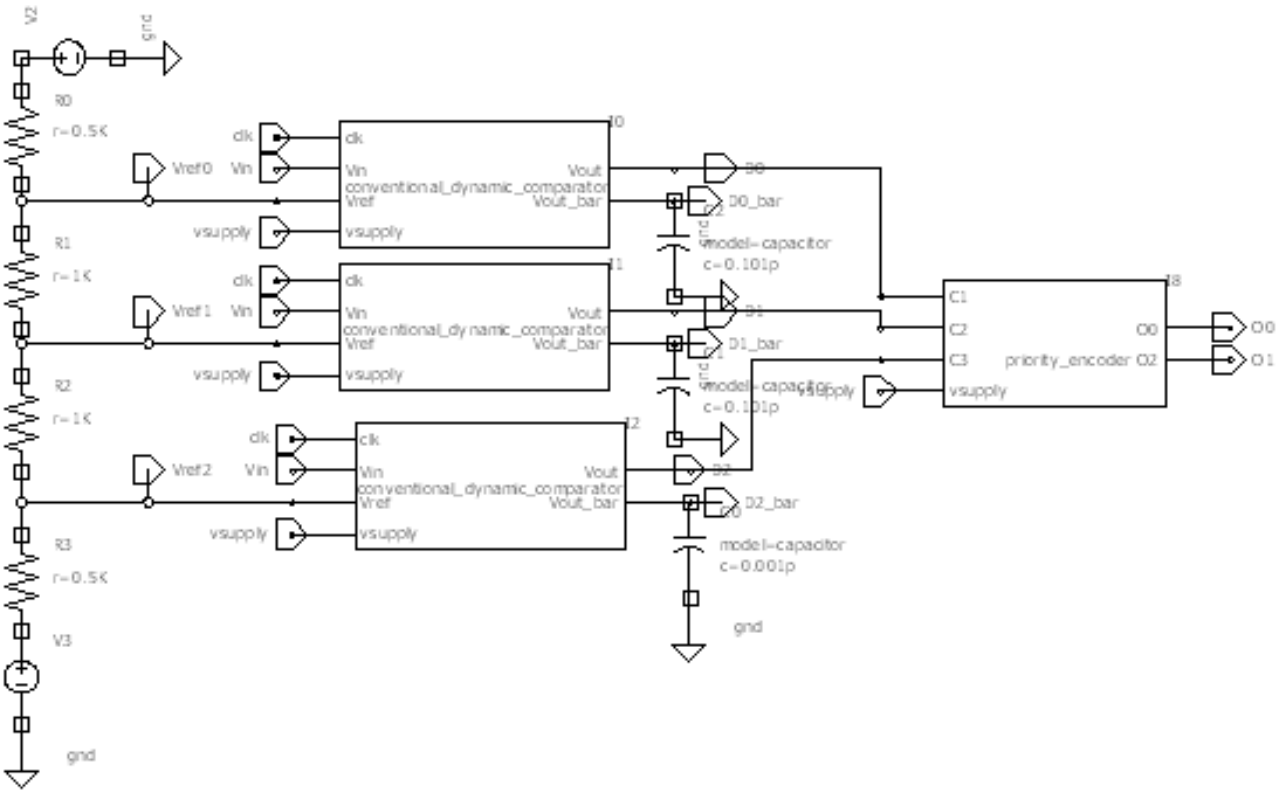

Figure 23: Schematic of Flash ADC

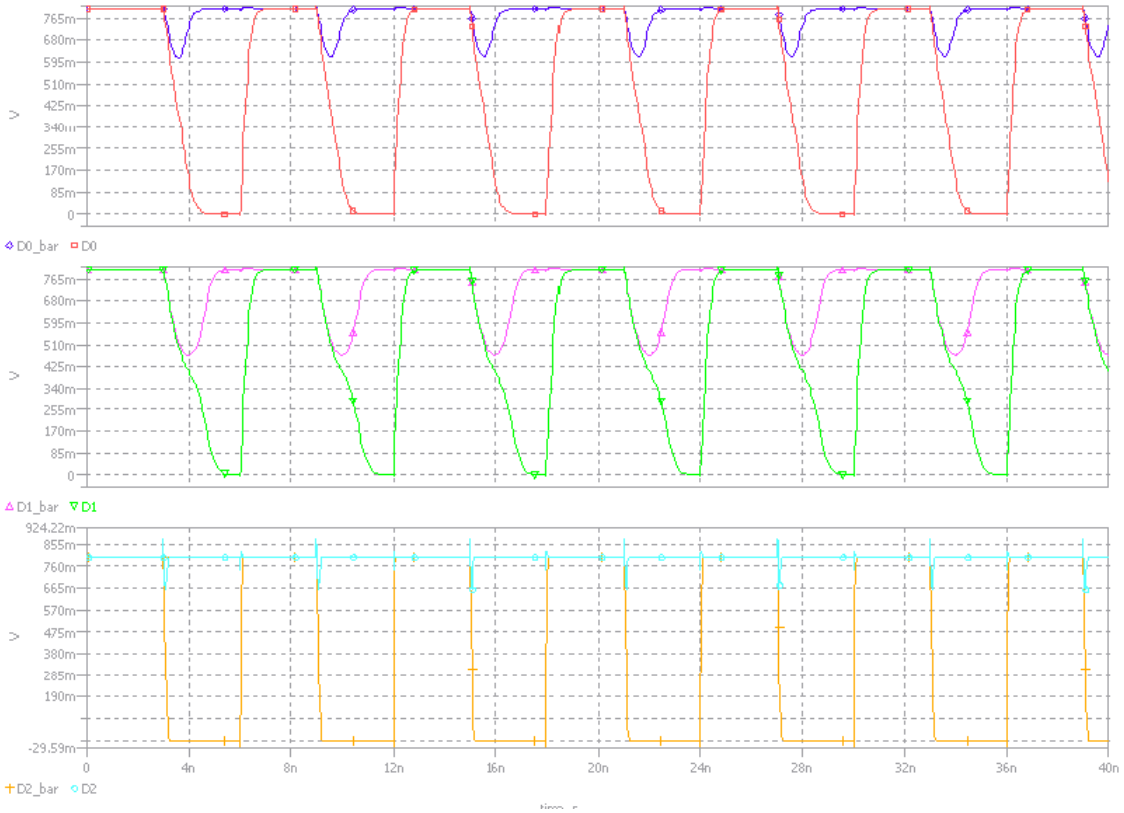

Figure 24: Output of Conventional Dynamic Comparator

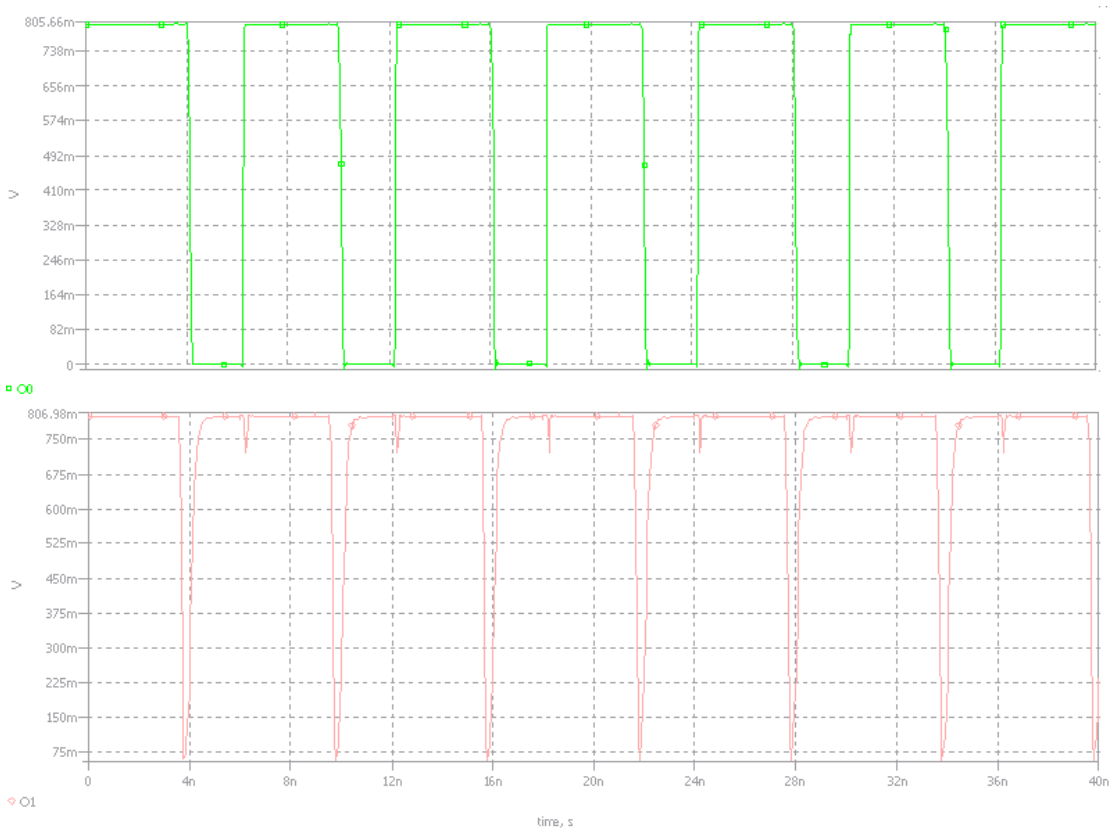

Figure 25: Output of Priority Encoder

6.1.2 FLASH ADC USING CONVENTIONAL DOUBLE TAIL COMPARATOR

Schematic of 4-bit flash ADC using conventional double tail comparator is shown in Figure 26. Figure 27 is showing the output of conventional double tail comparator at supply voltage of 0.8V with input voltage of 0.645V. Figure 28 represents the output of priority encoder.

The output of priority encoder is 01 which represents 0.6V.

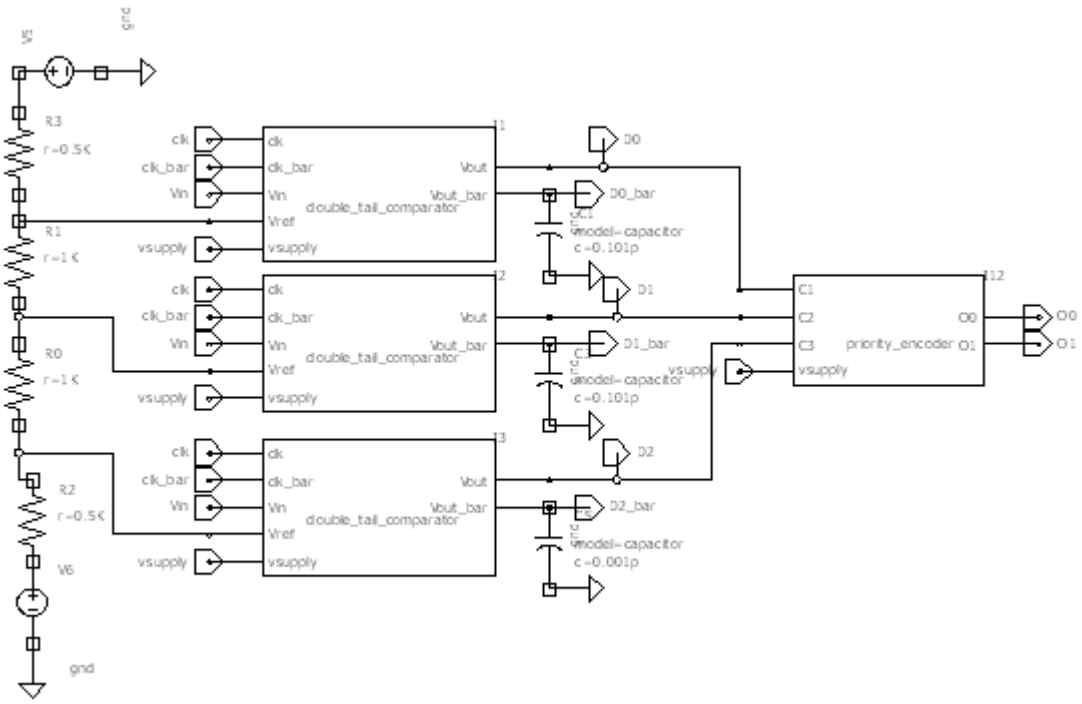

Figure 26: Schematic of Flash ADC

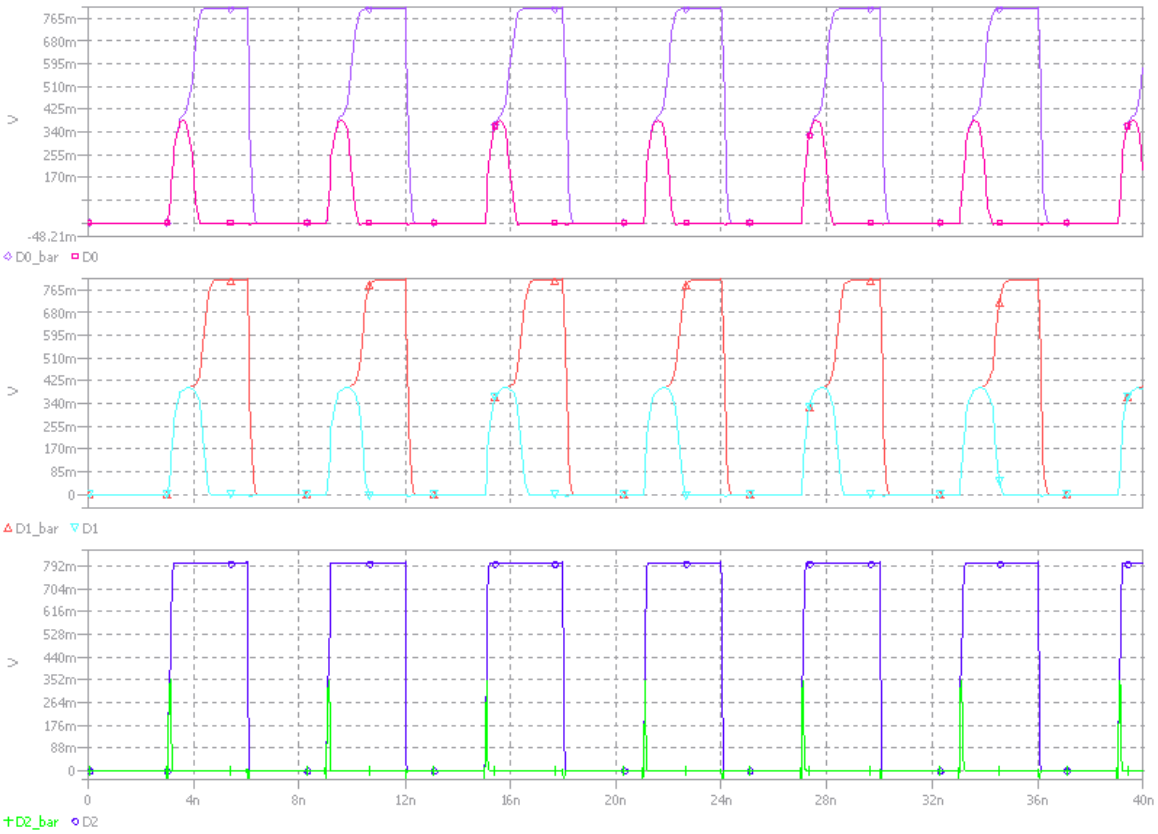

Figure 27: Output of Conventional Double Tail Comparator

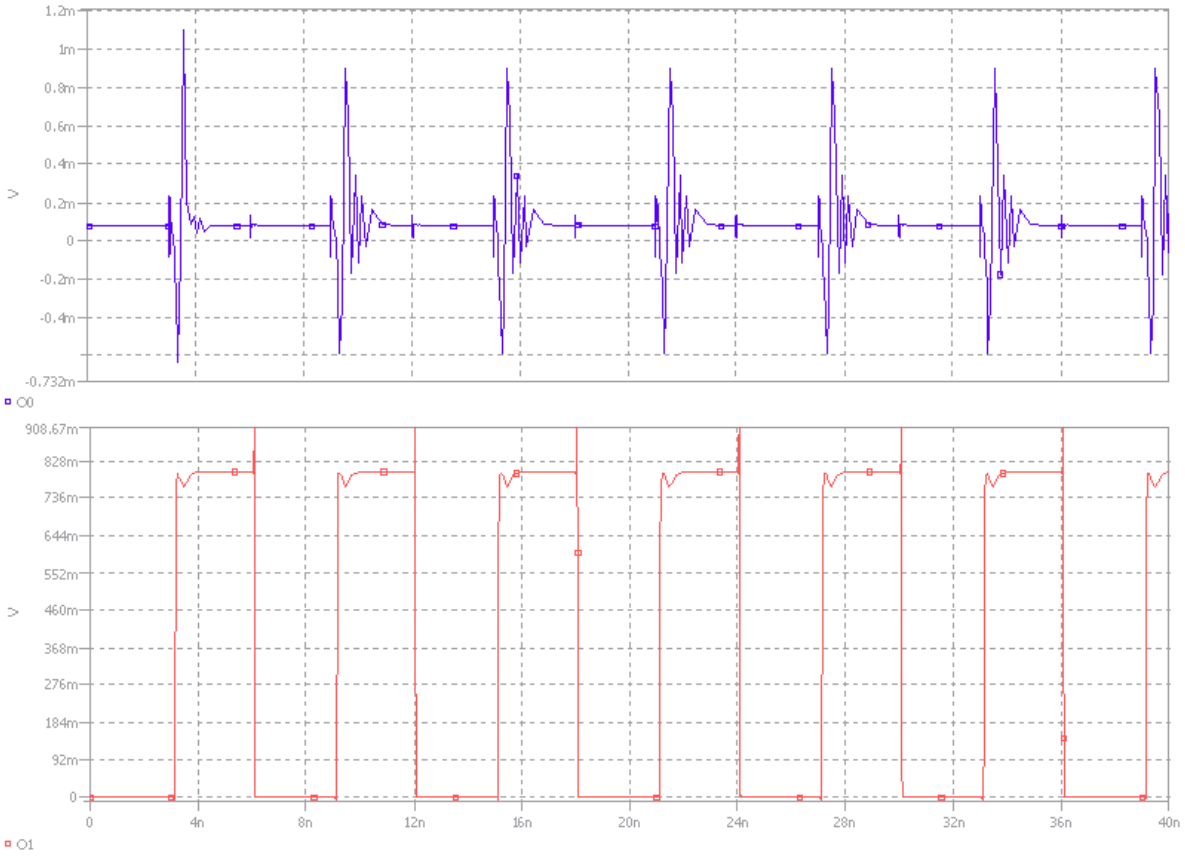

Figure 28: Output of Priority Encoder

6.1.3 FLASH ADC USING MODIFIED DOUBLE TAIL COMPARATOR

Schematic of 4-bit flash ADC using conventional double tail comparator is shown in Figure 29. Figure 30 is showing the output of conventional double tail comparator at supply voltage of 0.8V with input voltage of 0.645V. Figure 31 represents the output of priority encoder.

The output of priority encoder is 01 which represents 0.6V.

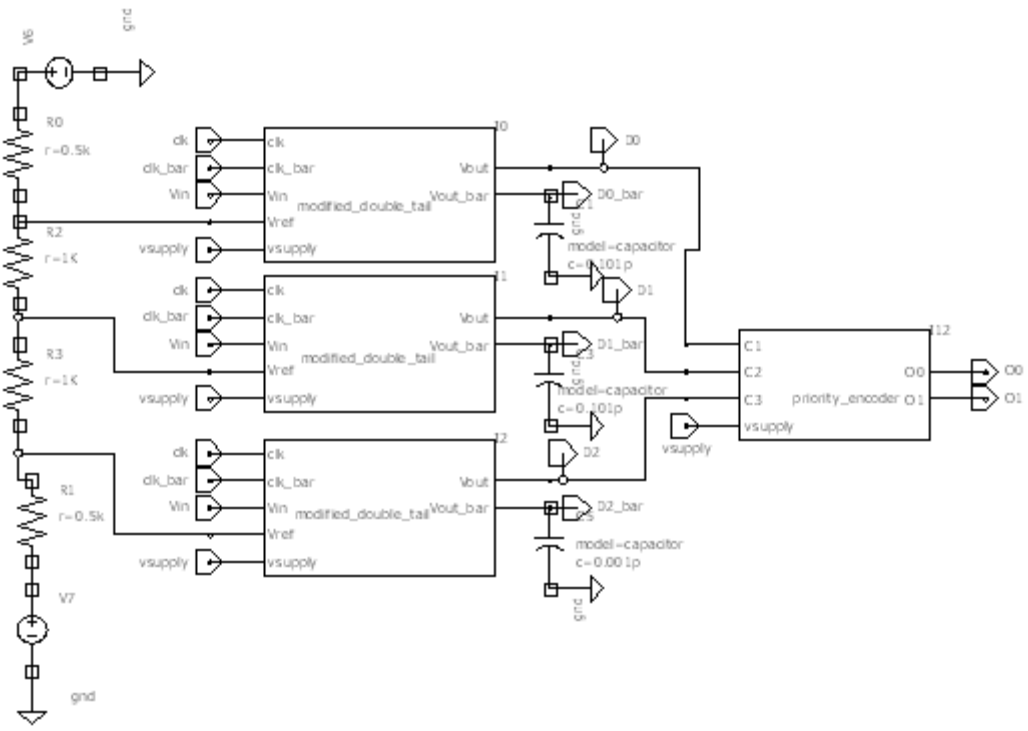

Figure 29: Schematic of Flash ADC

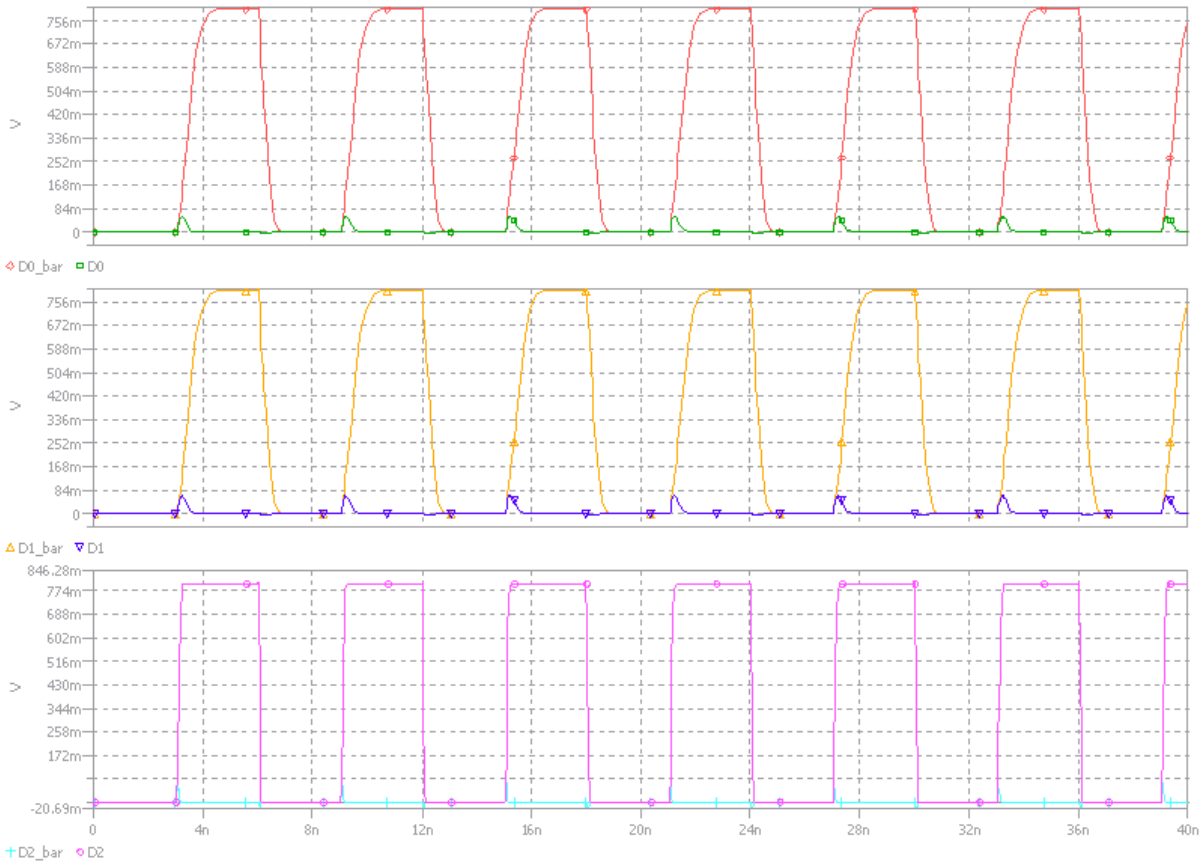

Figure 30: Output of Modified Double Tail Comparator

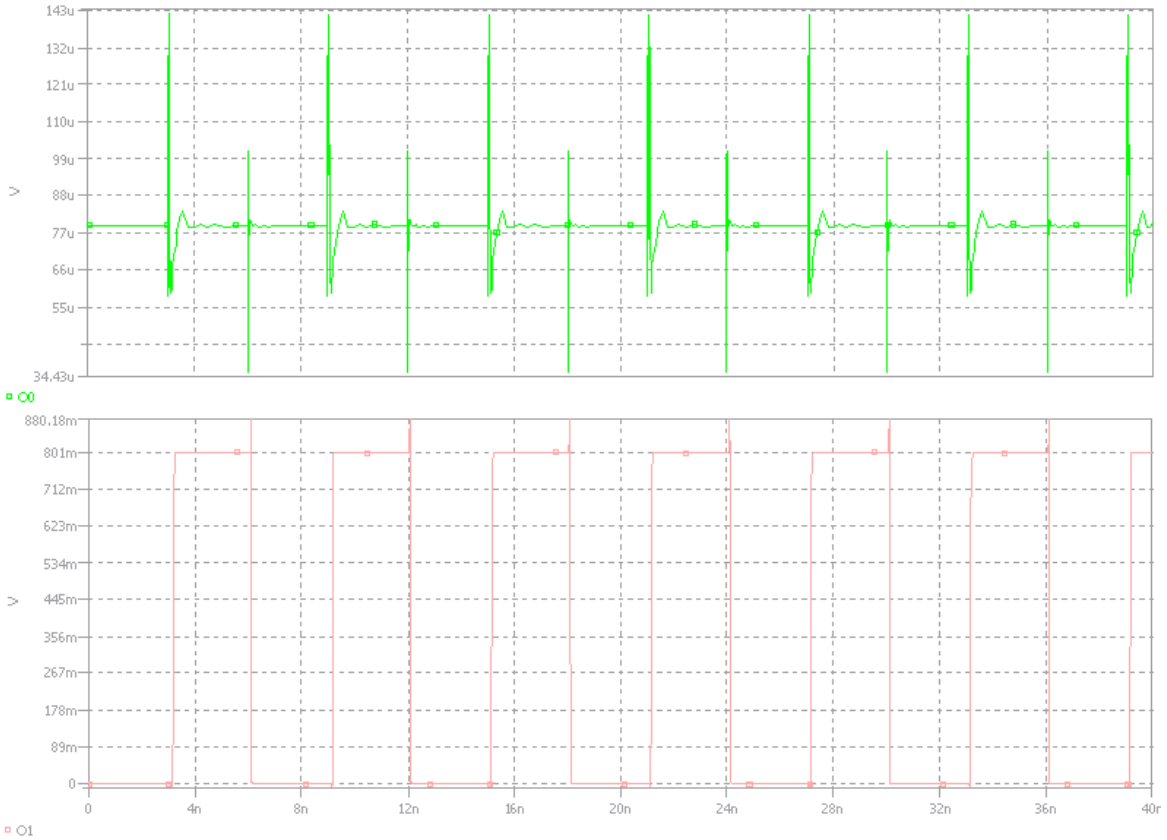

Figure 31: Output of Priority Encoder

6.2 SCHEMATIC AND RESULTS OF FLASH ADC USING VARIOUS DYNAMIC COMPARATORS USING ADIBATIC LOGIC

Fig.32 is showing the value of input and reference voltages to the comparators, pulsed power and the clock signal at which circuit is working. The input voltage is 0.645V.

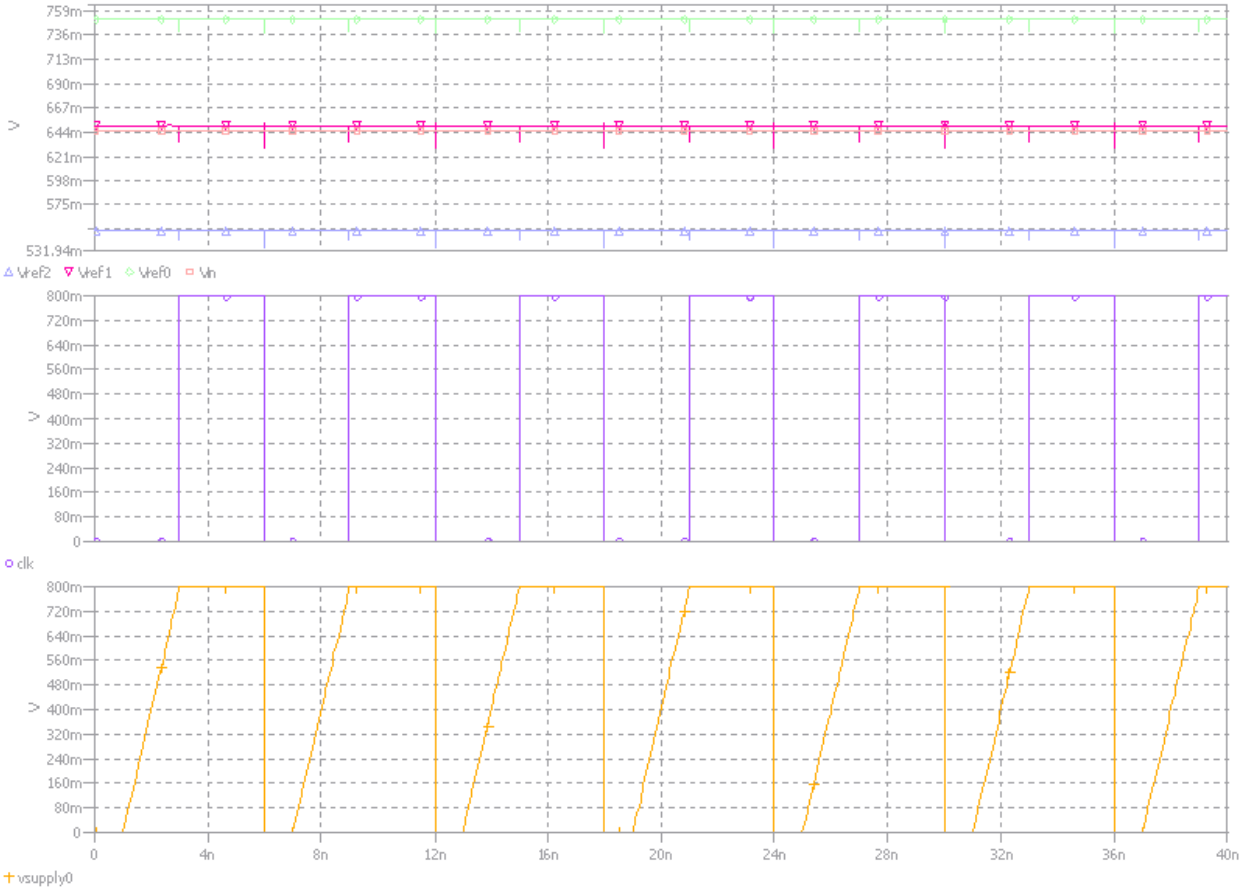

Figure 32: Value of input and reference voltages, pulsed power and clock signal

6.2.1 FLASH ADC USING CONVENTIONAL DYNAMIC COMPARATOR

Schematic of 4-bit flash ADC using conventional dynamic comparator is shown in Figure 33. Figure 34 is showing the output of conventional dynamic comparator at supply voltage of 0.8V with input voltage of 0.645V. Figure 35 represents the output of priority encoder.

The output of priority encoder is 01 which represents 0.6V.

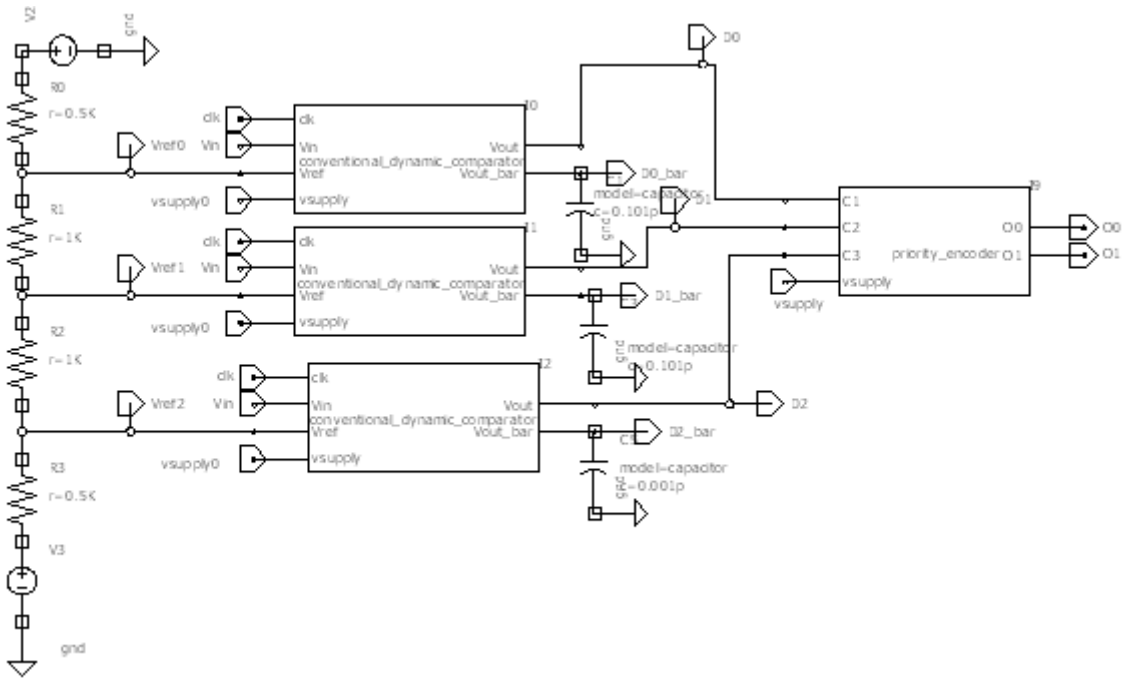

Figure 33: Schematic of Flash ADC

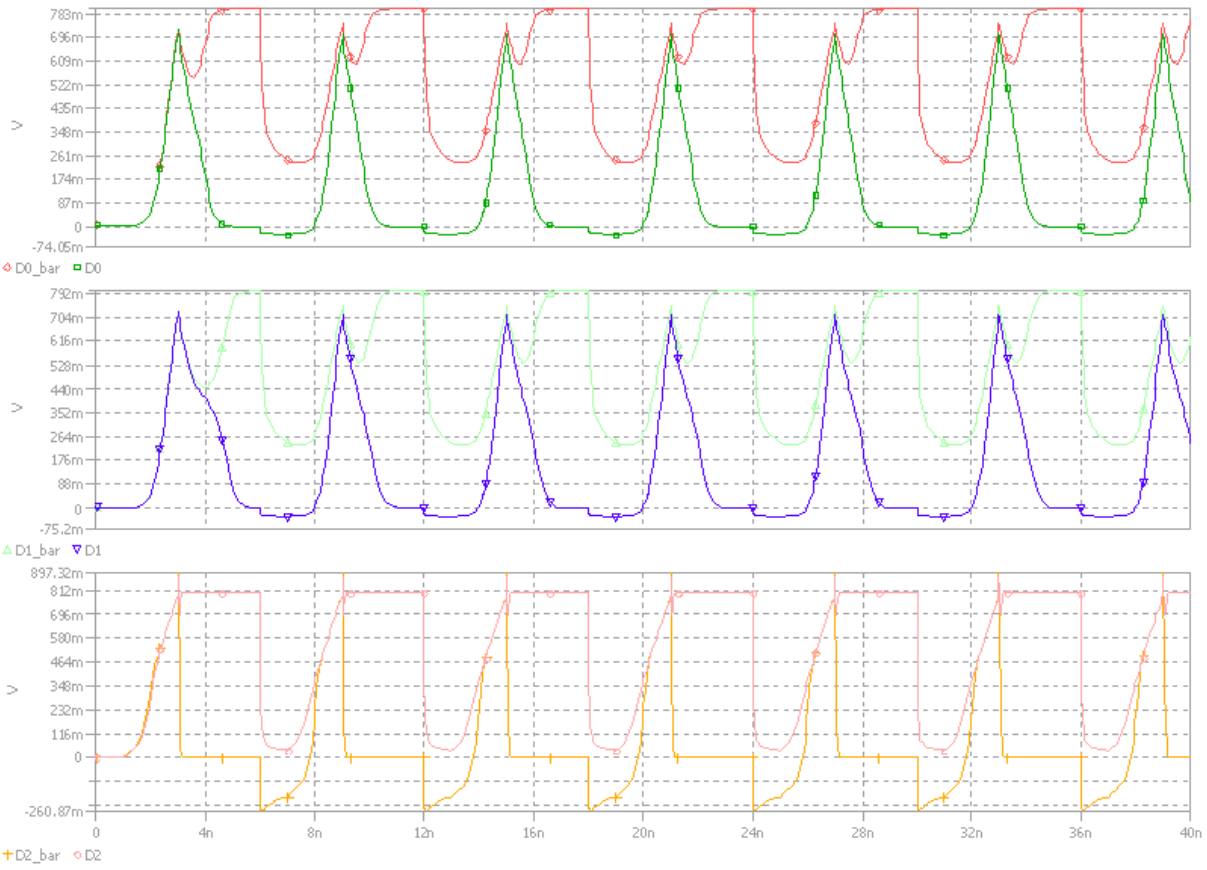

Figure 34: Output of Conventional Dynamic Comparator

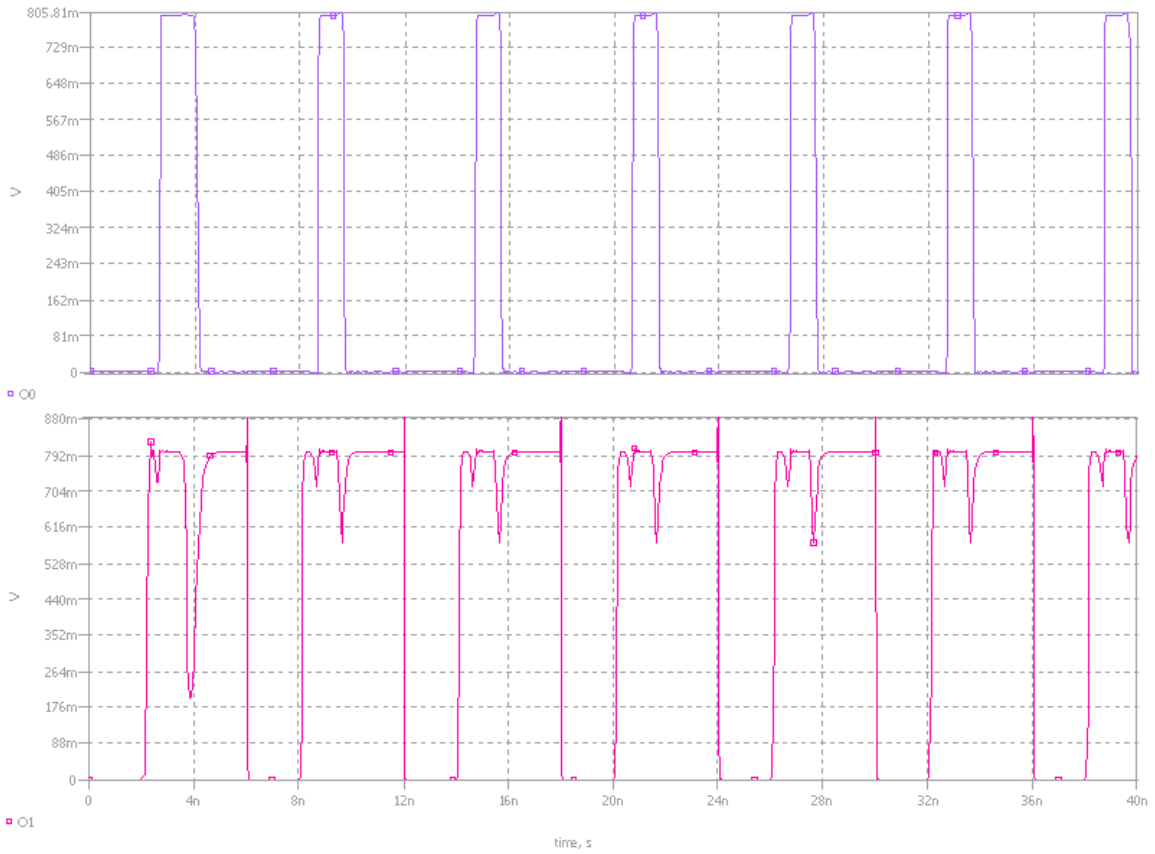

Figure 35: Output of Priority Encoder

6.2.2 FLASH ADC USING CONVENTIONAL DOUBLE TAIL COMPARATOR

Schematic of 4-bit flash ADC using conventional double tail comparator is shown in Figure 36. Figure 37 is showing the output of conventional dynamic comparator at supply voltage of 0.8V with input voltage of 0.645V. Figure 38 represents the output of priority encoder.

The output of priority encoder is 01 which represents 0.6V.

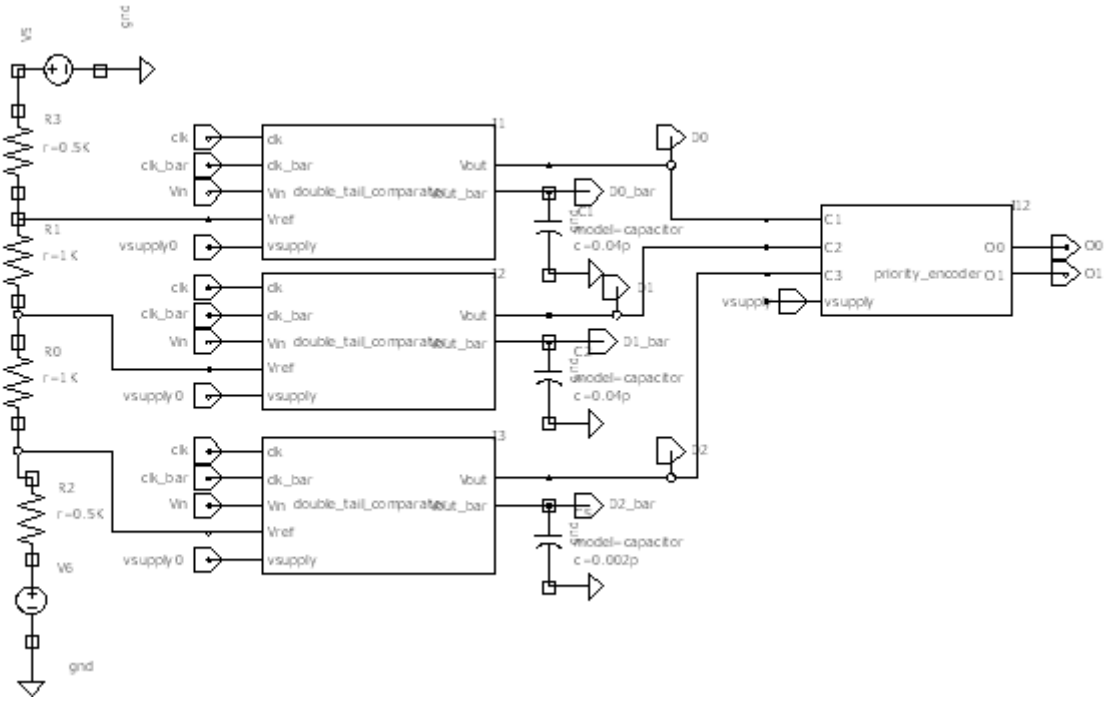

Figure 36: Schematic of Flash ADC

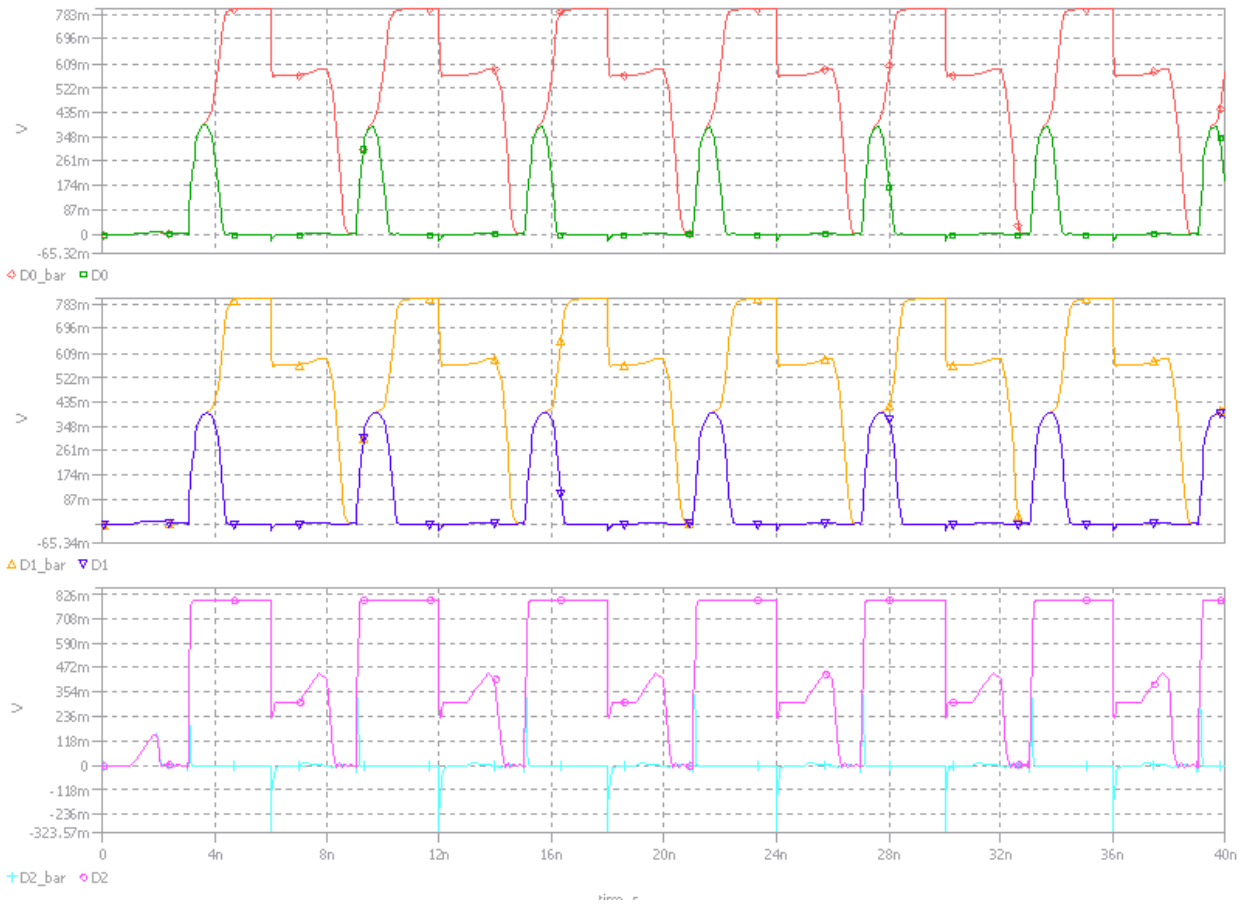

Figure 37: Output of Conventional Double Tail Comparator

Figure 38: Output of Priority Encoder

6.2.3 FLASH ADC USING MODIFIED DOUBLE TAIL COMPARATOR

Schematic of 4-bit flash ADC using modified double tail comparator is shown in Figure 39. Figure 40 is showing the output of conventional dynamic comparator at supply voltage of 0.8V with input voltage of 0.645V. Figure 41 represents the output of priority encoder.

The output of priority encoder is 01 which represents 0.6V.

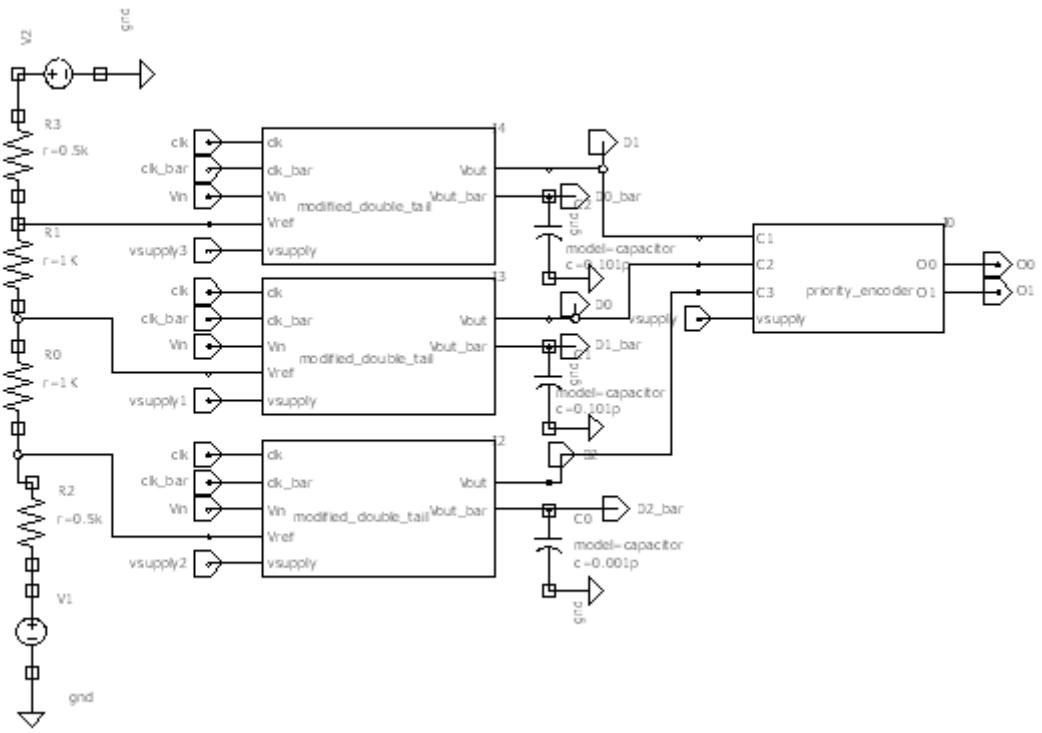

Figure 39: Schematic of Flash ADC

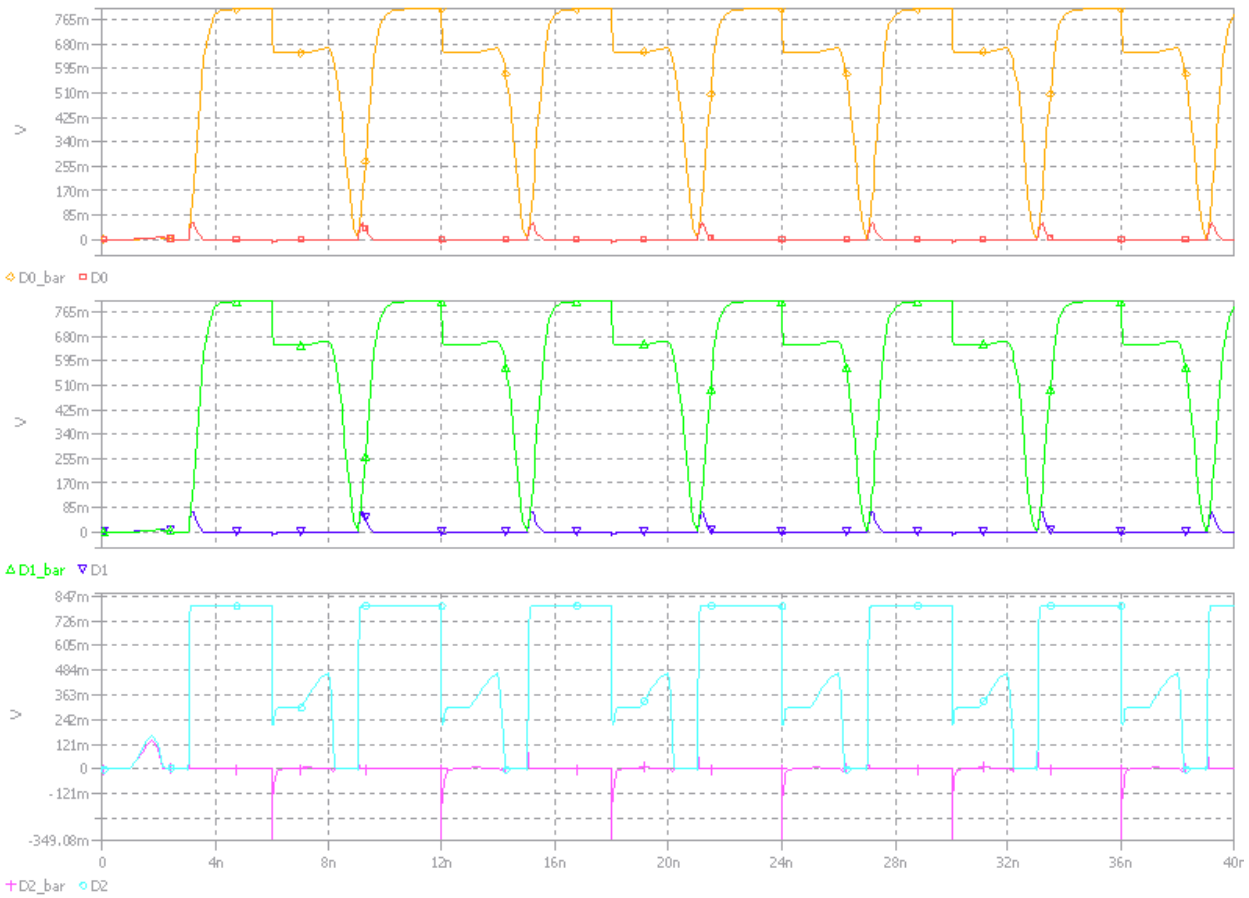

Figure 40: Output of Modified Double Tail Comparator

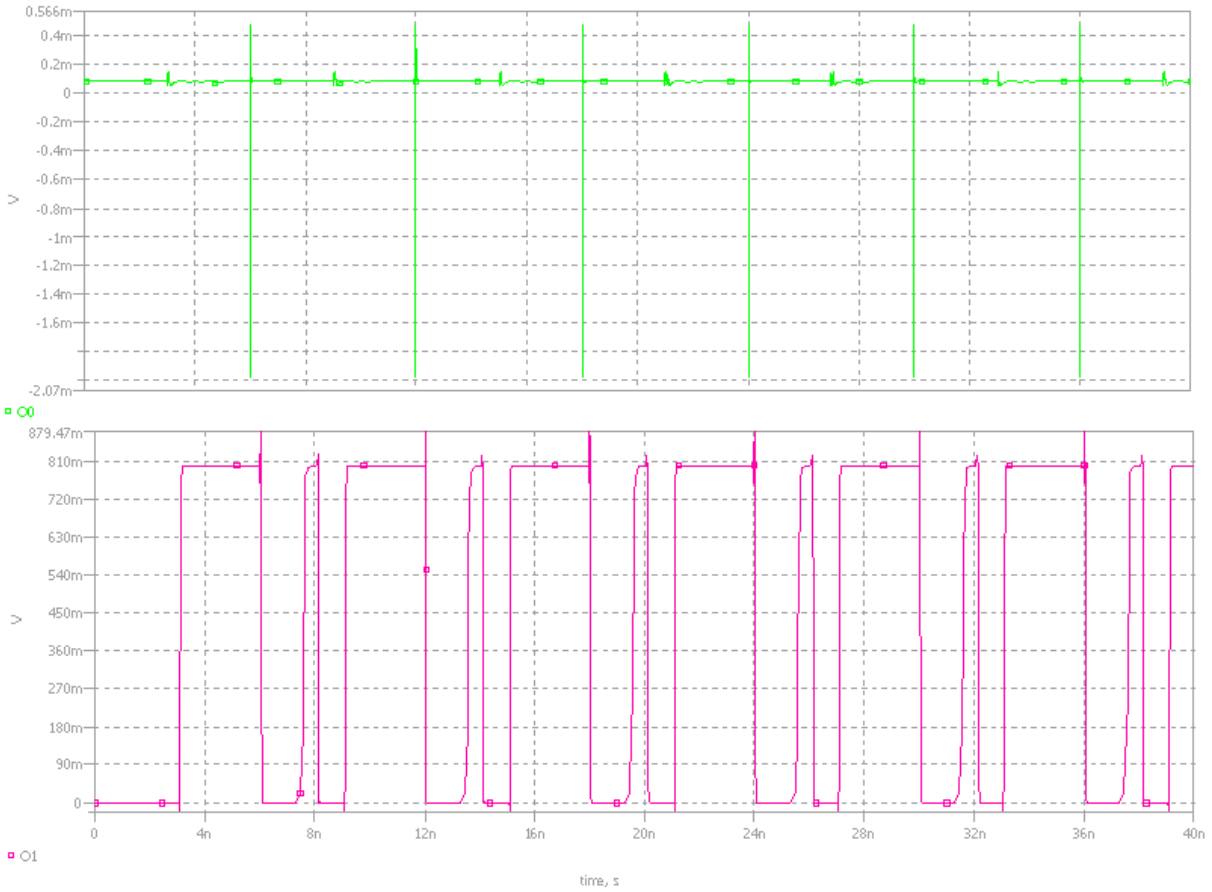

Figure 41: Output of Priority Encoder

Comparator without using Adiabatic Logic			
	Propagation Delay(ns)	**Power Dissipation(µW)**	**Frequency(MHz)**
Conventional Dynamic	1.145	169.3	33
Conventional Double Tail	0.747	220.31	56
Modified Double Tail	0.550	110.73	67
Comparator with Adiabatic Logic			
	Propagation Delay(ns)	**Power Dissipation(µW)**	**Frequency(MHz)**
Conventional Dynamic	1.315	90.425	25
Conventional Double Tail	0.763	130.52	34
Modified Double Tail	0.574	60.42	38

Table 5: Propagation Delay and Power Dissipation of Flash ADC

CHAPTER7: CONCLUSION AND FUTURE SCOPE

CONCLUSION

In this thesis, flash ADC using various dynamic comparators with and without adiabatic logic has been simulated at 90nm PTM model using symica and LTspice. Propagation delay and power dissipation has been calculated. It has been noticed that by using adiabatic logic, power dissipation has been reduced up to great extent. The flash ADC using conventional dynamic, conventional double tail and modified double tail comparator with difference voltage of 5mV and common mode voltage of 0.64V using adiabatic comparator can reduce the power dissipation by 46%, 40.7% and 45.43% respectively with resolution of 0.05V.

FUTURE SCOPE

In flash ADC using dynamic comparator the delay and power dissipation has been reduced but it requires a high common mode voltage of at least 0.5V which has reduced the input voltage range and minimum difference voltage of 5mV is required for proper functioning of comparator. So, common mode voltage and difference voltage can be reduced for high input range and for more accurate comparison and frequency can also be improved.

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