M. Tech (VLSI Design & Embedded System) ANIL KUMAR 2018

IMPLEMENTION OF LOW POWER VDBA AND ITS APPLICATION

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI Design &Embedded System

Submitted by:

ANIL KUMAR

2K16/VLS/04

Under the supervision of

Prof. Rajeshwari Pandey

Electronics & Communication Engineering
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

(Session: 2016-18)

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Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, ANIL KUMAR, Roll No.2K16/VLS/04 student of M. Tech **VLSI & Embedded System,** hereby declare that the project Dissertation titled "**Implementation of Low power VDBA and its Application**" which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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ANIL KUAMR

ROLL NO. 2K16/VLS/04

M.TECH (VLSI)

Electronics & Communication Engineering
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled "**Implementation of Low power VDBA and its Application**" which is submitted by **ANIL KUMAR**, **Roll No. 2K16/VLS/04**, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology/Bachelor of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi **PROF.RAJESHWARI PANDEY**

Date: (**SUPERVISOR)**

ABSTRACT

This desertion is about designing low-voltage low- power (LVLP) analog VDBA by utilizing new device Dyanmic threshold MOSFET (DTMOS).

During the past few years demand for high-performanceand low-power digital systems has grown rapidly. Severalfactors have contributed to this fast growth. First, laptopand notebook computers, and personal communication systemshave gained popularity. Consequently, portable applicationsthat traditionally required a modest performance (such as wristwatches and calculators), are now dominated by devices that demand a very high performance. The demand for portabilityof these new systems limits their battery weight and size,placing a severe constraint on their power dissipation. Second,speed, density, and size of non-portable CMOS based systemshave increased considerably in recent years. Thus, powerconsumption that was not a concern in these systems, is nowbecoming a critical parameter.New devices and Gadgets such as; smart wearable's, long-term physiological monitoring, and handheld devices need to be small and lightweight. In addition to this long life battery is necessary for these devices.

DTMOShas proved to be effective for reducing the voltage supply of the circuit towards threshold voltage of the MOS Transistor Here significant features of the DTMOS have been discussed in detail and the DTMOS is utilized to implement LV structure of Voltage differencing buffer amplifier (VDBA). Also be verify the performance of the proposed structure, it was utilized in realizing application. The output of the proposed active device and its application was done through PSPICE simulation using 0.18μm CMOS technology.

Keywords

Analog circuit design, Active element, Low-voltage Low-power, DTMOS.

Electronics & Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

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ANIL KUMAR

Roll no: 2K16/VLS/04

M.TECH. (VLSI Design and Embedded System)

Department of Electronics & Communication Engineering

Delhi Technological University
Delhi – 110042

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LIST OF ABBREVIATIONS

Abbreviation	Full form
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
VLSI	Very Large Scale Integration
ABB	Analog building blocks
ASP	Analog Signal Processing
OP-AMP	Operational amplifiers
OTA	Operational Transconductance Amplifier
DO-OTA	Dual Output Operational Transconductance Amplifier
I/P O/P	Input-Output
IC	Integrated Circuit
LP	Low Power
LV	Low Voltage
CM	Current Mode
VM	Voltage Mode
MM	Mixed Mode
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
DXCCII	Dual X current conveyors
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Trans-conductance Amplifier
CDU	Current Differencing Unit
VDBA	Voltage Differencing Buffered Amplifier
ZC-VDTA	Z Copy Voltage Differencing Trans-conductance Amplifier
ZC-VDCC	Z Copy Voltage Differencing Current Conveyor
$\mathbf{A_v}$	Votage Gain

AC	Alternating Current
HPF	High Pass Filter
LPF	Low Pass Filter
APF	All Pass Filter
BPF	All Pass Filter
BRF	Band Reject Filter
B.W	Bandwidth
MISO	Multiple Input Single Output

CHAPTER-1

INTRODUCTION

1.1Background:

In electronics background low–power (LP) and low–voltage (LV)designing of integrated circuits for a variety of applications has gained significant attention in the industry. It is seen from the trend of the semiconductor industry that with the continuous downsizing of feature size of the transistors, the optimal supply voltage of CMOS integrated circuits has been dramatically declined because the emerging consumer market wants portable devices that needed to be light and must operate for a long duration of time with the small battery. When a MOS transistor size is downsized, the thickness of the oxide is reduced. Therefore, if a MOS transistor has a thinner gate oxide then to safeguard the transistor from a breakdown due to the higher electrical field across the gate oxide, i.e. to ensure its reliability, the supply voltage needed to be reduced [1–5]. Therefore, low–power (LP) and low–voltage (LV) analog circuits are receiving appreciable attention and are becoming the first choice in the electronic industry. Electronic systems that could monitor physiological parameters, or worn by people, or even provide some kind of treatment are made accomplishable by new advance LP LV circuit design [6].

1.2 Analog Circuit Design

In the mid of 1960s, complementary metal oxide semiconductor (CMOS) devices were introduced, initiating a revolution in the semiconductor manufacturing. Both analog and digital circuit on the same chip fabricated with low cost and with the possibility of placing so as to improve the overall performance and reduce the cost of casing made CMOS technology attractive. In the past two decades, CMOS technology has hastily embraced the field of integrated circuits(IC), provided that low-power dissipation, low-cost and high-performance solutions and increasing to lead the market. IC design can be divided into the two categories of digital and analog.

Digital signal processing is becoming increasingly extra powerful and important while advances in IC technology give compact, proficient implementation in silicon. Although many types of signal processing have in reality moved to digital field, analog circuits

have proved primarily compulsory in many of today's complex, high performance system so that naturally occurring signals are analog. Analog circuits act as a connection between the real world and digital systems.

Although in most modern electronic systems, signal processing and storage are performed in digital domain, ASP (Analog Signal Processing) is still required since the real world signal is represented in the analog form. As a result, most electronic equipments comprise analog processing circuitry that acts as interface between the digital world and the real world. However, analog signal is processed for variety of purposes, such as to remove unwanted noise, to correct distortion, to make the signal suitable for transmission or to extract certain meaningful information. The term ASP expresses plentiful of techniques that can be implemented to process analog signals including the theory and application of filtering, coding, transmitting, estimating, detecting, analyzing and reproducing analog signals

Operational amplifiers (OP-AMP) were the unavoided basic building blocks at the beginning of Analog circuit design. However, their performance such as limited gain-bandwidth (GBW) product problems, low slew rate at its output etc. leads the analog designer to look for other possibilities and other blocks. As a result other basic building blocks such as Operational transconductance Amplifiers (OTA), Current Conveyors (CC), Voltage Followers (VF), multiple-output second generation current conveyors (MO-CCII), third generation current conveyor (CCIII) , dual X current conveyors (DXCCII), etc. find most applicationsin the current-, voltage- or mixed-mode signal processing.

1.3Voltage Mode &Current Mode

Many years ago, analog blocks called active elements, have been appeared .These active blocks replaced the passive ones. Through active elements numerous of applications can be designed to process analog signal such as filters, oscillators, rectifiers and so forth. However, the term CM (Current Mode), VM (Voltage Mode) and MM (Mixed Mode) is inherent to active element term in the recent times, various novel alternative active elements for analog signal.

Representing the processing signal by voltage quantities is called VM, while the CM technique involves using current signals. Now let us try to answer first question about definitions of current mode and voltage circuits. However, any of the definitions reported in the literature are not accurate. For example, some authors write that in

voltage mode circuits the representation of information is done by the voltage at the specified nodes of the circuit. Whereas the representation of information in current mode circuits is done by current flowing in the branches of the circuit. This is not a unambiguous definition because of the reason that in every circuit every node has an incorporated voltage and every branch an incorporate current, and this is issue of definition that which ones represent signals and which ones does not.

Furthermore, CM signal processing may be defined as the processing of current signals in an environment where voltage signals are irrelevant in determining circuit performance. Moreover, the term CM has also been used to describe a system which has a current transfer function. Recently, there have been attempts at applying CM techniques to various kinds of electronic circuit design; this is motivated by the quest for higher frequency performance/ inherent signal bandwidths, greater linearity, wider dynamic range, trend to lower supply voltages, lower power consumption and simplicity in implementing operations over its counterpart 'VM'. However, it should be noted here that in CM elements the voltage values appear naturally at the impedance nodes. This value should be low to get rid of distorted signal; this can be achieved by making the node impedance as low as possible [3] and [4]. The aforementioned advantages of CM lead to be utilized in many attractive applications such as CM filters, oscillators and many others processing are introduced. Voltage mode (VM) analog signal processing techniques offer several advantages convenience in measuring nodal voltages, easily achievable high voltage gain, infinite input impedance of MOS transistors and low voltage circuit design[1].

A number of analog building blocks (ABB) such as Current Differencing Buffered Amplifier (CDBA) [3], Differential Difference Current Conveyor (DDCC) [4], Current Differencing Transconductance Amplifier (CDTA) [5], second generation current conveyor (CCII) [6] Differential Voltage Current Conveyor (DVCC) [7], Operational Transconductance Amplifiers (OTAs) [8] and many others as listed have been reported in literature to overcome the limitations Op-Amp based circuits. However, all these blocks process current signals only.

The voltage differencing buffered amplifier (VDBA) is an alternate ABB which not only is free from slew limitation but also processes the voltage signals. As the name suggests the VDBA uses voltage differencing input stage and provides a current output, given by the product of the differential input voltage and transconductance gain.

The transconductance being the bias current dependent enables electronic tuning of circuit parameters [9]. This results in simpler circuit design with lesser passive component count. It also provides a buffered voltage output which results in easily cascadable structures [10]. Additionally, since the VDBA provides both voltage and current outputs it further enhances the design flexibility [11]. Thus the VDBA has evolved as a promising choice for analog applications.

Among several VM active elements, VDBA (Voltage Differencing Buffered Amplifier) has attractive properties of current mode technology such as reduced power consumption, larger bandwidth, wider linearity and higher slew rate compared to OP-AMP [12].LV/LP electronics are highly desired in modern portable consumer electronics and battery-operated wearable and implantable biomedical devices. Although, there are performance differences between voltage mode and current circuits reported in papers. The reason for this being voltage-mode and current-mode circuits are ordinarily built with different design methodology. Voltage-mode circuits commonly employees greater loop gains in comparison to that of current-mode circuits, and current-mode circuits are usually having less complexity than the voltage-mode circuits. The inference from the whole discussion is that one must not use current-mode vs. voltage-mode distinction to divide all circuits in two categories.

The example for voltage mode and current mode circuit is shown in Fig1.1 and 1.2 respectively. As it is seen from figure that the circuit is same for both voltage mode and current mode the only difference is how we view this circuit.

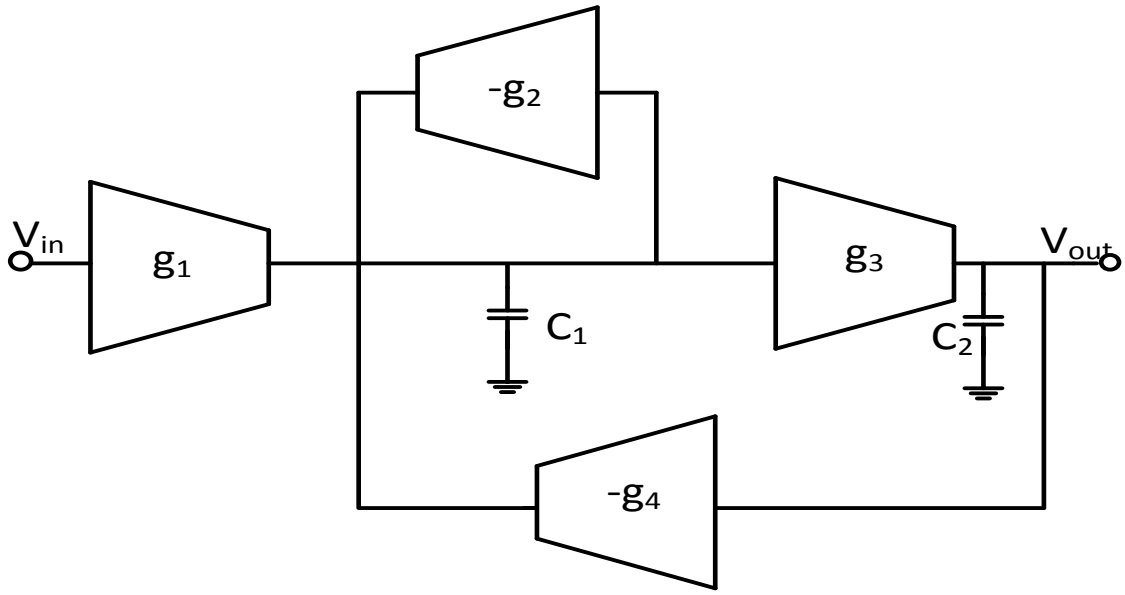

Fig 1.1 Example of Voltage mode(VM) Circuit

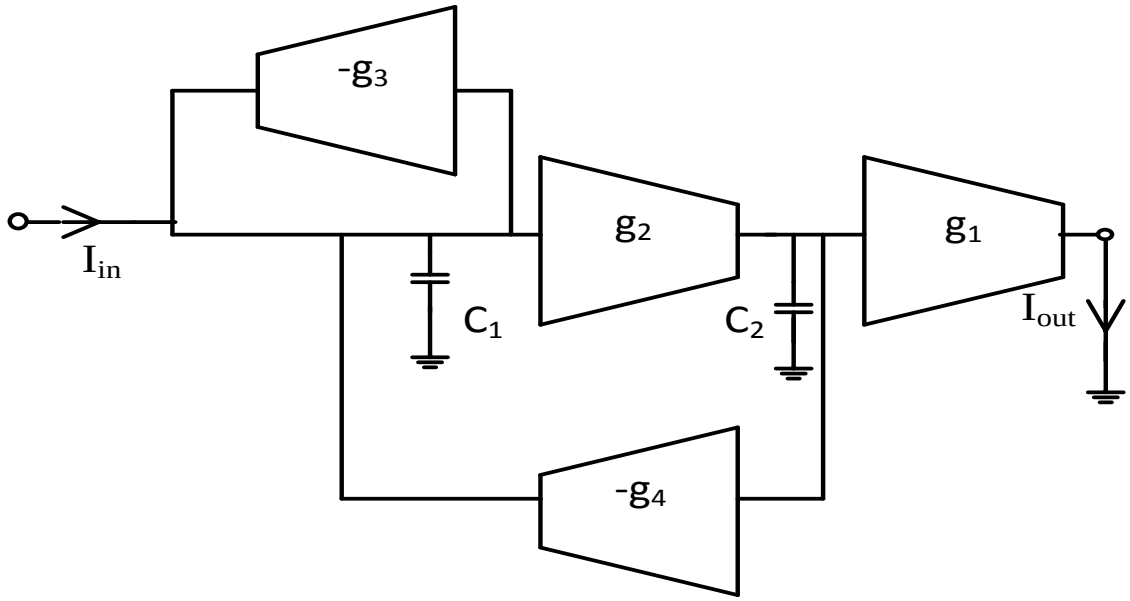

Fig1.2 Example of Current mode(CM) Circuit

1.3 Objective of thesis

In the few year ago, various number of active elements were designed and introduced in area of ASP. However still designers intend to expand new active elements or even advance the characteristics of the old ones to achieve better features than their counterparts. These better features can be described as higher frequency performance inherent signal bandwidths, greater linearity, wider dynamic range, lower supply voltages, lower power consumption and simplicity in designing. Therefore, the main objective of this thesis is to implement and improve various types of active elements .However, the aim of this thesis is to find new active elements or even improve the existing ones and applying those to new applications such as filters and oscillators. Factually, the main focus of this thesis is on LV LP (Low voltage Low Power) field for implementing analog circuits because this field has become essential in IC design in order to ensure reliable functioning of devices, to prevent overheating caused by increasing density of components per unit area and to prolong the battery lifetime in case of portable electronic equipment and implantable medical devices.

The field of LV LP CMOS technology has grown rapidly in recent years; it is an essential prerequisite particularly for portable electronic equipment and implantable medical devices due to its influence on battery lifetime. Recently, significant improvements in implementing circuits working in the LV LP area have been achieved,

but circuit designers face severe challenges when trying to improve or even maintain the circuit performance with reduced supply voltage.

In order to achieve an excellent performance of analog circuits, the input and output voltage swing capability should be extended, preferably to obtain rail to rail input and output operation capability. However, to achieve this, the threshold voltage of MOST needs to be reduced. Indeed, the threshold voltage does not scale down with reducing supply voltage of standard CMOS technologies; hence analog designers face many difficulties and challenges due to the limited voltage headroom.

Several MOST (MOSFET Transistor) design techniques exist for LV LP analog circuit design. However, only a few of them have found their way in modern designs, for instance, MOSTs operating in the sub threshold (weak inversion) region, level shifter techniques, selfcascode structures, BD (Bulk Driven) technique, FG (Floating Gate) approach , QFG (Quasi Floating Gate), DTMOS (Dynamic threshold MOSFET)

1.4 Outline Of Thesis

Chapter 1: In this chapter, basic voltage mode and current mode scenario in the analog circuits has been presented along with the salient features of the VM devices.

Chapter 2: In this chapter, literature on VDBA is presented and basic block which are used in designing of VDBA block are discuss in detail.

Chapter 3: Identification of the various problems related to power dissipation in analog circuits and solutions to minimize these power dissipation using DTMOS. And also new modified circuit of VDBA has been presented based on DTMOS.

Chapter 4: Application of the VDBA based on DTMOS as a VM Universal Biquad has been presented.

Chapter 5: Further work that can be done in the direction of the low power devices has been presented in this chapter.

1.5 Simulations

PSpice simulation using 0.18μm CMOS technology is used to verify the proposed circuits. PSpice demonstrates the performance of the CMOS analog building blocks Design kit of the TSMC 0.18μmCMOS process was used. Different simulation setups were used for different behavior analysis.

Due to the n-well process, all NMOS transistors bulk (B) terminals are shorted to the most negative power supply, namely V_{SS} and "B" terminals of all PMOS transistors are shorted to V_{DD} terminal. These connections can be seen in Fig. 1.1.

The supply voltage (V_{DD} =V_{SS}) were set to 0.9 V. Note that, three-terminal (drain, gate and source) MOSFET symbols are used in circuit schematics to avoid complexity.

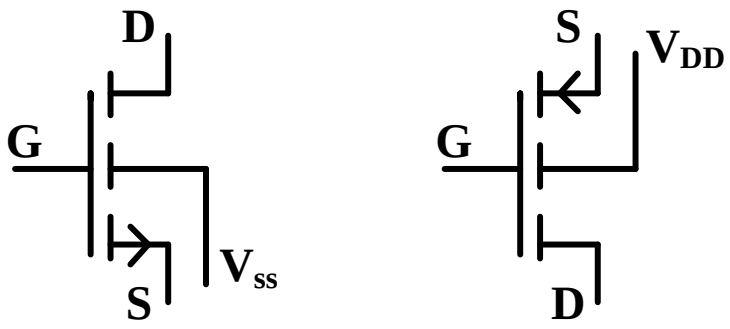

Fig.1.1 Bulk connections of Transistors (a) NMOS (b) PMOS

CHAPTER 2

Literature Survey& Building Blocks

2.1 Literature Survey:

As this study is focused on the design of the universal Analog Building Blocks (ABB) the Current Conveyor (CC) and Operational Transconductance Amplifier (OTA), the subsequent section discusses the state of the art recently proposed CCs, OTAs and their variants to emphasize the importance of the body techniques. A large number of circuit topologies have been proposed in the literature for analog signal processing such as active filters, oscillators etc. At the beginning, let's say until twenty years ago, the researchers were proposing this type circuit topologies without giving any realization circuit and application example.

In past few decades the VM analog signal processing has received considerable interest owing to the advantages offered by VM techniques which have been elaborated in chapter 1.This has resulted in emergence of various VM analog building blocks and VDBA is one among those.

In past years, operational amplifier which is an active building block played a prime role and a vastpublication comes into existence in the literature. But, op-amp based circuits have limited BW and SR results in drawback of performance. Therefore, Because of the merits of VM analog circuits as illustrated previously, the VM analog circuits are becoming popular. This results in emergence of various analog blocks.

From last few year, VM active building blocks like VDCC, Z-VDCC, VDBA, VDTA, Z-VDBA etc.

A literature review of such analog active block is presented in [7]. Additionally different types of active elements like DVCC, ECCII, DDCC, CCIII, DO-OTA and FTFN are presented in the literature [5–10].

In year 1999, a new building block: current differencing buffered amplifier (CDBA) was introduced by Acar and Ozoguz [11]. The CDBA can offer such as high-slew rate, wide bandwidth and simple implementation [12]. The CDBA can be viewed as cascade of CDU and buffer amplifier. In which the first unit provides the difference of current at one output Z, and second stage i.e. buffer stage provide voltage at W terminal which is same as the voltage developed at Z terminal.

The VDBA can be implemented using Fully Balanced Voltage Differencing Buffered Amplifier (FB-VDBA) was firstly published by Biolek and others in [7].

VDBA input point is consisted of the differential OTA input and the voltage buffer is associated with current OTA output. Furthermore, the differential input voltage of OTA generates output current known as voltage controlled current source (VCCS).

Generally, a buffer amplifier presents electrical impedance changed over through the circuits. the transconductance of the amplifier is controlled using the multi input current that is generally exists in such VDBA filter circuits. The typical operational amplifier is considered analogous to the Operational Transconductance Amplifier OTA because both have high impedance differential input stage, and the last can be used to create the negative feedback.

The block diagram of VDBA and internal circuit given in fig 2.1 and 2.2.

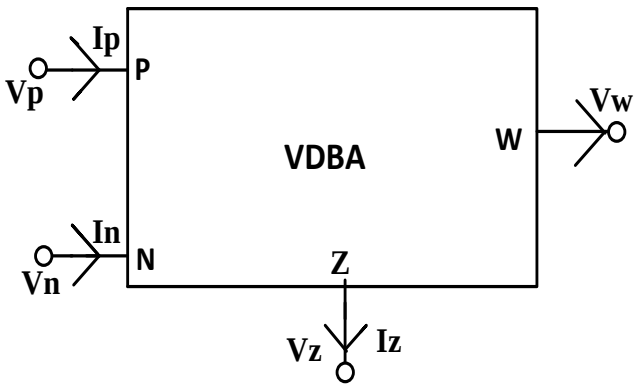

Fig. 2.1 The block diagram of VDBA

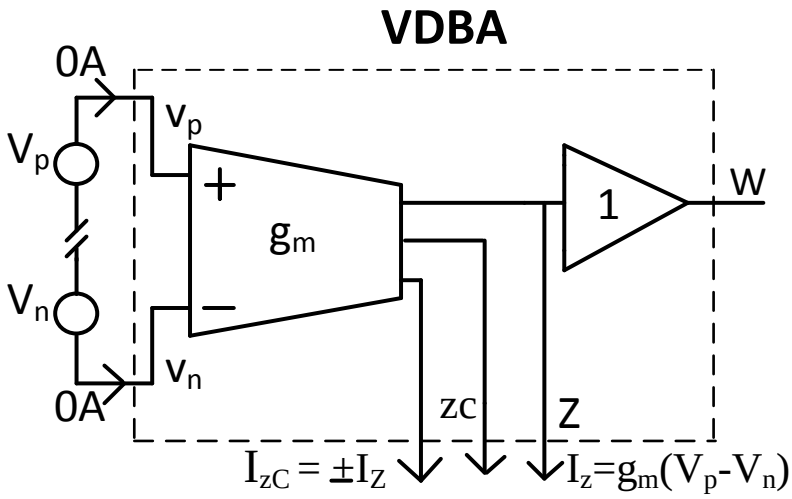

Fig. 2.2 -The internal diagram of VDBA

Basically VDBA is originated from the operational amplifier (OP-AMP), which is basically a voltage differencing unit. Operational amplifiers are an integral part of many analog and mixed signal systems. The op-amp is one type of differential amplifier. Other types of differential amplifier include the fully differential amplifier (similar to the op-amp, but with two outputs), the instrumentation amplifier (usually built from three op-amps), the isolation amplifier (similar to the instrumentation amplifier, but with tolerance to common-mode voltages.

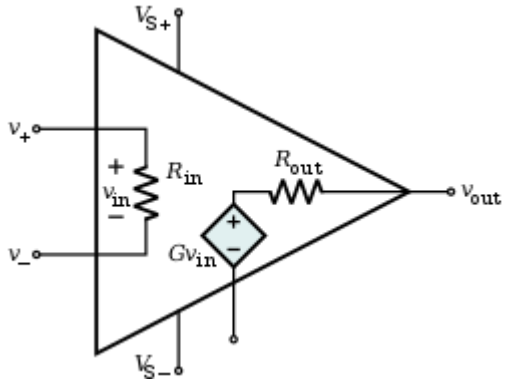

Fig 2.4 Equivalent circuit of op-amp

An ideal op-amp is usually considered to have the following characteristics:

- Infinite open-loop gain G = v_{out} / v_{in}
- Infinite input impedance R_{in}, and so zero input current
- Zero input offset voltage
- Infinite output voltage range
- Infinite bandwidth with zero phase shift and infinite slew rate
- Zero output impedance R_{out}
- Zero noise
- Infinite common-mode rejection ratio (CMRR)
- Infinite power supply rejection ratio.

2.2 FUNDAMENTAL BUILDING BLOCKS:

- Operational Transconductance Amplifier (OTA)
- Voltage Buffer

2.2.1 Operational Transconductance Amplifier (OTA)

An Ideal Operational transconductance amplifier (OTA) is a voltage controlled current source with constant transconductance and infinite input/output impedances, that takes the differential voltage as input and provide current as the output, on the other hand conventional Op-Amp, which is a voltage-controlled voltage source. However, they become inaccurate when a practical OTA at high frequency or with large input signal is concerned. OTA is a trans-conductors type device, which means that the input voltage controls an output current by controlling the device transconductance.

More specifically, the term "operational" comes from the fact that it takes the difference of two voltages as the input for the current conversion. The schematic symbol and equivalent circuit of the ideal OTA. The output current is related to the differential input voltage as:

$$\mathbf{I_{out} = (V_{p+} - V_{n-})g_m} \qquad \mathbf{(2.1)}$$

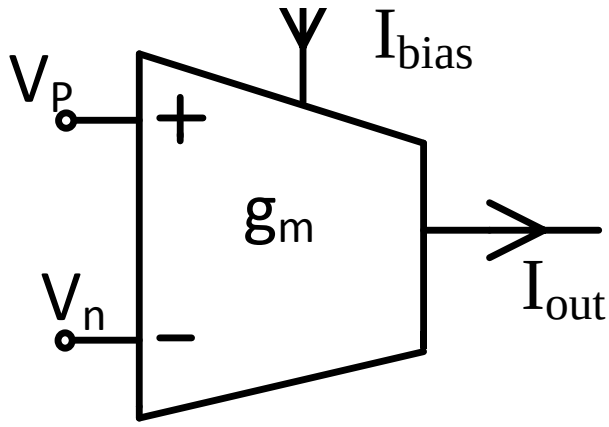

Fig 2.3-Schematic symbol of OTA

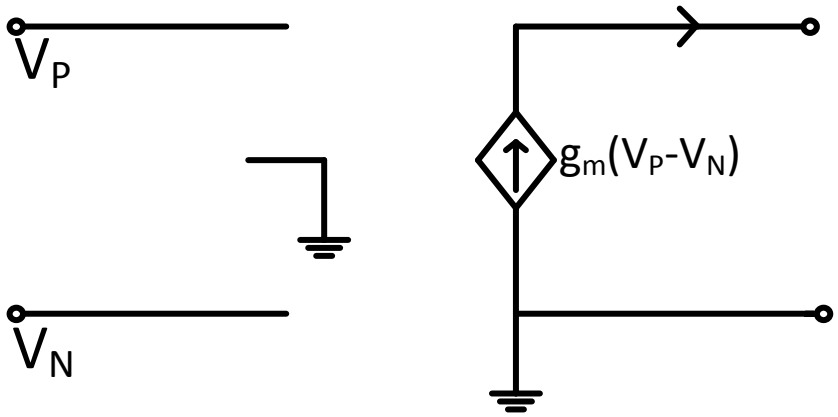

Fig 2.4- Ideal equivalent circuit of OTA

2.2.2 Characteristics of OTA

The ideal OTA is a voltage-controlled current source (VCCS), with infinite input and output impedances and frequency independent transconductance. OTA has two attractive features.

1-Changing the external dc bias current or voltage can control its transconductance

2-It can work at high frequencies.

- Input impedance = Infinite
- Output impedance =Infinite
- Bandwidth =Infinite

$I_o = 0$ when $V_{in+} = V_{in-}$ (Perfect balance)

Transconcutance (g_m) finite and controlled by the bias current I_{bias}.

2.2.3 Circuit of Balanced OTA

It basically consists of three kinds of sub-circuit:

1. Differential pair
2. Current source
3. Current mirrors

The internal circuit of OTA consists of a differential input stage while the remaining part of the OTA is composed of current mirrors. The geometry of these mirrors is kept such that the current gain is unity. Thus the output current is precisely defined by the differential input amplifier.

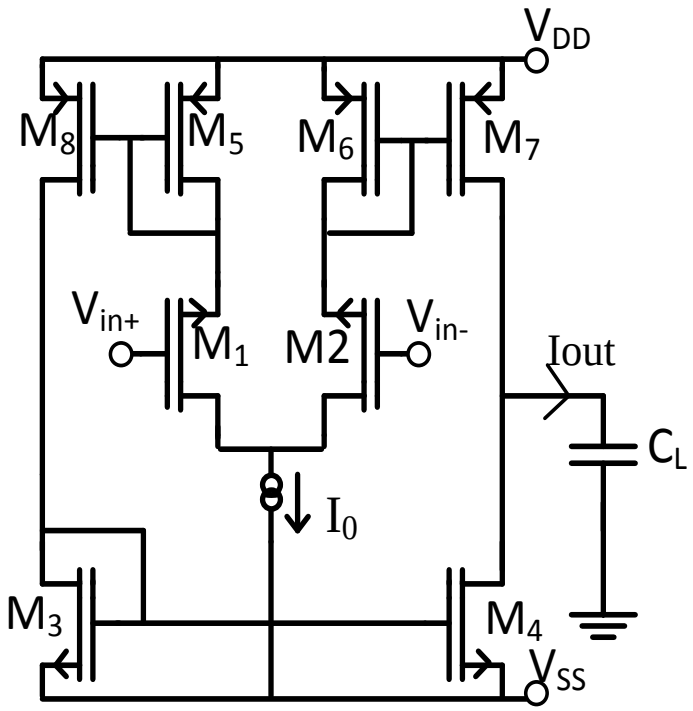

Fig 2.5 Balance OTA circuit

Table no. 2.1 Transistor ratios of OTA

Transistor	W(µm)	L(µm)
M_1-M_2	16	0.25
M_3-M_4	3	0.25
M_5-M_6-M_7	5	0.25
M_8	5	0.25

2.3 BUFFER AMPLIFIER

A buffer amplifier (sometimes simply called a buffer) is one that provides electrical impedance transformation from one circuit to another, with the aim of preventing the signal source from being affected by whatever voltage (or currents, for a voltage buffer) that the load may produce.

Buffers are basically two types:

1-Voltage Buffer

2- Current Buffer.

2.3.1 Voltage Buffer

A voltage buffer amplifier is used to transfer a voltage from a first circuit, having a high output impedance level, to a second circuit with a low input impedance level. The interposed buffer amplifier prevents the second circuit from loading the first circuit unacceptably and interfering with its desired operation. In the ideal voltage buffer in the diagram, the input resistance is infinite; the output resistance zero (output impedance of an ideal voltage source is zero).

Other properties of the ideal buffer are: perfect linearity, regardless of signal amplitudes; and instant output response, regardless of the speed of the input signal.

If the voltage is transferred unchanged (the voltage gain A_v is 1), the amplifier is a unity gain buffer; also known as a voltage follower because the output voltage follows or tracks the input voltage. Although the voltage gain of a voltage buffer amplifier may be (approximately) unity, it usually provides considerable current gain and thus power gain. However, it is commonplace to say that it has a gain of 1 (or the equivalent 0 dB), referring to the voltage gain.

As an example, consider a Thevenin source (voltage V_A series resistance R_A) driving a resistor load R_L. Because of voltage division (also referred to as "loading") the voltage across the load is only $V_A R_L / (R_L + R_A)$. However, if the Thévenin source drives a unity gain buffer such as that in Figure 1 (top, with unity gain), the voltage input to the amplifier is V_A, and with no voltage division because the amplifier input resistance is infinite. At the output the dependent voltage source delivers voltage $A_v V_A = V_A$ to the load, again without voltage division because the output resistance of the buffer is zero.

A Thévenin equivalent circuit of the combined original Thévenin source and the buffer is an ideal voltage source V_A with zero Thévenin resistance.

A buffer amplifier provides that impedance transformation from one stage to another. A voltage buffer is used to transfer a voltage from a first circuit, have a high output impedance level, to a second circuit with a low input impedance level. Analog voltage buffers find use in many analog applications such as current conveyors, current feedback amplifiers and analog filter realization. An ideal voltage buffer is shown in Fig. 2.6.As it can be seen the figure, the ideal voltage buffer have infinite input resistance and zero output resistance.

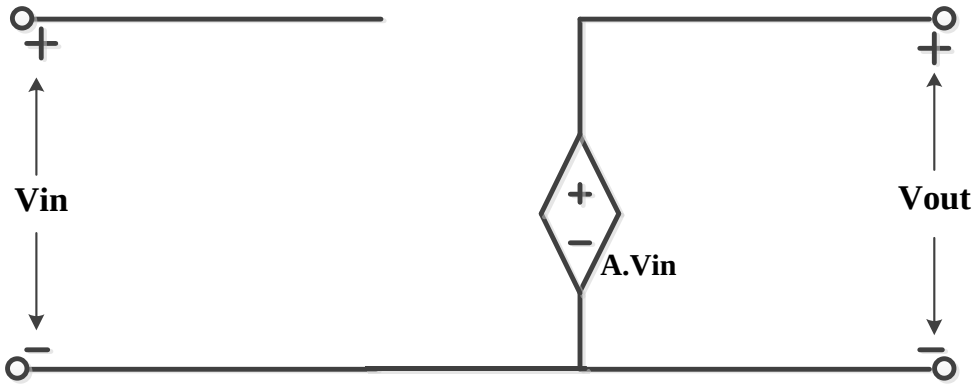

Fig 2.6-Equivalent circuit of ideal Voltage buffer

The Buffer amplifier can be implemented using OPAMP as shown in Fig 2.7.In this buffer output directly is connected to inverting terminal i/p of op-amp.

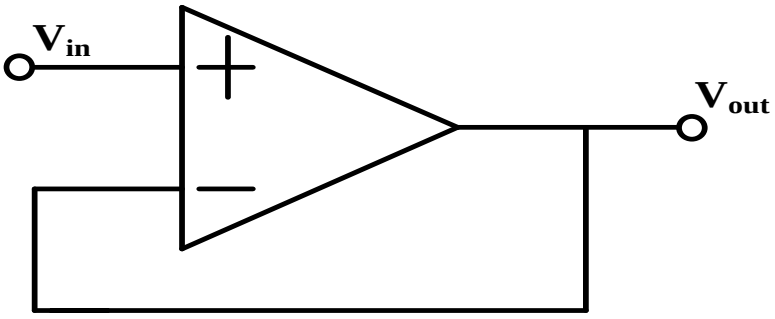

Fig.2.7- op-amp based Voltage follower

2.3.2 CMOS realization of voltage buffer:

CMOS structure was used in Fig. 2.8 The voltage buffer consists of a differential amplifier (M1-M4) and a feedback transistor M5 from output the negative input. This feedback transistor guaranties low output impedance. Transistors sizes are given in Table 3.1.

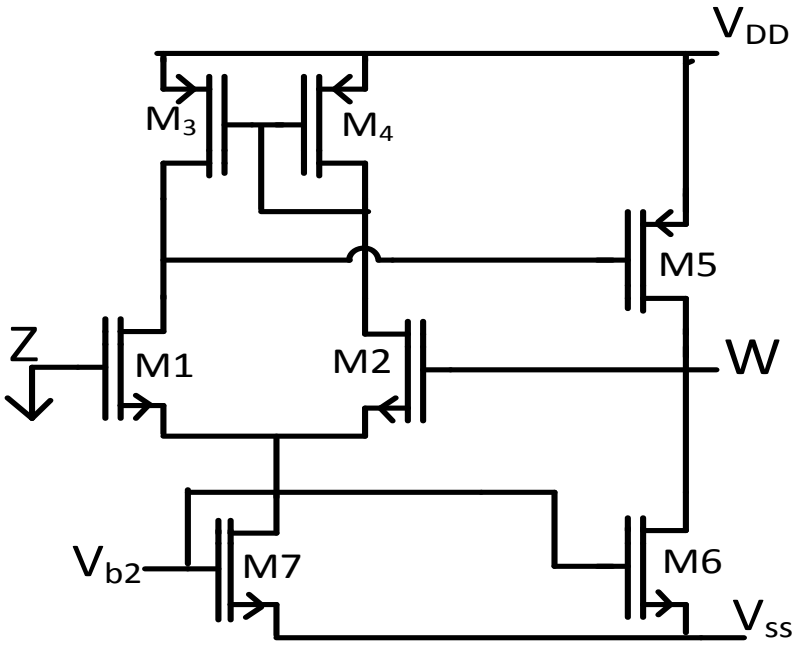

Fig.2.8 CMOS based Voltage follower

Table no. 2.2 Transistor ratios of Buffer

Transistor	W(µm)	L(µm)
M_1,M_2, M_6,M_7	7	0.35
M_3,M_4,M_5	14	0.35

2.4 Summary:

In the last, it can be summarized that this chapter presents the relavent literature survey of analog buildings block VDBA. After that discuss about OTA and buffer circuit in the detail . These are basic part of internal structure of VDBA block.

CHAPTER-3
CMOS VDBA & DTMOS based VDBA realization

3.1Introduction

OPAMP and VDBA are related to each other in their characteristics especially the high input and the low output impedances that are realized by both of them. In the few year ago operational amplifier which is an active building block played a prime role and a vast publication comes into existence in the literature. But, op-amp based circuits have limited Bandwidth and slew rate results in drawback of performance. Therefore, because of the merits of voltage mode analog circuits, the voltage mode analog circuits are becoming popular. This results in emergence of various analog blocks .Among several VM active elements, VDBA (Voltage Differencing Buffered Amplifier) has attractive properties of current mode technology such as reduced power consumption, larger bandwidth, wider linearity and higher slew rate compared to OP-AMP [12] VDBA circuit is alternative to CDBA [7] .The main difference is between them is that the voltage is set as input to VDBA, whereas, the current is set as input to CDBA. In this chapter we will discuss a new voltage mode active building block named as voltage differencing buffer amplifier (VDBA).

3.2 VDBA Realization

3.2.1 Ideal VDBA

As voltage-mode circuits are becoming popular with advancement of time and because of their applications, a new active block was found in, and this new block is called voltage differencing buffered amplifier (VDBA) .The circuit symbol of VDBA is shown in Fig. 3.1, A voltage differencing buffered amplifier (VDBA) is a multi-terminal active block having two input port and two output port .Where P and N are the input terminals and Z and W are the output ones. Hence, Z is the current output terminal and current through Z terminal follows the difference of the voltages at P and N terminals by transconductances g_m. Voltage of W terminal follows the voltage of Z one. The electronically tunable VDBA has advantage over the conventional one by possible controlling of g_m through the bias current I_b.

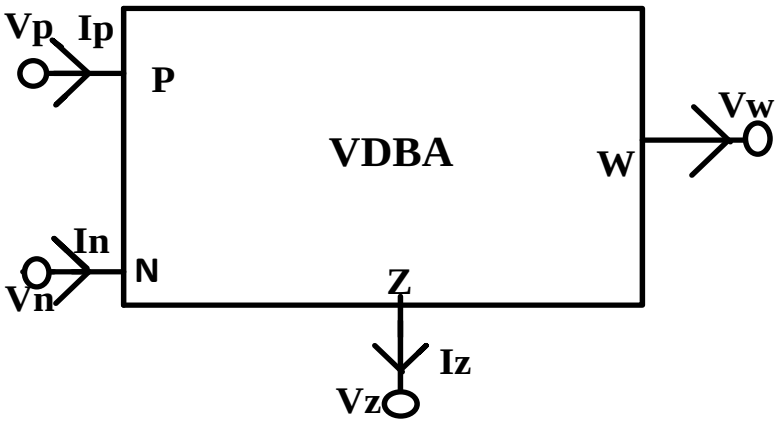

Fig.3.1 VDBA block

The input voltage of the circuit is converted to current at side (z) using voltage drop and Transconductance gain. New reflection happens at side (z) to another impedance zone identified as side (w). According to the comparison between VDBA and OP-AMP [8,9]at current mode sides, VDBA gives some properties such as good linearity, less power consumption, high slew rate, and larger bandwidth. The point that states that VDBA contains low output impedance which can be considered as the main difference between VDBA and OTA, makes it more adaptable than voltage circuit due to the effect of the loading that is typically faded out. The circuit works without using exterior resistance, therefore VDBA remains making use of the transconductance characteristics specially, controlling the value of the transconductance electronically.

Equivalent internal circuit diagram of VDBA is shown in fig. 3.2.

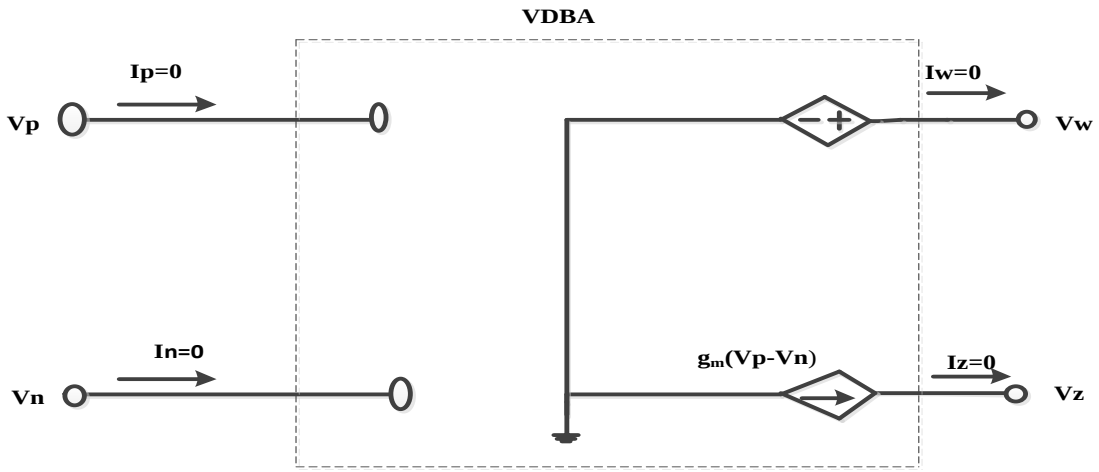

Fig.-3.2 Equivalent circuit of VDBA

The ideal characteristics of block VDBA is defined by the following hybrid matrix.

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_W \\ I_W \end{bmatrix} \quad \textbf{(3.1)}$$

3.2.2 Non ideal VDBA:

Fig. 2.63 shows the non ideal model of VDBA, where Z_P, Z_N, Z_Z and Z_W denote the parasitic impedances of P, N, Z and W terminals, respectively, and β is the voltage transfer between the W and Z terminals of the VDBA.

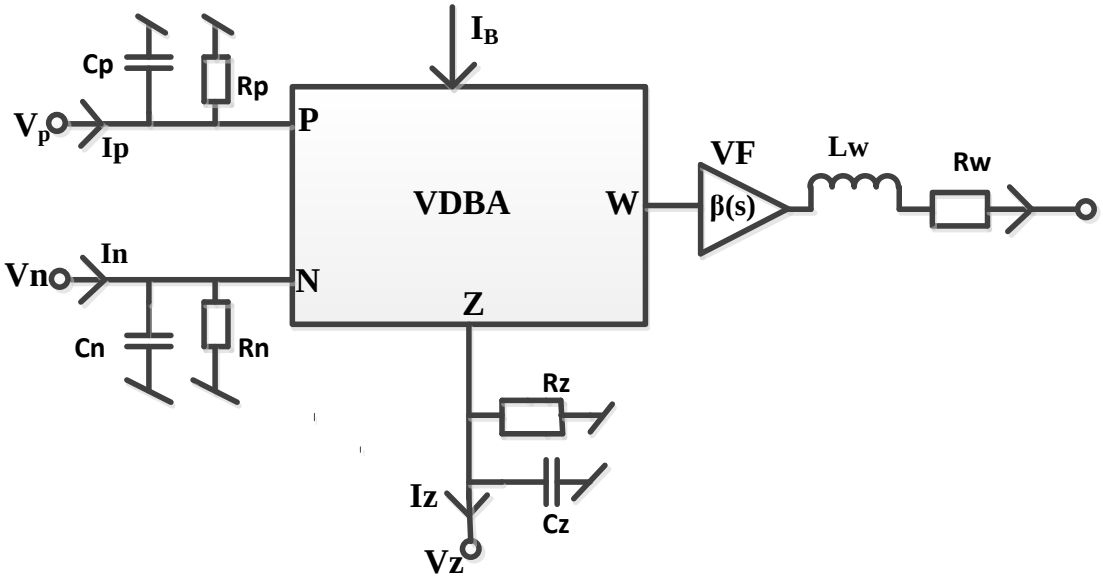

Fig. 3.3- Circuit symbol of non-ideal VDBA

Taking the non idealities and the influence of parasitic impedances of the VDBA into account, the relationship of the terminal voltages and currents given with Eq. (3.2) can be rewritten as:

$$\begin{bmatrix} I_p \\ I_p \\ I_p \\ I_p \end{bmatrix} = \begin{bmatrix} 1/Z_P & 0 & 0 & 0 \\ 0 & 1/Z_N & 0 & 0 \\ g_m(s) & -g_m(s) & 1/Z_Z & 0 \\ 0 & 0 & \beta(s)Z_w & \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_W \end{bmatrix} \quad \textbf{(3.2)}$$

The resistive behavior at lower frequencies and capacitive behavior at higher frequencies are the attributes of each P, N and Z terminals. Therefore, the total P, N and Z terminal parasitic impedances consist of a parallel combination of a parasitic resistance $R_{P,N,Z}$ and a

capacitance $C_{P,N,Z}$ respectively. The value of each parasitic capacitance $C_{P,N,Z}$ can be determined by the formula.

$$\mathbf{Cp,n,z} = \frac{\mathbf{1}}{\mathbf{2\pi f_{p,n,z,-3db}\ R_{p,n,z}}} \quad \textbf{(3.3)}$$

Where$f_{p,n,z,,-3db}$ denotes the 3 db cutoff frequency of $Z_{p,n,z}$ respectively.

The resistive behavior at lower frequencies and an inductive behavior at higher frequencies are the attributes of the output voltage terminal W. The total W terminal parasitic impedance Z_W then consists of a serial combination of parasitic resistance R_W and parasitic inductance L_W.

The value of L_W can be determined by –

$$\mathbf{L_W} = \frac{\mathbf{R_W}}{\mathbf{2\pi f_{w,+3db}}} \quad \textbf{(3.4)}$$

Where$f_{w,+3db}$ denotes the +3 dB cutoff frequency of Z_W.

The transconductance g_m can be assumed as:

$$\boldsymbol{g_m(S)} = \frac{\boldsymbol{g_{m0}}}{\mathbf{1}+\frac{\boldsymbol{s}}{\boldsymbol{\omega_{g_m}}}} \quad \textbf{(3.5)}$$

Where g_{mo} the value of OTA transconductance at low frequencies, and ω represents its corresponding pole frequency.

The voltage transfer of the VDBA is given by β(s):

$$\boldsymbol{\beta(s)} = \frac{\boldsymbol{\beta_0}}{\mathbf{1}+\frac{\boldsymbol{s}}{\boldsymbol{\omega_\beta}}} \quad \textbf{(3.6)}$$

Where $\beta_0$the value of the voltage is transfer at low frequencies, and ω_β represents the corresponding pole frequencies.

It's important to state that the non ideal properties of VDBA having some discrepancies from the ideal one because of abovementioned parasitic impedance influences. To deal with of this problem the internal implementation of the circuit should be designed in a good manner.

3.3CMOS Realization of VDBA:

VDBA can also be realized using CMOS devices. As discussed above VDBA is composed to two units namely voltage differencing unit (VDU) and other one is buffer amplifier. As discussed earlier VDBA is composed of two units namely Voltage differencing unit (VDU) and another one is buffer amplifier. It is a four terminal device out of which two terminals are input terminal and two are output terminal. The two input terminals P and N takes voltage as input to it and provides output as difference of two voltage at Z terminal and also provide a voltage at W terminal which developed across the load which is connected at Z terminal. The CMOS implementation of VDBA is shown in Fig 3.4.

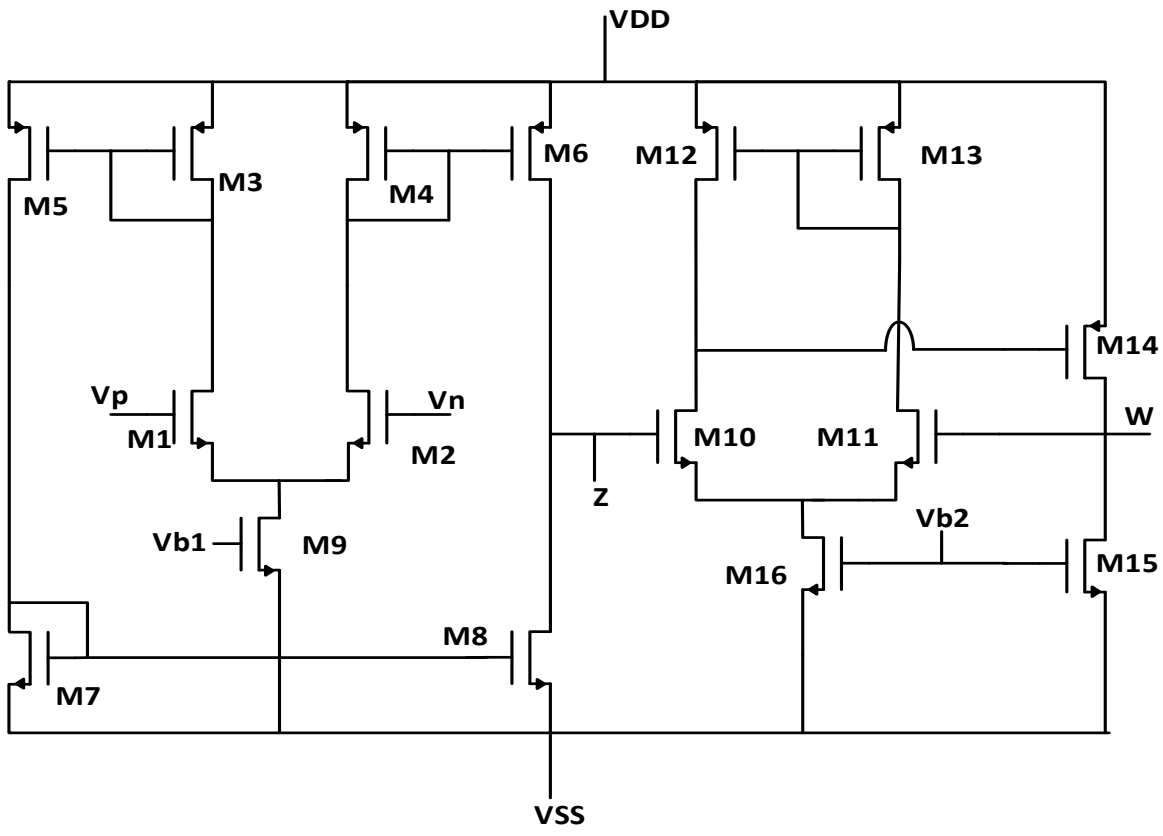

Fig 3.4CMOS Implementation of VDBA

The W/L ratios of VDBA is shown in table 3.1.

Table 3.1: W/L ratios of VDBA

Transistors	W(µm)	L(µm)
M_1-M_4, M_{10}, M_{11}, M_1, M_{16}	7	0.35
M_5, M_6	21	0.7
M_7, M_8	7	0.7
M_9	3.5	0.7
M_{12}- M_{14}	14	0.35

3.4 VDBA Characterization:

The SPICE schematic used for VDBA characterization is shown in Fig 2.7. The value of Vb1, Vb2,is -0.44V, -0.9 respectively. The supply voltage used for the device is ±1.5V. The circuit is simulated using 0.18µm technology node. The main DC and AC characteristics of VDBA, such as plots of I_Z against V_P, plots of V_Z against V_W, frequency responses of I_Z/V_P and V_W/V_Z are obtained from LTSPICE simulations.

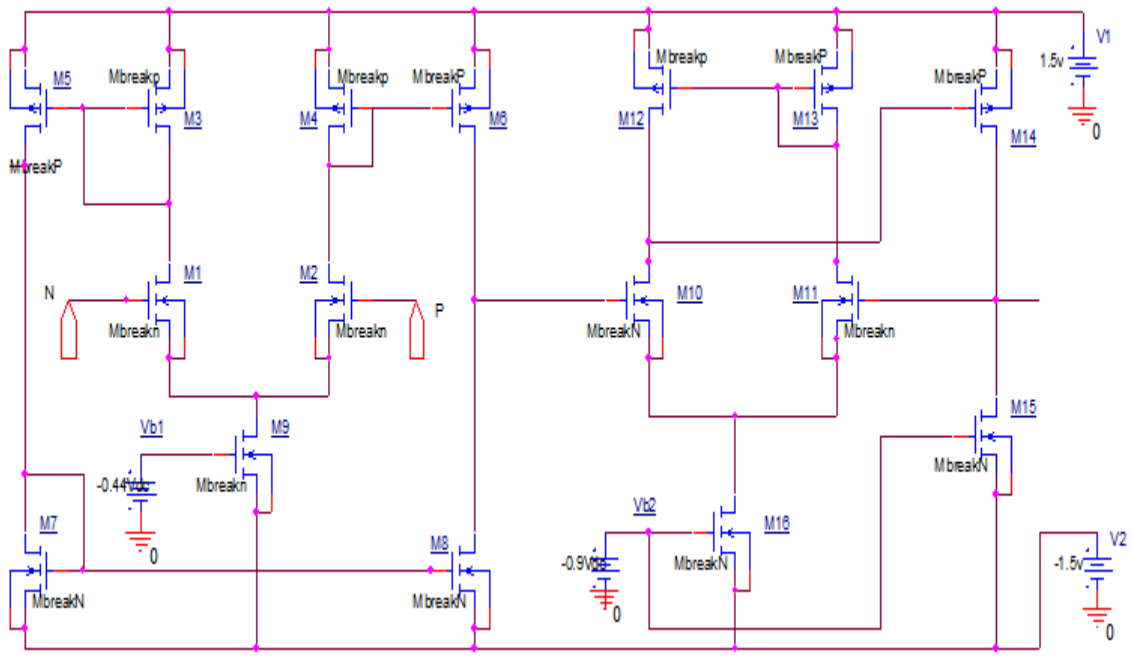

Fig. 3.5 Schematic of CMOS Based VDBA

3.4.1 DC transfer characteristics at input stage

The DC transfer characteristic of I_Z against V_P for VDBA is shown in Fig. 4.6 that is obtained when one input (terminal N) is grounded, and I_z against V_n for VDBA is obtained when one input(terminal P) is grounded.

The linearity extends in the range ±0.4Vwhile a non-linear behavior is observed elsewhere. The operation of OTA stage of the proposed VDBA, depicting I_Z against V_p and V_n for different supply voltages.

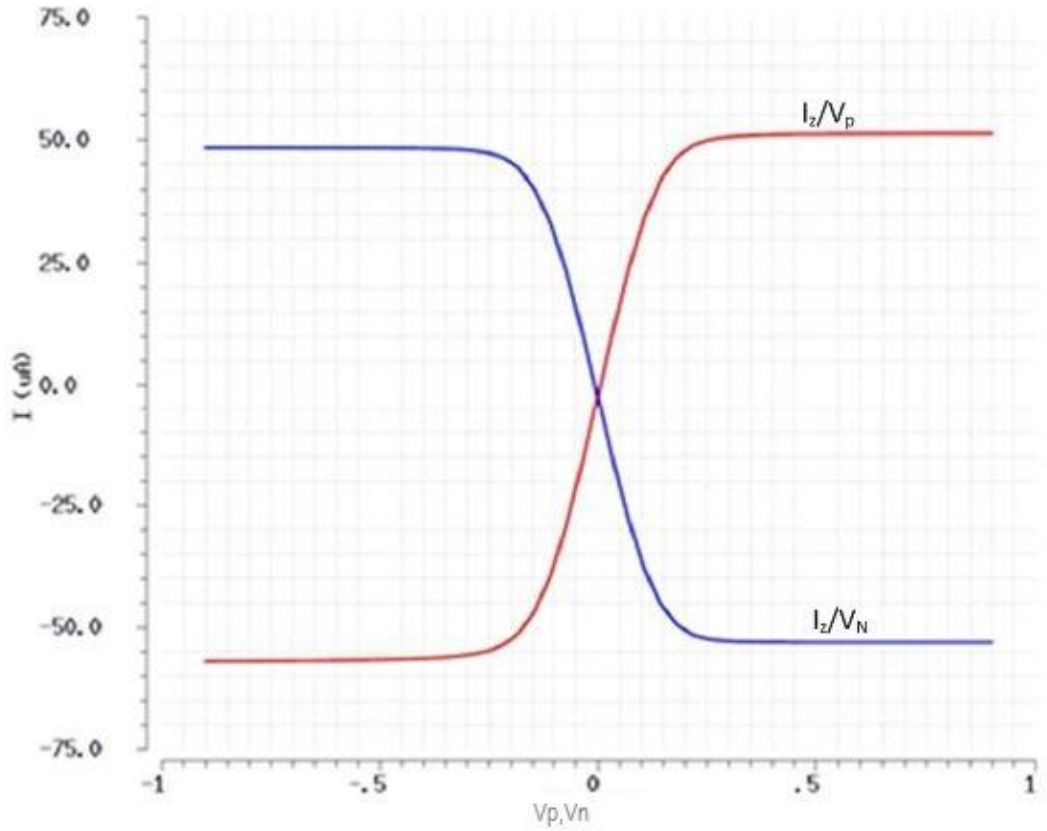

Fig 3.6 DC transfer characteristic I_Z vs V_P and V_N

The operation of OTA stage of the proposed VDBA, depicting I_Z against V_P for different supply voltages .Though the swing for which the OTA justifies its operation decreases by reducing the power supply; approximately±350μA at supply voltage of ±1.45V, ±300μA at supply voltage of ±1.35V, ±250μA at supply voltage of ±1.25Vand ±200μA at supply voltage of ±1.15V.

3.4.2Output impedance at terminal Z

For measurement of impedance at o/p terminal Z ,the I / P terminals are kept grounded and then a test AC input signal is applied to the terminal at which the impedance is to be measured. After that the ratio of voltage and current of this test signal is plotted w.r.t to frequency. From the Fig.3.7, the impedances seen through and terminals are found out to be small as it is required to be, theoretically.

The values of these impedances measured using point A from their corresponding frequency responses are as follows:

Z_Z =111.721K ohm

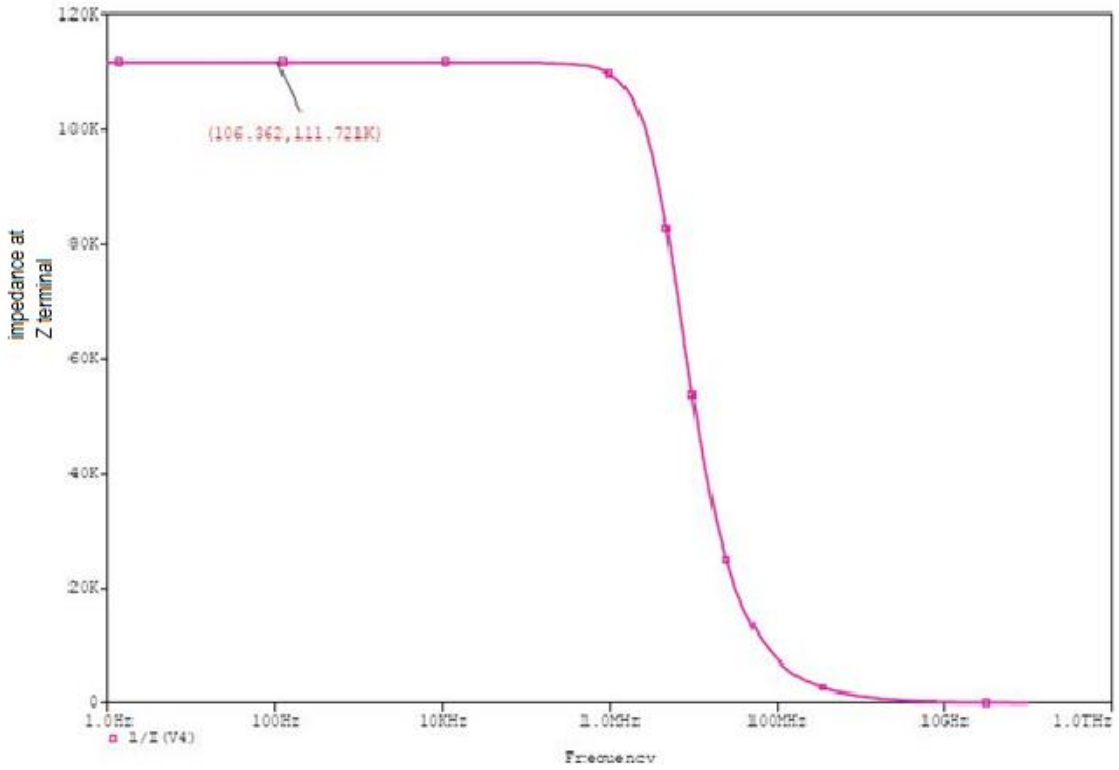

Fig 3.7 Impedance seen from Z terminal of VDBA

3.4.3 Voltage transfer Characteristics of buffer

The voltage transfer characteristic can be plotted by connecting DC source at input of buffer stage and then by doing DC sweep of that source and measuring voltage the output stage. It is shown in Fig 3.8.The tracking behavior as shown in Fig 3.9 shows that in buffer stage output voltage follows the input voltage between -0.35V to 0.65V.

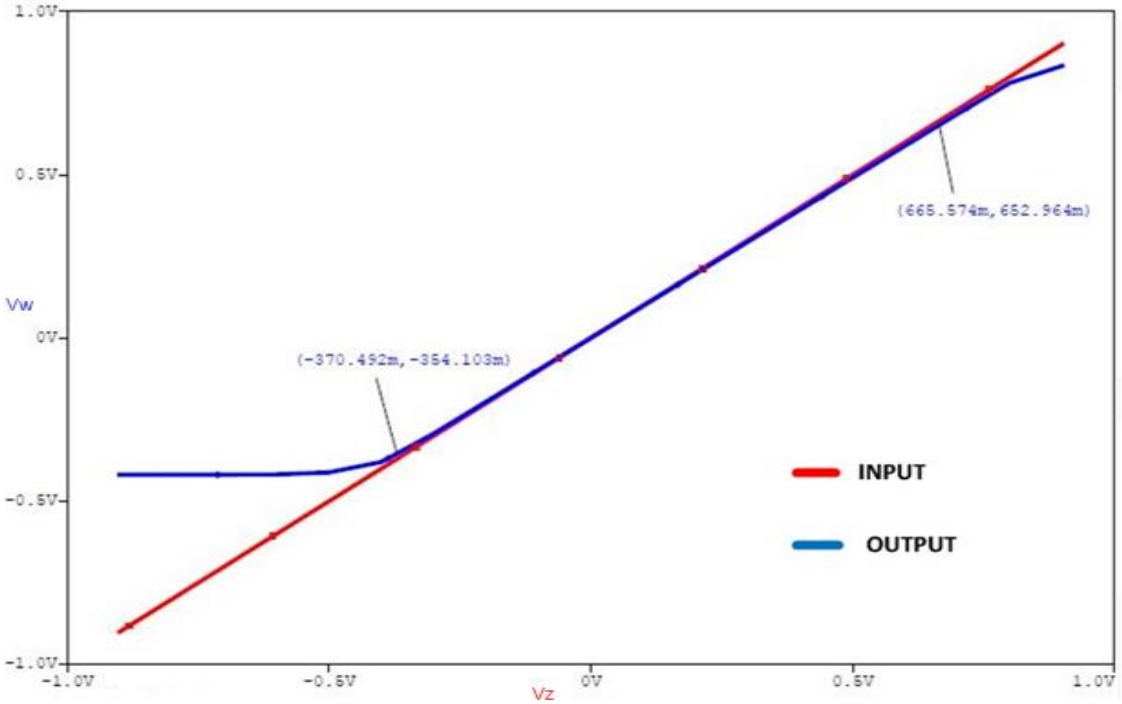

Fig 3.8 Voltage Transfer Characteristics of Buffer stage of VDBA

There is some error in input and output voltage levels in linear range which is known as tracking error. The Plot for tracking error is shown in Fig 3.9 which obtained by subtracting input and output voltage. The range in which tracking error is Zero denotes therange in which ouput voltage follows the input voltage.

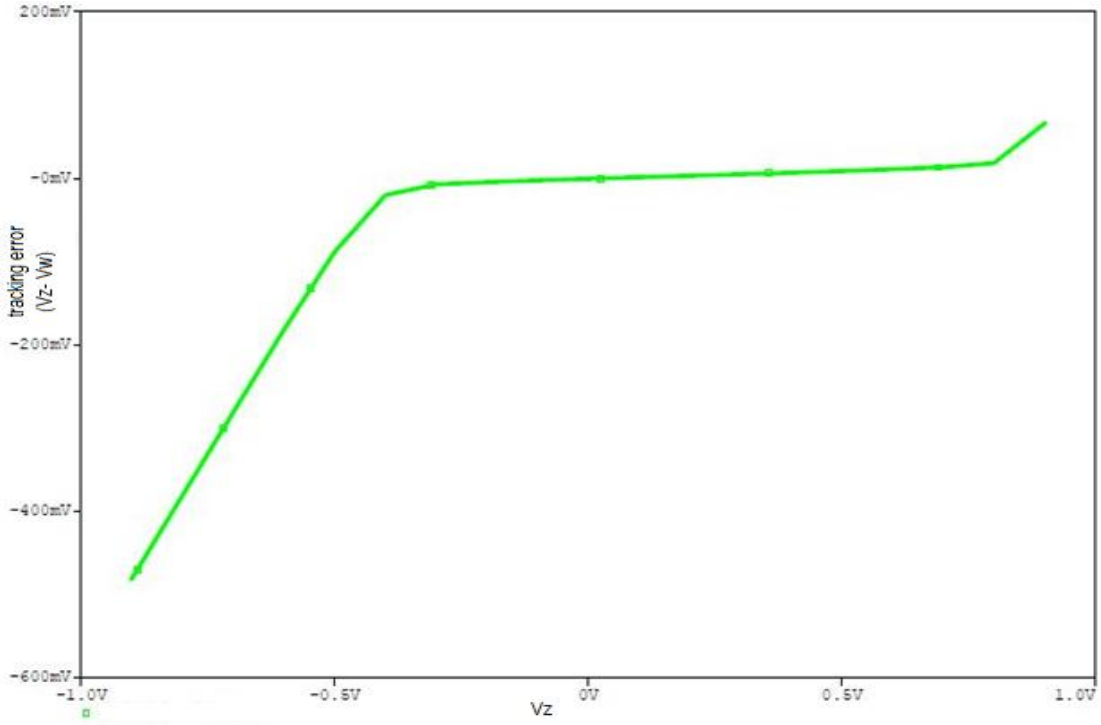

Fig 3.9Tracking error of Buffer stage of VDBA

3.4.4 AC Transfer characteristics of output stage of VDBA

The AC transfer characteristic can be plotted by connecting AC source at input of buffer stage and connected output voltage is taken at the output. After that taken the ouput to input voltage transfer ratio. It is shown in fig 3.10, and it's value is very close to unity which is desired value for ideal buffer stage.

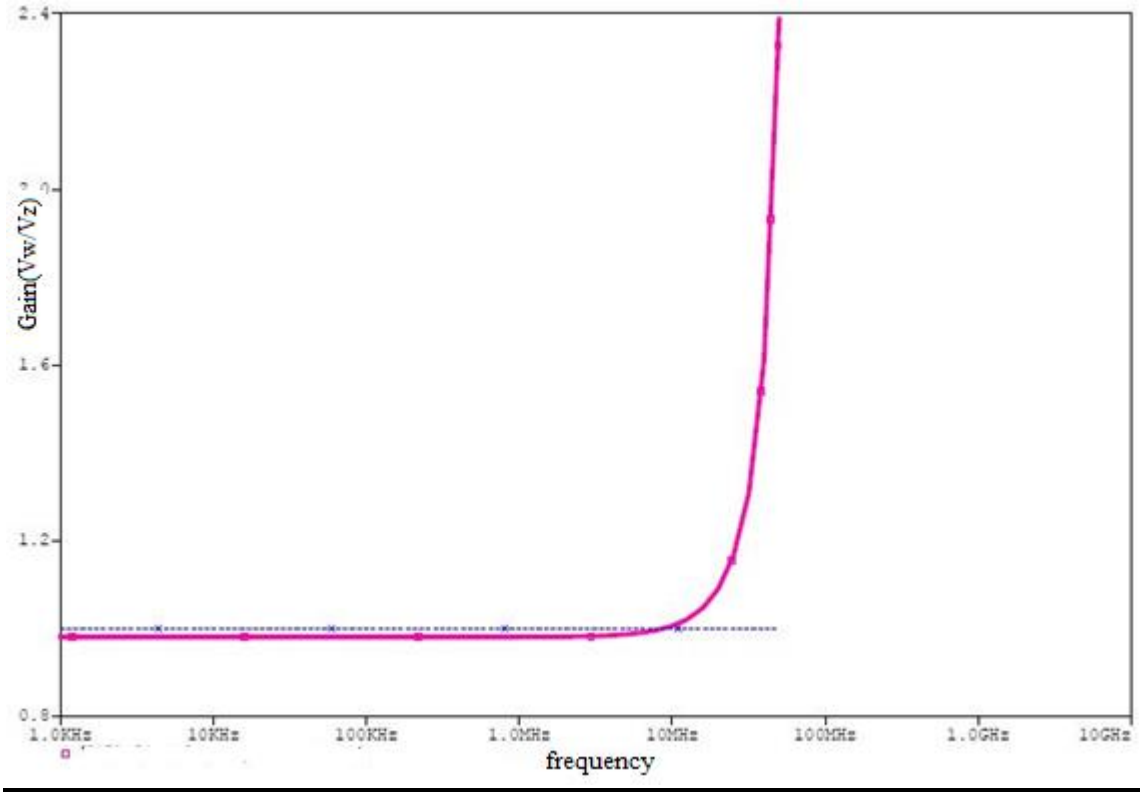

fig 3.10-The AC transfer characteristics of output stage of VDBA

3.4.5 Output Impedance at W terminal:

Measure of impedance at o/p terminal W, the i/p terminal of buffer amplifier Z is kept grounded and then a AC test input signal is applied to the terminal at which the impedance is to be measured. After that the ratio of voltage and current of this test signal is plotted w.r.t. to frequency. From the Fig. 3.11, the impedances seen through and terminals are found out to be small as it is required to be, theoretically.

The values of these impedances measured using point A from their corresponding frequency responses are as follows :

$$Z_w = 96.8\Omega$$

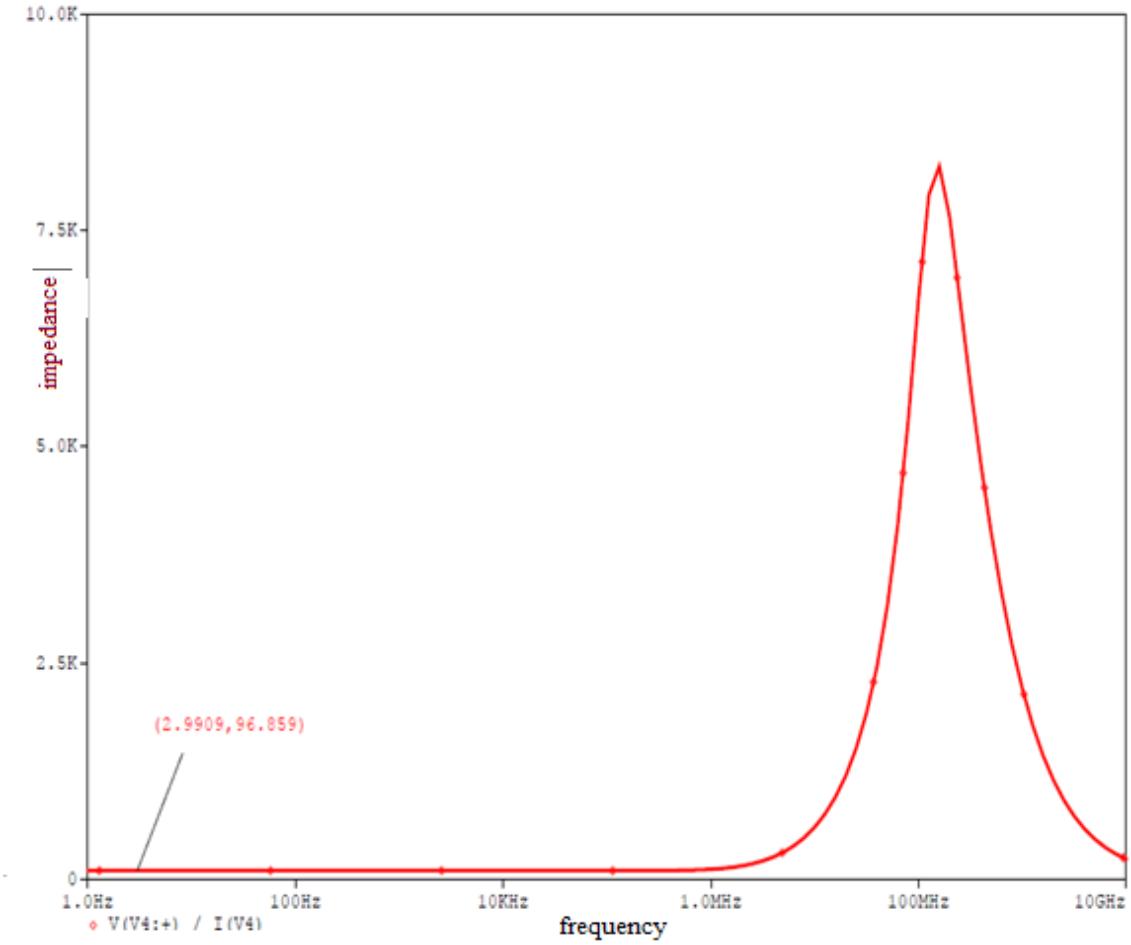

Fig. 3.11- Impedance seen from W terminal of VDBA

3.4.6Frequency response at input stage

Frequency response of input stage is measure by connecting a ac source to the i/p terminal of any P or N terminal and other end terminal grounded and connect a register at output and measure the current at the output stage of z terminal. Frequency response of i/p stage shown as fig. 3.12.

Measure current value is I =0.916 mA

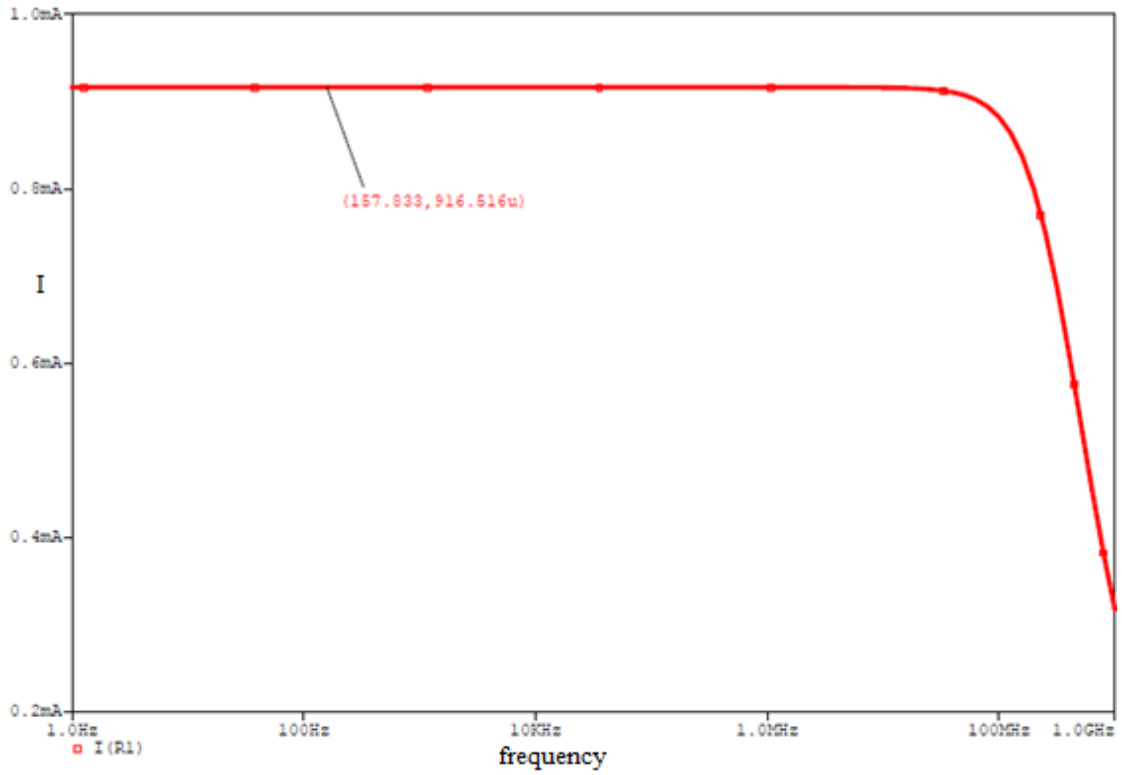

Fig. 3.12 Frequency response at input stage of VDBA

3.5 Summary

At last, it can be summarized that, this chapter presents the introduction of a basic VDBA block. Further, internal structure of VDBA and its ideal and non-ideal behavior are discussed in detail. After that CMOS realization of VDBA is done. At last we analyze the characteristics of CMOS based VDBA by SPICE simulations.

3.6DTMOS Based VDBA

3.6.1Introduction:

Designing of integrated circuits for a variety of applications has gained significant attention in the industry. It is seen from the trend of the semiconductor industry that with the continuous downsizing of feature size of the transistors, the optimal supply voltage of CMOS integrated circuits has been dramatically declined because the emerging consumer market wants portable devices that needed to be light and must operate for a long duration of time with the small battery. Therefore, low–power (LP) and low–voltage (LV) analog circuits are receiving appreciable attention and are becoming the first choice in the electronic industry. Since battery technologies do not evolve proportionally with the requirement of the applications demand. Therefore the primary challenge is to decrease the power consumption of the circuits.

Anyway, when we are moving to a low voltage supply, digital circuits do not suffer degradation in performance, however, the performances of analog circuits; such as speed, bandwidth linearity, dynamicrange, gain etc. are overripe by reduced supply voltage .So, there is crucial requirement to develop new design techniques for analog circuits which use the amount of power in the nano-watt range. From the last ten years, CMOS technology has played a great role in the rapid improvement of VLSI systems and the increased integration of VLSI systems. Characteristics of CMOS devices includes extremely low input offset voltage, low switching power consumption, very high input impedance, high packing density, due to these they can be easily scaled. So the requirement of the area for the circuit will be reduced. As a consequence of which, the parasitic capacitances are decreased because of smaller geometry, which in turns leads to more operating speed.

Average power consumed by any circuit is composed of two components which are static power and dynamic power.

$$P_{avg} = P_{static} + P_{dynamic} \quad (3.7)$$

$$P_{avg} = V_{DD} I_{leakage} + C V_{DD}^2 f \quad (3.8)$$

Where$V_{DD}$is power supply voltage, $I_{leakage}$ is sub– threshold leakage current of MOS transistor , C represents the total capacitance of a system, and f denotes the denotesthe frequency at which a circuit operates.

The most essential factors of CMOS VLSI design is the threshold voltage of the MOS devices that is V_T.Since, it has been clearly seen that the declining of $V_T$is not possible as quickly as V_{DD} does in each new process generation and also a MOSFET's sub–threshold leakage current, $I_{leakage}$, has the exponential dependency on the threshold voltage of MOSFET subsequently resulting in concerns over increasing P_{avg} through P_{static}

3.6.2Low voltage techniques

The key technologies used for LP and LV Integrated Chip design are:

- CMOS technology [19]: CMOS technology is a MOS technology in which incorporation of both *N*–channel and *P*–channel MOS transistors are fabricated on the same silicon chip. If in the bulk of the circuit *P*–doping or acceptor ions has been doped then the MOSFET is labeled as N–channel transistors whereas the *P*–channel devices require a well (tube) having N- doping or donor ions. The technology in which such a well is required is termed *N*–well technology. For a N–type substrate the arrangement is complementry the *P*–channel transistors are made in the substrate and the *N*–channel transistors sit inside the *P*–well [20]). In the fabrication of typical microchips, CMOS technology is employed, since it is cheaper than SOI & Bi-CMOS technologies and offers low–power dissipation, high performance high density.

.

- Bi-CMOS technology [21,22]: In this technology both MOS & BJT transistors are incorporated on a single integrated circuit, therefore this technology comprises the pros of both MOS& BJT transistors. Numerous advantages can be accomplished using this highly developed semiconductor technology such as: reduced value of power dissipation over purely CMOS technology, higher speed over purely bipolar technology, improved current drive over CMOS and obtaining high input impedance, low output impedance, latch–up immunity high analog performance, low noise, high gain, flexible I/Os for high performance,

smaller IC size and of more reliable IC. However, Bi-CMOS technology requires extra fabrication steps, which makes the technology not cost– effective.

- SOI (Silicon On Insulator) technology [23–27]: In this technology a layer of silicon dioxide is implanted below the surface by oxidation of Si or by oxygen implantation into Si. This implanted silicon dioxide below the surface is called buried oxide (BOX) and helps reducing parasitic capacitances, and as a result of this is improved performance of the device. SOI can be categorized into two types : fully depleted FD and partially depleted PD,

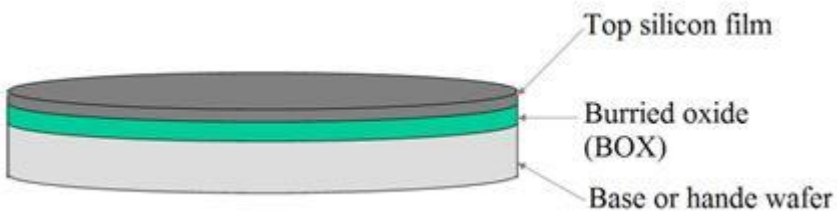

Figure 3.13 FD–SOI starting wafer.

SOI technology has numerous merits such as channel effects capacitance reduction, lower supply voltage, lower device threshold, soft error rate effects, smaller layout area, ideal device isolation, high switching speed and lower–power consumption. However, fabrication of this technology is more expensive featuring higher self–heating because of poor thermal conductivity of the insulator.

DTMOS (Dynamic Threshold MOS) (19-20): In this technology the input is applied at gate and bulk terminal of the MOSFET simultaneously or in other words we can say that bulk and gate of the MOSFET are connected. This connection of the device will decrease the V_T of the device and hence we can reduce the supply voltage of the device while maintaining current deriving capability. SOI technique can be use to manufacture the practical DTMOS which combines the pros of SOI technology and DTMOS.

3.6.3-DTMOS:

Due to the growing demand for longer battery life in mobile devices, mobile integrated circuit (IC) designers have focused on reducing the power consumption of circuits, especially for supply voltage scaling. As a result, the supply voltage has been greatly reduced, and subthreshold circuits have been developed.

Since the threshold voltages have not scaled as aggressively as the supply voltage, the static noise margin of digital circuits has continuously decreased.

The power delivered in CMOS circuit is directly proportional to square of supply voltage as given by equation 3.3:

$$P = CV_{DD}^2 f \qquad (3.9)$$

Where C is the total switching capacitance, V_{DD} is the supply voltage or swing across the capacitor and f is the switching fequency.

Though the decreasing of power supply less than three times the threshold voltage i.e. $3V_T$ will result in degradation circuit speed extensively, therefore the scaling of the power supply must be accompanied by threshold voltage reduction [28]. But lower limit of V_T is set by the amount of off state leakage current that can be tolerated.The relation between V_T and lekage current is given in equation 3.4

$$I_D = I_0 e^{\frac{q}{nk_BT}(V_{gs} - V_T + \gamma V_{bs} + \eta V_{ds})}\left(1 - e^{\frac{-qV_{ds}}{k_BT}}\right) \qquad (3.10)$$

In order to reduce Supply Voltage, DTMOS was proposed. Thus to reduce Supply Voltage to ultra-low voltages (0.6 V and below) a Dynamic Threshold Voltage MOSFET (DTMOS) was introduced, which have a high $V_T$at zero input bias and a low V_T at high input bias.DTMOS is abbreviation for Dynamic threshold metal oxide semiconductor.

.In DTMOS when no input is applied in between gate and source terminal i.e. Vgs =0 then the value of $V_T$remain same as conventional MOSFET and when applied input i.e.

Vgs increases then V_T must decreases consequences of which results in larger current driving capability than a standard MOSFET at lower power supply.V_T.

For DTMOS: V_T= V_{T0}at Vgs = 0

V_T= lowest $V_T$at Vgs = Vdd.

Now let us consider the equation of threshold voltage as given below by equation 3.11

$$V_T = V_{T0} + \gamma \left(\sqrt{|2\varphi_F| + V_{SB}} + \sqrt{|2\varphi_F|}\right) - \eta V_{DS} \qquad (3.11)$$

In equation 3.11,

φ_F is Fermi potential of bulk, V_{SB} is source to bulk voltage,

V_T is the threshold voltage when $V_{SB} \neq 0$ i.e the bulk and source are at different potential,

V_{T0} is threshold voltage when $V_{SB} = 0$ i.e. the bulk and substrate are at same potential.

γ is called Body effect coefficient and is given by:

$$\gamma = \frac{\sqrt{2qN_A \in_{Si}}}{C_{ox}} \qquad (3.12)$$

Typical value of γ is 0.4 .

ηV_{DS} represents the effect of DIBL and typical value of η is 0.02 – 0.1 .

From equation 3.5 it is evident that when the Body to source junction is forward biased (at less than 0.6V) causes the threshold voltage to drop. This is due to reason that when bulk potential is increased positively then this results in reduction of junction width and hence depletion region charge density and therefore V_T reduces.And when the body to source is reverse biased i.e. the body potential is decreased then it results in Reverse bias of junction consequently increases the depletion region width and hence increases body charge due to which V_T increases. This is the operation of DTMOS.

Since threshold voltage of MOSFET is changed dynamically that is why it is called dynamic threshold MOSFET.

3.6.3.1 Structure of DTMOS

DTMOS can be built by two techniques.

1- Simply connecting bulk and gate.

2- SOI (Silicon On Insulator)

1- Simply connecting bulk and gate

DTMOS can be simply by connecting body and bulk of transistor as shown in fig 3.14. However the same technique cannot be functional to NMOS transistor in the conventional bulk CMOS technology this is because of reason that on Integrated circuit all NMOS transistors share the common substrate therefore if it is applied to NMOS then it will effect all devices on chip. It can only be applied to PMOS transistors because every PMOS transistor is fabricated in its own N well.

To extend the application of DTMOS to NMOS we can use triple well technique which is very expensive as the fabrication cost increases.

(a) **NMOS** **(b)PMOS**

Fig 3.14 DTMOS by Simply connecting bulk and gate

2- SOI (Silicon On Insulator):

In SOI many author's tried to take advantage of the extra current produced by the lateral bipolar transistor to explain the operation of DTMOS .This requires body voltage to 0.6V or larger. The extra drain current comes at the expense of the large input (base) current which contributes more to leakage current than drain current. Large improvement in I_D is achieved at gate voltage less than 0.6V.Same idea can be achieved in bulk devices but isolation of the MOSFET body can be accomplished more easily in SOI because of very small junction areas and hence the capacitance can be much less than a bulk MOSFET. Also DTMOS technique can be applied to both NMOS and PMOS in the SOI technology. SOI based DTMOS is shown in Figure 3.15.

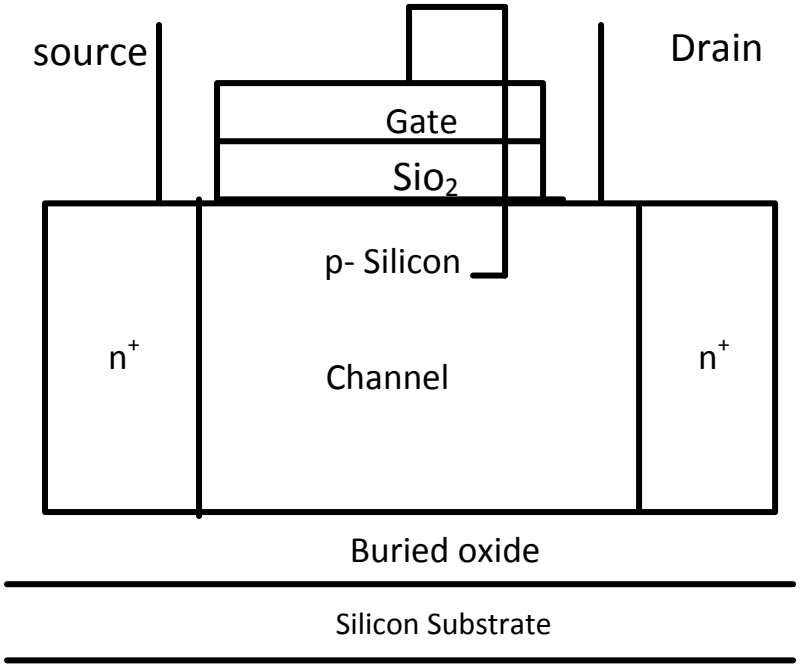

Fig 3.15 SOI based DTMOS

3.6.3.3 -Transfer Characteristic & Output Characteristic comparison of DTMOS with conventional MOSFET

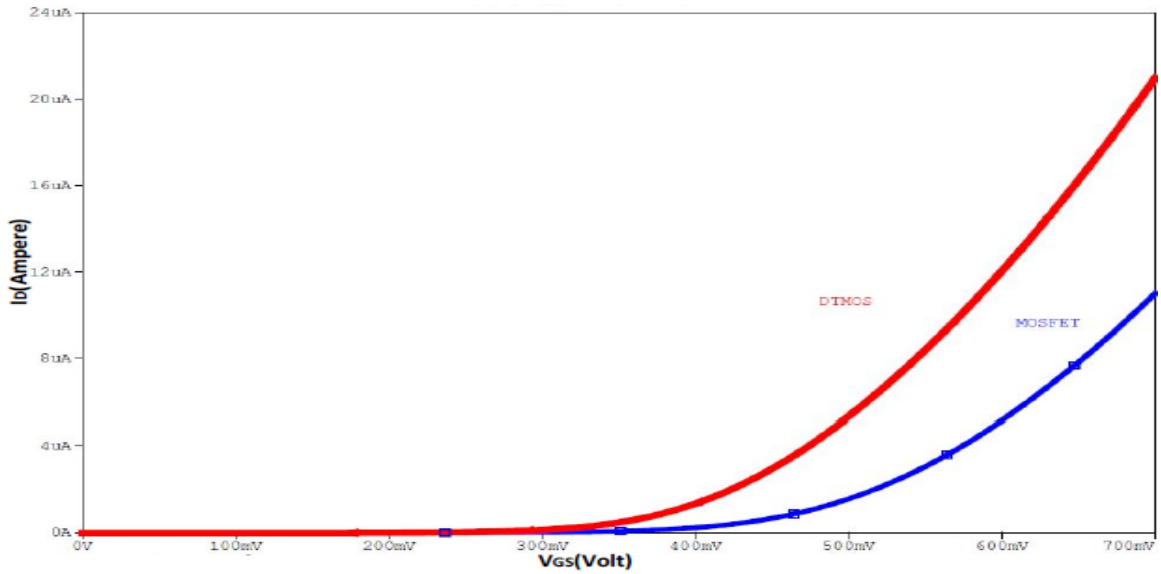

Fig 3.16 Transfer characteristic comparison of DTMOS Vs MOSFET

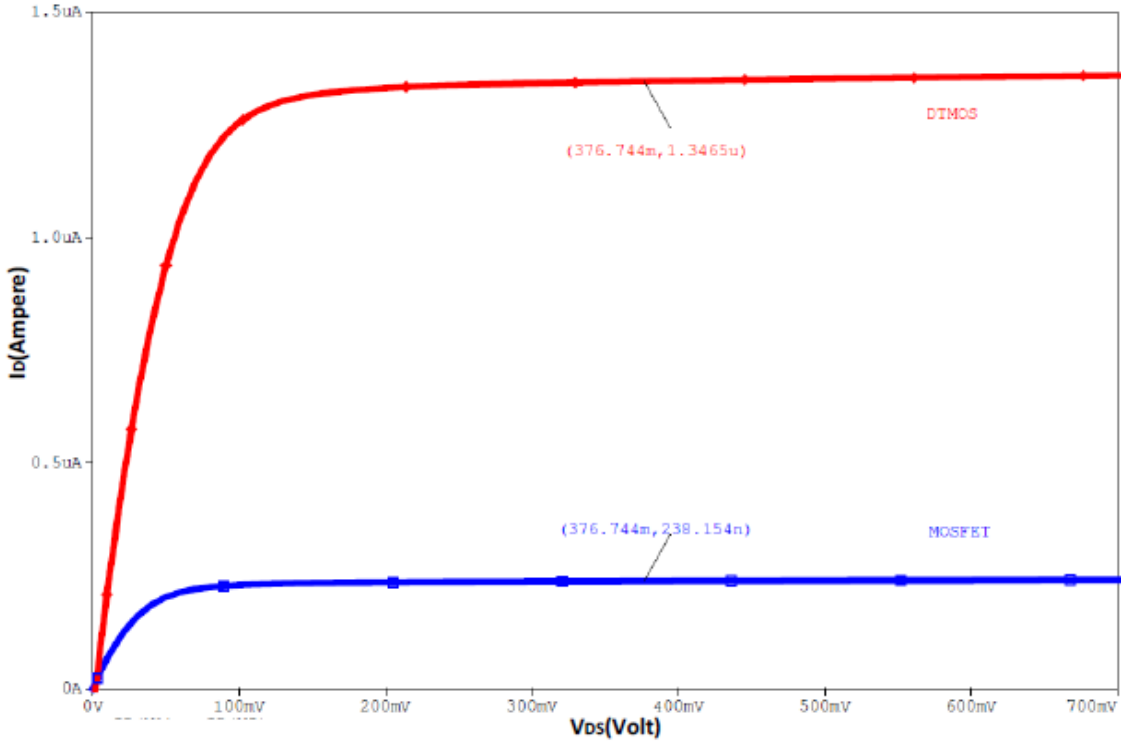

Fig 3.17 Output characteristic comparison of DTMOS Vs MOSFET

3.7 Realization of DTMOS Based VDBA

The internal construction of DTMOS based ULV and ULP proposed VDBA circuit is shown as in fig.3.18.The transistors from M1 to M5 and M11 to M13 are the PMOS DTMOS.DTMOS transistors, which have available voltage headroom, can be used efficiently under the ultra-low supply voltage of±0.4V.

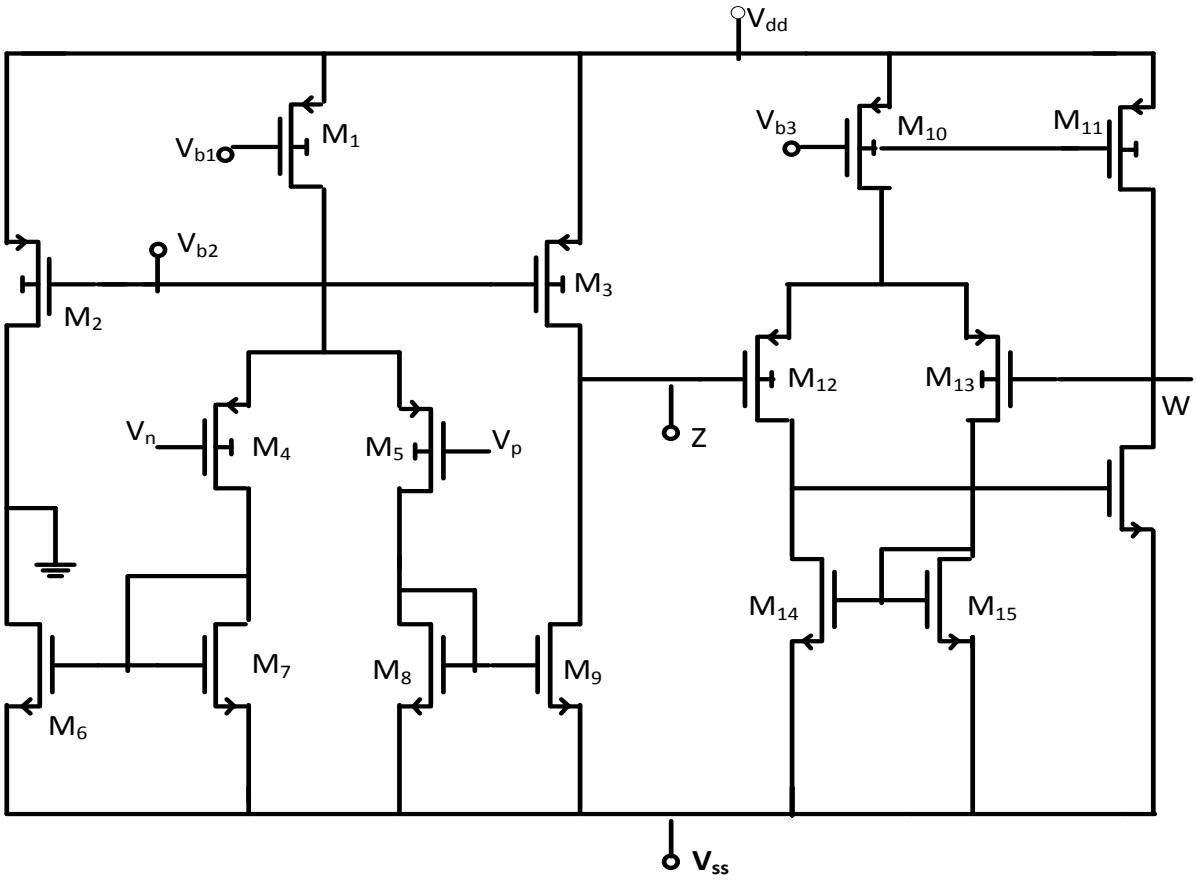

Fig. 3.18DTMOS-based VDBA circuit.

Table 3.2: W/L ratios of VDBA

Transistors	W(µm)	L(µm)
M_1,M_2,M_3,M_{10},M_{11}	5	2
M_4,M_5,M_{12},M_{13}	300	2
M_7,M_8,M_{14}.M_{15}	50	5
M_6,M_9,M_{16}	100	5

3.8 Characterization of DTMOS based VDBA

This DTMOS based VDBA circuit is achieved by connecting the bulk and gate of PMOS transistors. The circuits have been simulated by using LTSpice program with TSMC CMOS 0.18 μm process parameters. Table 4.2 shows avove the aspect ratios of the transistors for the proposed VDBA circuit. Supply Voltages are V_{dd} = -V_{ss} = 0.4 V and all the biasing voltages are grounded in this application (V_{b1} = V_{b2} = V_{b3} = 0 V).

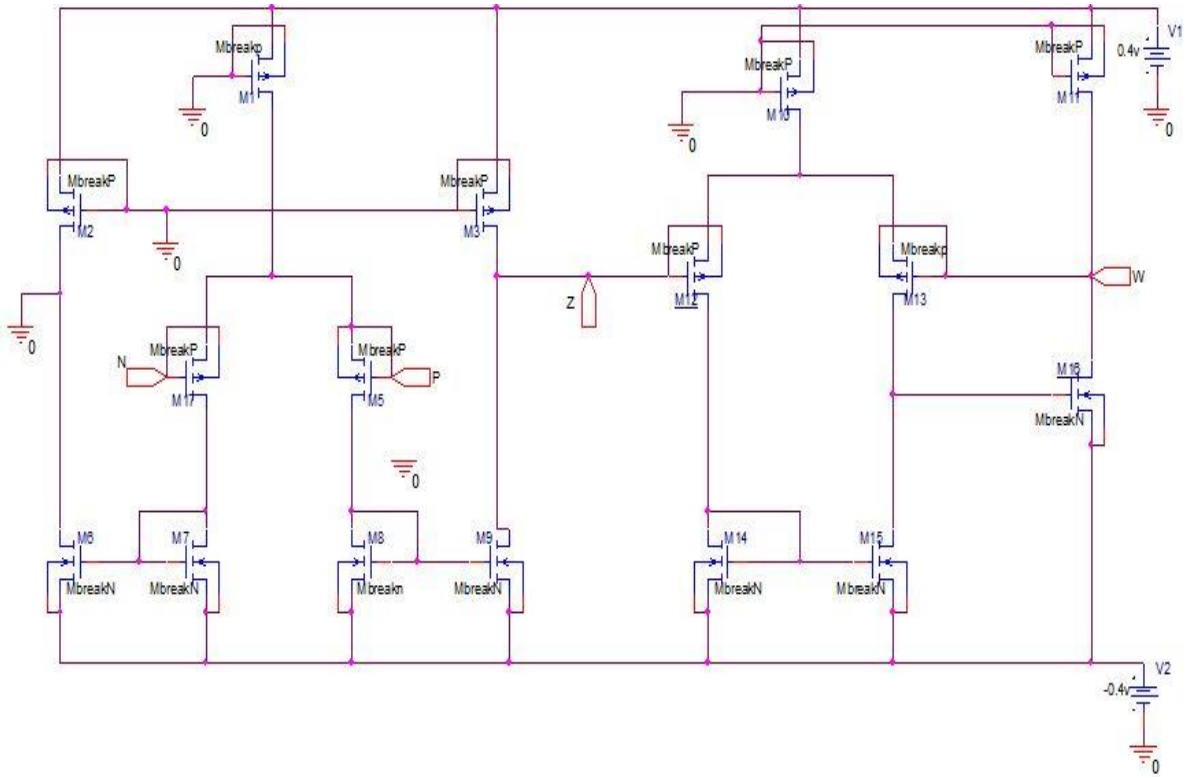

Figure 3.19 Schematic DTMOS based CDBA

All the characterization of VDBA is also done by DTMOS based VDBA and simulated using 0.18μm technology node PSPICE. The main DC and AC characteristics of VDBA, such as plots of I_Z against V_P, plots of V_Z against V_W, frequency responses of I_Z/V_P and V_W/V_Z are obtained from LTSPICE simulations.

3.8.1DC transfer characteristics at input stage:

The DC transfer characteristic of I_Z against V_P for DTMOS VDBA is shown in Fig. 3.20 that is obtained when one input (terminal N) is grounded, and I_z against V_n for VDBA is obtained when one input(terminal P) is grounded.

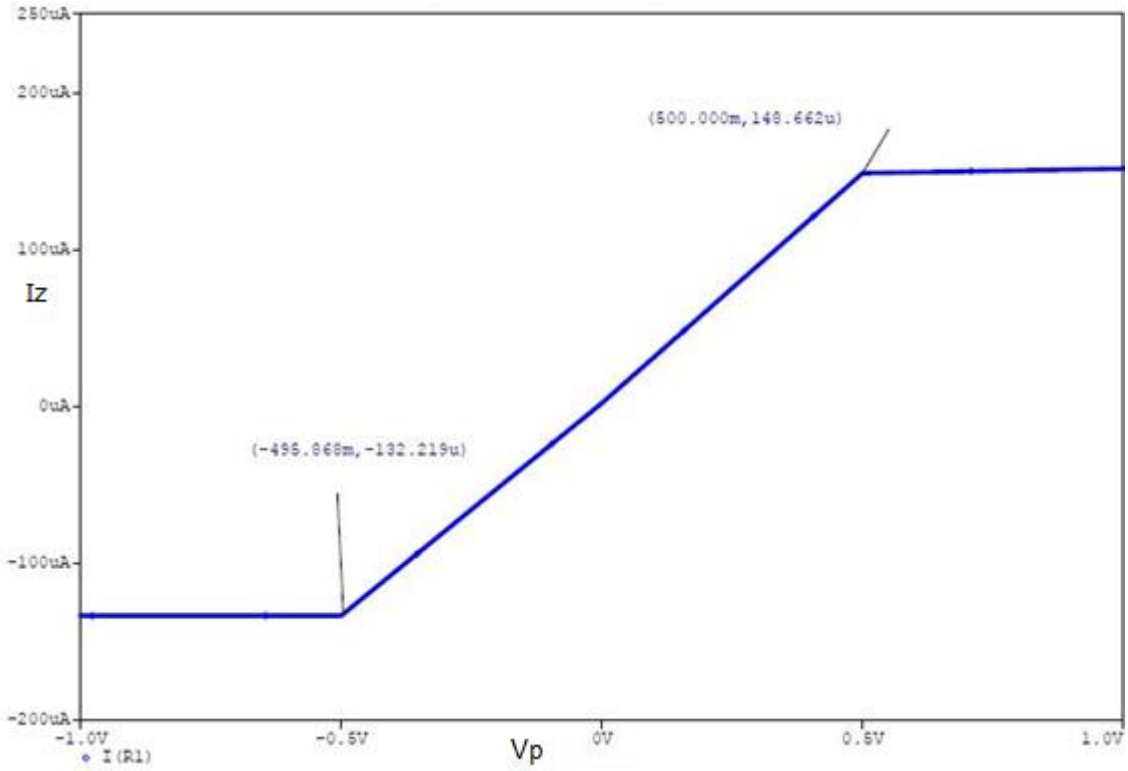

Fig 3.20 DC transfer characteristic I_Z vs V_P

The linearity extends in the range ±0.5Vwhile a non-linear behavior is observed elsewhere. Linearity range in DTMOS is greater in comparison to CMOS VDBA.

The operation of OTA stage of the DTMOS based VDBA, depicting I_Z against V_p and V_n for different supply voltages.

3.8.2Voltage transfer Characteristics of buffer

The voltage transfer characteristic can be plotted by connecting DC source at input of buffer stage and then by doing DC sweep of that source and measuring voltage the output stage. It is shown in Fig 3.8.The tracking behavior as shown in Fig 3.21 shows that in buffer stage output voltage follows the input voltage between -0.09V to 0.55V.

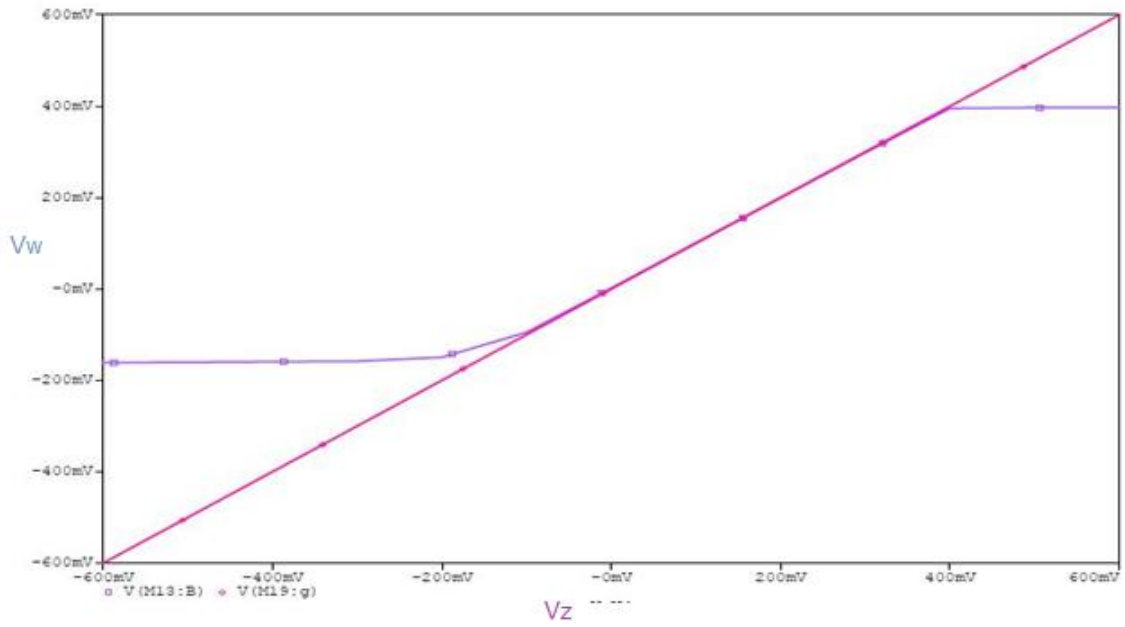

Fig 3.21 Voltage Transfer Characteristics of Buffer stage of DTMOS based VDBA

There is some error in input and output voltage levels in linear range which is known as tracking error. The Plot for tracking error is shown in Fig 3.22which obtained by subtracting input and output voltage. The range in which tracking error is Zero denote the range in which output voltage follows the input voltage.

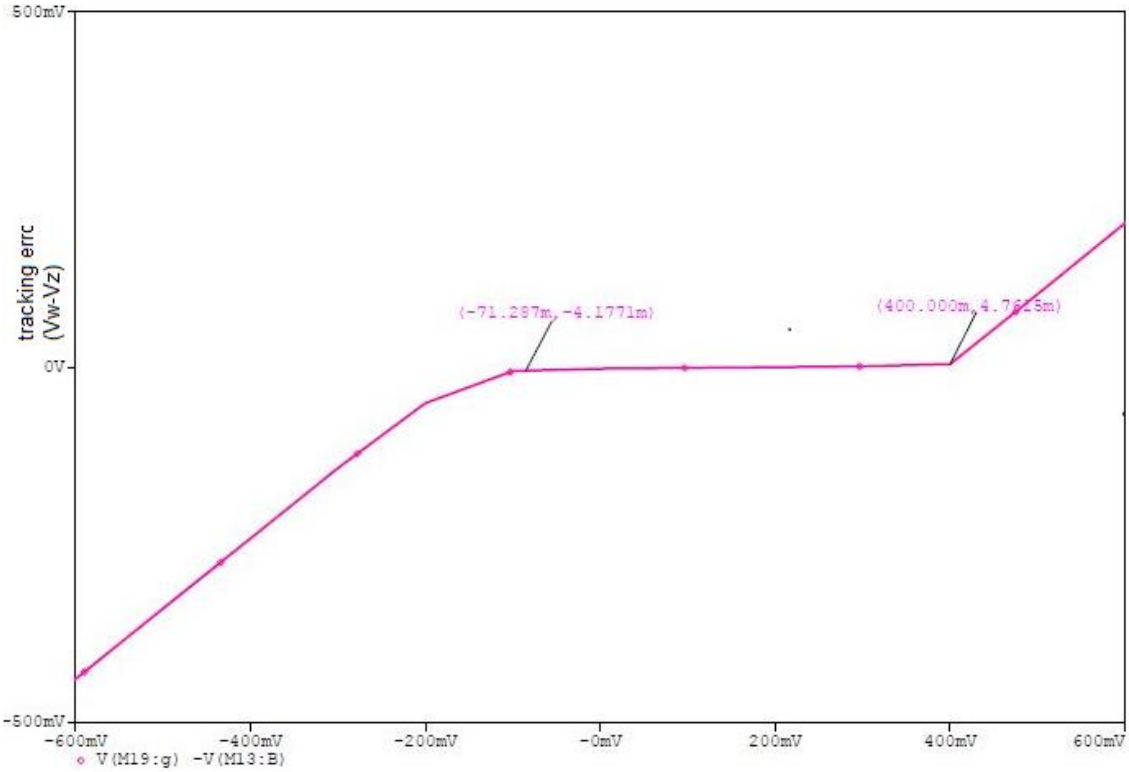

Fig 3.22 Tracking error of Buffer stage of DTMOS based VDBA

3.8.3 AC Transfer characteristics of output stage of VDBA

The AC transfer characteristic can be plotted by connecting AC source at input of buffer stage and connected output voltage is taken at the output. After that taken the output to input voltage transfer ratio. It is shown in fig 3.23, and it's value is very close to unity which is desired value for ideal buffer stage.

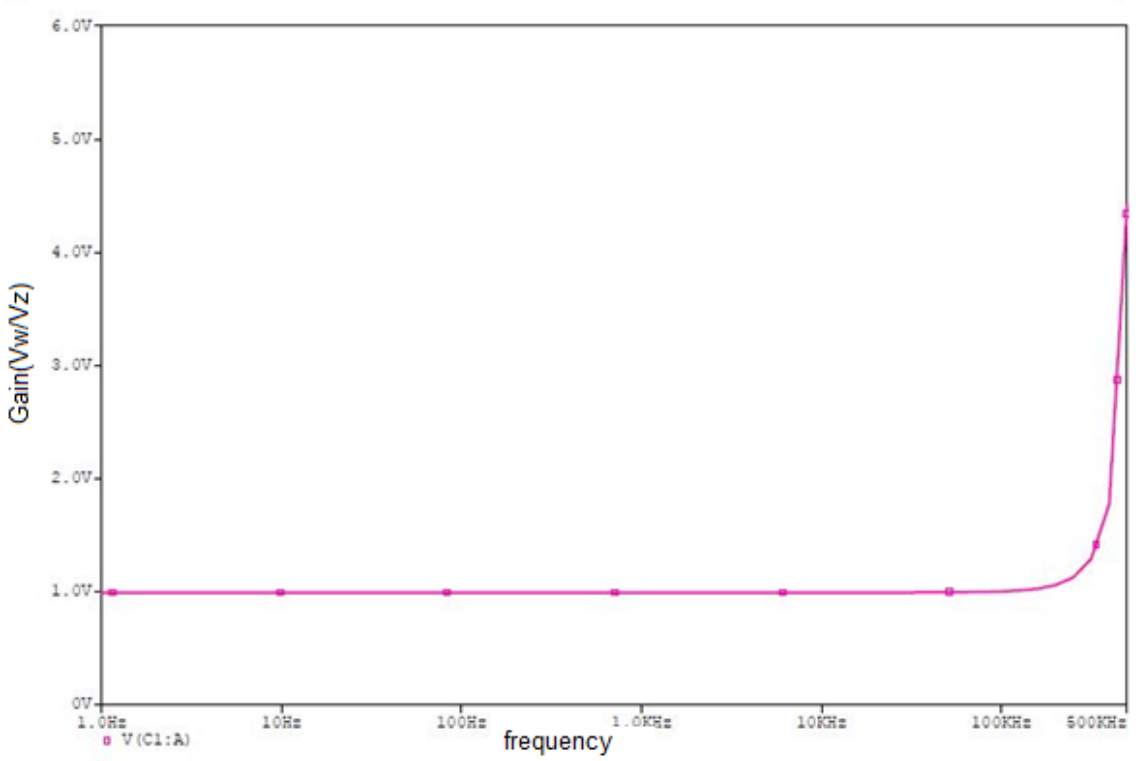

fig 3.23The AC transfer characteristics of output stage of DTMOS based VDBA

3.8.4Output Impedance at W terminal of DTMOS based VDBA

Measure of impedance at o/p terminal W, the i/p terminal of buffer amplifier Z is kept grounded and then a AC test input signal is applied to the terminal at which the impedance is to be measured. After that the ratio of voltage and current of this test signal is plotted w.r.t. to frequency. From the Fig. 3.25, the impedances seen through and terminals are found out to be small as it is required to be, theoretically.

The values of these impedances measured using point A from their corresponding frequency responses are as follows :

$$Z_w = 648\Omega$$

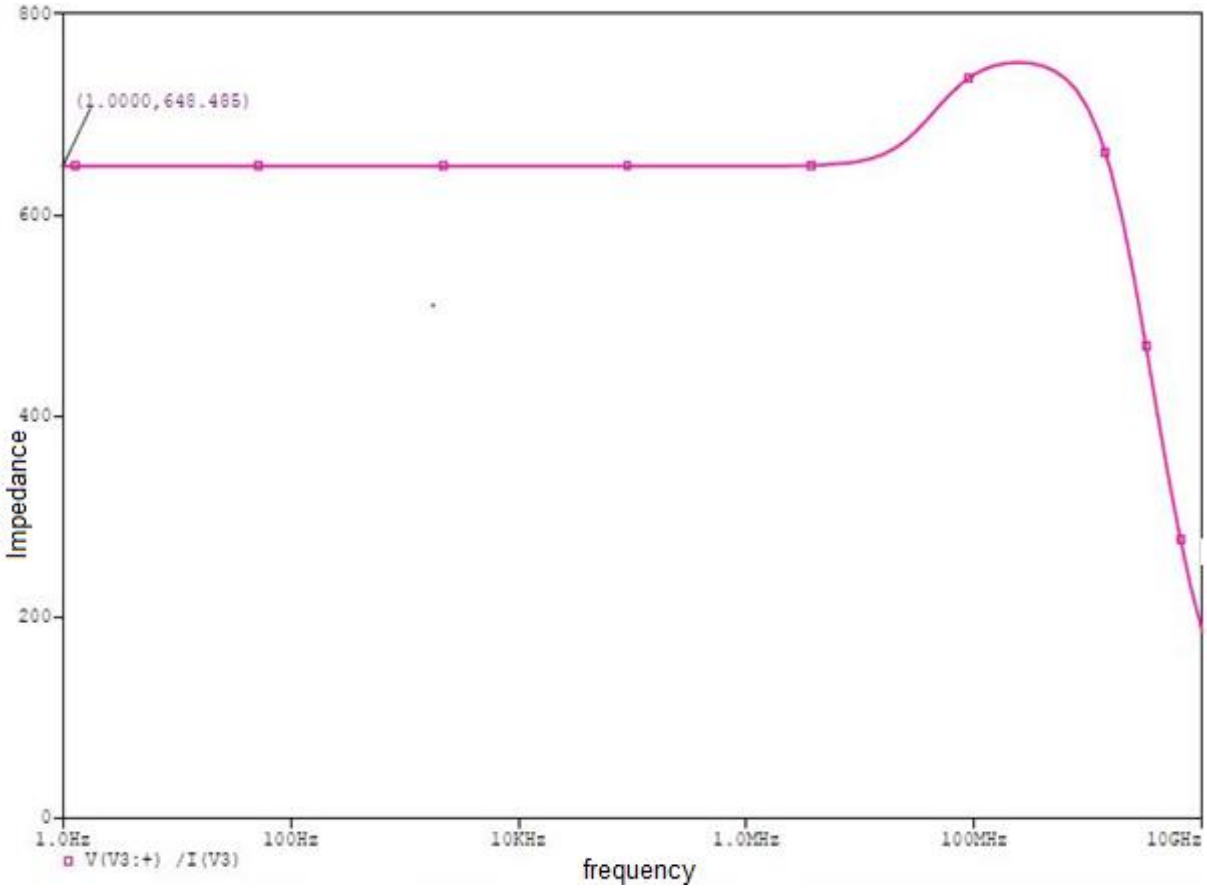

Fig 3.24 output Impedance at W terminal of DTMOS based VDBA

3.9 Summary

In the last, it can be summarized that after simulation of all characteristics CMOS based VDBA in section 3.4 in this chapter after that presents the detail of low power techniques. Detail analysis DTMOS technology, later which utilized for realization of VDBA. Therefore, DTMOS based VDBA is presented in this chapter also it's characteristics are observed using SPICE simulation

CHAPTER-4

APPLICATION

4.1Introduction:

To verifying the DTMOS based VDBA a universal filter design as proposed CMOS based VDBA. All filters can be classified on the basis of their topology i.e variable and fixed topology type. It is further divided into three categories current mode (CM), voltage mode (VM) and mixed mode (MM) types, which is further subdivided based on how to responses are obtained w.r.t. combinations of input's and output's.

i) single-input multiple-output (SIMO) type filters,
ii) multiple-input single-output (MISO) type filters
iii) multiple-input multiple-output (MIMO) type filter

One of the most widely used universal analog filters topology is a MISO type VM filters. By simply controlling the input voltages or by doing the same along with their different combinations, various filter functions can be realized.
In this chapter we present MISO type VDBA based voltage mode universal filter which is simulated by utilizing CMOS based VDBA and DTMOS based VDBA which were discussed in previous chapter and verify the working of DTMOS based CDBA.

4.2The Filter Application of DTMOS based VDBA

The block diagram in fig 4.1presents MISO filter module that allows multi voltage input and single voltage output.
In this chapter a new voltage mode VDBA based on DTMOS filter applications are designed, which consist two VDBAs, two capacitor three input and one output. This applications realized (low pass, band pass, high pass, and all pass) filter function. This shows that two VDBA filter application circuits based on MISO diagram module.

The passive elements with a certain limits must be used to design the biquad VDBA filters in order to realize all filter functions with the same pole frequency and quality factor.

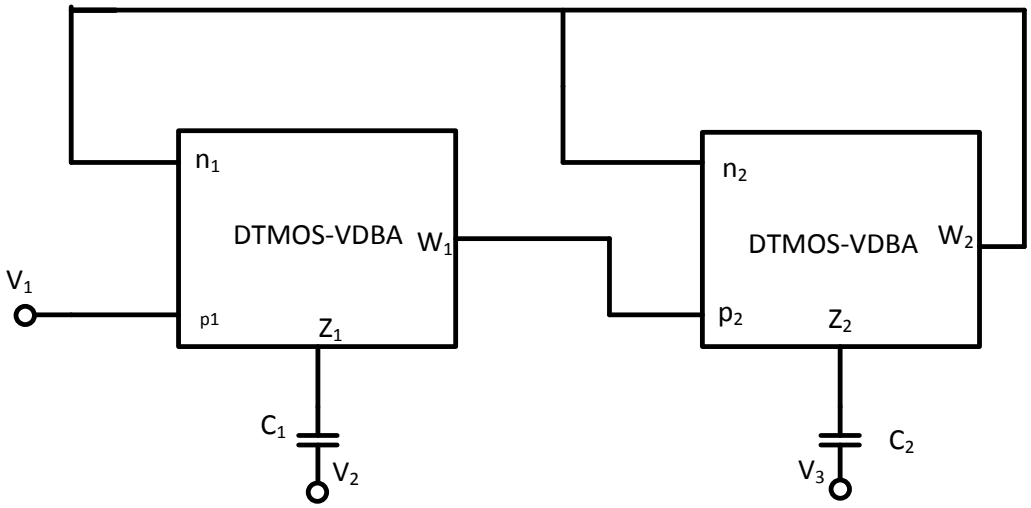

Fig 4.1 MISO Filter using DTMOS based VDBA block

Analyzing the above circuit by considering the ideal VDBA yields relation between o/p voltage and i/p voltages as below:

$$V_0 = \frac{V_1 g_{m1} g_{m2} + V_2 g_{m2} sC_1 + V_3 s^2 C_1 C_2}{g_{m1} g_{m2} + g_{m2} sC_1 + s^2 C_1 C_2} \quad (4.1)$$

Above equation can be manipulated for realizing various filters as:

1-Low pass filter (LPF):

Condition for LPF is: $V_1 = V_{in}$ .and $V_2 = V_3 = 0$

And low pass gain is $H_{LP} = 1$.

The transfer function is reduced as :

$$V_0 = \frac{V_1 g_{m1} g_{m2}}{g_{m1} g_{m2} + g_{m2} sC_1 + s^2 C_1 C_2} \quad (4.2)$$

2-High pass filter (HPF) :

Condition for HPF is: $V_1 = V_2 = 0$ and $V_3 = V_{in}$.

And low pass gain is $H_{HP} = 1$.

The transfer function is reduced as :

$$V_0 = \frac{V_3\, s^2 C_1\, C_2}{g_{m1}\, g_{m2} + g_{m2}\, sC_1 + s^2 C_1\, C_2} \qquad (4.3)$$

3-Bandpass filter (BPF) :

Condition for BPF is: $V_1 = V_3 = 0$ and $V_2 = -V_{in}$.

And low pass gain is $H_{BP} = 1$.

The transfer function is reduced as :

$$V_0 = \frac{V_2\, g_{m2}\, sC_1}{g_{m1}\, g_{m2} + g_{m2}\, sC_1 + s^2 C_1\, C_2} \qquad (.4.4)$$

4- Band reject filter (BRF) ::

Condition for BRF is: $V_1 = V_3 = V_{in}$ and $V_2 = 0$

And low pass gain is $H_{BS} = 1$.

The transfer function is reduced as :

$$V_0 = \frac{V_1\, g_{m1}\, g_{m2} + V_3\, s^2 C_1\, C_2}{g_{m1}\, g_{m2} + g_{m2}\, sC_1 + s^2 C_1\, C_2} \qquad (4.5)$$

5-All pass filter (APF) :

Condition for LPF is: $V_1 = -V_2 = V_3 = V_{in}$

And low pass gain is $H_{AP} = 1$.

The transfer function is reduced as :

$$V_0 = \frac{V_1\, g_{m1}\, g_{m2} - V_2\, g_{m2}\, sC_1 + V_3\, s^2 C_1\, C_2}{g_{m1}\, g_{m2} + g_{m2}\, sC_1 + s^2 C_1\, C_2} \qquad (4.6)$$

The ideal pole frequency(ω_o)and the quality factor (Q_O)for such proposed circuits are obtained as follows:

$$Q = \sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}} \tag{4.7}$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m1}}{C_2C_1}} \tag{4.8}$$

The passive sensitivities of the pole frequency(ω_o) and the quality factor(Q_O) for the proposed configuration with respect to active and passive elements yield:

$$S_{(g_{m1})}^{(w_0)} = S_{(g_{m2})}^{(w_0)} = -S_{(g_{c1})}^{(w_0)} = S_{(g_{c1})}^{(w_0)} = \frac{1}{2} \tag{4.9}$$

$$S_{(g_{m1})}^{(Q_0)} = S_{(g_{m2})}^{(Q_0)} = -S_{(g_{c1})}^{(Q_0)} = S_{(g_{c1})}^{(Q_0)} = \frac{1}{2} \tag{4.10}$$

The absolute value of the sensitivity for the pole frequency and the quality factor at the ideal case is obtained by choosing the value of all passive elements equaled to 0.5 as given in equation (4.9) and (4.10).

4.2 Simulated output:

This filter is designed with pole frequency (ω_o) of 10KHz and quality factor(Q_O)=1 and passive element with capacitor $C_1 = C_1 = 0.1nF$.

The simulation of filters are done in SPICE using 0.18um technology by using the values of resistors and capacitors as mentioned above and output for both DTMOS based VDBA filters and CMOS based VDBA filters are observed in Fig 4.2 , Fig 4.3 , Fig 4.4 , Fig 4.5 , Fig 4.6 .

1-LPF:

From simulated graph the 3dB cut off frequency for CMOS based VDBA and DTMOS based VDBA LPF are found to be 10.447 kHz and 9.188 kHz respectively

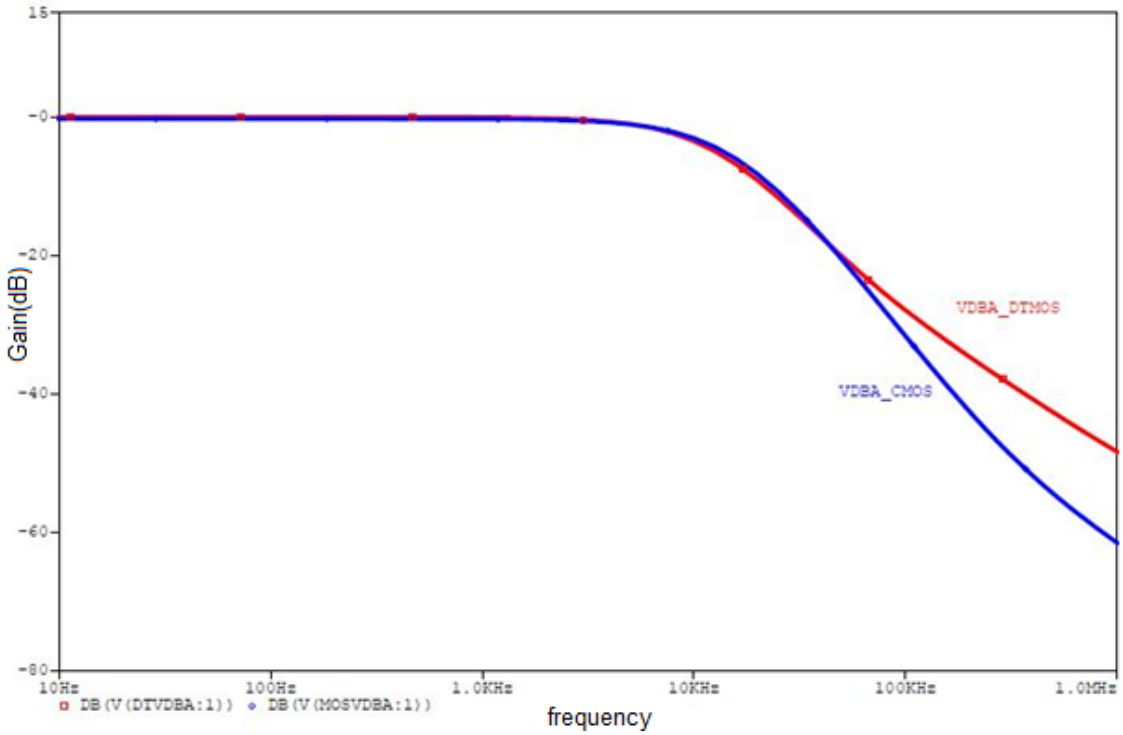

Figure 4.2 Simulated waveform of LPF using DTMOS based VDBA& CMOS based VDBA.

2-HPF: From simulated graph the 3dB cut off frequency for CMOS based VDBA and DTMOS based VDBA HPFs are found to be 24.760 kHz and 22.321 kHz respectively

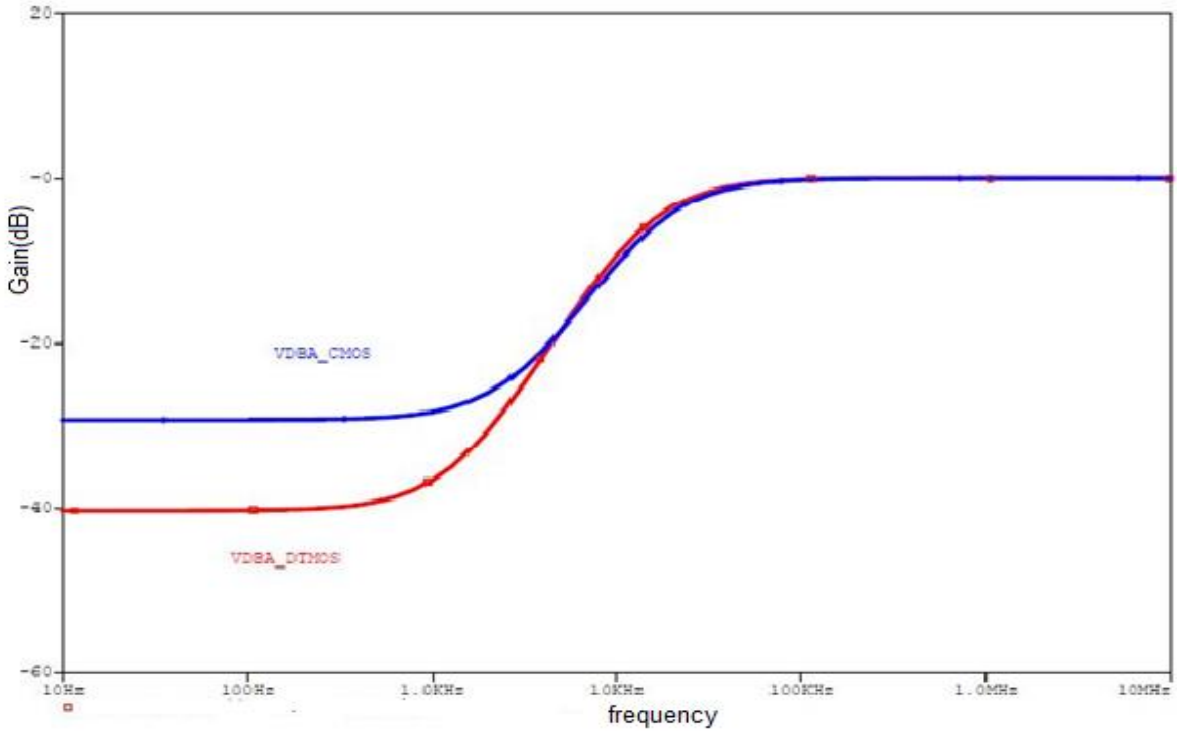

Figure 4.3 Simulated waveform of HPF using DTMOS based VDBA& CMOS based VDBA

3-BPF: From simulated graph the 3dB bandwidth for CMOS based VDBA and DTMOS based VDBA BPFs are found to be 32.287 kHz and 28.374 kHz respectively;

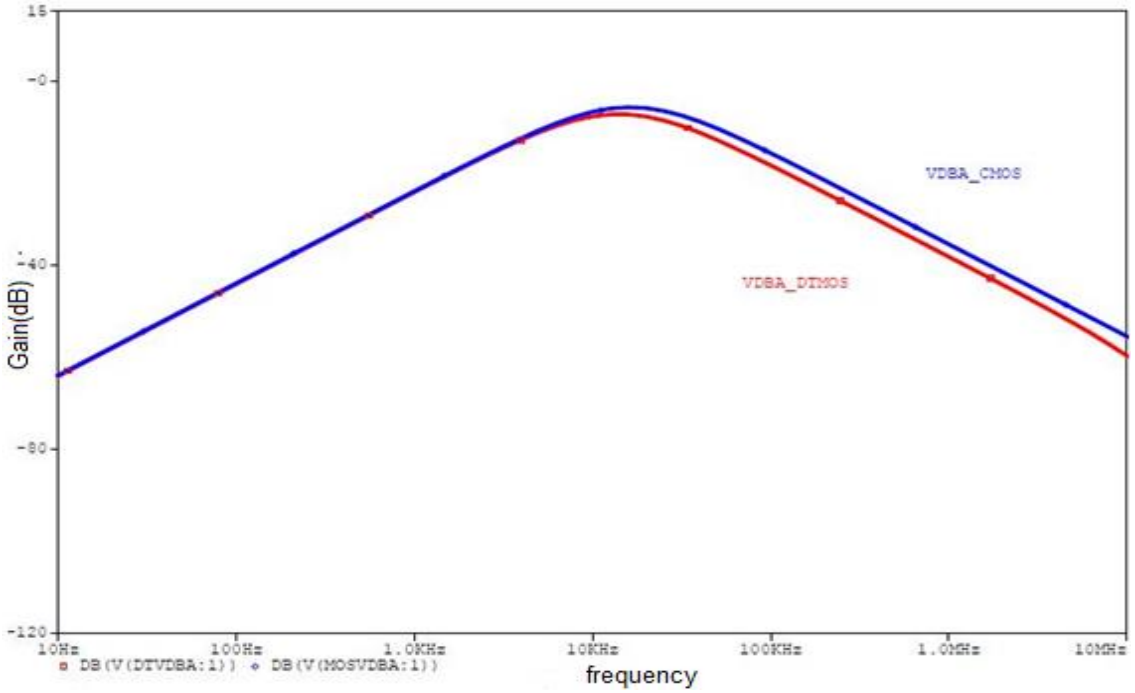

Figure 4.4 Simulated waveform of BPF using DTMOS based VDBA& CMOS based VDBA

4-BRF: From simulated graph the 3dB bandwidth for CMOS based VDBA and DTMOS based VDBA BRFs are found to be 32.710 kHz and 28.136 kHz respectively.

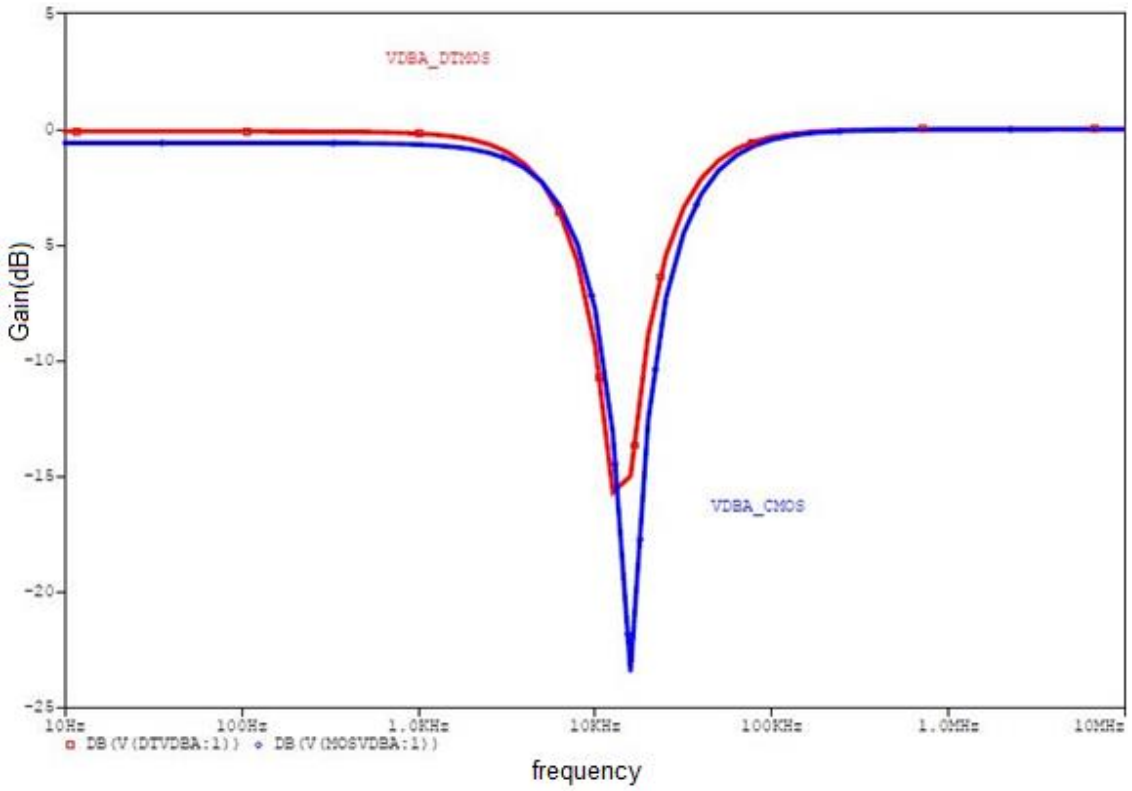

Figure 4.5 Simulated waveform of BRF using DTMOS based VDBA& CMOS based VDBA.

5-APF:

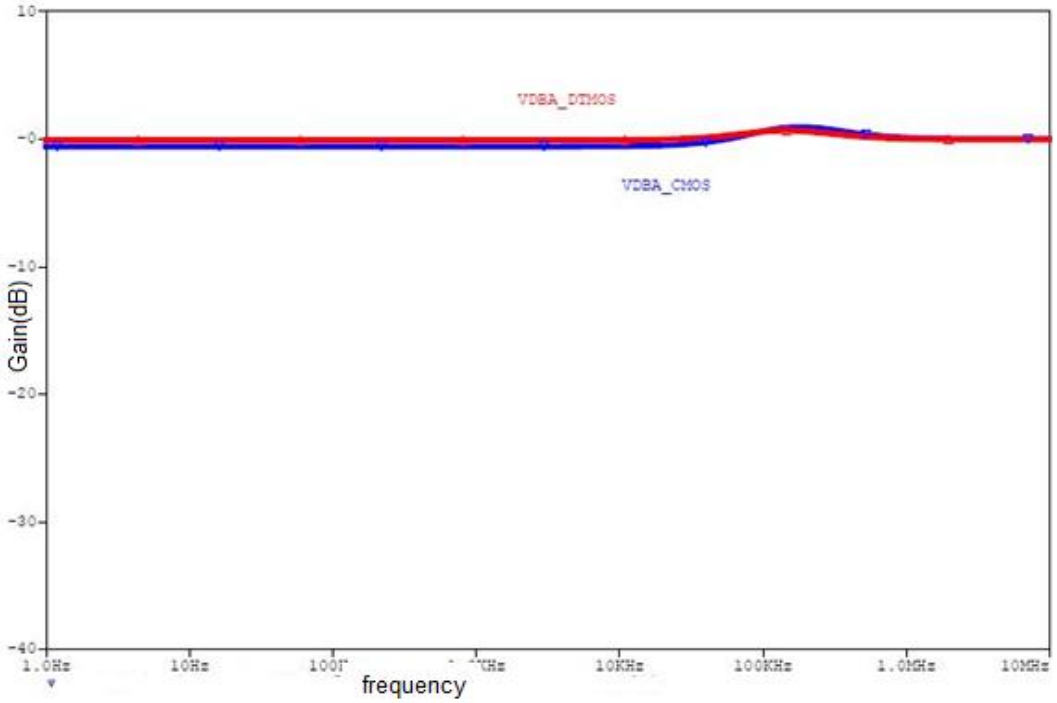

Figure 4.6 Simulated waveform of APF using DTMOS based VDBA& CMOS based VDBA.

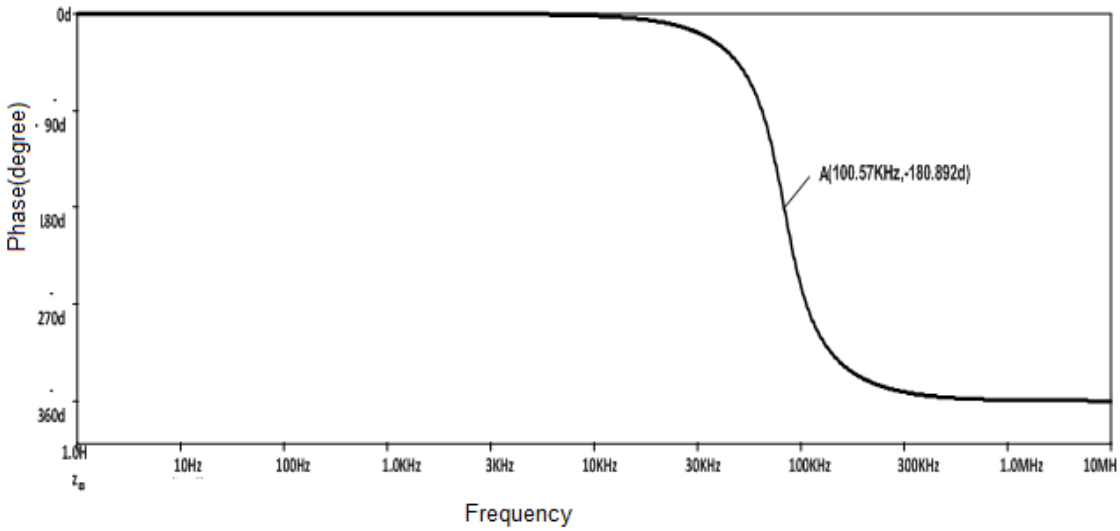

Fig 4.7 Phase response of APF using DTMOS based VDBA

4.3 Bandwidth Comparison Of CMOS VDBA & DTMOS VDBA Filters

The 3dB cut off frequency and bandwidth for DTMOS based VDBA and CMOS based VDBA filters which are observed from simulated graphs are summarized in table 4.1 as shown below:

Table 4.1 : Bandwidth Comparison Of CMOS VDBA & DTMOS VDBA filters

Filter	CMOS based CDBA Filter	DTMOS based CDBA Filter
LPF	10.447K	9.188K
HPF	24.760K	22.319K
BPF	32.287K	28.374K
NOTCH	32.710K	28.136K

4.4 Summary:

In the last, it can be summarized that in this chapter presents the VDBA based voltage mode universal filter which is modified by replacing the CMOS based VDBA with DTMOS based VDBA . At the end 3-dB Bandwidth Comparison Of CMOS VDBA & DTMOS VDBA Filters is analyzed. All the working of DTMOS based VDBA is verified by the simulated output of the filters.

CHAPTER-5
Conclusion & Future Scope

DTMOS realization of VDBA that operates on low voltage with reduced power consumption was illustrated with detail and verify all the proposed active circuit. DTMOS based VDBA is able to work with 0.4 V voltage and only consuming very less power, which are suitable value for ultra-low voltage and ultra-low power operations. The proposed VDBA was tested with an application example of the filter. The LTSpice simulation results were depicted and according to simulations, both VDBA and filter have performed very well &Sensitivity analyses.

The proposed active block has been worked in weak inversion area, so the working frequency is not very high. It works in low frequencies. It is verified that the DTMOS based VDBA circuit and filter will be useful in the design of ULV and ULP analog signal processing applications and biomedical applications.

There are various methods available in literature to reduce the power consumption of integrated circuits.As most of the electronic devices we encounter in our daily life are battery operated, there is huge demand of low power IC's. As power consumption is directly proportional to the square of power supply voltage, reduction in power supply voltage is mandatory in order to reduce the power consumption. DTMOS transistor offers the advantage of implementing low power analog circuits by dynamically varying the threshold voltage. In this work we have modified the best available structure of VDBA to obtain low power VDBA by replacing existing PMOS transistors with DTMOS based PMOS transistors.

In this thesis, modified version of VDBA is implemented which has the importance of having only $\pm$0.4V supply voltage. Since, supply voltage is reduced to great extent therefore power consumption of circuit is also reduced to considerably and hence we are able to increase the battery life. Another advantage of DTMOS is higher trans-conductance and transition frequency.

One of the drawbacks associated with DTMOS based VDBA is that its linear range of operation decreases. The linear range of buffer stage is from between -0.09V to 0.55V.Therefore, the further work in low power VDBA deals with increasing linear range of circuit.

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