REALIZATION OF DXCCII BASED HALF WAVE AND FULL WAVE RECTIFIER

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I, (Vishwajeet Singh), Roll No. 2K15/VLS/20 student of M.Tech (VLSI design & Embedded systems), hereby declare that the project Dissertation titled "Realization of DXCCII based Half wave and Full wave rectifier" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "Realization of DXCCII based Half wave and Full wave rectifier" which is submitted by Vishwajeet Singh, 2K15/VLS/20, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Rectification is a demanding aspect when it comes to electronic equipment. The demand of low supply voltage and high speed devices has increased the demand of such rectifiers which can process low amplitude signals with high efficiency and can operate at high frequencies. Such rectifiers are called as the precision rectifiers which are used for signal processing, measurement and control of the low level signals.

In the past operational amplifiers have been used to develop the precision rectifiers but they failed to operate at high frequencies due to their slew rate limitations. They also needed passive devices such as diodes and matching resistors which offered difficulties in their integration. The employment of current mode techniques either by using current conveyors or by creating dedicated CMOS circuits have fruitfully resolved the conventional limitations by providing much enhanced performance of precision rectifiers.

Concerned about the above mentioned issues, three newly proposed circuits are presented to serve the applications of precision rectification. Each circuit employs single Dual-X Second Generation Current Conveyor (DXCCII) as the active building block and uses one or two NMOS transistors for the switching purposes.

The first two proposed circuits are voltage mode precision half wave rectifiers. The first proposed precision half wave rectifier rectifies the positive half cycles of the input AC (Alternating Current) voltage signal while the second proposed precision half wave rectifier rectifies the negative half cycles of the input AC voltage signal. The third proposed circuit is a voltage mode precision full wave rectifier that provides the full wave rectification of the input AC voltage signal.

Further two voltage mode digital modulators have been proposed i.e. Binary Amplitude Shift Keying (BASK) and Binary Phase Shift Keying (BPSK). BASK uses one DXCCII and one NMOS transistor. BPSK uses one DXCCII, one NMOS transistor and one PMOS transistor.

All the above proposed circuits have the advantage of having proper input impedance and use of grounded resistor. The rectifiers provide additional advantage of using no diodes for rectification, rather NMOS transistors are used.

All the proposed circuits have been simulated with SPICE using 0.35µm CMOS technology parameters. The supply voltage of $\pm 1.8V$ is used. Much satisfactory results have been obtained with all the proposed circuits.

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LIST OF ABBREVIATIONS AND SYMBOLS

[1] CC : Current Conveyor

[2] CCI : First Generation Current Conveyor

[3] CCII : Second Generation Current Conveyor

[4] CCII+ : Positive type Second Generation Current Conveyor

[5] CCII- : Negative type Second Generation Current Conveyor

[6] CCIII : Third Generation Current Conveyor

[7] CCIII+ : Positive type Third Generation Current Conveyor

[8] CCIII- : Negative type Third Generation Current Conveyor

[9] CCCS : Current Controlled Current Source

[10] VCVS : Voltage Controlled Voltage Source

[11] VCCS : Voltage Controlled Current Source

[12] CCVS : Current Controlled Voltage Source

[13] NIV : Negative Impedance Inverter

[14] INIC : Inverting Negative Impedance Converter

[15] Op-Amp : Operational Amplifier

[16] DO-CCII : Dual Output Second Generation Current Conveyor

[17] CFCCII : Current Follower Second Generation Current Conveyor

[18] CFCCIIp : Positve type Current Follower Second Generation Current Conveyor

[19] CFCCIIn : Negative type Current Follower Second Generation Current Conveyor

[20] DVCCII : Differential Voltage Second Generation Current Conveyor

[21] DVCCC : Differential Voltage Complementary Current Conveyor

[22] ICCII : Inverting Second Generation Current Conveyor

[23] DDCC : Differential Difference Current Conveyor

[24] DCC : Differential Current Conveyor

[25] MDCC : Modified Differential Current Conveyor

[26] DXCCII : Dual-X Second Generation Current Conveyor

[27] FDCCII : Fully Differential Second Generation Current Conveyor

[28] FBCCII : Fully Balanced Second Generation Current Conveyor

[29] MCCII : Modified Second Generation Current Conveyor

[30] OFC : Operational Floating Conveyor

[31] UCC : Universal Current Conveyor

[32] CCCII : Current Controlled Second Generation Current Conveyor

[33] CGCCII : Current Gain Second Generation Current Conveyor

[34] EXCCII : Extra-X Second Generation Current Conveyor

[35] DV-DXCCII : Differential Voltage Dual-X Second Generation Current Conveyor

[36] MO-DXCCII : Multiple Output Dual-X Second Generation Current Conveyor

[37] MO-CCCII : Multiple Output Current Controlled Second Generation Current Conveyor

[38] OTRA : Operational Trans Resistance Amplifier

[39] CFOA : Current Feedback Operational Amplifier

[40] UVC : Universal Voltage Conveyor

[41] OTA : Operational Transconductance Amplifier

[42] DO-OTA : Dual Output Operational Transconductance Amplifier

[43] FCS : Floating Current Source

[44] ZCD : Zero Crossing Detector

[45] TE : Transconductance Element

[46] CCIICS : Current Conveyor Based on Current Steering Output Stage

[47] FDNR : Frequency Dependent Negative Resistance

[48] IC : Integrated Circuit

[49] RF : Radio Frequency

[50] IR : Infrared

[51] RFID : Radio Frequency Identifier

[52] SR : Slew Rate

[53] SNR : Signal to Noise Ratio

[54] RMS : Root Mean Square

[55] P_e : Probability of Error

[56] BER : Bit Error Rate

[57] AWGN : Additive White Gaussian Noise

[58] CM : Current Mirror

[59] MOS-R : MOS Resistor

[60] BJT : Bipolar Junction Transistor

[61] MOSFET : Metal Oxide Semiconductor Field Effect Transistor

[62] JFET : Junction Field Effect Transistor

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Designing of the analog circuits itself has been through the evolution process, together with the evolution in the technology and the performance requirements. Today, for the development of microelectronic industry, there is a need of electronic circuits which can operate on extremely low supply voltages consuming the least amount of power. Also, there is a need of extreme speed of operation along with the high accuracy. However, it has still not been possible to satisfy all the needs simultaneously, to improve one performance parameter the other parameter has to be compromised, therefore many trade off solutions are employed in practice.

There is a big range of applications of analog signal processing where there is a need of an active building block, hence the development and improvement of the active elements also is of prime concern in today's generation. Within the last decade, many active analogue building blocks or elements have been introduced which offers the feature of electronic tunability. The behavior or response of the active building block can therefore be controlled electronically. Such devices offer facility of single parameter control for example the input impedance, trans resistance, trans conductance, voltage gain and current gain can be controlled electronically. Recently, many methods have been proposed for multi parameter control also i.e. they allow control of more than one parameter simultaneously hence make the active block more versatile and efficient.

In the development process, a new trend emerged to describe the circuit that is called as the current mode approach. The current mode processing may be defined as the processing environment where signals in the voltage form are irrelevant and processing is done in the form of current signals to determine the performance of the circuits. This is particularly used in the case of a circuit that has low impedance nodes and voltage swing is small and time constant is small. Therefore, usually to describe an electronic circuit the two terms are often used, i.e. the current mode circuit or the voltage mode circuit. Although, there is no clear cut definition of current mode or voltage mode available in the literature, but a working definition can be, that a current mode circuit is that in

which the state variables are represented in the form of currents, and in the dual sense, a voltage mode circuit is that in which the state variables are represented in the form of voltages [51]. A voltage mode circuit can be transformed in to a current mode circuit using a theorem known as the adjoint network theorem [52], where the modelling of circuits is done in the form of passive network segments and the controlled sources. Also a current mode circuit can be obtained from their voltage mode equivalent circuit by interchanging the position of nullators and norators [53]. With the emergence of the current mode applications, mixed mode circuits also gained attention to fulfil the optimization requirement of the interfaces in between the sub blocks of a system that operate in different modes.

With the advancement in time, CMOS VLSI technology has become more popular and much efforts have been devoted to reduce the dimensions of CMOS devices in order to reduce the area requirements and to make them operate on as low power supply as possible to reduce the power requirements. This led to an aggressive decrement in the supply voltage and a moderate decrement in the threshold voltage of the CMOS technology. Therefore when it comes to the CMOS based voltage mode circuits, these changes have greatly affected their performance. The performance of CMOS based voltage mode circuits has degraded because of these changes, for example, there has been a reduction in the dynamic range, an increment in the propagation delay and reduction in the noise margins. However when it comes to the current mode circuits, the impact of these changes in CMOS technology on their performance is less severe when compared to voltage mode circuits. This is due to the reason that in a current mode circuit the design emphasis is on the currents in the branches of the circuit rather than the voltages at the nodes of the circuit. The more immunity of the current mode circuits over voltage mode circuits towards the difficulties being born because of the reduction in the supply voltage of CMOS technology and increment in the operational speed has captured much attention of both the industry and the academia recently, thus has increased the popularity of current mode circuits. The design principles of the voltage mode and the current mode circuits are different, as in case of a voltage mode circuit, the design focus is on the intrinsic characteristics of the nodal voltages, while in case of a current mode circuit, the design focus is on the intrinsic characteristics of the currents flowing in the branches of the circuit.

1.2 CURRENT MODE VERSUS VOLTAGE MODE

1.2.1 DEFINING CURRENT MODE AND VOLTAGE MODE APPROACHES

A current mode technique is that technique which tends to reduce the voltage swing or voltage variation and deal with the current, whereas, a voltage mode technique is that technique which tends to reduce the current swing or current variation and deal with the voltage [55].

The information contained in an electronic circuit can be represented either by the nodal voltages or by the branch currents of the circuit. When nodal voltages are used to describe a circuit's equations and information, it is called as the voltage mode circuit while if branch currents are used to describe the information and equations of a circuit, it is called as the current mode circuit.

A voltage mode circuit often uses high loop gain and is more complex while a current mode circuit often uses less loop gain and is less complex [56].

For a voltage mode circuit, the input impedance must be high while the output impedance must be low. And for a current mode circuit the input impedance must be low while the output impedance must be high. When voltage mode and current mode are taken together, the behavior of a circuit can be characterized completely.

1.2.2 THE DOMINANCE OF VOLTAGE MODE

Although, the concept of an ideal current mode circuit similar to that of an ideal voltage mode circuit had been introduced like four decades ago, still, voltage mode circuits became more popular and found much more number of applications than the current mode counterparts. This can be seen by the fact that countless texts are available on voltage mode circuits but comparatively very little literature is available for the current mode circuits.

The reasons for high popularity of the voltage mode circuits can be described as follows

1) In voltage mode, the voltages at various nodes can be measured easily using voltmeters and there is no need to modify the circuit topology for this purpose. Whereas in the current mode, it is not easy to measure the currents flowing in the branches of a circuit and it mostly needs to change the circuit topology or needs an additional circuitry.

2) The impedance of the gate terminal of a MOSFET is infinite and it makes MOSFETs the ideal choice to realize a voltage mode circuit, especially in configuration employing cascading of different blocks, for example a multi stage voltage amplifier.

3) It is easy to get the high voltage gain in case of a voltage mode circuit by using certain techniques for example cascodes, regulated cascodes etc.

4) In the past high supply voltages were available, so designing of a circuit with a low voltage power supply was not a critical concern.

5) As high supply voltage was available, therefore switching noise was not a big issue to be concerned about.

6) In the past there were low speed requirements, it allowed the charging and discharging times of the nodal capacitors to be large.

The analog signal processing was considered superior in the voltage mode topology, but since the development of CMOS technology, the supply voltage greatly reduced and this has adverse effect on the performance of the voltage mode circuits. Whereas the negative effect on the current mode circuits performance is much less than compared to that of voltage mode circuits. Therefore, lately, the current mode topology has gained much interest of the circuit designers because of the advantages they offer over the voltage mode circuits. However, in reality, there is no single

topology among the voltage mode and current mode topologies that can be used to satisfy all the required performance parameters. To satisfy some parameters, other parameters have to be compromised and a tradeoff solution has to be considered where the parameters of less importance are compromised and the important performance parameters are given more attention regarding improvement in the performance. Therefore one must analyze the performance parameters first and then decide which topology among the voltage mode topology and current mode can be considered optimum to get the required performance of a certain application.

1.2.3 COMPARISON BETWEEN THE CURRENT MODE AND VOLTAGE MODE TOPOLOGIES

Below is the relative comparison between the current mode and voltage mode topologies [57].

1) **Delay and power dissipation:** With the shrinking technology there has been an increment in the interconnect delays and it has become a dominant transistor gate delay. As the delay has increased the speed has therefore decreased and also, delays can give rise to a faulty output which is undesired. With signaling in the voltage mode, insertion of buffer comes out to be very effective in delay reduction but it needs extra chip area for the buffer and also the power dissipation of buffer leads to an increment in the overall power dissipation of the circuit. But when it comes to the current mode interconnects, a low impedance is there at the output and it is found that these circuits give less delay when compared to that of voltage mode interconnect circuits. The voltage swing can't be decreased below a certain level in voltage mode circuits, as it is limited by the signal to noise ratio (SNR) required in the application. But in case of the current mode circuits, the charging and discharging currents can be increased and it results in delay reduction and therefore the current mode circuits give faster response than the voltage mode circuits.

2) **Voltage swing reduction:** When compared to the voltage mode circuits, the current mode circuits can operate at the lower voltage swings of the input signal. The output of a voltage mode circuit directly varies with the variations in the input signal, the output thus gets

distorted or noisy when the input voltage swings are reduced. As mentioned above that the voltage swing can't be decreased in voltage mode circuits below a certain level, as it is limited by the SNR required in the application, it therefore results in the slow response offered by the circuit.

3) **Supply voltage reduction:** The voltage mode circuits have an adverse effect on their performance because of the reduction in the input supply voltage and also because of the ground fluctuations. This is due to the direct linear relation of the output signal with the input signal. However in current mode circuits the output is in the form of current signal and the attenuation on the circuit performance due to the decrement in the input supply voltage is very less.

4) **Bandwidth improvement:** The bandwidth offered by the current mode circuits is higher than the bandwidth offered by the voltage mode circuits. Therefore the signals in the current mode can be transmitted faster thus offering higher speed of operation than the voltage mode circuits.

5) **Electrostatic discharge (ESD):** As with the advancement in CMOS technology size of the device is reducing, the gate oxide thickness is also getting reduced. Due to this there is an increment in the electrostatic discharge induced failures in the MOSFET. This occurs due to the breakdown of the insulators used in the gate oxide of MOSFETs. Because of the high impedance available at the input of the voltage mode circuits, electrostatic charge accumulates at the input terminal which is basically the gate of the MOSFET, the voltage mode devices are therefore in a more vulnerable condition to such failures than the current mode circuits. The input impedance of the current mode circuit is low and it doesn't allow the electrostatic charge to accumulate at the input terminal and therefore the current mode circuits are much immune to such failures and offers a safer design approach.

Therefore in summary it can be concluded that with the increased popularity of the CMOS technology, performance of the voltage mode circuits degraded and the current mode circuits gained more interest of the designers therefore increasing its popularity in the recent times. The

current mode circuits are favored because they provide efficient solutions to various problems occurred in the circuit designing and because of having advantages as mentioned in the literature like the potential to reach at higher frequencies, lower power consumption even at these high frequencies, better linearity, high slew rate availability, better accuracy, smaller chip area requirement, high immunity to the voltage fluctuations, increased speed of operation, less switching noise, low cross talk and suitability for the low voltage and low power applications. But these advantages are often fulfilled at the cost of increment in the distortion and higher gain variations [56].

1.3 THESIS STRUCTURE

CHAPTER 1: Gives introduction about the increasing demand of low power devices, increased popularity of the current mode technique, advancements in the CMOS VLSI technology and their impact on voltage mode circuits. Then explains the current mode and voltage mode approaches. It also gives the thesis structure.

CHAPTER 2: Explains the history of Current Conveyors (CCs), about their invention and their three generations. Explains the growth in popularity of the Second Generation Current Conveyor (CCII) and brief introduction about their various versions evolved with time.

CHAPTER 3: Gives introduction about the Dual-X Current Conveyor (DXCCII). Explains ideal and non ideal behavior and its parasitic model. Simulation results have also been provided at the end to justify the theory.

CHAPTER 4: Gives introduction to the precision rectifiers, various limitations of conventional Operational Amplifier (Op-Amp) based precision rectifiers. Gives a literature review about various voltage mode full wave rectifiers reported in the open literature along with a concluding summary table. Then proposed topologies of precision half and full wave rectifiers using DXCCII are explained in detail along with the simulations results.

CHAPTER 5: Introduces the various digital modulation schemes. Gives a literature survey of the reported digital modulators along with the summary table. Further, proposed BASK and BPSK modulators are explained in detail along with the simulation results.

CHAPTER 6: Concludes the overall work described in this thesis with possible future improvements. The thesis work ends with this chapter.

CHAPTER 2

HISTORY OF CURRENT CONVEYORS

2.1 THE FIRST GENERATION CURRENT CONVEYOR (CCI) [45], [46]

The concept of Current Conveyor (CC) was first proposed by K. C. Smith and A. Sedra in the year 1968 [45]. The current conveyor's circuit implementation of first order was also presented. It employed three matched npn Bipolar Junction Transistors (BJTs), two matched pnp BJTs and three matched resistors. The current conveyor has three terminals named as X, Y and Z. A voltage applied at the input terminal Y is reflected at the other input terminal X as if there is a virtual short circuit between the two terminals. In the dual manner, if some current is forced at the input terminal X, an equal amount of current flows through the input terminal Y. The current at terminal X is also conveyed to the output terminal Z. Because of its current conveying property it was therefore named as the current conveyor. This was later called as the first generation current conveyor (CCI) [46]. Figure 1 represents the block diagram of the current conveyor [46]. The relations between the input and output variables of the current conveyor are given in matrix (1) below [46].

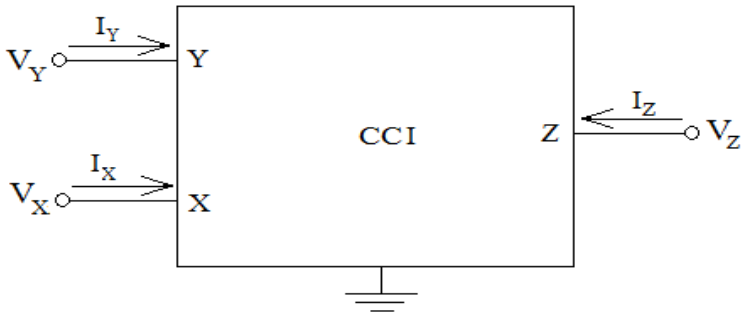

Figure 1: CCI block diagram [46]

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \quad (1)$$

The matrix can be written in equation form also as below.

$$V_X = V_Y \quad (2)$$

$$I_Y = I_X \quad (3)$$

$$I_Z = \pm I_X \quad (4)$$

The input terminal X has low impedance while the output terminal Z has high impedance, hence its current conveying action is also called as the transfer of current from a low impedance level to a high impedance level. The impedance of input terminal Y is low. The X and Z terminals if taken together can be called as the Current Controlled Current Source (CCCS) where terminal Z is working as the current source and terminal X is controlling it with the use of current.

Because of the current characteristics, the current conveyor CCI was used in several instrumentation and communication systems. Because of its voltage characteristics, it was used as voltage to current converter, digital to analog converter with current source output and used in DC offset control of the wide band signals. It was also used as negative impedance converter and as an amplifier whose gain could be controlled electronically. Because of its current mode operation it offered high speed along with reasonable accuracy [45].

2.2 THE SECOND GENERATION CURRENT CONVEYOR (CCII) [46]

The upgradation of current conveyor was done and therefore a new version of current conveyor known as the second generation current conveyor (CCII) was proposed, again by K. C. Smith and A. Sedra in the year 1970 [46]. The limitation of CCI is the low input impedance of the input terminal Y. In many applications it is considered undesirable. But in CCII there is no such limitation and all terminals are at the proper impedance level. The block diagram of CCII is same

CCI as shown below in figure 2, but the port matrix is a bit different. The port matrix [46] is given in (5) below.

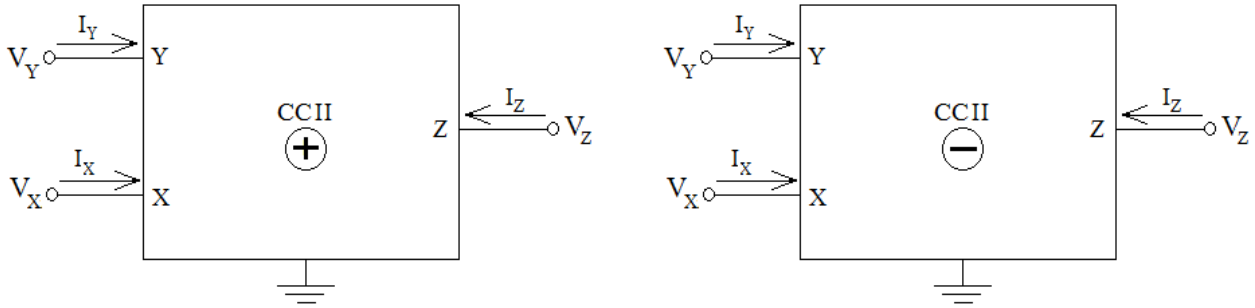

Figure 2: (a) The positive type second generation current conveyor (CCII+) [46]
(b) The negative type second generation current conveyor (CCII−) [46]

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \tag{5}$$

The matrix can thus be written in equation form as below.

$$V_X = V_Y \tag{6}$$

$$I_Y = 0 \tag{7}$$

$$I_Z = \pm I_X \tag{8}$$

The difference between CCI and CCII is the huge difference in the input impedance level of the input Y terminal. The impedance of input Y terminal of CCI is very low, while that of CCII the impedance of input Y terminal is very high. Therefore CCII can be used in more number of applications than CCI as CCII has all the terminals at the proper impedance levels. The terminal Y can be used only as the input terminal for the voltage input signal. But the terminal X can be used both ways i.e. as an input terminal for the current input signal and as an output terminal for the voltage output signal.

Further in [46], the current conveyors are also classified as the positive type current conveyor and the negative type current conveyor. If the current direction at the input X terminal and the output Z terminal is same than it is called as the positive type current conveyor (CCII+), however if the direction of currents at the input terminal X and the output terminal Z is different than the current conveyor is called as the negative type current conveyor (CCII−). Also, taking the voltage and current characteristics together, the CCII can be called as the combination of a voltage follower and a current follower.

Several applications of the CCII have also been reported in [46], they include the use of CCII in realization of the Voltage Controlled Voltage Source (VCVS), Voltage Controlled Current Source (VCCS), Current Controlled Current Source (CCCS), Current Controlled Voltage Source (CCVS), Negative Impedance Inverter (NIV), Inverting Negative Impedance Converter (INIC) and the gyrator. The application of current conveyor as the element of analog computer is also reported. For analog computation it can be used to realize various current mode functional elements, i.e. current amplifier, current differentiator, current integrator, current summer and weighted current summer.

2.3 THE THIRD GENERATION CURRENT CONVEYOR (CCIII) [47]

In the year 1995, a further updated version of the current conveyor called as the third generation current conveyor (CCIII) was introduced by A. Fabre [47]. The CCIII is all similar to the CCI in terms of the impedances of the three terminals X, Y and Z but is different from CCII when it comes

to the direction of the current at terminal Y. The direction of current flowing in terminal Y of CCIII is exactly opposite to the direction of the current flowing in terminal Y of the CCII. This is also represented in the below port matrix (9) of CCIII. The CCIII too is classified as the positive type third generation current conveyor (CCIII+) and the negative type third generation current conveyor (CCIII−).

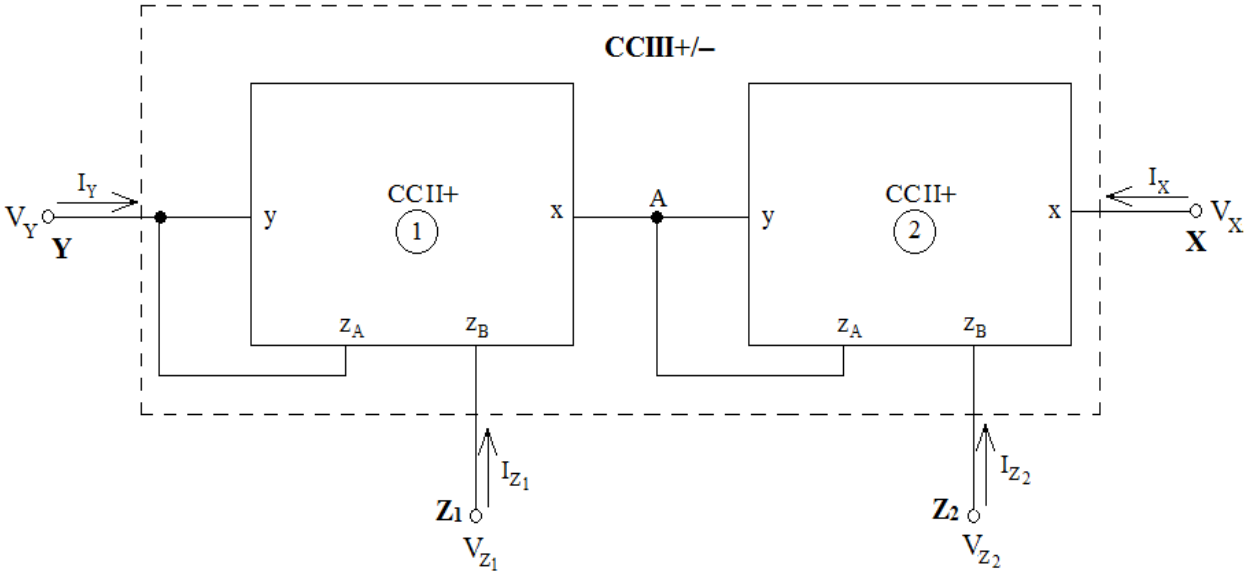

Figure 3: Block diagram of CCIII [47]

The reported block diagram [47] of the CCIII is shown above in figure 3. It employs two CCII+s with each current conveyor CCII+ having two output terminals named as z_A and z_B having the same direction of current flowing through them. The CCIII thus obtained also has the two output terminals named as Z_1 and Z_2, where currents flowing through both terminals are 180° out of phase with one another. Thus the CCIII provides both the output currents simultaneously i.e. the non inverted current as well as the inverted current or it can be concluded that the CCIII performs the operation of CCIII+ and CCIII− simultaneously.

The terminals voltage and current relations are mentioned in the matrix (9) below

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \quad (9)$$

The matrix can thus be written in equation form as below.

$$V_X = V_Y \quad (10)$$

$$I_Y = -I_X \quad (11)$$

$$I_Z = \pm I_X \quad (12)$$

The CCIII can be employed in the input section of the probes and in the current measuring devices [47].

2.4 VERSIONS OF CURRENT CONVEYORS

Although in the beginning, the current conveyor was not preferred in many applications because the advantages of current conveyor were not appreciated widely over the advantages of the conventional operational amplifier (Op-Amp) and there was no commercial availability of the integrated circuit (IC) implementation of the current conveyor. However, later in the year 1989 an IC for current conveyor was finally introduced by Wadsworth [48]. It was named as PA630, its mass production was carried out by Phototronics Ltd. of Canada. And almost at the same time

when the current conveyor's IC was introduced, the operational transimpedance amplifier's IC named AD844 was recognized to be internally consisting of CCII+ following a voltage follower [49].

Since the year 1995 particularly, there has come many modifications and improvements in the basic CCII so that it can be used more efficiently and can be employed in more number of applications. With time there increased a demand of availability of current conveyor with multiple output, hence a Dual Output Second Generation Current Conveyor (DO-CCII) was introduced which is a combination of both the CCII+ and CCII−, so that the output current in both directions can be provided. If the dual output current conveyor has the same direction of both the output currents then it is called as the Current Follower Second Generation Current Conveyor (CFCCII). Depending on the direction of the output currents, it also has its positive type and negative type versions denoted as CFCCIIp and CFCCIIn respectively [50].

Then, with the further evolution, there came many versions of current conveyors [50]. They are the Differential Voltage Second Generation Current Conveyor (DVCCII), the Differential Voltage Complementary Current Conveyor (DVCCC), the Inverting Second Generation Current Conveyor (ICCII), the Differential Difference Current Conveyor (DDCC) which is an upgradation of the current conveyor DVCCII, the Differential Difference Complementary Current Conveyor (DDCCC) which is an upgraded version of DDCC with an extra output Z terminal to provide the output current in both directions, Differential Current Conveyor (DCC) which is a current conveyor CCII with two X terminals, the modified version of DCC i.e. Modified Differential Current Conveyor (MDCC), the Dual X Second Generation Current Conveyor (DXCCII) which is a combination of CCII and ICCII, Fully Differential Second Generation Current Conveyor (FDCCII) in which the three terminals (X,Y,Z) occur in pairs, Fully Balanced Second Generation Current Conveyor (FBCCII), Modified Second Generation Current Conveyor (MCCII), Operational Floating Conveyor (OFC) which is obtained by joining the two CCII−s, Universal Current Conveyor (UCC), Modified Current Conveyor Third generation (MCCIII), Current Controlled Second Generation Current Conveyor (CCCII), Current Gain Second Generation Current Conveyor (CGCCII) [50].

The most recent version of current conveyor is the Extra X Second Generation Current Conveyor (EXCCII) [59] which has two identical input X terminals. It is much similar to DXCCII, the only difference is that in EXCCII both the X terminals produces the non inverting voltage applied at the input.

Among the various version of current conveyor, a version named as the DXCCII has been used in this thesis to propose two precision half wave rectifiers, one precision full wave rectifier, a BASK modulator and a BPSK modulator.

2.5 ADVANTAGES OF CURRENT CONVEYOR

Lately the current conveyor has gained the consideration of being a universal analog active building block as it offers several advantages as follows

- More versatility
- Low power
- More accuracy
- Availability of very high slew rates
- Availability of wider bandwidth
- Offers large dynamic range
- And the most important is the availability of the integration.

2.6 APPLICATIONS OF CURRENT CONVEYORS

It can used in a number of applications employing the current mode, voltage mode and the mixed mode operations. However its features make it more preferable for the current mode applications.

The applications of current conveyors mostly include realization of

- Filters
- Oscillators
- Precision rectifiers
- Gyrators
- Analog computation circuits
- Transfer function realization
- Inductor simulation circuits
- Frequency Dependent Negative Resistance (FDNR) device
- Grounded capacitance multiplier
- Four quadrant multiplier
- Vector summation circuit etc.

CHAPTER 3

THE DUAL-X CURRENT CONVEYOR (DXCCII)

3.1 INTRODUCTION OF DXCCII [34]

Since the CCII was first introduced [32], it had gained much attention in designing of the integrated continuous time filters. These filters required tuning in order to compensate for the behavioral deviations that occurred due to the process tolerances, effect of parasitics, effect of temperature and aging etc. But the RC filters based on the CCII failed to provide the needed tunability. Therefore, the requirement of the needed tunability for these continuous time filters led to the invention of the new active block named as the dual-X second generation current conveyor (DXCCII) [34]. The DXCCII, conceptually, is a combination of CCII [32] and ICCII [33]. It is therefore more versatile building block as it has the features of both the current conveyors i.e. CCII and ICCII.

The block diagram of DXCCII [34] is shown below in figure 4. It has 5 terminals named as Y, Xp, Xn, Zp and Zn. Xp is called as the non inverting X terminal while Xn is called as the inverting X terminal. Y is an input terminal with high impedance. Xp and Xn are terminals with low impedance while Zp and Zn are terminals with high impedance.

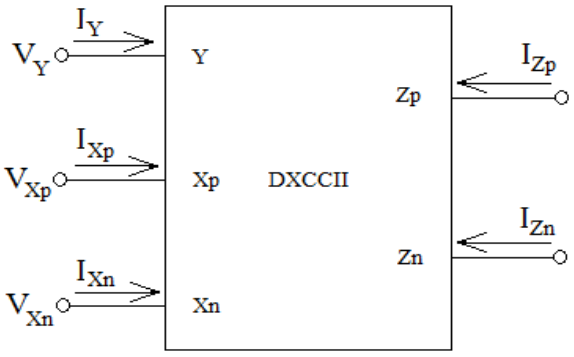

Figure 4: Block diagram of DXCCII [34]

When a voltage is applied at the Y terminal the current drawn by Y terminal is zero ideally. With the application of the voltage at Y terminal, an equal and in phase voltage is generated at the Xp terminal, and an equal but 180° out of phase voltage is generated at the Xn terminal. The current developed at Zp terminal is equal to the current developed at the Xp terminal and the current developed at Zn terminal is equal to the current developed at the Xn terminal but the currents developed at the Zp and Zn terminals have no direct relation with each other. Mathematically, it can be expressed in the matrix form [34] as mentioned below in (13).

$$\begin{bmatrix} I_Y \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \\ I_{Zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{Xp} \\ I_{Xn} \end{bmatrix} \tag{13}$$

The terminal voltage and current relations can also be written in the equation form as written below

$$I_Y = 0 \tag{14}$$

$$V_{Xp} = V_Y \tag{15}$$

$$V_{Xn} = -V_Y \tag{16}$$

$$I_{Zp} = I_{Xp} \tag{17}$$

$$I_{Zn} = I_{Xn} \tag{18}$$

Where, V_Y is the voltage applied at Y terminal. V_{Xp} and V_{Xn} are the voltages developed at Xp and Xn terminals respectively. I_{Xp}, I_{Xn}, I_{Zp} and I_{Zn} are the currents developed at Xp, Xn, Zp and Zn terminals respectively.

3.2 CMOS IMPLEMENTATION OF DXCCII [35]

Figure 5 shows the CMOS implementation of DXCCII. As mentioned already, it has cascading of the inverting and non inverting second generation current conveyors. The inversion of voltage from terminal Y to terminal Xn is done in the same way as it is done in the inverting second generation current conveyor. In order to provide the copy of the current generated at non inverting X terminal Xp to the Zp terminal, a non inverting current mirror is used. While to provide the copy of the current generated at the inverting X terminal Xn to the Zn terminal, an inverting current mirror has been used. The terminal Y needs to have high impedance and zero current drawn by it as the port matrix of DXCCII says. So in order to satisfy these needs the gate terminal of the MOSFET is used as the Y terminal, since the gate of MOSFET has very high resistance and therefore ideally no current is drawn by it. Also an NMOS transistor M_{13} and a PMOS transistor M_{15} are employed additionally in order to transfer the current generated at the Xp terminal to the Zp terminal. The total count of transistors used is twenty, out of which eleven are PMOS transistors and the remaining nine transistors are NMOS transistors.

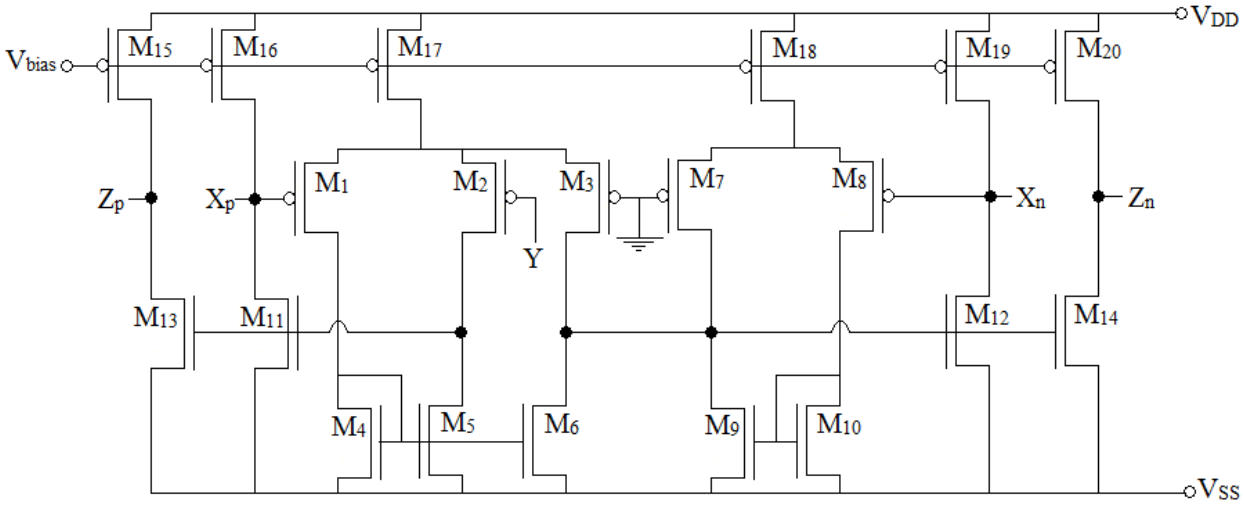

Figure 5: CMOS implementation of DXCCII [35]

The aspect ratio of transistors used in the implementation of DXCCII are given in table 3 [35].

Table 1: (W/L) Ratio of CMOS used in the DXCCII [35]

Transistor	**W(µm)**	**L(µm)**
M_1, M_2	1.4	0.7
M_3, M_7, M_8	2.8	0.7
M_4, M_5	2.4	0.7
M_6, M_9, M_{10}	4.8	0.7
M_{11} to M_{20}	9.6	0.7

3.3 NON IDEAL MODEL OF DXCCII [35]

Four parameters are introduced which describe the non ideal behavior of the DXCCII. These are, the voltage transfer gains i.e. α_p and α_n, and the current transfer gains i.e. β_p and β_n. Ideally value of all these parameters is unity. But practically they are not exactly unity but much close to unity for a very high range of frequencies i.e. in Giga hertz (GHz) range [35].

Because of the non idealities in the DXCCII, the port matrix [35] can therefore be modified as shown below in (19).

$$\begin{bmatrix} I_Y \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \\ I_{Zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha_p & 0 & 0 \\ -\alpha_n & 0 & 0 \\ 0 & \beta_p & 0 \\ 0 & 0 & \beta_n \end{bmatrix} \begin{bmatrix} V_Y \\ I_{Xp} \\ I_{Xn} \end{bmatrix} \quad (19)$$

The terminal voltage and current relations in the equation form is also modified then, as written below

$$I_Y = 0 \tag{20}$$

$$V_{Xp} = \alpha_p V_Y \tag{21}$$

$$V_{Xn} = -\alpha_n V_Y \tag{22}$$

$$I_{Zp} = \beta_p I_{Xp} \tag{23}$$

$$I_{Zn} = \beta_n I_{Xn} \tag{24}$$

Here

α_p is the voltage transfer gain from Y to Xp terminal.
α_n is the voltage transfer gain from Y to Xn terminal.
β_p is the current transfer gain from Xp to Zp terminal.
β_n is the current transfer gain from Xn to Zn terminal.

α_p, α_n, β_p, β_n are given by the following equations below.

$$\alpha_p = 1 - \varepsilon_{Vp} \tag{25}$$

$$\alpha_n = 1 - \varepsilon_{Vn} \tag{26}$$

$$\beta_p = 1 - \varepsilon_{Ip} \tag{27}$$

$$\beta_n = 1 - \varepsilon_{In} \tag{28}$$

Where

ε_{Vp} is the voltage tracking error at Xp terminal.

ε_{Vn} is the voltage tracking error at Xn terminal.

ε_{Ip} is the current tracking error at Zp terminal.

ε_{In} is the current tracking error at Zn terminal.

ε_{Vp}, ε_{Vn}, ε_{Ip}, ε_{In} are zero ideally but practically they are much smaller than one, i.e.

$$\varepsilon_{Vp} \ll 1 \tag{29}$$

$$\varepsilon_{Vn} \ll 1 \tag{30}$$

$$\varepsilon_{Ip} \ll 1 \tag{32}$$

$$\varepsilon_{In} \ll 1 \tag{32}$$

Theoretically α_p, α_n, β_p, β_n are also defined by the following equations below.

$$\alpha_p = \frac{V_{Xp}}{V_Y} \tag{33}$$

$$\alpha_n = \left|\frac{V_{Xn}}{V_Y}\right| \tag{34}$$

$$\beta_p = \frac{I_{Zp}}{I_{Xp}} \tag{35}$$

$$\beta_n = \frac{I_{Zn}}{I_{Xn}} \tag{36}$$

Where

V_Y is the voltage applied at Y terminal.

V_{Xp} and V_{Xn} are the voltages developed at Xp and Xn terminals respectively.

I_{Xp}, I_{Xn}, I_{Zp} and I_{Zn} are the currents developed at Xp, Xn, Zp and Zn terminals respectively.

3.4 PARASITIC MODEL OF DXCCII [35]

There are various parasitic resistances and capacitances at the terminals of DXCCII. The two X terminals have only parasitic resistance associated with them while the Y terminal and the two Z terminals have both, the parasitic resistance as well as the parasitic capacitance associated with them. The block diagram of DXCCII revealing its associated parasitics is shown in figure 6 [35].

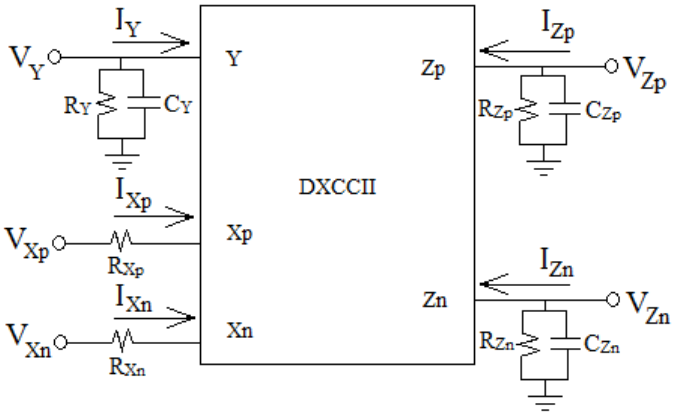

Figure 6: DXCCII parasitic model [35]

It can be observed from the block diagram that for the terminals Y, Zp and Zn, the respective parasitic resistance and the parasitic capacitance appears in parallel combination with each other, this parallel combination being connected between the respective terminal and the ground.

The notation of the various parasitic resistances and capacitances shown in the above block diagram are described as follows.

R_{Xp} and R_{Xn} are the parasitic resistances of the Xp and Xn terminals respectively.

R_Y and C_Y are the parasitic resistance and capacitance of the Y terminal.

R_{Zp} and C_{Zp} are the parasitic resistance and capacitance of the Zp terminal.

R_{Zn} and C_{Zn} are the parasitic resistance and capacitance of the Zn terminal.

The parasitic resistances of X terminal i.e R_{Xp} and R_{Xn} are much smaller in magnitude. While the parasitic resistances of Y, Zp and Zn terminals i.e. R_Y, R_{Zp} and R_{Zn} are much higher in magnitude. Further, this assumption is taken in to consideration that the circuits employing DXCCII are restricted to perform correctly only for the frequencies which are much lower than the corner frequencies of the various voltage and current gains i.e. α_p, α_n, β_p, β_n. Also, practically the parasitic resistances at Y, Zp and Zn terminals are assumed to be much higher in value than the value of the external resistors used in the DXCCII based circuit, but the value of these external resistors is assumed to be much higher than the parasitic resistances value of the Xp and Xn terminals [35].

3.5 ADVANTAGES OF DXCCII

DXCCII basically consists of the main advantages of CCII and ICCII. With the addition of a triode MOSFET efficient tunability is provided without affecting the high linearity for the large signals. This tunability helps to compensate for the behavioral deviations that occurred due to the process tolerances, effect of parasitics, effect of temperature, aging etc. The dual-X terminals provides the added features such as inverting input voltage is also available at its Xn terminal other than the non inverting input voltage at its Xp terminal, therefore these added features helped to reduce the elements count used in the continuous time filters [34].

Also, like the other current mode active blocks, the DXCCII provides some superior features over its voltage mode equivalent [37]. These features are as follows

- The usable gain is higher.
- At the sensitive nodes the voltage excursion is further reduced.
- Greater linearity.
- Power dissipation is less.
- Wider bandwidth.

- Accuracy is better.
- Larger dynamic range.

3.6 APPLICATIONS OF DXCCII

There are a variety of applications employing the DXCCII as the active block as reported in the open literature such as a tunable gyrator, current mode biquad filter using tunable gyrator, grounded inductance design, oscillator design, and filter design etc. Some of these applications are mentioned below.

- After the DXCCII was proposed, it was first employed in the applications to make a tunable transconductor, voltage mode lossless and lossy integrator, current mode lossless and lossy integrator, current mode Tow Thomas filter and a current mode sinusoidal oscillator [34].

- The four quadrant analog multiplier have been proposed with two topologies, the first one uses one DXCCII while the second one uses two DXCCII [36].

- A precision voltage mode full wave rectifier has been proposed with only one DXCCII and three NMOS transistors. It has high input impedance which supports its easy cascading [37].

- Further a new CMOS implementation of DXCCII has been reported to improve its performance and a vector summation circuit is proposed which uses two DXCCIIs along with seven MOS transistors [38].

- The hardware realization of DXCCII with commercially available ICs has been reported. Fourteen hardware implementations are proposed. Seven implementations employ only AD844 ICs and the other seven implementations employ AD843 opamps ICs and AD844s

ICs. The total number of ICs used is every proposed implementation is four. Also all of these implementations have additional advantage of availability of the buffered voltage outputs, which is not provided in the conventional DXCCII. A quadrature oscillator has been also been proposed with these hardware implementation. Further feature enhancement is done of DXCCII and thus a gain variable DXCCII has been proposed [39].

- A tunable grounded capacitance multiplier has been presented, it uses only one DXCCII block [40].

- A new CMOS DXCCII has been proposed and it is used to realize a FDNR (Frequency Dependent Negative Resistance) element [41].

- Differential Voltage Dual-X second generation Current Conveyor (DV-DXCCII) has been used in the proposed all pass filter of first order, it gives both inverting and non inverting responses [42].

- First and second order current mode all pass filter has been proposed using a multiple output DXCCII (MO-DXCCII). Four Z terminals are there in the MO-DXCCII. [43]

- Differential Voltage Dual-X Current Conveyor (DV-DXCCII) has been used to propose a fully differential first order all pass filter [44].

- Recently a digital modulator circuit has also been proposed which can perform BASK and BPSK modulation processes simultaneously. The modulator uses only one DXCCII along with two NMOS transistors and three grounded resistors [59].

3.7 SIMULATION RESULTS OF DXCCII

The various characteristics of DXCCII are simulated using PSpice software. 0.35µm CMOS technology parameters are used. The supply voltage for the active block DXCCII [35] is taken as $\pm$1.8V and the voltage V_{bias} is set to 1.05V.

The transient response of the terminals Xp and Xn for a sinusoidal excitation with a frequency of 500KHz at the input terminal Y (figure 7) is shown in figure 8. It can be observed that the non inverted and inverted input voltage signal are produced at the terminal Xp and Xn respectively.

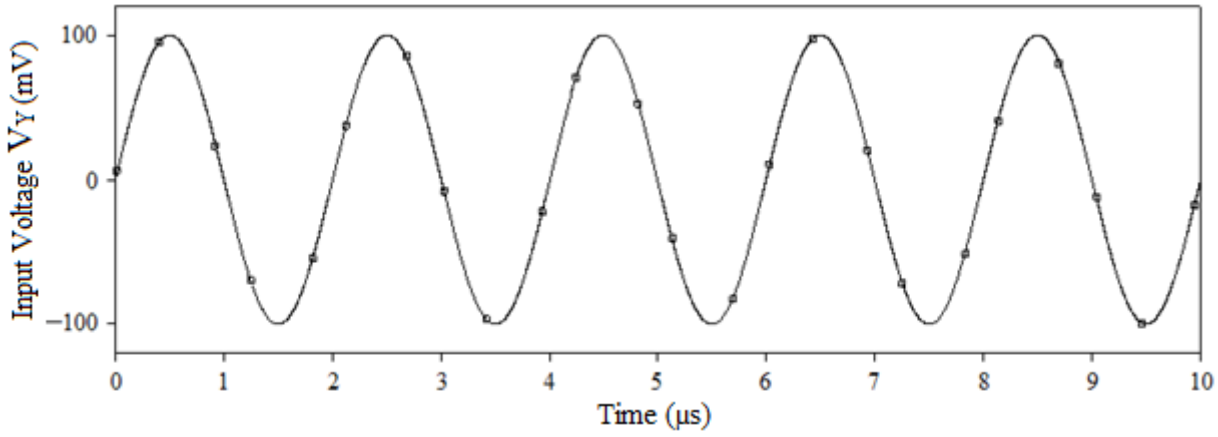

Figure 7: Input voltage, V_Y

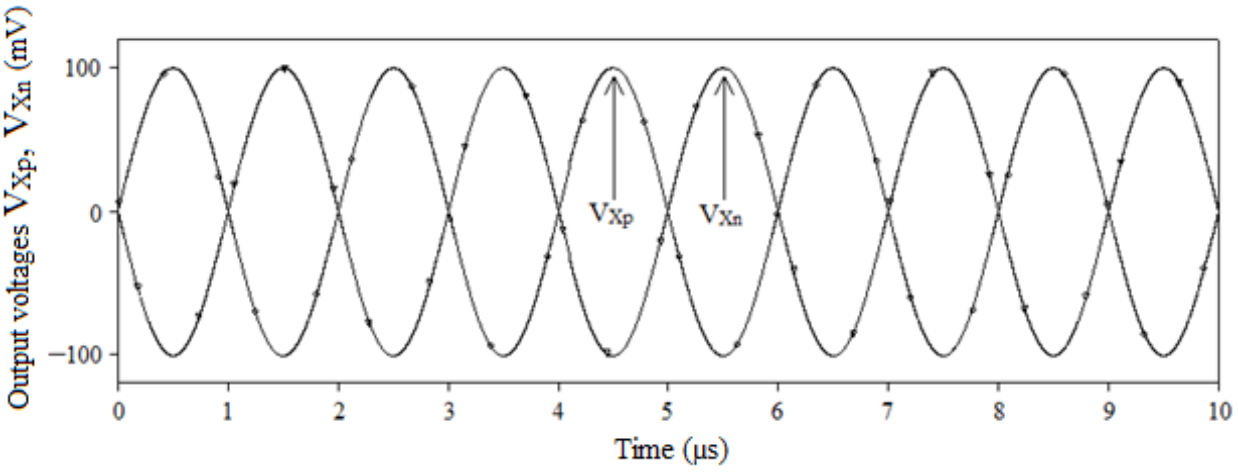

Figure 8: Output voltages, V_{Xp}, V_{Xn}

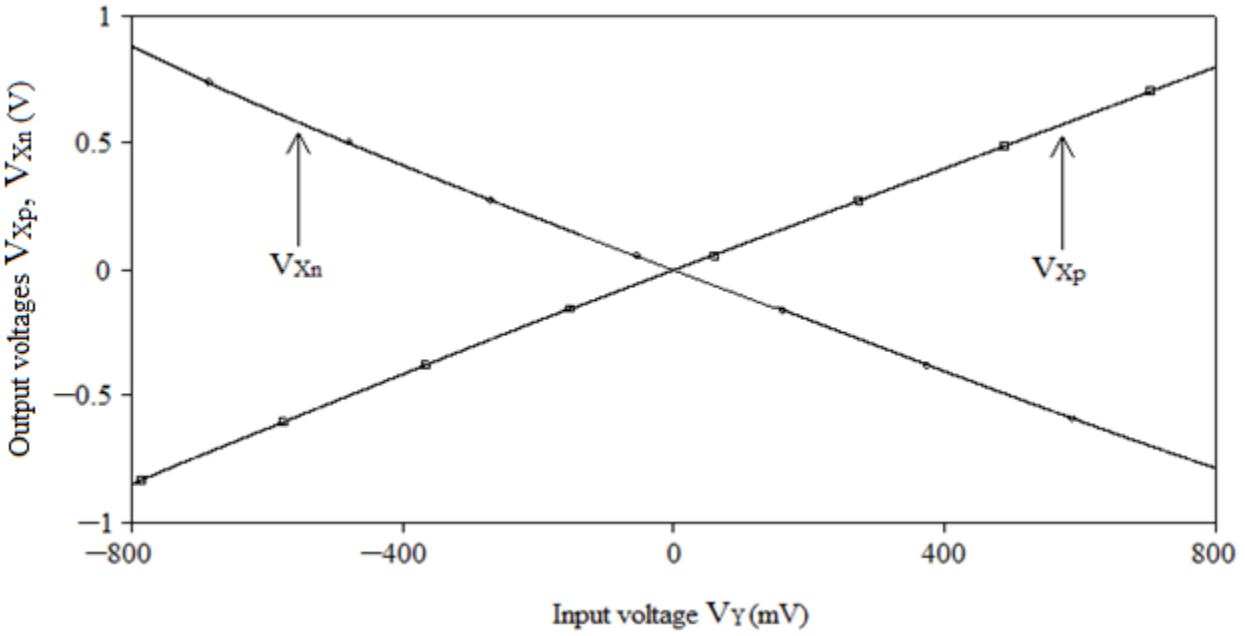

Figure 9: DC voltage characteristics of terminals Xp and Xn

Figure 9 shows the DC voltage characteristics of terminals Xp and Xn. It can be observed that as the input voltage signal applied at terminal Y varies, the output voltages at the terminals Xp and Xn also varies linearly.

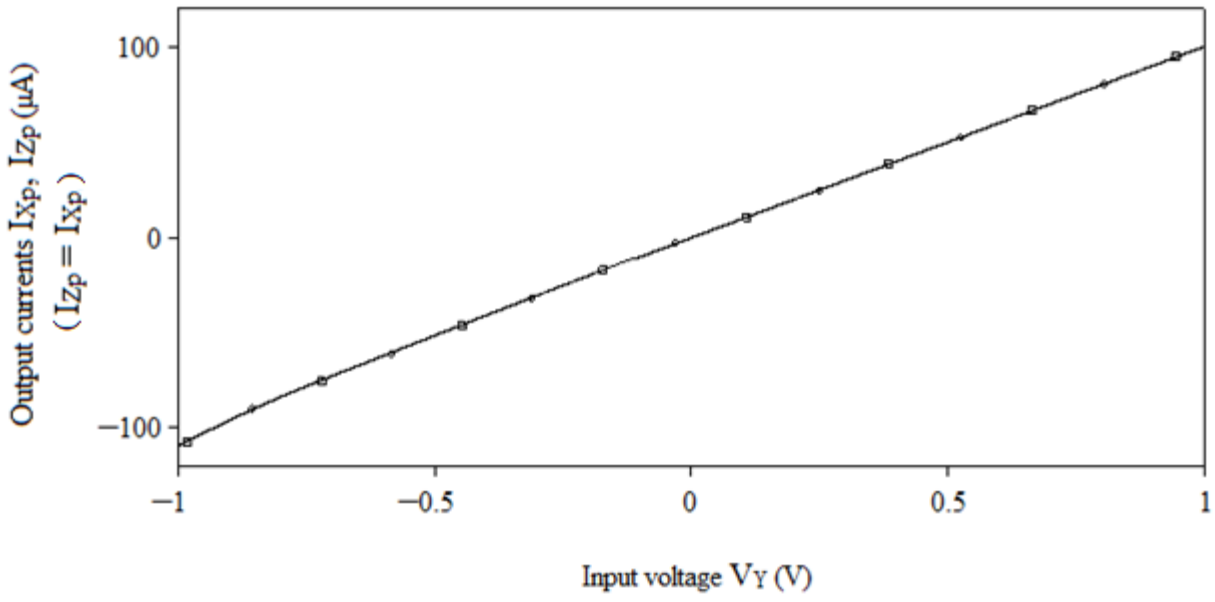

Figure 10: Variation in the output currents, I_{Xp} and I_{Zp} with input voltage, V_Y

Figure 10 shows the linear variation in the output currents at terminals Xp and Zp with the variation in the input voltage at terminal Y. It also shows that currents at the terminals Xp and Zp are equal.

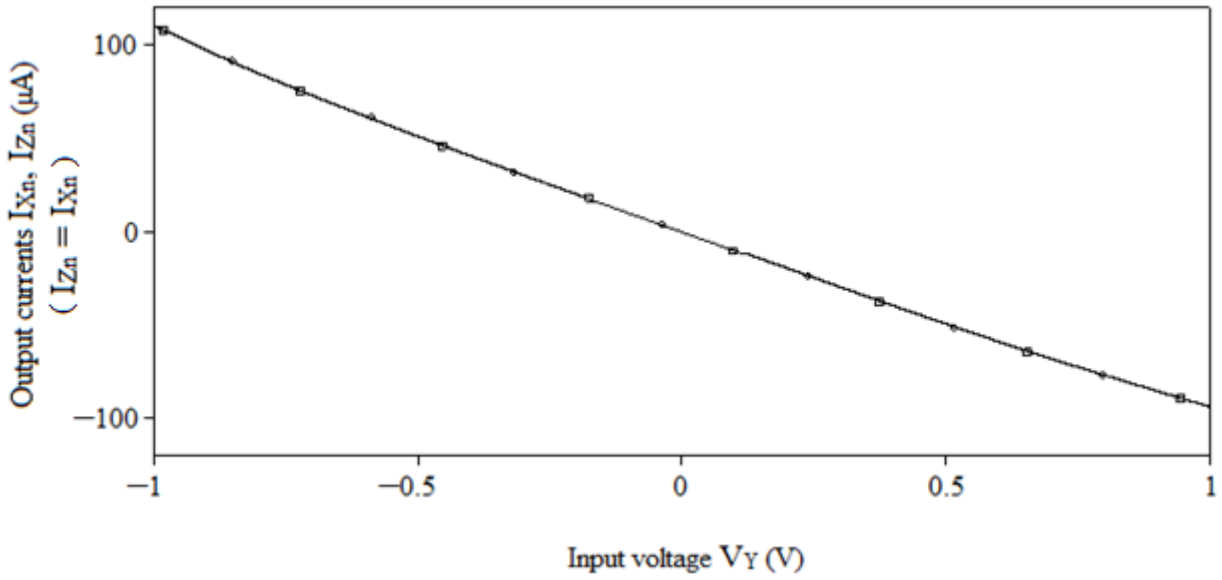

Figure 11: Variation in the output currents, I_{Xn} and I_{Zn} with input voltage, V_Y

Figure 11 shows the linear variation in the output currents at terminals Xn and Zn with the variation in the input voltage at terminal Y. It also shows that currents at the terminals Xn and Zn are equal.

Figure 12 shows the DC current characteristic of terminal Zp. It can be observed that the output current at terminal Zp is exactly same as the applied input current at terminal Xp.

Figure 13 shows the DC current characteristic of terminal Zn. Here also it can be observed that the output current at terminal Zn is the exact copy of the input current applied at the terminal Xn.

Figure 14 shows the linear variation in the output currents, I_{Xp} and I_{Zp} with the voltage, V_{Xp}.

Figure 15 shows the linear variation in the output currents, I_{Xn} and I_{Zn} with the voltage, V_{Xn}.

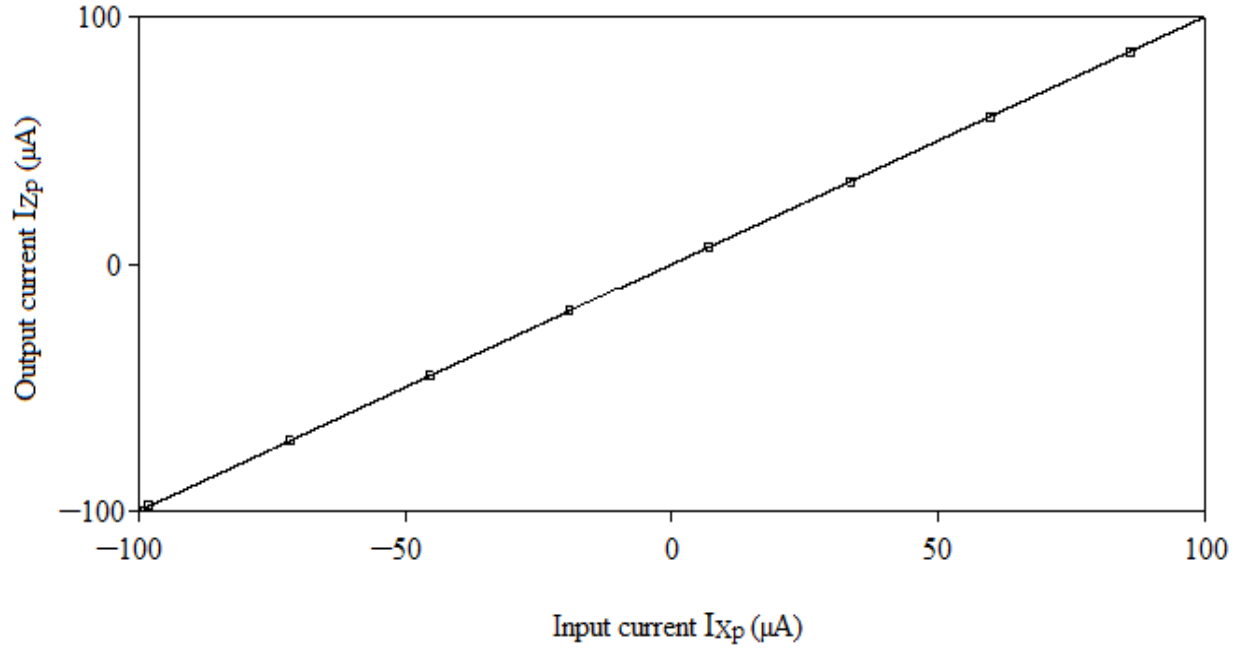

Figure 12: DC current characteristic of terminal Zp

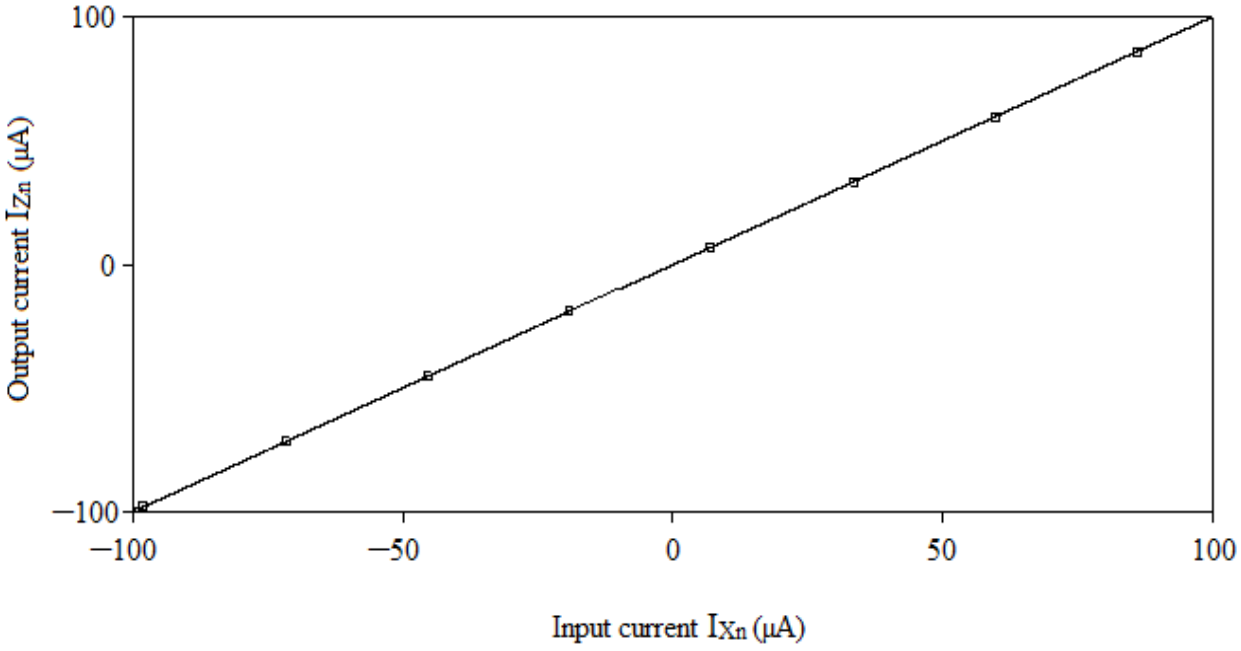

Figure 13: DC current characteristic of terminal Zn

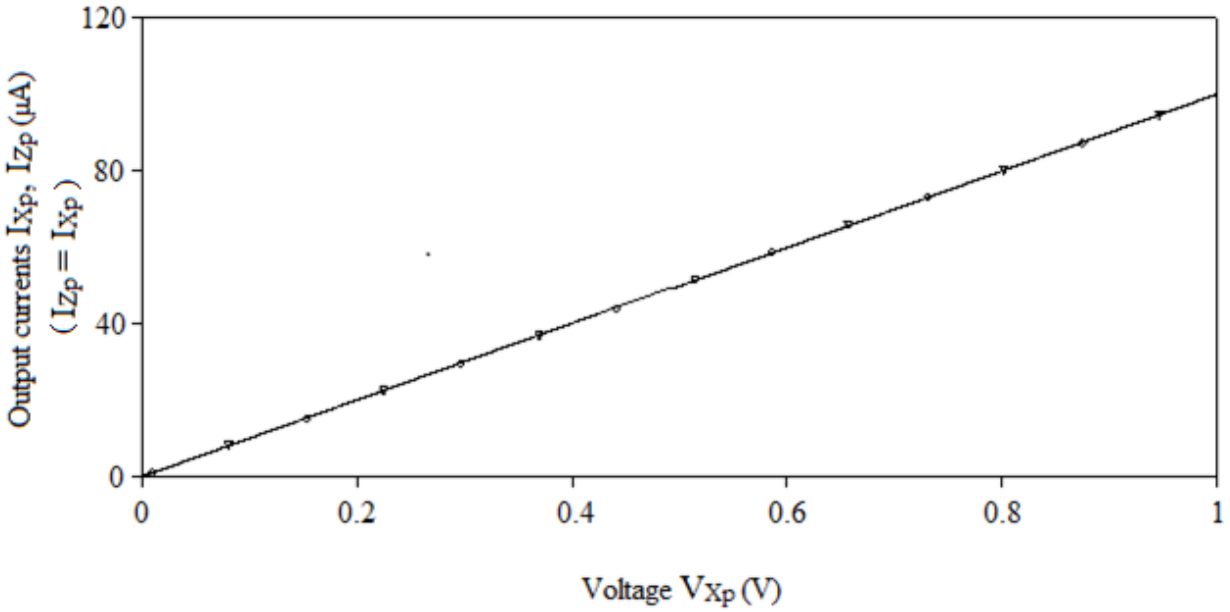

Figure 14: Variation in the output currents, I_{Xp} and I_{Zp} with the voltage, V_{Xp}

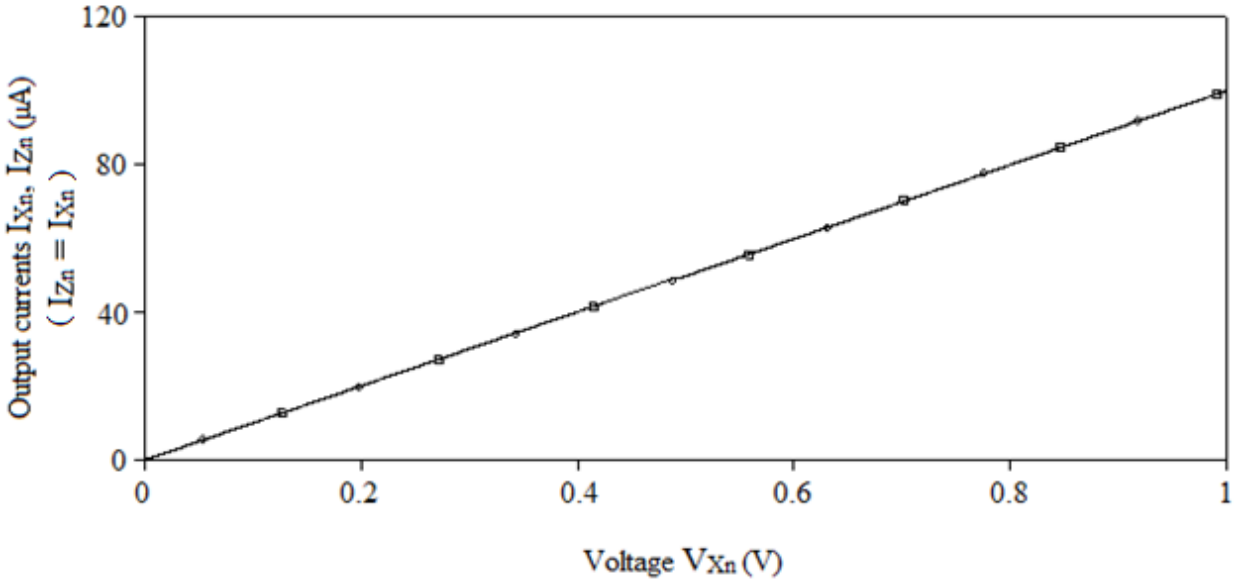

Figure 15: Variation in the output currents, I_{Xn} and I_{Zn} with the voltage, V_{Xn}

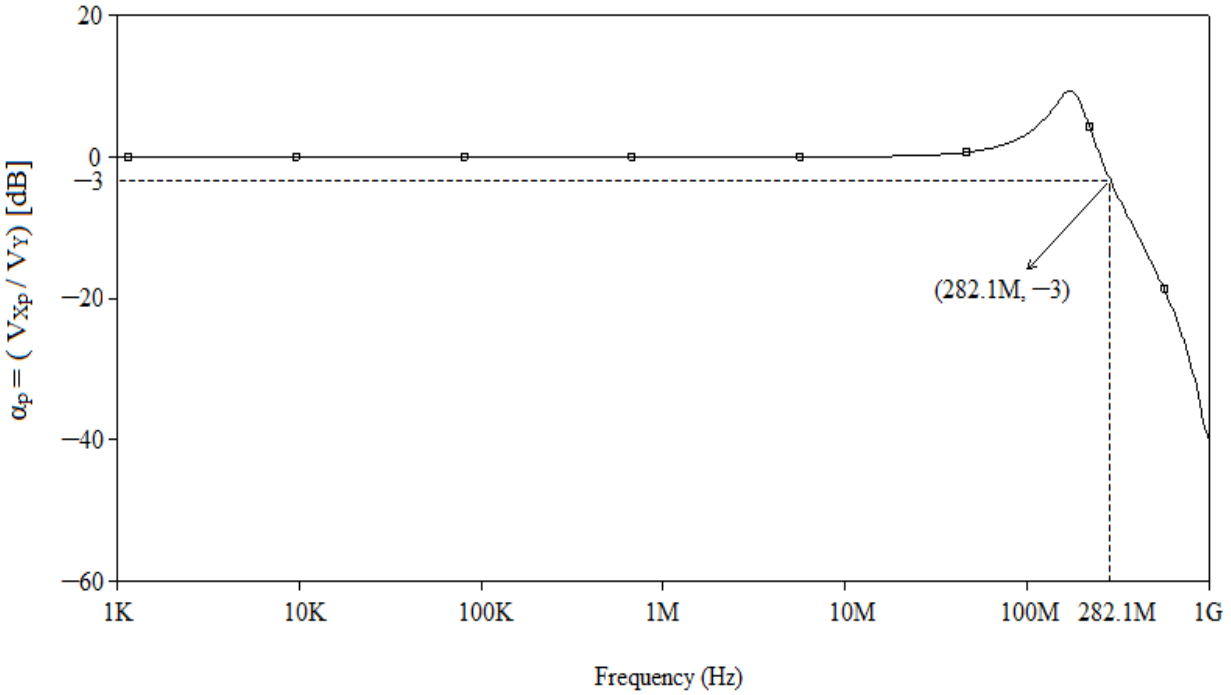

Figure 16: Simulated frequency response of the voltage gain, α_p from terminal Y to terminal Xp

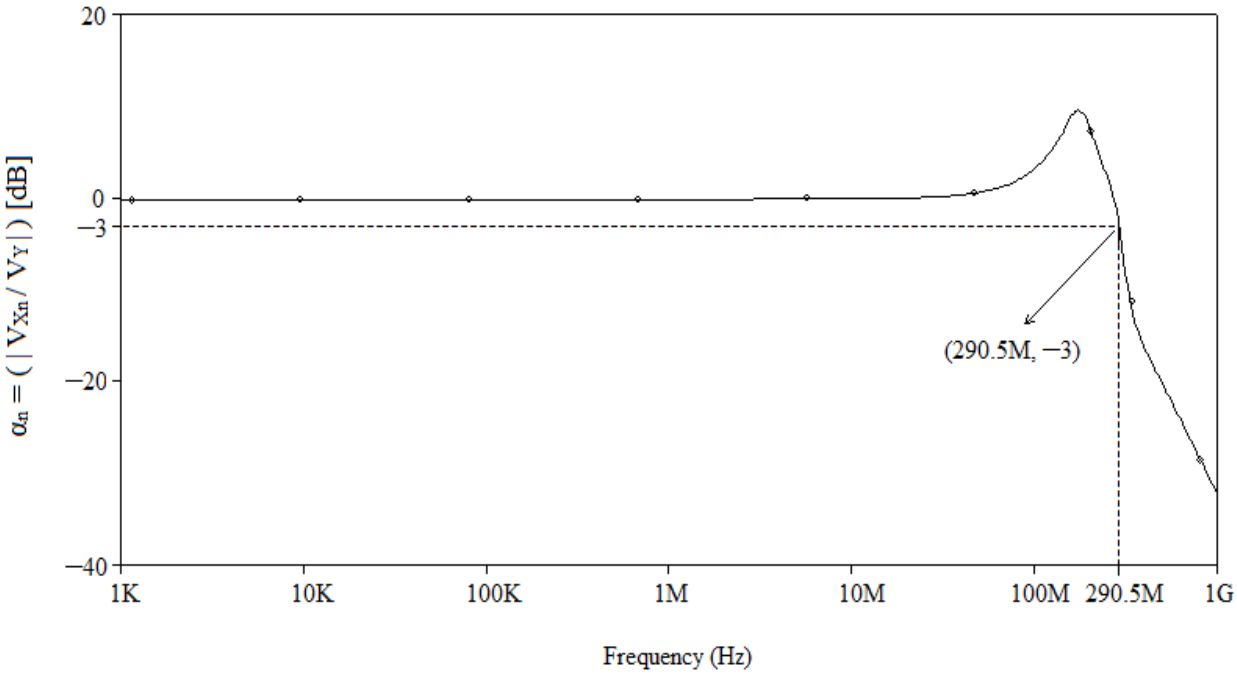

Figure 17: Simulated frequency response of the voltage gain, α_n from terminal Y to terminal Xn

Figure 16 above shows the simulated frequency response of the voltage gain, α_p from terminal Y to terminal Xp. The simulated 3 dB cut off frequency for the voltage gain, α_p is observed to be 282.1 MHz.

Figure 17 above shows the simulated frequency response of the voltage gain, α_n from terminal Y to terminal Xn. The simulated 3 dB cut off frequency for the voltage gain, α_n is observed to be 290.5 MHz.

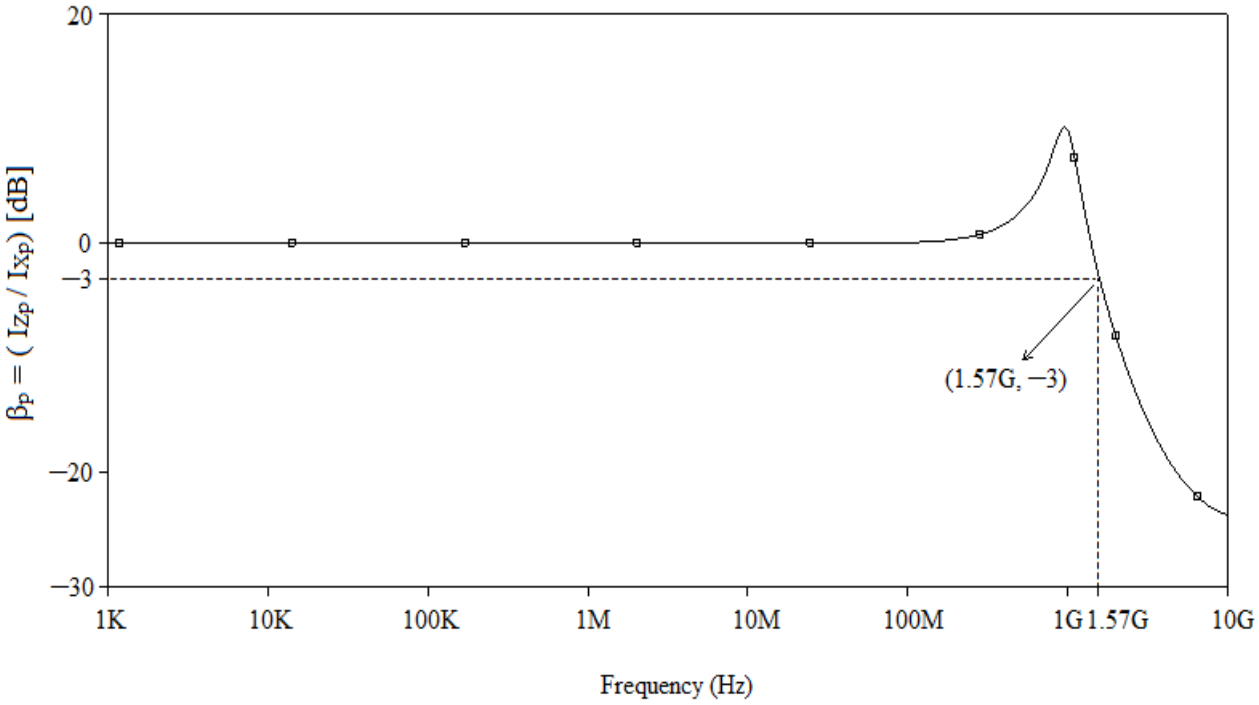

Figure 18: Simulated frequency response of the current gain,β_p from terminal Xp to terminal Zp

The simulated frequency response curve for the current gain, β_p from terminal Xp to terminal Zp is shown above in figure 18. The 3 dB cut off frequency is observed to be 1.57 GHz.

CHAPTER 4

RECTIFIERS

4.1 INTRODUCTION OF RECTIFIERS

The rectifier is a device that converts AC (Alternating Current) signal that periodically reverses direction into the pulsating DC (Direct Current) signal that flows only in one direction. This process of conversion of a bidirectional signal in to a unidirectional signal is known as rectification.

For large signals the concept of rectification is well developed. However, with time there has been a growth in the demand of portable circuits that can operate on low supply voltages. This therefore raised the need of such circuits that can process naturally occurring very small analog signals and can handle the frequencies associated with them. One such circuit is precision rectifier. Much research studies have now been focused on designing such rectifiers which can rectify very small signals, these rectifiers are referred as the precision rectifiers.

In the conventional rectifiers, simply diodes can be used for rectification. But these conventional diode rectifiers fail to rectify those signals whose amplitudes are below the cut in voltage of the diode. For example, the semiconductor silicon (Si) diode has a cut in voltage of 0.7 V and germanium (Ge) diode has a cut in voltage of 0.3 V, therefore the rectifier using silicon diodes fails to rectify the signals in the range from -0.7 V to 0.7 V while the rectifier using germanium diodes fails to rectify the signals in the range from -0.3 V to 0.3 V [26]. Therefore the conventional diode only rectifiers, for example half wave rectifier, full wave bridge rectifier and full wave center tapped rectifier, are employed in those applications only where rectification in the range of cut in voltages of the diodes is of less importance, for example in Radio Frequency (RF) demodulation, in DC voltage supplies etc. Since the cut in voltages of the semiconductor diodes don't allow the conventional rectifiers to be used in those cases where rectification of low level voltage signals is needed, precision rectifiers using active elements have to be employed.

In the last few decades such precision rectifiers have been developed using operational amplifier (Op-Amp) and passive components such as diodes and resistors, often with the matching conditions of these resistors, and many of these external passive components are in the floating condition. Many precision rectifiers employing Op-Amp, passive components such as diodes and resistors have been reported in the open literature. In these rectifiers the diodes are connected directly to the output terminal of the active block [26], [31].

But there are certain limitations of the precision rectifiers making use of Op-Amps. Due to the voltage mode processing of the operational amplifiers, their Slew Rate (SR) is limited. This gives rise to a classical problem known as the corner distortion. It's a distortion that occurs during the zero crossings of the input signal because the diodes and Op-Amp have to recover during the transition from the conducting state to the non conducting state and vice versa with in finite small signal slew rate. This distortion is more for the low level signals. The employment of high slew sate Op-Amps does not solve this problem either, since this problem is a small signal transient problem [6]. These limitations therefore restricts the correct operation of the conventional Op-Amp based precision rectifiers to low frequencies only. These low frequencies are much lower than the gain bandwidth product of the operational amplifier used. Also, since these conventional precision rectifiers use Op-Amp and resistors, these are therefore not suitable for the IC fabrication. These conventional precision rectifier circuits also give rise to noise problems associated with the resistors used in them.

An improvement in the precision rectification of high frequency signals has been achieved by using the current mode technique [10]. Current mode or current sensing approach has several advantages over the voltage mode counterparts, for example current mode approach offers higher frequency of operation, larger dynamic range, wider bandwidth, and also the offset value is lower at the zero crossing areas of the input signal. Therefore high frequency rectification could be achieved using current mode technique.

Although the current mode circuits provide the advantage of high frequency precision rectification, some of the reported precision rectifiers which achieved this improvement employing the CCs are not ideal for the IC fabrication because they make use of either grounded or floating resistors. In

addition to this, some of the precision rectifiers need two identical CCs. Mismatching of these affects the output of the full wave precision rectifier, that is, the amplitude of the first half cycle may be different than the amplitude of the second half cycle of the full wave rectified output waveform [10].

In general, it can be said that the precision rectifier circuits have been developed with diodes, active analog building blocks, for example CCIIs, Op-Amps, etc. or both [1-3, 5, 7, 9-18, 20, 27]. CCIIs provides a very high Slew Rate and bandwidth in comparison to the conventional Op-Amp. This makes CCIIs of primary importance when it comes to the design of modern analog ICs.

Other rectifiers have been developed with different active building blocks for example precision rectifiers making use of the Operational Trans conductance Amplifiers (OTAs) [19, 22, 23] provide the attractive feature of IC implementation, some of them nevertheless suffer from the application of a large number of active components and limitation to the high frequency performance.

Recently efforts have been made to replace diode with active elements, for example a MOS transistor is employed in place of diode for switching purpose. In this thesis also two MOS transistors are employed in the newly proposed precision full wave rectifier using DXCCII as the active building block. In addition, there have been several rectifiers reported in the literature that make use of only MOS transistors and no passive element is used in their construction. Such precision rectifiers are very suitable for the Complementary Metal Oxide Semiconductor (CMOS) technology IC implementation. One benefit of the IC precision rectifiers developed by making use of the simple active blocks such as Op-Amps, CCs and active or passive elements such as transistors, diodes and resistors as components, is that they can be fabricated in many countries.

4.2 CLASSIFICATION OF RECTIFIERS

- They are basically of two types when the alternating voltage used as input is concerned. They are:

    1) Single phase rectifiers
    2) Poly-phase rectifiers (for example: 3-phase rectifier)

- When the switching device used is taken in to account the rectifiers have two categories, that is:

    1) Uncontrolled rectifiers
    2) Controlled rectifiers

  Also, as per the of functionality limitation of the switching device is concerned there can be a sub division also named as half controlled rectifiers.

- When the period of conduction is concerned rectifiers have two categories. They are:

    1) Half-wave rectifiers
    2) Full-wave rectifiers

  Full wave rectifiers can further have two classifications when the nature of the circuit connections is concerned. They are:

    1) Centre tapped full-wave rectifier
    2) Bridge full-wave rectifier

- Synchronous rectifiers: When the active element is employed for switching purposes instead of diodes than the rectifier is called as the synchronous rectifier or active rectifier. To overcome the diode losses active elements are used in place of diodes and it significantly improves the efficiency levels also.

In view of the availability of a variety of different types of rectifier circuits, there is often a good choice available to the user of which type of rectifier to use. In many cases it depends on the level of performance required, and usually a type of full wave rectifier is required. Usually bridge full wave rectifier is the cheapest option as it is available with low cost rather than center taped transformer type full wave rectifier where less diodes are used in comparison with bridge rectifier but it requires a center taped transformer which is expensive. Now in the modern power supplies which require high level of efficiency, the designers are looking to employ the synchronous or active rectifiers. Though synchronous or active rectifiers are more complicated and therefore are more costly, but still this increased cost often gives the returns in terms of increasing the level of efficiency.

4.3 SWITCHING DEVICES USED IN RECTIFIERS

One of the most important component that needs to be considered in power electronics before designing of any circuit is the switching device. It is assumed that switching device will behave as an ideal switch but it is not practically true. There can be two groups when it comes to the classification of the switching devices. They are

1) Uncontrolled Switching Device

An example of uncontrolled switching device is diode whose state completely depends on the power circuit that is connected externally to it. Ideally a diode has two states of operation, first is ON state (or forward biased state) where diode is considered to be an on switch or closed switch and second is OFF state (or reverse biased state) where diode is considered as an off switch or open switch. During forward-biased condition of the diode,

ideally the voltage across its terminals is zero, no matter what amount of current is flowing through it. While during reverse-biased state of the diode, ideally no current flows through it or say the current flow through the diode is zero no matter what the voltage across its terminals is, provided the reversed biased voltage doesn't exceed the reverse breakdown voltage of the diode. Diodes find applications in the designing of rectifiers, voltage clipper, voltage clamper, schmitt trigger, constable multivibrator, voltage multiplier etc.

2) **Controlled switching device**

In this category, there are semi-controllable and fully-controllable switches. Semi-controllable switches are like thyristors and fully-controllable switches are like BJT (Bipolar Junction Transistor**)**, JFET (Junction Field Effect Transistor), MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) etc.

Below is a brief introduction of various types of active devices used in the rectifiers.

1) **Thyristors -** There are three terminals in a thyristor called as anode terminal, cathode terminal and gate terminal. It is made up with four semiconductor material layers. There can be three modes or states of operation of a thyristor called as reverse blocking mode or state, forward blocking mode or state and forward controlling mode or state.

When the thyristor is operated in the reverse blocking mode, the direction of application of voltage across thyristor is same as the direction of voltage applied in a reversed biased diode and no current flows through it. When the thyristor is operated in forward blocking mode or state, the application of voltage applied across it has the same direction as the direction of voltage applied in a forward biased diode is, and still the current flow through it is zero and there is a control on the trigger of the thyristor into conduction state via its gate terminal. And during the forward conducting mode of operation, the thyristor is made to conduct by triggering it with its gate terminal and current begins to flow through it and voltage drop across it reduces to a very small value, now it will turn off only when the

current flowing through it is made to fall below a certain threshold value called as the holding current.

Thyristors have many types, for example - SCR, MOS-controlled thyristor, optically triggered thyristor, static induction thyristor.

2) **BJT (Bipolar Junction Transistor) –** BJT is a current-controlled switch and can be considered as combination of two diodes connected in as way where the anode terminals of both diodes are shorted. BJT has three terminals named as the base, collector and the emitter terminal. The base current is required to be supplied to turn on the BJT. The input resistance of the BJT is low and it is a temperature sensitive device. In a BJT the internal current is due to both electrons and holes i.e. it is bipolar while the external current is only due to electrons i.e. it is unipolar. BJTs are now being replaced by MOSFETs for they have better efficiency, more thermal stability and low power dissipation.

3) **MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) –** MOSFET is an electric field controlled device. The MOSFET has four terminals named as the gate, drain, and source terminal and has the additional fourth terminal called as the body or base or substrate. MOSFET has negligible power dissipation. Input resistance of the MOSFET is high. It is a symmetrical and voltage controlled device of which the high input resistance is due to silicon dioxide. The source, drain and gate terminals of a MOSFET are similar to the emitter, collector and base terminals of a BJT. MOSFET is basically like a capacitor and it is a less noisy device than the BJT and has better thermal stability than BJT. MOSFET requires less than the 5% of the area required by the BJT thus MOSFET provides high packing density.

In general, with the same configuration of the rectifier, there is a large variation in the efficiency when different switching devices are used that is the efficiency of rectifier varies by varying the switching device used in it.

4.4 SYNCHRONOUS RECTIFIER: ACTIVE RECTIFIER

When in a rectifier, the active building blocks and active switching elements are used in place of semiconductor diodes, then it is called as the synchronous rectifier. The diode rectifiers can't be used to provide rectification of low amplitude voltage signals as a practical diode has some turn on voltage, so until the diode turns on no output is provided by the diode rectifiers, therefore the efficiency of these rectifiers is poor and thus synchronous rectifiers are employed in the place of diode rectifiers because they can rectify even low amplitude signals and therefore provide much better efficiency. In a diode rectifier, during forward biased state the diode turns on and during reverse biased state the diode turns off, this on and off switching mechanism can be provided with the active element too by controlling it in such a way and thus it can provide the same effect as the diode does in the diode rectifier and this forms the basis of synchronous rectification. As the switching of the active element has to be timed correctly, it is actually in synchronism with the waveform being rectified, it is for this reason that these rectifiers are known as synchronous rectifiers or sometimes also called as active rectifiers in the sense that they use active elements. Examples of active switching elements include the transistors that can be power BJTs or power MOSFETs that are turned on and off at the needed times to allow the rectification of the signal to occur.

The advantage with an active rectifier is that the conducting resistance and voltage drop are much less than they are with diodes and thus efficiency level is very high.

The downside of the active rectifiers is the need of a control circuitry to ensure the needed synchronization. Circuitry needed for the control of active rectifier usually includes the voltage level detectors and a drive circuity to drive the active elements.

When there is a need of much higher efficiency levels in some of the power supplies, synchronous or active rectifiers are used. These rectifiers are costly as they need more components but the performance provided by them is far better than the performance provided by the ordinary diode rectifiers. Synchronous rectification enables the minimization of power losses and improvement in the efficiency levels but at the cost of additional circuit complexity.

4.5 FULL WAVE RECTIFIER ADVANTAGES AND DISADVANTAGES

Though a full wave rectifier needs more number of diodes or active elements than the half wave rectifier, it gives an advantage of using both halves of the input supply AC voltage waveform in order to provide the rectified output.

4.5.1 FULL WAVE RECTIFIER ADVANTAGES

- Utilizes both cycles i.e. positive as well as negative cycle of the input AC waveform.
- It is easier to provide smoothing because of the increased ripple frequency.
- The average DC output voltage of a full wave rectifier is higher than that of the half wave rectifier.

4.5.2 FULL WAVE RECTIFIER DISADVANTAGES

- It has more complicated circuit when compared with half wave rectifier circuit.
- The ripple frequency is twice than that of half wave rectifier thus this increased ripple frequency hum may be more audible on an audio circuit.

In view of the advantages of the full wave rectifier, they are virtually always employed in preference to the half wave rectifier circuits. The increased efficiency along with the better ability of smoothing of the full wave rectifier arises from the fact that there is shorter time period between the peaks of output voltage when compared with that of the output voltage of the half wave rectifier. Thus the advantages of a full wave rectifier outweighs its disadvantages by a long way. Only occasionally, for low power supply requirements a half wave rectifier is preferred and used over the full wave rectifier.

4.6 APPLICATIONS OF RECTIFIER

Rectification is an essential and demanding aspect when it comes to telecommunication equipment and a number of many other electronic equipment. Precision rectifiers are used for signal processing, conditioning, instrumentation, measurement and control of the low level signals. There are various applications of rectifiers as mentioned below: -

- The rectifiers are primarily used to drive the DC power from an AC source that is they work as AC to DC converter or Root Mean Square (RMS) to DC converter.
- The diode only rectifiers are usually employed in such applications where there is less importance of the precision which is in the range of cut in voltage, such as in radio frequency demodulation and in DC voltage supply.
- They are widely used in AC volt meters and ammeters, watt meters.
- They are also used in linear function generators.
- They are used in various nonlinear analogue signal processing circuits like in detection circuits for example in sample and hold circuits, signal polarity detectors, Radio Frequency (RF) demodulators or Amplitude Modulated (AM) signal detectors, peak value detectors.
- They also find applications in the averaging circuits, function fitting, error measurements, clipper circuits, triangular wave frequency doubling, absolute value computation, and in floor detectors used in ultrasonic.
- Rectifiers can be used to supply polarized voltage for welding. Here control on the output current is needed. Sometimes this control is achieved by using thyristors in place of some of the diodes used in the rectifier. The thyristor has a gate terminal which can be used to control it and this feature is used to design the rectifier with control on its output current.

4.7 LITERATURE SURVEY OF VOLTAGE MODE FULL WAVE RECTIFIERS

In [1], a novel precision full wave rectifier is proposed. It employs one active element i.e. the EXCCII along with one NMOS transistor working as a switch, and one passive resistor. The simulation results are shown with maximum simulated frequency of 5 MHz. The circuit is simple and doesn't involve use of any diode. The output impedance is proper but input impedance is not.

In [2], a single circuit as precision half and full wave rectifier is presented. The single active block used is EXCCII, with two NMOS transistors working as a switch, and three passive grounded resistors. The advantage is that it can simultaneously provide the half and full wave rectified outputs. Other than this, it has proper input impedance and doesn't use any diode. The simulated results shows a maximum frequency of 500 KHz.

In [3], a precision full wave rectifier is presented which employs one Multiple Output Current Controlled Current Conveyor (MO-CCCII), a Zero Crossing Detector (ZCD), and one active MOS resistor. The circuit has the advantage of having proper input impedance, and use of active resistor along with the ability to rectify high frequency signals and having wide bandwidth. The simulated results shows a maximum frequency of 100 MHz.

In [4], a programmable precision full wave rectifier is reported. It uses three Operational Trans Resistance Amplifiers (OTRAs), six MOS transistors, along with eight passive resistors. The maximum simulated frequency shown in 1 KHz.

In [5], the full wave rectifier consists of a CCII-, two diodes and two resistors out of which one is grounded and one is floating. The maximum simulated frequency shown in 10 KHz. This circuit has a limitation of not having proper input and output impedances.

In [6], the reported rectifier uses two Current Feedback Operational Amplifiers (CFOAs) and three MOS transistors. The Circuit has the advantage of having proper input and output impedances and thus it facilitates its easy cascading with other voltage mode circuits. It also has advantage of not using any passive component. The maximum simulated frequency shown in 1 MHz.

In [7], the rectifier consists of two DVCC+s, two grounded resistors, and two diodes. The circuit possess advantage of having proper impedances at the input and output terminals. 1 MHz is the maximum frequency shown in simulation results. The circuit has a limitation of requirement of matching resistors. But both the grounded resistors favors the integrated circuit fabrication and facilitates cancellation of the parasitic effects.

In [8], a fully integrated full wave rectifier is reported. It employs a Floating Current Source (FCS) and four MOS transistors out of which two MOS transistors are used to form an active resistor. The circuit has the advantage of having proper input impedance and it uses no passive components, thus is fully suitable for fabrication. The circuit shows the highest frequency of 1 GHz when compared with the other reported rectifiers. However the output impedance is not proper for this rectifier.

In [9], two rectifiers are presented. Each one uses one DXCCII, one CCII, two diodes and two resistors. In the first rectifier, both resistors are grounded and it has proper input impedance. But the second one has one grounded resistor and it doesn't have proper input and output impedances. The maximum simulated frequency shown for both the rectifiers is 10 MHz.

In [10], rectifier consists of one CCII, and five current mirrors and five active resistors each one made up of two MOS transistors. The advantage provided are the proper impedances and use of no diodes. The maximum frequency shown is 100 MHz.

In [11], two rectifiers are reported. Each one uses one DVCC, two resistors. The first one uses two additional MOS transistors used for switching purpose and it provides single ended output voltage. The second one uses four extra MOS transistors and it provides differential full wave output voltage. Both rectifiers provide gain control facility. The maximum simulated frequency shown is 1 MHz and both the rectifiers have proper input impedances and use no diodes as an advantage.

In [12], the reported rectifier consists of two CCII+s, one grounded resistor and two floating resistors, along with two diodes. The circuit has proper impedances at the input and output. The

maximum simulated frequency shown is 10 MHz. This rectifier is better to drive loads because of its high voltage and low impedance at the output.

In [13], rectifier consists of two CCII+s, one buffer and one MOS transistor along with four resistors. The advantage is no diode used and proper impedance at the input. It possess simple circuitry and wide range of frequencies.

In [14], each of the two reported rectifiers use two DXCCII and two MOS transistors. The first one uses an extra grounded resistor. Both provide the advantage of high input impedance. The second rectifier uses no passive component and thus is more suitable for fabrication.

In [15], the first rectifier uses two CCIIs, one buffer, one MOS transistor and four resistors. The second rectifier uses two DVCCs, one buffer, one MOS transistor and three resistors. The hardware implementation can be achieved using IC AD844. The simulated maximum frequency shown is 1 MHz for both.

In [16], the rectifier uses only two DDCCs as the active block. It has proper impedances at the input and output thus doesn't need any buffer circuit. It has the advantage of using no diodes in its construction.

In [17], two CCIIs are used along with two diodes and three grounded resistors. The circuit has proper input impedance and performs better than the conventional Op-Amp based precision rectifiers. The maximum simulated frequency shown is 1 MHz.

In [18], the rectifier consists of one CCII and one Universal Voltage Conveyor (UVC), two diodes and two grounded resistors. The circuit overcomes the limitations of the conventional Op-Amp based precision rectifiers and is able to perform well for frequency of 500 KHz. The advantage given is the proper input and output impedances.

In [19], a Dual Output Operational Trans conductance Amplifier (DO-OTA) is used along with one grounded MOS resistor and four diodes. The advantage is the proper input impedance and the ability to perform better at high frequencies of up to 100 MHz.

In [20], only two DDCCs are used as the active block. The advantage of this rectifier is no use of passive elements and proper input impedance.

In [21], three Transconductance Elements (TEs) are used along with two MOS transistors and one grounded resistor. The high input impedance is the advantage of this circuit other than no use of diodes. The zero crossing distortion is low. It can rectify high frequencies up to 200 MHz.

In [22], one OTA is used along with one grounded resistor and two MOS transistors. The advantage includes no use of diode, high input impedance, large input range and high frequency rectification up to 200 MHz.

In [23], one OTA is used along with two grounded resistor and two MOS transistors. The advantage includes no use of diode, high input impedance, and high frequency rectification up to 200 MHz.

In [24], circuit uses a Current Conveyor based on Current Steering Output Stage (CCIICS), three resistors and four diodes. It provides advantage of high input impedance, low sensitivity to temperature and the level of DC offset at the output is low. The circuit is implemented using BJTs and 100 KHz is the maximum frequency shown in the simulation results.

In [25], one DXCCII and three MOS transistors are used. It gives advantage of high input impedance and use of no passive components which facilitates its easy integration.

In [26], one CCII+, two Op-Amps, three resistors and two diodes are used. The big advantage is the high input impedance and low output impedance which supports its easy cascading.

In [27], two CCII+, and three MOS transistors are employed. The circuit is simple and less number of transistors are requires and it gives the advantage of using no passive component. However, none of its terminals are at proper impedance level.

In [28], five OTAs are used along with two grounded resistors. The advantage is high input impedance and no use of diodes. In order to avoid the use of diode the characteristic of differential amplifier of the OTA has been used. The circuit provides significant improvement regarding problems of the limited input voltage swing and the dependence of the transconductance gain of the OTA on temperature.

In [29], two topologies are proposed. The first one uses four Current Controlled Current Conveyors (CCCIIs), three grounded resistors and two floating resistors. The second topology uses three CCCIIs, two grounded resistors and three floating resistors. Both provide the advantage of proper input impedance and use of no diodes.

In [30], one CCII+, four current mirrors, two transistors and two grounded resistors are used. The circuit offers high input impedance and requires no diodes.

In [31], one CC, two Op-Amps, three floating resistors and two diodes are used. The circuit is developed with slight modification in the standard Op-Amp based precision full wave rectifier. To overcome the diode resistance, the high output impedance of the CC is used. The circuit now provides a significant improvement in the performance in comparison with the conventional standard Op-Amp based precision rectifier and is capable to generate undistorted output up to 100 KHz frequency input signal.

The summary of the above reported precision full wave rectifier circuits is shown in table 2.

Table 2: Comparison of various voltage mode precision full wave rectifiers

Reference no.	Active elements	No. of floating / grounded resistors	No. of diodes	No. of transistors (MOS)	Input impedance	Output impedance	Max. frequency shown (Hz)	Supply voltage	Year
[1]	1 EXCCII 1 MOS	1/0	0	23+1	Low	Low	5M	±1.25	2018
[2]	1 EXCCII 2 MOS	0/3	0	21+2	High	High	500K	±1.25	2017
[3]	1 DDCCCII 1 ZCD 1 MOS-R	1(MOS)/0	0	(18+9)BJT +2	High	High	10M	±1.2	2017
[4]	3 OTRA 6 MOS	8/0	0	3×14+6	Low	High	1K	±2	2017
[5]	1 CCII–	1/1	2	16	Low	High	10K	±1.65	2017
[6]	2 CFOA 3 MOS	0/0	0	2×18+3	High	Low	1M	±1.25	2017
[7]	2 DVCC+	0/2	2	2×12	High	Low	1M	±1.25	2016
[8]	1 FCS 1 MOS-R 2 MOS	0/1(MOS)	0	4+2+2	High	High	1G	±2.4	2015
[9] Fig 2(a)	1 DXCCII 1 CCII	0/2	2	20+9	High	High	10M	±2.5	2014
Fig 2(b)	1 DXCCII 1 CCII	1/1	2	20+9	Low	High	10M	±2.5	
[10]	1 CCII 6 CM 5 MOS-R	0/5	0	9+6×2+ 5×2+6	High	Low	100M	±1.2	2014
[11] Fig 2(b)	1 DVCC 2 MOS	0/2	0	20+2	High	High	1M	±1.5	2013
Fig 2(c)	1 DVCC 4 MOS	1/1	0	20+4	High	High	1M	±1.5	
[12]	2 CCII+	2/1	2	2×18	High	Low	10M	±12	2013
[13]	2 CCII+ 1 Buffer 1 MOS	3/1	0	2×9+8+1	High	High	1M	±2.5	2012
[14] Fig 3	2 DXCCII 2 MOS	0/1	0	2×24+2	High	High	1.25M	±1.25	2012
Fig 5	2 DXCCII 2 MOS	0/0	0	2×24+2	High	High	1M	±1.25	

[15] Fig 4	2 CCII+ 1 Buffer 1 MOS	3/1	0	2×9+8+1	Low	High	1M	±2.5	2012
Fig 6	2 DVCC 1 Buffer 1 MOS	3/0	0	2×20+8+1	Low	High	1M	±2.5	
[16]	2 DDCC	0/0	0	2×12	High	Low	1M	±2.5	2011
[17]	2 CCII	0/3	2	2×40	High	High	1M	NA	2011
[18]	1 CCII 1 UVC	0/2	2	20+40	High	Low	500K	NA	2010
[19]	1 DO-OTA 1 MOS-R 2 MOS	0/(1MOS)	4	20+2+2	High	High	100M	±5	2010
[20]	2 DDCC	0/0	0	2×12	High	Low	1M	±2.5	2009
[21]	3 TE 2 MOS	0/1	0	3×4+2	High	High	200M	±5	2009
[22]	1 OTA 2 MOS	0/1	0	24+2	High	High	200M	±5	2009
[23]	1 OTA 2 MOS	0/2	0	24+2	High	High	200M	±5	2009
[24]	2 CCIICS	1/2	4	2×17 BJTs	High	High	100K	NA	2008
[25]	1 DXCCII 3 MOS	0/0	0	20+3	High	High	1M	±1.25	2008
[26]	1 CCII+ 2 OPA	1/2	2	NA	High	Low	500K	±15	2007
[27]	2 CCII+ 3 MOS	0/0	0	2×10+3	Low	High	250K	±1.25	2006
[28]	5 OTA	0/2	0	NA	High	High	10K	±15	2005
[29] Fig 2	4 CCCII	2/3	0	4×15	High	High	100K	±15	2004
Fig 3	3 CCCII	3/2	0	3×15	High	High	100K	±15	
[30]	1 CCII+ 4 CM 2 BJTs	0/2	0	18+4×4+2 BJTs	High	High	100K	±10	2001
[31]	1 CC 2 OPA	3/0	2	NA	Low	High	100K	NA	2000
Proposed	1 DXCCII 2 MOS	0/1	0	20+2	High	High	500K	±1.8	-

4.8 PROPOSED PRECISION HALF WAVE RECTIFIER (POSITIVE HALF CYCLE)

The proposed precision half wave rectifier which rectifies only the positive half cycle of the input AC voltage signal V_{in} is shown in figure 19 below.

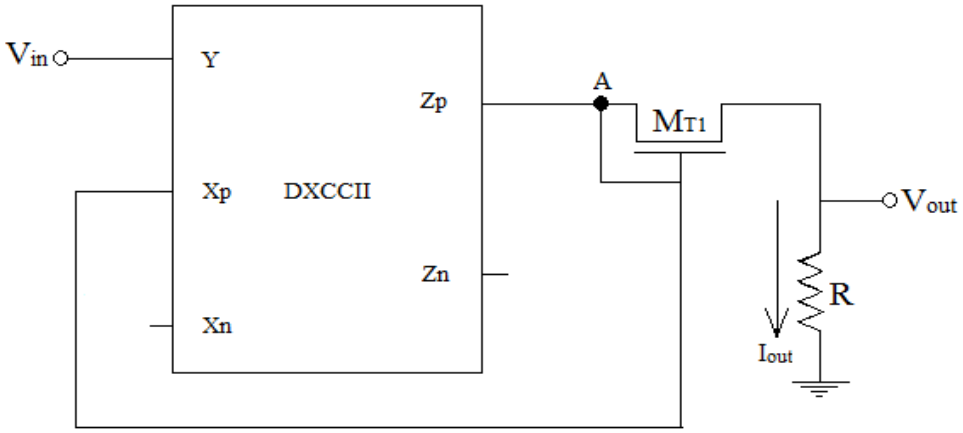

Figure 19: Proposed precision half wave rectifier for positive half cycle

An NMOS transistor M_{T1} and a resistor R are connected with the active block DXCCII in a particular configuration as shown above in figure 18. The shorted gate and drain terminals of M_{T1} are connected with the shorted Xp and Zp terminals of DXCCII and the source terminal of M_{T1} is connected to one terminal of the resistor R and the other terminal of this resistor R is connected to the ground. The output voltage V_{out} is obtained across the resistor R.

4.8.1 OPERATION OF THE PROPOSED PRECISION HALF WAVE RECTIFIER FOR POSITIVE HALF CYCLE

The input AC supply voltage V_{in} is applied at the high impedance Y terminal of the DXCCII. This voltage is copied at the Xp terminal of DXCCII,

i.e. $$V_{Zp} = V_{Xp} = V_{in} \quad (37)$$

Therefore when input voltage V_{in} is positive, voltage V_{Xp} is also positive.

Input voltage V_{in} is a sinusoidal AC voltage and is given by the following equation

$$V_{in} = A_c \mathrm{Sin}(2\pi f_c t) \tag{38}$$

where

A_c is the amplitude of the input voltage V_{in},

t is the time period and f_c is the frequency in hertz (Hz) or cycles/second.

M_{T1} is a diode connected NMOS transistor, that means its gate and drain terminals are shorted together. Now this MOSFET always works in saturation region as it always holds the condition of working in saturation which is written below,

i.e. $$V_{DSn} \geq (V_{GSn} - V_{THn}) \tag{39}$$

where

V_{DSn} is the drain to source voltage of M_{T1}.
V_{GSn} is the gate to source voltage of M_{T1}.
and V_{THn} is the threshold voltage of M_{T1}. V_{THn} for NMOS is positive.

For an NMOS transistor

if	$V_{GSn} \geq V_{THn}$;	NMOS transistor turns on	
and if	$V_{GSn} < V_{THn}$;	NMOS transistor turns off	(40)

The MOSFET whose gate and drain terminals are connected together is called as the diode connected transistor because it behaves like a semiconductor p-n junction diode. The shorted drain and gate terminals work as the p terminal of the diode and the source terminal works as the n terminal of the diode. This MOSFET always works in either saturation region i.e. as a closed switch or in the cut off region i.e. as an open switch. If the voltage at the shorted gate and drain

terminals of this MOSFET is positive than it turns on and works in the saturation region, that is works as a closed switch or on switch, and if the voltage at the shorted gate and drain terminals of this MOSFET is negative than it turns off and works in the cut off region, that is works as an open switch or off switch.

Now when the input voltage V_{in} is positive than voltage V_{Xp} is also positive. Voltage V_{Xp} appears at the shorted drain and gate terminals of the $M_{T1.}$ M_{T1} turns on whenever voltage V_{Xp} is positive. Therefore for every positive cycle of the input voltage V_{in}, M_{T1} turns on, and for every negative cycle of the input voltage V_{in}, M_{T1} turns off. When M_{T1} is on, equal amount of currents flow from the Xp and Zp terminals of the DXCCII towards node A, as no current goes in to the gate terminal of M_{T1}, these currents therefore add up at node A and the resultant current then passes through the M_{T1} which then passes through the resistor R and then goes to the ground. The currents developed at Xp and Zp terminals linearly depend on the positive half cycle of the voltage at Xp terminal of the DXCCII that is at voltage V_{Xp}. Thus the currents developed because of the voltage V_{Xp} are DC in nature. Therefore for every positive cycle of the input voltage $V_{in,}$ M_{T1} turns on, and there flows a current through resistor R and a voltage is developed across it which is considered as the output voltage $V_{out.}$ And for every negative cycle of the input voltage V_{in} , the M_{T1} turns off and there flows no current through resistor R and therefore voltage developed across it is zero, thus output voltage V_{out} is zero. This way, there is an output voltage V_{out} available only for the positive half cycles of the input voltage V_{in}. Thus the half wave rectified output voltage V_{out} for the positive half cycle of the input voltage V_{in} is obtained across the resistor R.

The overall operation of the proposed precision half wave rectifier for the positive half cycle can be summarized by the following equations below

$V_{out} = I_{out} \times R \cong V_{in}$; for $V_{in} \geq 0$ i.e. for the positive half cycle (NMOS M_{T1} is on)

$V_{out} = 0$; for $V_{in} \leq 0$ i.e. for the negative half cycle (NMOS M_{T1} is off)

where, I_{out} is the output current or the current across the resistor R.

4.8.2 SIMULATION RESULTS OF THE PROPOSED PRECISION HALF WAVE RECTIFIER FOR POSITIVE HALF CYCLE

The proposed precision half wave rectifier for the positive half cycle is simulated with SPICE using 0.35µm CMOS technology parameters are used. The supply voltage for the active block DXCCII [35] is taken as $\pm 1.8V$ and the voltage V_{bias} is set to 1.05V. The aspect ratio (W/L) of the M_{T1} used as a switch is $(40\mu m/0.7\mu m)$. The input voltage V_{in} used in the simulation is having peak amplitude A_c of 100mV and frequency f_c of 500 kHz.

The waveforms of the input voltage V_{in} and the output voltage V_{out} are shown below in the figure 20 and figure 21 respectively.

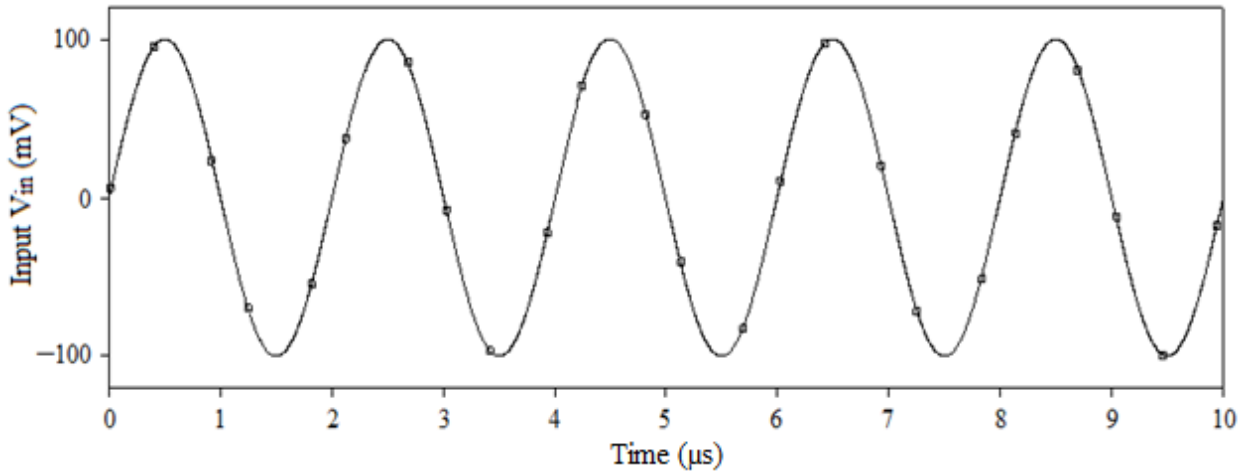

Figure 20: Waveform of the input voltage V_{in}

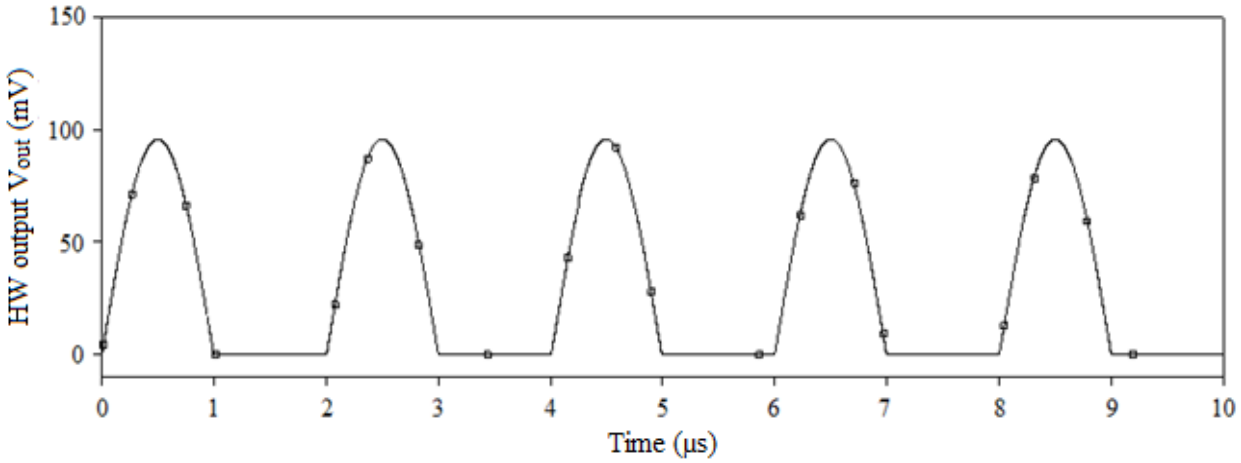

Figure 21: Half wave rectified output V_{out} for the positive cycle of the input voltage V_{in}

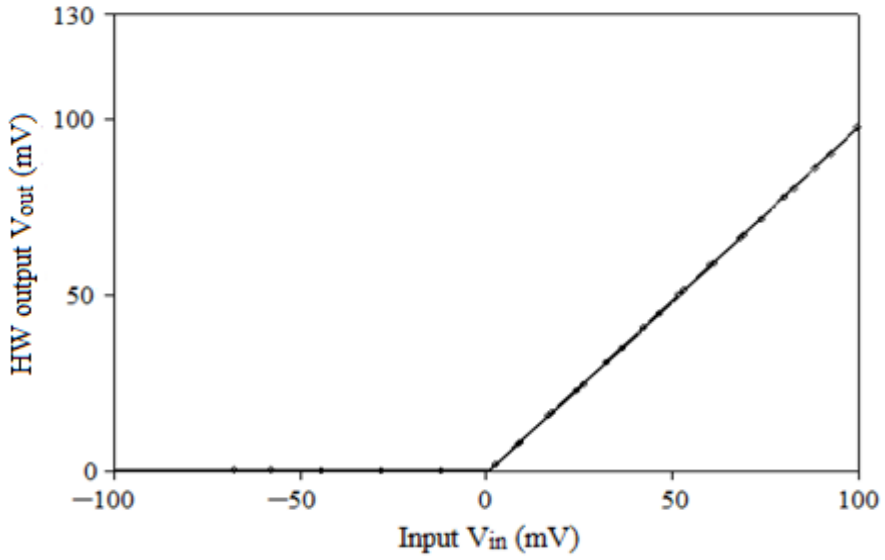

Figure 22: DC transfer characteristics of the proposed precision half wave rectifier for the positive cycle

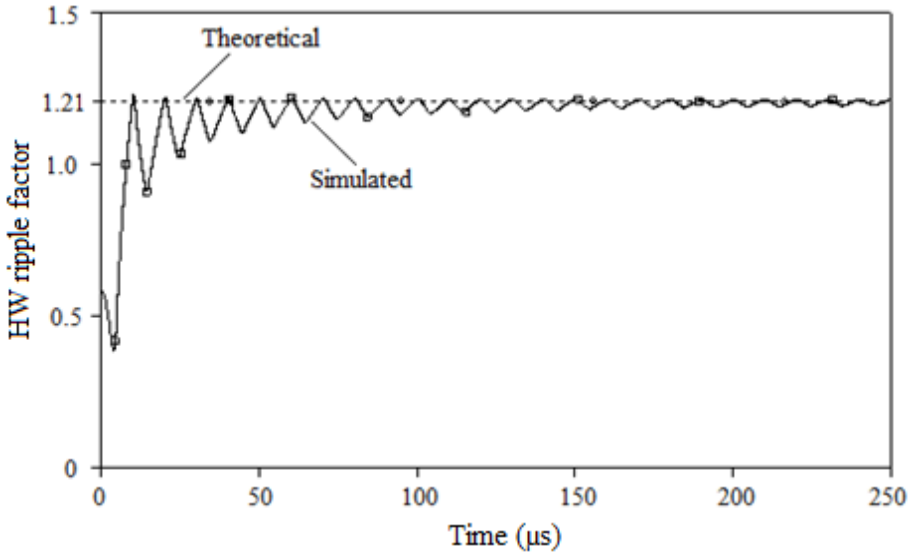

Figure 23: Waveform for the ripple factor of the proposed precision half wave rectifier for positive cycle

The simulated DC transfer characteristics of the proposed precision half wave rectifier for the positive cycle is shown in figure 22 and the waveform for the simulated and the theoretical ripple factor is shown in figure 23 above. It can be seen that the simulated ripple factor is approximately 1.20 which is much close to the theoretical ripple factor of 1.21.

4.9 PROPOSED PRECISION HALF WAVE RECTIFIER (NEGATIVE HALF CYCLE)

The proposed precision half wave rectifier which rectifies only the negative half cycle of the input AC voltage signal V_{in} is shown in figure 24 below.

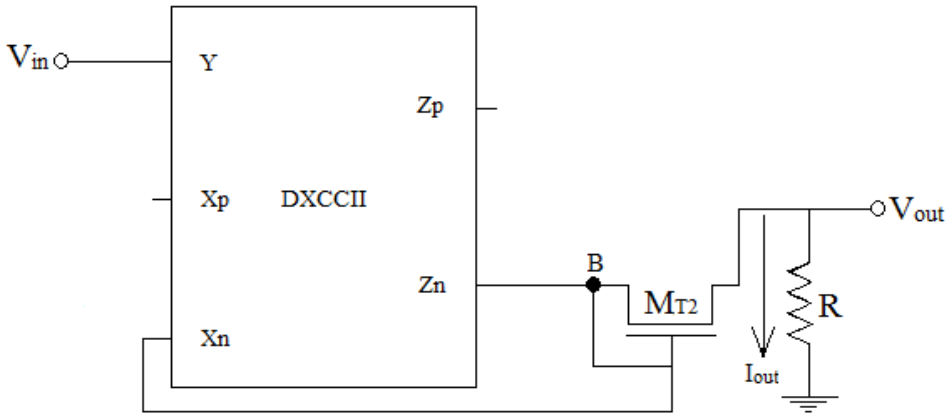

Figure 24: Proposed precision half wave rectifier for negative half cycle

An NMOS transistor M_{T2} and a resistor R are connected with the active block DXCCII in a particular configuration as shown above in figure 24. The shorted gate and drain terminals of M_{T2} are connected to the shorted Xn and Zn terminals of DXCCII and the source terminal of M_{T2} is connected to one terminal of the resistor R and the other terminal of this resistor R is connected to the ground. The output voltage V_{out} is obtained across the resistor R.

4.9.1 OPERATION OF THE PROPOSED PRECISION HALF WAVE RECTIFIER FOR NEGATIVE HALF CYCLE

The input AC supply voltage V_{in} is applied at the high impedance Y terminal of the DXCCII. This voltage is copied at the Xn terminal of DXCCII but with a phase shift of 180° or it can be said that the inverted input voltage V_{in} is available at the Xn terminal.

i.e. $$V_{Zn} = V_{Xn} = -V_{in} \quad (41)$$

Therefore when input voltage V_{in} is negative, voltage V_{Xn} is positive.

M_{T2} is again a diode connected NMOS transistor, that means its gate and drain terminals are shorted together. Now this MOSFET too always works in either saturation region or in the cut off region.

Now when the input voltage V_{in} is negative then voltage V_{Xn} is positive. Voltage V_{Xn} appears at the shorted drain and gate terminals of the $M_{T2.}$ M_{T2} turns on whenever voltage V_{Xn} is positive. Therefore for every negative cycle of the input voltage V_{in}, M_{T2} turns on, and for every positive cycle of the input voltage V_{in}, M_{T2} turns off. When M_{T2} is on, equal amount of currents flow from the Xn and Zn terminals of the DXCCII towards node B, as no current goes in to the gate terminal of M_{T2}, these currents therefore add up at node B and the resultant current then passes through the M_{T2}, which then passes through the resistor R and then goes to the ground. The currents developed at Xn and Zn terminals linearly depend on the positive half cycle of the voltage at Xn terminal of the DXCCII that is at voltage V_{Xn}. Thus the currents developed because of the voltage V_{Xn} are DC in nature. Therefore for every negative cycle of the input voltage $V_{in,}$ M_{T2} turns on, and there flows a current through resistor R and a voltage is developed across it which is considered as the output voltage V_{out}. And for every positive cycle of the input voltage V_{in} , the M_{T2} turns off and there flows no current through the resistor R and therefore voltage developed across it is zero thus the output voltage V_{out} is zero. This way there is an output voltage V_{out} available only for the negative half cycles of the input voltage V_{in} and thus the half wave rectified voltage V_{out} is obtained across the resistor R.

The overall operation of the proposed precision half wave rectifier for the negative half cycle can be summarized by the following equations below

$V_{out} = 0;$ for $V_{in} \geq 0$ i.e for the positive half cycle (NMOS M_{T2} is off)

$V_{out} = I_{out} \times R \cong -V_{in};$ for $V_{in} \leq 0$ i.e for the negative half cycle (NMOS M_{T2} is on)

where, I_{out} is the output current or the current across the resistor R.

4.9.2 SIMULATION RESULTS OF THE PROPOSED PRECISION HALF WAVE RECTIFIER FOR NEGATIVE HALF CYCLE

The proposed precision half wave rectifier for the negative half cycle is simulated with SPICE using 0.35µm CMOS technology parameters are used. The supply voltage for the active block DXCCII [35] is taken as $\pm 1.8V$ and the voltage V_{bias} is set to 1.05V. The aspect ratio (W/L) of the M_{T2} used as a switch is $(40\mu m/0.7\mu m)$. The input voltage V_{in} used in the simulation is having peak amplitude A_c of 100mV and frequency f_c of 500 kHz.

The waveforms of the input voltage V_{in} and the output voltage V_{out} are shown below in the figure 25 and figure 26 respectively.

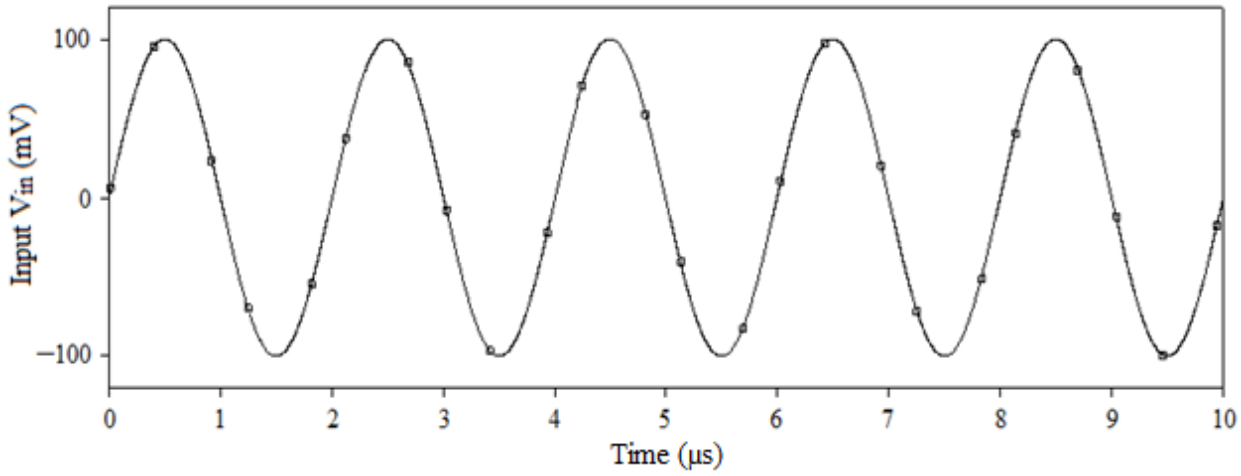

Figure 25: Waveform of the input voltage V_{in}

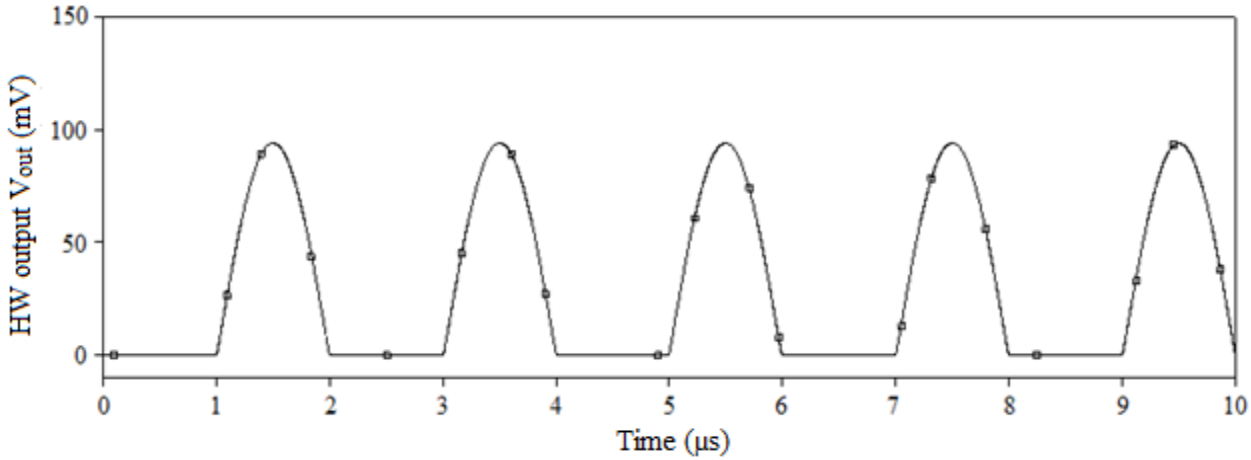

Figure 26: Half wave rectified output V_{out} for the negative cycle of the input voltage V_{in}

The simulated DC transfer characteristics of the proposed precision half wave rectifier for negative cycle is shown in figure 27 and the waveform for the simulated and the theoretical ripple factor is shown in figure 28 below. It can be seen that the simulated ripple factor is approximately 1.23 which is much close to the theoretical ripple factor of 1.21.

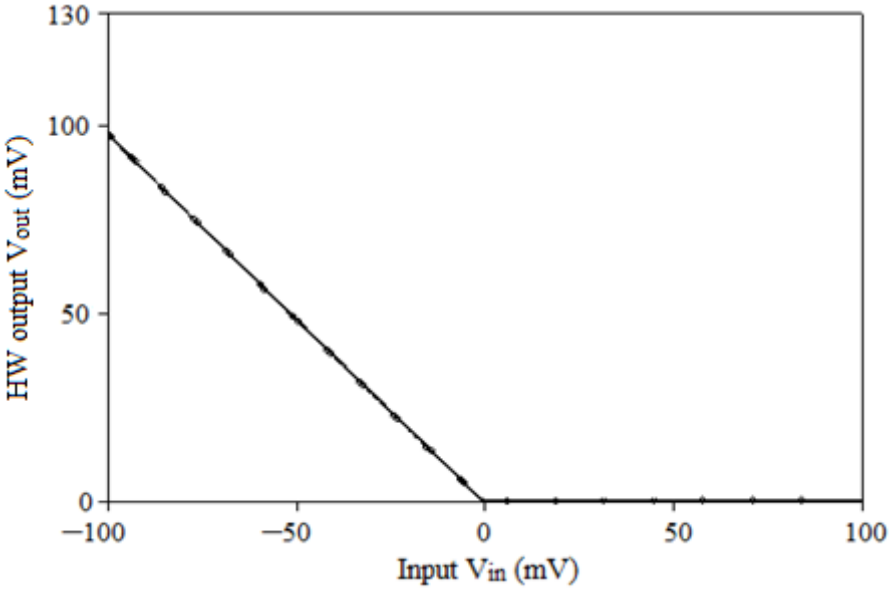

Figure 27: DC transfer characteristics of the proposed precision half wave rectifier for the negative cycle

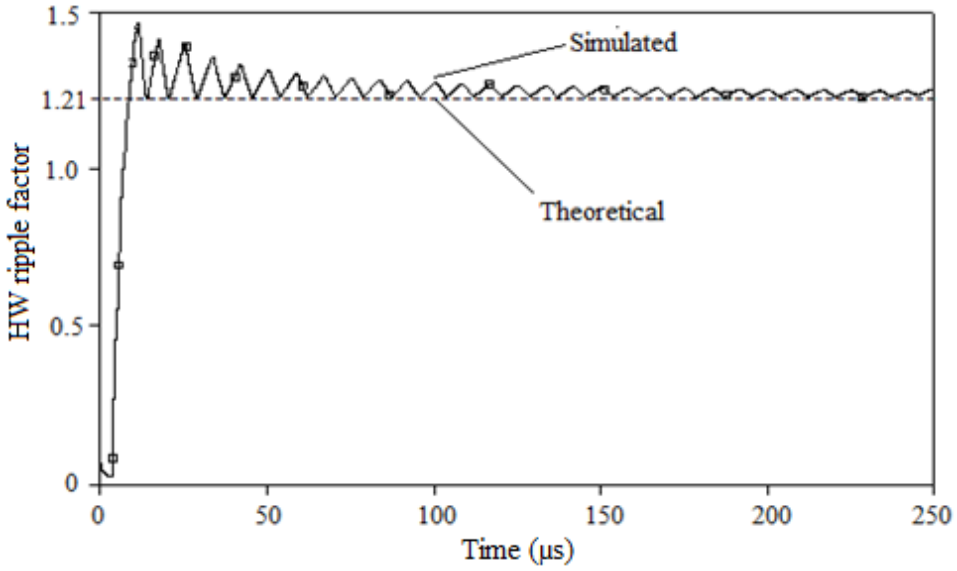

Figure 28: Waveform for the ripple factor of the proposed precision half wave rectifier for negative cycle

4.10 PROPOSED PRECISION FULL WAVE RECTIFIER

The proposed precision full wave rectifier is shown below in figure 29.

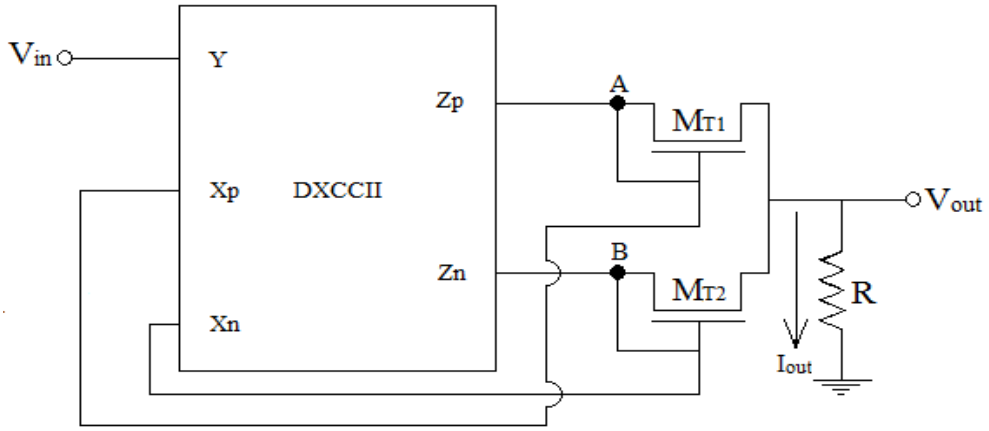

Figure 29: Proposed precision full wave rectifier

Two NMOS transistors M_{T1} and M_{T2} and a resistor R are connected with the active block DXCCII in a configuration as shown above in figure 25. The shorted gate and drain terminals of M_{T1} are connected to the shorted Xp and Zp terminals of the DXCCII whereas the shorted gate and drain terminals of M_{T2} are connected to the shorted Xn and Zn terminals of the DXCCII and the source terminals of M_{T1} and M_{T2} are shorted together and are then connected to one terminal of the resistor R and the other terminal of this resistor R is connected to the ground. The output voltage V_{out} is obtained across the resistor R.

4.10.1 OPERATION OF THE PROPOSED PRECISION FULL WAVE RECTIFIER

The input AC supply voltage V_{in} is applied at the high impedance Y terminal of the DXCCII. This input voltage V_{in} voltage is copied at the Xp terminal of DXCCII.

i.e. $$V_{Zp} = V_{Xp} = V_{in} \quad (42)$$

The input voltage V_{in} voltage is also copied at the Xn terminal of DXCCII with 180° phase shift or it can be said that the inverted input voltage is available at the Xn terminal.

i.e. $$V_{Zn} = V_{Xn} = -V_{in} \quad (43)$$

Therefore when input voltage V_{in} is positive, voltage V_{Xp} is positive and when input voltage V_{in} is negative, voltage V_{Xn} is positive.

M_{T1} and M_{T2} are again diode connected NMOS transistors, that is these are having their corresponding gate and drain terminals shorted together. These MOSFETs named as M_{T1} and M_{T2} therefore always work in either the saturation region or in the cut off region.

Now when the input voltage V_{in} is positive than voltage V_{Xp} is positive and when the input voltage V_{in} is negative than voltage V_{Xn} is positive. Voltage V_{Xp} appears at the shorted drain and gate terminals of the M_{T1} and the voltage V_{Xn} appears at the shorted drain and gate terminals of the $M_{T2.}$ M_{T1} turns on whenever voltage V_{Xp} is positive whereas the M_{T2} turns on whenever voltage V_{Xn} is positive. Therefore for the every positive cycle of the input voltage V_{in}, M_{T1} turns on, and for the every negative cycle of the input voltage V_{in}, M_{T2} turns on.

During the positive half cycle of the input voltage V_{in}, the M_{T1} turns on and the M_{T2} turns off, and equal amount of currents flow from the Xp and Zp terminals of the DXCCII towards the node A, as no current goes in to the gate terminal of $M_{T1,}$ these currents therefore add up at node A and then the resultant current passes through the $M_{T1,}$ which then passes through the the resistor R and then goes to the ground. The currents developed at Xp and Zp terminals linearly depend on the positive half cycle of the voltage at Xp terminal of the DXCCII that is at voltage V_{Xp} and are therefore DC in nature. And during the negative half cycle of the input voltage $V_{in,}$ the M_{T1} turns off and the M_{T2} turns on, and equal amount of currents flow from the Xn and Zn terminals of the DXCCII towards the node B, as no current goes in to the gate terminal of M_{T2}, these currents

therefore add up at node B and then the resultant current passes through the $M_{T2,}$ which then passes through the resistor R and then goes to the ground. The currents developed at Xn and Zn terminals linearly depend on the positive half cycle of the voltage at Xn terminal of the DXCCII that is at voltage V_{Xn} and therefore are DC in nature.

Therefore, for every positive cycle of the input voltage $V_{in,}$ only M_{T1} turns on, and there flows a current through the resistor R, and for every negative cycle of the input voltage $V_{in,}$ only the M_{T2} turns on and again there flows a current through the resistor R in the same direction. Thus the voltage developed across this resistor R is unipolar in nature i.e. DC in nature and this voltage is considered as the output voltage V_{out}. This way an output voltage V_{out} is obtained for both the half cycles of the input voltage V_{in} i.e. the positive half cycle as well as the negative half cycle. The full wave rectified voltage waveform V_{out} is therefore obtained at the resistor R.

The overall operation of the proposed precision full wave rectifier can be summarized by the following equations as mentioned below

$V_{out} = I_{out} \times R \cong V_{in};$ for $V_{in} \geq 0$ i.e for the positive half cycle (only NMOS M_{T1} is on)

$V_{out} = I_{out} \times R \cong -V_{in};$ for $V_{in} \leq 0$ i.e for the negative half cycle (only NMOS M_{T2} is on)

or in general

$$V_{out} = I_{out} \times R \cong |V_{in}| \quad (44)$$

where, I_{out} is the output current or the current across the resistor R.

4.10.2 SIMULATION RESULTS OF THE PROPOSED PRECISION FULL WAVE RECTIFIER

The proposed precision full wave rectifier is simulated with SPICE using 0.35µm CMOS technology parameters are used. The supply voltage for the active block DXCCII [35] is taken as $\pm 1.8V$ and the voltage V_{bias} is set to 1.05V. The aspect ratios (W/L) of the transistors M_{T1} and M_{T2} used as the switches are same i.e. $(40\mu m/0.7\mu m)$. The input voltage V_{in} used in the simulation is having peak amplitude A_c of 100mV and frequency f_c of 500 kHz.

The waveforms of the input voltage V_{in} and the output voltage V_{out} are shown below in the figure 30 and figure 31 respectively.

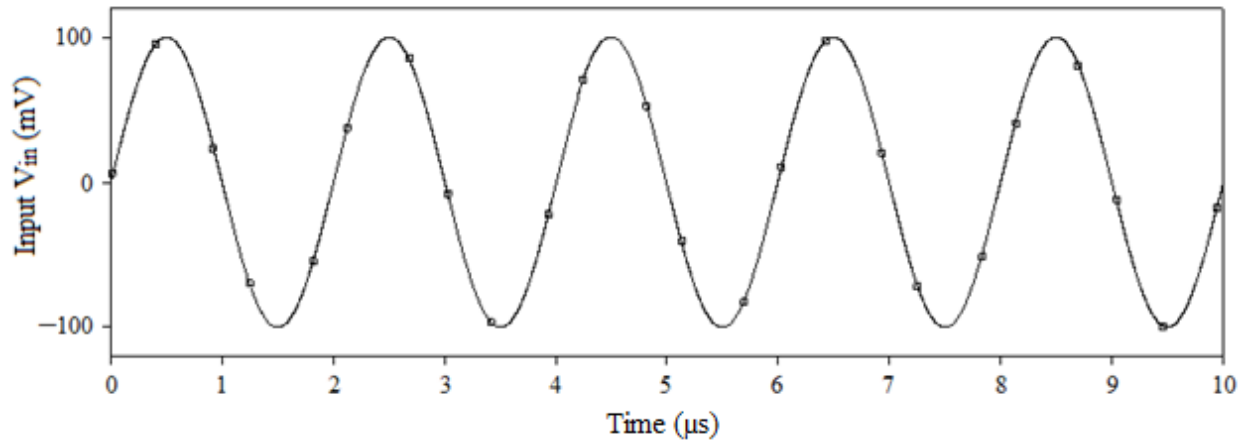

Figure 30: Waveform of the input voltage V_{in}

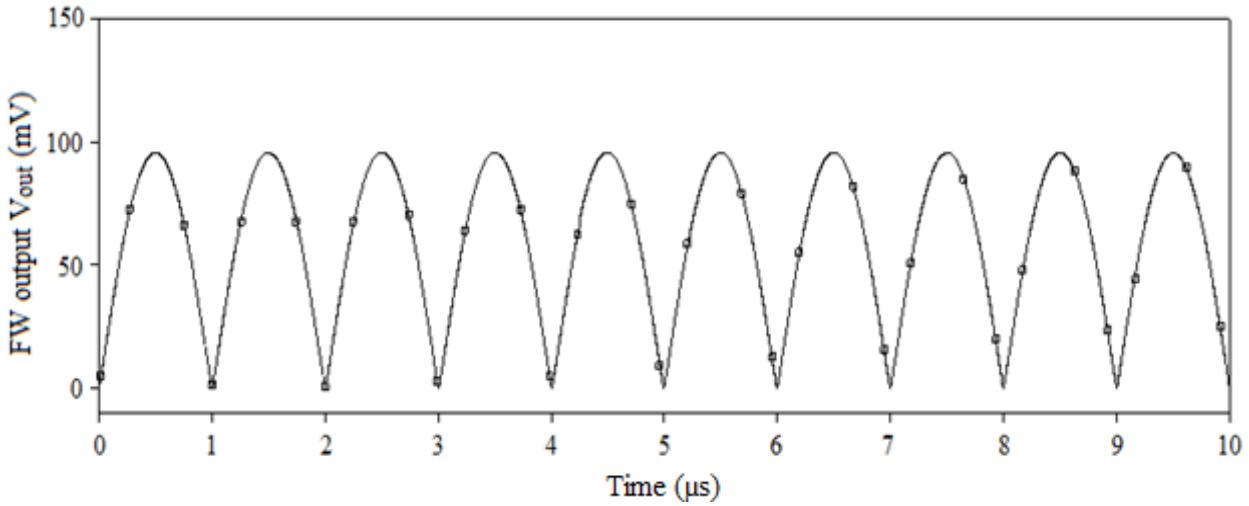

Figure 31: Full wave rectified output V_{out} for the input voltage V_{in}

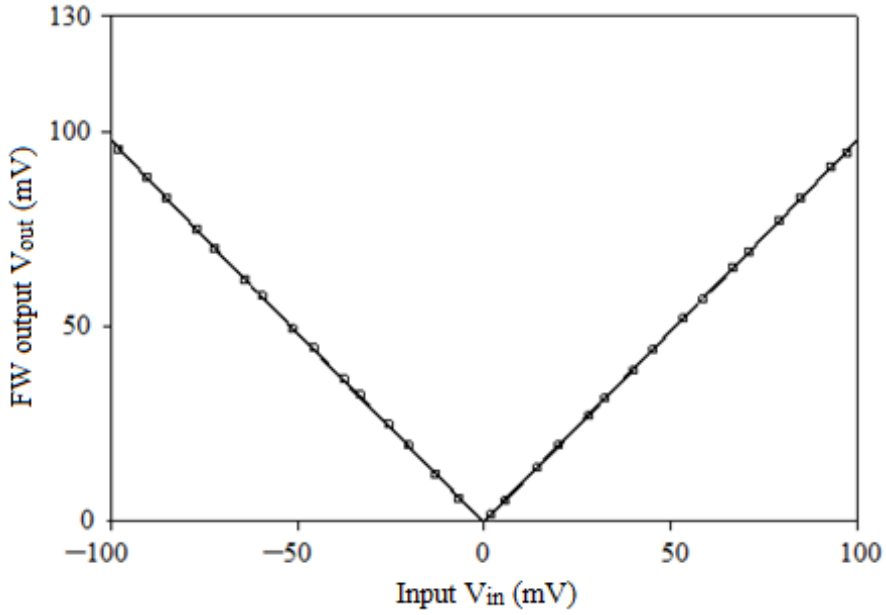

Figure 32: DC transfer characteristics of the proposed precision full wave rectifier

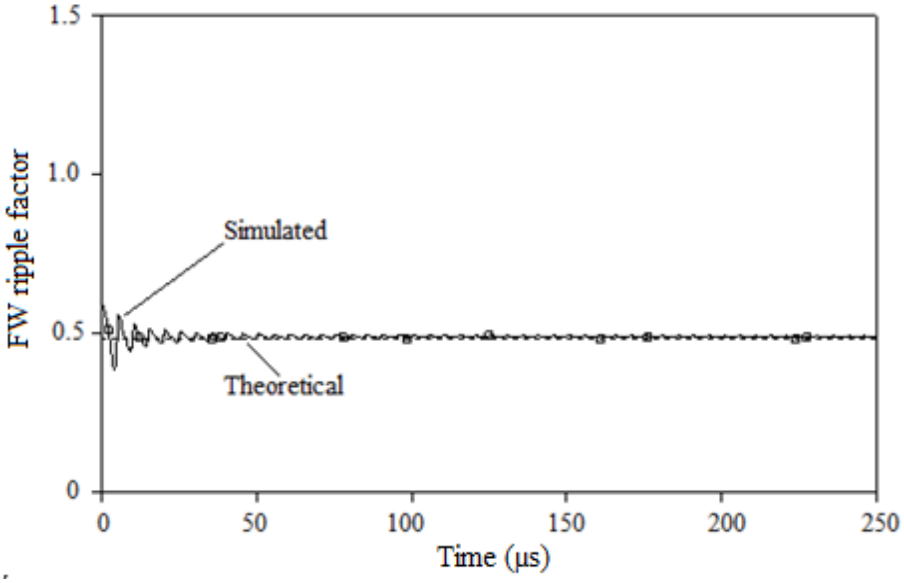

Figure 33: Waveform for the ripple factor of the proposed precision full wave rectifier

The simulated DC transfer characteristics of the proposed precision full wave rectifier is shown in figure 32 and the waveform for the simulated and the theoretical ripple factor is shown in figure 33 above. It can be observed that the simulated ripple factor is approximately 0.49 which is much closer to the theoretical ripple factor of 0.483

In conclusion the output voltage V_{out} of the above proposed precision half wave rectifier for the positive cycle, precision half wave rectifiers for the negative cycle and the precision full wave rectifier can mathematically be written in the tabulated form as shown below in the table 4.

Table 3: Summary of outputs of the proposed precision half and full wave rectifiers

Input signal (V_{in}) $V_{in} = A_c Sin(2\pi f_c t)$	**HW output (V_{out}) Half wave rectifier (positive cycle)**	**HW output (V_{out}) Half wave rectifier (negative cycle)**	**FW output (V_{out}) Full wave rectifier**
Positive cycle ($V_{in} \geq 0$)	$A_c Sin(2\pi f_c t)$	0	$A_c Sin(2\pi f_c t)$
Negative cycle ($V_{in} \leq 0$)	0	$-A_c Sin(2\pi f_c t)$	$-A_c Sin(2\pi f_c t)$

CHAPTER 5

DIGITAL MODULATORS

5.1 DIGITAL MODULATION

Modulation is a process where one of the parameters of the carrier signal, which can be amplitude, phase or frequency, is varied linearly according to the variations in the message signal or modulating signal. With the modulation, the information contained in the message signal is transferred to the carrier signal. When modulation is done for the digital signals then it is known as the digital modulation. The device that performs this modulation is known as the digital modulator. Digital modulation is carried out when there is a need to transmit the information through free space. The digital signal is a basically a binary signal in the form of 0s and 1s and it is a low pass signal and can't be transmitted through the wireless medium, so in order to transmit the digital signal through wireless medium, modulation is required.

5.2 TYPES OF DIGITAL MODULATION

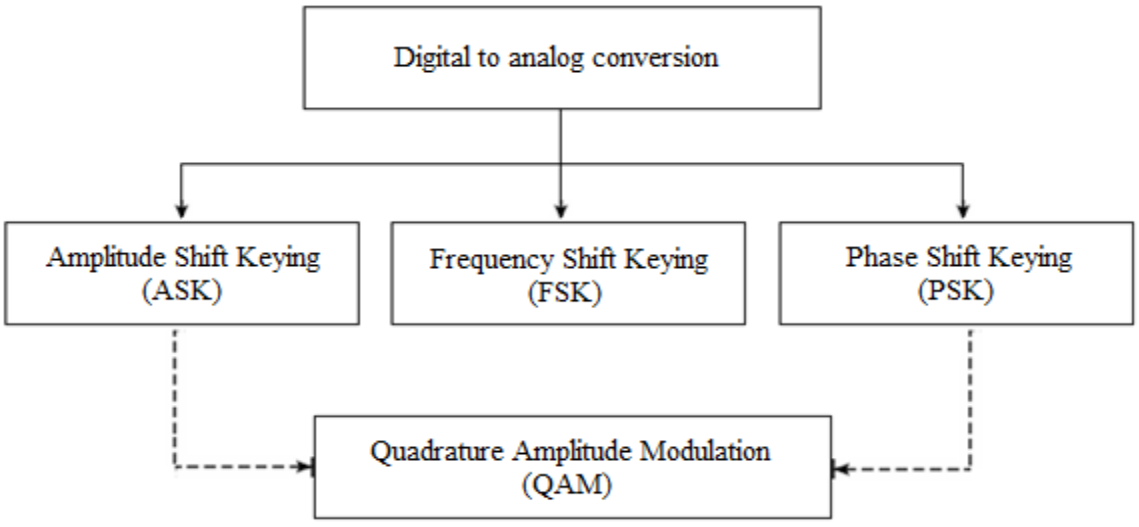

Figure 34: Types of digital modulation

Depending upon the parameter of the carrier signal which is used for modulation, the digital modulation is basically of three types, i.e.

1. Amplitude Shift Keying (ASK)
2. Phase Shift Keying (PSK)
3. Frequency Shift Keying (FSK)

When in a modulation some properties of ASK and PSK are used together then the modulation is called as Quadrature Amplitude Modulation (QAM).

5.2.1 AMPLITUDE SHIFT KEYING (ASK)

In this, the amplitude of the radio frequency carrier signal is varied in accordance with the amplitude of the modulating digital signal. The binary 1 is represented by the presence of carrier signal while binary 0 is represented by the absence of carrier signal. When the digital signal is two level only then modulation is called as the Binary Amplitude Shift Keying (BASK). A basic block diagram is shown in figure 35.

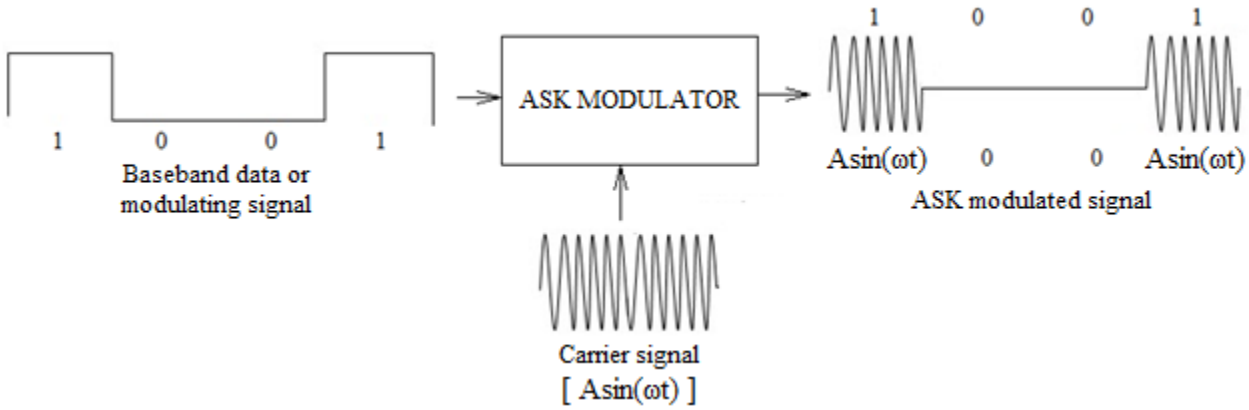

Figure 35: Block diagram of BASK modulator

BASK modulation can be expressed by the following equations

$s(t) = A\sin(2\pi ft);$ for Binary Logic-1 (45)

$s(t) = 0;$ for Binary Logic-0 (46)

Where, $s(t)$ is the BASK modulated output, A is the amplitude of the carrier signal and f is the frequency of the carrier signal.

5.2.1.1 ADVANTAGES OF ASK

- High bandwidth efficiency.
- Simple receiver design.
- Processes of modulation and demodulation are comparatively inexpensive.

5.2.1.2 DISADVANTAGES OF ASK

- High probability of error (P_e)
- Signal to Noise Ratio (SNR) is less
- Lowest immunity against noise
- Lower power efficiency

5.2.1.3 APPLICATIONS OF ASK

- Infrared (IR) remote controls
- Transmitter and receiver in optical fiber communication

5.2.2 PHASE SHIFT KEYING (PSK)

In this, the phase of the radio frequency carrier signal is varied in accordance with the amplitude of the modulating digital signal. The binary 1 is represented by the presence of in phase carrier signal while binary 0 is represented by the presence of 180° out of phase carrier signal. When the digital signal is two level only then modulation is called as the Binary Phase Shift Keying (BPSK).

The functional block diagram of BPSK modulation process is shown in figure 36.

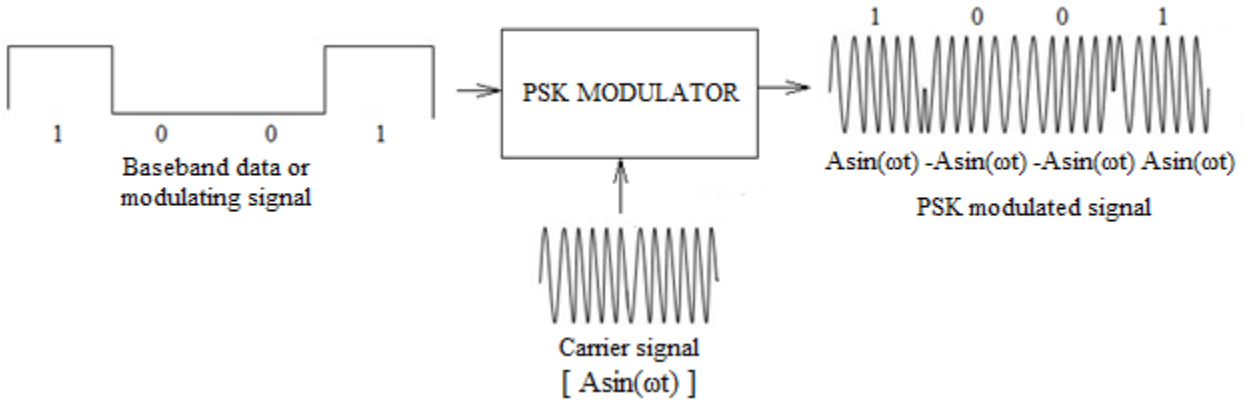

Figure 36: Block diagram of BPSK modulator

BPSK modulation can be expressed by the following equations

$s(t) = A\sin(2\pi ft);$ for Binary Logic-1 (47)

$s(t) = -A\sin(2\pi ft);$ for Binary Logic-0 (48)

Where,

$s(t)$ is the BPSK modulated output, A is the amplitude of the carrier signal and f is the frequency of the carrier signal.

5.2.2.1 ADVANTAGES OF PSK

- Least P_e among all the three modulation schemes.
- High SNR.
- More power efficient compared to the other two modulation schemes.
- Same bandwidth efficiency as ASK.

5.2.2.2 DISADVANTAGES OF PSK

- Complex than ASK.

5.2.2.3 APPLICATIONS OF PSK

- Broadband modems.
- Satellite communication.
- Mobile phones.

5.2.3 FREQUENCY SHIFT KEYING (FSK)

In this, the frequency of the radio frequency carrier signal is varied in accordance with the amplitude of the modulating digital signal. The binary 1 is represented by the presence of a high frequency carrier signal while binary 0 is represented by the presence of a low frequency carrier signal. When the digital signal is two level only then modulation is called as the Binary Phase Shift Keying (BFSK).

The functional block diagram of BFSK modulation process is shown in figure 36.

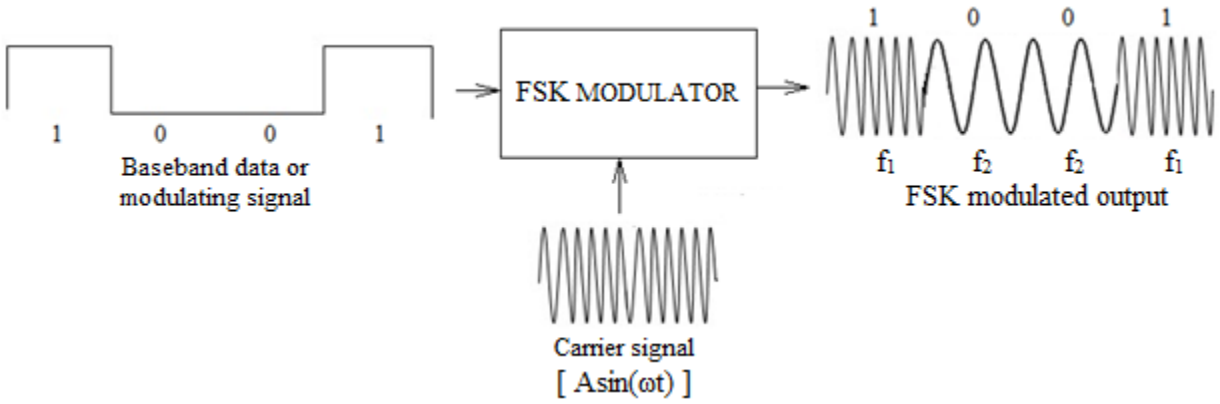

Figure 37: Block diagram of BFSK modulation process

BFSK modulation can be expressed by the following equations

$s(t) = A\sin(2\pi f_1 t);$ for binary logic 1 (49)

$s(t) = A\sin(2\pi f_2 t);$ for Binary Logic-0 (50)

Where $f_1 > f_2$

$s(t)$ is the BFSK modulated output signal, A is the amplitude of the carrier signal and f_1 is the higher frequency of the carrier signal and f_2 is the lower frequency of the carrier signal.

Before modulation the carrier signal is having frequency f but after modulation the amplitude A and phase of the carrier remains unchanged but its frequency is increased to f_1 when modulating binary digital signal is at logic high level and its frequency is decreased to f_2 when modulating binary digital signal is at logic low level.

5.2.3.1 ADVANTAGES OF FSK

- P_e is less than ASK.
- SNR is higher than in ASK.
- Higher noise immunity than ASK.

5.2.3.2 DISADVANTAGES OF FSK

- Largest bandwidth requirement among all the three modulation schemes. Hence it's not a bandwidth efficient modulation scheme.
- The Bit Error Rate (BER) performance in Additive White Gaussian Noise (AWGN) channel is poor when compared to PSK.

5.2.3.3 APPLICATIONS OF FSK

- Many modems uses FSK in telemetry system.
- Used in voice grade lines up to data rates of 1200 bits per second (bps).
- In coaxial cable based Local Area Network (LAN) at high frequencies.
- High frequency data transmission from 3 to 30 MHz.
- In the development and design of modem.

5.3 LITERATURE SURVEY OF DIGITAL MODULATORS

In [58], a circuit for digital modulation purpose is reported. The circuit performs the dual functions of BASK and BPSK simultaneously. The carrier signal applied is sinusoidal in nature, whereas the modulating signal applied is binary in nature. The binary modulating signal controls the switch operation of the circuit. The simulation results are shown for carrier signal frequency of 5 MHz and 20 MHz and frequency for modulating signal is 250 KHz. The circuit is simple, employs one active block i.e. the EXCCII along with one MOS transistor for switching purpose and one resistor. The circuit is versatile and can perform half and full wave rectification also with slight modification.

In [59], a novel modulation circuit is reported that performs BASK and BPSK simultaneously. The circuit consists of one EXCCII, two MOS transistors for switching purposes and three grounded resistors. The circuit is versatile and can perform simultaneous half and full wave rectification also with a little modification. The maximum carrier signal frequency shown in the simulation results is 20 MHz. The circuit provides the advantage of high input impedance for the carrier signal and the modulating signal and involves the use of grounded resistors. The same circuit implementation has also been given using the DXCCII in place of EXCCII.

In [60], a quadrature oscillator is reported that can perform the functions of AM and BPSK modulation also. The circuit consists of two Multiple Output Current Controlled Current Conveyor Transconductance Amplifiers (MO-CCCCTAs) and three grounded capacitors. The circuits has the advantage of having low sensitivity performance.

In [61], the reported circuit can perform BASK and BFSK. The circuit uses CCCII+s, two capacitors and one grounded resistor. The maximum simulated carrier signal frequency shown is 20.78 MHz.

In [62], the proposed circuit uses memristors, one resistor and one capacitor. The word memristor is the short form of Memory Resistor. The binary modulating signal is stored in the memristor.

The modulator is versatile as it performs various modulation processes, i.e., AM, BASK, BPSK, BFSK only with single carrier signal. The circuit works in current mode.

In [63], the circuit uses a digitally programmable Second Generation Current Conveyor (DPCCII) and two grounded resistors to implement a novel BASK modulator that is usually used for modulation of the digital code of Radio Frequency Identifier (RFID). The RFID tags are used for security purposes, animal identification and asset tracking. The circuit offers advantage of high input impedance and can provide amplification to the BASK modulated signal.

In [64], a versatile modulator is reported that can perform BASK, BPSK, BFSK, QAM. The circuit uses a MO-CCII, three fixed valued resistors, three fixed valued capacitors and several digitally controlled switches. The maximum simulated carrier signal frequency shown is 1.5 MHz.

In [65], a novel versatile modulator is presented that can perform various analog and digital modulations namely AM, Frequency Modulation (FM), BASK, BPSK, BFSK and QAM. The circuit operates on low supply voltage of $\pm 0.8V$ and uses single Digitally Programmable Current Differencing Transconductance Amplifier (DP-CDTA) along with two grounded resistors and two capacitors. The maximum simulated carrier signal frequency shown is 34.39 MHz.

In [66], the proposed versatile modulator uses two Multiple Output Operational Transconductance Amplifiers (MO-OTAs), one grounded resistor, three capacitors and a number of switches that can be controlled digitally. The modulator is a digital modulator that can BASK, BPSK, BFSK and QAM

The summary of the above reported digital modulators is shown in table 3.

Table 4: Comparison of the various digital modulators

Reference no.	Active elements	No. of floating / grounded resistors	No. of capacitors	No. of transistors (MOS)	BASK / BPSK	Max. carrier signal frequency shown (Hz)	Supply voltage	Year
[58]	1 EXCCII 1 MOS	1/0	0	23+1	Both	20M	±1.25	2018
[59]	1 EXCCII 2 MOS	0/3	0	21+2	Both	20M	±1.25	2017
[60]	2 MO-CCCCTA	0/0	3	2×26	ASK	2.11M	±0.9	2016
[61]	1 CCCII+	0/1	2	NA	ASK	20.78M	±1.5	2013
[62]	1 VCCS Memristors	0/1	1	NA	Both	1K	NA	2013
[63]	1 DPCCII	0/2	0	18	ASK	125K	±0.75	2013
[64]	1 MO-CCCC	1/2	3	NA	Both	1.5M	NA	2002
[65]	1 Digitally programmable CDTA	0/2	2	67	Both	34.39M	±0.8	2015
[66]	2 MO-OTA	0/1	3	NA	Both	NA	NA	2001
Proposed	1 DXCCII 1 MOS	0/1	0	20+1	ASK	20M	±1.8	-
Proposed	1 DXCCII 2 MOS	0/1	0	20+2	PSK	20M	±1.8	-

5.4 PROPOSED BASK MODULATOR

The proposed BASK modulator is shown in figure 38 below.

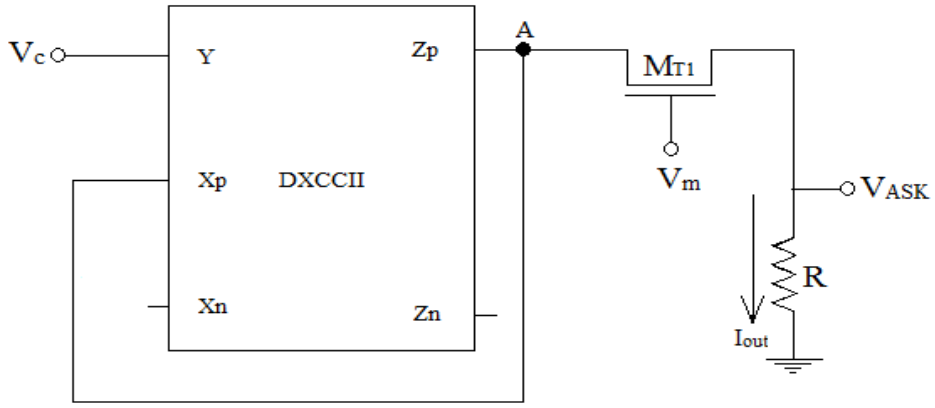

Figure 38: Proposed BASK modulator

The shorted Xp and Zp terminals of the active block DXCCII are connected with the drain terminal of the NMOS transistor M_{T1}. The source terminal of the M_{T1} is connected with one terminal of the resistor R and the other terminal of this resistor R is connected to the ground. The voltage developed across the resistor R is the ASK modulated output voltage denoted by V_{ASK}.

5.4.1 OPERATION OF THE PROPOSED BASK MODULATOR

V_c is the sinusoidal carrier signal. It carries the modulating signal V_m. Voltage V_c is applied at the high input impedance terminal Y of the DXCCII. Voltage V_c is given as

$$V_c = A_c \mathrm{Sin}(2\pi f_c t) \tag{51}$$

Where

A_c is the amplitude of the carrier signal voltage V_c,

t is the time period and f_c is the frequency in hertz (Hz) or $\mathrm{cycles/second}$.

This carrier signal voltage V_c is copied at the Xp terminal of the DXCCII, that is

$$V_{Zp} = V_{Xp} = V_c \tag{52}$$

Voltage V_m is the bipolar modulating signal.
Voltage V_{ASK} is the BASK modulated output voltage signal.

The M_{T1} is used as a switch. The modulating signal V_m is applied at the high impedance gate terminal of this transistor. When voltage V_m is positive, the M_{T1} turns on and works as a closed switch, and when voltage V_m is negative, the M_{T1} turns off and works as an open switch.

The gate voltage of M_{T1} depends on the amplitude of the modulating signal V_m. And the drain voltage of M_{T1} depends on the amplitude of the carrier signal V_c, which is very small as voltage V_c is much smaller in magnitude than voltage V_m. The source voltage of M_{T1} depends on the voltage V_{ASK} developed across the resistor R. Therefore whenever M_{T1} is on, it always works in the non-saturation region or the ohmic region as it always holds the condition of working in ohmic region which is given as

$$V_{DSn} < V_{GSn} - V_{THn} \tag{53}$$

where

V_{DSn} is the drain to source voltage of M_{T1}.
V_{GSn} is the gate to source voltage of M_{T1}.
and V_{THn} is the threshold voltage of M_{T1}. V_{THn} for NMOS is positive.

The on resistance of this M_{T1} used as a switch is denoted by $R_{on,n}$. From [2], for the ohmic region, the resistance $R_{on,n}$ is therefore expressed as

$$R_{on,n} = \frac{1}{(W/L)_n \mu_n C_{ox,n}(V_{GSn} - V_{THn} - V_{DSn})} \tag{54}$$

Where

$(W/L)_n$ is the aspect ratio of M_{T1}

μ_n is the mobility of electron

$C_{ox,n}$ is the gate oxide capacitance per unit area, of M_{T1}

It can be seen from the above equation that the $R_{on,n}$varies with voltage V_{GSn} and voltage V_{DSn}. But, since the on resistance $R_{on,n}$ is much smaller in magnitude than the magnitude of the external resistor R, therefore the effect of variation of $R_{on,n}$ on the BASK modulated output voltage V_{ASK} is negligible. Mathematically, it can be expressed by the following equations written below

$$R_{on,n} \ll R \tag{55}$$

The BASK modulated output voltage is given as

$$V_{ASK} = I_{out} \times R \tag{56}$$

The voltage V_A at node A is equal to the voltage V_{Xp}, that is

$$V_A = V_{Xp} \tag{57}$$

Also, when the M_{T1} is on, then the total resistance $R_{total,n}$ between node A and ground is equal to the sum of the on resistance $R_{on,n}$ of the M_{T1} and the external resistance R, i.e.

$$R_{total,n} = R_{on,n} + R \tag{58}$$

The output current I_{out} is given as

$$I_{out} = \frac{V_A}{R_{total,n}} \tag{59}$$

From equations (57), (58) and (59)

$$I_{out} = \frac{V_{Xp}}{R_{on,n} + R} \tag{60}$$

From equations (55) and (58)

$$R_{total,n} = R_{on,n} + R \cong R \tag{61}$$

Therefore from equations (60) and (61), I_{out} is given as

$$I_{out} \cong \frac{V_{Xp}}{R} \tag{62}$$

Thus from the equations (56) and (62), it can be concluded that the variation in the output current I_{out} because of $R_{on,n}$ is negligible and therefore, the effect on the output voltage V_{ASK} because of the variations in $R_{on,n}$ is also negligible.

When the M_{T1} working as a switch is in off condition than the associated resistance is denoted by $R_{off,n}$. $R_{off,n}$ is ideally infinite as the M_{T1} is in non-conducting state.

Now when the voltage of the modulating signal V_m is positive (logic high), M_{T1} turns on and the equal amount of the currents developed at Xp and Zp terminals of the DXCCII flow towards the node A, which then get added up at the node A as no current goes to the gate terminal of M_{T1} and then the net current flows through the transistor M_{T1} and then flows through the resistor R and then goes to the ground. The two currents developed at Xp and Zp terminals of the DXCCII linearly depend on the voltage V_{Xp} as can be observed from the equation (62). As the voltage V_{Xp} is AC in nature therefore the currents developed because of it are also AC in nature and since these two currents add up at the node A and therefore the resultant current is also AC in nature which flows through the resistor R developing an AC voltage V_{ASK} in return across it which is in phase with the carrier signal voltage V_c. When the voltage of the modulating signal V_m is negative (logic low), M_{T1} turns off and therefore no current flows through the resistor R and the voltage V_{ASK} developed across it is zero. This way, the ASK modulated output voltage V_{ASK} is thus obtained across the resistor R.

The overall operation of the proposed BASK modulator can therefore be summarized by these two equations as mentioned below

$V_{ASK} = I_{out} \times R \cong V_c = A_c \sin(2\pi f_c t)$; when V_m is positive or logic high (NMOS M_{T1} is on)

$V_{ASK} = 0$; when V_m is negative or logic low (NMOS M_{T1} is off)

5.4.2 SIMULATION RESULTS OF THE PROPOSED BASK MODULATOR

The proposed BASK modulator is simulated with SPICE. The CMOS implementation of the active block DXCCII is taken from the reference [35]. 0.35µm CMOS technology parameters are used. The supply voltage for the active block DXCCII is taken as $\pm 1.8V$ and the voltage V_{bias} is set to 1.05V. The aspect ratio (W/L) of the transistor M_{T1} used as the switch is $30\mu m/0.7\mu m$

The waveform of the input carrier voltage signal V_c is shown in the figure 39 below. The carrier signal V_c is having a peak amplitude A_c of 100mV and frequency f_c of 20MHz.

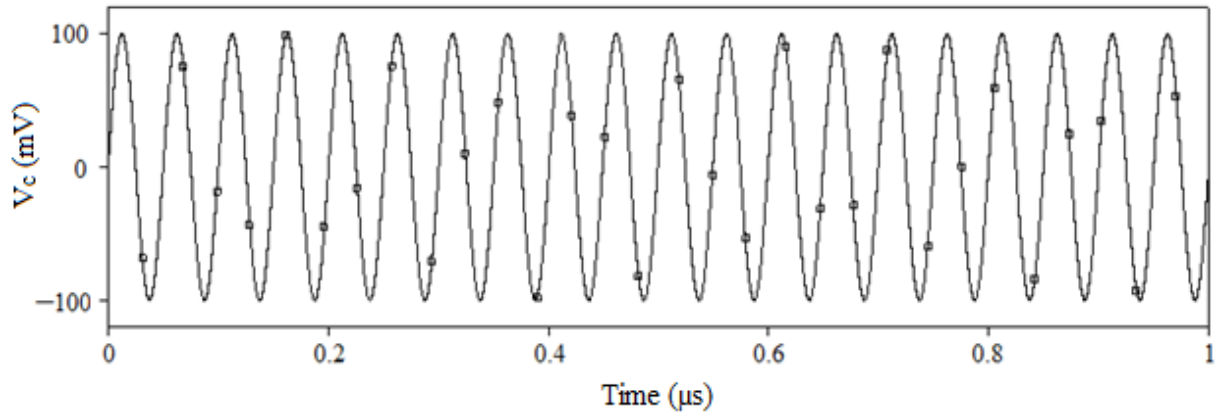

Figure 39: Waveform of the carrier signal V_c

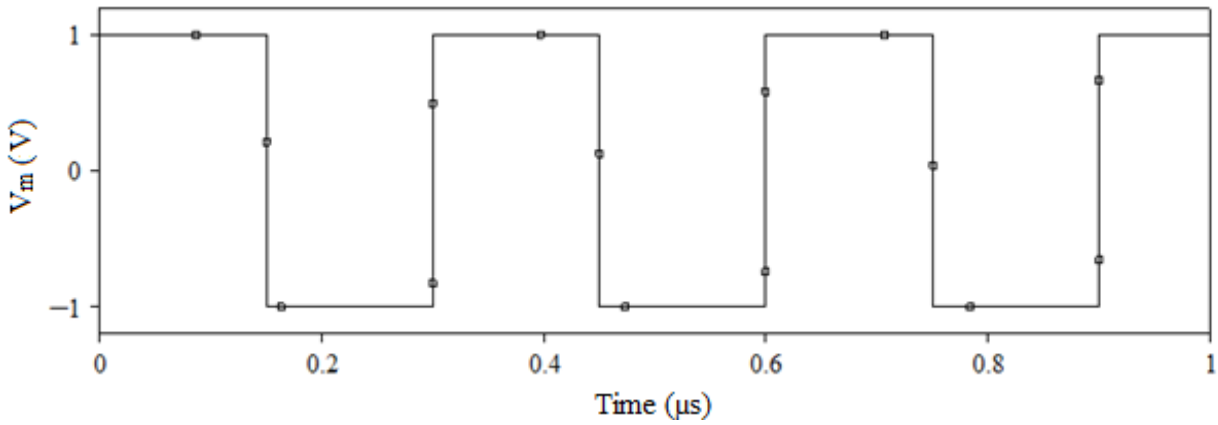

Figure 40: Waveform of the modulating signal V_m

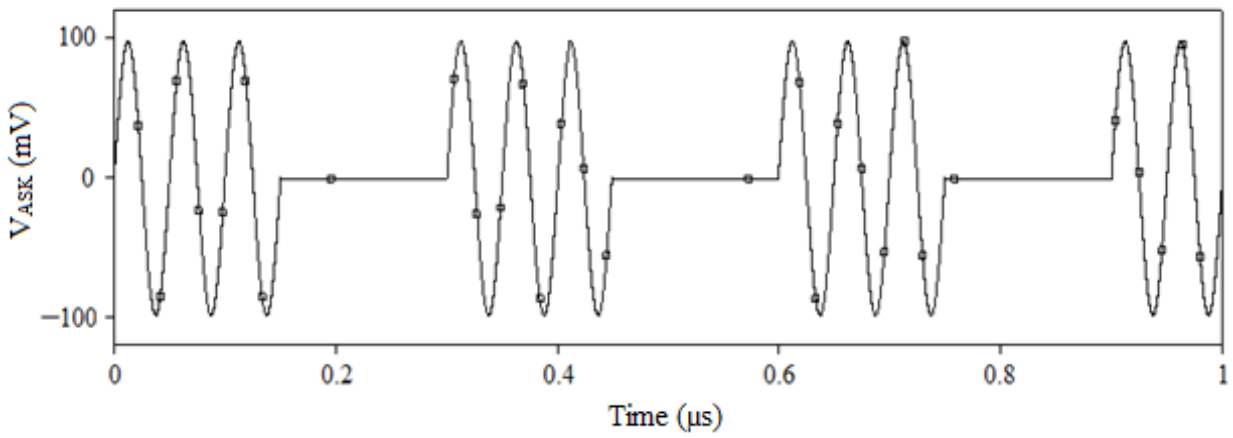

Figure 41: ASK modulated output voltage V_{ASK}

The waveforms for the modulating signal V_m and the ASK modulated output voltage V_{ASK} are shown above in figure 40 and figure 41 respectively.

The logic high and logic low levels of the modulating signal V_m are defined as follows

$V_m = 1V;$ for logic high or logic 1 or bit 1

$V_m = -1V;$ for logic low or logic 0 or bit 0

From the simulation results shown above it can be observed that the information of the modulating signal V_m is transferred in to the BASK modulated signal V_{ASK} with the help of the presence or absence of the carrier signal V_c. That means, when the modulating signal V_m is at logic high level then the BASK modulated signal V_{ASK} is equal to the carrier signal V_c in both amplitude and phase i.e. the presence of carrier signal V_c, and when modulating signal V_m is at logic low level then then the BASK modulated signal V_{ASK} is equal to zero i.e. absence of carrier signal V_c.

5.5 PROPOSED BPSK MODULATOR

The proposed BPSK modulator is shown in figure 42 below.

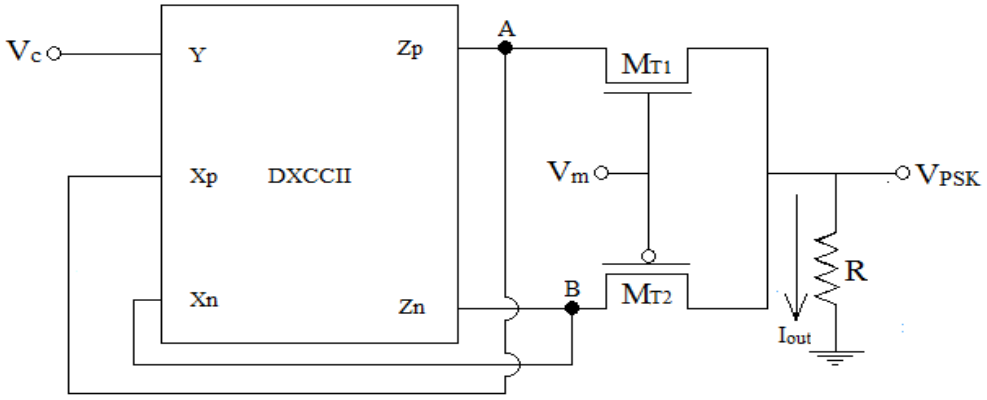

Figure 42: Proposed BPSK modulator

The shorted Xp and Zp terminals of the active block DXCCII are connected with the drain terminal of the NMOS transistor M_{T1} and the shorted Xn and Zn terminals of the active block DXCCII are connected with the source terminal of the PMOS transistor M_{T2}. The source terminal of M_{T1} and the drain terminal of M_{T2} are shorted together and then are connected with one terminal of the resistor R and the other terminal of this resistor R is connected to the ground. The voltage developed across the resistor R is the PSK modulated output voltage denoted as V_{PSK}.

5.5.1 OPERATION OF THE PROPOSED BPSK MODULATOR

V_c is the sinusoidal carrier signal. It carries the modulating signal V_m. V_c is applied at the high input impedance terminal Y of the DXCCII. V_c is given as

$$V_c = A_c \mathrm{Sin}(2\pi f_c t) \tag{63}$$

Where

A_c is the amplitude of the carrier signal voltage V_c,

t is the time period and f_c is the frequency in hertz (Hz) or cycles/second.

This carrier voltage V_c is copied at the Xp terminal of the DXCCII, that is

$$V_{Zp} = V_{Xp} = V_c = A_c Sin(2\pi f_c t) \quad (64)$$

And the voltage developed at the Xn terminal of DXCCII is the inverted carrier voltage V_c, that is

$$V_{Zn} = V_{Xn} = -V_c = A_c Sin(2\pi f_c t) \quad (65)$$

V_m is the bipolar modulating signal.
V_{PSK} is the BPSK modulated output voltage signal.

The M_{T1} and M_{T2} are used as the two switches. The modulating signal V_m is applied at the high impedance gate terminals of these transistors, M_{T1} and M_{T2}. When voltage V_m is positive M_{T1} turns on and works as a closed switch while M_{T2} turns off and works as an open switch. And when voltage V_m is negative M_{T1} turns off and works as an open switch while M_{T2} turns on and works as a closed switch.

The gate voltages of M_{T1} and M_{T2} depend on the amplitude of the modulating signal V_m. And the drain voltage of M_{T1} and the source voltage of M_{T2} depend on the amplitude of the carrier signal V_c, which are very small as voltage V_c is much smaller in magnitude than voltage V_m. The source voltage of M_{T1} and the drain voltage of M_{T2} depend on the voltage developed across the resistor R. Therefore whenever M_{T1} and M_{T2} are on, they always work in the non-saturation region or the ohmic region as they always hold the condition of working in the ohmic region. The conditions for operation in the ohmic region for M_{T1} and M_{T2} are given below in equations (66) and (67) respectively.

For M_{T1}

$$V_{DSn} < V_{GSn} - V_{THn} \quad (66)$$

For M_{T2}

$$V_{DSp} > V_{GSp} - |V_{THp}| \quad (67)$$

where

V_{DSn} is the drain to source voltage of M_{T1}.

V_{GSn} is the gate to source voltage of M_{T1}.

V_{THn} is the threshold voltage of the M_{T1}. V_{THn} for NMOS is positive.

V_{DSp} is the drain to source voltage of M_{T2}.

V_{GSp} is the gate to source voltage of M_{T2}.

V_{THp} is the threshold voltage of the M_{T2}. V_{THp} for PMOS is negative.

The on resistances of the transistors M_{T1} and M_{T2} used as switches are denoted by $R_{on,n}$ and $R_{on,p}$ respectively. From [2], for the ohmic region, the resistances $R_{on,n}$ and $R_{on,p}$ can be expressed as

$$R_{on,n} = \frac{1}{(W/L)_n \mu_n C_{ox,n}(V_{GSn} - V_{THn} - V_{DSn})} \quad (68)$$

and

$$R_{on,p} = \frac{1}{(W/L)_p \mu_p C_{ox,p}(V_{GSp} - V_{THp} - V_{DSp})} \quad (69)$$

where

$(W/L)_n$ is the aspect ratio of the M_{T1}

μ_n is the mobility of electron

$C_{ox,n}$ is the gate oxide capacitance per unit area, of M_{T1}

$(W/L)_p$ is the aspect ratio of M_{T2}

μ_p is the mobility of hole

$C_{ox,p}$ is the gate oxide capacitance per unit area, of M_{T2}

It can be seen from the above equations (25) and (26), that $R_{on,n}$ varies with the V_{GSn} and V_{DSn}, while $R_{on,p}$ varies with the V_{GSp} and V_{DSp}. But, since both of these on resistances i.e. $R_{on,n}$ and $R_{on,p}$ are much smaller in magnitude than the magnitude of the external resistor R therefore the effect of variations of $R_{on,n}$ and $R_{on,p}$ on the BPSK modulated output voltage V_{PSK} is negligible. Mathematically, it can be expressed by the following two equations written below

$$R_{on,n} \ll R \tag{70}$$

$$R_{on,p} \ll R \tag{71}$$

The BPSK modulated output voltage is given as

$$V_{PSK} = I_{out} \times R \tag{72}$$

The voltage V_A at node A is equal to the voltage V_{Xp}, that is

$$V_A = V_{Xp} \tag{73}$$

The voltage V_B at node B is equal to the voltage V_{Xn}, that is

$$V_B = V_{Xn} \tag{74}$$

Also, only of the transistors is on at a time i.e. either M_{T1} or M_{T2}. When M_{T1} is on, then the total resistance $R_{total,n}$ between node A and ground is equal to the sum of the on resistance $R_{on,n}$ of the M_{T1} and the external resistance R. And when the M_{T2} is on, then the total resistance $R_{total,p}$ between node B and ground is equal to the sum of the on resistance $R_{on,p}$ of M_{T2} and the external resistance R. Mathematically $R_{total,n}$ and $R_{total,p}$ are given as

$$R_{total,n} = R_{on,n} + R \tag{75}$$

$$R_{total,p} = R_{on,p} + R \tag{76}$$

When only M_{T1} is on, then the output current I_{out} is

$$I_{out} = \frac{V_A}{R_{total,n}} = \frac{V_{Xp}}{R_{on,n} + R} \quad (77)$$

From equations (70) and (75)

$$R_{total,n} = R_{on,n} + R \cong R \quad (78)$$

Therefore from equations (77) and (78)

$$I_{out} \cong \frac{V_{Xp}}{R} \quad (79)$$

Now when only M_{T2} is on, then the output current I_{out} is

$$I_{out} = \frac{V_B}{R_{total,p}} = \frac{V_{Xn}}{R_{on,p} + R} \quad (80)$$

From equations (71) and (76)

$$R_{total,p} = R_{on,p} + R \cong R \quad (81)$$

Therefore from equations (80) and (81), I_{out} is given as

$$I_{out} \cong \frac{V_{Xn}}{R} \quad (82)$$

Thus from the equations (79) and (82), it can be concluded that the variation in the output current I_{out} due of $R_{on,n}$ and $R_{on,p}$ is negligible and therefore, the effect on the output voltage V_{PSK} because of the variations in $R_{on,n}$ and $R_{on,p}$ is also negligible.

When M_{T1} and M_{T2} working as the switches are in off condition than the associated resistances are denoted by $R_{off,n}$ and $R_{off,p}$ respectively. $R_{off,n}$ and $R_{off,p}$ are infinite ideally as the M_{T1} and M_{T2} transistors are in non-conducting state or off state.

Now when the voltage of the modulating signal V_m is positive (logic high), M_{T1} turns on and M_{T2} turns off and the currents developed at Xp and Zp terminals of DXCCII flow towards node A, which then get added up at node A as no current goes in to the gate terminal of M_{T1} and then the net current flows through the transistor M_{T1} and then through the resistor R and then goes to the ground. The two currents developed at Xp and Zp terminals of DXCCII linearly depend on the voltage V_{Xp} as can be seen in equation (79). As the voltage V_{Xp} is AC in nature therefore the currents developed because of it are also AC in nature and since these two currents add up at the node A and therefore the resultant current is also AC in nature which flows through the resistor R developing an AC voltage V_{PSK} in return across it which is in phase with the carrier signal voltage V_c. And when the voltage of the modulating signal V_m is negative (logic low), M_{T1} turns off and M_{T2} turns on and the currents developed at Xn and Zn terminals of DXCCII flow towards node B, which then get added up at node B as no current goes in to the gate terminal of M_{T2} and then the net current flows through the M_{T2} and then through the resistor R and then goes to the ground. The two currents developed at Xn and Zn terminals of DXCCII linearly depend on the voltage V_{Xn} and it can be seen in equation (82). As the voltage V_{Xn} is AC in nature therefore the currents developed because of it are also AC in nature and since these two currents add up at the node A and therefore the resultant current is also AC in nature which flows through the resistor R developing an AC voltage V_{PSK} in return across it which is 180° out of phase with the carrier signal voltage V_c.

The operation can be summarized by these two equations as mentioned below

$V_{out} = I_{out} \times R \cong V_c = A_c Sin(2\pi f_c t);$ when V_m is positive or logic high (NMOS M_{T1} is on and PMOS M_{T2} is off)

$V_{out} = I_{out} \times R \cong -V_c = -A_c Sin(2\pi f_c t);$ when V_m is negative or logic low (NMOS M_{T1} is off and PMOS M_{T2} is on)

5.5.2 SIMULATION RESULTS OF THE PROPOSED BPSK MODULATOR

The BPSK modulator is simulated with SPICE. The CMOS implementation of the active block DXCCII is taken from the reference [35]. 0.35µm CMOS technology parameters are used. The supply voltage for the active block DXCCII is taken as $\pm 1.8V$ and the voltage V_{bias} is set to 1.05V. The aspect ratios (W/L) of the transistors M_{T1} and M_{T2} used as the switches are same i.e. $30\mu m/0.7\mu m$

The waveform of the input carrier voltage signal V_c is shown in the figure 43 below. The carrier signal V_c is having a peak amplitude A_c of 100mV and frequency f_c of 20MHz.

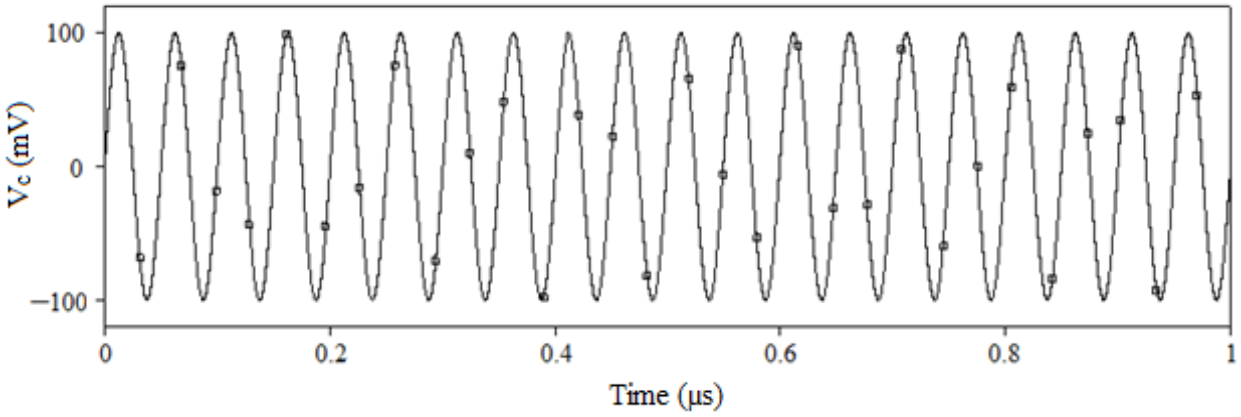

Figure 43: Waveform of the carrier signal V_c

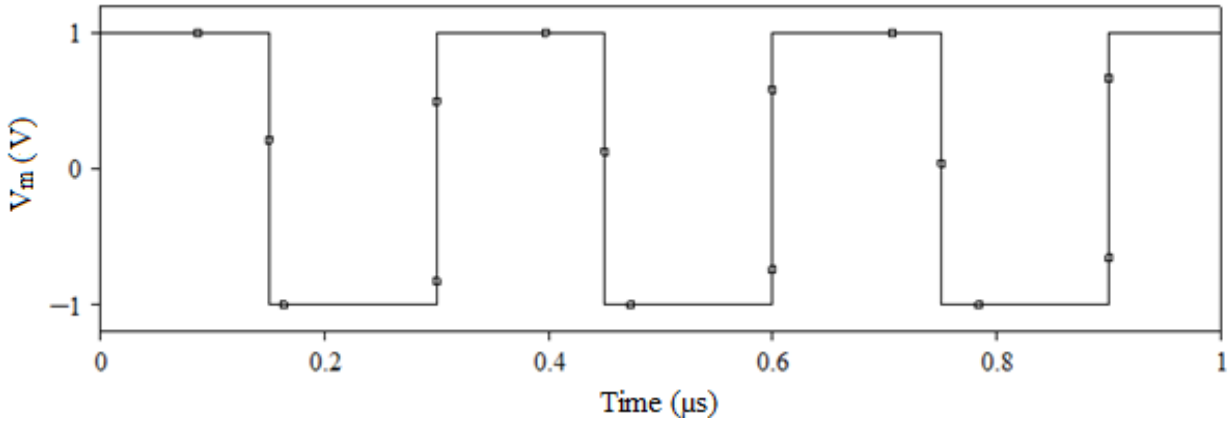

Figure 44: Waveform of the modulating signal V_m

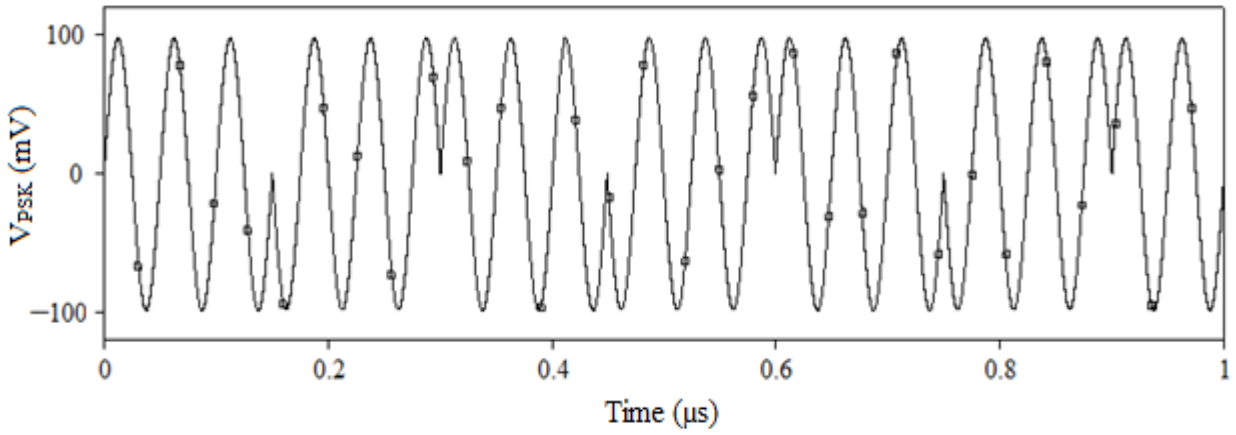

Figure 45: PSK modulated output voltage V_{PSK}

The waveforms for the modulating signal V_m and the PSK modulated output voltage V_{PSK} are shown above in figure 44 and figure 45 respectively.

The logic high and logic low levels of the modulating signal V_m are defined as follows

$V_m = 1V$; for logic high or logic 1 or bit 1

$V_m = -1V$; for logic low or logic 0 or bit 0

From the simulation results shown above it can be observed that the information of the modulating signal V_m is transferred in to the BPSK modulated signal V_{PSK} with the help of the presence of either the in phase carrier signal V_c or the 180° out of phase carrier signal denoted as $-V_c$. That means, when the modulating signal V_m is at logic high level then the BPSK modulated signal V_{PSK} is equal to the carrier signal V_c in both amplitude and phase i.e. the presence of in phase carrier V_c, and when the modulating signal V_m is at logic low level then then the BPSK modulated signal V_{PSK} is equal to the carrier signal V_c with same amplitude but opposite phase i.e the presence of 180° phase shifted carrier denoted as $-V_c$.

In conclusion, the output voltage V_{ASK} of the proposed BASK modulator and the output voltage V_{PSK} of the proposed BPSK modulator can mathematically be written in the tabulated form as shown below in the table 5.

Table 5: Summary of outputs of the proposed BASK and BPSK modulators

Modulating signal (V_m)	**BASK output (V_{ASK})**	**BPSK output (V_{PSK})**
Logic HIGH (1V)	$A_c Sin(2\pi f_c t)$	$A_c Sin(2\pi f_c t)$
Logic LOW ($-1V$)	0	$-A_c Sin(2\pi f_c t)$

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

Three proposed voltage mode precision rectifier circuits have been presented along with their detailed theoretical explanation. The first two proposed circuits are precision half wave rectifiers that provide the rectification of the positive cycle of the input AC voltage signal and negative cycle of the input AC voltage signal respectively. Each half wave rectifier employs one DXCCII, one NMOS transistor and one passive resistor. The third proposed circuit is the precision full wave rectifier that provide the full wave rectification of the input AC voltage signal. The full wave rectifier uses one DXCCII, two NMOS transistors and one passive resistor.

Further two voltage mode digital modulators have been proposed namely BASK and BPSK. BASK employs one DXCCII and one NMOS transistor while BPSK employs one DXCCII, one NMOS and one PMOS transistor.

All the above proposed circuits provide the advantage of having proper input impedance and use of grounded resistor. The rectifiers provide additional advantage of using NMOS transistors in place of diodes which facilitate their easy fabrication.

All the proposed circuits have been simulated with SPICE using 0.35µm CMOS technology parameters. The supply voltage of $\pm 1.8V$ is used. Convincing results have been obtained with all the proposed circuits.

In future, efforts can be made to free the proposed circuits from all the passive elements for example MOS resistor can be employed at the place of passive resistor. Other similar current mode blocks can also be explored for the same work. Also, further efforts can be made to employ the same proposed topologies in the updated technology. Supply voltage and MOS transistors dimensions can be reduced which will provide the enhanced advantage of reduction in the power consumption and area requirement of the devices.

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