INTELLIGENT CONTROL ALGORITHMS FOR DSTATCOM AND ITS APPLICATIONS

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CERTIFICATE

This is to certify that the thesis entitled "**Intelligent Control Algorithms for DSTATCOM and its Applications**" which is being submitted by Mr. **Md. Tausif Ahmad** for the award of degree of **Doctor of Philosophy in Electrical Engineering**, Delhi Technological University, Delhi, is a record of student's own work carried out by him under our supervision and guidance. The matter embodied in this thesis has not been submitted in part or full to any other university or institute for award for any others degree.

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ABSTRACT

Power quality in power distribution systems has been the topic of much research with the significant benefits and advancements in the applications of power electronics at utility appliances due to its compactness; energy efficient and reliability. In a three-phase distribution system, all possible situations are included, which deviate the quality of waveform of voltage or current at the point of common coupling (PCC) from the sinusoidal waveform with amplitude corresponding to the rated root mean square (RMS) value at rated frequency for all three phases have been included. This lures to a decrease of power transfer and a poor power factor. However, distribution systems do not behave in an ideal power quality limit. The systems react dynamically to changes in active and reactive powers, influencing the magnitude of the voltage and power factor of the distribution systems. Quite often, it gives rise to a myriad of losses and operational problems; the power distribution operator has to intervene to try to achieve power redistribution with good quality. The distribution static compensator (DSTATCOM) is one of the custom power devices used to enhance the quality and reliability of power delivered to customers. The functions of DSTATCOM solely depend on developed control algorithms. The developed intelligent control algorithms for the DSTATCOM open up new opportunities for controlling and enhancing power quality without and as well as with integrated renewable sources in power distribution systems. The opportunities arise through the ability of DSTATCOM to control the interrelated parameters that govern the operation of harmonics elimination, load balancing, voltage regulation and power factor improvement.The DSTATCOM integrated distribution system is effectively examined and investigations have been made to mitigate the power quality issues under balanced and unbalanced loads.

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LIST OF SYMBOLS

% !, % ", % #	Phase-a, b, c PCC voltages
!, ", #	Phase-a, b, c supply currents
$!, $", $#	Phase-a, b, c load currents
(!, (", (#	Phase-a, b, c compensating currents components
. and /	Source resistance and inductance
$0_{\&\#}$	DC bus capacitance of voltage source converter
&#	DC bus voltage of voltage source converter
$/_1$	Inductance of interfacing inductor
$\cdot_1$	Resistance of interfacing inductor
$\cdot_2$ and 0_2	Resistance and capacitance of ripple filter
$*_{+!}, *_{+"}, *_{+\#}$	Unit inphase templates
$*_{3!}, *_{3"}, *_{3\#}$	Unit quadrature templates
4	Terminal voltage amplitude of AC bus at PCC
$5_{\&6}$	Cross-correlation vector
$\cdot_6$	Correlation matrix of input data
μ	Step size parameter
$-_{!+}, -_{"+}, -_{\#+}$	Fundamental active power weights of phase a, b ,c of load currents
$-_{!3}, -_{"3}, -_{\#3}$	Fundamental reactive power weights of phase a, b ,c of load currents

7_{8}	Summation neuron
$\Sigma_{8:}$	Summation neuron of active current components
π	Product neuron
λ	Weighted convergence coefficient
η	Weight learning parameter
γ	Stabilization factor
α	Momentum
$-_{;8:<}$, $-_{;8:=}$, $-_{:8:>}$	Summation neuron weight of phase ‘a’, ‘b’ and ‘c’
$-_{?:<}$, $-_{?:=}$, $-_{?:<}$	Product neuron weight of phase ‘a’, ‘b’ and ‘c’
ω and g	Network parametric weights
S, S_1 and S_2	Total set of parameters, set of premise parameters and set of consequent parameters

ABBREVIATIONS

ANN	Artificial neural network
ADALINE	Adaptive linear neuron
BP	Back-propagation
DPI	Discrete proportional-integral
DSTATCOM	Distribution static compensator
DVR	Dynamic voltage restorer
GD	Gradient descent
GDM	Gradient descent with momentum
GNN	Generalized neural network
HB	Hysteresis bandwidth
HPF	High pass filter
IGBT	Insulated-gate bipolar junction transistor
IRP	Instantaneous reactive power
LMS	Least mean square
LPF	Low pass filter
MLPNN	Multilayer perceptron neural network
NN	Neural network
OLS	Optimum least square
PCC	Point of common coupling

CHAPTER 1
INTRODUCTION

1.1 GENERAL

With the growth and development of technologies, power distribution systems and the loads, have increasingly concentrated on the quality of power supply. In the recent years, various highly sensitive medical equipments, high-speed motors, and computer-controlled processing plants, require the power source of high quality and good reliability. Over the last decade, substantial research has been carried out on power distribution systems to overcome most severe power disturbances such as harmonics elimination, mitigation of voltage sags, load balancing, voltage regulation and interruptions of renewable resources [1]. The required techniques have been developed to analyze, predict, and mitigate these disturbances in system-equipment interactions [2]-[3]. To assess and to maintain the good quality of power in power distribution systems, presently electrical supply industries are becoming efficient without compromising the quality of power supply service [4]-[5]. Providing new solutions for this newly power quality paradigm in distribution systems by custom power devices (CPDs) has reduced the complexity, costs and has increased the reliability of power supply [6]-[11].

In addition, the demand for electricity is increasing due to urbanization and growth of population. Renewable energy resources integration is playing an important role to meet the demand in distribution systems. However, issues of power delivery quality of the supply voltage or current from the sinusoidal waveform with the amplitude at rated frequency, have deviated the quality of waveforms.

1.2 STATE OF THE ART ON POWER QUALITY

The power quality problems in the distribution systems are mainly due to the proliferation of different types of nonlinear loads, unplanned expansion of the distribution system, etc [12]-[13]. Therefore, power quality is quantified in terms of voltage, current, or frequency deviation of the supply system, which may result in failure or mal-operation of customer's equipment [8]. The degradation of power quality leads to low power factor, low efficiency, over heating of transformers, and so on. In distribution systems, the power quality problems can reduce the power supplied to the customers from its nominal value. The utility and the users are responsible in polluting the supply network due to operating large loads [14]-[15]. Power quality has taken an increasing importance in view of the widespread use of power electronic equipment [16]-[18]. Power quality problems related to the voltage, are voltage harmonics, surge, sag/dip, spikes, notches, unbalance, swell, fluctuations, and so on at the point of common coupling (PCC) where various loads are connected. However, some power quality problems related to the currents drawn from the AC mains, are poor power factor, reactive power burden, harmonic currents, unbalanced currents, and an excessive neutral current in poly-phase systems due to unbalancing and harmonic currents generated by some nonlinear loads. In distribution systems, power quality issues related to voltage and current drawn from AC mains at point of common coupling (PCC) like unbalanced voltages supply, active and reactive power demands, are affecting performance of customer equipment [19]-[21]. A power quality problem is any occurrence manifested in voltage, current, or frequency deviations, which are major impacts to a distribution system that result in failure of customer equipment [22]-[27]. These aspects become important when power supply is not ideal

i.e., it deals with unbalance, harmonics, faults and fluctuations in frequency [28], [29]. The mitigation of power quality issues has been provided by filters such as passive, active and hybrid in series, shunt or combination of both [30]-[50]. Power electronics based controllers have played a vital role to enhance the quality and reliability of power delivered by electric distribution system. These devices can be shunt connected, series connected or a combination of both series and shunt connected at PCC [51]-[61]. A number of international standards are developed by various organizations such IEEE (Institute of Electrical and Electronics Engineers) and IEC (International Electrotechnical Commission) to specify the permissible limit of power quality problems and to provide guidelines for the end users, manufacturers and utilities to improve the quality of power [62]-[68]. The critical and sensitive loads are protected from power quality problems by monitoring these power quality events. The objectives of power quality monitoring, are prediction of performance of the load and the selection of power quality mitigation system [69]-[79].

Further, with the deregulation of the power industry, competitive pressure forces electric utilities to cut cost, which sometimes affects power quality and reliability. Hence, it must be ensured by suitable regulations that customers do not suffer from reduced power quality and reliability.

1.3 TRANSITION TO SMART POWER DISTRIBUTION SYSTEMS

With the help of intelligent custom power devices (CPDs) in distribution systems such as distribution static compensators (DSTATCOMs), dynamic voltage restorers (DVRs), and unified power quality conditioners (UPQCs), power quality problems arising due to various disturbances in the system or due to the presence of various

nonlinear loads such as furnaces, uninterruptible power supplies (UPSs), and adjustable speed drives (ASDs), which have evolved inherently, can be monitored and mitigated. These intelligent CPDs make the power distribution systems smart [30]-[36]. Intelligent CPDs use experiential knowledge about the process that generally produces a model in terms of input–output behaviour. The acceptable controller to mitigate current related power quality problems at distribution level is distribution static compensator (DSTATCOM), which is also named as an active shunt compensator or filter [52]-[61]. The DSTATCOM is used for mitigation of current related power quality problems such as harmonics distortion, poor power factor, load unbalancing and voltage regulation etc. Tremendous progress in the field of power semiconductor devices and signal processing, has made the cost effective implementation of DSTATCOM [50]-[58]. The research in this area has led to the developments in the area of different configurations and control algorithms for control of the shunt compensator. The DSTATCOM is configured based on the number of switching devices, the use of isolation transformer and the use of type of transformer for neutral current compensation. Mainly DSTATCOM configurations are divided into two major categories such as three phase three wire and three phase four wire [69]-[79].

1.3.1 Limitations of CPDs

The ability of the DSTATCOM as a compensator is impaired by control algorithms of the following steady-state and dynamic-state limitations. The control algorithm should have fast response and stable operation in both steady state and dynamic conditions. The selection of a control algorithm depends upon processing time,

mathematical complexity, fast response, stable operation and easy implementation. The primary objectives of the DSTATCOM in a distribution system are:

- DC link voltage control: Maintaining desired level of voltage, prevention of transient under dynamic condition of load and fast response under steady state.
- Power flow control: Increased power factor, minimization of loop flows and voltage regulation.
- Load balancing: During, transient, steady-state and dynamic state.
- Harmonics elimination: Reduction in losses, reduction in overload capacity and increase in efficiency of utility equipments.

1.3.2 Concept of Intelligent CPDs

The modeling of intelligent CPDs to be computationally efficient to deal with the power quality problems is related to the current drawn from the AC mains. There are three basic approaches to intelligent controls [80].

- Knowledge-based systems
- Fuzzy logic
- Neural networks.

Knowledge-based systems utilize a collection of information in different forms such as facts, heuristics, common sense and other forms of knowledge and use reasoning methods to inferences. In this approach, measurements, process modeling and control can never be exact for real and complex processes. Moreover, there are uncertainties such as incompleteness, randomness, and ignorance of data in the process model [81]-[85].

Fuzzy logic can incorporate certain types of unknown nonlinearity from imprecise and incomplete information by giving definitions to vague terms and allowing construction of knowledge-base in form of rules [86]-[89].

Neural network based control has received considerable interest over the last two decades because neural networks have been shown to be able to approximate any nonlinear function defined on a compact set of data to a specified accuracy and secondly most control systems exhibit certain types of unknown nonlinearity, which suits neural networks as an appropriate control technology [85]-[95].

1.4 SCOPE OF THE WORK

After carrying out a brief literature survey on control algorithms of the CPDs like UPQC, DVR and DSTATCOM, it has been identified that the advanced intelligent control of DSTATCOM builds the distribution system smart and intelligent. The aspects of advanced intelligent control strategies comprise of different issues that include the speed of response, convergence, computational burden, complexity, static error, robustness and stable operation in the steady state and dynamic conditions with verification by an experimental prototype.

The main objectives of the proposed research work are as follows:

- To design and develop a prototype configuration of three-phase distribution system with DSTATCOM in the laboratory.
- To develop the mathematical model of the proposed control algorithms and their experimental realization through the digital signal processor (DSP).
- To investigate the implication on real-time application to mitigate the power quality issues of the configuration taken under consideration.

- To assess the effectiveness of the developed advanced intelligent control algorithms based on neural network and nonlinear adaptive filter under different operating conditions.

The proposed research work has been carried out as follows:

1.4.1 Control Strategy for DSTATCOM

The control strategy for DSTATCOM is implemented in three stages, which are required for implementing developed control algorithms. In the first stage, current and voltage signals are sensed using Hall Effect sensors (LEM make) to take system parameters. In the second stage, developed model of control algorithms on MATLAB Simulink platform, are used to drive the DSTATCOM to deliver current compensation signals in order to mitigate current related issues of power quality. In the third and last stage, the gating signals for controlled switches (IGBTs) are driven using hysteresis current controller (HCC) logic based pulse width modulation (PWM) control technique. To design the control part in real time, digital signal processor (DSP) based on dSpace-1104 is used. Earlier this work has been carried out through complex analog and digital circuits.

1.4.1.1 Sensing of signals

For implementing control algorithm, instantaneous voltage and current signals are sensed. These signals are used to evaluate various parameters like THDs, power factor, crest factor, active and reactive power, etc. The Hall Effect voltage sensors (LV-25P) are used to sense the voltage signals such as phase voltages of AC supply at PCC and DC bus voltage of VSC based DSTATCOM. The Hall Effect current sensors (LA-25) are used to sense current signals such as load currents, supply currents at PCC. Current and voltage

signals have to be filtered to avoid any noise or interference problems using R-C series low pass filter (LPF). The required levels of sensed signals are maintained by dSPACE, which has DSP based platform, by passing through power conditioning circuits. In hardware, the ripple filters are designed using analog circuit.

1.4.1.2 Reference currents generation

The generation of the reference currents comprises of extracted fundamental active and reactive current components of the load current, respectively. The switching has been initiated by taking the error of sensed and reference fundamental currents that results into injecting compensating current signals. To draw compensating current signals, some control algorithm based on either frequency domain or time domain has to be designed.

In frequency domain, Fourier analysis is generally used to extract fundamental current components, for which switching frequency for the device is kept twice of highest frequency component for accurate and effective compensation. Fourier transform has a disadvantage of producing large response time in the system.

In time domain, instantaneous values of compensation currents or voltages are generally derived from polluted currents or voltages signals. Here, a number of control methods have been derived such as synchronous reference frame, instantaneous active and reactive power theory, adaptive filter based techniques etc.

1.4.1.3 Switching pulse generation

The error signal of fundamental current is passed to PWM based hysteresis current control method that generates required gate signals at a frequency of around 10 kHz.

1.4.2 Fast Multilayer Neural Network Based Control Algorithm

The back-propagation learning has various drawbacks such as slowness in learning, stuck in local minima, and requires functional derivative of aggregation and threshold functions to minimize error function. Various researchers have suggested a number of improvements in simple back-propagation learning algorithm [96]-[120]. On the primary objectives of advanced intelligent control, fast multilayer neural network based control algorithm is developed that has enhanced the convergence speed of the developed backpropagation (BP) algorithm in three-phase three-wire distribution system using three-leg VSC for reactive power compensation, harmonics eliminations, and load balancing. The developed algorithm is validated experimentally in the laboratory on the developed prototype of DSTATCOM.

1.4.3 Generalized Neural Network based Control Algorithm

In the available ANN based algorithms, the sigmoid threshold function and ordinary summation or product as aggregation functions in the existing models, fail to cope with the nonlinearities present in the AC supply current or voltage sinusoidal waveforms. To deal with such nonlinearities, the proposed generalized neuron has both sigmoid and Gaussian functions with weight sharing. The generalized neuron has flexibility at both the aggregation and threshold function level to cope with the nonlinearity present in the sinusoidal waveforms [121]-[145]. This new concept has reduced the complexity of multilayer into single layer, which reduces the computational time. GNN has reduced network problem and learning complexity on training of input signals in three-phase three-wire distribution system using DSTATCOM for reactive power compensation,

harmonics eliminations, and load balancing. The developed algorithm is validated experimentally in the laboratory on the developed prototype of DSTATCOM.

1.4.4 Nonlinear Adaptive Filter based Control Algorithm

In the literature survey, the applications of non-linear filter based control algorithms for DSTATCOM, are rarely available. However, linear filter based control algorithms, are effective in a variety of performances improvement of DSTATCOM [146]-[165]. Moreover, in nonlinear signal processing where linear filters do not give satisfactory performance, nonlinear filtering techniques are able to provide better performance. Performance of these control algorithms are analyzed in three-phase three-wire system using three-leg VSC for reactive power compensation, harmonics eliminations and load balancing.

1.5 OUTLINE OF CHAPTERS

This thesis consists of seven chapters including introduction, literature review, design and development of DSTATCOM in a three phase distribution system, which deals with the control strategy for DSTATCOM, realization of developed advanced intelligent control algorithms such as fast multilayer neural network based control of DSTATCOM, generalized neural network based control of DSTATCOM, nonlinear adaptive Volterra second order filter (AVSF) based control of DSTATCOM, main conclusions and suggestions for further work followed by references.

Chapter-1: This chapter covers introductory concepts of power quality issues and their mitigation in a distribution system and transition to smart power distribution system integrated with custom power devices and their control techniques. The scope of work includes advanced intelligent control algorithms for improving power quality problems

such as harmonics, reactive power and load unbalancing. This classification of control algorithms, includes fast multilayer neural network based control algorithm, generalized neural network based control algorithm, and nonlinear adaptive filter based control algorithm.

Chapter-2: The brief literature review on power quality standards, issues, monitoring and their mitigation in the distribution system, is described in this chapter. Further, a comprehensive literature review on multifunction operation and control of DSTATCOM is also reported in detail. The performance of DSTATCOM on configurations and control algorithms for load compensation, is also discussed in this chapter. Based on the exhaustive literature review, identified research areas are presented at the end of this chapter.

Chapter-3: This chapter deals with the design and development of DSTATCOM in a three phase distribution system. Mathematical modeling and selection of various components of DSTATCOM such as VSC, DC bus voltage, DC bus capacitance, interfacing inductors, and ripple filter are presented. Design and testing of voltage sensor circuits, current sensor circuits, and gate driver circuits with signal conditioning for generation of pulses for control of VSC, are discussed here. In addition, the interfacing inductors are also designed in the laboratory for the hardware of prototype of DSTATCOM.

Chapter-4: This chapter addresses the mathematical modeling and analysis of the proposed fast multilayer neural network based control algorithm for DSTATCOM. Mathematical formulation, MATLAB modeling and DSP based implementation of the proposed control algorithms, are discussed in detail. Simulation and test results of the

proposed algorithm are also given in detail. Test configuration of DSTATCOM, has been simulated and validated with the experimental results for linear/nonlinear loads under various conditions.

Chapter-5: This chapter presents a generalized neural network (GNN) based control algorithm and its mathematical formulation for DSTATCOM. Investigations on the performance of GNN based control algorithms include power factor correction and zero voltage regulation modes of DSTATCOM. Mathematical formulation and MATLAB models have been developed for real time applications on a developed prototype of DSTATCOM. The control algorithm investigated, is validated using simulation as well as experimental results obtained on a developed prototype of DSTATCOM at linear/nonlinear loads under various conditions.

Chapter-6: In this chapter, the nonlinear adaptive Volterra second order filter (AVSF) based control algorithm for DSTATCOM is presented and its mathematical formulation is given in detail. The performance of the proposed nonlinear adaptive theory based algorithm such as Volterra second order filter, is demonstrated. Mathematical formulation and MATLAB models, have been developed for real time applications on a developed prototype of DSTATCOM using DSP. Simulation and test results of this algorithm, are given in detail. Performance of the DSTATCOM has been studied through simulation results and validated with the experimental results on developed prototype at linear/nonlinear loads under various conditions.

Chapter-7: This chapter provides a summary of conclusions drawn from the different aspects of the developed control algorithms proposed for DSTATCOM and highlights its

feasibility. Some suggestions are also presented for further work in the areas covered in the thesis at the end of this chapter.

CHAPTER 2
LITERATURE REVIEW

2.1 INTRODUCTION

In this chapter, the literature review is carried out and presented in respect of control algorithms of the custom power devices (CPD) like UPQC, DVR and DSTATCOM. The operating principles of CPDs, their modelling control and applications, are well described [6], [8]-[10]. Distribution Static Compensator (DSTATCOM) is a device to enhance the power quality of the existing distribution system. Over the last two decades, very wide ranges of research publications from different aspects of control algorithms have appeared in the literature. Several publications dealing with power quality mitigation, different configurations of DSTATCOM, and contrary approaches of control algorithms have been reported in the literature [8], [11]. A large number of research publications have appeared in the area of DSTATCOM. A variety of algorithms, have emerged based on conventional, transform, adaptive and soft computing theory [11]. The brief literature review on DSTATCOM of relevant publications is discussed here.

2.2 POWER QUALITY ISSUES AND THEIR MITIGATION

In the recent scenario, power quality has become an issue for power distribution systems. For decades, all over the world, the research has been carried out on the improvement of power quality on different aspects such as voltage, current and frequency deviation. In many research publications, detailed study of the power quality problems, is made including its mitigation with the help of CPDs [1]-10]. The control of the CPDs plays vital role in mitigation and monitoring power supply and even at the suggested standard limits specifications for the required power [11]. Several publications have appeared on

the impact of the deviation of the supply voltage and current waveforms, which have used the term power quality in relation to airborne distribution systems and power systems using CSDs [12]-[18]. The recent increased interest in power quality has been explained in a number of ways [19]-[30]. Consequences of the increased interest in power quality are given and summarized by many researchers in their publications [31]-[45].

2.2.1 Equipments Sensitive to Voltage Disturbances

Power electronics and electronic equipments have especially become much more sensitive than its counterparts of last two decades. Voltage disturbances have introduced increased sensitivity to term power quality often cited in the research publications [46]-[58]. These equipments have become more sensitive, companies have also become more sensitive to loss of production time due to their reduced profit margins [42], [46]. In this modern technology, the electricity is more and more in demand, the grid integration of renewable energy resources (RES) looks a solution. The consequence is that an interruption of the supply with poor quality, leads to complaints, even if there are no damages or costs related to it.

2.2.2 Equipments Cause Voltage Disturbances

Due to the disturbances in the supply voltage, the equipment tripping is often described by customers as a “bad power quality”. At the other end of the utilities, the disturbances in main power quality, are due to the end-user equipment. Modern utility appliances and medical equipments are equipped with the power electronics converters, which are not only sensitive to voltage disturbances but they also cause disturbances for other customers at the point of common coupling (PCC). The increased use of converter-driven equipment such as computers and consumer electronics, adjustable-speed drives have also led to a large growth of voltage disturbances. The rectifiers and inverters have given

rise to non-sinusoidal currents [47]-[56]. The input current not only contains a fundamental frequency component, but it also consists of its multiple of the fundamental frequency so-called harmonics components. The harmonic distortion of the currents leads to harmonic components in the supply voltages [57]-[61]. Recently, equipment via power electronic converters produced harmonic distortion, has enormously increased in the last few decades. Moreover, adjustable-speed drives also cause a large part of the harmonics voltage distortion. Each individual device does not generate many harmonic currents but all of them together cause a serious distortion of the supply voltages [23]-[36].

2.2.3 Standardization and Performance Criteria

The consumers are to be viewed as "load". The consumers deal with the interruptions and other voltage disturbances at utility end, and the utility has decided what has been reasonable. Taken under consideration, certain characteristics have been recommended by power quality standards [62]-[68]. Any customer who has not been satisfied with the offered reliability and quality, has to pay the utility for improving the supply [65]. The qualitative and quantitative voltage or current disturbances from utility need to be improved at PCC, so that; it does not impact on other customers one way or the other. The DSTATCOM is viewed as one of the CPDs with certain characteristics, which mitigates power quality issues improving the power supply, delivers the electrical energy with a given reliability and quality in a distribution system [69]. The DSTATCOM performance results have been viewed as the solutions of all issues of power quality taken under considerations for reliable and quality power at PCC of the distribution systems [70]. It is no longer that the customer has argued that the utility is responsible for reliable and quality power. However, what about the control of the DSTATCOM? The control of

DSTATCOM states the responsibility of power quality problems mitigation, so that the customer has a reliable and quality electrical power supply [71].

2.3 POWER QUALITY STANDARDS

A number of international standards have been developed by various organizations such as IEEE (Institute of Electrical and Electronics Engineers) and IEC (International Electrotechnical Commission) to specify the permissible limit of power quality problems and to provide guidelines for the end users, manufacturers, and utilities to improve the quality of power [62]-[68]. The critical and sensitive loads are protected from power quality problems by monitoring these power quality events. The objectives of power quality monitoring, are prediction of the load performances and the selection of power quality mitigation system [67].

2.4 POWER QUALITY MONITORING

The power quality monitoring can provide the information such that safety hazards resulting from equipment maloperation or the failure can be avoided. Guidelines and specifications database improve equipment compatibility for developing future equipment improvements. In addition, causes for disturbances can be recorded and used to make system improvements. For assessing the harmonics distortion, performance indices that measure system reliability in terms of voltage outages, are defined by standard guidelines. Power quality monitoring is required since its inception at the utility. However, as a result of deregulation in the customers, the power quality is likely to fall below the prescribed standard limit. Hence, feeders supplying their major customers are likely to undertake monitoring on control of power quality. The data required to monitor power quality are usually voluminous.

2.4.1 Utilities Demand for Good Power Supply

In this world of technology, most utilities require a good power supply that has been committed to that for many decades. Designing a distribution system with a DSTATCOM has given high reliability of supply, for a limited cost. It is appealed to resolve many power quality issues of industry, and hopefully it still does in the future.

2.4.2 Good Power Supply

The high quality of the supply voltage in the presence of DSTATCOM, avoids the phenomena like voltage sags, load unbalancing, voltage regulation and harmonics distortion due to the interruptions that are imposed by consumers always.

2.4.3 Measurements of Power Quality

The availability of electronic devices to measure and record waveforms, has certainly contributed to the interest in power quality. Harmonic currents and voltage sags have been simply hard to measure on a large scale in the past. Measurements have been restricted to rms voltage, frequency, and long interruptions; phenomena, which are now considered part of power quality, but have been simply part of power system operation in the past.

2.5 INVESTIGATIONS ON PERFORMANCE OF DSTATCOM

Passive shunt filters or VAR compensation techniques are known to be effective in shunt compensation for power quality improvement and the control at distribution systems. However, the utility appliances are operating on principle of power electronics converters where passive filters do not give satisfactory performance, active shunt filtering techniques are able to provide improved performance at distribution systems.

Power distribution system can also be seen as the interconnection of generating renewable energy sources (RES) and customer loads through a distribution network. However, distribution systems do not behave in an ideal power quality limit. The systems react dynamically to changes in active and reactive powers, influencing the magnitude of the voltage and power factor of the distribution systems. Quite often, it gives rise to a myriad of losses and operational problems; the power distribution operator has to intervene to try to achieve power redistribution with good quality. Substantial literature has been reported on the shunt compensators and their control techniques for power quality improvements at distribution level. Shunt compensation provides several power quality improvement features such as harmonics elimination, reactive power compensation, load balancing and PCC voltage regulation [28]-[61]. The distribution static compensator (DSTATCOM) is one of the custom power devices used to enhance the quality and reliability of power delivered to customers [32]-[53]. The functions of controllers solely depend on developed control algorithms. The developed control algorithms for the DSTATCOM open up new opportunities for mitigating and enhancing power quality without and as well as with integrated renewable source in power distribution systems. The opportunities arise through the ability of CPDs to control the interrelated parameters that govern the operation of harmonics elimination, load balancing, voltage regulation and power factor improvement. These constraints cannot be overcome, while maintaining the required system reliability, by means of passive filter or VAR compensation. By controlling DSTATCOM as shunt compensator, the distribution line can be made to carry good quality power closer to its specified rating. Thus, the custom power devices in a power distribution system, can potentially overcome the issues

of harmonics elimination, load balancing, voltage regulation and power factor improvement. By facilitating current compensation using DSTATCOM, these issues have been overcome within the allowable limit of total harmonic distortions (THDs) to enhance power transfer in the distribution system.

2.5.1 Principle of Operation and Control of DSTATCOM

DSTATCOM is used in correcting power factor, maintaining constant distribution voltage and mitigating harmonics in a distribution network. The main advantage of the DSTATCOM is the ability to generate the rated current at virtually any network voltage and an improved dynamic response and the use of a relatively small capacitor on the DC bus. It is connected near the load in the distribution systems. The main components of a DSTATCOM are as follows:

- Voltage Source Converter (VSC)
- DC link capacitor
- One or more inverter modules
- An AC filter
- Interfacing inductors
- Sensors
- PWM control strategy
- Processor (DSP)

The performance of the mitigating devices further depends on the control technique of these devices. Researchers and scientists are contributing to this field by investigating various mitigation devices and their control techniques. There are several studies

contributed by many researchers and engineers on control algorithms of the DSTATCOM [54], [60].

The internal control of DSTATCOM is a prerequisite to generate gating pulses of its VSC and to achieve desired performance in steady state as well as dynamic load conditions.

2.5.2 Classification of DSTATCOM Configurations

Different configurations of DSTATCOM are possible, which include three-leg, four-leg and six-leg VSCs, respectively [59], [69].

Karanki *et al* [70] have proposed a DSTATCOM topology with reduced DC-link voltage rating for load compensation with non-stiff source. With the reduction in DC-link voltage, the average switching frequency of the insulated gate bipolar transistor (IGBT) switches of the DSTATCOM is also reduced. Kim *et al* [55] have described three-phase three-wire series active power filter, which compensates for harmonics and reactive power. Singh *et al* [59] have presented a T-connected transformer and three-leg VSC based DSTATCOM configuration to a three-phase four-wire power distribution system for power quality improvement. Moreover, Singh *et al* [74] have given a comprehensive study of DSTATCOM configurations. Ertao *et al* [76] have discussed an improved transformer winding tap injection DSTATCOM topology for medium-voltage reactive power compensation. Chandan *et al* [78] have proposed an improved hybrid DSTATCOM topology to compensate nonlinear loads.

2.6 REQUIREMENT OF CONTROL ALGORITHMS IN DSTATCOM

The control algorithms required for DSTATCOM, are used to estimate the reference supply currents. The PCC voltages, supply currents, load currents and self-sustained DC bus voltage of VSC, are sensed and given input to the control algorithm. These input

signals are processed in the control algorithm and reference supply currents are estimated. The estimated reference supply currents are compared with the sensed supply currents and generated currents errors, which are used to drive PWM current controller, for generating switching pulses for IGBTs of three phase VSC used as a DSTATCOM.

2.6.1 Investigations on Control Algorithms of DSTATCOM

Performance of DSTATCOM depends on control algorithms used for generation of reference currents. These control algorithms are categorised as conventional control algorithms, adaptive theory based control algorithms, transform based control algorithms and artificial intelligence based control algorithms. Many control algorithms based on mathematical approach and soft computing techniques like neural network and neuro-fuzzy control algorithm, etc. are reported in the literature [91]-[95]. The application of the control algorithms is to ensure switching of power devices that result into the improvement of the performance of DSTATCOM. Nowadays, artificial intelligence based techniques mainly based on neural network are used at large scale.

The performance of the categorised algorithms is available in the literature, which are studied in power factor correction (PFC) and voltage regulation modes under nonlinear loads. These developed algorithms are investigated in various isolated power distribution systems and renewable energy source integrated grid.

The developed control approach provides self-adjustment of controller parameters in real time to achieve desired performance in steady state and dynamic load conditions. The control algorithms investigated, include linear adaptive theory, multilayer neural network and mathematical approach. Different variations of algorithms are studied and compared to control DSTATCOM [71]-[73].

Artificial intelligence based control algorithms work on the principle of human intelligence to achieve a specific task for which they are designed. These control algorithms have the capability of learning, self-organizing or self-adapting. The control algorithms investigated under this category, are based on intelligent techniques such as linear adaptive theory, real-time recurrent learning (RTRL) and neural network for the control of three-phase DSTATCOM.

2.7 IDENTIFIED RESEARCH AREAS

Based on the exhaustive literature review on the design and development of DSTATCOM and its control techniques, it has been identified that there are some major issues in the development of control algorithms, which needs to be investigated. These issues include the speed of response, convergence, computational burden, complexity, static error, robustness and stable operation in steady state and dynamic conditions. Therefore, these issues have been taken under consideration to develop intelligent control algorithms to mitigate the problems of power quality in a three phase distribution system. The aim of the control scheme is to maintain constant voltage magnitude and sinusoidal voltage and current waveforms of the grid at the point where a sensitive load is connected, under unbalanced conditions.

2.8 PROBLEM FORMULATION

Keeping in view of these research gaps, intelligent control algorithms (ICAs) with the following features are selected for investigations:

- Fast convergence rate and dynamic response
- Small steady state error
- Good detection accuracy
- Wide range of adjustment of internal parameters

- Fast response, flexibility and robustness

ICAs improve the performance of DSTATCOM to mitigate the issues of power quality at distribution level delivering power to linear/ nonlinear loads.

Three phase distribution system configurations with DSTATCOM are considered in the presented research work in the following manner:

- Solid state devices such as IGBTs with anti-parallel diodes, are used as switch of VSC.
- VSC is placed suitable to weak AC networks, i.e. without local voltage sources.
- High-frequency switching is required for VSC operation.
- ICAs provide fast switching to IGBTs.
- Specified vector control strategy can perform independent control of active/reactive power at both ends.
- For power reversal, the DC voltage polarity remains the same for VSC based system.

2.9 CONCLUSIONS

The extensive research work has been carried out in the area of nonlinear adaptive theory application, fast training and convergence as well as reduced multilayer neural network concept in the developed intelligent control algorithms and its applications for DSTATCOM to enhance the power quality of three-phase distribution systems. This technology has been found to be well established and practical shunt compensators are installed at distribution level for mitigating current related power quality problems. It has been concluded after review of the literature that the significant development is carried

out in the broad area of active shunt compensators. However, there exists a scope in terms of development of fast, less complex and accurate control algorithms with less computational burden. The application of DSTATCOM for integrating RES such as photovoltaic (PV) generation to the grid is a recent trend and needs to be explored further.

CHAPTER 3
DESIGN AND DEVELOPMENT OF DSTATCOM

3.1 INTRODUCTION

In this chapter, design and implementation of a voltage source converter (VSC) based distribution static compensator (DSTATCOM) having the coupling inductor topology, are carried out in a three phase system. Three phase VSC with full-bridge IGBT modules based DSTATCOM with coupling inductors for connection to medium voltage bus at distribution level, input filter, and uncontrolled diode rectifier as nonlinear load, constitute the prototype system. The power stage of VSC based DSTATCOM is composed of high rating of IGBT modules for the elimination of harmonics, reactive power compensation and AC bus voltage regulation. An input filter is used to filter out the switching harmonics of the converter.

A two level, 3 leg converter is used with PWM technique as DSTATCOM. This offers low quantities of harmonics with optimised switching frequency. The high frequency switching of DSTATCOM induces ripples that are suppressed using an RC filter across supply voltages at PCC. At one end of PCC, linear/nonlinear loads are connected to the balanced source voltages of a three phase distribution system. The proposed DSTATCOM uses the PCC voltages in the reference current generation algorithm. In the simulation study, realization and control of DSTATCOM are carried out as a current source and hence it is termed as current control mode of operation. An experimental prototype of DSTATCOM is developed and realized with the control algorithms using a digital signal processor (DSP). The simulated performance results are validated with the test results obtained on a prototype in the laboratory.

The system configuration, simulation and hardware development of DSTATCOM are discussed in detail in different sections of this chapter.

3.2 CONFIGURATION OF DSTATCOM

The developed DSTATCOM configuration used in a three phase distribution system is shown in Fig. 3.1. A three leg VSC along with interface inductors (L_f) known as DSTATCOM, is shunt connected at PCC. Each leg of VSC connected two power semiconductor devices as IGBTs and an anti-parallel diode combination in series, are connected to a common DC storage capacitor (C_{dc}). A path for C_{dc} to sustain the voltage (V_{dc}), is provided at PCC. By placing additional series R_r- C_r filters called ripple filters at PCC suppress the high frequency harmonics of DSTATCOM.

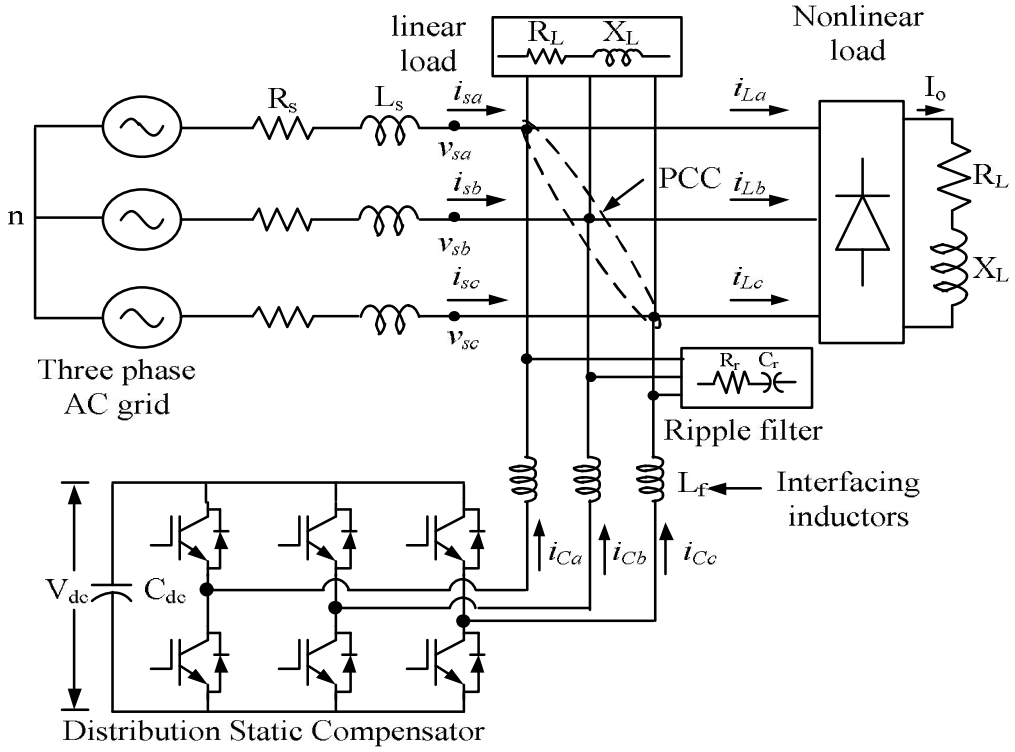


Fig. 3.1 DSTATCOM in a three phase distribution system

A three phase distribution grid of PCC voltages v_{sa}, v_{sb} and v_{sc} in series with source impedance R_s- L_s feeds the linear and nonlinear loads. The three phase loads are

realized using series R- L branch in star connection as linear load whereas a diode based bridge rectifier module loading with a series R- L branch as nonlinear load. The operation of DSTATCOM is realized through a control algorithm.

3.3 PRINCIPLE, OPERATION AND CONTROL OF DSTATCOM

DSTATCOM is a shunt device, which is built around a VSC with a DC bus capacitor interfaced through inductors at PCC to a distribution system. The VSC consists of IGBT switches, which are turned on and off through the gate driver circuits. The anti-parallel diodes allow flow of currents in the reverse direction. The gating pulses to the DSTATCOM are generated using hysteresis (carrier less PWM) or PWM (fixed frequency) current control over reference and sensed supply currents resulting in an indirect current control. DSTATCOM performs load compensation i.e. power factor correction (PFC), harmonics filtering, load balancing and voltage regulation when connected to a distribution bus. The operating characteristics of a DSTATCOM, are to inject an unbalanced and harmonically distorted currents to eliminate unbalance or distortions in the consumer load currents or otherwise in the system and it provides balanced currents in the supply with its DC bus voltage regulation.

3.3.1 Load Compensation using DSTATCOM

The distribution system feeds the loads, which may be reactive, nonlinear and unbalanced with DSTATCOM as shown in Fig. 3.2 (a). The DSTATCOM is operating in current control mode, therefore, it is represented by the current source i_C as depicted in Fig. 3.2 (b). In this mode, the VSC maintains the DC bus voltage constant against any unbalance or distortion in the distribution system. The RMS output voltage between phases of VSC is given as,

$$V_{L-L} = \frac{\sqrt{3}mV_{dc}}{2\sqrt{2}} \tag{3.1}$$

Where V_{dc} is the DC bus voltage and m is the modulation index. The DSTATCOM is able to supply leading reactive power if V_{L-L} is greater than v_{ab}, the line voltage of AC bus at PCC, otherwise it draws lagging reactive power from distribution grid. Referring to Fig. 3.2 (b), using KCL at PCC, the load current i_L is defined as,

$$i_L = i_s + i_C \tag{3.2}$$

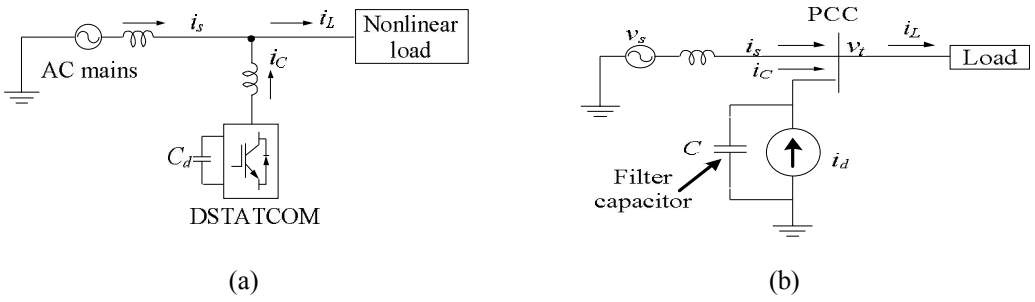


Fig. 3.2 (a) Schematic diagram of compensation (b) ideal load compensation

Before switching ON of DSTATCOM, the compensator current component i_C is zero, hence, the supply current i_s is same as the load current i_L. This makes the supply currents i_s unbalanced and distorted if the load is reactive, nonlinear and unbalanced. For such loads, the load current i_L at k^{th} sampling instant has fundamental and harmonic parts, which are given as,

$$i_L(k) = \mathrm{I}_{fL}\sin(\omega k + \phi_f) + \sum_{h=3,5,7\ldots}^{\infty} \mathrm{I}_{\mathrm{hL}}\sin(h\omega k + \phi_h). \tag{3.3}$$

Where I_{fL} is the peak amplitude and ϕ_f is the phase angle of the fundamental part of load current, ω is the angular frequency. Likewise, I_{hL} is the peak amplitude and ϕ_h

is the phase angle of the harmonic part of load current, respectively. The load current in eq. (3.3) is given as,

$$i_{fL}(k) = \mathrm{I}_{fL}\sin\left(\omega k + \phi_f\right) \; and \qquad i_{hL}(k) = \sum_{h=3,5,7\ldots}^{\infty} \mathrm{I}_{\mathrm{hL}}\sin(h\omega k + \phi_h) \qquad (3.4)$$

With the help of trigonometric function, the fundamental and harmonic parts in eq. (3.4) of the load current, are expanded that results in active power current components and reactive power current components in each part, respectively. Hence eq. (3.4) may be expressed as,

$$i_{fL}(k) = \mathrm{I}_{fL}\sin\omega k\cos\phi_f + \mathrm{I}_{fL}\sin\phi_f\cos\omega k = i_{fLp} + i_{fLq} \quad and$$

$$i_{hL}(k) = \sum_{h=3,5,7\ldots}^{\infty} \mathrm{I}_{\mathrm{hL}}(\sin h\omega k\cos\phi_h + \sin\phi_h\cos h\omega k) = i_{hLp} + i_{hLq}. \qquad (3.5)$$

Therefore, the load current is expressed as,

$$i_L = i_{fLp} + i_{fLq} + i_{hLp} + i_{hLq}. \qquad (3.6)$$

The DSTATCOM generates a current i_C such that it should compensate for fundamental reactive component (i_{fLq}), harmonic components (i_{hLp}, i_{hLq}) and unbalancing of the load current in such a way that the supply current i_s provides only fundamental active current (i_{fLp}) component of the load current.

$$i_s = i_{fLp}$$

$$i_C = i_{fLp} + i_{fLq} + i_{hLp} + i_{hLq} - i_{fLp}$$

The compensator injects current that has reactive and harmonic components only given as,

$$i_C = i_{fLq} + i_{hLp} + i_{hLq}. \qquad (3.7)$$

3.3.2 Voltage Regulation using DSTATCOM

The schematic diagram of an ideal shunt compensator acting as a voltage regulator is shown in Fig. 3.3 (a). Here, the ideal compensator is represented by a voltage source and it is connected to the PCC. However, it is difficult to realize this circuit and the alternate structure is shown in Fig. 3.3 (b). It can be seen that this is the same structure as used for load compensation. It has the advantage that the harmonics can be bypassed by the filter capacitor C.

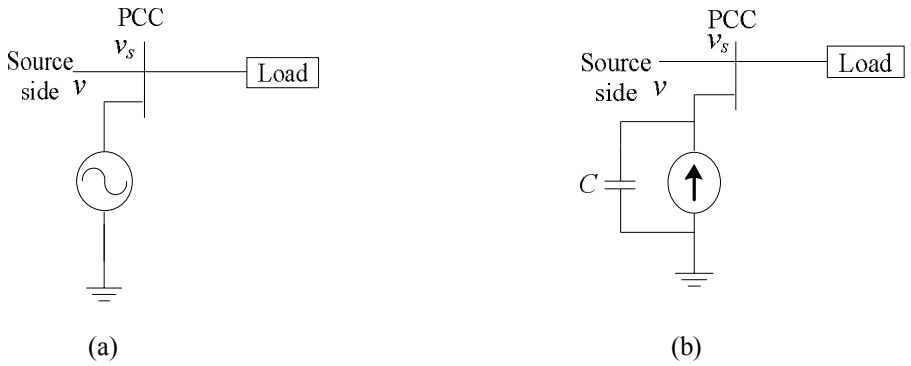


Fig. 3.3 (a) Ideal voltage controller (b) Practical realization

The basic idea here is to inject the current i_C in such a way that the voltage V_t (amplitude of v_s) follows a specified reference. The compensator must be operated such that it does not inject or absorb any real power in the steady state. Therefore, the relations given in eqn. (3.1) and eqn. (3.7) are also valid in this case. The value of the voltage V_t can be arbitrarily chosen. However, its phase angle must be chosen such that the relation $i_s = i_{fLp}$ is satisfied.

3.4 DESIGN OF DSTATCOM

For the development of a prototype of DSTATCOM in a three phase distribution system, the selection of DSTATCOM configuration involves design, estimation and selection of various components such as VSC, interfacing inductors, and a ripple

filter. The design of interfacing inductors and a ripple filter, are carried out to limit the ripple in the currents and voltages. The specification of a DC bus capacitor depends on its energy storage capacity during transient conditions. The rating of these components, depends upon the compensation requirement such as harmonics elimination, reactive power compensation and load balancing. The choice of the DSTATCOM depends on the required reactive power, harmonics compensation and degree of unbalancing in the load. The current rating of the DSTATCOM is selected for load power rating of 25kVA and its voltage rating for DC bus voltage designed for 415V, 50Hz supply. The design equations for the estimation and selection of the components are given in the following sections.

3.4.1 Mathematical Modeling of DSTATCOM

Fig 3.4 shows the equivalent circuit of DSTATCOM connected to a distribution system through interfacing inductors. v_{sa},v_{sb},v_{sc} which represent the three phase line-to-neutral system voltages at PCC. e_a, e_b, e_c represent the fundamental three phase line-to-neutral output voltages of the DSTATCOM's converter. The resistance (R_f) and inductance (L_f) represent reactance of interfacing inductors. R_p accounts for losses in the converter. i_{Ca}, i_{Cb}, i_{Cc} represent line currents flowing through VSC. C_{dc} is capacitance on DC side of converter.

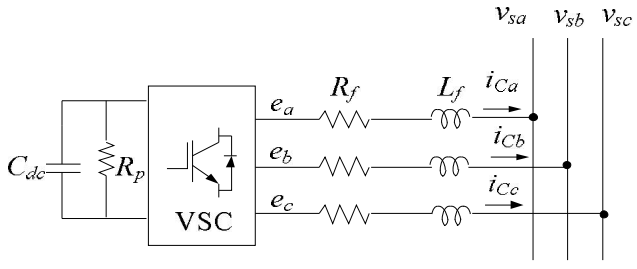


Fig. 3.4 Equivalent circuit of DSTATCOM

From Fig.3.4, KVL equations at PCC can be written as,

$$e_a = i_{Ca}R_f + L_f\frac{di_{Ca}}{dt} + v_{sa} \tag{3.8}$$

$$e_b = i_{Cb}R_f + L_f\frac{di_{Cb}}{dt} + v_{sb} \tag{3.9}$$

$$e_c = i_{Cc}R_f + L_f\frac{di_{Cc}}{dt} + v_{sc} \tag{3.10}$$

In matrix form, these equations can be written as,

$$\frac{d}{dt}\begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & 0 & 0 \\ 0 & \frac{-R_f}{L_f} & 0 \\ 0 & 0 & \frac{-R_f}{L_f} \end{bmatrix}\begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} e_a - v_{sa} \\ e_b - v_{sb} \\ e_c - v_{sc} \end{bmatrix} \tag{3.11}$$

If $\frac{d}{dt}$ is represented as p, then above eqn. (3.11) becomes as,

$$p\begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & 0 & 0 \\ 0 & \frac{-R_f}{L_f} & 0 \\ 0 & 0 & \frac{-R_f}{L_f} \end{bmatrix}\begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} e_a - v_{sa} \\ e_b - v_{sb} \\ e_c - v_{sc} \end{bmatrix} \tag{3.12}$$

Converting a-b-c to d-q quantities using Parks transformation using eqn. (3.12), it can be written as,

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta - \frac{2}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix}. \tag{3.13}$$

eqn. (3.12) and eqn. (3.13) can be written as,

$$p\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & \omega \\ -\omega & \frac{-R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} e_d - v_d \\ v_q - e_q \end{bmatrix} \quad (3.14)$$

where, $\omega = \frac{d\theta}{dt}$, eqn. (3.14) may be written in the following form,

$$p\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & \omega \\ -\omega & \frac{-R_f}{L_f} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad (3.15)$$

Where, $x_1 = \frac{1}{L_f}(e_d - v_d)$ and $x_2 = -\frac{1}{L_f}(e_q)$. Considering that q-axis coincides with the voltage vector v_d, then v_q becomes zero. Neglecting the voltage harmonics produced by the inverter, one can write the pair of equations, for e_d and e_q as,

$e_d = kV_{dc}\cos\alpha$ and $e_q = kV_{dc}\sin\alpha$

where k is a factor, which relates the DC-side voltage, V_{dc} to the amplitude (peak) of the phase–to-neutral voltage V_{ta} at AC-side terminal of the DSTATCOM. V_{dc} is DC bus voltage and α is the angle by which the DSTATCOM voltage leads the line voltage vector.

3.4.2 Design of DC Bus Voltage

For proper operation of the VSC as DSTATCOM, a minimum DC-link voltage is needed to obtain current compensation waveforms. The required DC-link voltage is obtained through rectification mode of VSC. To have a full control of the VSC, the diode across the IGBT must be polarized negatively at all values of ac-voltage supply. To keep the diodes blocked, one needs to ensure a DC-link voltage higher than the peak DC-voltage generated by the diodes alone. Theoretically for rectification mode

of VSC, the maximum DC output voltage is the peak value of line-to-line RMS voltage as shown in Fig. 3.5, is given as,

$$V_{dcmin} > \sqrt{2}V_{L-L(rms)} = \sqrt{2}.\sqrt{3}V_{L-N(rms)}$$

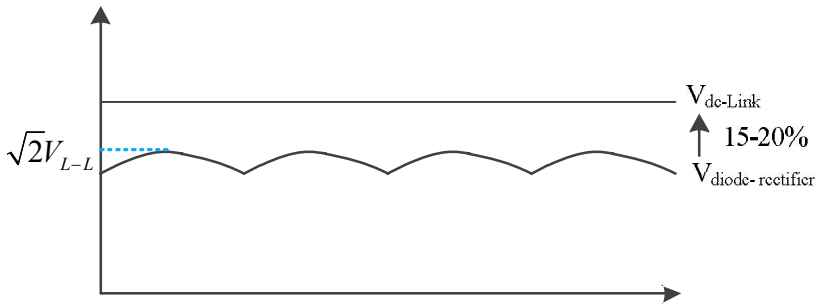


Fig. 3.5 DC link voltage condition

It is better to select a DC-link voltage about 15-20% more than $\sqrt{2}V_{L-L}$. No line impedance $(R_f = 0, L_f = 0)$ is taking into account here. The DC-link voltage depends on the PWM method. In case of a sinusoidal PWM, the maximum reference voltage is $\frac{V_{dc}}{2}$ (as shown in Fig. 3.6).

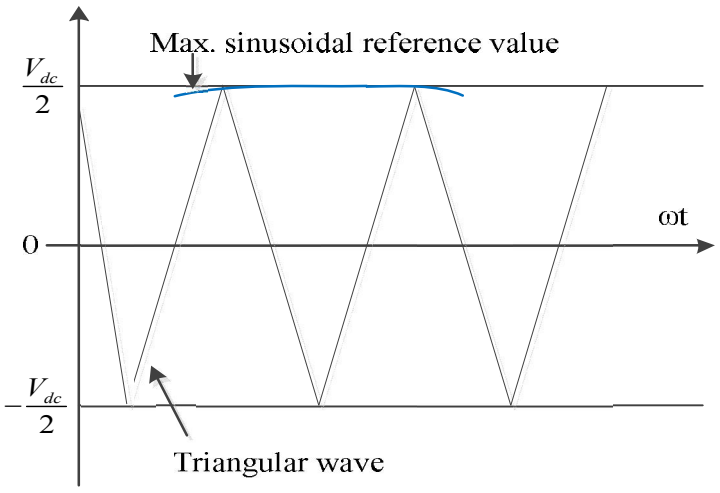


Fig 3.6 Maximum sinusoidal reference voltage (converter voltage V_s) for sinusoidal PWM

Finally, the minimum DC-link voltage is as,

$$V_{L-N(peak)} = \frac{V_{dc}}{2}$$

$$\frac{V_{L-L(rms)}}{\sqrt{3}}\sqrt{2} = \frac{V_{dc}}{2}$$

$$V_{dc(min)} > 2V_{L-N(peak)} = \frac{2\sqrt{2}}{\sqrt{3}}V_{L-L(rms)} = V_{dc} \tag{3.16}$$

The specification of DC bus voltage of the VSC based DSTATCOM should be greater than twice of the peak of the phase voltage of the distribution system. The DC bus voltage is calculated as per [8],

$$V_{dc} = 2\sqrt{2}V_{L-L}/(\sqrt{3}\,m) = 2\sqrt{2} \times 415/(\sqrt{3}\ \times 1) = 677.69\ \text{V}.$$

where V_{L-L} is the AC line voltage of the shunt compensator and m is the modulation index. The modulation index, m is selected 1 and AC line voltage of DSTATCOM is 415V, then V_{dc} is obtained as 677.69V. Thus, the DC bus voltage is selected as 700V.

3.4.3 Design of DC Bus Capacitor

The design of the DC capacitor is governed by the net variation in the DC bus voltage i.e. reduction during application of the load and rise in the DC bus voltage during removal of the load. Using the principle of energy conservation, the equation governing C_{dc} is written as,

$$\frac{1}{2}C_{dc}[V_{dc}^2 - V_{dc1}^2] = 3k_1aVIt \tag{3.17}$$

where V_{dc} is the reference DC voltage and V_{dc1} is the minimum voltage level of the DC bus, a is the over loading factor, V is the phase voltage, I is the phase current of the VSC and t is time for which the DC bus voltage is to be recovered. Considering the reference DC bus voltage $V_{dc} = 700$ V, and minimum voltage level of DC bus as

$V_{dc1} = 677.69$ V, $V = 239.60\,V$, $I = 20\,A$, $t = 30\,ms$, $a = 1.2$, and variation of energy during dynamics =10 % ($k_1 = 0.1$), the calculated value of C_{dc} is 3367 µF and is selected as 3500 µF.

3.4.4 Design of AC Interfacing Inductors

The selection of the AC inductance (L_f) of a VSC depends on the current ripple, i_{cr-pp}, switching frequency f_s , and DC bus voltage (V_{dc}), and it is given as,

$$L_f = \sqrt{3}mV_{dc}/\left(12af_s i_{cr-pp}\right), \tag{3.18}$$

Where m is the modulation index, V_{dc} DC bus voltage and a is the overloading factor. $i_{cr-pp} = 15$ %. The switching frequency, f_s depends upon the speed of the DSP processor and the highest order harmonic to be compensated by the DSTATCOM. Here, the sampling frequency is selected as $f_s = 10$kHz, $m = 1$, $V_{dc} = 700$ V, and $a = 1.2$, the value of L_f is calculated as 2.8 mH. The round-off value of 3 mH is selected.

3.4.5 Design of Passive High Pass Ripple Filters

A passive high pass first order filter tuned at half the switching frequency is used to filter the high frequency noise from the voltage at PCC. The time constant of the filter should be very small compared with the fundamental time period (T), $R_r C_r \leq T_f$. Considering small time constant of the filter $R_r C_r = T_s/10$, where R_r, C_r, and T_s are the ripple filter resistance, ripple filter capacitance and switching time, respectively. For a switching frequency of 10 kHz, the value of ripple filter parameters are calculated as $R_r = 5\,\Omega$ and $C_r = 10$µF. The impedance offered for switching frequency, is 5.25 Ω and impedance offered to fundamental frequency current is

318.37Ω, which is sufficiently large and hence, ripple filter draws negligible fundamental frequency current.

3.4.6 Selection of Voltage and Current Ratings of IGBTs

The voltage rating (V_{sw}) of the IGBTs of DSTATCOM under dynamic load conditions is given as,

$$V_{sw} = V_{dc} + \Delta V_{dc} \tag{3.19}$$

where ΔV_{dc} is the 10% overshoot in the DC bus voltage under dynamic conditions of load. The DC bus voltage is selected as 700V, a reference value, then $\Delta V_{dc} = 0.1 \times 700 = 70\,V$. The voltage rating of the IGBT is calculated as 770V. Considering appropriate safety factor of IGBTs in VSC, these are selected for 1200V voltage rating used in the DSTATCOM.

The current rating I_{sw} of the IGBTs of VSC under dynamic load condition is given as,

$$I_{sw} = 1.25\left(I_{cr-pp} + I_{peak}\right) = 1.25(3 + 20) = 28.75\,A \tag{3.20}$$

where I_{cr-pp} and I_{peak} are the allowed ripple currents considering 15% and the peak values of compensator current (30A for SKD 35 of SEMIKRON make diode bridge rectifier module). The current rating of the IGBT, is calculated as 28.75 A. The IGBT module SKM150GB12V of SEMIKRON make, is used for the development of VSC.

3.5 DEVELOPMENT OF PROTOTYPE OF DSTATCOM

The three phase prototype of DSTATCOM includes various components for its development in the laboratory. This includes three dual pack IGBT modules for VSC with a DC voltage storage capacitor, voltage and current sensing with signal conditioning circuits, interfacing inductors, capacitor and rheostat as ripple filter,

series RL load as linear and diode rectifier module as nonlinear loads. The developed prototype of DSTATCOM uses VSC, voltage sensors, current sensors, gate driver circuit for IGBTs, interfacing inductors and ripple filters which are given in details as follows:

3.5.1 Development of Voltage Source Converter (VSC)

The developed prototype of DSTATCOM is implemented in the laboratory. The performance of the developed hardware prototype is implemented at low rating of voltage 110V, 50Hz due to constraints available on equipments rating in the laboratory. The layout of the developed hardware setup for three-phase DSTATCOM is shown in Fig. 3.7. The input of auto-transformer is the three phase AC mains of 415V, 50Hz and the output voltage is set at 110V. It feeds linear and nonlinear loads. The DSTATCOM is designed using three phase VSC. This uses six IGBTs with anti-parallel diodes and high value capacitor at DC side. The IGBT module (Semikron make SKM150GB12V) is used in VSC [168]. The control operation of the VSC used as DSTATCOM, is performed with the help of DSP (dSPACE 1104 R&D controller board) embedded in personal computer (PC). The DSP (dSPACE 1104) is real time controller based on a Power PC 603 floating-point processor [166]. This includes slave DSP subsystem based on the TMS320F240. The PCC voltages (v_{sa}, v_{sb}), supply currents (i_{sa}, i_{sb}), load currents (i_{La}, i_{Lb}, i_{Lc}) and DC bus voltage (V_{dc}) are sensed by Hall Effect voltage and current sensors. Appropriate buffer circuitry is designed for voltage and current sensors using operational amplifier (OP07). A buffer isolates or separates one circuit from another.

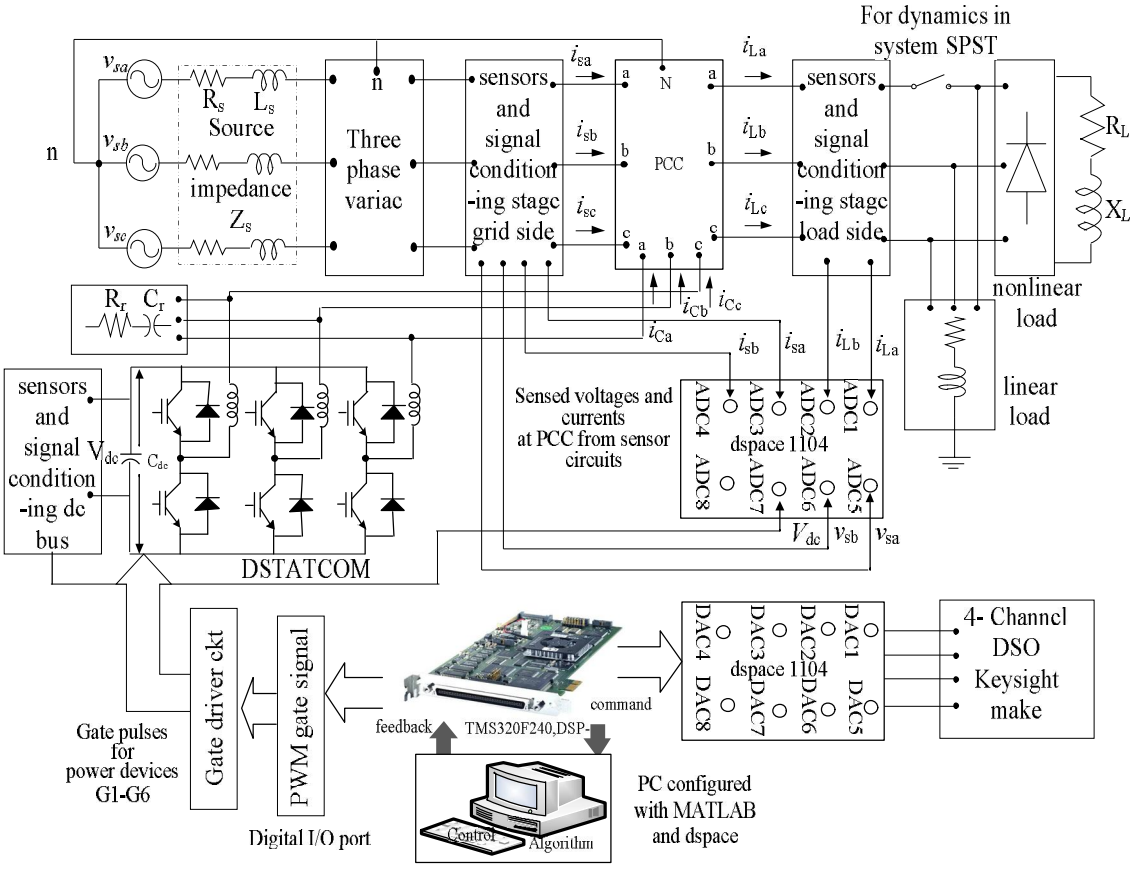


Fig. 3.7 Functional block diagram of developed hardware prototype DSTATCOM

The snapshot of developed experimental test setup of three phase distribution system with DSTATCOM in the laboratory is shown in Fig. 3.8. The parameters for developed prototype DSTATCOM system, are given in Appendix-A. The control algorithm for generation of reference supply currents, is developed in MATLAB environment using SIMULINK and SPS tool boxes.

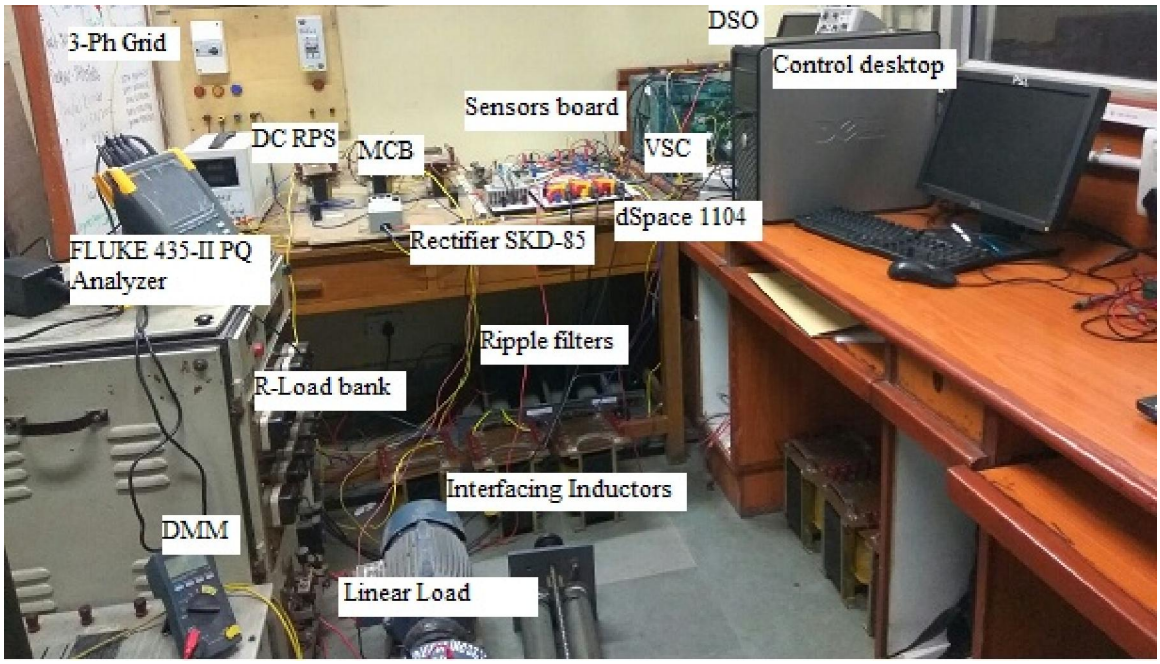


Fig. 3.8 Experimental prototype developed of DSTATCOM in the laboratory

This algorithm is implemented using DSP dSPACE as shown in Fig. 3.9. The DSP based implementation is mainly divided into three blocks, ADC block, scaling of signals along with control algorithm block and PWM current controller block. The output of voltage and current sensors are given as inputs to the ADC channels of DSP (dSPACE 1104R&D controller board). The DSP dSPACE 1104 contains two different types of ADCs for the analog input channels. The first type contains one 16-bit ADC with four multiplexed (ADC1-ADC4) input signals. The second type contains four 12-bit parallel ADCs with one input signal each (ADC5-ADC8). The signals from ADC channels are scaled up to get the actual values of PCC voltages, supply currents, load currents and DC bus voltage. These signals are given as inputs to the control algorithm for generation of reference supply currents. The switching pulses for VSC, are taken from PWM port of DSP-dSPACE through the gate driver circuit. The AC side of the VSC, is connected to the PCC with the help of interfacing

inductors. An implementation of DC and AC bus PI voltage controllers are shown in Figs. 3.10 and 3.11. An implementation of pulse width modulation (PWM) switching in DSP-dSPACE using DS 1104SL_DSP_I/O port is shown in Fig. 3.12.

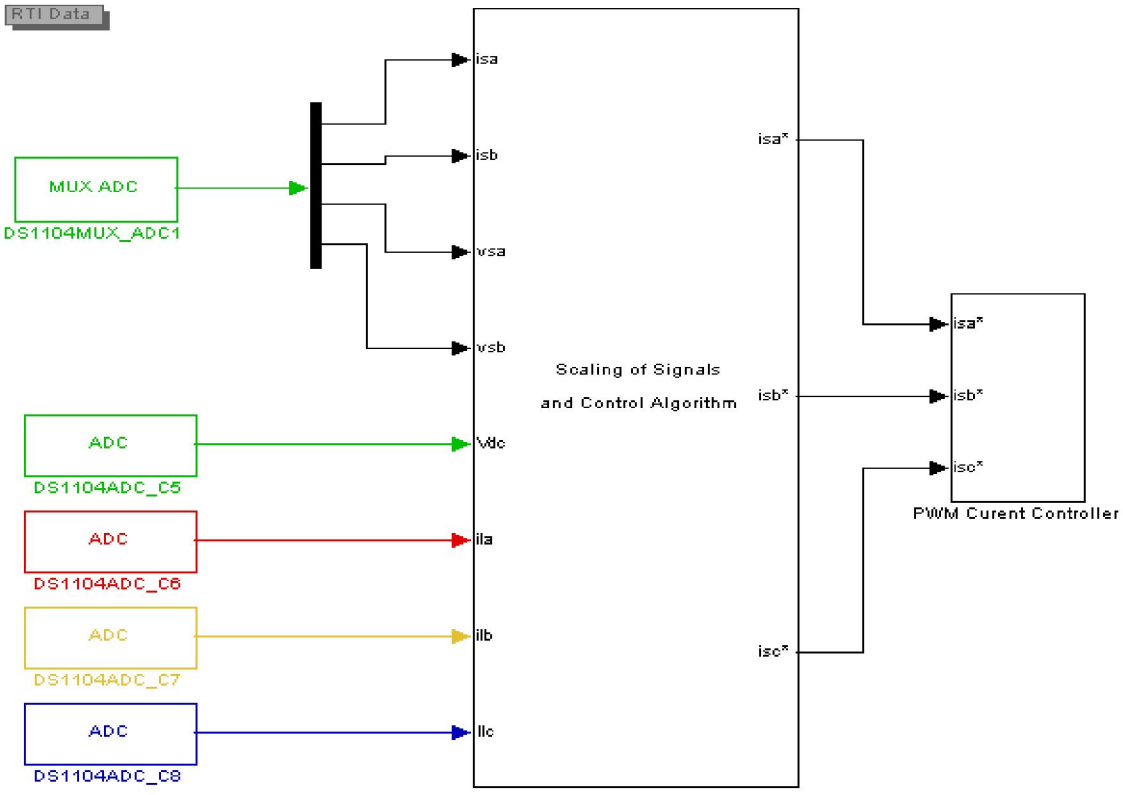


Fig. 3.9 MATLAB based real time interface (RTI) control of DSTATCOM on DSP implementation

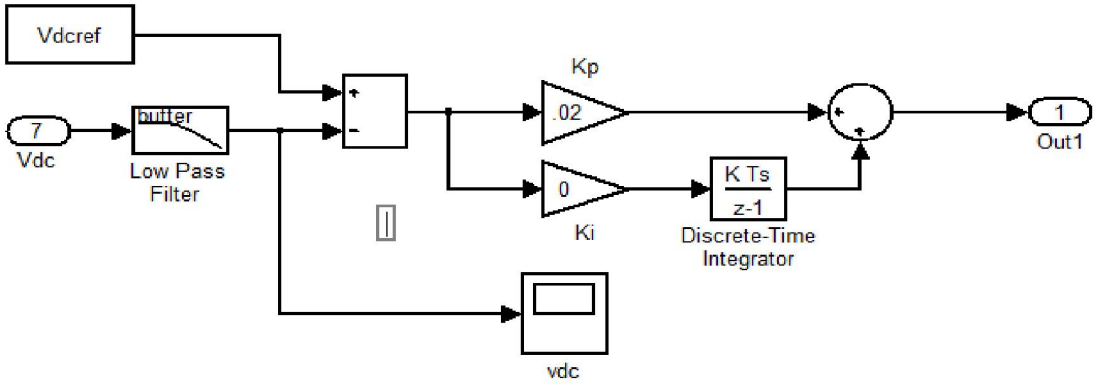


Fig. 3.10 Implementation of DC bus PI controller

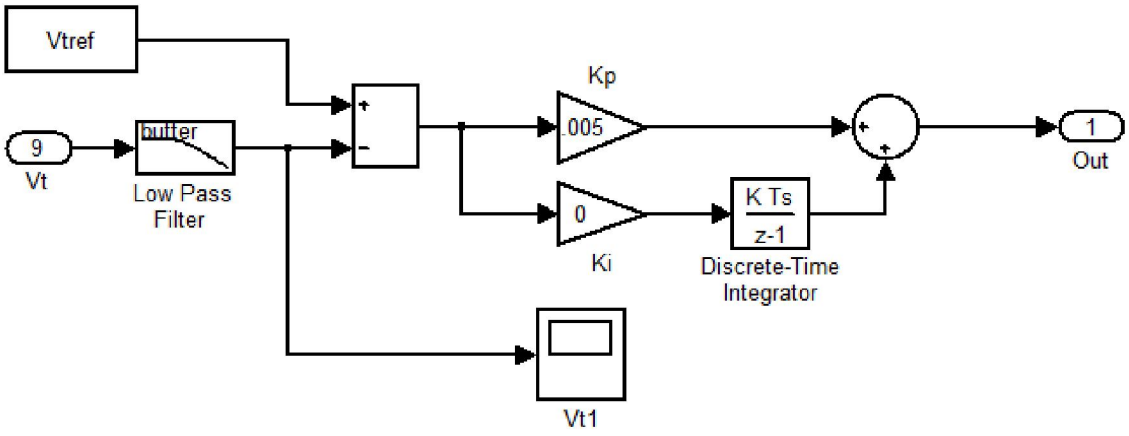


Fig. 3.11 Implementation of AC bus PI controller

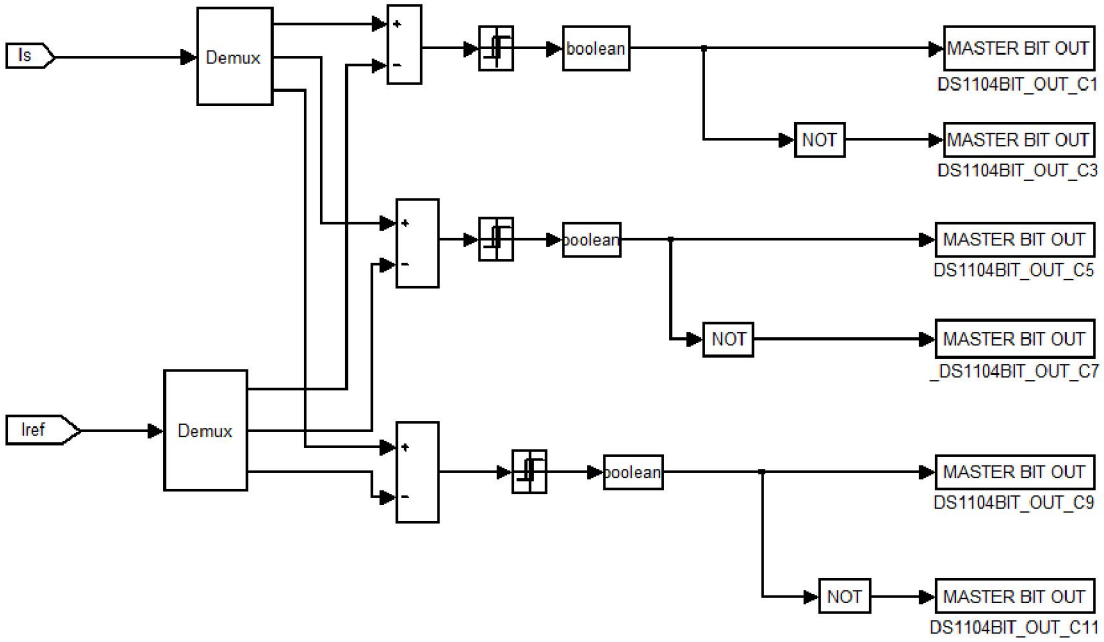


Fig. 3.12 Implementation of Hysteresis PWM current controller

Fig. 3.13 shows the snap shoot of VSC model of **MD B6U 415/560-45F + MD B6C 1800/415-35F** (Semikron make) used to develop prototype of DSTATCOM in the laboratory. It consists of insulated gate bipolar transistors (IGBTs) with anti-parallel diodes. The ratings of the DC bus capacitor and DC bus voltage of capacitor are 1650μF and 800V, respectively. The control of VSC is performed with the help of

control algorithm implemented on DSP-dSPACE. Switching pulses are generated from PWM port of DSP- dSPACE and fed to gate driver circuit, which gives 15V output pulses for operation of IGBTs of VSC.

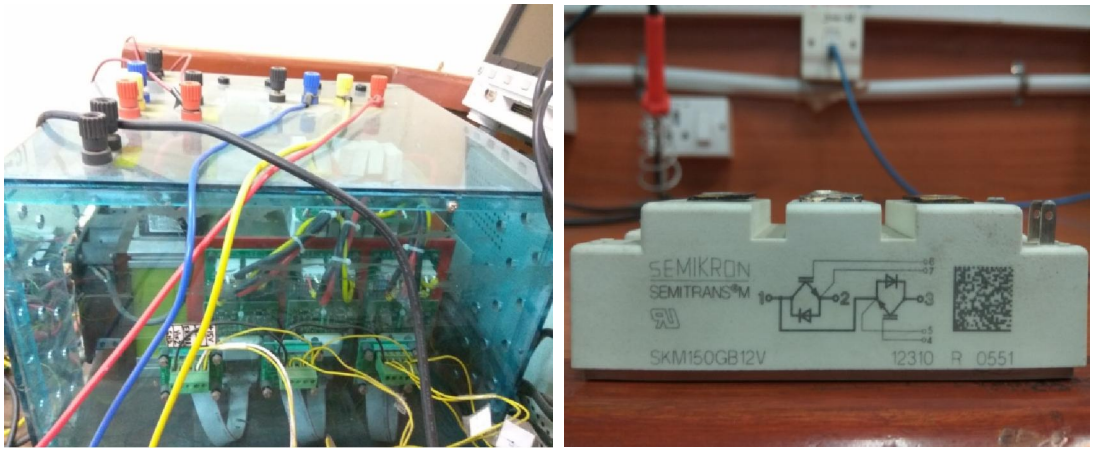
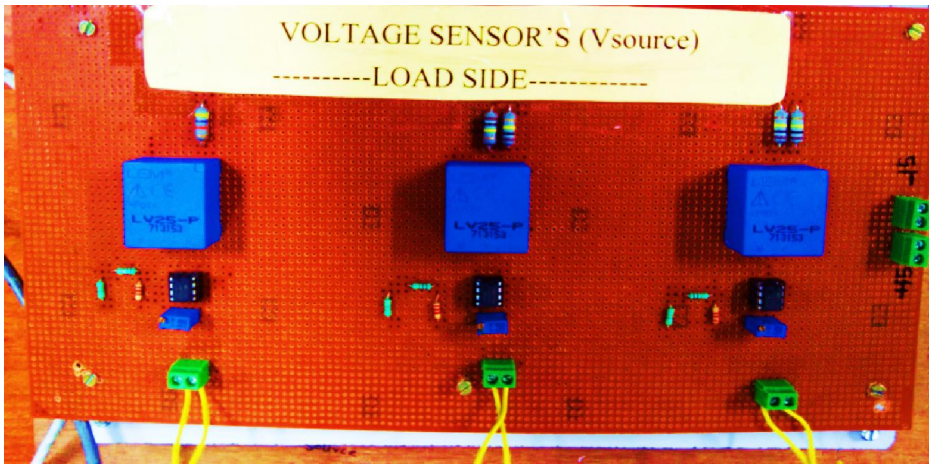


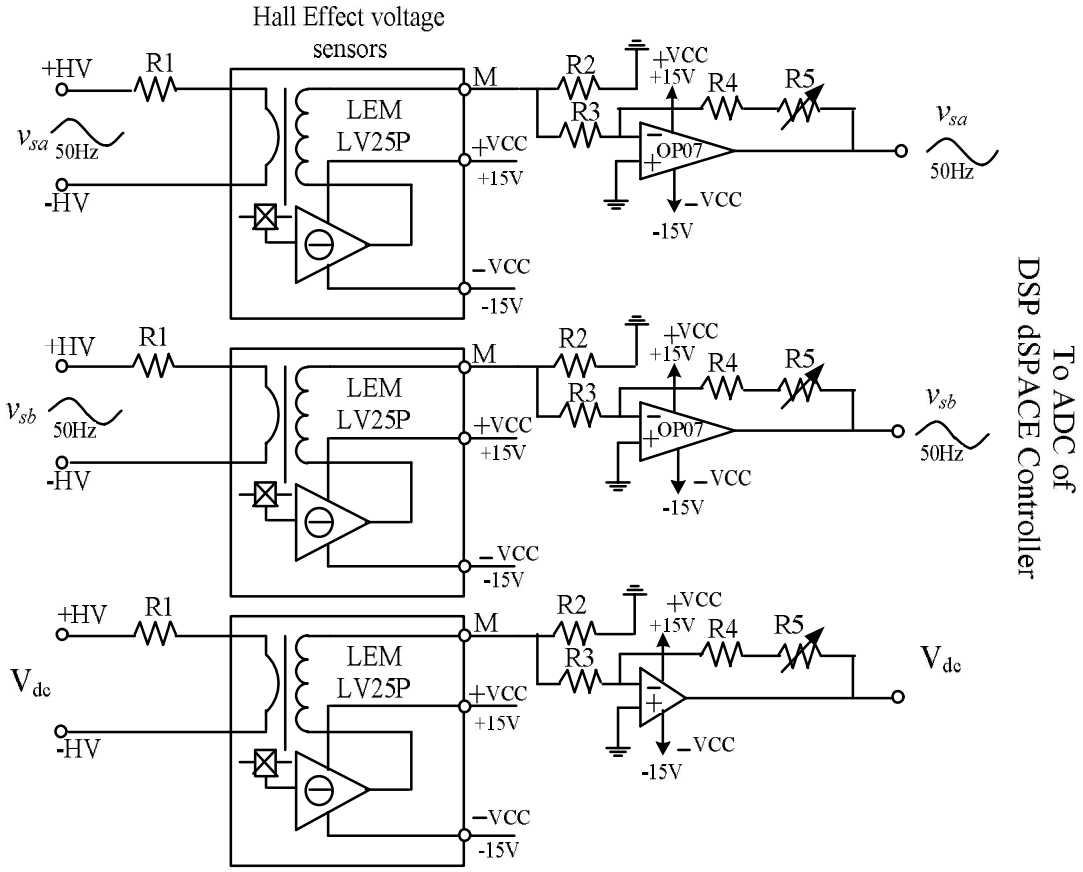
Fig. 3.13 IGBTs (SEMIKRON MAKE) based VSC

3.5.2 Development of Voltage Sensors Circuit

Figs. 3.14(a) and (b) show the snapshot of developed model and schematic diagram of voltage sensors circuit. The voltage sensors are used to sense voltages at PCC and DC link voltage of DSTATCOM. For the three phase balanced AC mains voltages, two voltage sensors (LEM LV25-P) are used to sense AC mains voltages and one voltage sensor (LEM LV25-P) is used to sense the DC link voltage of VSC based DSTATCOM [169]. These voltage sensors operate at ±15V DC supply as shown in Fig. 3.14(b). The sensed voltage signal from the voltage sensor is fed to the buffer circuitry. The buffer circuitry is designed using operational amplifier (OP07) with appropriate resistances values. A buffer is a unity-gain amplifier that has an extremely high input resistance and an extremely low output resistance. This means that the buffer can be modeled as a voltage controlled voltage source that has a gain of one.



(a)

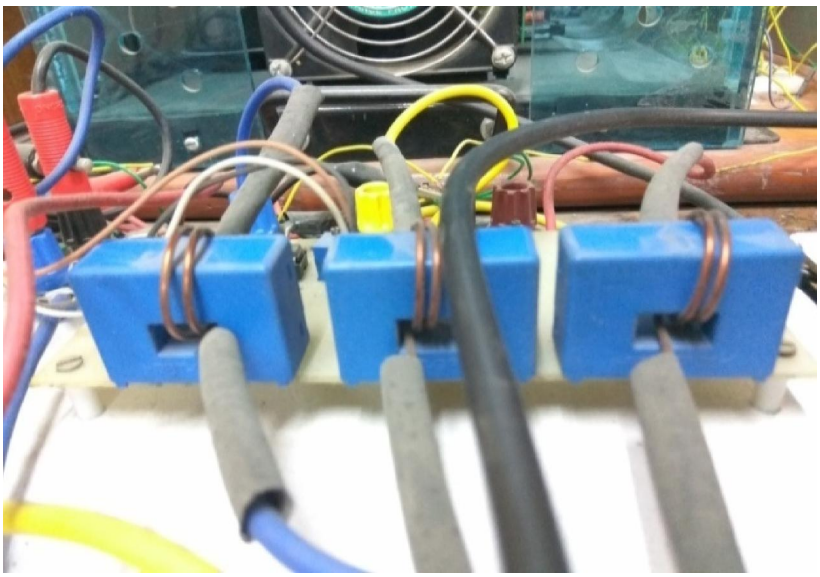


(b)

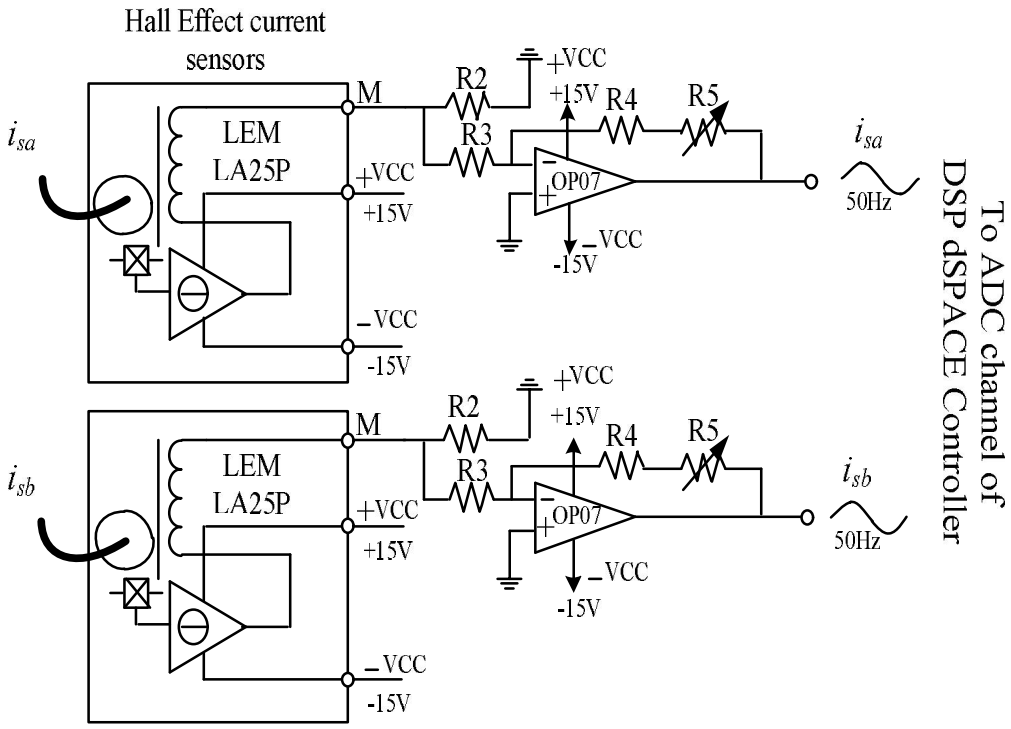
Fig. 3.14 (a) Developed prototype test model (b) Schematic diagram of voltage sensors with power signal conditioner

3.5.3 Development of Current Sensors Circuit

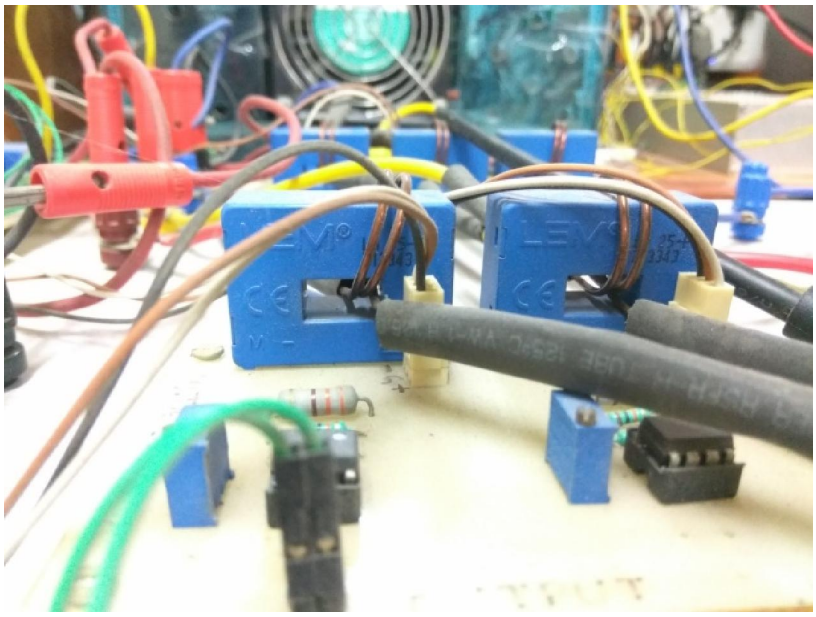
Figs. 3.15 (a) and (b) show the snapshot and schematic diagram of Hall Effect current sensors circuit for sensing the supply currents at PCC. For level translation, buffers are used that let the output side be powered from a different voltage than the input side for translating voltage levels for DSP dSPACE controller. For balanced three phase AC mains, two Hall Effect current sensors (LEM LA-25) are used for sensing supply side currents as shown in Fig. 3.15(b) of phase 'a' and 'b', respectively. Similarly, two current sensors (LEM LA-25) are utilized for sensing the load side currents as shown in Fig. 3.15(c) and its schematic diagram is shown in Fig. 3.15(d). These current sensors operate at ±15V DC supply as shown in Fig. 3.15 (b) and Fig. 3.15 (d), respectively [170]. The outputs of the sensors are fed to the ADC channels of DSP-dSPACE through appropriate buffer circuitry.



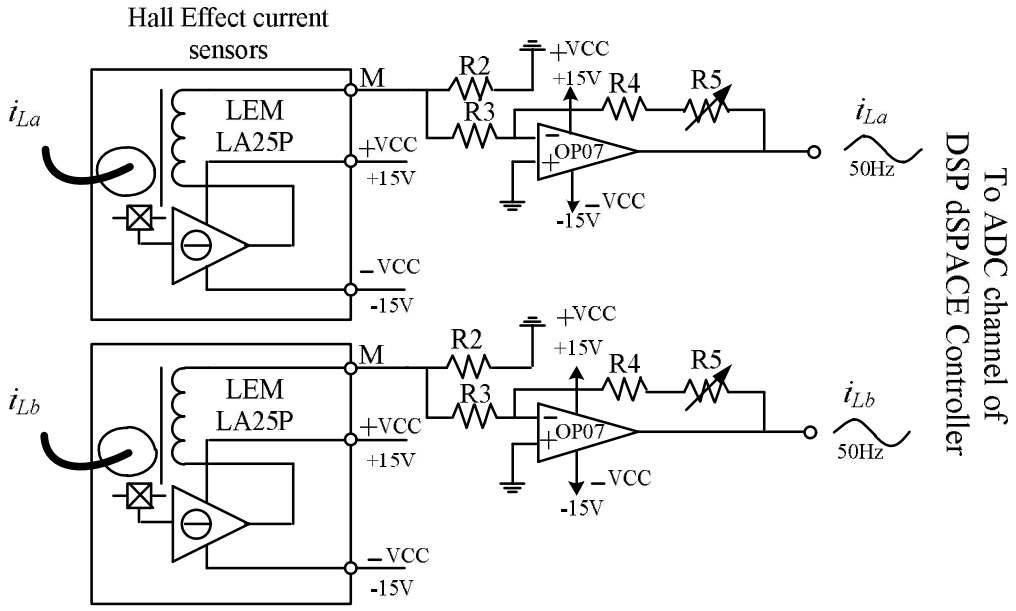
(a)


Hall Effect current sensors
i_{sa}
LEM LA25P
M
+VCC
+15V
-VCC
-15V
R2
R3
R4
R5
OP07
50Hz
i_{sb}
To ADC channel of DSP dSPACE Controller

(b)



(c)



(d)

Fig. 3.15 (a) Snapshot of sensed grid currents (b) schematic diagram of grid current sensors and signal conditioner circuit (c) snapshot of sensed load currents (d) schematic diagram of load currents with buffer circuit

Fig. 3.16 shows RTI interface of the sensed parameters of the developed prototype DSTATCOM using dSPACE-1104.

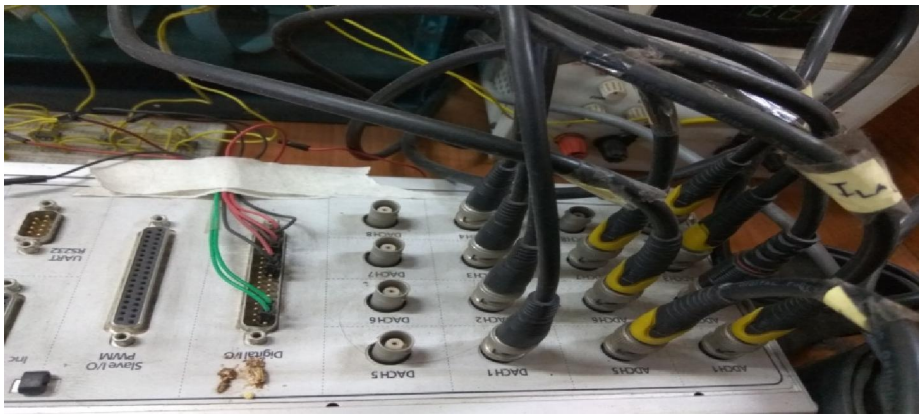


Fig. 3.16 RTI interface of the sensed parameters using dSAPCE-1104

3.5.4 Development of AC Interfacing Inductors

The design and selection of interfacing circuit are given in section 3.4.4 and the photograph of interfacing inductors is shown in Fig. 3.17. The value of interfacing

inductors depends upon value of DC bus voltage of VSC, switching frequency and allowed percentage ripple current. The rating of interfacing inductor designed here, is 3 mH inductance and the gauge of wire used to withstand flow of maximum 10A current. The equation for calculating the number of turns (N) [167], of the inductor is given as,

$$N = \frac{LI_m}{A_c B_m} = \frac{3 \times 0.001 \times 10 \times \sqrt{2}}{8.658 \times 10^{-4} \times 1} = 49 \tag{3.21}$$

where L is inductance in Henry, I_m is peak value of rated inductor current in Ampere, A_c is core cross sectional area m^2 and B_m is the flux density in Tesla, selected as 1T for CRGO core. The value of N calculated from eqn. (3.21) is 49 and it is selected as 50. The gauge of wire is given as,

$$a = \frac{I}{j} = \frac{10}{3} = 3.33\ mm^2 \tag{3.22}$$

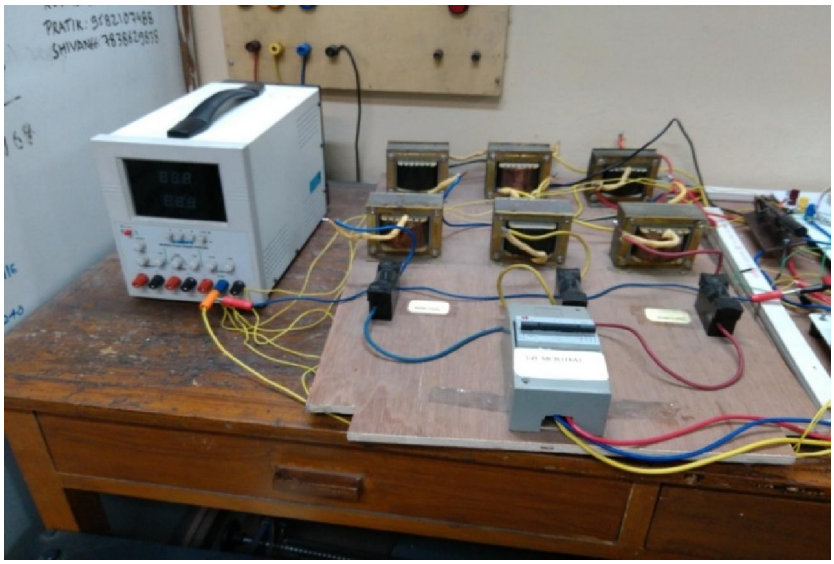
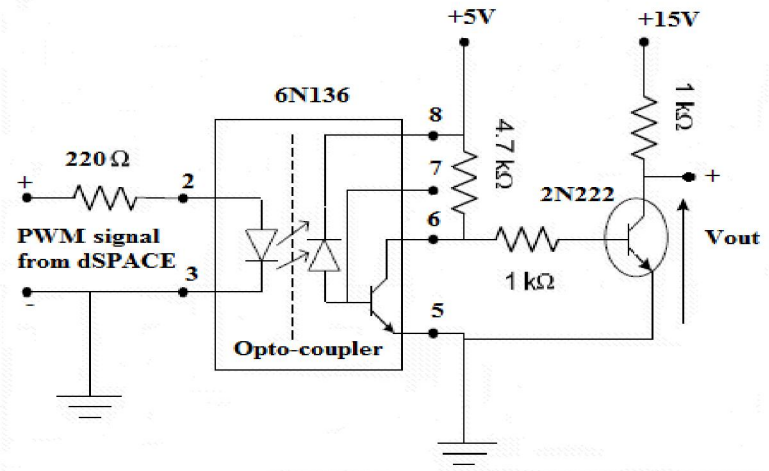


Fig. 3.17 Developed interfacing inductors

3.5.5 Development of Gate Driver Circuit

Figs. 3.18 (a) and (b) show the snapshot of developed gate driver circuit and schematic diagram of gating circuit. The magnitude of output pulses from PWM port of DSP-dSPACE is 0-5V, but the IGBTs of VSC operates at 0-15V gating pulses. Therefore, the gating circuit is required, which amplify output gating pulses from PWM port of DSP to 15V. This circuit is designed using op-amp level shifter circuit, n-p-n transistor (2N2222) and appropriate resistances. Six similar circuits are designed to provide 15V gating pulses to operate the six IGBTs of VSC.

(a)



(b)

Fig. 3.18 (a) Snapshot of developed gate driver (b) Schematic diagram of gating circuit

3.5.6 Development of Passive High Pass Ripple Filters

The design of series R-C ripple filter is shown in Fig 3.19. The values of R and C are selected here as 5Ω and 10μF, respectively. The design of these filters is the same as presented in section 3.4.5. These filters are connected at the PCC in parallel with the load and offer high impedance (318.78 Ω) to the fundamental frequency current. Therefore, negligible fundamental current is drawn by the ripple filter. However, its impedance at switching frequency of 10 kHz is 5.25 Ω. This is quite suitable to suck all switching ripples. The loss in this ripple filter is 2.25W only, which is negligible.

Fig. 3.19 Development of resistive capacitive (R-C) ripple filters

3.6 RESULTS AND DISCUSSION

The detailed discussion on designed and selected values of the components of DSTATCOM for simulation purpose and developed components for hardware prototype is presented here. Test results of developed DSTATCOM components such as voltage sensors, current sensors, gating circuit and interfacing inductors are also presented.

3.6.1 Test Results of Prototype of DSTATCOM

The design and simulation are carried out at full rating of AC mains 415V, 50Hz according to Indian power distribution system. The design and selection of various

components of DSTSTCOM such as VSC, DC bus capacitance, DC bus voltage, interfacing inductors and ripple filters are same as given in section 3.4. The VSC is selected of 415V, 50Hz and 25kVA rating. The selected IGBT module for VSC is SKM150GB12V (Semikron MAKE), having voltage and current rating as 1200V and 231A. The DC bus voltage and DC bus capacitance are selected as 700V and 1650μF. The value of interfacing inductor is selected around 3mH. The R-C value of ripple filter is selected around 5Ω and 10μF. The designed values of these components are given in Table-3.1.

The experimental prototype of the DSTATCOM is developed in the laboratory at the lower rating of 110V, 50Hz due to available equipment rating constraints in the laboratory. The design and selection of various components of DSTATCOM such as VSC, DC bus capacitance, DC bus voltage, interfacing inductors and ripple series R-C filters, are same as given for simulation purpose. The development of VSC, voltage sensors, current sensors, gating circuit, interfacing inductors and ripple filters is same as discussed in section 3.5.

TABLE-3.1 System parameters of DSTATCOM for simulation

Supply voltage (v_s)	3-ϕ, 50 Hz, 415 V
Source impedance (Z_s)	(0.314+0.04)**Ω**
VSC rating	3-ϕ, 25kVA
DC bus capacitance	3500μF
DC bus voltage	700 V
Interfacing inductors	2.5~3 mH
Ripple $R_f - C_f$ series filter	5Ω, 10μF
Load parameters	3-ϕ, Diode bridge configuration with R=12Ω, L=150mH
Switching frequency	10 kHz

The selected IGBT module for VSC is SKM150GB12V. The value of DC bus capacitance, DC bus voltage, interfacing inductors and ripple $R_f - C_f$ filters are selected 5000μF, 200V, 3mH and 5Ω, 10μF, respectively, for developed prototype of DSTATCOM. The rating of components selected for developed prototype is summarized in Table-3.2.

TABLE-3.2 System parameters of developed DSTATCOM

Supply voltage (v_s)	3-ϕ, 50 Hz, 415 V
Source impedance (Z_s)	(0.88+0.12)**Ω**
VSC rating	3-ϕ, 25kVA
DC bus capacitance	5000μF
DC bus voltage	700 V
Interfacing inductors	3~3.5mH
Ripple $R_f - C_f$ series filter	5Ω, 10μF
Load parameters (nonlinear)	3-ϕ, Diode bridge configuration with R=12Ω, L=150mH
Switching frequency	10 kHz

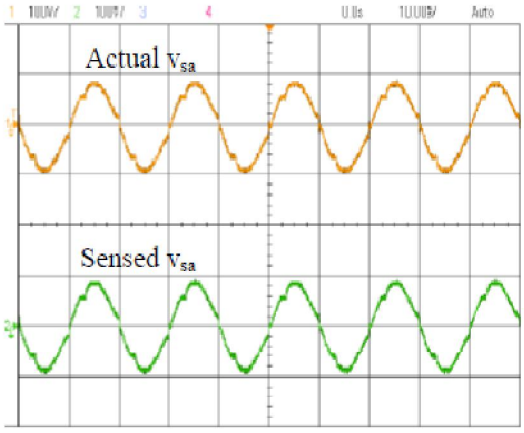
Test results of developed system components such as voltage sensors, current sensors, gating circuit and interfacing inductors are presented here. The interfacing of voltage and current sensors signals with DSP-dSPACE is through ADC channels and selection of gain values for sensors output are also presented.

3.6.1.1 Test results of voltage sensors

Fig. 3.20 shows the test results of AC bus voltage sensors at PCC. Due to limited ADC channel availability of DSP-dSPACE 1104, only two phase voltages are sensed at PCC, which are required for balanced three phase system. With the help of balanced system, the third phase voltage is calculated from sensed voltages of two

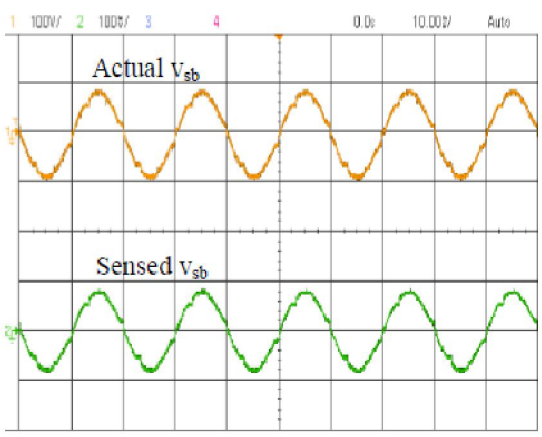
phases. Figs. 3.20 (a) and (b), present actual and sensed voltages of phase ‘a’ and ‘b’ corresponding at PCC, respectively. The actual magnitude of PCC voltages are obtained from high voltage differential voltage probe (Tektronix P5200A). The actual PCC voltage magnitude is 179.8V (P-P), whereas the sensors sensed PCC voltage magnitude is 185mV (P-P). Therefore, the value of gain is selected around 971.89, for output signals of PCC voltage sensors to achieve actual magnitudes. Fig. 3.20(c) shows waveforms of sensed phase ‘a’, sensed phase ‘b’ and calculated phase ‘c’ of PCC voltages.

Fig. 3.20 (d) shows waveforms of actual and sensed DC bus voltage of VSC used as DSTATCOM. Initially, the DC bus voltage magnitude is at peak amplitude of line voltage around 155.5V and the output of DC bus voltage sensor is 279 mV. Therefore, the gain value selected for DC bus voltage sensor is around 557.3, used to obtain actual value of DC bus voltage.



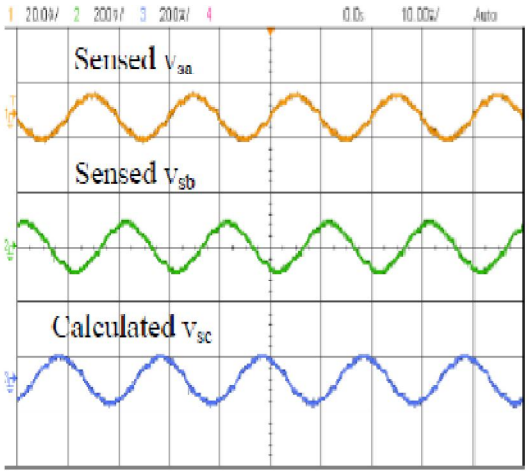
Ch.1-2-100V/div-100mV/div,Time axis-10ms/div

(a)



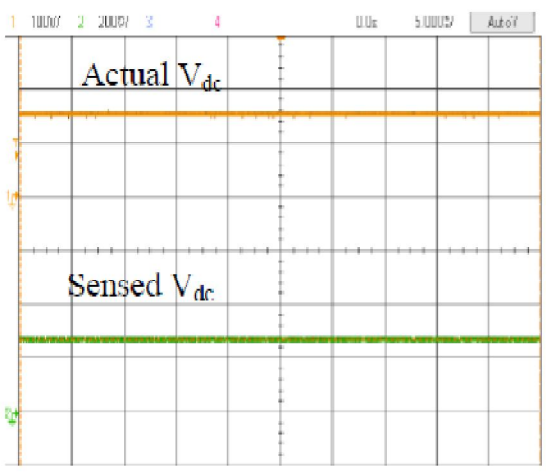
Ch. 1-2- 100V/div-100mV/div, Time axis- 10ms/div

(b)



Ch. 1, 2 and 3- 200mV/div, Time axis-10ms/div

(c)



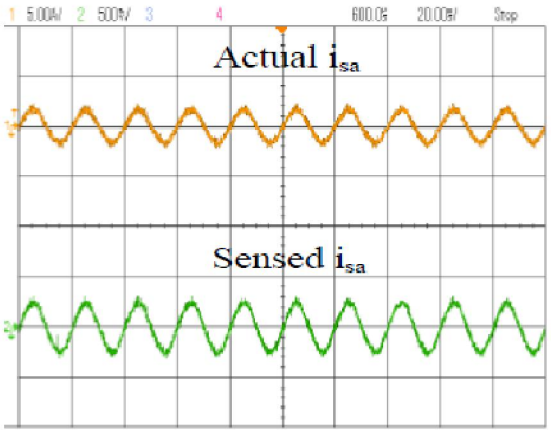
Ch. 1-2- 100V/div-200mV/div, Time axis-5ms/div

(d)

Figs. 3.20 (a) - (b) Actual and sensed voltages at PCC corresponding to phase 'a' and 'b' (c) Balanced three phase voltages (d) Actual and sensed DC bus voltage

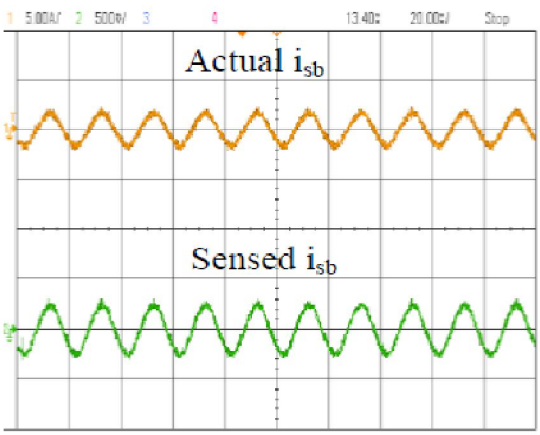
3.6.1.2 Test results of source current sensors

Fig. 3.21 shows test results of supply current sensors. For three wire three phase system, only two phases (phase 'a' and 'b') of three are required to be sensed. Third phase (phase 'c') is calculated from the currents of the other two phases. Fig. 3.21(a) and (b) depict waveforms of actual current and sensed current corresponding to phase 'a' and phase 'b', respectively. The actual waveforms of currents are obtained from current probes (Agilent 1146A). It is observed from these results that the actual magnitude of phase 'a' of supply current is 5A (P-P), whereas magnitude of sensed current is 165 mA (P-P). Therefore, the selected gain value for supply current is around 30.3, which is used to obtain actual magnitude. Fig. 3.21(c) depicts waveforms of sensed phase 'a', sensed phase 'b' and calculated phase 'c' for balanced three phase system.



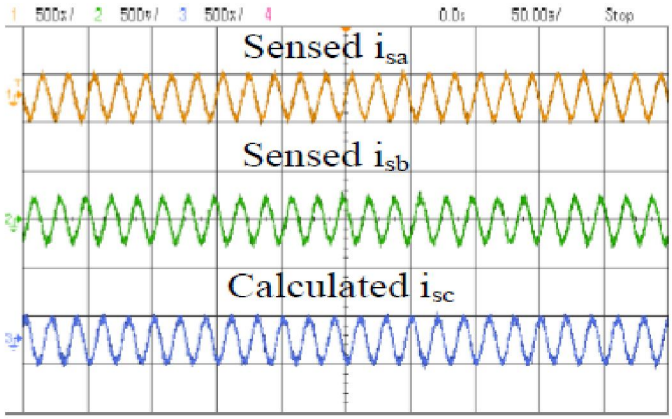
Ch. 1-2- 5A/div-500mA/div, Time axis-20ms/div

(a)



Ch. 1-2- 5A/div-500mA/div, Time axis 20ms/div.

(b)



Ch. 1, 2 and 3 -500mA/div, Time axis-50ms/div

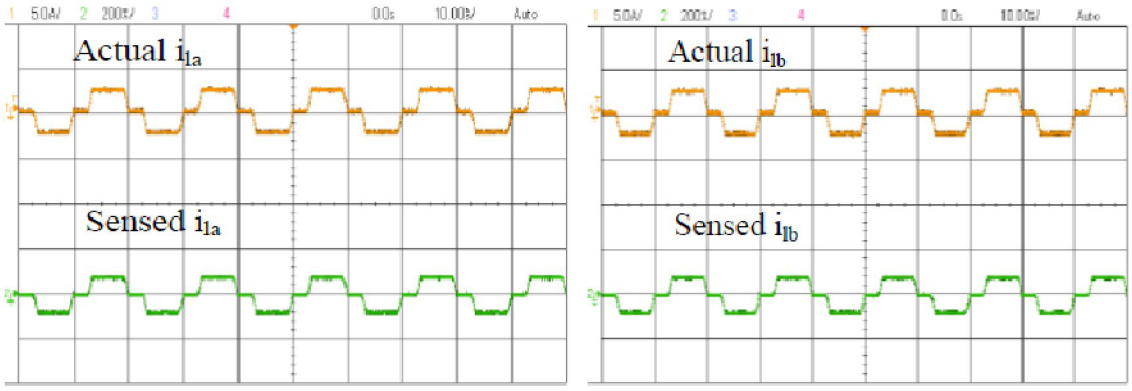
(c)

Figs. 3.21 (a)-(b) Actual and sensed supply currents i_{sa}, i_{sb} (c) Calculated supply current i_{sc}

3.6.1.3 Test results of load current sensors

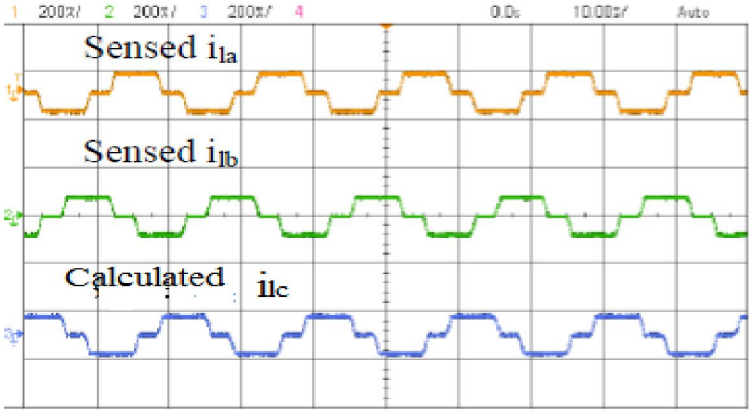
Fig. 3.22 shows the test results of load current sensors. Two current sensors are required for sensing two phases of load currents. Figs. 3.22 (a), (b) show waveforms of actual load currents and sensed load currents corresponding to phase 'a' and phase 'b', respectively. Fig. 3.22 (c) shows the calculated phase 'c' load current using sensed load currents of phase 'a' and 'b', respectively. The load currents are observed by using current probe (Agilent 1146A). The gain value selected for load current

sensor is 30.3, same as selected for supply currents sensors. Fig. 3.22(d) shows waveforms of sensed load currents of all three phases.



Ch. 1-2- 5A/div-200mA/div, Time axis-10ms/div Ch. 1-2- 5A/div-200mA/div, Time axis-10ms/div

(a) (b)



Ch. 1-2- 5A/div-200mA/div, Time axis-10ms/div

(c)

Fig. 3.22 (a)-(b) Actual and sensed load currents of phase 'a' and 'b' (c) Calculated load current i_{Lc}

3.6.1.4 Test results of interfacing inductors

The VSC based DSTATCOM is connected through interfacing inductors to the AC grid side of PCC. The fixed value of inductor is designed for interfacing VSC to the PCC point. The design of interfacing inductors is same as given in section 3.4. Fig. 3.23 shows test results of designed interfacing inductor. This result shows variation of inductor value with the output current of the compensator. It is observed from this

result that variation in inductance is from 2.9 mH to 3.2 mH, while variation in current is from 1A to 9A. Small variation in inductance value is observed in the operating current range.

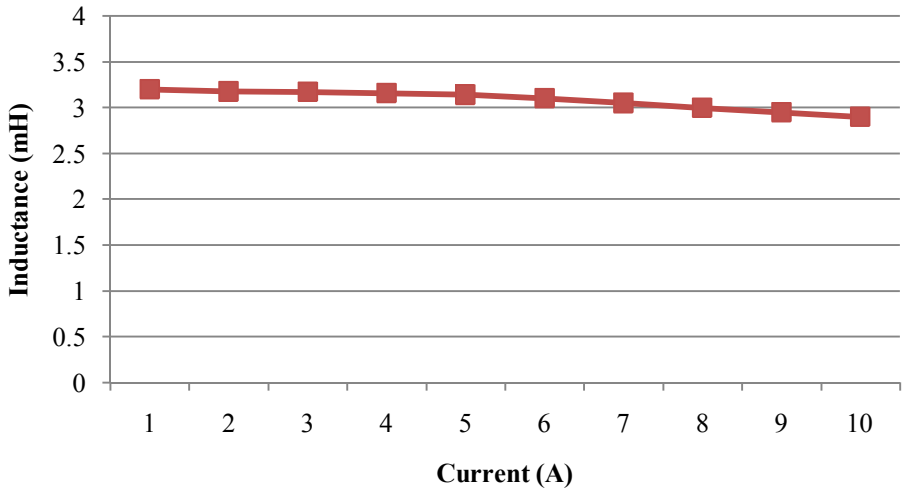
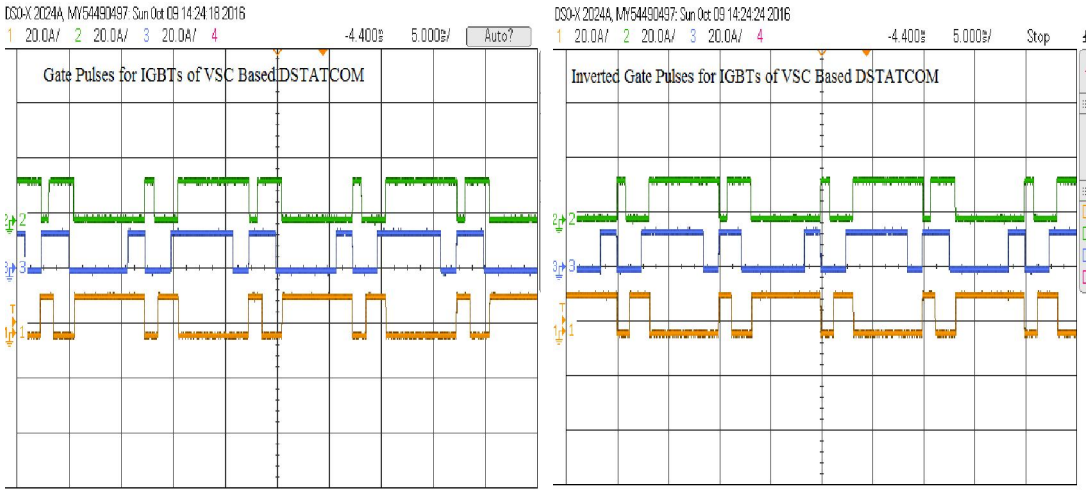


Fig. 3.23 Variation of inductance value with current

3.6.1.5 Test results of gate driver circuit

The gating circuit is developed to amplify gating pulses generated from digital I/O port of DSP-dSPACE. Fig. 3.24 shows the test results of gate pulses circuit. Figs. 3.24(a) and (b) show gate pulses and inverted gate pulses output from digital I/O port of DSP-dSPACE 1104. To drive the IGBTs of VSC, these pulses are amplified using level shifter circuit after that the gate pulses are applied to phase 'a', phase 'b' and phase 'c', respectively. The amplitude of the pulses is amplified to 15V through the gate driver circuit. These amplified gating pulses are sufficient to drive IGBTs of VSC based DSTATCOM.



(a) (b)

Fig. 3.24 (a) Gating pulses (b) Inverted gating pulses, for three phase VSC

3.6.2 Hardware Results with DSP

The outputs from voltage and current sensor circuits are send to DSP (dSPACE 1104 R&D controller board) through its ADC channels. After scaling, these signals can be observed with the help of DAC channels of DSP as shown in Fig. 3.25- Fig. 3.27:

3.6.2.1 Hardware results of voltage sensors

Fig. 3.25 shows waveforms of PCC voltages (v_{sa}, v_{sb} and v_{sc}) and DC bus voltage (V_{dc}) from DAC channels of DSP-dSPACE after scaling.

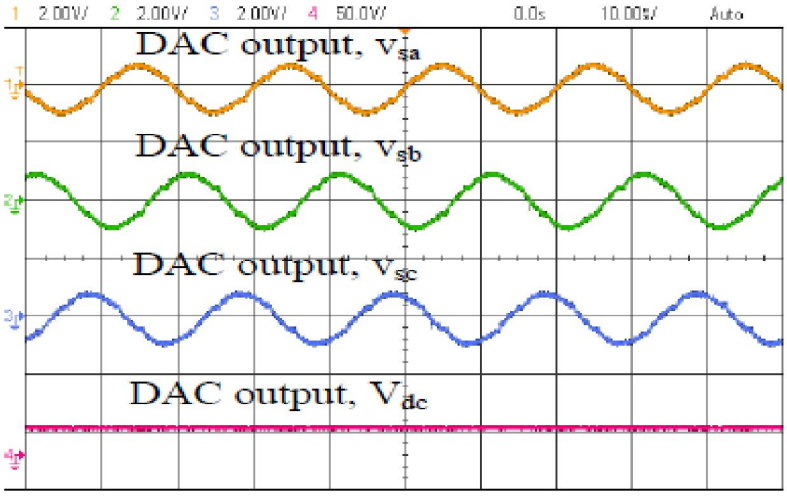
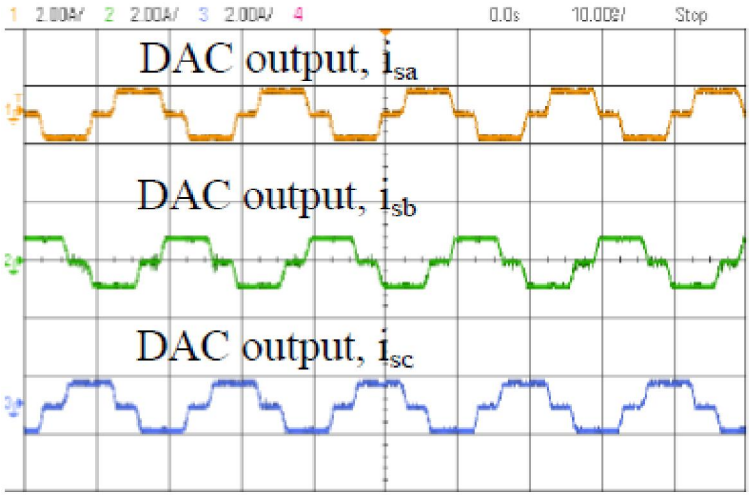


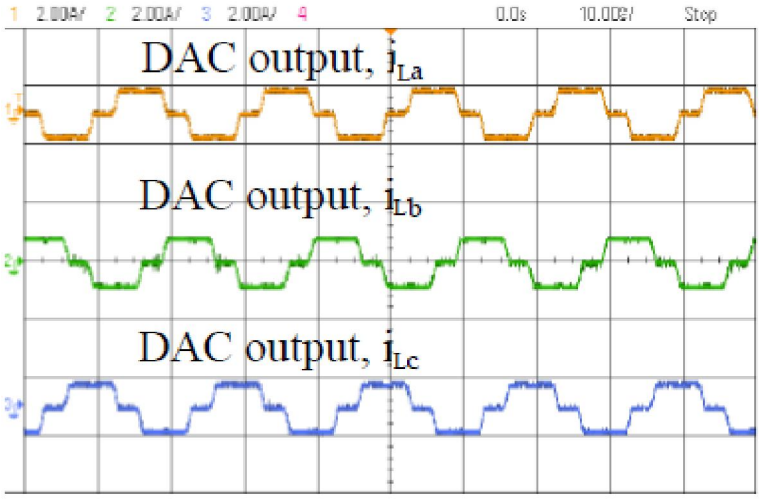
Fig. 3.25 Sensed PCC voltages (v_{sa}, v_{sb} and v_{sc}) and DC bus voltage (V_{dc})

3.6.2.2 Hardware results of current sensors

Figs. 3.26 (a) and (b) show waveforms of supply currents (i_{sa}, i_{sb} and i_{sc}) and load currents (i_{la}, i_{lb} and i_{lc}) from DAC channels of DSP-dSPACE. These signals are scaled up and given as input to the control algorithm for estimation of reference supply currents.



(a)

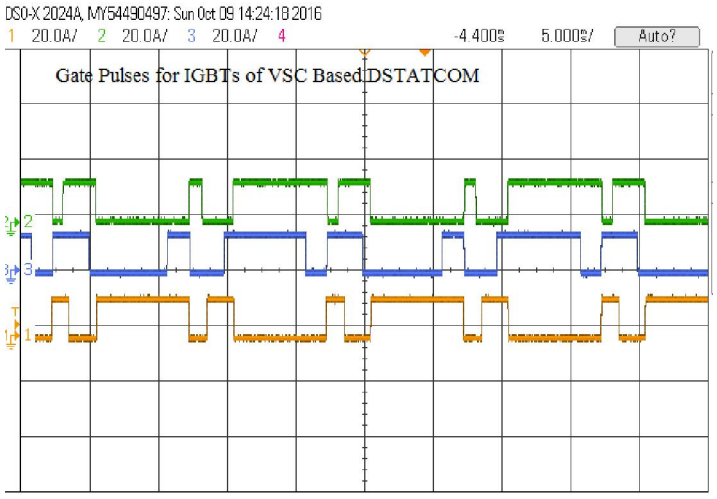


(b)

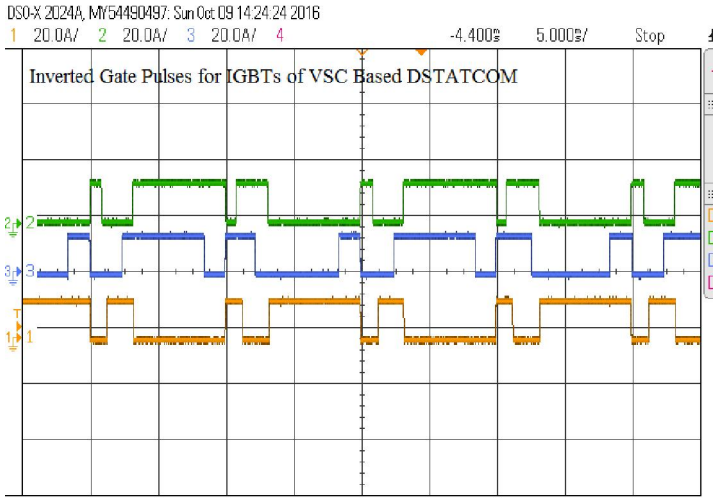
Fig. 3.26 Sensed (a) supply currents (i_{sa}, i_{sb} and i_{sc}) (b) Load currents (i_{la}, i_{lb} and i_{lc})

3.6.2.3 Hardware results of gate driver circuit

The gating pulses for IGBTs of VSC from PWM current controller are shown in Figs. 3.27 (a) and (b). These pulses are given as input to the gating circuit for amplification and amplified pulses are used to control three phase VSC.



(a)



(b)

Fig. 3.27 Generated (a) PWM pulses (b) Inverted PWM pulses, using HCC from I/O ports I/O ports of DSP dSPACE

3.7 CONCLUSIONS

The developed prototype of DSTATCOM for three phase distribution system, has been validated through hardware implementation. The developed prototype components of DSTATCOM such as VSC, DC bus capacitance, interfacing inductors, ripple filters and rating of IGBTs, have been tested and results are presented. The design and selection of different components of DSTATCOM such as VSC, DC bus capacitance, interfacing inductors, ripple filters and rating of IGBTs have been given in detail. Hall Effect voltage and current sensors with appropriate buffer circuitry have been developed for sensing signals for real time implementation. The ADC channels, DAC channels and PWM port of DSP-dSPACE have also been tested for signal processing of the developed algorithms on prototype DSTATCOM. Gating circuit has been developed for amplification of gating pulses from PWM current controller of DSP-dSPACE. The interfacing inductors and ripple filters have also been developed and fixed at their designed values. The simulation model of control algorithm has been implemented in real time validation using dSPACE, which is based on DSP-DS1104 R&D controller and a slave DSP subsystem based on TMS320F240 DSP.

CHAPTER 4
FAST MLPNN BASED CONTROL ALGORITHM FOR DSTATCOM

4.1 INTRODUCTION

The applications of neural networks have been receiving a lot of attention referring to advanced computational intelligent control approach in electrical engineering. The engineers and researchers have used neural networks for digital signal processing, system modeling, automatic control, and others [87]. Neural network based control of DSTATCOM is used for current compensation in a three phase distribution system. The appropriate architecture of neural network selection plays an important role [96]-[97]. Supervised learning of backpropagation (BP) based control of current compensation for improving the power quality at PCC of a distribution system is discussed in [98]-[99]. Since, BP is multilayer feedforward architecture, the learning process of BP is slow [96]. The conventional trainings of neural networks are mainly based on optimization theory [100]. Because of slow training, the applications of BP algorithms are restricted. Fast learning process of BP is a necessary requirement to train feedforward multilayer perceptron neural network (MLPNN); particularly for the shunt compensator in a three-phase distribution system. Fast learning improves the convergence of the BP algorithm to update the network weights iteratively to minimize globally the difference between the actual output vector of the network and the desired output vector [101]-[105]. A fast feedforward training algorithm using a modified form by taking the error in linear and quadratic form is proposed here. The rate of convergence of BP is improved using the proposed technique.

4.2 SYSTEM CONFIGURATION

A three-phase test system under study is presented in Fig. 4.1. The proposed system consists of a three-phase balanced AC supply at 50 Hz with source impedances (Z_{sa}, $Z_{sb}$and Z_{sc}) connected to a three-phase linear/nonlinear load across a DSTATCOM. The interfacing inductor (L_f) is used to interface shunt connected DSTATCOM in each phase at its AC output side to make compensating currents ripple free. Similarly, a series combination of capacitor (C_f) and a resistor (R_f) is connected to reduce the high-frequency switching noise arising due to DSTATCOM at the PCI. The required compensating currents ($i_{Ca}, i_{Cb}\ and\ i_{Cc}$) at PCI are injected from the DSTATCOM for harmonics suppression, load balancing, and reducing reactive power components of load currents. A three-phase diode bridge rectifier is considered as three-phase nonlinear load connected in series with X_L and R_L. The complete specifications of the three-phase test system are presented in Table 4.1. Power factor correction (PFC) and zero voltage regulation (ZVR) have been obtained at the PCI of the test system.

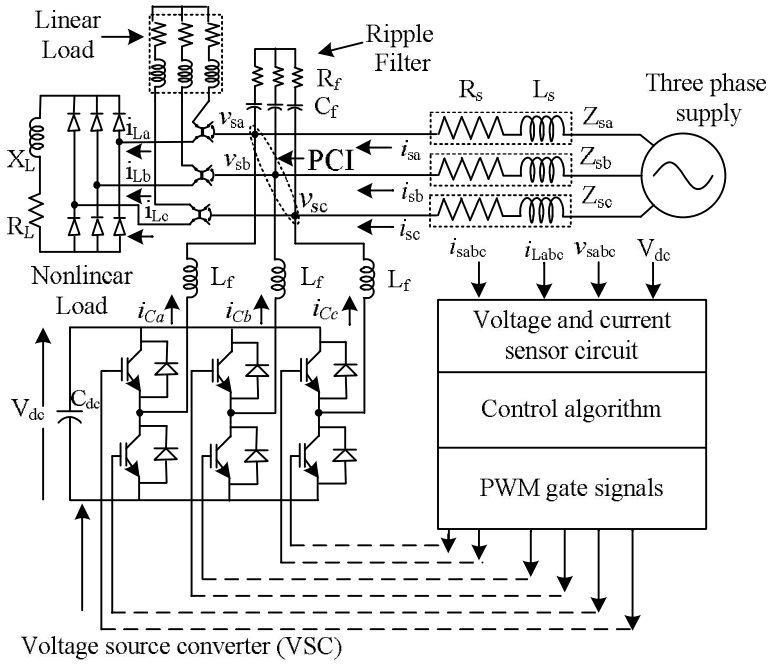


Fig. 4.1 Three-phase test system schematic diagram

Table 4.1 Design specifications of the developed test model of a three-phase distribution system

Sl. No.	Components	Specifications
1.	AC Supply	3ϕ, 415V(L-L), 50 Hz
2.	Source Impedance(Z_s)	(0.08+j0.565) Ω
3.	Ripple filter (R_f and C_f)	5Ω & 20μF
4.	Interfacing Inductor (L_f)	2.2 mH
5.	Reference DC Bus voltage (V_{dc}^*)	700V
6.	3ϕ Diode bridge rectifier module with R_L&X_L	12.5 Ω, 47.2 Ω
7.	Gains of PI controller for DC bus K_{pdc} and K_{idc}	5.75 & 0.065
8.	Gains of PI controller for terminal voltage at PCI bus K_{pt} and K_{it}	0.03 & 0.01
9.	Selected initial weights value w_0	0.5
10.	R and L for RL load	R = 8Ω, and L = 19 mH.

4.3 STANDARD BACKPROPAGATION ALGORITHM

The backpropagation (BP) algorithm is used to learn the weights of a multilayer neural network with a fixed architecture. It performs gradient descent to minimize the sum squared error between the network's output values and the given target values [97]. A network forward propagates activation to produce an output and its backward propagates error to determine weight changes.

One of the common issues about the standard backpropagation algorithm (SBP) is that it is very slow and even simple problems may take hundreds of iterations to converge. SBP algorithm reduces only non-linear errors. A reasonable work, therefore, has been done in search of fast methods. One of such approach is modified form of the SBP algorithm. Modified backpropagation algorithm consists of minimizing the sum of the squares of linear and non-linear errors for all output units. This leads to an efficient process in the network [102]-[105].

The neural network is used in signal detection for the control of the shunt active power filter and harmonics detection [106]-[111]. Moreover, the control of current compensation using DSTATCOM is available in the literature [112]-[113]. The generalization of BP based real time control of DSTATCOM is implemented using DSP to compensate unbalanced nonlinear loads [114]-[116]. The selection of the

proper neural network sizes and architecture, plays an important role in fast convergence rate of BP [117]-[119]. To deal with the dynamics of utility loads on the distribution system, the control of DSTATCOM using BP algorithm with fast convergence rate, makes the power quality under the standard limit [62].

4.4 FAST MLPNN BASED CONTROL OF DSTATCOM

Fast MLPNN based control of DSTATCOM ensures perfect regulation of the voltage and power factor at the point of common coupling (PCC) and provides means for rejecting voltage disturbances. The AC bus voltage control loop should offer zero voltage regulation performance. The DC bus voltage control loop should offer impeccable power factor by means of MLPNN. This chapter presents a newly designed MLPNN based switching of IGBTs of VSC based DSTATCOM for voltage regulation and power factor control, interfaced with a three phase distribution system.

Severe and random voltage disturbances might be initiated by time-varying loads, current distortion framed by harmonics injection caused by nonlinear load. The voltage transients associated with parallel connected loads, and voltage transients caused by capacitor switching, lead to power quality problems [98]-[99]. The proposed learning process minimizes the objective function of the BP [96]. The objective function comprises of the sum of the quadratic linear and nonlinear error signals [102]. The error signal of the quadratic linear part is appropriately weighted. This fast MLPNN based control algorithm is used to extract the weighted value of the fundamental active and reactive current components from the load currents from which the reference source currents are estimated. Case studies are presented for zero voltage regulation (ZVR) and power factor correction (PFC) in a standard three-wire distribution system feeding a nonlinear load and current compensation using a DSTATCOM. The proposed algorithm is found to be quite effective in the

improvement of power quality in three-phase distribution system under dynamic operation of nonlinear load in both PFC and ZVR modes, as validated in the case studies.

Power electronic devices are deteriorating the quality of power in distribution systems [98]. There are various issues related to power quality including harmonics suppression, load balancing, reactive power compensation for power factor correction (PFC) and zero voltage regulation (ZVR) in [18]-[19]. The distribution static compensators (DSTATCOMs) are generally used for shunt compensation. DSTATCOMs are also used as the shunt devices in three-phase distribution system because of various advantages like compensation of neutral current, improvement of power factor, load balancing, voltage regulation and harmonics current compensation [19]. However, the control of DSTATCOM is a challenging task, various algorithms are available in the literature for control of DSTATCOMs [39], [59], [98]-[99]. Neural network based control algorithms have been quite popular in implementing control algorithms for active power filter (APF) [107]-[113]. Progressive work on neural network based control algorithms is already available in the literature [107]-[119]. Moreover, many approaches have been proposed to improve the convergence of learning process for training feedforward multilayer perceptron neural network (MLPNN); however, these approaches have certain limitations [93]-[95]. For example, the learning process of BP has slow convergence for training feedforward MLPNN [96]-[98]. Training for feedforward for MLPNN, requires reasonable computation time. In addition, the selection of convergence parameters may adversely affect the convergence [100]-[102]. In comparison, the proposed learning process of the BP minimizes the objective function by taking the sum of the quadratic linear and nonlinear error signals with the application of gradient descent method. The quadratic

linear error signal with weighted convergence coefficient 'λ' is taken into account for optimization [102]. The update of weight depends on both quadratic and linear error signals; however, the linear error term depends on the choice of 'λ', which is obtained from the ranks and their asymptotic constant error values [102]. Its values lie between $0 \leqslant \lambda \leqslant 1$. The most attractive feature of the proposed algorithm is the adjustable adaptation gain rate parameter improving the convergence ability and accelerating the MLPNN learning process.

The proposed fast learning process extracts the amplitude of the fundamental active power current components from the load currents at each stage of the network. Using these amplitudes and the in-phase and quadrature templates obtained from the sensed voltages at the point of common interface (PCI), the reference source currents are estimated and the switching of DSTATCOM for PFC and ZVR in three-phase distribution system is done. An improved convergence of the backpropagation algorithm is achieved using learning rate adaptation methods. The goal of supervised training is to update the network weights iteratively to minimize globally the difference between the actual output vector of the network and the desired output vector. The rapid computation of such a global minimum is a rather difficult task since, in general, the number of network variables, is large and the corresponding nonconvex multimodal objective function possesses multitudes of local minima and has broad flat regions adjoined with narrow steep ones.

4.5 MATHEMATICAL MODELING OF FAST MLPNN ALGORITHM

Standard back-propagation (SBP) is the supervised learning method of multilayer perceptron neural network [100]-[102]. SBP is the most popular method used to select values for ANN free parameters [103]. It is done iteratively, calculating the error gradients of the data in respect to the free parameters and then updating them

appropriately [104]. The error gradients are calculated starting from the error on the outputs and works backwards [105]-[107]. Each iteration of all the training data is called an epoch. It is a steepest decent search for minima, like a ball rolling down a hill [103].

The schematic diagram of the proposed fast learning process of BP to train feedforward MLPNN based control algorithm for the shunt compensator is presented in Fig. 4.2. The proposed learning process is initiated at the output layer due to known linear and nonlinear errors, while the learning process of hidden layer takes place later as their errors are unknown and estimated using the output parameters of the updated weights. The proposed optimization criterion function 'E' of BP for MLPNN is defined as,

$$E = \sum \frac{1}{2}(e_1)^2 + \sum \lambda \frac{1}{2}(e_2)^2 \tag{4.1}$$

where λ is a weighting coefficient, and e_1 and e_2 are nonlinear and linear error signals. The learning process to update the weights of the output layer, is realized using least mean square (LMS) algorithm with the application of gradient descent method to eqn. (4.1). An additional term '$\sum \lambda \frac{1}{2}(e_2)^2$, is added to the proposed optimization criteria on function to improve the learning process, which is not available in the SBP [102]. This optimization criterion converges faster than the standard BP for the MLPNN. The choice of the value of 'λ' is proved in [101]. A very small value of 'λ' does not influence the convergence speed, whereas a high value may cause the divergence of the algorithm.

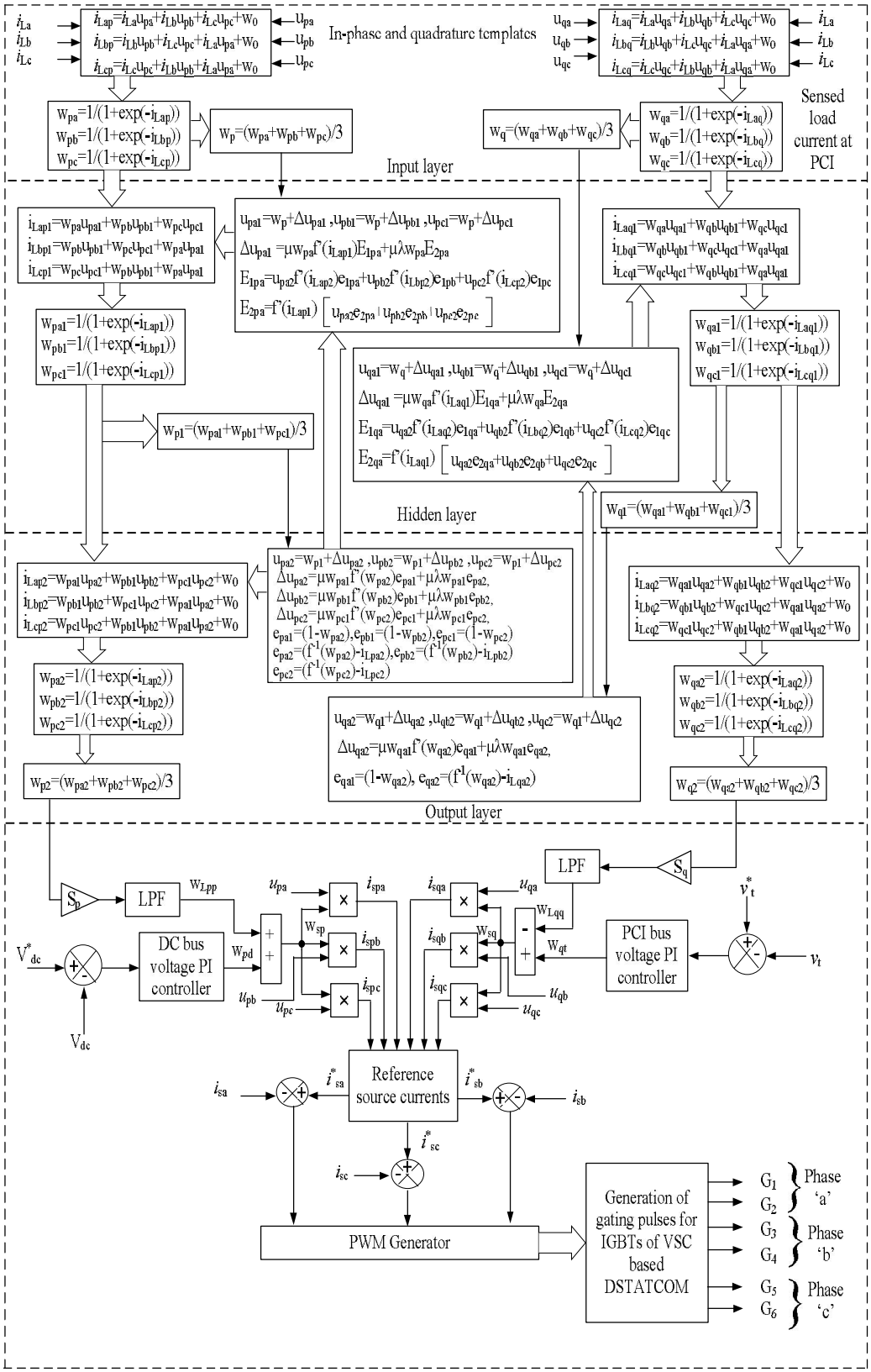


Fig. 4.2 Functional block diagram of MLPNN algorithm

4.6 ESTIMATION OF FUNDAMENTAL REFERENCE SOURCE CURRENTS

The estimation of fundamental reference source currents comprises of active and reactive components extracted from the load currents and the amplitude of the reference source currents of active and reactive power current components. The amplitude of the fundamental active current components is computed using load currents and by taking the error of DC link voltage between reference and sensed values. Similarly, the amplitude of the fundamental reactive current component is estimated by taking the error of the amplitude of the AC bus voltage at PCC and extracted reactive component of the load current. These components are estimated as follows:

4.6.1 Amplitude Estimation of Fundamental Load Active Current Components

The three-stage network model of the fast MLPNN algorithm is shown in Fig. 4.3. The MLPNN is a summation type neural network that contains aggregation and sigmoid function in each stage. The proposed algorithm is used to estimate the weighted value of the fundamental active ($w_{pa2}, w_{pb2}, w_{pc2}$) and reactive ($w_{qa2}, w_{qb2}, w_{qc2}$) current components from the polluted load currents (i_{La}, i_{Lb}, i_{Lc}). The weighted values of the fundamental active and reactive current components are estimated at input, hidden and output layers of the MLPNN.

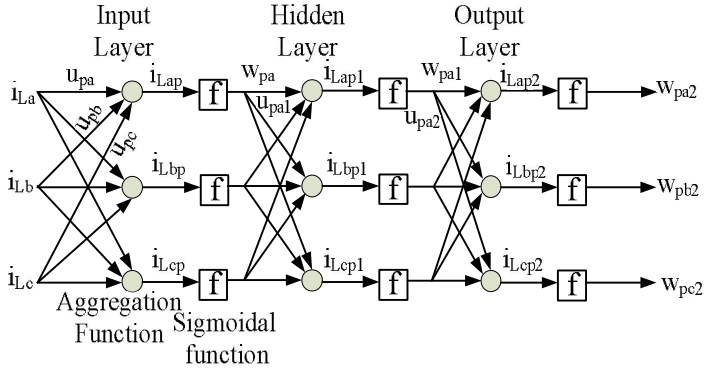


Fig. 4.3 Proposed three-stage MLPNN model of the weighted fundamental active current components

The load currents (i_{La}, i_{Lb}, i_{Lc}), source currents (i_{sa}, i_{sb}, i_{sc}) and line voltages (v_{ab}, v_{bc}, v_{ca}) are sensed at PCI of the three-phase distribution system. These parameters are the inputs of the MLPNN. The output of the sigmoidal functions at each layer results into the extraction of weighted value of the fundamental active current component. The aggregation function is the summation of the products of the input signals (i_{La}, i_{Lb}, i_{Lc}) with their weights ($u_{pa}, u_{pb} and\ u_{pc}$) calculated from phase voltages (v_{sa}, v_{sb}, v_{sc}) at each node of the input layer, and these are expressed as,

$$i_{Lap} = i_{La}u_{pa} + i_{Lb}u_{pb} + i_{Lc}u_{pc} + w_0 \tag{4.2}$$

$$i_{Lbp} = i_{Lb}u_{pb} + i_{Lc}u_{pc} + i_{La}u_{pa} + w_0 \tag{4.3}$$

$$i_{Lcp} = i_{Lc}u_{pc} + i_{Lb}u_{pb} + i_{La}u_{pa} + w_0 \tag{4.4}$$

where w_0 is a bias that acts exactly as a weight on a connection from a unit whose activation is always 1.

However, the in-phase unit templates are estimated with the help of phase voltages (v_{sa}, v_{sb}, v_{sc}), which are obtained from sensed instantaneous line voltages v_{ab} and v_{bc} at PCI. The estimation of phase voltages $v_{sa}, v_{sb}\ and\ v_{sc}$ are determined as,

$$v_{sa} = \left(\frac{2}{3}v_{ab} + \frac{1}{3}v_{bc}\right) \tag{4.5}$$

$$v_{sb} = \left(-\frac{1}{3}v_{ab} + \frac{1}{3}v_{bc}\right) \tag{4.6}$$

$$v_{sc} = \left(-\frac{1}{3}v_{ab} + \frac{2}{3}v_{bc}\right) \tag{4.7}$$

The in-phase unit templates relate the phase voltages and the amplitude of the PCI voltage (V_t). The amplitude of the PCI voltage V_t is calculated as,

$$V_t = \left\{\frac{2}{3}((v_{sa})^2 + (v_{sb})^2 + (v_{sc})^2)\right\}^{\frac{1}{2}}. \tag{4.8}$$

Using eqns. (4.5)-(4.8), the in-phase unit templates ($u_{pa}, u_{pb} and\ u_{pc}$) are estimated as,

$$u_{pa} = \frac{v_{sa}}{V_t}, u_{pb} = \frac{v_{sb}}{V_t} \; and \; u_{pc} = \frac{v_{sc}}{V_t} . \tag{4.9}$$

The output of the aggregation neuron of each phase, passed through sigmoidal function, to estimate the weighted value at the input layer is given as,

$$f(i_{Lap}) = w_{pa} = \frac{1}{1 + exp(-i_{Lap})} \tag{4.10}$$

$$f(i_{Lbp}) = w_{pb} = \frac{1}{1 + exp(-i_{Lbp})} \tag{4.11}$$

$$f(i_{Lcp}) = w_{pc} = \frac{1}{1 + exp(-i_{Lcp})} \tag{4.12}$$

The estimated weighted values w_{pa}, w_{pb} and w_{pc} are used to estimate the average weighted value of the fundamental active current component w_p of the load current at the input layer as a feedback signal, which is given as,

$$w_p = \frac{(w_{pa} + w_{pb} + w_{pc})}{3} \tag{4.13}$$

The weighted neurons (w_{pa}, w_{pb} and w_{pc}) of the input layer, are the input along with their updated weights (u_{pa1}, u_{pb1} and u_{pc1}) for the feedforward to the hidden layer of MLPNN. With these parameters, the activity of the network is propagated feedforward with aggregation function in the hidden layer as,

$$i_{Lap1} = w_{pa}u_{pa1} + w_{pb}u_{pb1} + w_{pc}u_{pc1} \tag{4.14}$$

$$i_{Lbp1} = w_{pb}u_{pb1} + w_{pc}u_{pc1} + w_{pa}u_{pa1} \tag{4.15}$$

$$i_{Lcp1} = w_{pc}u_{pc1} + w_{pb}u_{pb1} + w_{pa}u_{pa1} \tag{4.16}$$

The updated weights of the hidden layer for 'k' instant is given as,

$$u_{pa1}(k) = w_p(k) + \Delta u_{pa1}(k) \tag{4.17}$$

$$u_{pb1}(k) = w_p(k) + \Delta u_{pb1}(k) \tag{4.18}$$

$$u_{pc1}(k) = w_p(k) + \Delta u_{pc1}(k) \tag{4.19}$$

The activation of the neuron in the hidden layer for the weighted value at each node is given as,

$$w_{pa1} = \frac{1}{1 + exp(-i_{Lap1})} \tag{4.20}$$

$$w_{pb1} = \frac{1}{1 + exp(-i_{Lbp1})} \tag{4.21}$$

$$w_{pc1} = \frac{1}{1 + exp(-i_{Lcp1})} \tag{4.22}$$

The average weighted value of the fundamental active component w_{p1} between hidden and output layer as feedback signal is estimated as,

$$w_{p1} = \frac{(w_{pa1} + w_{pb1} + w_{pc1})}{3} \tag{4.23}$$

The activities at the output node in the network, are further propagated with the aggregation function and activation function to get the desired weighted value of fundamental active power current components, and are estimated as,

$$i_{Lap2} = w_{pa1}u_{pa2} + w_{pb1}u_{pb2} + w_{pc1}u_{pc2} \tag{4.24}$$

$$i_{Lbp2} = w_{pb1}u_{pb2} + w_{pc1}u_{pc2} + w_{pa1}u_{pa2} \tag{4.25}$$

$$i_{Lcp2} = w_{pc1}u_{pc2} + w_{pb1}u_{pb2} + w_{pa1}u_{pa2} \tag{4.26}$$

The activation of the neuron in the output layer for the weighted value at each node is expresses as,

$$w_{pa2} = \frac{1}{1 + exp(-i_{Lap2})} \tag{4.27}$$

$$w_{pb2} = \frac{1}{1 + exp(-i_{Lbp2})} \tag{4.28}$$

$$w_{pc2} = \frac{1}{1 + exp(-i_{Lcp2})} \tag{4.29}$$

The weights of the hidden layer, are obtained with the updates to the weights of output layer using error BP. The updates of the weights of the output layer are estimated for all the three phases as,

$$u_{pa2}(k) = w_{p1}(k) + \Delta u_{pa2}(k) \tag{4.30}$$

$$u_{pb2}(k) = w_{p1}(k) + \Delta u_{pb2}(k) \tag{4.31}$$

$$u_{pc2}(k) = w_{p1}(k) + \Delta u_{pc2}(k) \tag{4.32}$$

The proposed technique of optimization criterion using least mean squared (LMS) algorithm that minimizes the sum of the squares of the errors between the actual and the desired output for phase 'a' between the output and the hidden layer is given as,

$$E_{pa} = \sum \frac{1}{2}\left(e_{1pa}\right)^2 + \sum \lambda \frac{1}{2}\left(e_{2pa}\right)^2 \tag{4.33}$$

where λ is weighting coefficient, and e_{1pa} and e_{2pa} are the nonlinear and linear errors of phase 'a', respectively. These errors are known at the output layer and are equal to,

$$e_{1pa} = 1 - w_{pa2} \tag{4.34}$$

$$e_{2pa} = \left[f^{-1}\left(w_{pa2}\right) - i_{Lap2}\right] \tag{4.35}$$

Similarly, the nonlinear and linear errors for phases 'b' and 'c' are calculated using the optimization criterion, given as,

$$e_{1pb} = 1 - w_{pb2} \tag{4.36}$$

$$e_{2pb} = \left[f^{-1}\left(w_{pb2}\right) - i_{Lbp2}\right] \tag{4.37}$$

and,

$$e_{1pc} = 1 - w_{pc2} \tag{4.38}$$

$$e_{2pc} = \left[f^{-1}\left(w_{pc2}\right) - i_{Lcp2}\right] \tag{4.39}$$

The application of the gradient descent method to the optimization criterion E_{pa} in the output layer leads to,

$$\Delta u_{pa2}(k) = \mu f'\left(i_{Lap2}\right) e_{1pa} w_{pa1}(k) + \mu\lambda e_{2pa} w_{pa1}(k) \tag{4.40}$$

$$\Delta u_{pb2}(k) = \mu f'\left(i_{Lbp2}\right) e_{1pb} w_{pb1}(k) + \mu\lambda e_{2pb} w_{pb1}(k) \tag{4.41}$$

$$\Delta u_{pc2}(k) = \mu f'\left(i_{Lcp2}\right) e_{1pc} w_{pc1}(k) + \mu\lambda e_{2pc} w_{pc1}(k) \tag{4.42}$$

The learning process between the hidden and output layers is given in eqns. (4.40)-(4.42) to update the weights as in eqns. (4.30)-(4.32). The modified form to improve the learning process of BP as in eqns. (4.40)-(4.42), depends on the choice of the weighted parameter λ termed as convergence coefficient. The value of the weighted parameter λ is obtained via rank convergence series analysis and asymptotic constant error values [101]. Similarly, the learning process between the input and hidden layers, is obtained by applying gradient descent method to E_{pa} for the hidden layer [102]. In the hidden layer, both the nonlinear and linear error outputs are unknown. These errors are estimated using the updating of weights with the linear and nonlinear errors of the output layer. The generalized result of the optimization criterion for phase 'a' of the hidden layer is defined as,

$$\Delta u_{pa1}(k) = \mu w_{pa} f'\left(i_{Lap1}\right) E_{1pa} + \mu\lambda w_{pa} E_{2pa} \tag{4.43}$$

where $E_{1pa} = \left[e_{1pa} f'\left(i_{Lpa2}\right) u_{pa2} + e_{1pb} f'\left(i_{Lpb2}\right) u_{pb2} + e_{1pc} f'\left(i_{Lpc2}\right) u_{pc2}\right]$

and, $E_{2pa} = f'\left(i_{Lpa1}\right)\left[e_{2pa} u_{pa2} + e_{2pb} u_{pb2} + e_{2pc} u_{pc2}\right]$

eqn. (4.43) contains the nonlinear error, E_{1pa} and linear error, E_{2pa}, between input and hidden layer for phase 'a'. In the similar manner, these errors can be obtained for phases 'b' and 'c' also.

The average weighted fundamental active power current component w_{p2} is obtained using the weighted fundamental active power current component of each phases 'a', 'b' and 'c', and is given as,

$$w_{p2} = \frac{\left(w_{pa2} + w_{pb2} + w_{pc2}\right)}{3} \tag{4.44}$$

The low-frequency components from w_{p2} are separated using first-order low-pass filters. The obtained output w_{pp} is multiplied by scaled factor "S_p" to get the actual value of the fundamental active power current component, as the output of the activation function is between 0 and 1. After separating the low-frequency components and scaling to the actual value, the fundamental active power current component is represented as w_{Lpp}.

4.6.2 Active Power Current Components Amplitude of Reference Source Currents

The amplitude of active power current components of the reference source currents is obtained by taking of the error of reference V_{dc}^{*} and observed V_{dc} values of DC link voltage at k^{th} sampling instant, and is given as,

$$V_{de}(k) = V_{dc}^{*}(k) - V_{dc}(k) \tag{4.45}$$

The estimated error value of DC bus voltage $V_{de}(k)$ at k^{th} sampling instant is passed through a discrete proportional–integral (PI) controller to maintain constant level of the DC link voltage, which is given as,

$$w_{pd}(k) = w_{pd}(k-1) + k_{pd}\{V_{de}(k) - V_{de}(k-1)\} + k_{id}V_{de}(k) \tag{4.46}$$

where k_{pd} and k_{id} are the proportional and integral gain constants of PI controller. The suitable values of gain constants are obtained from Ziegler–Nichols tuning formula [120]. $V_{de}(k)$ and $V_{de}(k-1)$ are error values of DC bus voltage, and $w_{pd}(k)$ and $w_{pd}(k-1)$ are the levels of the magnitude of the fundamental active power current component of the reference source current at k^{th} and $(k-1)^{th}$ sampling instants, respectively.

The sum of the controlled output of DC bus voltage w_{pd} and mean amplitude of the active power current component w_{pp}, gives the amplitude of the active power current components of the reference source current, w_{sp} as,

$$w_{sp} = w_{Lpp} + w_{pd} \tag{4.47}$$

4.6.3 Amplitude Estimation of Fundamental Load Reactive Current Components

Similarly, the weighted amplitude of the reactive power components ($w_{qa2}, w_{qb2}\ and\ w_{qc2}$) of the load currents are estimated. The steps to estimate the reactive power current component w_{qa2} of phase 'a' follow the similar manner of processing the neuron signal in the MLPNN. The network input neurons flow with their weights through aggregation to the sigmoidal function in determining the weighted amplitude of the reactive power component of the fundamental load current. The net input at the first node of MLPNN network for fundamental reactive power component of phase 'a' is given as,

$$i_{Laq} = i_{La}u_{qa} + i_{Lb}u_{qb} + i_{Lc}u_{qc} + w_0 \tag{4.48}$$

$$f(i_{Laq}) = w_{qa} = \frac{1}{1 + exp(-i_{Laq})} \tag{4.49}$$

The quadrature unit templates components u_{qa}, u_{qb} and u_{qc} are considered as the weights and the load currents (i_{La}, i_{Lb}, i_{Lc}), are taken as input signals at the input layer of MLPNN network. The quadrature unit templates ($u_{qa}, u_{qb} and\ u_{qc}$) are estimated using eqn. (4.9) as,

$$u_{qa} = \frac{(-u_{pb} + u_{pc})}{\sqrt{3}}, u_{qb} = \frac{(3u_{pa} + u_{pb} - u_{pc})}{2\sqrt{3}},$$

$$u_{qc} = \frac{(-3u_{pa} + u_{pb} - u_{pc})}{2\sqrt{3}} \tag{4.50}$$

The weighted value w_{qa} is the input between the input and the hidden layer with their new weight u_{qa1}. The average weighted fundamental reactive component w_q in between stages is calculated using the weighted value of the fundamental reactive components of all the phases as,

$$w_q = \frac{\left(w_{qa} + w_{qb} + w_{qc}\right)}{3} \tag{4.51}$$

With the estimated weighted values of the fundamental reactive power current components and weights, the processes of aggregation and sigmoidal functions are again repeated at hidden layer and is given as,

$$i_{Laq1} = w_{qa}u_{qa1} + w_{qb}u_{qb1} + w_{qc}u_{qc1} \tag{4.52}$$

$$w_{qa1} = \frac{1}{1 + exp\left(-i_{Laq1}\right)} \tag{4.53}$$

The sum of the average weighted fundamental reactive component w_q and change in the weights Δu_{qa1}through learning process between input and hidden layer at k^{th} instant is estimated as,

$$u_{qa1}(k) = w_q(k) + \Delta u_{qa1}(k) \tag{4.54}$$

The average weighted fundamental reactive component w_{q1} is estimated using the fundamental reactive components w_{qa1}, w_{qb1} and w_{qc1} of the phases at the hidden layer, and is given as,

$$w_{q1} = \frac{\left(w_{qa1} + w_{qb1} + w_{qc1}\right)}{3} \tag{4.55}$$

The learning process to obtain the change in weight $\Delta u_{qa1}(k)$ in eqn.(4.54) between input and hidden layers through BP is achieved with the optimization technique proposed for fundamental active power current component defined in eqn. (4.43). Therefore, the learning process to update the weight of the hidden layer from [101] for phase 'a' is obtained as,

$$\Delta u_{qa1}(k) = \mu w_{qa} f'\left(i_{Laq1}\right) E_{1qa} + \mu\lambda w_{qa} E_{2qa}\ , \tag{4.56}$$

Where $E_{1qa} = \left[e_{1qa}f'\left(i_{Lqa2}\right)u_{qa2} + e_{1qb}f'\left(i_{Lqb2}\right)u_{qb2} + e_{1qc}f'\left(i_{Lqc2}\right)u_{qc2}\right]$ and

$E_{2qa} = f'\left(i_{Laq1}\right)\left[e_{2qa}u_{qa2} + e_{2qb}u_{qb2} + e_{2qc}u_{qc2}\right]$.

The estimated values of linear and nonlinear errors are E_{1qa} and E_{2qa} in eqn. (4.56) between input and hidden layers, respectively. Similarly, the linear and nonlinear errors e_{1qa} and e_{2qa} between hidden and output layers for phase 'a' are calculated as,

$$e_{1qa} = 1 - w_{qa2} \tag{4.57}$$

$$e_{1qa} = \left[f^{-1}(w_{qa2}) - i_{Laq2}\right] \tag{4.58}$$

The resultant output of the output layer is again processed with the aggregation and sigmoidal function to get the desired weighted fundamental reactive current components w_{qa2}, w_{qb2} and w_{qc2} with their weights, as follows,

$$i_{Laq2} = w_{qa1}u_{qa2} + w_{qb1}u_{qb2} + w_{qc1}u_{qc2} \tag{4.59}$$

$$i_{Lbq2} = w_{qb1}u_{qb2} + w_{qc1}u_{qc2} + w_{qa1}u_{qa2} \tag{4.60}$$

$$i_{Lcq2} = w_{qc1}u_{qc2} + w_{qb1}u_{qb2} + w_{qa1}u_{qa2} \tag{4.61}$$

$$w_{qa2} = \frac{1}{1 + exp(-i_{Laq2})} \tag{4.62}$$

$$w_{qb2} = \frac{1}{1 + exp(-i_{Lbq2})} \tag{4.63}$$

$$w_{qc2} = \frac{1}{1 + exp(-i_{Lcq2})} \tag{4.64}$$

Using eqns. (4.62)-(4.64), the average weighted value of the fundamental reactive current component w_{q2} is estimated as,

$$w_{q2} = \frac{(w_{qa2} + w_{qb2} + w_{qc2})}{3}. \tag{4.65}$$

The low-frequency component of average weighted fundamental reactive power component w_{q2} is separated using first-order low-pass filter. The extracted weighted fundamental reactive current component value is multiplied by scaled factor "S_q" to get the actual value because the output of the activation function lies between 0 and 1 and is represented as w_{Lqq}. Using this, AC bus voltage regulation at PCI is achieved.

4.6.4 Reactive Power Current Components Amplitude of Reference Source Currents

For the voltage regulation, leading reactive power components from DSTATCOM compensate the drop of AC bus voltage at PCI. The voltage regulation is achieved by taking the error of the terminal voltage 'V_{te}' between the reference 'V_t^*'and observed terminal voltage 'V_t' of AC bus voltage of PCI at the k^{th} sampling instant, given as,

$$V_{te}(k) = V_t^*(k) - V_t(k) \tag{4.66}$$

The weighted resultant error signal V_{te} is regulated through a PI controller to maintain constant level of AC bus voltage at PCI. It is expressed as,

$$w_{qt}(k) = w_{qt}(k-1) + k_{pt}\{V_{te}(k) - V_{te}(k-1)\} + k_{it}V_{te}(k) \tag{4.67}$$

where $w_{qt}(k)$ and $w_{qt}(k-1)$ are the reactive power current components of the reference source current, and $V_{te}(k)$ and $V_{te}(k-1)$ are the errors of terminal voltage at k^{th} and $(k-1)^{th}$ sampling instants of AC bus voltage at PCI. The constants k_{pt} and k_{it} are proportional and integral gain constants of PI controller of the AC bus voltage. Suitable values of gain constants are obtained from Ziegler–Nichols tuning method given in [120].

In this case, the reactive power current component leads AC bus voltage at PCI. The amplitude of the reactive power component w_{sq} of the reference source current is obtained by taking the difference of controlled output current w_{qt} and average amplitude of the load reactive power current component w_{Lqq} as,

$$w_{sq} = w_{qt} - w_{Lqq} \tag{4.68}$$

4.6.5 Generation of Switching Gate Pulses of DSTATCOM

The fundamental reference source currents are obtained using the estimated amplitude of the active and reactive power current components of the load currents with in-phase and quadrature templates of PCI voltages. The products of these estimated

active and reactive power current components of the reference source current with the in-phase and quadrature unit templates of each phase (a, b and c) are given as,

$$i_{spa} = w_{sp} * u_{pa},\ i_{spb} = w_{sp} * u_{pb},\ i_{spc} = w_{sp} * u_{pc} \tag{4.69}$$

$$i_{sqa} = w_{sq} * u_{qa},\ i_{sqb} = w_{sq} * u_{qb},\ i_{sqc} = w_{sq} * u_{qc} \tag{4.70}$$

The sum of these components, gives the fundamental reference source currents for phases 'a', 'b' and 'c' as,

$$i_{sa}^{*} = i_{spa} + i_{sqa}, \qquad i_{sb}^{*} = i_{spb} + i_{sqb}, \qquad i_{sc}^{*} = i_{sqa} + i_{sqc} \tag{4.71}$$

The errors of the source currents (i_{sa}, i_{sb}, i_{sc}) and the reference source currents ($i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*}$) are amplified and multiplied to signals that are compared with the triangular wave of carrier frequency of the order of 10 kHz, which results in a pulse width modulation (PWM) signals, for power devices namely insulated-gate bipolar transistors (IGBTs) G1 to G6 of the VSC-based DSTATCOM.

4.7 RESULTS AND DISCUSSION

The proposed algorithm has been implemented in MATLAB SIMULINK platform using Sim Power System (SPS) tool boxes to develop the model to control DSTATCOM in three-phase distribution system for power factor correction (PFC) and zero voltage regulation (ZVR) at PCI under linear/nonlinear loading conditions.

4.7.1 *Case Study I*: Performance of DSTATCOM in PFC Mode

In this case study, the DSTATCOM is operated in the PFC mode under nonlinear and linear load conditions:

4.7.1.1 Simulation results at nonlinear load conditions

The MLPNN network at input, hidden and output stages, is used to estimate the amplitude of the fundamental active power current components with the modified learning process of the BP. The MLPNN network signals are system parameters which are shown in Fig. 4.4, and their corresponding estimated intermediate signals

are shown in Fig. 4.5, respectively. Fig. 4.4 shows simulated results under steady state and dynamic condition at nonlinear load in PFC mode. These results present waveforms of PCC voltages (v_s), supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_{Ca}, i_{Cb}, i_{Cc}), AC bus voltage amplitude (V_t) and DC bus voltage (Vc_d), respectively. Supply currents are observed balanced and sinusoidal during steady state (before t=1.1s) and during unbalanced load conditions (t=1.1s to t=1.3s). Due to the action of PI controller, the voltage at DC bus of VSC is regulated at the reference value of 700V. The amplitude of AC bus voltage (V_t) at PCI is deviated from the reference value between 337.5V to 339V under steady state and dynamic performance of DSTATCOM in PFC mode.

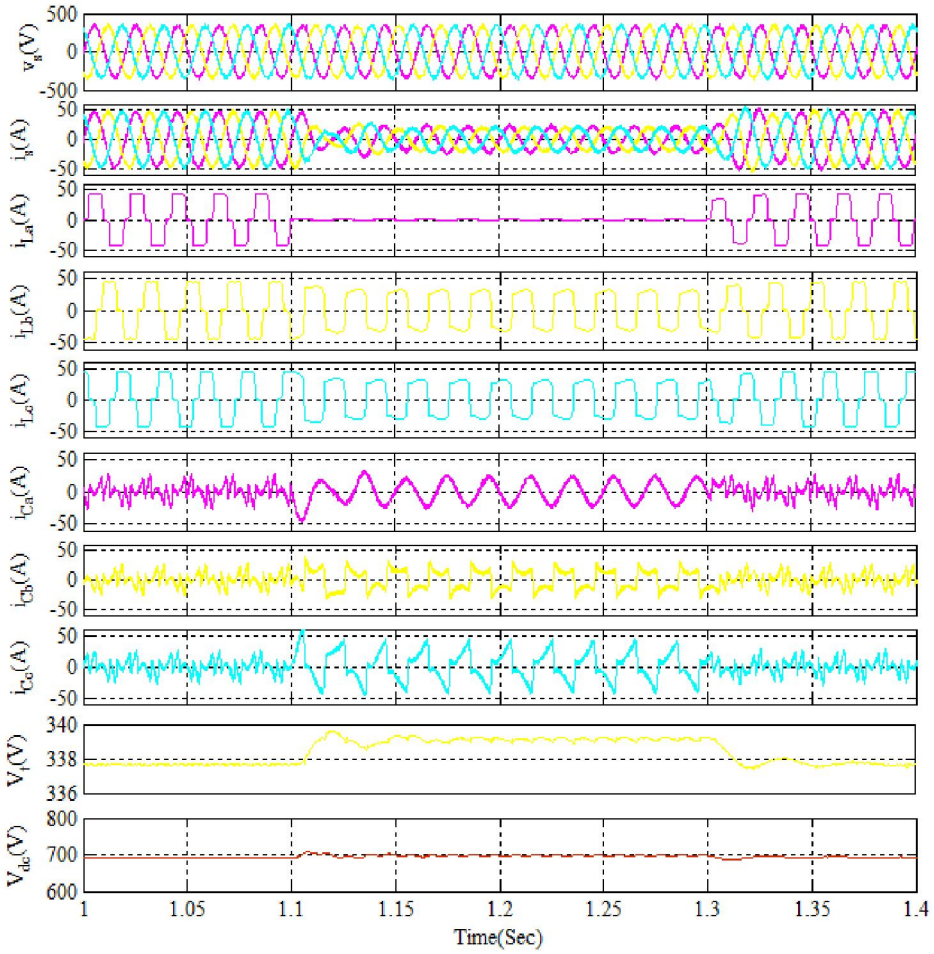


Fig. 4.4 Simulated performance of DSTATCOM at nonlinear load in PFC mode

Figs. 4.5 shows, the intermediate signals of the proposed MLPNN algorithm at input, hidden and output layers for the extraction of active power current component from load current of phase ‘a’.

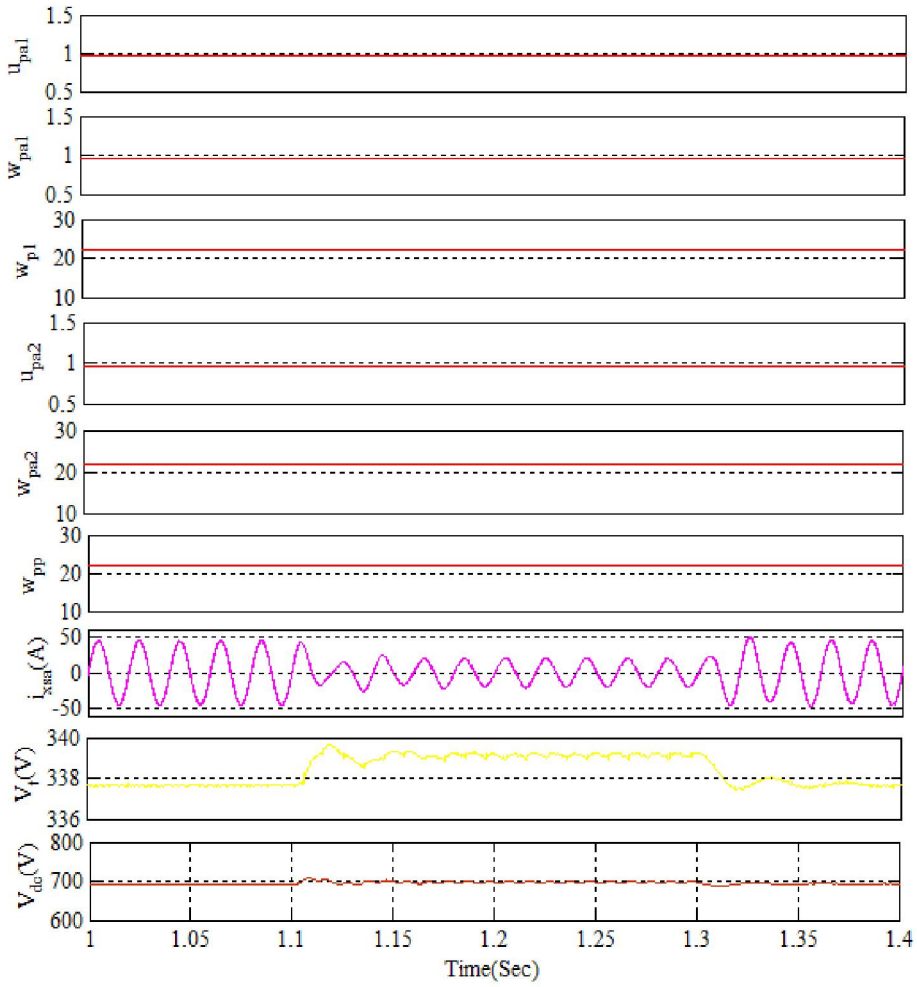


Fig. 4.5 Intermediate signals of MLPNN algorithm in PFC mode

The intermediate signals are coefficient (u_{pa1}) of the weighted neuron of active current component (w_{pa1}) of phase ‘a’ and weighted mean (w_{p1}) of active current component of all the three phases ($w_{pa1}, w_{pb1}, w_{pc1}$) at hidden layer after scaling. The extracted weight coefficient (u_{pa2}) of the active neuron (w_{pa2}) of phase ‘a’ and the mean active neuron (w_{pp}) of all the three phases ($w_{pa2}, w_{pb2}, w_{pc2}$) at the output layer, the error between the desired value and the actual value is backpropagated to

minimize it. The fast learning of the MLPNN has been observed after extraction of the active power current component for all the phases. These extracted active power current components are further used to estimate the fundamental reference source currents (i_{xs}). The amplitude of the DC bus voltage (V_{dc}) is deviated under unbalance load condition (t=1.1s to t=1.3s), which is maintained to the reference level by the action of PI controller tuned using Ziegler Nichols method. Moreover, the amplitude of the AC bus voltage (V_t) is also deviated simultaneously. The switching of the DSTATCOM takes place by comparing the fundamental source currents and the estimated reference source currents, and this error is fed to hysteresis current controller (HCC) for generation of PWM pulses. The injected compensating currents improve the THDs in supply current due to action of the DSTATCOM and are found within the limit specified by IEEE-519 standard.

Power quality is also based on the percentage value of the total harmonic distortion (THD). The THDs of phase 'a' voltage (v_{sa}), current (i_{sa}) and load current (i_{La}) are obtained from the captured waveforms, and the THDs are observed as 1.66%, 2.06% and 24.14%, respectively, which are shown in Figs.4.6 (a)-(c), and the obtained results of THDs are also compared with SBP in Table 4.2. The THDs of PCI voltage and source current are within 5%, a limit of an IEEE standard. Fig. 4.6(b) shows source current waveform and its frequency spectrum after the compensation is provided by DSTATCOM. Source current waveform is sinusoidal in nature and frequency spectrum shows only fundamental component of the source current of phase 'a'.

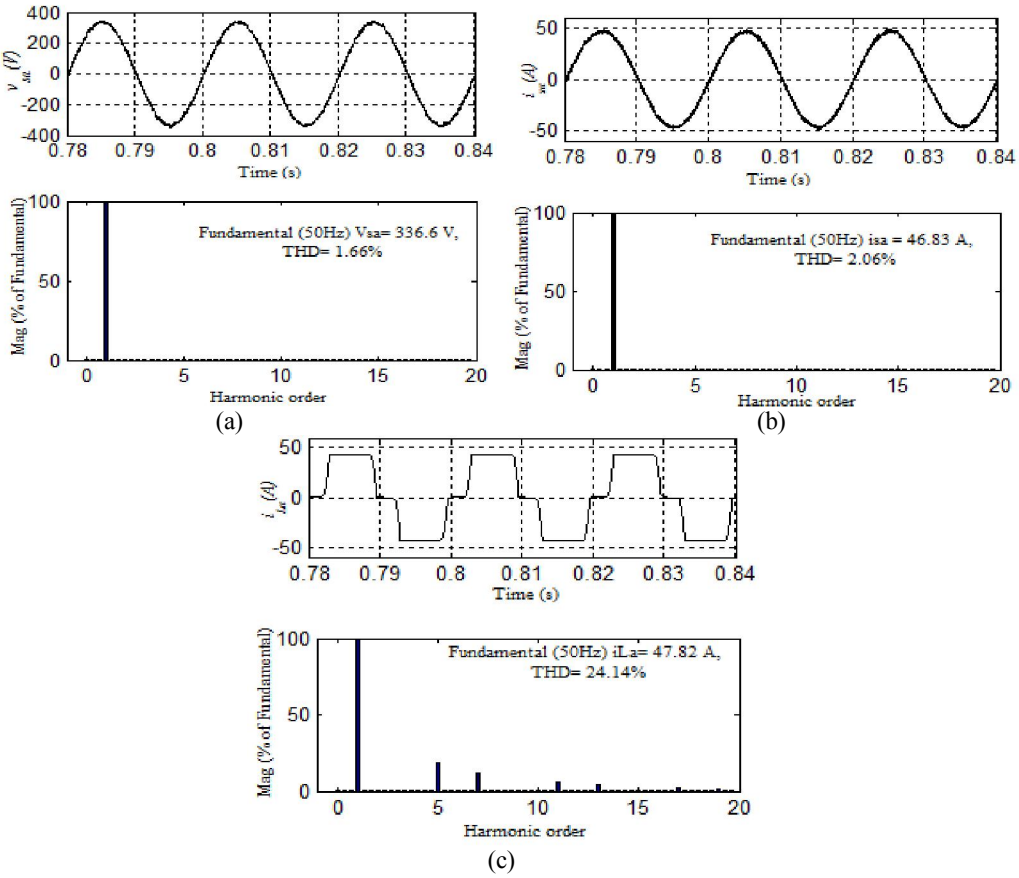


Fig. 4.6 Waveforms and harmonic spectra of (a) PCI voltage (b) Source current, and (c) Load current of phase 'a'

4.7.1.2 Simulation results at linear load conditions

Fig. 4.7 shows the dynamic performance of DSTATCOM in PFC mode using MLPNN based control algorithm. These results present waveforms of PCI voltages (v_s), supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_{Ca}, i_{Cb}, i_{Cc}), reference source currents (i_{xs}), AC bus voltage amplitude (V_t) and DC bus voltage (V_{dc}), respectively. A linear load, specified as per Table 4.1, is connected to the system. At t=1.1s, the linear load of phase 'a' is removed. At t=1.3s, this load is suddenly injected to establish the implementation of proposed control algorithm during dynamic conditions. Due to this sudden change in load, voltage across DC bus is deviated from its constant value to supply power to the load. Within a half cycle of

the fundamental frequency, the DC bus voltage attains its previous value again i.e. the reference value. This indicates that the proposed MLPNN algorithm converges faster than the BP algorithm. There is a compensation delay because of presence of low pass filter which is used to filter out power signals. Moreover, for MLPNN, phase calculation uses voltage signals; any noise or distortion in voltage produces inaccurate reference source currents.

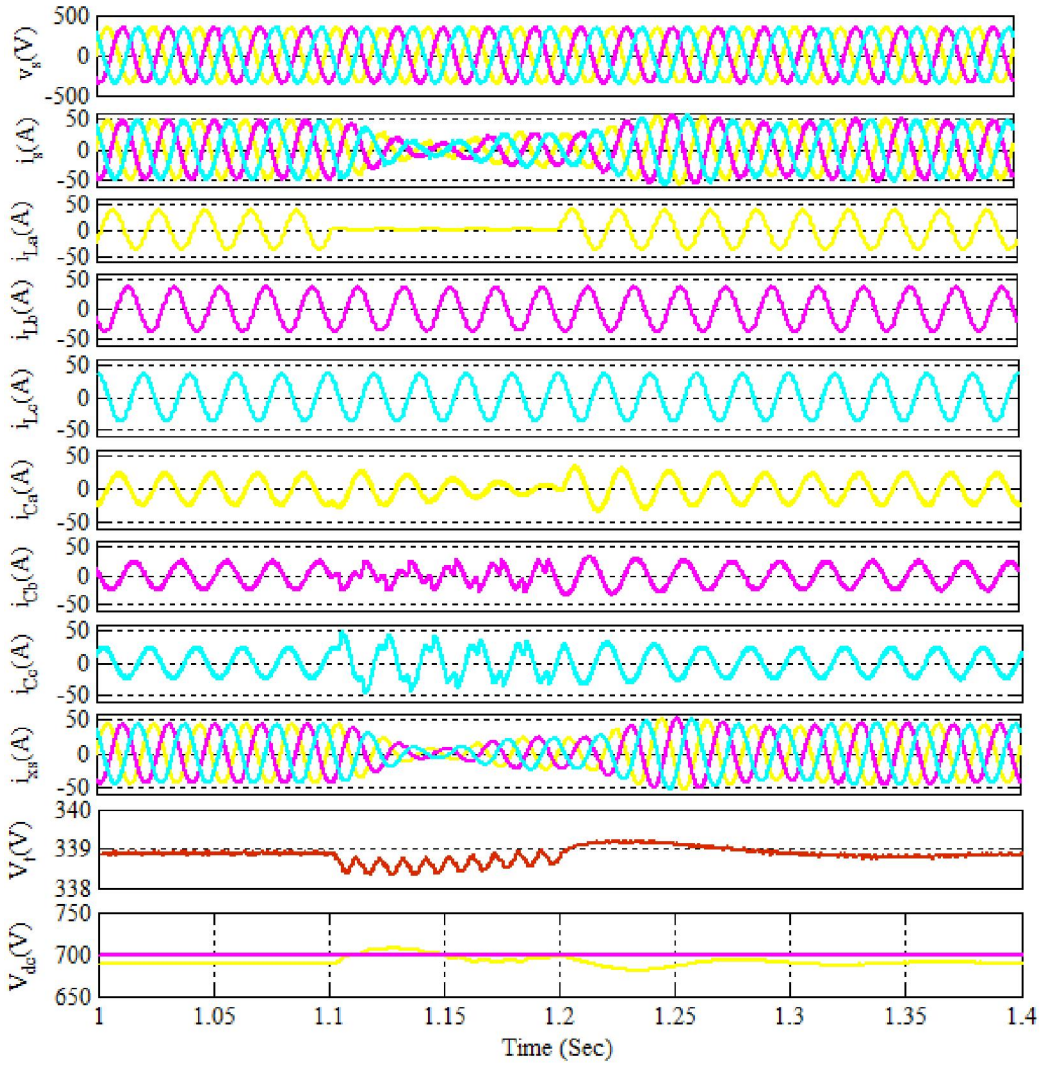


Fig. 4.7 Simulated performance of DSTATCOM at linear load in PFC mode

Fig. 4.8 shows the performance parameters of phase 'a' source voltage (v_{sa}), source current (i_{sa}) and load current in PFC mode of DSTATCOM. The source voltage (v_{sa})

and source current (i_{sa}) are found in same phase, whereas, the load current (i_{La}) of phase 'a' lags the source voltage (v_{sa}).

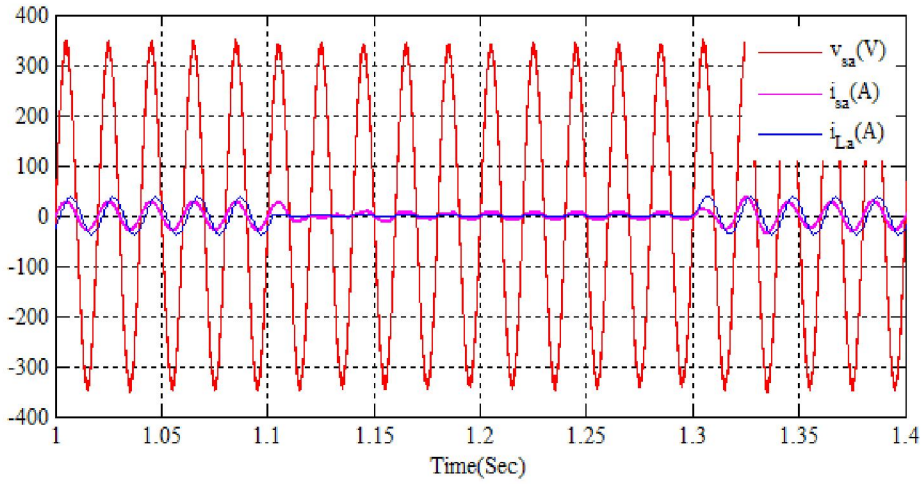


Fig. 4.8 Performance parameters of phase 'a' in PFC mode of DSTATCOM

4.7.2 *Case Study II*: Performance of DSTATCOM in ZVR Mode

The performance of DSTATCOM at linear and nonlinear loads under balanced/unbalanced conditions is discussed here:

4.7.2.1 Simulation results at linear load conditions

Fig. 4.9 shows the performance of DSTATCOM in ZVR mode, the deviated AC bus voltage (V_t) under unbalanced linear load (t=1.1s to t=1.3s) conditions at PCI is regulated to reference level due to the action of the PI controller. In this mode, the estimated fundamental reference source current is the sum of the extracted fundamental active and reactive power current components. The reactive current compensation at PCI took place using PWM switching of DSTATCOM. The regulated amplitude of the AC bus voltage (V_t), source voltages (v_s), source currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), injected compensating current components (i_{Ca}, i_{Cb}, i_{Cc}), estimated fundamental reference source currents, respectively, are also shown in Fig. 4.9.

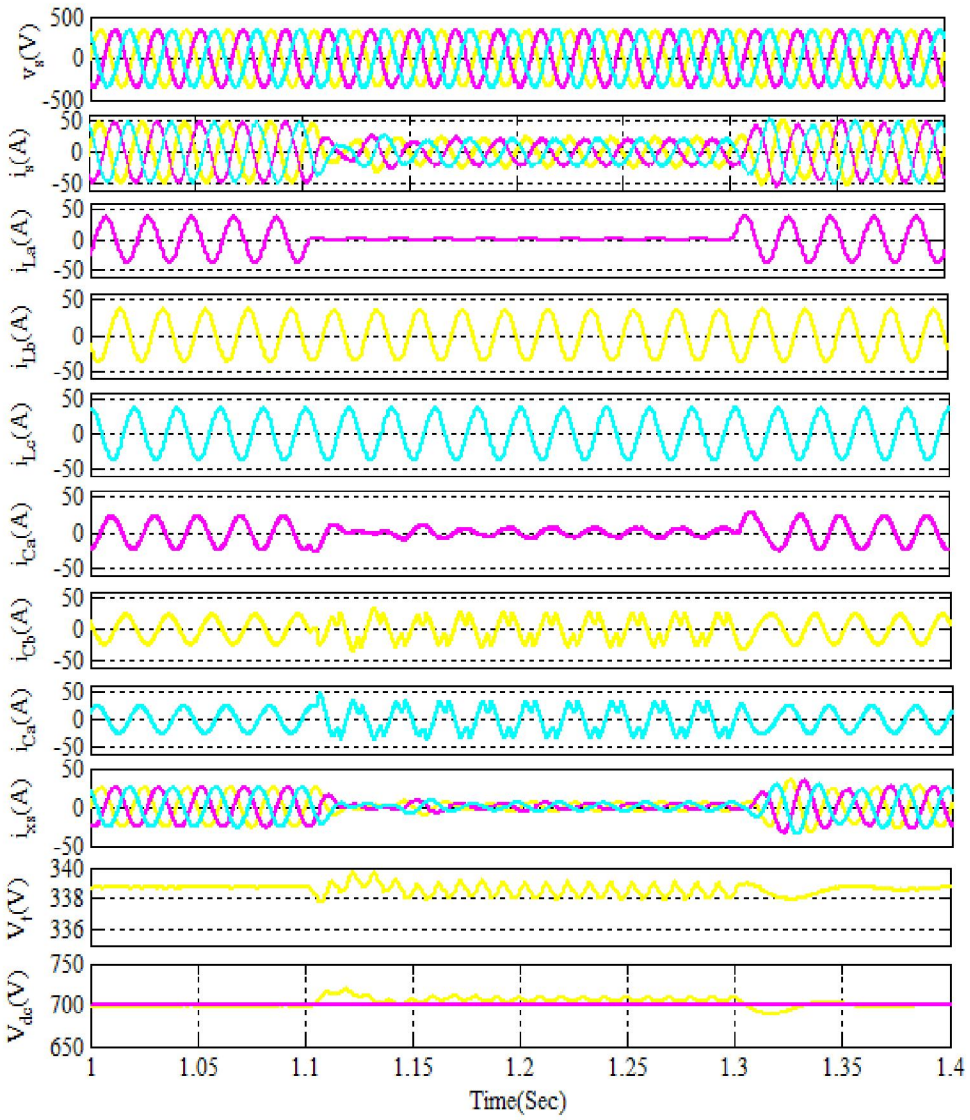


Fig. 4.9 Simulated performance of DSTATCOM at linear load in ZVR mode

4.7.2.2 Simulation results at nonlinear load conditions

Fig. 4.10 shows the performance of DSTATCOM in ZVR mode under nonlinear load. These results present waveforms of PCI voltages (v_s), supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_{Ca}, i_{Cb}, i_{Cc}), reference source currents (i_{xs}), AC bus voltage amplitude (V_t) and DC bus voltage (V_{dc}), respectively.

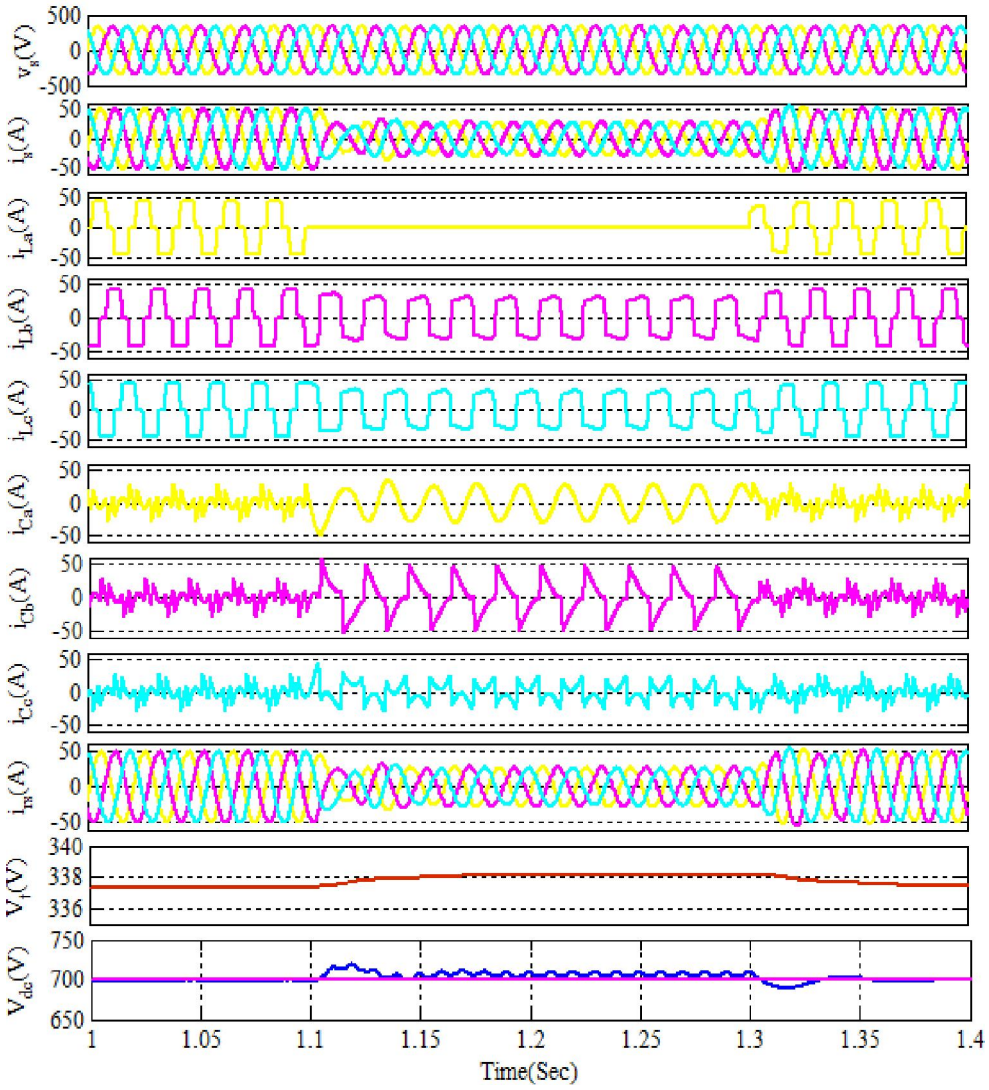


Fig. 4.10 Simulated performance of DSTATCOM at nonlinear load in ZVR mode

Supply currents are observed balanced and sinusoidal during steady state (before t=1.1s) and at unbalance load (t=1.1s to t=1.3s). Due to the action of PI controller, the voltage at DC bus of VSC is regulated at the reference value of 700V. The amplitude of AC bus voltage (V_t) at PCC is regulated to reference level under steady state and dynamic performance of DSTATCOM in ZVR mode.

Figs. 4.11 shows various intermediate signals of the proposed MLPNN algorithm at input, hidden and output layers for the extraction of reactive power current component from linear load current of phase 'a'. The intermediate signals are weighted neuron

component (w_{qa1}) of reactive current, its coefficient (u_{qa1}) of phase 'a' and weighted mean (w_{q1}) at hidden layer after scaling. The weighted active neuron (w_{qa2}) its coefficient (u_{qa2}) of phase 'a' and the weighted mean active neuron (w_q) at the output layer, weighted reactive power (w_{qt}) of DSTATCOM, and extracted weighted reactive power current component (w_{sq}) and the estimated reference fundamental current component (i_{xsa}) of phase 'a' are shown in Fig. 4.11. With the help of the proposed fast learning of the MLPNN algorithm, reactive power current component (i_{xsq}) of fundamental reference source currents are estimated for all the phases.

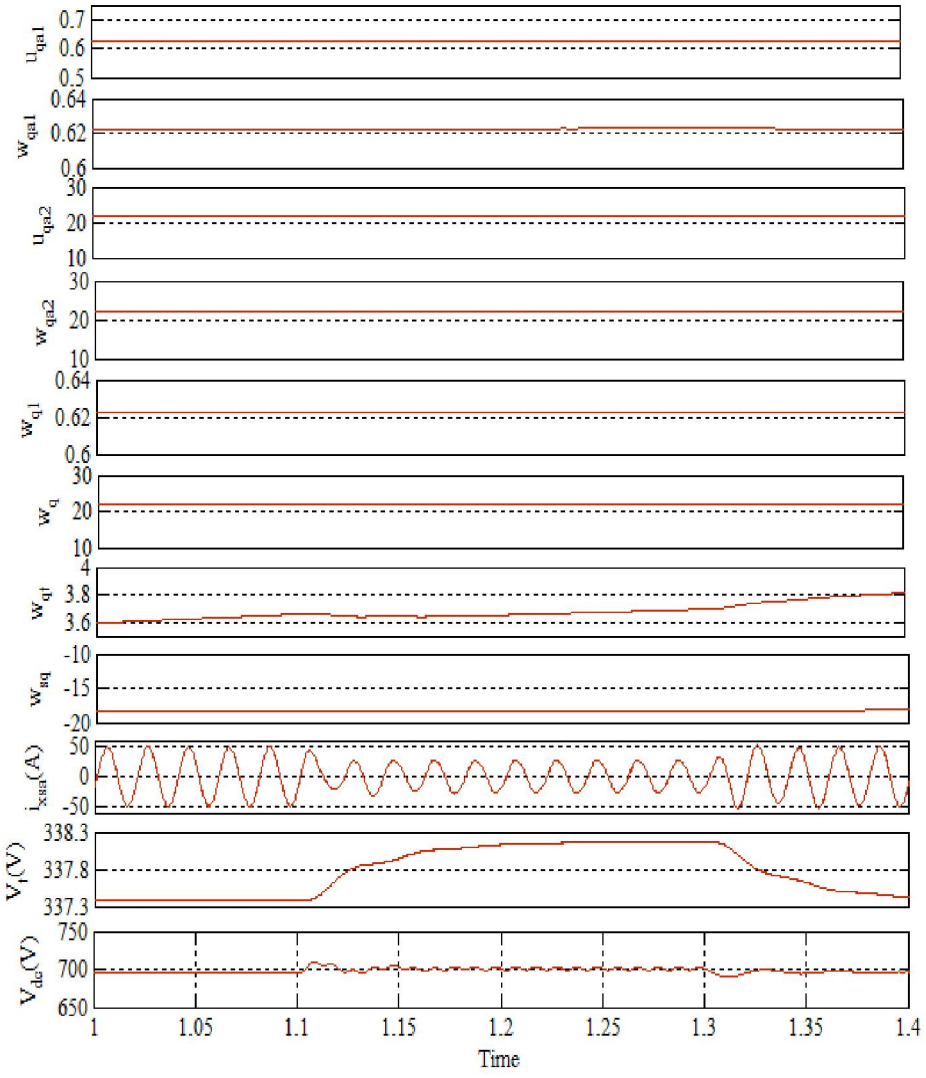


Fig. 4.11 Intermediate signals of MLPNN algorithm in ZVR mode

These extracted reactive power current components are further used to estimate the fundamental reference source currents (i_{xs}). Under unbalance load (t=1.1s to t=1.3s) conditions, the deviated amplitude of the AC bus voltage (V_t) is maintained to the reference level by the action of PI controller, which is tuned using Ziegler Nichols method. The DSTATCOM switching has been taken place by PWM pulses generated from HCC, as their input is error of the fundamental source currents and the estimated reference source currents. The injected reactive current components regulate the deviation of the AC bus voltage, which shows the action of the DSTATCOM in ZVR mode.

The harmonic spectra of phase 'a' voltage (v_{sa}), current (i_{sa}) and load current (i_{La}) are obtained from the captured waveforms, and their THDs are 1.72%, 2.08% and 24.20%, which are shown in Figs.4.12 (a)-(c).

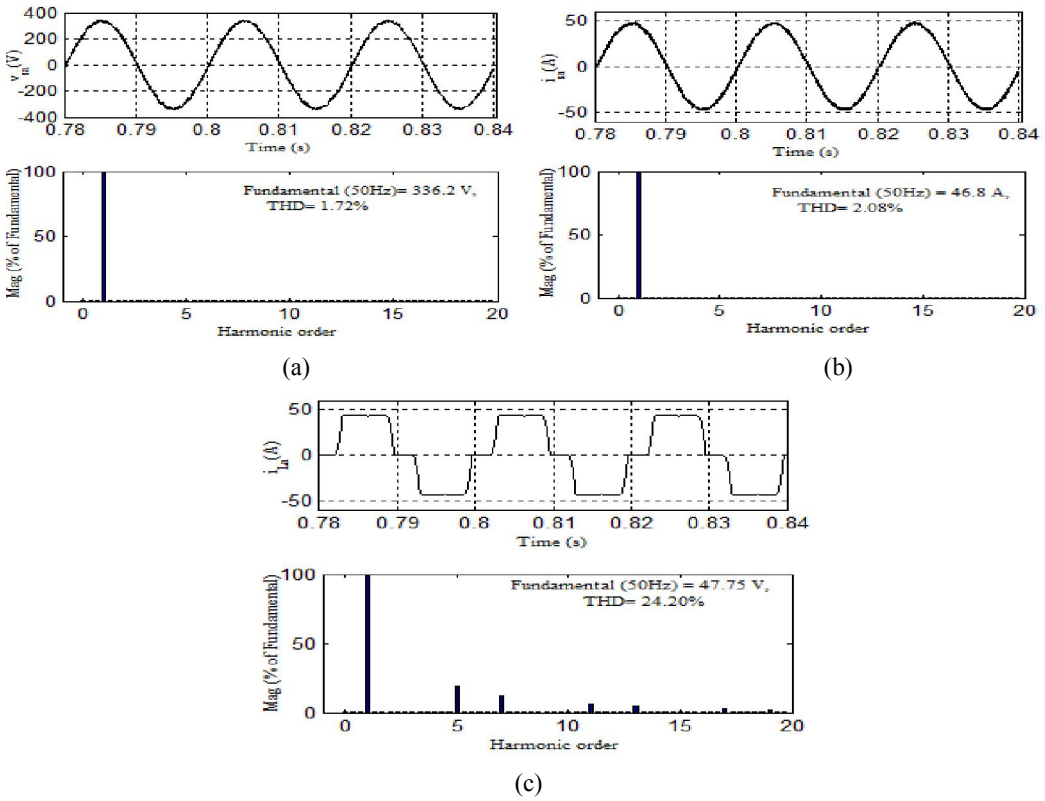


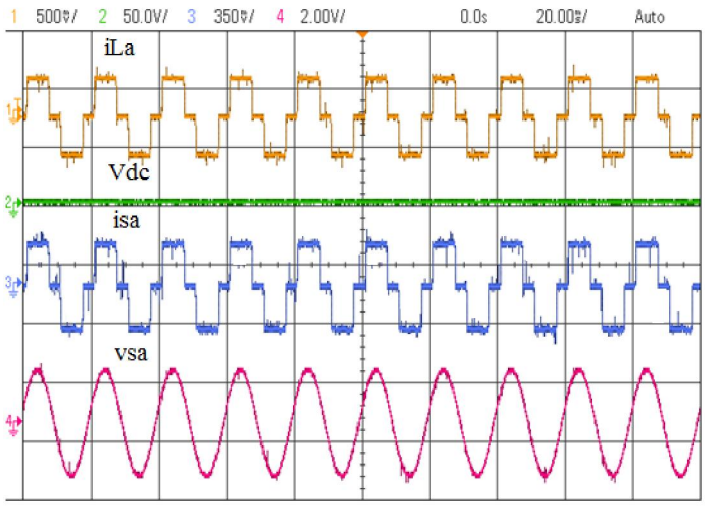
Fig. 4.12 Waveforms and harmonic spectra of (a) PCI voltage (b) Source current (c) Load current, of phase 'a'

The obtained results of THDs are also compared with SBP in Table 4.2. The THDs of PCI voltage and supply current are within 5%, a limit of an IEEE standard. From the obtained results, it is proved that the reactive power current compensation from DSTATCOM using MLPNN algorithm is quite effective for the improvement of power quality in three-phase distribution system under dynamic operation of nonlinear load in ZVR mode.

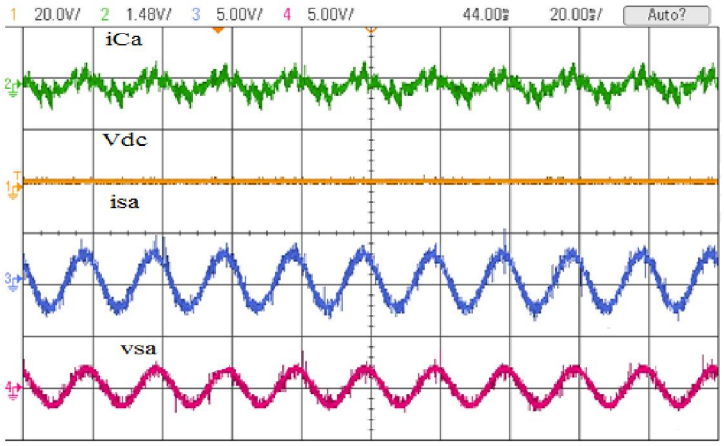
From these results, it is revealed that the proposed algorithm is quite effective in the improvement of power quality in three-phase distribution system under dynamic operation of nonlinear and linear loads in PFC and ZVR modes.

4.7.3 Experimental Results in PFC Mode

The experimental performance of DSTATCOM in PFC mode under nonlinear load is shown in Fig 4.13. Fig. 4.13 (a) shows load current (i_{La}), DC link voltage (V_{dc}), source current (i_{sa}), which is same as load current before compensation. Fig. 4.13 (b) shows compensating current (i_{Ca}), DC link voltage (V_{dc}), source current (i_{sa}) and source voltage (v_{sa}) of phase 'a' after compensation.



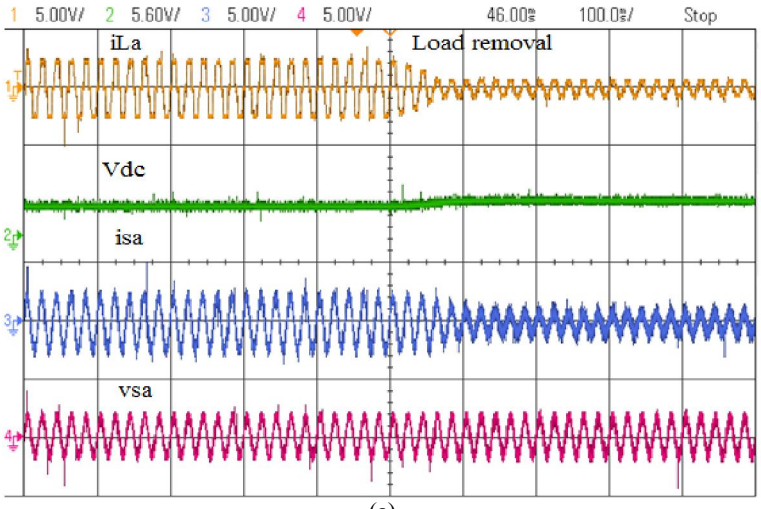
(a)



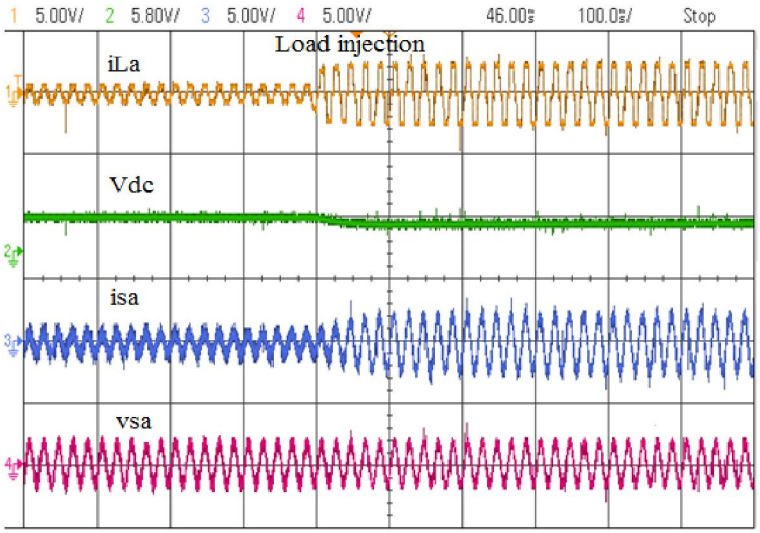
(b)

Fig. 4.13 (a) Load current (i_{La}), dc link voltage (V_{dc}), source current (i_{sa}) and source voltage (v_{sa}) of phase 'a' when DSTATCOM is in OFF state (b) Compensating current (i_{Ca}), dc link voltage (V_{dc}), source current (i_{sa}) and source voltage (v_{sa}) of phase 'a' when DSTATCOM is in ON state

Figs. 4.14 (a) and (b) show the performance parameters under unbalanced load condition at nonlinear load. The DC bus voltage of DSTATCOM is deviated from its reference value when load of phase 'a' is suddenly removed and injected. It has been observed that the parameters of phase 'a' including source voltage, source current and load current remain balanced in all conditions.



(a)



(b)

Fig. 4.14 Dynamics of unbalancing load by (a) Load removal (b) Injecting load, in phase 'a'

Table 4.2 shows the performance parameters of DSTATCOM for MLPNN and SBP algorithms under nonlinear load conditions in PFC and ZVR modes.

Table 4.2 Performance parameters of DSTATCOM

Operating mode	Performance parameters	Nonlinear load (as 3-phase diode rectifier module) with R and L	
		MLPNN	Standard BP
PFC mode	PCI voltage (V),%THD	336.2V, 1.66%	237.02V, 2.86%
	Supply current (A),%THD	46.83 A, 2.06%	32.17A, 2.94%
	Load current (A),%THD	47.82 A, 24.14%	32.58A, 24.82%
ZVR mode	PCI voltage (V),%THD	336.2 V, 1.72%	239.63V, 3.09%
	Supply current (A),%THD	46.80 A, 2.08%	33.82A, 2.99%
	Load current (A),%THD	47.75 A, 24.20%	32.94A, 24.94%
	DC bus voltage (V)	700 V	700V

4.8 CONCLUSIONS

A new fast training BP algorithm for MLPNN based on linear and nonlinear error signals is proposed. Both these error signals are considered in a generalized least mean square (LMS) algorithm to form the optimization criterion that minimizes the sum of the squares of the errors. The weight updating rule is derived by applying gradient descent method to the optimization criterion. The fast learning of MLPNN is achieved with the additional linear error signal term added to the LMS optimization criterion. The linear error signal term depends on the value of convergence coefficient 'λ' taken into account. For a suitable choice of the learning parameters, the optimal value of the convergence coefficient 'λ' is determined via rank convergence series analysis and asymptotic constant error values, which results in fast convergence of training BP for feedforward MLPNN network. The proposed algorithm is implemented on control operation of DSTATCOM for PFC and ZVR modes under nonlinear load. The results have proved the improvement of power quality with reactive power compensation, load balancing and harmonics elimination on a three-phase distribution system. THDs of source voltages and source currents are found within 5%, a limit of an IEEE standard.

CHAPTER 5

GENERALIZED NEURAL NETWORK BASED CONTROL ALGORITHM FOR DSTATCOM

5.1 INTRODUCTION

In this chapter, a new concept is presented to control a distribution static compensator (DSTATCOM) based on generalized neural network (GNN) in a 3-phase power distribution system. Artificial neural network (ANN) based controllers play the vital role in the improvement of the performance of DSTATCOM. However, their applications are limited due to the increased complexity as well as the computational time. The proposed GNN algorithm is a combination of Gaussian, sigmoidal and linear transfer functions within a layer to improve the control strategy of DSTATCOM. This algorithm estimates the amplitude of the active power and reactive power current components of the load currents for harmonics elimination and reactive power compensation by the DSTATCOM. The model of algorithm is developed in MATLAB. The case studies validate its superiority over ANN based control algorithms. The proposed method needs less number of training patterns and unknown weights compared to other algorithms, which reduce the complexity and the computational time. It also improves the performance of DSTATCOM due to estimation of the weights and its learning online. This shows the main merits of this proposed GNN algorithm. Its other inherent advantages are ease of design, robustness and its adaptivity with dynamics of the load at utility end.

5.2 THREE PHASE DISTRIBUTION SYSTEM TEST MODEL

A 3-ϕ distribution static compensator configuration is shown in Fig. 5.1. It comprises of voltage source (v_s) with impedance (Z_s) feeding to an uncontrolled rectifier with R_L and X_L as nonlinear load. The demand of reactive power and unbalanced currents

of loads at PCI are compensated by DSTATCOM for power quality improvement. The VSC (Voltage Source Converter) of DSTATCOM is placed using interfacing inductors (L_f) at PCI and it is operating at high switching frequency, causing noise, which is suppressed by a ripple filter consisting of a resistance R_r and a capacitance C_r, respectively.

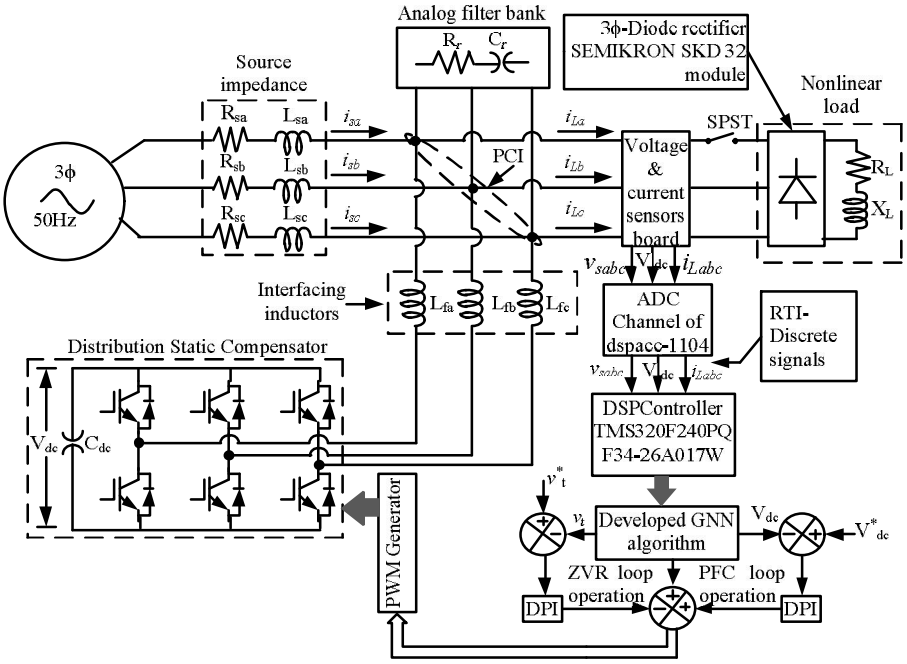


Fig. 5.1 DSTATCOM for three phase distribution system

Table 5.1 Parameters of developed 3-ϕ distribution system

Serial No.	Components of the test system model	Specifications
1.	AC Grid supply	3 ϕ, 415 V, 50 Hz,
2.	Impedance of source (Z_s)	(0.02+j0.34)Ω
3.	Ripple filter (R_f and C_f)	5 Ω and 30 µF
4.	Interfacing inductor ($L_{fa} = L_{fa} = L_{fc}$)	3.35 mH
5.	IGBT based Voltage source converter (VSC)	3 ϕ, 415 V
6.	Linear load (series of inductance and resistance)	25 kVA, 0.8 Pf (lagging)
7.	3 ϕ uncontrolled rectifier module with R_L and X_L	(12+j45) Ω
8.	DC link capacitance of VSC (C_{dc})	15 mF
9.	Reference DC link voltage (V_{dc}^*)	700 V
10.	Gains for DC link DPI controller K_{pdc} and K_{idc}	2.78 and 0.06
11.	Gains for AC bus DPI controller $K_{pt}$and K_{it}	0.02 and 0.21

The parameters of the test system are listed in Table-5.1. Sensor circuits at PCI are used to sense all required parameters like PCI voltages ($v_{\mathrm{sa}}, v_{\mathrm{sb}}, v_{\mathrm{sc}}$), currents ($i_{\mathrm{sa}}, i_{\mathrm{sb}}, i_{\mathrm{sc}}$), DC-link voltage ($V_{\mathrm{dc}}$) of DSTATCOM and load currents ($i_{\mathrm{La}}, i_{\mathrm{Lb}}, i_{\mathrm{Lc}}$). A switch is placed between PCI and the load of a phase for dynamic operation. The DSTATCOM injects the compensating currents ($i_{\mathrm{Ca}}, i_{\mathrm{Cb}}, i_{\mathrm{Cc}}$) at PCI.

5.3 FUNDAMENTAL CONCEPT OF GENERALIZED NEURAL NETWORK (GNN)

The power distribution system has to be made to deliver effective real power with controlled harmonics to end users and utilities [121]. The distribution system integrated with DSTATCOM is effectively examined to control harmonics, to meet the reactive power demand of load as well as for voltage regulation under balanced and unbalanced loads [53]. The switching of power electronics devices increases the harmonics order while electric machines demand reactive power at utility end, which result into the deterioration of power quality in a distribution system [58]. The custom power devices like DSTATCOM, dynamic voltage restorer (DVR) and unified power quality conditioner (UPQC) are used to mitigate the power quality problems [121]. However, the nonlinearity of source currents caused by load currents at the distribution level, has been mitigated by injecting current components at PCI by the DSTATCOM [121]-[127]. The compensation current components at PCI using DSTATCOM are provided through the control algorithms reported in [121]-[131]. Therefore, a substantial research is carried out by researchers for improvement in the performance of DSTATCOM with the help of control algorithms on the aspects of computation time, reliability and simplicity. A numbers of control algorithms based on ANN, are available in the literature under dynamic conditions of nonlinear/linear loads [121]-[134].

Ahmad *et al.* [129] have presented fast learning of BP based control algorithm to enhance the performance of the shunt compensator. Janpong *et al.* [134] have presented a literature review of neural network (NN) applications for the shunt active power filters. Radzi *et al.* [135] have reported NN and bandless hysteresis approach for reduction of harmonics using active power filter. Vazquez *et al.* [136] have discussed control of APF using NN based control algorithm. Further, Chauhan *et al.* [137] have reported different schemes for generation of reference current of a shunt compensator. Applications of NN based control algorithms and their comparison for improvement in the performance of DSTATCOM in the distribution system are reported in [138]-[140]. These algorithms have complexity in their learning, which require more computational time. To reduce this complexity and computational time, the control strategies based on generalized neuron (GN) model, are developed in [141]-[145].

ANN based algorithms reported in the literature, have used back propagation training with slow convergence and conductance estimation to improve the control functions of DSTATCOM [121]-[141]. However, the fast convergence of ANN trained network has improved the performance of DSTATCOM more effectively compared to conventional and adaptive methods [134]. The convergence rate of such algorithms could not meet the required control functions of DSTATCOM as per dynamics of load due to its predefined values. ANN based control algorithms have only Gaussian or sigmoidal transfer function to train the network to cope up with the dynamics of load. Saribulut *et al.* [127] have reported a combination of ANN and discrete-fuzzy logic based controller for improving the performance of an active power filter. Recently, ANN and fuzzy set based control algorithms for DSTATCOM have been proposed for improving its performance. The closed loop control algorithm becomes

complicated in terms of computation time for deriving the control signals. Both these approaches have pros and cons. The integration of both techniques has resulted into GNN model. This model not only reduces training time but it also improves the dynamics capabilities of ANN, which further enhances the performance of DSTATCOM [141]-[145].

The applications of GNN in electrical machines, load forecasting, solar energy estimation, load frequency control, power system stabilizer and aircraft landing control system, are becoming the attraction to provide accuracy in the estimation due to its combinational neuron structure [142]-[144]. However, the application of GNN in DSTATCOM is rarely available in the literature. A control algorithm based on GNN is proposed to make fast switching of DSTATCOM to enhance the power quality in the distribution system. The proposed algorithm is used for two case studies for balanced /unbalanced conditions of linear and nonlinear loads. Power factor correction (PFC) mode of DSTATCOM is used for power quality improvement under linear/nonlinear loads. While zero voltage regulation (ZVR) mode of DSTATCOM is used to regulate the AC bus voltage at PCI under dynamics of liner/nonlinear loads. Both these two modes of PFC and ZVR may not be achieved, simultaneously. The obtained THDs (Total Harmonic Distortions) of supply currents validate the performance improvement of DSTATCOM with proposed algorithm for both case studies of PFC and ZVR.

5.4 MATHEMATICAL MODELING OF GNN ALGORITHM

A proper study of the DSTATCOM operation, especially when it comes to transients and unbalanced linear/nonlinear loads, requires effective mathematical model of control. The GNN based control of DSTATCOM in three-phase distribution system represents all the equations that describe the relationships for transients and

unbalanced linear/nonlinear loads. The mathematical model represents all the equations that describe the relationships between power current components and the weights quantities. The model equations stand on summation and product neurons of the summation GNN. A generalized neuron (GN) model for classification, nonlinear and transients estimation of loads application is discussed here. Further, a summation neuron model of GN, called summation GN is discussed here for chaotic loads prediction. At the utility end, a wide class of complex nonlinear loads when one has no complete model information, or even one considers the load as a black-box. This study uses a BP algorithm for fast and optimal training of GN. The compactness of GN has smaller numbers of trainable weights than in MLP, and the convergence speed of GN over BP as a training algorithm is exploited in this chapter. As an MLP training algorithm, GN has been shown to outperform MLP in terms of the speed and the quality of training [142]-[145]. A small number of trainable weights make GN a compact structure suitable for real time hardware implementation on simple hardware platforms such as DSP processor based on dSPACE-1104. A typical neuron in GN uses summation aggregation functions, and hard-limiter linear activation functions.

5.4.1 Estimation of Weights for Active Power Current Components

The error E_{pj} is obtained by comparing actual output (O_{pj}) with the desired output (d) of GNN. Using the gradient descent with momentum learning rule, the error E_{pj} is minimized to train and strengthen the network connections with the modified weights. By reverse pass through backpropagation algorithm, the error E_{pj} is minimized and it is defined as,

$$E_{pj} = \left(d - O_{pj}\right) \tag{5.1}$$

The convergence of all the patterns is obtained by summing the squared error, which is given as,

$$E_{pj} = 0.5 \sum_{j=1}^{3} \left(d - O_{pj}\right)^2 \tag{5.2}$$

Where 'j' denotes the phase, 0.5 is taken as multiplier to simplify the calculations. The weight linked with Σ_1 and Σ part of the summation GNN model is updated as,

$$W_{pj}(n) = W_{pj}(n-1) + \Delta W_{pj} \tag{5.3}$$

Where $\Delta W_{pj} = \eta \delta_k \left(O_{\Sigma 1\mathrm{p}} - O_{\pi\mathrm{p}}\right) i_{\mathrm{Lj}} + \alpha W_{pj}(n-1)$, and δ_k is the sum of the errors of all the phases given as,

$$\delta_k = \sum_{j=1}^{3} \left(d - O_{pj}\right).$$

The weight linked with Σ_1 neuron of the GNN model is updated as,

$$w_{\Sigma 1pj}(n) = w_{\Sigma 1pj}(n-1) + \Delta w_{\Sigma 1pj} \tag{5.4}$$

Where $\Delta w_{\Sigma 1pj} = \eta \delta_{\Sigma 1pj} i_{\mathrm{Lj}} + \alpha w_{\Sigma 1pj}(n-1)$ and

$$\delta_{\Sigma 1pj} = \sum_{j=1}^{3} \delta_k \, W_{pj}\left(1 - O_{\Sigma 1\mathrm{p}}\right) * O_{\Sigma 1\mathrm{p}}.$$

The weight linked with π neuron of the GNN model is updated as,

$$w_{\pi\mathrm{p}}(n) = w_{\pi\mathrm{p}}(n-1) + \Delta w_{\pi\mathrm{p}}(n) \tag{5.5}$$

Where $\Delta w_{\pi\mathrm{p}} = \eta \delta_{\pi pj} i_{\mathrm{Lj}} + \alpha w_{\pi\mathrm{p}}(n-1)$ and

$$\delta_{\pi pj} = \sum_{j=1}^{3} \delta_k \left(1 - W_{pj}\right) * \left(-2 * \pi_p\right) * O_{\pi p}.$$

Where α and η are momentum factor and learning rate, respectively, to speed up the convergence, and their values are taken abruptly between 0 and 1. The weights $w_{\Sigma 1p}$ of Σ_1 and $w_{\pi\mathrm{p}}$ of π part of the GNN model obtained from eqns. (5.4) and (5.5) have been multiplied by in-phase unit templates (u_{ap}, u_{bp}, u_{cp}) in order to obtain the

weights for the extraction of active power current components from the load currents and are expressed as,

$$W_{\Sigma 1\mathrm{pa}} = w_{\Sigma 1pa} * u_{ap}, \quad W_{\Sigma 1\mathrm{pb}} = w_{\Sigma 1\mathrm{pb}} * u_{bp}, \quad W_{\Sigma 1\mathrm{pc}} = w_{\Sigma 1\mathrm{c}} * u_{cp} \tag{5.6}$$

$$W_{\pi\mathrm{pa}} = w_{\pi\mathrm{pa}} * u_{ap}, \quad W_{\pi\mathrm{pb}} = w_{\pi\mathrm{pb}} * u_{bp}, \quad W_{\pi\mathrm{pc}} = w_{\pi\mathrm{pc}} * u_{cp} \tag{5.7}$$

5.4.2 Estimation of Weights for Reactive Power Current Components

A comparison is made between the output of GN model and the desired output (d) to find the error E_{qj}. The sum of squares of errors is used to obtain the convergence pattern of the network in order to train and strengthen the network connections with the modified weights. By reverse pass through backpropagation algorithm, the error E_{qj} is minimized and it is defined as,

$$E_{qj} = \left(d - O_{qj}\right) \tag{5.8}$$

The convergence of the entire pattern is obtained by summing the total mean square error (MSE), which is given as,

$$E_{qj} = 0.5 \sum_{j=1}^{3} \left(d - O_{qj}\right)^2 \tag{5.9}$$

Where 'j' denotes the phase, 0.5 has been taken as multiplier for simplification of the calculations. The weight linked with Σ_1 and Σ part of the summation GNN model, is updated as,

$$W_{qj}(n) = W_{qj}(n-1) + \Delta W_{qj} \tag{5.10}$$

Where $\Delta W_{qj} = \eta \delta_{\boldsymbol{k1}} \left(O_{\Sigma q} - O_{\pi q}\right) i_{Lj} + \alpha W_{qj}(n-1)$ and

$$\delta_{k1} = \sum_{j=1}^{3} \left(d - O_{qj}\right)$$

The weight linked with Σ_1 neuron of the GNN model, and it is updated as,

$$w_{\Sigma 1qj}(n) = w_{\Sigma 1qj}(n-1) + \Delta w_{\Sigma 1qj} \tag{5.11}$$

Where $\Delta w_{\Sigma 1qj} = \eta \delta_{\Sigma 1qj} i_{Lj} + \alpha w_{\Sigma 1qj}(n-1)$, and

$$\delta_{\Sigma 1qj} = \sum_{j=1}^{3} \delta_{k1} W_{qj} \left(1 - O_{\Sigma 1q}\right) * O_{\Sigma 1q}.$$

The weight linked with π neuron of the GNN model is updated as,

$$W_{qj}(n) = W_{qj}(n-1) + \Delta W_{qj} \tag{5.12}$$

Where $\Delta W_{qj} = \eta \delta_{\pi qj} i_{Lj} + \alpha W_{qj}(n-1)$ and

$$\delta_{\pi qj} = \sum_{j=1}^{3} \delta_{k1} \left(1 - W_{qj}\right) * \left(-2 * \pi_q\right) * O_{\pi q}.$$

Where α and η are momentum factor and learning rate to speed up the convergence, and their values are taken abruptly between 0 and 1. The weights $w_{\Sigma 1q}$ of Σ_1 and $w_{\pi q}$ of π part of the GN model obtained from eqns. (5.11) and (5.12), are multiplied by quadrature unit templates (u_{aq}, u_{bq}, u_{cq}) in order to obtain the weights for the extraction of active power current components from the load currents and are expressed as,

$$W_{\Sigma 1qa} = w_{\Sigma 1qa} * u_{aq}, \quad W_{\Sigma 1qb} = w_{\Sigma 1qb} * u_{bq}, \quad W_{\Sigma 1qc} = w_{\Sigma 1qc} * u_{cq} \tag{5.13}$$

$$W_{\pi qa} = w_{\pi qa} * u_{aq}, \quad W_{\pi qb} = w_{\pi qb} * u_{bq}, \quad W_{\pi qc} = w_{\pi qc} * u_{cq} \tag{5.14}$$

5.5 GNN BASED CONTROL ALGORITHM FOR DSTATCOM

In order to develop the model to extract fundamental active power current components from load currents (i_{La}, i_{Lb}, i_{Lc}) using GNN, which comprises of summation (Σ_1) and product (π) neurons with their unknown weights ($w_{\Sigma 1}$) and (w_{π}), respectively. The outputs of the neurons are summed up with 'W' weight related to Σ_1 and Σ, which give the resultant output of the GNN. The total number of weights required in the developed model is twice the number of input plus one, which are obtained online through training.

5.5.1 Estimation of Amplitude of Active Current Components

A summation type GNN model network for amplitude estimation of active power current component of phase 'a' is shown in Fig. 5.2. The sensed load currents ($i_{\mathrm{La}}, i_{\mathrm{Lb}}, i_{\mathrm{Lc}}$) are the number of input applied to summation (Σ_1) and product (π) neurons with their unknown weights ($w_{\Sigma 1\mathrm{pa}}, w_{\Sigma 1\mathrm{pb}}, w_{\Sigma 1\mathrm{pc}}$) and ($w_{\pi\mathrm{pa}}, w_{\pi\mathrm{pb}}, w_{\pi\mathrm{pc}}$), respectively. The outputs of the neurons are summed up with 'W_{pa}' weight by linear function that relates to Σ_1 and Σ gives GNN output for phase 'a' and likewise other phases outputs are obtained. In order to estimate the active power current component amplitude, in-phase templates (u_{ap}, u_{bp}, u_{cp}) are used as the reference weights multiplier to find the actual weights of Σ_1 and π neurons, respectively.

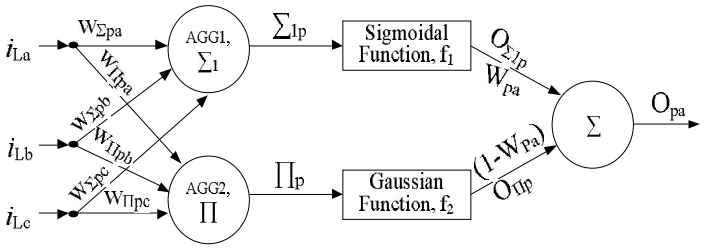


Fig. 5.2 Summation type GNN model for amplitude estimation of active current component of phase 'a'

The aggregation function of Σ_1 of the forward calculations for phase 'a' is given as,

$$\Sigma_{1\mathrm{p}} = i_{\mathrm{La}} w_{\Sigma 1\mathrm{pa}} + i_{\mathrm{Lb}} w_{\Sigma 1\mathrm{pb}} + i_{\mathrm{Lc}} w_{\Sigma 1\mathrm{pc}} + \Sigma_{bias} \tag{5.15}$$

Where Σ_{bias} is the initial bias of Σ_1 network neuron, while the output is threshold using sigmoidal transfer function, which is defined as,

$$O_{\Sigma_1 p} = f_1(\Sigma_{1p}) = \frac{1}{1 + e^{-\lambda_\Sigma * \Sigma_{1P}}} \tag{5.16}$$

The aggregation function of π part of the forward calculations is given as,

$$\pi_{\mathrm{p}} = i_{\mathrm{La}} w_{\pi\mathrm{pa}} * i_{\mathrm{Lb}} w_{\pi\mathrm{pb}} * i_{\mathrm{Lc}} w_{\pi\mathrm{pc}} * \pi_{bias} \tag{5.17}$$

Where π_{bias} is the initial bias of π part network neuron, while the output is threshold using Gaussian transfer function, which is defined as,

$$O_{\pi p} = f_2(\pi_p) = e^{-\lambda_{\pi} * \pi_p{}^2} \tag{5.18}$$

Where λ_{Σ} and λ_{π} are gain scale factors of Σ_1 and π part network neuron. In this case, the gain factors are unity. The aggregation and transfer functions eqns. (5.15)-(5.18) are general equations for all the three phases.

The outputs of summation type GNN, are expressed through linear transfer functions for all phases and are given as,

$$O_{pa} = O_{\pi p}(1 - W_{pa}) + O_{\Sigma 1 p} W_{pa} \tag{5.19}$$

$$O_{pb} = O_{\pi p}(1 - Wp_b) + O_{\Sigma 1 p} W_{pb} \tag{5.20}$$

$$O_{pc} = O_{\pi p}(1 - W_{pc}) + O_{\Sigma 1 p} W_{pc} \tag{5.21}$$

Where W_{pa}, W_{pb} and W_{pc} are weights that relate Σ_1 and Σ neurons of GNN, respectively. The output of GNN lies between 0 and 1. To obtain the actual active power current component; the outputs are multiplied by a scale factor 'K', which is measured from the load current.

The load balancing is performed by taking average amplitude of the weighted value of GNN neuron. The mean active power current components (w_{Lp}) amplitude is obtained as,

$$w_{Lp} = \frac{(O_{pa} + O_{pb} + O_{pc})}{3} \tag{5.22}$$

An independent DC voltage control is carried out by placing a discrete proportional integrator (DPI) as controller over which the error V_{de} of reference V_{dc}^* and sensed V_{dc} DC link voltage is passed to estimate the loss of active power current component (w_{pdc}) of DSTATCOM. The controller output at k^{th} instant sample is defined as,

$$w_{pdc}(k) = w_{pdc}(k-1) + k_{pd}\{V_{de}(k) - V_{de}(k-1)\} + k_{id} V_{de}(k) \tag{5.23}$$

Where $V_{de} = V_{dc}^* - V_{dc}$, k_{id} and k_{pd} are integral and proportional gains of the DPI controller, which is added with w_{Lp}.

The net active power current components amplitude is given as,

$$I_{\mathrm{Lp}} = w_{\mathrm{pdc}} + w_{\mathrm{Lp}} \tag{5.24}$$

The reference fundamental net active power current component of the source currents are obtained with the help of eqn. (5.24) and in phase unit templates estimated from the AC bus voltage amplitude for PFC mode of operation in an indirect current control of the VSC based DSTATCOM.

The estimated amplitude of active power current components is multiplied with the in-phase templates that result into the fundamental reference active power current components. The in-phase templates are estimated with the help of sensed phase voltages ($v_{\mathrm{sa}}, v_{\mathrm{sb}}, v_{\mathrm{sc}}$) at PCI, the amplitude of phase voltages (V_{ta}, V_{tb} and V_{tc}) are calculated as,

$$V_{ta} = \sqrt{\left[2\left(\frac{v_{sa}}{2}\right)^2\right]}, V_{tb} = \sqrt{\left[2\left(\frac{v_{sb}}{2}\right)^2\right]}, V_{tc} = \sqrt{\left[2\left(\frac{v_{sc}}{2}\right)^2\right]} \tag{5.25}$$

Where $v_{\mathrm{sa}} = V_{ta}\sin\omega t$, $v_{\mathrm{sb}} = V_{tb}\sin\left(\omega t - {}^{2\pi}/_{3}\right)$ and $v_{\mathrm{sc}} = V_{tc}\sin\left(\omega t - {}^{4\pi}/_{3}\right)$.

The AC voltage amplitude at PCI is defined as,

$$v_{tp} = \sqrt{\left[\frac{2({v_{sa}}^2 + {v_{sb}}^2 + {v_{sc}}^2)}{3}\right]} \tag{5.26}$$

There are ripples in v_{tp}, which is induced from load fundamental negative sequence voltage components. It is processed out through low pass filter (LPF) and hence positive sequence fundamental voltage amplitude V_t at PCI is obtained. The in-phase unit templates of v_{sa}, v_{sb}, and v_{sc} are obtained as [121],

$$u_{ap} = \frac{v_{\mathrm{sa}}}{V_t}, u_{bp} = \frac{v_{\mathrm{sb}}}{V_t}, u_{cp} = \frac{v_{\mathrm{sc}}}{V_t} \tag{5.27}$$

The three phase active power current components of reference source currents are calculated as,

$$i_{\mathrm{psa}} = I_{Lp} * u_{ap}, \qquad i_{\mathrm{psb}} = I_{Lp} * u_{bp}, \qquad i_{\mathrm{psc}} = I_{Lp} * u_{cp} \tag{5.28}$$

5.5.2 Estimation of Amplitude of Reactive Current Components

A summation type GNN model network for amplitude estimation of reactive power current component of phase 'a' is shown in Fig. 5.3. The sensed load currents $(i_{\mathrm{La}}, i_{\mathrm{Lb}}, i_{\mathrm{Lc}})$ are the number of input applied to summation (Σ_1) and product (π) neurons with their weights $(w_{\Sigma 1qa}, w_{\Sigma 1qb}, w_{\Sigma 1qc})$ and $(w_{\pi qa}, w_{\pi qb}, w_{\pi qc})$, respectively. The outputs of the neurons are summed up with 'W_{qa}' weight by linear function that relates to Σ_1 and Σ gives GNN output for phase 'a' and likewise other phases outputs are obtained. In order to determine the reactive power current component amplitude, quadrature templates (u_{aq}, u_{bq}, u_{cq}) are used as the reference weights multiplier to find the actual weights of $\Sigma_1$and π neurons, respectively.

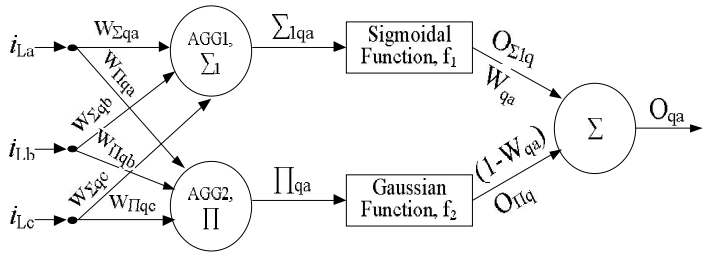


Fig. 5.3 GNN model for amplitude estimation of reactive current component of phase 'a'

The output of the Σ_1 aggregation function for phase 'a' is defined as,

$$\Sigma_{1q} = i_{\mathrm{La}} w_{\Sigma 1qa} + i_{\mathrm{Lb}} w_{\Sigma 1qb} + i_{\mathrm{Lc}} w_{\Sigma 1qc} + \Sigma_{bias} \tag{5.29}$$

To achieve threshold, the output Σ_{1q} neuron is passed through sigmoidal function, which is given as,

$$O_{\Sigma_1 q} = f_1(\Sigma_{1q}) = \frac{1}{1 + e^{-\lambda_s * \Sigma_{1q}}} \tag{5.30}$$

Similarly the π aggregation function of the summation type GNN for phase 'a' is defined as,

$$\pi_{\mathrm{q}} = i_{\mathrm{La}} w_{\pi qa} * i_{\mathrm{Lb}} w_{\pi qb} * i_{\mathrm{Lc}} w_{\pi qc} * \pi_{bias} \tag{5.31}$$

To achieve threshold, the output π_q neuron using Gaussian function is given as,

$$O_{\pi q} = f_2(\pi_q) = e^{-\lambda_p * \pi_q^2} \tag{5.32}$$

The gain scale factors λ_s and λ_p of the aggregation functions are considered to be unity. Using eqns. (5.30) and (5.32), the GNN models output for all phases are defined as,

$$O_{qa} = (1 - W_{qa})O_{\pi q} + W_{qa}O_{\Sigma_{1q}} \tag{5.33}$$

$$O_{qb} = (1 - W_{qb})O_{\pi q} + W_{qb}O_{\Sigma_{1q}} \tag{5.34}$$

$$O_{qc} = (1 - W_{qc})O_{\pi q} + W_{qc}O_{\Sigma_{1q}} \tag{5.35}$$

Where W_{qa}, W_{qb} and W_{qc} are the weights related to Σ_1 and Σ of the GNN model.

The average amplitude of the GNN neuron weighted value of reactive power current components (w_{Lq}) is estimated with the help of reactive power current components of load currents of all phases of the GNN model, which is given as,

$$w_{Lq} = \frac{(O_{qa} + O_{qb} + O_{qc})}{3} \tag{5.36}$$

The reactive power current component w_{qt} of DSTATCOM is estimated by taking error V_{te} between sensed and reference terminal voltage amplitude V_t and V_t^*, respectively at PCI passing through a DPI controller for maintaining the constant amplitude of AC grid voltage. The controller output at k^{th} instant is defined as,

$$w_{qt}(k) = w_{qt}(k-1) + k_{pt}\{V_{te}(k) - V_{te}(k-1)\} + k_{it}V_{te}(k) \tag{5.37}$$

Where $V_{te} = V_t^* - V_t$ and w_{qt} is a part of the reactive power current component of source current, and the gains of the DIP controller are proportional k_{pt} and integral k_{it}.

Similarly, the net reactive power current components amplitude of the load currents is calculated as,

$$I_{\mathrm{Lq}} = w_{\mathrm{qt}} - w_{\mathrm{Lq}} \tag{5.38}$$

Where w_{qt} is the output of the DPI controller and w_{Lq} is the reactive power current component amplitude of the load current.

The quadrature unit templates of v_{sa}, v_{sb}, and v_{sc} are derived using in-phase unit templates u_{ap}, u_{bp}, and u_{cp}which are given as,

$$u_{\mathrm{aq}} = \left(\frac{u_{\mathrm{cp}} - u_{\mathrm{bp}}}{\sqrt{3}}\right),\ u_{\mathrm{bq}} = \left(\frac{u_{\mathrm{bp}} + 3u_{\mathrm{ap}} - u_{\mathrm{cp}}}{2\sqrt{3}}\right), u_{\mathrm{cq}} = \left(\frac{u_{\mathrm{bp}} - 3u_{\mathrm{ap}} - u_{\mathrm{cp}}}{2\sqrt{3}}\right) \tag{5.39}$$

The three phase reactive power current components are calculated as,

$$i_{\mathrm{qsa}} = I_{Lq} * u_{aq}, \qquad i_{\mathrm{qsb}} = I_{Lq} * u_{bq}, \qquad i_{\mathrm{qsc}} = I_{Lq} * u_{cq} \tag{5.40}$$

5.5.3 Estimation of Switching Gate Pulses for DSTATCOM

The sum of estimated active and reactive power current components in eqns. (5.28) and (5.40) gives fundamental reference source currents ($i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*}$), which are calculated as,

$$i_{sa}^{*} = i_{\mathrm{psa}} + i_{\mathrm{qsa}}, \qquad i_{sb}^{*} = i_{\mathrm{psb}} + i_{\mathrm{qsb}}, \qquad i_{sc}^{*} = i_{\mathrm{psc}} + i_{\mathrm{qsc}} \tag{5.41}$$

A comparison is made between reference source currents ($i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*}$) and sensed source currents ($i_{\mathrm{sa}}, i_{\mathrm{sb}}, i_{\mathrm{sc}}$) and the PI current regulator is used to amplify the current error of each phase current and the resultant outputs are compared with carrier triangular signal of 10 kHz, which results into pulse gating signals for switching power devices of DSTATCOM.

5.6 RESULTS AND DISCUSSION

The developed GNN algorithm for DSTATCOM control in three phase distribution system is successfully tested in simulation and real time implementation using DSP based processor based on dSPACE 1104 in MATLAB environment. The performance of the DSTATCOM has been tested in order to maintain unity power factor and zero voltage regulation of AC bus at PCI. With the help of two case studies, these performances are presented under dynamic condition of linear/ nonlinear loads. The

performance results of the proposed algorithm indicate that it has reduced the complexity of multilayer neural network improving the accuracy as well as high generality degree.

5.6.1 *Case study I*: Performance of DSTATCOM in PFC Mode

The proposed GNN based control algorithm is developed using the mathematical modeling as discussed in section 5.4 in MATLAB Simulink environment. The test model of three phase distribution system with DSTATCOM is simulated and its behavior in PFC mode is validated. The simulation performance results are discussed here under linear/nonlinear load conditions:

5.6.1.1 Simulation results at nonlinear load conditions

Fig. 5.4 shows simulated performance results of DSTATCOM under balanced and unbalanced load conditions at nonlinear load in PFC mode. These results present waveforms of PCI voltages (v_s), supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_{Ca}, i_{Cb}, i_{Cc}), reference source currents (i_{xs}), AC bus voltage amplitude (V_t) and DC bus voltage (V_{dc}), respectively. Supply currents are observed balanced and sinusoidal during steady state (before t=1.1s) and unbalance load (t=1.1s to t=1.3s) conditions. Due to the action of PI controller, the voltage at DC bus of VSC is regulated at the reference value of 700V. The amplitude of AC bus voltage (V_t) at PCI is deviated from the reference value under unbalanced load conditions in PFC mode.

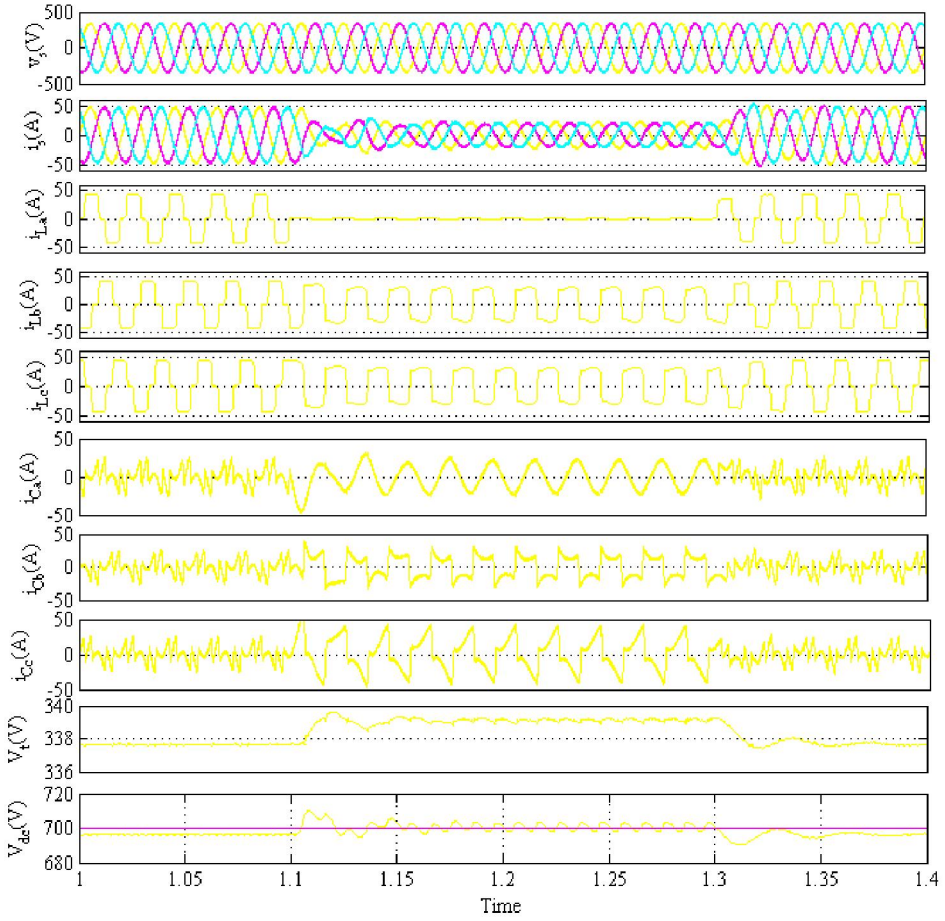
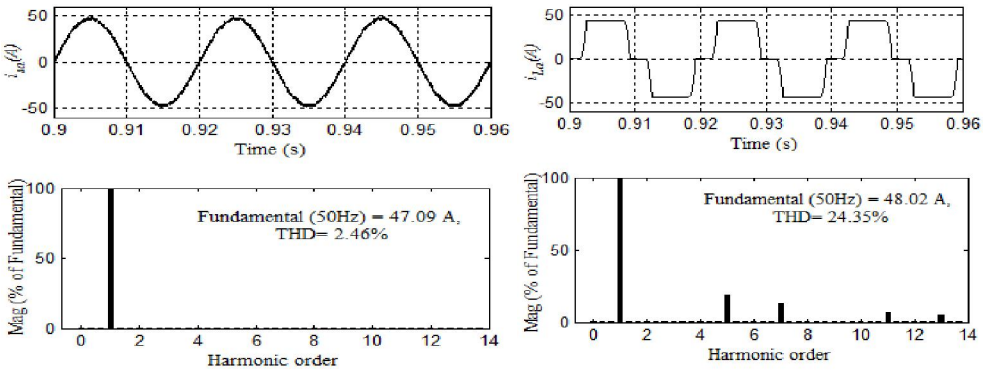


Fig. 5.4 Simulated performance of DSTATCOM at nonlinear load

Figs. 5.5 (a)-(b) show the waveforms, harmonic spectra and THDs at PCI of phase 'a' source and load currents, which are obtained as 2.46% and 24.35%, respectively. The low THDs prove that the DSTATCOM controlled by GNN algorithm, has improved the power quality.



(a) (b)

Fig. 5.5 Waveforms and harmonic spectra of (a) Source current (b) Load current in PFC mode of phase 'a'

5.6.1.2 Simulation results at linear load conditions

Fig. 5.6 shows simulated performance results of DSTATCOM under steady state and dynamic conditions of load at linear load in PFC mode. These results present waveforms of PCI voltages (v_s), supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_{Ca}, i_{Cb}, i_{Cc}), reference source currents (i_{xs}), AC bus voltage amplitude (V_t) and DC bus voltage (V_{dc}), respectively.

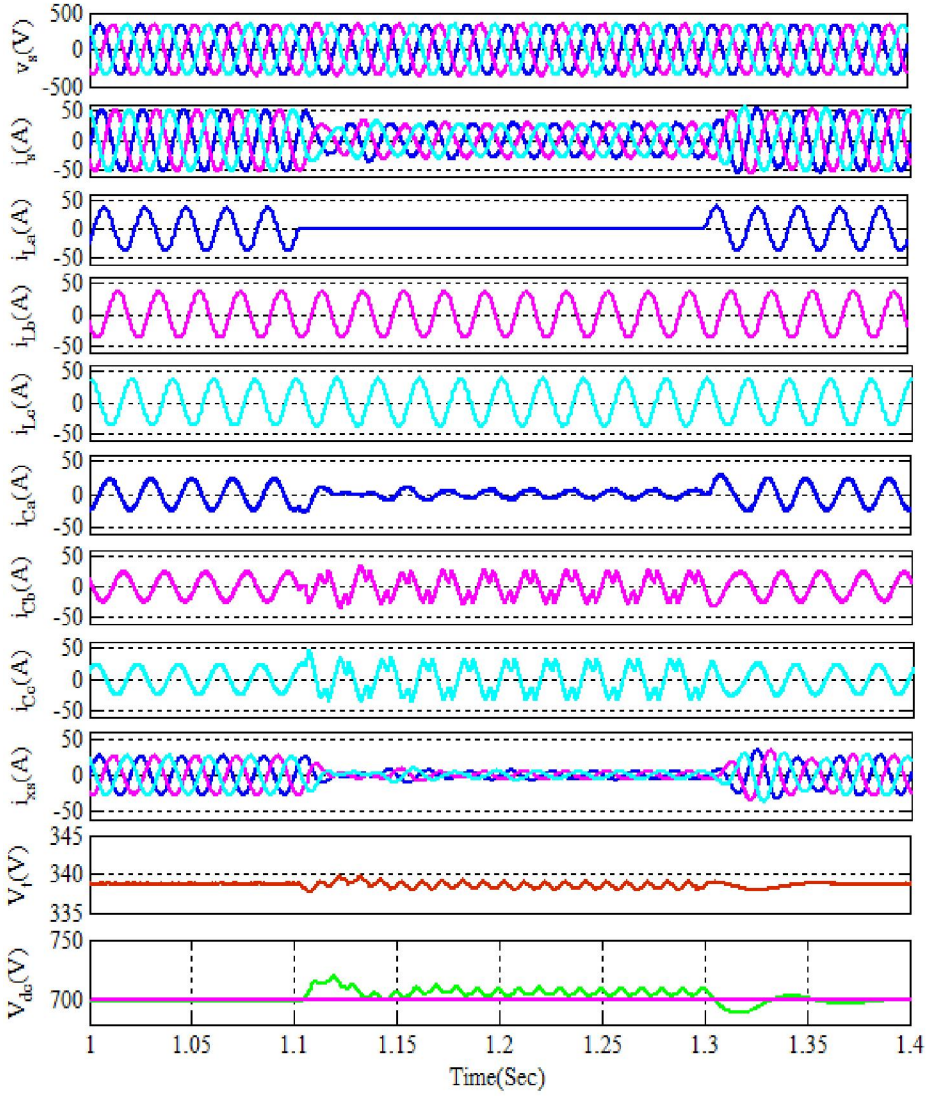


Fig. 5.6 Performance of DSTATCOM at linear load

Supply currents are observed balanced and sinusoidal during steady state (before t=1.1s) and unbalance load (t=1.1s to t=1.3s) conditions. Due to the action of PI

controller, the voltage at DC bus of VSC is regulated at the reference value of 700V. The amplitude of AC bus voltage (V_t) at PCI is deviated from the reference value under unbalanced load conditions in PFC mode. Moreover, the amplitude of the AC bus voltage (V_t) is also deviated simultaneously, shown in Fig. 5.6, respectively.

The GNN algorithm based switching of DSTATCOM has improved the power factor of the grid at PCI under linear balanced and unbalanced load conditions. The switching of the DSTATCOM takes place by comparing the fundamental source currents and the estimated reference source currents, and their error are fed to hysteresis current controller (HCC) for generation of PWM pulses. The injected compensating currents improve THDs in supply current due to action of the DSTATCOM in PFC mode and within the limit specified by IEEE-519 standard.

The relationship between in-phase voltage and supply current waveforms of distribution system at fundamental frequency delivering power to the linear/nonlinear load at PCI is maintained by using DSTATCOM. The required demand of harmonics compensation at PCI has been fulfilled by the DSTATCOM with its controlled operation performed by GNN based control algorithm. The proposed algorithm is evaluated through combination of summation and product neurons together in one layer. Each neuron possesses different weights with their inputs.

Fig. 5.7 shows the intermediate indices of the GNN algorithm for the extraction of active power current component of phase 'a'. The estimated weights; W_{pa} of linear transfer function Σ, $w_{\pi pa} = w_{pia}$ weight of product neuron and $w_{\Sigma 1pa} = w_{sa}$weight of summation neuron Σ_1, respectively.

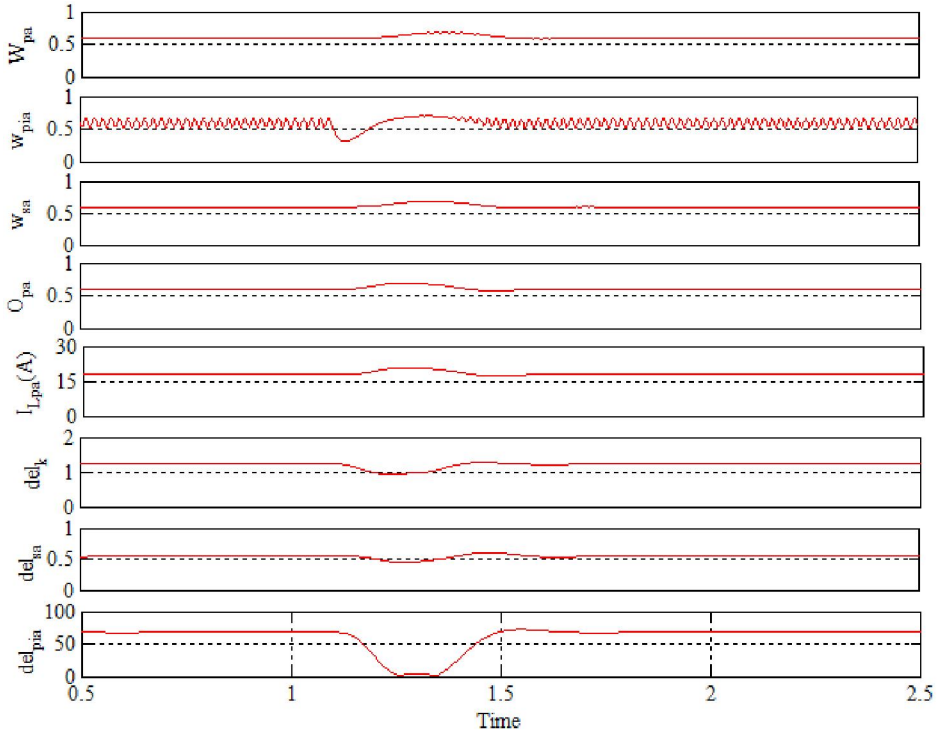


Fig. 5.7 Intermediate indices for amplitude estimation of active current component of phase 'a'

δ_k=del_k is the learning parameter of W_{pa}, $\delta_{\Sigma 1pa} = del_{sa}$ is the learning parameter of w_{sa} and $\delta_{\pi pa} = del_{pia}$ is the learning parameter of $w_{\pi pa}$ of phase 'a' at PCI under varying load conditions. The estimated GNN neuron output of the active power current component of the load current is represented by O_{pa} and its actual value is obtained by scaling and is shown by I_{Lpa}, respectively. These results indicate that the estimated weights are also varying accordingly under unbalanced load condition at an interval, t = 1.1 s to 1.3 s.

Fig. 5.8 shows the performance parameters of phase 'a' source voltage (v_{sa}), source current (i_{sa}) and load current in PFC mode of DSTATCOM. The source voltage (v_{sa}) and source current (i_{sa}) are found in same phase, whereas, the load current (i_{La}) of phase 'a' lags the source voltage (v_{sa}).

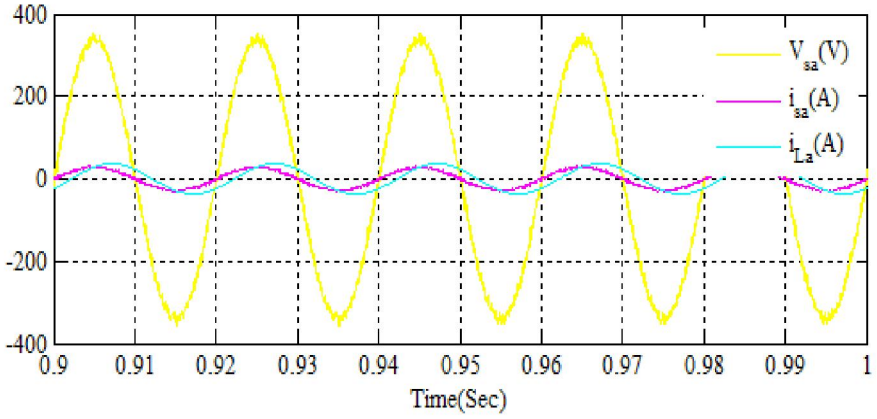


Fig. 5.8 Performance parameters of phase 'a' in PFC mode of DSTATCOM

5.6.2 *Case Study II*: Performance of DSTATCOM in ZVR Mode

In this case study, extra reactive power leading current components are injected to regulate the AC bus voltage to the reference level. The performance results of simulation of the test model for AC bus voltage regulation and provide balanced sinusoidal currents in the test system. Zero AC bus voltage regulation at PCI is also achieved by modifying the algorithm suitably. The performance of DSTATCOM under linear and nonlinear load conditions in ZVR mode is discussed here:

5.6.2.1 Simulation results at linear load conditions

Fig. 5.9 shows the performance of DSTATCOM in ZVR mode, the deviated AC bus voltage (V_t) under unbalanced linear load (t=1.1s to t=1.3s) conditions at PCI is regulated to reference level by the action of the PI controller. In this mode, the fundamental reference source current is the sum of the extracted fundamental active and reactive power current components. The reactive current compensation at PCI takes place using PWM switching of DSTATCOM. The regulated amplitude of the AC bus voltage (V_t), source voltages (v_s), source currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), injected compensating current components (i_{Ca}, i_{Cb}, i_{Cc}), estimated fundamental reference source currents are also shown in Fig. 5.9, respectively.

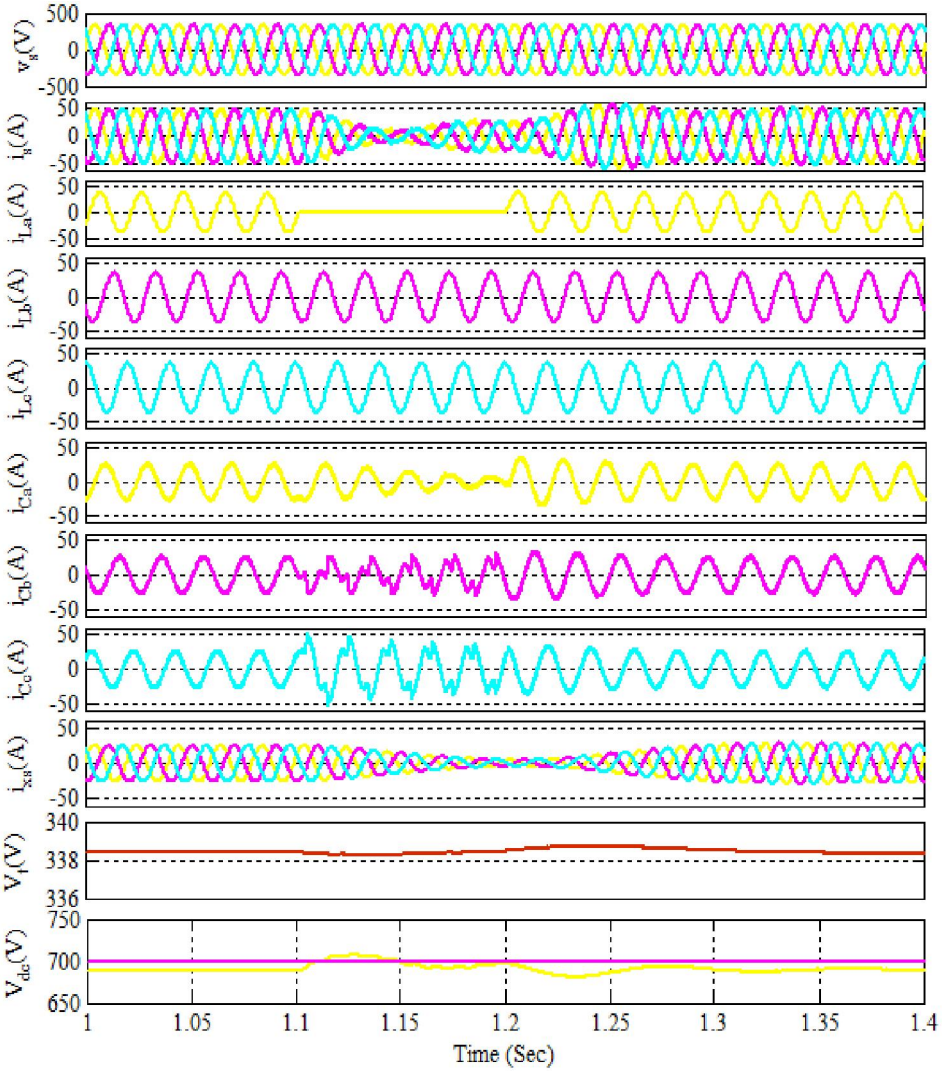


Fig. 5.9 Simulated performance of DSTATCOM at linear load

5.6.2.2 Simulation results at nonlinear load conditions

Fig. 5.10 shows the performance of DSTATCOM in ZVR mode under nonlinear load. These results present waveforms of PCI voltages (v_s), supply currents (i_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_{Ca}, i_{Cb}, i_{Cc}), reference source currents (i_{xs}), AC bus voltage amplitude (V_t) and DC bus voltage (V_{dc}), respectively.

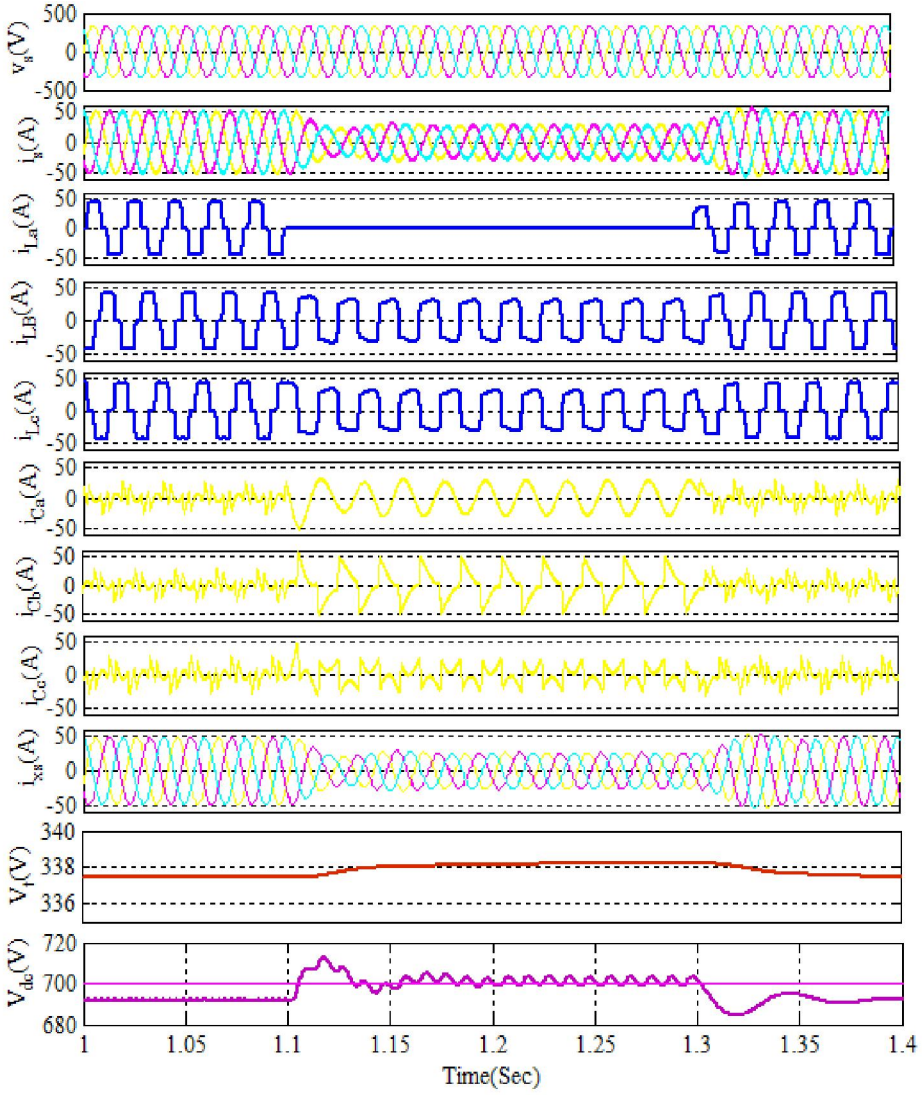


Fig. 5.10 Simulated performance of DSTATCOM at nonlinear load

Supply currents are observed balanced and sinusoidal during steady state (before t=1.1s) and unbalance load (t=1.1s to t=1.3s) conditions. Due to the action of PI controller, the voltage at DC bus of VSC is regulated at the reference value of 700V. The amplitude of AC bus voltage (V_t) at PCI is regulated to reference level under steady state and dynamic performance of DSTATCOM in ZVR mode. The PI voltage controller on the AC bus provides zero regulation at PCI. The amplitude of AC bus voltage is regulated within the deviation of 0 and 1 V.

Fig. 5.11 shows the intermediate indices of the GNN algorithm for the extraction of reactive power current component of phase 'a' at linear/nonlinear loads. The estimated weights of the neuron are shown in Fig. 5.11, the weights of the neuron for various transfer functions are W_{qa} of linear transfer function Σ, $w_{\pi qa} = w_{pia1}$ weight of product neuron and $w_{\Sigma 1qa} = w_{sa1}$ weight of summation neuron Σ1, respectively. δ_{k1}=del_{k1} is the learning parameter of W_{qa}, $\delta_{\Sigma 1qa} = del_{sa1}$ and $\delta_{\pi qa} = del_{pia1}$ are learning parameters of w_{sa1} and $w_{\pi qa}$ of phase 'a', respectively, at PCI under varying load conditions. The estimated GNN neuron output of the reactive power current component of the load current is represented by O_{qa} and its actual value is obtained by scaling and is shown by I_{Lqa}, respectively. For unbalanced condition the phase 'a' load is switched OFF at interval t=1.1 s and switched ON at t=1.3s. The observed waveforms of sensed parameters and various intermediate signals of the algorithms are captured. These results indicate that the estimated weights are also varying accordingly under unbalanced load condition during the interval at t = 1.1 s to 1.3 s.

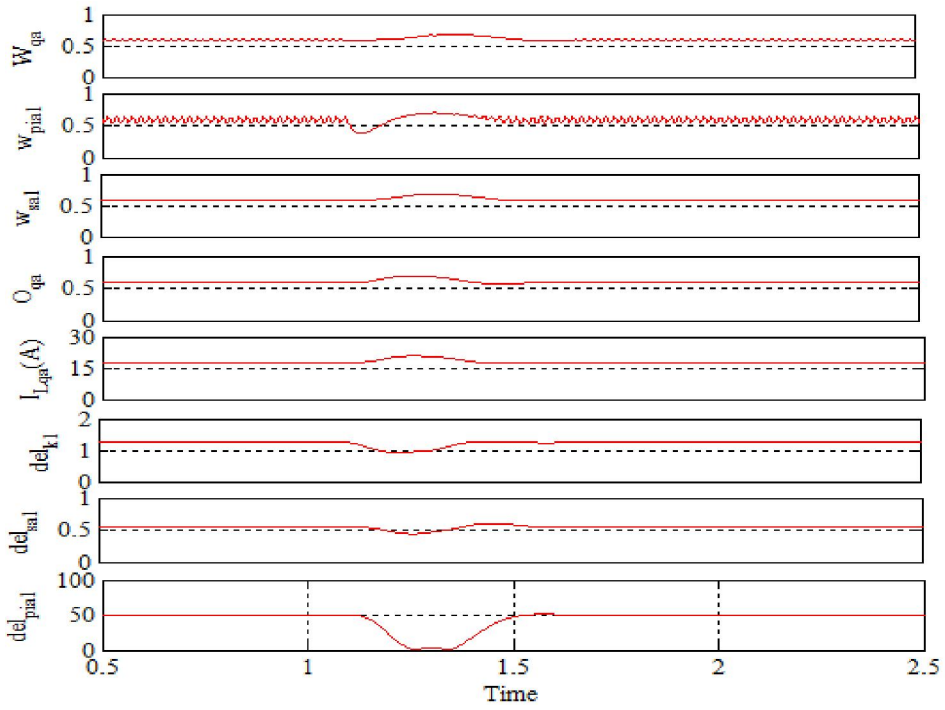


Fig. 5.11 Intermediate indices for amplitude estimation of reactive current component of phase 'a'

Figs. 5.12 (a)-(b) show the waveforms and harmonic spectra i.e. THDs at PCI of phase 'a' source and load currents which are obtained as 2.41% and 24.35%, respectively. It reveals that the GNN based control algorithm for DSTATCOM is able to regulate the PCI voltage at 338 V within the deviation of 0 to 1V, which effectively indicates the achievement of the developed algorithm.

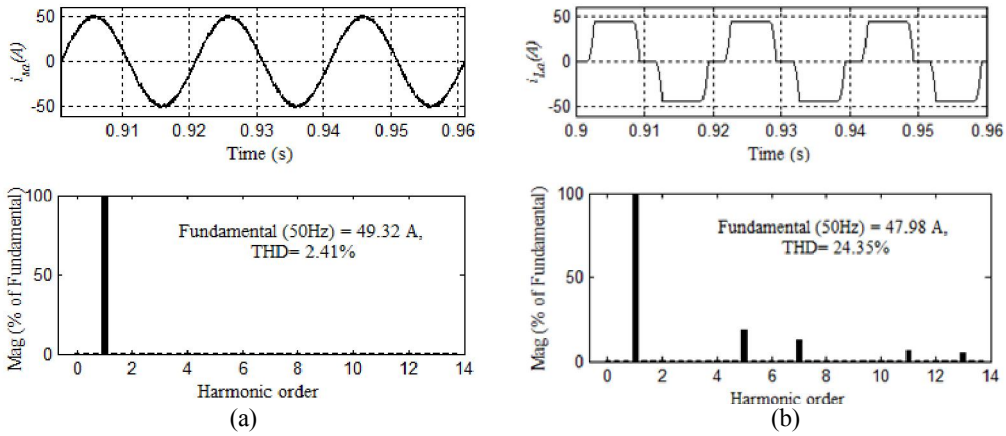


Fig. 5.12 Waveforms and harmonic spectra of (a) Source current (b) Load current of phase 'a'

5.6.3 Experimental Results in PFC Mode

The configuration of the test system for simulation and experimentation is same as shown in Fig. 5.1. The prototype test system is developed by connecting different units such as three phase AC grid, interfacing inductors, VSC with IGBT switches, high pass ripple filter, and linear/ nonlinear loads. For sensing of current and voltage signals, Hall-Effect current sensors (LA25P) and voltage sensors (LV25P) are used, respectively. These low voltage signals from the sensors are amplified by an amplifier (IC OP07) and these signals are utilized for the control of DSTATCOM through ADC and DAC of a DSP (in a dSPACE 1104). VSC-based DSTATCOM is controlled by the algorithm. A power analyser (Fluke 435) and a digital storage oscilloscope (DSO-X-2024A of Keysight make) are used for recording the waveforms. Experimental results are obtained for both load conditions (linear and nonlinear) at steady-state and dynamic conditions. The details of developed prototype hardware are shown in Appendix A.

The developed GNN based control algorithm for DSTATCOM has been validated with the required compensation at PCI to a desired value with sampling time of 70 μs on real time implementation in DSP processor. Moreover, it does not lead to any computational complexity. The performance of the DSTATCOM using the proposed GNN algorithm is satisfactory to overcome all the levels of distortion in the grid current. Experimental results are obtained and discussed as follows:

5.6.3.1 Performance of DSTATCOM at nonlinear load

The developed experimental setup has been implemented for PFC mode at nonlinear load. The performance results are captured and presented here. The waveforms of source voltages v_s and source currents i_s for all phases (a, b and c) are captured and shown in Figs. 5.13 (a)-(b) at PCI, respectively. Correspondingly, the harmonic

spectra of these waveforms are also captured and shown in Fig. 5.13 (c)-(d), respectively, when the DSTATCOM is in OFF state. The %THD of the PCI voltages v_s and source current i_s for all phases are found to be 6.5% and 25.2% which are above the permissible limit.

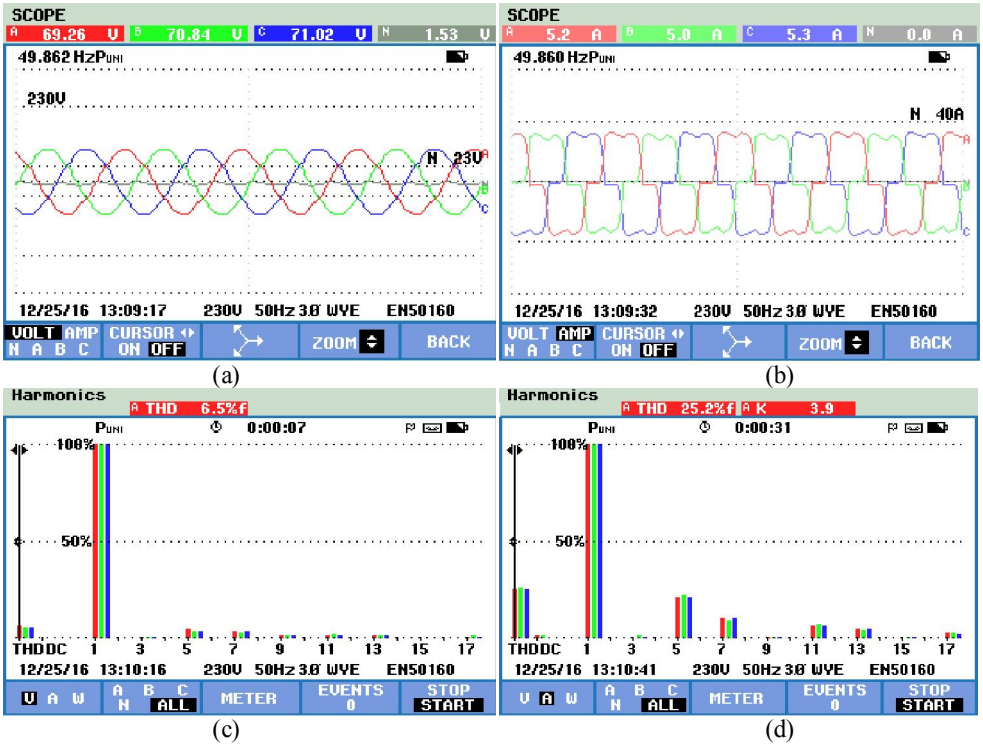


Fig. 5.13 Performance of DSTATCOM (a) Source voltages v_s (b) Source currents i_s (c)-(d) Harmonics spectra, for all phases during OFF state of DSTATCOM

Figs. 5.14 (a)–(b) show the waveforms of source voltages v_s and currents i_s, while their harmonic spectra, are shown in Figs. 5.14 (c)-(d), respectively, at PCI, when the DSTATCOM is switched ON for all phases. The %THD of PCI voltages and currents for all phases are reduced drastically to 2.1% and 4.9%, respectively which satisfy IEEE-519 standard. It is observed that the DSTATCOM mitigates the harmonics to make the source currents sinusoidal even at nonlinear load.

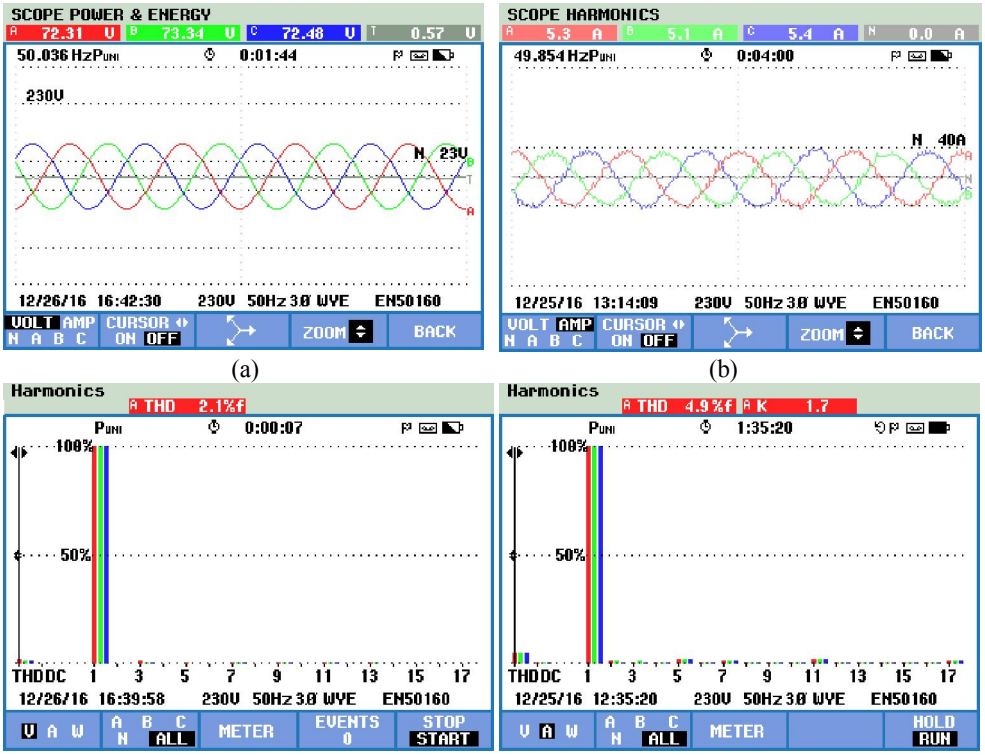


Fig. 5.14 Performance of DSTATCOM (a) Source voltages v_s (b) Source currents i_s (c) - (d) Harmonics spectra, for all phases during ON state of DSTATCOM

The source current and PCI voltage of phase 'a' are in same phase as shown in Fig. 5.15 (a), also Fig. 5.15 (b) shows the phasor diagram for maintaining voltage and current in same phase at PCI under steady state and dynamic conditions of nonlinear load while DSTATCOM is switched ON.

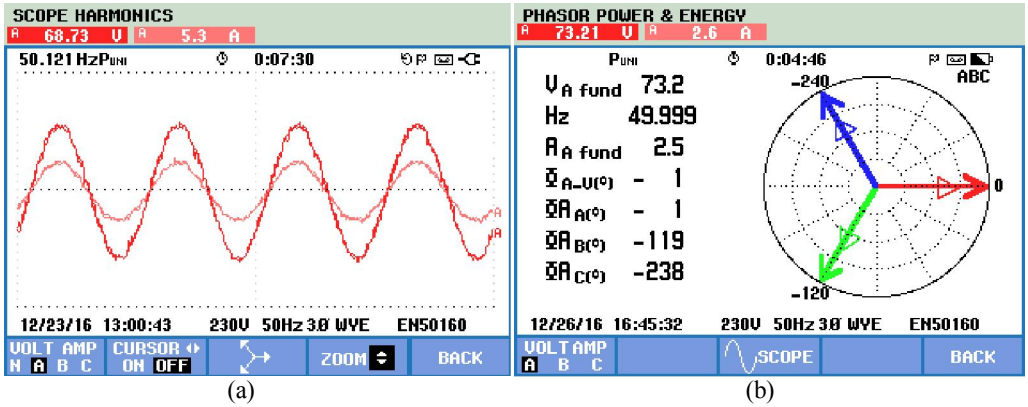
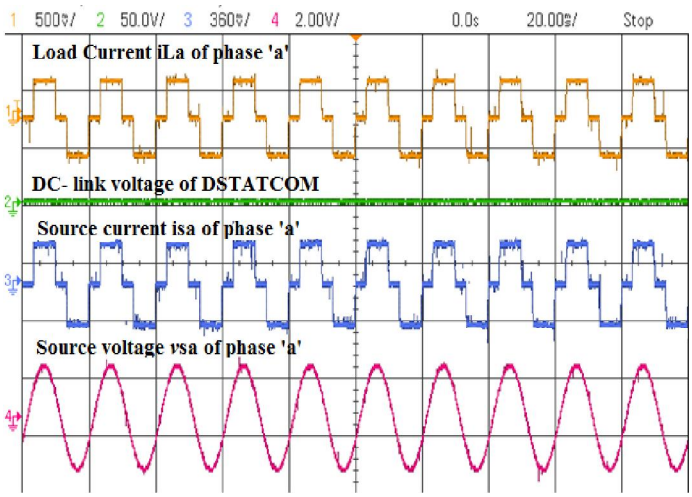
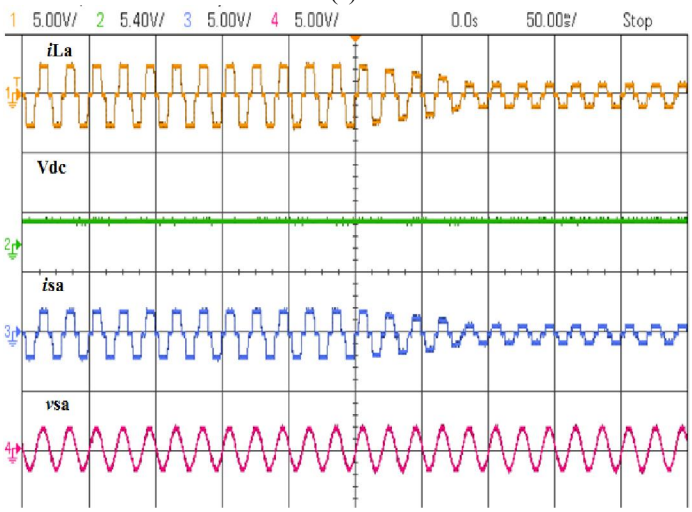


Fig. 5.15 (a) Source voltage v_{sa} and source current i_{sa} of phase 'a' (b) Phasor diagram of source voltages and currents, after switching ON DSTATCOM

Fig. 5.16 (a) shows the captured waveforms of performance parameters at PCI under steady state and dynamic conditions. The performance parameters at PCI are load current i_{La}, DC link voltage V_{dc} source current i_{sa}, and PCI voltage v_{sa}, of phase 'a'. The dynamic performance at PCI is obtained by reducing the load of phase 'a' for a very short interval which is shown in Fig. 5.16 (b), when DSTATCOM is in OFF state.



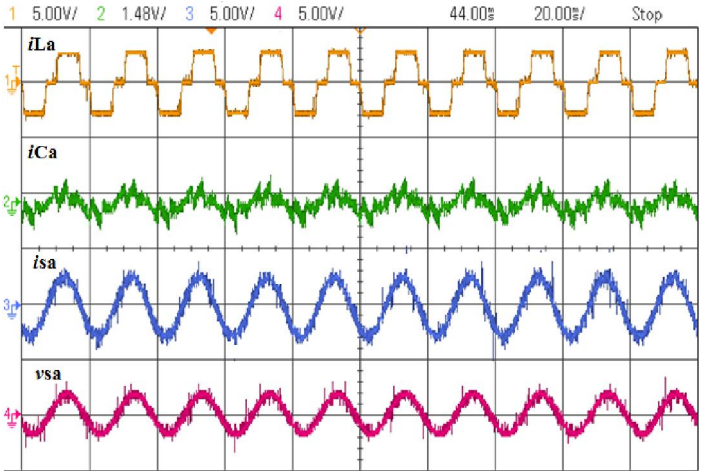
(a)



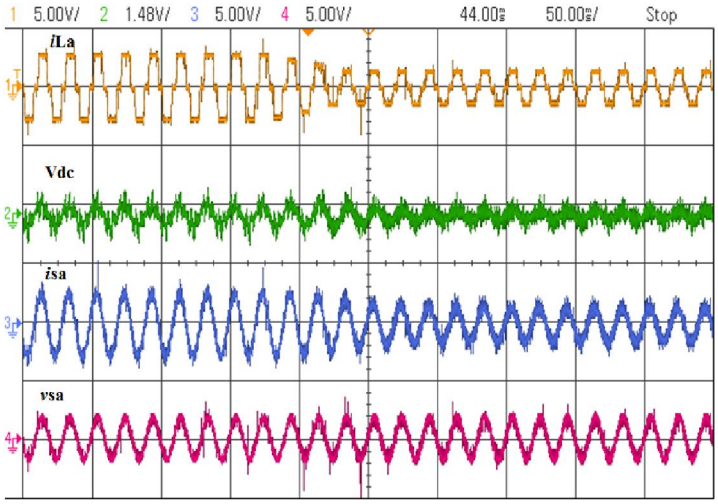
(b)

Fig. 5.16 Performance parameters (a) Load current i_{La}, DC-bus voltage V_{dc}, source current i_{sa}, and source voltage v_{sa}, under static condition (b) i_{La}, V_{dc}, i_{sa} and v_{sa} under varying load condition, when DSTATCOM is OFF

Fig. 5.17 (a) shows the performance parameters such as load current i_{La}, compensating current i_{Ca}, source current i_{sa}, and PCI voltage v_{sa}, of phase 'a' at PCI, when DSTATCOM is in ON state. Fig. 5.17 (b) shows the performance parameters under varying load condition of phase 'a'.



(a)



(b)

Fig. 5.17 Performance parameters (a) Load current i_{La}, compensating current i_{Ca}, source current i_{sa} and source voltage v_{sa} (b) i_{La}, V_{dc}, i_{sa}, and v_{sa}, of phase 'a' when DSTATCOM is in ON state under varying load condition

The experimental results shown in Figs. 5.13-5.17 are recorded with DC bus voltage at 200 V of VSC based DSTATCOM and AC bus voltage at PCI is considered as 120

V (L-L). The obtained waveforms show that the developed GNN algorithm is successfully implemented to control the DSTATCOM.

5.6.3.2 Performance of DSTATCOM at linear load

The results of proposed GNN algorithm at linear load under steady state condition are shown in Figs. 5.18. A three phase induction motor coupled to a DC generator, is taken as a linear load. The waveforms of three phase source voltages (v_{sa}, v_{sb} and v_{sc}), source currents (i_{sa}, i_{sb} and i_{sc}) connected to linear load, are shown in Figs. 5.18 (a)-(b). The load draws reactive power, which can be realized through phasor diagram shown in Fig. 5.18 (c), and the corresponding power factor is 0.82, shown in Fig. 5.18 (d), respectively, when the DSTATCOM is in the OFF state.

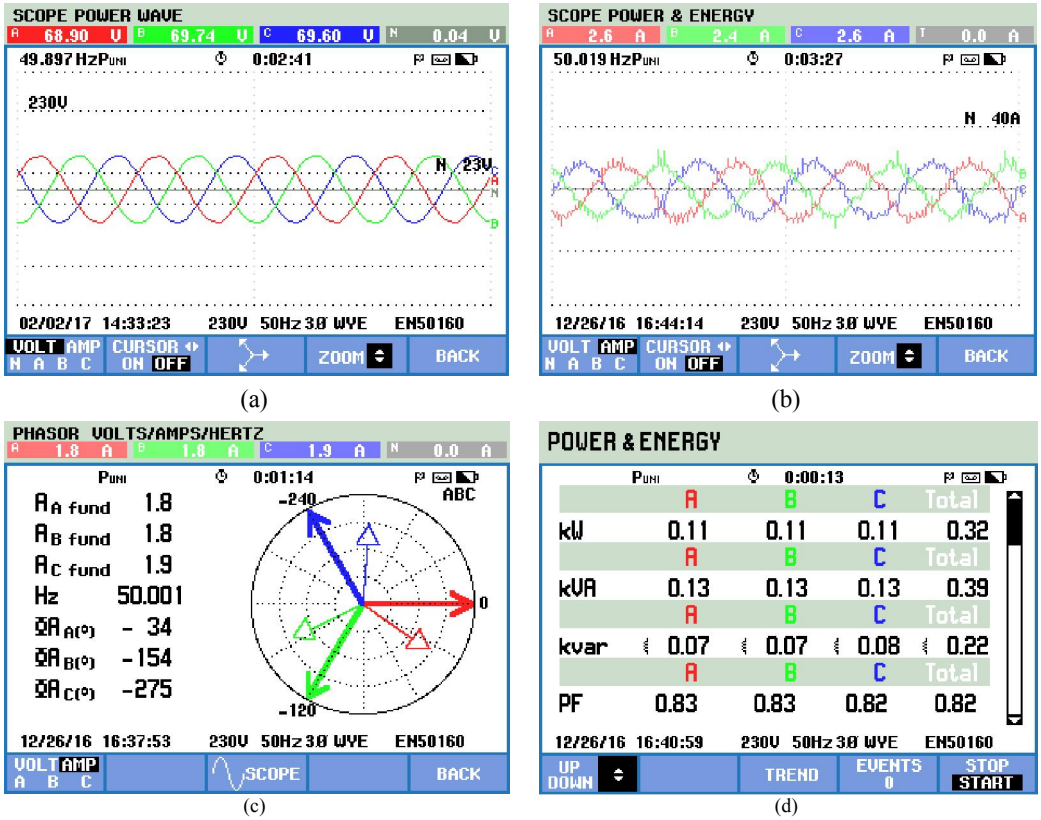


Fig. 5.18 Performance of DSTATCOM (a) Source voltages v_s (b) Source currents i_s (c) Phasor diagram of v_s- i_s (d) Power and power factor, when DSTATCOM is in OFF state

When DSTATCOM is switched ON, the reactive current components are injected at PCI that improves the power factor about to unity as shown in Fig. 5.19 (a) and

correspondingly THDs of the source current is found to be 1.3 %, shown in Fig. 5.19 (b). Fig. 5.19 (c) shows the phasor diagram that realizes that the reactive power demand of the load is compensated by the DSTATCOM at PCI as all voltages and currents of the source are in same phase. Fig. 5.19 (d) shows the improved power factor to 0.98, which is close to unity.

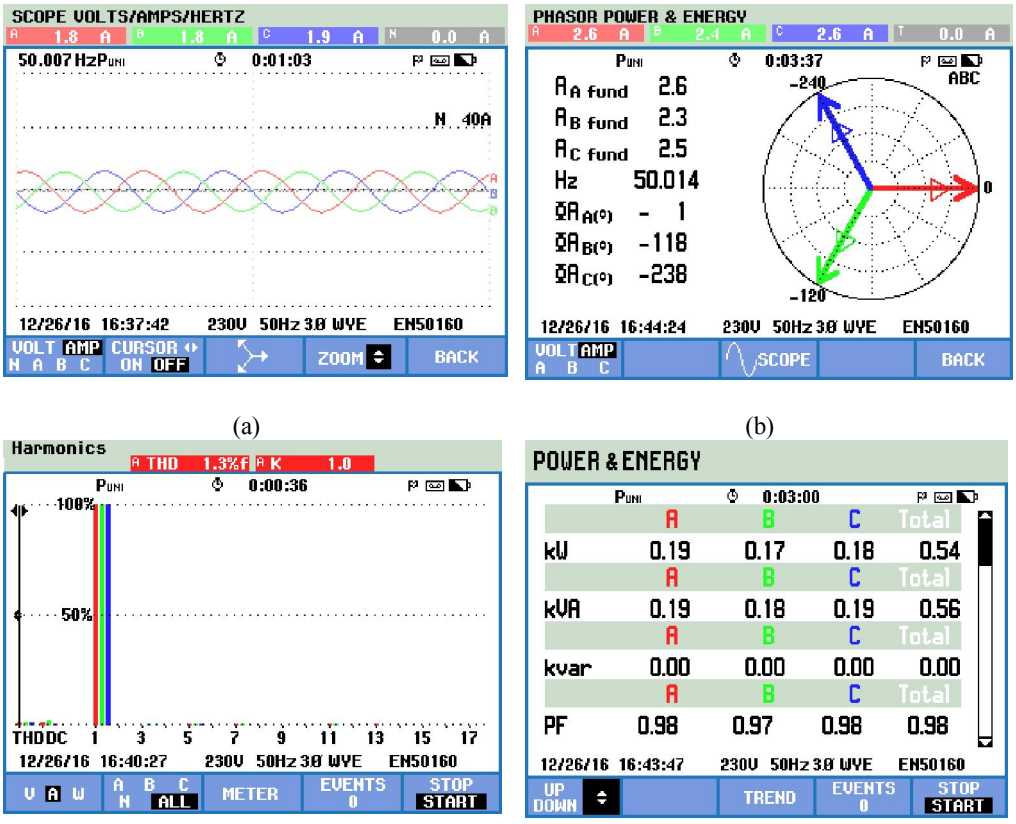


Fig. 5.19 Performance parameters (a) Source currents i_s (b) Phasor diagram of v_s- i_s (c) Harmonics spectra of i_s and (d) Power and power factor, when DSTATCOM is switched ON

It is observed that waveforms of PCI voltage and source current are made sinusoidal and in same phase in order to maintain unity power factor at PCI under both conditions (steady state and dynamic) for both nonlinear and linear loads using DSTATCOM. On the basis of the performance parameters, a comparison of

developed GNN algorithm with the other multilayer neural network algorithm is given in Table 5.2.

Table 5.2 Comparison of ANN and GNN based controllers

Performance parameters	**ADALINE**	**MLPNN**	**RBF**	**GNN**
Learning rule	Gradient decent (GD)	GD/GDM	Spread parameters	GDM
Training rule	LMS	BP	OLS LMS	BP
No. of layers	Two	Three	Two	One
Protocol training pattern	Online Training	Offline stochastic training	Offline training	Online training
Estimation nature	Linear	Nonlinear	Nonlinear	Both
Transfer function	Linear	Sigmoidal	Gaussian	All
Weight update Time	15.7 µs	82 µs	50 µs	8 µs
Settling period of dc link voltage	1 cycle	2 ½ cycles	2 cycles	1½ cycles
Max change in dc link voltage	4.8 V	11 V	12 V	6 V

The developed GNN based control algorithm is observed as the superior than ANN based ADALINE, feed-forward MNN, BP (Back-Propagation) and RBF (Radial Basis Function) control algorithms. A comparative analysis is made among existing ANN and proposed GNN controller as shown in Table 5.3 for nonlinear load in PFC and ZVR modes.

Table 5.3 Performance parameters of DSTATCOM

Operating mode	Performance parameters	GNN based control algorithm	ANN based control algorithm	Experimental results	
				Without DSTATCOM	With DSTATCOM
PFC mode	Grid voltage(V), %THD at PCI	338 V, 1.02 %	237.02 V, 2.86 %	69.26 V(ph) 6.5%	68.53 V (ph) 3.5 %
	Grid current (A), %THD at PCI	47.09 A, 2.46 %	32.17 A, 2.94 %	5.2 A, 25.2%	5.3 A, 4.9 %
	Load current (A), %THD at PCI	48.02 A, 24.35%	32.58 A, 24.82 %	5.2 A, 25.2%	5.2 A, 25.2%
ZVR mode	Grid voltage(V), %THD at PCI	337.8 V,1.10 %	239.63 V, 3.09 %		
	Grid current (A), %THD at PCI	49.32 A, 2.41 %	33.82 A, 2.99 %		
	Load current (A), %THD at PCI	47.98 A, 24.35%	32.94 A, 24.94 %		
	DC voltage of DSTATCOM	700 V	700V	200V	

The proposed control algorithm has made improvement in THDs of PCI voltages and source currents compared to the existing ANN control algorithms. The less number of unknown weights due to only one layer make the controller more precise under both the conditions (i.e. steady state and dynamic) of nonlinear and linear loads. Moreover, it improves response, estimation and learning speed.

5.7 CONCLUSIONS

The proposed GNN based control algorithm has improved the performance of distribution static compensator in a three phase distribution system. This algorithm is developed in MATLAB simulation environment and its performance is validated under both conditions (i.e. steady state and transient) at nonlinear load. In this control algorithm, a new concept of single layer is proposed with different transfer functions using summing and product neurons together in a pattern. This makes the algorithm more flexible in training the network on load dynamics. The DSTATCOM introduces the leading reactive power and suppressed harmonics as on demand at PCI from the load. With this improvement, the test system with DSTATCOM has maintained its power quality limit with sinusoidal PCI voltage and current. The improvements in THDs of source voltages and currents have proven the clear advantage of adopting the modified form of the neural network architecture to control DSTATCOM.

CHAPTER 6
AVSF BASED CONTROL ALGORITHM FOR DSTATCOM

6.1 INTRODUCTION

Recent trends have shown that the power quality has been adversely affected due to increased power electronics based devices at the utility grid in the distribution system. Suppression of harmonics and reactive power current compensation at point of common coupling (PCC), improve the power quality using a distribution static compensator (DSTATCOM). The development of new control algorithm based on adaptive Volterra second-order filter (AVSF) for DSTATCOM to extract the fundamental power current components from the polluted load currents of nonlinear load in distribution system is presented in this chapter. The AVSF is a combination of linear and nonlinear functions of the input signals. Both linear and quadratic functions optimize filter coefficients with fast convergence, which is quite important in the success of an adaptive solution. The proposed algorithm is also related to autocorrelation matrix and step size, which are used for rapid convergence. The performance of proposed algorithm for DSTATCOM is validated through experimental results for unity power factor of AC source and zero voltage regulation of the terminal voltage at PCC.

6.2 TEST MODEL CONFIGURATION

The test system consists of a distribution system having a nonlinear load. The test system with the shunt-connected DSTATCOM is shown in Fig. 6.1.

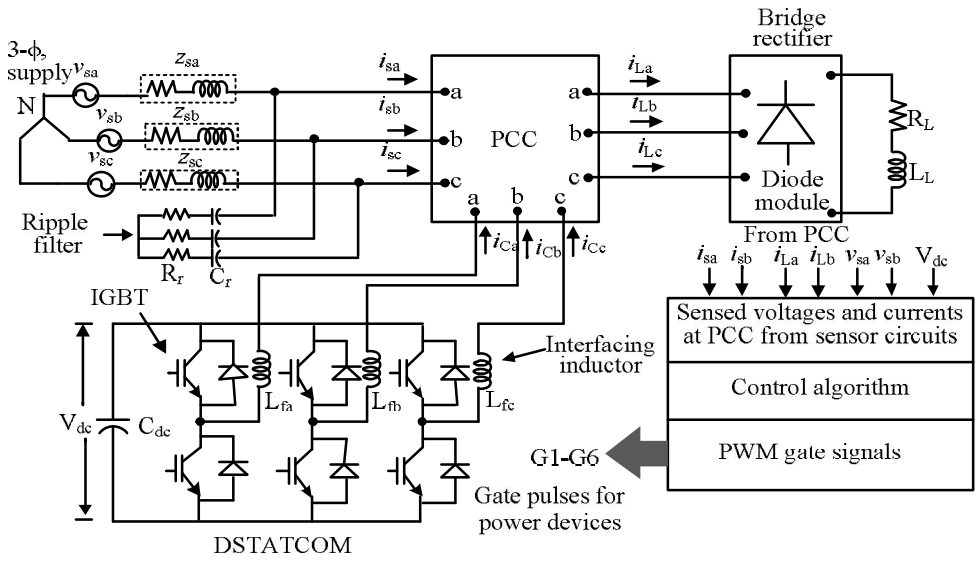


Fig. 6.1 Three phase distribution system with a DSTATCOM

A three-phase source with source impedances (Z_{sa}, Z_{sb}, and Z_{sc}) is feeding to a 3-phase bridge rectifier load (inductance L_L and resistance R_L). The DSTATCOM is placed using interfacing inductors (L_{fa}, L_{fb} and L_{fc}) in the test model. These interfacing inductors make the injected compensating currents ripple free with appropriate value, whereas the noise of fast switching of power devices, i.e., insulated-gate bipolar transistors (IGBTs), is passed through ripple filter with series combination of low resistance R_r and capacitance C_r in each phase at PCC from DSTATCOM. The compensating currents (i_{Ca}, i_{Cb} and i_{Cc}) are injected from DSTATCOM at PCC to improve the power quality. The DC link capacitance C_{dc} design depends on 3-phase AC supply and ratings of nonlinear load at PCC of the distribution system. Table 6.1 consists of test model configuration parameters.

Table 6.1 Configuration parameters and design specifications of test system

Sl No.	Test system parameters	Simulation specifications	Hardware specifications
1.	3 ϕ AC Source supply	3 ϕ, 415 V, 50 Hz	3 ϕ, 110 V, 50 Hz
2.	Source resistance and inductance R_s+j X_s	(0.05+j0.214) Ω	---
3.	Filter impedance (R_r-jX_{Cr})	(5 –j160) Ω	(5 -j80) Ω
4.	Inductors (L_{fa}= L_{fb}= L_{fc}) to interface with VSC	2.68 mH	3.32 mH
5.	Voltage source converter (VSC) of IGBT	3 ϕ,415 Vac	SEMIKRON MD B6U 415/560-43F + MD B6CI 600/415-35F
6.	Linear load (series of inductance and resistance)	25kVA, 0.8 Pf (lagging)	20 mH and 15 Ω/ ph
7.	3- ϕ uncontrolled rectifier module with R_L and X_L	(15+j47) Ω	SEMIKRON SKD 85 With (20+j57) Ω
8.	DC link capacitance of VSC (C_{dc})	15 mF	4.7 mF
9.	Reference DC link voltage (V^*_{dc})	700 V	700 V
10.	Gains for DC link DPI controller K_{pdc} and K_{idc}	1.25 and 0.001	0.325 and 0.012
11.	Gains for AC bus DPI controller K_{pt} and K_{it}	2.25 and 0.001	0.125 and 0.001

6.3 CONCEPT OF NONLINEAR ADAPTIVE FILTER

The growing application of devices based on power electronics in the utility grid has adversely affected the power quality in the distribution systems. These devices impose harmonics, and unbalanced loading causes poor power factor as well as induces negative sequence voltage, which causes unbalanced voltages. To maintain the allowable distortions limit framed by standard guidelines [62] is a challenging task for the

researchers. The power quality can be improved within the limit with the help of DSTATCOM [29]. The shunt compensator performs load balancing and harmonics suppression under both linear and nonlinear loads [53]-[60]. The improvement in the power quality directly depends on fast and reliable operation of DSTATCOM, which is decided by the control algorithms. In recent years, besides conventional control algorithms, soft computing methods such as artificial neural network (ANN), adaptive filter theory and recursive techniques based many control algorithms have been developed for efficient operation as reported in the literature [146]–[152].

The development of many control algorithms has been carried out based on linear adaptive theories to improve the performance of DSTATCOM. The adaptive theory is based on LMS (Least Mean Square) algorithm, which has slow convergence rate. With the improved convergence rate, many control algorithms have been developed and their performances are discussed in [149]–[155]. These algorithms increase the convergence rate and decrease the dependency on the input conditioning of the LMS algorithm. Singh *et al.* [154] and [155] have discussed LMS algorithms, such as adjustable step and leaky, and analyzed their performance on DSTATCOM. Aboulnasr *et al.* [156] have reported fast convergence of LMS algorithm at early stages of adaptation. Górriz *et al.* [157] have described a novel LMS algorithm based on the minimization of the difference weight vector under a stability constraint. Douglas [158] has presented modified FXLMS (Filtered –XLMS) algorithm to improve the convergence speed by removing the output delay within the error signal caused by the secondary path. The efficient implementation of filtered-X LMS algorithm has been carried out by Rigling *et al.* [159], which deals with many LMS algorithms including subspace leaky, leaky, and circular leaky and analysis of

their performances are presented. However, the choice of linear adaptive filters may not be suitable for nonlinear input signals. Therefore, the application of nonlinear adaptive filter for nonlinear input signal is quite effective instead of linear adaptive filters.

The nonlinear characteristics of the load help in adaption of nonlinear filtering techniques to provide improved performance. One of the examples of nonlinear filter is polynomial filter where Volterra series is selected as the major tool for processing nonlinear signals. The Volterra series is selected for estimation and for processing of nonlinear signals in the available literature. The structure of the Volterra series filter is determined in terms of order and length by truncating the series. Volterra series has been quite attractive in modeling adaptive filter applications for signal processing of nonlinear systems [160]. It can be broadly used for extraction and estimation of signals in nonlinear systems. The output of the filter varies linearly with the input with respect to coefficients, which shows that LMS algorithm can be directly applied. Ogunfunmi *et al.* [161] have reported the second-order Volterra system identification based on discrete nonlinear Wiener model. Davila *et al.* [162] have discussed AVSF (Adaptive Volterra Second Order Filter) with fast convergence for updating both weights linear and quadratic. Ten *et al.*[163] have presented the application of VFXLMS (Volterra filtered-X LMS) algorithm for feed forward ANC (Active Noise Control) to reduce the noise. Koh and Powers [164] have used a factorization technique to design and implement an AVSF to decrease the filtering operations complexity considerably. Dogancay [165] has discussed the complexity considerations in adaptive filters.

Adaptive filtering algorithms consider computational complexity and convergence speed as two important factors. The computational complexity is proportional to the number of

filter coefficients for an adaptive filtering algorithm [165]. The convergence speed of AVSF is dependent on the Eigen value spread of the autocorrelation of the input signals with their coefficients. The Eigen value spread depends on the spectral distribution of the input signals. The convergence rate of AVSF is inversely proportional to the ratio of maximum to minimum Eigen values.

In this proposed work, a LMS algorithm for AVSF is developed to extract the fundamental components of the polluted load currents to estimate the reference source currents to produce high frequency switching gate pulses for DSTATCOM. AVSF is modeled and designed with finite length and finite order to suppress third-, fifth-, and seventh-order harmonics. The optimum filter weight is estimated from a method reported in [164], by virtue of which Volterra filter with minimum mean square error (MSE) is obtained. As a result, the magnitude error and phase delay in estimating fundamental component of load current, are reduced improving the filter accuracy. The convergence rate and stability of proposed algorithm, depend on step size parameters (μ), which is directly determined by the Eigen value of the covariance matrix of the filter input vector. The developed LMS algorithm for AVSF on DSTATCOM has been implemented successfully to suppress harmonics, to compensate reactive power, and to regulate terminal voltage to rated level at PCC in the test system. The performance results are found to be under the standard allowable limits [62]. The proposed algorithm has certain advantages such as it is adjusted automatically with the system dynamics and its convergence rate is determined with help of the system parameters over the existing linear adaptive algorithms. Moreover, it is superior to linear adaptive algorithms to enhance the performance of DSTATCOM to improve the power quality in the distribution system.

6.4 MATHEMATICAL MODELING OF AVSF BASED CONTROL ALGORITHM

This algorithm is designed and modeled by expansion of second order Volterra series on discrete Fourier transform (DFT) of length three to suppress the 3rd, 5th and 7th harmonic components, and hence the named adaptive Volterra second order filter (AVSF). The mathematical modeling of nonlinear adaptive filter is carried out to extract and detect a signal from nonlinear system using Volterra series, which is given in eqn. (6.1). The series has been terminated to a finite length and order, to specify the characteristic of the filter. The nonlinear model of Volterra adaptive filter is shown in Fig. 6.2, which consists of linear, quadratic and offset parts. The test system taken under consideration is loss less, therefore, its offset part h_0, is taken as zero, $h_0 = 0$. The other parts are linear and quadratic, which are obtained from sensed input load current at instants 't', 't-1'and 't-2', respectively.

The SVF series has the form,

$$\mathrm{Y}(t) = h_0 + \sum_{M_1=0}^{t-1} h_1(m_1)X(t-m_1) + \sum_{k=1}^{t-1}\sum_{M_1=M_2}^{t-1} h_2(m_1,m_2)\,X(t-M_1)X(t-M_2) \qquad (6.1)$$

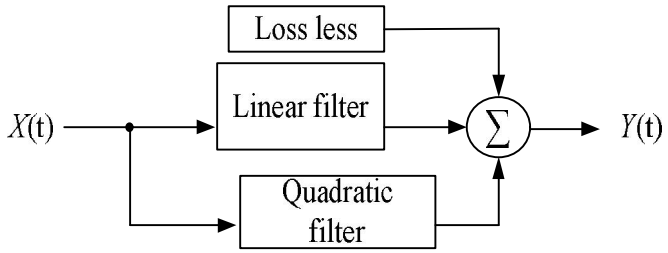


Fig. 6.2 Nonlinear adaptive model of Volterra filter

Where $X(t)$ and $Y(t)$ are input and output of the Volterra filter, respectively. The coefficients $h_1(m_1), h_2(m_1, m_2)$ are called Volterra kernel functions of the filter. The

length of the series is addressed by *t.* Generality loss in the filter is not considered, which means that the filter coefficients are symmetrical i.e. $h_2(m_1, m_2) = h_2(m_2, m_1)$ for indices $m_1 \, and \, m_2$ in respect of variables given in eqn. (6.1). The filter has linear relationship with its input and output through coefficients, which is expressed as,

$$Y(t) = A^T(t)X(t) \tag{6.2}$$

Where $A(t)$ is the weight vector containing $N \times 1$ linear weight vector and $N \times N$ quadratic weight vector of the SVF, defined as,

$$A(t) = [a_1(0), \dots, a_1(N-1)], [a_2(0,0), a_2(0,1), \dots$$
$$\dots, a_2(N-1, N-2), a_2(N-1, N-1)] \tag{6.3}$$

The linear $N \times 1$ and quadratic $N \times N$ input vector $X(t)$ is defined as

$$X(t) = [x(t), x(t-1), \dots, x(t-N+1)], [x^2(t), x(t)x(t-1), \dots, x^2(t-N+1)] \tag{6.4}$$

The length of the truncated SVF is $l(l+3)/2$. The SVF output $Y(t)$ is given as,

$$Y(t) = {A_{opt}}^T(t)X(t) \tag{6.5}$$

Where A_{opt} is the optimal value of the weight vector, which minimizes MSE error taken from desired signal $S(t)$ and actual value $Y(t)$, given as,

$$E[e^2(t)] = E\left[\left(S(t) - Y(t)\right)^2\right] \tag{6.6}$$

The weight vector $A(n)$ of SVF is updated using LMS algorithm as,

$$A(t+1) = A(t) + \mu e(t)X(t) \tag{6.7}$$

Where μ is step size with small positive constant value, the algorithm convergence speed is controlled by it. The error $e(t)$ at t^{th} sampling instant of the desired signal $S(t)$ and actual signal $\mathrm{Y}(t)$ value is given as,

$$e(t) = S(t) - Y(t) \tag{6.8}$$

The value of μ is determined from [160], in this case the value is randomly selected. The selected value of μ lies in,

$$0 < \mu < \frac{2}{\lambda_{max}} \tag{6.9}$$

The optimum value of weight vector $w_{opt}(t)$ is given as,

$$A_{opt} = R_x^{-1} p \tag{6.10}$$

Where R_x is the input $X(t)$ autocorrelation matrix, given as,

$$R_x = E[X^*(t)X^T(t)] \tag{6.11}$$

and p is the cross-correlation vector, defined as,

$$p = E[Y(t)X(t)] \tag{6.12}$$

With the help of mathematical modeling of the proposed AVSF control algorithm, the reference fundamental current components are detected and estimated from the load currents to perform the switching of DSTATCOM. The Volterra series in eqn. (6.1) has been truncated to second order as the dynamic in the linear/nonlinear load possesses linear and quadratic functions characteristic.

6.5 ESTIMATION OF FUNDAMENTAL REFERENCE SOURCE CURRENTS

The reference source currents of three phase distribution system, are estimated with the help of proposed AVSF based control algorithm. The number weight coefficients of the SVF series, depends on the memory length N of the input. The SVF series length is $N(N+3)/2$, which comprises of linear and quadratic components. AVSF has three memory lengths of the input, which results into nine (for N=3, $N(N+3)/2$) weight vectors. The algorithm requires sensed instantaneous source currents (i_{sa}, i_{sb} and i_{sc}) and voltages (v_{sa},$v_{sb}$and v_{sc}), DC link voltage (V_{dc}) and load currents (i_{La}, i_{Lb} and i_{Lc}), respectively. The estimated fundamental current components from the load currents are

used to estimate the fundamental reference source currents. The developed AVSF control algorithm estimates the reference template of source currents, and further, it compares the reference and actual source currents resulting into generation of high frequency pulse width modulation (PWM) switching pulses for IGBTs of DSTATCOM. The amplitudes of the active and reactive power current components are estimated as follows:

6.5.1 Amplitude Estimation of Fundamental Load Active Current Components

The developed AVSF model decomposes the sensed load currents in Fourier Transform according to [160]. Amplitude of fundamental load active current components is calculated using decomposed sensed load currents. The load currents are defined as,

$$i_{La}(t) = I_0 + \sum_{k=1}^{N} (I_{mk} \sin(k\omega t) + I_{mk} \cos(k\omega t))$$

$$i_{Lb}(t) = I_0 + \sum_{k=1}^{N} (I_{mk} \sin(k\omega t + 2\pi/3) + I_{mk} \cos(k\omega t + 2\pi/3))$$

$$i_{Lc}(t) = I_0 + \sum_{k=1}^{N} (I_{mk} \sin(k\omega t - 2\pi/3) + I_{mk} \cos(k\omega t - 2\pi/3)) \quad (6.13)$$

Where, I_0 is the DC component, I_{mk} is the magnitude of current and ω is the angular frequency of fundamental components, respectively. The weight coefficients of input load currents to AVSF are in-phase unit templates u_{pa}, u_{pb} and u_{pc}. These are estimated using phase voltages $v_{sa}, v_{sb,}$ and v_{sc} which are calculated from the sensed instantaneous line voltages v_{ab} and v_{bc} at PCC as,

$$v_{sa} = \left(\frac{2}{3} v_{ab} + \frac{1}{3} v_{bc}\right) \quad (6.14)$$

$$v_{sb} = \left(-\tfrac{1}{3} v_{ab} + \tfrac{1}{3} v_{bc}\right) \quad (6.15)$$

$$v_{sc} = \left(-\frac{1}{3}v_{ab} + \frac{2}{3}v_{bc}\right) \tag{6.16}$$

By using the estimated phase voltages, the PCC voltage (V_t) amplitude is calculated as,

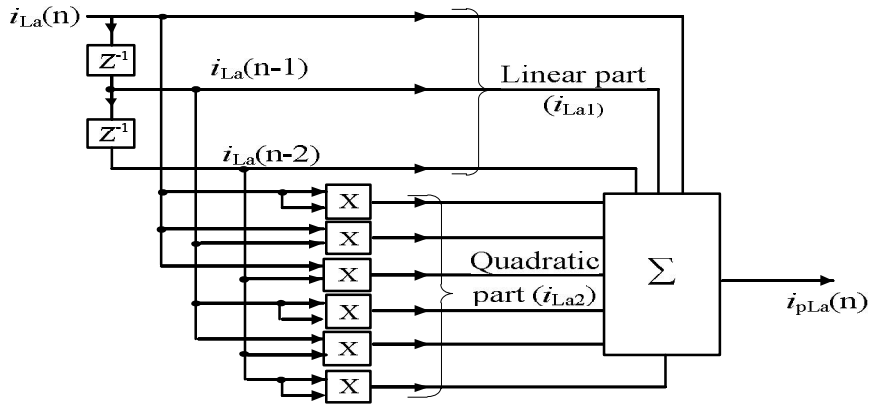
$$V_t = \sqrt{\left\{\frac{2}{3}((v_{sa})^2 + (v_{sb})^2 + (v_{sc})^2)\right\}} \tag{6.17}$$

The ratios of phase voltages to PCC voltage amplitude, result into in-phase unit templates (u_{pa}, u_{pb} and u_{pc}), expressed as,

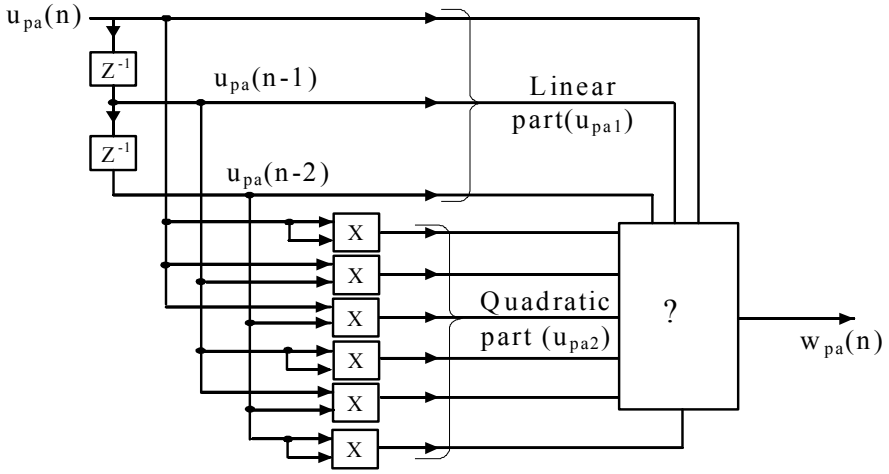
$$u_{pa} = \frac{v_{sa}}{V_t}, u_{pb} = \frac{v_{sb}}{V_t} \; and \; u_{pc} = \frac{v_{sc}}{V_t} \tag{6.18}$$

The estimated in-phase unit templates in eqn. (6.18) are weight coefficients of the input vector. Two impulses are applied, at $(n-1)$ and $(n-2)$ sampling instants of the sensed load current (i_L) at n^{th} sample and in-phase unit template (u_p), simultaneously to obtain Volterra series. Figs. 6.3 (a)-(b) show the decomposition of input vector load current of Phase 'a' and correspondingly its weight coefficient u_{pa} using proposed SVF based control algorithm. The length of the decomposed components, is the memory length of the SVF, here it is nine. In the similar manner, the phases 'a', 'b' and 'c' with their in-phase templates are decomposed. The fundamental active current components of all the three phases are estimated, which are further used to generate reference template for switching DSTATCOM.

The decomposed components have linear part at 'n', 'n-1' and 'n-2' sampling instants, and quadratic part contains their cross-products of the linear part excluding the generality loss in the filter.



(a)



(b)

Fig. 6.3 Decomposition of (a) Load current (b) In-phase unit template of phase 'a'

Fig. 6.3 (b) shows the weight coefficient vector $w_{pa}(n)$ in response to its input vector $i_{pLa}(n)$ obtained from load current $i_{La}(n)$ in Fig. 6.3 (a). Mathematically, the load current $i_{La}(n)$ as input vector at n^{th} sampling instant is decomposed as,

$$i_{La}(n) = I_0 + \sum_{m_1=0}^{N-1} I_{m_1 k} \cos \omega(kn - \varphi_1)\, I_{m_1 k} \sin \omega(kn - \varphi_1) +$$

$$\sum_{k=1}^{N-1}\sum_{m_1=m_2}^{N-1} I_{m_1k}\cos\omega(kn-\varphi_1)\, I_{m_1k}\sin\omega(kn-\varphi_2)\, I_{m_2k}\cos\omega(kn$$

$$-\varphi_2)\, I_{m_2k}\sin\omega(kn-\varphi_2) \tag{6.19}$$

Where I_0 is DC component while I_{m_1k} and I_{m_2k} (i.e. in-phase unit template and load current waveforms) are two input vectors amplitudes with frequency kn and phases φ_1 and φ_2, respectively. A Volterra series that relates the input and output signals of eqn. (6.19) is formed up to length of nine. The amplitude of each phase fundamental active current component is estimated separately and is designated as i_{pLa}, i_{pLb} and i_{pLc}, respectively. For simplicity, only magnitude of the fundamental active current component i_{pLa} of phase 'a' is mathematically described while other two phase components are directly assigned. This general approach can be extended to nonlinear, if two impulses are applied, at $(n-1)$ and $(n-2)$ of n^{th} sampling instant of $i_{La}(n)$, respectively. The nonlinear response of two impulses can be written as,

$$i_{La1}(n) = [i_{La}(n)\ \ i_{La}(n-1) i_{La}(n-2)] \tag{6.20}$$

$$i_{La2}(n) = \begin{bmatrix} i_{La}(n)i_{La}(n) & i_{La}(n)i_{La}(n-1) & i_{La}(n)i_{La}(n-2) \\ i_{La}(n-1)i_{La}(n) & i_{La}(n-1)i_{La}(n-1) & i_{La}(n-1)i_{La}(n-2) \\ i_{La}(n-2)i_{La}(n) & i_{La}(n-2)i_{La}(n-1) & i_{La}(n-2)i_{La}(n-2) \end{bmatrix} \tag{6.21}$$

The linear part $i_{La1}(n)$ in eqn. (6.20) has three components. The first is the sensed load current at n^{th} sampling instant $i_{La}(n)$ while the other two terms are obtained by providing unit delay of interval as $i_{La}(n-1)$ and $i_{La}(n-2)$, respectively. The quadratic part $i_{La2}(n)$ in eqn. (6.21) is obtained by multiplying the elements of the linear part. The sum of the elements of linear and quadratic parts, is the total length of the input vector $i_{pLa}(n)$ of the AVSF for phase 'a' which is defined as,

$$i_{pLa}(n) = i_{La1}(n) + i_{La2}(n) + \varepsilon_1 \tag{6.22}$$

Where $i_{pLa}(n)$ is summed up amplitude of fundamental active current components, and the magnitude error $\varepsilon_1$is the difference between two impulse responses. Likewise, the weight coefficients vector $w_{pa}(n)$ of $i_{pLa}(n)$ is estimated. The weight coefficients of linear part $i_{La1}(n)$ and quadratic part $i_{La2}(n)$ are estimated using in-phase unit template u_{pa} of phase 'a'. The elements of the linear part $u_{pa1}(n)$ are as follows,

$$u_{pa1}(n) = \left[u_{pa}(n)u_{pa}(n-1)u_{pa}(n-2)\right] \tag{6.23}$$

and the elements of the quadratic part $u_{pa2}(n)$ are as follows,

$$u_{pa2}(n) = \begin{bmatrix} u_{pa}(n)u_{pa}(n) & u_{pa}(n)u_{pa}(n-1) & u_{pa}(n)u_{pa}(n-2) \\ u_{pa}(n-1)u_{pa}(n) & u_{pa}(n-1)u_{pa}(n-1) & u_{pa}(n-1)u_{pa}(n-2) \\ u_{pa}(n-2)u_{pa}(n) & u_{pa}(n-2)u_{pa}(n-1) & u_{pa}(n-2)u_{pa}(n-2) \end{bmatrix} \tag{6.24}$$

The sum of weight coefficients of linear part $u_{pa1}(n)$ in eqn. (6.22) and quadratic part in eqn. $u_{pa2}(n)$ gives the set of weight vector $w_{pa}(n)$ with respect to their linear and quadratic input vectors $i_{pLa}(n)$ and is expressed as,

$$w_{pa}(n) = u_{pa1}(n) + u_{pa2}(n) + \varepsilon_1 \tag{6.25}$$

Using eqns. (6.24) and (6.25), the output of the AVSF for estimation of the magnitude of the fundamental load active current component i_{pa} for n^{th} sampling instant is given as,

$$i_{pa}(n) = w_{pa}^{T}(n)i_{pLa}(n) \tag{6.26}$$

Due to the presence of quadratic parts, the resultant value of the output $i_{pa}(n)$ comes in the higher range, which can be made threshold within 0 and 1 with the help of sigmoidal function. Hence, the resultant value of i_{pa} lies within the threshold limits. Comparison of this value with the desired value i.e. maximum threshold limit (d_p=1) results into an error signal $e(n)$, which is expressed as,

$$e(n) = d_p(n) - i_{pa}(n) \tag{6.27}$$

This signal has been used in the LMS algorithm to update the weight coefficient, given as,

$$w_{pa}(n+1) = w_{opa}(n) + \mu e(n) i_{pLa}(n) \tag{6.28}$$

Where the step size (μ) is taken as 0.5 but it can also be obtained from [163]. The optimal value of weight coefficient $w_{pa}(n)$ is calculated as in [164] to minimize MSE, and is expressed as,

$$w_{opa}(n) = {i_{ap}}^{-1} p \tag{6.29}$$

Where i_{ap} is the covariance matrix of filter input vector i_{pLa} and the vector p is the cross correlation vector between the i_{pLa} and d_p which is expressed as,

$$p = E\left[d_p(n) i_{pLa}(n)\right] \tag{6.30}$$

The term i_{ap} in eqn. (6.29) is the inverse of autocorrelation function of the input vector i_{pLa}, given as,

$$i_{ap} = E\left[{i_{pLa}}^{*}(n) {i_{pLa}}^{T}(n)\right] \tag{6.31}$$

Where i_{ap} is usually positive definite, and is a necessary condition for the convergence. The rate of convergence depends on Eigen value of i_{ap}.

Fig. 6.4 shows functional layout of the proposed AVSF based control algorithm to generate reference template for switching DSTATCOM. To estimate the active current components amplitude of the reference template, sensed load currents at PCC are inputs to AVSF. The in-phase unit templates are weight coefficients of the input vector, which are estimated from eqn. (6.18), respectively. Active current components amplitude i_{pLa}, i_{pLb} and i_{pLc} of all phases are estimated separately. Phase 'a' fundamental active current component amplitude i_{pa} of the reference template is estimated using eqn. (6.26). Likewise other phases 'b' and 'c' are also estimated.

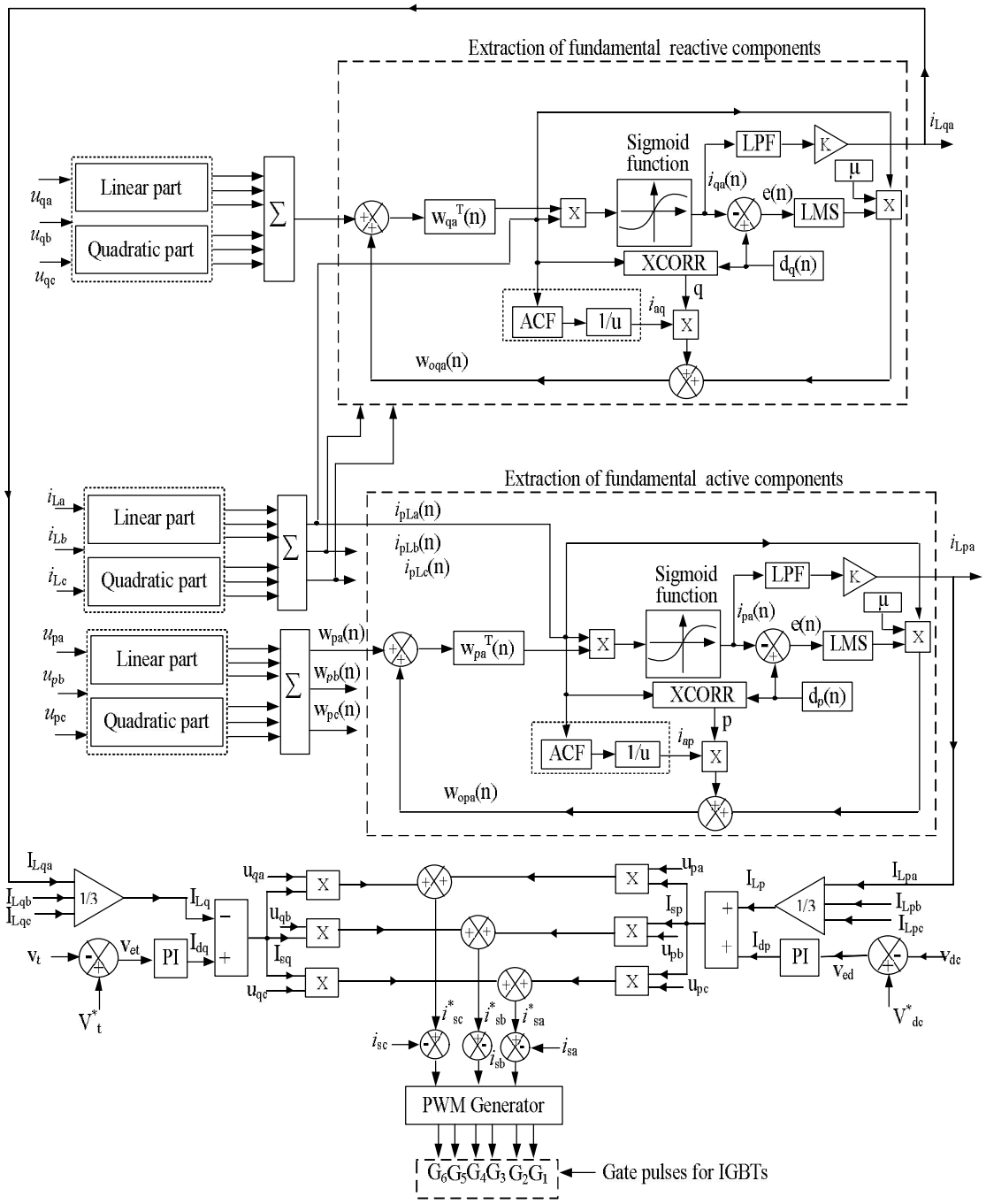


Fig. 6.4 Functional layout of the proposed AVSF based control algorithm to generate reference template for switching DSTATCOM

A second-order LPF (low-pass filter) is used to separate the low-frequency components of i_{ap}. The actual value of fundamental load active current component i_{Lpa} is obtained by multiplying LPF output with scaled factor '*K*'.

Similarly, i_{Lpb} and i_{Lpc} for phases 'b' and 'c' respectively are calculated. The mean amplitude of fundamental load active current component $I_{Lp}(n)$ at n^{th} sampling instant is expressed as,

$$I_{Lp} = \frac{(i_{Lpa} + i_{Lpb} + i_{Lpc})}{3} \tag{6.32}$$

The low-frequency components of I_{Lp} are suppressed using second order LPF.

The error of DC-link bus voltage V_{ed} of DSTATCOM is determined by comparing the reference V_{dc}^{*} with actual V_{dc} value of DC-bus voltage at n^{th} sampling instant, which is given as,

$$V_{ed}(n) = V_{dc}^{*}(n) - V_{dc}(n) \tag{6.33}$$

The DC-link bus voltage is maintained at a constant level by feeding the error to proportional–integral (PI) controller. The PI controller output to DC bus voltage $V_{ed}(n)$ is given as,

$$I_{dp}(n) = I_{dp}(n-1) + K_{pd}\{V_{ed}(n) - V_{ed}(n-1)\} + K_{id}V_{ed}(n) \tag{6.34}$$

Where proportional (K_{pd}) and integral (K_{id}) are the PI controller gain constants, $V_{ed}(n)$ and $V_{ed}(n-1)$ are error values of DC bus voltage, and $I_{dp}(n)$ is considered as an active component of source current at $(n-1)^{th}$ and n^{th} sampling instants, respectively.

The active current component amplitude of reference source current I_{sp} is obtained as,

$$I_{sp} = I_{Lp} + I_{dp} \tag{6.35}$$

6.5.2 Amplitude Estimation of Fundamental Load Reactive Current Components

Fundamental reactive current component i_{Lq} of each phase is estimated by taking sensed load currents i_L as input vectors and quadrature templates ($u_{qa}, u_{qb}, \text{and } u_{qc}$). The quadrature templates are calculated using in-phase templates ($u_{pa}, u_{pb}, \text{and } u_{pc}$), which are the weight coefficients of input vectors i_{qL} of AVSF. The amplitude of each phase fundamental reactive component is estimated separately and designated as i_{qLa}, i_{qLb} and i_{qLc}, respectively. For simplicity, only magnitude of the fundamental reactive current component i_{qLa} of phase 'a' is mathematically described while other two phase components are directly assigned. Primarily, phase 'a' load current $i_{La}(n)$ as input vector at n^{th} sampling instant is decomposed by AVSF. The estimation of linear and quadratic parts of the load currents is obtained using eqns. (6.20)-(6.22), respectively. The quadrature unit templates ($u_{qa}, u_{qb}, \text{and } u_{qc}$) are estimated as,

$$u_{qa} = \frac{(-u_{pb}+u_{pc})}{\sqrt{3}}, u_{qb} = \frac{(3u_{pa}+u_{pb}-u_{pc})}{2\sqrt{3}}, u_{qc} = \frac{(-3u_{pa}+u_{pb}-u_{pc})}{2\sqrt{3}} \tag{6.36}$$

As the coefficient weight vectors are defined in eqns. (6.23)-(6.24), the coefficients of both parts (linear and quadratic) of the reactive weight vectors are given as,

$$u_{qa1}(n) = \left[u_{qa}(n)u_{qa}(n-1)u_{qa}(n-2)\right] \tag{6.37}$$

$$u_{qa2}(n) = \begin{bmatrix} u_{qa}(n)u_{qa}(n) & u_{qa}(n)u_{qa}(n-1) & u_{qa}(n)u_{qa}(n-2) \\ u_{qa}(n-1)u_{qa}(n) & u_{qa}(n-1)u_{qa}(n-1) & u_{qa}(n-1)u_{qa}(n-2) \\ u_{qa}(n-2)u_{qa}(n) & u_{qa}(n-2)u_{qa}(n-1) & u_{qa}(n-2)u_{qa}(n-2) \end{bmatrix} \tag{6.38}$$

The sum of eqns. (6.37) and (6.38) is the weight coefficients $w_{qa}(n)$ of input vectors, expressed as,

$$w_{qa}(n) = u_{qa1}(n) + u_{qa2}(n) \tag{6.39}$$

The weight coefficients vector $w_{qa}(n)$ can be shown similar to Fig. 6.3(b). The AVSF output is the fundamental load reactive current component i_{qa} which is estimated using eqns. (6.22) and (6.39), given as,

$$i_{qa}(n) = w_{qa}^{T}(n) i_{qLa}(n) \tag{6.40}$$

The obtained output i_{qa} is compared with the desired value d_q to get the error signal which is given as,

$$e(n) = d_q(n) - i_{qa}(n) \tag{6.41}$$

Error signal $e(n)$ is used to update the filter coefficients w_{qa} of AVSF as,

$$w_{qa}(n+1) = w_{oqa}(n) + \mu e(n) i_{qLa}(n) \tag{6.42}$$

The optimal value of weight coefficient $w_{qa}(n)$ is calculated to minimize MSE, and is expressed as,

$$w_{oqa}(n) = {i_{aq}}^{-1} q \tag{6.43}$$

Where i_{aq} is the covariance matrix of filter input vector i_{qLa} and the vector q is the cross correlation vector between the i_{qLa} and d_q which is expressed as,

$$q = E\left[d_q(n) i_{qLa}(n)\right] \tag{6.44}$$

The term i_{aq} in eqn. (6.43) is the inverse of auto-correlation function of the input vector i_{qLa}, given as,

$$i_{aq} = E\left[{i_{qLa}}^{*}(n) {i_{qLa}}^{T}(n)\right] \tag{6.45}$$

i_{aq} is usually positive definite, and is a necessary condition for the convergence. The rate of convergence depends on Eigen value of i_{aq}. Fig.6.4 shows the block diagram to update

weight coefficients for load reactive fundamental current component for phase 'a', which minimizes the error.

Similarly, the estimation is carried out for the other two phases 'b' and 'c' to find out the actual fundamental reactive current components 'i_{qb}'and 'i_{qc}'. The mean amplitude of fundamental reactive current component $I_{Lq}(n)$ at n^{th} sampling is calculated as,

$$I_{Lq} = \frac{(i_{Lqa} + i_{Lqb} + i_{Lqc})}{3} \tag{6.46}$$

The estimated mean amplitude of the fundamental reactive current component I_{Lq} also contains low-frequency components, which are suppressed with the help of second-order LPF.

The behavior of the AC bus under consideration at PCC is taken to obtain the reactive current component amplitude. The error signal of AC-bus voltage V_{et} at PCC is the difference between reference value V_t^* and sensed value V_t and its value at n^{th} sampling instant is expressed as,

$$V_{et}(n) = V_t^*(n) - V_t(n) \tag{6.47}$$

The rated value of terminal voltage of the AC bus at PCC is maintained constant by feeding the error to PI controller, expressed as,

$$I_{qt}(n) = I_{qt}(n-1) + K_{pt}\{V_{et}(n) - V_{et}(n-1)\} + K_{it}V_{et}(n) \tag{6.48}$$

Where $V_{et}(n-1)$ and $V_{et}(n)$ are voltage error values at $(n-1)^{th}$ and n^{th} sampling instants and $I_{qt}(n-1)$ and $I_{qt}(n)$ are the magnitudes of the fundamental reactive power current components of the reference source current. The values of proportional and integral constants K_{pt} and K_{it} of PI controller are directly calculated with the help of Ziegler-Nichols method in [120].

The total reactive current component (I_{sq}) value of reference source current is expressed as,

$$I_{sq} = I_{qt} - I_{Lq} \tag{6.49}$$

6.5.3 Generation of Switching Gate Pulses for DSTATCOM

The reference fundamental source currents are calculated by taking amplitude of active load current components I_{sp} and reactive load current components I_{sq} with the unit templates (in-phase and quadrature). The products of power current components with both unit templates for each phase are given as,

$$i_{spa} = I_{sp}u_{pa}, \qquad i_{spb} = I_{sp}u_{pb}, \qquad i_{spc} = I_{sp}u_{pc} \tag{6.50}$$

$$i_{sqa} = I_{sq}u_{qa}, \qquad i_{sqb} = I_{sq}u_{qb}, \qquad i_{sqc} = I_{sq}u_{qc} \tag{6.51}$$

The reference source current for each phase is calculated by adding the reference source components (active and reactive) as,

$$i_{sa}^{*} = i_{spa} + i_{sqa}, \qquad i_{sb}^{*} = i_{spb} + i_{sqb}, \qquad i_{sc}^{*} = i_{sqa} + i_{sqc} \tag{6.52}$$

The above reference source currents ($i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*}$) are compared with sensed source currents (i_{sa}, i_{sb}, i_{sc}) to calculate the error. The error signal of each phase is fed to PWM current controller which results into gating pulses to DSTATCOM.

6.6 RESULTS AND DISCUSSION

The AVSF based control algorithm for DSTATCOM is developed in SIMULINK of MATLAB for 3-phase distribution system. Case studies are demonstrated for power factor improvement to unity and for regulation of the AC bus voltage at PCC under linear and nonlinear load conditions. The THDs (Total Harmonic Distortions) of source currents are found under standard limit.

6.6.1 Performance of DSTATCOM in PFC Mode

The proposed algorithm is implemented successfully in a three phase distribution system delivering power to linear and nonlinear loads under balanced and unbalanced load conditions to control DSTATCOM. The performance of DSTATCOM using AVSF based control algorithm is validated by simulation as well as experimentation. The PFC mode function of DSTATCOM using AVSF algorithm have been carried out and presented here.

6.6.1.1 Simulation results at nonlinear load conditions

The performance results of DSTATCOM at nonlinear load under balanced and unbalanced load conditions are shown in Fig. 6.5. The sensed parameters of the developed test system are PCC voltage (v_s), source currents (i_s), load currents (i_{La}, i_{Lb}, and i_{Lc}), compensating currents (i_{Ca}, i_{Cb}, i_{Cc}), estimated reference source currents (i_{xs}), amplitude of AC bus voltage (V_t) and DC link voltage of DSTATCOM (V_{dc}). The load of phase 'a' is removed at t=1.1s and injected at t=1.3s under unbalanced load conditions. Due to unbalancing in the load, the amplitude of the DC bus voltage (V_{dc}) is kept to the reference level using discrete PI controller. In this mode, the reference source currents (i_{xs}) have active power current components i_{Lp}, that makes the switching of DSTATCOM. At the same instant the amplitude of the AC bus voltage (V_t) fluctuates from its reference value. The AC bus voltages and currents are brought in the same phase at unity power factor under nonlinear load conditions by current compensation provided by DSTATCOM at PCC.

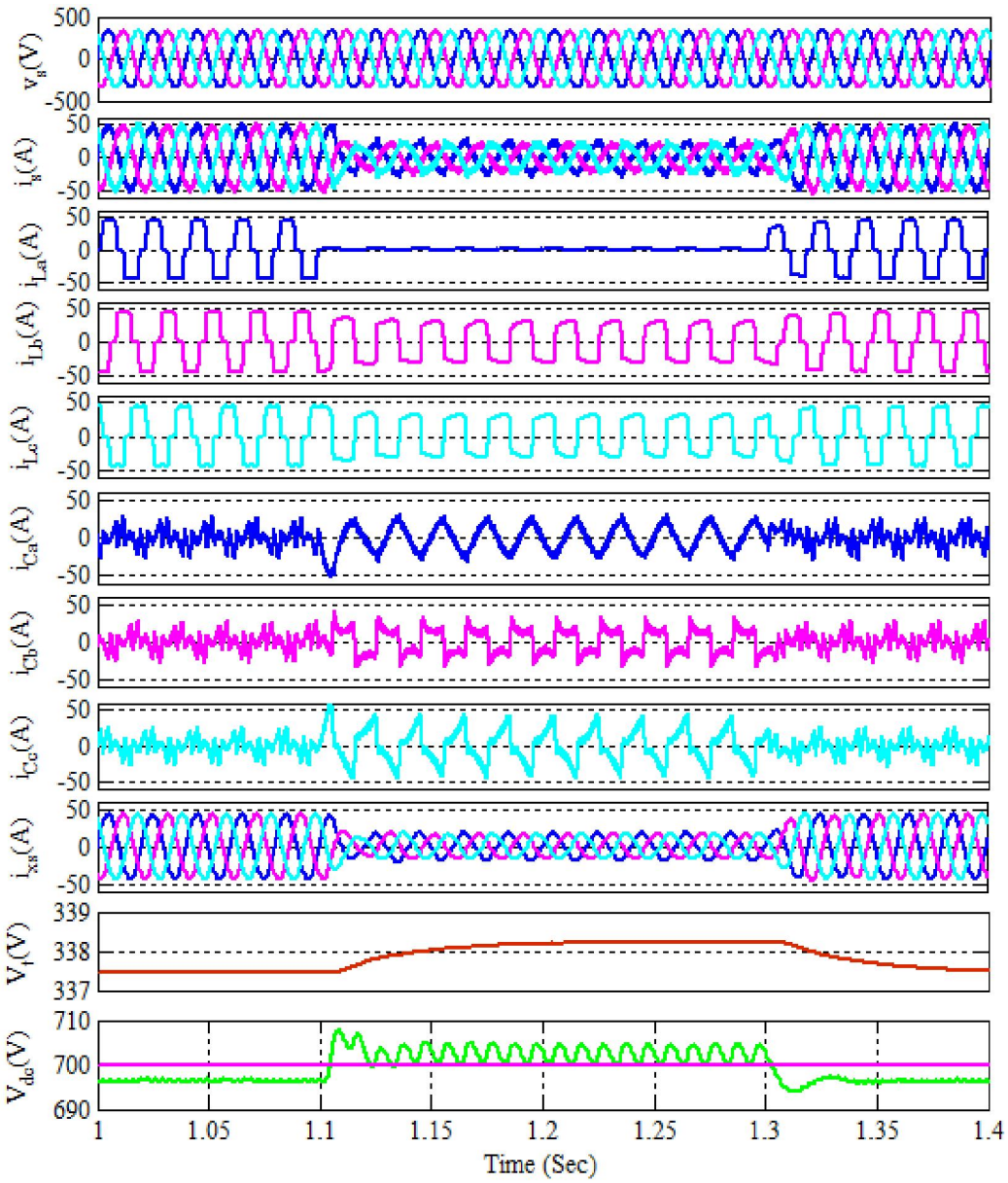


Fig. 6.5 Performance of DSTATCOM at nonlinear load

6.6.1.2 Simulation results at linear load conditions

The performance results of DSTATCOM at linear load under balanced and unbalanced load conditions are shown in Fig. 6.6. The sensed parameters of the developed test system are PCC voltage (v_s), source currents (i_s), load currents ($i_{La}, i_{Lb},$ and i_{Lc}), compensating currents (i_{Ca}, i_{Cb}, i_{Cc}), estimated reference source currents (i_{xs}), amplitude

of AC bus voltage (V_t) and DC link voltage of DSTATCOM (V_{dc}). The load of phase 'a' is removed at t=1.1s and injected at t=1.3s for unbalancing the load conditions.

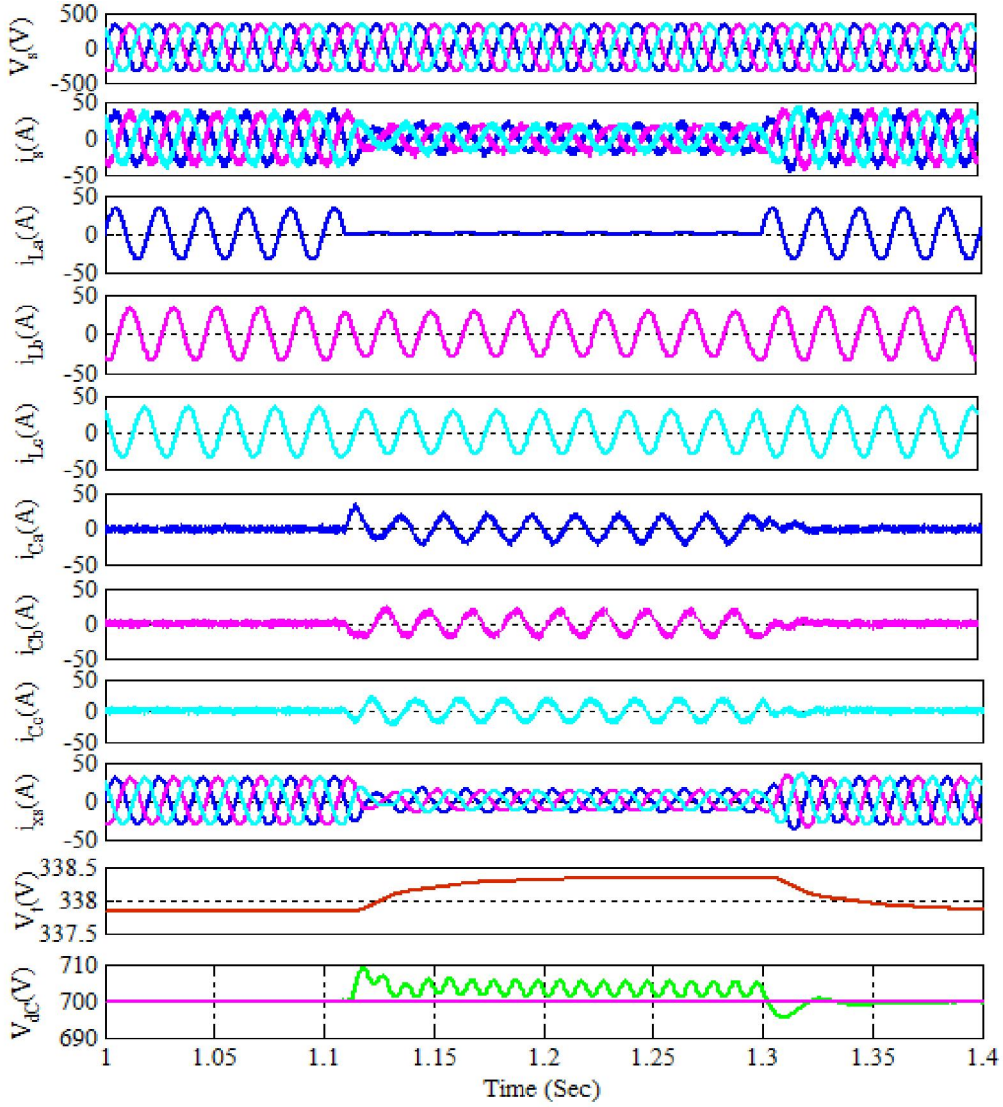


Fig. 6.6 Performance of DSTATCOM at linear load

Fig. 6.7 shows the performance results of the intermediate signals of the proposed AVSF algorithm in PFC mode. The sensed parameters are PCC voltage (v_{pcc}), source current (i_{sa}), load current (i_{La}), compensating source current (i_{Ca}), linear (i_{La1}) and quadratic parts (i_{La2}) of load current (i_{La}), the extracted fundamental active current component (i_{pLa}) and estimated weighted active fundamental current component (i_{pa}) after passing

through sigmoidal function, actual weighted fundamental load active current component (i_{Lpa}) after scaling of phase 'a', with DC-link voltage (V_{dc}), after switching ON of DSTATCOM.

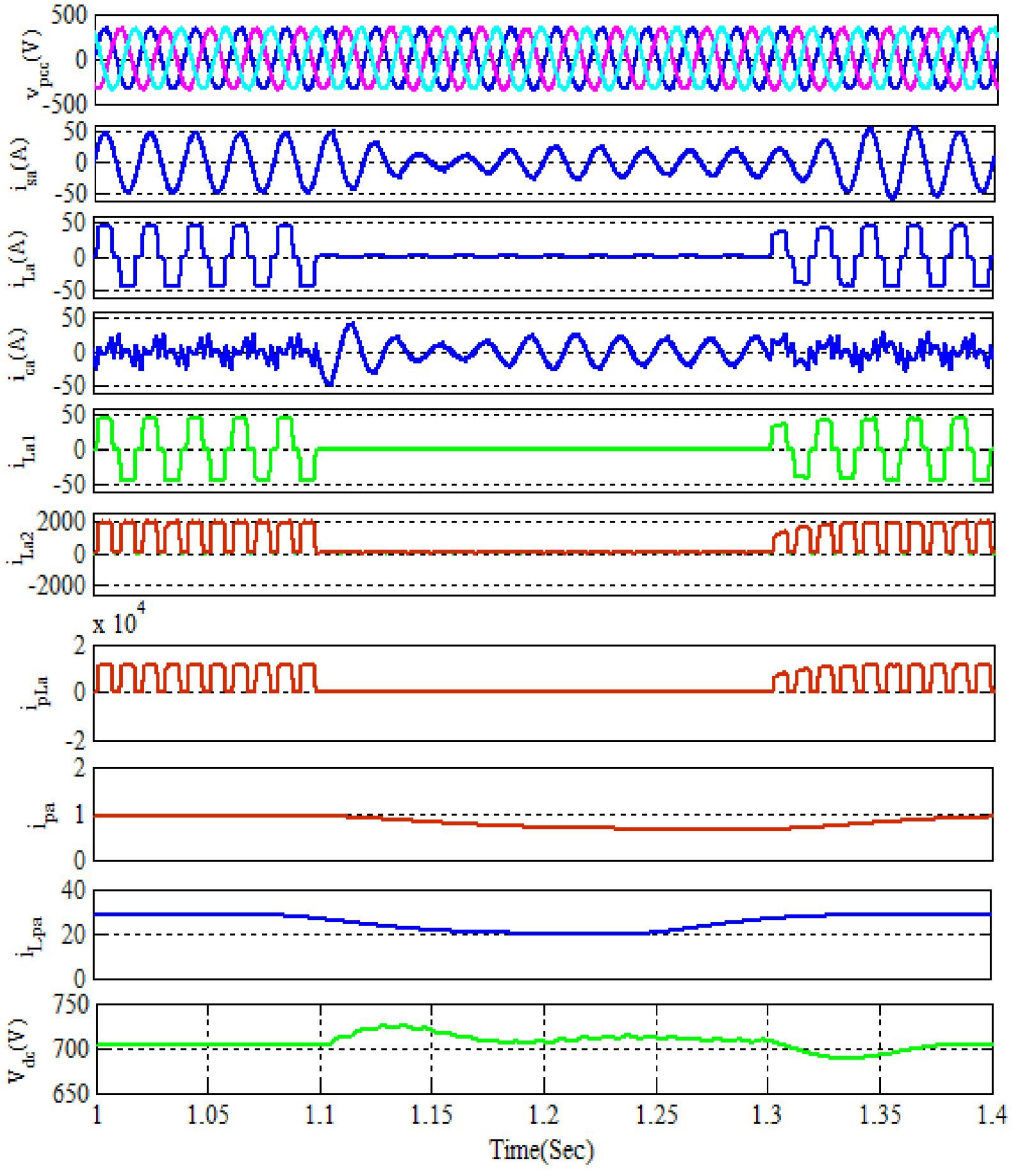


Fig. 6.7 Intermediate signals at nonlinear load

Fig. 6.8 shows the waveforms and harmonic spectra of source voltage (v_{sa}), source current (i_{sa}) and load current (i_{La}) of phase 'a' in PFC mode. The source voltage and current of phase 'a' are brought in same phase to achieve the unity power factor, whereas

the % THDs indicates the power quality of the test system. Since the load is nonlinear, the source current is non sinusoidal, therefore, when DSTATCOM is switched ON, the harmonics of the source current is also eliminated at PCC resulting into sinusoidal source current. The measured THDs of phase 'a' are seen from the recorded harmonic spectra and waveform, observed as 1.99% for source voltage(v_{sa}), 2.63% for source current (i_{sa}), and 24.14% for load current (i_{La}), which are within the desired IEEE-519 standard limit and are given in Table 6.2.

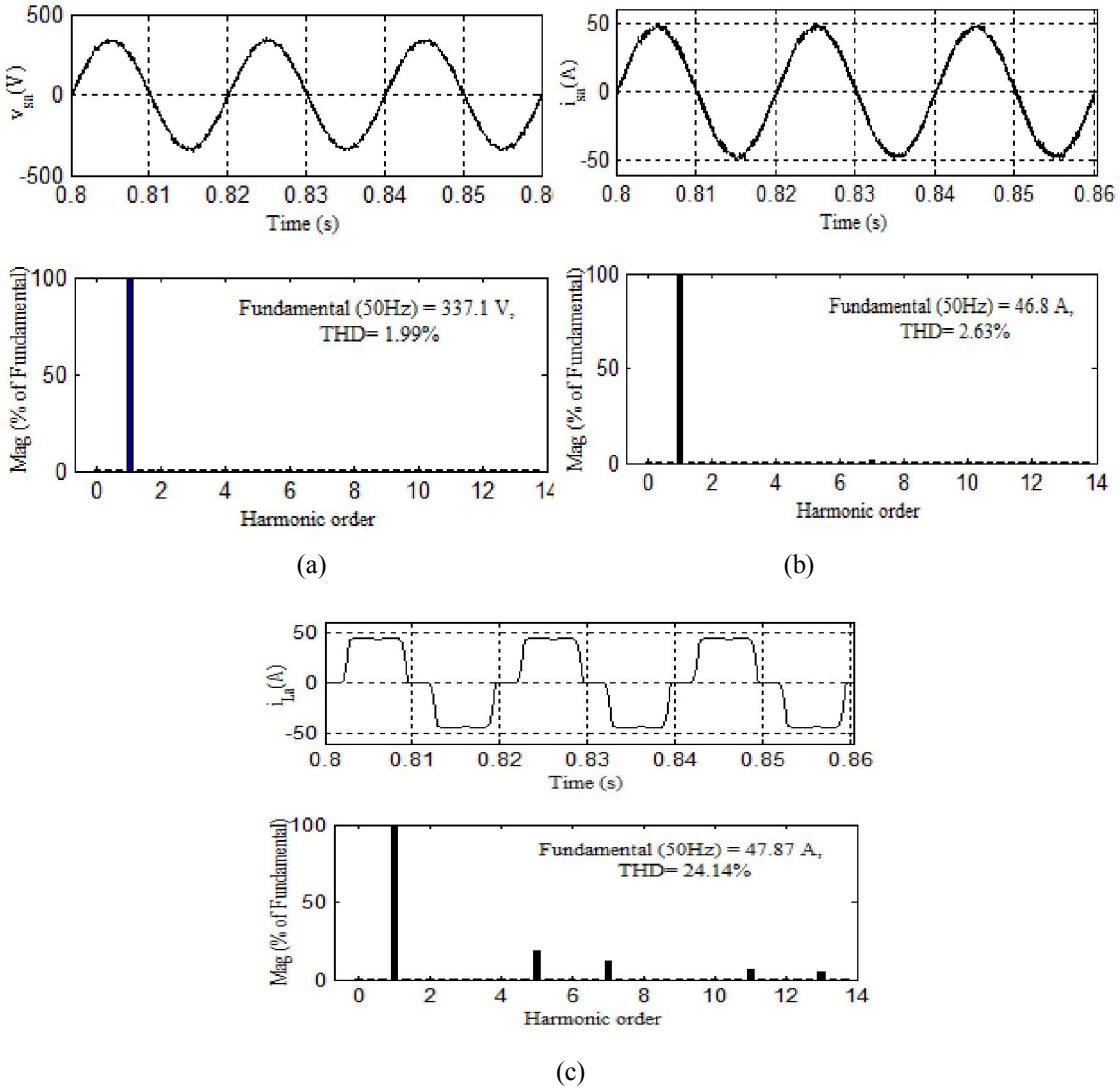


Fig. 6.8 Waveforms and harmonic spectra (a) Source voltage v_{sa} (b) Source current i_{sa} (c) Load current i_{La}, of phase 'a'

Table 6.2 Simulated performance results of AVSF based control algorithm

Modes of operation	Performance parameters at PCC	3-phase bridge rectifier with series RL connected load
Power factor correction (PFC) mode	Grid voltage (V), %THD	337.1V, 1.99%
	Grid current (A), %THD	46.8 A, 2.63%
	Load current (A), %THD	47.87 A, 24.14%
Zero voltage regulation (ZVR) mode	Grid voltage (V), %THD	338.4 V, 1.83%
	Grid current (A), %THD	47.14 A, 3.19%
	Load current (A), %THD	48.07 A, 24.18%
	DC bus voltage (V)	700 V

6.6.2 Performance of DSTATCOM in ZVR Mode

The rated value of the AC bus at PCC is maintained at nonlinear load under balanced and unbalanced load conditions using DSTATCOM. In this mode, the reference fundamental source currents (i_{xs}), constitute of extracted active (i_{Lpa}), and reactive (i_{Lqa}) power current components for switching of DSTATCOM. The performance of DSTATCOM with this control algorithm is validated by simulation as well as experimentation.

6.6.2.1 Simulation results at nonlinear load conditions

Fig. 6.9 shows the performance parameters of DSTATCOM in ZVR mode under balanced and unbalanced load conditions. The parameters are PCC voltage (v_s), source currents (i_s), load currents (i_{La}, i_{Lb}, and i_{Lc}), compensating currents (i_{Ca}, i_{Cb}, i_{Cc}), estimated

reference source currents (i_{xs}), amplitude of AC bus voltage (V_t) and DC link voltage of DSTATCOM (V_{dc}).

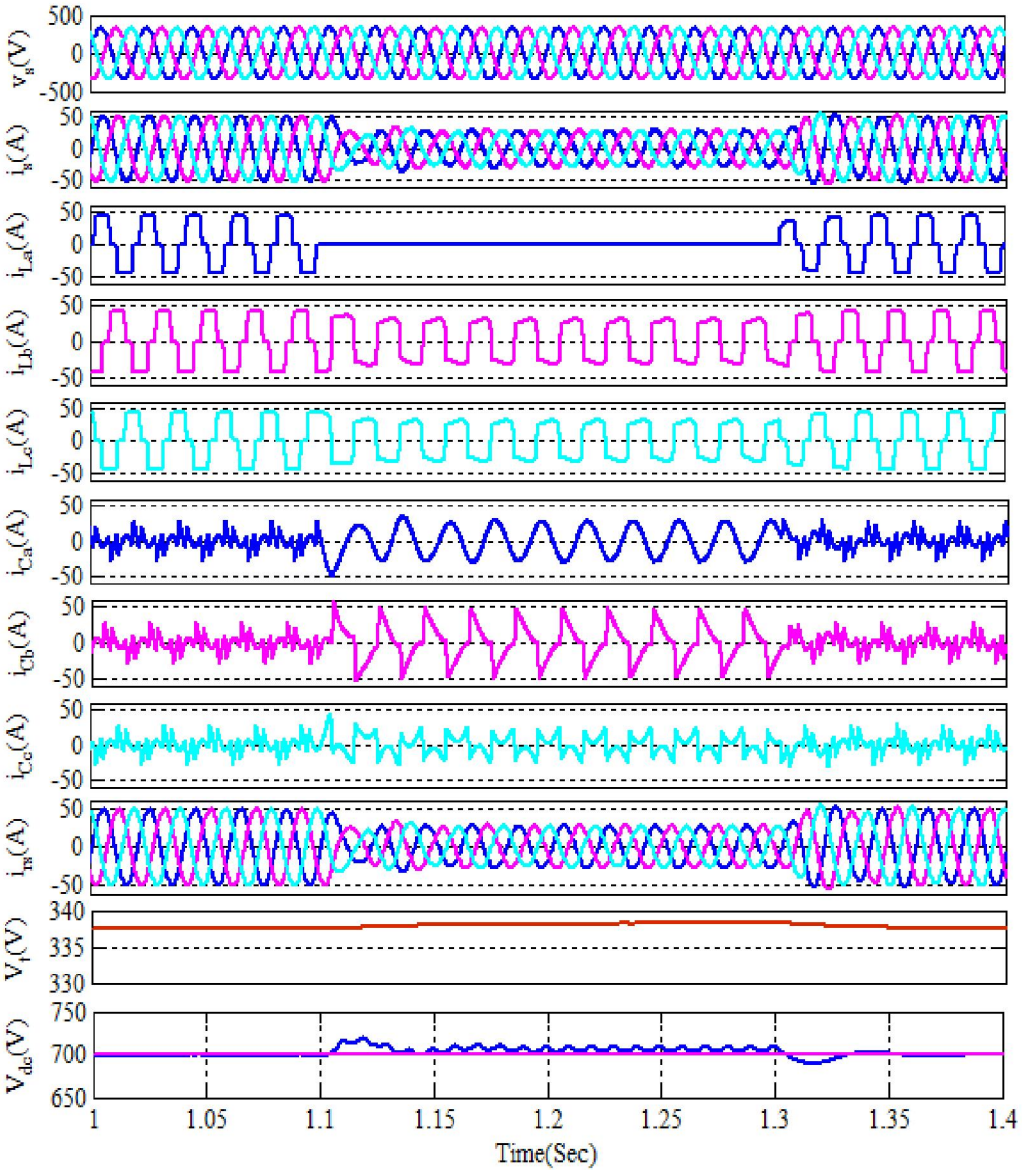


Fig. 6.9 Performance indices of DSTATCOM at nonlinear load

The load of phase 'a' is removed at t=1.1s and injected at t=1.3s under unbalanced load conditions. Due to unbalancing in the load, the amplitude of the AC bus voltage (V_t) is maintained to the reference level using discrete PI controller. In this mode, the reference source current (i_{xs}), has active (i_{Lpa}) and reactive (i_{Lqa}) power current components, that

makes the switching of DSTATCOM. The amplitude of the AC bus voltage (V_t) is brought to the reference voltage at nonlinear load conditions due to current compensation provided by DSTATCOM at PCC. Moreover, the load balancing is also done here.

6.6.2.2 Simulation results at linear load conditions

Fig. 6.10 shows the performance parameters of DSTATCOM in ZVR mode at linear load condition under balanced and unbalanced load conditions.

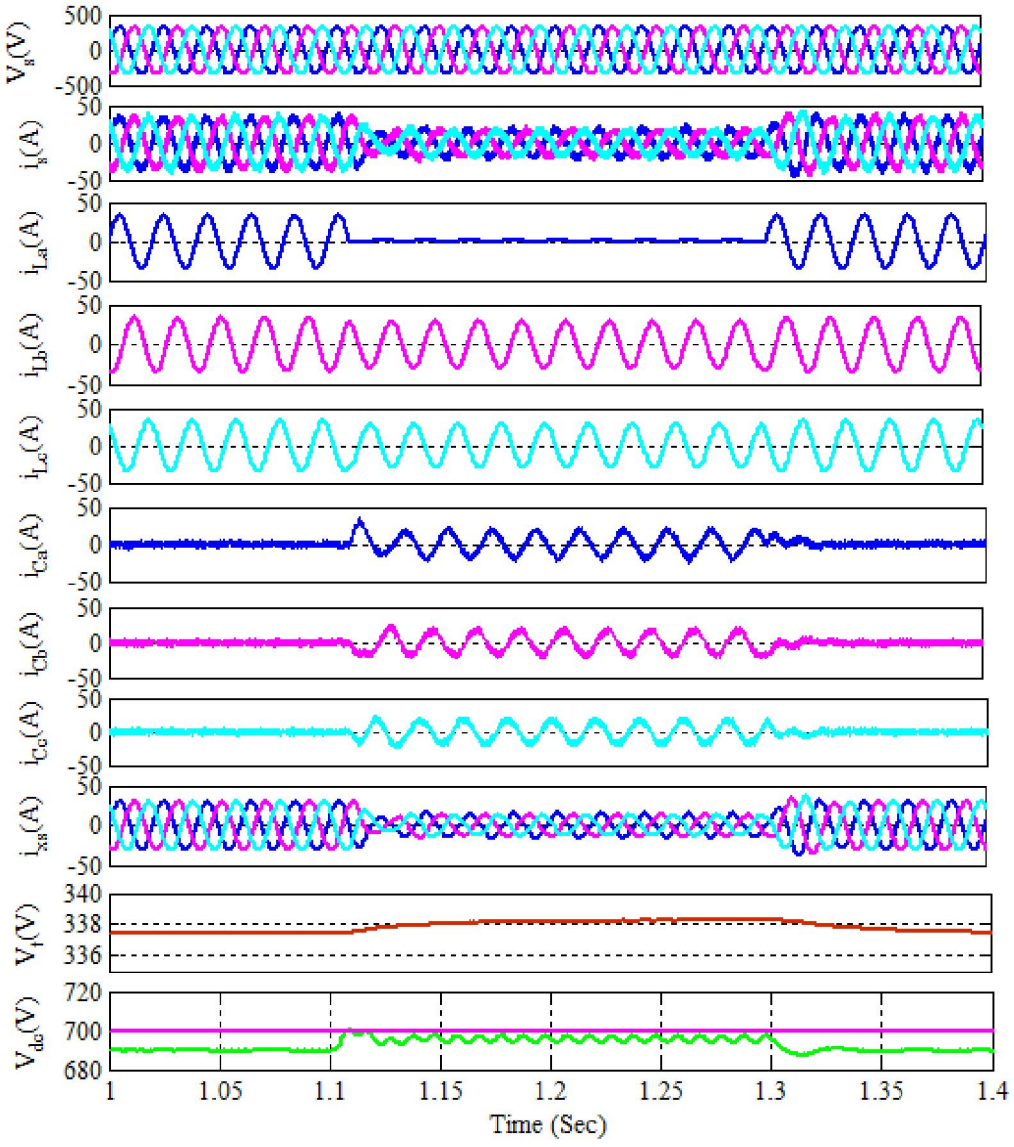
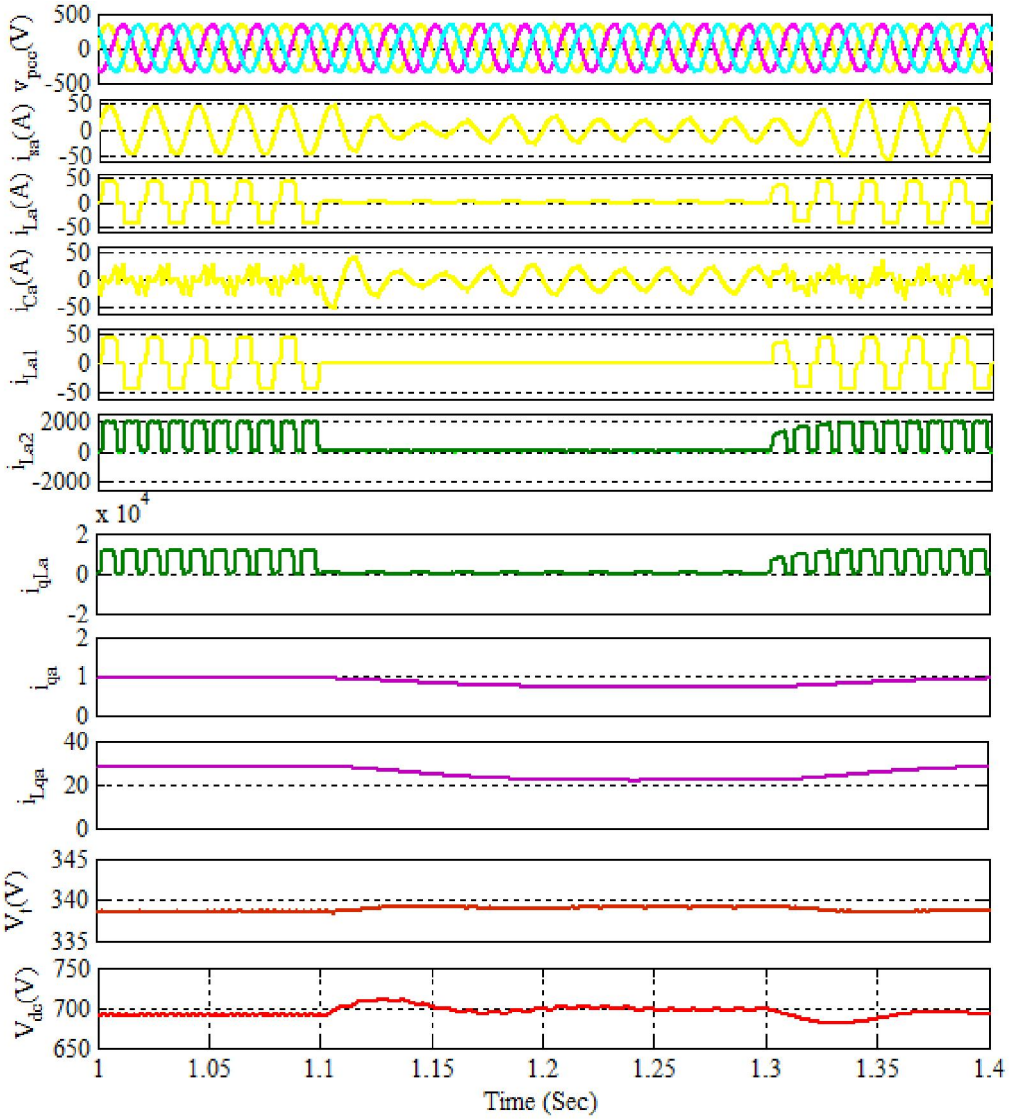


Fig. 6.10 Performance indices of DSTATCOM at linear load

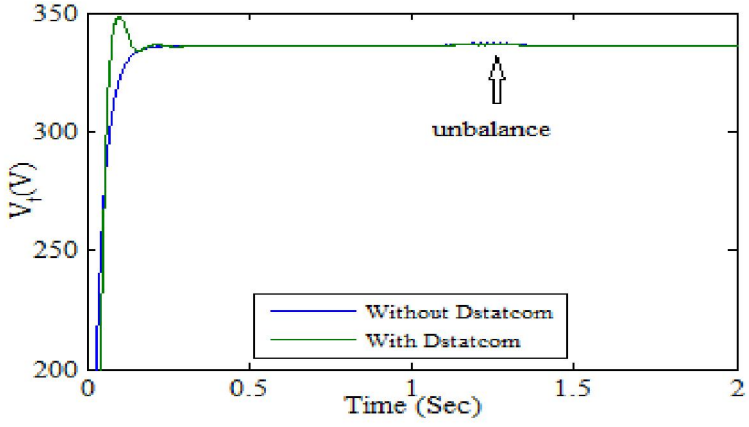
The parameters are PCC voltage (v_s), source currents (i_s), load currents (i_{La}, i_{Lb}, and i_{Lc}), compensating source currents (i_{Ca}, i_{Cb}, i_{Cc}), estimated reference source currents (i_{xs}), amplitude of AC bus voltage (V_t) and DC link voltage of DSTATCOM (V_{dc}).

Fig. 6.11 shows the intermediate signals of the proposed algorithm. The sensed parameters are PCC voltage (v_{pcc}), source current (i_{sa}), load current (i_{La}), compensating source current (i_{Ca}), linear (i_{La1}) and quadratic parts (i_{La2}), of decomposed load current (i_{La}) of phase 'a', extracted fundamental load reactive current component (i_{qLa}), weighted fundamental reactive current component (i_{qa}) after transforming through sigmoidal function, and extracted actual value of fundamental load reactive current component (i_{Lqa}) after scaling of phase 'a' with terminal voltage of PCC (V_t) and DC-link voltage (V_{dc}), which are presented in Fig. 6.11(a).

The zero voltage regulation (ZVR) is achieved as the terminal voltage at PCC is maintained to its rated value with compensation provided by DSTATCOM during dynamic conditions of nonlinear load. From these obtained results of the performance parameters, the effectiveness of the proposed algorithm is established to regulate the AC bus voltage in a three phase distribution system with DSTATCOM under nonlinear load conditions in zero voltage regulation mode as shown in Fig. 6.11 (b).



(a)



(b)

Fig. 6.11 Performance parameters of DSTATCOM (a) Intermediate signals (b) Voltage regulation of AC bus voltage with and without DSTATCOM

Fig. 6.12 shows the waveforms and harmonic spectra of source voltage(v_{sa}), source current (i_{sa}), and load current (i_{La}) of phase 'a' in ZVR mode. The measured THDs of source voltage(v_{sa}), source current (i_{sa}), and load current (i_{La}) of phase 'a' are obtained from the recorded harmonic spectra and waveforms, observed as 1.83% for source voltage (v_{sa}), 3.19% for source current (i_{sa}), and 24.18% for load current (i_{La}), which are within the desired IEEE-519 standard limit, and given in Table 6.2.

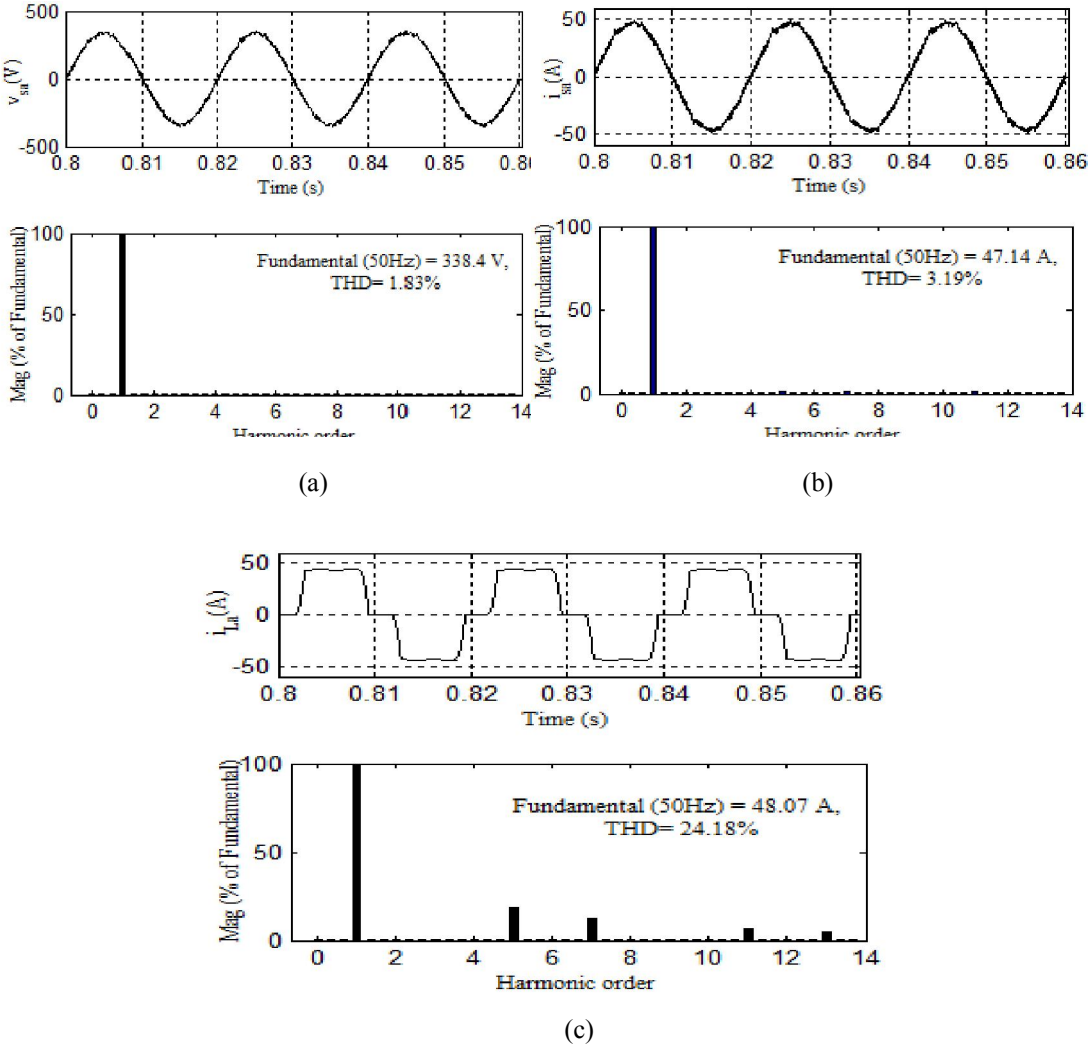


Fig. 6.12 Waveforms and harmonic spectra (a) Source voltage v_{sa} (b) Source current i_{sa} (c) Load current i_{La}, of phase 'a'

6.6.3 Experimental Results in PFC Mode

The test system for simulation and experimental configuration is shown in Fig. 6.1. The prototype is developed in the laboratory using different electrical components such as three phase balanced AC grid, interfacing inductor, VSC as DSTATCOM, RC ripple filter, diode rectifier module of Semikron make SKD-85 as nonlinear load and RL series circuit as a linear load. Hall Effect current sensors (LA25P) and voltage sensors (LV25P) are used to sense the required current and voltage signals for algorithm. A level shifter using IC OP07C is required for sensor's signal amplification followed by signal conditioning circuit to input signals through ADC of dSPACE 1104 (DSP processor) for execution of AVSF algorithm. Using these signals, the DSTATCOM is controlled in above mentioned both PFC and ZVR modes by implementing the proposed algorithm. A Keysight make 4-channel DSO-X-2024A and power analyser of Fluke (435) are used for recording of waveforms. Performance results of AC grid under nonlinear and linear loads are found satisfactory. The specification of hardware is given in Table 6.1. Sample time of 40 μs is taken for the proposed AVSF algorithm for hardware implementation using DSP processor dSPACE 1104. The proposed AVSF algorithm has successfully brought the THDs of grid within its specified limit.

6.6.3.1 Test performance of DSTATCOM at nonlinear load

Fig.6.13 shows the captured waveforms by power analyzer (Fluke make 534 series) of source voltages v_s and source currents i_s with their THDs before and after switching ON the DSTATCOM using the proposed AVSF based control algorithm. Before switching the DSTATCOM, the captured waveforms of source voltages v_s and source currents i_s are shown in Fig.6.13(a)-(b), while correspondingly THDs of the source voltages v_s is

3.5% and source currents is 25.2%, respectively, as shown in Fig. 6.13(c)-(d). When the DSTATCOM is switched ON, DSTATCOM injects the compensating currents i_C at PCC making the source current sinusoidal with reduced THDs 6.7%, which is acceptable considering the combination of many laboratory equipments. The captured waveform of source currents is and its THDs are shown in Figs. 6.13(e)-(f), respectively.

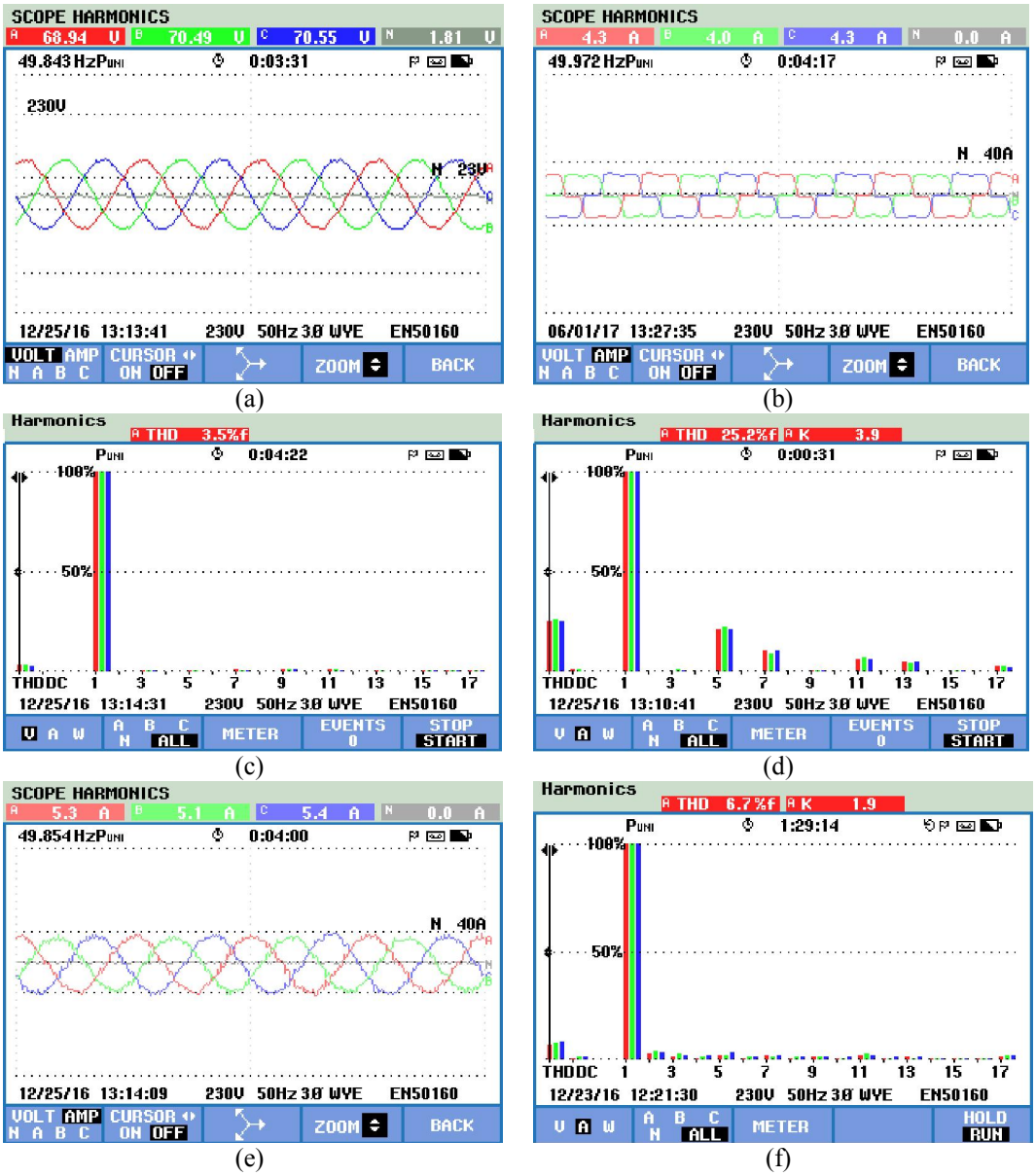
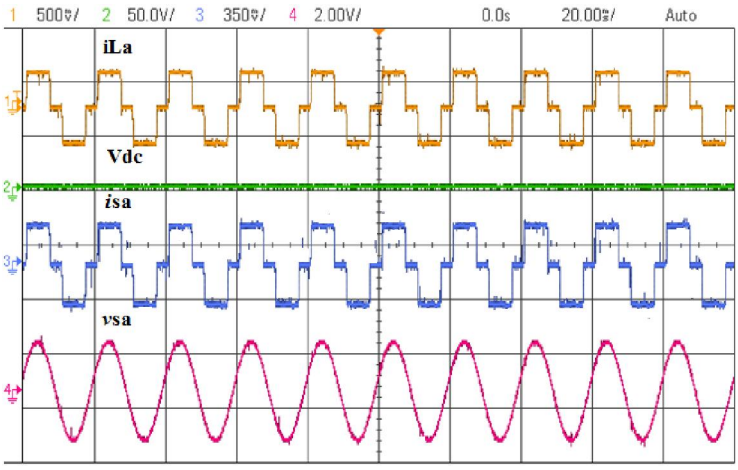


Fig. 6.13 Performance parameters of test system (a) Source voltages v_s (b) Source currents i_s (c) %THDs of v_s (d) %THDs of i_s, for all phases, when DSTATCOM is in OFF state (e) Source currents i_s (f) %THDs of i_s, when DSTATCOM is switched ON

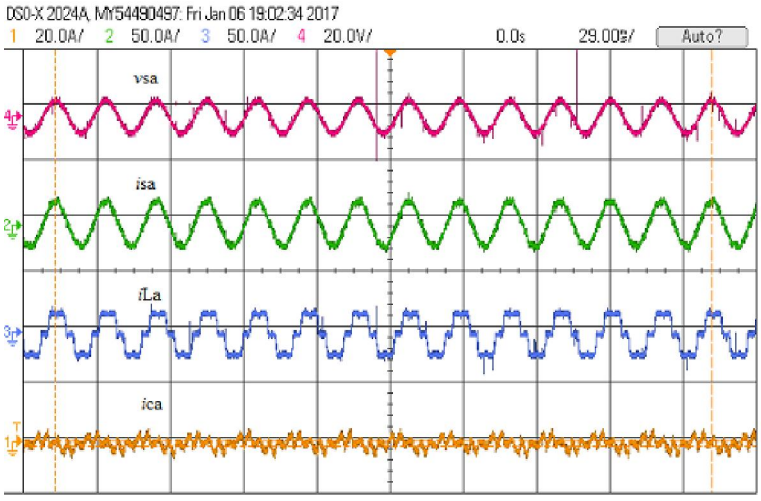
The obtained %THDs reveal that the proposed AVSF algorithm is quite effective to control the DSTATCOM in order to eliminate the harmonics from the source current and to maintain the waveform sinusoidal for all phases (a, b, and c). The mitigation of harmonics by DSTATCOM results into sinusoidal source currents even for nonlinear load conditions as shown in Fig. 6.13(e). The % THDs of the source currents are found 6.7 %, due to the limitations of laboratory equipments, which is closer to allowable standard limit as shown in Fig. 6.13 (f), respectively.

Fig. 6.14 (a) shows the captured sensed signals including load current i_{La}, DC- bus voltage V_{dc} of DSTATCOM, source current i_{sa} and source voltage v_{sa} at PCC of phase 'a' before switching ON the DSTATCOM, on DSO (Keysight make 2024A) from dSPACE 1104. It is observed from Fig. 6.14 (a) that the source current i_{sa} and load current i_{La} of phase 'a' are non-sinusoidal. Fig. 6.14 (b) shows the source voltage v_{sa}, source current i_{sa}, load current i_{La} and compensating current i_{Ca} of phase 'a'. It is observed from Fig. 6.14 (b) that when the DSTATCOM is switched ON, the injected compensating currents from DSTATCOM make the source currents sinusoidal of phase 'a'.

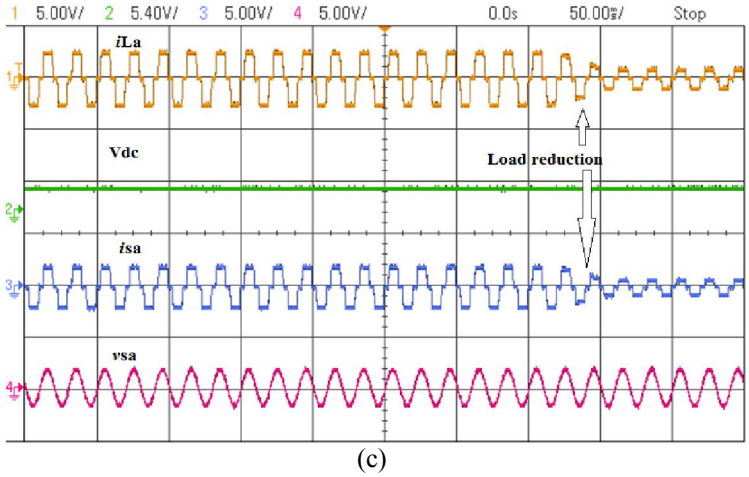
Figs. 6.14 (c)-(d) show load current i_{La}, DC- bus voltage V_{dc}, source current i_{sa}, and source voltage v_{sa} of phase 'a' before and after switching ON the DSTATCOM, respectively under dynamic load conditions.


1 500mV/ 2 50.0V/ 3 350mV/ 4 2.00V/ 0.0s 20.00ms/ Auto
iLa
Vdc
isa
vsa

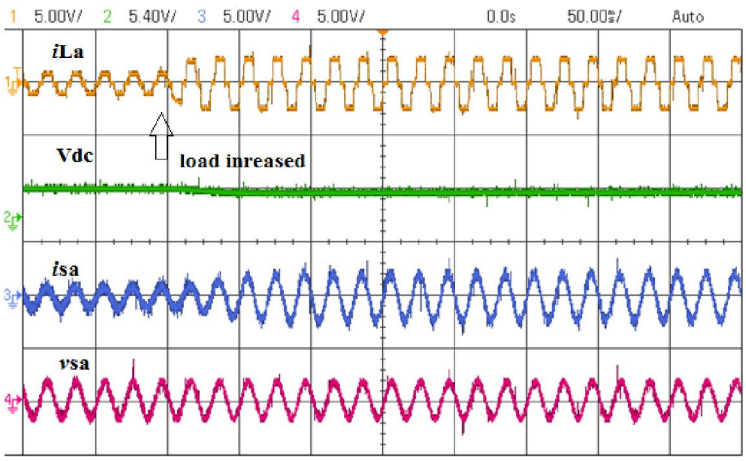
(a)


DSO-X 2024A, MY54490497: Fri Jan 06 19:02:34 2017
1 20.0A/ 2 50.0A/ 3 50.0A/ 4 20.0V/ 0.0s 29.00ms/ Auto?
vsa
isa
iLa
ica

(b)


1 5.00V/ 2 5.40V/ 3 5.00V/ 4 5.00V/ 0.0s 50.00ms/ Stop
iLa
Vdc
Load reduction
isa
vsa

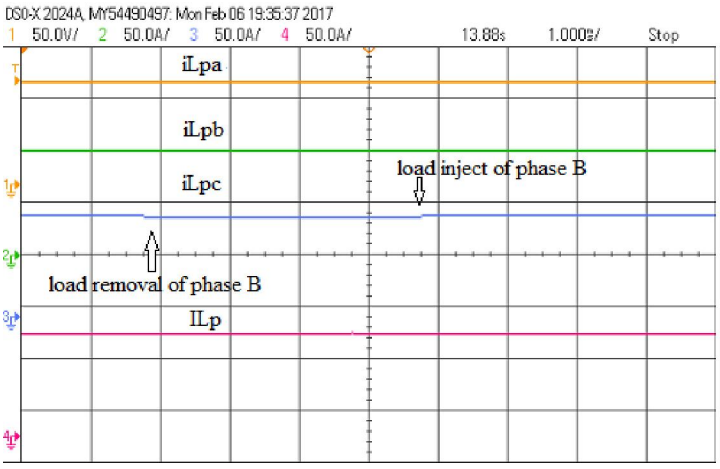
(c)



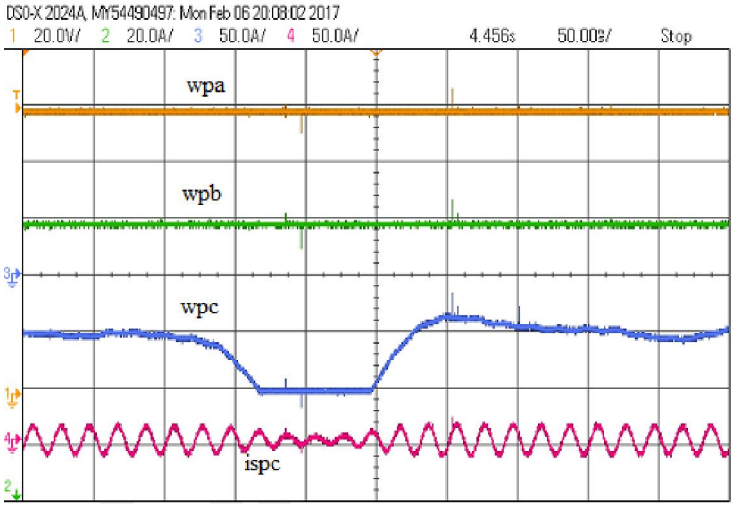
(d)

Fig. 6.14 Performance parameters (a) i_{La}, V_{dc}, i_{sa} and v_{sa} (b) v_{sa}, i_{sa} , i_{La} and i_{Ca} , before and after switching DSTATCOM (c) i_{La} , V_{dc}, i_{sa} and v_{sa} (d) i_{La}, V_{dc}, i_{sa} and v_{sa} before and after switching DSTATCOM under dynamic load conditions, of phase 'a'

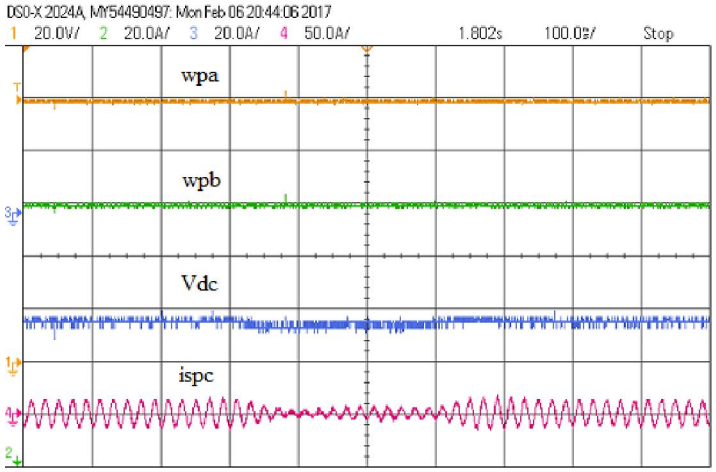
Fig. 6.15 shows the experimentally obtained intermediate control signals of AVSF algorithm. Figs. 6.15(a)-(c) show the intermediate control signals of the proposed AVSF based control algorithm under static and dynamic conditions of nonlinear load.



(a)



(b)



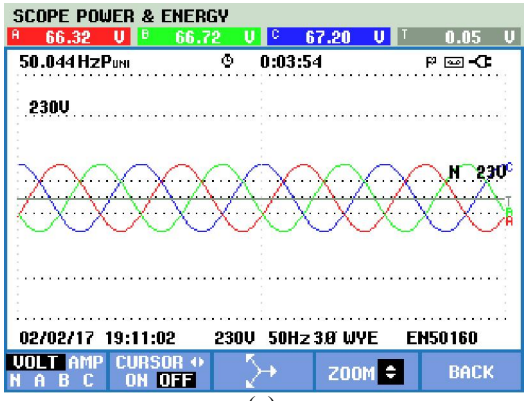
(c)

Fig. 6.15 (a) Intermediate control signals i_{Lpa}, i_{Lpb}, i_{Lpc} and I_{Lp} (b) Weights of each phase w_{pa}, w_{pb}, w_{pc} and extracted fundamental active reference source current i_{spc} (c) w_{pa}, w_{pb}, V_{dc} and i_{spc}

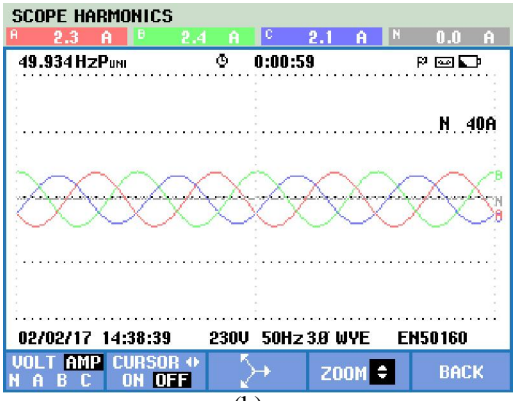
Fig. 6.15(a) shows the extracted active current component of each phase (i_{Lpa}, i_{Lpb} and i_{Lpc}) and its mean value (I_{Lp}). Fig. 6.15 (b) shows weight coefficients of each phase corresponding to input vector (w_{pa}, w_{pb} and w_{pc}) and active reference fundamental current component (i_{spc}) of phase 'c'. Fig. 6.15 (c) shows weight coefficients of phase 'a' and 'b' (w_{pa}, w_{pb}), along with DC link voltage (V_{dc}) and active reference fundamental current component (i_{spc}) of phase 'c'.

6.6.3.2 Test performance of DSTATCOM at linear load

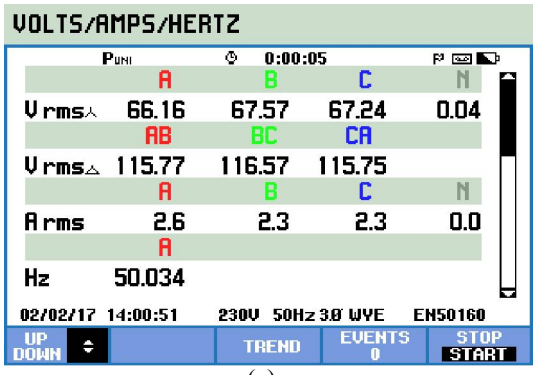
Fig. 6.16 shows the captured experimental parameters of the AVSF based control of DSTATCOM on power analyzer (Fluke make 534 series) in a balanced three phase distribution system delivering power to a linear load. The control of DSTATCOM takes place by switching ON the power devices (IGBTs) of the VSC using the AVSF algorithm. A three phase RL series circuit has been taken as a linear load. The captured waveforms of sensed source voltages v_s and source currents i_s are shown in Figs. 6.16(a)-(b), respectively. The RMS and peak values of the sensed voltages and currents are shown in Figs. 6.16 (c)-(d). Phase difference between voltage and current of phase 'a' as well as phasor diagram are shown in Figs. 6.16 (e)-(f). The captured power and power factors are shown in Figs. 6.16 (g)-(h), respectively, before compensation. When AVSF based switching of DSTATCOM takes place, phase difference between voltages and currents waveforms of source side is disappeared as shown in Figs. 6.16 (i)-(j). Fig. 6.14 (k) shows the waveform of voltage and current, which are in same phase of phase 'a', and power factor is improved to unity as shown in Fig. 6.16 (l), which proves the quite satisfactory performance of the proposed algorithm.



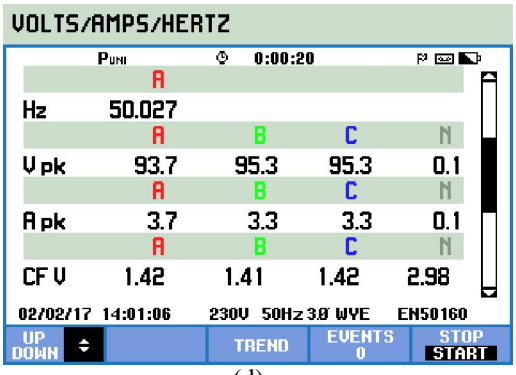
(a)



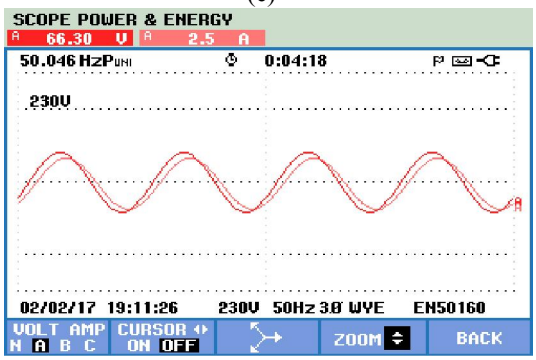
(b)


VOLTS/AMPS/HERTZ
0:00:05
A B C N
V rms⏅ 66.16 67.57 67.24 0.04
AB BC CA
V rms△ 115.77 116.57 115.75
A B C N
A rms 2.6 2.3 2.3 0.0
A
Hz 50.034
02/02/17 14:00:51 230V 50Hz 3Ø WYE EN50160
UP DOWN
TREND
EVENTS 0
STOP START

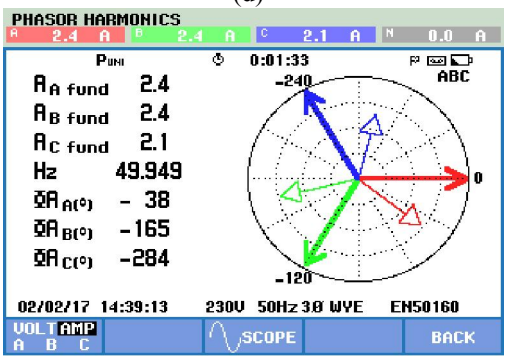
(c)


VOLTS/AMPS/HERTZ
0:00:20
A
Hz 50.027
A B C N
V pk 93.7 95.3 95.3 0.1
A B C N
A pk 3.7 3.3 3.3 0.1
A B C N
CF V 1.42 1.41 1.42 2.98
02/02/17 14:01:06 230V 50Hz 3Ø WYE EN50160
UP DOWN
TREND
EVENTS 0
STOP START

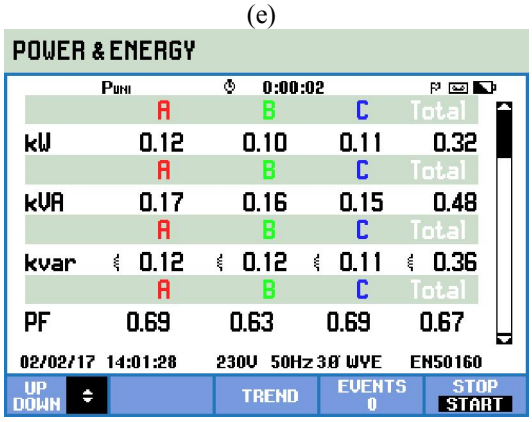
(d)


SCOPE POWER & ENERGY
A 66.30 V A 2.5 A
50.046 HzPUNI 0:04:18
230V
02/02/17 19:11:26 230V 50Hz 3Ø WYE EN50160
VOLT AMP N A B C
CURSOR ON OFF
ZOOM
BACK

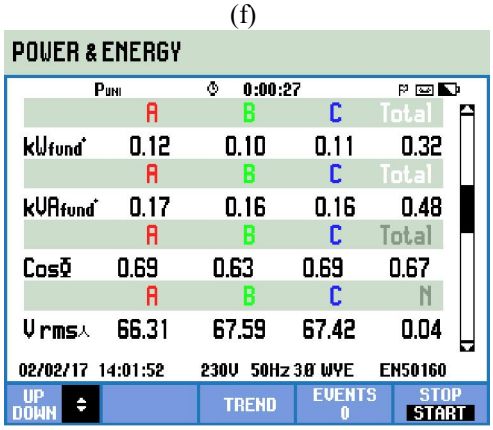
(e)


PHASOR HARMONICS
A 2.4 A B 2.4 A C 2.1 A N 0.0 A
0:01:33
ABC
-240
0
-120
IA A fund 2.4
IA B fund 2.4
IA C fund 2.1
Hz 49.949
ØIA A(°) - 38
ØIA B(°) -165
ØIA C(°) -284
02/02/17 14:39:13 230V 50Hz 3Ø WYE EN50160
VOLT AMP A B C
SCOPE
BACK

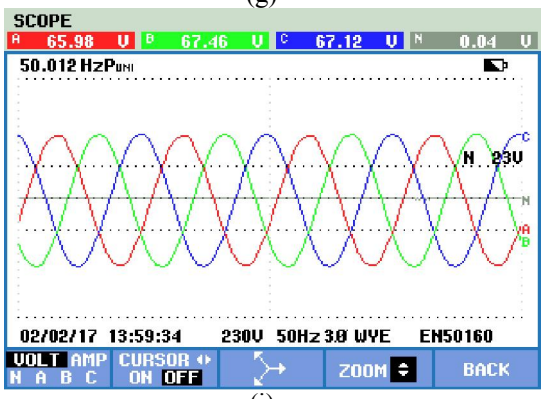
(f)


POWER & ENERGY
0:00:02
A B C Total
kW 0.12 0.10 0.11 0.32
A B C Total
kVA 0.17 0.16 0.15 0.48
A B C Total
kvar 0.12 0.12 0.11 0.36
A B C Total
PF 0.69 0.63 0.69 0.67
02/02/17 14:01:28 230V 50Hz 3Ø WYE EN50160
UP DOWN
TREND
EVENTS 0
STOP START

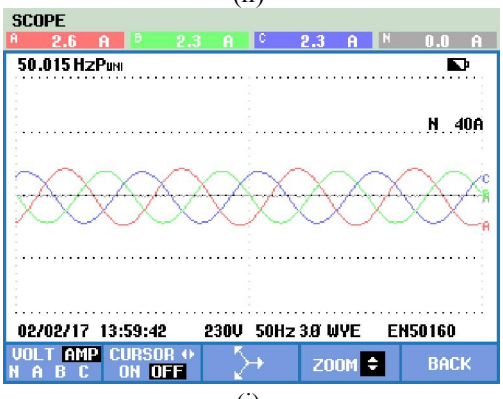
(g)


POWER & ENERGY
0:00:27
A B C Total
kWfund 0.12 0.10 0.11 0.32
A B C Total
kVAfund 0.17 0.16 0.16 0.48
A B C Total
CosØ 0.69 0.63 0.69 0.67
A B C N
V rms⏅ 66.31 67.59 67.42 0.04
02/02/17 14:01:52 230V 50Hz 3Ø WYE EN50160
UP DOWN
TREND
EVENTS 0
STOP START

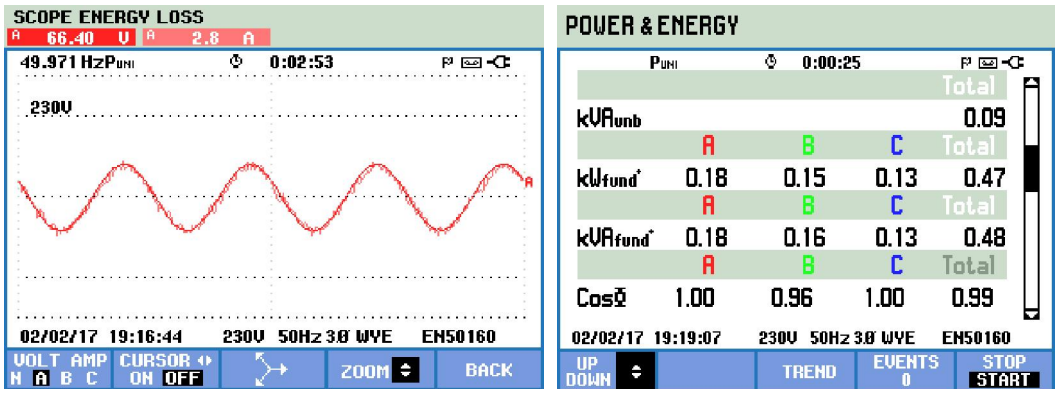
(h)


SCOPE
A 65.98 V B 67.46 V C 67.12 V N 0.04 V
50.012 HzPUNI
N 23V
02/02/17 13:59:34 230V 50Hz 3Ø WYE EN50160
VOLT AMP N A B C
CURSOR ON OFF
ZOOM
BACK

(i)


SCOPE
A 2.6 A B 2.3 A C 2.3 A N 0.0 A
50.015 HzPUNI
N 40A
02/02/17 13:59:42 230V 50Hz 3Ø WYE EN50160
VOLT AMP N A B C
CURSOR ON OFF
ZOOM
BACK

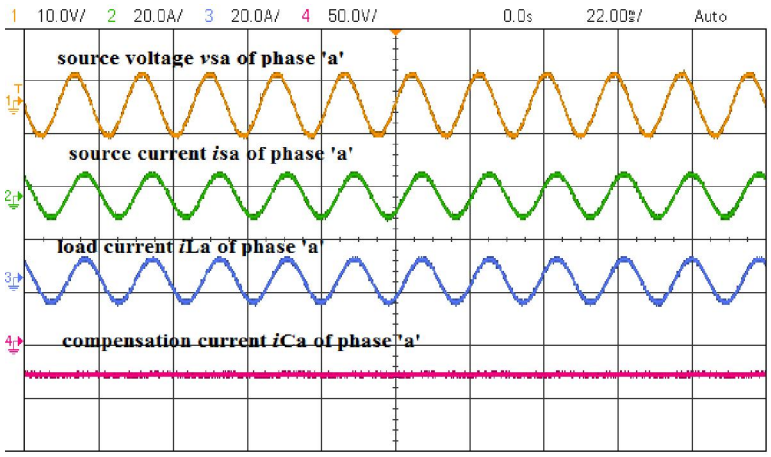
(j)



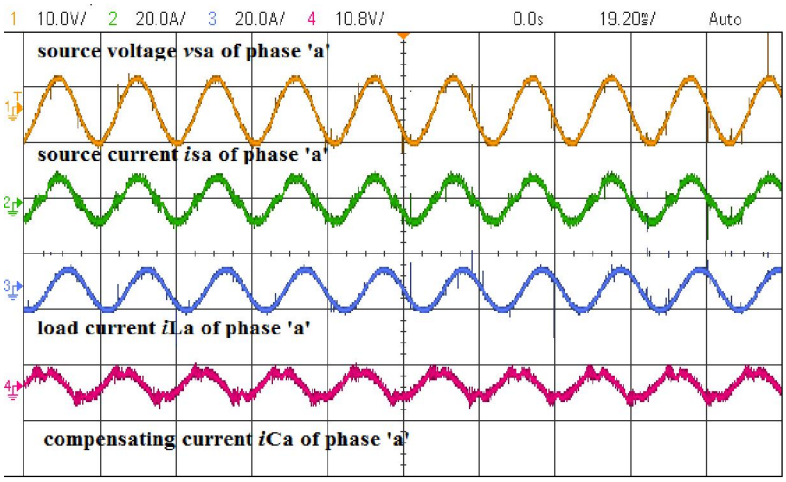
(k) (l)

Fig. 6.16 Performance parameters of test system (a) Source voltages v_s (b) Source currents i_s (c)-(d) Power and power factor (e) Waveforms of voltage v_{sa} and current i_{sa} of phase 'a' (f) Phasor diagram, when DSTATCOM is in OFF state, (g) Source voltages v_s (h) Source currents i_s, RMS values, (i) Source voltages v_s (j) Source currents i_s (k) voltage v_{sa} and current i_{sa}, of phase 'a' (l) Power and power factor, when DSTATCOM is switched ON

Fig. 6.17 shows the captured waveforms of voltage and currents of phase 'a' before and after switching ON DSTATCOM DSO (Keysight make 2024A). In Fig 6.17 (a), the sensed source voltage v_{sa}, source current i_{sa}, load current i_{La}, and compensating current i_{Ca} of phase 'a' before switching the DSTATCOM are shown. It is observed that the source voltage v_{sa}, and source current i_{sa}, are not in same phase. Whereas the source current i_{sa} and load current i_{La} are in same phase, also as the DSTATCOM is switched OFF the compensating current i_{Ca} is at zero level. After switching ON the DSTATCOM, the source voltage v_{sa}, and source current i_{sa}, become in same phase. Whereas the source current i_{sa} and load current i_{La} are not in same phase, also the injected compensating current i_{Ca} of phase 'a' from DSTATCOM is not at zero level as shown in Fig. 6.17 (b). It reveals that the injected reactive power from DSTATCOM meets the demand of the load at PCC to make the power factor unity at PCC.



(a)



(b)

Fig. 6.17 Voltage and currents waveforms of phase 'a' (a) Before switching ON DSTATCOM (b) After switching ON DSTATCOM

6.7 CONCLUSIONS

The control of DSTATCOM for harmonics elimination, power factor improvement, reactive power compensation, load balancing and zero voltage regulation using the proposed AVSF algorithm has been implemented successfully. The nonlinearity of the Volterra filter is quite suitable to deal with the nonlinear load as well as the dynamics of load to control the DSTATCOM. The proposed algorithm has an advantage of detecting the changes in waveforms of the source current and voltage with its past history in

memory. This algorithm has also been validated by test results in real time application using DSP processor controller. The THDs of source currents and voltages are found under IEEE standard limit. This algorithm adjusts with the change in system dynamics, which results into fast convergence and low complexity. The efficiency of the polynomial series adaptive Volterra filter is found quite suitable at nonlinear loads for extraction of the active and reactive current components instead of simple linear adaptive filter. The linear and quadratic parts of the AVSF based algorithm play a vital role in updating weights; as the sigmoidal function results into between 0 and 1, the error is minimized, which results into very fast error convergence.

CHAPTER 7

MAIN CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

7.1 GENERAL

Modern operation of distribution systems with custom power devices (CPD) are characterized by an increased demand of good quality power supply, an integrated renewable energy sources (RES), and a strong demand to feed nonlinear loads at the utility end. This requires the ability to handle qualitative and quantitative information in the distribution system with different levels of precision and complexity. These tasks are mainly fulfilled by different aspects of researchers for the control of CPDs such as DSTATCOM, DVR and UPQC, which are incorporated in distribution systems. The demands for flexibility and fast reactions in distribution systems require a dynamic and reactive power response at all levels of controlling of CPDs. Intelligent control algorithms that cope naturally with dynamic systems, are well equipped to address these problems and can play an important role to improve the interferences in distribution systems.

The main objectives of this research work have been to design and develop a DSTATCOM and its control techniques using proposed advanced computational intelligent control algorithms in three phase distribution system to improve the power quality. Followings are main findings of this research work:

7.2 MAIN CONCLUSIONS

The dynamic properties of the distribution system significantly influence the power quality, voltage regulation, unbalancing etc., which can be mitigated by controlling the DSTATCOM. With the help of control algorithm of DSTATCOM incorporated in three phase distribution system, power quality issues have been maintained within the prescribed standard limits. This seems to be an easy question, because many algorithms have been developed by the researches since last two decades as most of these algorithms such as conventional, transformation, adaptive theory and artificial intelligence etc are simple. However, behind the developed algorithms, none of the algorithms have taken nonlinear characteristics in their mathematical model to deal with the dynamics of utility end. The chosen quantity is perhaps a substitute for the non real quantity, one wants to control: the quality of supply power, demand of reactive power from loads, AC bus voltage regulation, load unbalancing, harmonics elimination, power factor correction, and the integration of renewable energy sources. One may think the basic questions, which should be posed when solving the power quality issues with DSTATCOM integrated distribution system:

- What should be controlled, what are the requirements and what type of control algorithm should be used?
- What is the dynamic behavior of the power quality in the distribution system to be controlled? Is the load of the distribution system linear or nonlinear, time-varying or the load exhibit delay time?
- What are the disturbances acting at PCC on the distribution system? Can they be measured and compensated for?

- Which quantities are measurable and which quantities can be reconstructed from measurements?
- Which quantities describe to a reasonable extent the unknown or non-measurable quantities we actually want to compensate?
- Which quantity should be controlled by which manipulated quantity?

In view of these standard questions and issues, advanced intelligent control algorithms have been developed for DSTATCOM in three phase distribution system.

The intelligent control algorithms have been developed using neural network with advanced computational techniques and nonlinear adaptive Volterra filter. Various functions of DSTATCOM are presented in the proposed work, which include harmonics current elimination, reactive power compensation and load balancing in PFC and voltage regulation modes under linear and nonlinear loads. The design and simulation of performance of DSTATCOM are performed in MATLAB environment using SIMULINK and SimPowerSystem tool boxes. An experimental prototype of DSTATCOM is developed in the laboratory using a VSC, DSP (dSPACE 1104 R&D controller), signal conditioning circuits and Hall Effect based voltage and current sensors.

The use of the *intelligent control algorithms approach* to study the dynamics of distribution systems, introduces a strong theoretical framework to analyze and design more complex controller. The main advantage of these intelligent control algorithms, is their universality in describing linear, nonlinear, multi-input multi-output, dynamics of load etc. within the same mathematical framework. Not only, it is the source-load behavior of the distribution system described but its performance parameters in these algorithms also. Based on this system description, one gets a complete framework for

DSTATCOM in three phase distribution system, which provides analysis and design for closed loop control of DSTATCOM. The combination with fast learning performance criteria has become quite effective, which led to optimize power quality issues using DSTATCOM. What is needed, is an adequate description of the distribution system, is a translation of the requirements into the parameters of the performance criterion, and the availability of the state of the system. The main problems encountered are the availability of a good convergence that can be updated around an operating point, the availability of all state variables, and the choice of the right parameters in the performance criterion.

The intelligent control algorithms have been designed and developed for the control of three-phase, three-leg DSTATCOM. These algorithms have been developed using neural network and nonlinear adaptive filter. The performance of these algorithms based on their design, tuning of parameters, computational complexity and implementation is discussed as follows.

- The mathematical modeling, design and development of advanced intelligent control algorithms for DSTATCOM have been carried out for mitigating current related power quality problems at the three phase distribution system. These control algorithms control the DSTATCOM for reactive power compensation resulting into AC bus voltage magnitude regulation at PCC. The voltage regulation is required in various isolated power generation systems and distributed generation system in islanded condition and it is an important power quality issue to be studied and investigated.
- The intelligent control algorithms based on neural network have been developed for control of DSTATCOM. The performance of the control algorithms have been presented for several power quality problems such as current harmonics elimination,

reactive power compensation and load balancing in PFC and voltage regulation modes. The algorithms based on fast multilayer perception (MLPNN), generalized neural network (GNN) and nonlinear adaptive Volterra second order filter theory, have been developed for DSTATCOM. The MLPNN based control algorithm has been found to be simple in implementation with improved convergence speed. The fast learning of BP based MLPNN control technique has been found suitable in terms of fast weight convergence and a low steady state error. The MLPNN based approach resolves the problem of convergence rate and steady state error and it has positive aspects such as faster convergence rate, lower steady state error and higher stability.

- The proposed GNN single layer concept of neural network based control algorithm for DSTATCOM has been implemented for current related power quality problems at the distribution system. The control of three phase VSC used as a DSTATCOM, has been performed satisfactorily with this control algorithm. This control technique has been utilized to estimate the weighted values corresponding to the fundamental active and reactive power components of the distorted load currents. The GNN based control has offered fast convergence rate and robustness with system parameters than the MLPNN. The GNN based control algorithm is found useful in terms of reduced computational complexity. This has been achieved because the computation of multilayer is not required. GNN based algorithm has been tested under steady state and unbalanced load conditions. Positive features of this control algorithm are that they are fast, single layer, require few mathematical operations and easy to implement using DSP.

- The developed intelligent control algorithms for DSTATCOM and their applications have been found superior than the existing control algorithms, which are evident from the comparison tables given in this work.

7.3 SUGGESTIONS FOR FURTHER WORK

The research areas for further work are suggested as follows:

- These algorithms can be extended for custom power devices incorporated in three phase four wire distribution system to mitigate power quality problems.
- Various other time domain and frequency domain, approach based control algorithms can be developed to achieve desired response of DSTATCOM.
- The developed control algorithms can be applied in isolated power generating systems such as wind, solar and micro-hydro based generation for power transfer to the loads, voltage regulation and compensation of power quality problems.
- Experimental verification of grid connected solar photovoltaic system with the proposed control algorithms can also be extended for power transfer to the grid along with compensation of power quality problems.

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APPENDIX-A

Design parameters of DSTATCOM for load power rating of 25kVA in a three phase distribution system.

AC mains: three phase 415V, 50Hz with source impedance ($R_s = 0.04$ and $L_s = 1mH$).

Design parameters of DSTATCOM:

DC bus voltage $V_{dc} = 700V$,

DC bus Capacitance $C_{dc} = 3500\mu F$

Interfacing inductors $L_f = 3mH$

Ripple series R-C filters: $R_r = 5\Omega$ and $C_r = 10\mu F$

Current rating of IGBT module SKM150GB12V= 30A

Switching frequency $f_{sw} = 10kHz$

Loads: Linear load of 20 kVA, 0.8 pf lagging

Nonlinear load, three phase diode rectifier module SKD 35 of SEMIKRON with R=12Ω and L= 150mH

LIST OF PUBLICATIONS

Following are the publications in SCI International journals and conferences out of this research work.

- **List of papers (s) published in Peer Reviewed Referred International Journals:**

1. Md. Tausif Ahmad, Narendra Kumar and Bhim Singh, "Fast multilayer perceptron neural network based control algorithm for shunt compensator in distribution systems", *IET Gener. Transm. Distrib.*, vol. 10, Iss. 15, pp. 3824–3833, 2016.
2. Md. Tausif Ahmad, Narendra Kumar and Bhim Singh, "AVSF Based Control Algorithm of DSTATCOM for distribution system", *IET Gener. Transm. Distrib.*, vol. 11, Iss. 13, pp. 3389-3396, 2017.
3. Md. Tausif Ahmad, Narendra Kumar and Bhim Singh, "Generalized Neural Network based Control Algorithm for DSTATCOM in Distribution Systems", IET Power Electron., vol. 10, Iss. 12, pp. 1529-1538, 2017.

- **List of Paper(s) Published in Peer Reviewed International/National Conference Proceedings/Presented in the Conference:**

1. Md. Tausif Ahmad, Narendra Kumar and Bhim Singh, "Implementation of Least Mean Square Algorithm for Second-Order Volterra Filter in a Distribution System", ***Proceedings of 16th IASTED (International Association of Science and Technology for Development)*** on Intelligent Systems and Control (ISC), Calgary, Canada, July 19-20, 2017. DOI: 10.2316/P.2017.854-014, Proceeding (853) Modelling, Simulation and Identification / 854: Intelligent Systems and Control – 2017. http://www.actapress.com/Abstract.aspx?paperId=456477.
2. Md. Tausif Ahmad, Narendra Kumar and Bhim Singh, "A Discrete Derivative Control Technique for DC-Link Voltage in Shunt Compensator", ***Proceedings of 12th IEEE India International Conference (INDICON 2015)*** entitled Electronics, Energy, Environment, Communication, Computer, Control (E^3-C^3), organized by Jamia Millia Islamia, New Delhi, India during December 17-20, 2015. http://ieeexplore.ieee.org/document/7443429/.
3. Md. Tausif Ahmad, Narendra Kumar and Bhim Singh, "Fast Learning Algorithm for Extraction of Harmonics and Reactive Current in Distribution Systems",

Proceedings of National Conference on Emerging Trends in Electrical and Electronics Engineering, vol. 2, pp. 44-52, organized by Jamia Millia Islamia, New Delhi, India during February 02-03, 2015.

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