A DISSERTATION ON

VLSI IMPLEMENTATION OF NON-LINEAR CIRCUITS

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MASTER OF TECHNOLOGY
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CERTIFICATE

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This is certified that the dissertation entitled "**VLSI Implementation of Non-Linear Circuits"** is a work of **Gavendra Singh** (University Roll No. – 2K11/VLS/19) is a student of Delhi Technological University. This work is completed under my direct supervision and guidance and forms a part of master of technology (Electronics & Communication Engineering) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other Institute / University for the award of any other degree to the best of my knowledge.

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ABSTRACT

The design of analog circuits with reduced power consumption, components count, low power supply, better accuracy and less propagation delay is a challenging task. A lot of work has been done on non linear circuits using CMOS technology. The least power consumption and highest fidelity is possible by using CMOS- Operational Transresistance Amplifier (OTRA) instead of Op-amp. As a consequence, the CMOS based circuits approach has been area of interest and challenge to provide advantages of higher bandwidth, lower power consumption, higher slew rates, improved linearity, and better accuracy. This report describes the implementation of some non linear circuits and their applications based on Operational Transresistance Amplifier (OTRA) using CMOS technology.

The operational transresistance amplifier (OTRA) is an amplifier which provides an output voltage with inputs as two differential currents. Thus, it is a current controlled voltage source. The transresistance required is very high so as to realize open loop circuits such as comparator and closed loop circuits such as filters.

In this work, non linear circuits such as multiplier, squarer, dsb-sc modulator, frequency multiplier has been implemented. A frequency mixer circuit and relaxation oscillator using OTRA has been implemented.

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1.1 INTRODUCTION

Electrical devices are built from nonlinear components. In order to understand the design of these devices, a fundamental understanding of nonlinear circuits is necessary. Moreover, non-linear circuit is where the real engineering comes in. That is, there are no hard and fast rules to analyze most non-linear circuits. To analyze non-linear circuits, the approach used depends on the type of circuit, generally the simplest approach is utilized.

It is easy to understand the difference between a linear and a nonlinear circuit by looking at the difference between a linear and a nonlinear equation:

$$y = x \tag{1.1}$$

$$y = x + 3 \tag{1.2}$$

$$y = x^2 \tag{1.3}$$

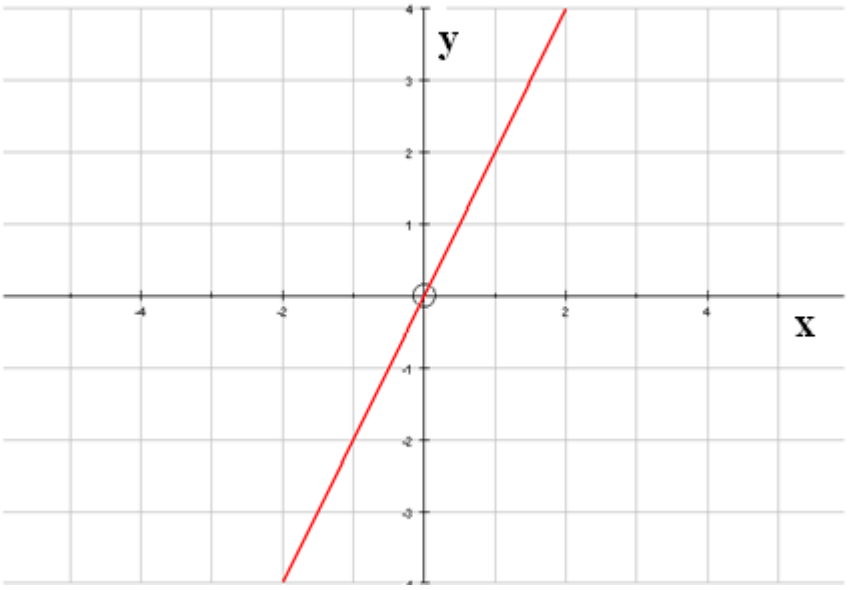

Figure 1.1 graph for equation 1.1 showing linear characteristic

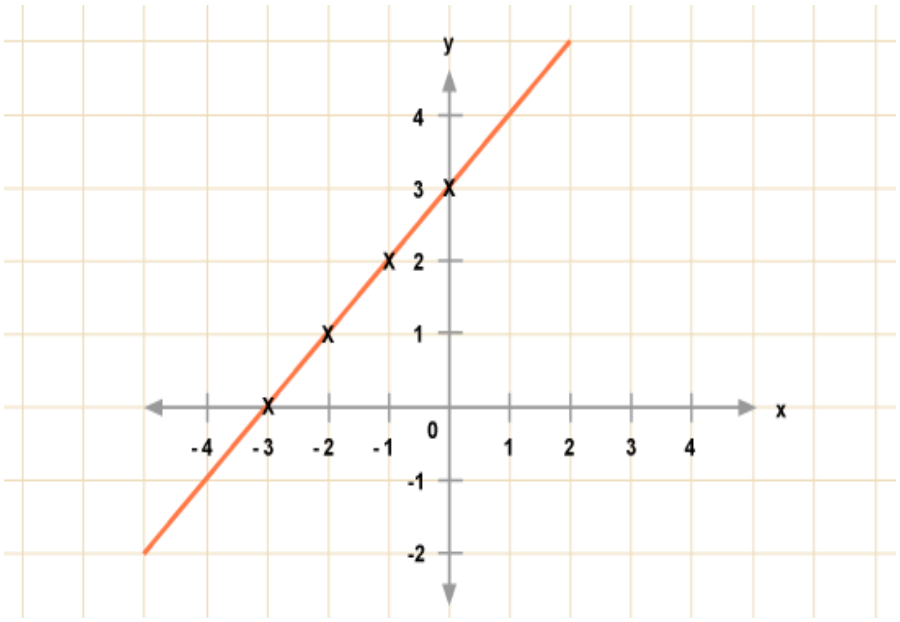

Figure 1.2 graph for equation 1.2 showing non linear characteristic

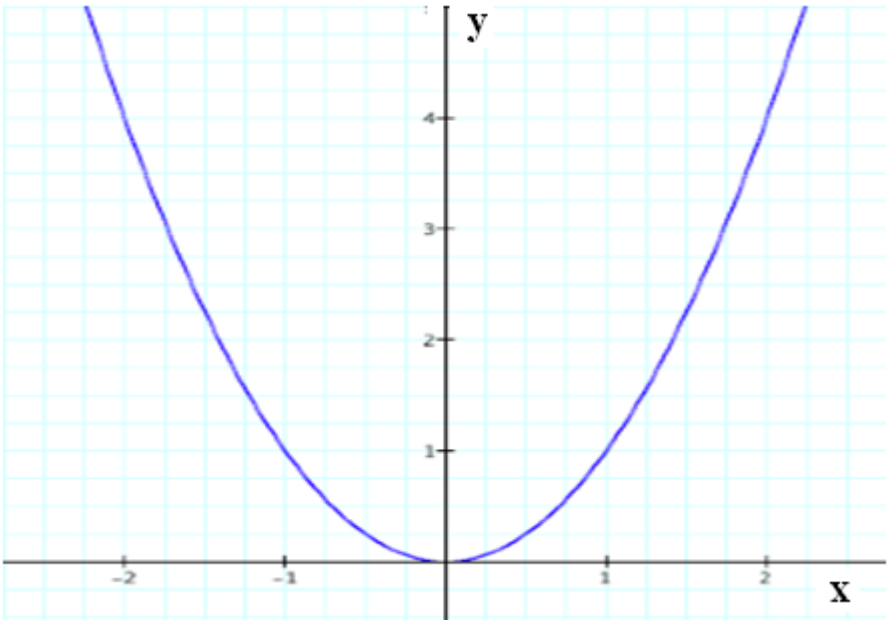

Figure 1.3 Graph for equation 1.3 showing non linear characteristic

1.2 MATHEMATICAL ILLUSTRATION OF LINEARITY

A system is said to be linear [1] if it follows the principle of superposition as well as homogeneity. If a system failed to follow any of these two principle is said to be non linear system[1].

1.2.1 SUPERPOSITION PROPERTY

Superposition property, states that, for all linear systems, the net response at a given place and time caused by two or more stimuli is the sum of the responses which would have been caused by each stimulus individually. So that if **A** produces response **X** and **B** produces response **Y** then input **A+B** produces response **X+Y**.

$$\boldsymbol{F(x1 + x2 + \ldots\ldots) = F(x1) + F(x2) + \ldots..} \quad (1.4)$$

1.2.2 HOMOGENEITY PROPERTY

Homogeneity property, states that, if **A** produces response **X** and **B** produces response **Y** then input p**A** produces response p**X** and q**B** produces response q**Y**.

$$\boldsymbol{A \rightarrow X \text{ , } then\ pA \rightarrow pX} \quad (1.5a)$$

$$\boldsymbol{B \rightarrow Y, then\ qB \rightarrow qY} \quad (1.5b)$$

On combining eq. (1.4) and (1.5), the condition for linearity is given as follows:

$$\boldsymbol{pA + qB \rightarrow pX + qY} \quad (1.6)$$

It is shown by the block diagram drawn below.

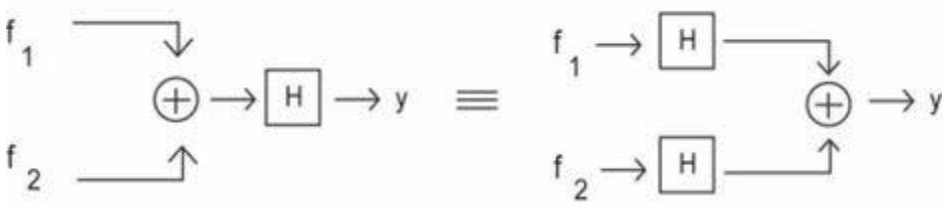

Figure 1.4 Block diagram for linearity

Analog Integrated Circuit Design using CMOS non linear circuit become increasingly important with growing opportunities. Coupled with the various technological

improvements such as the continuously shrinking feature size of the devices on IC's and the most attractive reduction of power supply voltages and power dissipation. This has led to creation of alternate analog design techniques.

The information processed by lumped electric networks can be represented by either the nodal voltages or branch currents of the networks. The former are referred to as voltage-mode circuits whereas the latter are known as current-mode circuits. Together, they provide a complete characterization of the behavior of the networks [2].

Historically analog design was viewed as a voltage dominated form of signal processing. This is apparent from the fact that current signals were transferred into voltage domain before any analogue signal processing could be done. But due to the advances in the process technology a shift is made to current mode of signal processing. Analog IC design is receiving a tremendous boost from the development and application of current mode processing which has an inherent performance feature of wider bandwidth [2].

1.3 CURRENT MODE SIGNAL PROCESSING

Analog signal processing will remain irreplaceable for the implementation of interface circuitry between digital processing and the external world. It also competes with digital signal processing with respect to speed and silicon area, which makes it more economic in many cases. Current-mode analog signal processing [3][4] has recently gained prominence because of its capability to minimize voltage swings, resulting in increased signal handling capability even at reduced supply voltages. This makes it suitable to be employed in mixed analog-digital IC's operating at supply voltages of 3.3v, which is likely to become the future CMOS industrial standard.

With the evolution of submicron technologies such as 0.18 micron and 0.13 micron, the supply voltages have been reduced to 3.3 Volts and lower. This makes it difficult to design a voltage mode CMOS circuits with high linearity and wide dynamic range. Recently, current mode circuits have become a viable alternative for future applications because of their inherent advantages over voltage mode circuits [5].

The main advantage of using current mode technique is because the non-linear characteristics exhibited by most field effect transistors. A small change in the input or controlling voltage results in a much larger change in the output current. Thus for a fixed supply voltage, the dynamic range of a current mode circuit is much larger than that of a voltage mode circuit. If a supply voltage is lowered, one can still get the required signals represented by the current.

A second advantage of current mode circuits is that they are much faster as compared to voltage mode circuits. The parasitic capacitances present in the analog circuits must be charged and discharged with the changing voltage levels. In a current mode circuit, a change in current level is not necessarily accompanied by a change in the voltage level. Hence, the parasitic capacitances will not affect the operating speed of the circuit by a significant amount.

Other advantages of using current mode circuits are that they do not require specially processed capacitors or resistors; they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible. Due to all the advantages of current mode analogue signal processing there has been an emergence of new analogue building blocks ranging from the current conveyor, OTA, OTRA and current feedback op-amps through to sampled data current circuits such as dynamic current mirrors and analogue neural networks.

REFERENCES

[1] *Linear and Non-Linear Circuits*: *Solutions Manual* **- Leon O. *Chua***

[2] CMOS Current-Mode Circuits for Data Communications - Fei Yuan

[3] A.F. Arbel, "A Unified Approach to the Design of Nuclear Instrumentation used in Low and High Energy Physics", D.Sc. Thesis, Technion-Israel Institute of Technology, 1966.

[4] Analogue IC Design: The Current-Mode Approach. Edited by C. Toumazou et al., Peter Peregrinus Ltd., London, 1990

[5] Toumazou C, Lidjey FJ, Haigh D. Analog IC design: the current-mode approach. Peter Peregrinus, UK: Exeter; 1990.

CHAPTER-2

BLOCKS USED IN ANALOG DESIGN

2.1 TRANSIMPEDANCE AMPLIFIER

Transimpedance amplifier[1] consists of an inverting amplifier accepting the input signal in form of a current from a high impedance signal source, such as a photodiode or a semiconductor based detector for radiation particles, and converts it into an output voltage. The transimpedance at DC and low frequencies is $\frac{v_o}{i} = R_f$. However, the high impedance signal source inevitably has a stray capacitance C_i , which deprives the amplifier from the feedback at high frequencies. Therefore the amplifier's feedback loop must be stabilized by a suitably chosen phase margin compensation capacitance C_f . Owed to the presence of these capacitances, and because of the amplifier's own limitations, the system response at high frequencies will be reduced accordingly.

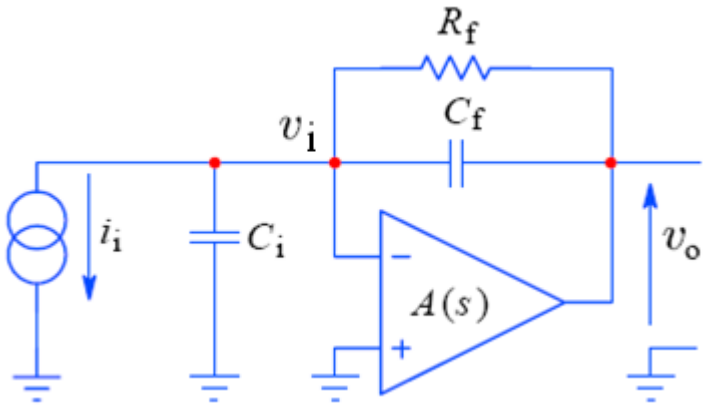

Figure 2.1 Generalized transimpedance system schematic diagram

The amplifier's inverting open loop voltage gain is modeled as:

$$\frac{v_o}{v_i} = -A(s) = -Ao\frac{-So}{S-So} = -Ao\frac{\omega o}{S+\omega o} \qquad (2.1)$$

where: S is the complex frequency variable;

A_O is the amplifier's open loop DC gain;

S_0 is the amplifier's real dominant pole, so that:

$\omega o = 2\pi f_O$, f_o is the open loop cutoff frequency

2.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current [2]. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

The OTA is not as useful by itself in the vast majority of standard op-amp functions as the ordinary op-amp because its output is a current. One of its principal uses is in implementing electronically controlled applications such as variable frequency oscillators and filters and variable gain amplifier stages which are more difficult to implement with standard op-amps. In the ideal OTA, the output current is a linear function of the differential input voltage, and is given by:

$$I_{out} = (V_{in+} - V_{in-}).g_m \tag{2.2a}$$

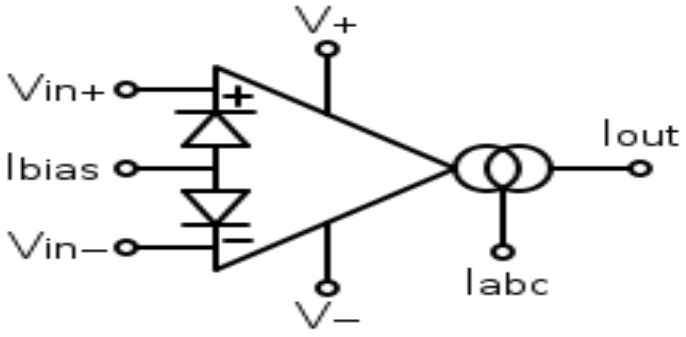

Figure 2.2 OTA Model

The amplifier's output voltage is the product of its output current and its load resistance:

$$V_{out} = I_{out} \, . R_d \tag{2.2b}$$

The voltage gain is then the output voltage divided by the differential input voltage:

$$G_{voltage} = R_d \cdot g_m \tag{2.2c}$$

The transconductance of the amplifier is usually controlled by an input current, denoted I_{abc}. The amplifier's transconductance is directly proportional to this current. This is the feature that makes it useful for electronic control of amplifier gain, etc.

As an ideal OTA is usually considered to have the following properties and they are considered to hold for all input voltages:

- Infinite input impedance
- Infinite output impedance (i.e., $R_{out} = \infty$).
- G_m is variable and $G_m = \frac{I_{abc}}{2V_T}$, we cannot make G_m infinite.

2.3 CURRENT FEEDBACK OPERATIONAL AMPLIFIER

The current feedback operational amplifier (CFOA) is a type of electronic amplifier whose inverting input is sensitive to current, rather than to voltage as in a conventional voltage-feedback operational amplifier (VFA). The CFA was invented by David Nelson at Comlinear Corporation, and first sold in 1982 as a hybrid amplifier, the CLC103. The first integrated circuits CFAs were introduced in 1987 by both Comlinear and Elantec (designer Bill Gross). They are usually produced with the same pin arrangements as VFAs, allowing the two types to be interchanged without rewiring when the circuit design allows. In simple configurations, such as linear amplifiers, a CFA can be used in place of a VFA with no circuit modifications, but in other cases, such as integrators, a different circuit design is required. The circuit symbol of CFOA is as shown in fig.2.3. Its port relations can be characterized by the following matrix form:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \\ I_o \end{bmatrix}$$

Therefore, this active element can be characterized with the following equations:

$i_y=0,\ v_x = v_y,\ i_{z=i_x},\ v_o = v_z$ (2.3)

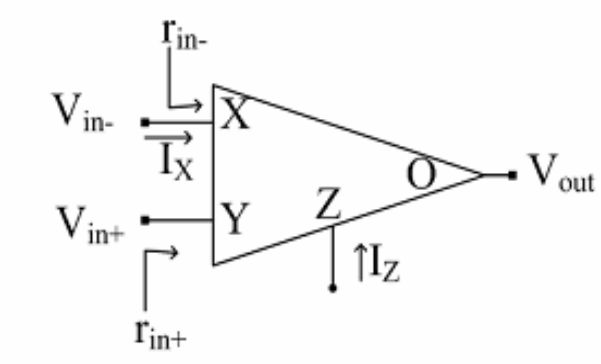

Fig.2.3 Circuit Symbol of CFOA

Current-Feedback Operational Amplifiers (CFOAs) are employed as an alternative to conventional voltage opamps because of their inherent advantages:

- The CFOA closed-loop bandwidth is independent of its close-loop gain, provided that the feedback resistance is kept constant
- The CFOA input and output stages work both in class AB and give high slew-rate values AD844A is CFOA chip which is commercially available in the market.

2.4 OPAMP

An operational amplifier, which is often called an op-amp, is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. Ideally the op-amp amplifies only the difference in voltage applied between its two inputs (V_+ andV_-), which is called the differential input voltage. The output voltage of the op-amp is given by the equation,

$$V_{out} = (V_+ - V_-).\, G_{open-loop} \tag{2.4}$$

Where V_+ is the voltage at the non-inverting terminal and V_- is the voltage at the inverting terminal and G open-loop is the open-loop gain of the amplifier.

The ideal operation is difficult to achieve and the non-ideal conditions often raise limitations like finite impedances and drift, their primary limitation being not especially fast. The typical performance degrades rapidly for frequencies greater than 1MHz, although some models are designed especially for higher frequencies. High input impedance at the input terminals (ideally infinite) and low output impedance at the output terminal(s) (ideally zero) are important typical characteristics. The other important fact about op-amps is that their open-loop gain is huge. This is the gain that would be measured from a configuration in which there is no feedback loop from output back to input. A typical open-loop voltage gain is ~ 10^4 -10^5 .

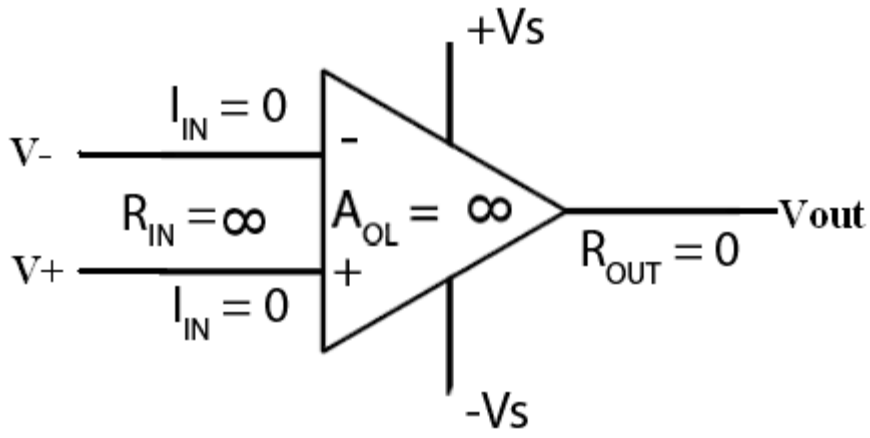

Figure 2.4 Ideal internal circuit of Op-amp

An ideal op-amp is usually considered to have the following properties, and they are considered to hold for all input voltages:

- Infinite open-loop gain.
- Infinite voltage range available at the output (V_{out}) (in practice the voltages available from the output are limited by the supply voltages Vs_+ and Vs_-)
- Infinite bandwidth

- Infinite input impedance
- Zero input current
- Zero input offset voltage
- Infinite slew rate
- Zero output impedance
- Infinite Common-mode rejection ratio (CMRR)
- Infinite Power supply rejection ratio for both power supply rails.

2.5 CURRENT CONVEYOR

The current conveyor (CC) is the basic building block of a number of applications both in the current and voltage and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [3]. Two years later, today's widely used second-generation CCII was described in [4], and in 1995 the third-generation CCIII [5]. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier were not widely appreciated. An IC Current Conveyor, namely PA630, was introduced by Wadsworth in 1989 and about the same time, the now well known CFOA AD844 was recognized to be internally a CCII+ followed by a voltage follower [6]. Today, the current conveyor is considered a universal analog building block with wide spread applications in the current mode, voltage mode, and mixed mode signal processing. Several generations of current conveyors have been defined over the years. Undoubtedly, the second generation conveyor (CCII) is the more well known of the device. The terminal relations of a CCII can be characterized by

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} \beta & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}$$

where $\alpha = 1 - \epsilon_i$ and $\beta = 1 - \epsilon_v$,$|\ \epsilon_i\ | << 1$ and $|\ \epsilon_v\ | << 1$ (2.5)

represent the current and voltage tracking errors, respectively, where the subscripts x, y, and z refer to the terminals labeled X, Y and Z in fig1 The CCII is defined in both a positive and a negative version where the +sign in the matrix is used for the CCII+ type conveyor and the –sign is used for the CCII- type conveyor. Its features find most applications in the current mode, when its voltage input y is grounded and the current, flowing into the low-impedance input x, is copied by a simple current mirror into the z output.

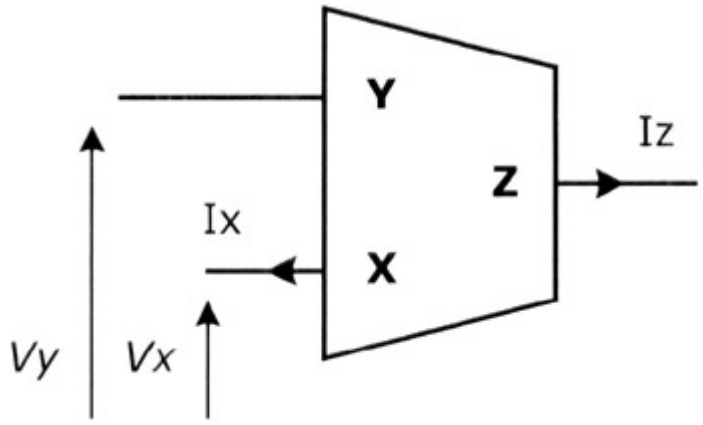

Fig 2.5 Block diagram of CCII

2.6 OPERATIONAL TRANSRESISTANCE AMPLIFIER

As signal processing extends to higher frequencies, traditional design methods based on voltage op-amps are no longer adequate. It is well known that a traditional operational amplifier has bandwidth which is dependent on the closed-loop voltage gain. The attempt to overcome this problem has led to a renewed interest in circuits which operate in current mode.

The OTRA is a current mode device that uses current mirrors and common source amplifier to give a current difference signal as input which in turn produce an appropriate voltage signal as output. The OTRA is a three terminal analog building block. Both the input and output terminals are characterized by low impedance. The circuit symbol of the OTRA is illustrated in Fig.2.6. The port relations of an OTRA can be characterized by the following matrix form [7].

$$\begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ i_z \end{bmatrix}$$

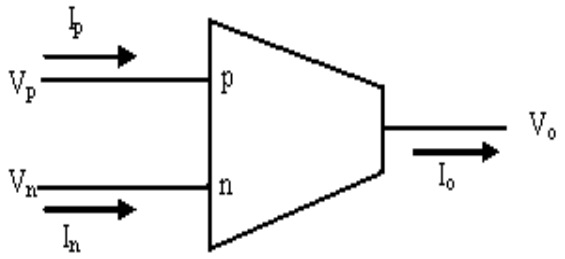

Fig 2.6 Circuit symbol of OTRA

It eliminates response limitations incurred by capacitive time constants leading to circuits that are insensitive to the stray capacitances at the input terminals. For ideal OTRA, the Transresistance gain, R_m, approaches infinity and external negative feedback must be used which forces the input currents to be equal [8]. Thus the OTRA must be used in a negative feedback configuration. Practically the Transresistance gain is finite and its effect should be considered.

The important advantages offered by OTRA are:

- Since the OTRA has one output terminal with low impedance and two input terminals that are virtually grounded, most effects of parasitic capacitances disappear and the remainder can be compensated without adding any extra components.
- Using current feedback techniques, OTRAs have a bandwidth almost independent of the closed loop-voltage gain.

- Due to the input terminals being virtually grounded, they are cascadable.

2.7 CURRENT DIFFERENCING TRANS-CONDUCTANCE AMPLIFIER

Current differencing transconductance amplifier (CDTA) is a new active circuit element. The CDTA is free from parasitic input capacitances and it can operate in a wide frequency range due to current mode operation. Some voltage and current mode applications using this element have already been reported in literature, particularly from the area of frequency filtering: general higher-order filters, biquad circuits, all-pass sections, gyrators, simulation of grounded and floating inductances and LCR ladder structures. Other studies propose CDTA-based high-frequency oscillators. Nonlinear CDTA applications are also expected, particularly precise rectifiers, current-mode Schmitt triggers for measuring purposes and signal generation, current-mode multipliers, etc.

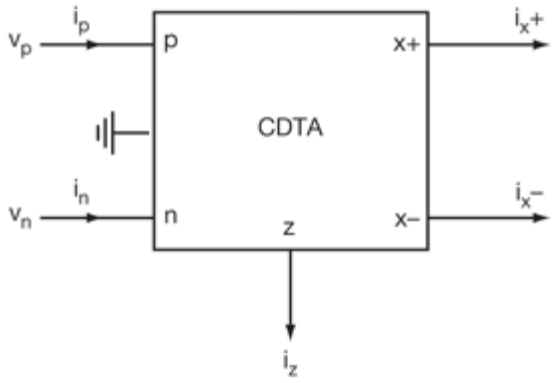

Figure 2.7 Block diagram of CDTA

The CDTA element with its schematic symbol in Fig 2.7 has a pair of low-impedance current inputs p, n and an auxiliary terminal z, whose outgoing current is the difference of input currents. Here, output terminal currents are equal in magnitude, but flow in opposite directions, and the product of transconductance (g_m) and the voltage at the z terminal gives their magnitudes. Therefore, this active element can be characterized with the following equations:

1. $V_P = V_N = 0$, (2.6a)

2. $I_Z = I_P - I_N$ (2.6b)

3. $I_{X+} = g_m V_Z$ (2.6c)

4. $I_{X-} = -g_m V_Z$. (2.6d)

Where $V_{Z-} = I_Z Z_Z$ and Z_Z is the external impedance connected to z terminal of the CDTA. CDTA can be thought as a combination of a current differencing unit followed by a dual-output operational transconductance amplifier, DO-OTA. Ideally, the OTA is assumed as an ideal voltage-controlled current source and can be described by $I_X = g_m(V_+ - V_-)$, where I_X is output current, V_+ and V_- denote non-inverting and inverting input voltage of the OTA, respectively. Note that g_m is a function of the bias current. When this element is used in CDTA, one of its input terminals is grounded (e.g., V_- = 0V). With dual output availability, $I_{X+} = -I_{X-}$ condition is assumed.

2.8 CURRENT DIFERENCING BUFFERED AMPLIFIER

CDBA, current differencing buffered amplifier, is a multi-terminal active component with two inputs and two outputs [9]. Its block diagram can be seen from figure 2.8. It is derived from current feedback amplifier (CFA).

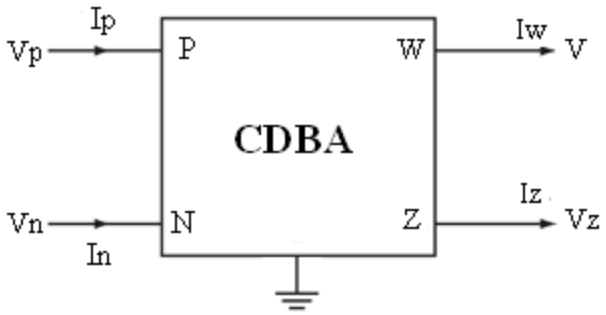

Figure 2.8 Block Diagram for CDBA

The characteristic equation of this element can be given as:

1. $V_P = V_N = 0$ (2.7a)

2. $I_Z = I_P - I_N$ (2.7b)

3. $V_W = V_Z$ (2.7c)

Here, current through z-terminal follows the difference of the currents through p-terminal and n-terminal. Input terminals p and n are internally grounded. The difference of the input currents are converted into the output voltage V_W, therefore CDBA element can be considered as a special type of current feedback amplifier with differential current input and grounded y input.

The CDBA is simplifying the implementation, free from parasitic capacitances, able to operate in the frequency range of more than hundreds of MHz (even GHz), and suitable for current mode operation while, it also provides a voltage output. Several voltage and current mode continuous-time filters, oscillators, analog multipliers, inductance simulators and a PID controller have been developed using this active element.

The CDBA offers several advantageous features viz., high slew rate, improved bandwidth, and accurate port tracking characteristics when configured with a pair of matched current feedback amplifier (AD-844-CFA) devices which leads to extremely low active circuit sensitivity.

REFERENCES

[6] B.Razavi, Design of Analog CMOS Integrated circuits: McGraw-Hill, 2001.

[7] A 0.8-V 0.25-mW Current-Mirror OTA With 160-MHz GBW in 0.18μm CMOS – Tsung Hsien Lin, IEEE feb 2007.

[8] SMITH, K.C., SEDRA, A. The current conveyor: a new circuit building block. *IEEE Proc.* CAS, 1968, vol. 56, no. 3, p. 1368-1369.

[9] SEDRA, A.S., SMITH, K.C. A second generation current conveyor and its application. *IEEE Trans*., 1970, CT-17, p. 132-134.

[10] FABRE, A. Third generation current conveyor: A new helpful active element. *Electron. Lett.*, 1995, vol. 31, no. 5, p. 338–339.

[11] WADSWORTH, D.C. Accurate current conveyor topology and monolithic implementation. *Proc. IEE G*, 1990, vol. 137, no. 2, p. 88-94.

[12] J.J. Chen, H.W. Tsao, and C. Chen, "Operational transresistance amplifier using CMOS technology." *Electronics Letters*, vol. 28, no. 22, pp. 2087–2088, 1992.

[13] K.N. Salama and A.M. Soliman, "CMOS operational transresitance amplifier for analog signal processing applications." *Microelectronics Journal*, vol. 30, pp. 235–245, 1999.

[14] Microelectronics Journal 30 (1999) 157–160 'A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters'

[15] Hassan Mostafa, Ahmed M. Soliman, A modified CMOS realization of the operational transresistance amplifier (OTRA) ." Frequenz, 60, pp. 70–76, 2006.

[16] U.Cam,C.Cakir and Oguzhan Cicekoglu,"Novel transimpedance type first order all-pass filter using single OTRA." *AE U—International Journal of Electronics and Communications*, vol. 58, pp. 296–298, 2004.

CHAPTER-3
LITERATURE SURVEY

Extensive literature survey shows that a lot of work has been done on analog signal processing using the voltage as a signal variable. Non-linear circuits using CMOS voltage mode circuit such as squarer, multiplier, log multiplier has been implemented enjoying the advantages of low power dissipation, voltage swing and applications in telecommunication, multimedia, signal processing etc. But with the increasing demand for high speed circuits operating in high frequency region, and the finite gain-bandwidth product associated with operational amplifiers, a different approach is required to be used. CMOS technology, using the current-mode circuits can achieve a considerable improvement in speed, accuracy and bandwidth, overcoming the finite gain–bandwidth product associated with operational amplifiers. Literature survey reveals the emergence of current-mode technology as an alternate approach. A variety of papers have been reported on OTRA during last one and a half decade. Current-mode techniques using the OTRA as active element has became a choice of modern analog design. This thesis includes CMOS realization of OTRA and a number of signal processing and generation applications such as voltage and current mode squarer, CMOS multiplier, frequency multiplier and frequency mixer realization.

3.1 OTRA REALIZATION

3.1.1 CMOS Realization

The realization of OTRA with CMOS, has increased input current range and also linearised the OTRA. Some of the attractive properties of OTRA are their fast speed in comparison with conventional op-amps. CMOS-OTRA is used in many of application instead of commercial operational amplifiers due to its features such as low power consumption, requirement of very low supply voltage and better result at high frequency. It reduces the zero cross-over distortion as compared to conventional op-amp. With the realization of CMOS-OTRA which is Transresistance amplifiers by which the above features arises results in improvement in multiplier, squarer or in any other circuit characteristics. The commercial realizations of operational transresistance amplifier under the name of current differencing amplifier or Norton

amplifier are not widely used as they do not provide internal ground at the input port and they allow the input current to flow in one direction only. The former disadvantage limited the functionality of the OTRA whereas the latter forced to use external dc bias current leading to complex and unattractive designs. In recent years, several high-performance CMOS OTRA realizations have been presented and. This leads to growing interest for the design of OTRA-based analog signal processing circuits.

3.1.2 CFOA Realization

OTRA can also be realized using two AD844AN, a commercially available CFOA integrated chip.

3.2 OTRA APPLICATIONS

3.2.1 Multiplier

An analog multiplier is a device which takes two analog signals and produces an output which is product of these two signals[1]. The analog multiplier is a very important building block of analog signal processing system. It has many applications in automatic gain controlling, phase locked loop, modulation, detection, frequency translation, square rooting of signals, neural networks and fuzzy integrated systems[I].The power consumption is a key parameter in the design of high performance mixed signal integrated circuit. Linearity and accuracy parameters are very important in the analog multiplier design.

The multiplier performs the product of two continuous signals x and y, yielding an output $Z = K.x.y$, where K is a constant with suitable dimension. The linearity, speed, supply voltage and power dissipation are the main goals of the design. The input signal of the analog multiplier circuit can be voltage or current. Thus, it may operate both as a voltage mode or current mode device. Extensive literature review reveals that a large number of analog multiplier configurations have been presented. A dual mode four quadrant multiplier is an important configuration of the analog multiplier which has been extensively worked upon [2-4].Each of these configurations

has it's own advantages and limitations which have been a case of improvement in the succeeding work.

3.2.2 Squarer

With decrease in dimensions of transistor, nonlinear CMOS analog circuits are gaining more attention [5-7]. One of the most useful non-linear block is the squarer[8, 9], since it is the basic circuit for the implementation of various non-linear functions. Some useful applications of squarer circuit are in instrumentation, communication, and control systems.

A squarer circuit produces an output signal proportional to the square of applied input signals. One of the simplest architecture of a squarer circuit is made up of the mixed signal circuit. Literature review shows that in addition to the mixed signal circuit, many more architectures of squarer circuits are available. However, the basic principle of all these architectures is that their output is proportional to the square of applied input signals. Let V_i be differential input signal to a squarer circuit and Vo be output of the squarer circuit. Then,

$$V_o = kV_i^2$$

Where **k** is a constant .

A common feature of all the architectures of the squarer circuit is the use of MOS transistor in saturation mode[10]. Here, the advantage of the input-output characteristic of MOS transistors in the saturation region is utilized. Some of the squarer design has a special quality of operating in both voltage and current mode, one mode at a time. It has two inputs one is current and other is voltage. In voltage mode it provides square of voltage input and in current mode it provides output of current input. Some of the parameters degrading the performance of the squarer circuits are second order effects such as mobility reduction, transistor mismatch, body effect, and channel length modulation[10]. Although, the channel length

modulation effect can be improved by using long-channel devices, other effects are the significant areas of research in the field of squarer circuit design.

3.2.3 Relaxation Oscillator

Square and Triangular waveform generators have wide applications in instrumentation, communication, and signal processing. Conventionally, a square/triangular waveform generator can be realized by using two opamps [11]. Apart from these opamp-based configurations, several new voltage-mode square/triangular waveform generators can be found in the literature [12,13]. Among them, one compact current- controllable generator is designed using two operational transconductance amplifiers (OTAs) [12]. The main drawback is that the oscillation frequency and the amplitude of the squarewave are dependent, which leads to restricted applications of this circuit. In order to solve this problem, a third OTA is included to independently control the oscillation frequency and the amplitude of the squarewave in [13].

Recently, an alternative approach called current-mode technology has attracted considerable attention for analog circuit designers due to its high performance and versatility [14]. Until now, there are many current-mode analog building blocks developed and the related applications have been reported [15].

Past studies have mentioned that the current mode circuits feature the advantages of a higher bandwidth, a better linearity, a larger dynamic range and the noninterference between the gain and the bandwidth [12]. Based on the above considerations, a single operational transresistance amplifier (OTRA) is used in this thesis to design squarewave generator. The function of an OTRA is first introduced in chapter 4. The circuits requiring only a small number of passive components are discussed and analysed.

3.2.4 Frequency mixer

Advancements in wireless technology have largely been driven by the desire for lower cost, low power dissipation, low voltage headroom consumption and low nonlinearity solutions in building high performance RF circuits in silicon, particularly CMOS. However the quest for higher data rate, network capacity, transmit range and multi standard radio solution has driven the CMOS process in high operating frequency band, further exploiting the transit frequency, f_T of the transistor and paving room in the realization of bulky on-chip passive devices, thus eliminating the need for costly discrete components integration.

The circuits for the front-end radio frequency (RF) signal processing[16] are typically implemented in silicon Bipolar, bipolar-complementary metal oxide semiconductor (BiCMOS), or in gallium arsenide (GaAs); whereas, these technologies offer better analog circuit performance in comparison to lossy silicon substrate which makes the design of high quality factor reactive components difficult.

The design architecture of the analog RF signal processing circuits in a standard CMOS technology has a growing concern of performance since a number of current mode circuits using cmos are implemented. OTRA is an active current mode block having advantage of higher bandwidth, better linearity, enhanced dynamic range. In this work an OTRA frequency mixer is implemented in chapter 6.

REFERENCES

[17] Ali Naderi, Abdollah Khoei, Khayrollah Hadidi, Hadi Ghasemzadeh, " A new high speed and low power four quadrant CMOS analog multiplier in current mode" Int JComm2008.

[18] Montree Kumngern, Kobchai Dejhan. "Versatile DualMode Class-AB Four-Quadrant Analog Multiplier" Int J Signal Process 2005;2(ISSN):1304-4494.

[19] Koichi Tanno, Okihiko Ishizuka, Zheng Tang, "Fourquadrant CMOS current-mode multiplier independent of device parameters". IEEE Trans Circuits Syst II 2000;47.

[20] Mirko Gravati, Maurizio Valle, Giuseppe Ferri, Nicola Guerrini, Linder Reyes, "A novel current-mode very low power analog CMOS four quadrant multiplier"

[21] **S.** Liu, Y. Hwang, "CMOS Four-Quadrant Using Bias Feedback Techniques," *IEEE Jour. of Solid-state Circ.,* Vol. 29, No. 6, pp. 750-752, June 1994.

[22] J. Schoeman, T. Joubert, "Four Quadrant Analogue CMOS Multiplier Using Capacitively Coupled Dual-Gate Transistors," *Electronics Letters,* Vol. 32, No. 3, pp. 209-210, Febr. 1996.

[23] S. Liu, C. Chang, *Y.* Hwang, "New CMOS Four-Quadrant Multiplier and Squarer Circuits," *Analog Integrated Circuits and Signal Processing,* Vol. 9, pp. 257-263, 1996.

[24] K. Kimura, "A Bipolar Four-Quadrant Analog Quarter-Square Multiplier Consisting of Unbalanced Emitter-Coupled Pairs and Expansions of Its Input Ranges," *IEEE Jour. of Solid-state Circ.,* Vol. 29, No. 1, pp. 46-55, Jan. 1994.

[25] I. Filanovsky, H. Baltes, "Simple CMOS Analog Square-Rooting and Squaring Circuits," *IEEE Trans.* ***on*** *Circuits and Systems -part I,* Vol. 39, No. 4, pp. 312-315, April 1992.

[26] Ittipong Chaisayun , Somkiat Piangprantong, Kobchai Dejhan, “Versatile analog squarer and multiplier free from body effect” 21 July 2011, Springer Science+Business Media, LLC 2011.

[27] A. S. Sedra and K. C. Smith*, Microelectronic Circuits*, 4th ed. New York: Oxford University Press, 2004.

[28] CA3080 Data Sheet Intersil, Milpitas, CA, Aug. 2004.

[29] W. S. Chung, H. Kim, H. W. Cha, and H. J. Kim, “Triangular/squarewave generator with independently controllable frequency and amplitude,”*IEEE Trans. Instrum. Meas.*, vol. 54, no. 2, pp. 105–109, Feb.2005.

[30] C. Toumazou, F. J. Lidegy, and D. Haigh, *Analog IC Design: The Current-Mode Approach*. Exeter, U.K.: Peter Peregrinus, 1990.

[31] K. Kim, H. W. Cha, and W. S. Chung, "OTA-*R* Schmitt trigger with independently controllable threshold and output voltage levels," *Electron. Lett.*, vol. 33, pp. 1103–1105, Jun. 1997.

[32] J. Crols, M. Steyaert, "A 1.5 *GHz* Highly Linear CMOS Downconversion Mixer," *IEEE Jour.* of *Solid-state Circ.,* Vol. 30, NO. 7, pp. 736-742, July 1995.

CHAPTER-4

CMOS REALIZATION OF OTRA

INTRODUCTION

Operational transresistance amplifier has been realized in a number of configuration by using CMOS circuits. Some of the above mentioned are realized in this chapter using PSPICE as simulation tool. OTRAs are commercially available from several manufacturers under the name of current differencing amplifier but it was not widely used until recently [3]. These commercial realizations do not provide internal ground at the input port and they allow the input current to flow in one direction only. The former disadvantage limited the functionality of the OTRA whereas the latter forced to use external dc bias current leading to complex and unattractive designs [6]. In recent years, several high-performance CMOS OTRA realizations have been presented in the literature [2] and [4]. This leads to growing interest for the design of OTRA-based analog signal processing and non-linear circuits.

4.1 OTRA CMOS REALIZATION-1

CMOS realization of OTRA as presented in [6] is shown in fig.4.1. It consists of a differential current controlled current source (DCCCS) followed by a voltage buffer.

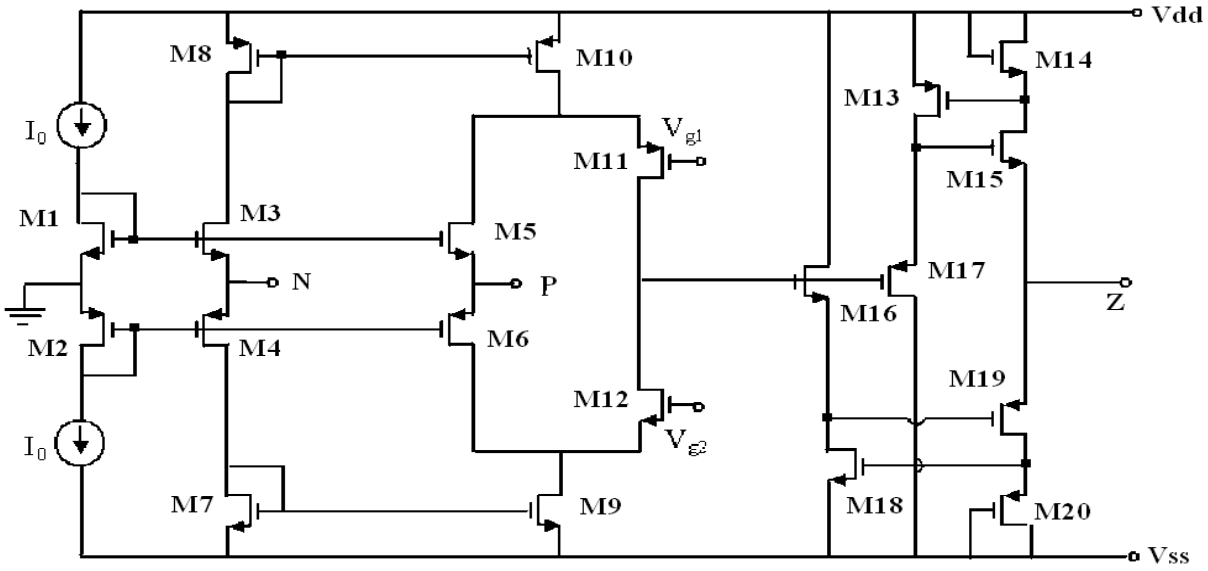

Fig.4.1 CMOS Realization of OTRA

In this circuit, the aspect ratio of the transistor M3 (M4) should be twice as large as those of M1 (M2) and M5 (M6). If the transistor M5 and M6 are removed, the implementation in fig. 4.1 becomes a CFOA, composed of a CMOS CCII followed by the voltage buffer. Since the OTRA can be considered as a collection of current and voltage-mode unity gain cell, this element is free from many parasitic and is expected to be suitable for high-frequency operation. The PSpice schematic of OTRA is shown in fig 4.2 and its simulated DC response is shown in fig.4.3.

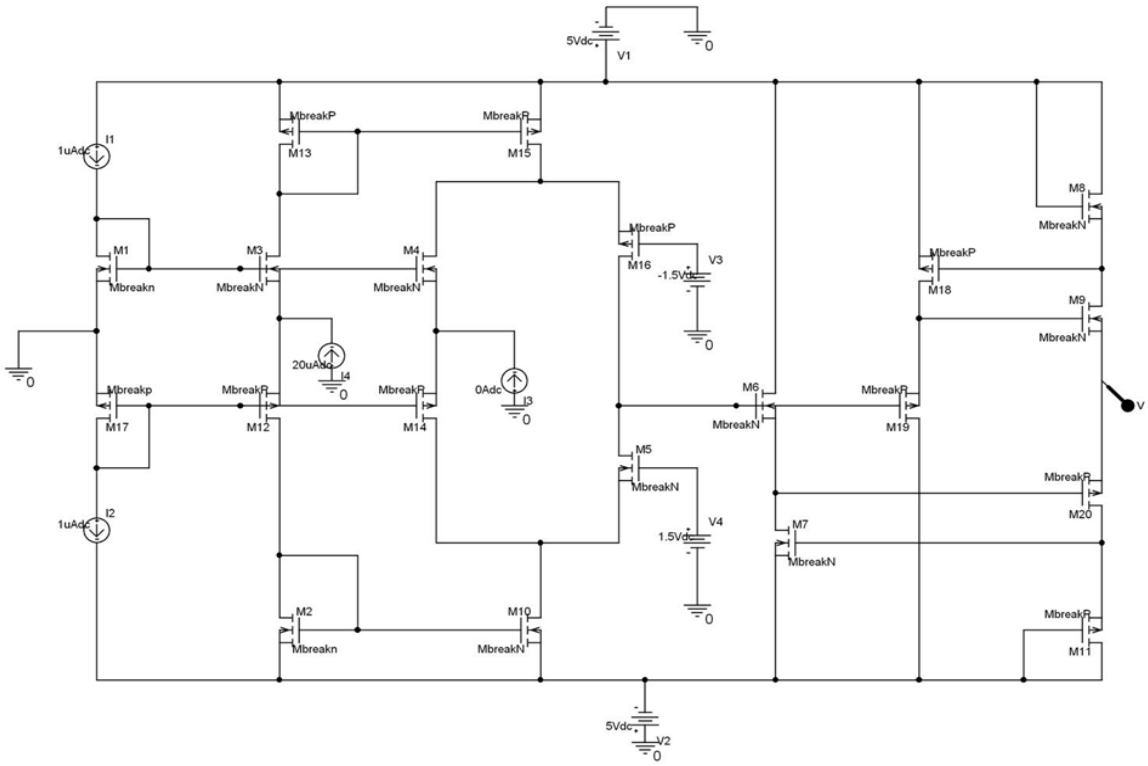

Fig.4.2 Pspice Schematic of CMOS realization of OTRA (Internal Block 1)

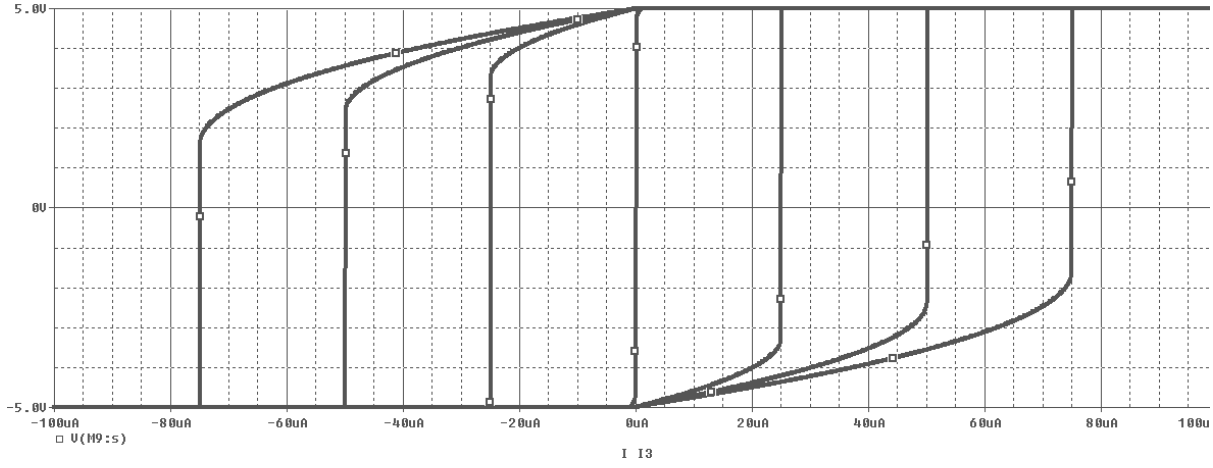

Fig.4.3 Simulated DC Response of the OTRA Circuit

4.2 OTRA CMOS REALIZATION-2

The OTRA presented in [3] is shown in fig.4.4. It is based on the cascaded connection of the modified differential current conveyor (MDCC) [5] and a common source amplifier. The MDCC provides the current differencing operation, whereas the common source amplifier provides high gain.

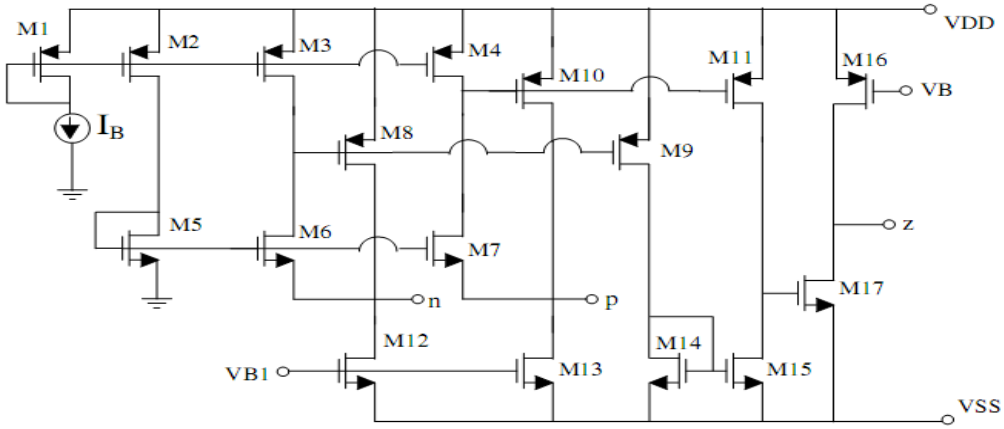

Fig.4.4 CMOS Realization of OTRA

The current mirrors formed by (M4-M7) forces equal currents (I_B) in the transistors M1, M2 and M3. This operation drives the gate to source voltages of M1, M2 and M3 to be equal and consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs (M4 and M5), (M8 and M9), (M10 and M11) and (M14 and M15) provide the current differencing operation, whereas the common source amplifier (M17) achieves the high gain stage [2]. In this operation it is assumed that each of the groups of the transistors (M1-M3), (M4-M7), (M8 and M9), (M10 and M11), (M12 and M13) as well as (M14 and M15) are matched and all the transistors operate in saturation region. The PSpice schematic of the circuit proposed in [3] is shown in fig 4.5 and simulated DC response of the same is shown in fig 4.6.

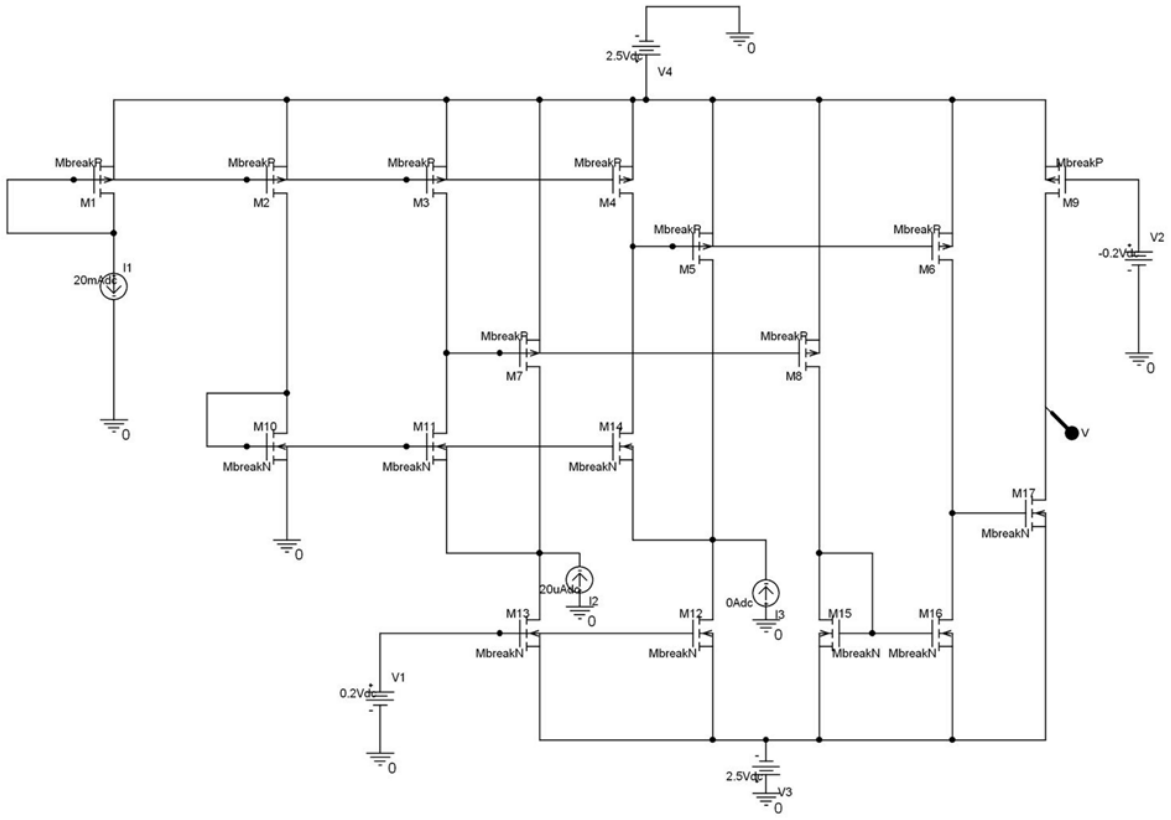

Fig.4.5 Pspice Schematic of CMOS realization of OTRA (Internal Block 2)

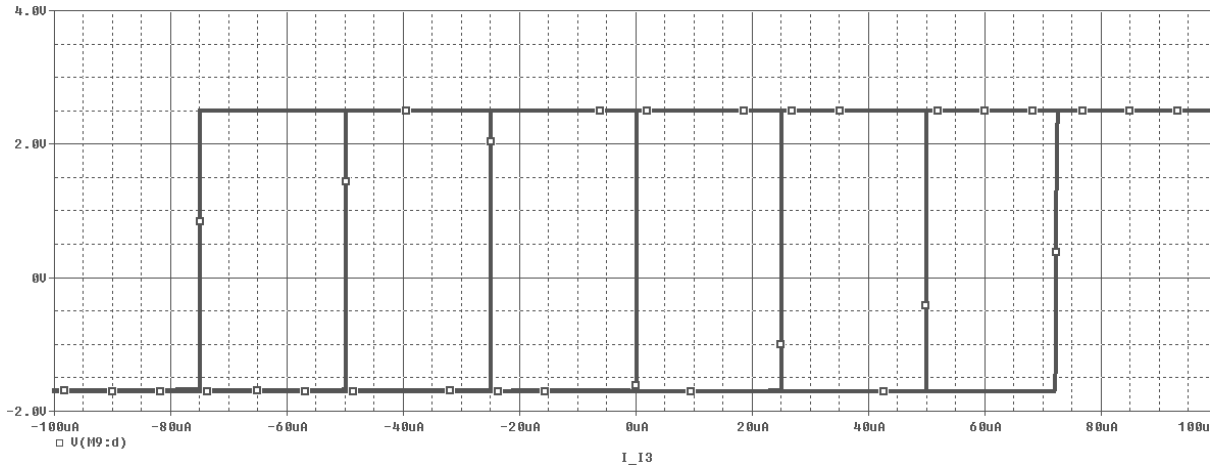

Fig.4.6 Simulated DC Response of the OTRA Circuit

4.3 OTRA CMOS REALIZATION-3

Another CMOS realization of the low power wide band OTRA as presented in [4] is shown in circuit 4.7. It is based on the cascaded connection of the modified differential current conveyor (MDCC) and a common source amplifier.

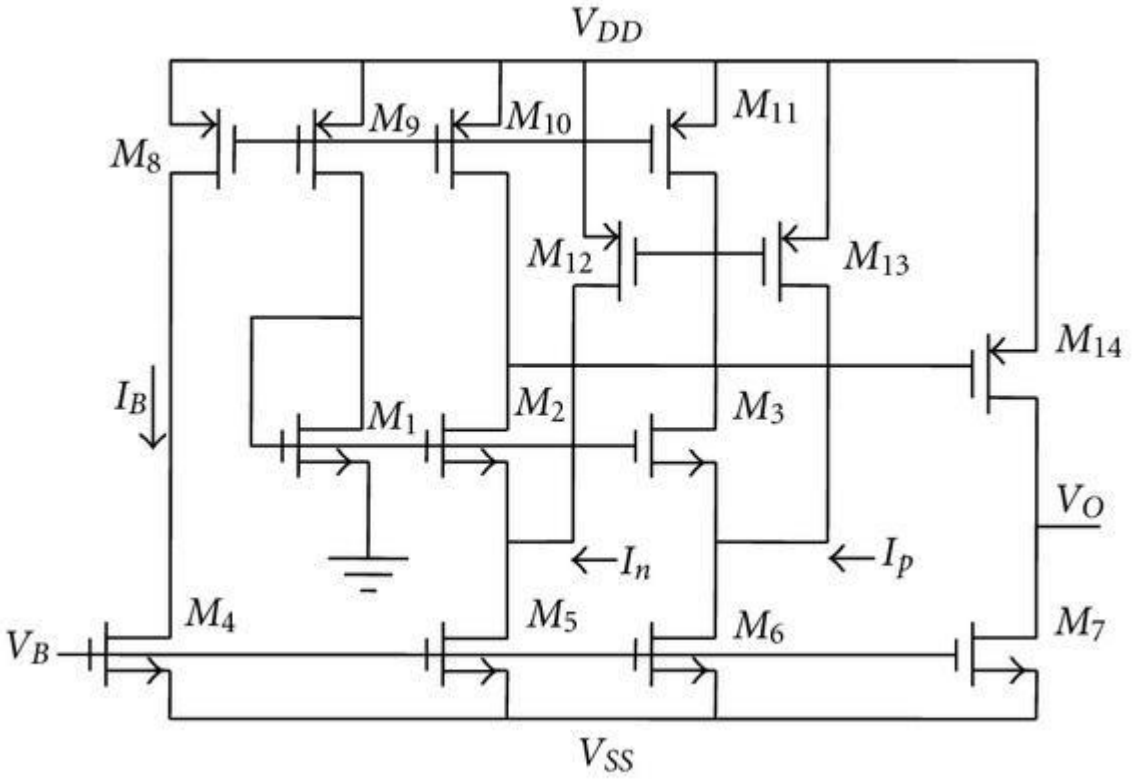

Fig.4.7 CMOS Realization of OTRA

Assuming that each of the groups of the transistors (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are matched and assuming that all the transistors operate in the saturation region, the circuit operation can be explained as follows.

The current mirrors formed by (M8-M11) forces equal currents (I_B) in the transistors M1, M2 and M3. This operation drives the gate to source voltages M1, M2 and M3 to equal and, consequently, forces the equal terminals to be virtually grounded.

The current mirrors formed by the transistor pair (M10 and M11) and (M12 and M13) provide the current differencing operation, whereas the common source amplifier (M14) achieves high gain. The modified OTRA has smaller number of current mirrors than the OTRA introduced in [2] which reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Moreover, this OTRA

uses smaller number of transistors which reduces the power dissipation. The PSpice schematic of the OTRA is shown in fig.4.8. The simulated DC response is shown in fig.4.9.

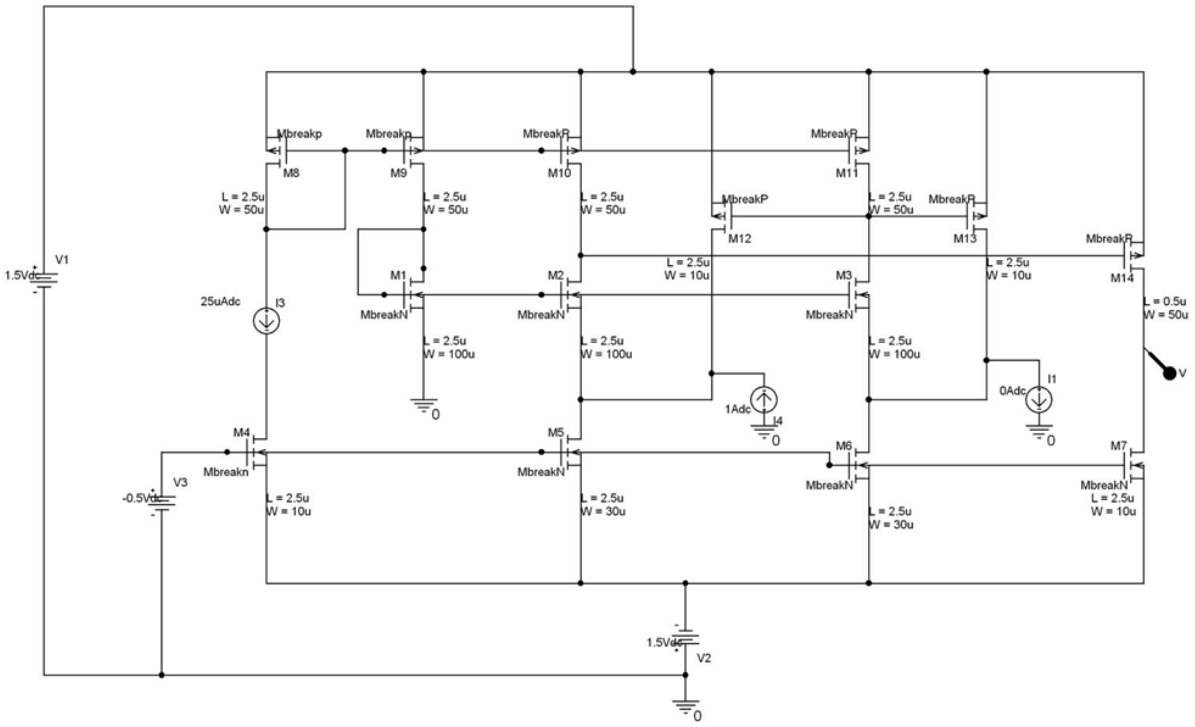

Fig.4.8 Pspice Schematic of CMOS realization of OTRA (Internal Block 3)

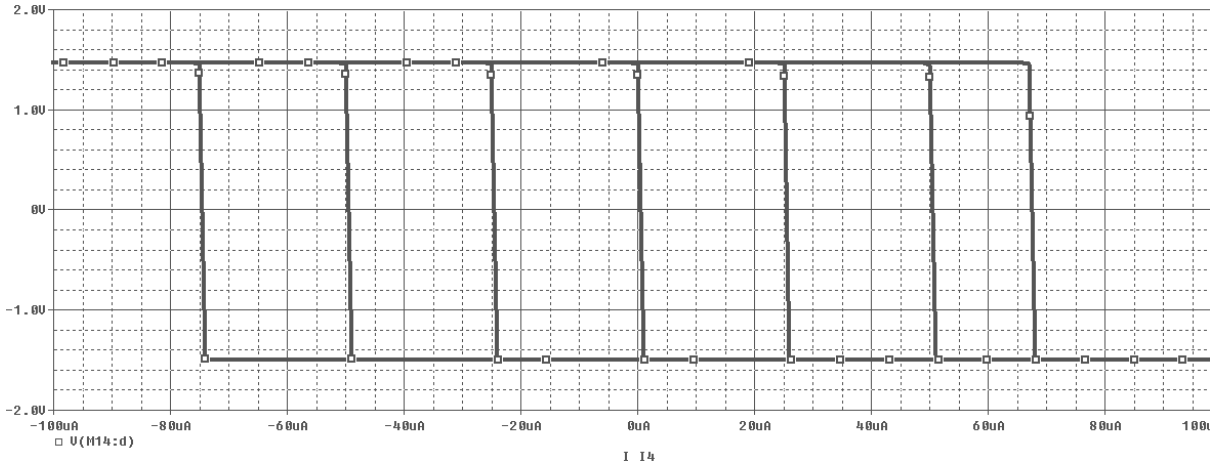

Fig.4.9 DC analysis of the realized OTRA

4.4 OTRA CFOA REALIZATION-4

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non- inverting applications. The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps.

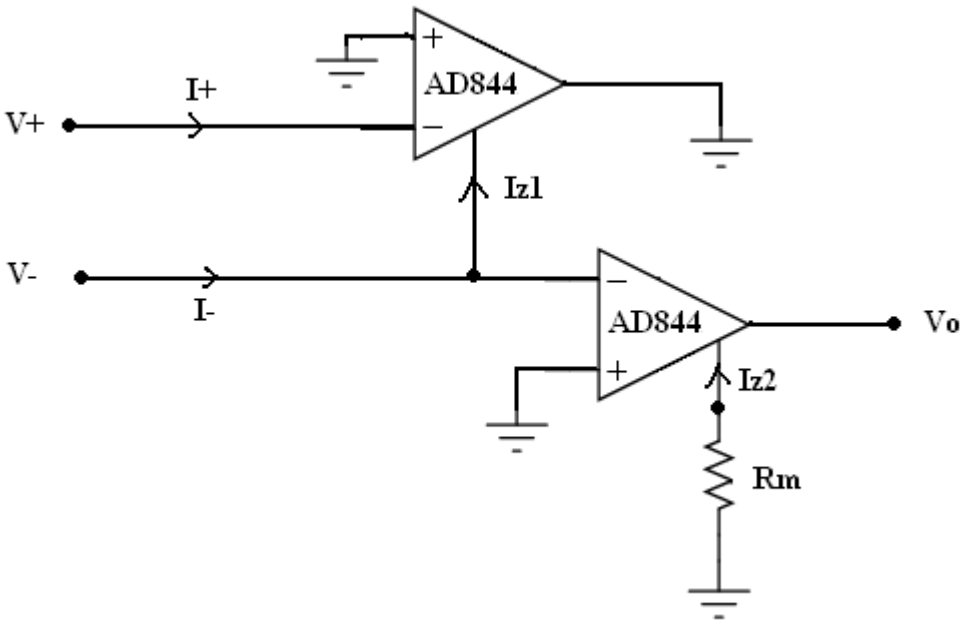

Fig.4.10 CFOA Realization of OTRA

In order to simulate the virtual ground for the two input terminals of the OTRA, the non-inverting terminals of the AD844ANs have been grounded. TheAD844AN differs from the conventional operational amplifier in that the voltage on the non inverting signal input is transferred to the inverting input. Thus an inherent virtual short exists

between these two terminals without any external negative feedback path. Owing to this characteristic, the following relations can be obtained.

$$V_{+} = V_{1-} = V_{1+} = 0 \;\; \& \;\; V_{-} = V_{2-} = V_{2+} = 0 \quad (4.1)$$

Another feature of the AD844AN is that the current into the inverting terminal is equal to the current into the slewing node T_Z & the output voltage is the same as the voltage appearing at this pin.

$$I_{T1} = I_{1-} = I_{1+} \quad (4.2)$$

$$V_{o1} = V_{T1} = V_{2-} = 0 \quad (4.3)$$

$$I_{T2} = I_{2-} = I_{-} - I_{T1} = I_{-} - I_{+} \quad (4.4)$$

$$V_o = V_{o2} = V_{T2} = -R_m * I_{T2} = R_m * (I_{+} - I_{-}) \quad (4.5)$$

Thus wiring two CFOAs in this manner shown in figure 4.10, the terminal equations of OTRA can be realized. Fig 4.11 is the schematic of OTRA realized using CFOAs and fig 4.12 shows the DC response.

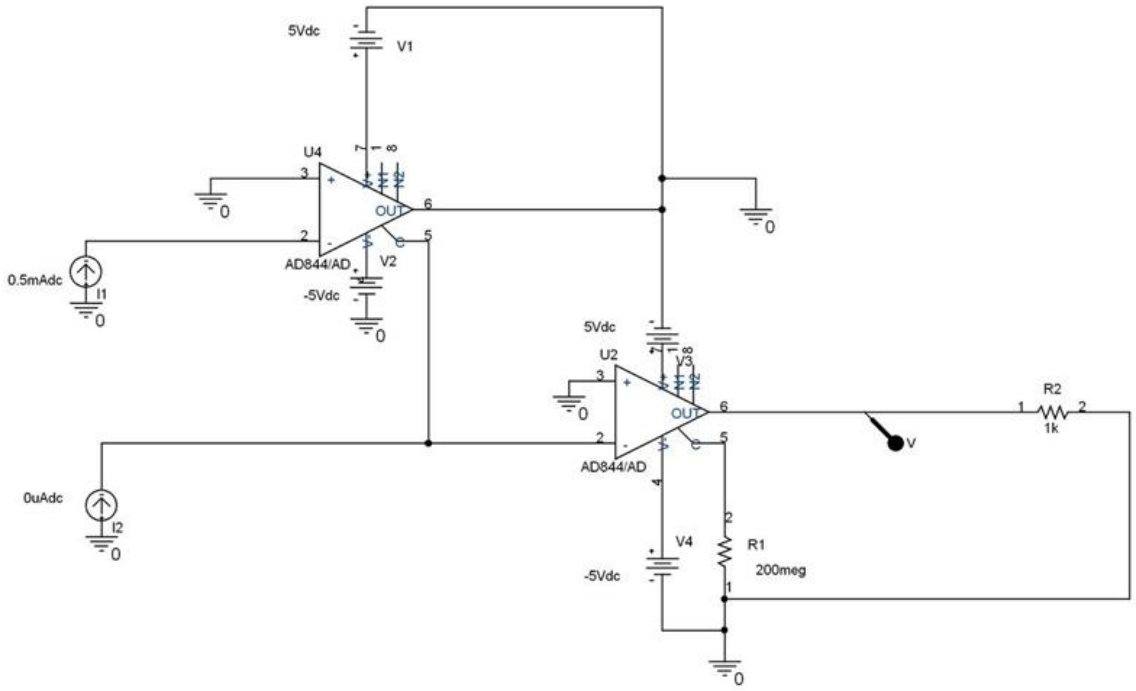

Fig.4.11 Pspice Schematic of CMOS realization of OTRA (Internal Block 4)

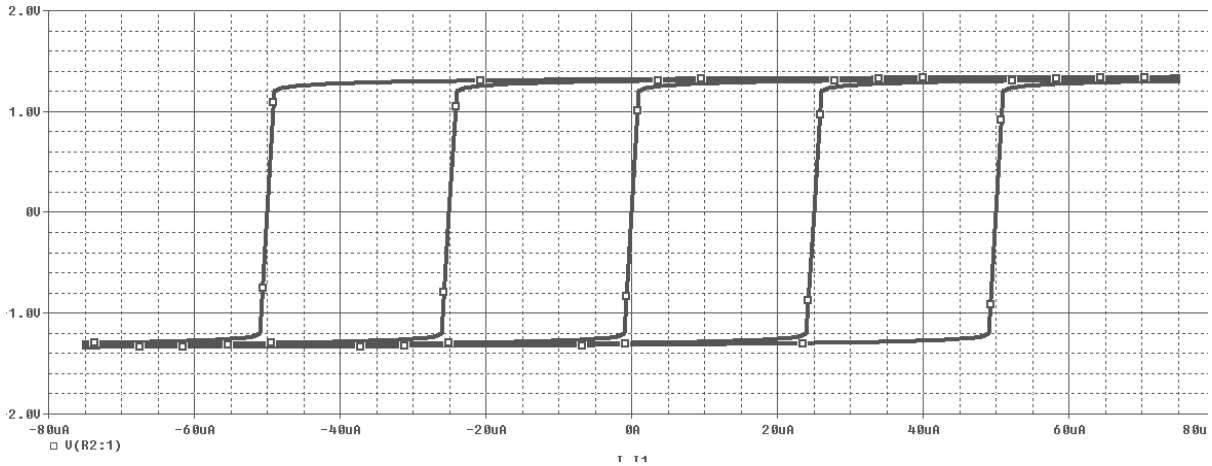

Fig.4.12 DC analysis of the realized OTRA

REFERENCES

[33] CMOS Current-Mode Circuits for Data Communications - Fei Yuan

[34] J.J. Chen, H.W. Tsao, and C. Chen, "Operational transresistance amplifier using CMOS technology." *Electronics Letters*, vol. 28, no. 22, pp. 2087–2088, 1992.

[35] Wadsworth, D.C. Accurate current conveyor topology and monolithic implementation. *Proc. IEE G*, 1990, vol. 137, no. 2, p. 88-94.

[36] Microelectronics Journal 30 (1999) 157–160 'A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters.

[37] H.O. Elwan, A.M. Soliman, CMOS differential current conveyors and applications for analog VLSI, Analog Integrated Circuits and Signal Processing 11 (5) (1996) 35–45.

[38] Hassan Mostafa, Ahmed M. Soliman, A modified CMOS realization of the operational transresistance amplifier (OTRA) ." Frequenz, 60, pp. 70–76, 2006.

[39] U.Cam,C.Cakir and Oguzhan Cicekoglu,"Novel transimpedance type first order all-pass filter using single OTRA." *AE U—International Journal of Electronics and Communications*, vol. 58, pp. 296–298, 2004.

[40] Toumazou C, Lidjey FJ, Haigh D. Analog IC design: the current-mode approach. Peter Peregrinus, UK: Exeter; 1990.

[41] CMOS operational transresistance amplifier for analog signal processing - Khaled n. Salama, Ahmed m. Soliman, 1999

[42] SEDRA, A.S., SMITH, K.C. A second generation current conveyor and its application. *IEEE Trans.*, 1970, CT-17, p. 132-134.

[43] FABRE, A. Third generation current conveyor: A new helpful active element. *Electron. Lett.*, 1995, vol. 31, no. 5, p. 338–339.

CHAPTER-5

CMOS REALIZATION OF NON-LINEAR CIRCUITS

INTRODUCTION

A non-linear circuit is an electrical system that does not follow the principle of superposition and homogeneity. It alters the characteristics of a signal with respect to it's system function. A non-linear circuit is not desirable for linear application such as amplifier. However non-linear circuits has its wide application in non-linear circuit such as squarer, multiplier, mixer circuit widely used in communication system. These are often used in electronic systems in signal processing for operations such as log, multiplication. Each signal requires some form of operation before it could be applied to some use. A number of active building blocks can be used to realize non-linear circuits such as OTRA, current conveyor (CCII), OPAMP, current feedback op-amps (CFOA), four-terminal floating nullor (FTFN) and operational transconductance amplifier (OTA) etc. In this section various non-linear circuits using CMOS have been designed and simulated using PSPICE software. In next section a number of non linear circuit are realized using OTRA as an active element.

5.1 SQUARER CIRCUIT REALIZATION USING CMOS

Squaring circuit is a nonlinear signal processing function which is very useful in instrumentation, communication, and control systems. Nonlinear circuits [1–10] have been published. Some nonlinear circuits operated in the voltage mode [1, 2] and some others were designed to operate in the current mode [3–5]. In the recent past, the analog circuit design using the current mode approach has gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slew rate, low power consumption, and simple circuitry [5]. However, some sensors and transducers give output signal as voltage signal; for example, voltage transformer and thermocouple. So the voltage mode analog circuits are still need. To design a circuit that can be connected to voltage or current mode analog circuit, the versatile analog multiplier using operational transconductance amplifier (OTA) [6] was proposed, but it acquired error due to finite input resistance. Then, the versatile analog multiplier

using second generation current controlled current conveyor (CCCII) [7] was reported, but it consumed more power consumption. The versatile CMOS analog multipliers [8, 9] and the two-output multiplier [10] that have low power consumption were proposed, but their output depended on the body effect. In this proposed work, we design the circuits that have low power consumption and are free from the body effect. In addition, the proposed circuits in which their inputs can take the current signal or the voltage signal are interesting for application as versatile blocks in library of circuit architectures for automated circuit design [11, 12].

Squarer circuit is most widely used in signal processing. They are generally used for squaring a signal which can be further used for multiplier and frequency multiplier circuits. The squarer consists of a mixed signal circuit, a voltage inverting amplifier, a differential amplifier, a current mirror, and a voltage divider. The mixed signal circuit formed from transistors M_1 and M_2 shown in Fig. 5.1 acts as mixing the input voltage (V_{in}) and the input current (I_{in}), and gives the output as the voltage signal (V_1).

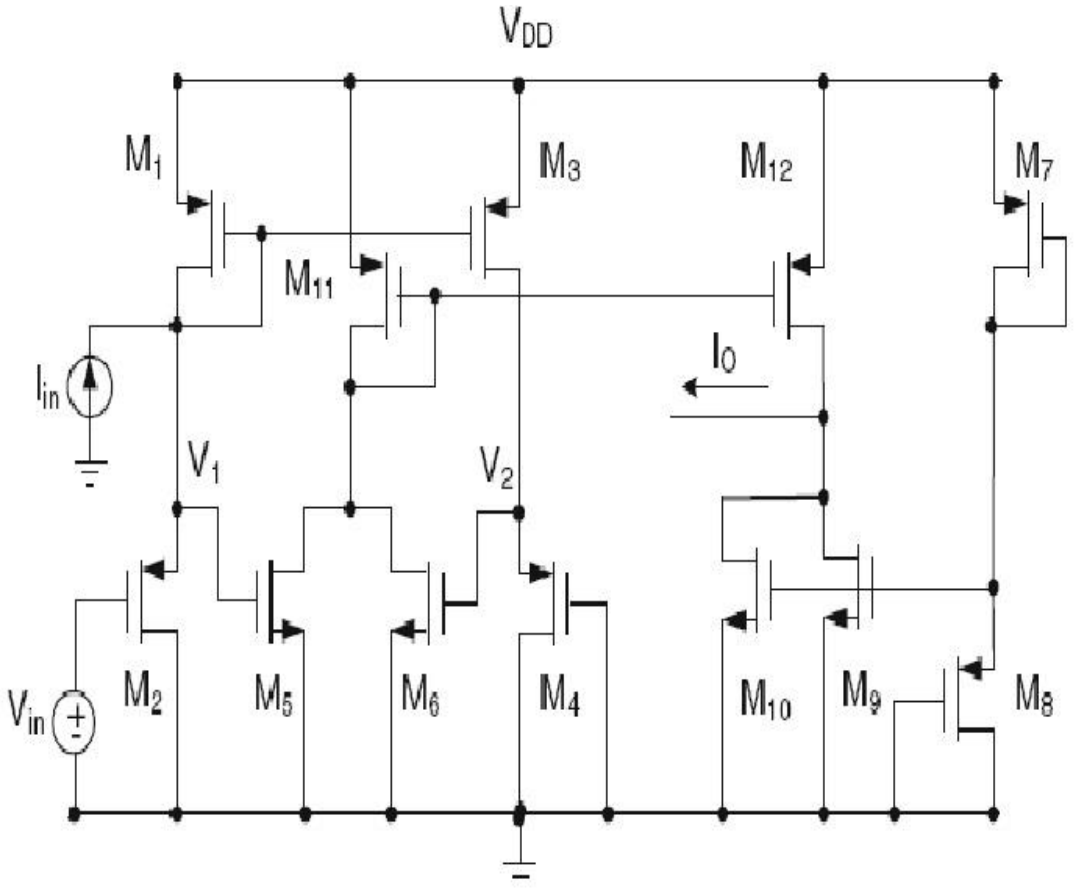

Fig 5.1 CMOS Squarer circuit

Applying Kirchhoff's current law at node V_1 obtains

$$I_{in} = I_{D2} - I_{D1} \tag{5.1a}$$

Since $I_D = K_N(V_{GS} - V_{TN})^2$; $V_{GS} > V_{TN}, V_{DS} \geq V_{GS} - V_{TN}$ (5.1b)

$I_D = K_P(V_{GS} - V_{TP})^2$; $V_{GS} < V_{TP}, V_{DS} \leq V_{GS} - V_{TP}$ (5.3b)

Where $K_N = 0.5\mu_n C_{OX} W/L$ and $K_P = 0.5\mu_p C_{OX} W/L$ are the trannsconductance parameters of NMOS and PMOS, respectively. V_{TN} and V_{TP} are the threshold voltages of respectively. V_{GS} and V_{DS} are the gate to source voltage and the drain to source voltage, respectively.

Now

$$I_{D1} = K(V_1 - V_{DD} - V_{TO})^2$$

$$I_{D2} = K(V_{in} - V_1 - V_{TO})^2$$

So from equation(5.1a)

$$I_{in} = I_{D2} - I_{D1}$$

(5.1d)

$$I_{in} = K(V_{in} - V_1 - V_{TO})^2 - K(V_1 - V_{DD} - V_{TO})^2$$

$$I_{in} = K(V_{in} - V_1 - V_{TO} + V_1 - V_{DD} - V_{TO})(V_{in} - V_1 - V_{TO} - V_1 + V_{DD} + V_{TO})$$

$$I_{in} = K(V_{in} - V_{DD} - 2V_{TO})(V_{in} - 2V_1 + V_{DD})$$

$$V_{in} - 2V_1 + V_{DD} = \frac{I_{in}}{K(V_{in} - V_{DD} - 2V_{TO})}$$

$$V_1 = \frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD} + 2V_{TO} - V_{in})} + \frac{V_{DD}}{2} \qquad (5.1e)$$

The voltage inverting amplifier formed from transistors M_3 and M_4, and the drain current of M_3 is equal to that of M_4. The voltage V_2 is calculated by using equation

$$V_2 = -\left[\frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD} + 2V_{TO} - V_{in})}\right] + \frac{V_{DD}}{2} \qquad (5.1f)$$

The differential amplifier consists of the transistors M_5 and M_6 which are perfectly matched, and the summation of the drain current of M_5 and M_6 can be expressed as

$$I_{D5} + I_{D6} = 2K\left[\left(\frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD} + 2V_{TO} - V_{in})}\right)^2 + \left(\frac{V_{DD}}{2} - V_{TO}\right)^2\right] \qquad (5.1g)$$

The voltage divider circuit, consisting the transistors M_7 and M_8 which are perfectly matched, is used for generating voltage signal VDD/2. The summation of the drain current of M_9 and M_{10} can be expressed as

$$I_{D9} + I_{D10} = 2K\left(\frac{V_{DD}}{2} - V_{TO}\right)^2 \qquad (5.1h)$$

The mixed signal circuit is applied to the proposed squarer which our squarer circuit versatile means we can apply voltage and current input.

The mixed signal circuit shown in fig 5.2

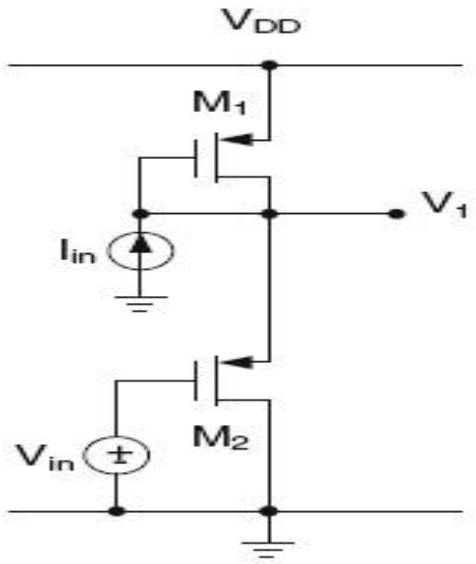

Fig 5.2 Mixed signal circuit

Suppose that the ratio of the current mirror formed from transistors M_{11} and M_{12} is equal to 1:1, and the output current of the squaring circuit can be defined and expressed as

$$I_o = I_{D5} + I_{D6} - I_{D9} - I_{D10} \tag{5.2a}$$

Thus ,

$$I_o = 2K\left(\frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD} + 2V_{TO} - V_{in})}\right)^2$$

Note that if V_{in}= 0, the output current will be the square of I_{in}

$$I_o = 2K\left(\frac{I_{in}}{2K\big((V_{DD} + 2V_{TO} - V_{in})\big)}\right)^2 \tag{5.2b}$$

and if I_{in} = 0, the output current will be the square of V_{in}

$$I_o = 2K\left(\frac{V_{in}}{2}\right)^2 \qquad (5.2c)$$

From (5.2b) and (5.2c), it can be shown that the proposed squarer is the versatile squarer.

The input range of the squarer is determined by the saturation condition of M_5 and M_6, and expressed as

$$V_{TO} - \frac{V_{DD}}{2} \leq \frac{V_{in}}{2} + \frac{I_{in}}{2K(V_{DD} + 2V_{TO} - V_{in})} \leq \frac{V_{DD}}{2} - V_{TO} \qquad (5.2d)$$

The Eq. 5.2d shows that the input range depends on difference of VDD/2 and V_{TO}. Consider the body effect on the proposed squarer circuit. All the NMOS transistors have sources connected to the ground, while all PMOS transistors, except M_2, M_4, and M_8 which have an independent n-well, have sources connected to the positive supply rail. This causes no variation in the threshold voltage because the source to body voltage is maintained equal to zero at all times. In addition, this squarer used only two CMOS transistors connected between power supply lines in order to operate under low power supply voltage.

5.1.1 Results

Simulation result :

The proposed circuits were simulated in PSpice using the 0.5μm MOSIS CMOS models with NMOS threshold voltage V_{TN} = 0.42 V and PMOS threshold voltage V_{TP} = -0.55 V. The aspect ratio of transistors is shown in Table 1.

Table 1: W/L ratio of squarer circuit

Transistor	**W/L(μm/μm)**
M_1-M_4	10/1
M_5-M_{10}	1/1
M_{11}-M_{12}	10/0.5

The bias voltage was set to V_B = 0.465 V and the output terminal was connected to $V_{DD}/2$. Substituting V_{TN} = 0.42 V and I_{in} = 0 into Eq. 5.2d, the input range of the proposed squarer is related to V_{DD} in Table 2.

TABLE 2 : voltage input range of proposed squarer

V_{DD}	**Voltage input range (V_{in})**	$\frac{\Delta Vin}{\Delta VDD} \times 100\%$
1.5	-0.66V<V_{in}<0.66V	88%
1.4	-0.56V<V_{in}<0.56V	80%
1.3	-0.46V<V_{in}<0.46V	71%
1.1	-0.26V<V_{in}<0.26V	47%
1.0	-0.16V<V_{in}<0.16V	32%
0.9	-0.06V<V_{in}<0.06V	13%

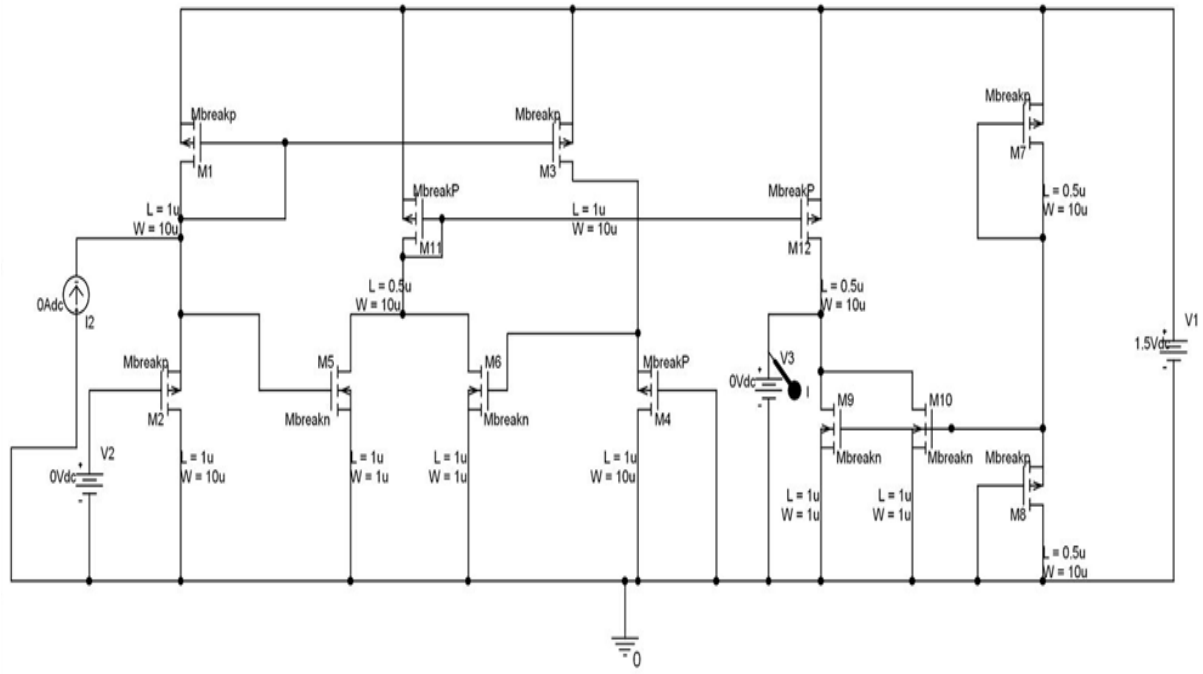

Fig.5.3 PSpice Schematic of versatile squarer circuit

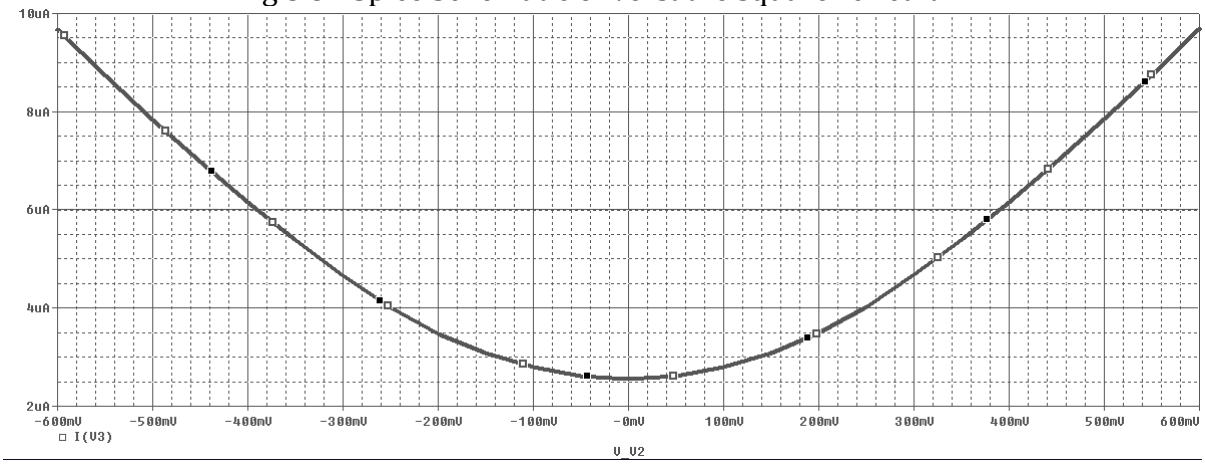

Fig.5.4 DC characteristic of squarer of votage input

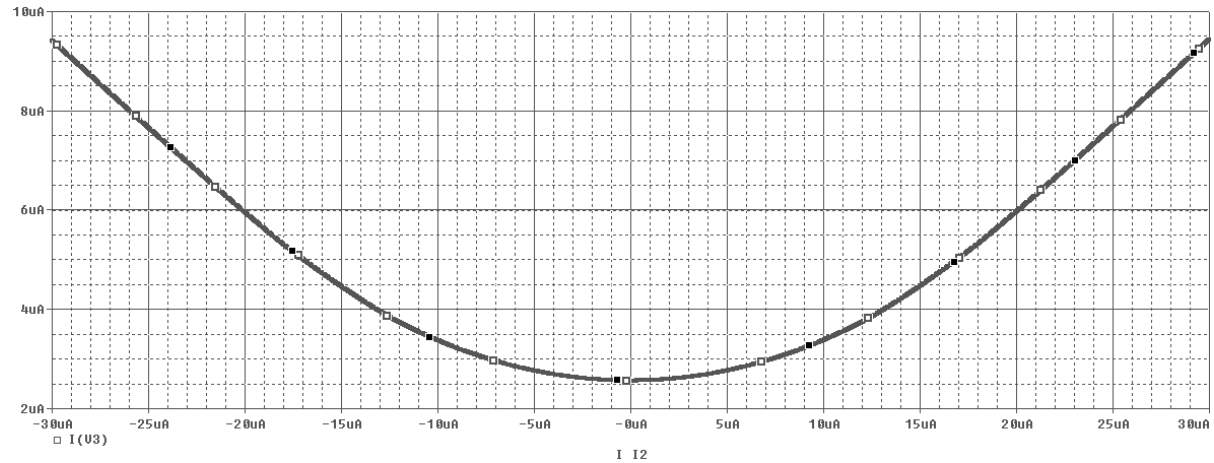

Fig.5.5 DC characteristic of squarer of current input

5.2 ANALOG ADDER CIRCUIT REALIZATION USING CMOS

Adder is important block we want to multiply to analog signal. Since basic idea of multiplication is such that:

Suppose there two analog signal A and B the to obtain multiplication of these signal we can write it as $(A+B)^2-(A-B)^2=4AB$; so first we have to add these signal and then squaring of these signal we get multiplication.

The adder circuit shown in fig.5.5 which consist a current mirror, the identical four transistor M_{11}-M_{14}, and the tail current source formed by transistor M_{20} and M_{21}

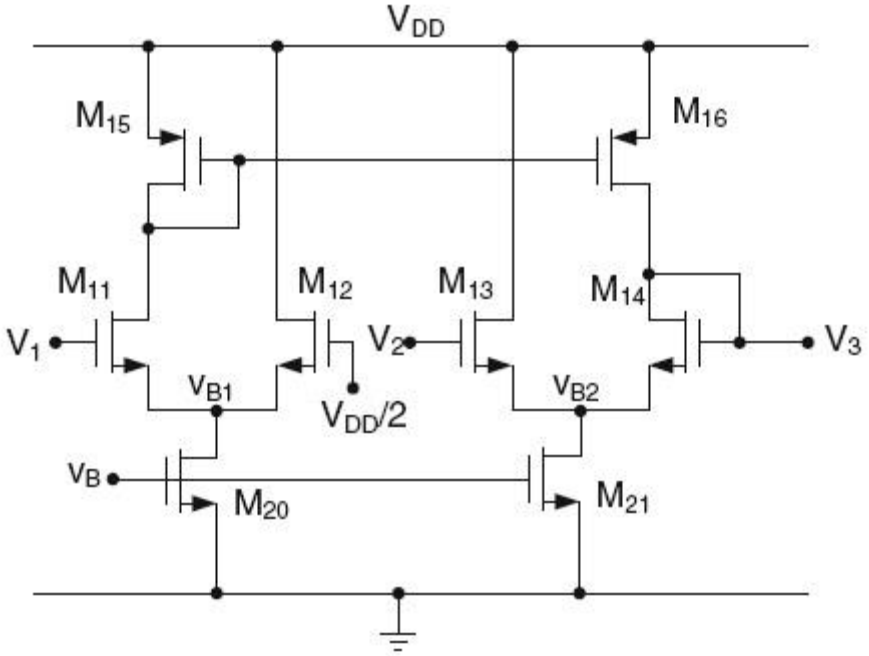

Fig.5.6 Analog adder circuit

Consider Fig. 5.5, if the groups of the transistors (M_{11}-M_{14}), (M_{15}-M_{16}), and (M_{20}-M_{21}) are perfectly matched, it finds $I_{D11} = I_{D14}$ and $I_{D12} = I_{D13}$. Then we can express the relation of the voltage signals V_1, V_2 and V_3 as follows

Since drain current I_{D11} can written as

$$I_{D11} = K(V_1 - V_{B1} - V_{TO})^2 \qquad (5.3a)$$

Since $I_{D11} = I_{D14} = K(V_1 - V_{B1} - V_{TO})^2$

Now I_{D12} can be written same way

$$I_{D12} = K\left(\frac{V_{DD}}{2} - V_{B1} - V_{TO}\right)^2 \qquad (5.2b)$$

And I_{D13} will be

$$I_{D13} = K(V_2 - V_{B2} - V_{TO})^2 \qquad (5.3c)$$

Since all transistor M_{20} and M_{21} are identical, applied gate to source voltage also equal so drain current through these transistor is also equal.

From adder fig. it is clearly indicate that

$$I_{D11} + I_{D12} = I_{D13} + I_{D14}$$

We already know that

$$I_{D11} = I_{D14};$$

$$I_{D12} = I_{D13}$$

$$K\left(\frac{V_{DD}}{2} - V_{B1} - V_{TO}\right)^2 = K(V_2 - V_{B2} - V_{TO})^2$$

$$\frac{V_{DD}}{2} - V_{B1} - V_{TO} = V_2 - V_{B2} - V_{TO}$$

$$V_2 = \frac{V_{DD}}{2} - V_{B1} + V_{B2}$$

Now writing the drain current equation for M14

$$I_{D14} = K(V_3 - V_{B2} - V_{TO})^2$$

$$K(V_1 - V_{B1} - V_{TO})^2 = K(V_3 - V_{B2} - V_{TO})^2$$

$$V_1 - V_{B1} - V_{TO} = V_3 - V_{B2} - V_{TO}$$

$$V_1 - V_{B1} + V_{B2} = V_3$$

$$V_3 = V_1 + V_2 - \frac{V_{DD}}{2} \qquad (5.3d)$$

5.2.1 Results

Table:3 W/L ratio of adder circuit

Transistor	**W/L(µm/µm)**
M_{11}-M_{14}	10/0.5
$M_{15}M_{19}$	5/0.5
M_{20}-M_{21}	5/0.5

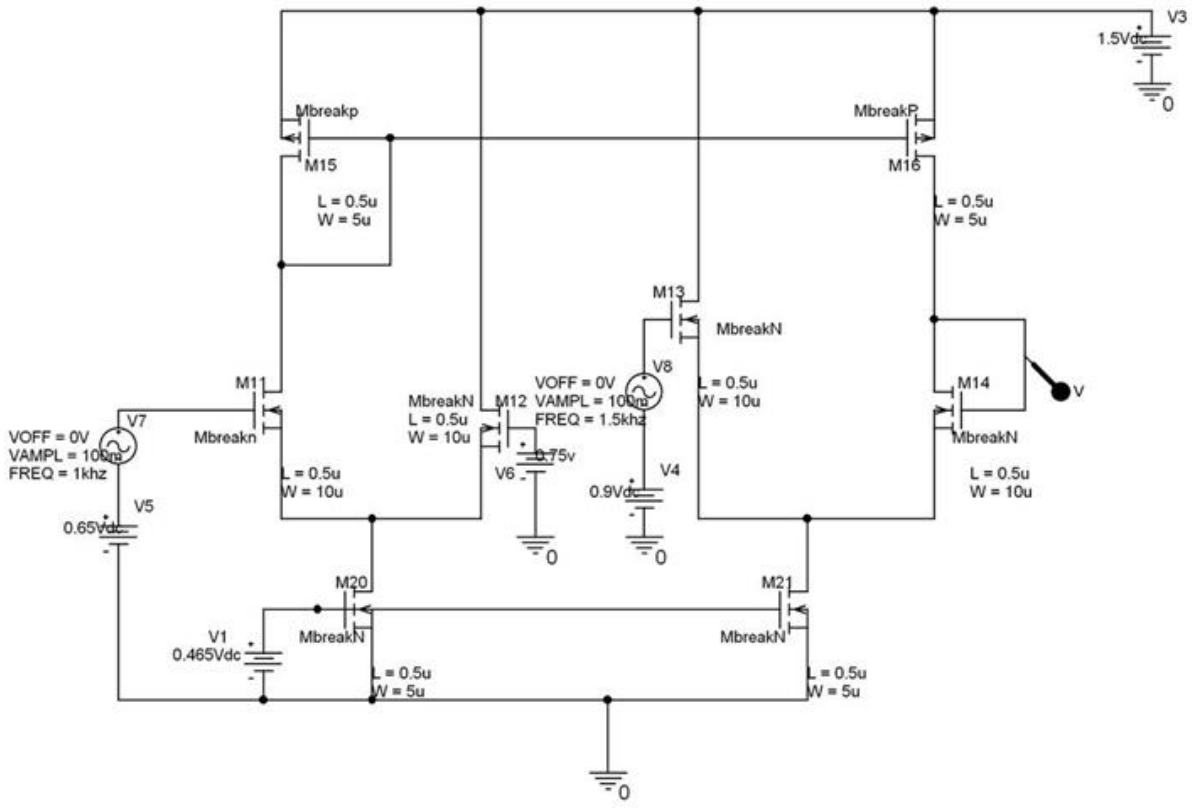

Fig.5.7 PSpice Schematic of analog adder circuit

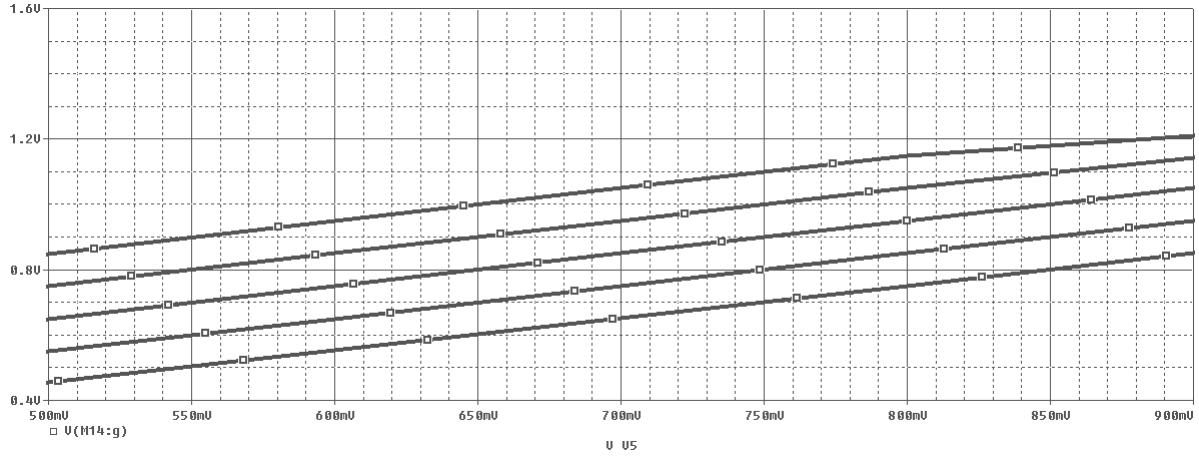

Fig.5.8 DC characteristc of analog adder circuit

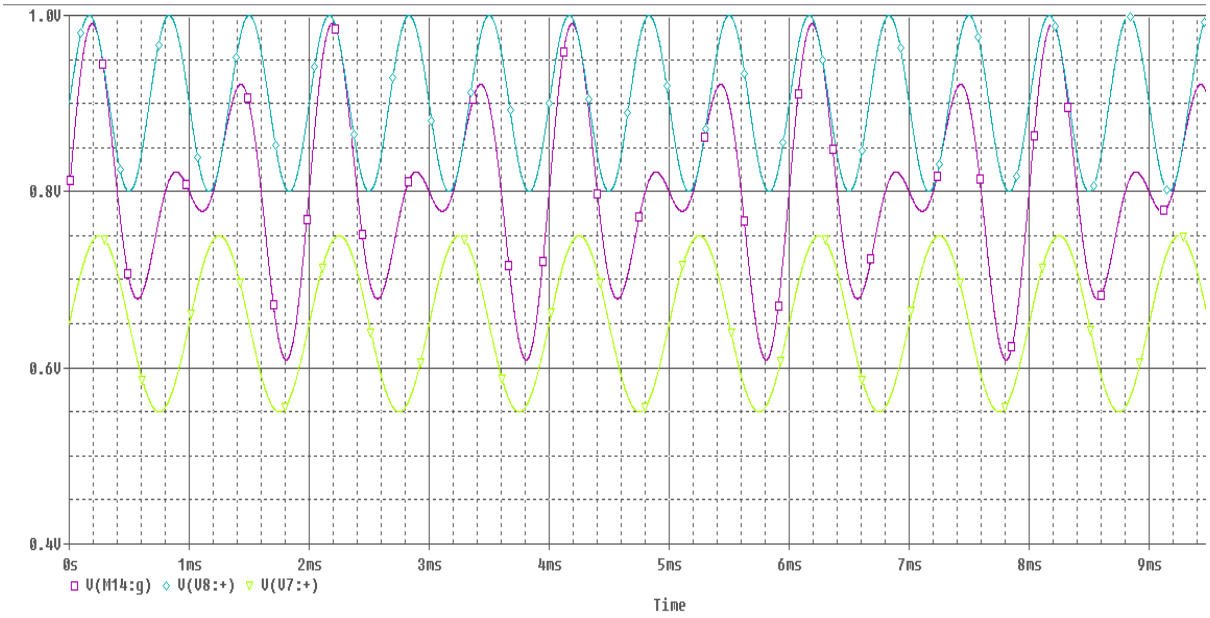

Fig.5.9 AC characteristc of analog adder circuit

5.3 MULTIPLIER CIRCUIT REALIZATION USING CMOS

The early attempts to realize multipliers used the triode region of operation in FET transistors. Later on, this mode of operation was used to build multipliers in an indirect way, via application of linear transconductance amplifiers. The triode region is nowadays widely used in continuous-time filters where the FET's are used as controlled resistors, but its application in multipliers, squarers, and square-rooters is only occasional. These circuits are designed using mainly the saturation (pinch-off) region of operation .

Yet the operation of the proposed circuits is based on the saturation operation. The circuits include the nested connection of two devices (this connection is sometimes used in current mirrors with a large ratio of the output and input currents). In this connection one of the devices will be in the pinch-off region.

Analog multipliers are important circuit blocks for many applications such as frequency mixers, variable frequency oscillators, adaptive filters, etc. In order to improve the overall power efficiency of such applications which is now regularly required for modern analog and mixed signal design dedicated for portable equipments, the analog multiplier to be used must be able to operate under a reduced supply voltage and consume low current. In CMOS technology, a low-voltage high

performance four-quadrant analog multiplier circuit may be implemented by cascading six identical 2-input "combiner" cells Fig.5.9. This topology has been particularly popular in RF applications for the implementation of up and down-conversion mixers . Since each combiner may be realized by a source drain coupled MOSFET pair connected to a resistor, the required supply voltage is very low (e.g., 1.2V). Although, the circuit has a very wide bandwidth, its linearity is degraded when component mismatch is concerned.

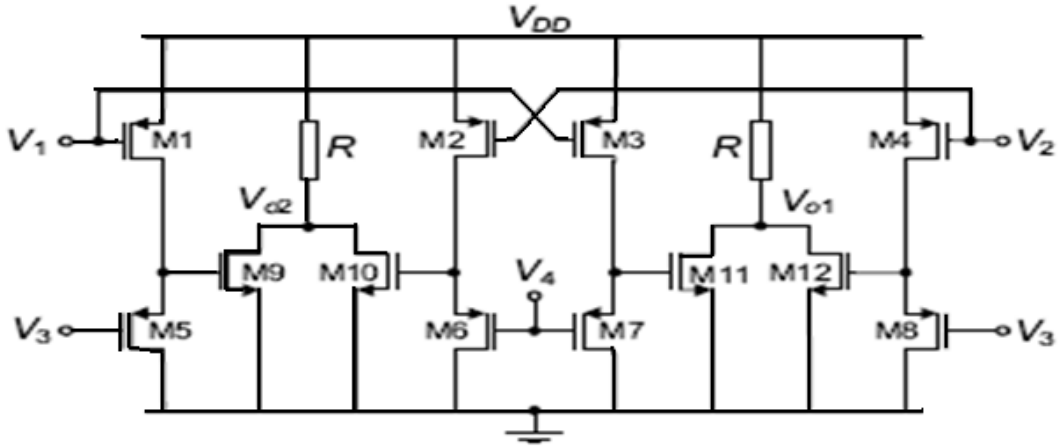

Fig.5.10 Four quadrant analog multiplier circuit

Differential input voltages, defined by $V_{id1} = V_1 - V_2$ and $V_{id2} = V_3 - V_4$, are applied to input terminals of the four subtractor cells (M1 & M5, M2 & M6, M3 & M7 and M4 & M8), the outputs of which are connected to input terminals of the two combiner cells (M9, M10 & R and M11, M12 & R). In order to bias the circuit to operate in the saturation region, the minimum supply voltage requirement is

$$V_{DD} = 2V_{effp} - |V_{tp}|$$

where V_{effp} is the effective (or saturation) voltage of the *p*channel devices M1-M8. Note that, for modern sub-micron CMOS process technologies with $|V_{tp}| < 0.6V$ and by careful selection of the device aspect ratios, this circuit can be made to operate under a supply voltage of $V_{DD} = 1V$.

5.3.1 Results

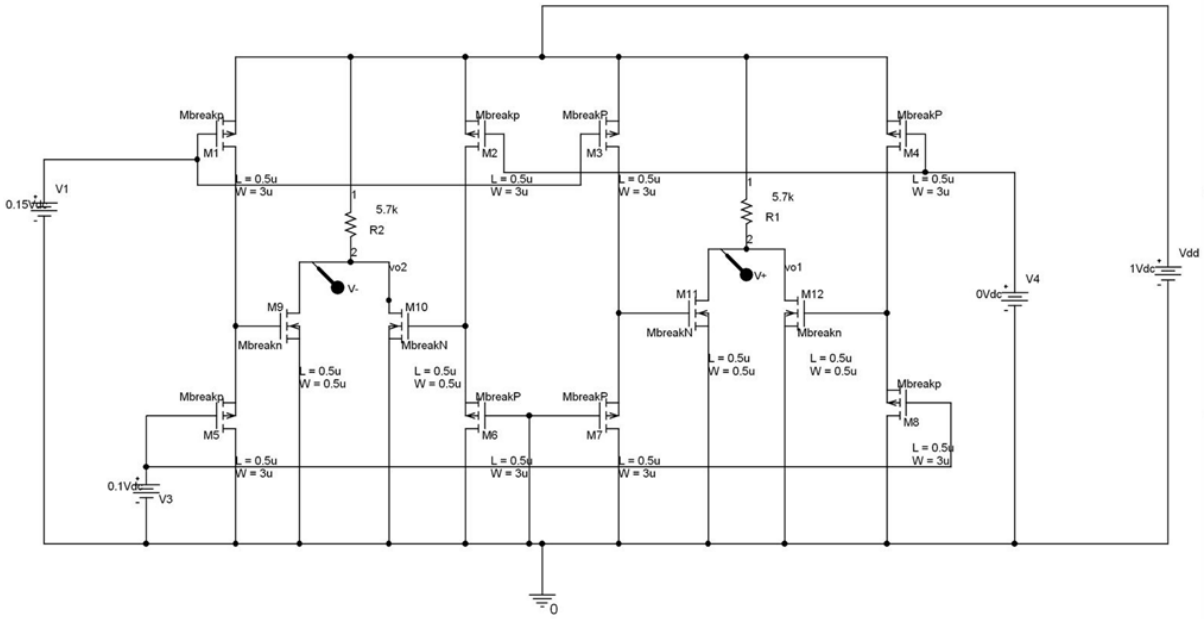

Fig.5.11 PSpice Schematic of four quadrant analog multiplier circuit

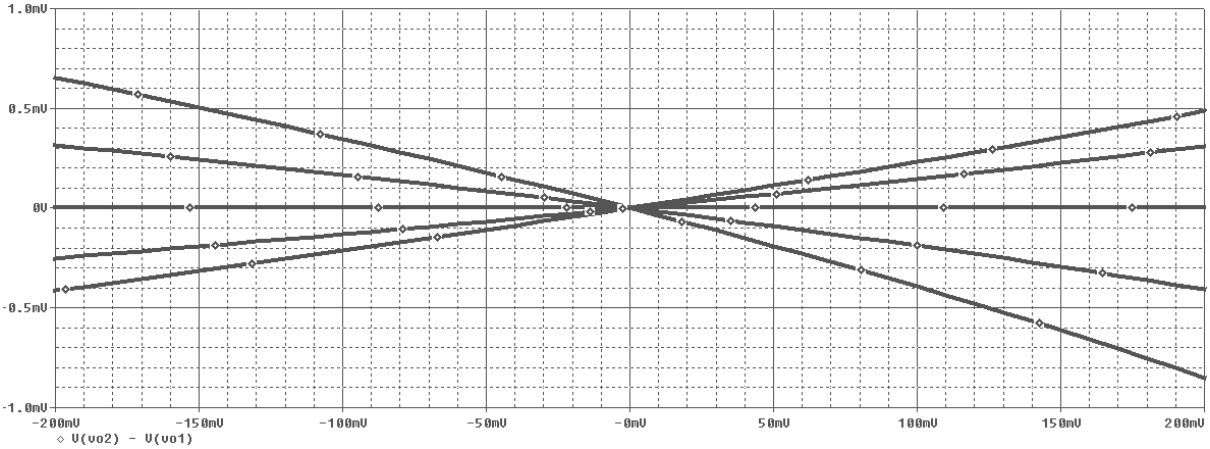

Fig.5.12 Output waveform for V_1 primary and V_2 secondary sweep

5.4 FREQUENCY MULTIPLIER CIRCUIT REALIZATION USING CMOS

A frequency multiplier is an electronic circuit that generates an output signal whose output frequency is a harmonic (multiple) of its input frequency. Frequency multipliers consist of a nonlinear circuit that distorts the input signal and consequently generates harmonics of the input signal. A subsequent filter (bandpass, lowpass or highpass) selects the desired harmonic frequency and removes the unwanted fundamental and other harmonics from the output.

Frequency multipliers are used in frequency synthesizers and communications circuits. It can be more economical to develop a lower frequency signal with lower power and less expensive devices, and then use a frequency multiplier chain to generate an output frequency in the microwave or millimeter wave range. Some modulation schemes, such as frequency modulation, survive the nonlinear distortion without ill effect (but schemes such as amplitude modulation do not).

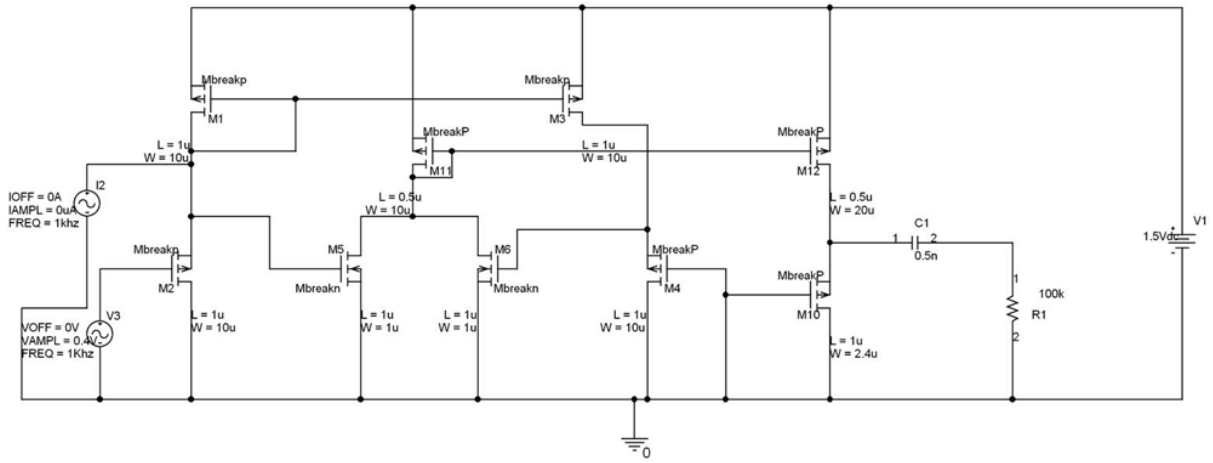

Fig.5.13 PSpice Schematic frequency multiplier circuit using squarer

5.4.1 Results

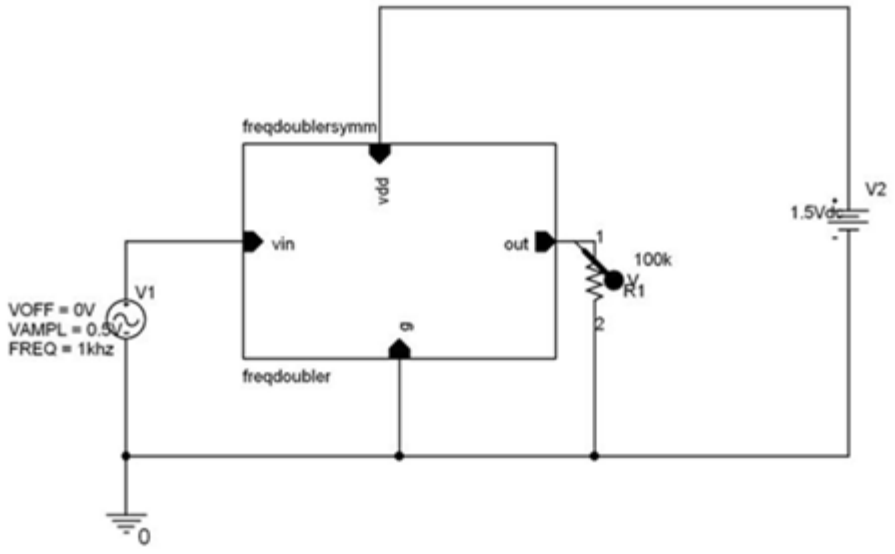

Fig.5.14 PSpice Schematic of requency doubler circuit using squarer

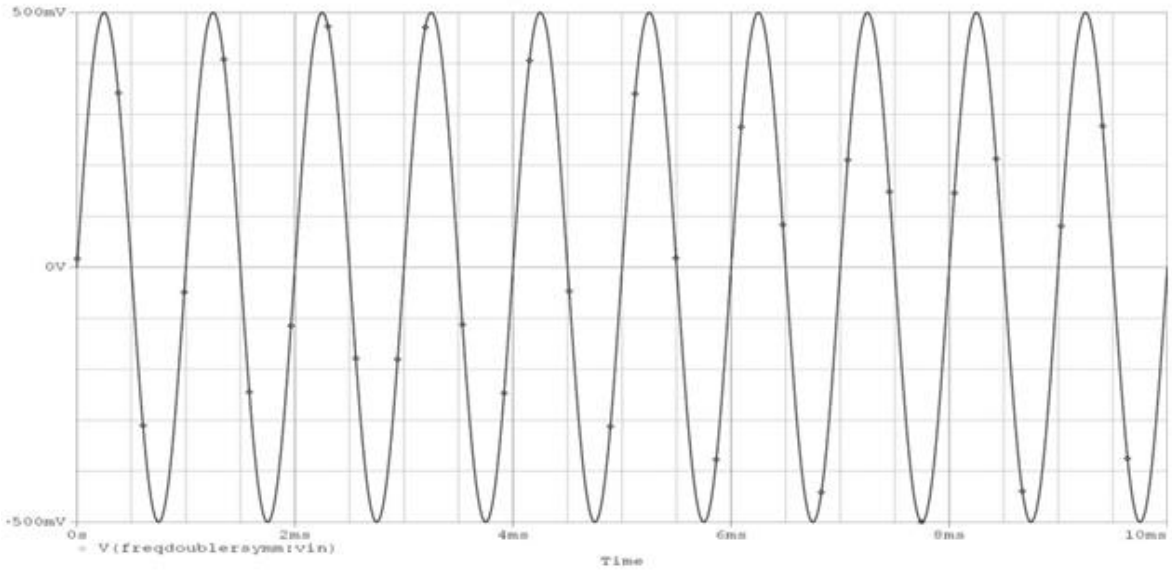

Fig.5.15 Input waveform of frequency doubler circuit

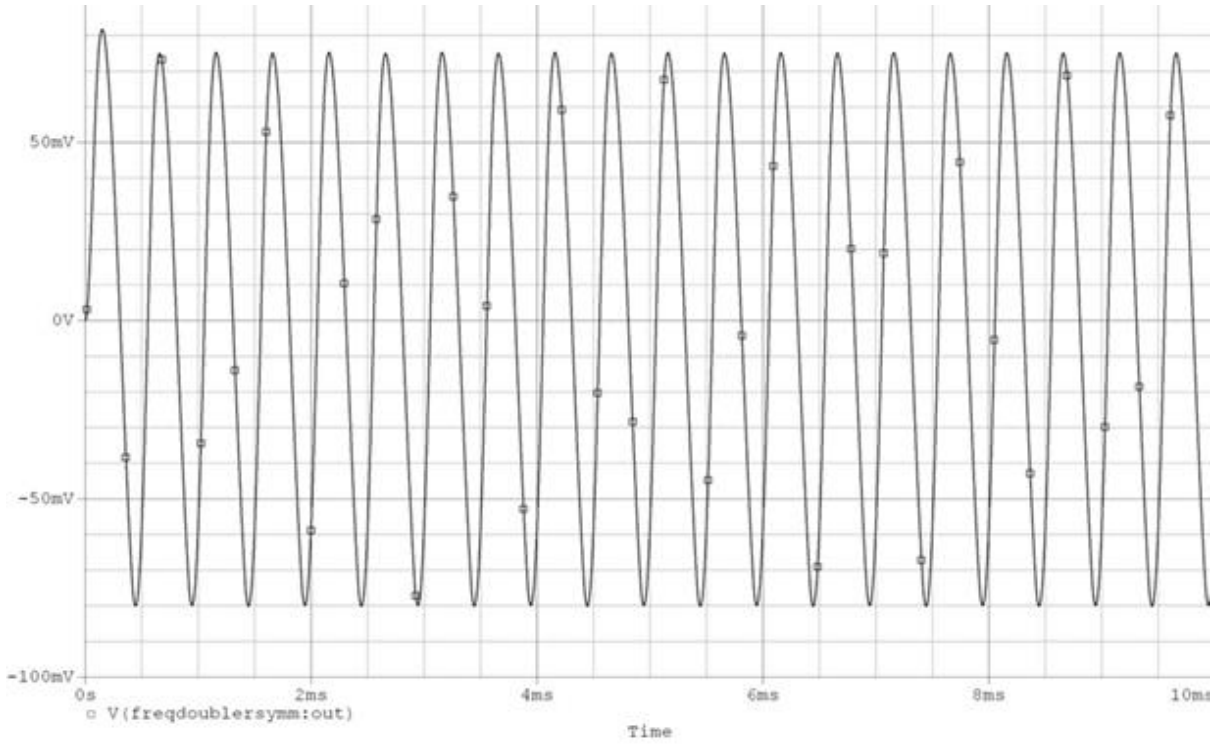

Fig.5.16 Output waveform of frequency doubler circuit

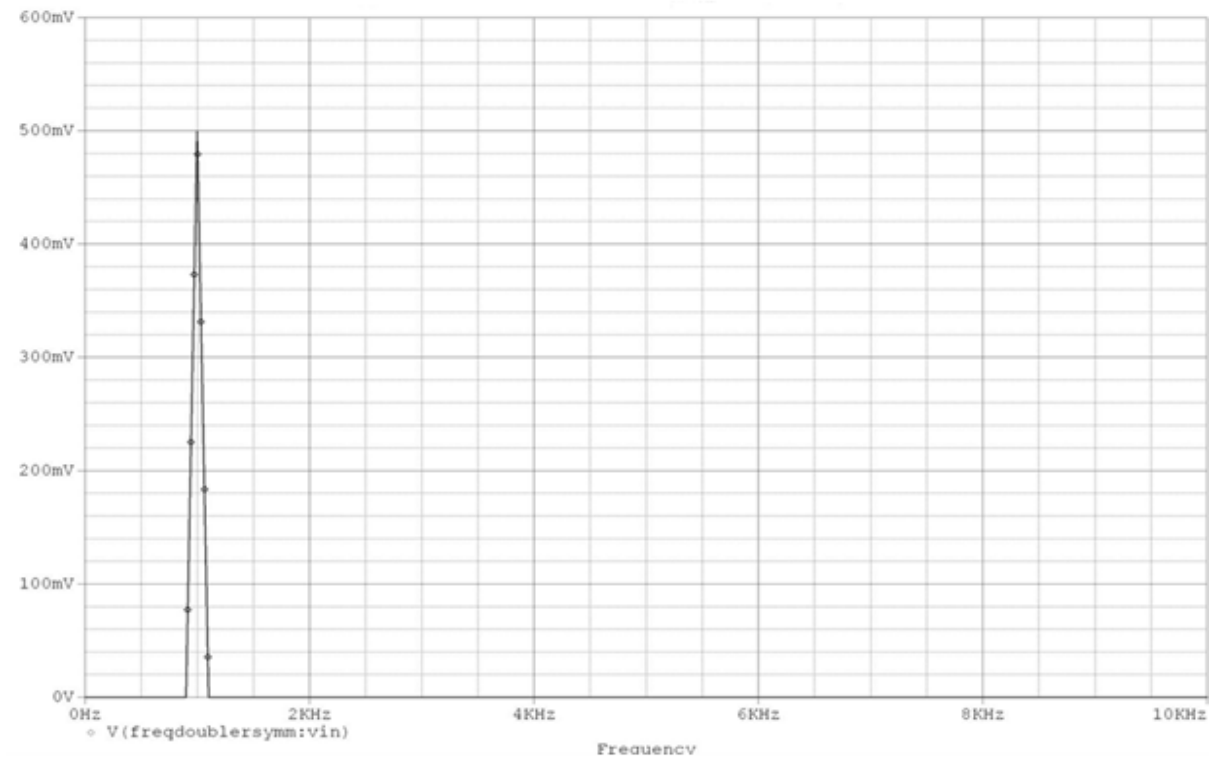

Fig.5.17 FFT of input waveform of frequency doubler circuit

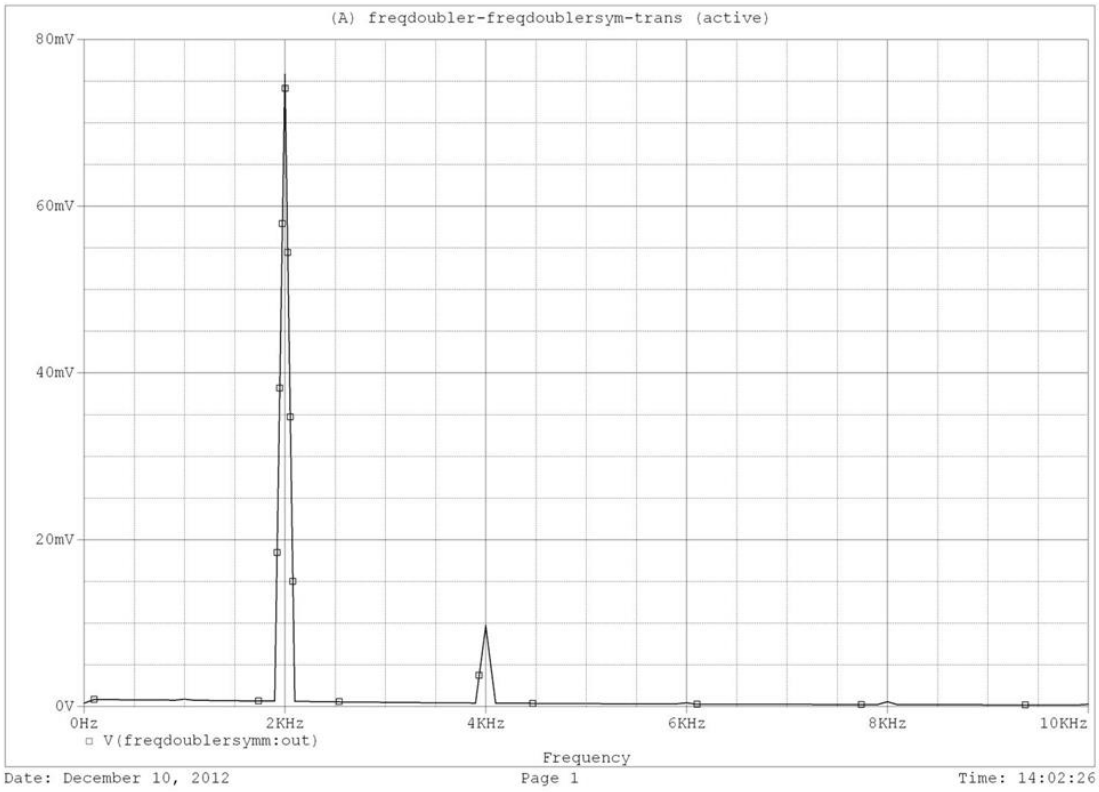

Fig.5.18 FFT of output waveform of frequency doubler circuit

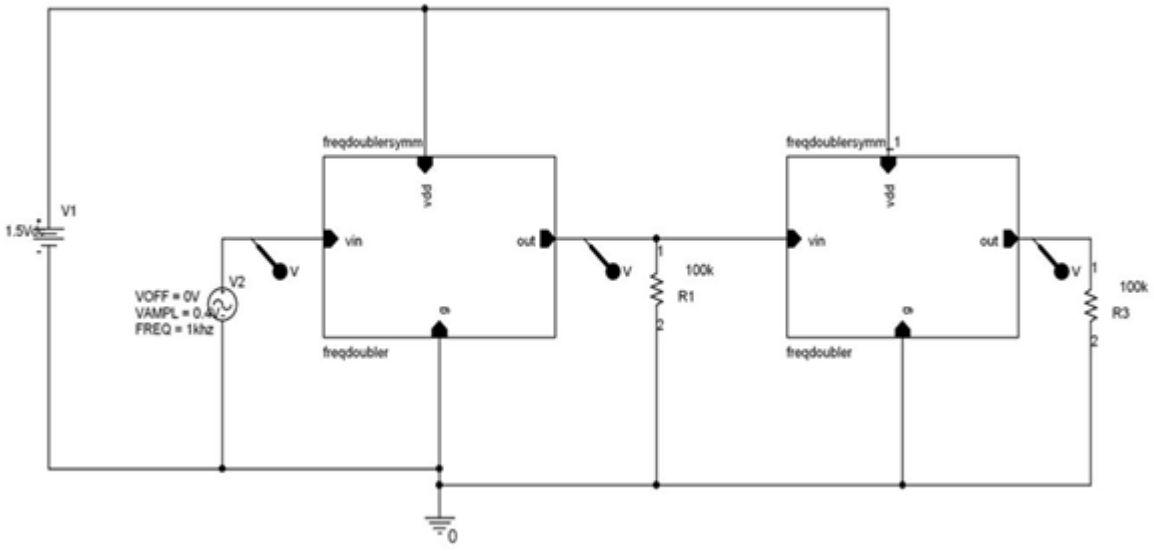

Fig.5.19 PSpice Schematic of frequency quadrupler circuit using squarer

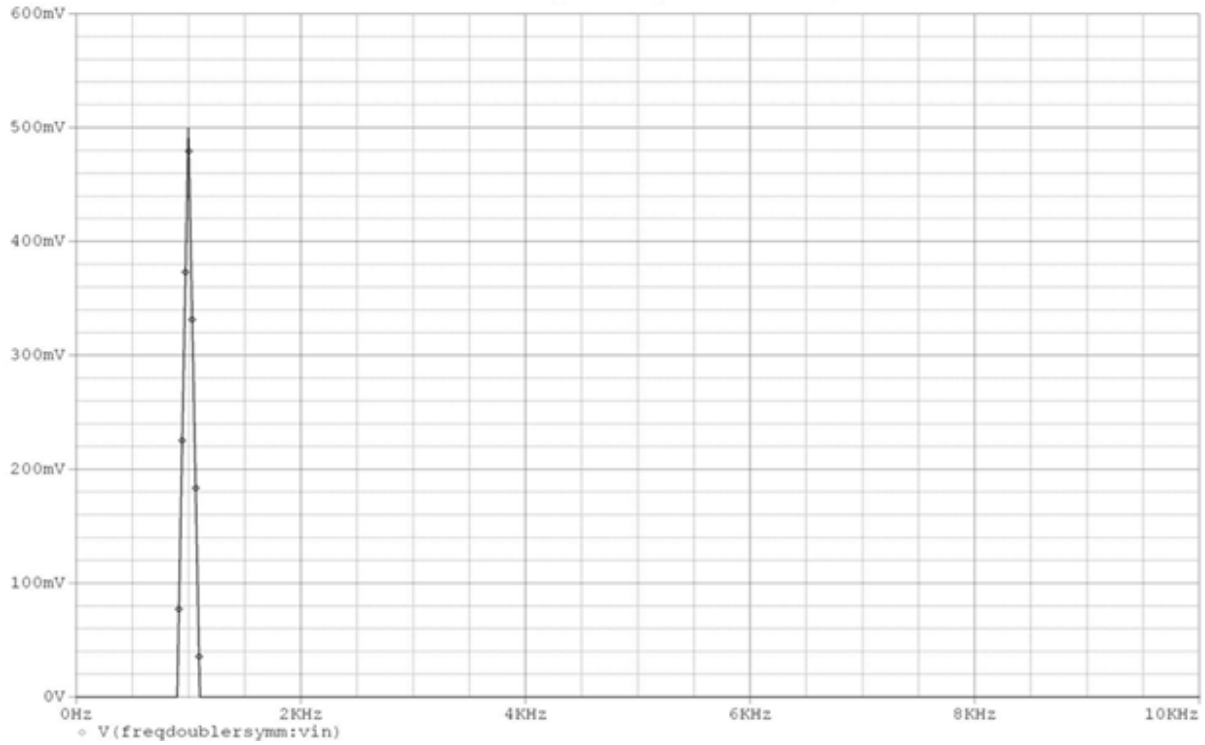

Fig.5.20 FFT of input waveform of frequency quadrupler circuit

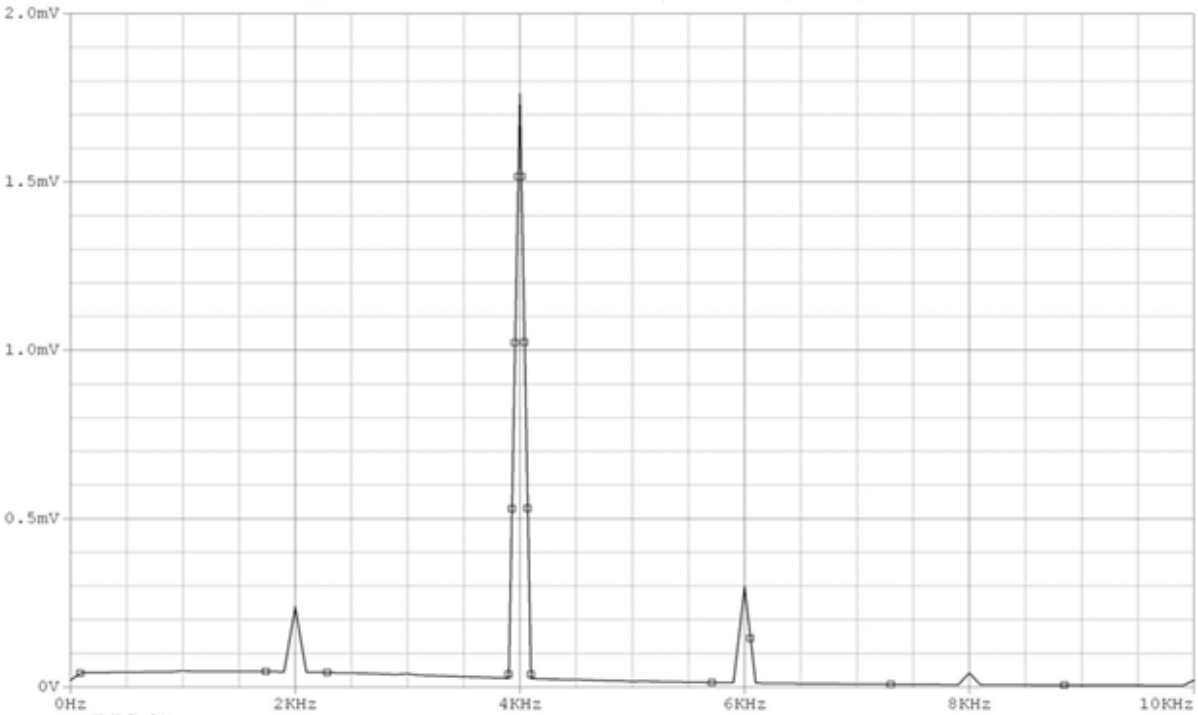

Fig.5.21 FFT of output waveform of frequency quadrupler circuit

References

[1]. Filanovsky, I. M., & Baltes, H. P. (1992). Simple CMOS analog square-rooting and squaring circuits. IEEE Transactions on Circuits and Systems, 39, 312–315.

[2]. Chen, C., & Li, Z. (2006). A low-power CMOS analog multiplier. IEEE Transactions on Circuits and Systems II, 53, 100–104.

[3]. Bult, K., & Wallinga, H. (1987). A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation. IEEE Journal of Solid-State Circuits, 22(3), 357–365.

[4]. Ravindran, A., Ramarao, K., Vidal, E., & Ismail, M. (2001).Compact low voltage four quadrant CMOS current multiplier.Electronics Letters, 37, 1428.

[5]. Naderi, A., Khoei, A., Hadidi, K., & Ghasemzadeh, H. (2009). A new high speed and low power four-quadrant CMOS analog multiplier in current mode. AEU International Journal of Electronics and Communications, 63, 769–775.

[6]. Piangprantong, S., Sakul, C., Dejhan, K., & Chaisayun, I. (2006).A Versatile OTA Analog Multiplier. In Proceeding of international technical conference on circuits/systems, computers and communications (ITC-CSCC) (pp. 513–516).

[7]. Piangprantong, S., & Hlungnamtip, S. (2007). A versatile analog multiplier using CCCIIs. In Proceeding of the 31st electrical engineering conference (EECON-31) (pp. 513–516). Thailand.

[8]. Chaisayun, I., & Dejhan, K. (2003). A versatile CMOS analog multiplier. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 85A, 1225–1232.

[9]. Chaisayun, I., & Dejhan, K. (2003). Low voltage, versatile CMOS analog multiplier. International Journal of Electronics,90, 635–644.

[10]. Chaisayun, I., & Piangprantong, S. (2010). A 1.5 V four-quadrant analog multiplier with two functions of output. In Proceeding of international technical conference on circuits/systems, computers and communications (ITC-CSCC) (pp. 644–647). Thailand.

[11]. Toumazou, C., & Barry, G. (1997). Intuitive analogue circuit design. Electronics & Communication Engineering Journal,231–239.

[12]. Chutham Sawaigun, Dipankar Pal(2007). A low voltage, low power, high linearity CMOS four-quadrant analog multiplier. IEEE 2007.

[13]. Lee, J., & Kim, Y.-B. (2006). A low power CMOS analog circuit design automation. Integration, the VLSI journal, 39, 157–181.

[14]. Tsividis, Y. P. (1978). Operation and modeling of the MOS transistor. New York: Mc Graw-hill.

[15]. Wong, S., & Salama, C. A. (1983). Impact of scaling on MOS analog performance. IEEE Journal of Solid-State Circuits, 18,106–114.

[16]. Razavi, B. (2000). Design of analog CMOS integrated circuits. New York: McGraw Hill.

[17]. Sedra, A. S., & Smith, K. C. (1991). Microelectronic circuits.Philadelphia: Saunders College Publishing.

CHAPTER 6

REALIZATION OF NON-LINEAR CIRCUITS USING OTRA

Recently, current-mode analog integrated circuits in CMOS technology have received considerable interest. Current-mode techniques can achieve a considerable improvement in amplifier speed, accuracy and bandwidth, overcoming the finite gain–bandwidth product associated with operational amplifiers (op amps) [1].

Non-linear circuits have a wide range of application in telecommunications, control systems, signal processing & measurement systems. A number of non-linear circuits using the CMOS as the active devices are available in the chapter 5. Several non-linear circuits have been introduced using output transconductance amplifier(OTA), the current conveyor as the active element [3] or the current feedback operational amplifier [2]. In this chapter non-linear circuits available in the literature [4,5] are discussed and simulated using OTRA.

6.1 ANALOG MULTIPLIER USING OTRA

6.1.1 Introduction

Analog multipliers find extensive application in the field of telecommunication, control, instrumentation, measurement, and signal processing [6]. A number of circuits are reported in literature relating to analog multipliers [7–10]. Circuits presented in [7–9] are based on Gilbert multiplier [11] and are suitable for CMOS integrated technology. Recently the OTRA has emerged as an alternate analog building block [1–4] which inherits all the advantages of current mode techniques. The OTRA is a high gain current input voltage output device. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances at the input. Several non-linear circuits use single active element such as classical voltage op-amp, current conveyor, current feedback amplifier or a four terminal floating nullor. A novel operational transresistance amplifier based analog multiplier with CMOS devices is presented here. It uses single OTRA, and few CMOS devices. The multiplier circuit provides its output as the multiplication of its two inputs.

6.1.2 Circuit description

6.1.2.1 Basic multiplier: The circuit of OTRA based basic multiplier is shown in fig.6.1.

Figure 6.1 Shows OTRA based multiplier structure. The transistors M1, M2 M3, and M4 are matched transistors and operate in the linear region. v_1 and v_2 represent small signals, whereas V_{c1}, V_{c2}, and V_{DC} are the bias voltages. OTRA inputs keep the sources of the two transistorsM1 andM2 virtually grounded. The drain current for the MOS transistor operating in triode region is given by [12].

$$I_D = k\frac{W}{L}\left((V_{GS} - V_T) - \frac{V_{DS}}{2}\right)V_{DS} \tag{6.1}$$

where k is transconductance;W and L respectively represent the channel width and length of the of the MOSFET. The other terms have their usual meaning.

Using (6.1) the currents through p and n terminals of OTRA, that is, i_p and i_n respectively, can be expressed as

$$i_p = K_n\frac{W}{L}\left(((V_{DC} + v_1) - V_T) - \frac{v_2}{2}\right)v_2 + K_n\frac{W}{L}\left(V_{C1} - V_T\right) - \frac{v_o}{2}\Big)v_o \tag{6.2a}$$

$$i_n = K_n\frac{W}{L}\left(V_{DC} - V_T\right) - \frac{v_2}{2}\Big)v_2 + K_n\frac{W}{L}\left(V_{C2} - V_T\right) - \frac{v_o}{2}\Big)v_o$$

(6.2b)

As R_m approaches infinity the input currents are forced to be equal resulting in

$$v_o = \frac{v_1 v_2}{(V_{C2} - V_{C1})} = K v_1 v_2 \tag{6.3}$$

where K is a proportionality constant and is the inverse differences of gate voltage of M_3 and M_4.

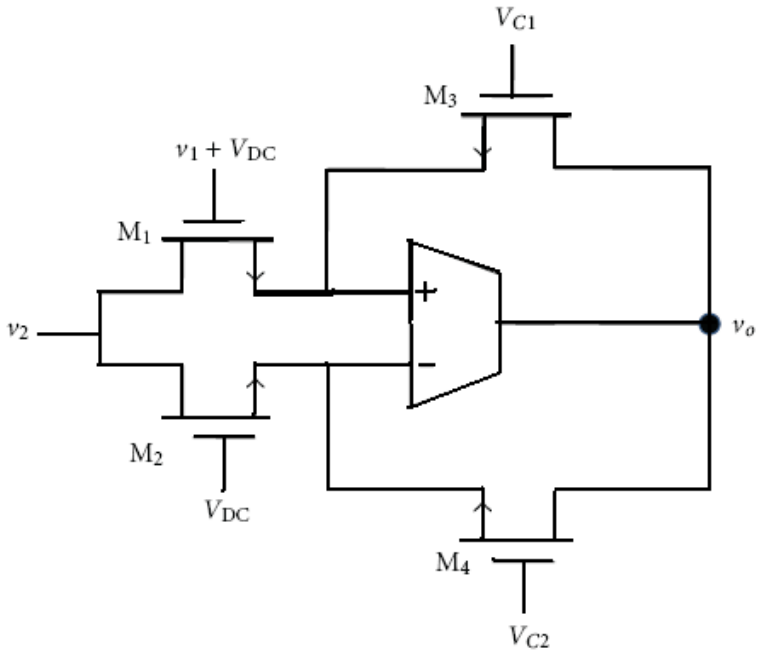

Fig. 6.1 Basic OTRA multiplier

6.1.2.2 Simulation results

The OTRA multiplier results is shown using OTRA block third in chapter 4. The PSPICE schematic of the multiplier is shown in fig 6.2.

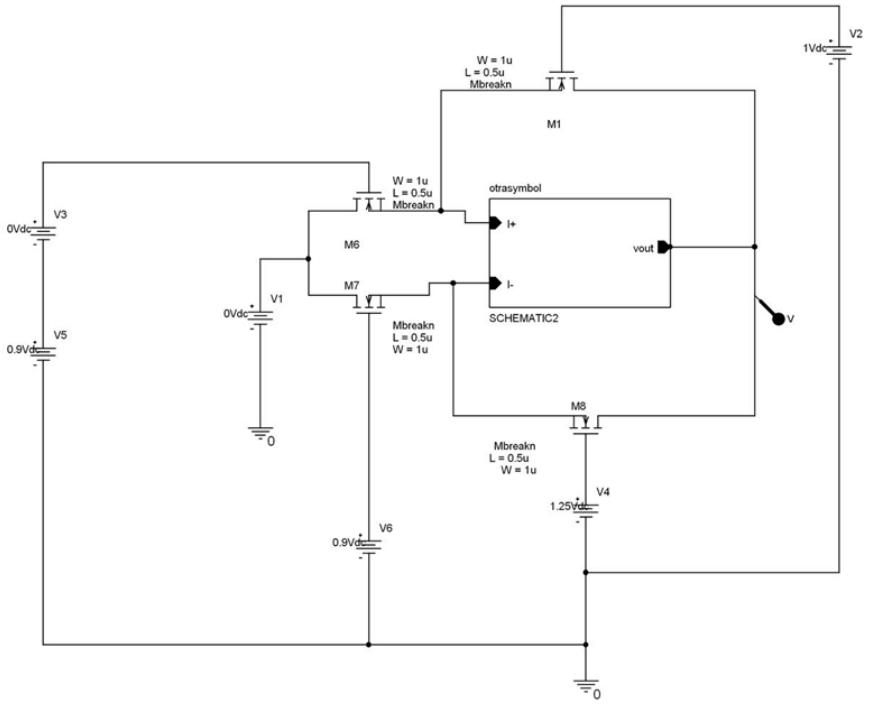

Fig. 6.2 PSpice schematic of basic multiplier circuit using OTRA block 3

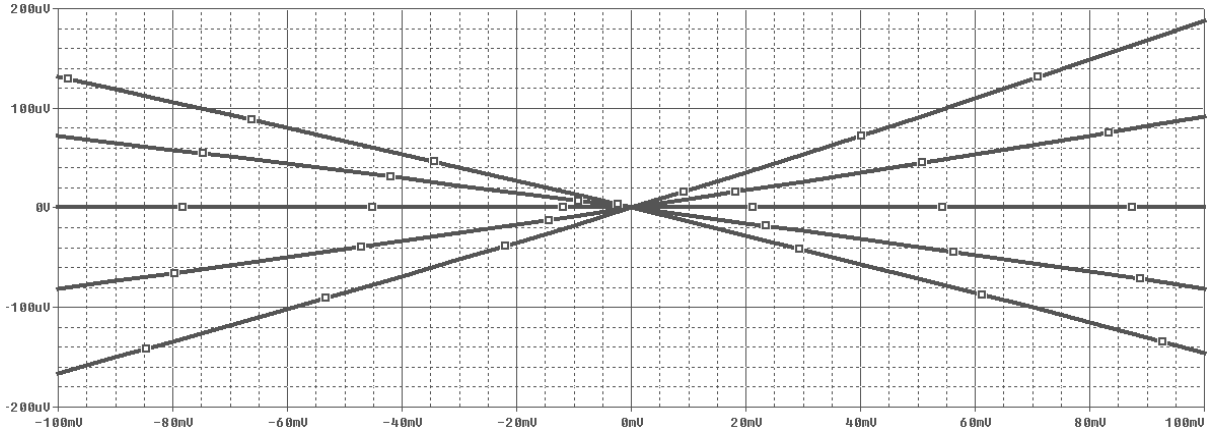

Fig.6.3 DC characteristic of multiplier using OTRA block 3

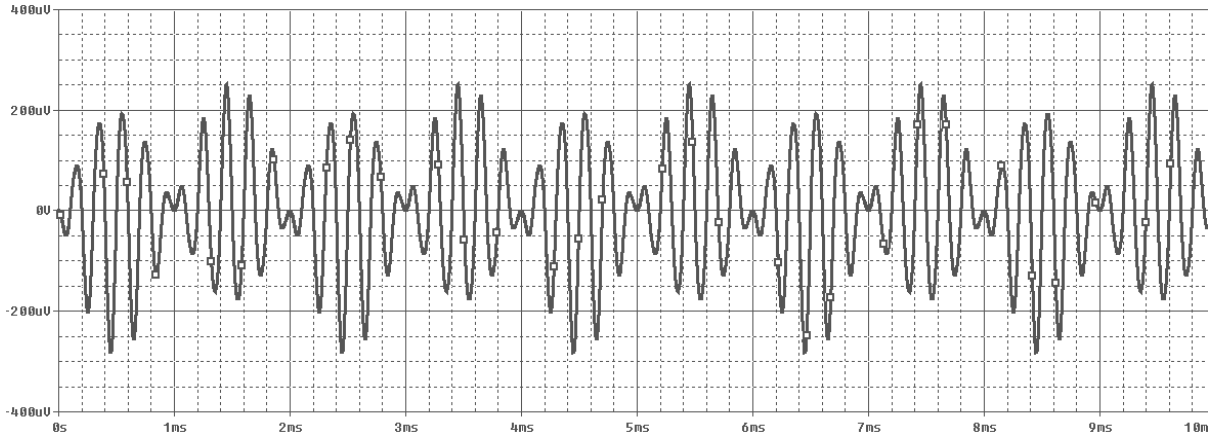

Fig.6.4 DSB SC modulated waveform using OTRA block 3

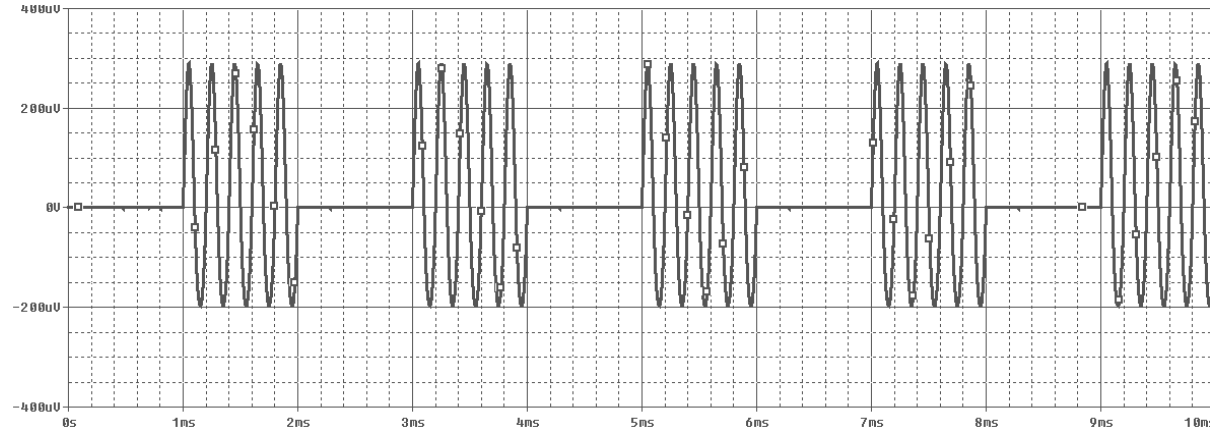

Fig.6.5 ASK modulated waveform using OTRA block 3

6.1.2.3 Simulation results

The OTRA multiplier results is shown using OTRA block four in chapter 4. The PSPICE schematic of the multiplier is shown in fig 6.6.

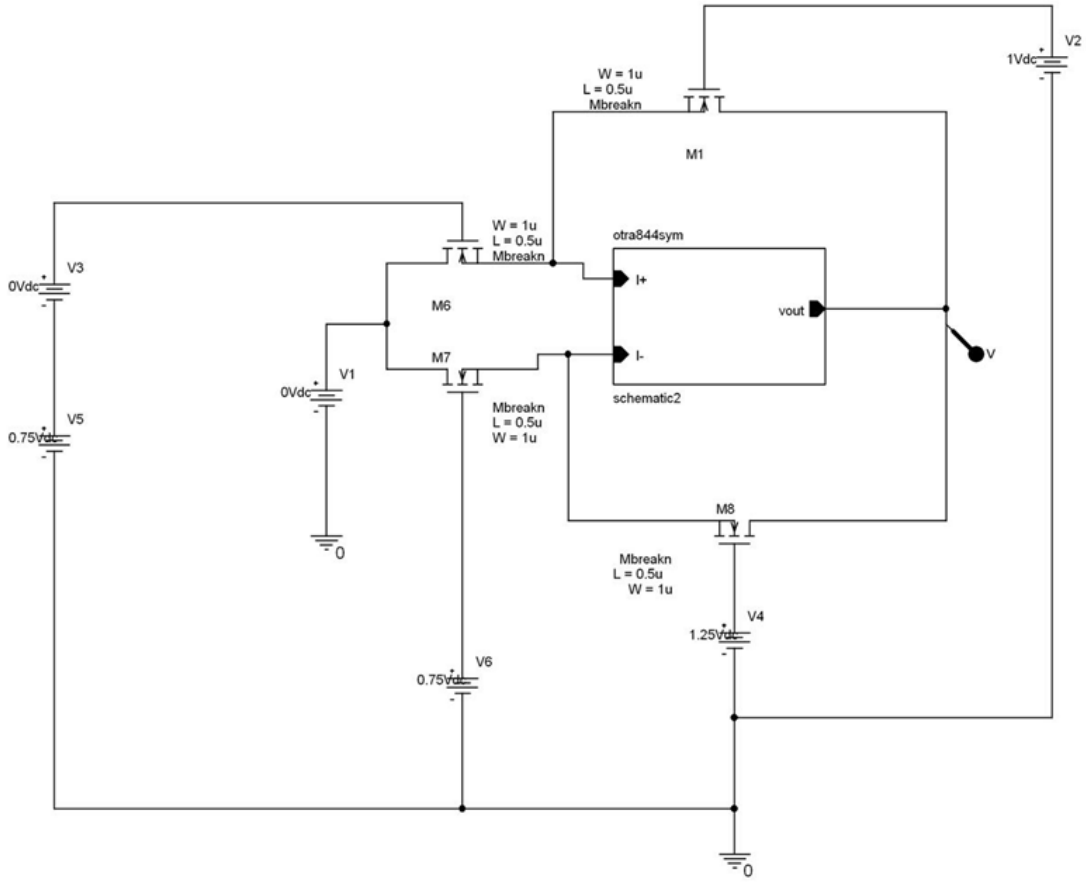

Fig. 6.6 PSpice schematic of basic multiplier circuit using OTRA block 4

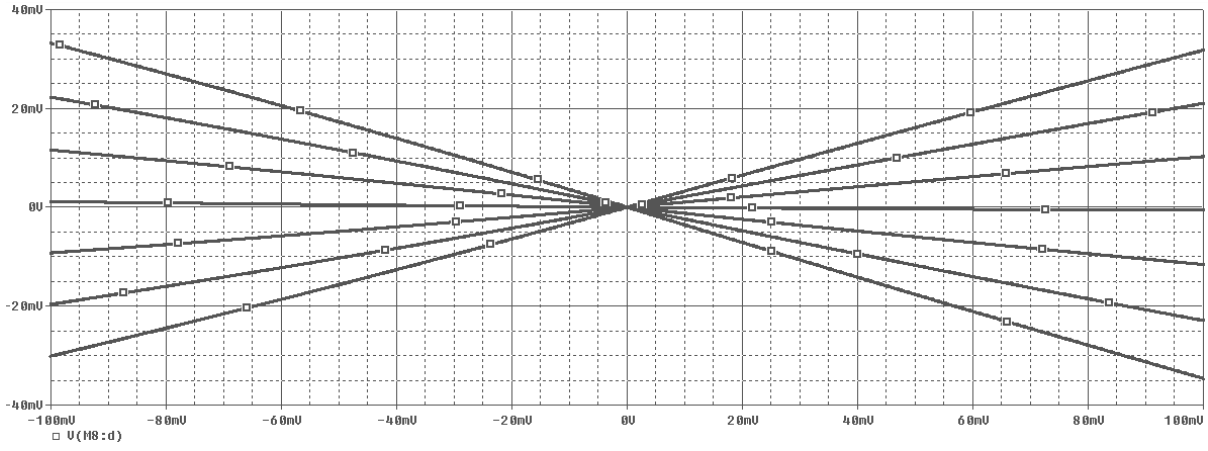

Fig.6.7 DC characteristic of multiplier using OTRA block 4

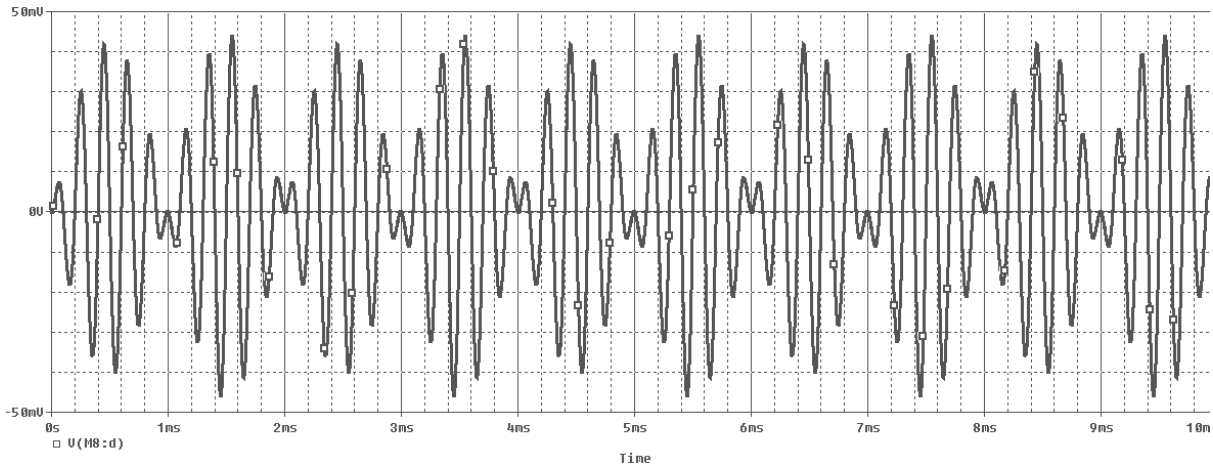

Fig.6.8 DSB SC modulated waveform using OTRA block 4

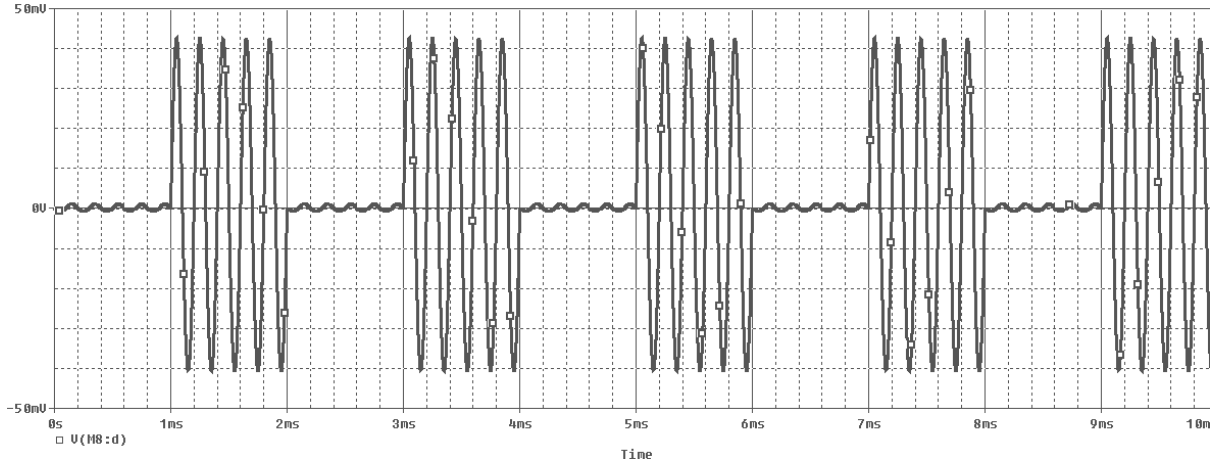

Fig.6.9 ASK modulated waveform using OTRA block 4

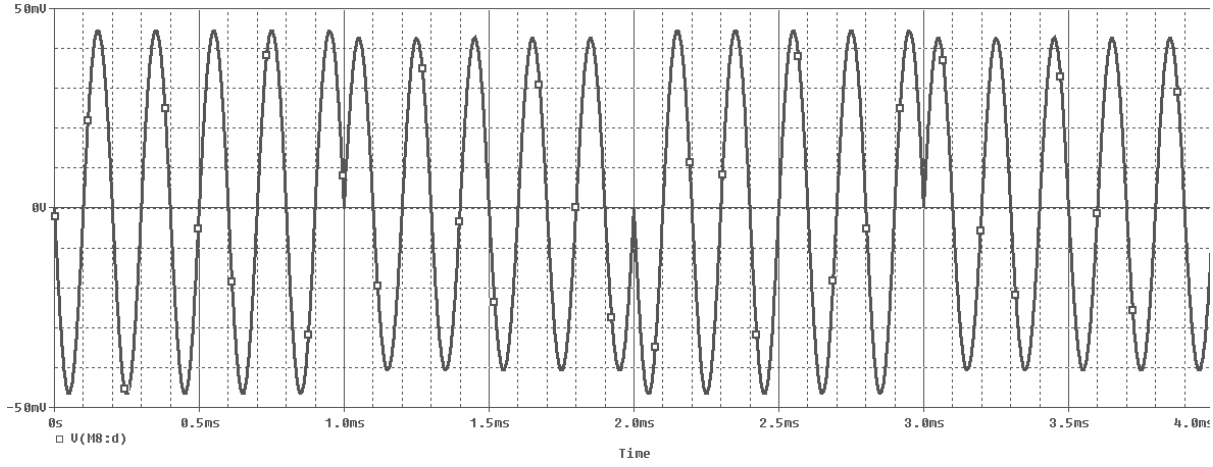

Fig.6.10 PSK modulated waveform using OTRA block 4

6.1.3 Circuit description

6.1.3.1 : The complete MOS based multiplier structure is depicted in fig. 6.11.

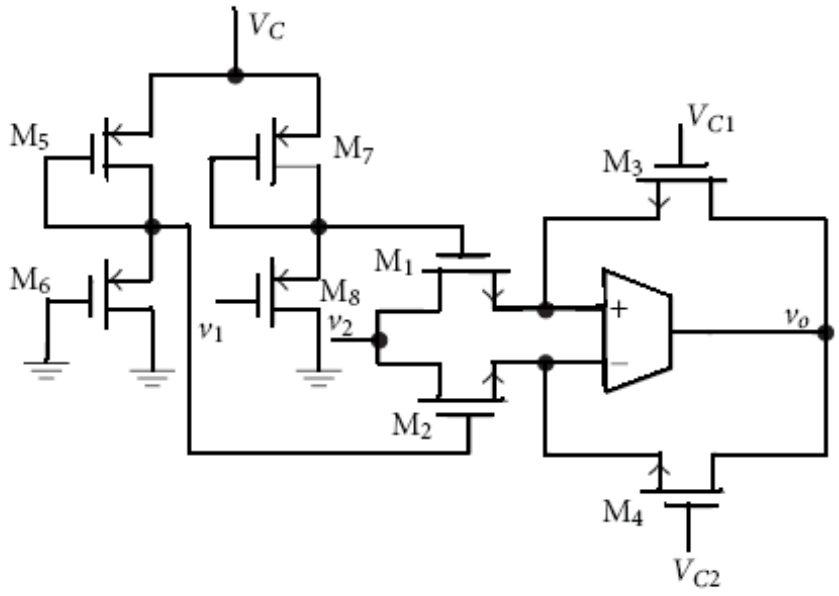

Fig. 6.11 Complete OTRA multiplier

6.1.3.2 Simulation results : The OTRA multiplier results is shown using OTRA block third in chapter 4. The PSPICE schematic of the multiplier is shown in fig 6.12.

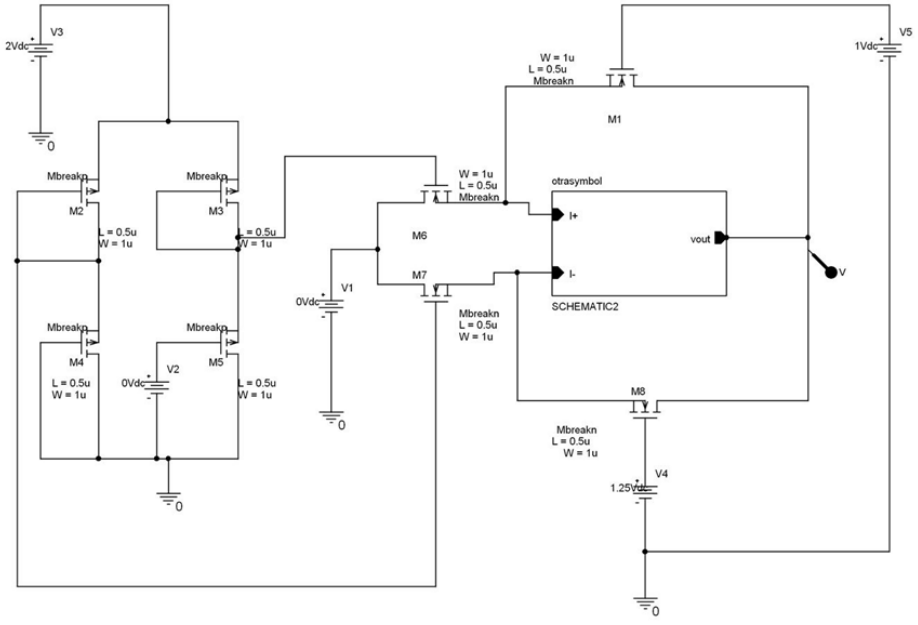

Fig. 6.12 PSpice schematic of complete multiplier circuit using OTRA block 3

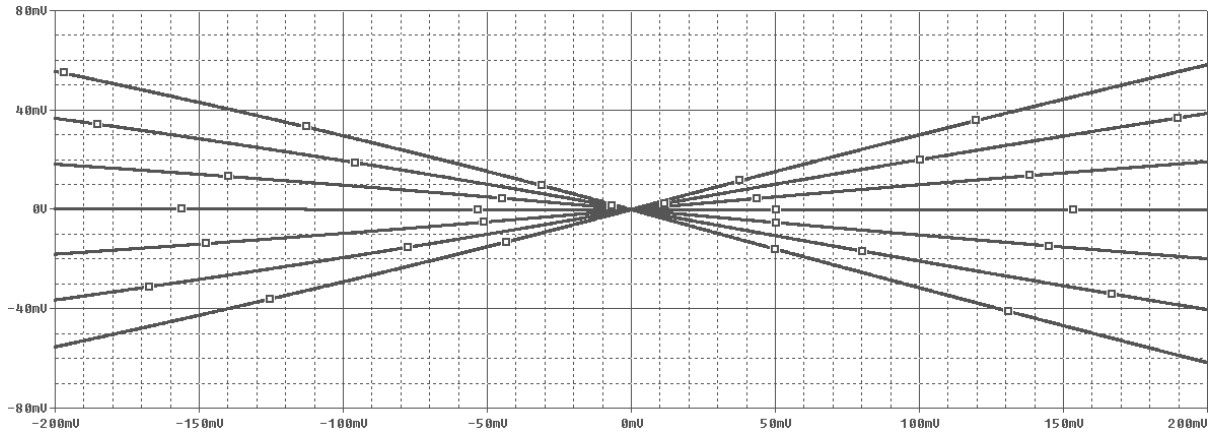

Fig.6.13 DC characteristic of multiplier using OTRA block 3

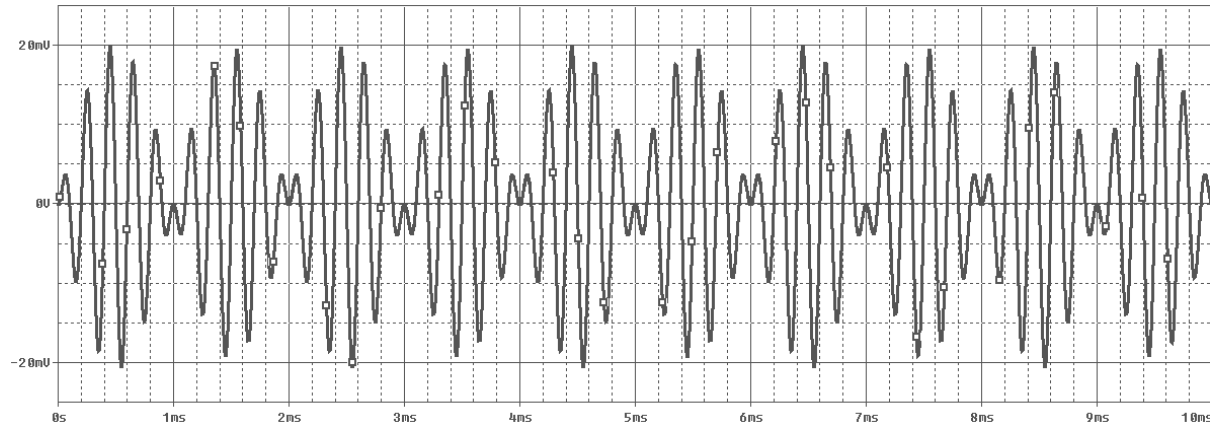

Fig.6.14 DSB SC modulated waveform using OTRA block 3

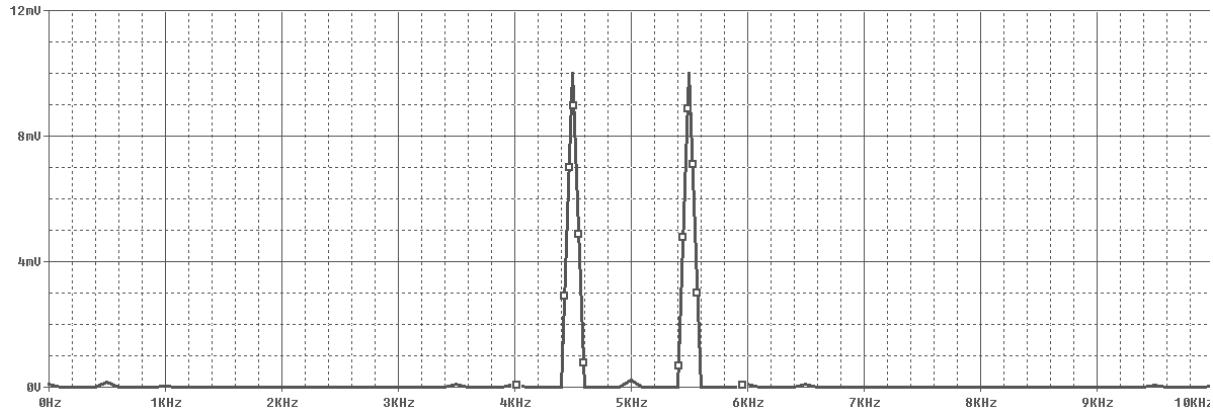

Fig.6.15 DSB SC modulated FFT waveform using OTRA block 3

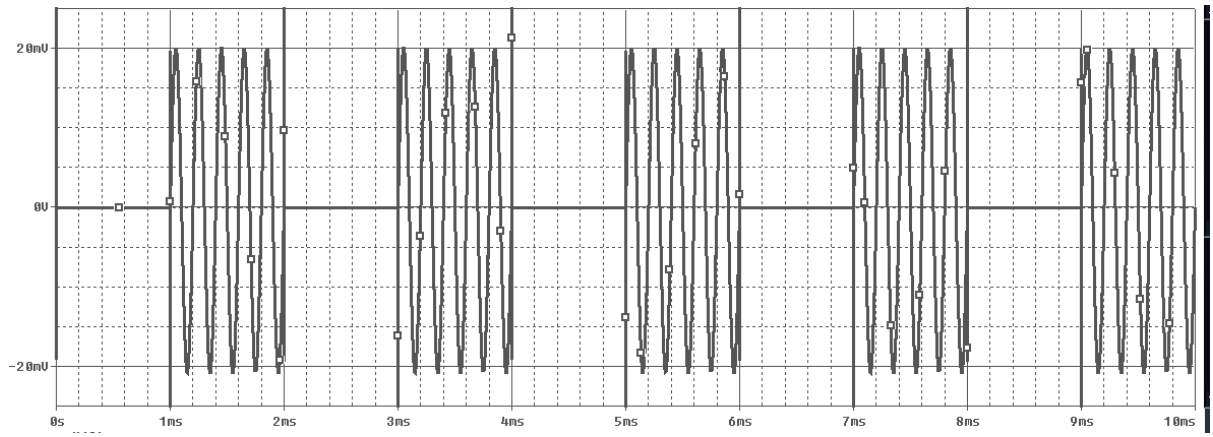

Fig.6.16 ASK modulated waveform using OTRA block 3

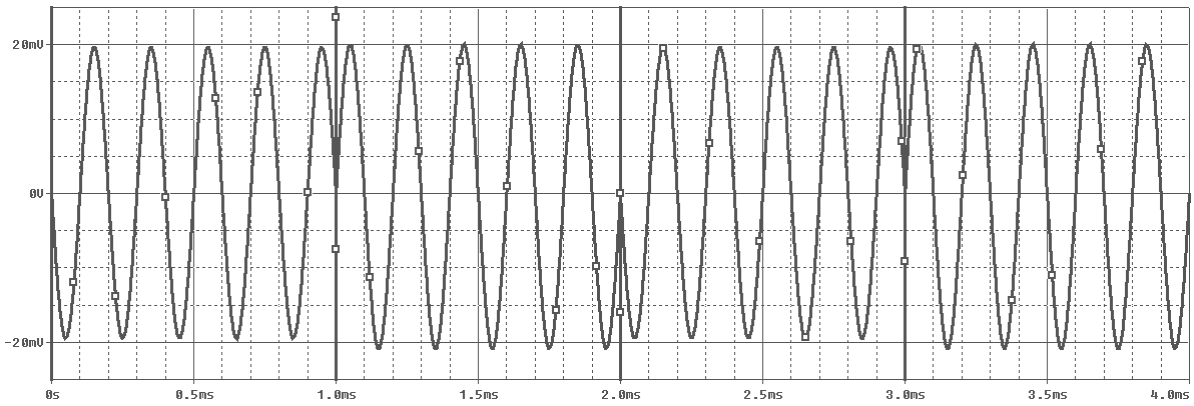

Fig.6.17 PSK modulated waveform using OTRA block 3

6.1.3.3 Simulation results : The OTRA multiplier results is shown using OTRA block four in chapter 4. The PSPICE schematic of the multiplier is shown in fig 6.18.

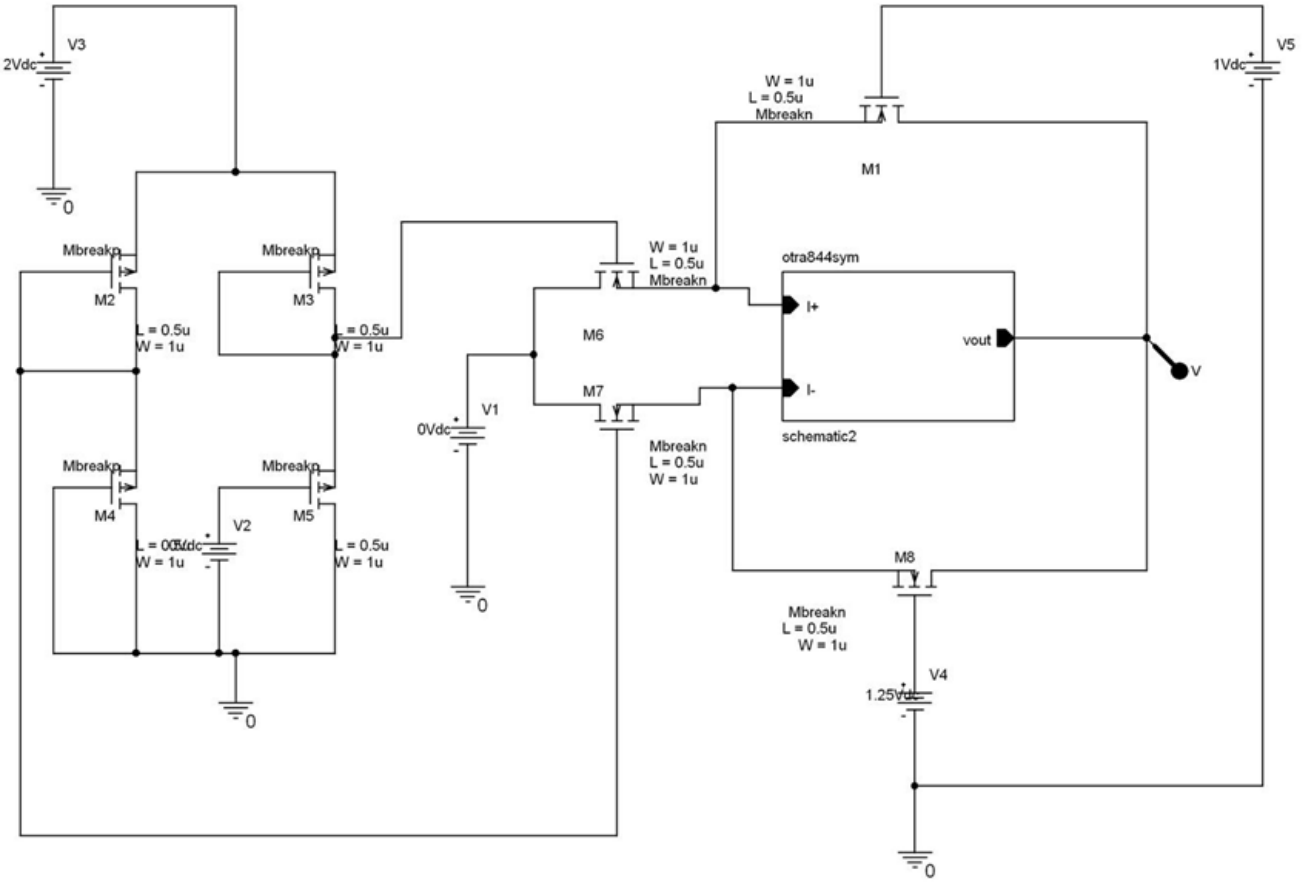

Fig. 6.18. PSpice schematic of complete multiplier circuit using OTRA block 4

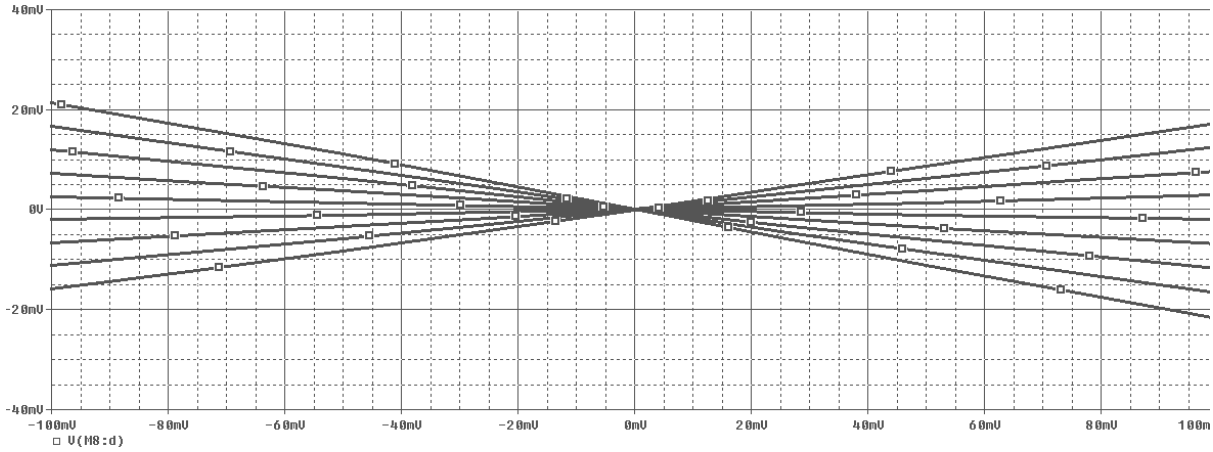

Fig.6.19 DC characteristic of multiplier using OTRA block 4

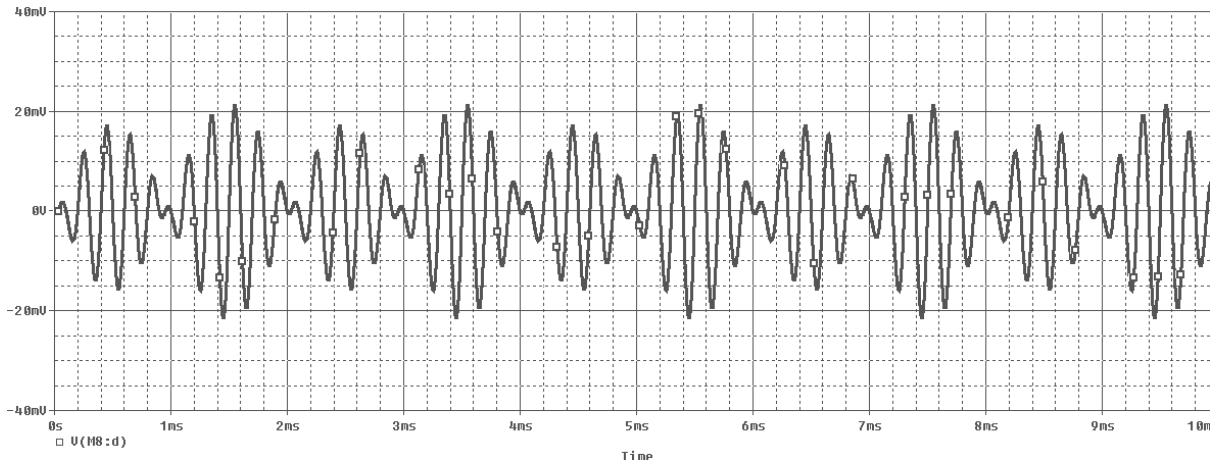

Fig.6.20 DSB SC modulated waveform using OTRA block 4

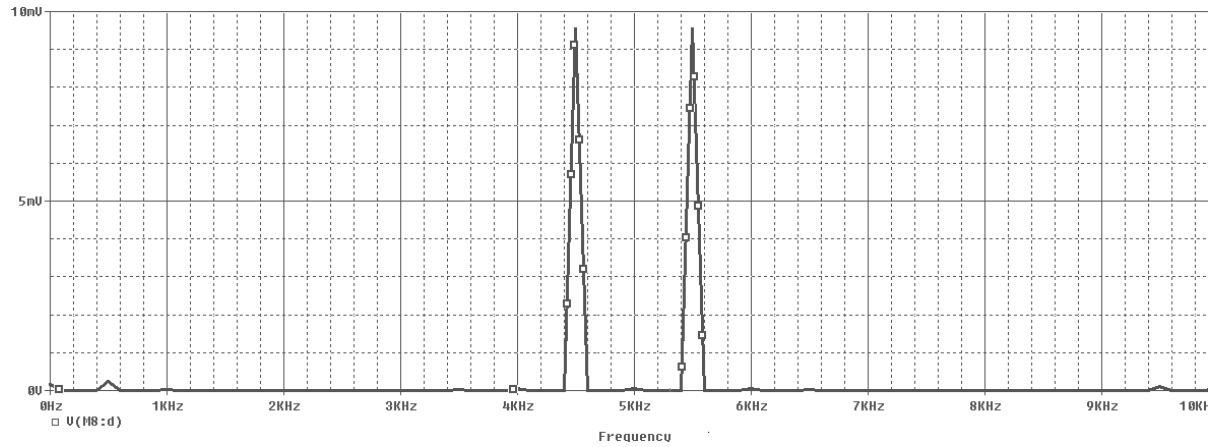

Fig.6.21 DSB SC modulated FFT waveform using OTRA block 4

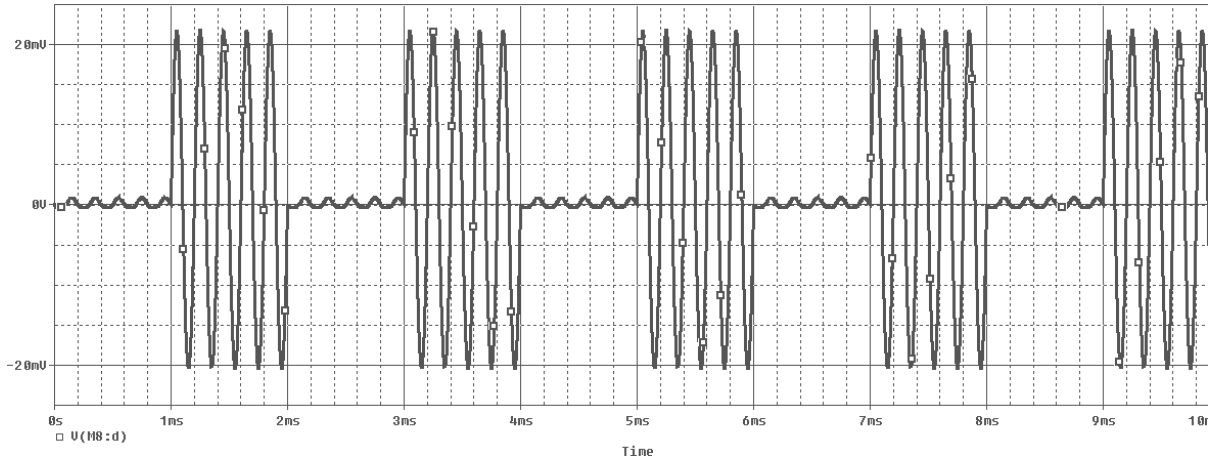

Fig.6.22 ASK modulated waveform using OTRA block 4

6.2 FREQUENCY MIXER USING OTRA

6.2.1 Introduction

A **mixer** or **frequency mixer**[13] is a nonlinear electrical circuit that creates new frequencies from two signals applied to it. In its most common application, two signals at frequencies f_1 and f_2 are applied to a mixer, and it produces new signals at the sum $f_1 + f_2$ and difference $f_1 - f_2$ of the original frequencies. Other frequency components may also be produced in a practical frequency mixer.

Mixers are widely used to shift signals from one frequency range to another, a process known as heterodyning[14], for convenience in transmission or further signal processing. For example, a key component of a superheterodyne receiver is a mixer used to move received signals to a common intermediate frequency. Frequency mixers are also used to modulate a carrier frequency in radio transmitters. The basic principle of frequency mixer is shown in fig. 6.23.

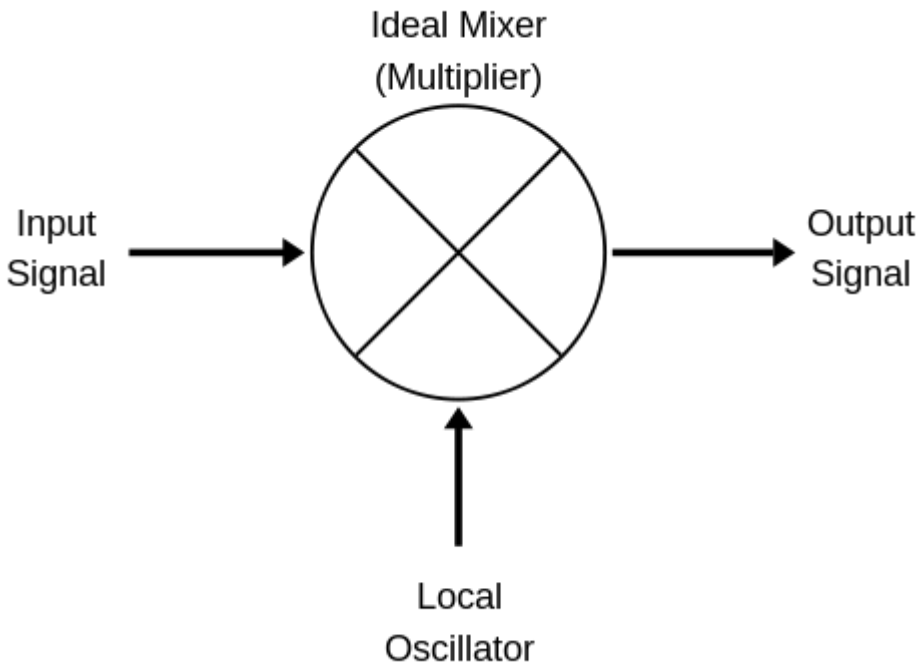

Fig.6.23 frequency mixer basic block

A device that has a non-linear (square law) characteristic can act as a mixer. Passive mixers use one or more diodes and rely on the non-linear relation between voltage

and current to provide the multiplying element. In a passive mixer, the desired output signal is always of lower power than the input signals.

Active mixers use an amplifying device (such as a transistor or vacuum tube) to increase the strength of the product signal. Active mixers improve isolation between the ports, but may have higher noise and more power consumption. An active mixer can be less tolerant of overload. A double balanced mixer has symmetrical paths for both inputs, so that neither input signal appears at the output, only the product (IF) signal. In this section a frequency mixer is implemented using OTRA multiplier and OTRA band pass filter.

6.2.2 Circuit description

6.2.2.1 The circuit of OTRA based frequency multiplier is shown in fig.6.24

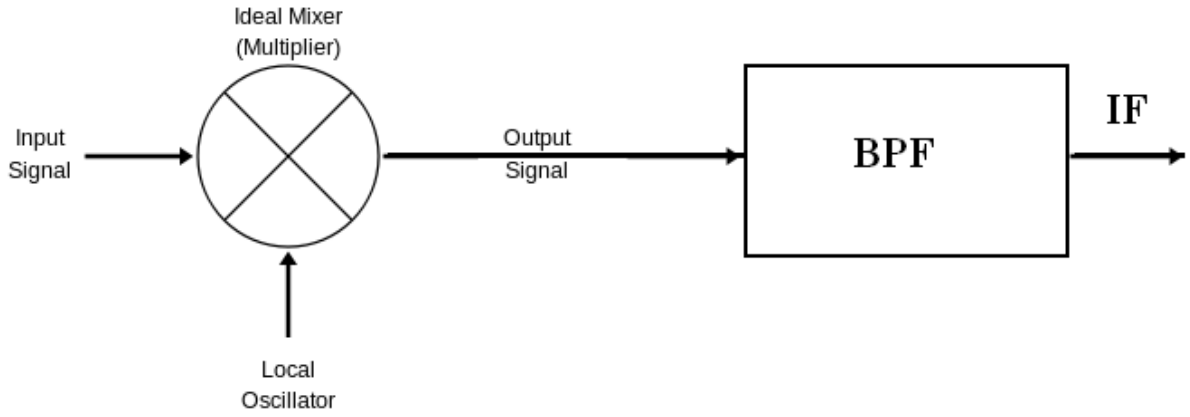

Fig.6.24 frequency mixer circuit with up conversion IF output

If two signals of different frequency are fed through a linear device, they will appear at the device output as the same two frequencies. To mix two signals we require a curved or non-linear characteristic. With non-linear circuits intrermodulation product occurs and by using appropriate band pass filter, the required IF frequency is passed by BPF. Fig 6.25. shows the PSpice implementation of mixer circuit in which both multiplier and BPF are implemented by OTRA. Multiplier has two inputs of different frequencies f_1 and f_2 and gives output as a modulated signal having sum and difference frequencies i.e. f_1+f_2 and $f_1- f_2$.

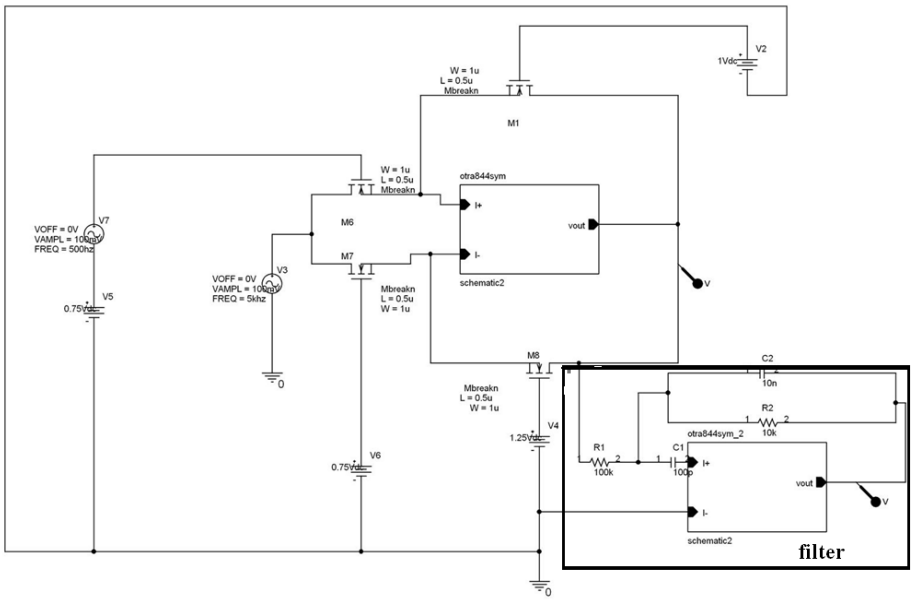

Fig.6.25 PSpice schematic of frequency mixer using OTRA

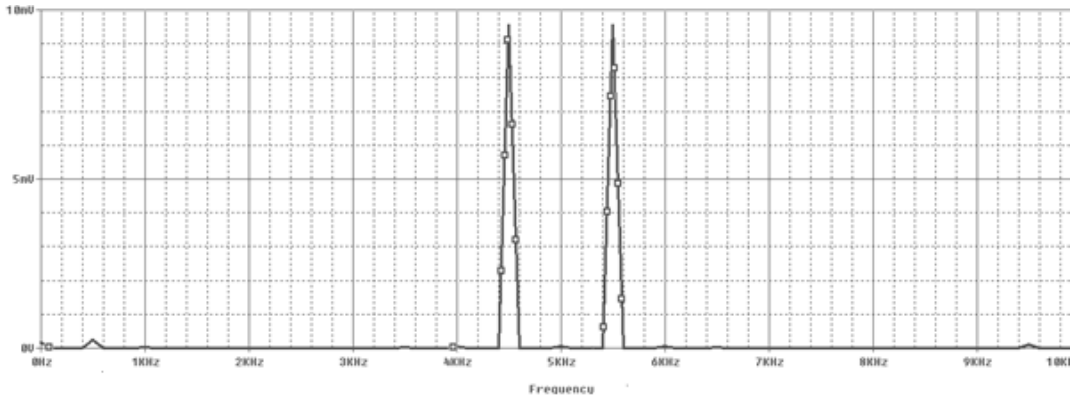

Fig.6.26 Waveform LSB and USB with f_1=5khz and f_2=500hz

Any one of these bands can be filtered out using appropriate BPF as shown in Fig.6.27

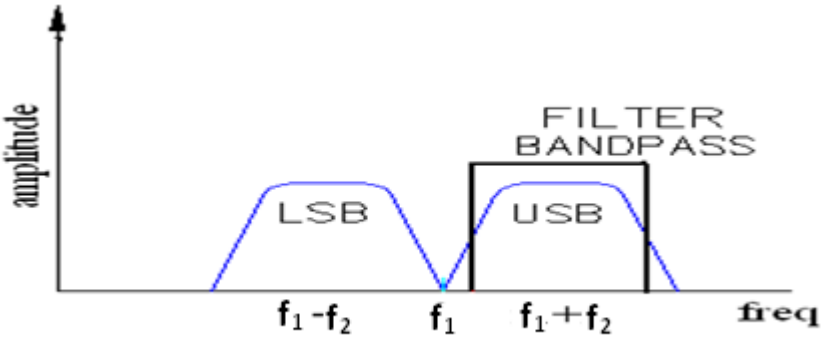

Fig.6.27 USB Band Pass filtered

6.3 RELAXATION OSCILLATOR USING OTRA

6.3.1 Introduction

A **relaxation oscillator**[17] is an oscillator based upon the behavior of a physical system's return to equilibrium after being disturbed. That is, a dynamical system within the oscillator continuously dissipates its internal energy. Normally the system would return to its natural equilibrium; however, each time the system reaches some threshold sufficiently close to its equilibrium, a mechanism disturbs it with additional energy. Hence, the oscillator's behavior is characterized by long periods of dissipation followed by short impulses. The period of the oscillations is set by the time it takes for the system to relax from each disturbed state to the threshold that triggers the next disturbance. Many electronic relaxation oscillators store energy in a capacitor and then dissipate that energy repeatedly to set up the oscillations. The capacitor can be charged toward a positive power supply until it reaches a threshold voltage sufficiently close to the supply. At that instant, the capacitor can be quickly discharged (e.g., shorted). Alternatively, when the capacitor reaches each threshold, the charging source can be switched from the positive power supply to the negative power supply or vice versa. In all such capacitor-based relaxation oscillators[16], the period of the oscillations is set by the dissipation rate(s) of the capacitor. Implementations of the later type of relaxation oscillators is shown here in using single OTRA.

6.3.2 Circuit description

A comparator based relaxation oscillator using voltage amplifier is shown in fig.6.28. This relaxation oscillator is a hysteretic oscillator, named this way because of the hysteresis created by the positive feedback loop implemented with the comparator . A circuit that implements this form of hysteretic switching is known as a Schmitt trigger. Alone, the trigger is a bistable multivibrator. However, the slow negative feedback added to the trigger by the RC circuit causes the circuit to oscillate automatically. That is, the addition of the RC circuit turns the hysteretic bistable multivibrator into an astable multivibrator. The system is in unstable equilibrium if both the inputs and outputs of the comparator are at zero volts. The

moment any sort of noise, be it thermal or electromagnetic noise brings the output of the comparator above zero, the positive feedback in the comparator results in the output of the comparator saturating at the positive rail.

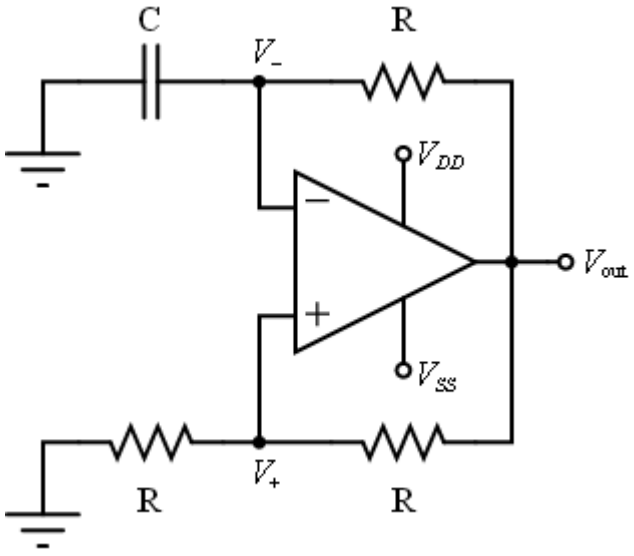

Fig.6.28 comparator based relaxation oscillator

Because the output of the comparator is now positive, the non-inverting input to the comparator is also positive, and continues to increase as the output increases, due to the voltage divider. After a short time, the output of the comparator is the positive voltage rail V_{dd}.

The inverting input and the output of the comparator are linked by a series RC circuit. Because of this, the inverting input of the comparator asymptotically approaches the comparator output voltage with a time constant RC. At the point where voltage at the inverting input is greater than the non-inverting input, the output of the comparator falls quickly due to positive feedback.

This is because the non-inverting input is less than the inverting input, and as the output continues to decrease, the difference between the inputs gets more and more negative. Again, the inverting input approaches the comparator's output voltage asymptotically, and the cycle repeats itself once the non-inverting input is greater than the inverting input, hence the system oscillates.

6.3.3 Simulation results

6.3.3.1 Circuit description

Relaxation oscillator using single OTRA in comparator mode is implemented here. The PSpice schematic of relaxation oscillator using OTRA block 3(chapter 4) is shown in fig.6.29.

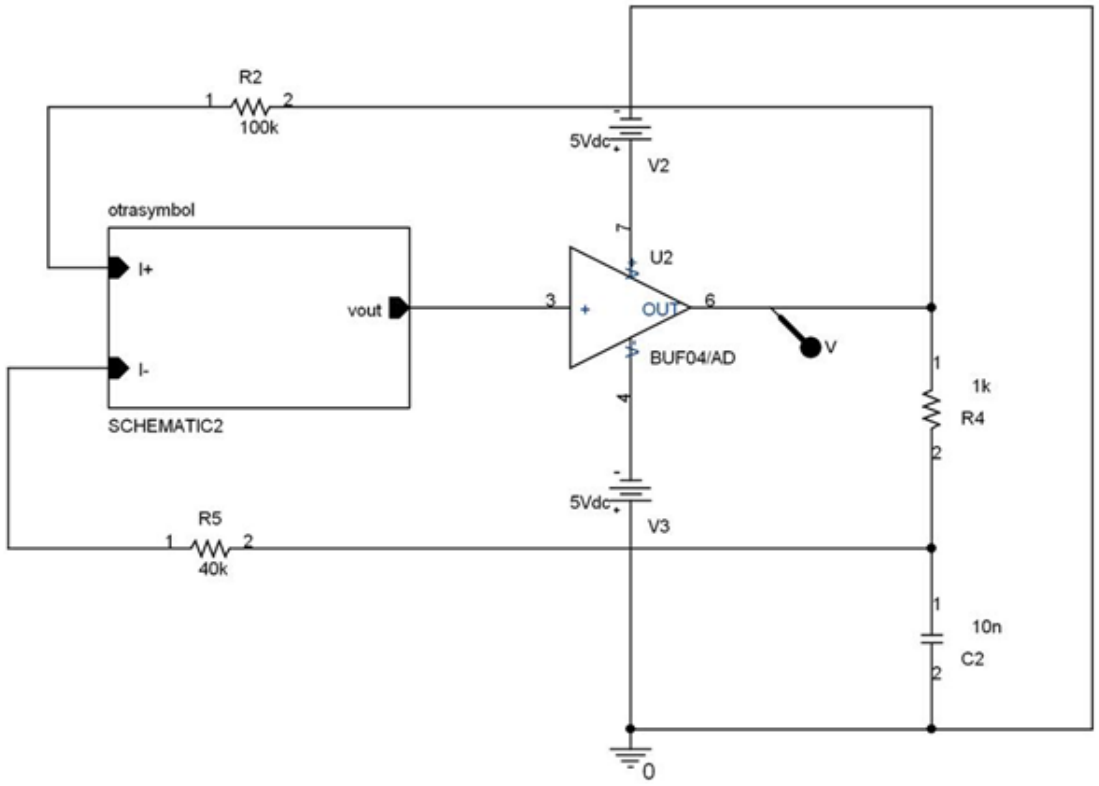

Fig.6.29 PSpice schematic of relaxation oscillator using OTRA block 3

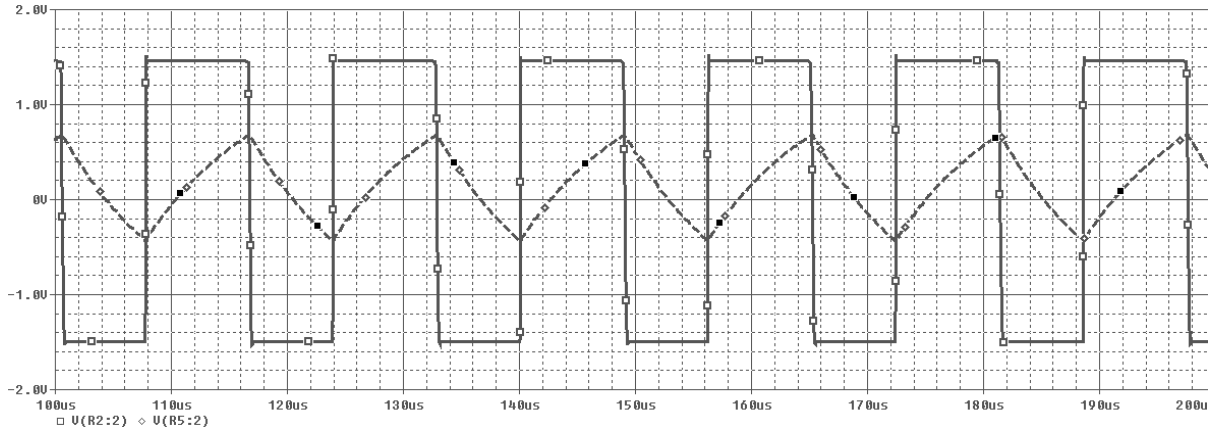

Fig.6.30 waveform of relaxation oscillator using OTRA block 3

6.3.3.2 Circuit description

Relaxation oscillator using single OTRA in comparator mode is implemented here. The PSpice schematic of relaxation oscillator using OTRA block 4(chapter 4) is shown in fig.6.31.

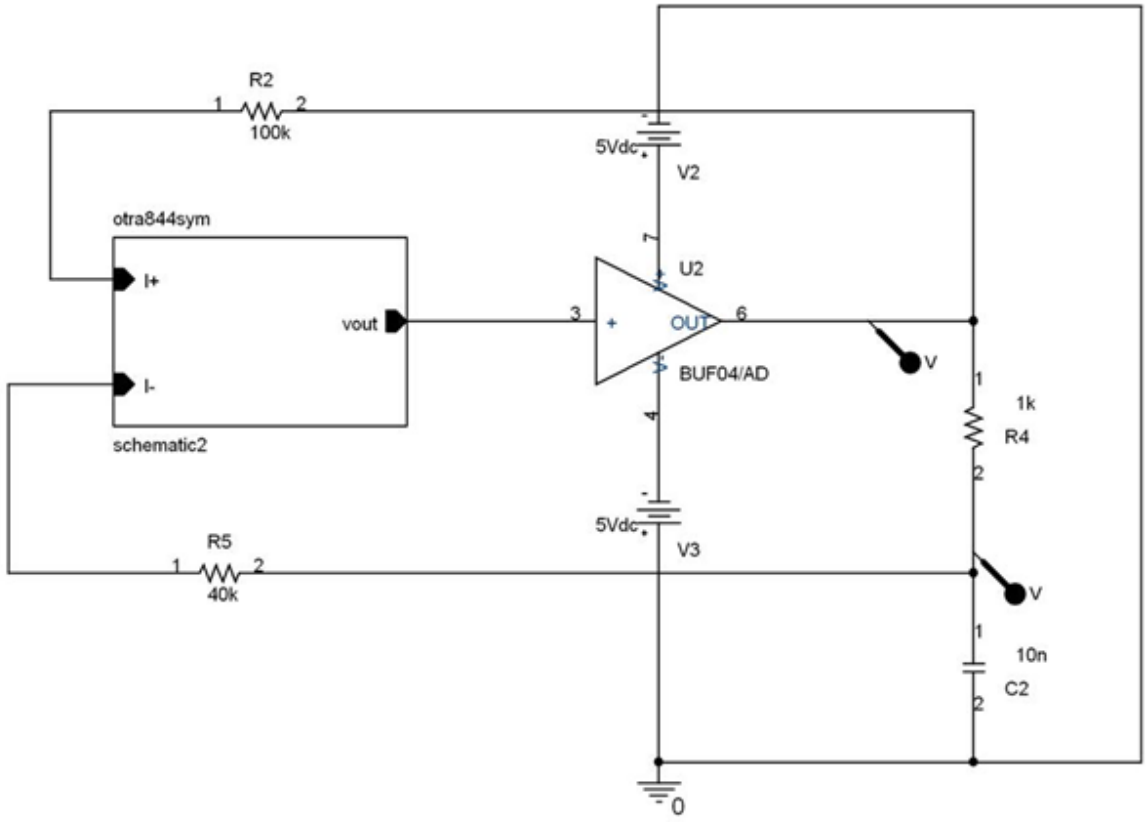

Fig.6.31 PSpice schematic of relaxation oscillator using OTRA block 4

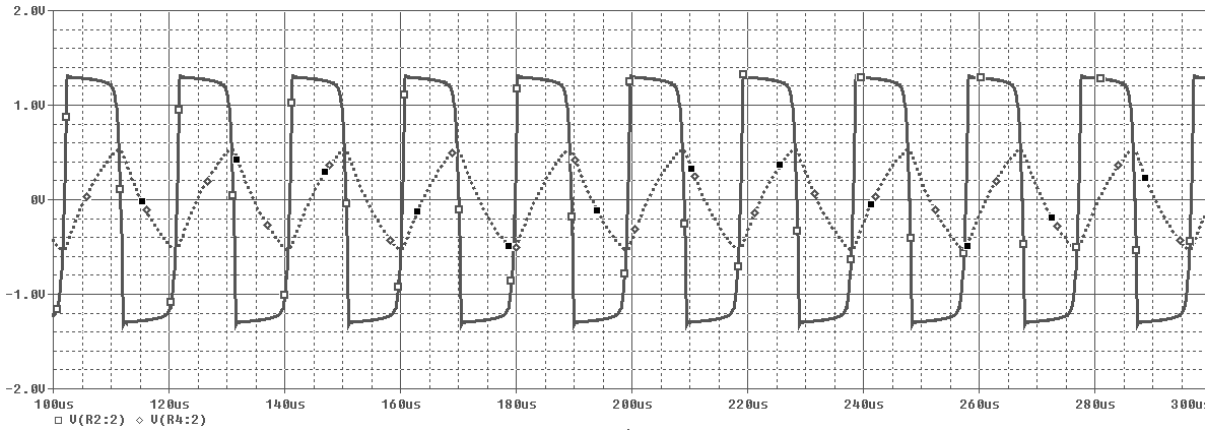

Fig.6.32 waveform of relaxation oscillator using OTRA block 4

REFERENCES

[44] CMOS Current-Mode Circuits for Data Communications - Fei Yuan

[45] R.Senani and V.K.Singh, "Synthesis of canonic single resistance controlled oscillators using a single current feedback amplifier." *IEE Proc. Circuit Devices and Systems* 143(3), pp. 71–72, 1996.

[46] Celma,S.,Martinez,P.A.andCarlosena,A.,"Minimalrealization for single resistance controlled sinusoidal oscillator using single CCII." *Electron. Lett.* 28, pp. 443–444, 1992.

[47] "Single OTRA Based Analog Multiplier and Its Applications" Rajeshwari Pandey, Neeta Pandey, B. Sriram, and Sajal K. Paul, International Scholarly Research Network ISRN Electronics Volume 2012, Article ID 890615.

[48] CMOS operational transresistance amplifier for analog signal processing - Khaled n. Salama, Ahmed m. Soliman, 1999

[49] K. Kaewdang, C. Fongsamut, and W. Surakampontorn, "A wide-band current-mode OTA-based analog multiplierdivider," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '03)*, vol. 1, pp. I349–I352,May 2003.

[50] S. I. Liu and D. J.Wei, "Analogue squarer and multiplier based on MOS square-law characteristic," *Electronics Letters*, vol. 32, no. 6, pp. 541–542, 1996.

[51] S. I. Liu and C. C. Chang, "Low-voltage CMOS four quadrant multiplier based on square-difference identity," *IEE*E *Proceedings Circuits, Devices and Systems*, vol. 143, pp. 174–176, 1996.

[52] WG.Weixin, C.Hongyi, and E. Seevinck, "Quadratic-translinear CMOS multiplier-divider circuit," *Electronics Letters*, vol. 33, no. 10, pp. 860–861, 1997.

[53] I. Baturone, S. Sanchez-Solano, and J. L. Huertas, "A CMOS current-mode multiplier/divider circuit," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '98)*, pp. 520–523, June 1998.

[54] B. Gibert, "A precision four-quadrant multiplier with subnanosecond response," *The IEEE Journal of Solid-State Circuits*, vol. 3, no. 6, pp. 353–365, 1968.

[55] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Oxford University Press, New York, NY, USA, 2004. 30 (1999) 157–160.

[56] D. Pozar, "Microwave and RF Design of Wireless Systems", John Wiley & Sons Inc, 2001.

[57] T. Vito and K. McClaning, "Radio Receiver Design". Atlanta, GA: Noble Publishing Corp, 2000.

[58] S. J. Erst, "Receiving Systems Design". Dedham, MA: Artech House, 1984.

[59] HOU C.L., CHIEN H.C., LO Y.K.: "Square wave generators employing OTRAs", IEEE Proc., Circuits Devices Syst., 2005, 152, (3), pp. 718– 722S.

[60] Robert Boyelstad, "Electronic circuit and devices", 2004.

[61] Ahmet Gocken and U.Cam, "MOS-C single amplifier biquads using the operational transresistance amplifier", 2008.

[62] K.N. Salama and A.M. Soliman, "Active RC applications of the Operational Transresistance Amplifier", Frequenz, pp.171-176,2000.

[63] U.Cam, "A Novel Single-Resistance-Controlled Sinusoidal Oscillator Employing Single Operational Transresistance Amplifier", Analog Integrated Circuits and Signal Processing, 32, pp. 183–186, 2002.

CONCLUSION AND FURTHER SCOPE

The squaring circuit has been presented. Simulation results of the squaring circuit using a 1.5 V power supply has been presented. The major advantages of this circuit is low power supply, multifunction of output, and free from the body effect. This circuit has application in analog multiplier, 2^N frequency multiplier. In addition, the proposed circuits in which their inputs can take the current signal or the voltage signal are interesting for application as versatile blocks in library of circuit architectures for automated circuit design.

Adder circuit act as combiner circuit and has application in implementation of various mathematical function. Multiplier circuit presented above has advantage of low power consumption and application as balanced modulator and mixer circuits in communication.

The OTRA is gaining increasing attention as a basic building block in analog circuit design. It is a building block having advantages of operating from low voltage supplies and overcomes the finite gain bandwidth product associated with traditional op-amp. The motive behind the design of OTRA is to provide amplification of high frequency signals with the ease of using standard operational amplifier.

In this thesis efforts are made to study the scope of OTRA as an active building block in analog circuits. Various CMOS realization of OTRA present in the literature are studied and these circuits are used to realize various signal processing and generating circuits having applications in communication. All the circuits were simulated using PSpice program and 0.5um process parameters. Simulation results show that the various characteristics are in good agreement with the theory. Slight variations in the results arise due to the non ideal behavior of the OTRA used.

Further, a number of non-linear circuits can be designed using OTRA. Operational amplifiers and some commercial IC's are commonly used to construct multipliers and multivibrators. But these voltage mode circuits have some disadvantages like complex internal circuitries and use of more passive components.