SIMULATION AND ANALYSIS OF GATE ALL AROUND TUNNEL FET FOR HIGH PERFORMANCE ANALOG AND RF APPLICATIONS

Thesis submitted by

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In Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

Under the Supervision of

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CERTIFICATE

This is to certify that the thesis titled "***Simulation and Analysis of Gate All Around Tunnel FET For High Performance Analog and RF Applications***" is being submitted by ***Miss. JAYA MADAN*** with registration number ***2K13/PHDAP/02*** to the Delhi Technological University for the award of the degree of Doctor of Philosophy in Applied Physics. The work embodied in this thesis is a record of bonafide research work carried out by me in the Microelectronics Research Lab, Applied Physics Department, Delhi Technological University (Formerly Delhi College of Engineering), New Delhi under the guidance of ***Dr. RISHU CHAUJAR***. It is further certified that this work is original and has not been submitted in part or fully to any other University or Institute for the award of any degree or diploma.

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ABSTRACT

SIMULATION AND ANALYSIS OF GATE ALL AROUND TUNNEL FET FOR HIGH PERFORMANCE ANALOG AND RF APPLICATIONS

Steeper subthreshold swing (SS) and lower OFF-state current (I_{OFF}) accessible by Tunnel FET offers great potentials in low power electronics applications. In this thesis, gate all around Tunnel FET's performance has been studied and various efforts have been done to overcome the major roadblock of TFET such as the lower ON-state current (I_{ON}), ambipolar conduction, higher threshold voltage (V_{th}) and the higher miller capacitance.

In this regard, firstly hetero gate dielectric (HD) and gate metal engineering (GME) are integrated simultaneously on a gate all around TFET i.e. HD-GME-GAA-TFET has been proposed. An analytical model for the proposed HD-GME-GAA-TFET has also been developed for its in-depth inspection. First and foremost, a drain current model for the proposed device is developed, and for the authentication of the developed model, the analytical results so obtained are matched with simulation results. For developing a drain current model, Poisson's equation is solved by using appropriate boundary conditions and continuity equations to obtain a surface potential profile, lateral electric field and finally by using the generation rate and tunneling barrier width, the drain current is obtained. Developed analytical model and the extensive simulations are used to determine the optimum value of hetero gate dielectrics and dual material gate work functions for acquiring best characteristics of the device. It is analyzed that the I_{ON} of GAA-TFET is enhanced from an order of 10^{-8}A to 10^{-4}A with the amalgamation of HD and GME. Furthermore, the SS of 49mV/decade at a V_{th} of 0.5V has been acquired. Moreover, the influence of gate and drain bias has also been analyzed on the electrical and analog performance of the proposed device. Further, the impact of gate oxide thickness has also been enlightened. It is analyzed that the SS of the proposed device in each case throughout the study, is much lesser compared to 60mV/decade

(fundamental limit on the SS of a conventional MOSFET), proving that the proposed device can be used for high performance switching applications in the future.

After analyzing the analog characteristics of HD-GME-GAA-TFET, and to account for the response time, switching speed and active power dissipation; the bias dependent intrinsic parasitic capacitances have been analyzed. The bias dependent parasitic capacitances have been examined under various gate bias, drain bias and also for different metal work function configuration of GME design. Further, for comprehensive RF analysis of GAA-TFET and its effectiveness at high frequency, various RF Figure of Merits (FOMs) such as maximum available power gain, maximum transducer power gain, cut-off frequency (f_T), maximum oscillation frequency (f_{MAX}) and intrinsic delay has also been studied for different gate metal work functions of GME engineering scheme integrated on GAA-TFET. The analyzed data would be beneficially providing detailed knowledge about the RF parameters of HD-GME-GAA-TFET at such aggressively scaled dimensions.

With the miniaturization of CMOS devices that marks in considerably high integration, the fabrication process damage, stress-induced damage and radiation damage at sub-nm regime result in solemn device reliability issues. These damages originate various interface trap charges (ITCs) at the Si-SiO_2 interface and thereby alters the ideal predicted device characteristics and is thus a serious issue that must be scrutinized before circuit designing. Thus, to account for the reliability of HD-GAA-TFET, the device is analyzed under the presence of ITCs of various polarity and density and the results are simultaneously compared with the ideal case in which the interface is free from defects. A comparative analysis of GAA-TFET and HD-GAA-TFET has been done in terms of various analog, RF and linearity parameters to inspect the impact of ITCs and thus the reliability. Results show that the integration of high-k dielectric near source side (to upgrade the device characteristics) concurrently leads to better immunity against the ITCs. Further, to find the pertinence of HD-GAA-TFET in wide temperature range ambience, the temperature robustness is also analyzed. Again the device analog and RF characteristics have been investigated at wide temperature range and it is realized that the HD-GAA-TFET and GAA-TFET have bias dependent temperature. Moreover, a severe degradation in I_{OFF} has been obtained at elevated temperatures, whereas at low temperatures (as compared to room temperature), the I_{OFF} reduces appreciably. Thus, the immunity against the ITCs and the marginally increased drain

current (in ON-state) marks the HD-GAA-TFET an efficient candidate for low power switching applications.

Afterwards, for comprehensively upgrading the performance of HD-GAA-TFET, the gate metal is overlapped near drain side that suppresses the ambipolar conduction. Extensive device simulations have been done to examine an optimum gate-drain overlap length (L_{ov}) at which the ambipolar current (I_{AMB}) is reduced efficiently. It is obtained that by overlapping the gate metal over the drain, the I_{AMB} is reduced to an order of 10^{-17}A. Additionally, the applicability of the HD-GAA-TFET as a Hydrogen gas sensor has been suggested by utilizing a Palladium (Pd) metal gate. Primarily, the Pd supported SiO_2 is used as a sensing media and sensing relies on the interaction of hydrogen gas molecules with Pd-SiO_2-Si. The sensitivity of the proposed gas sensor is compared with its conventional counterparts and it is obtained that the proposed design of gas sensor has appreciably high sensitivity. Further, the stability of the sensor with respect to temperature affectability has also been studied, and it is found that the device is reasonably stable and highly sensitive over the bearable temperature range. The successful utilization of HD-GAA-TFET in gas sensors may open a new door for the development of novel nanostructure gas sensing devices with a sensitivity of the order of 10^3 i.e. considerably higher than as obtained for a conventional MOSFET.

Another effort to overcome the major shortcoming of conventional TFET is done by integrating the efficient engineering schemes i.e. a n^+ source pocket and gate-drain underlapping (GDU) on GAA-TFET that form GDU-PNIN-GAA-TFET. The n^+ source pocket improves the analog and RF characteristics; on the other hand, the GDU controls the ambipolar conduction. Thereby, the GDU-PNIN-GAA-TFET gathers the collective merits of GDU (reduces the I_{AMB}) and n^+ source pocket (enhances I_{ON}). Hence, GDU-PNIN-GAA-TFET results in an up-gradation in the overall performance and offers a SS of 17mV/decade at a V_{th} of 0.4V, I_{AMB} of 10^{-18}A, and I_{ON}/I_{OFF} ratio of the order of 10^{12}.

Furthermore, the reliability issues of the PNIN-GAA-TFET have also been discussed. To study the reliability issues, at first, the effect of ITCs polarity, which is common during the pre and post-fabrication process, has been studied on the device analog/RF characteristics followed by the influence of ITCs density. Additionally, to examine the temperature robustness of the PNIN-GAA-TFET various electrical, analog and high-frequency parameters have been examined under different trap charge density and polarity at wide temperature

range. It is revealed that the donor traps are much hazardous in comparison to acceptor traps. In fact, at substantially higher density of donor traps, the subthreshold characteristics are found to be degraded tremendously that reduces the current switching ratio from an order of 10^{12} to 10^{5}. The temperature associativity reveals that PNIN-GAA-TFET has positive temperature coefficient in contrast to MOSFET. Moreover, the PNIN-GAA-TFET promises bearable immunity against ITCs along with stability to employ under wide temperature range.

Thus, the lower SS, high current switching ratio, lower I_{OFF}, superior RF performance, temperature robustness, and better reliability in terms of ITCs makes HD-GAA-TFET and PNIN-GAA-TFET, a promising candidate for employing in a low power, high switching speed and high performance applications even at wide temperature range.

LIST OF FIGURES

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LIST OF PUBLICATIONS

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CHAPTER 1

INTRODUCTION

First and foremost, this chapter discusses the background of the work that primarily describes the MOSFET and the quest for steeper subthreshold devices. In this regard, the chapter introduces the tunnel field effect transistor, i.e., TFET and continues to illustrate the fundamental operating principle of TFET. Thereafter, the significant merits offered by TFET are discussed that is extended with the major challenges faced by the conventional TFET. Also, the chapter describes the various engineering schemes that are reported to overcome the challenges faced by TFET to make it suitable for various analog and RF applications. In the next section, the chapter describes the reliability issues of CMOS devices. In this respect, the origin of interface trap charges, that are inevitably present in any practical device is discussed and is followed by the discussion of the reliability of TFET. Further, the chapter describes the research gaps that are found while literature survey and is followed by the several possible solutions to overcome these gaps. Thereafter, the chapter describes the primary objective of this thesis followed by an overview of all the chapters.

1.1 BACKGROUND

Since the invention of the first Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in early 1960's at Bell labs, MOS transistors have become the core of the integrated circuits (ICs) *(Shockley, 1976)*. Moreover, the Complementary MOSFET (CMOS) technology forms the heart of global electronic industry *(Hu, 2011)*. The unrelenting ever increasing demand for high speed and dense ICs is the driving force for scaling down the CMOS technology to nanometer nodes that has resulted into transforming the state of art of designing the IC, by providing the stability of operation, low static power dissipation and noise immunity to devices *(Heyns and Tsai, 2009, Moore, 1975, Moore, 2003)*. The great triumph of the CMOS devices is necessarily offered by the enhanced drive current and the higher cut off frequency acquired by scaling down the CMOS devices. The scaling of the CMOS devices follows the well-known Moore's law proposed by Gordon Moore (the co-founder of Intel Corporation) in 1960's that predicts that the number of transistors per IC would double approximately every 18 months *(Moore, 1975, Moore, 2003)*. Aggressive scaling of MOSFET down to nanometer regime is administered by the need of higher packing density, low operating power and high switching speed. The constant scaling of MOSFET enhances its switching speed and also the cut-off frequency to Giga-Hertz regime and thus makes it appropriate for wireless and high-frequency applications.

However, the aggressive scaling of MOSFET fallouts into several critical issues such as various short channel effects (SCEs) *(Chaudhry and Kumar, 2004)*. These SCEs degrades the performance of MOSFET and also increases the subthreshold swing (SS) to a value greater than the fundamental limit of MOSFET, i.e., 60mV/decade. Moreover, the SCEs increases the leakage current, while the supply voltage can no longer be scaled down, both of which result in increased power consumption. Along with various SCEs, with the reduced channel length, the passive power density approaches the active power density (in magnitude). To mitigate the standby power dissipation, lower OFF-state current (I_{OFF}) is required. However, the leakage current increases exponentially because the SS of MOSFET has a minimum value of 60mV/decade at room temperature. To overcome these flaws, various novel device architectures and materials engineering have been proposed such as multi-gate architectures of MOSFET, new gate dielectric materials, asymmetric channel doping engineering and much more *(Ferain et al., 2011, Park et al., 1998, Kranti et al., 2004)*. Since MOSFET is employed as a switch in digital applications; thus, the prime requirement for

switching applications is steeper ON/OFF transitions, i.e., lower SS and higher current switching ratio, i.e., I_{ON}/I_{OFF} ratio. The lower SS reduces the static power dissipation whereas, the higher I_{ON}/I_{OFF} ratio determines the performance level of the device. However, the variously reported device architectures for MOSFET successfully enhances the I_{ON}/I_{OFF} ratio, but the fundamental limit of MOSFET put constraints on SS and limit SS to 60mV/decade. Thus, the MOSFET has a fundamental limitation on SS to 60mV/decade at room temperature that is primarily offered by its current switching process, i.e., thermionic (temperature dependent) injection of electrons over the energy barrier. This fundamental limit on SS restricts further scaling of supply voltage below 1V due to the increased leakage current and various SCEs *(Sakurai, 2004, Bernstein et al., 2010, Seabaugh and Zhang, 2010).*

These fundamental limitations have inspired researchers to explore other paradigms of transistor construction that differ from MOSFETs in the underlying mechanism of carrier injection, and yet preserve the qualities that make MOSFET a successful candidate in the first place *(Ionescu and Riel, 2011, Madan and Chaujar, 2017c).* Another critical factor that must be taken into account is the compatibility of the device under consideration with the existing CMOS architecture *(Gandhi et al., 2011).* A promising candidate in this regard is the Tunnel Field Effect Transistor (TFET). A TFET is a gated p-i-n junction that is operated in reverse bias *(Madan and Chaujar, 2016b, Madan and Chaujar, 2017a, Madan and Chaujar, 2017b, Boucart and Ionescu, 2007, Chen et al., 2009, Choi et al., 2007)*. Majority carriers are injected from the source into the channel through quantum mechanical Band-to-Band Tunneling (BTBT) which is a result of finite, but non-zero, probability of tunneling through a potential barrier. This lifts the aforementioned fundamental limitation of a minimum SS of 60 mV/decade, allowing TFETs to have SS as low as 20 mv/decade *(Khatami and Banerjee, 2009).* Apart from TFET, there are many other devices whose working principle is not governed by the drift-diffusion mechanism as in the case of MOSFET. These steeper subthreshold devices comprise: impact ionization–MOS or I-MOS *(Björk et al., 2007),* nano-electro-mechanical FETs or NEMS FETs *(Kam et al., 2005)* and suspended gate MOSFETs *(Abelé et al., 2005).* However, the work in this thesis encompasses the TFET for low power high switching analog and RF performance.

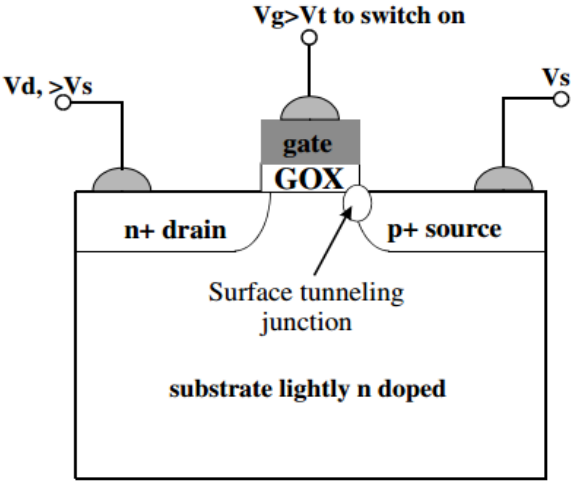
1.2 TUNNEL FIELD EFFECT TRANSISTOR (TFET)

1.2.1 OPERATING PRINCIPLE

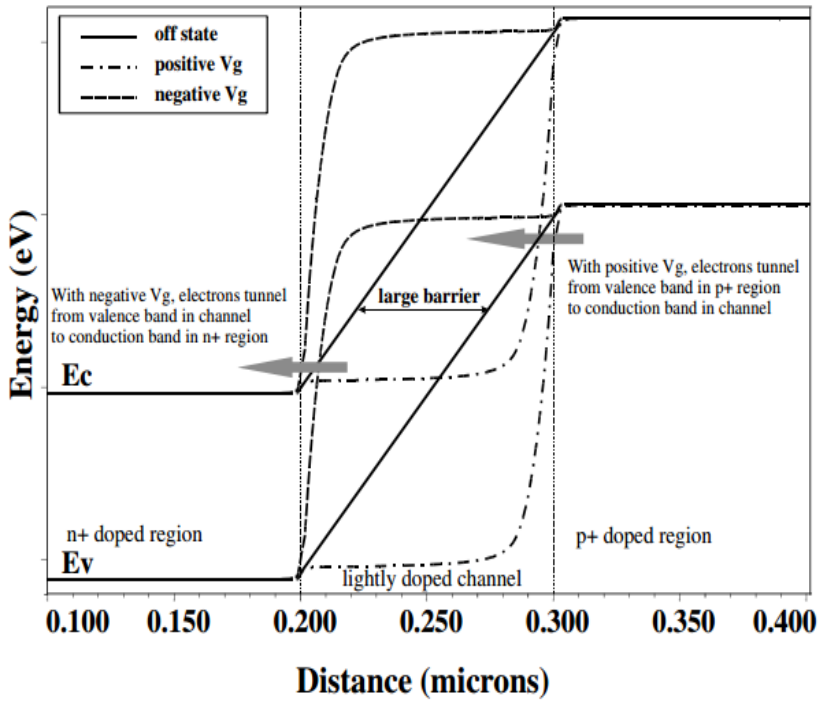
The fundamental TFET is a metal-gated p-i-n structure with the metallic gate deposited at the entire intrinsic channel region, and the p and n region is doped degenerately that principally acts as a source and drain respectively in case of n-TFET. The applied bias at the gate metal essentially controls the BTBT at the source and channel junction. **Figure 1.1(a)** depicts the schematic view of n-type TFET and its corresponding energy band diagram in ON, OFF and ambipolar state is represented in **Figure 1.1(b)**. It is worth mentioning that TFET works in reverse bias conditions to get the ultra-low leakage current. In comparison to MOSFET, the device structure of TFET is similar to MOSFET, with an exception that in TFET, the source and drain doping are asymmetric. Specifically, for an n (p)-type TFET, the source is $p^+(n^+)$ doped and drain is $n^+(p^+)$ doped. This asymmetric source/drain doping results into a staircase like energy band profile in TFET. Moreover, the Quantum Mechanical BTBT is the primary carrier injection mechanism in TFETs as opposed to thermal carrier injection in MOSFETs *(Ionescu and Riel, 2011, Khatami and Banerjee, 2009, Nagavarapu et al., 2008, Choi and Lee, 2010)*. In TFETs, BTBT takes place at the source-channel interface due to the bending of energy bands owing to the applied voltages *(Madan and Chaujar, 2016a, Madan and Chaujar, 2017a)*. In case of n-TFET,

i. For a reverse biased p-i-n junction and V_{gs}=0 V, i.e., the OFF state of TFET, the energy bands are aligned in such a way that there is a large tunneling barrier width present at the source channel (tunneling) junction. This wide barrier width and the barrier for thermal emission restrict the tunneling of electrons and this inherent physics of TFET upshots into a very low subthreshold leakage current (generally of the order of femto Amperes). Ideally, the tunneling barrier width at V_{gs}=0 V is identical to the channel length.
ii. For an increase in positive voltage at the gate metal, i.e., for V_{gs}>0, an accumulated or inverted n-channel is formed. This pushes down the energy bands in the channel region, and subsequently, the valence band of the p^+ overlaps with the conduction band of the channel that reduces the tunneling barrier width. This results in the formation of a surface tunnel junction at the p^+ and channel junction as illustrated in **Figure 1.1(a)**. The resultant electron energy band diagram is presented in **Figure**

1.1(b). The reduced barrier width allows the tunneling of electrons from the valence band of the p^+ region to the conduction band of the channel. After tunneling to channel region via BTBT mechanism, electrons transport to drain via drift-diffusion, resulting in drain current.



(a)



(b)

Figure 1.1 (a) Schematic view of basic n-Type TFET (b) energy band diagram of 100nm n-Type TFET in OFF, ON and ambipolar state, with 100nm channel length; the n^+ doped region is positive biased and p^+ doped region is grounded *(Wang et al., 2004)*.

iii. For applied negative gate bias, i.e., for $V_{gs}<0$, an inverted or accumulated p-channel is formed. This leads to lifting the energy bands of the channel region upwards and consequently moves the surface tunnel junction at the n^+ and channel junction. Furthermore, it leads to narrower barrier width at the drain and channel junction that becomes favorable for tunneling and thereby results in an ambipolar conduction in TFET. Principally, in this case, electrons tunnel from the valence band of the channel to the conduction band of the n^+ region (drain). The holes generated in the channel flows to the p^+ region (source). Consequently, in this case, the p^+ region acts as drain (drain of holes) and the n^+ region acts as source. Thus, TFET does not turn OFF for the negative gate bias as opposed to n-MOSFET which has a negligible current for negative gate bias. This conduction of TFET for negative gate bias is the ambipolar conduction of TFET.

1.2.2 MERITS OF TFET

The significant impediments of MOSFET while scaling down to the sub-nanometer regime is the SCEs, that has been overwhelmed by the intrinsic tunneling barrier width present at the source channel junction of TFET and makes TFET insusceptible to SCEs. However, at very short channel lengths, the drain potential can affect the tunneling junction which can be resolved by reducing the V_{ds} that is primarily enabled by the lower SS of TFET. The insusceptibility of TFET to SCEs allow further downscaling of TFET, prolonging the Moore's Law and thereby poses it to be a superior candidate for ultra-low power era *(Choi et al., 2007)*. Moreover, TFET works on BTBT as its inherent transport mechanism instead of drift-diffusion of charge carrier as in case of MOSFET. Thus, the independence of tunneling on temperature results in the weak temperature dependence of TFET characteristics *(Mookerjea et al., 2010)*. Hence, TFET overcomes the fundamental limitations of MOSFET that limits its SS at 60mV/decade at 300K. In other words, the SS of TFET can be smaller than 60mV/decade, and thus allows further downscaling of the supply voltage, due to the lower SS, the supply voltage required for operating TFET is lower, that turns in lower static and dynamic power dissipations *(Khatami and Banerjee, 2009)*. Additionally, as the gate controls the tunneling barrier width, accordingly at lower gate voltages, the broad tunneling width at the source channel junctions inhibits the tunneling of electrons, and there is only feeble current $\sim 10^{-15}$A (lesser than the I_{OFF} of MOSFET). This lower I_{OFF} translates into lower

static power dissipation. Furthermore, TFET has compatibility with already existing standard CMOS fabrication technology that ensures the viability of TFETs fabrication and also its cost-effectiveness *(Moselund et al., 2016)*. These benefits of TFET make it a potential candidate to replace MOSFET, as TFET would contribute to the goal of reducing the operational speed (instigated by lower V_{dd}) along with the standby power, which has sturdy implications on electrical power consumption today.

1.2.3 CHALLENGES CONFRONTED BY TFET

In the previous subsection, the significant merits of TFET have been discussed, and this section continues to summarize the problems confronted by TFET. It is essential to tackle these challenges to employ TFET for wide scale applications. Heretofore, it is reported in various research articles that the lower tunneling probability in TFET leads to inferior ON current (I_{ON}) of TFET in comparison with MOSFET. This lower I_{ON} limits the device speed and also translates in higher threshold voltage (V_{th}). Thus, the primary challenge in TFET to outperform CMOS transistors is to realize high I_{ON} without any degradation in the I_{OFF} *(Anghel et al., 2010)*. Various device and material engineering schemes have been reported for enhancing the tunneling rate of electrons, that thereby conquer the lower I_{ON} and higher V_{th} of TFET and will be extensively discussed in the next part of this chapter.

Moreover, in contrast with the n-MOSFET, (which is switched ON for a $V_{gs}>0$ and is switched OFF for $V_{gs}<0$), TFET works as both n-type and p-type for positive and negative V_{gs}. Specifically, for an n-TFET with a positive bias applied to the drain, the electrons tunnels from p^+ source to channel for $V_{gs}>0$ (tunneling at the source channel junction). Additionally, for $V_{gs}<0$, with the same drain bias, the holes will tunnel from the n^+-drain to channel (tunneling at the drain channel junction) and constitute drive current mostly of the same order of magnitude as for $V_{gs}>0$. This is primarily the ambipolar conduction of TFET, that is undesirable for logic devices specifically inverters that demands the unipolar behavior i.e. for perfect levels of OFF and ON states *(Wang et al., 2004)*. Briefly, ambipolar conduction is caused by the lowering of barrier width at the drain-channel junction for negative gate bias (for the case of n-TFET). The various previously reported device design architectures and material engineering schemes for suppressing the ambipolar conduction have also been discussed in the next section of this chapter.

Further, one more challenge of TFET is the pronounced miller effect attributed by the dominant gate to drain capacitance in comparison with gate to source capacitance that collectively contributes to the total gate capacitance *(Gnani et al., 2015, Mookerjea et al., 2009)*. The inherent BTBT negligibly contributes to the inversion charge density thereby the gate to source capacitance contributes negligibly to total gate capacitance in comparison with gate to drain capacitance.

1.2.4 DEVICE ENGINEERING TECHNIQUES FOR OVERWHELMING CHALLENGES FACED BY TFET

1.2.4.1 HETEROSTRUCTURE TFET

To enhance I_{ON}, the concept of different source material other than channel is proposed and is known as the heterostructure TFET. The source material is chosen such as it must have a smaller energy bandgap as compared to the bandgap of channel material. The small bandgap material in source region radically reduces the tunneling barrier width between the source and channel junction that in turn enhances the tunneling probability and thereby the drain current *(Hanna et al., 2015, Moselund et al., 2016, Hanna and Hussain, 2015)*. For example - a Ge-Si heterostructure TFET, in which source is of Ge that has a lower bandgap, with Si used as channel and drain. With the Ge source, the band bending at the tunneling junction is molded such as the barrier width is reduced that translate into higher tunneling rate of electrons.

1.2.4.2 DUAL MATERIAL GATE (DMG) OR GATE METAL ENGINEERED (GME) OR HETEROMATERIAL GATE (HMG) TFET

To acquire a simultaneously up-gradation in ON and OFF-state characteristics (without affecting the chip density), a Dual Material Gate TFET is proposed by Vishnoi et al. *(Vishnoi and Kumar, 2014)*. In DMG-TFET, the gate metal is divided into two parts viz. the tunneling gate (near the source side) and the auxiliary gate (near the drain side) as depicted in **Figure 1.2**. For n-channel TFET, the metal near the source, i.e., the tunneling metal has lower work function and the metal near the drain, i.e., the auxiliary gate has higher work function. The aim of implementing a lower work function metal near source is to enhance the tunneling rate owing to the reduced flatband voltage that lowers the barrier width at

comparatively lower gate bias. Subsequently, the higher tunneling rate enhances the drain current and also reduces the V_{th}. Moreover, by using a higher metal work workfunction material near the drain, the subthreshold characteristics of TFET are controlled.

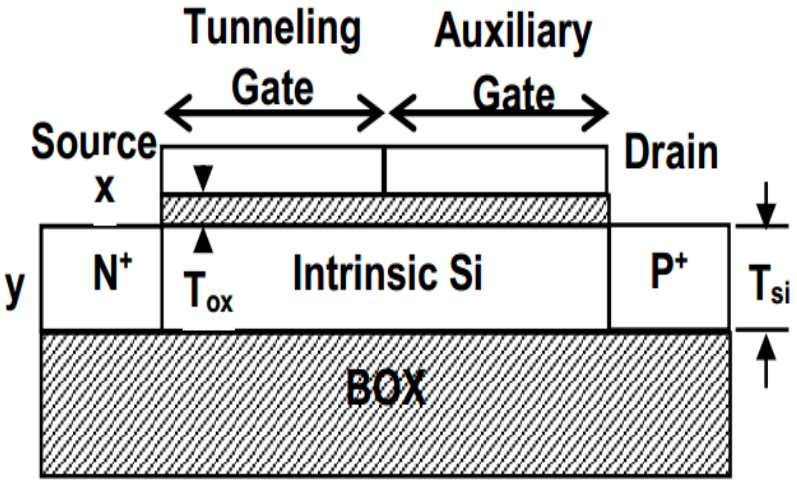


Figure 1.2 Schematic representation of a p-type DMG-TFET *(Vishnoi and Kumar, 2014)*.

1.2.4.3 HIGH-K DIELECTRIC TFET AND HETERO GATE DIELECTRIC TFET (HD-TFET)

To increase the I_{ON} and also to reduce V_{th}, the high-k gate dielectric has been introduced as opposed to conventional SiO_2 *(Boucart and Ionescu, 2007)*. The high-k material such as Hafnium dioxide (HfO_2) with k~21, Silicon Nitride (Si_3N_4) with k~7.5, Zirconium dioxide or Zirconia (ZrO_2) with k~25, etc. can be implemented as the gate oxide in TFET. The high-k dielectric material as gate oxide primarily increases the surface potential as inferred by Equation 1.1

$$V_{gs} = -\frac{q_s t_{ox}}{\varepsilon_{ox}} + \phi_s \tag{1.1}$$

Where;

q_s is the charge density per unit area,

t_{ox} is the gate oxide thickness,

ε_{ox} is the permittivity of the gate oxide material and,

ϕ_s is the surface potential.

It is deduced from Equation 1.1 that at a constant gate bias, the surface potential has a direct reliance on the high-k dielectric. For higher tunneling rate, lower barrier width and

thereby steeper band bending are required that demands for high surface potential and thus for a high-k gate oxide. The lower barrier width at the source channel junction offered by the high-k gate oxide enhances the tunneling rate and henceforth mitigates the major roadblocks of TFET, i.e., lower I_{ON} along with higher V_{th}.

However, the concomitant challenge with high-k gate dielectric is the simultaneous increase in the ambipolar current (I_{AMB}). Thus, to overwhelm this, i.e., to acquire higher I_{ON} without any increase in the I_{AMB}, a hetero gate dielectric (HD) engineering scheme is proposed by Choi et al. *(Choi and Lee, 2010)*. In HD engineering scheme, a high-k material is locally implanted in the oxide near the source-channel junction as shown in **Figure 1.3**. The high-k material located partially in the oxide near the source side over the channel induces a local minimum in the conduction band at the tunneling junction. However, the rest oxide, i.e., the dielectric near the drain side consists of conventional SiO_2 that prevents the ambipolar conduction. Therefore, in HD-TFET, the I_{ON} is enhanced by the high-k dielectric material and is substantially followed by the TFET with high-k dielectric at entire gate oxide. Simultaneously, the I_{AMB} is followed by the case as that of TFET with SiO_2 as gate dielectric that thereby inhibits the ambipolar conduction. Consequently, HD-TFET concurrently employs the welfare of both SiO_2 dielectric (in ambipolar state and OFF-state) and high-k dielectric (in ON-state), thus offers lower I_{OFF} and higher I_{ON} respectively. Apart from improved I_{ON} and suppressed I_{AMB}, HD-TFET also offers lesser gate to drain capacitance (w.r.t. the case of high-k dielectric TFET) that is desirable for higher switching speed of any transistor.

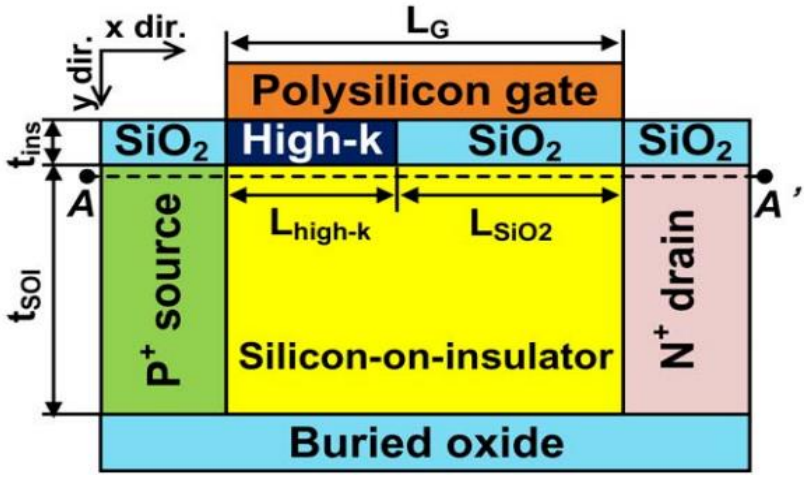


Figure 1.3 Schematic representation of a hetero gate dielectric TFET *(Choi and Lee, 2010)*.

1.2.4.4 TUNNEL SOURCE P-N-P-N TFET

One of the approaches for mitigating the issues of lower I_{ON} and also higher V_{th} is implantation of a n^+ pocket in the channel region adjacent to the source side proposed by Nagavarapu et al. *(Nagavarapu et al., 2008)*. The schematic view of an n^+ source pocket PNIN-TFET is displayed in **Figure 1.4**. The critical parameters for designing an optimised PNIN-TFET are the source pocket doping and the source pocket width. Additionally, tilt angled implantation process can fabricate the n^+ pocket that ensures its fabrication feasibility. The up-graded parameters such as higher I_{ON}, lower V_{th} and lower SS can be acquired by implanting a n^+ pocket in the channel near source side owing to the formation of a local minima in the conduction band that subsequently, narrows the barrier width *(Madan and Chaujar, 2017a, Jhaveri et al., 2011)*. The narrow tunneling barrier enhances the tunneling generation rate and thereby overcome the issues of lower I_{ON} and simultaneously reduces the V_{th} of TFET.

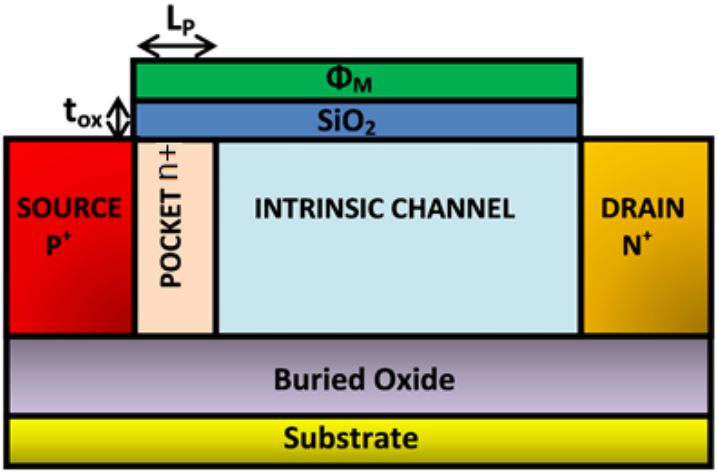


Figure 1.4 Schematic device structure of n^+ source pocket PIN-TFET or PNIN-TFET.

1.2.4.5 MULTI-GATE TFET

Apart from the above engineering schemes that account for the alterations in the gate oxide, gate metal and channel engineered; multigate architectures TFET has also been reported such as the double gate TFET (DG-TFET), FINFET, Triple gate (or л-gate), Omega gate (Ω-gate) and the Gate All Around TFET (GAA-TFET). In DG-TFET, there are two independent gates fabricated in such a way that the channel is sandwiched between them. Moreover, the gate oxide thickness and metal work workfunction of both the gate metals are

same, i.e., both the gates are symmetric with a common gate bias that tied them together. The primary idea of designing DG-TFET is to enhance the gate controllability over the channel and thereby, the effective electric field at the tunneling junction increases that is followed by the steeper band bending that enhances the tunneling rate of electrons and hence, increases the drain current. The DG-TFET is substantially similar to the design of DG-MOSFET that was proposed by T. Sekigawa et al. in 1984 *(Sekigawa and Hayashi, 1984)*. Thereafter, in 1987 Balestra et al. *(Balestra et al., 1987)*, have reported the concept of volume inversion in DG-MOSFET that results in an advantage in scaling about two times. Further, a gate all around MOSFET (or the surrounding gate MOSFET or Wrap around gate MOSFET) in which the gate surrounds the entire silicon beam is reported *(Colinge et al., 1990, Takato et al., 1991, Leobandung et al., 1997, Auth and Plummer, 1997)*. It is worth mentioning that the silicon beam may be wide or narrow, square, rectangular or circular and of any of the orientation. It is investigated by Leobandung et al. that GAA-MOSFET can be scaled further about 50% in comparison with DG-MOSFET owing to the extra degree of electrostatic confinement offered by the GAA architecture *(Leobandung et al., 1997)*. Furthermore, the GAA architectures ensure the merits of extremely high packing density that is desirable for proper memory storage. Primarily, the GAA geometry increases the electrostatic control and thereby allows further gate length scalability. Among all the geometries of GAA, the cylindrical gate geometry is of ultimate importance as it provides further gate length scalability. The cylindrical GAA-TFET enhances the tunneling volume and thus lifts the tunneling probability that leads to improved I_{ON}. These abundant merits of GAA-TFET are the key motivating force for exploring it and thereby the entire research work done in this thesis is principally based on cylindrically GAA-TFET.

1.2.4.6 SHORT GATE TFET OR GATE-DRAIN UNDERLAPPED (GDU) TFET

Verhulst et al. *(Verhulst et al., 2007)* have introduced the concept of gate metal underlapping near drain side also stated as the short gate TFET. In short gate engineering, the gate metal is not over the entire channel length and is underlapped near drain side or is limited to the source *(Verhulst et al., 2007, Chattopadhyay and Mallik, 2011)*. In doing so, the underlapped gate metal near drain side limits the charge carrier (that is built-up underneath the gated region) to the gated region or restricts its extension towards the underlapped region. Hence, the short metal gate controls the ambipolar conduction *(Wang et al., 2014)*. Besides

reducing the I_{AMB}, the GDU-TFET also decreases the intrinsic gate to drain capacitance (C_{gd}) that is one of the major hindrances while designing TFET circuitry. Moreover, GDU is of prime importance due to its viability offered by the simple fabrication process.

1.2.4.7 GATE-DRAIN OVERLAPPED TFET

The gate-drain overlapping (GDO) scheme is also one of the engineering used to suppress the ambipolar conduction. Conventionally, the gate metal exists only over the channel region. However in GDO, the gate metal is extended towards the drain region beyond the channel such that it overlaps the drain region as illustrated in **Figure 1.5**. It is reported that the overlapped gate metal over drain side limits the gate to control only the source channel junction irrespective of the gate bias polarity *(Abdi and Kumar, 2014)*. For n-type TFET, with the integration of GDO, the band bending at the source channel junction remains same as for the case when gate metal is not overlapped over the drain. But with overlapping gate metal over the drain and applying a negative gate bias, the effect of gate bias is primarily same on drain channel junction as that of the channel region. This result in broadening of barrier width at the drain channel junction and thereby controls the ambipolar conduction. Moreover, it is worth mentioning that the GDO doesn't alter the device characteristics for the positive gate bias region *(Shaker et al., 2015)*. For processing of GDO, the electron beam lithography is used for patterning of the gate metal, and then the electron beam evaporation is used for gate metallization *(Madan and Chaujar, 2016a)*.

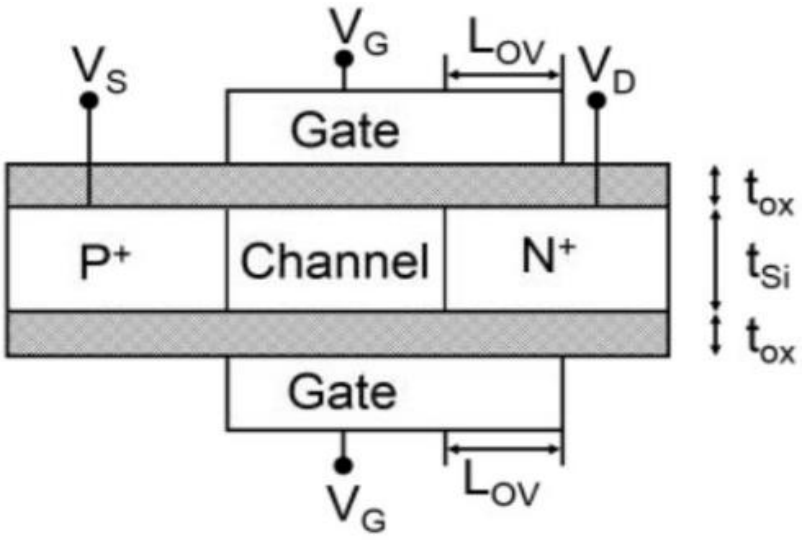


Figure 1.5 Schematic view of gate-drain overlapped TFET (GDO-TFET) *(Abdi and Kumar, 2014)*.

1.2.4.8 ASYMMETRIC SOURCE/DRAIN DOPING

To alleviate the ambipolar conduction, the viewpoint is to decrease the tunneling at the drain channel junction such that the tunneling at the source channel junction remains unaltered. The most straightforward engineering approach reported for suppressing the ambipolar conduction or to acquire unipolarity, is an asymmetrically doped source and drain TFET. It has been reported that by employing an asymmetry such that the drain doping is less than the source doping efficiently reduces the ambipolarity with insignificant alteration in I_{ON} *(Wang et al., 2004).*

1.3 RELIABILITY ISSUES OF CMOS DEVICES

1.3.1 INTERFACE TRAP CHARGES

With intensification in the complexity and density of VLSI chips, the assessment of the long-term reliability of CMOS devices becomes compulsory. The reliability of MOS devices is very much affected by the quality of interface of semiconductor and oxide. Precisely, the Si-SiO_2 interface may be associated with four types of charges viz. fixed oxide charges, mobile oxide charges, oxide trapped charges and interface states. Moreover, these charges inevitably appear during the fabrication of the MOS devices. Although the number of such charges has been reduced significantly with continuous improvements in fabrication technology, still they cause a substantial degradation in the operation of the device due to the high packing density of transistors in microchips today.

The origin of these interface states are primarily offered by the high electric field present at the source channel junction (in case of TFET) for the positive gate and drain bias, that is generated in TFET by the steeper band bending at the source channel junction. The charge carriers that tunnel through the source channel junction get across this considerably high electric field, and thereby gain an expressively enormous amount of energy between two scattering events. Few of these energetic charge carriers may gain enough energy (about 1.12eV) that generate the electrons and holes by impact ionization. However, a small fraction of charge carriers gain even large energy (~ 3.2eV for electrons and 4.7eV for holes), that they may surmount the interface of Si-SiO_2 and may penetrate inside the SiO_2 and may constitute the gate leakage current. Among these penetrated charge carriers few of them may remain trapped in the oxide and if they are still energetic enough, they may subsequently

break some of the Si-H or similar weak bonds in the SiO_2. This penetration may translate to a permanent modification of the characteristics of the device and thereby degrades the functioning of integrated circuits. Additionally, the passage of ionizing radiation in the oxide may also turn to generate the trapped charges in the oxide layer. The electron-hole pair thereby created may recombine or move in the electric field of oxide; such that the generated holes move towards the metallic gate and the electron travels toward the interface of Si and SiO_2. The holes moving towards the metallic gate may be trapped in the oxide and leads to the generation of a positive charge in the oxide. Besides, the generation of trapped charges, the ionization radiation may produce new energy levels in the bandgap at Si-SiO_2 interface that may be occupied by the charge carriers depending on the Fermi level position at the interface and the oxide charge will be added/subtracted to the correspondingly charge value *(Oldham and McLean, 2003, Neamen, 2003).*

The most critical factors accountable for the device damage complications are: process induced damage *(Poindexter, 1989)*, radiation-induced damage *(Lho and Kim, 2005)*, stress-induced damage *(Trabzon and Awadelkarim, 1998)* and hot carrier induced damage *(Naseh et al., 2006)*. In the era of sub-100nm, device designing plasma etching used for pattern transfer process may produce electrical and processing damage (falls under the category of stress-induced damage), and thereby damage the Si-oxide interface along with the oxide and consequently degrades the performance, yield, and reliability of the device.

Mostly the interface trap charges are of two types; viz. the acceptor type and donor type interface state. The acceptor type interface states behave as electrically neutral when it is empty, and it comes to be negatively charged when filled with an electron. Whereas, the donor type interface states behave electrically neutral when filled with an electron and turn into positively charged when it is empty *(Madan and Chaujar, 2016b, Madan and Chaujar, 2017b)*. Apart from donor/acceptor, a specific interface state is also characterized by (i) the exact energy level in the bandgap i.e. measured in eV from the valence band edge, (ii) its spatial location in the device, for example distance from the source side and (iii) its density i.e. the number of states/cm^2 for discrete states.

The position of the Fermi level in the energy band gap accounts the net charge quantitatively in the respective interface state *(Neamen, 2003).* It is reported by Neamen *(Neamen, 2003)* that the acceptor (donor) states lie in the upper (lower) half of the energy bandgap. Moreover, these interface states act as a fixed positive/negative charge as if in case

the acceptor interface trap will accept an electron if the trap level is beneath the Fermi level and so the interface state will behave as a negative fixed charge. Similarly, a donor type interface trap acts as a positive fixed charge and thereby in this thesis, these interface traps are accounted as effective positive and negative fixed interface charges.

1.3.2 RELIABILITY OF TUNNEL FET

Furthermore, the reliability of TFET is a more prominent issue as compared to MOSFET, because of the change in tunneling field impacted by these interface trap charges (ITCs). As in TFET, the BTBT rate of electrons is highly sensitive to the electric field along the channel direction E_y, being proportional to $\exp(-A/E_y)^6$ *(Qiu et al., 2014)*. The effect of ITCs on the electric field thus strongly effects the BTBT rate of electrons, and hence the overall device characteristics. Furthermore, the high electric field needed at the tunneling junction for augmenting the tunneling rate (or lowering the tunneling barrier width) at the source-channel junction has counter effects of generation of ITCs (both donor and acceptor type).

1.4 RESEARCH GAPS

1. *Designing of a comprehensively upgraded TFET that may efficiently uproot the significant roadblocks of TFET such as the lower I_{ON}, higher V_{th}, higher miller capacitances and ambipolar conduction simultaneously.*
2. *As the response time, active power dissipation and switching speed of the TFET are interdependent on the parasitic capacitances, analysis of the RF performance and the intrinsic parasitic capacitances of TFET for realizing TFET as amplifiers and receivers for RF communication are mandatory.*
3. *To run into the perpetual call of transistors with high and low-temperature tolerance desirable in aircraft, space, and automotive technology, temperature affectability over device performance must be analyzed.*
4. *For sub-100-nm devices, the reliability of TFET is a serious concern, owing to the strong electric field at the source-channel junction that has not been accounted till date.*

5. *The fabrication processes for sub-100-nm devices, such as plasma etching may damage the gate oxide as well as the interface of the Si-SiO_2 interface. These defects are the origin of interface trap charges and oxide charges that alters the ideal predicted characteristics. Thus, the device performance must be analyzed in the presence of these default traps to ensure the reliability.*

6. *H_2 gas sensors have perpetual demand for automotive, environmental monitoring, petroleum refining process, and medical industries. Thus, it is needed to design an H_2 gas sensor leverages the benefits of TFET.*

1.5 POSSIBLE SOLUTIONS

To design a TFET, that can collectively overcome the major roadblocks of TFET such as lower I_{ON}, higher V_{th}, and ambipolar conduction. Aiming this there are various possible solutions:-

1. Integration of various engineering schemes in such a manner, that their collective merits may resolve the significant shortcomings of conventional TFET. In this respect, the hetero gate dielectric (HD) and Gate Metal Engineering (GME) can be collectively amalgamated over GAA-TFET. The elementary logic behind the integration of HD and GME is to design a single TFET with considerably reduced challenges of both the engineering, i.e., the low I_{ON} and high I_{AMB} of GME and; the high I_{OFF} and high SS of HD. It is anticipated that the integrated HD-GME-GAA-TFET will offer lower SS, higher I_{ON}, suppressed I_{AMB} along with low leakage current.

2. As sufficiently high I_{ON} has been attained by the HD engineering; thus another potential possible solution is to integrate another engineering scheme to suppress I_{AMB}. The two engineering schemes must be implemented in such a way that one should not affect the other. In this regard, the gate metal can be overlapped over drain side on HD-GAA-TFET to control the ambipolar conduction, thereby, to reduce the I_{AMB} along with higher I_{ON} acquired by the high-k dielectric material used in the HD engineering scheme.

3. Furthermore, the high-k materials owe various constraints such as they generate the high fringing field from gate to the source region in case of HD engineering scheme (from gate to source as well as drain if deposited at the entire gate oxide). Moreover, the HD engineering scheme enhances the intrinsic parasitic capacitances that limit its switching

speed. Thus, one more engineering scheme namely n^+ source pocket has been reported that implants an n^+ pocket in the channel region near the source side. The n^+ source pocket can be implanted on GAA-TFET that results in the formation of PNIN-GAA-TFET. By implanting a n^+ source pocket near the source, only the positive transfer characteristics are upgraded that overcome the issues of lower I_{ON}, higher V_{th}, and higher SS without any degradation of intrinsic parasitic capacitances as in case of HD-GAA-TFET. Furthermore, as n^+ source pocket doesn't control the ambipolar conduction, the concept of the short metal gate can also be simultaneously integrated on PNIN-GAA-TFET to account for the ambipolar conduction. Therefore, collectively with GDU and PNIN, the GAA-TFET can overall results in superior characteristics.

1.6 OBJECTIVE OF THESIS

1. To design a TFET, that can collectively overcome the major roadblocks of TFET such as lower I_{ON} and ambipolar conduction. For this, various engineering schemes such as hetero gate dielectric (HD) and Gate Metal Engineering (GME) have been amalgamated over GAA-TFET.

2. To develop an analytical drain current model for HD-GME-GAA-TFET and investigate its various electrical and analog characteristics such as the surface potential, electric field, BTBT rate of electrons, energy band diagram, transfer characteristics, output characteristics, etc.

3. To optimize the device characteristics for various high-k dielectrics (for HD engineering scheme) and gate metal work functions (for GME engineering scheme).

4. To examine the viability and applicability of the device at RF and microwave frequencies (regarding various power gains and RF FOMs) that are the fundamental requisite for an RFIC designer for wireless communication and RF applications. This would strengthen the applicability of device for HF wireless communications.

5. To investigate the device reliability in terms of interface trap charge polarity and density in terms of various analog and RF performance metrics for high-performance CMOS applications.

6. To overlap the gate metal near drain side on HD-GAA-TFET for reducing ambipolar conduction along with higher I_{ON}.

7. To examine the device robustness at the wide temperature range needed in some extreme conditions (where the operating temperature is different from the nominal room temperature) such as the furnace temperature control, satellite communications, military, aerospace, automobile, nuclear sectors. This can serve as a worthy design tool for circuits operating at a wide range of temperatures.
8. To design a highly sensitive Hydrogen Gas Sensor by integrating the merits of BTBT mechanism, offered by TFET and to analyze the performance of the sensor at various gas pressure range at elevated temperatures. The successful utilization of HD-GAA-TFET in gas sensors may open a new door for the development of novel nanostructure gas sensing devices.
9. To integrate the merits of various engineering schemes such as n^+ source pocket and gate-drain underlapping for acquiring a comprehensively upgraded TFET with higher I_{ON}, lower V_{th} and lower I_{AMB}.

The major perspective behind these objectives is to design a new TFET device that may simultaneously overcome the challenges faced by conventional TFET and thereby make it an eligible candidate for applicability in various low power, high switching speed, digital, analog and RF applications. Further, the proposed devices are examined for better reliability and also its applicability for temperature sensitive environment.

1.7 THESIS OVERVIEW

This thesis is organized into seven chapters to accommodate all the research objectives. Each chapter is organized to be fundamentally self-contained. The references to each chapter are listed at the end of the respective chapter.

Chapter 1 describes the shortcoming of the MOSFET and the need of TFETs. Thereafter, the chapter progresses towards the basic working principle of TFET, its potential advantages and drawbacks, a brief comparison of MOSFET and TFET. The ambipolar conduction of TFET for negative gate voltages is also discussed. Further, the possible solutions that are reported in different research articles have been presented that overcome the roadblocks of TFET. In this regard, various reported device engineering schemes such as heterostructure TFET, high-k dielectric TFET, hetero gate dielectric TFET, dual material gate

(or gate metal engineering) TFET, n^+ source pocket TFET, asymmetric source/drain doped TFET, gate metal underlapping and overlapping, multi-gate TFET such as double gate and gate all around TFET has been discussed. The chapter continues to discuss the reliability issues of TFET such as the origin of interface traps and precisely the reliability of TFET. Thereafter, the research gaps found during the literature survey have been discussed that is continued with the major objective of the thesis. Lastly, the overall organization of the thesis along with the importance of the research work presented in this thesis is discussed.

Chapter 2 discusses the device structure and the default device parameters followed by the simulation approach. Thereafter, the models used in the simulation validated by the experimental data to authorize the simulation setup, is also described. The model validation part is followed by the fabrication process flow of the proposed device that shows the fabrication feasibility of the device. Next, the chapter describes the analytical drain current model for a hetero dielectric – gate metal engineered- gate all around TFET (HD-GME-GAA-TFET). Rest of the chapter examines the developed model to analyze the analog performance of the device for different high-k dielectrics (such as Si_3N_4, HfO_2, and ZrO_2). Moreover, the impact of scaling the gate oxide thickness and bias variations has also been demonstrated. Further, to optimize the effect of metal work function on analog performance, three different combinations of GME configurations have been studied *(Madan et al., 2015, Madan et al., 2017a).*

Chapter 3 investigates the effect of gate metal work function engineering (GME), gate bias and drain bias on the bias dependent parasitic capacitances of HD-GME-GAA-TFET. Moreover, various RF Figure of Merits (FOMs) such as power gains, cut-off frequency (f_T), maximum oscillation frequency (f_{Max}) and intrinsic delay of HD-GME-GAA-TFET are studied and are compared with HD-GAA-TFET. The motivation of analyzing the parasitic capacitances of HD-GME-GAA-TFET is the entirely different switching mechanism of TFET. So, for the design of the circuits containing TFETs, the understanding of these capacitances is important. Moreover, the response time, switching speed and active power dissipation ($C_{gg}V_{dd}^2 f$) are interdependence on various parasitic capacitances and thus the parasitic capacitances along with the RF FOMs are examined for the variation of both gate and drain bias. To analyze the effect of gate metal work function, the dielectric constant of

oxide for heterogeneous gate dielectric is kept constant throughout the simulation. The admittance parameters have also been discussed in latter part of this chapter. This study indicates that HD-GME-GAA-TFET is a promising candidate for RF/microwave applications *(Madan et al., 2017b).*

Chapter 4 explores the reliability issues of HD-GAA-TFET. In this regard, the impact of interface traps both donor (positive interface charges) and acceptor (negative interface charges) present at the Si-SiO_2 interface, on analog/RF performance and linearity distortion analysis of HD-GAA-TFET is examined. Additionally, to account for the temperature associated reliability issues of HD-GAA-TFET, the effect of ITCs at various operating temperatures on the device analog parameters and RF FOMs has been illustrated. Various RF FOMs and linearity parameters such as cut off frequency f_T, maximum oscillation frequency f_{Max}, transconductance frequency product (TFP), higher order transconductance coefficients (g_{m1}, g_{m3}), V_{IP2}, V_{IP3}, IIP3, IMD3, zero crossover point and 1dB compression point has been investigated and the results so obtained are simultaneously compared with GAA-TFET. Thus, this chapter provides the detailed knowledge about the reliability and robustness of device *(Madan and Chaujar, 2016b, Madan and Chaujar, 2017c).*

Chapter 5 consists of 2 parts. Part-I of the chapter focus on the major impediments of TFET such as inherent I_{AMB} and the lower I_{ON}. To account for the ambipolar conduction, gate-drain overlap (GDO) engineering scheme has been incorporated over the cylindrical GAA-TFET. Additionally, to enhance the I_{ON}, hetero gate dielectrics (HD) are used in the gate oxide region. Thereby, an amalgamated GDO-HD-GAA-TFET has been explored in the part-I of the chapter. Later stage of part-I illustrates an optimization of GDO length, i.e., the effect of GDO length (L_{ov}) has also been studied. Part-II of the chapter, proposes a Palladium metal gate based HD-GAA-TFET hydrogen gas sensor; the motivation behind H_2 sensing, the basis of sensing and the simulation approach is described in detail. Thus, in part-II of the chapter, a novel highly sensitive HD-GAA-TFET based Hydrogen Gas Sensor, incorporating the advantages of the BTBT mechanism has been reported. The conduction path of the sensor which is dependent on sensors radius has also been varied for the optimized sensitivity and static performance analysis of the sensor. Stability of the sensor concerning temperature affectability has also been studied. The successful utilization of HD-GAA-TFET in gas

sensors may open a new door for the development of novel nanostructure gas sensing devices *(Madan and Chaujar, 2016a, Madan and Chaujar, 2016c).*

Chapter 6 is divided into two parts. Part-I aims to overcome the major roadblocks of TFET. In this regard, the merits of gate-drain underlapping (GDU) and n^+ source pocket are integrated on cylindrical GAA-TFET to form GDU-PNIN-GAA-TFET. The aim of implanting an n^+ source pocket at the source-channel junction is to enhance the I_{ON} of GAA-TFET. Additionally, by integrating GDU, the ambipolar conduction is suppressed, and the parasitic capacitances of GAA-TFET are reduced parallelly. Consequently, the amalgamated merits of both engineering schemes are obtained in GDU-PNIN-GAA-TFET that thus conquers the greatest challenges faced by TFET; has also been proposed in this chapter. After analyzing the analog and RF performance of the GDU-PNIN-GAA-TFET, the reliability of PNIN-GAA-TFET has been investigated in Part-II of the chapter. To examine the reliability of PNIN-GAA-TFET; 1) the impact of interface trap charge (ITC) density and polarity and 2) the temperature affectability on analog/RF performance of the device has been explored. The results so obtained can be served as a worthy design tool for circuits operating at a wide range of temperatures *(Madan and Chaujar, 2017a, Madan and Chaujar, 2017b).*

Chapter 7 summarizes the overall research work illustrated in this thesis along with the concrete conclusions drawn from the results presented in this thesis. This chapter also discusses the future scope of the present work and how can this work be extended and used in future for further research directions.

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CHAPTER 2

ANALYTICAL MODELING AND SIMULATION OF HD-GME-GAA-TFET FOR ELECTRICAL AND ANALOG PERFORMANCE

This chapter focus on developing an analytical drain current model for a gate dielectric engineered (Hetero Dielectric) – dual material gate (Gate Metal Engineered) - Gate All Around Tunnel Field Effect Transistor (HD-GME-GAA-TFET). In this respect, parabolic approximation is used to solve the 2-D Poisson's equation with appropriate boundary conditions and continuity equations; with an aim to derive analytical expressions for surface potential, electric field, tunneling barrier width and drain current. The developed model is used to examine the electrical and analog performance parameters such as subthreshold swing (SS), threshold voltage (V_{th}), transconductance (g_m), drain conductance (g_d), device efficiency (g_m/I_{ds}), intrinsic gain (g_m/g_d), channel resistance (R_{ch}) and output resistance (R_o). The analytical results acquired from the proposed model show good agreement with the simulated results obtained with the ATLAS device simulator. Further, the analog performance of the device is examined for altered dielectrics near source side (Si_3N_4, HfO_2 and ZrO_2), and it has been found that the problem of lower I_{ON}, can be overcome by using the hetero-gate engineering scheme. Additionally, the impact of scaling gate oxide thickness and bias variations has also been investigated. Further, after optimizing the dielectrics in hetero gate dielectric engineering scheme, the metal work functions in gate metal engineering scheme has been tuned to optimize the gate metal work function for better analog performance. In this respect, various combinations of GME configurations have been studied. The results demonstrated that for a gate metal with work function of 4.3eV and 4.8eV near source and drain side, and a dielectric of HfO_2 near source and SiO_2 near drain, the analog performance of the device is optimized for improved performance. Low OFF-current and high value of ON-current resulting in a higher I_{ON}/I_{OFF} ratio has been obtained, which is appropriate for sub-nanometre devices and low standby power applications.

2.1 INTRODUCTION

Unceasingly scaling down the MOSFETs dimensions to the sub-nanometer region during the last few decades lead to an escalation in the power consumption (active and passive) in modern microelectronic circuits. Reducing the applied bias (according to the scaling factor) to solve this dilemma leads to reduction in gate overdrive. Along with higher power density, the fundamental limit of kT/q (due to thermal process) which corresponds to a subthreshold swing (SS) of 60mV/dec hinders further scaling of V_{th} and OFF-current. To overcome these boundaries, there is a renewed interest in exploring new devices that uses a new current mechanism, and does not involve carriers traveling over a potential barrier. Among various new devices Tunnel Field Effect Transistor (TFET) has been studied extensively in the past few years. TFET relies on the band to band tunneling (BTBT) mechanism at the tunneling junction (the source channel junction) and normal drift-diffusion mechanism away from the tunneling junction *(Cho et al., 2011)*. TFET has established the potential to prevail the SS limit of MOSFETs and acts as a capable candidate for further extending the Moore's law as discussed in **Chapter 1** *(Aydin et al., 2004, Bhuwalka et al., 2006, Choi et al., 2007)*. Due to BTBT tunneling mechanism, TFETs are able to operate as steeper switches at lower supply voltages. Along with ultra-low SS, TFETs also have very low I_{OFF} and lessened short channel effects (SCE) due to the built-in tunneling barrier width. Lower I_{OFF} of TFET leads to higher I_{ON}/I_{OFF} and hence, improves the device performance. Therefore, TFET seems to be a well adaptive candidate for ultimately scaled switches and low standby power devices with excellent immunity to SCEs *(Born et al., 2006, Mookerjea et al., 2009, Nirschl et al., 2006)*. However, TFET also suffers from few challenges that act as the major roadblock for its practical applicability. The major obstruction with TFET is its lower ON-current (I_{ON}), ambipolar conduction and the higher V_{th} *(Madan et al., 2015b)*.

The major impediment with the planar TFETs is caused by the small amount of BTBT at the source channel junction i.e. the lower I_{ON} (lower than the ITRS requirement), which results in lower operating speed. In order to enhance the tunneling rate or to enhance the I_{ON}, numerous kinds of TFETs with various structures and materials such as double-gate *(Boucart and Ionescu, 2007a)*, delta layer of SiGe at the edge of the source *(Bhuwalka et al., 2004)*, SiGe *(Shih and Chien, 2011)*, a high-k gate dielectric *(Boucart and Ionescu, 2007a)* dual material gate *(Saurabh and Kumar, 2011)*, a thin silicon body *(Toh et al., 2007)*, low-k spacer *(Anghel et al., 2010)* and a p-n-p-n TFET with a heavily doped fully depleted pocket region in

between source and channel *(Jhaveri et al., 2011)* have been reported as briefly described in **Chapter 1**. Thus, the major engineering challenge with TFET is to boost the lower I_{ON} without degrading the I_{OFF}.

Another major challenge with TFET is ambipolar conduction *(Shaker et al., 2015, Wang et al., 2004)* which means conduction in two directions, both for positive and negative gate voltages while keeping the V_{ds} only in one direction (negative for p-type devices and positive for n-type devices). To reduce the ambipolar conduction, many methods are reported such as: the hetero gate dielectric (HD) TFET *(Choi and Lee, 2010),* asymmetric source/drain doping *(Wang et al., 2004),* gate-drain underlap or short gate TFET *(Verhulst et al., 2007),* and hetero-junction TFET *(Hanna et al., 2015)* as described in **Chapter 1**. Further, to resolve the issue of high V_{th}, many structures such as: tunnel bandgap modulation, gate work function engineering, vertical TFET with SiGe delta-doped layer, high-k gate dielectric with double gate, higher source doping and abrupt doping profile were proposed.

To improve I_{ON}, tunneling rate at the source channel junction must be increased. It is reported that tunneling rate can be increased by using a high-k dielectric (over the entire gate length) which basically improves the electrical coupling between the gate and the tunneling junction (the source-channel junction) due to increase in gate capacitance *(Boucart and Ionescu, 2007a).* Although by using high-k over the entire gate length results in improved I_{ON}, but the major issue with high-k dielectric TFET is increase in I_{OFF} and the ambipolar current. Thus, to conquer this issue, the hetero gate dielectric (HD) TFET was proposed by *(Choi and Lee, 2010)* in which a high-k dielectric material is located near the source side and low-k dielectric is placed near drain side as depicted in **Figure 1.3** on page 10 in **Chapter 1** *(Mallik and Chattopadhyay, 2011).* The presence of high-k dielectric near source side leads to higher band bending that reduces the minima of conduction band and hence, the tunneling barrier width. Reduced barrier width leads to higher tunneling rate and thereby enhances the drain current. Thus, the use of high-k at the source side increases the I_{ON} and with low-k dielectric such as SiO_2 improves the OFF-state characteristics and also reduces the ambipolarity. As by using a HD-TFET both I_{ON} and ambipolarity can be improved hence, we have chosen HD architecture to improve the analog characteristics of the TFET in this chapter. Additionally, the concept of gate metal engineered (GME) namely dual material gate was proposed by *(Saurabh and Kumar, 2011),* to enhance the drain current of TFET. In GME a metal with high metal work function is used near drain side and a comparatively lower work function metal is

used near source side as shown in **Figure 1.2** on page 9 in **Chapter 1**. The lower metal work function near source side increases the band overlap in the ON-state. This increased band overlap results into lowering of the tunneling barrier width, which further results into increase in the tunneling probability of electrons from valence band (VB) of the source to the conduction band (CB) of the channel and thus, enhances the tunneling drain current. These electrons after tunneling from source to channel move towards drain side by drift diffusion. Simultaneously, the higher metal work function near the drain side increases the tunneling barrier width at the drain channel junction in the OFF state and hence reduces the tunneling probability at the drain channel junction which eventually decreases the I_{OFF} and also controls the ambipolar conduction *(Pandey et al., 2015, Vishnoi and Kumar, 2014)*. The GME-TFET improves the ON and OFF-state characteristics simultaneously. However, the value of metal work function value at source and drain side should be chosen so as to acquire an optimum ON and OFF characteristics.

The GME offers lower SS and lower I_{OFF} and it was reported that a GME with high-k dielectric TFET results in very low SS, lower V_{th} and lower leakage current *(Cui et al., 2011)*. It however, suffers from high ambipolar current. To overwhelm ambipolar conduction, HD-TFET was reported which has a high I_{ON} and reduced ambipolar conduction but it offers higher SS. Hence, individual GME and HD engineering are not adequate to overcome the challenges faced by TFET. Consequently, the key idea of this chapter is to amalgamate both the GME and HD, in a single TFET. Furthermore, to enhance the I_{ON}, silicon nanowire TFET has already been fabricated *(Gandhi et al., 2011a, Gandhi et al., 2011b)*. These nanowires TFET have better electrostatic control over the channel and also results in higher tunneling rate of electrons. Thus, with an anticipation of the combined advantages of BTBT and gate all around geometry for improved device characteristics; GAA-TFET is analyzed throughout the thesis. In this chapter, a heterogate dielectric, gate metal engineered, gate-all-around structure has been integrated onto TFET namely HD-GME-GAA-TFET, to acquire an improved analog performance of the device and an analytical drain current model is developed for the same.

This chapter is structured as follows: First part of the chapter describes the device structure, structural parameters and simulation models used in this work. The second part of the chapter shows the calibration of the models used in the simulation setup with the experimental reported data and thereby shows the validation of the simulation setup. Next part of the chapter describes the fabrication feasibility of the proposed device. The chapter

continues to describe the analytical model formulation of the proposed device in the succeeding section. Later part of the chapter describes the results obtained via simulation and the developed model, in which the effect of gate and drain bias, high-k dielectric for hetero gate dielectric scheme, gate oxide thickness and the gate metal work function for gate metal engineered scheme; on the electrical and analog performance of HD-GME-GAA-TFET is discussed. Finally, the summary of the chapter is drawn in the last section.

2.2 DEVICE STRUCTURE AND PARAMETERS

The simulated device structure i.e. HD-GME-GAA-TFET consisting of gate metal engineered and heterogate dielectric and its cut plane view respectively are shown in **Figures 2.1(a)-(b).** The device structural parameters and their values are listed in **Table 2.1**. During the simulation, silicon is used as source, channel and drain material. Cylindrical gate all around structure with channel radius (R) = 10nm, channel length L_g (=L_1+L_2) = 50nm (=20nm+30nm) and gate oxide thickness (t_{ox}) = 3nm is used. The source is p^+ type doped ($10^{20}cm^{-3}$); body is lightly p-type doped ($10^{16}cm^{-3}$) and drain is n^+ doped (5×10^{18} cm^{-3}). To reduce ambipolarity effect (tunneling at drain and channel junction), source and drain are doped asymmetrically *(Wang et al., 2004)*. All simulations have been performed using the ATLAS device simulator *(Manual, 2010)*. The source and drain junctions are abruptly doped for an effective BTBT and the interface of high-k and SiO_2 is abrupt.

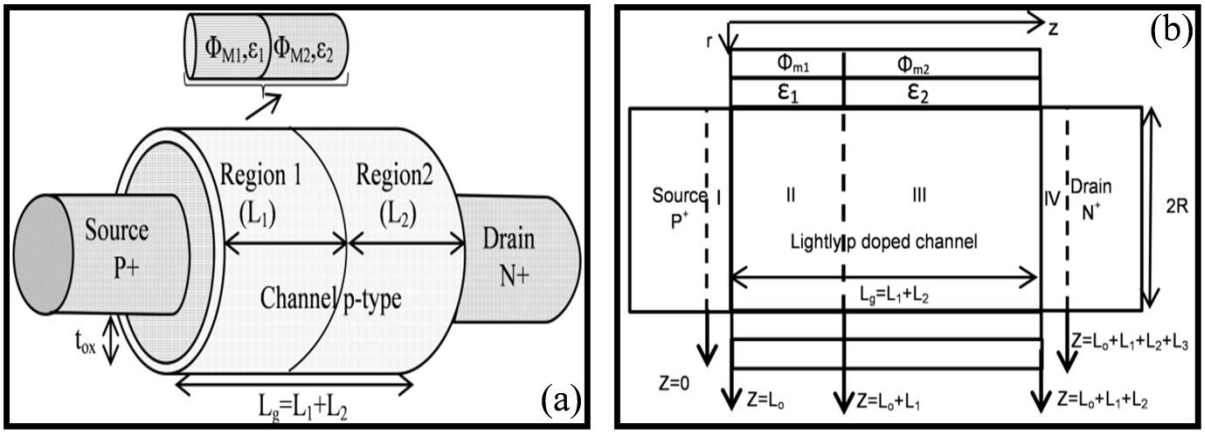

Figure 2.1 Structure of n-type Heterogate Dielectric- Gate Metal Engineered-Gate all Around-Tunnel FET (HD-GME-GAA-TFET) (a) simulated 3D view (b) schematic two-dimensional cross-sectional view *(Madan et al., 2015a, Madan et al., 2016)*.

TABLE 2.1

DEVICE GEOMETRICAL PARAMETERS AND THE DEFAULT VALUES USED IN THE ANALYSIS (MADAN ET AL., 2015A).

Parameter symbol	Technology parameter	Value
L	Channel Length	50nm
R	Channel radius	10nm
$\mathbf{t_{ox}}$	Gate oxide thickness	3nm
$\mathbf{N_s}$	Source doping (P^+)	$10^{20}cm^{-3}$
$\mathbf{N_{ch}}$	Channel doping lightly p-type	$10^{16}cm^{-3}$
$\mathbf{N_d}$	Drain doping (N^+)	$5\times10^{18}cm^{-3}$
$\boldsymbol{\varepsilon_1}$	Dielectric constant of region 1	21
$\boldsymbol{\varepsilon_2}$	Dielectric constant of region 2	3.9
$\boldsymbol{\Phi_{m1}}$	Metal work function of region 1	4.1eV
$\boldsymbol{\Phi_{m2}}$	Metal work function of region 2	4.4eV
$\mathbf{L_1}$	Length of region 1	20nm
$\mathbf{L_2}$	Length of region 2	30nm

The models activated during simulation are: concentration and field dependent mobility model, Shockley-Read-Hall (SRH) for carrier recombination, non-local BTBT, band gap narrowing (BGN) and Fermi Dirac statistics *(Biswas et al., 2012)*. Shockley Read Hall (SRH) Recombination also called trap-assisted recombination is used to incorporate minority recombination effects with carrier lifetime (TAUP0 = 1×10^{-7}s). This process is the dominant generation and recombination process in silicon and other indirect bandgap materials. Moreover, the carrier transport model used in this work is drift-diffusion, which solves the Poisson's and current continuity equations self-consistently. Instead of Boltzmann statistics, the Fermi-Dirac statistics is used in this work so as to account the effect of heavily doped (degenerate) materials (source and drain in this work), such as reduced carrier concentrations in heavily doped regions (statistical approach). Moreover, the experimental work has shown that the p-n product in silicon becomes doping dependent for higher doping ($> 10^{18}cm^{-3}$); generally a decrease in bandgap is found at higher doping levels *(Slotboom, 1977)*. To incorporate such effects, the BGN model is invoked in the simulation. Moreover, as tunneling current have strong band gap dependence and the band gap of semiconductor reduces for heavily doped semiconductors; thus, the BGN model is employed to consider the effects of degenerately doped source/drain. The most significant model for TFET simulations is the BTBT model. A non-local model is chosen in this work instead of local model, to incorporate the effect of electric field at each point in the tunneling path. In local models such as Kane's

model, the triangular barrier approximation of energy bands results into constant electric field at the entire tunneling path *(Biswas et al., 2012)*. However, the non-local BTBT incorporates the dynamic changes in the electric field at each point in the entire tunneling path and thus depends upon the band edge profile in the tunneling path. Thus, the non-local BTBT that calculates the generation rate at each mesh point in the tunneling region and thereby the non-local BTBT model have a more physical basis as the field changes at each point in the tunneling path. According to non-local BTBT, the tunneling happens through the 1D slice, at the tunnel junction, where each slice and the tunnel junction are perpendicular to each other. These slices are parallel to themselves. For non-local BTBT model, the quantum tunneling meshing has been used at the source-channel junction. In n-TFET, the electrons tunnel through the VB of the source to CB of the channel by BTBT mechanism and then the carriers drift from channel to drain. Thus, to incorporate the transport away from the tunneling junction, drift-diffusion model is used *(Boucart and Ionescu, 2007b)*. Thus, to account the spatial variation dependence of electric field on energy bands, the nonlocal BTBT model is considered, that takes into account the electrons energy for evaluating electric field at the individual mesh points in the simulated device structure, rather assuming a constant electric field as in local BTBT models such as Kane model *(Biswas et al., 2012)*. Thus, more realistic results have been obtained by incorporating the nonlocal BTBT model. The source and drain junctions are abruptly doped for an effective BTBT. Besides, Gummel (decoupled) and Newton (Fully coupled) has been utilized to numerically solve the carrier transport equation.

2.3 MODEL VALIDATION

For simulating the device structure, a well-calibrated TCAD setup has been used to calibrate the simulation models with the already published experimental results *(Chen et al., 2009)*. In this respect, the GAA-TFET is designed with the same structural device parameters as by Chen at al. For calibrating the Non-local BTBT model, the tunneling masses were adjusted from their default values i.e. m_e.tunnel=0.322m_o and m_h.tunnel=0.549m_o to make it finest fit with the experimental data *(Chen et al., 2009)*, where, m_o is the rest mass of the electron, the adjusted value of m_e.tunnel=0.22m_o and m_h.tunnel=0.52m_o. In simulation, the value of effective tunneling mass has been set on the material statement for silicon material used in source, channel and drain. The tuning of the effective tunneling masses is mainly attributed to the fact that tunneling probability depends exponentially on electron and hole

tunneling masses. Moreover, reduced electron tunneling mass enhances the tunneling probability and thus, the drain current. The calibration of simulation models with experimental data for transfer characteristics shows close proximity as evident from **Figure 2.2**, hence, validates the choice of model parameters considered in simulation setup *(Chen et al., 2009)*.

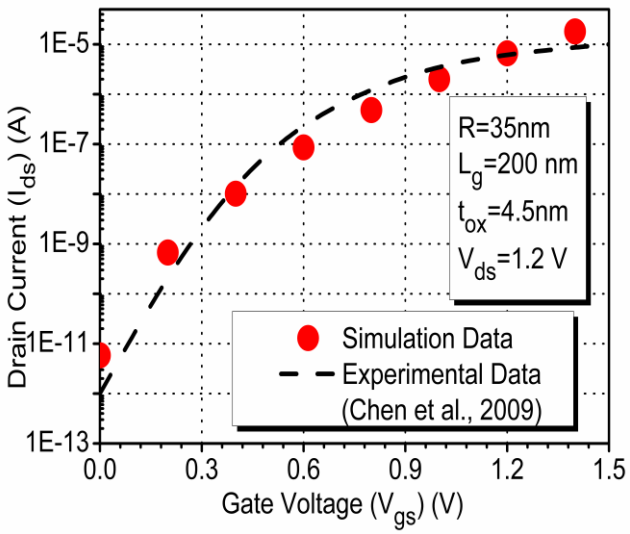

Figure 2.2 Comparison of experimental published results *(Chen et al., 2009)*, and simulated I_{ds}-V_{gs} characteristics of 200nm gate length SiNW-TFET at V_{ds}=1.2V, T_{ox}=4.5nm, diameter=70nm of GAA-TFET.

2.4 FABRICATION PROCESS FLOW OF HD-GME-GAA-TFET

The proposed summary of fabrication process flow for HD-GME-GAA-TFET is shown in **Table 2.2**. The fabrication feasibility of GAA-TFET has already been reported in several literatures such as *(Chen et al., 2009)* fabricated vertical silicon nanowire TFET, *(Gandhi et al., 2011a, Gandhi et al., 2011b)* fabricated both vertical Si-nanowire n-type and p-type TFET. Furthermore, for the realization of GME architecture, various schemes have been reported such as tilt angle evaporation technique *(Long et al., 1999)*, metal interdiffusion process *(Polishchuk et al., 2001)*. Thus, the HD-GME-GAA-TFET can be fabricated using the above device design schemes, in which the benefits of HD and GME engineering scheme have been combined with GAA-TFET for accomplishing improved characteristics.

TABLE 2.2

SUMMARY OF FABRICATION PROCESS FLOW FOR HD-GME-GAA-TFET IMPLEMENTATION *(BROUZET ET AL., 2015, CHOI AND LEE, 2010, LONG ET AL., 1999, VALLETT ET AL., 2010)*.

- Starting material- SiNW grown by CVD-VLS using Gold colloid particles as catalysts in low pressure CVD reactor (Vallett et al. 2010)

⇩

- Axially doping for p- (source) using diborane B_2H_6 gas and n- (drain) using phosphine PH_3 type-segments (Vallett et al. 2010)

⇩

- Suspend axially doped SiNW ultrasonically in an isopropanol solution and transfer it to a silicon wafer covered with oxide for isolation (Brouzet et al. 2015)

⇩

- Define source and drain contacts using optical lithography; Metallize contacts using electron beam evaporator (Brouzet et al. 2015)

⇩

- Deposit $SiO_2$by atomic layer deposition at 250° C(Brouzet et al. 2015)

⇩

- Hetero gate dielectric layer is formed by isotropic etching SiO_2 followed by deposition of high-k material (Choi et al. 2010)

⇩

- Deposit the tunneling gate using precise tilt angle evaporation technique and auxiliary gate by normal evaporation technique (Long et al. 1999)

⇩

- HD-GME-GAA-TFET is formed.

Continue processing

2.5 MODEL FORMULATION FOR HD-GME-GAA-TFET

This section of the chapter focuses on developing an analytical drain current model for the proposed device i.e. Heterogate Dielectric– Gate Metal Engineered - Gate All Around TFET i.e. HD-GME-GAA-TFET. In this regard, the parabolic approximation is used to solve the 2-D Poisson equation with appropriate boundary conditions and continuity equations to evaluate analytical expressions for surface potential, electric field, tunneling barrier width and drain current.

Assuming that the influence of the charge carriers and fixed carriers are uniform in the channel, it can be neglected. The Poisson's equation can be written as

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{\partial \psi_{Si}(r,z)}{\partial r}\right)+\frac{\partial^2 \psi_{Si}(r,z)}{\partial z^2}=\frac{qN_i}{\varepsilon_{Si}} \tag{2.1}$$

Where, $\psi_{si}(r, z)$ denotes the surface potential for each region. N_i is N_s, N_{ch}, N_{ch}, N_d for regions i=1, 2, 3, 4 respectively. ε_{si} is the permittivity of silicon. Further, the parabolic potential profile along the radial direction is assumed.

$$\psi_{Si}(r,z) = A_{0i}(z) + A_{1i}(z)r + A_{2i}(z)r^2 \tag{2.2}$$

The following boundary conditions are applied to evaluate the coefficients A_{0i}, A_{1i} and A_{2i}.

1). The surface potential is only z-dependent

$$\psi_{si}(R,z) = \psi_{si}(z) \tag{2.3}$$

2). The electric field at the center of the channel is zero

$$\left.\frac{d\psi_{si}(r,z)}{dr}\right|_{r=0} = 0 \tag{2.4}$$

3). Electric field at Si/SiO_2 interface is continuous

$$\left.\frac{d\psi_{si}(r,z)}{dr}\right|_{r=R} = \frac{C_{fi}}{\varepsilon_{si}}\left[V_{GS} - \psi_{si}(z) - V_{FBi}\right] \tag{2.5}$$

After applying the boundary conditions, we get;

$$A_{0i}(z) = \psi_{Si}(z) - A_{2i}(z)R^2 \tag{2.6a}$$

$$A_{1i}(z) = 0 \tag{2.6b}$$

$$A_{2i}(z) = \frac{C_{fi}}{2R\varepsilon_{si}}\left[V_{gs} - \psi_{si}(z) - V_{FBi}\right] \tag{2.6c}$$

Where; C_{fi} (Gate capacitance per unit area of the gate dielectric) and V_{FBi} (flatband voltage) of each region are given in Equations 2.7(a-d)-2.10(a-d) as follows.

For i=1, (depletion region of source $0 \le z \le L_0$)

$$C_{f1} = \frac{2}{\pi}\frac{\varepsilon_1}{R\ln\left(1+\frac{t_{ox}}{R}\right)}, \tag{2.7a}$$

$$V_{FB1} = \phi_{m1} - \phi_{s1}, \tag{2.7b}$$

$$\phi_{s1} = \chi_{Si} + \frac{E_g}{2q} + \phi_{F1}, \tag{2.7c}$$

$$\phi_{F1} = \frac{k_B T}{q}\ln\left(\frac{N_s}{n_i}\right) \tag{2.7d}$$

For i=2, (tunneling region $L_0 \le z \le L_1$)

$$C_{f2} = \frac{\varepsilon_1}{R\ln\left(1+\frac{t_{ox}}{R}\right)}, \tag{2.8a}$$

$$V_{FB2} = \phi_{m1} - \phi_{s2}, \tag{2.8b}$$

$$\phi_{s2} = \chi_{Si} + \frac{E_g}{2q} + \phi_{F2}, \tag{2.8c}$$

$$\phi_{F2} = \frac{k_B T}{q} \ln\left(\frac{N_{ch}}{n_i}\right) \tag{2.8d}$$

For i=3, (remaining channel $L_1 \leq z \leq L_2$)

$$C_{f3} = \frac{\varepsilon_2}{R \ln\left(1 + \frac{t_{ox}}{R}\right)}, \tag{2.9a}$$

$$V_{FB3} = \phi_{m2} - \phi_{s2}, \tag{2.9b}$$

$$\phi_{s2} = \chi_{Si} + \frac{E_g}{2q} + \phi_{F2}, \tag{2.9c}$$

$$\phi_{F2} = \frac{k_B T}{q} \ln\left(\frac{N_{ch}}{n_i}\right) \tag{2.9d}$$

For i=4, (i=4 Depletion region of drain $L_2 \leq z \leq L_3$)

$$C_{f4} = \frac{2}{\pi} \frac{\varepsilon_2}{R \ln\left(1 + \frac{t_{ox}}{R}\right)}, \tag{2.10a}$$

$$V_{FB4} = \phi_{m2} - \phi_{s3}, \tag{2.10b}$$

$$\phi_{s3} = \chi_{Si} + \frac{E_g}{2q} + \phi_{F3}, \tag{2.10c}$$

$$\phi_{F3} = \frac{k_B T}{q} \ln\left(\frac{N_d}{n_i}\right) \tag{2.10d}$$

Where;

ϕ_{si} is the Si work function,

ϕ_{Fi} is the Fermi potential,

n_i is intrinsic carrier concentration, and

t_{ox} is the gate oxide thickness.

The parameters, symbols and their values used in the analysis are listed in **Table 2.3**.

TABLE 2.3

LIST OF CONSTANT PARAMETERS *(MADAN ET AL., 2016)*

Parameters	Symbol	Value and Unit
Electron affinity	χ_{si}	4.17eV
Permittivity of silicon	ε_{Si}	11.8
Bandgap of silicon,	E_g	1.08eV
Temperature	T	300K
Boltzmann constant	k_B	1.38066×10^{-23} J/K
Elementary charge	q	1.60219×10^{-19} C
Plank's constant	h	6.63×10^{-34} Js

Solving Equations (2.1)-(2.10), we get:

$$\frac{\partial^2 \psi_{si}(z)}{\partial z^2} - k_i^2 \psi_{si}(z) = \beta_i \tag{2.11}$$

The general solution of (2.11) for region i is

$$\psi_{si}(z) = P_i \exp(k_i z) + Q_i \exp(-k_i z) - \frac{\beta_i}{k_i^2} \tag{2.12}$$

$$\text{where } k_i^2 = \frac{2C_{fi}}{R\varepsilon_{Si}} \text{ and } \beta_i = \frac{qN_i}{\varepsilon_{Si}} - k_i^2 \left[V_{gs} - V_{FBi} \right] \tag{2.13}$$

Now using the continuity conditions (given below) at the interface of each region, coefficients P_i and Q_i can be determined.

At the source depletion width end

$$\psi_{s1}(0) = -\frac{k_B T}{q} \ln\left(\frac{N_s}{n_i}\right) = V_{bi1} \tag{2.14a}$$

At the tunneling junction

$$\psi_{s1} = \psi_{s2}\big|_{z=L_0} \text{ and } \frac{d\psi_{s1}}{dz} = \left.\frac{d\psi_{s2}}{dz}\right|_{z=L_0} \tag{2.14b}$$

At the interface of region 1 and 2

$$\psi_{s2} = \psi_{s3}\big|_{z=L_0+L_1} \text{ and } \frac{d\psi_{s2}}{dz} = \left.\frac{d\psi_{s3}}{dz}\right|_{z=L_0+L_1} \tag{2.14c}$$

At the channel and drain junction

$$\psi_{s3} = \psi_{s4}\big|_{z=L_0+L_g} \text{ and } \frac{d\psi_{s3}}{dz} = \frac{d\psi_{s4}}{dz}\bigg|_{z=L_0+L_g} \tag{2.14d}$$

At the drain depletion width end

$$\psi_{s4}(L_0+L_1+L_2+L_3) = \left(\frac{k_B T}{q}\right)\ln\left(\frac{N_d}{n_i}\right) + V_{ds} = V_{bi2} + V_{ds} \tag{2.14e}$$

Where L_0 and L_3 are the length of depletion widths at the source and drain side respectively given as:

$$L_0 = \sqrt{\frac{2\varepsilon_{Si}}{q}\frac{1}{N_{ch}}\frac{k_B T}{q}\ln\left(\frac{N_s N_{ch}}{n_i^2}\right)} \tag{2.15a}$$

$$L_3 = \sqrt{\xi\left[\frac{k_B T}{q}\ln\left(\frac{N_d N_{ch}}{n_i^2}\right) + V_{ds}\right]} - \sqrt{\xi\left[\frac{k_B T}{q}\ln\left(\frac{N_d N_{ch}}{n_i^2}\right) - V_{gs}\right]} \tag{2.15b}$$

where $\xi = 2\varepsilon_{Si} / q\left(1/N_{ch} + 1/N_d\right)$ (2.16)

$$P_1 = \left(-V_{bi1}\gamma_2 - \gamma_2\frac{\beta_1}{k_1^2} + V_{bi2} + V_{ds} - \gamma_3\right)/\left(\gamma_1 - \gamma_2\right) \tag{2.17a}$$

$$Q_1 = \left(V_{bi1}\gamma_1 - V_{bi2} - V_{ds} + \gamma_3 + \frac{\eta_1\gamma_1}{k_1^2}\right)/\left(\gamma_1 - \gamma_2\right) \tag{2.17b}$$

For i = 2, 3, 4

$$P_i = 0.5\left(P_{i-1}\left[1+\frac{k_{i-1}}{k_i}\right]e^{\left(-k_i+k_{i-1}\right)\left[\sum_{j=0}^{i-2}L_j\right]} + Q_{i-1}\left[1-\frac{k_{i-1}}{k_i}\right]e^{\left(-k_i-k_{i-1}\right)\left[\sum_{j=0}^{i-2}L_j\right]} + \left[\frac{\beta_i}{k_i^2}-\frac{\beta_{i-1}}{k_{i-1}^2}\right]e^{-k_i\left(\sum_{j=0}^{i-2}L_j\right)}\right) \tag{2.17c}$$

$$Q_i = 0.5\left(P_{i-1}\left[1-\frac{K_{i-1}}{K_i}\right]e^{\left(K_i+K_{i-1}\right)\left[\sum_{j=0}^{i-2}L_j\right]} + Q_{i-1}\left[1+\frac{K_{i-1}}{K_i}\right]e^{\left(K_i-K_{i-1}\right)\left[\sum_{j=0}^{i-2}L_j\right]} + \left[\frac{\beta_i}{K_i^2}-\frac{\beta_{i-1}}{K_{i-1}^2}\right]e^{K_i\left(\sum_{j=0}^{i-2}L_j\right)}\right) \tag{2.17d}$$

where $\lambda_1 = e^{k_4(L_0+L_1+L_2+L_3)}$ and $\lambda_2 = e^{-k_4(L_0+L_1+L_2+L_3)}$ (2.18a)

$$\alpha_1 = 0.5\,e^{k_3(L_0+L_g)}\left[\lambda_1 e^{-k_4(L_0+L_g)}\left[1+k_3/k_4\right] + \lambda_2 e^{k_4(L_0+L_g)}\left[1-k_3/k_4\right]\right] \tag{2.18b}$$

$$\alpha_2 = 0.5\,e^{-k_3(L_0+L_g)}\left[\lambda_1 e^{-k_4(L_0+L_g)}\left[1-k_3/k_4\right] + \lambda_2 e^{k_4(L_0+L_g)}\left[1+k_3/k_4\right]\right] \tag{2.18c}$$

$$\alpha_3 = \left[0.5\lambda_1\,e^{\left(-k_4(L_0+L_1+L_2)\right)} + 0.5\lambda_2\,e^{\left(k_4(L_0+L_1+L_2)\right)}\right]\left[\beta_4/k_4^2 - \beta_3/k_3^2\right] - \beta_4/k_4^2 \tag{2.18d}$$

$$\sigma_1 = 0.5\left[\alpha_1 e^{(k_2-k_3)(L_0+L_1)}\left[1+k_2/k_3\right]+\alpha_2 e^{(k_2+k_3)(L_0+L_1)}\left[1-k_2/k_3\right]\right] \tag{2.18e}$$

$$\sigma_2 = 0.5\left[\alpha_1 e^{(-k_2-k_3)(L_0+L_1)}\left[1-k_2/k_3\right]+\alpha_2 e^{(-k_2+k_3)(L_0+L_1)}\left[1+k_2/k_3\right]\right] \tag{2.18f}$$

$$\sigma_3 = 0.5\left(\frac{\beta_3}{k_3^2}-\frac{\beta_2}{k_2^2}\right)\left(\alpha_1 e^{-k_3(L_0+L_1)}+\alpha_2 e^{k_3(L_0+L_1)}\right)+\alpha_3 \tag{2.18g}$$

$$\gamma_1 = 0.5\left[\sigma_1\left(1+k_1/k_2\right)\mathrm{e}^{(k_1-k_2)L_0}+\sigma_2\left(1-k_1/k_2\right)\mathrm{e}^{(k_1+k_2)L_0}\right] \tag{2.18h}$$

$$\gamma_2 = 0.5\left[\sigma_1\left(1-k_1/k_2\right)\mathrm{e}^{(-k_1-k_2)L_0}+\sigma_2\left(1+k_1/k_2\right)\mathrm{e}^{(-k_1+k_2)L_0)}\right] \tag{2.18i}$$

$$\gamma_3 = 0.5\left(\beta_2/k_2^2-\beta_1/k_1^2\right)\left[\sigma_1 e^{-k_2L_0}+\sigma_2 e^{k_2L_0}\right]+\sigma_3 \tag{2.18j}$$

The obtained potential is then used to find the energy band diagram and electric field at the tunneling junction. The lateral electric field (2D) is given by

$$E_z(r,z) = -\frac{d\psi_{si}(r,z)}{dz} \tag{2.19}$$

The lateral surface electric field is given by

$$E_{sz}(r,z) = k_i\left(P_i e^{K_i z}-Q_i e^{-K_i z}\right) \tag{2.20}$$

And transverse electric field (2D) is given as

$$E_{ri}(r,z) = 2rA_{2i}(z) \tag{2.21}$$

Kane's formulation is used for determining the drain current *(Kane, 1960)*. Drain current is obtained by integrating the tunneling generation rate over the volume $\pi r^2 W_T$, where W_T (tunneling barrier width) is the shortest distance (lateral) between VB of the source and CB of the channel. W_T can be determined from the surface potential profile. It is basically the difference between the points where the surface potential falls ~E_g/q below the surface potential and where the potential is Φ_s. The tunneling barrier width is obtained and is given as:

$$w_T = \frac{1}{K_2}\ln\left[\left(\psi_{s2}(z)+\frac{E_g}{q}+\frac{\beta_2}{k_2^2}+\sqrt{\left(\psi_{s2}(z)+\frac{E_g}{q}+\frac{\beta_2}{k_2^2}\right)^2-4P_2Q_2}\right)/2P_2\right] \tag{2.22}$$

With the Kane's model, tunneling generation rate can be evaluated as

$$G(E) = A\left(\frac{E^D}{E_g^{1/2}}\right)e^{\left(\frac{-BE_g^{3/2}}{|E|}\right)} \tag{2.23}$$

Where;

A and B are the parameters of the Kane's model and depends on the effective mass of electron and hole in the CB and VB. The default value of D= 2.

$$A = \left(q^2\sqrt{2m_{tunnel}}\right)/h^2E_g^{1/2} \text{ and } B = \left(\pi^2E_g^{3/2}\sqrt{0.5m_{tunnel}}\right)/qh \tag{2.24}$$

$$1/m_{tunnel} = 1/m_{ee} + 1/m_{eh} \tag{2.25a}$$

Where $m_{ee} = m_e m_0$ and $m_{eh} = m_h m_0$ (2.25b)

Where m_e and m_h are the effective masses of electron and hole respectively, and m_0 is the rest mass of an electron. The average electric field E_{avg} is calculated by integrating the total electric field E_{Tot} over the barrier width W_T as:

$$E_{Tot} = \sqrt{|E_z|^2 + |E_r|^2} \quad \text{and} \quad E_{avg} = \left(\int_{w_T} E_{Tot}dz\right)/w_T \tag{2.26}$$

The expression for drain current (I_{ds}) is then given as:

$$I_{ds} = q\pi R^2 w_T G(E_{avg}) \tag{2.27}$$

2.6 RESULTS VERIFICATION AND DISCUSSION

2.6.1 IMPACT OF GATE AND DRAIN BIAS

This sub-section discusses the influence of gate and drain bias on electrical and analog characteristics of the proposed device i.e. HD-GME-GAA-TFET. **Figure 2.3(a)** represents the surface potential profile of HD-GME-GAA-TFET along the channel length at different V_{gs}. It is depicted that with an increase in V_{gs}, there is an increase in the channel potential which results in higher band bending of the energy bands in the channel. Moreover, it is evidently examined that the model developed is in well agreement with the simulation data that validates the developed analytical model. **Figure 2.3(b)** shows the nonlocal BTBT rate of electron at different V_{gs}. It is examined that at V_{gs}=0.0 V, there is no tunneling of electrons from the VB of source to the CB of channel owing to the large W_T present at the source-channel junction. But, with an increase of V_{gs}, higher band bending in the channel results in lowering of W_T that allows more number of electrons to tunnel through the source-channel junction, and thus increases tunneling rate to an order of 10^{25} (/cm^{3}s)(approx.).

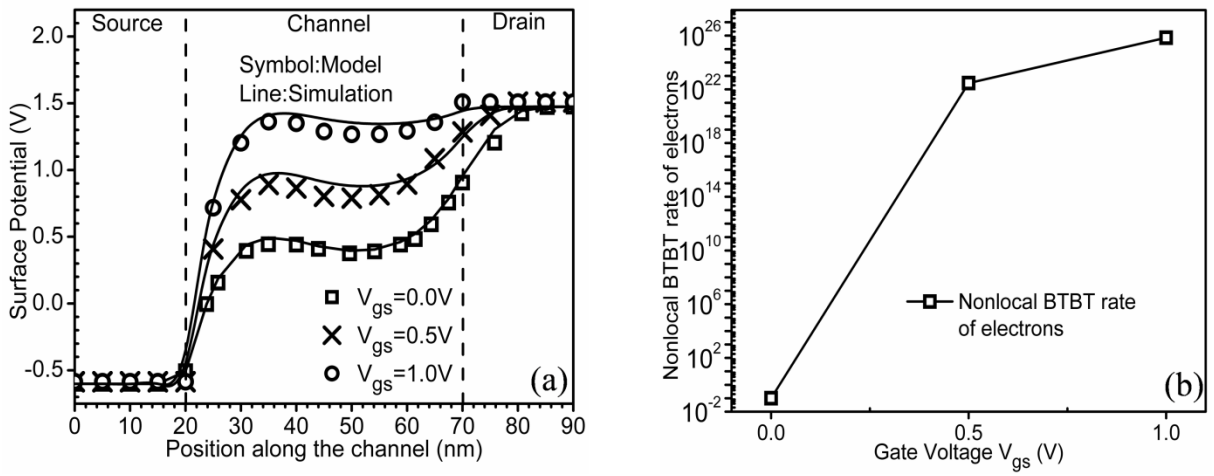

Figure 2.3 (a) Surface Potential along the channel length from source to drain, for V_{gs}=0.0 V, 0.5 V and 1.0 V at V_{ds}=1V. (b) Nonlocal BTBT electron tunneling rate as a function of V_{gs} *(Madan et al., 2015a)*.

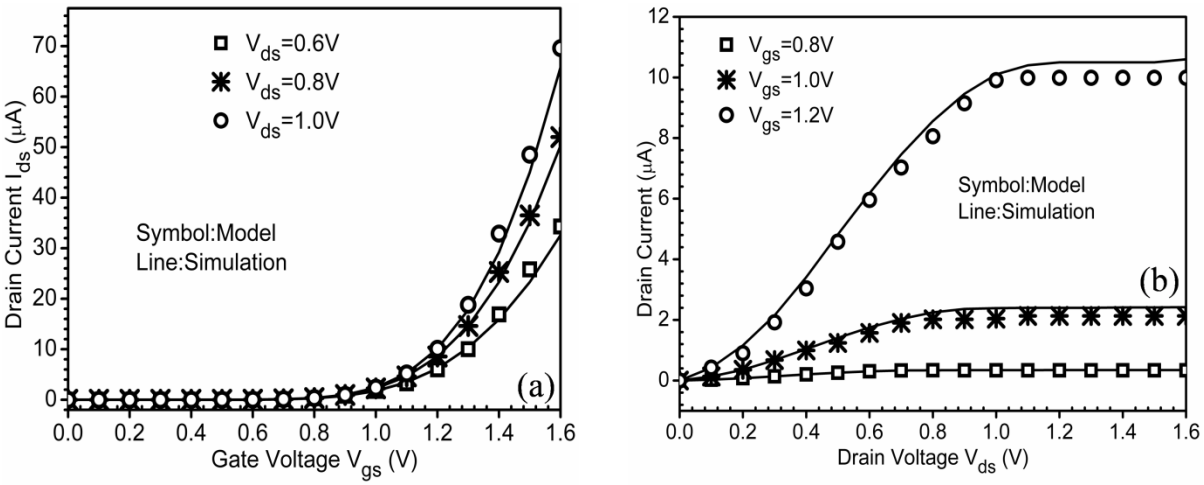

Figure 2.4 Impact of (a) drain bias on transfer characteristics and (b) gate bias on output characteristics *(Madan et al., 2015a)*.

The variations of transfer characteristics at different V_{ds} is shown in **Figure 2.4 (a)**. It is evidently shown in **Figure 2.4(a)** that the tunneling current increases with an increase in V_{gs}. This enhanced drain current is due to the lowering of W_T with rise in V_{gs}, which in turn enhances the tunneling generation rate as discussed for **Figure 2.3(b)** and hence, the drain current. Also the I_{ON} is higher for greater V_{ds}. The impact of V_{gs} on output characteristics is shown in **Figure 2.4(b)**. Again tunneling current increases as the V_{ds} is increased. Additionally, the device shows good saturation at higher V_{ds}. In consistent with previous results, an increase in V_{gs} results in higher tunneling current.

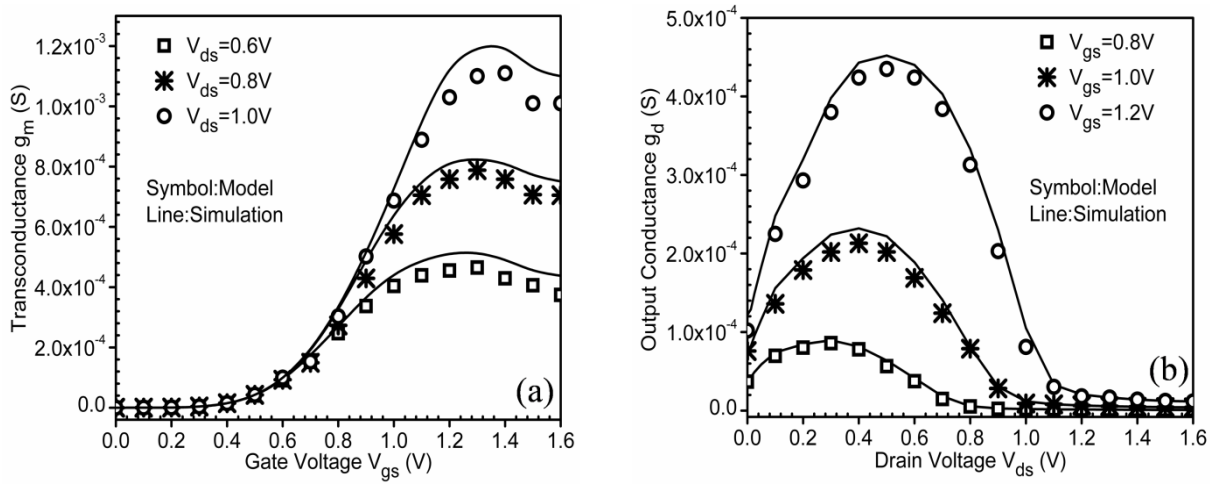

Figure 2.5 Impact of (a) drain bias on transconductance and (b) gate bias on output conductance *(Madan et al., 2015a)*.

Transconductance g_m, that is the first-order derivative of I_{ds} with respect to V_{gs} at constant V_{ds}, is shown in **Figure 2.5(a)**. The peak of g_m curve gives the optimum bias point if device is to be used as an amplifier *(Boucart and Ionescu, 2007c)*. The g_m is examined at three drain biases. It clearly shows that the peak of g_m is high for higher drain bias. This enhancement is because of the higher drain current at higher V_{ds} as discussed in **Figure 2.4(a)** on page 42. Output-conductance g_d, which is first-order derivative of drain current with respect to V_{ds} at a constant V_{gs}, is shown in **Figure 2.5(b)**. The output conductance is obtained for three gate biases. It is examined that the curve has been shifted to superior value for every increase in gate bias. Moreover, it is evident from **Figure 2.4** and **Figure 2.5** that the model developed is in well agreement with the simulation data that authenticates the developed analytical model.

2.6.2 IMPACT OF HIGH-K DIELECTRIC

In this sub-section, the developed analytical model is used to study the electrical and analog performance of the device i.e. HD-GME-GAA-TFET for three high-k dielectrics (Si_3N_4, HfO_2 and ZrO_2), and it has been investigated that the problem of lower I_{ON}, can be overcome by using the hetero-gate architecture. While analyzing an optimum high-k gate dielectric configuration for HD scheme, the gate metal work functions for GME engineering schemes are kept constant i.e. Φ_{M1} and Φ_{M2} are 4.1eV and 4.4eV respectively.

In HD-TFET, the presence of high-k near source side results into a higher band bending due to increase in surface potential (at a constant V_{gs}) as is evident from Equation 2.28 *(Lee et al., 2012)*. This higher band bending leads to reduction in W_T that increases the generation rate followed by the I_{ON}.

$$V_{gs} = \psi_s - Q_s t_{ox} / \varepsilon_{ox} \tag{2.28}$$

Where;

Q_S charge density per unit area,

ε_{ox} is the permittivity of insulator and

ψ_s is surface potential.

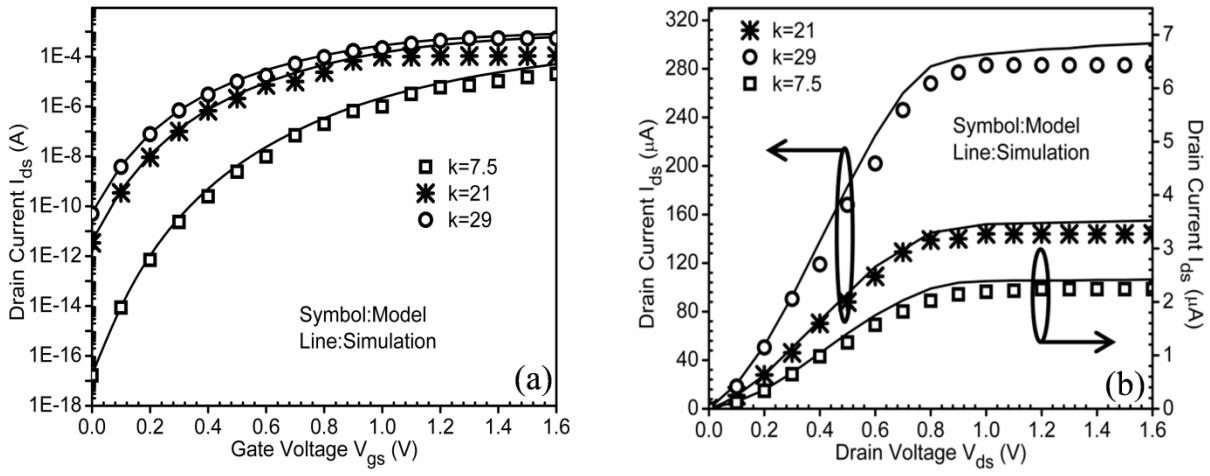

Figure 2.6 (a) Drain current as a function of V_{gs} for different high-k dielectric at V_{ds}=0.8V. (b) Drain current as a function of V_{ds} for different high-k dielectric at V_{gs}=1.0V *(Madan et al., 2015a)*.

The impact of high-k gate dielectric namely Si_3N_4 (k=7.5), HfO_2 (k=21) and ZrO_2 (k=29) on transfer characteristics at constant V_{ds}=0.8V is presented in **Figure 2.6(a)**. It is evident from the graph that among the three dielectrics, the higher value of dielectric constant corresponds to higher current driving capability. This is offered by the higher band bending for higher dielectric constant, which reduces W_T and hence, enhances the generation rate as discussed in the previous section. But the counter effect of high-k is the degradation of OFF characteristics; due to comparative higher band bending at higher gate dielectric resulting in tunneling of electrons at lower V_{gs}. This results in higher leakage current and thereby leads to higher static power dissipation. Hence, a trade-off between I_{ON} and I_{OFF} to acquire an optimum I_{ON}/I_{OFF} ratio and the SS is needed. It is evaluated that the highest I_{ON}/I_{OFF} ratio is

for Si_3N_4 i.e. 3.81×10^{12}. The impact of high-k gate dielectric on output characteristics at a constant V_{gs} = 1.0V is demonstrated in **Figure 2.6(b)**. It is clear that the device predicts a qualitative agreement in linear regime and also shows a good saturation in drain current for higher V_{ds}. It has been observed that ZrO_2 has the better output characteristics as compared to Si_3N_4 and HfO_2. Again good agreement between the model prediction and the device simulations are obtained in all regions.

Figure 2.7(a) shows the variation of barrier width lowering with respect to V_{gs} for different high-k dielectrics. W_T decreases with an increase in gate bias due to higher band bending for higher V_{gs} and alignment of VB of source and CB of channel. Moreover, at a particular V_{gs} the barrier width is lowest for ZrO_2 in comparison with HfO_2 and Si_3N_4. It was reported by Bhuwalka et al., that for TFET, the V_{th} is the gate voltage for which the energy barrier narrowing starts to saturate with applied V_{gs} *(Bhuwalka et al., 2005)*. **Figure 2.7(b)** indicates the drain current with respect to W_T for different high-k dielectrics of HD engineering scheme. By using the constant current method, the V_{th} of TFET can be extracted i.e. $V_{th}=V_{gs}$ @ $I_{DS}=10^{-7}$A *(Boucart and Ionescu, 2007c)*.

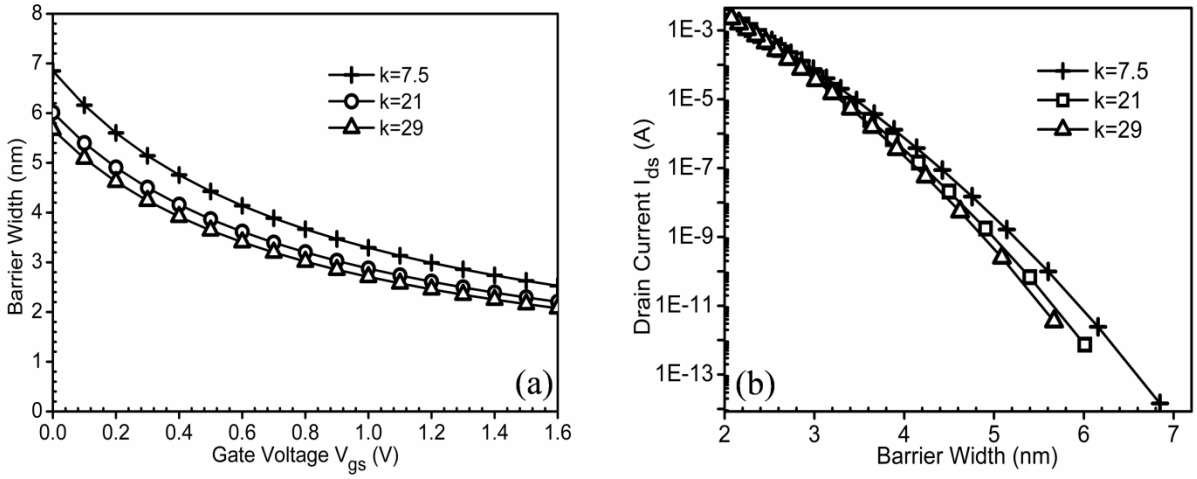

Figure 2.7 (a) Barrier width as a function of V_{gs} for different high-k dielectric, (b) Drain current as a function of barrier width for different high-k dielectric *(Madan et al., 2015a)*.

Impact of high-k dielectric on I_{ON} and I_{OFF} of the device is shown in **Figure 2.8(a)**. Among the three dielectrics, ZrO_2 has the maximum I_{ON}, but on the same side, I_{OFF} of the device is higher for the same dielectric and hence an optimization has to be done for optimum I_{ON}/I_{OFF} ratio. Quantitatively, it is evaluated that the highest I_{ON}/I_{OFF} ratio is for Si_3N_4 (k=7.5)

i.e. 3.81×10^{12}. The impact of high-k dielectric on V_{th} and SS of the device is shown in **Figure 2.8(b)**. It is evident that V_{th} decreases as we move from Si_3N_4 to HfO_2 followed by ZrO_2. But simultaneously, the SS of the device increases significantly from 34mV/decade to 53mV/decade as we use higher dielectric constant. So an optimized value of high-k dielectric can be taken for optimum SS and V_{th}. Moreover, it is clearly evident that the SS has been reduced considerably from the fundamental physical limit of conventional MOSFET on the SS i.e. $(k_BT/q)\ln10$ (~60mV/decade) at normal room temperature.

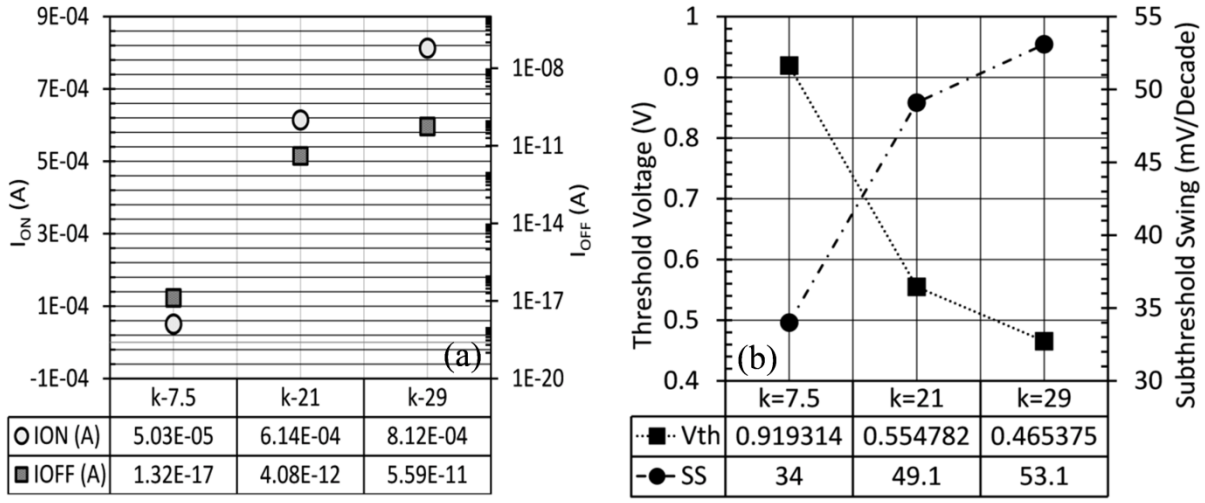

Figure 2.8 (a) Tunneling Current I_{ON} and I_{OFF} (b) V_{th} and SS of HD-GME-GAA-TFET for various high-k *(Madan et al., 2015a)*.

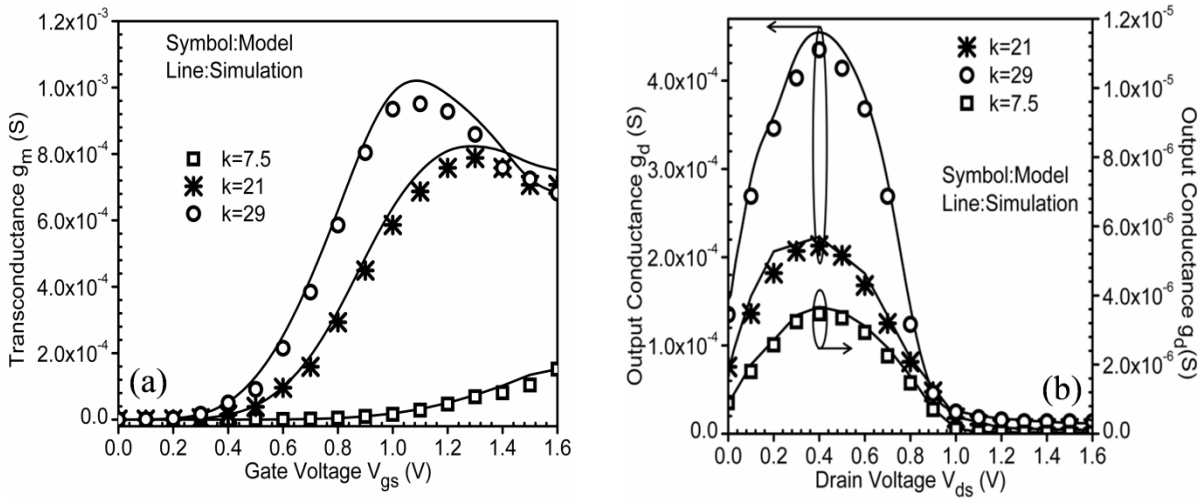

Figure 2.9 (a) g_m as a function of gate bias for different high-k dielectric. (b) g_d as a function of V_{ds} for different high-k dielectric *(Madan et al., 2015a)*.

Variation of g_m for the three dielectrics with respect to V_{gs} at constant V_{ds}=0.8V, is shown in **Figure 2.9(a)**. By setting the DC bias close to V_{gs} (at $g_m=g_{mmax}$), higher g_m can be realized. This optimum bias point, shifts towards lower V_{gs} by 15.38% for higher gate dielectric (near source side) as compared to lower gate dielectric. This change is due to decrease in W_T with high-k dielectric. It is clearly shown that among the three dielectrics; g_m of the device is higher for the case when high dielectric constant is used near source side and is due to the enhanced electrical coupling between the gate and the tunneling junction. This coupling enhances the tunneling rate i.e. more number of electrons tunnel through the barrier which eventually leads to enhanced I_{ds} and g_m. The variation of output-conductance g_d, with respect to the V_{ds} at a constant V_{gs}, is shown in **Figure 2.9(b)**. Again the g_d has a higher peak for ZrO_2 and is increased by an order of 100 (approximately) with respect to Si_3N_4.

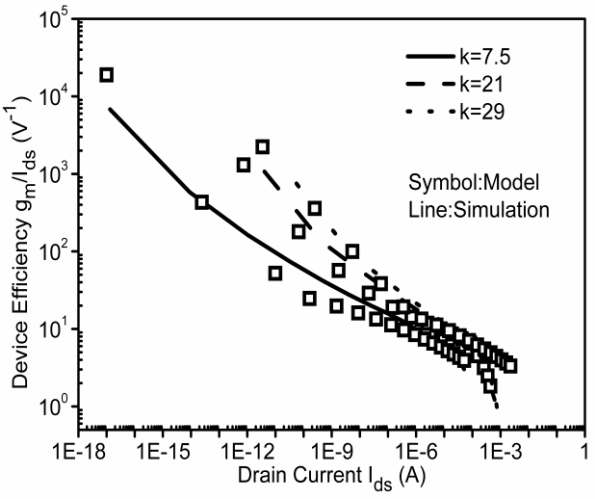

Figure 2.10 Device efficiency as a function of tunneling current for different high-k dielectric *(Madan et al., 2015a)*.

The capability to convert dc power into ac gain performance at a particular drain bias is defined as device efficiency (g_m/I_{ds}). **Figure 2.10** illustrates the comparison of g_m/I_{ds} for three high-k dielectrics. For each case, the highest value of g_m/I_{ds} is obtained in the weak inversion region and an almost linear decrease in g_m/I_{ds} profile has been obtained with increase in tunneling current. Device having ZrO_2 as a high-k dielectric has better device efficiency as compared to the device which uses HfO_2 and Si_3N_4. Also for each case, the device efficiency has reached a value greater than $40V^{-1}$ (the fundamental limit of conventional MOSFET) in subthreshold region.

2.6.3 IMPACT OF SCALING OXIDE THICKNESS

The impact of scaling the gate oxide thickness has been studied in this subsection on the analog performance of the device. In this regard, the transfer characteristics and the output characteristics of the proposed device are examined for T_{ox}=2nm, 3nm and 4nm. It is assessed that the I_{ON} of the device increases by 2.3 times as we reduce T_{ox} from 4nm to 2nm as shown in **Figure 2.11(a)**. Because with scaling of T_{ox}, gate controllability over the tunneling junction electrostatics improves, which results in increased electric field at the tunneling junction for lower T_{ox} and allows more number of charge carriers to tunnel through the junction (enhanced generation rate), eventually resulting in enhancement of I_{ds}. The impact of T_{ox} on output characteristics is shown in **Figure 2.11(b)**. Again the drain current is improved by 9.6 times with reduction in T_{ox} from 4nm to 2nm.

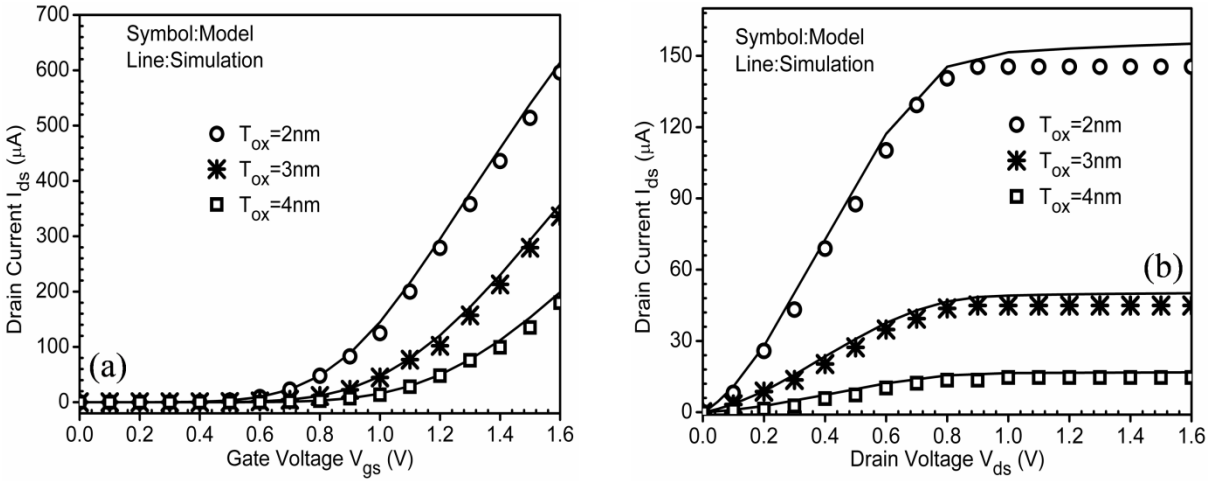

Figure 2.11 (a) Drain current as a function of (V_{gs}) for different T_{ox} at V_{ds}=0.8V. (b) Drain current as a function of (V_{ds}) for different T_{ox} at V_{gs}=1.0V *(Madan et al., 2015a)*.

2.6.4 IMPACT OF GATE METAL WORK FUNCTION

The chapter is further extended to examine the welfares of gate metal engineering scheme for VLSI/analog applications. In this respect, various critical analog parameters such as transconductance g_m, output conductance g_d, early voltage V_{EA}, device efficiency g_m/I_{ds}, intrinsic gain A_v, channel resistance R_{ch} and output resistance R_{out} have been studied for various gate metal work function configurations, to examine optimum gate metal work function for GME engineering for best device performance.

To assess an optimized value of metal work functions for the GME engineering

scheme, the analog performance of the proposed device is analyzed for three different combinations of GME configurations as stated below:

Case1. Φ_{M1}=4.1eV (Al) and Φ_{M2}=4.8eV (Au)

Case2. Φ_{M1}=4.3eV (Cr) and Φ_{M2}=4.8eV

Case3. Φ_{M1}=4.4eV (Ti) and Φ_{M2}=4.8eV

Case4. Φ_{M}=4.8eV (Single metal gate)

While analyzing the effect of gate metal work function, the dielectric constant of oxide for heterogeneous gate dielectric is kept constant throughout the simulation i.e. region 1 with dielectric constant ε_1=21 (HfO_2) and region 2 with ε_2=3.9 (SiO_2). According to the previously reported work *(Choi and Choi, 2013)*, the I_{ON} can be enhanced by using a gate metal of lower work function near the source in comparison with work function of the metal used near drain side. Moreover, to reduce the I_{OFF}, metal work function near drain should be high as compared to the metal used near the source. So, in order to achieve an optimum device performance, metal work function near drain is kept constant (Φ_{M2}=4.8 eV) and the metal work function near source side is varied. The transfer characteristics (I_{ds}-V_{gs}) of HD-GME-GAA-TFET for different Φ_{M1} at a constant Φ_{M2} are shown in **Figure 2.12(a)** in both log scale and linear scale for each case. I_{OFF} of the order of 10^{-17}A and I_{ON} of the order of 10^{-4}A is obtained for case-2 that result in I_{ON}/I_{OFF} ratio of the order of 10^{13}. The lower I_{OFF} offered by the high Φ_{M2} results in reduced static power dissipation. Further, the I_{ON} is enhanced by 1.5 times for lower Φ_{M1} i.e. in case 1 as compared to case 3, but simultaneously I_{OFF} has also been increased significantly. Thereby, it is needed to optimize the values of metal work function to obtain an optimum value of I_{ON}/I_{OFF} ratio depending on the application. The increase in I_{ON} is the main advantage of heterogate dielectric and gate metal engineering. Also, it can be clearly seen from the graph that the developed model and ATLAS device simulations are in good agreement. Transconductance g_m, with respect to the gate voltage at constant drain voltage, is shown in **Figure 2.12(b)**. g_m decides the current driving capability of the device for a given input voltage swing. It is clear from **Figure 2.12(b)** that among the three cases, the higher value of g_m is achieved for case-1. In each case, g_m of the device is very much higher in the case of ON-state as compared to OFF-state. So for enhanced tunneling current and g_m, Φ_{M1} should be low and Φ_{M2} should be possibly large.

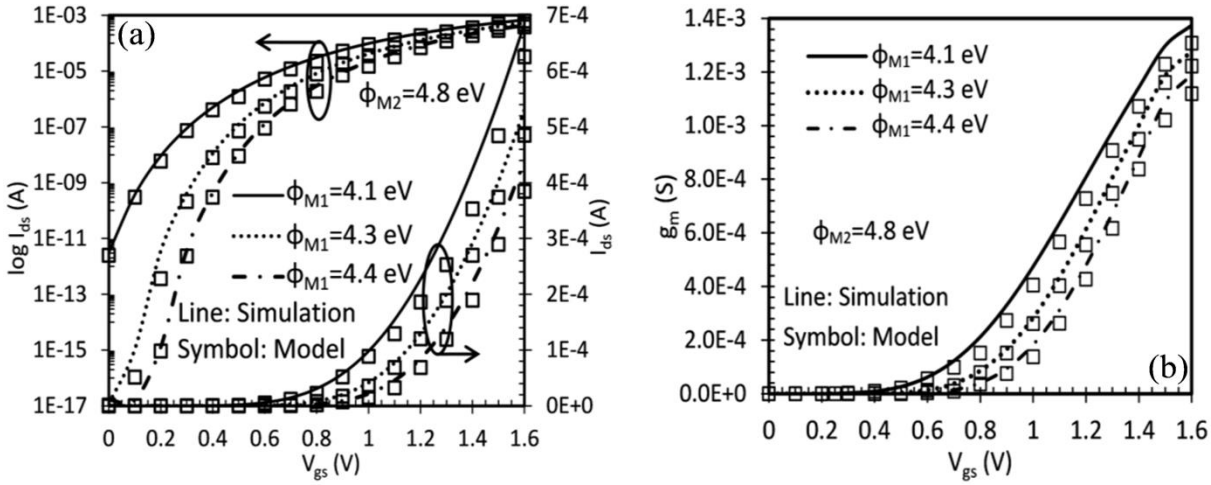

Figure 2.12 (a) Transfer characteristics (I_{ds}-V_{gs}) in the log and linear scale (b) Transconductance (g_m) as a function of V_{gs} for different metal work function for HD-GME-GAA-TFET at constant V_{ds}=1.0 V *(Madan et al., 2016)*.

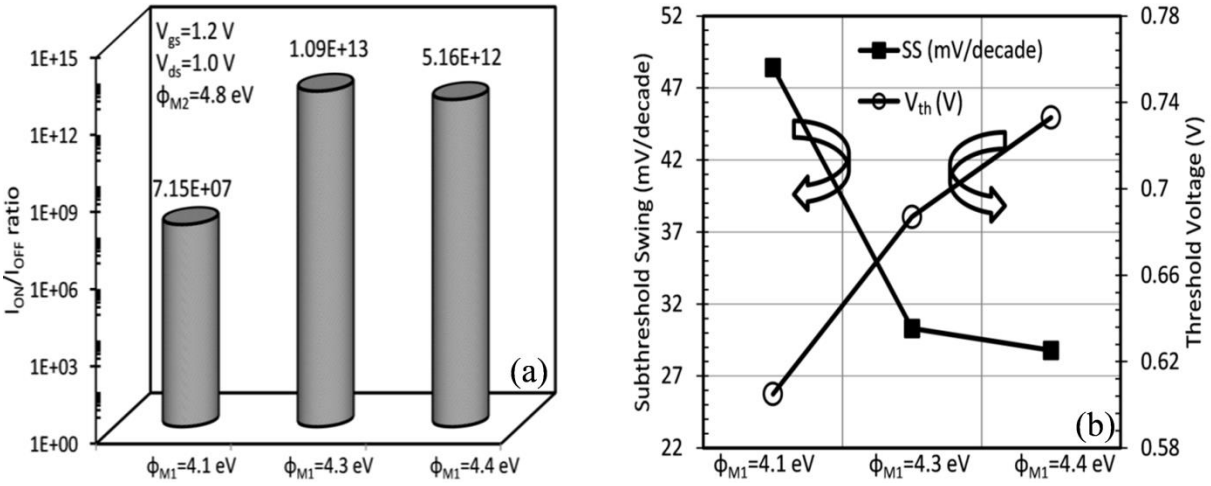

Figure 2.13 (a) I_{ON}/I_{OFF} ratio (b) SS and V_{th} for different metal work function of HD-GME-GAA-TFET *(Madan et al., 2016)*.

Figure 2.13(a) shows the variation of switching ratio i.e. I_{ON}/I_{OFF} for different metal work function configurations of GME. It is apparent from the bar graph that as Φ_{M1} increases from 4.1eV to 4.3eV, the I_{ON}/I_{OFF} ratio enhances by an order of 10^5 times. Moreover, for Φ_{M1}=4.4eV, the I_{ON}/I_{OFF} ratio reduces by 0.47 times w.r.t. case 2 and increases by many orders w.r.t. case 1. The reduction in I_{ON}/I_{OFF} ratio in case 3 w.r.t. case 2 is mainly attributed to enhanced I_{OFF} as discussed in **Figure 2.12(a)**. Further, the SS is the amount of V_{gs} required for 1-decade change in the drain current. In order to reduce the switching power of CMOS circuits, SS of the device should be as low as possible. Moreover, to accurately predict the

circuit behavior, V_{th} is an important parameter. The influence of metal work functions on the SS and V_{th} of the device is shown in **Figure 2.13(b)**. As we increase Φ_{M1} from 4.1 to 4.4 eV, the SS of the device decreases, but the V_{th} increases. So the metal work function should be chosen such that the device is optimized in terms of both SS and V_{th}.

The output characteristic (I_{ds}-V_{ds}) for each case is shown in **Figure 2.14(a)**. The saturation mechanism of output characteristics in the case of TFET is mainly attributed to the saturation of tunneling barrier width for higher drain bias at a constant gate bias *(Boucart and Ionescu, 2007b)*. It is evident from **Figure 2.14(a)** that the device predicts a qualitative agreement in linear regime and also shows a good saturation in drain current for higher drain voltages. Among the three cases, the tunneling current is enhanced by 2.7 times in case 1 w.r.t. case 3; which makes it suitable for analog applications. **Figure 2.14(b)** illustrates the effect of GME configurations on drain/output conductance g_d. In order to achieve high gain, transistors should have low g_d for analog applications. g_d is increasing with an increase in V_{ds} and then attains maxima. Further increase of V_{ds} reduces g_d because of higher drain resistance at higher drain bias. For higher Φ_{M1}, g_d decreases owing to the reduced drain current as described in **Figure 2.14(a)**.

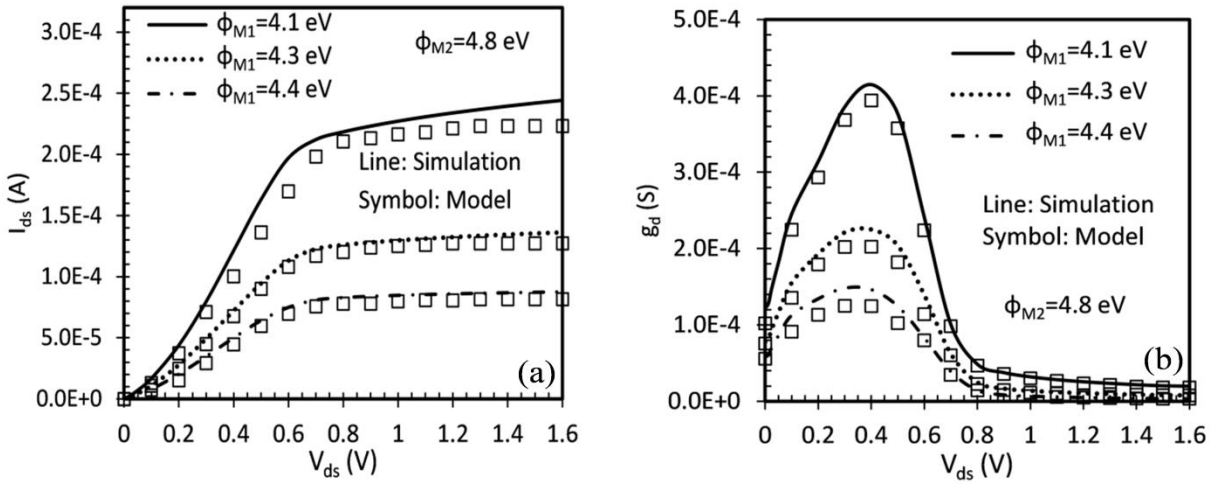

Figure 2.14 (a) Output characteristics (I_{ds}-V_{ds}) and (b) output conductance (g_d) for different metal work function of HD-GME-GAA-TFET at constant V_{gs}=1.2 V *(Madan et al., 2016)*.

Figure 2.15(a) demonstrates comparison of the device efficiency g_m/I_{ds} for each case. g_m/I_{ds} signifies the ability to convert dc power into ac gain performance at a constant drain bias. For each case, the highest value of g_m/I_{ds} is obtained for the weak inversion region and

then a linear decrease is obtained with an increase in V_{gs}. Among the three cases, case 3 has higher device efficiency. It must be noted that for each case, the device efficiency has reached a value greater than 40 V^{-1} (the fundamental limit of conventional MOSFET) in the subthreshold region. Intrinsic gain A_v (i.e. ratio of transconductance and output conductance g_m/g_d) is a valuable analog circuit design parameter used for designing amplifiers such as an operational transconductance amplifier (OTA). For better analog performance, A_v of the device should be as high as possible. The intrinsic voltage gain is obtained at the constant V_{ds}=1.0 V, making use of the relation $A_v=g_m/g_d$. Comparative analysis of A_v for different metal work function configuration with respect to V_{gs} is shown in **Figure 2.15(b)**. Highest intrinsic gain for a metal work function difference of 0.4 eV is attributed to the dominated decrease in g_d in comparison with the increase in g_m.

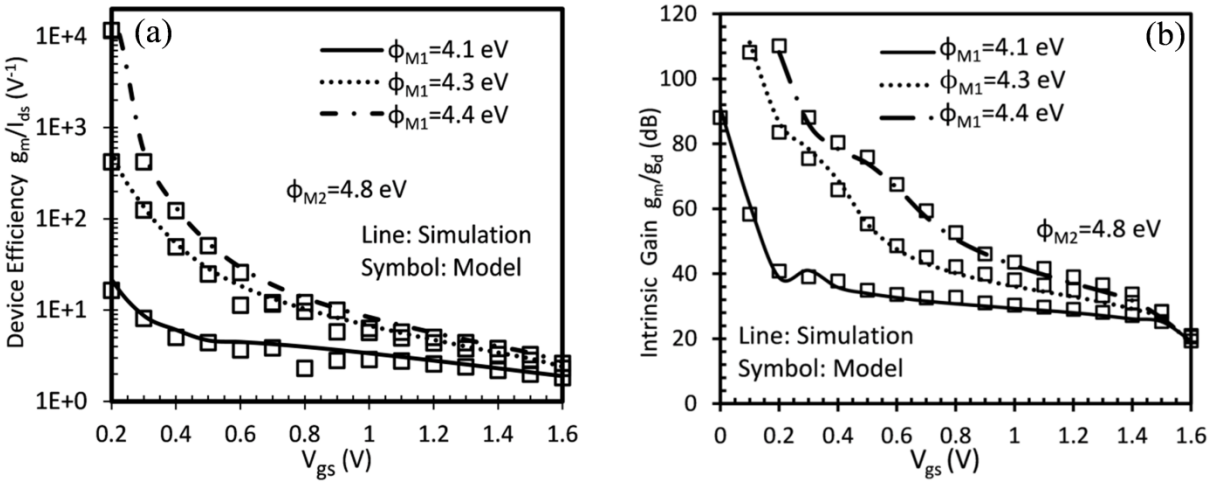

Figure 2.15 (a) Device efficiency and (b) Intrinsic gain as a function of gate voltage V_{gs} for different metal work function for HD-GME-GAA-TFET at V_{ds}=1.0V *(Madan et al., 2016)*.

The influence of gate voltage and gate metal engineering configurations on channel resistance R_{ch} is demonstrated in **Figure 2.16(a)**. For V_{gs}=0 V, no band bending is there, ensuring higher tunneling barrier width at the source channel junction and consequential very high $R_{ch} \sim 10^{15}$ Ω. As the V_{gs} increases, bands in the channel move downwards resulting in lowering of the tunneling barrier width as if a conductive channel is formed and thus drops the R_{ch} to a value of several KΩs. Moreover, at lower V_{gs}, higher R_{ch} has been obtained for the case when Φ_{M1} is 4.4 eV, which shows better OFF-state characteristics for this configuration in comparison with the rest of the cases when Φ_{M1} is reduced. Another

important parameter for analog application is the output/drain resistance R_o. Drain resistance is numerically equal to the inverse of the output conductance.The variation of R_o with V_{ds} is shown in **Figure 2.16(b)**. It is clearly shown in the **Figure 2.16(b)** that in the linear region, R_o is very small, because of strong reliance of the drain current on drain voltage. At higher V_{ds}, R_o increases monotonically owing to the saturation of drain current at higher V_{ds}. It is evident from the **Figure 2.16(b)** that for the case when Φ_{M1} is 4.4 eV, R_o is found to be extremely high offered by the better output saturation current as depicted in **Figure 2.14(a)**.

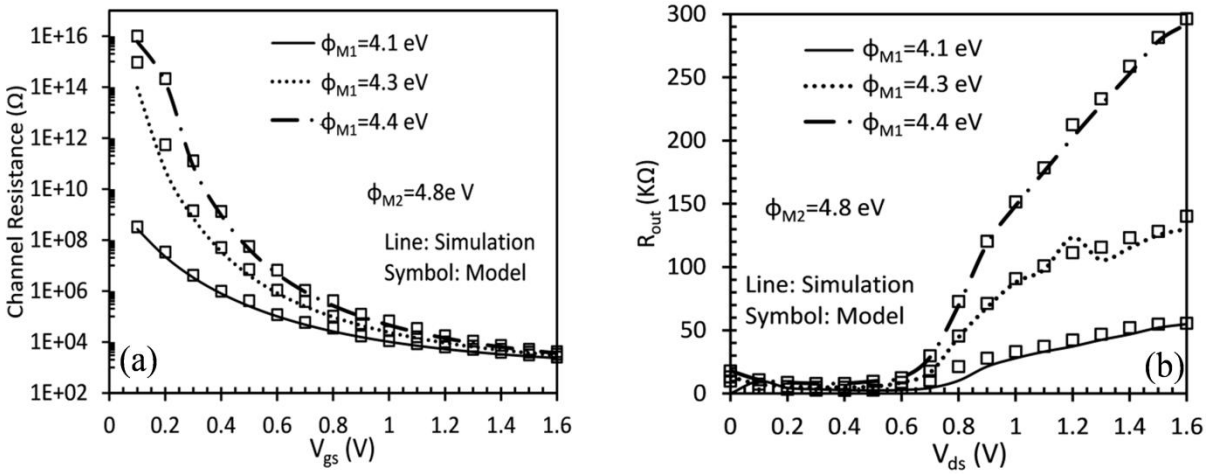

Figure 2.16 (a) Channel resistance (R_{ch}) and (b) output resistance (R_o) for different metal work function of HD-GME-GAA-TFET *(Madan et al., 2016)*.

2.7 SUMMARY

In this chapter, a hetero gate dielectric- gate metal engineered-gate all around-tunnel FET i.e. HD-GME-GAA-TFET has been proposed and detailed mathematical modeling insight for analog performance analysis has been developed. The model unites the effect of gate dielectric, gate bias, gate metal work function and oxide thickness and is used to examine the electrical and analog performance of the proposed device. Results show that by using a high-k dielectric near the source side; I_{ON} and transconductance is enhanced. The output characteristic shows a very good saturation for higher drain bias. As in most of the conventional amplifiers, MOSFET is operated in saturation region or in linear region; therefore the device is well suited for analog applications and as sub-nanometer device. The improvement in SS and diminution in V_{th} has been obtained by using higher-k dielectric. Additionally, the variation of oxide thickness on the analog performance has been

investigated for in-depth investigation of device physics. The T_{ox} variation reveals that by using a thinner gate oxide TFET, the analog performance can be improved. Additionally, the tuning of metal work functions has been done to optimize the effect of gate metal engineered on the analog performance. It is examined that both the device efficiency and device gain are improved for a gate metal work function near source and drain of 4.3eV and 4.8eV respectively. Decrease in SS and increase in V_{th} is found on increasing the work function of metal near the source. Enhancement of channel resistance and output resistance is obtained for higher metal work function near source side. Moreover, it has been evaluated that SS is less than 60 mV/decade for each case, and device efficiency is more than 40 V^{-1} in the subthreshold region. This indicates that the developed model also validates with the fact that TFET overcomes the fundamental limits of MOSFET. The results revealed that for a gate metal work function of 4.3eV and 4.8eV near source and drain side, and a dielectric of k=21 i.e. HfO_2 (near source) and k=3.9 i.e. SiO_2 (near drain), the analog performance of the device is optimized. The optimized I_{ON}/I_{OFF}~1.09×10^{13}, $I_{OFF}=1.18\times10^{-17}$A, V_{th}=0.6V and SS=30.31mV/decade. The less static power dissipation, lower SS, higher device gain, better device efficiency and the higher I_{ON}/I_{OFF} ratio make HD-GME-GAA-TFET an effective candidate for the low power analog applications. The analytical results obtained from the proposed model shows good agreement with the simulated results obtained with the ATLAS device simulator.

Further, as downscaling of CMOS devices not only promises high integration but must also provide superior RF performance. Additionally, the rising interests of wireless and RF applications motivate to analyze the RF performance efficacy of given technology and is the central point of discussion for the next chapter of this thesis.

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CHAPTER 3

SMALL SIGNAL BEHAVIOR AND RF PERFORMANCE OF HD-GME-GAA-TFET

This chapter investigates the influence of gate metal work function engineering (GME), gate bias and drain bias on the bias dependent parasitic capacitances quantitatively. Additionally, RF Figure of Merits (FOMs) such as various power gains, cut-off frequency (f_T), maximum oscillation frequency (f_{Max}) and intrinsic delay (τ) of hetero-dielectric gate-metal-engineered gate-all-around Tunnel FET (HD-GME-GAA-TFET) are also studied and are simultaneously compared with HD-GAA-TFET. Simulation results show a substantial up-gradation in RF FOMs with the amalgamation of GME architecture on HD-GAA-TFET. Further, it has been evaluated that GME exhibits 3.76 times enhancement in cut-off frequency as compared to its conventional counterparts. Additionally, the quantitative examination reveals that the intrinsic delay reduces from an order of 10^{-10}s to 10^{-12}s with the integration of GME scheme that makes it a promising candidate for low power switching applications. Further, the small signal Y-parameters have also been investigated which indicates that HD-GME-GAA-TFET is a promising candidate for RF/microwave and wireless applications.

3.1 INTRODUCTION

The successful downscaling of MOSFETs to the deep sub-nanometer regime has upgraded the unity gain cutoff frequency to an order of several Giga-Hz along with the substantial improvement in the current driving capability. These evolutions have marked MOSFET applicability for realizing low-cost system-on-chip designs encompassing digital, analog and radio frequency (RF) circuitry *(Camilleri et al., 1993, Raynaud et al., 1991, Schmitz et al., 1991).* Additionally, this remarkable progress of VLSI technology resulted in proliferate growth of wireless mobile communication. However, the static and dynamic power dissipation of ICs is the main hindrance in growing demands of smartphones and laptops, which require semiconductor devices with low standby power operation *(Abou-Allam and Manku, 1997, Rudell et al., 1997).* As the conventional MOSFET has a thermodynamic limit of $60mVdec^{-1}$ at room temperature on the subthreshold swing (SS), thus, it is needed to explore new devices, which uses a new operation mechanism other than diffusion over a thermal barrier. In this regard, Tunnel FET has emerged as a possible replacement candidate for MOSFET. The presence of reverse biased tunneling junction in TFET eliminates the high-energy tail present in the Fermi-Dirac distribution of the valence band of the source and thereby offers a smaller SS in OFF-state *(Villalon et al., 2014, Wang et al., 2004, Wang et al., 2014).* Due to its steeper subthreshold slope, lower OFF-current, reduced power consumption, lower value of leakage current and negligible short channel effects, TFET has achieved a lot of attention in the recent years *(Choi et al., 2007, Ionescu and Riel, 2011).*

TFET uses the band to band tunneling (BTBT) mechanism; moreover, the gate voltage controls the position of the energy bands, and thus controls the barrier width at the source channel junction (the tunneling junction). For n-type TFET, a positive gate bias lowers the energy band of the channel, and for a gate voltage where the conduction band of the channel goes below the valence band of the source, the tunneling of electrons from source to channel takes place which results in drive current. In the OFF-state of TFET, the valence band of source is below the conduction band of channel, resulting in a large barrier width at the tunneling junction, which obstructs the tunneling of electrons and results into an OFF current of the order of approximately femto amperes *(Toh et al., 2008, Toh et al., 2007).*

Despite its lower I_{OFF}, steeper SS and negligible short channel effects, TFET suffers from very low ON-state current which makes it unsuitable for practical application. Many innovative strategies that modify the basic pin TFET architecture were proposed in order to

improve the I_{ON}, such as bandgap engineering (narrow bandgap materials III-V semiconductors), high-k dielectric materials, dual material gate, highly doped pocket geometry as discussed in **Chapter 1**. Another problem with TFET is its ambipolar conduction as described in the introductory chapter i.e. **Chapter 1** of the thesis. For lowering ambipolar current and simultaneously enhancing the I_{ON}, hetero-gate dielectric (HD) TFET have been proposed by Choi et al. *(Choi and Lee, 2010).* In HD-TFET a high-k material located partially near the source side induces a local minimum of the conduction band at the source channel junction and hence reduces the tunneling barrier width and thus enhances the I_{ON} and the low-k dielectric present near the drain side suppresses the ambipolar current *(Lee et al., 2013, Lee and Choi, 2012).*

Moreover, the higher miller capacitance, i.e., gate to drain capacitance (C_{gd}) is another challenge for practical usage of TFET. The higher C_{gd} leads to substantial high voltage overshoot/undershoot in the transient characteristics of TFET when employed as an inverter. To circumvent this higher C_{gd}, a low bandgap material such as InAs has been proposed *(Mookerjea et al., 2009b),* that reduces the tunneling barrier width and thereby reduces the C_{gd}. It is reported in *(Koswatta et al., 2009)* that the smaller charge involved in the entire switching process of TFET delivers higher intrinsic speed. These inherent parasitic capacitances offer parasitic losses that adversely affect the gain of RF amplifiers. The maximum achievable speed in digital switching circuits is also adversely affected by these parasitic capacitances. Moreover, these parasitic capacitances also degrade the rise and fall time of the digital devices *(Malik et al., 2012).* Thus, it is a requisite to analyze these intrinsic parasitic capacitances. Besides, the different working principle of TFET is the key motivation behind the analyses of the intrinsic parasitic capacitances.

Subsequently, in this chapter, the intrinsic parasitic capacitances of the proposed device, i.e., HD-GME-GAA-TFET has been examined with variation in gate and drain bias. Moreover, these intrinsic capacitances are investigated for different gate metal work function combinations of GME engineering scheme and are also compared with its conventional counterparts, i.e., HD-GAA-TFET or HD-SMG-GAA-TFET. The chapter extends to examine the RF performance of the device in terms of various RF FOMs and power gains, and the results are compared with HD-GAA-TFET. Lastly, the chapter describes the admittance parameters, i.e., Y-parameters for various combinations of GME scheme.

The chapter is organized as follows: Section II describes the device structure and simulation models, section III describes the results obtained for parasitic capacitance and RF FOMs. Finally, the conclusions are drawn in section IV.

3.2 SIMULATION METHODOLOGY

This chapter examines the influence of GME scheme on the RF performance of the device by keeping the metal workfunction near drain side as constant and varying the metal workfunction near source side. The device architecture and the structural parameters are same as discussed in **Chapter 2** of the thesis and is also presented in **Figure 3.1**. To analyze the effect of gate metal work functions of GME scheme, the dielectric constant of oxide for heterogeneous gate dielectric is kept constant throughout the analysis, i.e., region-1 consists of dielectric constant ε_1=21 HfO_2 (near the source) and region-2 contains ε_2=3.9 SiO_2 (near the drain) for all the cases. For analyzing the influence of GME, the RF performance of the proposed device is explored for the following cases:-

Case1. Φ_{M1}=4.1eV (Al) and Φ_{M2}=4.8eV (Au)

Case2. Φ_{M1}=4.3eV (Cr) and Φ_{M2}=4.8eV

Case3. Φ_{M1}=4.4eV (Ti) and Φ_{M2}=4.8eV

Case4. Φ_{M}=4.8eV

Case 1-3 corresponds to HD-GME-GAA-TFET whereas case-4 is HD-SMG-GAA-TFET (or HD-GAA-TFET).

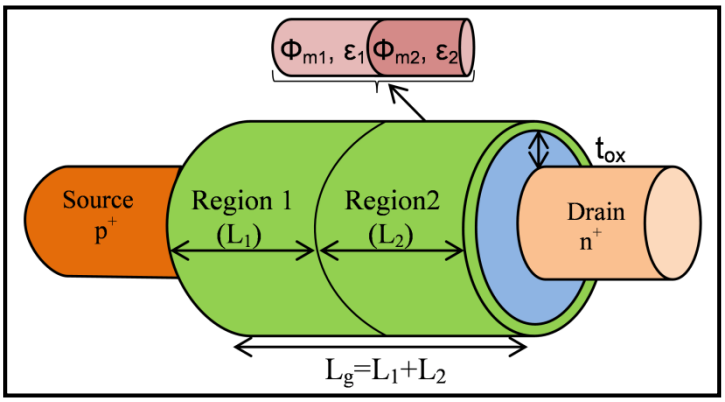

Figure 3.1 Simulated structure of Heterogate Dielectric- Gate Metal Engineered-Gate all Around-Tunnel FET (HD-GME-GAA-TFET). Default device parameters are: Channel length (L_g) =50nm (L_1=20nm and L_2=30nm), channel radius (R) =10nm, gate oxide thickness (t_{ox}) =3nm, source doping (p^+) =$10^{20}cm^{-3}$, channel doping (p) =$10^{17}cm^{-3}$, drain doping (n^+) =$5\times10^{18}cm^{-3}$ (Madan et al., 2016).

Various parasitic capacitances between each pair of electrode are extracted by small signal AC analysis at 1MHz frequency after post-processing of DC solution. These parasitic capacitances are reliant on the gate and drain bias and therefore the influence of the gate and drain bias on these capacitances has also been investigated. Additionally, the response time of the device is dependent on the gate to drain capacitance, so the drain capacitance is analyzed for the variation of both gate and drain bias. Further, the active power dissipation ($C_{gg}V_{dd}^2f$) has interdependence on the total gate capacitance, i.e., C_{gg}, so the effect of gate and drain bias on C_{gg} is also investigated. Then, to analyze the switching speed of the device, f_T is studied. Moreover, the effect of GME configurations on various high-frequency gains and the admittance parameters has also been studied.

3.3 RESULTS VERIFICATION AND DISCUSSION

Figure 3.2(a) compares the drain current of HD-GME-GAA-TFET with HD-GAA-TFET (or HD-SMG-GAA-TFET) of the same dimensions at a constant V_{ds}=1.0V. It is revealed from **Figure 3.2(a)**, that the drain current of HD-GME-GAA-TFET is much greater than drain current of HD-GAA-TFET. It is clearly evident from **Figure 3.2(a)** that for HD-GME-GAA-TFET, the presence of lower Φ_{M1} enhances the drain current drivability. This enhanced drain current is offered by the steeper band bending at the source channel junction for lower Φ_{M1} (present near the source side) as enlightened in **Chapter 2** of the thesis. Quantitatively for case-1, I_{ON} is higher by 2.68 times in comparison with case-3. Thereby, the major hindrance of TFET for practical applicability, i.e., the lower I_{ON} has been overcome via integrating the GME (Lee et al. 2012). Additionally, the I_{ON} of case 4, i.e., HD-GAA-TFET is much lower as compared to HD-GME-GAA-TFET. Moreover, the I_{OFF} is defined as the I_{ds} at V_{gs}=0.0V and V_{ds}=1.0V and is an important parameter to assess the static power dissipation. It is obtained that as the Φ_{M1} is reduced from 4.4eV to 4.1eV, the I_{OFF} increases from an order of 10^{-17}A to 10^{-11}A. Thus, it is determined that for lower Φ_{M1}, I_{ON} and I_{OFF} both are increased, and thus it is needed to optimize the device for I_{ON}/I_{OFF} ratio for superior analog performance.

An important device parameter that measures the device gain is the transconductance, i.e. (g_m). For a constant V_{ds}, g_m decides the current driving capability of the TFET. Furthermore, higher g_m is desirable for acquiring higher gain. Comparative analysis of g_m for HD-GME-GAA-TFET and HD-GAA-TFET are presented in **Figure 3.2(b)**. It is analyzed that with the integration of GME scheme, g_m of HD-GAA-TFET is enhanced considerably. This

enhancement in g_m of HD-GME-GAA-TFET is owned to the upgraded driving current obtained by GME architecture. The superior g_m is acquired for the presence of lower metal work function near source side, i.e., for Φ_{M1}=4.1eV. However, as discussed in **Figure 3.2(a)**, at Φ_{M1}=4.1eV, I_{OFF} degrades significantly. Thus, it is examined at an optimized value of Φ_{M1}=4.3eV; at which both the current switching ratio and the g_m have an optimum value.

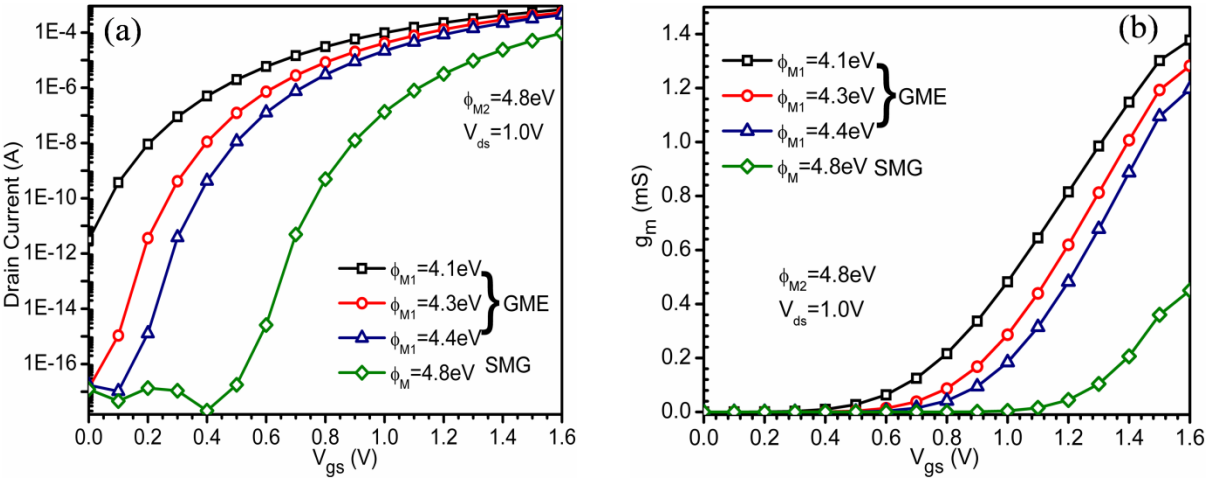

Figure 3.2 (a) Transfer characteristics (b) Transconductance of HD-GME-GAA-TFET and HD-GAA-TFET for various metal work function values as a function of V_{gs} *(Madan et al., 2016)*.

Furthermore, the reliance of switching speed of integrated circuits on the parasitic capacitances is the key motivation for analyzing the intrinsic parasitic capacitances. It is reported that for higher switching speed, parasitic capacitances should be as small as possible (Madan et al. 2015b). So, understanding of these capacitances is essential for the design of the circuits comprising TFETs. Henceforth, in this chapter, the reliance of parasitic capacitances of HD-GME-GAA-TFET on the gate and drain bias, and metal work function variation is studied using the physics-based ATLAS technology-aided design (TCAD) simulator.

The previously published works by various researchers have reported that for MOSFET working in the linear region, C_{gg} is equally apportioned between both the source/drain regions as the inversion region formed underneath the gate dielectric region is connected to both source and drain regions. But for TFET, it is reported that the different inversion charge distribution results in the connection of only the drain to the inversion layer and consequently results in larger C_{gd} as compared to C_{gs} in both linear and saturation regions *(Mookerjea et al., 2009b, Gnani et al., 2015)*. Moreover, as C_{gg}=C_{gd}+C_{gs} results in C_{gg}~C_{gd},

i.e., a major fraction of C_{gg} is contributed by C_{gd} in comparison with C_{gs} (Yang et al. 2010). Additionally, in TFET, at a constant gate bias (in ON-state), the formation of inversion layer starts from the drain side, and an increase in drain bias pinches the inversion layer towards the source side (contrasting with MOSFET where pinch off occurs towards the drain side).

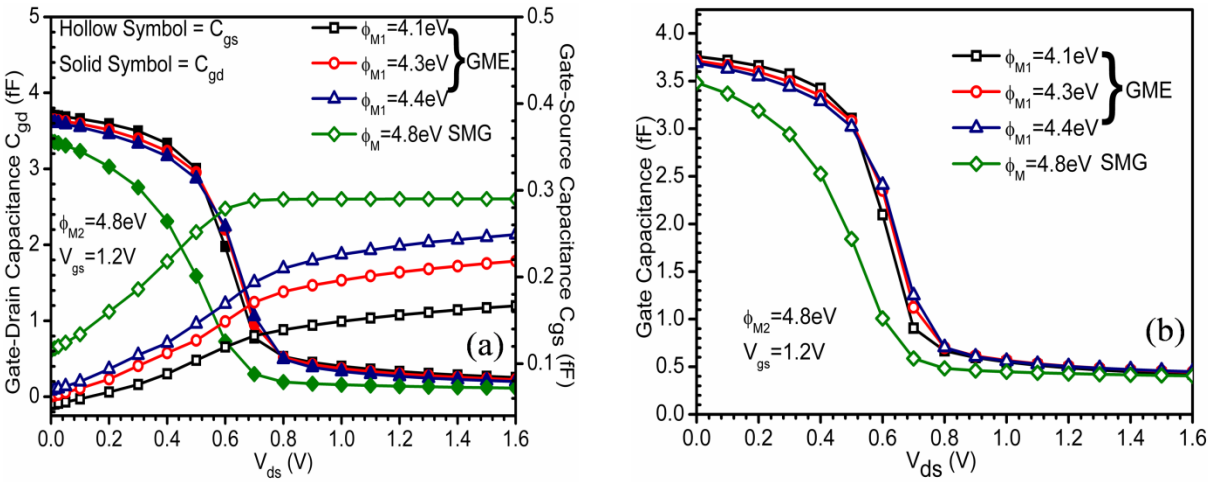

Figure 3.3 (a) Gate-drain and Gate-source capacitance (b) Gate capacitance of HD-GME-GAA-TFET and HD-GAA-TFET for various metal work function values as a function of V_{ds} *(Madan et al., 2016)*.

Figure 3.3(a) illustrates variation of C_{gd} and C_{gs} with V_{ds} at a constant V_{gs}=1.2V. It is clearly evident that the intrinsic parasitic capacitances depend on the voltage applied to the drain of the device. It is evidently shown that for lower $V_{ds,}$ i.e., in the linear region (device is in ON-state), C_{gd} is comparatively large. With an increase in V_{ds}, the inversion layer shifts towards source side that consequently reduces C_{gd}. For the region before the inversion layer formation, C_{gd} is more in case of HD-GME-GAA-TFET as compared to HD-GAA-TFET, but for a higher V_{ds}, the C_{gd} is almost equivalent for HD-GME-GAA-TFET and HD-GAA-TFET. Before inversion occurs, C_{gs} is very small because, for lower V_{ds}, all the inversion charges are near the drain. With an increase in drain bias, the inversion layer shifts towards the source side that enhances C_{gs} as illustrated in **Figure 3.3(a)**. Furthermore, for HD-GME-GAA-TFET, C_{gs} is small as compared to HD-GAA-TFET. From **Figure 3.3(a)**, it is clear that lower Φ_{M1} near source side of HD-GME-GAA-TFET offers reduced C_{gs}. Moreover, the order of C_{gs} is very much less than that of C_{gd} as evident from **Figure 3.3(a)**. Therefore, the higher I_{ON} obtained with HD-GME-GAA-TFET with no adverse effect on the parasitic capacitances makes GME a better candidate for future demands. Total gate capacitance (C_{gg}) which is

essentially equivalent to the addition of C_{gs} and C_{gd} is presented in **Figure 3.3(b)**. However, the fact that C_{gs} is smaller than C_{gd} leads to the similar profile of C_{gd} and C_{gg} as demonstrated in **Figure 3.3(b)**, i.e., the C_{gd} contributes dominantly to C_{gg}.

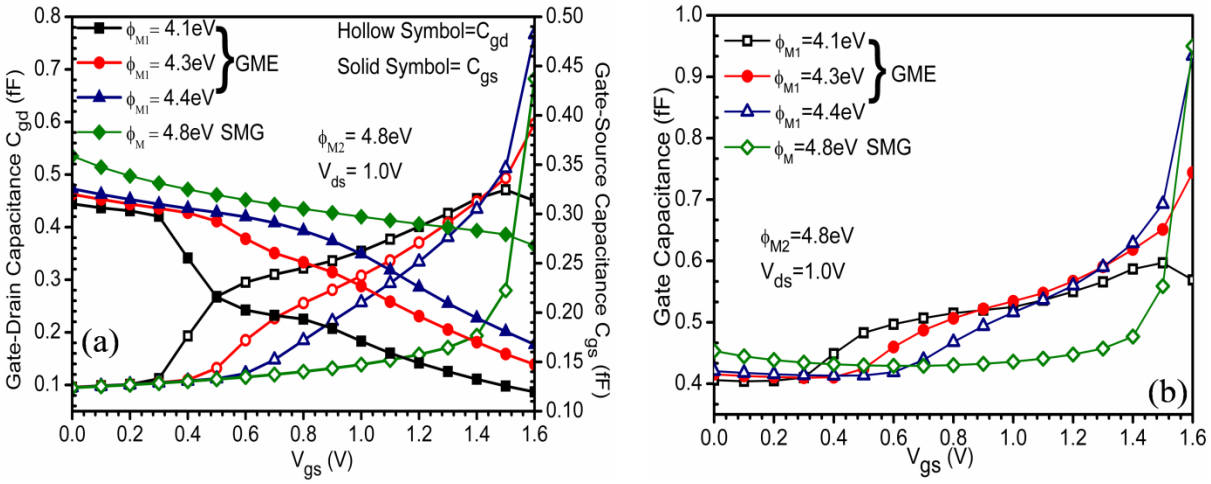

Figure 3.4 (a) Gate drain and Gate-source capacitance (b) Gate capacitance of HD-GME-GAA-TFET and HD-GAA-TFET for various metal work function values as a function of V_{gs} *(Madan et al., 2016)*.

The plot of C_{gd} and C_{gs} of both HD-GME-GAA-TFET and HD-GAA-TFET with respect to V_{gs} at constant V_{ds}=1.0V is shown in **Figure 3.4(a)**. With an increase in gate bias, the inversion layer moves from the drain towards source and consequently increases the C_{gd} with V_{gs} at a constant V_{ds}. The extension of inversion layer towards source decreases the coupling between gate and source. The consequence of decoupling of the source and gate is monotonically decreased C_{gs} with increase in V_{gs} as presented in **Figure 3.4(a)**. The influence of Φ_{M1} of GME engineering scheme on the C_{gg} as a function of gate bias is shown in **Figure 3.4(b)**. The significant contribution of C_{gd} (in comparison with C_{gs}) is evident from the similar C_{gd} and C_{gg}. Additionally, to analyze the efficacy of the GME scheme at high frequency, the RF performance of the HD-GME-GAA-TFET, in terms of RF metrics has been evaluated. The RF Figures of Merits (FOM) are analyzed in terms of cut off frequency (f_T) and maximum oscillation frequency (f_{Max}). Current gain and unilateral power gain are extracted for evaluating the values of f_T and f_{Max} respectively. **Figure 3.5(a)** demonstrates the influence of GME and SMG on the current gain. It is examined that the current gain has been enhanced considerably with the amalgamation of GME scheme onto HD-GAA-TFET. Also, current gain is marginally increased as the Φ_{M1} is reduced from 4.4eV to 4.1eV.

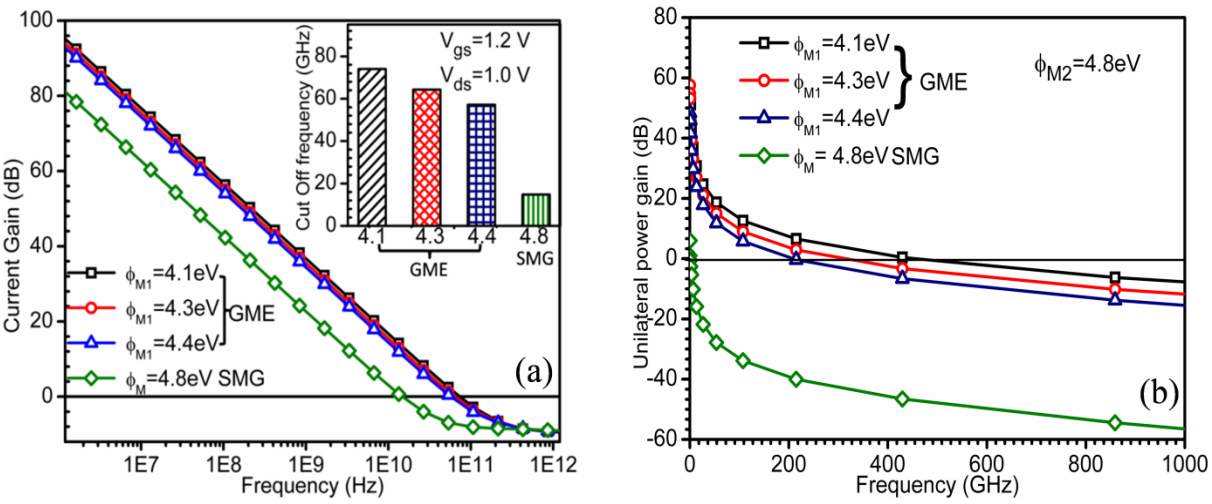

Figure 3.5 (a) Current gain, *Inset* cut off frequency (f_T) (b) unilateral power gain of HD-GME-GAA-TFET and HD-GAA-TFET at V_{gs}=1.2V and V_{ds}=1.0V for various metal work function values as a function of frequency *(Madan et al., 2016)*.

The cut off frequency (f_T) of the device is an important design parameter for RF/microwave application. The inset of **Figure 3.5(a)** shows the f_T altogether for all the cases. f_T is evaluated from the plot of current gain and is defined as the frequency at which the current gain falls to 0 dB. It is clearly evident that f_T of HD-GME-GAA-TFET is higher than the f_T of HD-GAA-TFET. The enhancement in f_T with GME is attributed to the direct dependence of f_T on g_m that has been enhanced considerably as discussed in **Figure 3.2(b)** on page 63. Quantitatively, it is assessed that f_T increases by 5, 4.34, and 3.86, times for the case 1, 2 and 3 respectively, in comparison to case 4. Furthermore, to explore the high-frequency performance of the device, the unilateral power gain has a prime significance. It is the highest achievable power gain and is the gain from a device at which no reverse transmission occurs (or good reverse isolation). **Figure 3.5(b)** presents the unilateral power gain for HD-GME-GAA-TFET and HD-GAA-TFET. Again the unilateral power gain increases with the integration of GME. Furthermore, at lower Φ_{M1}, the unilateral power gain is higher in comparison to rest of the cases.

Figure 3.6(a) compares f_T of HD-GME-GAA-TFET and HD-GAA-TFET as a function of gate bias. The increase in drain current followed by the increase in transconductance with gate bias; results in increase in f_T with gate bias. Moreover, the switching speed of the device depends on f_T. It is investigated from **Figure 3.6(a)** that a substantially higher f_T is acquired with the integration of GME scheme onto HD-GAA-TFET,

which leads to higher switching speed. The superior f_T with GME is owed to the enhanced g_m as previously discussed in **Figure 3.2(b)** on page 63. Further, increase in f_T in case of HD-GME-GAA-TFET for lower metal work function near source side has been obtained. Maximum oscillation frequency (f_{Max}) is a useful FOM for microwave applications because microwave designers are typically concerned with power gain under conjugately matched conditions (Razavi 1998). **Figure 3.6(b)** describes the f_{Max} that is extracted from the unilateral power gain at which the power gain is unity. It is clear from the **Figure 3.6(b)** that in case of GME, for lower Φ_{M1} (case 1), the f_{Max} is almost double as compared to case 3. Additionally, the f_{Max} in case of HD-GAA-TFET is much smaller than HD-GME-GAA-TFET.

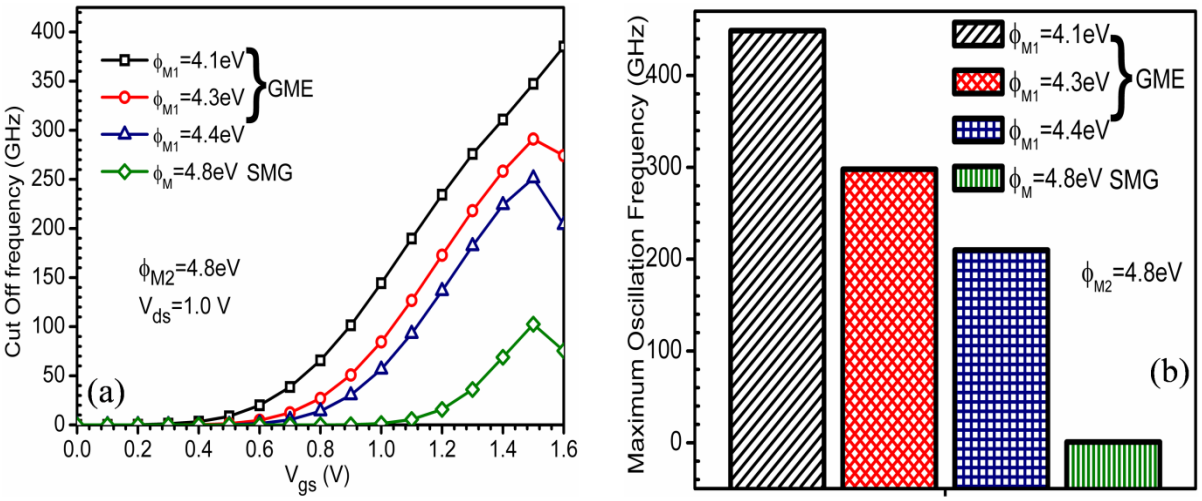

Figure 3.6 (a) Cut off frequency as a function of gate bias (b) Maximum oscillation frequency of HD-GME-GAA-TFET and HD-GAA-TFET at V_{gs}=1.2V and V_{ds}=1.0V for various metal work functions *(Madan et al., 2016)*.

Further, transconductance frequency product (TFP) is an important high-frequency circuit design parameter. It is defined as the product of device efficiency and cut off frequency, i.e. $(g_m/I_d)*f_T$. TFP is used to tradeoff between power and bandwidth. As is apparent from **Figure 3.7(a)**, TFP is enhanced in case of HD-GME-GAA-TFET by 1.52 times as compared to HD-GAA-TFET. This is because of the enhancement of f_T and device efficiency with the amalgamation of GME scheme on HD-GAA-TFET. Moreover, the peak of TFP is further enhanced for lower gate metal work function, i.e., Φ_{M1}.

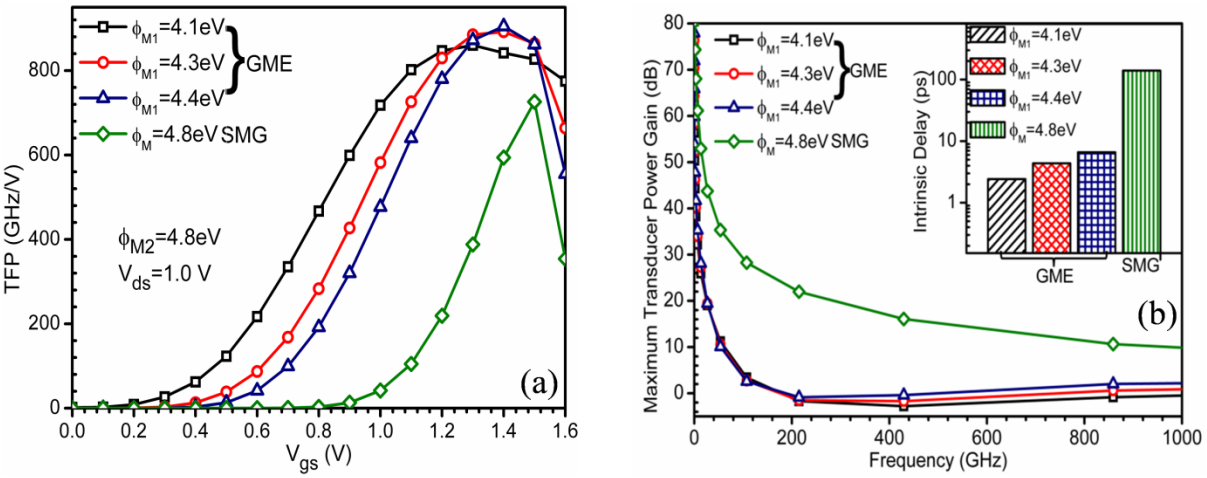

Figure 3.7 (a) Transconductance frequency product (TFP) at V_{ds}=1.0V as a function of gate bias (b) Maximum transducer power gain of HD-GME-GAA-TFET and HD-GAA-TFET at V_{gs}=1.2V and V_{ds}=1.0V for various metal work function values as a function of frequency. *Inset* Intrinsic delay at V_{ds}=1.0V *(Madan et al., 2016)*.

Additionally, intrinsic delay (τ) is an important FOM for assessing the transistors speed. τ is the reciprocal of intrinsic switching frequency f_i and is expressed as *(Mookerjea et al., 2009a)*:

$$\tau = \frac{C_{gg} * V_{dd}}{I_{ON}} \tag{3.1}$$

Where;

C_{gg} is the total gate capacitance,

V_{dd} is the drain voltage and

I_{ON} is the saturation drain current.

It is clearly evident from the bar graph presented in the inset of **Figure 3.7(b)** that there is an intensive reduction in intrinsic delay with the integrity of GME engineering scheme on HD-GAA-TFET as compared to HD-SMG-GAA-TFET. This reduction is due to the enhanced I_{ON} and reduced parasitic capacitance of the device with GME, that consequently enhances the switching speed of the device (as f_i=1/τ). Moreover, the intrinsic delay is further reduced with reduction in gate metal work function near source side in GME scheme. It is evaluated that with a reduction of Φ_{M1} from 4.4eV to 4.1eV, the intrinsic delay is reduced by 63.34%.

Figure 3.8 indicates the improvement of high-frequency maximum available power

gain (Gma) of HD-GME-GAA-TFET over HD-GAA-TFET. This enhancement is due to the enhanced drain current followed by the increase in transconductance and reduction in intrinsic parasitic capacitances as discussed previously. Moreover, with alteration of metal work function near source side in GME scheme, such as lower Φ_{M1} also results in enhanced Gma.

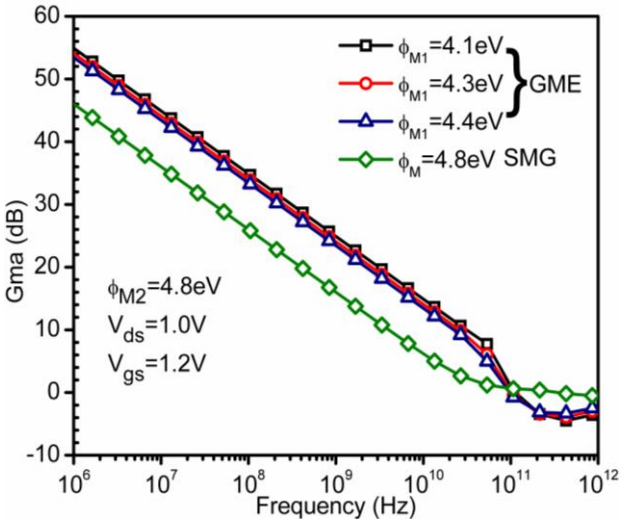

Figure 3.8 Maximum available power gain (Gma) of HD-GME-GAA-TFET and HD-SMG-GAA-TFET at V_{gs}=1.2V and V_{ds}=1.0V *(Madan et al., 2016)*.

Under small-signal conditions, the transistor can be described by a small-signal equivalent circuit. TFET can be replaced by its Y-parameters equivalent circuit consisting of the four Y-parameters Y_{11}, Y_{12}, $Y_{21,}$ and Y_{22}. The Y parameters are defined under AC short-circuit conditions (either at the input or at the output). Values of Y-parameters depend on the DC bias conditions as well as on the operating frequency. At low frequencies, ac voltages and ac currents can be easily measured, but at high frequency, the measurement of these parameters becomes exceptionally complicated. Thus, an alternative set of parameters i.e. scattering (S)-parameters can be measured at such high frequencies. But as Y-parameters are more closely associated with device physics and design, so S-parameters are again converted into Y parameters. Hence, analyzing the Y-parameters becomes obligatory *(Kang et al., 2011, Cho et al., 2011).*

Y_{11} is the short circuit input admittance, Y_{22} is the short circuit output admittance, Y_{12} is the short circuit forward transfer admittance, and Y_{21} is the short circuit reverse transfer admittance. **Figures 3.9 (a-d)** compares the real and imaginary component of Y-parameters of HD-GME-GAA-TFET and HD-SMG-GAA-TFET. It is noticeably illustrated that Y_{11} and Y_{22}

are lower at low frequency and increases gradually as frequency increases, while Y_{12} and Y_{21} are higher at low frequency and decreases gradually with increase in frequency thus, giving useful information to the RF engineers.

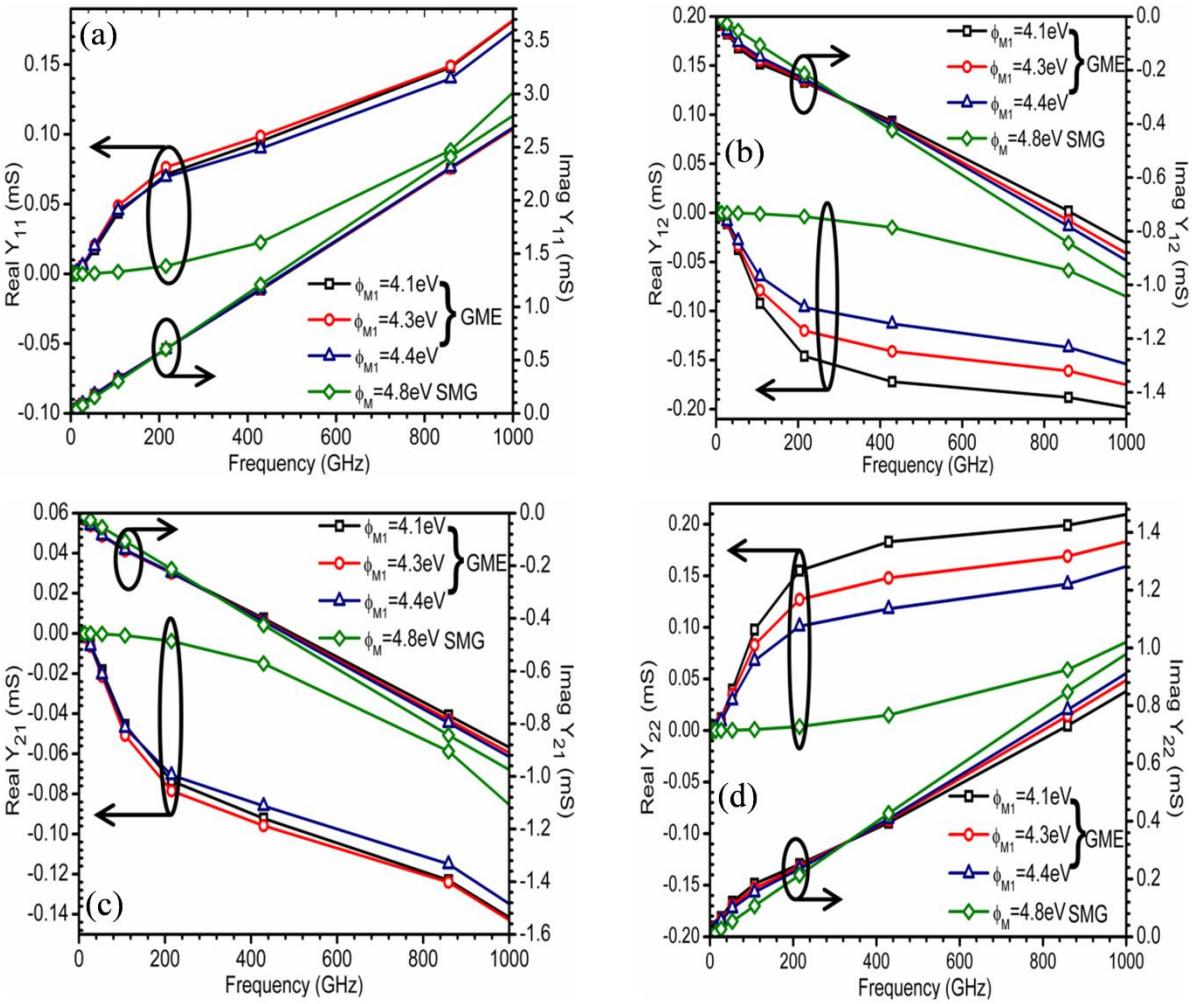

Figure 3.9 Y-parameters of HD-GME-GAA-TFET and HD-GAA-TFET as a function of frequency at V_{gs}=1.2V and V_{ds}=1.0V. (a)Y_{11}, (b) Y_{12}, (c) Y_{21}, (d) Y_{22} *(Madan et al., 2016)*.

3.4 SUMMARY

This chapter explores the small signal parameters and RF performance of HD-GME-GAA-TFET and HD-GAA-TFET such as parasitic capacitances, power gains (Gma and unilateral power gain), cut off frequency (f_T), maximum oscillation frequency (f_{Max}), intrinsic delay (τ) and admittance parameters using TCAD device simulations. It is obtained that with the implementation of GME; superior benefits of TFET are acquired in all RF metrics. With

the integration of GME scheme, the parasitic capacitances are decreased, the cutoff frequency is increased, and the maximum oscillation frequency is also manifold increased compared to its conventional counterparts. The better RF performance exhibits its effectiveness for high-frequency amplifier and microwave applications. Furthermore, it has been observed that with the amalgamation of GME scheme on HD-GAA-TFET, I_{ON} is enhanced and parasitic capacitances are reduced, resulting in enhancement of numerous power gains thus giving a new opening for HF wireless and switching applications. Also, the reduction in intrinsic delay and parasitic capacitances with GME architecture makes it applicable for analog and digital switching applications. For comprehensive RF analysis of HD-GME-GAA-TFET and its efficacy at HF, the small signal Y-parameters are required that are useful for evaluating the microwave performance in terms of input/output and transfer admittance. Henceforth, the chapter revealed the improvement in small signal Y-parameters obtained with the GME architecture which is beneficial for the RF communication. So, the HD-GME-GAA-TFET can find applications in high-switching-speed electronics.

Moreover, since the electronic devices, unlike mechanical systems, do not undergo mechanical wear out, different definitions and methods of analyzing electronic device reliability are required. While electronic device reliability is mainly considered to be based on phenomena like electromigration and environmental factors like temperature, pressure and other transient stresses over the lifetime of the device, there is one crucial factor that plays a role during fabrication of device itself, i.e., introduction of Interface Trap Charges (ITC) at the dielectric-semiconductor interface. By implication, there are no traps in SiO_2 or along the SiO_2-Si interface. However, in reality, a large number of positive or negative charges can be found along the SiO_2-Si interface. Additionally, ionic charges may be found within the SiO_2 layer as well. These charges inevitably appear during the fabrication of the transistor. The reliability of the device is however strongly affected by the presence of ITC. Therefore, the next chapter probes the effect of ITC on the operation and reliability of the device. Along with ITC, the temperature affectability over the device analog/RF performance has been the key encompassing area of the next chapter.

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CHAPTER 4

TEMPERATURE ASSOCIATED RELIABILITY ISSUES OF HETEROGENEOUS GATE DIELECTRIC-GATE ALL AROUND TUNNEL FET

This chapter explores the reliability of GAA-TFET by studying the impact of interface traps-both donor (positive interface charges) and acceptor (negative interface charges) present at the Si-SiO_2 interface, on analog/RF performance and linearity distortion analysis. In addition to GAA-TFET, the reliability of Hetero gate Dielectric GAA-TFET (HD-GAA-TFET), has also been probed. The reliability is investigated by analysing various RF Figure of Merits (FOMs) such as cut off frequency f_T, maximum oscillation frequency f_{Max}, transconductance frequency product (TFP) and numerous linearity parameters such as higher order transconductance coefficients (g_{m1}, g_{m3}), V_{IP2}, V_{IP3}, IIP3, IMD3, zero crossover point and 1dB compression point. Numerical simulations reveal that HD-GAA-TFET is more immune towards the interface trap charges in comparison with GAA-TFET and hence can act as a reliable candidate for low power switching applications. Additionally, the robustness of device against temperature variations including reliability issues of HD-GAA-TFET have also been addressed, and the results are simultaneously compared with GAA-TFET. This is done by investigating the effect of interface trap charges at various operating temperatures on the device analog parameters and RF FOMs. It is observed that, at high gate bias, TFET exhibits weak temperature dependence in comparison to the large temperature variation for lower gate bias. Results reveal that extremely high OFF current at elevated temperatures degrades the device performance, making the device less reliable for high-temperature applications.

4.1 INTRODUCTION

Unique properties of TFET offered by the band to band tunneling (BTBT) such as low I_{OFF}, sub-60mV/decade subthreshold swing (SS), immunity against short channel effects and its compatibility with the CMOS process makes it a suitable candidate for ultra-low power applications *(Ionescu and Riel, 2011, Madan et al., 2015)*. Due to low power dissipation, TFET has gained a lot of attraction and has become an attractive candidate for ultralow power applications. However, TFET suffers from low ON-state current, lower than the ITRS requirement (because of limited rate of tunneling of carrier); making it incompatible to meet the increased demand for high speed with low power consumption applications. Abundant techniques have been proposed to improve the driving current of TFET as previously discussed in **Chapter 1** *(Chang et al., 2009, Choi and Lee, 2010, Cui et al., 2011, Loh et al., 2011, Nagavarapu et al., 2008)*. Another shortcoming of TFET is the ambipolar conduction (i.e., conduction in both the directions) *(Wang et al., 2004)*; this can cause severe problems such as malfunction of the inverter-based logic circuits. To overcome these challenges collectively, a Hetero gate Dielectric TFET (HD-TFET) was proposed *(Choi and Lee, 2010)*, which combines the merits of TFET with high-k material as dielectric (at higher gate bias) and TFET with SiO_2 as dielectric (at lower gate bias) as described in **Chapter 1** of the thesis. In HD-TFET, the local minima formed at the tunneling junction enhances the I_{ON} of TFET while; the SiO_2 placed over the drain-channel junction mitigate the ambipolar behavior of TFET.

However, in the past, a lot of research work has been carried out on TFET with the main focus on various novel device architectures and material engineering of TFET, in order to overcome the challenges faced by TFET. However, the device reliability is always a major concern for nanoscale devices. The increased packing density of integrated circuits may adversely affect the device reliability due to the enhanced probability of generation of interface traps. During the fabrication process of nanoscale devices, the process induced, stress-induced and radiation-induced damage results in the conception of interface trap charges (ITC). It is reported that these interface states cause a reduction in device reliability and lifetime *(Pala et al., 2012, Wang et al., 2013)*. A lot of work has already been done to study the device reliability of MOSFET owed by the ITC *(Rai, 2017, Suk et al., 2005)*. But there is a need to estimate the performance degradation due to the interface traps present at the Si-SiO_2 interface in TFET as the fundamental working principle of TFET is entirely

different from that of MOSFET. However, work done earlier in TFET domain seldom takes into account the device reliability, which must be considered for any realistic transistor under consideration *(Avci et al., 2011, Damrongplasit et al., 2011, Fan et al., 2013, Jiao et al., 2009b).* This is due to the general assumption of silicon dioxide (SiO_2) being a perfect insulator. By implication, there are no traps in SiO_2 or along the SiO_2-Si interface. However, in reality, a large number of positive or negative charges can be found at the SiO_2-Si interface. Additionally, ionic charges may be located within the SiO_2 layer as well. In general, there are four types of charges that can be found at the SiO_2-Si interface and inside the SiO_2 layer – oxide charges (fixed and mobile), oxide trapped charges and interface charges *(Khor and Yeow, 2003).* These charges inevitably appear during the fabrication of the transistor. Although the number of such charges has been reduced significantly with continuous improvements in fabrication technology, still, they lead to a strong degradation in the operation of the device due to the high packing density of transistors in microchips today. It is reported that the interface defects which is attributed to the unsaturated fourth bond present at the interface, have energy level lying in the energy band gap of the silicon (unlike in the conduction and valence band). Electrons and holes that are present in these levels cannot move freely (or are localized) due to the larger distance between the neighboring interfacial trivalent silicon atoms *(Khor and Yeow, 2003).* Also, a donor type interface trap can act as a positive localized charge (when it is empty) or neutral localized charge (when it is filled with an electron). An acceptor type interface trap can act as a negative localized charge (when it is filled with an electron) or neutral localized charge (when it is empty). Primarily, donor traps usually lie near above the valence band, and acceptor traps often lie near below the conduction band.

Moreover, it has been reported that the reliability of TFET is a more prominent problem due to the modification in tunneling field induced by ITCs, in comparison with MOSFET *(Jiao et al., 2009a).* In case of TFET, a higher electric field near the tunneling junction (the source-channel junction) is desired for lowering of the tunneling barrier width, but on the counterparts, this high transverse field results into the generation of interface traps (donor and acceptor) and hence the localized charges (both positive and negative). Apart from the high electric field, hot carrier stress (HC) and positive bias temperature instability (PBTI) are also attributed to the generation of ITC *(Qiu et al., 2014).* Additionally, the BTBT rate in TFET is proportional to $\exp(-A/E_y)^6$, hence is very sensitive to the electric field. The presence

of interface traps at the Si/SiO_2 interface results in degradation of the electric field along the channel length near the tunneling junction and thus results in degradation of tunneling current followed by the analog performance of the device. Hence, these trap charges can cause severe issues on device reliability and lifetime of the device *(Madan and Chaujar, 2016)*. Thus, as the reliability of the device is strongly affected by the presence of ITC, therefore, this chapter probes the effect of ITC on the operation and reliability of GAA-TFET and HD-GAA-TFET.

Furthermore, the on-chip performance of the device is always subject to the operating temperature. The increased number of transistors on the chip enhances the heat dissipation and thus raises the operating temperature of the chip and the device significantly. Besides, as the properties of the semiconductor are also temperature dependent, thus, there is a need to study the effect of temperature on the device characteristics in order to investigate the temperature stability of the device *(Dutta et al., 2016, Zhu et al., 2014)*. Moreover, from the perspective of application of transistors in some extreme conditions (where the operating temperature is different from the nominal room temperature) such as the furnace temperature control, satellite communications, military, medical equipment, aerospace, automobile, nuclear sectors, wireless/mobile communications, it is important to investigate the device behaviour at a wide range of temperatures.

Thus, to consider the device reliability and applicability for wide range of temperature applications, the temperature affectability as well as the influence of ITC must be analyzed. As a consequence, the core aim of this chapter is to fulfill the above desires, i.e., the need to investigate the reliability concern of GAA-TFET subjective to the impact of operating temperature and effect of the ITCs. This is done by studying the impact of ITCs and temperature on the analog/RF performance and linearity analysis of GAA-TFET and HD-GAA-TFET. Further, the gate metal engineering (GME) is not accounted in this chapter to scrutinize the reliability of HD scheme individually. Instead, the device characteristics are optimized by tuning the single gate metal work function for minimized subthreshold characteristics at 4.3eV.

The organization of this chapter is such that after introduction in Section-I, the Section-II presents the device structure and structural parameters. The chapter continues to Section-III that describes the simulation methodology. Then, Section-IV consists of 2 parts; in part-1, the influence of ITCs at constant temperature on the analog/RF performance of GAA-TFET and HD-GAA-TFET are explored. In part-2, the device characteristics are examined at

different ambient temperatures. Finally, summarization of the work is done in section V.

4.2 DEVICE STRUCTURE AND PARAMETERS

Figure 4.1(a) shows the simulation structure of hetero gate dielectric gate all around tunnel FET, i.e., HD-GAA-TFET. The 2D cross-sectional view of HD-GAA-TFET, illustrating the presence of ITC in the channel region near the source side is shown in **Figure 4.1(b)**. For HD-GAA-TFET, region-1 consists of dielectric constant ε_1=21 (HfO_2) (near the source) and region-2 consists of ε_2=3.9 (SiO_2) (near the drain). For GAA-TFET, region-1 and region-2 are joined such that the entire gate oxide is of SiO_2, i.e., ε_1= ε_2=3.9 (SiO_2). Silicon is used as source, drain, and channel material. The radius (R) and gate oxide thickness (t_{ox}) are 10nm and 3nm respectively for both HD-GAA-TFET and GAA-TFET. The gate length L_g of HD-GAA-TFET and GAA-TFET is 50nm with L_1=10nm, L_2=40nm for HD-GAA-TFET. In both the devices under consideration, the source is p^+-type doped ($1\times10^{20}cm^{-3}$), channel is lightly p-type doped ($1\times10^{16}cm^{-3}$), and drain is n^+-doped ($5\times10^{18}cm^{-3}$). To constrain the ambipolarity effect, (tunneling at the drain-channel junction) source and drain are doped asymmetrically *(Boucart and Ionescu, 2007)*. The optimum value of gate metal work function i.e., 4.3eV has been chosen for better OFF-state characteristics for both the devices.

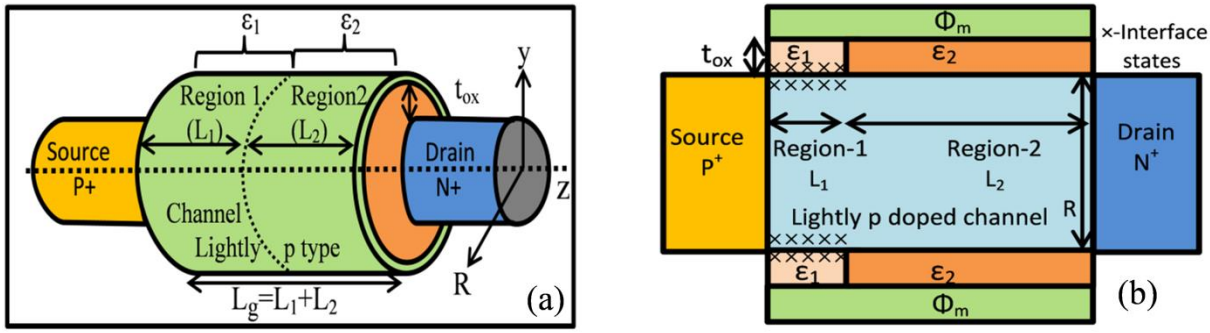

Figure 4.1 (a) Structure of n-type Heterogeneous gate Dielectric-GAA-TFET (HD-GAA-TFET) used for simulation (b) Schematic cross-sectional view of cylindrical HD-GAA-TFET illustrating the ITCs *(Madan and Chaujar, 2016, Madan and Chaujar, 2017)*.

4.3 SIMULATION METHODOLOGY

The numerical simulation of the device has been performed on Silvaco Technology Computer Aided Design (TCAD) *(SILVACO, 2011)*. In the process of device simulation of

TFET, it is essential to accurately simulate quantum mechanical BTBT of electrons from the source to the channel. In general, one of two simulation models can be used for this purpose. The first is the Kane model which approximates the tunneling barrier to be triangular in nature, while the second is the Non-local BTBT model that accounts for the dynamic variation in the electric field at the tunneling junction *(Biswas et al., 2012)*. Therefore, the latter becomes a natural choice as it provides more accurate simulation results owing to its ability to perform numerical calculation over the true potential barrier that electrons moving from the source to the channel tunnel through in a physical device. The concentration and field dependent mobility model accounts for the drift and diffusion of charge carriers through the device by solving Poisson's and continuity equations. While the recombination of the majority and minority charge carriers in the device is accounted for by the Shockley-Read-Hall (SRH) Recombination model. Being fermions, the majority carriers occupy energy states in accordance with Fermi-Dirac statistic. Hence, their distribution in the device is simulated using the Fermi-Dirac Statistical model. Finally, the Band Gap Narrowing (BGN) model is used for mathematically modeling doping induced shrinkage of the bandgap leading to changes in carrier transport across the junctions in the device, an effect commonly called band gap narrowing *(Slotboom, 1977)*. Numerical methods, Gummel (decoupled) and Newton's (Fully coupled) have been incorporated to solve the carrier transport equation.

Furthermore, to account for the device reliability, a uniform distribution of ITCs is considered at the Si-SiO_2 interface, just near the source side up to a length of 10nm over the tunneling junction. The key motivation for considering the presence of ITC only near the source-channel junction lies in the fact that in TFET, the transverse electric field attains its peak value at the tunneling junction. This forms the logical foundation of the aforementioned consideration as maximum degradation due to ITC must take place in the region on the device where the electric field attains its maximum value *(Madan and Chaujar, 2016)*. In addition to the high electric field, there are various other factors that induce the generation of interface traps. The most vital factors are:- the fabrication processes damages *(Poindexter, 1989)*, radiation-induced damages *(Lho and Kim, 2005)*, stress-induced damages (includes the electrical and processing damages) *(Trabzon and Awadelkarim, 1998)*, etc. These damages result in trapping of charges in the gate-oxide as well as at the interface of the Si-SiO_2 interface. If the trap level is located below the Fermi level, then the damaged region will accept an electron and acts as a negative fixed/localized charge. However, if the trap level is

located above the Fermi level, then the damaged region will donate the electron and acts as a positive fixed/localized charge. Thus, these traps act as a localized/fixed trap charges. Therefore, the interface traps can be transformed, into its equivalent localized charges; (positive/negative localized charge for donor/acceptor traps) *(Huang et al., 2010)*. Moreover, on the basis of various experimental data, the ITC density of positive and negative charge is taken as $N_f = \pm 1\times10^{12}$ cm^{-2} *(Chim et al., 1997)*. The influence of both acceptor and donor traps has been simulated to analyze the device characteristics along with the ideal case wherein there is no ITC. To define the density of interface fixed charges and their position present at the interface of Si-SiO_2, INTERFACE statement is used during simulation *(SILVACO, 2011)*. Further, the distribution of interface charges is assumed to be uniform during the entire simulation. Although the interface traps are also present at the interface of dielectrics in HD-GAA-TFET and will be absent in case of GAA-TFET; currently, we have only considered the ITCs along the channel length at the silicon and oxide interface. The main motivation for overlooking the ITCs at the HfO_2/SiO_2 interface is that in case of TFETs, essentially the tunneling junction and the drain junction affects the device behavior majorly so in this work, we haven't considered the ITCs at the HfO_2/SiO_2 interface *(Mallik and Chattopadhyay, 2012)*. For considering the temperature effect on the device performance, the temperature is altered from 200K to 500K. The device reliability and temperature robustness are investigated in terms of analog, RF and linearity FOMs.

4.4 RESULTS VERIFICATION AND DISCUSSION

4.4.1 IMPACT OF ITC ON ANALOG AND RF PERFORMANCE

Figure 4.2(a) shows the influence of donor type traps (positive ITC), acceptor type traps (negative ITC) and absence of ITC on nonlocal BTBT rate of electrons for GAA-TFET and HD-GAA-TFET. It is evident from the **Figure 4.2(a)** that due to the presence of acceptor traps, the BTBT rate of electrons is decreased in both the devices, while the donor traps increases the BTBT rate. Primarily, the presence of positive (negative) ITCs reduces (enhances) the flatband voltage (V_{fb}) that translates in increase (decrease) in the effective gate voltage ($V_{eff}=V_{gs}-V_{fb}$) at the tunneling junction followed by the increase (decrease) in band bending and thus narrows (broadens) the tunneling barrier width and eventually enhances (reduces) the BTBT rate of electrons. Further, it is clearly depicted that the BTBT is increased

from an order of 10^{22} to 10^{25} with the integration of HD engineering scheme over GAA-TFET. It is reported by Arora et al. that the ITC present at the Si/SiO_2 interface causes modifications in the band bending evaluated as *(Arora, 1993)*

$$\Delta V_{fb} = \frac{qN_f}{C_{ox}} \tag{4.1}$$

Where;

ΔV_{fb} is the change in flat band voltage,

q is the electronic charge,

N_f is the trap charge density and

C_{ox} is the oxide capacitance.

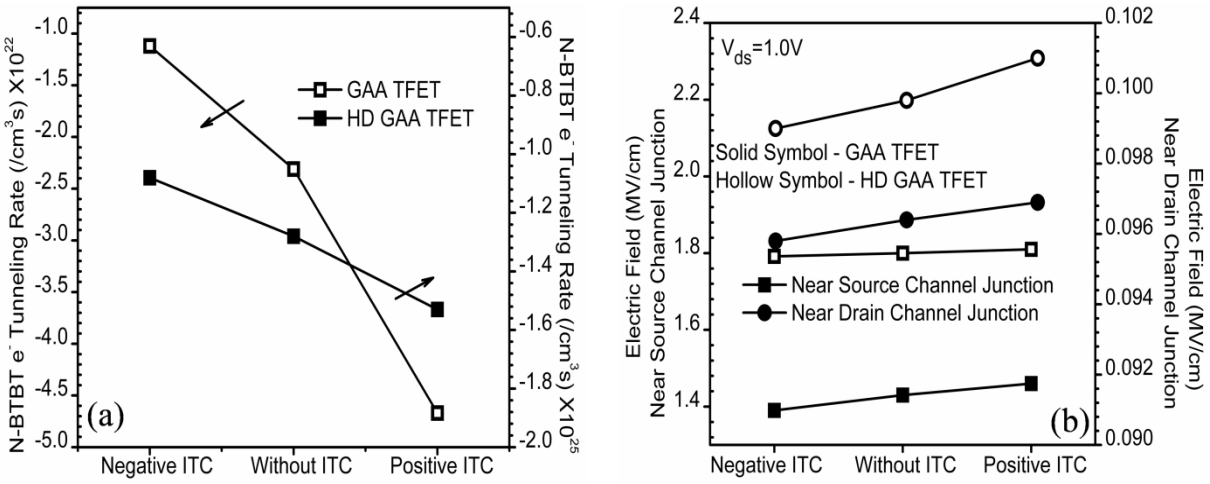

Figure 4.2 (a) Nonlocal BTBT rate at tunneling junction. (b) Electric Field near the source and drain side of HD-GAA-TFET and GAA-TFET for acceptor, donor, and absence of ITC *(Madan and Chaujar, 2016)*.

Thus, as in case of HD-GAA-TFET, the oxide capacitance in region-1 is increased (offered by the presence of high-k dielectric) and the inverse reliance of ΔV_{fb} and C_{ox} results in reduction of the ΔV_{fb}. Thus, BTBT is less influenced by the ITC for HD-GAA-TFET in comparison with GAA-TFET. The effect of ITCs on electric field close to the source and drain side for both the aforementioned devices are shown in **Figure 4.2(b)**. It must be noted that the electric field is higher at the tunneling junction for all the cases. In case of HD-GAA-TFET, the dielectric near source side is replaced by a high-k, and the dielectric near drain is SiO_2. Consequently, the effect of HD is concentrated at the tunneling junction only and the field near drain side is very less affected by the application of HD as is evident from **Figure**

4.2(b). Again due to higher (lower) band bending, the electric field is enhanced (reduced) for the positive (negative) traps near the tunneling junction. Electric field near drain side is also enhanced (reduced) for positive (negative) ITCs for both the devices under consideration.

The effect of ITC on transfer-characteristics of both the devices is presented in **Figure 4.3(a)**. As discussed before, the presence of donor (acceptor) traps increases (decreases) the band bending. This increase (decrease) results in the higher (lower) BTBT rate that translates in increase (decrease) in I_{ON}. Quantitatively, it is evaluated that the donor (acceptor) ITC increases (decreases) the I_{ON} by 117% (57%) and 8.6% (8.2%) in case of GAA-TFET and HD-GAA-TFET respectively. Again, the effect of ITC is less in case of HD-GAA-TFET as compared to GAA-TFET. This results in superior device reliability with the integration of HD engineering scheme. The effect of ITC on output characteristics of both the devices is illustrated in **Figure 4.3(b)**. It is clearly shown that the donor (acceptor) traps increases (decreases) the tunneling current. Again the impact of ITCs is relatively less in case of HD-GAA-TFET as compared to GAA-TFET. Consequently, HD-GAA-TFET is immune to the presence of ITCs and thus is more reliable in comparison to GAA-TFET.

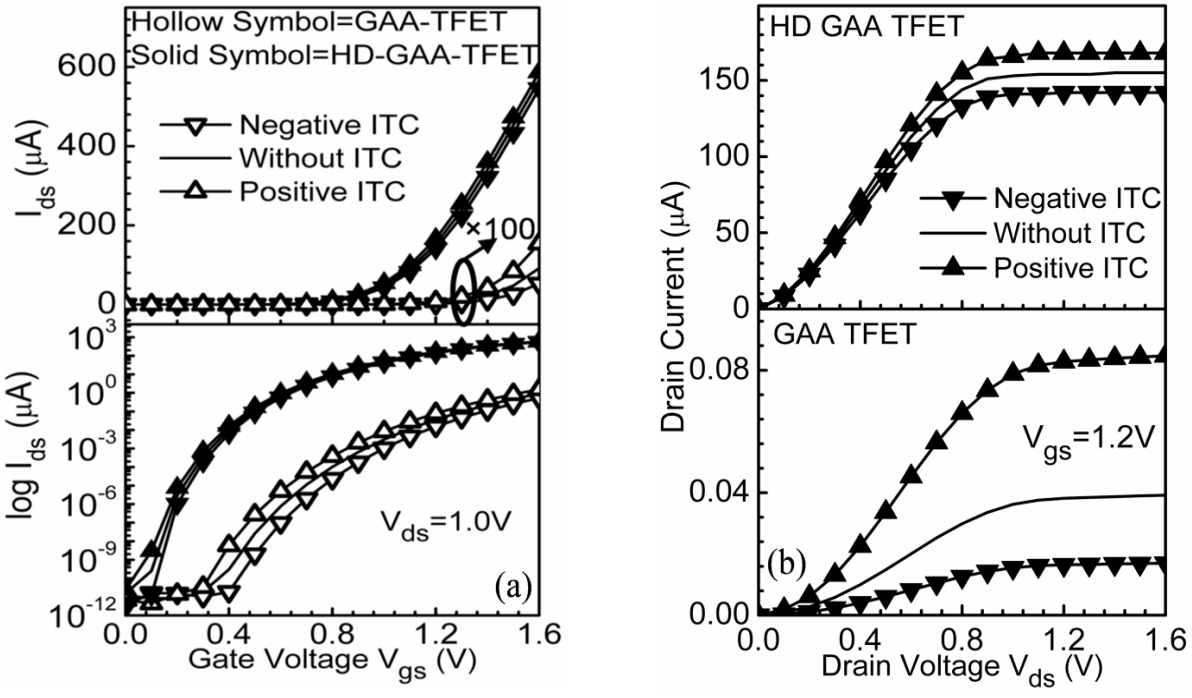

Figure 4.3 (a) Transfer characteristics and (b) output characteristics of HD-GAA-TFET and GAA-TFET as a function of the gate to source voltage for acceptor, donor, and absence of ITC ***(Madan and Chaujar, 2016)*****.**

Another vital device design parameter is the device efficiency that is evaluated as the ratio of transconductance and drain current, i.e., g_m/I_{ds}. The device efficiency gives the measure of efficiency to convert current (power) into transconductance (speed). The influence of ITCs on device efficiency is shown in **Figure 4.4**. Enhancement (reduction) in I_{ds} and transconductance (as shown in **Figure 4.3(a)** on page 82 and **Figure 4.9** on page 88 respectively) due to positive (negative) ITCs, results into decrease (increase) in device efficiency for both the devices. The decrease (increase) in device efficiency due to the occurrence of positive (negative) ITCs is mainly attributed to larger deviations in drain current in comparison to transconductance.

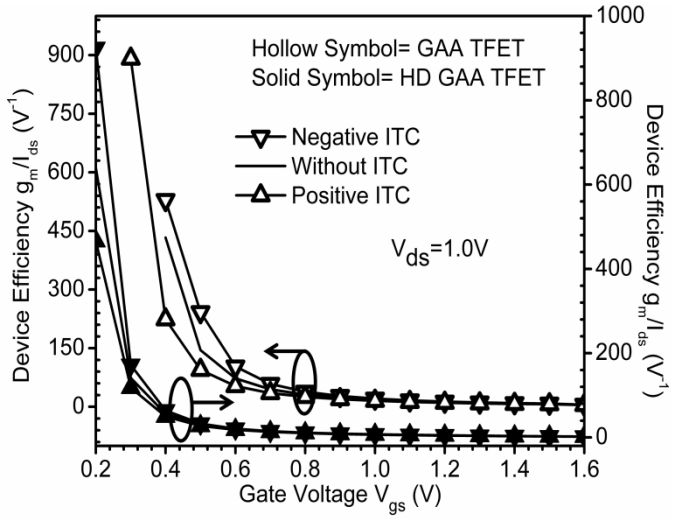

Figure 4.4 Impact of ITC on device efficiency of HD-GAA-TFET and GAA-TFET *(Madan and Chaujar, 2016)*.

The effect of ITCs on output resistance (or the drain resistance) with respect to the V_{ds} is presented in **Figure 4.5**. The R_{out} is mathematically equal to the inverse of drain conductance (g_d), higher R_{out} is desired for better analog performance in order to realize higher voltage gain, $A_v=g_m*R_{out}$. It is noticeably illustrated in **Figure 4.5** that R_{out} of HD-GAA-TFET is many orders lower than R_{out} of GAA-TFET. However, the higher g_m of HD-GAA-TFET (shown in **Figure 4.9** on page 88) counterbalances the degradation of R_{out} and hence alleviates the value of the intrinsic gain of the device. Moreover, the presence of acceptor (donor) ITCs results into increase (decrease) of R_{out}, but again the increase/decrease in case of HD-GAA-TFET is very much less in comparison with GAA-TFET.

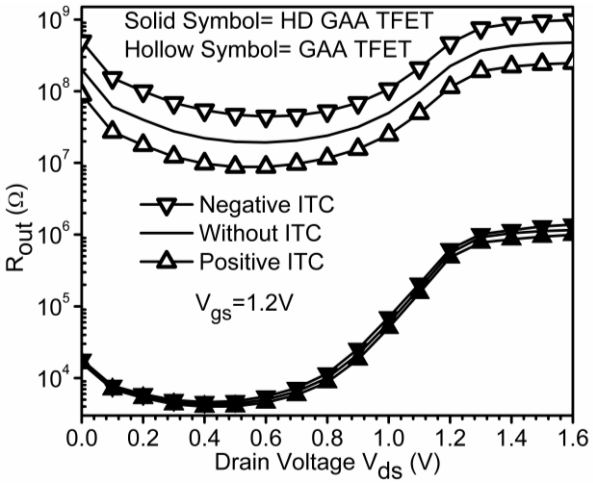

Figure 4.5 Impact of ITCs on output resistance of HD-GAA-TFET and GAA-TFET *(Madan and Chaujar, 2016)*.

After investigating the effect of ITCs on analog performance, the influence of ITC on the high-frequency performance of both the devices has also been analyzed. In this respect, numerous RF Figures of Merits (FOMs) and high frequency (HF) gains such as cut off frequency (f_T), maximum oscillation frequency (f_{Max}), transconductance frequency product (TFP), unilateral power gain and maximum transducer power gain have been evaluated. Cut off frequency (f_T) is a very vital parameter for assessing and designing the RF performance of the device. f_T is also defined as the frequency at which short-circuit current gain drops to unity (or the input and output currents are equal). f_T of both the devices has been illustrated in **Figure 4.6(a)**. Numerically f_T is given by *(Kaur et al., 2007)*:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4.2}$$

Where;

g_m is the transconductance and,

C_{gs} and C_{gd} are gate-to-source and gate-to-drain capacitance respectively.

It is clearly depicted in **Figure 4.6(a)** that the magnitude of f_T of HD-GAA-TFET is several orders greater than GAA-TFET. The direct reliance of f_T on g_m result in increase (decrease) of f_T of both the devices due to the presence of donor (acceptor) ITCs as illustrated in **Figure 4.6(a)** and **Figure 4.9** on page 88. Quantitatively it is evaluated that at V_{gs}=1.2V, the donor (acceptor) traps results into an increase (decrease) of 93% (51%) and 12% (3%) of f_T for GAA-TFET and HD-GAA-TFET respectively. Another unique FOM of HF

performance is the transconductance frequency product (TFP). TFP is numerically given by Equation 4.3 and is plotted in **Figure 4.6(b)** for donor, acceptor, and absence of ITCs for both the devices under considerations *(Pradhan et al., 2014).*

$$TFP = \left(\frac{g_m}{I_{ds}}\right) \times \left(f_T\right) \tag{4.3}$$

TFP is primarily the product of device efficiency (g_m/I_{ds}) and f_T. It represents a trade-off between power and bandwidth and is used for moderate to high-speed designs *(Pradhan et al., 2014).* It is evident from **Figure 4.6(b)** that TFP of HD-GAA-TFET is almost 10 decades higher w.r.t TFP of GAA-TFET. Also, TFP increases linearly before inversion region for both the device and after attaining a maximum value, it starts decreasing for the higher V_{gs}. Due to the presence of donor (acceptor) ITC, TFP increases (decreases) in both the devices. It is evaluated that at V_{gs}=1.0V, the increase (decrease) in case of GAA-TFET and HD-GAA-TFET is by 104% (54%) and 5% (5%) respectively.

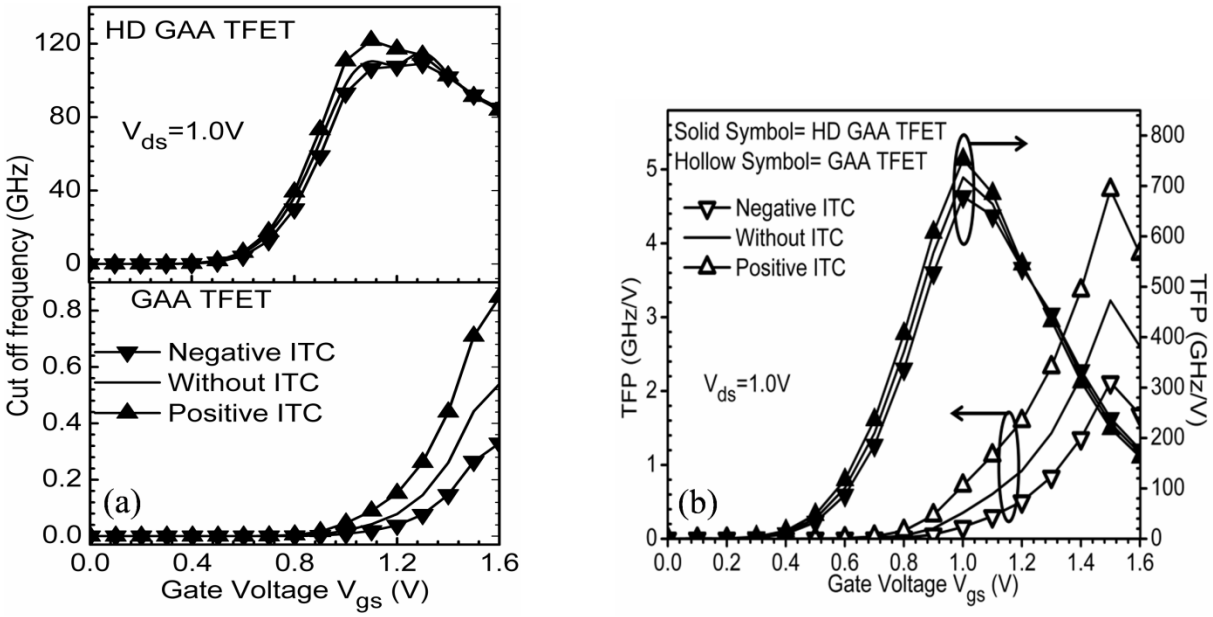

Figure 4.6 (a) Cut off frequency and, (b) transconductance frequency product (TFP) as a function of the gate voltage of HD-GAA-TFET and GAA-TFET *(Madan and Chaujar, 2016)*.

Further, unilateral power gain has been extracted for determining the value of maximum oscillation frequency (f_{Max}). Unilateral power gain is defined as the power gain with no reverse transmission or nearly very minute reverse transmission. f_{Max} is the frequency at which the Mason's unilateral power gain drops to unity (corresponds to 0dB). **Figure**

4.7(a) indicates the influence of ITCs on unilateral power gain of both the devices. It is analyzed that with the application of HD on GAA-TFET, unilateral power gain is enhanced. The positive (negative) ITCs enhances (reduces) the unilateral power gain in case of GAA-TFET, and the presence of high-k dielectric near source reduces (enhances) the unilateral power gain for positive (negative) ITCs. Moreover, the effect of ITCs is very less in case of HD-GAA-TFET in comparison with GAA-TFET. Maximum transducer power gain (G_{MT}) is fundamentally a measure of efficacy of the two ports. In case of a two-port network, G_{MT} is defined as the ratio of average power delivered to the load by a source to a maximum available power from the source. **Figure 4.7(b)** indicates the influence of ITCs on G_{MT} of both HD-GAA-TFET and GAA-TFET. Faintly degradation in the performance of GMT in case of HD-GAA-TFET has been obtained in comparison to GAA-TFET at high frequency beyond 100GHz. The effect of ITCs is negligible less for frequency greater than 10GHz, but at lower frequencies increase (decrease) in GMT due to negative (positive) ITCs have been found.

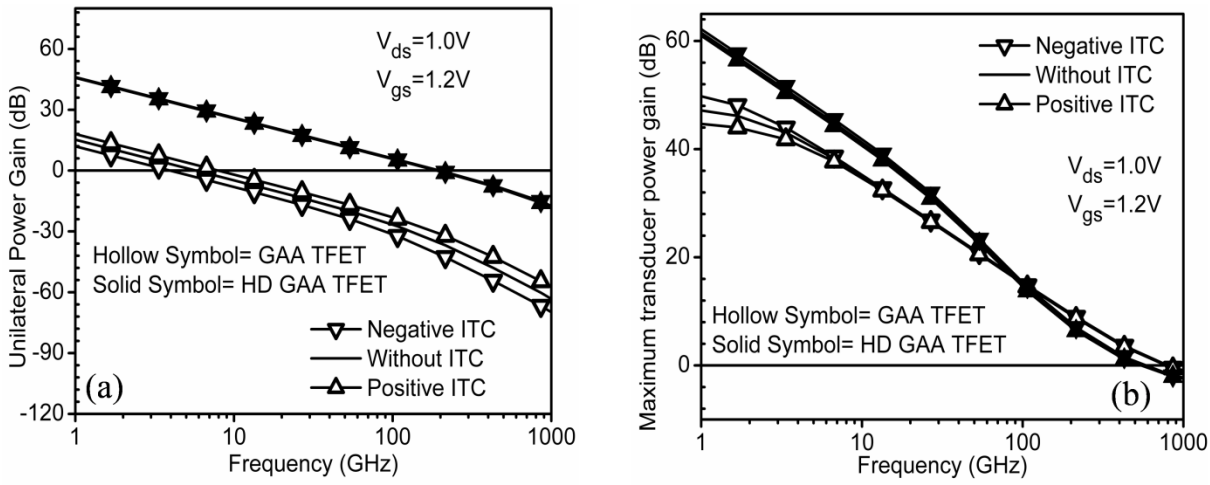

Figure 4.7 (a) Unilateral power gain (b) maximum transducer power gain as a function of frequency of HD-GAA-TFET and GAA-TFET *(Madan and Chaujar, 2016)*.

Figure 4.8 compares f_{Max} of both the devices for the donor, acceptor, and absence of ITC evaluated from unilateral power gains. It is assessed from both the bar graphs that f_{Max} for HD-GAA-TFET is 49.2, 34.17 and 23.62 times greater than f_{Max} of GAA-TFET for positive, without and negative ITCs respectively. For HD-GAA-TFET, f_{Max} increases (decreases) by 1.02% (2.97%) for acceptor (donor) trap charges. Thus, results indicate that with the

application of HD engineering, superior analog as well as HF performance of TFET is acquired, making it a better candidate for high switching speed electronic applications.

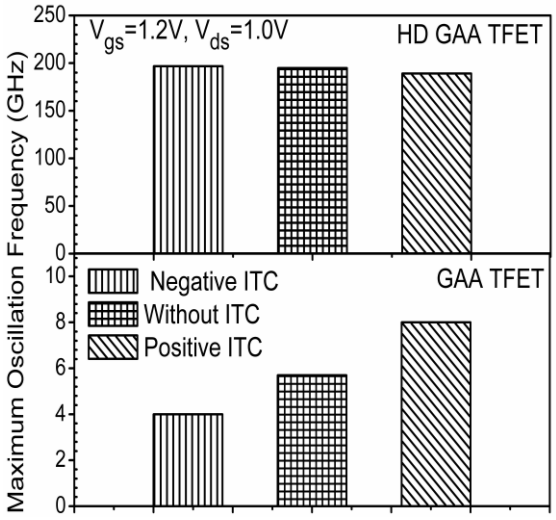

Figure 4.8 Maximum oscillation frequency of HD-GAA-TFET and GAA-TFET ***(Madan and Chaujar, 2016).***

4.4.2 EFFECT OF ITCS ON LINEARITY AND DISTORTION PERFORMANCE

Along with the high-speed, modern communication systems must give assurance for minimum signal distortion to determine the suitability of the device for analog and RF applications. If the linearity is not preserved by a device, then the nonlinear parts at the output may swamp out the desired signal. However, in many analog/RF circuits such as low noise amplifier and power amplifier, nonlinearity may degrade the system performance. For better linearity of a system, g_m should be constant over the input voltage but the reliance of g_m of both MOSFET and TFET on the input voltage translate into the nonlinear behavior of a MOSFET as well as TFET. Thus in this chapter, the influence of ITCs on linearity and RF distortion of GAA-TFET and HD-GAA-TFET are analyzed by metrics V_{IP2}, V_{IP3}, IMD3, IIP3, g_{m3}, 1dB compression point and zero-crossover point.

Transconductance (g_m) is primarily the gain of the device, and it also decides the current driving capability of the device. The peak value of the curve (g_m=$g_{m|max}$) gives the optimum bias point for which the device gives the maximum gain (used in case of amplifiers). **Figure 4.9** demonstrates the influence of ITC on g_m of both the devices under consideration. It is analyzed that the presence of donor (acceptor) traps increases (decreases) the g_m. It is examined that at V_{gs}=1.2V, g_m is enhanced (reduced) by 94 % (51%) and 13% (2.4%) for the

donor (acceptor) traps w.r.t the case when there are no ITCs for GAA-TFET and HD-GAA-TFET respectively. Thus, with the integration of HD onto GAA-TFET, the device reliability is also improved along with the analog performance. The higher order transconductance coefficient, i.e., g_{mn} are evaluated as *(Chaujar et al., 2008)*:

$$g_{mn} = \frac{\partial^n I_{ds}}{\partial V_{gs}^n} \tag{4.4}$$

The third order transconductance coefficient, i.e., g_{m3} is plotted as a function of V_{gs}, in **Figure 4.9**. For better linear performance, the amplitude of g_{m3} should be as low as possible. g_{m3} is mainly responsible for the distortion of fundamental amplitude via signals in the adjacent bands or the intermodulation distortions. It is clearly marked in **Figure 4.9** that peak of the g_{m3} is lower in case of HD-GAA-TFET and is also shifted towards lower V_{gs}. Further, the variation against ITCs is also less in case of HD-GAA-TFET.

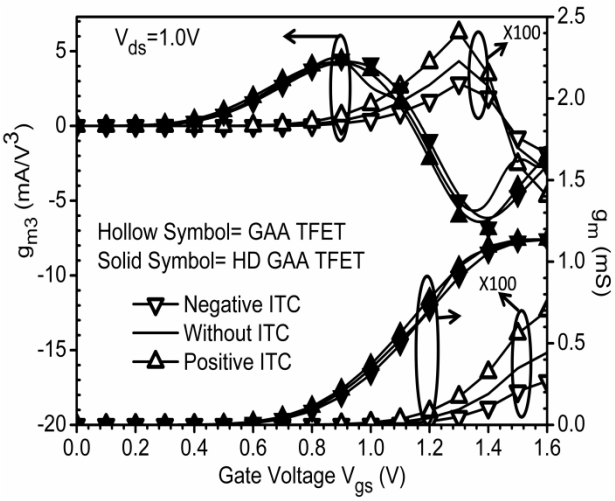

Figure 4.9 g_m and g_{m3} as a function of gate bias of HD-GAA-TFET and GAA-TFET for various types of ITCs *(Madan and Chaujar, 2016)*.

V_{IP2} represents the extrapolated input voltage at which first second-order harmonic voltages are equal, and V_{IP3} represents the extrapolated input voltage at which first and third-order harmonic voltages are equal. V_{IP2} and V_{IP3} are evaluated as *(Woerlee et al., 2001)*:

$$V_{IP2} = 4 \times \frac{g_{m1}}{g_{m2}} \tag{4.5}$$

$$V_{IP3} = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}} \tag{4.6}$$

Figures. 4.10(a-b) shows the influence of ITCs on V_{IP2} and V_{IP3} as a function of V_{gs} at a constant V_{ds}=1.0V for GAA-TFET and HD-GAA-TFET. For improved linearity performance and low distortion operations, V_{IP2} and V_{IP3} should be as high as possible *(Chaujar et al., 2008)*. The amplitude of V_{IP3} is higher for HD-GAA-TFET as compared to GAA-TFET, which reveals that along with superior analog performance, HD engineering exhibits high linearity and low distortion in comparison with conventional GAA-TFET. Moreover, the peak of the V_{IP3} is also shifted towards the lower V_{gs}; it infers that a lower V_{gs} is essential to preserve linearity with the amalgamation of HD engineering onto GAA-TFET. Further, the peak value of V_{IP3} increases (decreases) with the presence of donor (acceptor) ITCs. V_{IP2} is used to determine the distortion characteristics for different DC parameters. As evident from **Figure 4.10(a)** that with the amalgamation of HD, V_{IP2} is enhanced, indicating an improved linearity of the device.

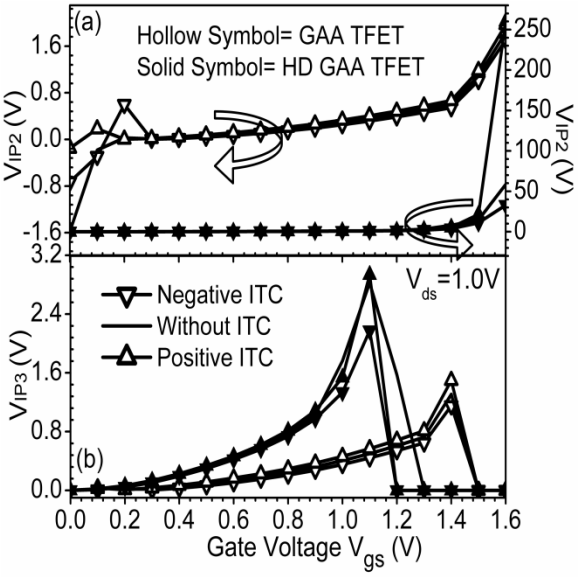

Figure 4.10 (a) V_{IP2} and (b) V_{IP3} as a function of V_{gs} of HD-GAA-TFET and GAA-TFET for various types of ITCs *(Madan and Chaujar, 2016)*.

Moreover, there are two important FOMs that governs the linearity and efficiency of amplifier viz. third order intermodulation distortion (IMD3) and third order input intercept point (IIP3). IMD3, i.e., the 3rd order intermodulation distortion, denotes the intermodulation harmonic power at which the 1st and 3rd order intermodulation harmonic powers are equal and is numerically evaluated as *(Kaya and Ma, 2004)*:

$$IMD3 = \left[\frac{9}{2} \times (V_{IP3})^3 \times g_{m3}\right]^2 \times R_s \tag{4.7}$$

Where R_s=50Ω for most of the RF applications.

IIP3 represents the extrapolated input power at which first and third-order harmonic powers are equal and is mathematically defined as *(Chaujar et al., 2008)*:

$$IIP3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_s} \tag{4.8}$$

Figures. 4.11(a-b) shows the variation of IMD3 and IIP3 with respect to V_{gs}. The results also comprise the influence of ITCs. For high linearity and lower distortion operation, IIP3 should be as high as possible, and IMD3 should be as low as possible. IMD3 have great significance in determining the intermodulation distortion in CMOS RF amplifiers as they utilize both the amplitude and phase modulation. Thus, for minimising the distortions and maximising the overall performance, reduced IMD3 is required for RF front-end transceiver parts. Similar to work reported earlier in many research papers, IIP3 increases with an increase in V_{gs} for both aforementioned devices. As evident from **Figure 4.11(b)**, HD-GAA-TFET has higher IIP3 in comparison with GAA-TFET, which indicates the potential of HD for better linearity and low distortions analog and RF applications. Moreover, better immunity against ITCs is achieved in case of HD-GAA-TFET as compared to GAA-TFET.

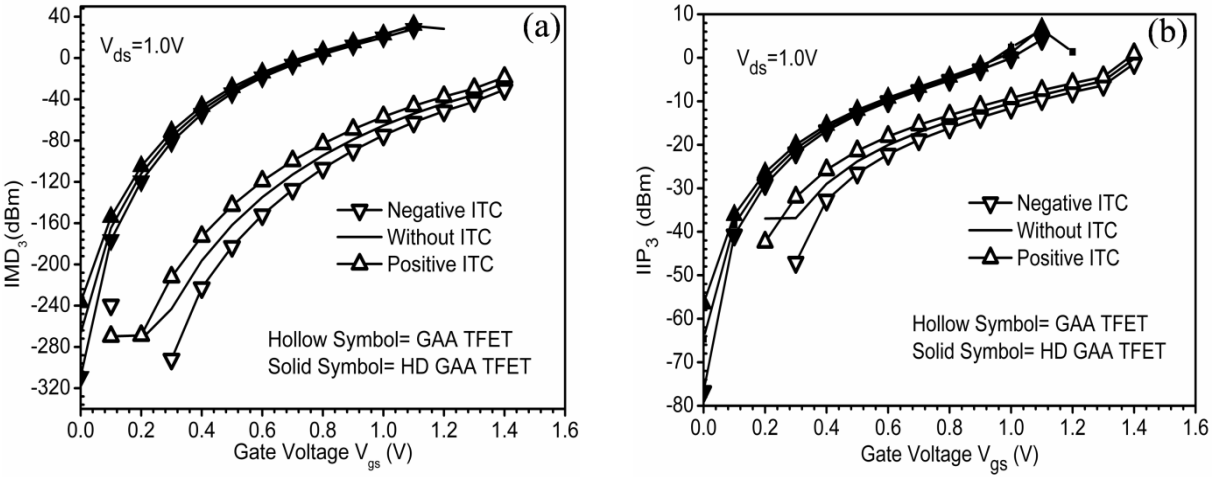

Figure 4.11 (a) IMD3 and (b) IIP3 as a function of gate bias of HD-GAA-TFET and GAA-TFET for various types of ITCs *(Madan and Chaujar, 2016)*.

1-dB compression point (P1dB) is defined as the input power which causes the gain to

drop by 1-dB. This can be considered as the onset of the distortion and is numerically evaluated as *(Biswas et al., 2015)*:

$$1-dB\,\text{Compression Point} = 0.22\sqrt{\frac{g_{m1}}{g_{m3}}} \tag{4.9}$$

P1dB gives the estimate of maximum input power, after which the gain of an amplifier decreases. **Figure 4.12(a)** shows the influence of ITCs on P1dB for both the devices under consideration. Thus, because of reduced signal distortion and high g_m in case of HD-GAA-TFET, P1dB is also enhanced in case of HD-GAA-TFET in comparison with GAA-TFET as demonstrated in **Figure 4.12(a)**. Further, there is an increase (decrease) in P1dB due to the presence of positive (negative) ITCs. The nonlinearity possessed by g_{m3} can be suppressed by selecting the optimum biased point; determined by the zero crossover point (ZCP) of g_{m3}. **Figure 4.12(b)** shows that a higher V_{gs} is needed in case of GAA-TFET to achieve better linearity in comparison with HD-GAA-TFET. Moreover, for positive (negative) ITCs, ZCP shift towards lower (higher) gate voltages, which is desirable for better linearity and low distortion.

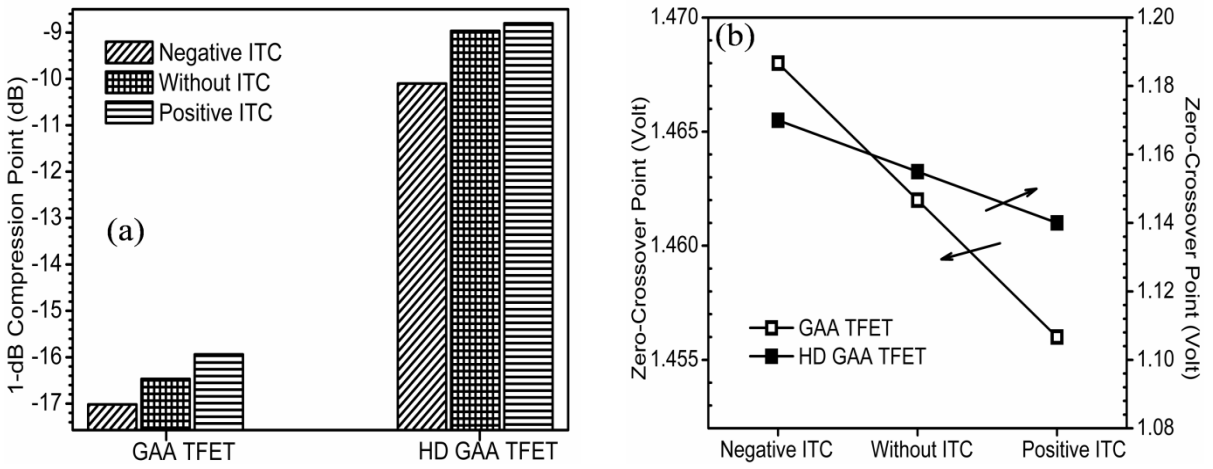

Figure 4.12 Comparison of (a) 1-dB compression point and (b) zero crossover point as a function of gate bias of HD-GAA-TFET and GAA-TFET for various types of ITCs *(Madan and Chaujar, 2016)*.

4.4.3 IMPACT OF TEMPERATURE AND ITCS ON ANALOG AND RF PERFORMANCE

After analyzing the influence of polarity of ITC on analog, RF and linearity performance of the GAA-TFET and HD-GAA-TFET, this section of the chapter continues to examine the temperature associated reliability issues of the devices under consideration. To

investigate the temperature associativity of the device, analog and RF performance of GAA-TFET and HD-GAA-TFET are examined under wide temperature range viz. 200K-500K. Moreover, while investigating the temperature affectability, the presence of ITCs is not overlooked, and the results are analyzed for both type of ITCs, i.e., donor and acceptor ITCs along with the ideal Si-SiO_2 interface, i.e., when no ITC are present.

Figure 4.13 demonstrates the influence of temperature and ITCs on the BTBT rate of electrons at the source channel junction of GAA-TFET and HD-GAA-TFET. It is examined that at higher temperatures, the BTBT rate of electrons increases; quantitatively, the increase is 7.38 times and 2.41 times for an increase in temperature from 200 K to 500 K for GAA-TFET and HD-GAA-TFET respectively at constant donor trap density of 1×10^{12} cm^{-2}. The enhanced BTBT rate of electrons is attributed to the bandgap narrowing at elevated temperatures that narrows the tunneling barrier width at the tunneling junction and consequently allows more number of electrons to tunnel through the valence band of the source to the conduction band of the channel.

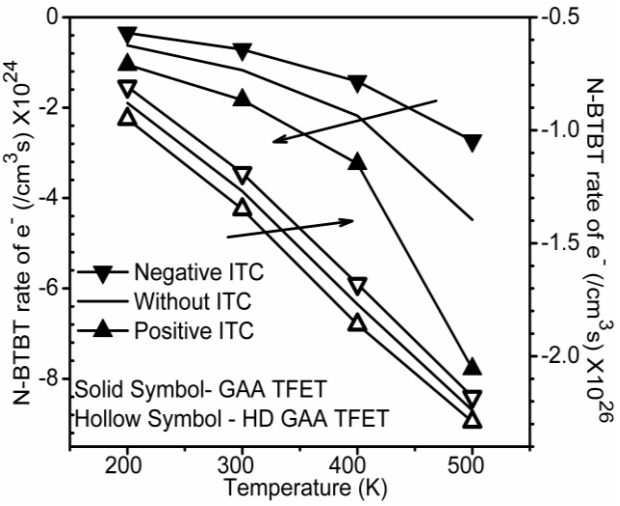

Figure 4.13 Variation of Nonlocal BTBT rate of electrons at tunneling junction with respect to temperature at V_{gs}=1.2 V and V_{ds}=1.0 V, for GAA-TFET and HD-GAA-TFET for fixed ITC density, N_f = ± 1 × 10^{12} cm^{-2}, and absence of ITC *(Madan and Chaujar, 2017)*.

Additionally, it is examined that the occurrence of positive (negative) ITCs reduces (enhances) the flatband voltage (V_{fb}) by a quantity of qN_f/C_{OX} [as described in Equation 4.1]. This reduced (enhanced) V_{fb} is followed by the increase (decrease) in the effective gate voltage, i.e. (V_{gs}-V_{fb}) at the tunneling junction that thereby enhances (reduces) the Non-local

BTBT rate of electrons at the tunneling junction. It should be remarked that the BTBT rate of electrons is considerably greater for HD-GAA-TFET as compared to GAA-TFET.

Power consumption is the major challenge for further down-scaling the FET based devices. Low operating voltage is essential for reducing the power consumption, and therefore a low V_{th} is necessary. **Figure 4.14(a)** displays V_{th} for both the devices under consideration as a function of temperature; the results also comprise the influence of ITCs. The constant current method, i.e., the V_{gs} @$I_{ds}=10^{-7}$A is used for calculating the V_{th}. The enhanced (reduced) effective gate voltage, i.e. (V_{gs}-V_{fb}), offered by the presence of positive (negative) ITCs, results in a decrease (increase) of V_{th} for both GAA-TFET and HD-GAA-TFET. Furthermore, the V_{th} decreases almost linearly with an increase in temperature. The reduction in V_{th} at elevated temperature is essentially endorsed by the higher tunneling rate of electrons at elevated temperature [see **Figure 4.13** on page 92], resulting into early switching of the devices and thus a reduction in V_{th} in both the devices. It is calculated that as the temperature increases from 200K to 500K, the V_{th} reduces by 4.18% and 20.6% in case of GAA-TFET and HD-GAA-TFET respectively.

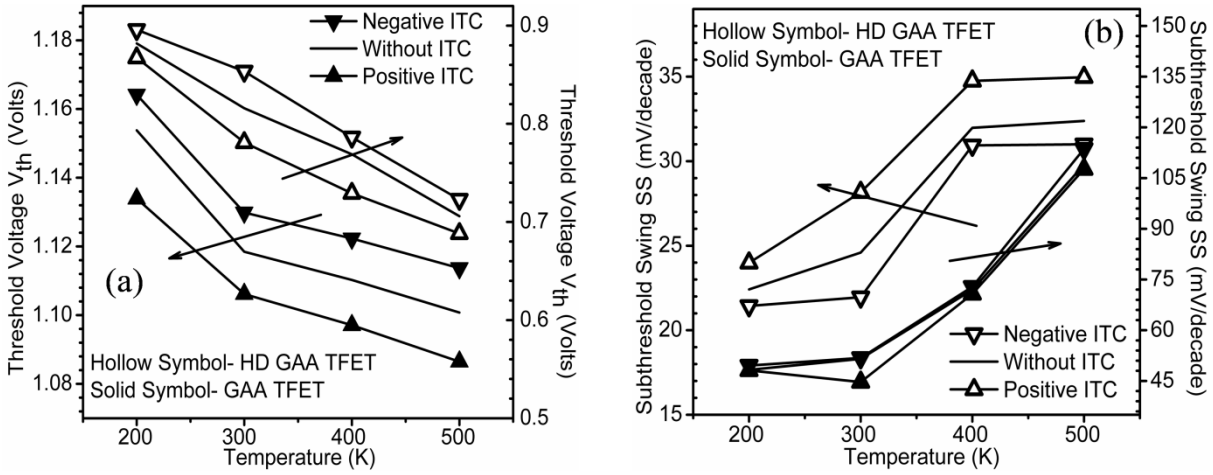

Figure 4.14 Impact of temperature and ITCs on (a) Threshold voltage and, (b) SS at V_{ds}=1.0 V of GAA-TFET and HD-GAA-TFET for fixed ITC density, $N_f=\pm\ 1\times10^{12}cm^{-2}$, and absence of ITC *(Madan and Chaujar, 2017)*.

SS is defined as the change in gate bias needed for one-decade change in drain current. To reduce the V_{th} without negotiating with I_{OFF}, small SS is required. Supplementary, for reduced switching power of CMOS circuits, the SS of FETs should be reduced. Thus, SS is a

primarily important parameter for TFET designing and hence, is inspected in this chapter to inspect its variation with temperature. SS of both the devices is presented in **Figure 4.14(b)** specifies that SS has overcome the fundamental boundary of MOSFETs in the case of HD-GAA-TFET at the entire temperature range. Moreover, the degradation in SS at elevated temperature is due to the deterioration in I_{OFF} [see **Figure 4.16(b)** on page 96] at higher temperatures in both the devices. It is evaluated that with an increase in temperature from 200K to 500K, the SS enhances by 2.29 and 1.36 times for GAA-TFET and HD-GAA-TFET respectively. Furthermore, it is also explored that the presence of donor (acceptor) ITCs increases (decreases) the SS.

The transfer characteristics of GAA-TFET and HD-GAA-TFET are illustrated in **Figures 4.15 (a-b)**. **Figure 4.15(a)** shows the variation of drain current as a function of gate bias for wide temperature range viz. 200-500 K, at a constant ITC of donor type density of 1×10^{12} cm^{-2}. The transfer characteristics reveal absolutely different behaviors at the subthreshold and superthreshold regime. In subthreshold regime, the drain current shows large variations with an increase in temperature in comparison with the superthreshold regime. This larger variation with temperature in the subthreshold region of transfer characteristics is due to the dominance of SRH recombination at lower V_{gs}, which has an exponential dependence on ambient temperature *(SILVACO, 2011)*and is given as:-

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left[n + n_i \exp\left(\frac{E_{TRAP}}{kT_L}\right)\right] + \tau_n\left[p + n_i \exp\left(-\frac{E_{TRAP}}{kT_L}\right)\right]} \tag{4.10}$$

Where;

τ_p ($=10^{-7}$ s) and τ_n ($=10^{-7}$ s) are the electron and hole lifetimes respectively,

E_{TRAP} is the difference between the trap energy and the intrinsic Fermi level, and

T_L is the lattice temperature in degree Kelvin.

This exponential dependence upshot into severe degradation in OFF characteristics at elevated temperatures. While, the most significant current component for TFET, i.e., the BTBT, dominates at the higher V_{gs} or in the superthreshold regime. BTBT being marginally temperature dependent (caused by the BGN) fallouts into an insignificant increase in drain current as the temperature rises. Thus, in the super-threshold regime, the drain current of both the devices increases slightly with temperature. This is due to the BGN at a higher temperature, causing an increase in BTBT rate of electrons followed by I_{ds}. Besides, the

temperature coefficient is positive for entire gate bias range in both GAA-TFET and HD-GAA-TFET. This is in conflict with the case of MOSFET where a positive/negative temperature coefficient exists for below/ above subthreshold regime respectively. **Figure 4.15(b)** shows the influence of ITC on transfer characteristics of both the devices at constant temperatures, i.e., T= 200 K and 500 K. The lowering of barrier width at the tunneling junction due to the presence of positive ITCs results into enhancement in the I_{ds} in both the devices as clearly marked in the **Figure 4.15(b)**. Thus, the presence of positive (negative) trap charges results in an increase (decrease) in drain current in both the aforesaid devices. Moreover, the presence of high-k material near source side, i.e., in region-1 reduces the change in V_{fb} as profound from Equation 4.1; being inversely proportional to oxide capacitance (higher in the case of HD-GAA-TFET) and thus resulting in better immunity against ITC as compared to GAA-TFET *(Madan and Chaujar, 2016).*

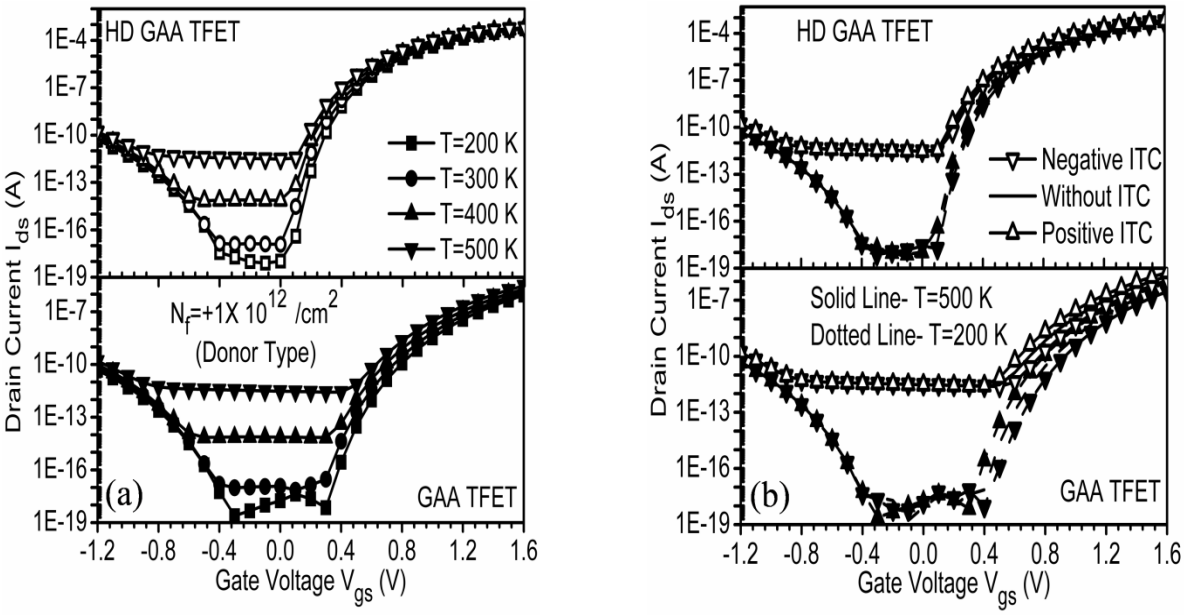

Figure 4.15 (a) Effect of temperature on drain current I_{ds} as a function of V_{gs} at V_{ds}=1.0 V and at constant donor type ITC density $N_f = 1 \times 10^{12}$ cm^{-2} for GAA-TFET and HD-GAA-TFET (b) Effect of ITC on drain current I_{ds} as a function of V_{gs} at V_{ds}=1.0 V and at constant temperatures T=200K and 500K *(Madan and Chaujar, 2017)*.

Figure 4.16(a-b) demonstrates the influence of ITC at various temperature on I_{ON} and I_{OFF} respectively of both GAA-TFET and HD-GAA-TFET. It is evident from **Figure 4.16(a)** that the I_{ON} of HD-GAA-TFET is much higher than GAA-TFET, quantitatively it is examined

that I_{ON} enhances from an order of 10^{-8}A (for GAA-TFET) to 10^{-4}A (for HD-GAA-TFET). This enhanced I_{ON} of HD-GAA-TFET is attributed to the presence of high-k material in region 1, which increases the tunneling rate of electrons and thus, the tunneling drain current. Further, with an increase in temperature, the bandgap narrowing (BGN), results in increase in the I_{ON} for both the devices. It is evaluated that the I_{ON} of HD-GAA-TFET and GAA-TFET increases by 1.8 times and 5.64 times respectively, for a rise in temperature from 200K to 500K at a constant donor trap density of $N_f=1\times10^{12}cm^{-2}$. Further, there is an increase (decrease) in I_{ON} due to the presence of donor (acceptor) ITCs. It is because the presence of positive (negative) ITC reduces (enhances) the flatband voltage, and thus results in an increase (decrease) in the effective gate voltage (V_{gs}-V_{fb}). Lowering (increasing) of the flat band voltage (V_{fb}), in turn, increases (decreases) the band bending of energy bands. This enhanced (reduced) band bending also results in lowering (higher) of tunneling barrier width *(Cao et al., 2011)* and hence enhances (reduces) the I_{ds}. Temperature affectability on I_{OFF} of both the devices is shown in **Figure 4.16(b)**. It is examined that at a higher temperature, the I_{OFF} degrades in both the devices under consideration. Results show that I_{OFF} of GAA-TFET and HD-GAA-TFET increases tremendously from an order of 10^{-18}A (at 200K) to an order of 10^{-12}A (at 500K), for an increase in temperature from 200K to 500K.

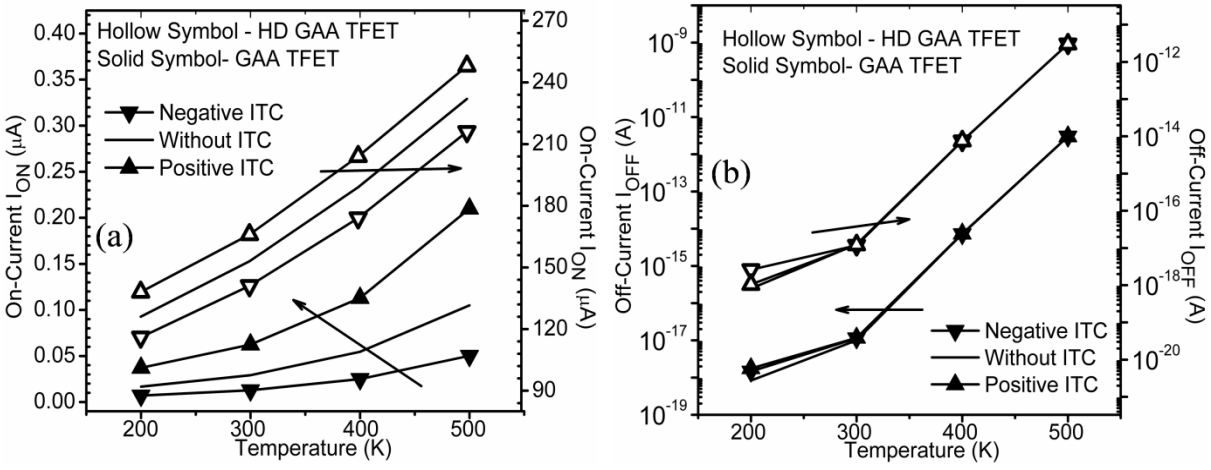

Figure 4.16 Impact of temperature and ITCs on (a) ON-state current (at V_{gs}=1.2V and V_{ds}=1.0V) and, (b) OFF-state current (at V_{gs}=0V and V_{ds}=1.0V) of GAA-TFET and HD-GAA-TFET for fixed ITC density, $N_f=\pm\ 1\times10^{12}\ cm^{-2}$, and absence of ITC *(Madan and Chaujar, 2017)*.

The significant variation in I_{OFF} is mainly due to the dominance of SRH in subthreshold regime, which has a strong dependence on temperature. However, less

temperature dependence in the superthreshold region is due to the dominance of BTBT phenomenon (which has weaker temperature dependence) at higher gate bias in both the devices *(Cheng et al., 1997, Der Agopian et al., 2012, Nirschl et al., 2004)*.

Temperature affectability and impact of ITC on I_{ON}/I_{OFF} ratio of both GAA-TFET and HD-GAA-TFET has been shown in **Figure 4.17(a)**. Significantly large I_{OFF} at higher temperatures result in tremendous degradation in switching ratio of both the devices at higher temperatures. This reduced I_{ON}/I_{OFF} ratio at high temperatures, causes the slow output transitions thereby degrading the device speed. Further, the presence of positive (negative) ITCs enhances (reduces) I_{ON}/I_{OFF} ratio. The reduction/enhancement is comparatively less in the case of HD-GAA-TFET, making it more reliable. Furthermore, the I_{ON}/I_{OFF} ratio is appreciably high in case of HD-GAA-TFET as compared to GAA-TFET, resulting in a higher device speed. BTBT at the drain-channel junction for negative gate bias leads to the ambipolar conduction of TFET. This I_{AMB} restricts the applicability and feasibility of TFET for circuit level applications. This necessitates the quantitative evaluation of I_{AMB} at elevated temperature. I_{AMB} in this work has been defined as the I_{ds} @ V_{ds}=1.0V and V_{gs}= -1.0V and is shown in **Figure 4.17(b)** for both the devices under consideration.

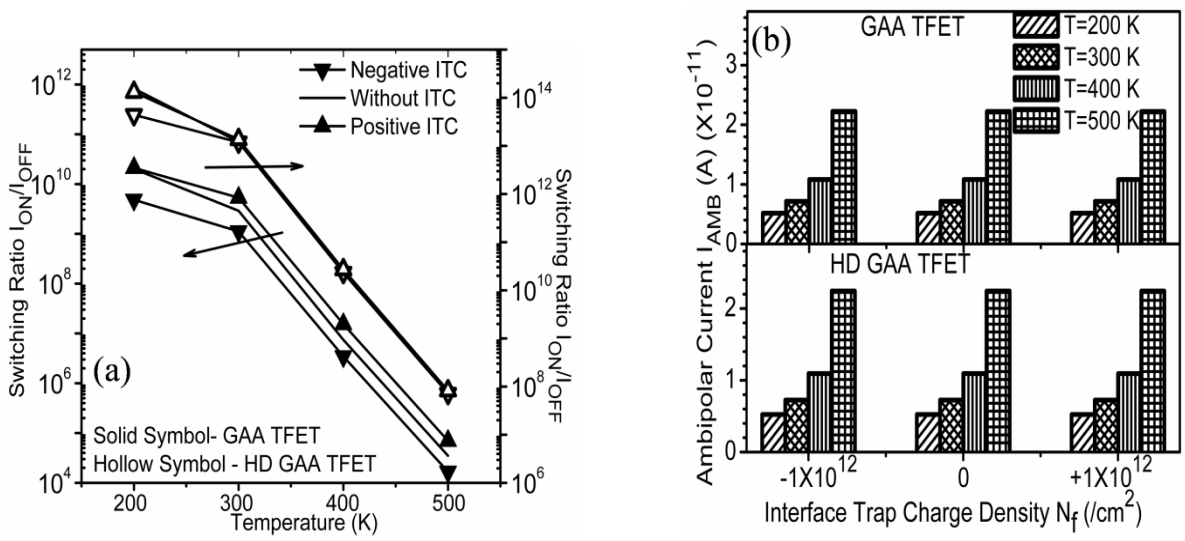

Figure 4.17 Impact of temperature and ITCs on (a) Switching ratio I_{ON}/I_{OFF} ratio and, (b) ambipolar current (at V_{gs}=-1.2 V and V_{ds}=1.0 V) for GAA-TFET and HD-GAA-TFET at fixed ITC density, $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC *(Madan and Chaujar, 2017)*.

It is obtained that the I_{AMB} is higher at elevated temperatures, due to increase in drain current with temperature. Moreover, in this chapter, the presence of ITCs is considered only

near the tunneling junction (due to the presence of high electric field), and the I_{AMB} is characterized by the drain-channel junction. Thus, the I_{AMB} is immune to the ITC as depicted in **Figure 4.17(b)**.

To analyze the effect of temperature and ITCs at high-frequency, a significant RF FOMs, i.e., cut-off frequency (f_T) has been examined. f_T is the parameter which is computed as the frequency at which the short-circuit current gain drops to unity. The unity current gain cut-off frequency f_T of both the devices under consideration is plotted as a function of temperature and for the donor, acceptor and absence of ITC in **Figure 4.18(a)**. As explained previously in this chapter, that, with an increase in temperature, BTBT rate of electrons increases thereby increasing the drain current and the transconductance of the device. Thus, f_T being directly related to the transconductance increases with a rise in temperature of both the devices. Moreover, the presence of positive (negative) ITC, enhances (lowers) the drain current and thus significantly increases (decreases) the f_T. Besides, the superior f_T is found in the case of HD-GAA-TFET in comparison to its conventional counterparts.

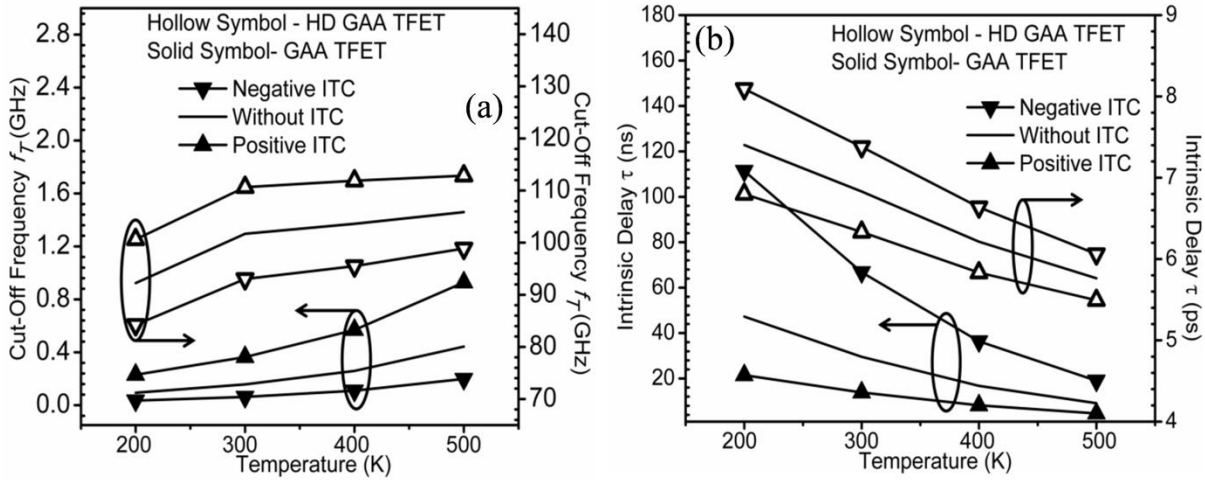

Figure 4.18 Effect of temperature on (a) cut-off frequency f_T and (b) Intrinsic delay as a function of temperature for GAA-TFET and HD-GAA-TFET at V_{ds}=1.0 V and at fixed ITC density, $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC *(Madan and Chaujar, 2017)*.

An essential parameter to benchmark the performance of transistor in circuit applications is the intrinsic delay τ, which is computed as *(Mohapatra et al., 2015)*

$$\tau = \frac{C_{gg} V_{dd}}{I_{ON}} \tag{4.11}$$

Where;

C_{gg} is the total parasitic gate capacitance,

I_{ON} is the ON-current and

V_{dd} is the drain bias voltage.

For digital logic applications, τ is a conventional metric. **Figure 4.18(b)** illustrates the comparison between GAA-TFET and HD-GAA-TFET in terms of τ w.r.t. temperature, including the influence of ITC as well. It is clearly depicted in **Figure 4.18(b)** that there is a substantial reduction in τ in case of HD-GAA-TFET in comparison with GAA-TFET for entire temperature range. Quantitatively, it is evaluated that τ reduces from an order of 10^{-8} s (for GAA-TFET) to 10^{-12} s (for HD-GAA-TFET) for whole temperature range. This reduction in τ is attributed to the higher I_{ON} in case of HD-GAA-TFET offered by the high-k material used near tunneling junction instead of SiO_2 as in case of GAA-TFET. Additionally, it is obtained at elevated temperature; τ of both the devices under consideration reduces. This reduction in τ is offered by the increase in drain current with temperature. It is calculated that for GAA-TFET, a rise in temperature from 200 K to 500 K, τ drops by 5.84 times, 5.17 times and 4.64 times for the case of presence of the acceptor, absence, and donor ITC respectively at the interface of Si-SiO_2. While, in the case of HD-GAA-TFET, the decrease in τ is by 1.33 times, 1.24 times and 1.23 times for the case of presence of the acceptor, absence, and donor ITC correspondingly.

The switching speed of FETs depends upon the parasitic capacitances, and the consequence of these parasitic capacitances cannot be overlooked at RF operations, as they determine the speed and power consumption characteristics of the device. Thus, for the designing TFET based circuits, the parasitic capacitances must be analyzed as they affect device properties such as the propagation delay and power dissipation and consequently, necessitates the quantitative examination of the parasitic capacitances. Thus in this chapter, the small signal AC analysis is done at f = 1MHz, to extract various bias dependent parasitic capacitances.

Further, as discussed in **Chapter 3** of the thesis, the capacitive distribution in case of TFET is entirely different from that of the MOSFET. In the case of TFET, the potential drop is very small at the drain-channel junction in contrast with MOSFET where a large reverse bias exists between drain-channel junction. This leads to a comparatively large gate-drain capacitance in TFET in comparison to MOSFET. Moreover, the smaller gate-source

capacitance C_{gs} (as compared with C_{gd}) in the case of TFET for entire bias situations, results into $C_{gg} \sim C_{gd}$. This is again in contrast with MOSFET in which C_{gg} is almost equally contributed by both C_{gd} and C_{gs}. The enhanced C_{gd} causes overshoot in transient response in case of digital inverter circuits *(Mookerjea et al., 2009)*. In the case of TFET, the inversion layer is formed initially at the drain side and moves towards the source side with an increase in gate bias. Thus, for TFET, C_{gd} contributes majorly to the total gate capacitance, i.e., C_{gg} in comparison to C_{gs} *(Gnani et al., 2015, Yang et al., 2010)*.

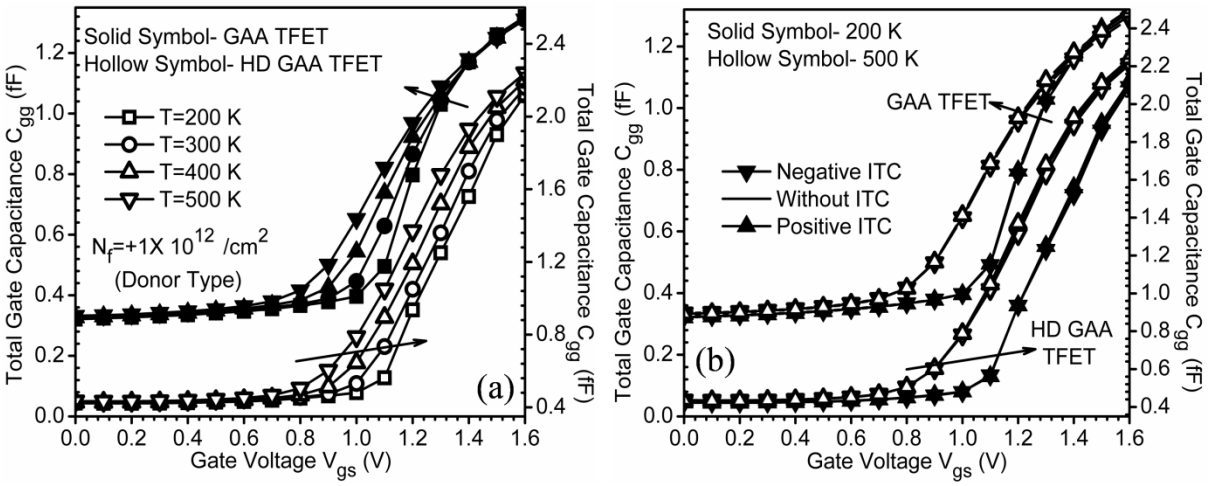

Figure 4.19 (a) Effect of temperature on total gate capacitance as a function of V_{gs} at V_{ds}=1.0 V and at constant donor type ITC density $N_f = 1 \times 10^{12}$ cm^{-2} for GAA-TFET and HD-GAA-TFET (b) Effect of ITC on total gate capacitance as a function of V_{gs} at V_{ds}=1.0 V and at constant temperatures T=200 K and 500 K at $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC *(Madan and Chaujar, 2017)*.

The influence of temperature on C_{gg} w.r.t. the V_{gs}, of the devices under consideration at a constant donor type trap density of 1×10^{12}cm^{-2} is shown in **Figure 4.19(a)**. It can be observed from **Figure 4.19(a)** that, C_{gg} increases with a rise in temperature, in both the devices under consideration. It is evaluated at V_{gs}=1.2V that with an increase in temperature from 200K to 500K, C_{gg} increases by 1.21 times and 1.45 times for GAA-TFET and HD-GAA-TFET respectively. Moreover, the consequence of the presence of high-k material near the source-channel junction in case of HD-GAA-TFET is the degradation in C_{gg} as compared to its counterparts. It is examined that, with the integration of HD engineering scheme, the degradation in C_{gg} is much smaller than the improvement in the drain current and the immunity against ITC. Consequently, the marginal increase in C_{gg} offered by the HD

engineering scheme can be overlooked against the superior drain current and the improved device reliability. **Figure 4.19(b)** shows the influence of ITC on C_{gg} of both the devices under consideration at constant temperatures viz. 200K and 500K. It is analyzed that the presence of positive (negative) ITC increases (decreases) the C_{gg}, in both the devices. Quantitatively, it is evaluated that for the case of GAA-TFET, the presence of donor (acceptor) ITC increases (decreases) the C_{gg} by 0.7% (0.7%) at 200K and by 6.0% (6.3%) at 500K. However, for HD-GAA-TFET, the presence of donor (acceptor) ITC increases (decreases) the C_{gg} by 0.1% (0.03%) at 200K and by 2.1% (2.2%) at 500K. With an increase in temperature, the parasitic gate capacitance degrades for both the devices, owing to the high leakage current, thus making the device more reliable for low temperature applications.

4.5 SUMMARY

This chapter explores the reliability issues of GAA-TFET and HD-GAA-TFET by analyzing the impact of interface traps charges such as donor (positive interface charges) and acceptor (negative interface charges) on various analog, RF and linearity parameters of the device. The results thus obtained are simultaneously compared with the case when the Si-SiO_2 interface is ideal, i.e., there are no interface traps. While analyzing the effect of interface charges on both GAA-TFET and HD-GAA-TFET, it is examined that HD-GAA-TFET is much immune to the presence of ITCs at the Si-SiO_2 interface in comparison to the GAA-TFET. Additionally, the improvement in transconductance, with the amalgamation of HD results in the enhancement of the high-frequency gain of the device. Furthermore, superior performance is obtained in terms of TFP, 1-dB compression point and zero crossover point with the amalgamation of HD engineering scheme onto GAA-TFET. Thus, HD offers collectively better immunity against ITC and thereby superior reliability along with improvement in the analog and RF performance of the GAA-TFET. As these ITCs always exists in a real device, thus study of performance degradation due to these interface charges is always needed so that device can be optimized accordingly. After analyzing the impact of ITC at room temperature, the temperature affectability over the device performance is also examined for both HD-GAA-TFET and GAA-TFET. While examining the temperature robustness, it is revealed that the reliance on temperature is bias dependent. Results show that below the threshold region, the effect of temperature is prominent due to the governance of SRH at low gate bias, which has exponential temperature dependence. However, above the

threshold regime, the BTBT phenomenon oversees which has weak temperature dependence and thus leads to smaller variations in drain current. Further, dissimilar to the case of MOSFET, a positive temperature coefficient has been obtained for the entire gate bias range in case of TFET. Moreover, the parasitic capacitances of the TFET also degrade with the rise in temperature. Thus, the characteristics of both the devices are degraded at high temperatures, indicating that device is less suitable for high-temperature applications. The suitability of HD-GAA-TFET at low temperatures can thus provide a pathway to meet the growing demand for low-temperature tolerance of the logic circuits in aircraft, space technology and for large-scale integration applications.

Till now, the ambipolar current of the GAA-TFET is not analyzed, which has implications for the applicability of TFET in digital applications. Thus, the next chapter focuses on suppression of ambipolar current and also explores the capability of GAA-TFET for gas sensing application.

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CHAPTER 5

GATE-DRAIN ENGINEERING IN HETERO GATE DIELECTRIC GAA-TFET FOR SUPPRESSED AMBIPOLAR CONDUCTION AND ITS APPLICATION AS A HYDROGEN GAS SENSOR

This chapter is broadly organized to meet two goals viz. (i) to overcome the major impediment of TFET, i.e., the inherent ambipolar conduction and (ii) to design a hydrogen gas sensor using palladium gate metal TFET. Consequently, the chapter has 2 parts; Part-1 of this chapter works on suppressing the ambipolar current (I_{AMB}). Gate-drain overlap (GDO) engineering scheme has been incorporated over the HD-GAA-TFET in order to accomplish the 1st aim, i.e., to suppress the I_{AMB}. It is explored that via GDO; I_{AMB} is reduced significantly. Consequently, the enhanced I_{ON} acquired with the amalgamation of HD scheme and reduced I_{AMB} with GDO; comprehensively upgrade the performance of GAA-TFET. Further, the optimization of GDO length (L_{ov}) has also been done to obtain a minimum I_{AMB}. Quantitative analysis of ambipolarity factor "α" reveals that at large L_{ov}, "α" improves. Nevertheless, degradation at the high frequency (HF) performance has also been observed due to enhanced parasitic capacitances with GDO. Hence, to surpass the deterioration at HF, the dielectric over GDO region has been altered and it is analyzed that by inserting a material of low-dielectric constant (k=1), parasitic capacitances of the device reduces, resulting in enhancement in f_T. Moreover, the low-k dielectric inserted over L_{ov} reduces the I_{AMB} supplementary, along with enhanced f_T. Suppressed I_{AMB} and increased f_T of GDO-HD-GAA-TFET with low-k dielectric over L_{ov} makes it adequate for application in HF and digital circuitry.

Afterwards, the hydrogen gas sensing application of HD-GAA-TFET device has been discussed as part-2 of the chapter. In this regard, a novel highly sensitive HD-GAA-TFET based H_2 Gas Sensor is designed by uniting the advantages of the band to band tunneling (BTBT) mechanism. Here, the Palladium (Pd) supported silicon dioxide (SiO_2) is used as a sensing media and sensing relies on the interaction of hydrogen with Pd-SiO_2-Si. The high surface to volume ratio in the case of cylindrical GAA structure enhances the fortuities for surface reactions between H_2 gas and Pd, and thus increases the sensitivity and stability of the sensor. The behavior of the sensor in the presence of hydrogen and at elevated temperatures is discussed. The conduction path of the sensor which is dependent on sensors radius has also been tuned for the optimized sensitivity of the sensor. Stability of the sensor with respect to temperature affectability has also been explored, and it is found that the device is reasonably stable and highly sensitive over the bearable temperature range. The successful utilization of HD-GAA-TFET in gas sensors may open a new door for the development of novel nanostructure gas sensing devices.

5.1 INTRODUCTION

Ambipolarity is an intrinsic behavior of TFET that refers to the conduction for both positive and negative gate biases at a constant drain bias. In the ambipolar region, conduction of holes (electrons) dominates for the p-type (n-type) behavior of TFET. It has grave consequences on TFET that obstructs its applicability for digital applications and also increases the leakage current. Nevertheless, the ambipolar effect has been used for sensing applications in *(Gao et al., 2016)* but, the ambipolar effect of the FET indeed limits its applications for digital inverters. It is reported that Schottky barrier (SB) transistors also suffer from the ambipolar conduction. However, the solution to reduce ambipolarity for SB transistors is comparatively simple as to choose the appropriate contacts for source and drain *(Lin et al., 2003)*. While in case of TFET, the ambipolarity is due to the lowering of barrier width at the drain-channel junction for negative gate bias. Various engineering schemes have been reported up to now to alleviate ambipolar behavior of TFET viz. a) hetero gate dielectric *(Choi and Lee, 2010, Madan and Chaujar, 2016b)*, b) gate-drain underlap or short gate TFET *(Verhulst et al., 2007)*, c) hetero-junction TFET *(Cho et al., 2011)*, d) Asymmetric source/drain doping *(Boucart and Ionescu, 2007, Madan et al., 2017b)*, and e) gate-drain overlapped TFET *(Mallik et al., 2013, Naderi and Keshavarzi, 2012)* as discussed in **Chapter 1**. Moreover, TFET has another shortcoming, i.e., lower I_{ON} (caused by lower tunneling rate of electronics) that limits its operation speed. Various techniques have been already discussed in **Chapter 1** of this thesis for enhancing the I_{ON} *(Choi and Lee, 2010, Verhulst et al., 2007).*

Thus, the 1st part of this chapter works on to meet the 1st goal, i.e., to suppress the ambipolar current (I_{AMB}) and also to enhance the I_{ON}. In this regard, gate-drain overlap (GDO) and hetero gate dielectric engineering scheme (HD) has been integrated onto GAA-TFET with an aim to acquire a comprehensively superior TFET that conquer the challenges of TFET. Specifically, GDO is used to reduce the I_{AMB} and HD is integrated to enhance the I_{ON} of GAA-TFET. Consequently, a comprehensively upgraded TFET has been acquired.

The chapter continues to discuss the applicability of the GAA-TFET for hydrogen gas (H_2) sensing as Part-2. The motivation of sensing H_2 is essentially the ever-increasing demand to reduce greenhouse emissions that comes from the inevitable need to make a transition to cleaner fuels. H_2 presents itself as one of the frontrunners in this quest for zero-emission fuels owing to its unique properties like its ability to burn with oxygen leading to the production of water as the only byproduct. Additionally, the commercial importance of H_2 is clear from its

use in a wide gamut of industries. H_2 is used as a crucial component of rocket fuel in the aerospace industry, as a coolant and to provide an inert environment in steam turbine generators, in various processes in semiconductor device fabrication and for processes like gas cutting, welding and also to produce smooth surface finish in industries like the automotive industry. With the advent of burgeoning fields like Hydrogen medicine, the importance of H_2 in the biomedical, pharmaceutical and healthcare industries cannot be undermined *(Choi et al., 2015, Hübert et al., 2011, Sun and Wang, 2007)*. However, H_2 is colorless and odorless. It burns in the presence of oxygen in the ultraviolet region of the EM spectrum making the flames invisible to human eyes. Among the many hypotheses put forth by experts who studied the Hindenburg disaster of 1937, the hydrogen hypothesis is most widely accepted, serving as a testimony to hydrogen's destructive nature, if handled carelessly *(DiLisi, 2017)*. Given the potential dangers associated with the use of H_2, it becomes imperative to develop accurate and reliable H_2 sensors before the gas becomes an integral part of our fuel economy *(Hübert et al., 2011, Cao et al., 2013)*. These gas sensors mainly work as a transducer that detects the presence of H_2 gas, measure its concentration, and produce an electrical signal that is further calibrated with the magnitude of H_2 gas concentration. Also, among various gas sensors such as catalytic sensors, semiconductor sensors, electrochemical sensors and infrared sensors; semiconductor sensors have numerous benefits and can be used for an extensive range of gases including toxic, combustible, etc. Being active semiconductor device, Field Effect Transistors (FETs) can be effectively used to fabricate sensors as they intrinsically amplify signals producing a significant change in drive current for a comparatively small change in the gate work function *(Eisele et al., 2001)*. Moreover, the low cost, high sensitivity, stability, fast response time, wide operating temperature range and reliability make it highly applicative for detection of variety of gases *(Sun and Wang, 2007, Kong et al., 2001, Mubeen et al., 2007)*. Therefore, FET based H_2 sensors are more sensitive to the parameter being sensed as compared to other H_2 sensors.

Additionally, Palladium (Pd) has a very high selectivity towards H_2 gas. Pd based gas sensor relies on the fact that after absorption of H_2 gas, a chemical species called palladium hydride is formed, which has a comparatively high electrical resistance. Apart from high selectivity, out of several catalytic metals, the sensitivity of Pd for hydrogen is highly appreciable because of the sites located at Pd-SiO_2 interface (in case of MOS architecture based FETs such as MOSFET and TFETs) along with the surface reactions, participating in

the catalytic reactions. It is also reported that at room temperature and atmospheric pressure, Pd can absorb hydrogen up to 900 times its volume *(D'amico et al., 1982, Papaconstantopoulos et al., 1978).*

The basis of sense is as follows: - when H_2 molecules interact with Pd surface, it dissociates on the surface of Pd into H atoms and some of the dissociated H-atoms diffuse into the bulk of the Pd metal. The probability of dissociation of H_2 on Pd is almost unity. Within a few nanoseconds, the diffused H-atoms reaches to the interface of Pd and SiO_2 (or the H-atoms get adsorbed at the SiO_2-Pd interface). This leads to the formation of a dipole layer at the Pd-SiO_2 interface in the device resulting in a modulation of the metal gate work function, conductivity, etc. Also, it is reported that the high sensitivity of Pd for H_2 is mainly attributed to the great polarization of H-atoms at the Pd-SiO_2 interface rather than the large diffusion of H-atoms through Pd *(Ekedahl et al., 1998, Fogelberg et al., 1995)*. Thus, the formation of dipole layer thereby results in a concomitant change in the device characteristics which depends on the polarization of H-atoms at the interface and, indirectly, on the pressure of the H_2 gas over the Pd gate. These alterations in the device characteristics are the key transduction parameter for calibration of the sensitivity of the sensor. However, the key focus of earlier research work had been to enhance sensitivity and selectively (for a particular gas) and is done by either exploring suitable sensitive films or by various device design engineering schemes. For high sensitivity and selectivity, numerous films such as metal compounds *(Dattoli et al., 2007, Li et al., 2003, Fan et al., 2004)*, polymers *(Liess et al., 1996)*, organic compounds *(Meister and Potje-Kamloth, 1997)*, hydrated salts *(Fuenzalida et al., 1999)* and catalytic metals *(Scharnagl et al., 2001b, Scharnagl et al., 2001a, Zimmer et al., 2001)* were used. In the novel device design, dual gate MOSFET; nanowire MOSFET, conventional TFET, etc. have already been taken into consideration. Additionally, to fulfill the requirement of sensing H_2 gas, silicon nanowire-based H_2 gas sensor was proposed by Cao A et al. *(Cao et al., 2013)*. Further, to obtain appreciable sensitivity, the surface of the SiNW-FET sensor was functionalized with catalytic layers of Pd nanoparticles by Bongsik Choi et al. *(Choi et al., 2015)*, for enhancing the selectivity and thus the sensitivity. Moreover, various gas sensors using metal oxide nanowires such as SnO_2, ZnO, and In_2O_3 have been reported previously. A lot of work in the field of semiconductor gas sensors has been carried out with MOSFETs. But there is a need to investigate TFET as a gas sensor, as TFET is highly suitable for low power digital CMOS applications.

Therefore, in the 2nd part of this chapter, Pd is used as the gate metal on which H_2 gas is adsorbed, and HD-GAA-TFET based hydrogen gas sensor has been proposed. In addition, the temperature stability of the device, which is a crucial parameter of any viable sensor, has also been studied. This chapter is structured as follows: - after the introductory part; the chapter continues to describe the device structure and structural parameters for both the parts of the chapter. Succeeding, the chapter describes the results in which initially the chapter deals with the ambipolar current via integrating the gate-drain overlapping scheme and then the proposed hydrogen gas sensor is examined for its sensitivity and stability. The summary of both the parts is drawn in the last section of the chapter.

5.2 DEVICE STRUCTURE AND PARAMETERS

5.2.1 SUPPRESSING AMBIPOLAR CONDUCTION

The schematic cross-sectional view of the device architectures (i.e., (a) GDO-HD-GAA-TFET, (b) GAA-TFET, (c) GDO-GAA-TFET, and (d) HD-GAA-TFET) considered in the 1st part of this chapter is shown in **Figures 5.1(a-d)** respectively. Further, the device structure parameters and their values are given in **Table 5.1**. The drain is intentionally lesser doped than the source to reduce the tunneling at the drain-channel junction for negative gate bias and thus the reduction of ambipolarity effect *(Wang et al., 2004)*. The models activated during simulation are same as discussed in **Chapter 2** of the thesis.

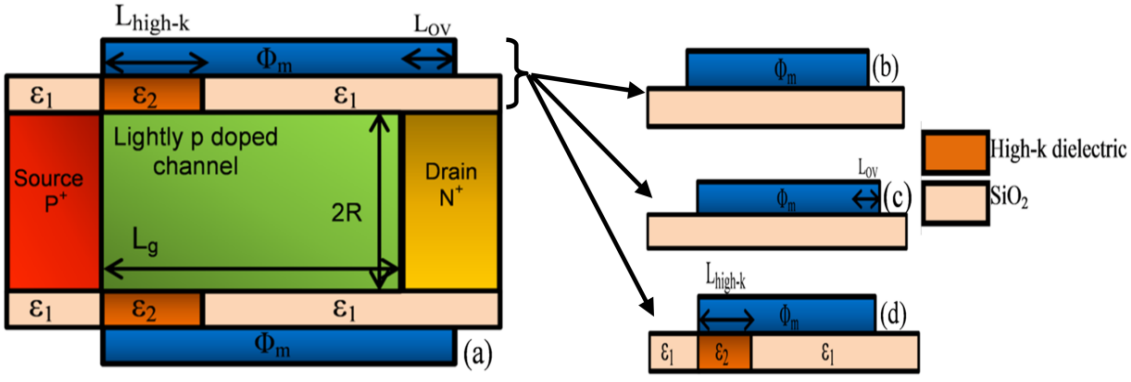


Figure 5.1 Schematic cross-sectional view of (a) gate-drain overlapped hetero gate dielectric gate all around tunnel FET (GDO-HD-GAA-TFET) (b) GAA-TFET, (c) GDO-GAA-TFET, (d) HD-GAA-TFET *(Madan and Chaujar, 2016a)*.

In addition, the experimental realization of GDO-HD-GAA-TFET can be done by integration of various previously reported process flow such as the HD dielectrics can be formed by etching SiO_2 followed by the deposition of high-k material *(Choi and Lee, 2010)* as discussed in **Chapter 2** of this thesis. Thereafter, for processing of GDO, the electron beam lithography can be used for patterning of gate metal and then the electron beam evaporation can be used for gate metallization *(Choi et al., 1991, Madan and Chaujar, 2016a).*

TABLE 5.1

DEVICE PARAMETERS AND VALUES *(Madan and Chaujar, 2016a)*.

Parameter	**Value**
Channel Length (L_g)	50nm
Channel Radius (R)	10nm
Gate oxide thickness (T_{ox})	2nm
Metal work function	4.3eV
High-k dielectric (ε_2)	HfO_2 (k=21)
ε_1	SiO_2 (k=3.9)
Length of high-k dielectric (L_{high-k})	10nm
Source doping (p^+)	$1 \times 10^{20} cm^{-3}$
Channel doping (lightly p-type)	$1 \times 10^{16} cm^{-3}$
Drain doping (n^+)	$5 \times 10^{18} cm^{-3}$

5.2.2 HYDROGEN GAS SENSOR

The basis of sensing the H_2 gas as described in the introduction section of this chapter is schematically shown in **Figure 5.2(a)**. The dissociation of H_2 molecules followed by diffusion in the Pd gate metal and then the formation of a dipole layer at the Pd-SiO_2 interface is clearly depicted in **Figure 5.2(a)**. Moreover, **Table 5.2** indicates the structural parameters of all four devices based gas sensor which are compared for the improved sensitivity. For GAA-TFET and HD-GAA-TFET, cylindrical geometry is considered as presented in **Figure 5.2(b)**. In the case of HD-GAA-TFET, the channel consists of two regions; region-1 (near the source L_1 =20nm) and region-2 (near the drain L_2=30nm). Region-1 consists of high-k dielectric (optimized value is k=21 corresponds to HfO_2) and region-2 is of low-k dielectric (SiO_2, k=3.9) whereas, in the case of GAA-TFET, the entire channel consists of SiO_2. In both the cases, radius (R) is 10nm. The models activated during simulation of TFET gas sensor are the same as discussed in **Chapter 2** of this thesis. Additionally, for conventional MOSFET

based gas sensor, models invoked for simulation are - Shockley-Read-Hall for carrier recombination, Lombardi CVT mobility model, concentration and field dependent mobility model and Boltzmann transport statistics. Both the numerical methods- Gummel (decoupled) together with Newton's (Fully coupled) have been incorporated to solve mathematically the carrier transport equation *(Manual, 2010)*. Moreover, Pd with work function 5.1eV is used as the catalytic metal gate, and gate oxide thickness is 2nm for all the cases. Unless specified the default analysis has been performed at room temperature. In addition, the work function of the Pd gate metal has been altered to incorporate the corresponding effect of change in H_2 gas pressure as reported by Sarkar et al. *(Sarkar et al., 2013)*.

Table 5.2

DEFAULT STRUCTURAL PARAMETERS FOR ALL THE DEVICES BASED GAS SENSORS *(Madan and Chaujar, 2016b)*.

Parameters / Device	Channel Length (nm)	Source doping (cm^{-3})	Drain doping (cm^{-3})	Channel/Substrate doping (cm^{-3})
Conventional MOSFET	50	n^+ -10^{19}	n^+ -10^{19}	p -10^{16}
Conventional TFET		p^+ -10^{20}	n^+ -5×10^{18}	p -10^{16}
GAA TFET		p^+ -10^{20}	n^+ -5×10^{18}	p -10^{16}
HD-GAA-TFET	50=20+30 $L=L_1+L_2$	p^+ -10^{20}	n^+ -5×10^{18}	p -10^{16}

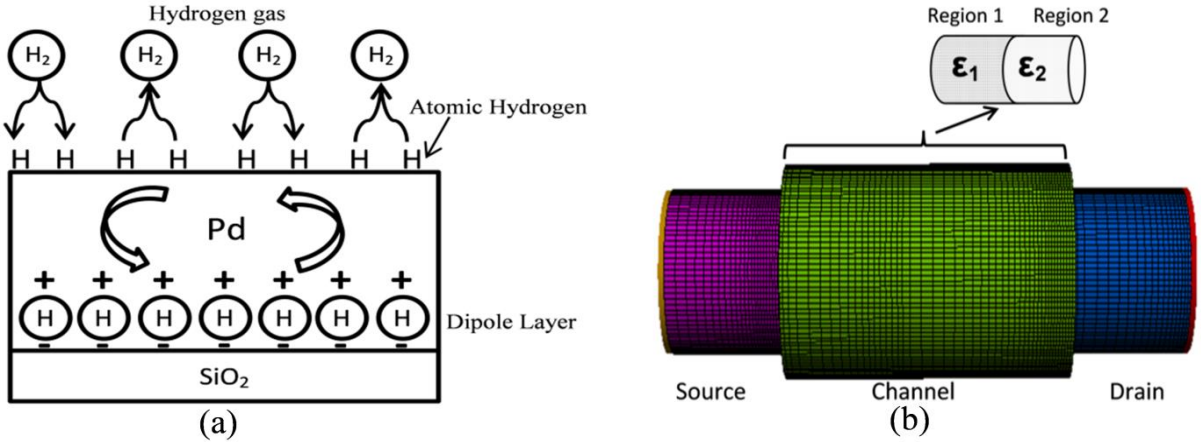


Figure 5.2 (a) Schematic of adsorption of H_2 gas molecules, diffused through Pd films and formation of dipoles at the Pd-SiO_2 interface. (b) Meshed structure of HD-GAA-TFET gas sensor *(Madan and Chaujar, 2016b)*.

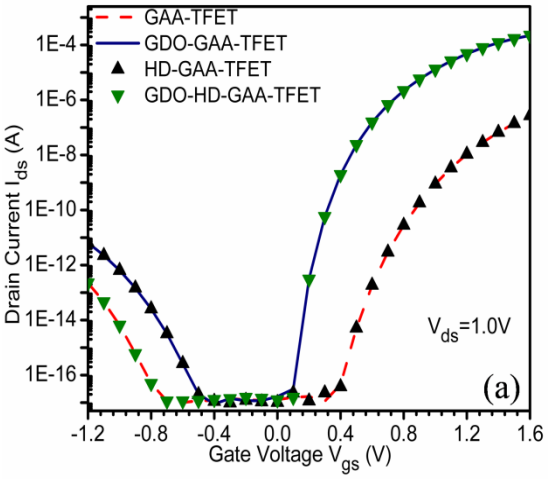
5.3 RESULTS VERIFICATION AND DISCUSSION

5.3.1 SUPPRESSING AMBIPOLAR CONDUCTION

5.3.1.1 IMPACT OF GDO AND HD ENGINEERING SCHEME

This subsection investigates the influence of GDO and HD architectures on GAA-TFET in terms of various analog and RF Figure of Merits (FOMs). First and foremost, the transfer characteristics of all the devices (stated in **Figure 5.1** on page 110) viz. GAA-TFET, GDO-GAA-TFET, HD-GAA-TFET, and GDO-HD-GAA-TFET are examined and are shown in **Figure 5.3(a)**. It is shown that GAA-TFET suffers from low I_{ON} and large I_{AMB}. The low I_{ON} of GAA-TFET is due to the wide tunneling barrier width that reduces the tunneling rate of electrons and thus the drain current. Both lower I_{ON} and large I_{AMB} restricts the practical applicability of GAA-TFET. Further, with the incorporation of GDO engineering scheme on GAA-TFET, i.e., for GDO-GAA-TFET, I_{AMB} reduces significantly from an order of 10^{-13}A to 10^{-15}A. This suppressed I_{AMB} for GDO-GAA-TFET is a consequence of the widened tunneling barrier width at the drain-channel junction offered by the overlapped gate metal over the drain. Remarkably, the drain current is unaltered in the positive gate bias range with the integration of GDO. This unaltered I_{ds} for GDO is principally due to the unaltered tunneling barrier width at the source-channel junction to the GDO. Further, the transfer characteristics of HD-GAA-TFET are also presented in **Figure 5.3(a)**, that shows a considerably large enhancement in I_{ON} from an order of 10^{-10}A to 10^{-5}A, without any variation in I_{AMB}. The enhanced I_{ON} of HD-GAA-TFET is offered by the high-k material present in the gate oxide near the tunneling junction in HD engineering scheme that translates into a steeper band bending at the tunneling junction and thereby increases the drain current *(Madan et al., 2015, Madan et al., 2017a).* However, the drain-channel junction that governs the ambipolar conduction is immune to the high-k material being present over the tunneling junction and thereby results into an unaltered I_{AMB} for HD-GAA-TFET. Subsequently, the merged merits of both GDO and HD engineering schemes have been acquired in GDO-HD-GAA-TFET that offers superior I_{ON} and I_{AMB} as is evident from **Figure 5.3(a)**. Further, a tabular representation of I_{ON}, I_{AMB}, $V_{th,}$ and SS of all the devices under consideration is shown in **Figure 5.3(b)** for quantitative assessment, where the I_{AMB} is defined as the I_{ds} @ V_{gs}=-1.0V and V_{ds}=1.0V. It is evidently shown that GAA-TFET and GDO-GAA-TFET have higher V_{th}, that is attributed to the large tunneling barrier width and lower tunneling rate of electrons. The barrier width is

reduced by integration of HD scheme on GAA-TFET, i.e., for HD-GAA-TFET and GDO-HD-GAA-TFET. The reduced barrier width via HD translates into tunneling of more electrons through the tunneling junction and subsequently reduces V_{th}. Moreover, the lower I_{ON} of GAA-TFET and GDO-GAA-TFET, fallouts into large SS. This SS is improved by the presence of the high-k material used in HD engineering scheme, i.e., for HD-GAA-TFET and GDO-HD-GAA-TFET. HD primarily enhances the I_{ON} without any negotiation in I_{OFF}, thereby provides lower SS. Thus, GDO-HD-GAA-TFET results in comprehensively upgraded analog performance and thereby may serve as a suitable candidate for high switching speed and digital applications.



Parameter / Device	I_{AMB} (A)	I_{ON} (A)	V_{TH} (V)	SS (mV/decade)
GAA-TFET	6.40×10^{-13}	8.83×10^{-10}	0.8918	48.879
GDO-GAA-TFET	6.48×10^{-15}	8.83×10^{-10}	0.89181	49.6642
HD-GAA-TFET	6.40×10^{-13}	1.31×10^{-5}	0.68013	23.9083
GDO-HD-GAA-TFET	6.49×10^{-15}	1.31×10^{-5}	0.68295	23.9542

(b)

Figure 5.3 (a) Transfer characteristics of GAA-TFET, HD-GAA-TFET, GDO-GAA-TFET and GDO-HD-GAA-TFET at constant V_{ds}=1.0V (b) Ambipolar current (I_{AMB}), ON-current (I_{ON}), threshold voltage (V_{th}) and Subthreshold swing (SS) of all the devices. For GDO architecture, L_{ov}=5nm; for HD scheme, HfO_2 is used as high-k gate dielectric ε_2=21 ***(Madan and Chaujar, 2016a)*****.**

In TFETs, the gate voltage controls the drain current and thus, the ratio of I_{ds} to the V_{gs} at constant V_{ds} defined as the transconductance or the mutual conductance (g_m) becomes an important performance parameter for TFET. High g_m is required for obtaining a high gain or large driving capability. The g_m of all the device architectures under consideration is shown in **Figure 5.4(a)**. Noteworthy improvement in g_m is achieved with the integration of HD engineering scheme onto GAA-TFET as evident from **Figure 5.4(a)**. Additionally, the similar g_m of GAA-TFET/GDO-GAA-TFET and HD-GAA-TFET/GDO-HD-GAA-TFET is ascribed to the similar transfer characteristics of these architectures in positive gate bias regime as described in **Figure 5.3(a)**. Furthermore, as the switching speed of TFET is affected by the

parasitic capacitances, so it is essential to explore the influence of both, HD and GDO engineering on the parasitic capacitances. Thus, the parasitic capacitances of all the devices under consideration are examined in terms of the gate to source capacitance (C_{gs}) and the total gate capacitance (C_{gg}) and is presented in **Figure 5.4(b)**. As explained in **Chapter 3** that in TFET, C_{gd} contributes majorly to C_{gg} is evident from **Figure 5.4(b)**, i.e., C_{gs} is considerably smaller than C_{gg} for all the cases *(Yang et al., 2010)*. It is obtained that HD degrades C_{gg} and C_{gs}. Thus, there is a need to tradeoff between the I_{ON} and the parasitic capacitance of TFET depending upon its applicability. Again the similar profile of C_{gs} for the case of GAA-TFET/GDO-GAA-TFET and HD-GAA-TFET/GDO-HD-GAA-TFET is due to the fact that GDO architecture (amalgamated for suppressing I_{AMB}), is at the drain-channel junction and it thus doesn't affect the C_{gs}.

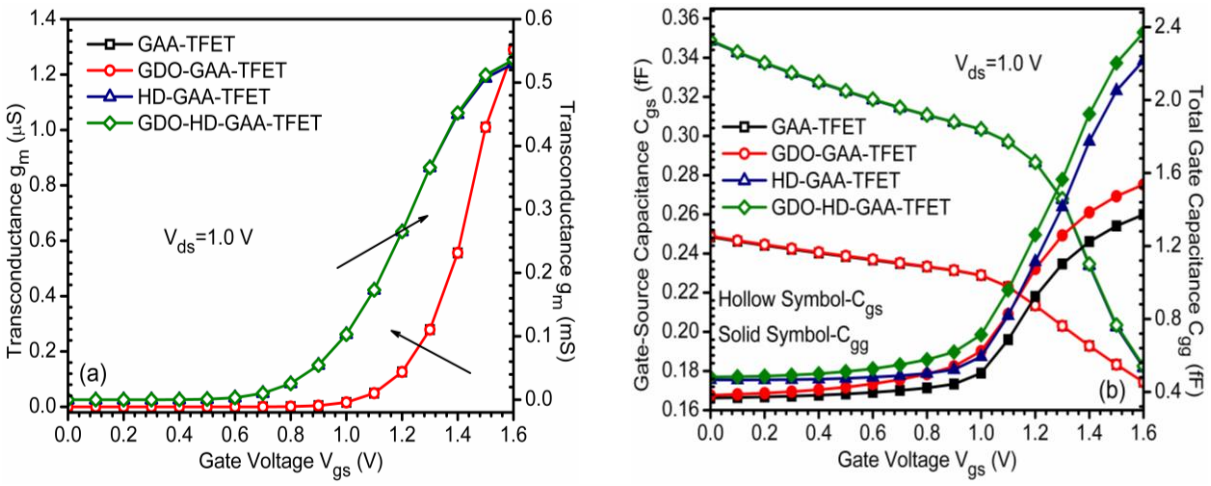


Figure 5.4 (a) Transconductance (b) Gate to source capacitance (C_{gs}) and total gate capacitance (C_{gg}) of GAA-TFET, HD-GAA-TFET, GDO-GAA-TFET and GDO-HD-GAA-TFET at constant V_{ds}=1.0V. For GDO architecture, L_{ov}=5nm; for HD scheme, HfO_2 ε_2=21 is used as high-k gate dielectric *(Madan and Chaujar, 2016a).*

To examine the high-frequency performance, the cut-off frequency (f_T) of all the devices is investigated. f_T is defined as the frequency at which the short-circuit current gain drops to 0dB, and mathematically it is stated as *(Kaur et al., 2007)*:-

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{5.1}$$

Where;

g_m is the transconductance,

C_{gs} and C_{gd} are gate to source and gate to drain capacitance.

As apparent from Equation 5.1, f_T depends directly on g_m and inversely on the parasitic capacitances. It is evidently shown in **Figure 5.5(a)** that the degradation in C_{gg} with HD engineering scheme has been overcome by the superior g_m. Consequently, the dominated g_m results in superior f_T for both GDO-HD-GAA-TFET and HD-GAA-TFET. Further, the peak value of f_T, increases remarkably from 0.15GHz to 38GHz, with the incorporation of HD engineering scheme.

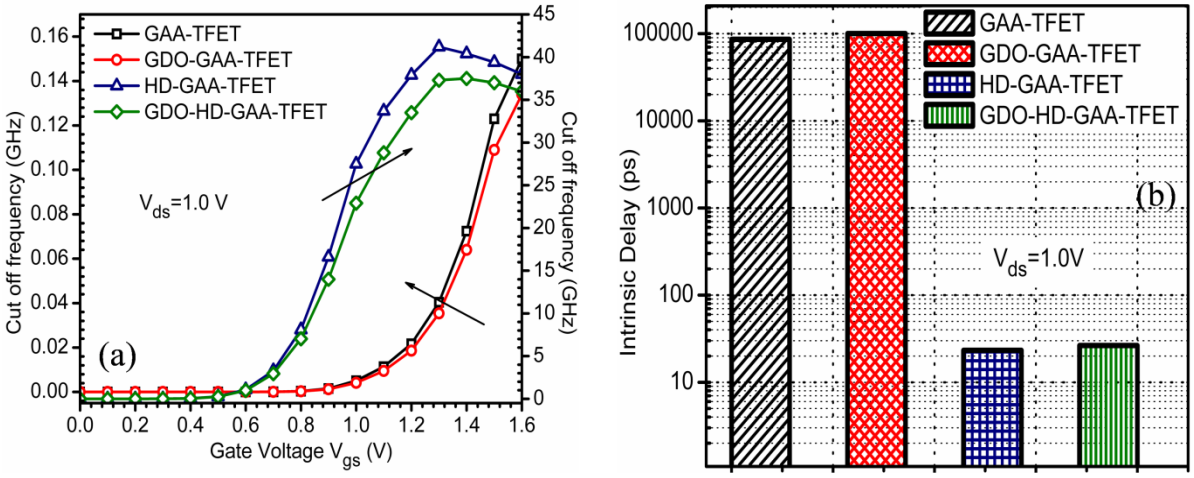


Figure 5.5 (a) Cut off frequency (f_T), (b) intrinsic delay (τ) of GAA-TFET, HD-GAA-TFET, GDO-GAA-TFET, and GDO-HD-GAA-TFET. For GDO architecture, L_{ov}=5nm; for HD scheme, HfO_2 $\mathfrak{E}_2$=21 is used as high-k gate dielectric *(Madan and Chaujar, 2016a)*.

Another vital performance parameter for assessment of the switching speed is the intrinsic delay (τ), mathematically equated as *(Mohapatra et al., 2015)*:-

$$\tau = \frac{C_{gg} V_{dd}}{I_{ON}} \tag{5.2}$$

Figure 5.5(b) shows the τ of all the device architectures. Tremendous reduction in τ has been acquired via integration of HD engineering scheme. The reduced τ for HD-GAA-TFET and GDO-HD-GAA-TFET is offered by the enhanced I_{ON} owing to the presence of high-k and inverse reliance of τ with I_{ON}. It is examined that the enhanced I_{ON} rules over the degraded parasitic capacitance, and thus improves the τ of HD-GAA-TFET and GDO-HD-GAA-TFET. Quantitatively, τ of HD-GAA-TFET and GDO-HD-GAA-TFET reduces to 20ps in comparison to τ of GAA-TFET and GDO-GAA-TFET for which τ is 100ns.

5.3.1.2 IMPACT OF GATE-DRAIN OVERLAP LENGTH (L_{ov}) ON GDO-HD-GAA-TFET

This section of the chapter examines the effect of L_{ov} on the performance of GDO-HD-GAA-TFET. **Figure 5.6(a)** illustrates the influence of L_{ov} on the transfer characteristics of GDO-HD-GAA-TFET. It is apparently shown in **Figure 5.6(a)** that the ON-state characteristic is immune to the variations of L_{ov}. The immunity of drain current against L_{ov} in positive gate bias region essentially lies in the fact that the overlapping near drain channel junction doesn't influence the tunneling junction that principally controls the ON-state characteristics. The main advantage of variant L_{ov} is for negative $V_{gs,}$ i.e., suppression of I_{AMB} with increase in L_{ov} as is clearly evident from **Figure 5.6(a)**. The reduced I_{AMB} with increase in L_{ov} is attributed to the improved effective control over the barrier width at the drain-channel junction for negative V_{gs} at higher L_{ov}. Also, it is obtained that the I_{AMB} is considerably large ~ 10^{-11}A at L_{ov} =0 nm (i.e., with no gate-drain overlapping), and is essentially due to narrowing of barrier width at the drain-channel junction for negative V_{gs}.

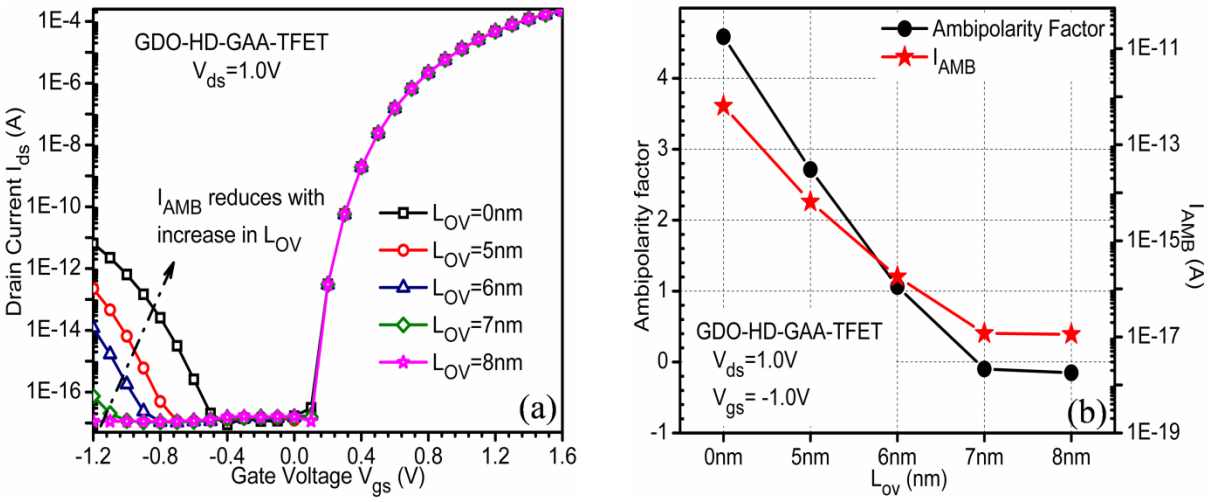


Figure 5.6 (a) Transfer characteristics of GDO-HD-GAA-TFET at constant V_{ds}=1.0V for various L_{OV}=0, 5, 6, 7 and 8nm (b) Ambipolar current and ambipolarity factor for all the cases *(Madan and Chaujar, 2016a)*.

Additionally, to compute the efficiency of GDO-HD-GAA-TFET, ambipolarity factor (α) is studied and is evaluated as *(Shaker et al., 2015)*.

$$\alpha = \log\left(\frac{I_{AMB}}{I_{OFF}}\right) \tag{5.3}$$

The influence of L_{ov} on I_{AMB} and α of GDO-HD-GAA-TFET is shown in **Figure 5.6(b)**. It has been observed that with an increase in L_{ov} from 0nm to 8nm, I_{AMB} reduces considerably from an order of 10^{-12}A to 10^{-17}A as evident from **Figure 5.6(b)**. Negative (or less value) of α demonstrates suppressed ambipolar conduction. As clearly shown in **Figure 5.6(b)**, a substantial reduction in α has been acquired with increase in L_{ov}. Furthermore, for L_{ov} =7nm and 8nm, α becomes negative indicating that there is no effect of ambipolar conduction in the analog performance.

The suppressed I_{AMB} with increase in L_{ov} can be better understood by examining the energy band diagram of GDO-HD-GAA-TFET at V_{gs}=-1.2V and V_{ds}=1.0V as presented in **Figure 5.7**. It must be pointed that the influence of L_{ov} on energy bands are concentrated only at the drain-channel junction. For negative V_{gs}, the bands near the drain are pulled upwards with an increase in L_{ov}, resulting into the broadening of tunneling barrier width at the drain channel junction. This broadened barrier width at the drain channel junction reduces the probability of tunneling of electrons at the drain channel junction and thus reduces the I_{AMB} as revealed in **Figure 5.6(a)** on page 117.

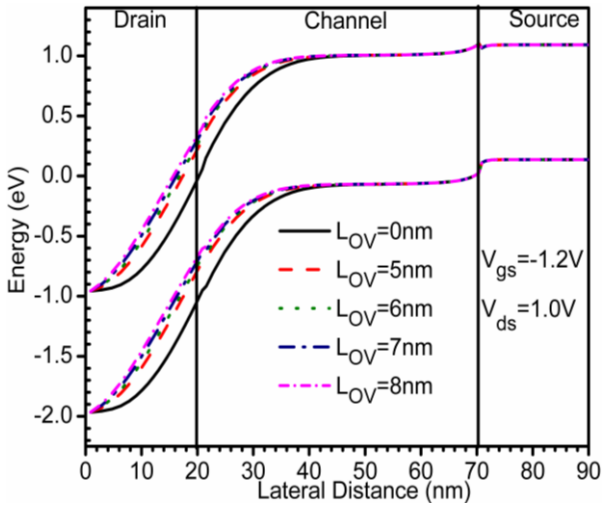


Figure 5.7 Energy band diagram along the channel length of GDO-HD-GAA-TFET at constant V_{ds}=1.0V and V_{gs}=-1.2V for various L_{OV}=0, 5, 6, 7 and 8nm *(Madan and Chaujar, 2016a)*.

The plot of electric field at a constant V_{gs}=-1.2V and V_{ds}=1.0V has also been examined and is displayed in **Figure 5.8(a)**. Because of the negative gate bias, the peak value of electric field at the drain channel junction is much higher than at the tunneling junction. Moreover, at the drain channel junction, the electric field is maximum for the case when no

gate-drain overlapping has been done, i.e., L_{ov}=0nm. Gradual reduction in the peak value of electric field at the drain channel junction has been obtained with increase in L_{ov}. This reduced electric field at the drain-channel junction is liable for the reduction in BTBT rate of electrons at the drain channel junction as shown in **Figure 5.8(b)**. Thus, the I_{AMB} is reduced with increasing L_{ov}.

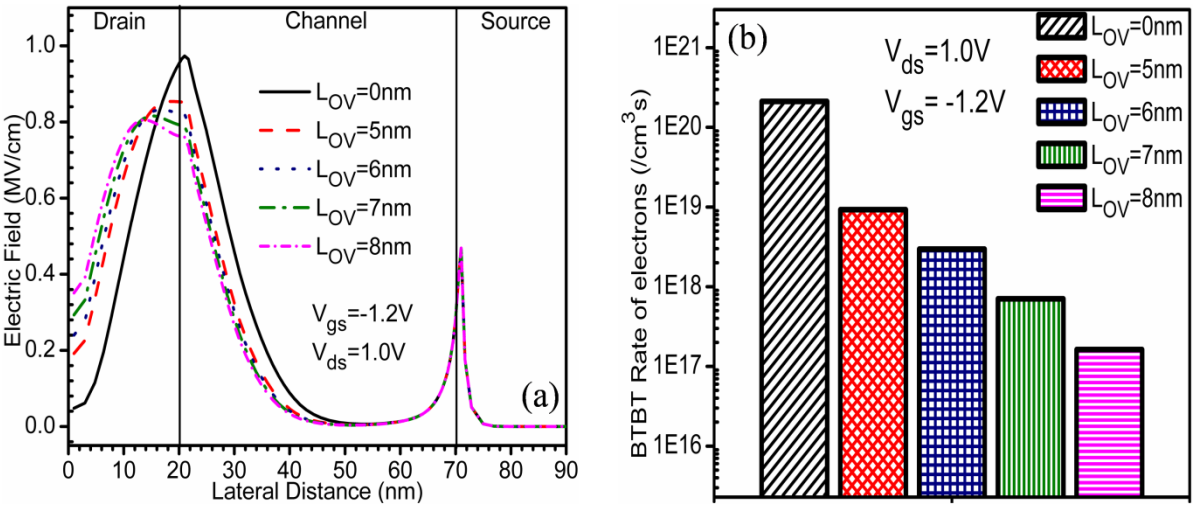


Figure 5.8 (a) Electric field along the channel length of GDO-HD-GAA-TFET at V_{ds}=1.0V and V_{gs}=-1.2V for various L_{OV}=0, 5, 6, 7 and 8nm (b) BTBT rate of electrons at the drain channel junction for all the cases *(Madan and Chaujar, 2016a)*.

The circuit performance of TFET is substantially affected by the intrinsic parasitic capacitance that confines the upper switching speed of the device. Moreover, the influence of these intrinsic parasitic capacitances can't be overlooked at HF operating regime. Additionally, in this part of the chapter, the gate oxide is being overlapped over drain (i.e., GDO engineering scheme), thus it is needed to examine the influence of drain overlapped capacitance (C_{dov}) over the gate-drain capacitance (C_{gd}) and hence, the total gate capacitance (C_{gg}) as C_{gd} is dependent on C_{dov}:-

$$C_{gd} = C_{of} + C_{dif} + C_{sif} + C_{dov} + C_{gd,inv} \tag{5.4}$$

Where;

C_{of} is the outer fringing capacitance,

C_{dif} and C_{sif} are the inner fringing capacitances at drain and source sides respectively.

Another essential parameter for assessing the HF performance of the device is the cut-off frequency (f_T). Thus, the influence of L_{ov} on the intrinsic parasitic capacitances and f_T has

also been examined and is shown in **Figure 5.9(a)** and **Figure 5.9(b)** respectively for GDO-HD-GAA-TFET. The same profile and magnitude of both C_{gg} and C_{gd} are mainly attributed to the fact that for TFET significant fraction of C_{gg} is contributed by C_{gd} as compared to C_{gs} *(Mookerjea et al., 2009)* also described previously in this **Chapter 3**. Further, as L_{ov} increases, the parasitic capacitance increases, thus resulting in decrease in f_T as shown in **Figure 5.9(a)** and **Figure 5.9(b)**. However, the decrease is only of 9% and 12% for L_{ov}=5nm and 8nm respectively.

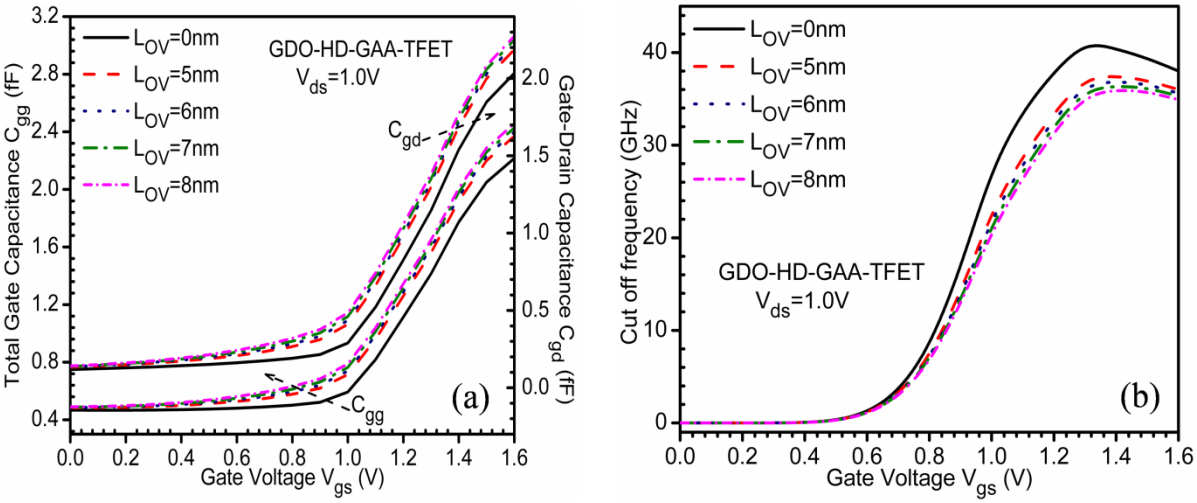


Figure 5.9 (a) Total gate capacitance, gate-drain capacitance and (b) Cut-off frequency of GDO-HD-GAA-TFET at V_{ds}=1.0V for various L_{OV}=0, 5, 6, 7 and 8nm *(Madan and Chaujar, 2016a)*.

5.3.1.3 IMPROVING THE HF PERFORMANCE OF GDO-HD-GAA-TFET

To surpass the degradation on f_T caused by GDO, the dielectric over GDO region has been altered from SiO_2 to Si_3N_4 (k=7.5) and to vacuum dielectric (k=1). C_{gg} is thus examined for various dielectrics over L_{ov} and is illustrated in **Figure 5.10(a)**. It is evident from **Figure 5.10(a)** that dielectric (inserted over L_{ov}) directly translates C_{gg}. Thus, the degradation instigated by GDO is replenished, by inserting a vacuum dielectric over L_{ov}. Additionally, the C_{gg} of GDO-HD-GAA-TFET with high-k over L_{ov} is also compared with HD-GAA-TFET. It is realized that the integration of GDO scheme increases the C_{gg} insignificantly. This degradation of parasitic capacitances however, can be overlooked in comparison with the decrease in ambipolar conduction that blocks the application of TFET in digital circuitry. The influence of inserted dielectric over L_{ov} on f_T is displayed in **Figure 5.10(b)**. f_T being inversely proportional to C_{gg} is thus enhanced with the presence of vacuum dielectric over L_{ov}. It is

evaluated that the peak value of f_T increases by 6.2% for the presence of vacuum dielectric over L_{ov} in comparison to SiO_2. Moreover, to comprehend the influence of GDO, f_T of HD-GAA-TFET is also analyzed. It is obtained that f_T degrades marginally with the amalgamation of GDO architecture. This degradation in f_T with the incorporation of GDO is offered by the enhanced parasitic capacitances for GDO (as presented in **Figure 5.10(a)**).

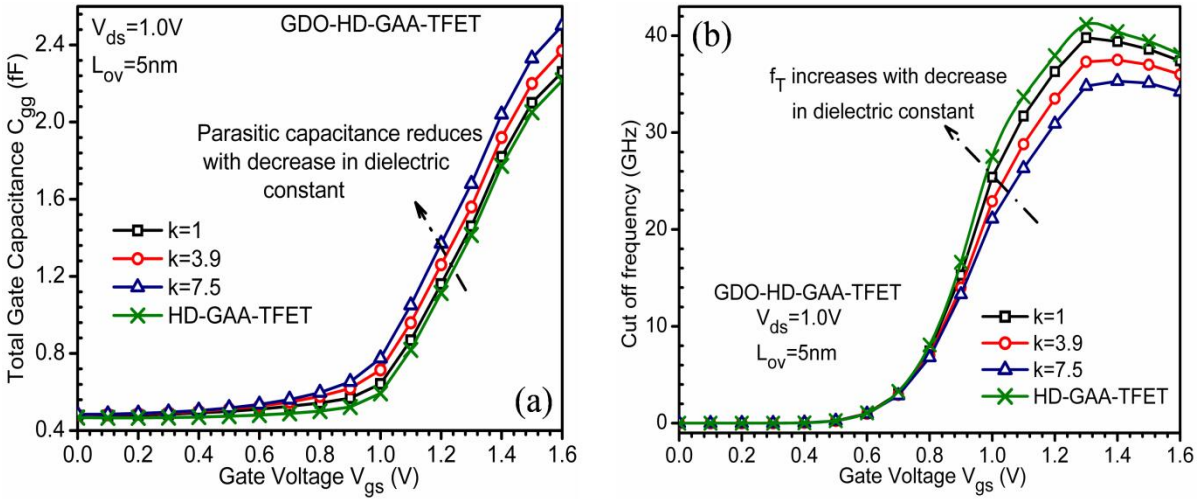


Figure 5.10 (a) Total gate capacitance and (b) Cut-off frequency of GDO-HD-GAA-TFET at V_{ds}=1.0V for L_{OV}=5nm and various dielectric materials *(Madan and Chaujar, 2016a)*.

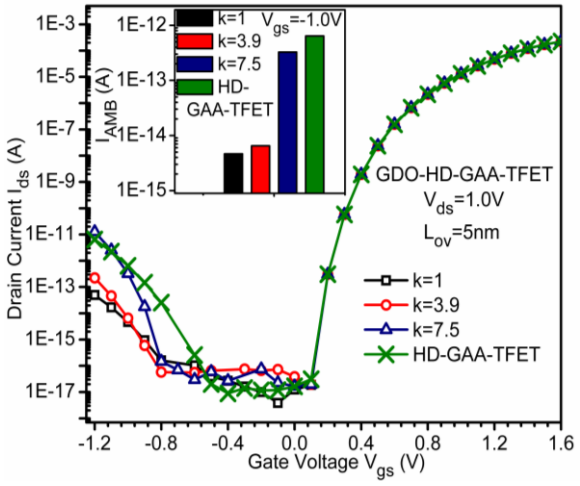


Figure 5.11 Transfer characteristics of GDO-HD-GAA-TFET at V_{ds}=1.0V for L_{ov}=5nm and various dielectric materials *(Madan and Chaujar, 2016a)*.

To evaluate the influence of inserted dielectric constant over L_{ov} region on the ambipolar characteristics, the transfer characteristics of GDO-HD-GAA-TFET with various

dielectric constants over L_{ov} region along with drain current of HD-GAA-TFET is investigated and is presented in **Figure 5.11**. It is obtained that for Si_3N_4, I_{AMB} is increased by 50.18 times and for the insertion of vacuum over L_{ov}, I_{AMB} is reduced by 1.39 times. It is examined that for HD-GAA-TFET, the I_{AMB} is significantly increased as compared to GDO-HD-GAA-TFET. The reduction in I_{AMB} is also shown in the inset of **Figure 5.11**. It is evident from the inset that the I_{AMB} of HD-GAA-TFET is remarkably higher in comparison with GDO-GAA-TFET. Suppressed I_{AMB} and enhanced f_T of GDO-HD-GAA-TFET with low-k dielectric over L_{ov} makes it eligible for application of digital circuitry.

5.3.2 H_2 GAS SENSOR: - SENSITIVITY ANALYSIS

5.3.2.1 DEVICE COMPARISON

This section of the chapter deals with the results of part-II of the chapter viz. designing of a hydrogen gas sensor. In this regard, the sensitivity (S) of the proposed gas sensor is defined as *(Sarkar et al., 2013)*;

$$S = \frac{I_{After\ gas\ adsortion} - I_{Before\ gas\ adsortion}}{I_{Before\ gas\ adsortion}} \tag{5.05}$$

Where;

I_{before} gas adsorption and I_{after} gas adsorption are the Ids before and after the gas adsorption respectively.

First and foremost, a comparative analysis of sensitivity towards H_2 gas has been done among 4 devices, as mentioned in **Table 5.2** on page 112 viz. conventional MOSFET, conventional TFET, GAA-TFET, and HD-GAA-TFET. The pressure range of H_2 gas (i.e. 1×10^{-15}Torr to 1×10^{-10}Torr) is chosen in accordance with data given by Sarkar et al. in *(Sarkar et al., 2013)*. The sensitivity is plotted as a function of gas pressure for the aforementioned FETs and is shown in **Figure 5.12**. It is acquired that the sensitivity of either of the TFET is higher in comparison to conventional MOSFET over the entire pressure range. The improved sensitivity in case of TFET is essentially due to the fact that TFET chokes the restriction of subthreshold swing (SS), i.e., limited to 60mV/decade in MOSFET. This limited SS of MOSFET confines the sensitivity of the sensor as is clearly depicted in **Figure 5.12**. Furthermore, at a pressure of 1×10^{-10} Torr, the sensitivity of conventional TFET is considerably higher than conventional MOSFET (numerically 626 times greater). Moreover,

with the amalgamation of GAA structure, the sensitivity is further enhanced by almost 3 times in comparison to conventional TFET. This increased sensitivity is offered by the enhanced gate controllability with cylindrical GAA geometry. Further, the higher surface to volume ratio of cylindrical architecture of GAA-TFET increases the probability of diffusion of H-atoms (which are dissociated) through the Pd, and therefore enhances the number of dipoles formed at the Pd-SiO_2 interface, thereby enhancing sensitivity of the sensor. Furthermore, the incorporation of HD scheme onto GAA architecture, i.e., for HD-GAA-TFET, the sensitivity is further improved. It is evaluated that at pressure of 1×10^{-10} Torr, the sensitivity of HD-GAA-TFET is 3.5×10^4 times, 56 times and 30 times higher in comparison with conventional MOSFET, conventional TFET, and GAA-TFET respectively. Enhanced sensitivity with the application of HD scheme is mainly due to the enhanced surface potential that translates in higher band bending at the tunneling junction, and thus increases the BTBT rate of electrons and drain current of the sensor.

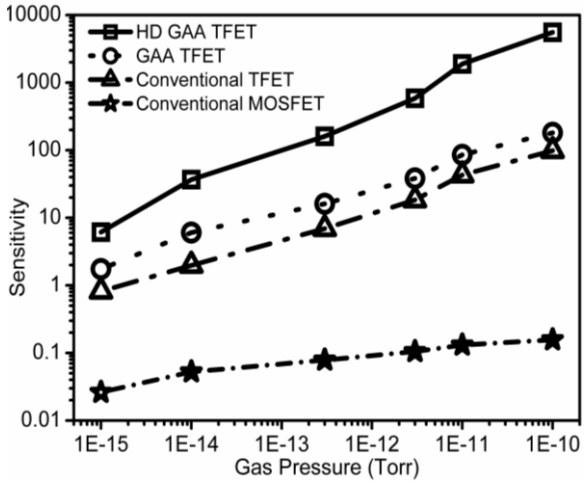


Figure 5.12 Sensitivity comparison of conventional MOSFET, conventional TFET, GAA-TFET and HD-GAA-TFET as a function of gas pressure *(Madan and Chaujar, 2016b)*.

5.3.2.2 IMPACT OF RADIUS AND TEMPERATURE

As among the various sensors, HD-GAA-TFET is highly sensitive and thus the rest of the chapter deals with HD-GAA-TFET based H_2 gas sensor. As the conduction path of the cylindrical GAA-TFET is essentially affected by the radius of the channel, thus it is needed to examine the influence of channel radius on the sensitivity of the proposed gas sensor. The influence of the radius of silicon pillar has been investigated by taking three different radii

such as 5nm, 10nm, and 15nm as demonstrated in **Figure 5.13(a)**. Results show that as the radius is reduced from 10nm to 5nm, the sensitivity of the sensor reduces extensively by many orders. This reduced sensitivity is essentially due to the reduced probability of surface reactions at the Pd surface (because of the reduction in surface area) with the H_2 gas molecules. Furthermore, with increase in channel radius from 10nm to 15nm, the sensitivity of the proposed gas sensor doesn't increase expressively. It is because the higher radius of the sensor enhances the surface area, but on the other side, it reduces the gate controllability over the channel. Thus, for the proposed gas sensor at radius of 10nm the sensor is optimized for superior sensitivity.

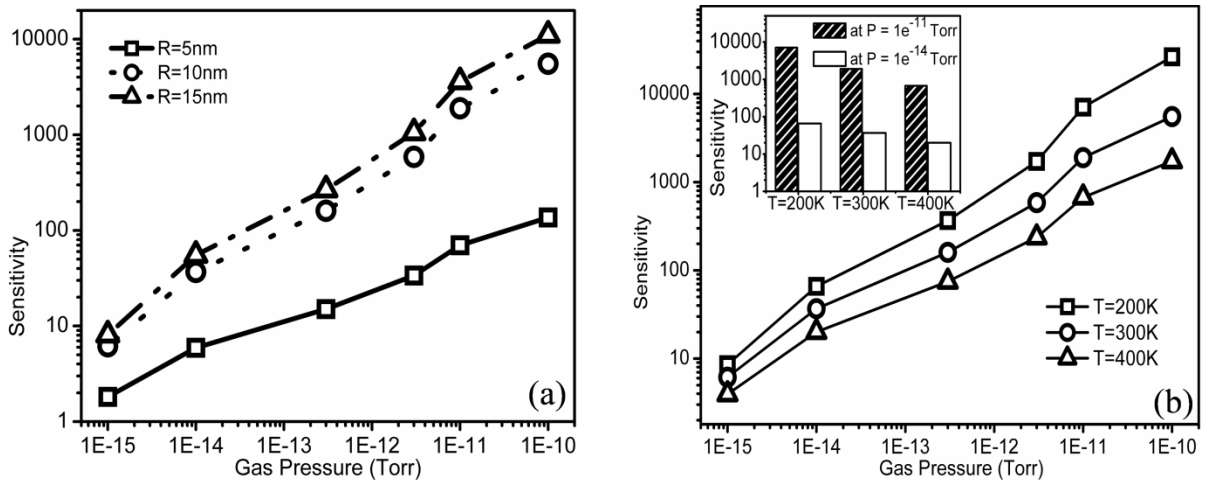


Figure 5.13 Sensitivity comparison of HD-GAA-TFET as a function of gas pressure at (a) different radius (b) various temperatures. ***Inset:*** **- Sensitivity at constant pressures values at temperature= 200K, 300K and 400K for HD-GAA-TFET** ***(Madan and Chaujar, 2016b)*****.**

Moreover, as the properties of the semiconductor, surface reactions between gas and catalytic metal are reliant on temperature, therefore it is a required to examine the influence of temperature so as to evaluate the temperature robustness of the proposed gas sensor. Furthermore, for stable operation of a sensor, the sensor should be least affected by the temperature variations. It is apparent from **Figure 5.13(b)** that at low pressure, the sensitivity is least affected by temperature whereas, at higher pressure, the effect of temperature is reasonably large. Overall, the sensor has an endurable stable response to H_2 gas over a wide temperature range that shows the viability of the sensor. The reduced sensitivity at elevated temperatures is attributed to the reduced H_2 coverage over the catalytic metal (Pd) that leads to reduction in sensitivity. Additionally, the influence of temperature at constant pressure is

shown in the inset of **Figure 5.13(b)** that shows small dependence of sensitivity on temperature at low pressure.

5.3.3 H_2 GAS SENSOR: -STATIC PERFORMANCE ANALYSIS

5.3.3.1 IMPACT OF TEMPERATURE

After exploring the sensitivity of the sensor, the influence of temperature on basic static performance parameters of sensor such as BTBT of electrons, threshold voltage (V_{th}), and SS is assessed. **Figures 5.14 (a-b)** shows the BTBT rate of electrons, V_{th} and SS of the HD-GAA-TFET H_2 gas sensor. It is noticeable from **Figure 5.14(a)** that the BTBT rate is higher when gas is present, as compared to the case when no gas molecules are there. Further, for low pressure, less number of H-atoms are diffused through the Pd-gate, followed by the lesser number of dipoles formations at the Pd-SiO_2 interface. Therefore, relatively less band bending will take place in the channel, resulting in lowering of BTBT rate. Moreover, with an increase in the gas pressure, more number of H-atoms are diffused through the Pd surface that enhances the number of dipoles formed at the Pd-SiO_2, thus lowers the barrier width at the tunneling junction and results in higher BTBT rate as is apparent from **Figure 5.14(a)**. With an increase in the temperature, the BTBT rate of electrons increases, since increase in temperature changes the properties of the semiconductor as well as the reaction rate between the gas and catalytic metal.

Figure 5.14(b) illustrates the influence of temperature on the V_{th} and SS of HD-GAA-TFET H_2 gas sensor. Results show that when no H_2 gas molecules are present, or the dipoles at the Pd-SiO_2 interface are not formed, the V_{th} of the sensor is comparatively large. It is attributed to the lower BTBT rate of electrons when the gas is absent, as depicted in **Figure 5.14(a)**. Moreover, as the pressure of the gas increases, the V_{th} of the sensor decreases, because of the aforesaid reason. Lastly, the influence of temperature and gas pressure is examined on the SS of HD-GAA-TFET H_2 gas sensor. It must be noted that the SS of HD-GAA-TFET gas sensor has overcome the fundamental limit of the MOSFET, i.e., limitation of 60mV/decade, for entire temperature range and at any gas pressure. The SS increases with an increase in gas pressure which is implicitly understood by the formerly mentioned reasons. Moreover, with an increase in temperature, the SS of the sensor increases. Thus, there is a trade-off between improved sensitivity and improved static performance at high temperatures.

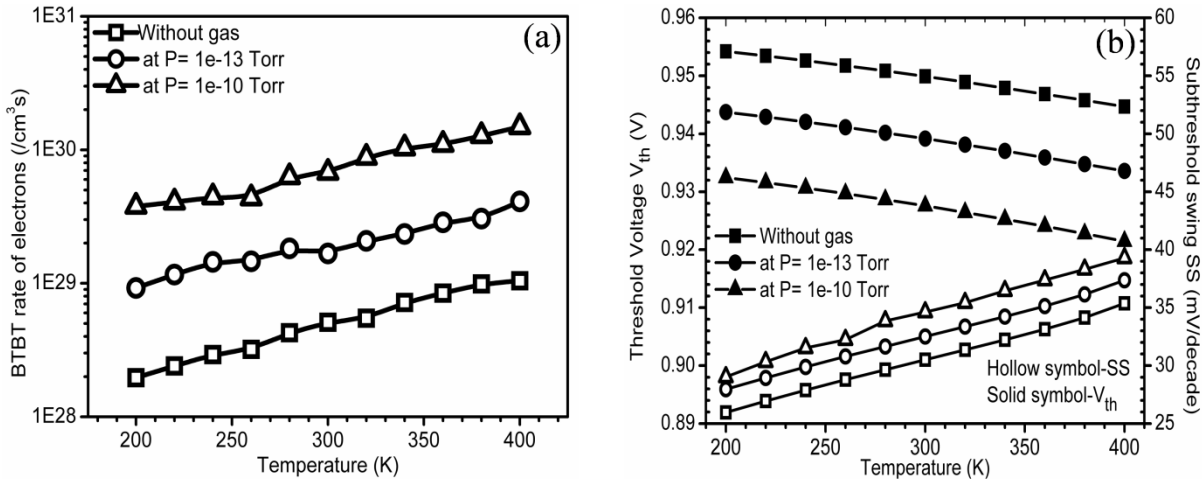


Figure 5.14 Influence of temperature variations on (a) BTBT rate of electrons, (b) V_{th} and SS of HD-GAA-TFET gas sensor with radius R=10nm at constant gas pressures *(Madan and Chaujar, 2016b)*.

5.3.3.2 IMPACT OF RADIUS

After investigating the influence of temperature, effect of channel radius of cylindrical GAA structure at constant gas pressures has been examined on the static performance of H_2-gas sensor. Impact of channel radius on BTBT rate of electrons for three cases can be realized in **Figure 5.15(a)**. It is clearly depicted that with reduction in channel radius, the BTBT rate enhances considerably. This rise in BTBT rate of electrons is mainly attributed to higher band bending at lower channel radius, which increases the probability of tunneling of electrons at the tunneling junction, and thus the BTBT rate of electrons.

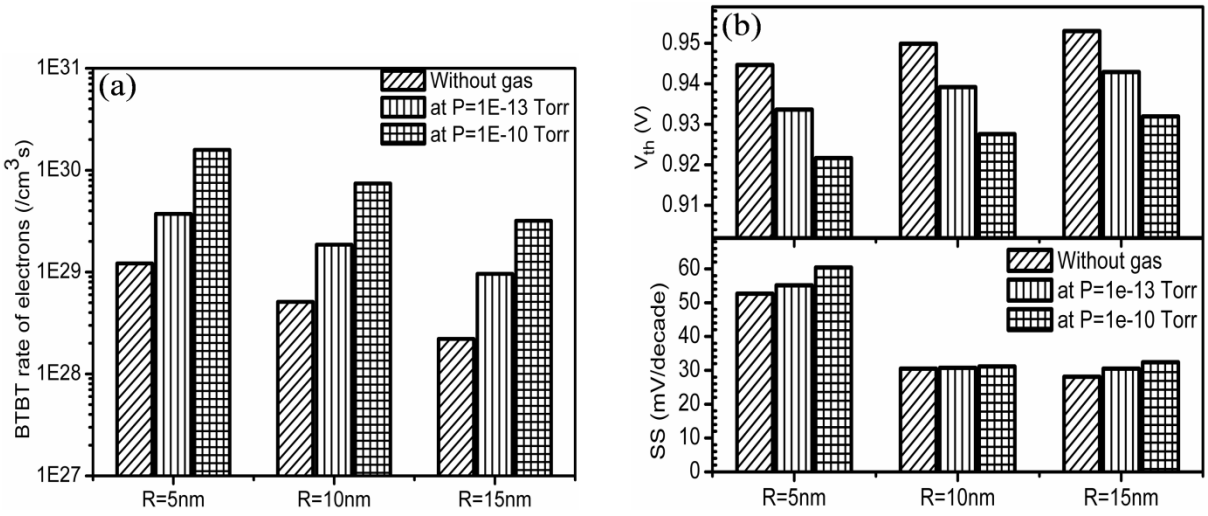


Figure 5.15 Effect of radius variations on (a) BTBT rate of electrons, (b) V_{th} and SS of HD-GAA-TFET gas sensor at T=300K and at constant gas pressures *(Madan and Chaujar, 2016b)*.

Furthermore, it is demonstrated that an increase in gas pressure results in a noteworthy enhancement in BTBT. As the pressure of the gas increases, more band bending occurs at the tunneling junction and consequently results in an increase of BTBT rate of electrons at different radii. The influence of gas pressure and channel radius on the V_{th} and SS has also been analyzed and is shown in **Figure 5.15(b)**. The increase in BTBT rate of electrons with pressure reduces the V_{th} of the sensor, as higher BTBT rate of electrons turns the device ON at lower gate voltage. Further, the V_{th} is higher for higher channel radius at any gas pressure. There is an increase (decrease) in SS with an increase in gas pressure (channel radius) respectively, because of the aforementioned reasons.

5.4 SUMMARY

The first part of this chapter proposed a TFET which overwhelms the major shortcomings of TFET viz. the lower I_{ON} and the ambipolar conduction. It is accomplished by integrating the GDO architecture that suppresses the ambipolar behavior and using hetero gate dielectrics to enhance the I_{ON} of the GAA-TFET. Suppressed I_{AMB} and increased I_{ON} thereby makes GDO-HD-GAA-TFET a suitable candidate for analog/digital circuitry applications. It is obtained that GDO improves the ambipolar characteristics, but it simultaneously degrades the HF performance of the GAA-TFET. Consequently, to overcome the degradation caused by GDO, vacuum gate dielectric is inserted over the region of L_{ov}. By inserting a vacuum dielectric over L_{ov}, the parasitic capacitances are reduced that results in conquering the degradation caused by GDO by enhancing the cut-off frequency of the device, thereby resulting in an overall device improvement (analog and HF performance). Hence, GDO-HD-GAA-TFET with vacuum dielectric over L_{ov} may be used for the development of better analog/low power RF circuits.

In the 2nd part of the chapter HD-GAA-TFET based H_2 gas sensor has been proposed. HD-GAA-TFET unites the advantages of BTBT of electrons in case of TFET along with hetero gate dielectric gate all around and delivers extensively high sensitivity as compared to conventional MOSFET, conventional TFET, GAA-TFET towards H_2 gas detection. It is realized that along with the high sensitivity, HD-GAA-TFET based H_2 gas sensor also has tolerable stability over wide temperature variations that result in a viable gas sensor. Results reveal that for a radius of 10nm, the sensor can be optimized in terms of high sensitivity. After analyzing the stability and sensitivity of the sensor, the temperature affectability and impact

of the radius has been considered on static performance parameters of the sensor such as BTBT rate of electrons, SS and V_{th}. It is found that this highly sensitive HD-GAA-TFET based hydrogen gas sensor may fulfill the everlasting demand for automotive, environmental monitoring, petroleum refining process, and medical industries.

However, as the high-k material in HD engineering scheme constrains the switching speed by enhancing the parasitic capacitance, thus new device engineering viz. n^+ source pocket in the channel near source side has been used in the next chapter to enhance the analog performance. Comprehensive investigation of n^+ source pocket GAA-TFET has been done in terms of analog/RF performance, interface trap charge reliability and temperature robustness.

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CHAPTER 6

PNIN-GAA-TFET: - INTEGRATION OF GDU FOR COMPREHENSIVELY UPGRADED ANALOG/RF PERFORMANCE AND ITS RELIABILITY ISSUES

First and foremost, the chapter works on to mitigate the bottlenecks of TFET and in this regard, the merits of n^+ source pocket and gate-drain underlapping (GDU) has been integrated on cylindrical GAA-TFET that results in GDU-PNIN-GAA-TFET. Specifically, the n^+ source pocket implanted in the channel at the source side leads to steeper band bending that narrows the tunneling barrier width and thereby enhances the ON-state current. While, by GDU viz. by underlapping the gate metal near drain side over channel, the carrier density extension (built-up under the gated region) is resisted towards the drain side (under the underlapped length). Thereby with GDU, the ambipolar current is suppressed. Consequently, by amalgamating the merits of both engineering schemes, GDU-PNIN-GAA-TFET is designed, that thus triumph over the shortcomings of TFET. Therefore, GDU-PNIN-GAA-TFET results in comprehensively up-gradation in the analog performance of GAA-TFET. Furthermore, it is examined that GDU reduces the parasitic capacitances supplementary. Additionally, it is obtained that the RF figure of merits such as cut-off frequency (f_T) and maximum oscillation frequency (f_{Max}) are also extensively enhanced with integration of n^+ source pocket on GAA-TFET. Hence, the comprehensively improved analog/RF performance of GDU-PNIN-GAA-TFET reveals its applicability for low power and high-speed applications. After designing the upgraded GAA-TFET, the chapter works on to investigate the reliability of PNIN-GAA-TFET. The reliability is inspected by analyzing the influence of interface trap charge (ITC) density, polarity and temperature robustness on analog/RF performance of device. It is examined that the interface traps existing at the Si/SiO_2 interface alter the flatband band voltage that further modifies the analog/RF characteristics of the device. Also, the performance is analyzed at various trap charge density and polarity. It is thereby acquired that for the higher trap charge density, the device characteristics alters remarkably. It is evaluated that OFF-state current degrades enormously at donor trap charge density of 3×10^{12} cm^{-2} (increases from an order of $10^{-17}A$ to $10^{-9}A$). Further, it is realized that the device has bias dependence temperature affectability. Specifically, the Shockley Read Hall phenomenon dominates at lower gate bias and degrades the subthreshold current at elevated temperatures. However, the band to band tunneling (BTBT) mechanism dominates for the super-threshold regime. It is examined that OFF-state current degrades enormously at elevated temperatures such that with an increase in ambient temperature from 200K to 400K, the I_{OFF} degrades by order of 10^5, i.e., increases from $10^{-18}A$ to $10^{-13}A$. Results specify that PNIN-GAA-TFET is insusceptible to the acceptor traps existing at the Si/SiO_2 interface in comparison with the donor traps. Hence, PNIN-GAA-TFET can act as a reliable and superior candidate for high switching speed analog/RF applications.

6.1 INTRODUCTION

From the last few decades, CMOS technology is competently meeting the rising demand for innumerable viable ICs by providing the low power consumption requisite for low power battery operated portable devices such as wireless devices, laptops, mobile phones, etc. *(Ionescu and Riel, 2011)*. Additionally, the relentless miniaturization of CMOS devices has exceptionally transfigured many areas such as security, military, mobile communications, and medicine. In this regard, TFET that utilizes the BTBT principle is reported as an energy efficient electronic device for acquiring sub- 60mV/decade subthreshold swing (SS) *(Khatami and Banerjee, 2009, Madan and Chaujar, 2016b)*. In addition to steep SS, the large tunneling barrier width at the tunneling junction for subthreshold region offers very low I_{OFF} (~10^{-17}~10^{-18} A) *(Boucart and Ionescu, 2007b, Boucart and Ionescu, 2007a)*. In consequence, the lower I_{OFF} and steeper SS accessible by TFET affords lower leakage current and lower static power dissipation and thereby making TFET an appropriate solution for ultra-low power applications. However, the exponential dependence of BTBT on the lateral electric field, which is lower in conventional TFET leads to low efficiency of BTBT, even at high gate bias. This, lesser BTBT rate of carriers results in low I_{ON} of TFET and high threshold voltage (V_{th}); and thereby restricts the applicability of TFET in high-speed analog applications *(Villalon et al., 2014)*. Furthermore, TFET also undergoes from high gate-drain parasitic capacitance and ambipolar conduction *(Madan and Chaujar, 2016a, Moselund et al., 2016)*. To mitigate the lower I_{ON} of TFETs, many device and material engineering schemes have already been reported and are also discussed in **Chapter 1**; such as heterojunction TFET using III-V materials *(Hanna and Hussain, 2015, Hanna et al., 2015, Moselund et al., 2016, Shih and Chien, 2011),* multi-gate architecture TFET (double gate, gate all around architectures) *(Gandhi et al., 2011),* dual material gate *(Madan et al., 2017),* heterogate dielectric *(Choi and Lee, 2010),* n^+ source pocket *(Jhaveri et al., 2011, Nagavarapu et al., 2008),* narrow band gap materials *(Toh et al., 2007)* etc. Among all device engineering architectures, the n^+ source pocket P-I-N TFET or PNIN-TFET proposed by Nagavarapu et al. *(Nagavarapu et al., 2008),* is a strong candidate as it collectively offers higher I_{ON} with lower V_{th} and SS. Therefore, in this chapter, a n^+ source pocket is implanted in the channel region near the source side so as to modulate the energy band profile at the source channel junction that increases the lateral electric field *(Jhaveri et al., 2011)*. The enhanced lateral electric field results in narrower tunneling barrier width and thereby increases the tunneling probability of electrons and

eventually improves the I_{ON} of TFET. Moreover, it is reported by Cao et al., that implanting a source pocket along with enhanced I_{ON} also provides superior reliability of TFET *(Cao et al., 2011)*, in comparison with conventional PIN-TFET. In addition, the fabrication process of PNIN architecture is also described by Nagavarapu et al., in accordance, after defining the gate metal, the tilt angled implant is used to form the n^+ source pocket *(Nagavarapu et al., 2008)*.

As described in **Chapter 5**, the tunneling at the drain-channel junction for negative gate bias in TFETs results in the ambipolar conduction, i.e., the conduction in both positive and negative gate bias regions *(Wang et al., 2004, Madan and Chaujar, 2016a)*. This ambipolar conduction in TFETs impedes TFET applicability for digital applications. Various device engineering schemes such as gate-drain underlapping (GDU) or shortened metal gate *(Verhulst et al., 2007)*, asymmetric source-drain doping *(Boucart and Ionescu, 2007a)*, hetero gate dielectric *(Madan et al., 2015)*, etc. have been described in **Chapter 5** for lowering the ambipolar current (I_{AMB}). Among these engineering schemes, gate-drain underlapping, i.e., GDU is of prime importance due to its viability offered by the simple fabrication process. In GDU, the underlapped gate metal near drain side resists the extension of carrier density that is built-up under the gated region towards the drain side or beneath the underlapped region. Thus, the underlapped gate metal controls the ambipolar conduction *(Wang et al., 2014)*. Besides reducing the ambipolar conduction, the GDU engineering scheme also reduces the intrinsic gate to drain capacitance (C_{gd}), which is a major hindrance while designing TFET circuitry. However, the hetero gate dielectric engineering scheme, that is used in the last few chapters of this thesis, reduces the I_{AMB}, but it has implications on enhanced parasitic capacitance due to the presence of high-k dielectric near source-channel junction as shown in **Chapter 3** of this thesis *(Kang et al., 2011)*. Therefore, in this chapter, the short metal gate or GDU engineering scheme is considered for reducing the I_{AMB} in GAA-TFET.

Nevertheless, the basic device characteristics such as improved analog, RF, and linearity of TFET have been the primary encompassing area of investigation up to now. Recently, Moselund et al.*(Moselund et al., 2016)* have fabricated lateral p-type InAs/Si TFET with I_{ON} of a few μA/μm for $|V_{ds}|=|V_{gs}|=0.5V$. A SiGe/Si heterostructure TFET has been fabricated by Blaeser et al. that shows I_{ON} of 6.7 μA/μm at $V_{dd}=0.5V$ and SS of about 80mV/decade *(Blaeser et al., 2016)*. However, for sub-100nm regime, the reliability of TFET is of critical concern, due to the strong electric field at the tunneling junction. This high

electric field, roots to the generation of defects at the interface of Si-SiO_2 *(Qiu et al., 2014).* Along with the high electric field, the fabrication processes for sub-100nm devices such as the plasma etching may also damage the gate oxide and the Si-oxide interface. These defects are the source of fixed interface and oxide charges. These fixed charges harmfully affect the yield, reliability and also modifies the ideal expected device characteristics *(Madan and Chaujar, 2016b, Pala et al., 2012).* Moreover, the influence of interface trap charges (ITCs) have also been inspected on lateral p-type InAs/Si (a III-V TFET) by Sant *et al*. *(Sant et al., 2016),* in which they described that the high concentration of trap centers present at the hetero-junction of III-V material (source side) and the silicon (channel region) owing to the carrier generation by the trap-assisted tunneling (TAT) at the hetero-junction, degrades the SS of TFET. The large trap centers at the interface of III-V material in heterojunction TFET assess the charge density at the interface and thus alter the device electrostatics. In addition to the traps present at the hetero-junction, for a III-V TFET, the traps at the interface of channel and oxide, add to the further degradation of the subthreshold characteristics of TFET. However, till date, not much has been reported regarding the influence of ITCs on the reliability of TFET *(Jiao et al., 2009, Madan and Chaujar, 2016b, Madan and Chaujar, 2017c, Pala et al., 2012, Qiu et al., 2014, Wang et al., 2013).*

In addition, to meet the unending demand of transistors with high and low-temperature tolerance desirable in aircraft, space, and automotive technology, the temperature affectability over the device performance must be investigated *(Der Agopian et al., 2012, Guo et al., 2009).* Moreover, with an increase in number of on-chip transistors, the heat dissipation increases significantly that translate into elevated operating temperature. Thus, for investigating the temperature robustness, it is essential to examine the performance of the device at various ambient temperatures. Dey *et al.* and Mookerjea *et al.* have reported that due to the onset of various conduction mechanisms at different gate bias regions, the temperature reliance of III-V TFET is a strong function of gate bias *(Dey et al., 2013, Mookerjea et al., 2010).* At lower gate bias region, the consequence of exponential temperature dependence of SRH generation recombination results in the exponential rise of I_{OFF}. Further increase in gate bias, thermally excites the carriers from the trap centers into the conduction band. But, at higher gate bias region, the BTBT underwrites the drain current with insignificant contribution from the trap centers. The surface passivation is suggested for decreasing the TAT and also for the degradation caused at the elevated temperatures to the SS and I_{OFF}.

In this chapter, firstly to acquire a comprehensive up gradation in GAA-TFET, both gate-drain underlapping and n^+ source pocket has been implanted onto the GAA architectured TFET. Elaborate studies of the resultant device, i.e., GDU-PNIN-GAA-TFET, in terms of various electrical and analog characteristics and RF figure of merits (FOMs), are done. After designing the proposed comprehensively device, the reliability in terms of ITCs density and polarity and temperature robustness of the proposed device is examined.

6.2 DEVICE STRUCTURE AND PARAMETERS

Figure 6.1(a) shows the schematic 3D structure of GDU-PNIN-GAA-TFET used for simulation. Moreover, for better visual perception, the 2D schematic cross-sectional view of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET, and GDU-PNIN-GAA-TFET has also been shown in **Figures 6.1(b-e)**. The design variables for acquiring an optimized GDU-PNIN-GAA-TFET are gate-drain underlapping length (L_{GDU}), source pocket doping (N_P) and source pocket width (L_P). For PNIN-GAA-TFET, source pocket is optimized for better I_{ON}/I_{OFF} ratio, $V_{th,}$ and SS by tuning L_p and N_p. It is obtained that at L_p=4nm and N_p=4×10^{19} cm^{-3} respectively, the PNIN engineering scheme is optimized in terms of high I_{ON}/I_{OFF} ratio,

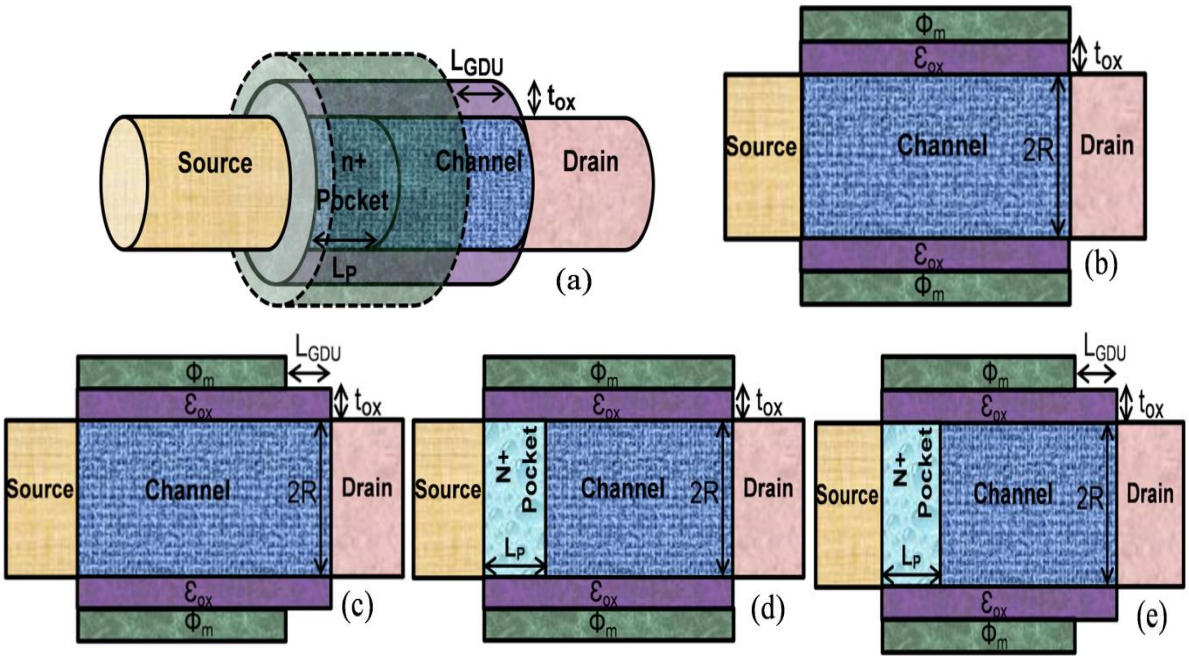

Figure 6.1 (a) Simulation structure of GDU-PNIN-GAA-TFET. Schematic 2-D cross-sectional view of (b) GAA-TFET, (c) GDU-GAA-TFET, (d) PNIN-GAA-TFET, and (e) GDU-PNIN-GAA-TFET ***(Madan and Chaujar, 2017a).***

low-V_{th} and low SS. The GDU engineering scheme is also optimized by altering the L_{GDU} for acquiring an optimum analog performance and parasitic capacitances and is discussed in the next section of this chapter. The source, channel, and drain are of Silicon. Furthermore, an optimum value of gate metal work function, i.e., 4.3eV has been chosen for optimal subthreshold characteristics. Various default design parameters used in the simulation are specified in **Table 6.1**. Additionally, the intrinsic parasitic capacitances are extracted through small signal AC analysis at a constant DC solution as also described in **Chapter 3** of this thesis (after solving the constant DC bias). Also, the inherent capacitances among each pair of electrode (i.e., source, gate, and drain) are calculated at a single constant frequency at 1MHz with a DC voltage ramp of 0 to 1.6V. Besides, for better convergence, the DIRECT parameter is incorporated while simulating the device.

TABLE 6.1

DEVICE DEFAULT DESIGN PARAMETERS USED IN SIMULATIONS *(MADAN AND CHAUJAR, 2017A)*

Parameters	**Value**
Drain (N^+) doping (N_d)	5×10^{18} cm^{-3}
Source (P^+) doping (N_s)	1×10^{20} cm^{-3}
Channel radius (R)	10nm
Source Pocket (n^+) doping (N_p)	4×10^{19} cm^{-3}
Source Pocket Width (L_p)	4nm
Channel Length (L_g)	50nm
Gate oxide thickness (t_{ox})	2nm
Gate metal workfunction (Φ_M)	4.3eV
Gate dielectric SiO_2 ($\mathcal{E}_{OX}$)	3.9
Gate drain underlapping length (L_{GDU})	15nm

Owing to the high electric field at the source-channel (tunneling) junction, the ITCs are considered only at 10nm length from the interface of source and n^+ pocket and along the Si-SiO_2 interface. Further, as the ITCs are present majorly over the tunneling junction and GDU administer the drain-channel junction, thus no drain underlapping is accounted for analyzing the reliability, i.e., the reliability of PNIN-GAA-TFET is investigated. Further, the reliability of device in terms of ITCs is examined by transmuting the equivalent positive (negative) localized charges at the Si-SiO_2 interface as also elucidated in **Chapter 4** of this thesis. The uniform distribution of ITC density is considered in the TCAD simulations. The parameters such as the trap charge density, polarity and their position along the channel are

defined in INTERFACE statement. Further, the density of interface charge density (N_f) is chosen in support with various formerly published experimental and simulation data that includes the process damage, radiation damage, and hot carrier damage and results in ITC density of 10^{11}-10^{13} $cm^{-2}eV^{-1}$ *(Pala et al., 2012, Qiu et al., 2014, Sant et al., 2016)*. Moreover, while analyzing the influence of ITCs on device characteristics, the temperature is kept constant at 300K, and during the investigation of temperature affectability, the trap charge density is held constant at N_f=±1x10^{12} cm^{-2}.

6.3 RESULTS VERIFICATION AND DISCUSSION

6.3.1 IMPACT OF GDU LENGTH: - AN OPTIMIZATION STUDY

This subsection works on to acquire an optimized gate metal underlapping length (L_{GDU}) for GDU-GAA-TFET. In this regard, transfer characteristics of GDU-GAA-TFET have been analyzed at various $L_{GDU.}$ Transfer characteristics depicted in **Figure 6.2** evidently shows that the effect of L_{GDU} is only in the negative V_{gs} and I_{ds} remains intact in positive V_{gs} for variations in L_{GDU}. The uninfluenced drain current for positive V_{gs} is due to the fact that the tunneling junction that governs the drain current for positive V_{gs} regime is unaffected by the GDU (being at the drain-channel junction).

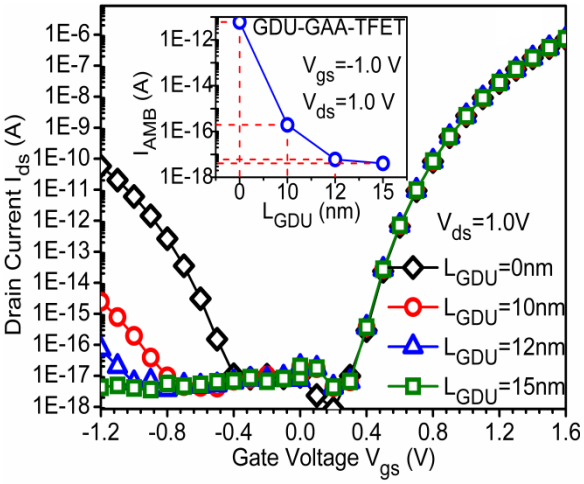

Figure 6.2 Transfer characteristics of GDU-GAA-TFET at various $L_{GDU.}$ *Inset*: I_{AMB} of GDU-GAA-TFET at various L_{GDU} *(Madan and Chaujar, 2017a)*.

Substantially suppressed I_{AMB} is acquired at larger underlapping length. It is examined that I_{AMB} is reduced from an order of 10^{-12}A (for GAA-TFET) to 10^{-18}A (for GDU-GAA-

TFET at L_{GDU}=15nm). Thus, considerably reduced I_{AMB}~10^{-18}A may satisfactorily overwhelm the challenges faced by TFET for digital applications. Therefore, at L_{GDU}=15nm, GDU-GAA-TFET is optimum from the perspective of I_{AMB} at the default design parameters mentioned in **Table 6.1**.

Furthermore, the reliance of response time and active power dissipation on intrinsic parasitic capacitances motivates for designing a TFET with minimum parasitic capacitances. Thus, the influence of L_{GDU} on C_{gs} and C_{gg} of GDU-GAA-TFET are investigated and are presented in **Figures 6.3(a-b)**. The unaltered C_{gs} with variations in L_{GDU} as depicted in **Figure 6.3(a)** is necessary due to the fact that gate metal is underlapped near the drain channel junction and C_{gs} is characteristic of the source and channel. Further, the reduced C_{gg} with L_{GDU} is offered by the reduction in the C_{gd} (as $C_{gg}=C_{gs}+C_{gd}$). It is evaluated that C_{gg} decreases by 38% for an increase in L_{GDU} from 0nm (GAA-TFET) to 15nm (GDU-GAA-TFET).

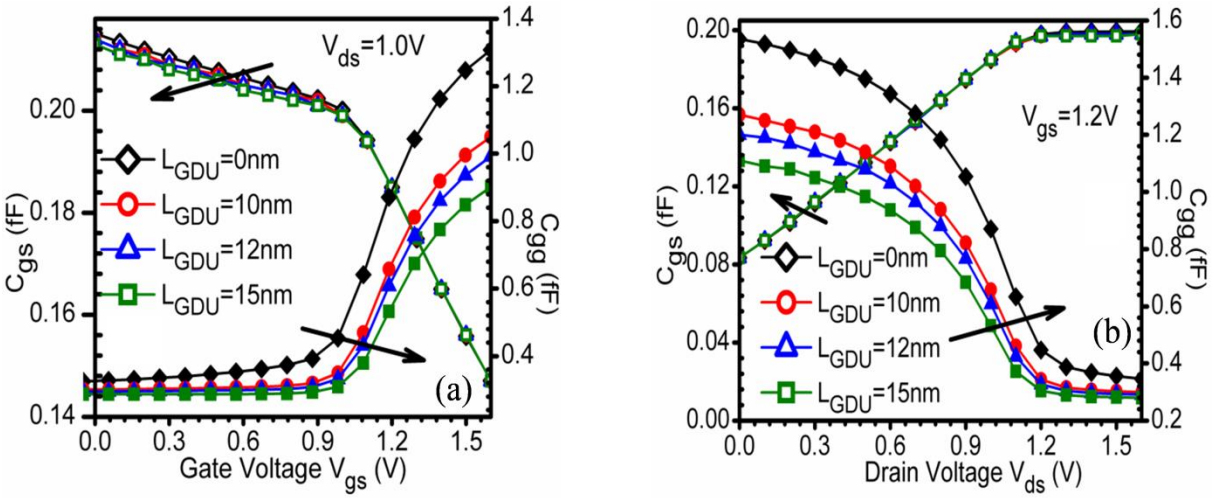

Figure 6.3 C_{gs} and C_{gg} of GDU-GAA-TFET as a function of (a) V_{gs} at V_{ds}=1.0V (b) V_{ds} at V_{gs}=1.2V at various L_{GDU}. L_{GDU}=0nm signifies GAA-TFET *(Madan and Chaujar, 2017a)*.

The influence of L_{GDU} is also analyzed on intrinsic capacitances as a function of V_{ds} at a constant V_{gs} and are displayed in **Figure 6.3(b)**. Considerably reduced C_{gg} for shorted gate metal is clearly depicted in **Figure 6.3(b)**. Furthermore, as the transfer characteristics for positive gate bias are immune towards variations in L_{GDU}, thus, the V_{th}, SS, I_{ON}, I_{ON}/I_{OFF} ratio, g_m and other analog and electrical parameters will also remain unaltered for variations in L_{GDU}. Therefore, it is assessed that at L_{GDU}=15nm, GDU-GAA-TFET shows an optimum

device performance in terms of I_{AMB} and parasitic capacitances. Consequently, for GDU engineering scheme, L_{GDU} is optimized at 15nm.

6.3.2 IMPACT OF GATE-DRAIN UNDERLAPPING AND SOURCE POCKET

This subsection of the chapter presents the comparative analysis of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET, and GDU-PNIN-GAA-TFET, in terms of various analog/RF FOMs. The default parameters for GDU architecture are L_{GDU}=15nm, and for n^+ source pocket PIN (i.e., PNIN) architecture is $N_p=4\times10^{19}cm^{-3}$, L_p=4nm. For an exhaustive understanding of the tunneling phenomenon, the energy band profiles of all the devices under consideration are studied in the ON-state (V_{gs}=1.2V and V_{ds}=1.0V) as well as in the ambipolar-state (V_{gs}=-1.0V and V_{ds}=1.0V) and are illustrated in **Figures. 6.4(a-b)**.

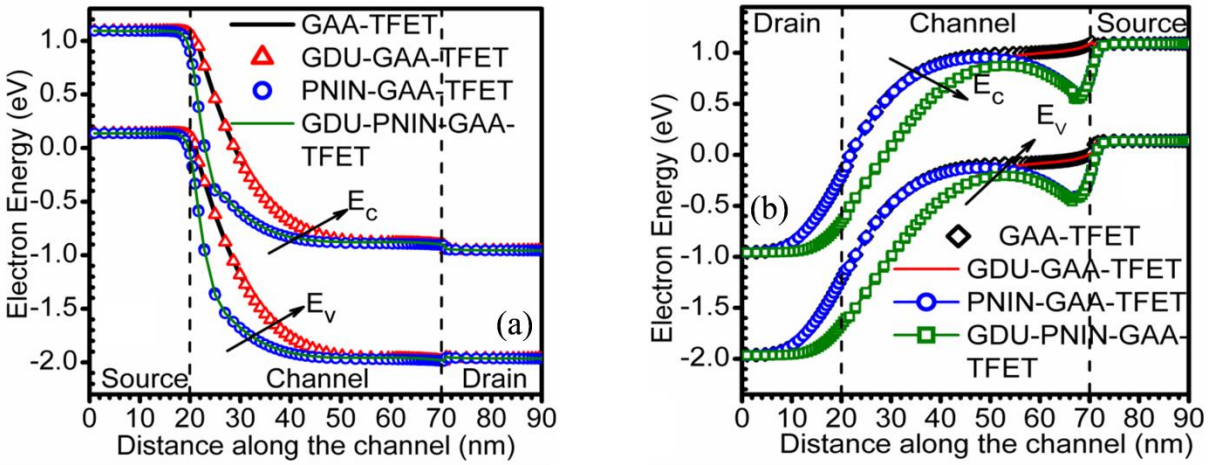

Figure 6.4 Energy band diagram of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET (a) in ON-state at V_{gs}=1.2V and V_{ds}=1.0V (b) in ambipolar state at V_{gs}= -1.0V and V_{ds}=1.0V as a function of channel length. For GDU architecture L_{GDU}=15nm *(Madan and Chaujar, 2017a)*.

The ON-state energy band profile shown in **Figure 6.4(a),** depicts the similar electron energy band profile for GAA-TFET and GDU-GAA-TFET that is primarily due to the fact that GDU (being at the drain channel junction) plays role for the negative gate bias to control the I_{AMB}. Additionally, implantation of n^+ pocket viz. PNIN-GAA-TFET and GDU-PNIN-GAA-TFET offer steeper band bending that lowers the barrier width and thereby enhances the tunneling probability of electrons in ON state. Further, the energy band profile for the ambipolar state depicted in **Figure 6.4(b)** evidently shows that the underlapped metal gate broadens the barrier width at the drain-channel junction and thereby resists the tunneling of

electrons at the drain-channel junction. This broadens the tunneling width due to GDU thereby reduces the I_{AMB}, and makes TFET eligible for digital switching applications.

Figure 6.5(a) demonstrates the n-BTBT rate of electrons and electric field at the tunneling junction for all the device configurations mentioned in **Figure 6.1(b-e)**. It is clearly depicted that the n-BTBT rate of electrons is unaltered by underlapping the gate metal, i.e., for GDU-GAA-TFET and is, therefore, equal in amount with GAA-TFET. Moreover, for GAA-TFET and GDU-GAA-TFET, the tunneling rate is meager that is due to the wide tunneling width. Furthermore, with implantation of n^+ source pocket in the channel near the source side, the band bending becomes steeper that translate into lowering of barrier width and thereby enhances the n-BTBT rate of electrons. The steeper band bending acquired via n^+ source pocket increases the electric field for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET. Quantitatively, with the implantation of n^+ source pocket, the electric field is increased by 2.2 times.

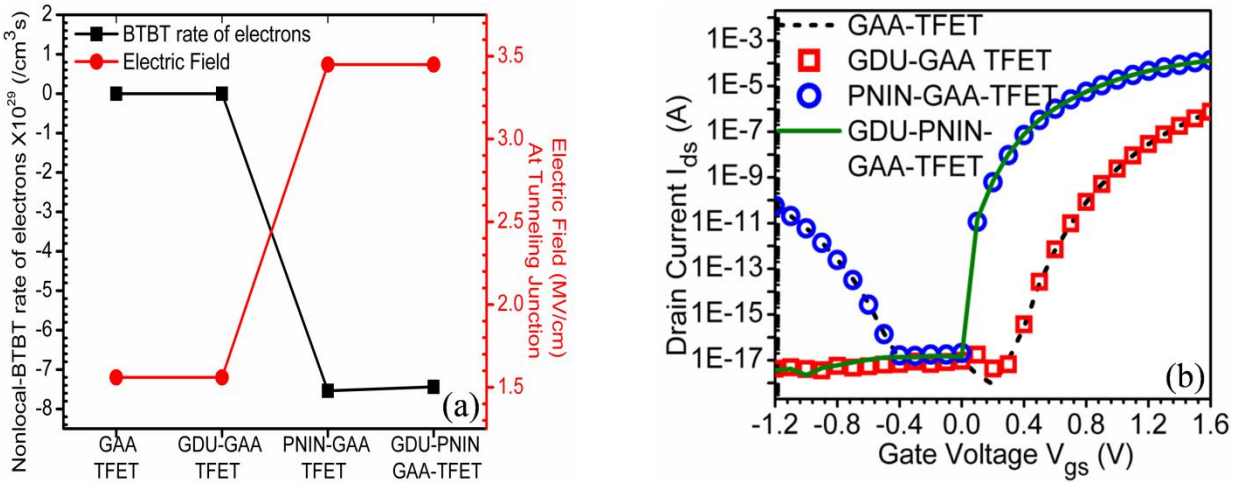

Figure 6.5 (a) n-BTBT rate, electric field at the tunneling junction at V_{gs}=1.2V and (b) Transfer characteristics of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET at V_{ds}=1.0V *(Madan and Chaujar, 2017a)*.

The transfer characteristics of all the devices mentioned in **Figure 6.1** on page 135 is shown in **Figure 6.5(b)**. It is clearly depicted that GAA-TFET suffers from lower I_{ON} and higher I_{AMB}. The I_{AMB} is reduced appreciably from an order of 10^{-12}A to 10^{-18}A, as the gate metal is underlapped near drain side, i.e., for GDU-GAA-TFET. The reduction in I_{AMB} offered by the GDU that primarily resists the extension of carrier density towards the drain side, and so repels the lowering of barrier width at the drain-channel junction (for negative

V_{gs}). This reduced I_{AMB} thus overcomes the major challenges faced by TFET and makes it suitable for digital applications. Moreover, the implantation of n^+ pocket enhances the n-BTBT rate of electrons as illustrated in **Figure 6.5(a)** that increases I_{ON} from an order of 10^{-8}A (for GAA-TFET) to 10^{-4}A (for PNIN-GAA-TFET). Consequently, the integration of both the scheme, i.e., for GDU-PNIN-GAA-TFET, both the complications (i.e., lower I_{ON} and higher I_{AMB}) are overwhelmed.

Quantitative representation of I_{AMB}, I_{ON}/I_{OFF} ratio, V_{th} and SS for all the device architectures under considerations are presented in **Table 6.2**. The ambipolar conduction is a major bottleneck for applicability of TFETs for low power analog and digital applications. In this thesis, I_{AMB} is defined as the I_{ds} at V_{gs}=-1.0V and V_{ds}=1.0V. It is apparently visible in **Table 6.2** that for the shorter gate metal, i.e., with GDU architecture, the I_{AMB} is suppressed significantly. This reduced I_{AMB} is mainly offered by the reduced accumulations of electrons under the underlapped region, followed by the broadened barrier width at the channel and drain junction; and thereby decreases the tunneling probability of electrons at the drain-channel junction. Consequently, the reduced tunneling of electrons suppresses the I_{AMB}, from 10^{-12}A (for GAA-TFET and PNIN-GAA-TFET) to 10^{-18}A (for GDU-GAA-TFET and GDU-PNIN-GAA-TFET) as depicted in **Table 6.2**.

TABLE 6.2

AMBIPOLAR CURRENT (I_{AMB}) AT V_{GS}=-1.0V, CURRENT SWITCHING RATIO (I_{ON}/I_{OFF}), THRESHOLD VOLTAGE (V_{TH}) AND SUBTHRESHOLD SWING (SS) OF GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET AND GDU-PNIN-GAA-TFET AT V_{DS}=1.0V *(Madan and Chaujar, 2017a)*.

Device Architecture	I_{AMB} (A)	I_{ON}/I_{OFF}	SS (mV/decade)	V_{th} (@I_{ds}= 10^{-7}A) (V)
GAA-TFET	6.03×10^{-12}	2.98×10^{9}	52.22	1.32
GDU-GAA-TFET	4.05×10^{-18}	3.06×10^{9}	53.37	1.32
PNIN-GAA-TFET	5.96×10^{-12}	2.21×10^{12}	17.41	0.41
GDU-PNIN-GAA-TFET	2.23×10^{-18}	3.20×10^{12}	16.59	0.40

Further, the current switching (I_{ON}/I_{OFF}) ratio, an essential parameter for digital circuit designing is also analyzed and is reported in **Table 6.2**. Here, the I_{ON} and I_{OFF} are defined as

the I_{ds} at V_{gs}=1.2V and 0V respectively, at V_{ds}=1.0V. The implantation of n^+ pocket boosts the I_{ON} of the TFET significantly (without any degradation in the I_{OFF}) [see **Figure 6.5(b)** on page 140], therefore enhances the current switching ratio of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET significantly to an order of 10^{12}. The improved I_{ON}/I_{OFF} ratio attained by the n^+ source pocket PNIN-GAA-TFET makes it a potential candidate for high switching speed applications. Moreover, the steeper band bending at the source channel for PNIN-GAA-TFET switches ON TFET at lower V_{gs}. Thus, there is a considerable reduction in the V_{th} for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in comparison with its conventional counterparts. Further, the integration of n^+ pocket in GAA-TFET enhances the I_{ON} without any degradation in the I_{OFF}, thereby reduces the SS of GAA-TFET by 3.14 times for PNIN-GAA-TFET.

Device efficiency (or the transconductance generation factor) and the output resistance (or the drain resistance) are the crucial device design parameters for analog applications. Device efficiency is assessed by the ratio of transconductance to drain current, i.e., g_m/I_{ds} at a constant V_{ds}. It is primarily the measure of available gain per unit power dissipation. Further, a higher value of device efficiency is appropriate for better analog performance. **Figure 6.6(a)** demonstrates the improved g_m/I_{ds} of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET as compared to GAA-TFET and GDU-GAA-TFET. This improvement is offered by the implantation of n^+ source pocket in PNIN-GAA-TFET that increases I_{ds} and g_m considerably. Thereby, the implantation of n^+ source pocket augments the amplification delivered by the GAA-TFET.

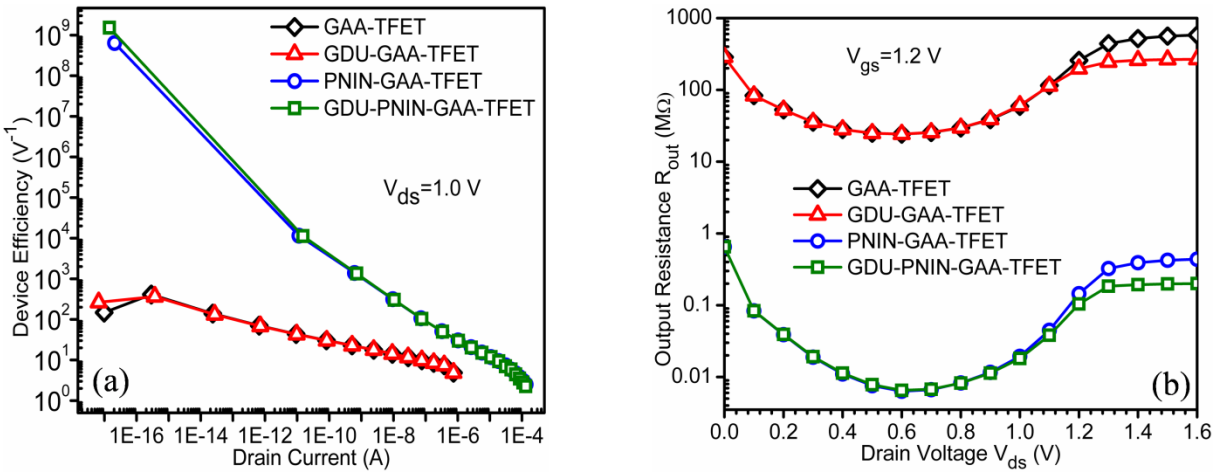

Figure 6.6 (a) Device efficiency at V_{ds}=1.0V, (b) Output resistance (R_{out}) at V_{gs}=1.2V of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET *(Madan and Chaujar, 2017a)*.

Figure 6.6(b) shows the output/drain resistance (R_{out}) of all the devices under discussion. It is obtained that the R_{out} of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET are substantially improved in comparison with GAA-TFET and GDU-GAA-TFET. This improvement in R_{out} for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET is essentially offered by the increased I_{ds} that enhanced the output conductance. Thus, the consequence of inverse relation of output conductance and R_{out}, decreases R_{out} from an order of $10^8\Omega$ (for GAA-TFET and GDU-GAA-TFET) to $10^5\Omega$ (for PNIN-GAA-TFET and GDU-PNIN-GDU-GAA-TFET). This upgraded device efficiency and R_{out} makes GDU-PNIN-GAA-TFET suitable for low power analog applications.

Merely increasing the I_{ON}, reduced V_{th} and lowered SS does not satisfactorily result in a superior TFET based circuit performance. Nevertheless, the static and dynamic power dissipations and the propagation delay are the fundamental performance metrics for designing digital circuits. The crucial device parameters that affect these performance metrics are the bias dependence inherent parasitic capacitances. Also, as reported in **Chapter 3** of this thesis that for TFET, C_{gd} and C_{gs} contribute unequally to C_{gg}, in contrary to MOSFET in which $C_{gg}/2 \sim C_{gd} \sim C_{gs}$ *(Gnani et al., 2015, Mookerjea et al., 2009)*. In TFETs, the source-channel junction being reverse biased effectively decouples the channel charge from the source. However, the degenerated (n^+) drain floods the channel region with electrons. Consequently, the channel charge is majorly coupled with the drain, and thus C_{gd} represents a significant fraction of C_{gg}. **Figures 6.7(a-d)** displays the C_{gs} and C_{gg} as a function of V_{gs} and V_{ds}. It is evidently shown in **Figure 6.7(a)** and **Figure 6.7(c)** that C_{gs} is many order less than C_{gd} that results in a similar profile of C_{gg} and C_{gd}. Further, it is analyzed that the C_{gs} is unaltered for the GDU engineering scheme because the gate metal is underlapped near the drain side. Moreover, the underlapped metal gate near the drain side reduces C_{gd} appreciably as is shown in **Figure 6.7(a)** and **Figure 6.7(c)** that translate into reduction in C_{gg} ($C_{gg}=C_{gs}+C_{gd}$). Thereby, a substantially reduced C_{gg} is obtained for GDU-GAA-TFET and GDU-PNIN-GAA-TFET, in comparison with GAA-TFET. Quantitatively, C_{gg} is reduced by 29% with the integration of GDU engineering scheme onto GAA-TFET as presented in **Figure 6.7(b).** Additionally, at lower V_{gs}, the inversion layer is first formed near the drain side, and then with an increase in V_{gs}, the inversion layer extends towards the source side. Thus, C_{gg} increases with an increase in V_{gs}. **Figures 6.7(c-d)** illustrates the C_{gs} and C_{gg} for all the device design architectures as a function of V_{ds} at a constant V_{gs}. At V_{gs}=1.2V (TFET is in ON-state), an increase in V_{ds}

pinches the inversion layer at the source side (in contrast to MOSFET, where pinch off occurs near drain side) and thereby, C_{gg} decreases with an increase in V_{ds}. Thus, the reduced C_{gd} and hence the C_{gg} with GDU engineering scheme results in lowering of parasitic capacitance for GDU-GAA-TFET and PNIN-GDU-GAA-TFET in comparison to GAA-TFET and PNIN-GAA-TFET. Consequently, as lower parasitic capacitances are desirable for faster switching and lower static power dissipation, GDU-PNIN-GAA-TFET may act as a superior candidate to come across these desires.

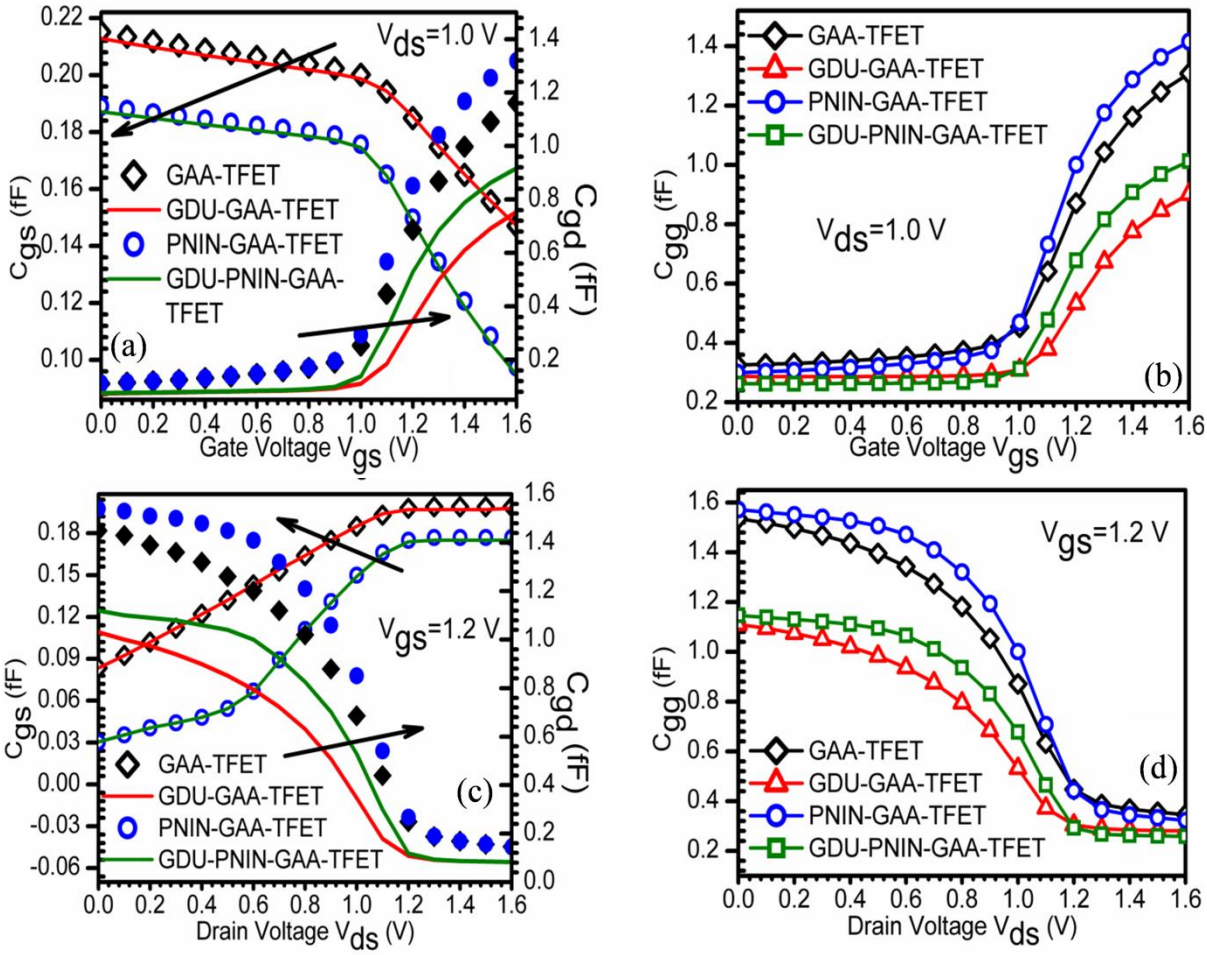

Figure 6.7 (a) C_{gs} w.r.t. V_{gs} at V_{ds}=1.0V (b) C_{gg} w.r.t. V_{gs} at V_{ds}=1.0V (c) C_{gs} w.r.t. V_{ds} at V_{gs}=1.2V (d) C_{gg} w.r.t. V_{ds} at V_{gs}=1.2V of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET ***(Madan and Chaujar, 2017a).***

The vital RF parameters required for designing analog/RF electronic circuits, i.e., cut off frequency (f_T) and the maximum oscillation frequency (f_{Max}) are presented in **Figures 6.8(a-b)**. The variations of f_T as a function of V_{gs} for all the device designs under

considerations are depicted in **Figure 6.8(a)**. It is analyzed that with increase in V_{gs}, f_T of all the devices increases until it attains a peak value. The rise in f_T with V_{gs} is attributed to the enhanced rate of carrier injection with V_{gs} followed by the increase in I_{ds} and g_m (first-order derivative of I_{ds}). Henceforth, as f_T *is* directly proportional to g_m, it increases with V_{gs}, before attaining a peak value. Furthermore, the increased drain current and thereby the g_m with the implantation of n^+ source pocket results into significantly upgraded f_T for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in comparison to GAA-TFET and GDU-GAA-TFET. It is evaluated that f_T is enhanced from an order of 10^8 Hz to 10^{10} Hz with the integration of n^+ source pocket. The f_T and f_{Max} of all the devices under consideration are also displayed in **Figure 6.8(b)**. f_T and f_{Max} are assessed as the frequencies at which short-circuit current gain and unilateral power gain drops to 0dB respectively. f_T and f_{Max} are immensely higher for the cases of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in comparison with GAA-TFET and GDU-GAA-TFET, due to the increased g_m that enhance the current gain and the unilateral power gain and consequently f_T and f_{Max} as evident from **Figure 6.8(b)**. Thus, it is determined that with the implantation of n^+ source pocket, analog as well as the HF performance of GAA-TFET are upgraded substantially, making it a superior candidate for high switching speed electronics application.

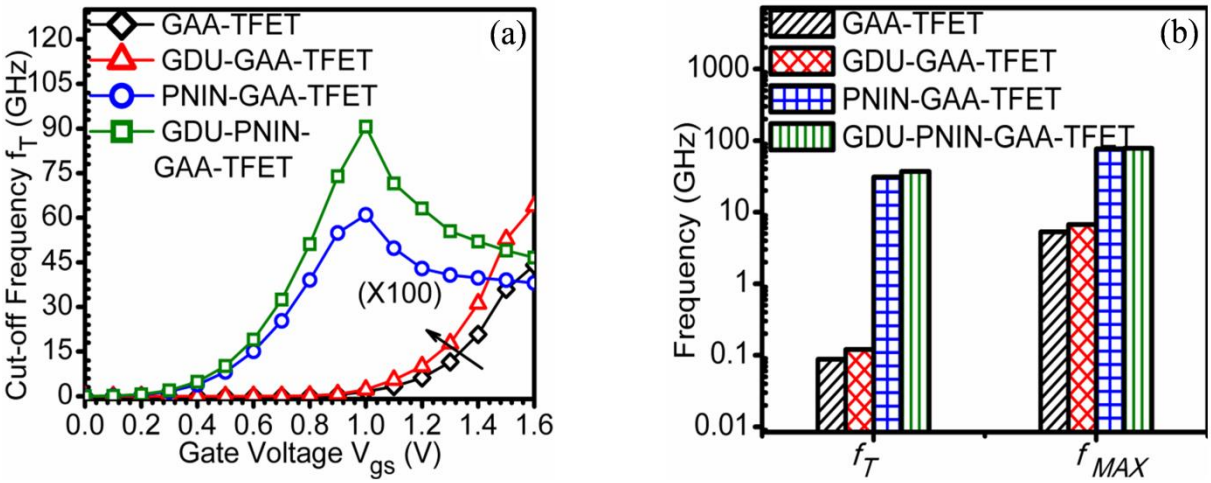

Figure 6.8 (a) f_T as a function of gate bias, at constant V_{ds}=1.0V (b) f_T and f_{Max} at V_{gs}=1.2V and V_{ds}=1.0V of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET *(Madan and Chaujar, 2017a).*

6.3.3 IMPACT OF INTERFACE TRAP CHARGES- DENSITY AND POLARITY

In this section, the effect of ITCs density and polarity of PNIN-GAA-TFET, depicted in **Figure 6.1(d)** is inspected at a constant temperature T=300K. The variations of the total electric field of PNIN-GAA-TFET at various interface charge density and polarity is illustrated in **Figure 6.9(a).** Moreover, the magnified view of the peak electric field (i.e., at the source channel junction) shows that with an increase of donor (acceptor) trap charge density, the peak of electric field increases (decreases) w.r.t the case of the undamaged device. This increase (decrease) in an electric field is due to the decrease (increase) in flatband voltage (V_{fb}) caused by the presence of donor (acceptor) trap charges, defined as:-

$$\Delta V_{fb} = \frac{qN_f}{C_{ox}} \tag{6.1}$$

Where;

q is the electronic charge,

N_f is the ITC density, and

C_{ox} is the gate oxide capacitance.

The presence of donor (acceptor) ITCs reduces (enhances) the V_{fb} and by this means increases (decreases) the effective gate bias ($V_{eff} = V_{gs}$-V_{fb}) at the source channel junction followed by the increase (decrease) of the electric field at the tunneling junction as depicted in **Figure 6.9(a)**. However, this substantially high electric field peak at the tunneling junction is a merit for tunneling rate of electrons. Nevertheless, it has counter effects of generation of trap centers near the source-channel junction. As reported by Cao et al. in *(Cao et al., 2011)*, the parallel component of electric field, i.e., E_y accounts for the tunneling rate of electrons and so affects the drive current of TFET. Principally, higher E_y is requisite for higher I_{ds}. However, the normal component of electric field, i.e., E_x is accountable for the reliability concerns such as the interface trap generation along with the gate leakage current. The lower E_x is a requisite for improved device reliability. Hence, the peak of parallel (E_y) and normal (E_x) component of electric field at the source channel junction as a function of ITC density is investigated and is depicted in **Figure 6.9(b)**. At higher donor (acceptor) trap charge density, the peak of both E_x and E_y is large (small). The higher E_y increases the tunneling rate of electrons, however, large E_x degrades the device reliability.

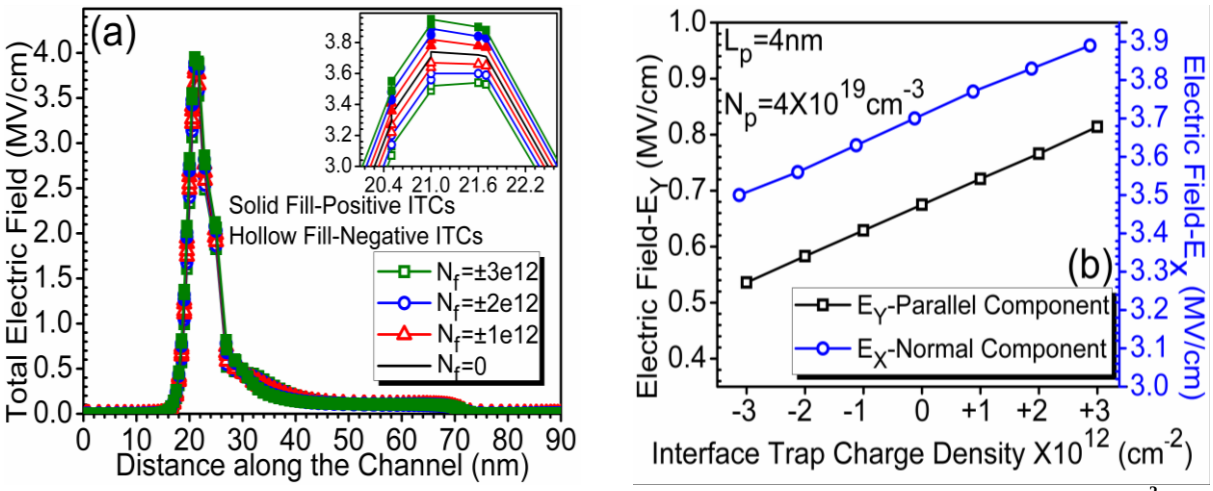

Figure 6.9 (a) Electric field profile along the channel of PNIN-GAA-TFET at N_f = ±1, 2, 3(×12) cm^{-2}, (b) Peak intensity of parallel and normal component of Electric Field near tunneling junction of PNIN-GAA-TFET as a function of ITC density *(Madan and Chaujar, 2017b)*.

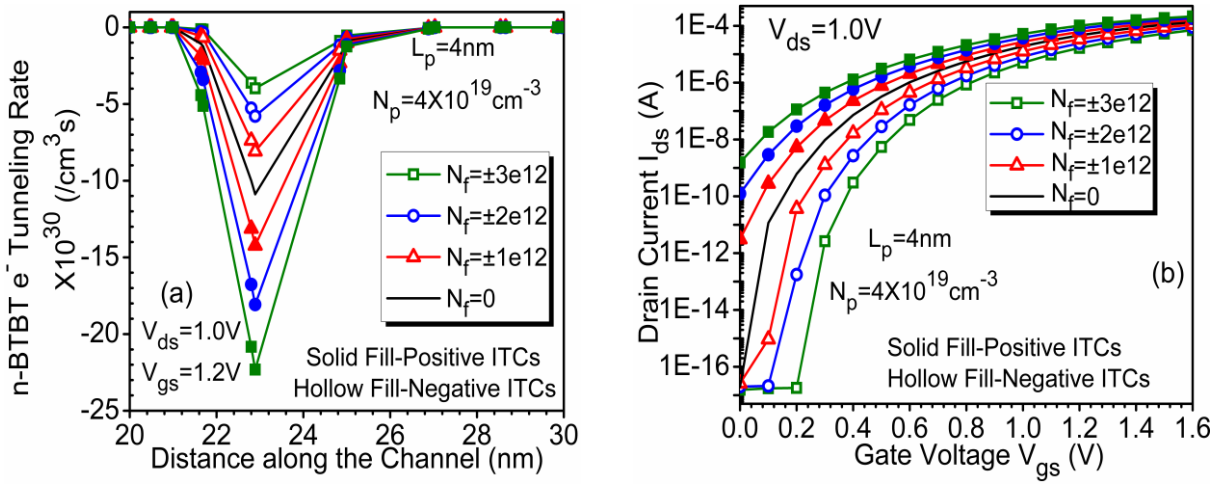

Figure 6.10 n-BTBT of electrons of PNIN-GAA-TFET as a function of channel length, (b) Impact of ITC density on transfer characteristics of PNIN-GAA-TFET at N_f = ±1, 2, 3(×12) cm^{-2} *(Madan and Chaujar, 2017b)*.

The plot of n-BTBT rate of electrons along the channel length for various ITC density of PNIN-GAA-TFET is shown in **Figure 6.10(a)**. Considerable increase (decrease) in the BTBT rate of electrons offered by the enhanced (reduced) electric field has been obtained with an increase in density of donor (acceptor) ITCs. The consequences of altered BTBT rate of electrons due to the presence of ITCs have been shown in the transfer characteristics of PNIN-GAA-TFET in **Figure 6.10(b)**. In consistent with above results, increase (decrease) in drain current with the donor (acceptor) traps caused by the enhanced (reduced) effective gate bias has been obtained. However, the degradation posed by the donor traps is more hazardous

for the device operated in subthreshold regime in comparison to the super-threshold regime. Moreover, it is examined that with an increase in donor trap charge density, the I_{OFF} degrades considerably from an order of 10^{-17}A to 10^{-9}A. Hence, as the fixed charges generated by the various process, radiation, and stress-induced damages are always present in a practically fabricated device, it may relentlessly degrade the device characteristics.

Figure 6.11(a) shows the effect of trap charge density on I_{OFF} and the current switching ratio (I_{ON}/I_{OFF} ratio) of PNIN-GAA-TFET. It is clearly depicted in **Figure 6.11(a)** that for damaged region with donor trap charges of 3×10^{12} cm^{-2}, I_{OFF} degrades enormously from an order of 10^{-17}A to 10^{-9}A. However, as presented in **Figure 6.10(b)** above, the existence of ITC changes the super-threshold current slightly, and hence the current switching ratio is essentially reliant on the I_{OFF}. It is evaluated that the current switching ratio reduces from an order of 10^{12} (for the undamaged device) to 10^{5} (for a damaged device with donor trap charge density of 3×10^{12} cm^{-2}).

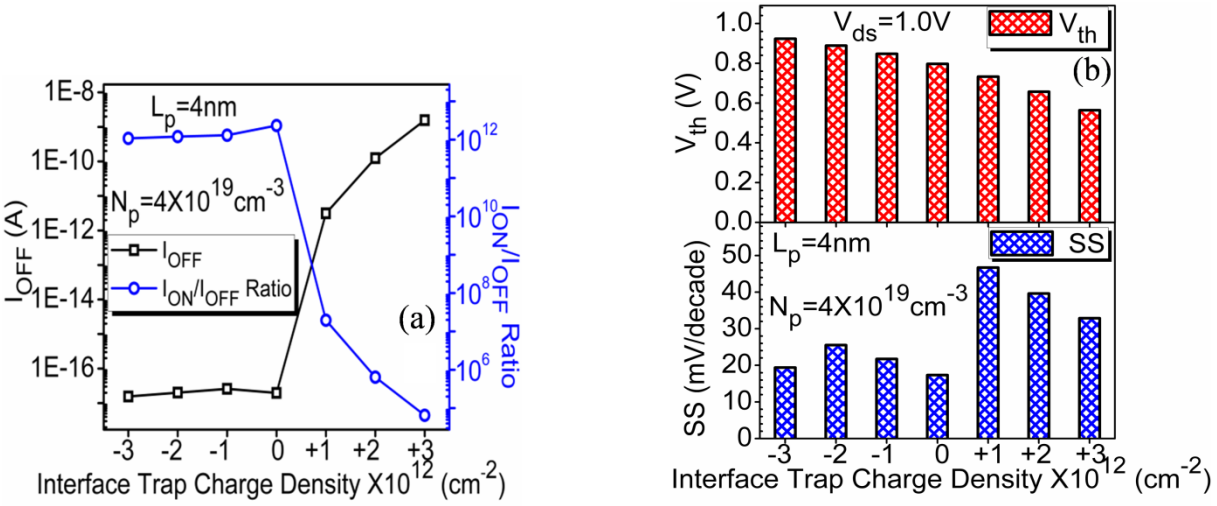

Figure 6.11 Impact of ITC density on (a) I_{OFF} and switching ratio (b) V_{th} and SS of PNIN-GAA-TFET at N_f = ±1, 2, 3(×12) cm^{-2} *(Madan and Chaujar, 2017b)*.

Moreover, the marginal variations of I_{OFF} for the presence of negative trap charges lead to unaltered I_{ON}/I_{OFF} for the presence of acceptor trap charges. The variations of V_{th} and the SS of PNIN-GAA- TFET for the presence of various ITC density and polarity is shown in **Figure 6.11(b)**. Results show that for the presence of positive (negative) ITCs, the V_{th} of the PNIN-GAA-TFET reduces (enhances). These shifts in the V_{th} caused by the localized charges are detrimental as it creates hindrance while using devices in circuits. However, the reduced

V_{th} for positive trap charges is attributed to the additional band bending that enhances the drive current and in a way switches the device ON at low gate bias. It is evaluated that the V_{th} reduces (enhances) by 29.26% (15.90%) at $N_f = \pm 3\times10^{12}$ cm^{-2}. The degradation in SS due to the presence of ITC is depicted clearly in **Figure 6.11(b)**. This deterioration in SS is due to the enormously enhanced I_{OFF} for positive ITC, though, the consequence of little variation in I_{OFF} and I_{ON} for acceptor ITCs is revealed by the insignificant change in SS at negative ITCs.

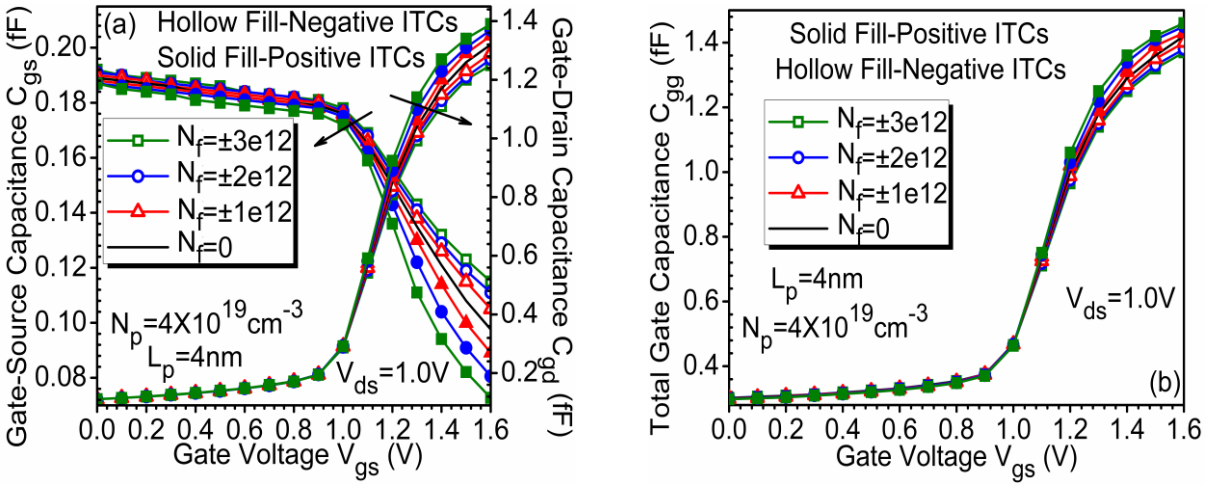

Figure 6.12 Influence of ITC density on (a) C_{gs}, C_{gd} and, (b) C_{gg} as a function of gate voltage of PNIN-GAA-TFET *(Madan and Chaujar, 2017b)*.

In addition, the dependence of operating speed of TFET on intrinsic capacitance and the unique switching mechanism of TFET dictates the examination of bias dependent intrinsic capacitances. **Figures 6.12(a-b)** presents the influence of ITC density on C_{gs}, C_{gd} and C_{gg} w.r.t V_{gs} at constant V_{ds}=1.0V. This shows that at lower V_{gs}, the inversion layer is first formed near the drain side, and with an increase in V_{gs}, it extends towards the source side as manifested in **Figure 6.12(a)**. Moreover, the reduced coupling between gate and source with an increase in V_{gs} monotonically decreases C_{gs} with increasing V_{gs}. Thereby, before the inversion layer formation, C_{gs} comprises the parasitic capacitance, and after the inversion layer is formed, the C_{gd} dominates. Additionally, the similar profile of C_{gg} and C_{gd} is essentially due to the small C_{gs} that results in similar C_{gg} and C_{gd}. It is assessed that the presence of positive (negative) ITCs increases (decreases) the C_{gd} by 0.1% (0.1%) at V_{gs}=0.0V and 8.5% (4.9%) at V_{gs}=1.2V. The effect of ITC density on C_{gg} as a function of V_{gs} of PNIN-GAA-TFET is displayed in **Figure 6.12(b)**. The consequence of immunity of C_{gd}

against ITC density due to low electric field at the drain channel junction is evident from the unaltered C_{gg} with ITC density.

An important RF FOM, i.e., f_T is plotted in **Figure 6.13** with respect to V_{gs} for various ITC density. It is observed that the presence of donor (acceptor) ITCs results in increase (decrease) of the f_T. This increase (decrease) of f_T is due to the enhanced (reduced) transconductance, on which f_T has a direct dependence. Furthermore, it is acquired that the peak of f_T, increases (decreases) more prominently at higher ITC density. It is examined at V_{gs}=1.0 V, that the presence of donor (acceptor) ITCs of $N_f = \pm 3\times12$ cm^{-2}, the f_T increases (decreases) by 2.06 (2.65) times respectively. As f_T of TFET has a direct variation with g_m and inverse variation with C_{gg}, thus, the demerit of higher C_{gd} in TFET, attributes to the lower f_T in comparison with the experimental conventional Si MOSFETs with equivalent gate length, as also reported in several published articles *(Yang et al., 2010, Cho et al., 2011, Mallik and Chattopadhyay, 2012)*.

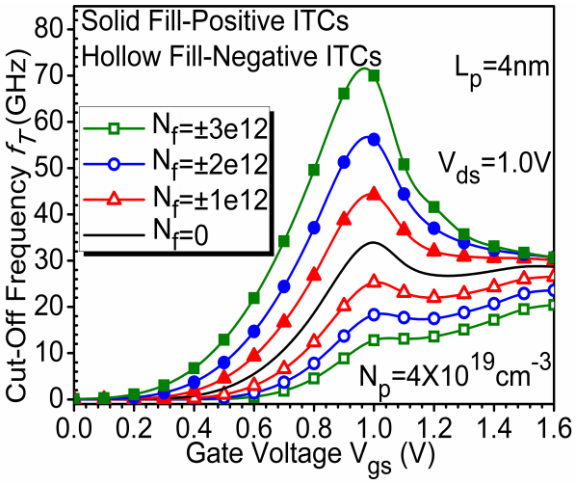

Figure 6.13 Effect of ITC density on f_T as a function of $V_{gs}$of PNIN-GAA-TFET (Madan and Chaujar, 2017b).

6.3.4 TEMPERATURE AFFECTABILITY

In this subsection, the temperature robustness of PNIN-GAA-TFET is investigated at constant ITC density. **Figure 6.14** shows the influence of temperature variations and ITCs on the n-BTBT rate. The motivation behind analyzing the temperature affectability is primarily the reliance of BTBT rate of electrons on temperature. Additionally, the property of semiconductor material used as source-drain and channel, such as the energy bandgap is also

reliant on temperature.

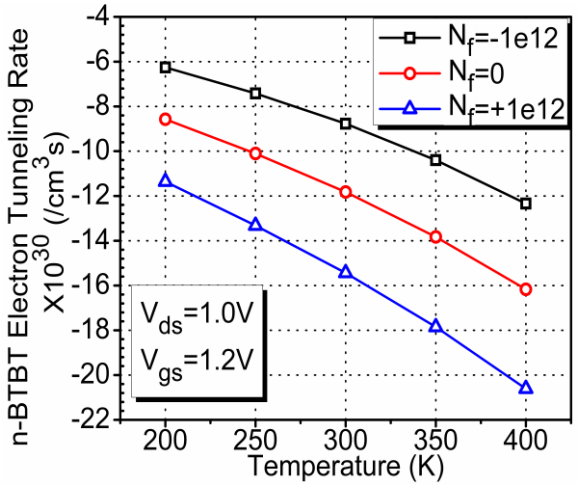

Figure 6.14 Variation of n-BTBT rate of electrons at the tunneling junction as a function of temperature of PNIN-GAA-TFET at $N_f = \pm 1\times12$ cm^{-2} *(Madan and Chaujar, 2017b).*

The energy band gap dependence on temperature has been experimentally measured *(Varshni, 1967)* and is numerically evaluated as:-

$$E_g(T) = E_g(0) - \frac{\alpha_E T^2}{T + \beta_E} \tag{6.2}$$

Where;

$E_g(0)$ is the energy band gap at T=0K, for Si, $E_g(0)$=1.170eV.

α_E, β_E are the material specific fitting constants, for Si, $\alpha_E=4.37\times10^{-4}$ eV/K, β_E=636K,

T is the absolute temperature.

It is inferred from Equation 6.2 that with an increase in temperature, the bandgap of a semiconductor decreases. Thereby, the reduced energy bandgap at elevated temperature narrows the tunneling barrier width and thus increases the BTBT rate of electrons. It is calculated that with an increase in temperature from 200K to 400K, the n-BTBT rate of electrons increases by 97.17%, and 81.46% for $N_f = 1\times12$ cm^{-2} and -1×12 cm^{-2} respectively.

The temperature robustness for a wide range of temperature (200K-400K) on the drain current as a function of V_{gs} at $N_f = \pm1\times12$cm^{-2} and for the undamaged device, i.e., with N_f=0 is shown in **Figure 6.15(a)**. It is examined that the transfer characteristics have bias dependent temperature affectability. The different transport mechanism for OFF and ON-state in TFETs is primarily liable for such asymmetric behavior in the subthreshold and

superthreshold regime for temperature variations. As is depicted in **Figure 6.15(a)**, that with the rise in temperature, the drain current increases exponentially in the subthreshold region. However, it increases marginally in the superthreshold regime. The exponential rise in the subthreshold region is offered by the dominance of Shockley-Read-Hall (SRH) recombination at lower gate bias; that has an exponential temperature dependence. However, in the superthreshold regime, the BTBT current dominates the conduction mechanism. The consequence of small temperature dependence of BTBT (that is caused by the bandgap narrowing with temperature) is dictated by the insignificant increase in I_{ds} at elevated temperatures in the superthreshold region. Moreover, the influence of temperature on transfer characteristics remains unaltered for donor/acceptor ITCs. The impact of temperature on I_{OFF} and the I_{ON}/I_{OFF} ratio at $N_f = \pm 1\times12$ cm^{-2} and for the undamaged device, i.e., with $N_f=0$ is presented in **Figure 6.15(b)**. Results show that with an increase in temperature from 200K to 400K, the I_{OFF} increases from 10^{-19}A to 10^{-15}A (for N_f=-1×12cm^{-2}) and from 10^{-14}A to 10^{-10}A (for N_f=+1×12 cm^{-2}). The degradation of I_{OFF} with temperature translates to deterioration in the current switching ratio. Quantitatively, degradation in I_{ON}/I_{OFF} from an order of 10^{14} to 10^{9}A (for N_f=-1×12cm^{-2}) and from 10^{9} to 10^{5} (for N_f=+1×12cm^{-2}) is observed with a rise in temperature from 200K to 400K.

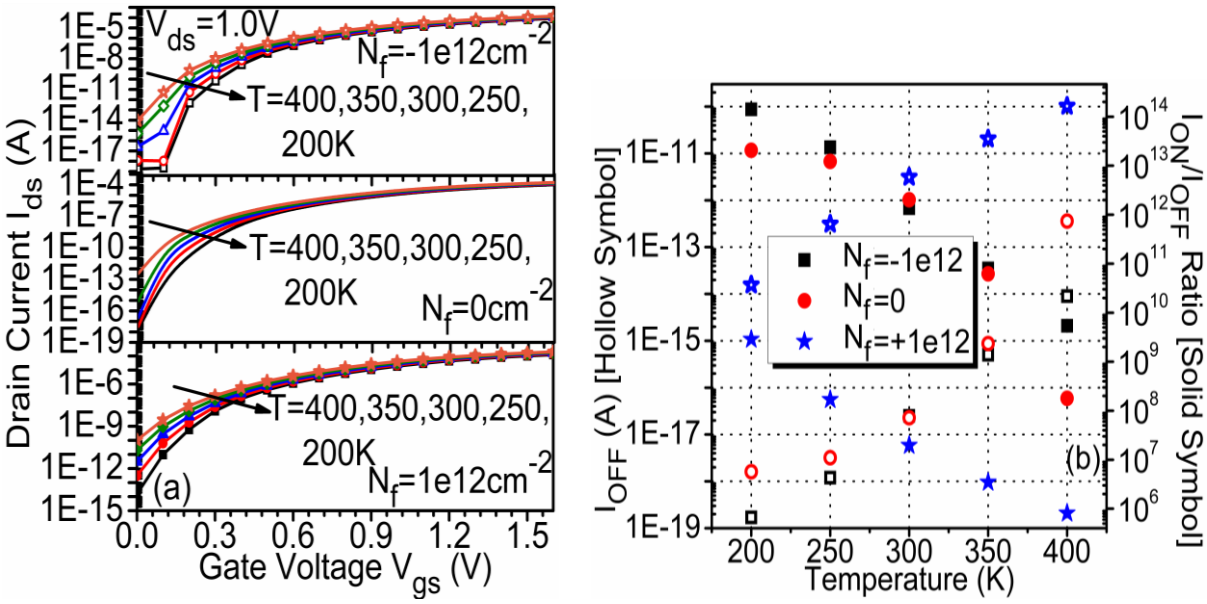

Figure 6.15 (a) Drain current (b) I_{OFF} and current switching ratio as a function of temperature (200-400K) of PNIN-GAA-TFET at $N_f = \pm 1\times12$ cm^{-2}*(Madan and Chaujar, 2017b).*

Figure 6.16(a) depicts the impact of temperature and ITCs polarity on V_{th} and SS of PNIN-GAA-TFET. The consequence of considerably high degraded I_{OFF} at elevated temperatures (instigated by SRH) and an inconsiderable increase in I_{ON} (induced by BTBT) is degradation of the SS at elevated temperatures. It has been evaluated that for an increase in temperature from 200K to 400K, the SS increases by 83.23% and 25.43% for N_f=-1×12cm^{-2} and N_f=1×12 cm^{-2} respectively. As discussed above in **Figure 6.15(a)**, I_{ds} increases at elevated temperature, i.e., PNIN-GAA-TFET have positive temperature coefficient for entire gate bias range viz. in both subthreshold and superthreshold region. This enhanced I_{ds} at elevated temperature marks in reduced V_{th}.

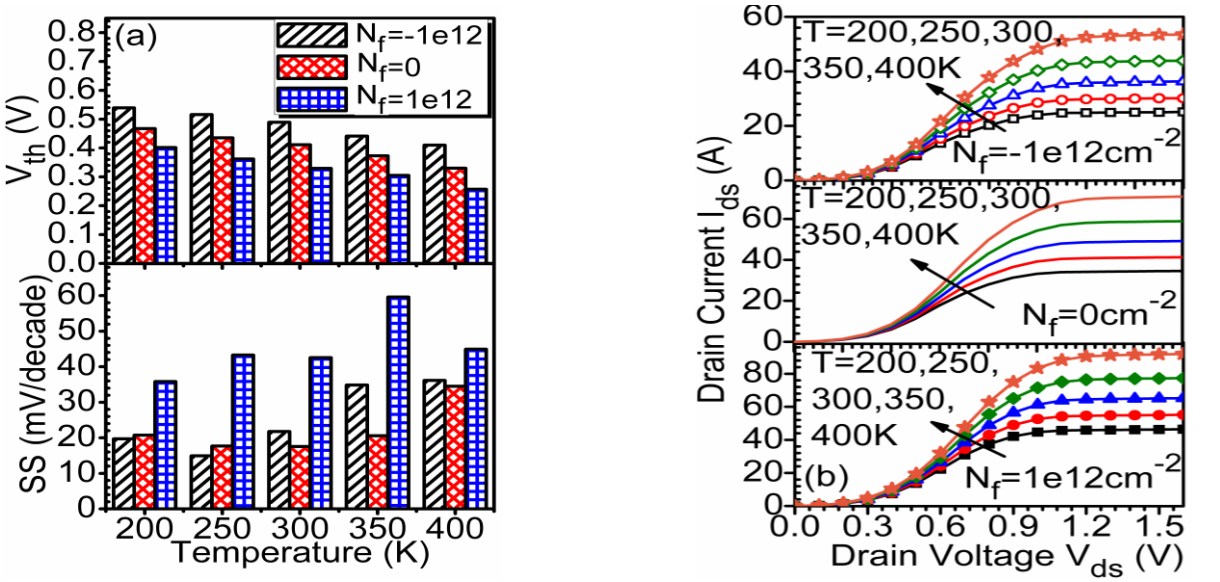

Figure 6.16 (a) V_{th} and SS as a function of temperature (b) output characteristics at V_{gs}=1.2V, for temperature range of (200-400K) of PNIN-GAA-TFET *(Madan and Chaujar, 2017b)*.

Further, as inferred from Equation 6.2, the bandgap of Si reduces at higher temperatures that consequently lowers the barrier width at the source and n^+ pocket of PNIN-GAA-TFET. The narrower barrier width translates into high tunneling probability of electrons and thereby switches the device at lower gate bias (reduces the V_{th}) at elevated temperatures. It is evaluated that for an increase in temperature from 200K to 400K, the V_{th} decreases by 23.92% and 36.05% for N_f=-1×12 cm^{-2} and N_f=1×12 cm^{-2} respectively. **Figure 6.16(b)** shows the output characteristics of PNIN-GAA-TFET for a wide temperature range of 200K - 400K including the impact of ITCs. In consistent with the above results, the drain current enhances at elevated temperatures. It is evaluated at V_{gs}=1.2V, that with a rise in temperature from

200K to 400K, the I_{ds} increases by 2.11 times, 2.03 times and 1.97 times for N_f=-1×12 cm^{-2}, N_f=0 and N_f=+1×12 cm^{-2} respectively.

The above analysis reveals that the temperature affectability is maximum in the subthreshold region. Thus, a quantitative analysis of the impact of ITCs on the temperature sensitivity (S_T) of the I_{OFF} variability has been done. The S_T of PNIN-GAA-TFET as a function of ITCs is depicted in **Figure 6.17** and is evaluated as *(Gautam et al., 2014)*:

$$S_T = \left(\frac{\partial \log(I_{OFF})}{\partial T} \right)^{-1} \text{ K/decade} \tag{6.3}$$

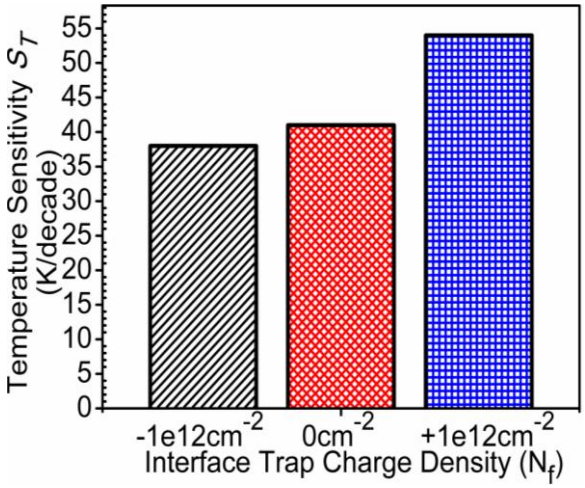

Figure 6.17 Influence of ITCs on temperature sensitivity of the I_{OFF} variability of PNIN-GAA-TFET at N_f = ±1×12 cm^{-2} and N_f=0cm^{-2} *(Madan and Chaujar, 2017b)*.

As is manifested from **Figure 6.17**, the presence of ITCs modifies the S_T of the device. It is assessed that the donor (acceptor) ITCs increases (decreases) the S_T of PNIN-GAA-TFET by 31.70% (7.89%) w.r.t the ideal device. Furthermore, it is examined that for the ideal device, a change in ambient temperature by 41K alters I_{OFF} by an order of a decade. However, for the presence of donor (acceptor) ITCs, a change in temperature by 54K (38K) alters I_{OFF} by an order of 1 decade. Subsequently, the presence of positive (negative) trap charges enhances (reduces) the temperature sensitivity that must be detrimental for the devices used for sensors applications, in temperature sensitive environment.

For the high-speed analog/digital applications, the inspection of intrinsic capacitances is necessary. To examine the behavior of inherent capacitances at wide temperature range, the total gate capacitance (C_{gg}) as a function of V_{gs} is plotted in **Figure 6.18(a)**. It is analyzed that

C_{gg} increases with an increase in V_{gs}. This increase in C_{gg} with V_{gs} is attributed to the fact that at constant V_{ds} and at low V_{gs}, the inversion layer is formed near the drain side. After the inversion layer formation, further increase in V_{gs} extends the inversion layer towards the source side. Additionally, it is exhibited that with an increase in temperature, the C_{gg} increases. It is evaluated at V_{gs}=1.1 V, that an increase in temperature from 200K to 400K, the C_{gg} increases by 51.87%. The temperature dependence of f_T as a function of gate bias is shown in **Figure 6.18(b)**. Due to the positive temperature coefficient of drain current, g_m also increases with temperature and hence results in increase in f_T with temperature. It is evaluated that at V_{gs}=1.0V, for N_f=-1×12 cm^{-2} and 1×12 cm^{-2}, an increase in temperature from 200K to 400K, increases f_T by 23.97% and 11.76% respectively.

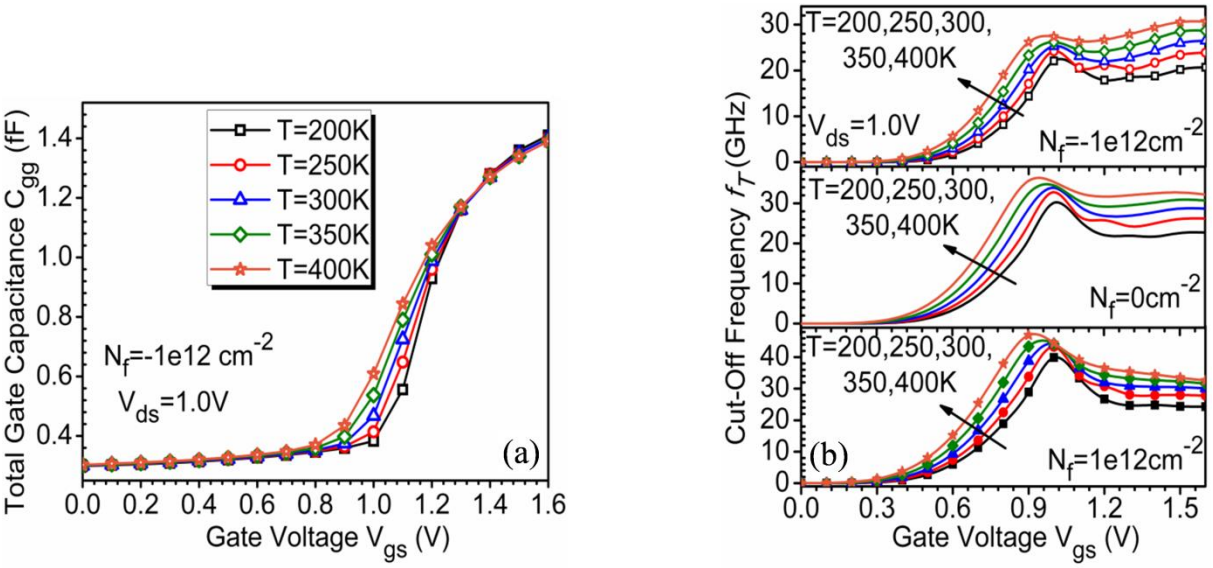

Figure 6.18 (a) Variations of C_{gg} as a function V_{gs} at temperature range of 200-400K (b) f_T as a function of V_{gs} at temperature range of (200-400K) of PNIN-GAA-TFET at N_f = ±1×12 cm^{-2} *(Madan and Chaujar, 2017b)*.

6.4 SUMMARY

Firstly, this chapter works on to design a gate-drain underlapped (GDU) n^+ source pocket gate all around tunnel FET (GDU-PNIN-GAA-TFET). In GDU-PNIN-GAA-TFET, the n^+ source pocket implanted in the channel near the source side pedals the tunneling junction and thus improves the ON-state characteristics of GAA-TFET. GDU administers the drain-channel junction and thus controls the ambipolar conduction in the device. Results show that jointly GDU and n^+ pocket leads to enormously improved ON-state characteristics, i.e.,

I_{ON} to an order of 10^{-4} A and V_{th} of 0.4V and suppresses ambipolar current to 10^{-18}A. Hence, the challenges faced by TFET that restricts it for the practical applications have been overcome. Additionally, GDU also reduces the parasitic capacitances, and n^+ pocket enhances the transconductance thereby, collectively GDU-PNIN-GAA-TFET leads to a superior RF performance. This exhaustive insight demonstration in terms of analog/RF performance for GDU-PNIN-GAA-TFET may assist the analog/RF circuit designers, and the proposed GDU-PNIN-GAA-TFET may work as a superior candidate for high speed and low power applications. The chapter continues to encompass the reliability of PNIN-GAA-TFET. The reliability is examined by analyzing the viability of the PNIN-GAA-TFET under (i) presence of different interface trap charges (donor and acceptor) of different density and (ii) wide temperature range. Results reveal that the presence of donor (acceptor) trap charges enhances (reduces) the parallel (E_y) and normal (E_X) component of the electric field. Consequently, the enhanced E_y increases the BTBT rate of electrons. On the other hand, the increased E_X contributes to the generation of interface defects and also to the gate leakage current and thereby vitiates the reliability of the device. Furthermore, detrimental degradation in I_{OFF} is realized for the presence of positive trap charges. In addition, for the presence of negative trap charges, there is a marginal variation in the I_{OFF}. Also, it is obtained that for the presence of ITCs, the super-threshold characteristics are marginally altered. While analyzing the device characteristics under wide temperature range, it is examined that the drain current degrades exponentially in subthreshold region, however, there is marginal increase in drain current in the superthreshold regime. Additionally, PNIN-GAA-TFET shows a positive temperature coefficient for the complete gate bias range. Importantly, it is investigated that the temperature sensitivity of the PNIN-GAA-TFET, is also altered by the ITCs; that is harmful to the device operating in the temperature sensitive ambience. The results acquired in this chapter could be of assistance while designing TFETs for employing in a temperature sensitive environment.

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CHAPTER 7

SUMMARY, CONCLUSION AND FUTURE SCOPE

This chapter recapitulates the overall work carried out in this thesis. In addition, the concrete conclusion drawn from the results obtained are also briefly highlighted. Thereafter, this chapter describes the possible future scope of the work that could be done in future to extend the research.

7.1 SUMMARY AND CONCLUSION

The un-scalable subthreshold swing (SS) owing to the inherent conduction mechanism of MOSFET is the dominant force for researchers to explore novel devices that primarily use another mode of carrier transport (other than thermionic emission of carriers). In this regard, the tunnel field effect transistor (TFET) that utilizes the interband tunneling could assist the next generation of logic transistors operational at less than 0.5V supply voltage. In this thesis, a Gate All Around architecture TFET is mainly encompassed as it provides the extremely high packing density and also significantly high tunneling area. Moreover, to overcome various challenges faced by conventional TFET, different engineering schemes have also been integrated on GAA-TFET. At the outset, a hetero gate dielectric, gate metal engineered gate all around TFET, i.e., HD-GME-GAA-TFET has been proposed to acquire lower SS, higher I_{ON}, suppressed I_{AMB} along with low leakage current. Furthermore, for exhaustive understanding, a mathematical modeling is developed for HD-GME-GAA-TFET, and the developed analytical model is used to analyze various electrical and analog parameters of the proposed device as illustrated in **Chapter 2**. The model is further used to optimize the parameters of the proposed device such as the gate metal work functions of GME scheme and the gate oxide dielectric for HD engineering. Moreover, to account for the gate and drain bias affectability over the device characteristics, the device is inspected under various gate and drain bias conditions. Further, the influence of gate oxide thickness has also been investigated, and it was obtained that for thinner gate oxides, the analog performance of the proposed TFET improves. While analyzing the impact of high-k dielectric present near the source side, it is achieved that at k=21, i.e., for HfO_2, the proposed GAA-TFET has shown superior characteristics regarding various analog parameters. Furthermore, the optimized results for GME engineering schemes have been obtained at a gate metal work function near the source and drain of 4.3eV and 4.8eV respectively. It is assessed at the optimized design of HD-GME-GAA-TFET, that the proposed device marks in $I_{ON}/I_{OFF}=1.09\times10^{13}$, $I_{OFF}=1.18\times10^{-17}$A, $V_{th}=0.6$V and SS=30.31mV/decade. Thereby, the considerably low I_{OFF} translates in lower static power dissipation along with the lower SS, higher device gain, better device efficiency, and the higher I_{ON}/I_{OFF} ratio and make HD-GME-GAA-TFET a competent candidate for the low power analog applications.

In addition to superior analog performance, the sub-nm scaled TFET that promises the high integration must ensure the excellent RF performance. Further, with the intensified

growth of wireless communication market, CMOS devices must guarantee for the minimum parasitic capacitances and subsequently, the high speed. Thus, to ensure for the superior RF/microwave performance of the proposed device, i.e., HD-GME-GAA-TFET has been explored for various small signal parameters and RF Figure of Merits (FOMs) and is the central point of discussion in **Chapter 3**. Thus, **Chapter 3** evaluates the intrinsic parasitic capacitances along with several power gains such as maximum available power gain (Gma) unilateral power gain, and current gain. Additionally, the critical RF FOMs, i.e., the cut off frequency (f_T), maximum oscillation frequency (f_{Max}), intrinsic delay (τ) has also been explored. Entire results have been examined for the various configurations of gate metals of the GME engineering scheme and are also compared with single metal gate configuration of the proposed device. It is investigated that with the application of GME engineering, superior benefits of TFET are acquired in all RF metrics. Appreciable enhancement in the cut off frequency and the maximum oscillation frequency has been obtained with the integration of GME scheme. This superior RF performance acquired by the GME scheme reveals the efficacy of the HD-GME-GAA-TFET for the high-frequency amplifier and microwave applications. Further, the enhanced ON-current and transconductance obtained by GME scheme results in increase in the various power gains consequently giving a new opening for HF wireless and switching applications. Additionally, the reduced intrinsic delay and parasitic capacitances with GME engineering make it appropriate for analog and digital switching applications. For comprehensive RF analysis of HD-GME-GAA-TFET and its effectiveness at HF, the admittance parameters are also requisite that is suitable for assessing the microwave performance regarding input/output and transfer admittance. Thereby, the chapter continues to investigate the small signal Y-parameters. The analysis of Y-parameters revealed the improvement in small signal Y-parameters obtained with the GME architecture which is beneficial for the RF communication. So, HD-GME-GAA-TFET can be efficiently employed in high-switching-speed electronics.

Furthermore, for sub-nm devices, reliability is of serious concern, owing to various process/stress/radiation damages that induce interface charges at the Si-SiO_2 interface. It is ideally assumed in almost all the research articles that the interface of Si-SiO_2 is free from any defects or there is no interface defect along the SiO_2-Si interface. However, practically a large number of positive/negative charges are present along the SiO_2-Si interface and also ionic charges may be found within the SiO_2 layer. These interface trap charges (ITC) may be

reduced significantly by advanced fabrication techniques but can never be uprooted, and thus they appear inevitably in any fabricated transistor. Thus, to ensure the reliability of the device, it is essential to investigate the characteristics of the device in the presence of various ITCs that is the primary focusing area of **Chapter 4**. Along with the reliability in terms of ITCs, the performance of the device regarding various analog and RF parameters has also been inspected under wide temperature range, to ensure the temperature range under which the device can be employed efficiently. Thus, a comparative analysis of GAA-TFET and HD-GAA-TFET has been done in the presence of ITC of different polarity, i.e., positive and negative ITCs, and the results are compared with the ideal device with no ITC. Precisely, the presence of positive (negative) ITC reduces (enhances) the flat band voltage (V_{fb}) that is followed by a linear increase (decrease) in the effective gate bias V_{eff} at the source channel junction. The enhanced (reduced) V_{eff} translates in increase (decrease) in the electric field and thereby enhances (reduces) the BTBT rate of electrons followed by the similar variations in the drive current. However, the corresponding increase/ decrease in V_{fb} and thus the drain current are not as much in HD-GAA-TFET w.r.t. its conventional counterparts, i.e., GAA-TFET. The reduced variations in case of HD-GAA-TFET are primarily offered by the presence of high-k dielectric near source side that enhances the gate oxide capacitance and thereby reduces the alterations in the flat band voltage V_{fb}. Thus, the HD-GAA-TFET results in better immunity against ITCs along with the superior analog and RF performance as discussed in **Chapter 2** and **Chapter 3**. The chapter continues to investigate the device for linearity and distortion parameters. The improved linearity FOMs such as superior higher order transconductance parameters, VIP_2, VIP_3, IMD_3, IIP_3, 1-dB compression point and zero crossover point has been acquired with the amalgamation of HD. Also the significantly improved high-frequency gain has also been obtained with HD engineering owing to the increased transconductance that has a direct reliance on the high-frequency gain. As ITCs inevitably occurs in a real device, thus the data investigated in this chapter would assist during device designing. Hereafter, the chapter examines the device performance at wide temperature range. In the course of examination of temperature robustness, it is revealed that the reliance of transfer characteristics of GAA-TFET on temperature is bias dependent. Precisely, the drain current has exponential temperature dependence in the subthreshold region owing to the dominance of SRH. Additionally, in the superthreshold region, the BTBT oversees the SRH, and governs the conduction mechanism. Being temperature independent the drain current

shows marginal enhancement (instigated by the band gap narrowing) with temperature in the superthreshold regime. It is worth to mention that this bias dependent temperature reliance in case of TFET is dissimilar to MOSFET, which shows a positive temperature coefficient all through. Further, it is obtained that the rise in temperatures degrades the parasitic capacitances. Results show the suitability of HD-GAA-TFET at low temperature that essentially provides a pathway to meet the growing demand for low-temperature tolerance of the logic circuits in aircraft, space technology and for large-scale integration applications.

However till this, the GAA-TFET is inspected for only the positive gate bias, and the negative gate bias has not been accounted, which fundamentally reveals the ambipolar behavior. As the ambipolar current of TFET put strong implications for its applicability in digital applications, thus the thesis continues to explore the ambipolar current of HD-GAA-TFET in **Chapter 5**. **Chapter 5** works on to suppress the ambipolar current such that the ON state current must not degrade. To suppress the ambipolar conduction, the gate metal is overlapped over the drain side, i.e., GDO engineering scheme has been amalgamated on GAA-TFET. Moreover, to enhance I_{ON}, HD engineering has also been integrated on GAA-TFET along with GDO. Consequently, the integration of both GDO and HD simultaneously on GAA-TFET (i.e., GDO-HD-GAA-TFET), improves the I_{AMB} and I_{ON} respectively, and thereby conquers the major bottleneck of TFET. Thus, the suppressed I_{AMB} and superior I_{ON} results in comprehensively enhanced analog performance of GDO-HD-GAA-TFET and make it a suitable candidate for analog/digital circuitry applications. It is quantitatively examined that GDO of length 8nm can reduce the I_{AMB} to 10^{-17}A. Results reveal that although the GDO controls I_{AMB} efficiently, it concurrently degrades the RF performance of GAA-TFET. Thus, to overwhelm the degradation caused by GDO, a vacuum gate dielectric has been inserted over the region of gate-drain overlap length. Results show that the vacuum dielectric inserted over the overlapped length reduces the parasitic capacitances and thereby improves the cut-off frequency. Therefore, GDO-HD-GAA-TFET with vacuum dielectric over L_{ov} may compete with the growing demand of high-speed analog and low power RF circuits.

Chapter 5 continues as its part-2 for the capability of GAA-TFET in gas sensing applications. In this regard, a Palladium gate metal is employed (instead of the conventional metal gate) that essentially have the high selectively for the hydrogen gas molecules. In this respect, a HD-GAA-TFET based H_2 gas sensor has been proposed. The proposed gas sensor combines the merits of interband tunneling (instigated by TFET) along with the GAA

architecture that gives the possibly high surface area and thereby the proposed HD-GAA-TFET, delivers substantially high sensitivity. Moreover, it is examined that the sensitivity of the proposed gas sensor towards H_2 gas detection is significantly high as compared to conventional MOSFET, conventional TFET, and GAA-TFET. Further, the performance of the proposed gas sensor has been inspected at wide temperature range. Results reveal that the proposed hydrogen gas sensor is adequately stable over wide temperature range of 200K-400K and thereby mark it a viable gas sensor. Furthermore, the radius of the proposed gas sensor is varied to judge it for the highest sensitivity and it is observed that at a radius of 10nm, the proposed gas sensor provides optimized sensitivity. After inspecting the sensitivity and stability of the proposed gas sensor, the chapter continues to examine its static performance in terms of BTBT rate of electrons, V_{th} and SS. Numerical simulations reveal that the highly sensitive proposed HD-GAA-TFET hydrogen gas sensor may fulfill the everlasting demand for automotive, environmental monitoring, petroleum refining process, and medical industries.

However, the presence of high-k dielectric material near source side in HD engineering scheme enhances the parasitic capacitances and thereby limits its switching speed. Thus, in **Chapter 6**, a new device with n^+ source pocket in the channel near source side i.e., PNIN-GAA-TFET is designed to overwhelm the challenge of lower I_{ON} and the higher V_{th} of TFET. **Chapter 6** is primarily divided into two parts; part-1 of the chapter integrates the merits of short gate (or the gate-drain underlapping) with PNIN-GAA-TFET that results in GDU-PNIN-GAA-TFET. The gate metal is underlapped near the drain to control the ambipolar conduction and the n^+ source pocket pedals to upgrade the drive current and the V_{th}. Exhaustive simulations have been done for a comprehensive inspection of gate-drain underlapped, n^+ source pocket GAA-TFET, i.e., GDU-PNIN-GAA-TFET. It is analyzed that implanting a n^+ pocket near source side leads to a steeper band bending at the tunneling junction. Consequently, the stepper band bending translates in high tunneling probability and eventually results in high I_{ON} and lower V_{th}. Additionally, via underlapping the gate metal near drain side, i.e., by GDU engineering scheme, the drain channel junction is administered. The GDU resists the extension of charge carrier density (build up under the gated region) towards the drain side precisely, underneath the underlapped region. The depletion of carrier density beneath the underlapped region broadens the tunneling width at the drain channel junction that subsequently suppresses the ambipolar conduction. Moreover, the GDU and n^+

source pocket are uncoupled and deal with the ambipolar and ON-state conduction respectively. Consequently, the collective amalgamation of GDU and n^+ pocket, i.e., GDU-PNIN-GAA-TFET results in comprehensive up gradation in analog performance. The designed GDU-PNIN-GAA-TFET, provides I_{ON}~10^{-4}A, V_{th}=0.4V and significantly suppressed I_{AMB} =10^{-18}A. Besides, the proposed device is analyzed for the HF performance and also for the parasitic capacitances. Results show that along with suppressing the ambipolar conduction, GDU reduces the Miller capacitances of GAA-TFET that is among one of the significant challenges faced by TFET. Thereby, the improved parasitic capacitance (prompted by GDU) and the enhanced transconductance (prompted by n^+ pocket) leads to a superior RF performance as well. Henceforth, the challenges faced by TFET that constrains it for the practical applications have been overcome. This thorough comprehension demonstration in terms of analog/RF performance for GDU-PNIN-GAA-TFET may assist the analog/RF circuit designers while designing a high speed and low power transistor. Part-2 of the chapter deals with the reliability and temperature robustness of PNIN-GAA-TFET. The impact of ITC density and polarity has been first examined for inspecting the viability of PNIN-GAA-TFET and after that, the effect of temperature variations is analyzed. It is reviewed that the positive (negative) ITC increases (reduces) both the electric field components, i.e., the parallel (E_y) and normal (E_X) electric field. The enhanced E_y directly impact the BTBT rate of electrons and E_X vitiates the reliability of the device by generating the interface defects. Moreover, it is examined that the donor trap density remarkably degrades I_{OFF} whereas for the acceptor traps, the I_{OFF} varies marginally. The superthreshold characteristics are, however, slightly altered by the presence of these ITCs. For inspecting the temperature robustness, the device attributes are investigated under wide temperature range. Temperature variations reveal that the subthreshold current enhances exponentially with temperature whereas the superthreshold current rises marginally at elevated temperature. One essential parameter, i.e., the temperature sensitivity of the device is also analyzed and is examined that it is altered by the ITCs that is harmful while employing device in the temperature sensitive ambience. The results acquired in this chapter could be of assistance while designing TFETs for employing in a temperature sensitive environment.

7.2 FUTURE SCOPE

The key encompassing objective of this thesis is to design a TFET which can overwhelm the major shortcomings of TFET. Further, the proposed device design is also investigated for their reliability in terms of interface trap charges that are inevitably present along the interface of Si-SiO_2 of any practical device. Another objective of this research work is to examine the proposed device under wide temperature range to check the temperature robustness while employing the device under temperature sensitive environment. Additionally, the applicability of the device as a gas sensor has also been investigated. All the objectives are though majorly accomplished through analytical modeling and extensive numerical simulations. However, in view of above work, it would be interesting to explore and extend the following aspects as the future aspects.

1. The work done in this thesis accounts for only the fixed ITC, and the impact of mobile charges are overlooked. Thus, to comprehend the reliability aspects in terms of defects, it is needed to analyze the device under both mobile and fixed ITC and hence it could be taken up as a future work.
2. The work done has accounted for only Si as a source, channel and drain material and chiefly the numerous engineering schemes have been explored for defeating the challenges faced by conventional TFET. Thus, the device must be analyzed by employing various materials that essentially deals with the material engineering and could be addressed in future.
3. Further, the device is inspected at wide temperature ranges for the analog and RF performance. Additionally, the thermal parameters can be investigated such as the heat capacity, heat conductivity, and total heat power to analyze its applications in the heat sink and a heat source in radiation tolerant applications of analog and digital circuits.
4. It would be worthy to explore the noise behavior of GAA-TFET regarding noise performance metrics such as Noise Figure, Auto-Correlation, Cross-Correlation, etc., hence, presenting it as an attractive solution for the on-going integration process in analog and digital design technology, and for designing Low-Noise Amplifiers.

5. The circuit response of the proposed GAA-TFET can also be done to employ it for digital circuit applications such as for CMOS inverters, RAM, and other gated logic designs.
6. Moreover, the device design can be utilized as a biochemical sensor which can sense both harmful gases as well as bio-molecules such as proteins, DNA, glucose or in cancer detection. GAA-TFET based sensor may offer several advantages, such as small detector size, lightweight, minimal power requirement, ease of use and instant readout.

Numerical Simulation of N^+ Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature

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***Abstract*— This paper investigates the reliability of PIN-gate-all-around (GAA)-tunnel field-effect transistor (TFET) with N^+ source pocket. The reliability of the PNIN-GAA-TFET is examined by analyzing: 1) the impact of interface trap charge (ITC) density and polarity and 2) the temperature affectability on analog/RF performance of the device. It is realized that the interface traps existing at the Si/SiO_2 interface modifies the flatband voltage and, thereby, alters the analog and RF characteristics of the device. The analysis is done at various trap charge densities and polarities. The results, thus, obtained reveal that, at higher trap charge density, the device performance alters significantly. It is obtained that, for a donor trap charge density of 3×10^{12} cm^{-2}, the off-state current of the device degrades tremendously (increases from an order of 10^{-17}–10^{-9}A). The temperature affectability over the device reveals that, at lower gate bias, the Shockley–Read–Hall phenomenon dominates and degrades the subthreshold current of the device at elevated temperatures. However, for the superthreshold regime, the band-to-band tunneling (BTBT) mechanism dominates. Furthermore, the results show enormous degradation in the off-state current at elevated temperatures, such that, with an increase in the ambient temperature from 200 K to 400 K, the I_{OFF} degrades by an order of 10^5, i.e., increases from 10^{-18} A to 10^{-13} A. The results specify that the PNIN-GAA-TFET is insusceptible to the acceptor traps existing at the Si/SiO_2 interface in comparison with the donor traps.**

***Index Terms*— Interface trap charges (ITCs), N^+ source pocket, temperature sensitivity, tunnel FET (TFET).**

I. Introduction

PERPETUAL miniaturization of complementary metal–oxide–semiconductor (CMOS) devices has incredibly revolutionized many areas, such as security, military, mobile communications, and medicine. However, downscaling the CMOS technology results in severe problems, such as high leakage current, high subthreshold swing (SS), and other short channel effects [1]. These challenges enforce for exploring the novel devices that work on new operation mechanisms other than thermionic emission over the thermal barrier as in the case of MOSFET. In this regard, tunnel field-effect transistors (TFETs) that use interband tunneling in the source and channel junction with a control of gate bias has attracted much attention [2]–[6]. The major challenges faced by MOSFET, such as the limitations on the SS that has a fundamental limit of 60 mV/decade and high OFF-state leakage current, have been overcome by TFET up to a great extent. In TFET, the large tunneling barrier width present at the source–channel junction at lower gate bias blocks the tunneling of electrons and, thereby, benefits a very low leakage current. However, the band-to-band tunneling (BTBT) of carriers from the source potentially allows a steep SS values [7]. Apart from these merits, TFET suffers from low ON-current, high threshold voltage (V_{th}), high gate–drain parasitic capacitance, and ambipolar current [8], [9]. For superior analog/RF performance, many device engineering architectures and III–V materials have also been proposed by various researchers [2], [8], [10]–[15]. Among all device engineering architectures, the N^+ source pocket p-i-n TFET or PNIN-TFET proposed by [14] is a strong candidate as it offers higher ON-current with lower SS and lower V_{th}. III–V TFET, however, mitigates the problem of lower I_{ON} offered by their lower bandgap, lower effective mass, and wide range of band alignments; thus, III-V material-based TFETs have the potential of high switching speed, but at the same time suffering from large SS [16]. However, the basic device characteristics, such as improved analog, RF, and linearity of TFET, have been the major encompassing area of the investigation up to now. Recently, Moselund *et al.* [9] fabricated lateral p-type InAs/Si TFET with I_{ON} of a few μA/μm for $|V_{ds}| = |V_{gs}| = 0.5$ V. A SiGe/Si heterostructure TFET has been fabricated by Blaeser *et al.* [17] that shows I_{ON} of 6.7 μA/μm at $V_{dd} = 0.5$ V and SS of ~80 mV/decade. Nonetheless, for sub-100-nm devices, the reliability of TFET is also a critical concern, owing to the strong electric field at the source–channel junction. This strong electric field roots to the generation of defects at the $Si–SiO_2$ interface [18]. Along with the high electric field, the fabrication processes for sub-100-nm devices, such as the plasma etching, may damage the gate oxide and the Si-oxide interface. These defects are the origin of fixed interface and oxide

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charges. These fixed charges can adversely affect the yield and reliability, and also alters the ideal predicted device characteristics [19], [20]. The impact of interface trap charges (ITCs) has also been investigated on lateral p-type InAs/Si (a III–V TFET) by Sant *et al.* [21], which reported that the high concentration of trap centers formed at the heterojunction of III–V material (source side) and the silicon (channel region) attributes to the carrier generation by the trap-assisted tunneling (TAT) at the heterojunction, which degrades the SS of TFET. The large trap centers at the interface of III–V TFET evaluate the charge density at the interface and, thereby, alter the device electrostatics. In addition to the traps present at the heterojunction, for a III–V TFET, the traps at the interface of channel and oxide add to further degradation of the subthreshold characteristics of TFET. However, till date, not much has been reported regarding the study of the impact of ITCs on the reliability of TFET [18]–[20], [22]–[24]. Moreover, to meet the everlasting demand of transistors with high- and low-temperature tolerance (other than the room temperature) needed in aircraft, space, and automotive technology, the temperature affectability over the device performance must be analyzed [25], [26]. In addition, with an increase in number of on-chip transistors, the heat dissipation increases drastically. Therefore, the operating temperature of transistor also increases. Thus, for better reliability, it is obligatory to analyze the performance of the device at various ambient temperatures. Dey *et al.* [16] and Mookerjea *et al.* [27] reported that the temperature dependence of III–V TFET is a strong function of gate bias, due to the onset of various conduction mechanisms at different gate-bias regions. At lower gate-bias region, the consequence of exponential temperature dependence of Shockley–Read–Hall (SRH) generation recombination results in the exponential rise of I_{OFF}. Further increase in the gate bias thermally excites the carriers from the trap centers into the conduction band. However, at higher gate-bias region, the BTBT contributes to the drain current with negligible contribution from the trap centers. Moreover, it is reported in [27] that the peak interface state density is in the middle of the energy bandgap. Therefore, the major contribution of the midgap traps at the oxide–semiconductor interface in the tunneling process causes a degradation in SS at elevated temperatures. The surface passivation is recommended for reducing the TAT and the degradation caused at the elevated temperatures and the ITCs to the SS and I_{OFF}. In this work, the gate-all-around (GAA) architecture with N^+ source pocket PIN-TFET is considered, and an elaborate study of its analog characteristics and RF figure of merits is reported, including the impact of ITC density and polarity at various ambient temperatures.

II. Device Analysis and Simulation

Fig. 1(a) shows the 3-D view of simulated device structure, i.e., N^+ source pocket PIN-GAA-TFET (PNIN-GAA-TFET). For PNIN-GAA-TFET, the source pocket length (L_p) and the source pocket (N^+) doping (N_p) are assessed for the optimized analog characteristics, and the optimum values of L_p and N_p are obtained as 4 nm and 4×10^{19} cm^{-3}, respectively, as shown in our previous work [4].

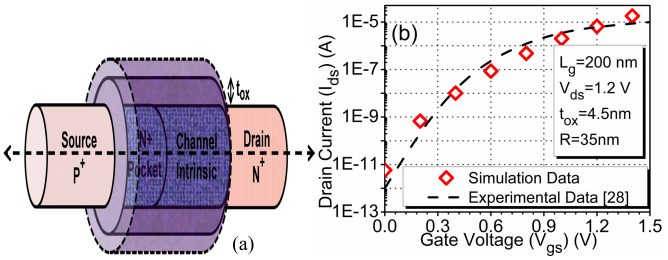

Fig. 1. (a) Simulation structure of PNIN-GAA-TFET. (b) Comparison of experimental [28] and simulated I_{ds}–V_{gs} of GAA-TFET.

The device parameters such as the channel length (L_g), gate oxide thickness (t_{OX}), and radius (R) of the device under consideration are 50, 3, and 10 nm, respectively. The source, channel, and drain are of silicon. The source (P^+), channel, and drain (N^+) regions are uniformly doped. The source is p^+-type doped (1×10^{20} cm^{-3}), and the drain is n^+-doped (5×10^{18} cm^{-3}). The drain doping is 5×10^{18} cm^{-3} (i.e., less than source doping), to minimize the drain–channel tunneling and, thus, the ambipolar conduction [29]. Furthermore, an optimum value of gate metal work function, i.e., 4.3 eV has been chosen for optimum better subthreshold characteristics.

A. Simulation Methodology

The PNIN-GAA-TFET is simulated using the ATLAS device simulator [30]. For TFETs, the BTBT model is significantly important. Local BTBT model estimates a triangular barrier approximation in the energy bands and, thus, considers a constant electric field at the entire tunneling region. However, the non-local BTBT incorporates the dynamic changes in the electric field at the entire tunneling path. Thus, the non-local BTBT that calculates the generation rate at each mesh point in the tunneling region is incorporated in this work [31]. In addition to the non-local BTBT model, concentration- and field-dependent mobility model, SRH model for carrier recombination, bandgap narrowing, and Fermi–Dirac statistics are also invoked during simulation. Besides, Gummel (decoupled) and Newton's (fully coupled) methods have been used to numerically solve the carrier transport equation. Owing to the strong electric field at the source–channel (tunneling) junction, the ITCs are considered only at 10-nm length from the interface of the source and the N^+ pocket and along the Si–SiO_2 interface [19]. In addition, the reliability of device in terms of ITCs is analyzed by transmuting the equivalent positive (negative) localized charges at the Si–SiO_2 interface. The uniform distribution of ITC density is considered in the TCAD simulations. The parameters such as the trap charge density, polarity, and their position along the channel are defined in INTERFACE statement. In this work, the density of the interface charge density (N_f) is chosen in support with various formerly published experimental and simulation data that includes the process damage, radiation damage, and hot carrier damage, and results in ITC density of 10^{11}–10^{13} cm^{-2} eV^{-1} [18], [20], [21]. The reliability of PNIN-GAA-TFET is analyzed in terms of various electrical, analog, and RF figures of merit. Moreover, while analyzing the influence of ITCs on device characteristics, the temperature is kept

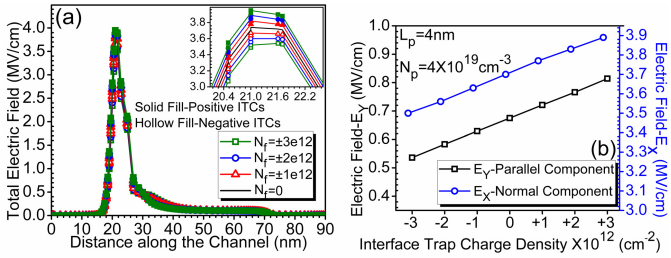

Fig. 2. (a) Electric field profile along the channel of PNIN-GAA-TFET at $N_f = \pm 1, 2, 3\ (\times 12)\ \text{cm}^{-2}$. (b) Peak intensity of parallel and normal components of electric field near tunneling junction of PNIN-GAA-TFET as a function of ITC density.

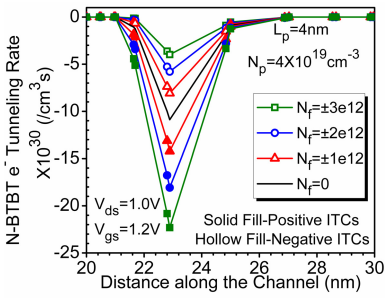

Fig. 3. Nonlocal BTBT of electrons of PNIN-GAA-TFET as a function of channel length at $N_f = \pm 1, 2, 3\ (\times 12)\ \text{cm}^{-2}$.

constant at 300 K, and during investigation of temperature affectability, the trap charge density is kept constant at $N_f = \pm 1 \times 10^{12}\ \text{cm}^{-2}$.

B. Model Validation

Simulation setup has been validated by the experimental data, before simulating the device structure [28]. The non-local BTBT model has been calibrated by tuning the tunneling masses from their default values to fit it with [28]. The adjusted value of me.tunnel $= 0.22\ m_o$ and mh.tunnel $= 0.52\ m_o$ [4], [19], where m_o is the rest mass of electron. The validation of simulation setup with the experimental data for the transfer characteristics is shown in Fig. 1(b). The close proximity of simulation model with the experimental data, thereby, authorizes the model considerations of simulation setup.

III. Results and Discussion

A. Impact of Interface Trap Charges—Density and Polarity

In this section, the influence of ITC density and polarity of PNIN-GAA-TFET is examined at a constant temperature of 300 K. Fig. 2(a) shows the impact of ITC density on the total electric field of PNIN-GAA-TFET. It is clearly evident from the inset (that shows the magnified view of the peak of the electric field at the tunneling junction) that, with an increase of donor (acceptor) trap charge density, the peak of electric field increases (decreases) with respect to the case of undamaged device. This increase (decrease) in an electric field is attributed to the decrease (increase) in the flatband voltage caused by the presence of positive (negative) trap charges, defined as

$$\Delta V_{fb} = \frac{qN_f}{C_{\text{ox}}}$$

where q is the electronic charge, N_f is the ITC density, and C_{ox} is the gate oxide capacitance. The presence of positive (negative) ITCs decreases (increases) the flatband voltage and, thereby, increases (decreases) the effective gate bias ($V_{\text{eff}} = V_{\text{gs}} - V_{\text{fb}}$) at the tunneling junction. The enhanced (reduced) V_{eff} caused by the occurrence of donor (acceptor) trap charges, thereby, enhances (reduces) the electric field at the tunneling junction as evident from Fig. 2(a). Moreover, the considerably high electric field peak at the tunneling junction (caused by the steeper band bending) is a merit for enhancing the tunneling rate of electrons, but it also attributes to the generation of trap centers near the source–channel junction. As reported in [32], the parallel component of the electric field, i.e., E_y contributes to the tunneling rate of electrons and, thereby, affects the drain current of TFET. Higher value E_y is required for enhanced BTBT rate of electrons and, thus, for the higher value of I_{ds}. However, the normal component of the electric field, i.e., E_x is responsible for the reliability concerns, such as the interface trap generation along with the gate leakage current. The lower value of E_x is required for improved device reliability. Thus, the peak of parallel (E_y) and normal (E_x) components of electric field at the tunneling junction as a function of ITC density is analyzed and is shown in Fig. 2(b). At higher donor (acceptor) trap charge density, the peaks of both E_x and E_y are large (small). The higher value of E_y enhances the tunneling rate of electrons; however, the larger value of E_x degrades the device reliability. Fig. 3 shows the impact of ITC density on nonlocal BTBT rate of electrons along the channel length. It is examined that, with an increase in the density of donor (acceptor) ITCs, the BTBT rate of electrons increases (decreases) extensively. This increase (decrease) in the BTBT rate of electrons is attributed to the enhanced (reduced) electric field at the tunneling junction, as shown in Fig. 2(a). Fig. 4(a) shows the impact of ITC density on the transfer characteristics of PNIN-GAA-TFET at $T = 300$ K. The result reveals that the positive (negative) traps enhances (reduces) the drain current. This increase (decrease) in the drain current is the consequence of the enhanced (reduced) effective gate bias caused by the reduced (increased) V_{fb} by the presence of positive (negative) trap charges. The degradation posed by the donor traps is more hazardous for the device operated in subthreshold regime in comparison with the superthreshold regime. Furthermore, it is analyzed that, with an increase in positive trap charge density, I_{OFF} degrades significantly from an order of 10^{-17} A to 10^{-9} A. Therefore, as the fixed charges generated by the various process-, radiation-, and stress-induced damages are always present in a practically fabricated device, it may severely degrade the device characteristics. Fig. 4(b) shows the impact of trap charge density on I_{OFF} and the current switching ratio ($I_{\text{ON}}/I_{\text{OFF}}$ ratio). As clearly shown in Fig. 4(b), the damaged region with donor trap charges of $3 \times 10^{12}\ \text{cm}^{-2}$ degrades I_{OFF} tremendously from an order of 10^{-17} A to 10^{-9} A. However, as shown in Fig. 4(a),

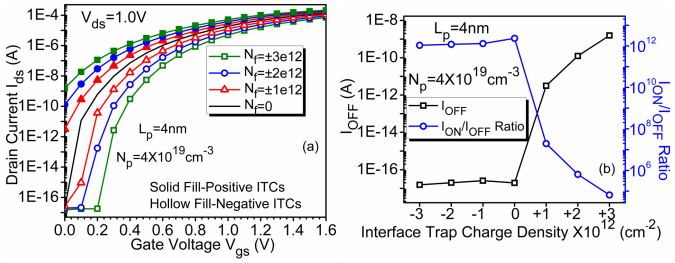

Fig. 4. Impact of ITC density on (a) transfer characteristics (b) I_{off} and switching ratio of PNIN-GAA-TFET at $N_f = \pm 1, 2, 3$ ($\times 12$) cm^{-2}.

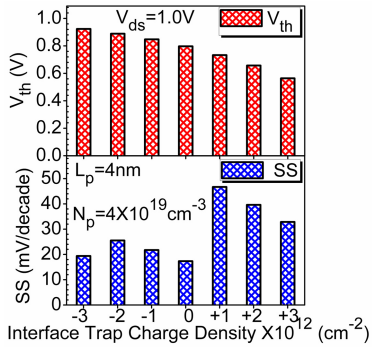

Fig. 5. Impact of ITC density on V_{th} and SS of PNIN-GAA-TFET at $N_f = \pm 1, 2, 3$ ($\times 12$) cm^{-2}.

the presence of ITC alters the superthreshold current marginally and, thus, the switching ratio is mainly affected by I_{OFF}. It is obtained that the switching ratio degrades from an order of 10^{12} (for the undamaged device) to 10^5 (for a damaged device with donor trap charge density of 3×10^{12} cm^{-2}). However, the consequence of immunity against the presence of acceptor trap charges is also observed in unaltered I_{ON}/I_{OFF} for the negative ITC density.

The impact of ITC density on V_{th} and the SS of PNIN-GAA-TFET are presented in Fig. 5. It is obtained that the presence of donor (acceptor) trap charges decreases (increases) V_{th}. The reduced V_{th} for donor trap charges is attributed to the additional band bending caused by the presence of positive trap charges. V_{th} reduces (enhances) by 29.26% (15.90%) at $N_f = \pm 3 \times 10^{12}$ cm^{-2}. The degradation in the SS due to the presence of ITC is elucidated clearly in Fig. 5. This degradation in the SS is due to the tremendously enhanced I_{OFF} for positive ITC. However, the consequence of little variation in I_{OFF} and I_{ON} for acceptor ITCs is shown by the slight change in the SS at negative ITCs.

Moreover, the reliance of operating speed of TFET on parasitic capacitance and the different switching operation of TFET necessitates the investigation of bias-dependent parasitic capacitances. In this work, the intrinsic capacitances are evaluated through the small-signal ac analysis, at a constant dc solution. In this regard, the intrinsic capacitances among each pair of electrodes (i.e., source, gate, and drain) are calculated at a single constant frequency at 1 GHz with a dc voltage ramp of 0–1.6 V. Moreover, for better convergence, DIRECT parameter is incorporated while simulating the device. As reported in [33], in TFETs, the inversion

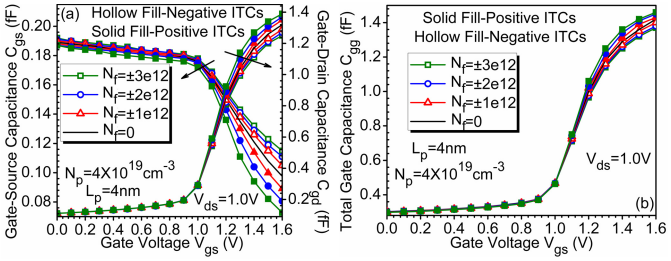

Fig. 6. Influence of ITC density on (a) C_{gs}, C_{gd}, and (b) C_{gg} as a function of gate voltage of PNIN-GAA-TFET.

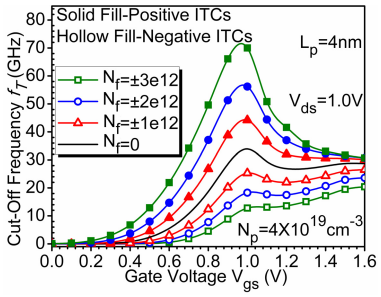

Fig. 7. Effect of ITC density on f_T as a function of V_{gs} of PNIN-GAA-TFET.

layer distribution is distinct from MOSFET. This results in fundamentally different partitions of total gate capacitance C_{gg} in TFET from that of a MOSFET. As shown in [34], for TFET, the drain is connected to the inversion layer and, therefore, C_{gd} contributes majorly to C_{gg}, in contrary to MOSFET, where $C_{gg}/2 \sim C_{gd} \sim C_{gs}$. Fig. 6(a) and (b) shows the impact of ITC density on C_{gs}, C_{gd}, and C_{gg} as a function of V_{gs} at the constant $V_{ds} = 1$ V. At lower value of V_{gs}, the inversion layer is first formed at the drain side, and with an increase in V_{gs}, it extends toward the source side as evident from Fig. 6(a). The reduced coupling between gate and source with an increase in V_{gs} monotonically decreases C_{gs} with increasing V_{gs}. Before the inversion layer formation, C_{gs} comprises the parasitic capacitance; after the inversion layer formation, C_{gd} dominates. In addition, the similar values of C_{gg} and C_{gd} are attributed to the small value of C_{gs} that results in almost the same values of C_{gg} and C_{gd}. It is evaluated that the presence of positive (negative) ITCs increases (decreases) the C_{gd} by 0.1% (0.1%) at $V_{gs} = 0$ V and 8.5% (4.9%) at $V_{gs} = 1.2$ V. The influence of ITC density on C_{gg} as a function of V_{gs} of PNIN-GAA-TFET is shown in Fig. 6(b). The consequence of immunity of C_{gd} against ITC density due to low electric field at the drain channel junction is evident from the unaltered C_{gg} with ITC density. An important RF figure of merit is the cutoff frequency (f_T) defined as the frequency at which the current gain falls to 0 dB. The impact of ITC density on f_T as a function of gate voltage is shown in Fig. 7. It is analyzed that the existence of positive (negative) ITCs increases (decreases) f_T. This increase (decrease) is due to the enhanced (reduced) drain current and, thus, the transconductance that has a direct dependence on f_T. Moreover, it is obtained that the peak of f_T, increases (decreases) more prominently at higher ITC density. It is evaluated that, at $V_{gs} = 1$ V, the presence of donor (acceptor) ITCs of $N_f = \pm 3 \times 12$ cm^{-2} increases

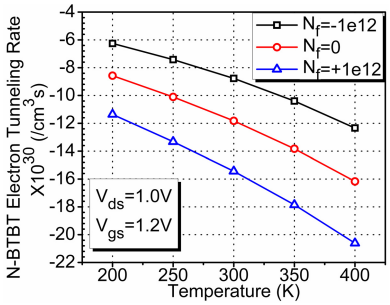

Fig. 8. Variation of nonlocal BTBT rate of electrons at the tunneling junction as a function of temperature of PNIN-GAA-TFET at $N_f = \pm 1 \times 12\ \text{cm}^{-2}$.

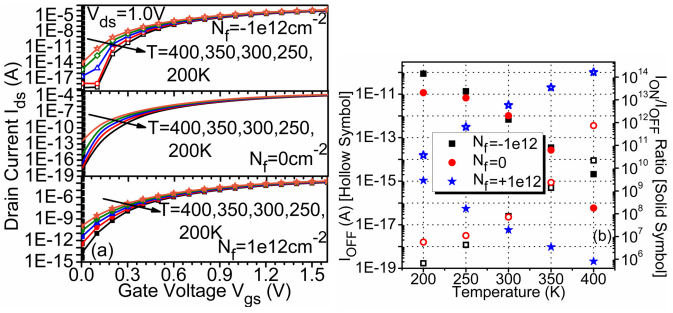

Fig. 9. (a) Drain current (b) I_{off} and current switching ratio as a function of temperature (200–400 K) of PNIN-GAA-TFET at $N_f = \pm 1 \times 12\ \text{cm}^{-2}$.

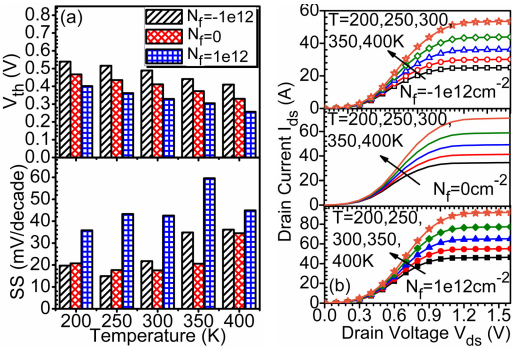

Fig. 10. (a) V_{th} and SS as a function of temperature (b) output characteristics at $V_{gs} = 1.2$ V, for the temperature range of 200–400 K of PNIN-GAA-TFET.

(decreases) f_T by 2.06 (2.65) times, respectively. As f_T of TFET has a direct variation with g_m and inverse variation with the total gate capacitance C_{gg} ($=C_{gs}+C_{gd}$), thus, the demerit of higher C_{gd} in TFET attributes to the lower f_T in comparison with the experimental conventional Si MOSFETs with comparable gate length, as also reported in various published articles [33].

B. Temperature Affectability

In this section, PNIN-GAA-TFET is analyzed at various ambient temperatures at constant ITC density. Fig. 8 presents the variations in the nonlocal BTBT rate at various temperatures, including the effect of ITCs. In the case of TFET, the BTBT rate is reliant on temperature. In addition, the property of semiconductor, such as the energy bandgap, is also dependent on temperature. The reliance of energy bandgap on temperature has been experimentally measured [35], and is defined as

$$E_g(T) = E_g(0) - \frac{\alpha_E T^2}{T + \beta_E}$$

where $E_g(0)$ is the energy bandgap at $T = 0$ K for Si, $E_g(0) = 1.170$ eV, α_E and β_E are the material specific fitting constants for Si, $\alpha_E = 4.37 \times 10^{-4}$ eV/K, $\beta_E = 636$ K, and T is the absolute temperature. With an increase in the temperature, the bandgap of a semiconductor decreases. Thus, the narrower bandgap at elevated temperature lowers the tunneling barrier width and, thereby, enhances the BTBT rate of electrons. It is evaluated that, with an increase in the temperature from 200 K to 400 K, the nonlocal BTBT rate of electrons increases by 97.17% and 81.46% for $N_f = 1 \times 12\ \text{cm}^{-2}$ and $-1 \times 12\ \text{cm}^{-2}$, respectively. The influence of temperature (200–400 K) on the drain current as a function of temperature at $N_f = \pm 1 \times 12\ \text{cm}^{-2}$ and for the undamaged device, i.e., with $N_f = 0$, is shown in Fig. 9(a). It is clearly evident from the results that the temperature affectability on the transfer characteristics is bias-dependent, due to the distinct transport mechanism in OFF and ON states. In the subthreshold region, the drain current increases exponentially with the rise in the temperature. This increase in the drain current is attributed to the dominance of SRH recombination at lower gate bias that has an exponential temperature dependence. However, with an increase in V_{gs}, the BTBT current dominates. The consequence of small temperature dependence of BTBT (that is caused by the bandgap narrowing with temperature) is dictated by the slight enhancement in the drain current at elevated temperature in the superthreshold region, as clearly shown in Fig. 9(a). The impact of temperature on transfer characteristics remains unaltered for donor/acceptor ITCs. The influence of temperature on I_{OFF} and the $I_{\text{ON}}/I_{\text{OFF}}$ ratio at $N_f = \pm 1 \times 12\ \text{cm}^{-2}$ and for the undamaged device, i.e., with $N_f = 0$, is shown in Fig. 9(b). The results reveal that, with an increase in the temperature from 200 K to 400 K, I_{OFF} increases from 10^{-19} A to 10^{-15} A (for $N_f = -1 \times 12\ \text{cm}^{-2}$) and from 10^{-14} A to 10^{-10} A (for $N_f = +1 \times 12\ \text{cm}^{-2}$). However, the current switching ratio degrades from an order of 10^{14}–10^{9} A (for $N_f = -1 \times 12\ \text{cm}^{-2}$) and from 10^{9} A to 10^{5} A (for $N_f = +1 \times 12\ \text{cm}^{-2}$). This degradation in the $I_{\text{ON}}/I_{\text{OFF}}$ ratio is attributed to the enhanced I_{OFF} at elevated temperatures. The influence of temperature and ITC polarity on V_{th} and the SS of PNIN-GAA-TFET is depicted in Fig. 10(a). The significantly high degradation in I_{OFF} at elevated temperatures (instigated by SRH) and an inconsiderable increase in I_{ON} (instigated by BTBT) degrade the SS at elevated temperatures. It has been analyzed that, for an increase in the temperature from 200 K to 400 K, the SS increases by 83.23% and 25.43% for $N_f = -1 \times 12\ \text{cm}^{-2}$ and $N_f = 1 \times 12\ \text{cm}^{-2}$, respectively. The temperature dependence of V_{th} is also shown in Fig.10(a). As discussed before, the drain current increases with an increase in the temperature, i.e., PNIN-GAA-TFET has positive temperature coefficient in both subthreshold and superthreshold regions. This higher drain current at elevated temperature results in reduced V_{th}.

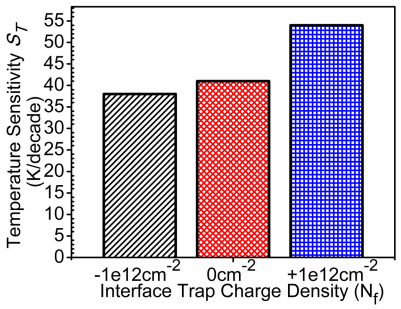

Fig. 11. Influence of ITCs on the temperature sensitivity of the I_{off} variability of PNIN-GAA-TFET at $N_f = \pm 1 \times 12$ cm^{-2} and $N_f = 0$.

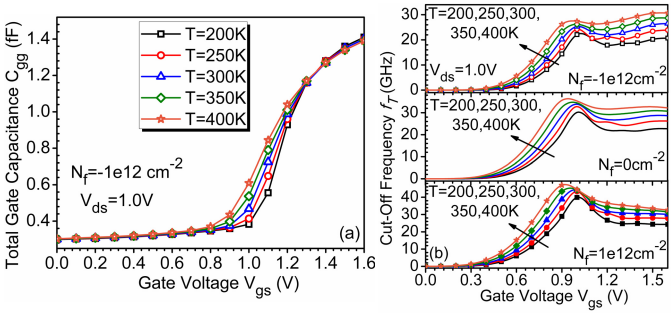

Fig. 12. (a) Variations of C_{gg} as a function of V_{gs} at the temperature range of 200–400 K and (b) f_T as a function of V_{gs} at the temperature range of 200–400 K of PNIN-GAA-TFET at $N_f = \pm 1 \times 12$ cm^{-2}.

In addition, the consequence of bandgap reduction of Si at elevated temperature is the lowered tunneling barrier width at the source–channel junction that, thereby, allows more number of carriers to tunnel through the valence band of the source to the conduction band of the channel. Thus, the band bending at lower gate bias at the tunneling junction for high ambient temperature enhances the tunneling rate at lower gate bias and subsequently decreases V_{th} of the device with an increase in the temperature. The results show that, for an increase in the temperature from 200 K to 400 K, V_{th} decreases by 23.92% and 36.05% for $N_f = -1 \times 12$ cm^{-2} and $N_f = 1 \times 12$ cm^{-2}, respectively. Fig. 10(b) illustrates the output characteristics of PNIN-GAA-TFET for a temperature range of 200–400 K at $N_f = \pm 1 \times 12$ cm^{-2} and for the case when localized charges are absent. In consistent with the above results, the drain current increases with an increase in the temperature. It is analyzed that, at $V_{gs} = 1.2$ V, with a rise in the temperature from 200 K to 400 K, the drain current increases by 2.11 times, 2.03 times, and 1.97 times for $N_f = -1 \times 12$ cm^{-2}, $N_f = 0$, and $N_f = +1 \times 12$ cm^{-2}, respectively.

As the temperature affectability is maximum in the subthreshold region, therefore, a quantitative analysis of the influence of ITCs on the temperature sensitivity (S_T) of the I_{OFF} variability has been done. S_T of PNIN-GAA-TFET as a function of ITCs is shown in Fig. 11, and is evaluated as

$$S_T = \left(\frac{\partial \log\ (I_{OFF})}{\partial T}\right)^{-1} \text{ K/decade.}$$

As shown in Fig. 11, the presence of ITCs modifies S_T of the device. It is assessed that the donor (acceptor) ITCs increase (decrease) S_T of PNIN-GAA-TFET by 31.7% (7.89%) with respect to the ideal device. Moreover, it is analyzed that, for the ideal device, a change in the ambient temperature by 41 K alters I_{OFF} by an order of a decade. However, for the presence of donor (acceptor) ITCs, a change in the temperature by 54 K (38 K) alters I_{OFF} by an order of a decade. Consequently, the presence of donor (acceptor) trap charges enhances (reduces) the temperature sensitivity that must be detrimental for the devices used for sensors applications, in temperature sensitive environment. For the analog and digital applications, the examination of parasitic capacitances is essential. In order to analyze the reliance of temperature on bias-dependent parasitic capacitance, the total gate capacitance as a function of gate bias is examined at various temperatures, and is shown in Fig. 12(a). It is examined that C_{gg} increases with an increase in the gate bias. This increase in C_{gg} with the gate bias is owing to the fact that, at fixed drain bias and at low gate bias, the inversion layer is formed near the drain side. After the inversion layer formation, further increase in the gate bias extends the inversion layer toward the source side. Moreover, it is obtained that, with an increase in the temperature, C_{gg} increases. It is examined that, at $V_{gs} = 1.1$ V, an increase in the temperature from 200 K to 400 K increases C_{gg} by 51.87%. Fig. 12(b) shows the influence of temperature variation on f_T as a function of gate bias. Owing to the consequence of positive temperature coefficient of the drain current, g_m also increases with the temperature and, thus, enhances f_T with the temperature. It is evaluated that, at $V_{gs} = 1$ V for $N_f = -1 \times 12$ cm^{-2} and 1×12 cm^{-2}, an increase in the temperature from 200 K to 400 K increases f_T by 23.97% and 11.76%, respectively.

IV. Conclusion

This work encompasses the reliability of N$^+$ source pocket PIN-GAA-TFET in terms of: 1) impact of ITC density and polarity and 2) temperature affectability over the device characteristics by numerical simulations. It is analyzed that the presence of donor (acceptor) trap charges enhances (reduces) the parallel E_y and normal E_x component of the electric field. The enhanced E_y increases the BTBT rate of electrons. However, the increased E_x contributes to the generation of interface defects and also to the gate leakage current and, thereby, degrades the reliability of the device. Moreover, it is obtained that the presence of donor trap charges tremendously degrades I_{OFF}. In addition, I_{OFF} is immune to the presence of acceptor traps. Furthermore, it is explored that the presence of ITCs alters superthreshold characteristics marginally. The temperature affectability over the device characteristics reveals a more prominent degradation in subthreshold characteristics in comparison with the superthreshold region. In addition, PNIN-GAA-TFET shows a positive temperature coefficient for the complete gate-bias range. Importantly, the temperature sensitivity of the device is also altered by the ITCs that is harmful to the device operating in the temperature sensitive ambience. The results obtained in this analysis could be beneficial while designing TFETs for a temperature sensitive environment.

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Gate Drain Underlapped-PNIN-GAA-TFET for Comprehensively Upgraded Analog/RF Performance

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ABSTRACT

This work integrates the merits of gate-drain underlapping (GDU) and N+ source pocket on cylindrical gate all around tunnel FET (GAA-TFET) to form GDU-PNIN-GAA-TFET. It is analysed that the source pocket located at the source-channel junction narrows the tunneling barrier width at the tunneling junction and thereby enhances the ON-state current of GAA-TFET. Further, it is obtained that the GDU resists the extension of carrier density (built-up under the gated region) towards the drain side (under the underlapped length), thereby suppressing the ambipolar current and reducing the parasitic capacitances of GAA-TFET. Consequently, the amalgamated merits of both engineering schemes are obtained in GDU-PNIN-GAA-TFET that thus conquers the greatest challenges faced by TFET. Thus, GDU-PNIN-GAA-TFET results in an up-gradation in the overall performance of GAA-TFET. Moreover, it is realised that the RF figure of merits FOMs such as cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) are also considerably improved with integration of source pocket on GAA-TFET. Thus, the improved analog and RF performance of GDU-PNIN-GAA-TFET makes it ideal for low power and high-speed applications.

1. Introduction

From the last few decades, CMOS technology is efficiently meeting the growing demand for various viable integrated circuits ICs by providing the low power consumption required for low power battery operated portable devices such as wireless devices, laptops, mobile phones, etc. [1]. However, relentless downscaling of MOSFET (metal oxide semiconductor field effect transistors) to below sub-22 nm technology node has stemmed into serious short channel effects (SCEs) [2]. These SCEs or the non-ideal effects, impede the MOSFET performance and thereby enforces a call for the novel devices that utilizes new device physics other than the thermionic emission of the carrier (as driven by MOSFET). In this regard, tunneling field effect transistor (TFET) that uses the band to band tunneling (BTBT) principle is reported as an energy efficient electronic device for acquiring sub- 60mV/decade subthreshold swing (SS) [3,4]. Along with steep SS, TFET offers lower I_{OFF} (of the order of 10^{-17}–10^{-18} A) owing to the large tunneling barrier width at the source-channel (or the tunneling junction) for lower gate bias, which reduces the tunneling probability of carrier from the valence band of the source to the conduction band of the channel at low gate bias [5,6]. Thus, the lower I_{OFF} and steeper SS offered by TFET provides lower leakage current and lower static power dissipations. Hence, TFET becomes an attractive device for ultra low power applications. However, the exponential dependence of BTBT on the lateral electric field, which is lower in conventional TFET leads to low efficiency of BTBT,

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even at high gate bias. This, lesser BTBT rate of carriers leads to low I_{ON} of TFET; and limits the TFET for high-speed analog applications [7]. To enhance the ON-state current in TFETs many device and material engineering schemes have been reported such as multi-gate architecture TFET (double gate, gate all around architectures) [8], dual material gate [9], heterogate dielectric [10], source N^+ pocket [11,12], narrow band gap materials [13] etc.

In this work, a N^+ source pocket is implanted at the source-channel junction. This N^+ source pocket modulates the energy band profile at the tunneling junction and thereby enhances the lateral electric field [11]. The enhanced lateral electric field reduces the tunneling barrier width at the source-channel junction and thereby increases the tunneling probability of electrons and thus, the I_{ON} of TFET. Moreover, an improved reliability of PNIN-TFET is reported in Ref. [14], in comparison with conventional PIN-TFET. Furthermore, the fabrication process of PNIN architecture is also reported in Ref. [12], in which after defining the gate metal the tilt angled implant is used to form the source N+ pocket.

Another major impedes suffered by TFET is ambipolar conduction i.e. the conduction in both positive and negative gate bias regions [15,16]. The main reason of ambipolar conduction in TFET is tunneling at the drain-channel junction for negative gate bias, caused by the lowering of barrier width at the drain-channel junction at negative gate bias. The ambipolar conduction in TFETs hampers TFET applicability for digital applications. Many device engineering schemes have been reported for lowering the ambipolar current such as gate-drain underlapping (GDU) or shortened metal gate [17], asymmetric source-drain doping [6], hetero gate dielectric [18], heterojunction TFET [19], etc.

In GDU scheme, the underlapped metal gate near drain side resists the extension of carrier density that is built-up under the gated region towards the drain side or beneath the underlapped region. Thus, the underlapped gate metal reduces the ambipolar conduction [20]. In addition to the reduction in ambipolar conduction, the underlapped metal engineering scheme also reduces the gate to drain parasitic capacitance (C_{gd}), which is a major obstacle of TFET for circuit designing. However, the hetero gate dielectric engineering scheme also reduces the ambipolar current, but it has implications on enhanced parasitic capacitance due to the presence of high-k dielectric near source-channel junction [21]. Therefore, in this work, the short metal gate or the GDU engineering scheme is considered for reducing the ambipolar current in TFET. In addition to GDU, asymmetric source-drain doping has also been incorporated to support the reduced ambipolar conduction further. Moreover, a cylindrical GAA architecture is considered to enhance the electrostatic control of gate over the channel region.

This work is organized as follows; Section 2 describes the device structures that are under considerations and their parameters used in the simulations. In Section 3, the simulation models are explained, and the calibration of simulation work with experimental data is also shown that ensures the feasibility of models used in TCAD simulations. Section 4 firstly refers the optimization of GDU engineering scheme in terms of gate-drain underlap length and then it describes the comparative analysis of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in terms of various analog and RF figure of merits. Finally, section 5 concludes the entire work.

2. Device architecture and parameters

ATLAS device simulator has been used to simulate GAA-TFET with GDU and N^+ source pocket. Fig. 1(a) shows the schematic structure of GDU-PNIN-GAA-TFET used for simulation. Moreover, for better understanding, the 2D schematic cross-

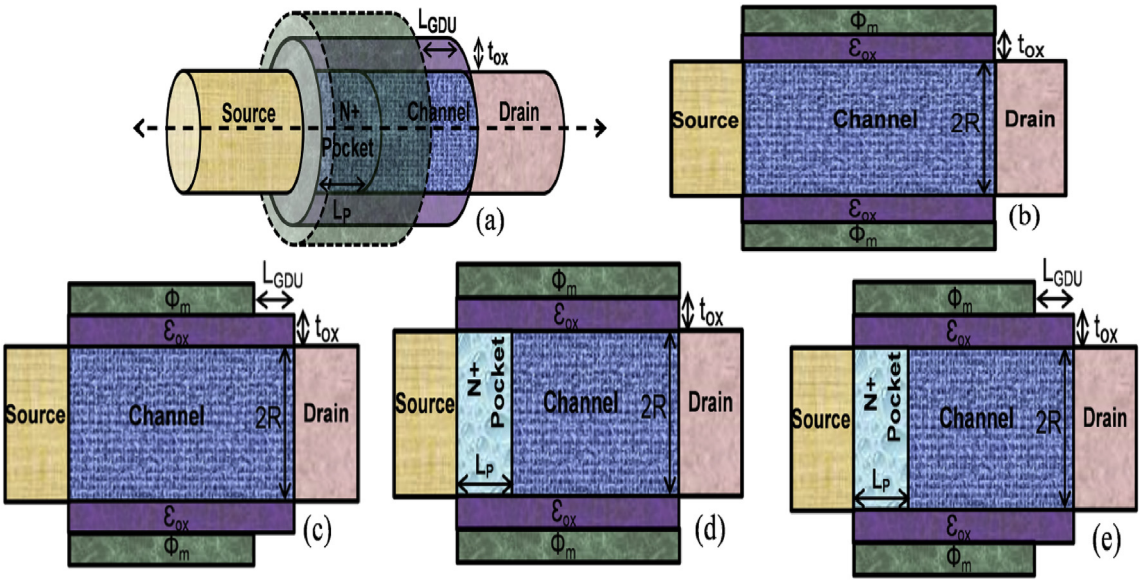


Fig. 1. (a) Simulation structure of GDU-PNIN-GAA-TFET. Schematic 2-D cross-sectional view of (b) GAA-TFET, (c) GDU-GAA-TFET, (c) PNIN-GAA-TFET, and (d) GDU-PNIN-GAA-TFET.

sectional view of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET has also been shown in Fig. 1(b–d). The design variables for acquiring an optimized GDU-PNIN-GAA-TFET are gate-drain underlapping length (L_{GDU}), source pocket doping (N_P) and source pocket width (L_P). For PNIN-GAA-TFET, source pocket is optimized for better I_{ON}/I_{OFF} ratio, V_{th}, and SS by tuning L_p and N_p. It is obtained that at $L_p = 4$ nm and $N_p = 4 \times 10^{19}$ cm^{-3} respectively, the PNIN engineering scheme is optimized in terms of high I_{ON}/I_{OFF} ratio, low-V_{th} and low SS. The GDU engineering scheme is also optimized by altering the L_{GDU} for acquiring an optimum analog performance and parasitic capacitances.

The minimum parasitic capacitances and high I_{ON}/I_{OFF} ratio are obtained at $L_{GDU} = 15$ nm. Therefore, for GDU engineering scheme, L_{GDU} is optimized at 15 nm. Typical default device design parameters used in simulations are listed in Table 1. Silicon is used as source, drain and channel material. To constrain the ambipolarity effect, i.e. tunneling at drain-channel junction source is heavily doped in comparison with drain. The optimum value of gate metal work function of 4.3eV has been chosen for better OFF-state characteristics for all the device architectures under consideration i.e. GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET, and GDU-PNIN-GAA-TFET.

3. Model validation

3.1. Simulation methodology

All simulations have been performed using the ATLAS device simulator [22]. To account the spatial variation dependence of electric field on energy bands, the nonlocal BTBT model is considered, rather the local models that make a triangular approximation and thereby assumes a constant electric field throughout the tunneling barrier regime. Thus, the nonlocal BTBT model takes into account the electrons energy for evaluating electric field at the individual mesh points in the simulated device structure, rather assuming a constant electric field as in local BTBT models such as Kane model [23]. Thus, more realistic results have been obtained by incorporating the nonlocal BTBT model. As tunneling current have strong band gap dependent and the band gap of semiconductor reduces for heavily doped semiconductors thus, the band gap narrowing model is also employed to consider the effects of degenerately doped source/drain. In addition, for accounting the carrier distribution, the Fermi-Dirac statistics is invoked. To describe the carrier's recombination Shockley Read Hall (SRH) recombination model is activated. Along with this, concentration and field dependent mobility model is also employed. The numerical methods used to mathematically solve the carrier transport equation are: Gummel (decoupled) and Newton's (Fully coupled). In this work the parasitic capacitances are extracted through small signal AC analysis (after solving the constant DC bias). The parasitic capacitances between each electrodes are evaluated at constant frequency i.e. 1 MHz.

3.2. Calibration with experimental data

To validate the simulation setup, the simulation models have been calibrated with the experimental results. In this respect, the GAA TFET is designed with the same structural device parameters as in Ref. [24]. To calibrate the Non-local BTBT model, the tunneling masses were adjusted from their default values to make it best fit with the experimental data. The adjusted value of me.tunnel $= 0.22 m_o$ and mh.tunnel $= 0.52\ m_o$. Where; m_o is the rest mass of electron. Fig. 2(a) shows the transfer characteristics of the data obtained by simulation results along with the extracted data from the reference [24]. A close match achieved between the TCAD simulation results, and the experimental characteristics validate the models parameters used in the simulation.

4. Results analysis

4.1. Impact of Gate-Drain Underlapping length: An optimization study

This subsection presents a comparative analysis of transfer characteristics and parasitic capacitances with the aim of attaining an optimized gate metal underlapping length (L_{GDU}) for GDU-GAA-TFET. To investigate an optimized L_{GDU} for the

Table 1
Device default design parameters used in simulations.

Parameters	Value
Drain (N^+) doping N_d	5×10^{18} cm^{-3}
Source (P^+) doping N_s	1×10^{20} cm^{-3}
Channel radius R	10 nm
Source Pocket (N^+) doping N_p	4×10^{19} cm^{-3}
Source Pocket Width L_p	4 nm
Channel Length L_g	50 nm
Gate oxide thickness t_{ox}	2 nm
Gate metal workfunction Φ_M	4.3 eV
Gate dielectric ε_{ox}	3.9 SiO_2
Gate drain underlapping length L_{GDU}	15 nm

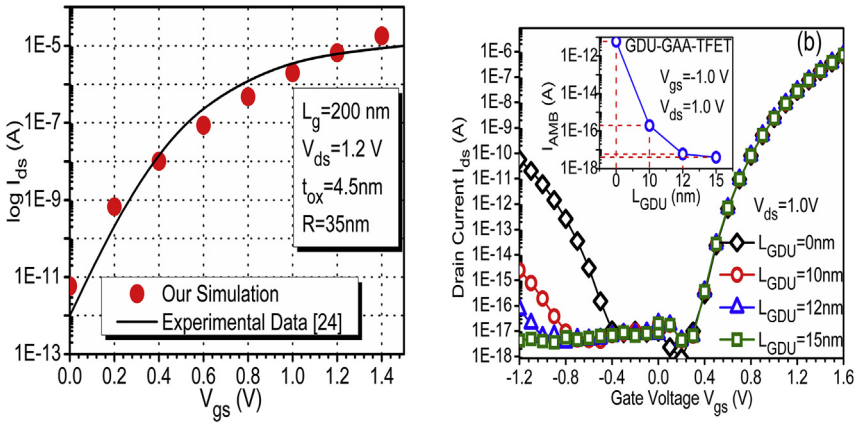


Fig. 2. (a) Calibration with the experimental data, transfer characteristics of the SiNW-TFET with 200-nm gate length at V_{ds} = 1.2 V, t_{ox} = 4.5 nm, and Radius = 35 nm. (b) Transfer characteristics of GDU-GAA-TFET at various L_{GDU}. Inset: I_{AMB} of GDU-GAA-TFET at various L_{GDU}.

GDU-GAA-TFET, the influence of L_{GDU} is studied on the transfer characteristics of GDU-GAA-TFET. From Fig. 2(b), it can be observed that underlapping the gate metal near drain side, affects the device characteristics only for negative gate bias (or the ambipolar current). Considerable suppression in ambipolarity is obtained with a shortened gate metal length. It is obtained that the ambipolar current (I_{AMB}) is reduced from an order of 10^{-12} A (for GAA-TFET) to 10^{-18} A (for GDU-GAA-TFET at L_{GDU} = 15 nm). However, as the tunneling junction is unaffected by the shortened gate metal (being at the drain-channel junction), the tunneling rate of electrons at source-channel junction remains immune against variations in L_{GDU} which is evident from the unaltered transfer characteristics for positive V_{gs} as shown in Fig. 2(b). Moreover, it is clearly evident that at L_{GDU} = 15 nm, I_{AMB} is significantly reduced, to an order of 10^{-18} A, that adequately overcome the challenges faced by TFET for digital applications. Thus, L_{GDU} = 15 nm is optimum from the perspective of I_{AMB} at the default design parameters mentioned in Table 1 for GDU-GAA-TFET.

Furthermore, it is requisite to study the intrinsic parasitic capacitances due to the fact that the important device design parameters such as the response time and the active power dissipation rely on these parasitic capacitances. Three main parasitic capacitances affect the device performance i.e. total gate capacitance (C_{gg}), gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}). The C_{gs} and C_{gg} of GDU-GAA-TFET at various L_{GDU} are examined as a function of both V_{gs} (at constant V_{ds} = 1.0 V) and V_{ds} (at constant V_{gs} = 1.2 V) and are shown in Fig. 3(a–b). It should be noted that L_{GDU} = 0 nm is the case of GAA-TFET. In Fig. 3(a) the solid fill notations used for C_{gg}, specifies a significant reduced in C_{gg} for GDU-GAA-TFET in comparison to GAA-TFET. The C_{gg} reduces by 38% for an increase in L_{GDU} from 0 nm (GAA-TFET) to 15 nm (GDU-GAA-TFET). However, the tunneling junction is immune to the underlapped length (being at the drain-channel junction), thereby the C_{gs} is almost unaltered for any variations in L_{GDU}. Also, the variations of these intrinsic capacitances are also analyzed as a function of V_{ds} at a constant V_{gs} as shown in Fig. 3(b). The C_{gg} of GDU-GAA-TFET at various L_{GDU} indicates a significant reduction in C_{gg} for shortened gate metal lengths, in comparison to GAA-TFET. Moreover, as the transfer characteristics for positive gate bias is immune towards variations in L_{GDU}, the V_{th}, SS, I_{ON}, I_{ON}/I_{OFF} ratio, g_m and other analog and electrical

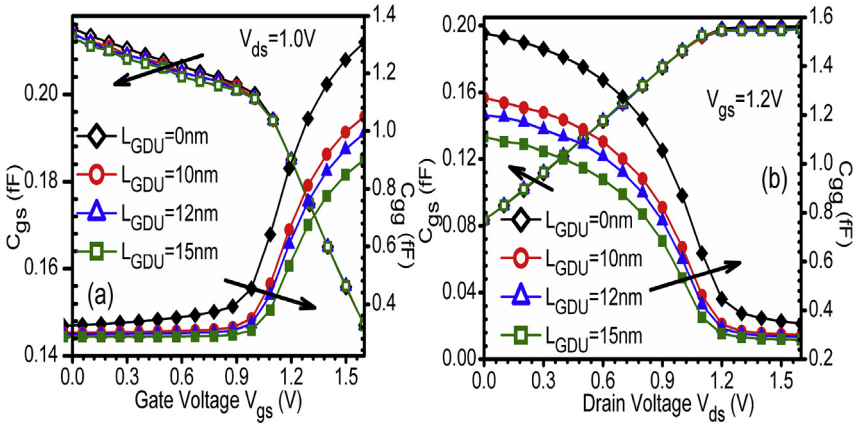


Fig. 3. C_{gs} and C_{gg} of GDU-GAA-TFET as a function of (a) V_{gs} at V_{ds} = 1.0 V (b) V_{ds} at V_{gs} = 1.2 V at various L_{GDU}. L_{GDU} = 0 nm signifies GAA-TFET.

parameters will also remain inviolate for variations in L_{GDU}. Thus, it is assessed that for $L_{GDU} = 15$ nm, GDU-GAA-TFET shows an optimum device performance in terms of I_{AMB} and parasitic capacitances.

4.2. Impact of Gate-Drain Underlapping and source pocket

This subsection presents the comparative analysis of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET, and GDU-PNIN-GAA-TFET, in terms of various analog and RF figure of merits such as: energy band diagrams (in ON-state and ambipolar-state), nonlocal BTBT rate of electrons, electric field, transfer characteristics, switching ratio, threshold voltage, subthreshold swing, parasitic capacitances, cutoff frequency (f_T) and maximum oscillations frequency (f_{MAX}). The default parameters for GDU architecture is $L_{GDU} = 15$ nm and for PNIN architecture is $N_p = 4 \times 10^{19}cm^{-3}$, $L_p = 4$ nm.

For analyzing the tunneling phenomenon, the energy band profiles of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in the ON-state ($V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V) as well as for the ambipolar-state ($V_{gs} = -1.0$ V and $V_{ds} = 1.0$ V) are studied as shown in Fig. 4(a–b). It is clearly evident from Fig. 4(a) that the electron energy band profile is almost same for the GAA-TFET and GDU-GAA-TFET owing to the fact that GDU plays role for the negative gate bias to control the ambipolar current. However, the integration of source pocket at the tunneling junction or, for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET, the bands at the tunneling junction bends steeply. This steeper band bending is due to the presence of N^+ source pocket, that lowers the barrier width and thereby enhances the probability of tunneling of electrons from valence band of source to conduction band of channel.

The energy band profile of all the aforementioned devices analyzed at the ambipolar state, is shown in Fig. 4(b). The broadened tunneling width at the drain-channel junction due to the underlapped metal gate that resists the tunneling of electrons at the drain-channel junction. This lowered tunneling due to the GDU thereby reduces the I_{AMB}, and makes the TFET eligible for digital switching applications.

Fig. 5 shows the comparison of the nonlocal-BTBT (N-BTBT) rate of electrons and electric field at the tunneling junction for different GAA-TFET configurations. In conventional GAA-TFET and GDU-GAA-TFET, the broader tunneling width contributes to the tremendously lower nonlocal BTBT rate of electrons. However, the steeper band bending attained by the N^+ source pocket considerably reduces the barrier width at the source-channel junction and thus enhances the N-BTBT rate of electrons as clearly shown in Fig. 5. The consequence of steeper band bending (obtained via N+ source pocket) is increased electric field for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET. Quantitatively, the electric field is increased by 2.2 times with the application of N+ source pocket onto GAA-TFET.

The transfer characteristics of all the devices i.e. GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET, and GDU-PNIN-GAA-TFET are shown in Fig. 6(a). It is evident that GAA-TFET suffers from lower I_{ON} and higher I_{AMB}. With the integration of GDU architecture on GAA-TFET, a significant reduction in I_{AMB} (from an order of 10^{-18}A to 10^{-12} A) is obtained. This decrease in I_{AMB} is due to the underlapping of gate metal near the drain-channel junction that resists the extension of carrier density towards the drain side and thus, repels the lowering of barrier width at the drain-channel junction (for negative V_{gs}) and thereby reduces the I_{AMB}. This reduced I_{AMB} thus overcomes the major challenges faced by TFET and makes it suitable for digital applications.

Furthermore, the amalgamation of N^+ pocket at the tunneling junction, enhances band bending at the source-channel junction [see Fig. 4(a)]. This steeper band bending thus increases the tunneling rate of electrons. Which thereby conquers the obstacle of lower I_{ON} of TFET, and hence I_{ON} increases from an order of 10^{-8} A (for GAA-TFET) to 10^{-4} A (for PNIN-GAA-TFET). Consequently, the integration of both the scheme i.e. GDU-PNIN-GAA-TFET improves both the hitches (i.e. lower I_{ON} and higher I_{AMB}) by enhancing the I_{ON} and reducing the I_{AMB} as evident by Fig. 6(a). The threshold voltage (V_{th}) and subthreshold swing (SS) of all the device architectures under considerations are shown in Fig. 6(b). The larger band bending at the

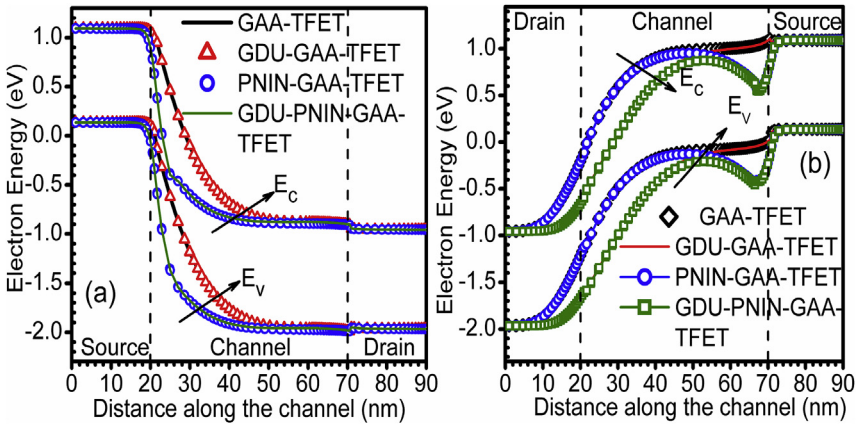


Fig. 4. Energy band diagram of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET (a) in ON-state at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V (b) in ambipolar state at $V_{gs} = -1.0$ V and $V_{ds} = 1.0$ V as a function of channel length. For GDU architecture $L_{GDU} = 15$ nm.

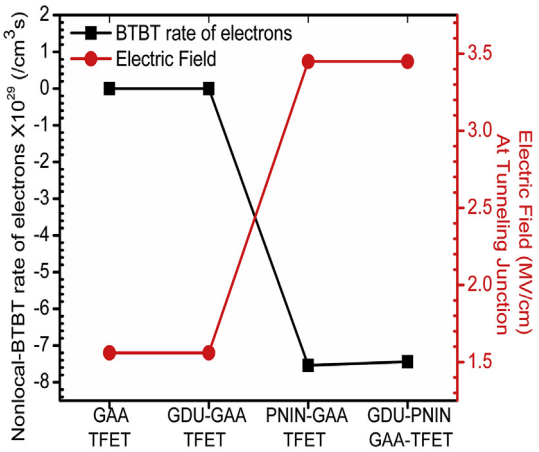
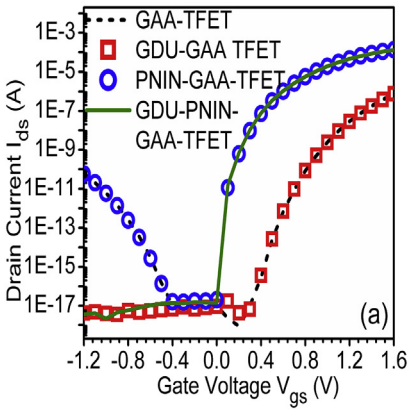


Fig. 5. Nonlocal BTBT rate and electric field at the tunneling junction of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V.



Device architecture	SS (mV/decade)	V_{th} (@I_{ds}= 10^{-7} A) (V)
GAA-TFET	52.22	1.32
GDU-GAA-TFET	53.37	1.32
PNIN-GAA-TFET	17.41	0.41
GDU-PNIN-GAA-TFET	16.59	0.40

(b)

Fig. 6. (a) Transfer characteristics, (b) threshold voltage (V_{th}) and subthreshold swing (SS) of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET at $V_{ds} = 1.0$ V.

tunneling junction for the PNIN-GAA-TFET switches ON TFET at the lower V_{gs}. Thus, there is a considerable reduction in the V_{th} for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in comparison with its conventional counterparts. Further, the integration of N^+ pocket in GAA-TFET enhances the I_{ON} without any degradation in the I_{OFF}, thereby reduces the SS of GAA-TFET by 3.14 times for PNIN-GAA-TFET.

The ambipolar current of TFETs is a major hindrance in the device designing for low power analog and digital applications. In this work, I_{AMB} is defined as the drain current at $V_{gs} = -1.0$ V and $V_{ds} = 1.0$ V and are plotted for all the aforementioned device architectures in Fig. 7(a). It is clearly evident from 8(a) that the GDU architecture suppresses the ambipolar current significantly. This suppressed I_{AMB} is attributed to the fact of reduced accumulations of electrons under the underlapped region. This reduction in accumulation in electrons broadens the barrier width between the channel and drain region and thereby reduces the tunneling probability of electrons at the drain-channel junction. Thus, the reduction in tunneling of electrons suppresses the I_{AMB}, from 10^{-12} A (for GAA-TFET and PNIN-GAA-TFET) to 10^{-18}A (for GDU-GAA-TFET and GDU-PNIN-GAA-TFET) as shown in Fig. 7(a). The switching (I_{ON}/I_{OFF}) ratio is an important parameter for digital circuit designing. In this work the I_{ON} and I_{OFF} are defined as the I_{ds} at $V_{gs} = 1.2$ V and 0 V respectively, at constant $V_{ds} = 1.0$ V. The presence of N^+ pocket enhances I_{ON} of the TFET significantly (without any degradation in the I_{OFF}) [see Fig. 6(a)], thus results in a considerable enhancement in the switching ratio of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET to an order of 10^{12}. The enhanced I_{ON}/I_{OFF} ratio acquired by the source pocket at the tunneling junction thereby makes source pocket-PIN-GAA-TFET, a potential candidate for high switching speed applications.

Desiging the FETs for analog applications the crucial design parameters are the device efficiency (or the transconductance generation factor) and the output resistance (or the drain resistance). The device efficiency is evaluated as the ratio of transconductance to drive current i.e. g_m/I_{ds} at a constant drain voltage. g_m/I_{ds} is a measure of available gain per unit power dissipation. Further, a higher value of device efficiency is desirable for better analag performance. Fig. 8(a) shows the

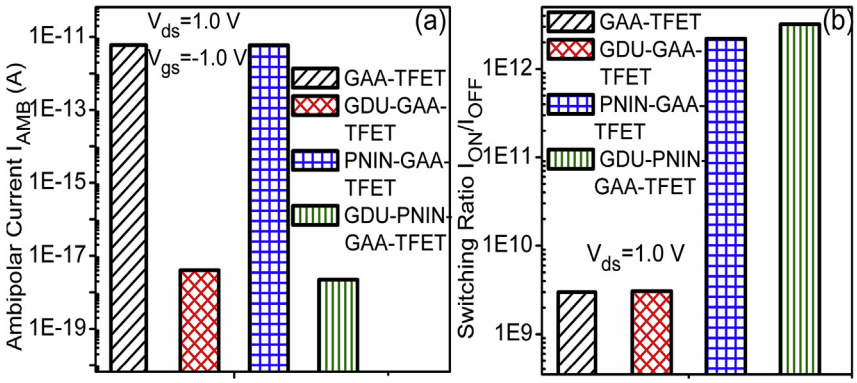


Fig. 7. (a) Ambipolar current (I_{AMB}) at $V_{gs} = -1.0$ V and $V_{ds} = 1.0$ V, (b) Switching ratio (I_{ON}/I_{OFF}) at $V_{ds} = 1.0$ V of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET.

improved device efficiency of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in comparsion with GAA-TFET and GDU-GAA-TFET. This improvement is attributed to the presence of N^+ source pocket in PNIN architecture that enhances the tunneling rate and thus increases the drain current and the transconductance significantly. The enhanced device efficiency acquired for the PNIN-GAA-TFET and GDU-PNIN-GAA-TFET, reveals that the incorporation of N^+ source pocket enhances the amplification delivered by the device. Fig. 8(b) illustrates the output resistance (R_{out}) of all the devices under consideration. It is clearly evident that the R_{out} of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET are appreciably improved in comparsion with GAA-TFET and GDU-GAA-TFET. This improvement in R_{out} for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET is due to the enhanced drain current that increases the output conductance. Thereby the consequence of inverse relation of output conductance and R_{out} reduces the R_{out} from an order of $10^8\Omega$ (for GAA-TFET and GDU-GAA-TFET) to $10^5\Omega$ (for PNIN-GAA-TFET and GDU-PNIN-GDU-GAA-TFET). This improved device efficiency and R_{out} makes GDU-PNIN-GAA-TFET suitable for low power analog applications.

Merely increasing the I_{ON}, reducing the V_{th} and lowered SS does not sufficiently result in a superior TFET based circuit performance. However, the power dissipations and the propagation delay are the key performance metrics for designing digital circuits. The prime important device parameters that affects these performance metrics are the intrinsic parasitic capacitances. Thus, it is necessary to analyze the impact of integration of the aforementioned device engineering schemes on the bias dependence inherent parasitic capacitances. As reported in Refs. [25,26] that for TFET the inversion charge distribution and thus the partition of C_{gg} is entirely different from that of MOSFET. This results in unequal contribution of C_{gs} and C_{gd} to C_{gg}, in contrary to MOSFET in which $C_{gg}/2 \sim C_{gd} \sim C_{gs}$. For TFETs, the source-channel junction being reverse biased, effectively decouples the channel charge from the source. However, the degenerated (N^+) drain floods the channel region with electrons. Therefore, the channel charge is majorly coupled with the drain, and thus C_{gd} represents a major fraction of C_{gg}.

Fig. 9(a–d) shows the C_{gs} and C_{gg} as a function of V_{gs} and V_{ds}. Fig. 9(a–b) clearly illustrates that C_{gs} is lesser than C_{gg}, attributed to the larger C_{gd}. Fig. 9(a) shows that C_{gs} is immune to the integration of GDU engineering scheme because the metal is underlapped near the drain side. Moreover, it is analyzed that for shorter metal gate, the parasitic C_{gg} is considerably reduced, due to the reduction in C_{gd} for underlapped metal gate. Thus, C_{gg} is appreciably reduced for GDU-GAA-TFET and GDU-PNIN-GAA-TFET, in comparison with GAA-TFET. Quantitatively, C_{gg} is reduced by 29% with the integration of GDU engineering scheme onto GAA-TFET as shown in Fig. 9(b). In addition to this, at lower gate bias, the inversion layer is first formed near the drain side, and then with an increase in gate bias, the inversion layer extends towards the source side. Thus, C_{gg} increases with an increase in gate bias. Fig. 9(c–d) shows C_{gs} and C_{gg} for all the device design architectures as a function of V_{ds} at a constant V_{gs}. At $V_{gs} = 1.2$ V (TFET is in ON-state), an increase in V_{ds} pinches the inversion layer at the source side (in contrast to MOSFET, where pinch off occurs near drain side). Thereby, C_{gg} decreases with an increase in V_{ds}. Consistent with the above explanations for shortened metal gate, the C_{gs} remains unaltered with the incorporation of GDU architectures. However, the reduction in C_{gd} with GDU engineering scheme results into lowering of C_{gg} for GDU-GAA-TFET and PNIN-GDU-GAA-TFET in comparison with GAA-TFET and PNIN-GAA-TFET. Thus, as lower parasitic capacitances are needed for higher switching speed and lower static power dissipation, GDU-PNIN-GAA-TFET may act as a superior candidate to meet these requirements.

An important RF figure of merit for a tunnel FET is the unity current gain or the intrinsic f_T. It is defined as the frequency at which the short circuit current gain falls to 0 dB. Mathematically, the intrinsic f_T is defined as

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{1}$$

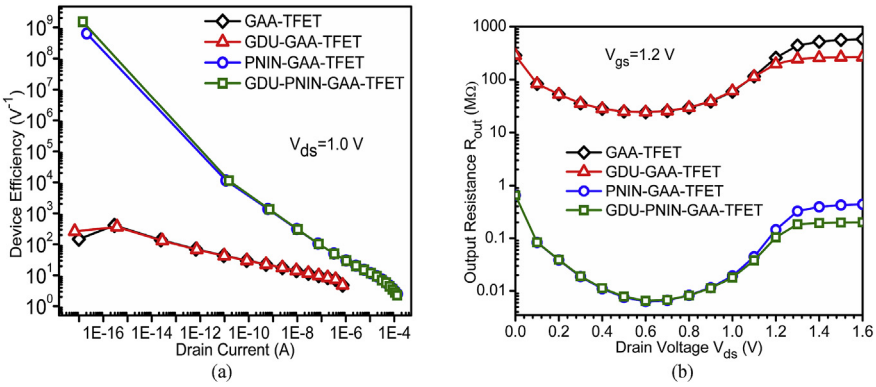


Fig. 8. (a) Device efficiency at V_{ds} = 1.0 V, (b) Output resistance (R_{out}) at V_{gs} = 1.2 V of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET.

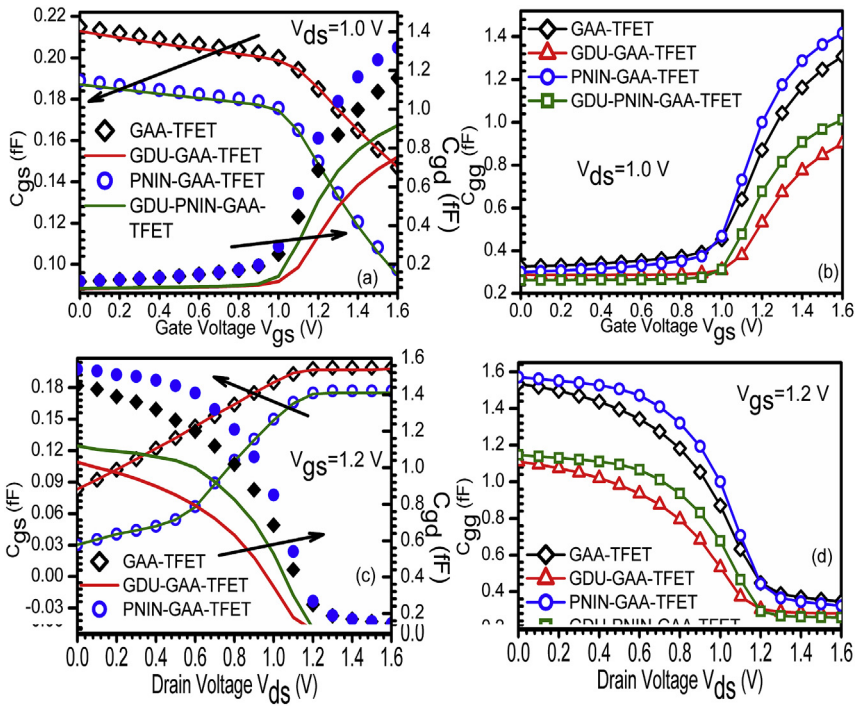


Fig. 9. (a) C_{gs} w.r.t. V_{gs} at V_{ds} = 1.0 V (b) C_{gg} w.r.t. V_{gs} at V_{ds} = 1.0 V (c) C_{gs} w.r.t. V_{ds} at V_{gs} = 1.2 V (d) C_{gg} w.r.t. V_{ds} at V_{gs} = 1.2 V of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET.

Where g_m is the transconductance, C_{gs} and C_{gd} are gate to source and gate to drain intrinsic parasitic capacitances. The vital RF parameters needed for designing analog/RF electronic circuits are shown in Fig. 10(a–b). The variations of f_T as a function of gate bias for all the device designs under considerations are shown in Fig. 10(a). Result shows that as the V_{gs} increases, f_T of all the devices increases until it attains a peak value. The increase in f_T with V_{gs} is attributed to the narrower tunneling barrier width that increases the rate of carrier injection at the tunneling junction and thus, increases the drain current and the transconductance (first order derivative of drain current). f_T being directly proportional to the g_m, increases with V_{gs}, before attaining a peak value. It is observed that the enhanced drain current with source pocket incorporation enhances the transconductance and thereby enhances f_T (being directly proportional to g_m) for PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in comparison with GAA-TFET and GDU-GAA-TFET. f_T is enhanced from an order of 10^8 Hz–10^{10} Hz with the integration of N^+ source pocket. The f_T and f_{MAX} of all the devices are also shown in Fig. 10(b). The frequencies at which the short circuit current gain and unilateral power gain drops to 0 dB are defined as the f_T and the f_{MAX} respectively. The f_T and f_{MAX} are tremendously enhanced for the cases of PNIN-GAA-TFET and GDU-PNIN-GAA-TFET in comparison with GAA-TFET and GDU-GAA-TFET, owing to the enhanced drain current and transconductance that enhance the current gain and the unilateral power gain and therefore results into a larger f_T and f_{MAX} as illustrated in Fig. 10(b). Thus, results indicate that with the integration of N^+

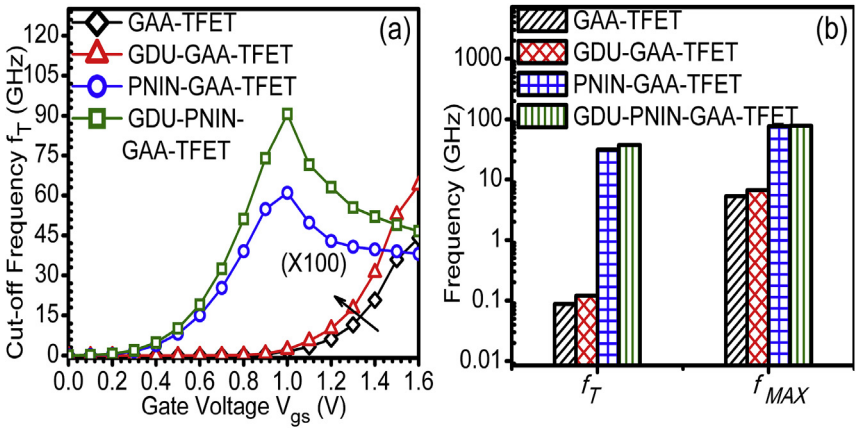


Fig. 10. (a) f_T as a function of gate bias, at constant $V_{ds} = 1.0$ V (b) f_T and f_{MAX} at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V of GAA-TFET, GDU-GAA-TFET, PNIN-GAA-TFET and GDU-PNIN-GAA-TFET.

source pocket engineering, analog as well as the high-frequency performance of TFET are improved appreciably, making it a superior candidate for high switching speed electronics application.

5. Conclusion

In this work, gate drain underlapped N^+ source pocket gate all around tunnel FET (GDU-PNIN-GAA-TFET) is realized. In GDU-PNIN-GAA-TFET, the source pocket pedals the source-channel junction and thereby improves the ON-state characteristics of TFET along with a reduced threshold voltage; however, the GDU governs the drain-channel junction and thus controls the ambipolar conduction of the device. Results show a tremendously improved ON-state characteristics i.e. the I_{ON} to an order of 10^{-4} A together with suppressed ambipolar current to 10^{-18}A with the amalgamation of source pocket and GDU engineering schemes respectively onto GAA-TFET. Hence, the challenges faced by TFET that restricts it for the practical applications have been overcome. Further, the reduction in parasitic capacitances offered by GDU and enhanced transconductance acquired by N^+ pocket leads to a superior RF performance. The detailed insight demonstration in terms of analog/RF performance for GDU-PNIN-GAA-TFET may be beneficial for analog/RF circuit designers and it may also serves as a superior candidate for high speed and low power applications.

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Temperature Associated Reliability Issues of Heterogeneous Gate Dielectric - Gate All Around - Tunnel FET

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***Abstract*—In this work, the temperature associated reliability issues of heterogeneous gate dielectric-gate all around-tunnel FET (HD GAA TFET) has been addressed, and the results are simultaneously compared with gate all around tunnel FET (GAA TFET). This is done by investigating the effect of interface trap charges such as donor (positive interface charges) and acceptor (negative interface charges) at various operating temperatures on the device analog parameters and RF figure of merits. It is observed that, at high gate bias, TFET exhibits weak temperature dependence owing to the weak dependence of band to band tunneling phenomenon on the temperature in comparison to the large temperature variation for lower gate bias due to the temperature dependence of Shockley-Read-Hall (SRH) phenomenon. Results reveal that extremely high OFF current at elevated temperatures degarades the device performance, making the device less reliable for high temperature applications. Moreover, at elevated temperature, the decrease in threshold voltage and intrnsic delay, and increase in cut off frequency is found, thereby upgrading the device characteristics. All the simulations have been done on ATLAS device simulator.**

***Index Terms*—Ambipolarity, Digital applications, Gate all around, Hetero gate dielectric (HD), Interface trap charges (ITC), Temperature Sensitivity, Tunnel FET (TFET).**

I. Introduction

Unique properties of tunnel FET (TFET) such as low I_{off}, sub-60mV/decade subthreshold swing (SS), immunity against short channel effects and its compatibility with the CMOS process makes it a suitable candidate for ultra low power applications [1, 2]. However, the ON-state current in TFET is limited due to the band to band tunneling (BTBT) phenomenon, making it incompatible to meet the increased demand for high speed with low power consumption applications. Many remedies have been proposed to improve the driving current of TFET [3-7]. Another shortcoming of TFET is the ambipolar conduction [8]; this can cause severe problems such as malfunction of the inverter-based logic circuits. To overcome these challenges collectively, a Hetero Gate dielectric TFET (HD TFET) was proposed [4], which combines the merits of TFET with high-k material as dielectric (at higher gate bias) and TFET with SiO_2 as dielectric (at lower gate bias). In HD TFET, the local minima formed at the tunneling junction enhance the ON current of TFET whereas; the SiO_2 placed over the drain-channel junction mitigate the ambipolar behavior of TFET.

Till now, mainly the device performance has been studied for various novel device architectures and material engineering of TFET to improve the device performance, but to consider the device reliability and applicability for wide range temperature applications, the temperature affectability as well as interface trap charges (ITC) must be analyzed. Moreover, it has been reported that the reliability of TFET is more prominent problem due to the change in tunneling field induced by ITCs, in comparison with MOSFET [9].

In case of tunnel FET, higher electric field near the tunneling junction (the source-channel junction) is desired for lowering of the tunneling barrier width, but on the contrary, this high transverse field results into the generation of interface traps (donor and acceptor) and hence the localized charges (both positive and negative). These trap charges can cause severe issues on device reliability and lifetime of the device [10]. As reported previously, the amalgamation of HD scheme on TFET significantly improves the analog [2] and RF performance [11] of the device. However, the on-chip performance of the device is always subject to the operating temperature. The increased number of transistors on the chip enhances the heat dissipation and thus raises the operating temperature of the chip and the device significantly. Also, as the properties of the semiconductor are also dependent on temperature, thus, there is a need to study the effect of temperature in order to investigate the stability of the device [12, 13]. Moreover, from the perspective of application of transistors in some extreme conditions (where the operating temperature is different from the nominal room temperature) such as the furnace temperature control, satellite communications, military, medical equipment, aerospace, automobile, nuclear sectors, wireless/mobile communications, it is important to investigate the device behaviour at a wide range of temperatures.

The core aim of this script is to fulfill the above desires, i.e. the need to investigate the reliability concern of TFET subjective to the impact of operating temperature and effect of the ITCs (owing to the fact of fabrication process damages).

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This is done by studying the impact of ITCs and temperature on the analog and RF performance of GAA TFET and HD GAA TFET.

The organization of the paper is such that section II presents the device structure and the simulation methodology. Then in section III various analog performances such as the transfer characteristics, switching ratio, ambipolar current, threshold voltage, SS and RF figure of merits such as cut-off frequency, intrinsic delay, parasitic capacitances has been presented. Finally, summarization of the work is done in section IV.

II. Device Analysis and Simulation

Fig. 1(a) shows the simulated 2D structure of cylindrical HD GAA TFET. For GAA TFET, the region 1 and region 2 are combined such that the entire gate oxide is of SiO_2. Whereas, for HD GAA TFET, region-1 consists of dielectric constant ε_1=21 (HfO_2) and region-2 consists of ε_2=3.9 (SiO_2). The radius (R) and gate oxide thickness (t_{ox}) is 10nm and 3nm respectively for both HD GAA TFET and GAA TFET. The gate length L_g of HD GAA TFET (L_1=10 nm, L_2=40 nm) and GAA TFET is 50nm. The source is p+ type doped ($1\times10^{20}cm^{-3}$), body is lightly p-type doped ($1\times10^{16}cm^{-3}$), and drain is n+ doped (5×10^{18} cm^{-3}) in both the aforesaid devices. The optimum value of gate metal work function Φ_M=4.3eV has been chosen for better OFF-state characteristics, for both the devices. To suppress the ambipolarity effect, source and drain are asymmetrically doped [14].

Simulation Methodology

All simulations have been performed using the ATLAS device simulator [15]. The models used during simulation are Shockley-Read-Hall (SRH) for carrier recombination, concentration and field dependent mobility model, non-local BTBT, band gap narrowing (BGN) and Fermi-Dirac statistics. Moreover, the carrier transport model used in this work is drift-diffusion, which solves the Poisson and carrier continuity equations self-consistently. The non-local BTBT model is invoked in this work, in contrast to the local tunneling models such as Kane model. The non-local BTBT model considers that the electric field changes dynamically at each point in the tunneling path and thus depends upon the band edge profile in the tunneling path. Whereas, the local tunneling models assume the triangular barrier approximation in the energy barrier, and thus undertakes the constant electric field at each point in the tunneling path [16]. The Fermi-Dirac statistics is used to take into account the effect of heavily doped materials (source and drain in this work), such as reduced carrier concentrations in heavily doped regions (statistical approach). Moreover, the experimental work has shown that the p-n product in silicon becomes doping dependent for higher doping (> $10^{18}cm^{-3}$), generally decrease in bandgap is found at higher doping levels [17]. To incorporate such effects, the BGN model is invoked in the simulation. Numerical methods, Gummel (decoupled) and Newton's (Fully coupled) have been incorporated to solve the carrier transport equation.

In this work, the ITCs are considered at the Si-SiO_2 interface, just near the source side for 10nm, which is mainly

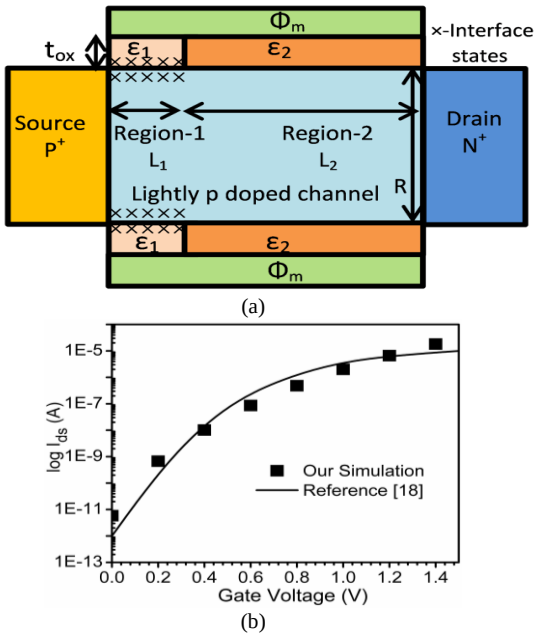

Fig. 1. (a) Schematic cross sectional view of cylindrical n-type Heterogeneous gate Dielectric-Gate All Around-Tunnel FET (HD GAA TFET) used for simulation. (b) Calibration with the published result [18], I_{ds}–V_{gs} characteristics of the 200-nm gate length SiNW-TFET at V_{ds} = 1.2 V, t_{ox} = 4.5 nm, and Diameter = 70nm.

attributed to the presence of high transverse electric field at the tunneling junction. In addition to the high electric field, there are various other factors that induce the generation of interface traps. The most vital factors are:- the fabrication processes damages [19], radiation induced damages [20], stress induced damages (includes the electrical and processing damages) [21] etc. These damages results in trapping of charges in the gate-oxide as well as at the interface of the Si-SiO_2 interface. If the trap level is located below the Fermi level, then the damaged region will accept an electron and acts as a negative fixed/localized charge. However, if the trap level is located above the Fermi level, then the damaged region will donate the electron and acts as a positive fixed/localized charge. Thus, these traps act as a localised/fixed trap charges. Therefore, the interface traps can be transformed, into its equivalent localized charges; (positive/negative localized charge for acceptor/donor traps) [22]. Moreover, on the basis of various experimental data, the ITC density of positive and negative charge is taken as $N_f = \pm1\times10^{12}$ cm^{-2} [23]. To define the density of interface fixed charges and their position present at the interface of Si-SiO_2 INTERFACE statement is used during simulation [15]. Further, the distribution of interface charges is assumed to be uniform during the entire simulation. For considering the temperature effect on the device performance, the temperature is altered from 200 K to 500 K.

Calibration

Before simulating the device structure, a well calibrated TCAD setup has been used to calibrate the simulation models with the already published results [18]. For calibrating the Non-local BTBT model, the tunneling masses were adjusted from their default values i.e. me.tunnel=0.322m_o and mh.tunnel=0.549m_o to make it finest fit with the experimental

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data [18]. Where, m_o is the rest mass of the electron. The adjusted value of me.tunnel=0.22m_o and mh.tunnel=0.52 m_o. Fig. 1(b) show the transfer characteristics of extracted data from the reference and results obtained from the simulations. The results so obtained are in close proximity, thus authorizing the model parameters during the simulations.

Fabrication Feasibility of HD GAA TFET

The fabrication feasibility of HD GAA TFET is shown in the Table 1. Moreover, the GAA TFET has already been fabricated by different researchers such as Chen et al, [18] fabricated vertical silicon nanowire TFET, Gandhi et al, [24, 25] fabricated both vertical Si-nanowire n-type and p-type TFET. Thus, the HD GAA TFET can be fabricated using the above device design schemes, in which the benefits of HD engineering scheme have been combined with GAA TFET for accomplishing improved characteristics.

Table I.
Summary of Process Flow for HD GAA TFET Implementaion [18, 26, 27]

- **Starting material- SiNW Synthesized by** [26]
- **Axially doping of SiNW** [26]
- **Thermal oxidation of SiNW** [26]
- **Formation of HD layer** [27]
- **Define and metalizing Source and drain contacts** [18]
- **To define metal gate** [18]

Continue processing

III. Results And Discussion

Fig. 2 shows the impact of temperature and ITCs on the BTBT rate of electrons at the tunneling junction of both GAA TFET and HD GAA TFET. At higher temperatures the BTBT rate of electrons increases, the increase is 7.38 times and 2.41 times for an increase in temperature from 200 K to 500 K for GAA TFET and HD GAA TFET respectively at constant donor trap density of 1×10^{12} cm^{-2}. The enhanced BTBT rate of electrons is mainly due to the bandgap narrowing at higher temperatures, which lowers the tunneling barrier width at the source-channel junction and thus allows more number of electrons to tunnel through the valence band of the source to the conduction band of the channel. Further, it is analyzed that the presence of positive (negative) ITCs reduces (enhances) the flatband voltage (V_{fb}) by an amount of qN_f/C_{OX}, where q is the electronic charge, N_f is the trap charge density and C_{OX} is the gate oxide capacitance. This reduced (enhanced) V_{fb} in turn enhances (reduces) the effective gate voltage i.e. (V_{gs}-V_{fb}) at the tunneling junction and thereby increases (decreases) the Non-local BTBT rate of electrons at the source-channel junction. It should be noticed that the BTBT rate of electrons is significantly higher in the case of HD GAA TFET as compared to GAA TFET.

Power consumption is the major problem for further down-scaling the FET based devices, low operating voltage is requisite for reducing the power consumption and thus a low threshold voltage is desirable. Fig. 3(a) shows V_{th} for both the devices at various temperatures; the results also include the impact of ITCs.

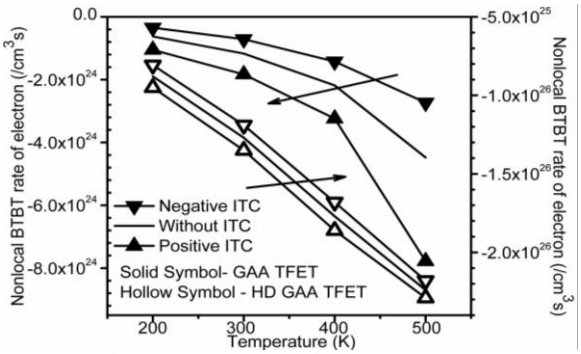

Fig. 2 Variation of Nonlocal BTBT rate of electrons at tunneling junction with respect to temperature at V_{gs}=1.2 V and V_{ds}=1.0 V, for GAA TFET and HD GAA TFET for fixed ITC density, $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC.

The constant current method i.e. the V_{gs} @I_{ds}=10^{-7}A is used for evaluating the V_{th}. The enhanced (reduced) effective gate voltage i.e. (V_{gs}-V_{fb}), due to the presence of positive (negative) ITCs, results in increases (decreases) the V_{th} of both the devices under consideration. Moreover, the V_{th} decreases almost linearly with an increase in temperature. The reduction in V_{th} with increase in temperature is mainly attributed to the higher tunneling rate of electrons at elevated temperature [see Fig. 2], resulting into early switching of the devices and thus a reduction in V_{th} in both the devices. As the temperature increases from 200 K to 500 K, the V_{th} reduces by 4.18% and 20.6% in case of GAA TFET and HD GAA TFET respectively.

SS is defined as the change in gate bias needed for one decade change in drain current. To decrease the V_{th} without negotiating with off current, reduced SS is essential.

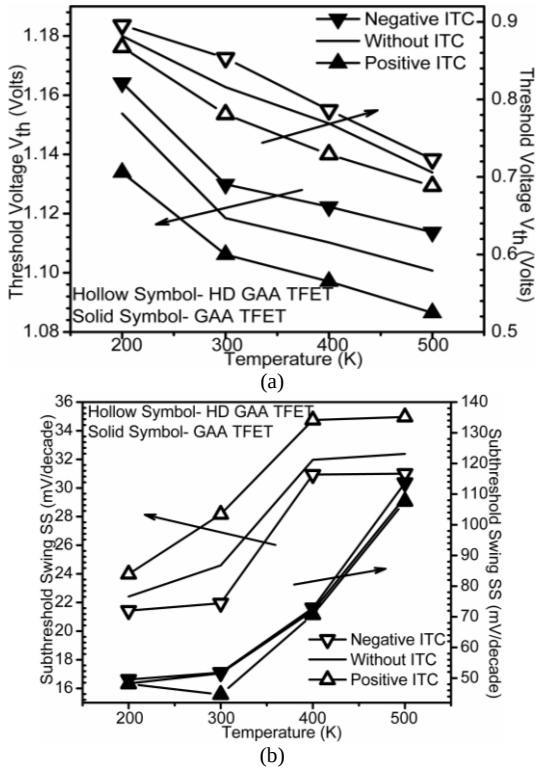

Fig. 3 Impact of temperature and ITCs on (a) Threshold voltage and, (b) subthreshold swing at V_{ds}=1.0 V of GAA TFET and HD GAA TFET for fixed ITC density, $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC.

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Further, for reduced switching power of CMOS circuits the SS of FETs should be reduced. SS of both the devices as shown in Fig. 3(b) indicates that SS has overcome the fundamental limit of MOSFETs in the case of HD GAA TFET at the entire temperature range. The degradation in SS at elevated temperature is due to the enhanced I_{OFF} [see Fig. 5(b)] at higher temperatures in both the devices. An increase in temperature from 200 K to 500 K enhances the SS by 2.29 and 1.36 times for GAA TFET and HD GAA TFET respectively. Moreover, it is also obtained that the presence of donor (acceptor) ITCs increases (decreases) the SS.

The transfer characteristics of GAA TFET and HD GAA TFET as a function of gate bias are shown in Figs. 4(a-b). Fig. 4(a) shows the effect of temperature (200-500 K), at a constant ITC of donor type density of 1×10^{12} cm^{-2}. It is clearly evident that for lower gate bias, there is a large variation in drain current w.r.t. temperature in comparison to the variations at higher gate bias. The higher variation with temperature in subthreshold region of transfer characteristics is due to the dominance of SRH recombination at lower gate bias, which has an exponential dependence on temperature [15].

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left[n + n_i \exp\left(\frac{E_{TRAP}}{kT_L}\right)\right] + \tau_n\left[p + n_i \exp\left(-\frac{E_{TRAP}}{kT_L}\right)\right]} \quad (1)$$

Where τ_p ($=10^{-7}$ s) and τ_n ($=10^{-7}$ s) are the electron and hole lifetimes respectively, E_{TRAP} is the difference between the trap energy and the intrinsic fermi level, T_L is the lattice temperature in degree Kelvin. This exponential dependence results into severe degradation in OFF characteristics at elevated temperatures. Whereas, the most relevant current component for TFET i.e. the BTBT, dominates at the higher gate bias. BTBT being smaller temperature dependence (caused by the BGN) results into slight increase in drain current as the temperature raises. Thus, in super-threshold regime the drain current of both the devices increases with temperature. This is due to the BGN at higher temperature, causing an increase in BTBT rate of electrons and thus the drain current. Moreover, the temperature coefficient is positive for entire gate bias range in both GAA TFET and HD GAA TFET. This is in contrary to the case of MOSFET where a positive/negative temperature coefficient exists for below/ above subthreshold regime respectively. Fig. 4(b) shows the impact of ITC on transfer characteristics of both the devices at constant temperature 200 K and 500 K. The lowering of barrier width at the tunneling junction due to the presence of donor trap charges results into enhancement in the drain current in both the devices as clearly evident from the Fig. 4(b). Thus, the presence of positive (negative) trap charges results in an increase (decrease) in drain current in both the aforesaid devices. Moreover, the presence of high-k material near source side i.e. in region-1 reduces the change in flat band voltage being inversely proportional to oxide capacitance (higher in the case of HD GAA TFET) and thus resulting in

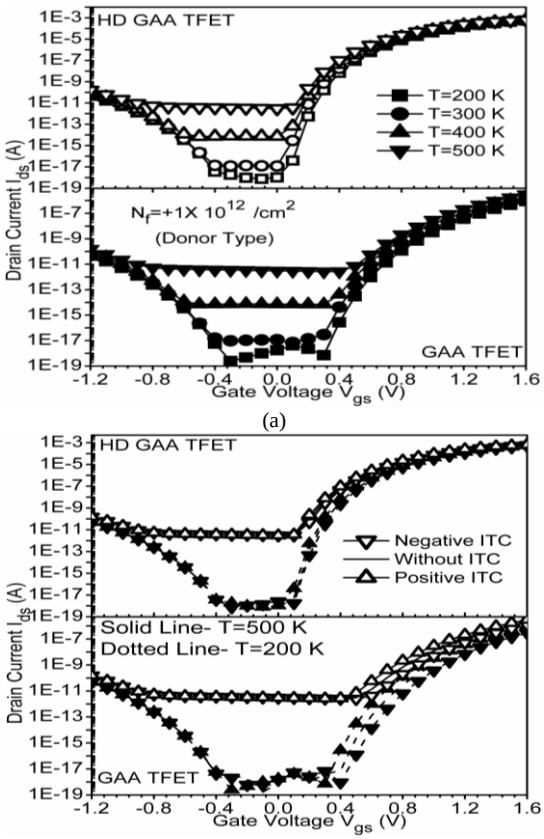

Fig. 4 (a) Effect of temperature on drain current I_{ds} as a function of V_{gs} at V_{ds}=1.0 V and at constant donor type ITC density $N_f = 1 \times 10^{12}$ cm^{-2} for GAA TFET and HD GAA TFET (b) Effect of ITC on drain current I_{ds} as a function of V_{gs} at V_{ds}=1.0 V and at constant temperatures T=200 K and 500 K.

better immunity against ITC in comparison to the case of GAA TFET [10].

Figs. 5(a-b) shows the effect of ITC and temperature on ON-state current (I_{ON}) and OFF state current (I_{OFF}) respectively of both GAA TFET and HD GAA TFET. It is clearly shown in Fig. 5(a) that the I_{ON} of HD GAA TFET is much higher than GAA TFET, quantitatively I_{ON} enhances from an order of 10^{-8} A (for GAA TFET) to 10^{-4} A (for HD GAA TFET). This enhanced I_{ON} of HD GAA TFET is attributed to the presence of high-k material in region 1, which enhances the tunneling rate of electrons and thus the drain current. The BGN with an increase in temperature, increases the I_{ON} in both the devices. The I_{ON} of HD GAA TFET and GAA TFET increases by 1.8 times and 5.64 times respectively, for a rise in temperature from 200 K to 500 K at a constant donor trap density of $N_F = 1 \times 10^{12}$ cm^{-2}. Further, there is an increase (decrease) in I_{ON} due to the presence of donor (acceptor) ITCs. It is because the presence of positive (negative) ITC reduces (enhances) the flatband voltage, and thus results in an increase (decrease) in the effective gate voltage (V_{gs}-V_{fb}). Lowering (enhancing) of the flat band voltage (V_{fb}), in turn, decreases (increases) the band bending of conduction and valence bands. This enhanced (reduced) band bending also results in lowering (higher) of tunneling barrier width [28] and hence enhances (reduces) the tunneling drain current.

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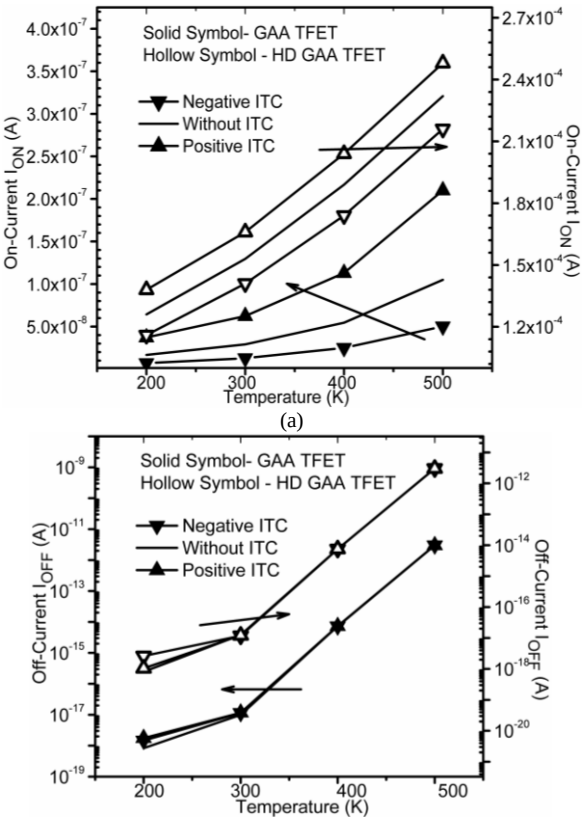

Fig. 5 Impact of temperature and ITCs on (a) ON-state current (at V_{gs}=1.2 V and V_{ds}=1.0 V) and, (b) OFF-state current (at V_{gs}=0 V and V_{ds}=1.0 V) of GAA TFET and HD GAA TFET for fixed ITC density, $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC.

Temperature affectability on I_{OFF} of both the devices is shown in Fig. 5(b). It is examined that at a higher temperature, the OFF-state characteristics degrade in both the aforementioned devices. Results show that I_{OFF} of GAA TFET and HD GAA TFET increases tremendously from an order of 10^{-18} A (at 200 K) to an order of 10^{-12} A (at 500K), for an increase in temperature from 200 K to 500 K. The large variation in I_{OFF} is mainly due to the dominance of SRH in subthreshold regime, which has a strong dependence on temperature. However, less dependence on temperature in both the devices in the superthreshold region is due the dominance of BTBT phenomenon at higher gate bias which has weaker temperature dependence [29-31].

Temperature affectability and impact of ITC on I_{ON}/I_{OFF} ratio of both GAA TFET and HD GAA TFET has been shown in Fig. 6(a). Significantly large I_{OFF} at higher temperatures results in tremendous degradation in switching ratio of both the devices at higher temperatures. This reduced I_{ON}/I_{OFF} ratio at high temperatures, causes the slow output transitions thereby degrading the device speed. Further, the presence of positive (negative) ITCs enhances (reduces) I_{ON}/I_{OFF} ratio. The reduction/enhancement is comparatively less in the case of HD GAA TFET, making it more reliable. Furthermore, the I_{ON}/I_{OFF} ratio is appreciably high in case of HD GAA TFET as compared to GAA TFET, resulting in a higher device speed. BTBT at the drain-channel junction for negative gate bias results into the ambipolar conduction of TFET. This I_{AMB}

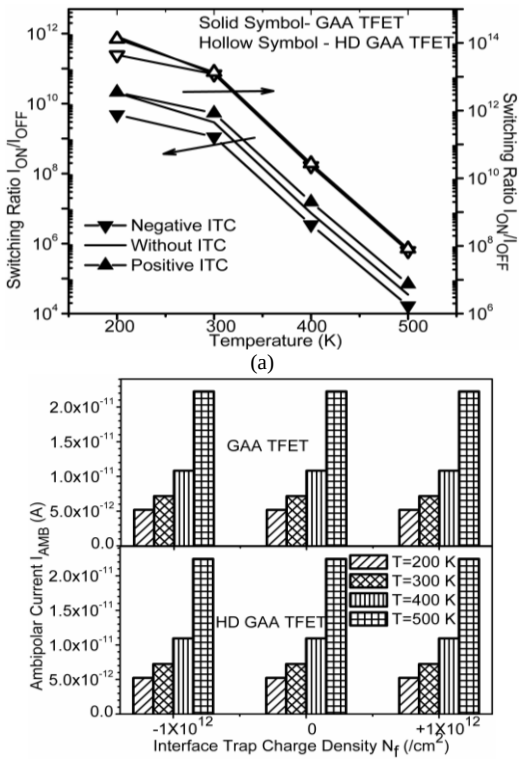

Fig. 6 Impact of temperature and ITCs on (a) Switching ratio I_{ON}/I_{OFF} ratio and, (b) ambipolar current (at V_{gs}=-1.2 V and V_{ds}=1.0 V) for GAA TFET and HD GAA TFET at fixed ITC density, $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC.

limits the applicability and feasibility of TFET for circuit level applications. Thus necessitates the quantitative evaluation of I_{AMB} at elevated temperature. I_{AMB} in our work has been defined as the drain current at V_{ds}=1.0V and V_{gs}= -1.0V and is shown in Fig. 6(b) for both the mentioned devices. I_{AMB} is higher at elevated temperatures, due to increase in drain current with temperature. Moreover, in this work the presence of ITC is considered only near the tunneling junction (due to the presence of high electric field), and the I_{AMB} is characterized by the drain-channel junction. Thus, the I_{AMB} is immune to the ITC.

To analyze the effect of temperature and ITCs at high-frequency, an important RF figure of merits i.e. cut-off frequency f_T has been studied. f_T is the parameter which is computed as the frequency at which the short circuit current gain drops to unity. The unity current gain cut-off frequency f_T of both the devices is plotted as a function of temperature and for the donor, acceptor and absence of ITC in Fig. 7(a). With an increase in temperature, BTBT rate of electrons increases thereby increases the drain current and the transconductance of the device. Thus, f_T of both the devices increases with a rise in temperature. Moreover the presence of positive (negative) ITC, enhances (lowers) the drain current and thus significantly increases (decreases) the f_T. Besides, the superior f_T is found in the case of HD GAA TFET in comparison to its counterparts. An important parameter to benchmark the performance of transistor in circuit applications is intrinsic delay τ, which is computed as [32]

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$$\tau = \frac{C_g V_{dd}}{I_{ON}} \qquad 2$$

Where C_{gg} is the parasitic gate capacitance, I_{ON} is the ON-current and V_{dd} is the drain bias voltage. For digital logic application intrinsic delay τ is a conventional metric. Fig. 7(b) shows the comparison between GAA TFET and HD GAA TFET in terms of intrinsic delay as a function of temperature, including the impact of ITC as well.

It is evident from Fig. 7(b) that there is considerable reduction in intrinsic delay in case of HD GAA TFET in comparison with GAA TFET. Quantitatively τ reduces from an order of 10^{-8} s (for GAA TFET) to 10^{-12} s (for HD GAA TFET) for entire temperature range. This reduction is due to the enhances I_{ON} in case of HD GAA TFET owing to the high-K material near tunneling junction instead of SiO_2 as in case of GAA TFET. Further, it is shown that at higher temperature intrinsic delay of both the devices reduces, due to the increase in drain current with temperature. For GAA TFET, a rise in temperature from 200 K to 500 K the intrinsic delay decreases by 5.84 times, 5.17 times and 4.64 times for the case of presence of the acceptor, absence, and donor ITC respectively at the interface of Si-SiO_2. Whereas, in the case of HD GAA TFET, the decrease in intrinsic delay is by 1.33 times, 1.24 times and 1.23 times for the case of presence of the acceptor, absence, and donor ITC respectively. The switching speed of FETs depends upon the parasitic capacitances, and the consequence of these parasitic capacitances cannot be overlooked at RF operations, as they determine the speed and power consumption characteristics of the device.

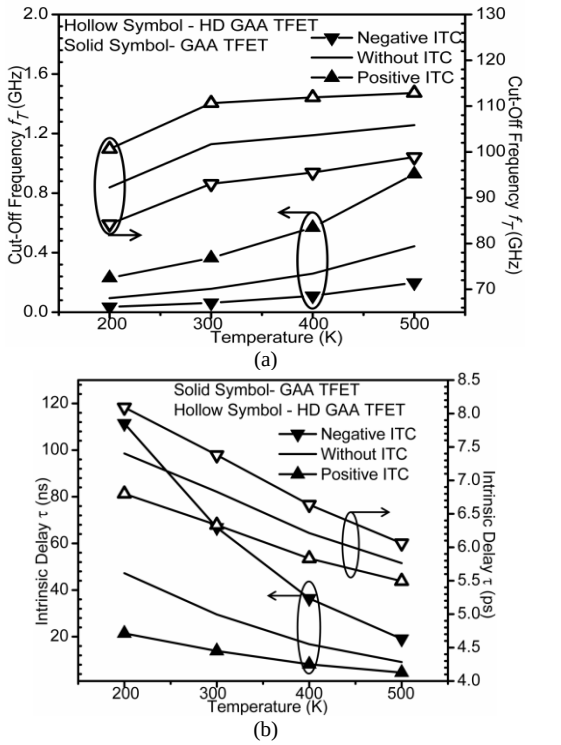

Fig. 7 Effect of temperature on (a) cut-off frequency f_T and (b) Intrinsic delay as a function of temperature for GAA TFET and HD GAA TFET at V_{ds}=1.0 V and at fixed ITC density, $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC.

Thus, for the design of TFET based circuits, the parasitic capacitances must be analyzed as they affect device properties such as the propagation delay and power dissipation. Therefore necessitates the quantitative examination of parasitic capacitances. In this work, the small signal AC analysis is done at f = 1MHz, to extract various parasitic capacitances. Further, as reported earlier, the capacitive distribution in the case of TFET is entirely different from that of MOSFET, due to the different energy band profiles of both.

In the case of TFET, the potential drop is very small at the drain-channel junction in contrast with MOSFET where a large reverse bias exists between drain-channel junction. This leads in a comparatively large gate-drain capacitance in TFET in comparison to MOSFET. Moreover the smaller gate-source capacitance C_{gs} (in comparison with C_{gd}) in the case of TFET for entire bias situations, results into $C_{gg} \sim C_{gd}$, this is again in contrast with MOSFET in which C_{gg} is almost equally contributed by both C_{gd} and C_{gs}. The enhanced C_{gd} causes overshoot in transient response in case of digital inverter circuits [33]. In the case of TFET, the inversion layer is formed initially at the drain side and moves towards the source side with an increase in gate bias. Thus, for TFET, gate to drain capacitances contributes majorly to the total gate capacitance in comparison to gate to source capacitance [34, 35]. The effect of temperature on total gate capacitance C_{gg} as a function of gate bias, of both the devices at a constant donor type trap density of 1×10^{12} cm^{-2} is shown in Fig. 8(a).

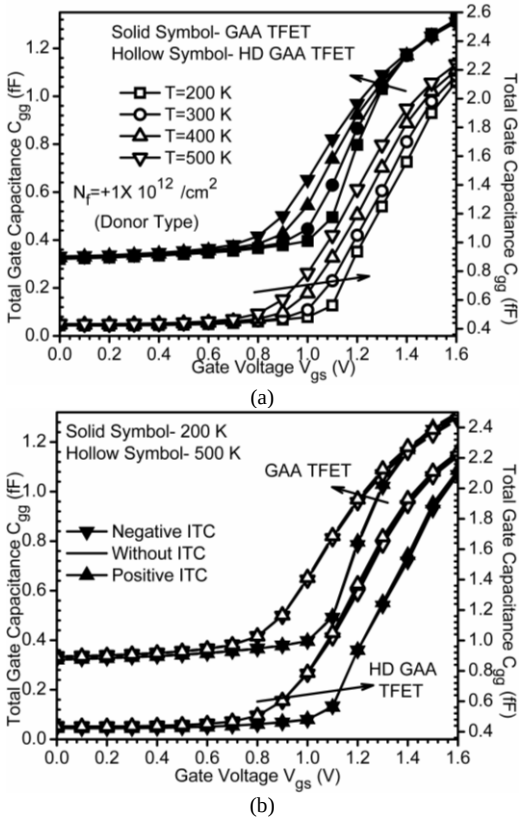

Fig. 8 (a) Effect of temperature on total gate capacitance as a function of V_{gs} at V_{ds}=1.0 V and at constant donor type ITC density $N_f = 1 \times 10^{12}$ cm^{-2} for GAA TFET and HD GAA TFET (b) Effect of ITC on total gate capacitance as a function of V_{gs} at V_{ds}=1.0 V and at constant temperatures T=200 K and 500 K at $N_f = \pm 1 \times 10^{12}$ cm^{-2}, and absence of ITC.

It can be observed from the Fig. 8(a) that, C_{gg} increases with a rise in temperature, in both the devices. At V_{gs}=1.2 V, there is an increase in C_{gg} by 1.21 times and 1.45 times for a rise in temperature from 200 K to 500 K for GAA TFET and HD GAA TFET respectively. Moreover, the higher C_{gg} in the case of HD GAA TFET as compared to its counterparts is owed to the presence of high-k material near the source-channel junction. Fig. 8(b) shows the impact of ITC on C_{gg} of both the devices at constant temperatures (200 K and 500 K). The presence of positive (negative) ITC increases (decreases) the C_{gg}, in both the devices. For the case of GAA TFET, the presence of donor (acceptor) ITC increases (decreases) the C_{gg} by 0.7% (0.7%) at 200 K and by at 6.0% (6.3%) at 500 K. Whereas for HD GAA TFET, the presence of donor (acceptor) ITC increases (decreases) the C_{gg} by 0.1% (0.03%) at 200 K and by at 2.1% (2.2%) at 500 K. With an increase in temperature, the parasitic gate capacitance degrades for both the devices, owing to the high leakage current, thus making the device more reliable for low temperature applications.

IV. Conclusion

Effect of ITCs and temperature has been studied on HD GAA TFET and GAA TFET. It is observed that with the application of hetero gate dielectric scheme, a superior device performance is achieved. Results demonstrate that HD GAA TFET has better immunity against ITCs and thus is more reliable. Results reveal that the reliance on temperature is device bias dependent. Below the threshold region, the impact of temperature is prominent due to the dominance of SRH at low gate bias, which has exponential temperature dependence. However, above the threshold regime, the BTBT phenomenon administers which has weak temperature dependence and thus leads to smaller variations in drain current. Further, in contrary to the case of MOSFET, a positive temperature coefficient has been obtained for the entire gate bias range in case of TFET. Moreover, the parasitic capacitances of the TFET also degrade with the raise in temperature. Thus, the characteristics of both the devices degrade at high temperatures, indicating that device is less suitable for high-temperature applications. The suitability of HD GAA TFET at low temperature can thus provide a pathway to meet the growing demand for low temperature tolerance of the logic circuits in aircrafts, space technology and for large-scale integration applications.

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TECHNICAL PAPER

Mathematical modeling insight of hetero gate dielectric-dual material gate-GAA-tunnel FET for VLSI/analog applications

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Abstract This paper presents a mathematical modeling insight for the novel heterogate dielectric-dual material gate-GAA TFET (HD-DMG-GAA-TFET) and validating the results with TCAD simulation. By using the appropriate boundary conditions and continuity equations, the Poisson's equation is solved to obtain the potential profile. The developed model is used to study the analog performance parameters such as subthreshold swing (SS), threshold voltage (V_{th}), transconductance (g_m), drain conductance (g_d), device efficiency (g_m/I_{ds}), intrinsic gain (g_m/g_d), channel resistance (R_{ch}) and output resistance (R_o). Further, to optimize the effect of metal work function on analog performance, three different combinations of DMG configurations has been studied. The results demonstrated that for a difference of 0.4 eV, the analog performance of the device is optimized. Low off current and high value of on current resulting into a higher I_{ON}/I_{OFF} ratio has been obtained, which is appropriate for sub-nanometre devices and low standby power applications. The analytical results obtained from the proposed model shows good agreement with the simulated results obtained with the ATLAS device simulator.

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1 Introduction

Continuously scaling down the MOSFETs dimensions to sub-nanometer region lead to escalation in the power consumption (active and passive) in modern microelectronic circuits. Reducing the applied bias (according to the scaling factor) to solve this dilemma leads to reduction in gate overdrive. Along with higher power density, the fundamental limit of kT/q (due to thermal process) which corresponds to a subthreshold swing (SS) of 60 mV/dec also hindered further scaling of threshold voltage (V_{th}) and off current. To overcome these limitations, there is a renewed interest in exploring new devices that uses a new current mechanism, and that does not involve carriers traveling over a potential barrier. Among various new devices Tunnel FET has been studied extensively in the past few years. TFET uses BTBT mechanism at the tunneling junction (the source channel junction) and normal drift diffusion mechanism away from the tunneling junction (Cho et al. 2011).

TFET has the potential to lower the SS beyond the 60 mV/dec limit of conventional MOSFETs along with the extremely low OFF-current. Therefore, TFET seems to be a well adaptive candidate for ultimately scaled switches and low power devices with excellent immunity to short channel effects (SCEs) (Bhuwalka et al. 2006; Born et al. 2006; Nirschl et al. 2006; Mookerjea et al. 2009). The major roadblock with the planar TFETs is its lower ON-state current (I_{ON}), which results in lower operating speed. In order to resolve this issue, numerous kinds of TFETs with various structures and materials such as double-gate, delta layer, SiGe, and PNPN structures have been proposed (Toh et al. 2007; Boucart and Ionescu 2007a, b; Toh et al. 2008; Mallik and Chattopadhyay 2011; Jhaveri et al. 2010; Cho et al. 2011; Lee et al. 2010; Noguchi et al. 2015). To enhance the I_{ON}, Silicon nanowire TFET has already been fabricated

(Gandhi et al. 2011). Further, a high-k material has been locally inserted (near the source side) in the gate dielectric to form heterogate-dielectric (HD) TFETs (Choi and Lee 2010; Mallik and Chattopadhyay 2011). The presence of high-k dielectric results into a higher band bending due to increase in surface potential (at a constant gate bias) (Jhaveri et al. 2010; Lee et al. 2012; Madan et al. 2015a, b). This higher band bending leads to reduction in tunneling barrier width, which further increases the generation rate and hence the I_{ON}.

Another major problem with TFET is ambipolarity. The ambipolarity in the device is the conduction for both high positive and high negative V_{gs} while keeping the V_{DS} only in one direction (negative for p-type devices and positive for n-type devices) (Cho et al. 2011; Conde et al. 2014; Hraziia et al. 2012; Lee et al. 2010; Shaker et al. 2015). Ambipolarity can be reduced by using a HD structure, in which the gate dielectric is split into two regions; high-k dielectric near the source side and low-k dielectric near the drain side. The higher value of dielectric improves the electrical coupling between the gate and the tunneling junction and hence, increases the tunneling rate. The DMG further helps in the improvement of ON and OFF current characteristics. Lower work function metal near the source side increases the band overlap and hence reduces the tunneling barrier width. This reduced tunneling barrier increases the tunneling probability, and the generation rate which results in higher I_{ON} and the higher value of work function near the drain side increases the tunneling barrier width and hence helps in reducing the I_{OFF}. So an optimum value of metal work function value at source and drain side should be chosen to trade-off between ON and OFF characteristics. In this work, a heterogate dielectric, Dual material gate, gate-all around (GAA) structure has been applied to TFET to enhance analog performance of the device (Madan et al. 2014).

The paper is structured as follows: Sect. 2 describes the device structure, parameters and simulation models used in this work, Sect. 3 describes the model formulation for the device Sect. 4 describes the results verification and discussions in which the effect of DMG configuration on the analog performance of the device has been studied. Finally, the conclusions are drawn in Sect. 5.

2 Device structure, parameters and simulation models

The device structural parameters used in both simulations and analytical model are fixed: channel length is 50 nm, with L_1 (20 nm) and L_2 (30 nm), gate oxide thickness (t_{ox}) = 3 nm and radius (R) = 10 nm. Further, the source (p+), drain (n+) and channel doping (p) are 10^{20}, 5×10^{18} and 10^{16} cm^{-3} respectively. To reduce ambipolarity effect source and drain are doped asymmetrically. In this analysis the analog performance is studied for the three different cases of DMG scheme to optimize the device for better analog performance and the cases are as stated below.

Case 1. $\Phi_{M1} = 4.1$ eV and $\Phi_{M2} = 4.8$ eV
Case 2. $\Phi_{M1} = 4.3$ eV and $\Phi_{M2} = 4.8$ eV
Case 3. $\Phi_{M1} = 4.4$ eV and $\Phi_{M2} = 4.8$ eV

Region 1 consists of dielectric constant $\varepsilon_1 = 21$ HfO_2 (near the source) and region 2 consists of $\varepsilon_2 = 3.9$ SiO_2 (near the drain) for all the cases. The source and drain junctions are abruptly doped for an effective band to band tunneling and the interface of high-k and SiO_2 is abrupt. The simulation device structure i.e. HD-DMG-GAA-TFET consisting of heterogate dielectric and Dual material gate is shown in Fig. 1. All simulations have been performed using the ATLAS device simulator. The most important model for TFET simulations is the band-to-band tunneling (BTBT) model. Non-local models have a more physical basis and don't depend on the electric field at the individual mesh points in the simulated device structure, but rather on band diagrams calculated along cross-sections through the device. According to BBT.NONLOCAL, the tunneling happens through the 1D slice, at the tunnel junction, where each slice and the tunnel junction are perpendicular to each other. These slices are parallel to themselves. For nonlocal BTBT model, the quantum tunneling meshing has been used at the source-channel junction. In n-TFET, the electrons tunnel through the valence band of the source to conduction band of the channel by BTBT mechanism and then the carriers drift from channel to drain. Thus, to incorporate the transport away from the tunneling junction drift diffusion model is used (Boucart and Ionescu 2007a, b). The bandgap narrowing model is used in the simulations to incorporate the effect of heavily doped source and drain regions (as tunneling current is a sturdy function of bandgap). Instead of Boltzmann statistics, Fermi–Dirac statistics have been used for the same reason (heavily source and drain doping). The models activated during simulation

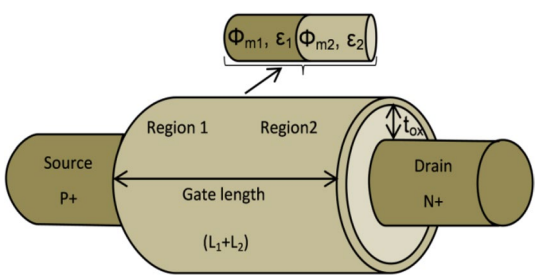

Fig. 1 Structure of n-type heterogate dielectric-dual material gate-Gate all around-tunnel FET (HD-DMG-GAA-TFET)

Table 1 Model parameters used in simulation

Physical model	Parameter	Value
Shockley–Read–Hall for carrier recombination (SRH)	TAUN0	1.0×10^{-7} s
	TAUP0	1.0×10^{-7} s
Bandgap narrowing (BGN)	BGN.E	6.92×10^{-3} V
	BGN.N	1.3×10^{17} cm^{-3}
Nonlocal band to band tunneling model (BBT. NONLOCAL)	BB.A	4.0×10^{14} V^{-2} s^{-1} cm^{-1}
	BB.B	1.9×10^{7} V cm^{-1}
	γ	2

Table 2 List of constant parameters

Parameters	Symbol	Value and unit
Electron affinity	χ_{si}	4.17 eV
Permittivity of silicon	ε_{Si}	11.8
Bandgap of silicon	E_g	1.08 eV
Temperature	T	300 K
Boltzmann constant	k_B	1.38066×10^{-23} J K^{-1}
Elementary charge	q	1.60219×10^{-19} C
Plank's constant	h	6.63×10^{-34} J s

are as follows: concentration and field dependent mobility model, Shockley–Read–Hall for carrier recombination, non-local band to band tunneling, band gap narrowing, Fermi–Dirac statistics and drift diffusion (Fukuda et al. 2013; Atlas User's Manual 2014). The parameters used in simulation along with their values are listed in Table 1.

3 Model formulation for HD-DMG-GAA-TFET

Assuming that the influence of the charge carrier and fixed carriers are uniform in the channel, it can be neglected. The parabolic potential profile along the radial direction is assumed and based on the following boundary conditions, the Poisson's equation is solved.

1. The surface potential is only z-dependent

$$\Phi_{si}(R,z) = \Phi_{si}(z) \tag{1}$$

2. The Electric field at the center of the channel is zero

$$\left.\frac{d\Phi_{si}(r,z)}{dr}\right|_{r=0} = 0 \tag{2}$$

3. Electric field at Si/SiO_2 interface is continuous

$$\left.\frac{d\Phi_{si}(r,z)}{dr}\right|_{r=R} = \frac{C_{fi}}{\varepsilon_{si}}[V_{GS} - \Phi_{si}(z) - V_{FBi}] \tag{3}$$

where; $V_{FBi} = \phi_{mi} - \phi_s$ is the flatband voltage. i = 1and 2 for region 1 and 2 respectively and Φ_s is the semiconductor work function.

$$\phi_s = \chi_{si} + E_g/2q + \phi_F \tag{4}$$

and $\phi_F = k_BT/q(\ln(N_{Ch}/n_i))$ is the fermi potential. Where the parameters, symbols and their values are as listed in Table 2.

C_{f1} and C_{f2} are the capacitances per unit area of the gate dielectric for region 1 and 2 respectively and are given by

$$C_{f1} = \frac{\varepsilon_1}{R\ln\left(1+\frac{t_1}{R}\right)} \text{ and } C_{f2} = \frac{\varepsilon_2}{R\ln\left(1+\frac{t_2}{R}\right)} \tag{5}$$

where $t_1 = t_2 = t_{ox}$, is the gate oxide thickness.

Solving Eqs. (1)–(5) we can obtain

$$\frac{\partial^2\Phi_{si}(z)}{\partial z^2} - k_i^2\Phi_{si}(z) = \eta_i \tag{6}$$

The general solution of (6) is

$$\Phi_{si}(z) = A_x\exp(k_iz) + A_y\exp(-k_iz) - \eta_i/k_i^2 \tag{7}$$

where $k_i^2 = \frac{2C_{fi}}{R\varepsilon_{Si}}$ and $\eta_i = \frac{qN_i}{\varepsilon_{Si}} - k_i^2\left[V_{gs} - V_{FBi}\right]$

Now using the following boundary conditions at the interface of each region, coefficients A_x and A_y can be determined.

At the source end

$$\Phi_{s1}(0) = -\frac{k_BT}{q}\ln\left(\frac{N_{source}}{n_i}\right) = V_{bi1} \tag{8a}$$

And at the drain end

$$\Phi_{s2}(L_g) = \frac{k_BT}{q}\ln\left(\frac{N_{Drain}}{n_i}\right) + V_{DS} = V_{bi2} + V_{DS} \tag{8b}$$

At the interface of region 1 and region 2,

$$\Phi_{s1}(L_1) = \Phi_{s2}(L_1) \tag{8c}$$

$$\left.\frac{d\Phi_{S1}}{dz}\right|_{z=L_1} = \left.\frac{d\Phi_{S2}}{dz}\right|_{z=L_1} \tag{8d}$$

The lateral electric field (2D) is given by

$$E_z(r,z) = -\frac{d\Phi_{si}(r,z)}{dz} \tag{9}$$

The lateral surface electric field is given by

$$E_{sz}(r,z) = A_xK_1e^{K_1z} - A_yK_2e^{K_2z} \tag{10}$$

Transverse electric field (2D)

$$E_r(r,z) = 2rP_2(z) \tag{11}$$

The tunneling generation rate determined by Eq. (13) is integrated over the volume ($\pi r^2 w_T$) to obtain the drain

current. Where w_T is the tunneling barrier width defined as the shortest distance between the valence band of the source and conduction band of the channel. It is determined from the surface potential profile, by taking the difference between the points where the surface potential falls by an amount equal to E_g/q below the surface potential and where the potential is Φ_s and is calculated as:

$$w_T = \frac{1}{K_1}\left[\ln\left[\frac{\Phi_s(z)+\frac{E_g}{q}+\frac{\eta_1}{K_1^2}+\sqrt{\left(\Phi_s(z)+\frac{E_g}{q}+\frac{\eta_1}{K_1^2}\right)^2-4C_1C_2}}{\Phi_s(z)+\frac{\eta_1}{K_1^2}+\sqrt{\left(\Phi_s(z)+\frac{\eta_1}{K_1^2}\right)^2-4C_1C_2}}\right]\right] \tag{12}$$

The tunneling generation rate can be evaluated as

$$G_{BBT} = AE^{\gamma}e^{-B/E} \tag{13}$$

where A, B and γ are the parameters dependent on the effective mass of electron and hole.

$$A = \frac{q^2\sqrt{2m_{tunnel}}}{h^2\sqrt{E_g}}, B = \frac{\pi^2 E_g^{3/2}\sqrt{m_{tunnel}/2}}{qh} \text{ and } \gamma = 2 \tag{14}$$

where m_{tunnel} is the effective mass $= 0.25m_0$ and m_0 is the rest mass of an electron. The values of A (BB.A) and B (BB.B) are listed in Table 1. The average electric field E_{avg} is calculated by integrating the total electric field E_{Tot} over the barrier width w_T as:

$$E_{Tot} = \sqrt{|E_z|^2+|E_r|^2} \text{ and } E_{avg} = \frac{\int_{w_T} E_{Tot}dz}{w_T} \tag{15}$$

The expression for drain current (I_{ds}) is obtained as:

$$I_{ds} = q\pi R^2 w_T G(E_{avg}) \tag{16}$$

4 Result verification and discussion

Figure 2 shows the comparison of proposed device i.e. HD-DMG-GAA-TFET with the gate all around tunnel FET as reported by Ying et al. (2014). As evident from Fig. 2 that the V_{th} of GAA-TFET is high as compared to the proposed device. Moreover, the I_{ON} of proposed device is 219 times enhanced in comparison to the GAA TFET. Both the lower V_{th} and higher drain current makes the DMG scheme beneficial for VLSI/analog applications. Therefore in this work, critical analog parameters such as transconductance g_m, output conductance g_d, early voltage V_{EA}, device efficiency g_m/I_{ds}, intrinsic gain A_v, channel resistance R_{ch} and output resistance R_{out} has been studied to analyze the effect of DMG on the device performance.

The effect of gate bias and metal work function on electric field near source and drain side is shown in Fig. 3a. As expected, the electric field is enhanced (near both source and drain side) with an increase in gate bias. Further, as the metal near drain side is constant; hence, the electric field near the drain is almost same for each case. With the increase in the difference in metal work function, the electric field near the source side enhances, which results in an additional lowering of barrier width and thus an increase in tunneling rate is obtained, which eventually leads to greater tunneling current and sought out the primary obstruction of TFET. Further, the SS is the amount of gate voltage required for one decade change in the drain current. In order to reduce the switching power of CMOS circuits, SS of the device should be as low as possible. Moreover, to accurately predict the circuit behavior, the V_{th} is an important parameter. The influence of metal work functions on the SS and V_{th} of the device is shown in Fig. 3b.

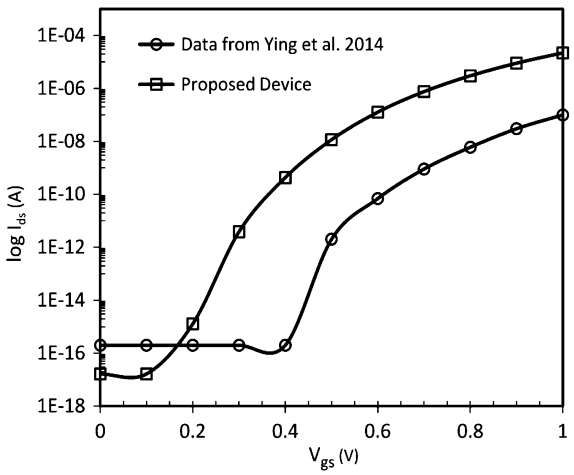

Fig. 2 Drain current–voltage comparison of proposed device HD-DMG-GAA-TFET with gate all around tunnel FET data from Ying et al. (2014)

According to the previously reported work (Choi and Choi 2013), the I_{ON} can be enhanced by using a gate metal of lower work function near the source in comparison with metal used near drain side and to reduce the I_{OFF}, metal work function near drain should be high as compared to the metal used near the source. So in order to achieve an optimum device performance, metal near drain is kept constant ($\Phi_{M2} = 4.8$ eV) and the metal near source side is varied. As we increase the work function of metal near source side from 4.1 to 4.4 eV, the SS of the device is decreasing, but the V_{th} of the device is increasing. So the metal work function should be chosen such that the device is optimized in terms of both SS and V_{th}.

The transfer characteristics (I_{ds}–V_{gs}) are shown in Fig. 4a in both log scale and linear scale for each case. The graph shows the I_{OFF} of the order of 10^{-17} A and I_{ON} of the order

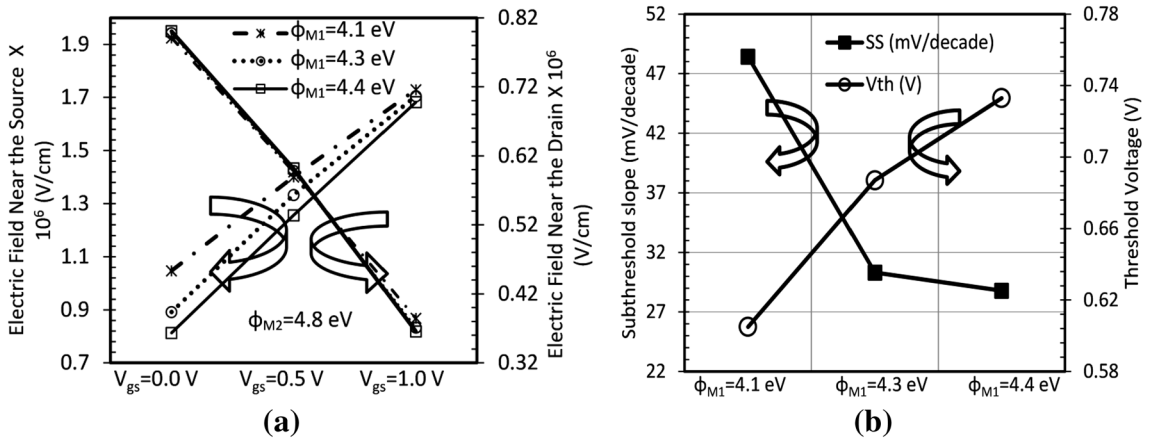

Fig. 3 **a** Electric field near source and drain side at constant $V_{ds} = 1.0$. **b** SS and V_{th} for different metal work function of HD-DMG-GAA-TFET

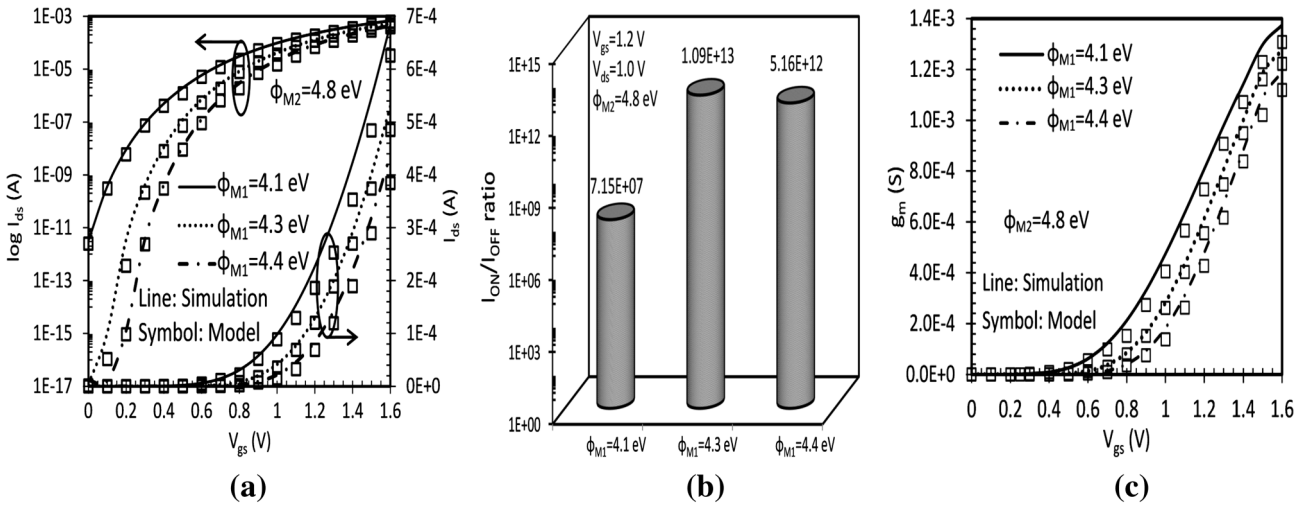

Fig. 4 **a** Transfer characteristics (I_{ds}–V_{gs}) in log and linear scale, **b** I_{ON}/I_{OFF} ratio, **c** transconductance as a function of V_{gs} for different metal work function for HD-DMG-GAA-TFET at constant $V_{ds} = 1.0$ V

of 10^{-4} A, which results in I_{OFF}/I_{ON} ratio of the order of 10^{13}. The lower value of I_{OFF} leads to a lower value of static power dissipation. Again, an increase in difference in metal work function leads to enhancement of I_{ON} by 1.5 times in case 1 as compared to case 3, but simultaneously I_{OFF} has also been increased significantly. So we need to optimize the values of metal work function to obtain an optimum value of I_{ON}/I_{OFF} ratio depending on the application. The increase in I_{ON} is the main advantage of heterogate dielectric and dual material gate. Also, it can be clearly seen from the graph that the model prediction and ATLAS device simulation are in good agreement. Figure 4b shows the variation of I_{ON}/I_{OFF} with different metal work function configurations of DMG. It is apparent from the bar graph that as work function of metal 1 increases from 4.1 to 4.3 eV the I_{ON}/I_{OFF} ratio enhances by an order of 10^5 times. Moreover for $\phi_{M1} = 4.4$ eV, the I_{ON}/I_{OFF} ratio reduces by 0.47 times w.r.t. case 2 and increases w.r.t. case 1. The reduction in I_{ON}/I_{OFF} ratio in case 3 w.r.t. case 2 is mainly attributed to enhanced I_{OFF} as shown in Fig. 4a. Transconductance g_m, which is basically the first order derivative of the drain current with respect to the gate voltage at constant drain voltage, is shown in Fig. 4c. Transconductance decides the current driving capability of the device for a given input voltage swing. It is clear from Fig. 4c that among the three cases, the higher value of transconductance is achieved for case 1. In each case, the transconductance of the device is very much higher in the case of on state as compared to off state. So for enhanced tunneling current and transconductance, the difference of metal work function should be possibly large.

The output characteristic (I_{ds}–V_{ds}) for each case is shown in Fig. 5a. The saturation mechanism of output characteristics in the case of TFET is mainly attributed to the saturation of tunneling barrier width for higher drain bias at a constant gate bias (Boucart and Ionescu 2007a, b, Madan et al. 2015a, b). It is evident from the figure that the device predicts a qualitative agreement in linear regime and also shows a good saturation in drain current for higher drain voltages. Among the three cases, the tunneling current is enhanced by 2.7 times in case 1 with respect to case 3; thus makes it suitable for analog applications. Figure 5b illustrates the effect of DMG configurations on drain/output conductance g_d. Further, in order to achieve high gain, transistors should have low output conductance for analog applications. The output conductance is increasing with an increase in drain bias and then attains maxima and further increase of drain bias reduces the drain conductance because of higher drain resistance at higher drain bias. As we reduce the metal work function difference, output conductance decreases, as is evident from Fig. 5b.

Figure 6a illustrates comparison of the device efficiency g_m/I_{ds} for each case. Device efficiency is the ability to convert dc power into ac gain performance at a particular drain bias. For each case, the highest value of g_m/I_{ds} is obtained for the weak inversion region and then a linear decrease is obtained with an increase in gate bias. Among the three cases, case 3 has higher device efficiency. For each case, the device efficiency has reached a value greater than 40 V^{-1} (the fundamental limit of conventional MOSFET) in the subthreshold region. Intrinsic gain is a valuable analog

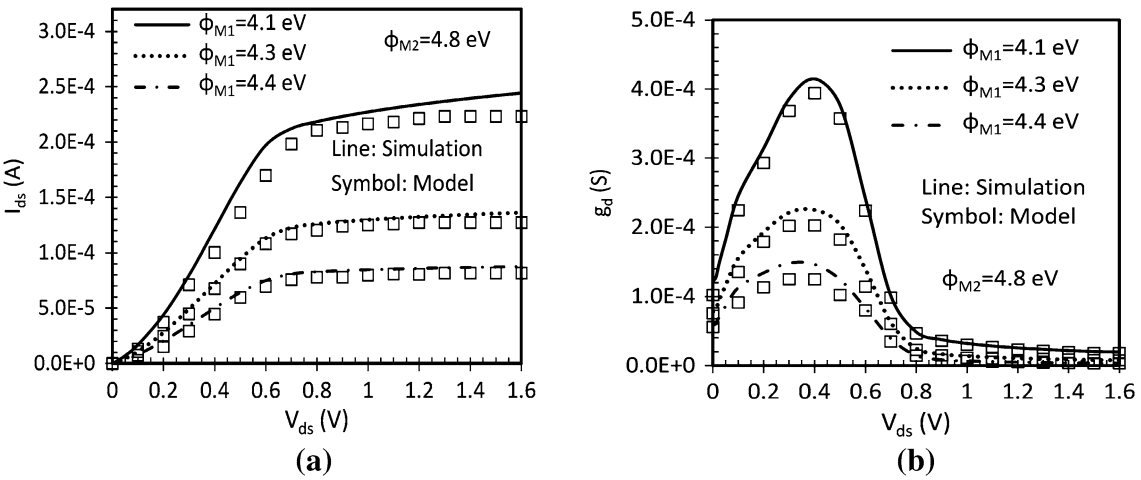

Fig. 5 **a** Output characteristics (I_{ds}–V_{ds}) and **b** output conductance for different metal work function of HD-DMG-GAA-TFET at constant $V_{gs} = 1.2$ V

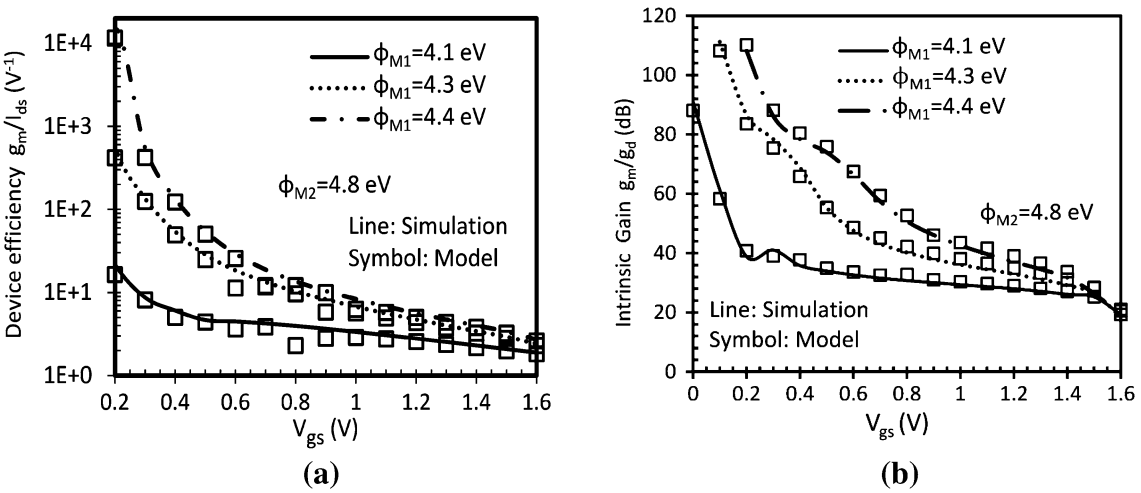

Fig. 6 **a** Device efficiency and **b** Intrinsic gain as a function of gate voltage V_{gs} for different metal work function for HD-DMG-GAA-TFET at $V_{ds} = 1.0$ V

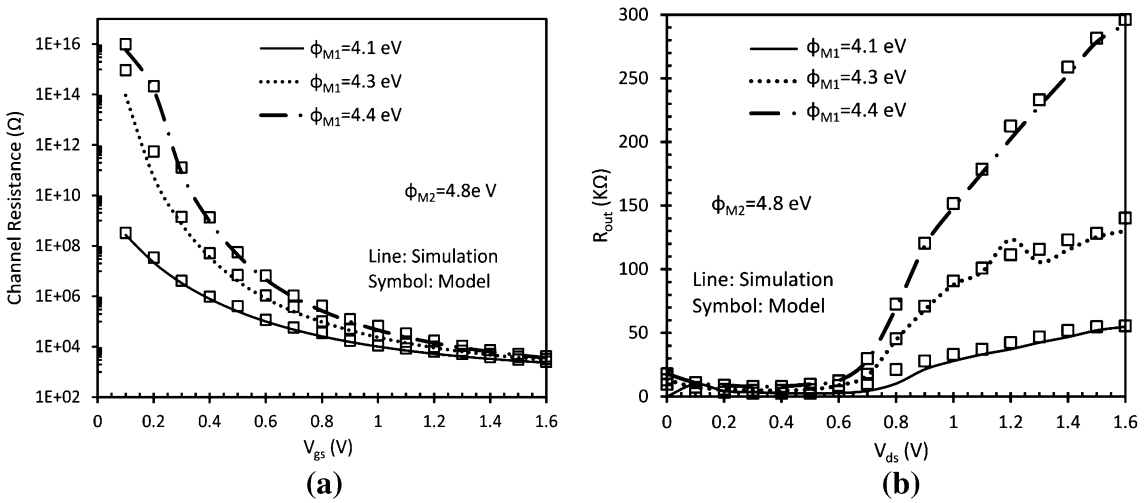

Fig. 7 **a** Channel resistance and **b** output resistance for different metal work function of HD-DMG-GAA-TFET

circuit design parameter used for designing amplifiers such as an operational transconductance amplifier (OTA). For better analog performance, an intrinsic gain of the device should be as high as possible. Comparison between of the intrinsic gain for different metal work function configuration with respect to gate bias is presented in Fig. 6b. The intrinsic voltage gain is obtained at the constant drain bias $V_{ds} = 1.0$ V, making use of the relation $A_v = g_m/g_d$. Highest intrinsic gain for a metal work function difference of 0.4 eV is attributed to the dominated decrease in output conductance in comparison with the increase in transconductance.

The influence of gate voltage and dual material gate configurations on channel resistance R_{ch} is demonstrated in Fig. 7a. For $V_{gs} = 0$ V, no band bending is there, ensuring into higher tunneling barrier width at the tunneling junction, resulting into very high R_{ch} of the order of 10^{15} Ω. As the gate bias increases, bands in the channel move downwards resulting in lowering of the tunneling barrier width as if a conductive channel is formed and thus drops the R_{ch} to a value of several KΩ's. Moreover, at lower gate bias, higher R_{ch} has been obtained for the case when metal work function difference is 0.4 eV, which shows a better OFF state characteristics for this configuration in comparison with the rest of the cases when the metal work function difference is 0.7 and 0.5 eV. Another important parameter for analog application is the output resistance or the drain resistance R_o. Drain resistance is numerically equal to the inverse of the output conductance. The variation of output resistance with the drain to source voltage is shown in Fig. 7b. It is clearly shown in the figure that in the linear region, the output resistance is very small, because of strong dependence of the drain current on drain voltage. But as the drain current saturates for the higher drain bias, R_o increases monotonically. It is evident from the figure that for the case when metal work function difference is 0.4 eV, R_o is found to be extremely high due to the better output saturation current as shown in Fig. 7b.

5 Conclusion

The present work is the detailed mathematical modeling insight for the analog performance of HD-DMG-GAA-TFET. The results obtained by simulations and analytical modeling are in good agreement. The tuning of metal work functions has been done to optimize the effect of Dual metal gate on the analog performance, which shows that both device efficiency and device gain are improved for a metal work function difference of 0.4 eV. Decrease in SS and increase in V_{th} is found on decreasing the difference between work functions of two metal used near source and drain junction. Moreover, I_{OFF}/I_{ON} ratio of the order of 10^{13} has been obtained for the same DMG configuration, making it suitable for low power applications. Enhancement of channel resistance and output resistance is obtained as we decrease the difference of the metal work functions. Moreover, it has been evaluated that SS is less than 60 mV/decade in each case, and device efficiency is more than 40 V^{-1} in the subthreshold region. This indicates that the developed model also validates with the fact that TFET overcomes the fundamental limit of MOSFET.

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TECHNICAL PAPER

Performance investigation of heterogeneous gate dielectric-gate metal engineered–gate all around-tunnel FET for RF applications

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Abstract In this work, the effect of gate metal work function engineering (GME), gate bias and drain bias on the bias dependent parasitic capacitances has been studied. Further, RF Figure of merits (FOMs) such as power gains, cut-off frequency (f_T), maximum oscillation frequency (f_{Max}) and intrinsic delay of hetero-dielectric gate-metal-engineered gate-all-around tunnel FET (HD-GME-GAA-TFET) are studied and compared with HD-GAA-TFET. Simulation results show an appreciable improvement in RF FOMs with the application of GME architecture on GAA TFET. Further, it has been observed that GME exhibits 3.76 times enhancement and 0.017 times reduction in cut-off frequency and intrinsic delay respectively as we increase the work function difference, which makes it a promising candidate for low power switching applications. Moreover, the small signal Y-parameters have also been studied which indicates that HD-GME-GAA-TFET is a promising candidate for RF/microwave applications. All the simulations have been done using ATLAS device simulator.

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1 Introduction

The escalating power crisis in the CMOS Technology due to aggressive device contraction has become an issue of concern for circuit designers. Along with enhanced static power dissipation, the conventional MOSFET faces arduous challenges such as numerous short channel effects (SCE) and leakage current. Extensive materials and novel device structures such as multi gate device architecture (Kavalieros et al. 2006), CNT/graphene based FET (Wang et al. 2008), alternate channel materials (Wu et al. 2009), were proposed to resolve these hitches. But due to the thermionic emission transport mechanism, the subthreshold swing of the MOSFET has a theoretical limitation of 60 mV/dec at room temperature. Therefore, one desires to design a device which uses other mode of carrier transport so that a lower subthreshold swing can be achieved. To overcome this, alternative device structures such as tunnel field-effect transistors (TFETs) are proposed. TFET uses a new current transport mechanism that does not involve Maxwell–Boltzmann statistics. Due to its built-in tunnel barrier, the TFET device does not suffer from SCEs, when compared to the conventional MOSFET devices. The basic architecture of TFET is a gated P-i-N diode with very high doping of P and N region working in reverse bias. Basic operation of TFET is based on Band to band tunneling of electrons from the valence band of the source to the conduction band of the channel, when a positive gate voltage greater than the threshold voltage is applied at gate such that it lower the bands in the channel and reduces the tunneling barrier width in case of n-TFET and allow electrons to tunnel through source to channel junction and then to drain (Madan and Chaujar 2016a). In the off-state for N-type TFET, the valence band of source is located below the conduction band of channel (Ionescu and Riel 2011). Due to the presence of large

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tunneling barrier at the source-channel junction, the probability of the tunneling of electrons through this barrier is negligible. This results into very small off-state leakage current. This in turn lowers the value of off-state leakage current and results into better SCE immunity, and reduction in static power dissipation. Due to steeper SS and low OFF state current, TFET has been regarded as the most promising candidate for low standby power applications (Vandooren et al. 2013; Ghosh and Akram 2013; Guo et al. 2013; Lee et al. 2013) But the limited transmission through the large tunneling barrier present at the source channel junction and the higher effective carrier mass results into a low ON state current. To improve the major shortcoming of TFET (lower I_{ON}) without sacrificing I_{OFF} is the major engineering challenge for low power applications. This dilemma can be resolved by modifying the structure architectures such as thin silicon body (Toh et al. 2008), multi gate architecture (Zhang et al. 2012), dual material gate (Saurabh and Kumar 2011), low-k spacer (Anghel et al. 2010), heterogate dielectric (Choi and Lee 2010; Madan et al. 2015a) and gate source/drain overlap/underlap (Chattopadhyay and Mallik 2011; Verhulst et al. 2007) or by using altered materials other than silicon such as a channel material with lower bandgap (Yang et al. 2013), Ge in the source side (Kim et al. 2009) and delta layer of SiGe at the edge of the source (Bhuwalka et al. 2004). Another major problem with TFET is the ambipolar conduction (Wang et al. 2004) means conduction in two directions, both for positive and negative gate voltages. In this work we have incorporated the gate all around geometry, dual metal gate and heterogate dielectric for acquiring better performance of the device (Madan et al. 2015a).

The paper is organized as follows: Sect. 2 describes the device structure and simulation models, Sect. 3 describes the simulation methodology and the calibration of our model with the simulation results, Sect. 4 describes the effect of gate and drain bias along with effect of GME on parasitic capacitance and the effect of gate metal engineering is studied on unilateral power gain, current gain, maximum transducer power gain, intrinsic delay, maximum available power gain, cut-off frequency, maximum oscillation frequency and the Y-parameters. Finally the conclusions are drawn in Sect. 5.

2 Device analysis and simulation

The device structure i.e. HD-GME-GAA-TFET consisting of Gate metal engineered and heterogate dielectric is shown in Fig. 1. During the simulation, silicon is used as source, channel and drain material, gate all around structure with channel radius (R) = 10 nm, channel length L_g (=L_1 + L_2) = 50 nm (=20 + 30 nm) and gate oxide

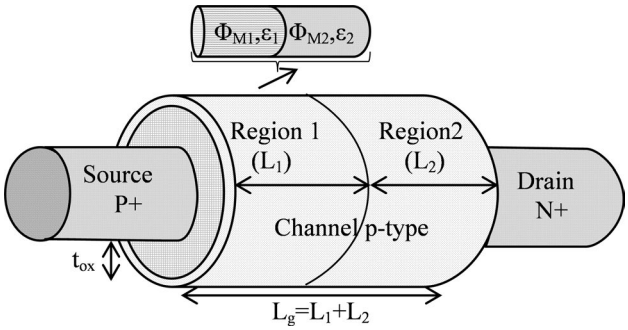

Fig. 1 Structure of n-type heterogeneous gate dielectric-gate metal engineered-GAA-TFET (HD-GME-GAA-TFET)

thickness (t_{ox}) = 3 nm is used. The source is p^+ type doped (10^{20} cm^{-3}), body is lightly p type doped (10^{16} cm^{-3}) and drain is n^+ doped (5×10^{18} cm^{-3}). To inhibit the ambipolarity effect, (tunneling at drain and channel junction) source and drain are doped asymmetrically.

Case 1. $\Phi_{M1} = 4.1$ eV (Al) and $\Phi_{M2} = 4.8$ eV (Au).
Case 2. $\Phi_{M1} = 4.3$ eV (Cr) and $\Phi_{M2} = 4.8$ eV.
Case 3. $\Phi_{M1} = 4.4$ eV (Ti) and $\Phi_{M2} = 4.8$ eV.
Case 4. $\Phi_{M} = 4.8$ eV.

Region 1 consists of dielectric constant $\varepsilon_1 = 21$ HfO_2 (near the source) and region 2 consists of $\varepsilon_2 = 3.9$ SiO_2 (near the drain) for all the cases. The source and drain junctions are abruptly doped for an effective band to band tunneling. In this work, the interface of high-k and SiO_2 is also abrupt with no interface defects. The interface defects however, had earlier been analyzed by (Madan and Chaujar 2016a). Various parasitic capacitances are extracted by small signal ac analysis at 1 GHz frequency. As the response time of the device is dependent on the gate to drain capacitance, so the drain capacitance is analyzed for the variation of both gate and drain bias. Further, the active power dissipation ($C_{gg}V_{dd}^2 f$) interdependence on the total gate capacitance C_{gg}, so the effect of gate and drain bias on total gate capacitance is also studied. Then to analyze the switching speed of the device f_T is studied. Moreover the effect of GME configurations on various high frequency gains and the admittance parameters has also been studied. To analyze the effect of gate metal work function, the dielectric constant of oxide for heterogeneous gate dielectric is kept constant throughout the simulation.

3 Model validation

3.1 Simulation methodology

All simulations have been performed using the ATLAS device simulator. The models invoked during simulation are described in Table 1. Both the numerical methods Gummel

Table 1 Simulations model

Physical models	Description
Mobility models	Concentration and field dependent mobility model is used
Recombination model	Shockley–Read–Hall (SRH) recombination also called trap assisted recombination is used to incorporate minority recombination effects with carrier lifetime (TAUP0 = 1×10^{-7} s). This process is the dominant generation and recombination process in silicon and other indirect bandgap materials
Statistics	Fermi–Dirac statistics, the use of Fermi–Dirac statistics are essential to account for certain properties of very highly doped (degenerate) materials. Such as reduced carrier concentrations in heavily doped regions (statistical approach)
Energy transport model	The simplest model of charge transport that is the drift–diffusion model is used. This model has the attractive feature that it does not introduce any independent variables in addition to ψ, n and p
Tunneling models	The most important model for Tunnel FET simulations is the band-to-band tunneling (BTBT) model. Non-local models have a more physical basis and do not depend on the electric field at the individual mesh points in the simulated device structure, but rather on band diagrams calculated along cross-sections through the device. According to BBT.NONLOCAL, the tunneling happens through 1D slice, at the tunnel junction, where each slice and the tunnel junction are perpendicular to each other. These slices are parallel to themselves
Bandgap narrowing model	For higher doping (>10^{18} cm^{-3}) experimental work has shown that the pn product in silicon becomes doping dependent. As the doping level increases, a decrease in the bandgap separation occurs

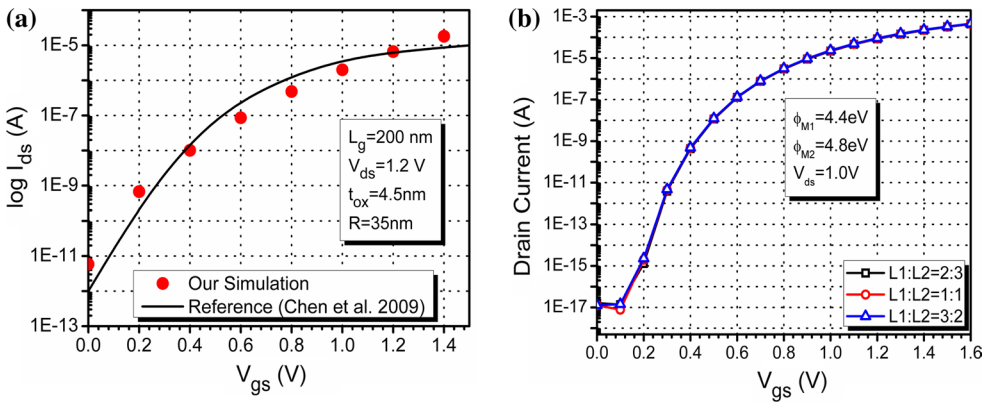

Fig. 2 **a** Calibration with the published result, I_{ds}–V_{gs} characteristics of 200 nm gate length SiNW-TFET (Chen et al. 2009). **b** Effect of tunneling gate length L_1 and auxiliary gate length L_2 on the transfer characteristics of HD-GME-GAA-TFET at constant $\Phi_{M1} = 4.4$ eV and $\Phi_{M2} = 4.8$ eV

(decoupled) together with Newton's (fully coupled) has been incorporated to mathematically solve the carrier transport equation (Atlas User's Manual 2014).

3.2 Calibration

Before simulating the device structure, the simulation models have been calibrated with the already published results (Chen et al. 2009). Figure 2a shows the transfer characteristics of the extracted data from the reference (Chen et al. 2009) and results obtained from the simulations. The results so obtained are in close proximity, thus validates the model parameters during the simulations. To analyze the impact of tunneling gate length and auxiliary gate length on the device performance, the effect of L_1 and L_2 has been studied on the transfer characteristics of HD-GME-GAA-TFET at a constant $\Phi_{M1} = 4.4$ eV and $\Phi_{M2} = 4.8$ eV. The plot of drain current with respect to gate voltage at a constant drain bias of 1.0 V for HD-GME-GAA-TFET at different combinations of L_1 and L_2 such as (20 + 30 nm), (25 + 25 nm) and (30 + 20 nm) is shown in Fig. 2b. It is clearly evident from the Fig. 2b that the drain current is immune to the variations of L_1 and L_2. This immunity against L_1 and L_2 is mainly attributed to the fact that TFET is a junction dependent device and its performance is mainly impacted by the tunneling junction and the drain channel junction. Thus, for the values of L_1 and L_2 lies in the range in between the channel length, will not affect the TFET performance. However, if L_1 is reduced to a value closer to the tunneling junction then the performance of TFET will be changed. However, in this work the impact of metal work functions of tunneling gate and auxiliary gate is studied on the capacitive and RF performance of the device keeping the length of tunneling gate and auxiliary gate as constant.

3.3 Fabrication process flow of HD-GME-GAA-TFET

The proposed summary of fabrication process flow for HD-GME-GAA-TFET is shown in Fig. 3. The fabrication

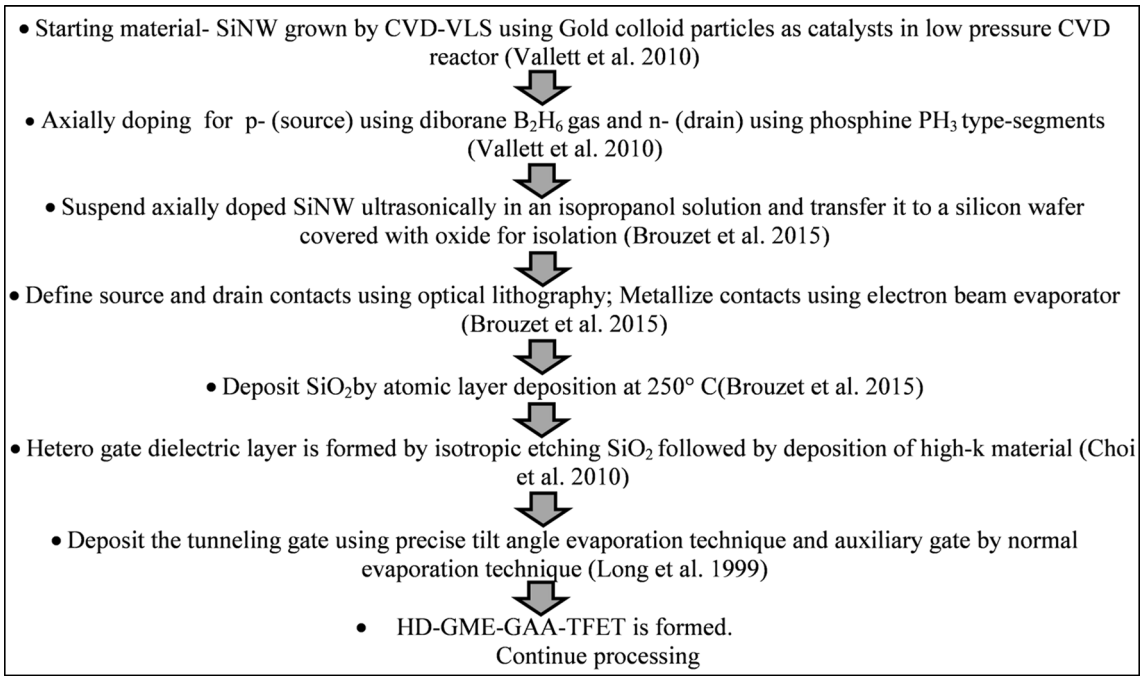

Fig. 3 Summary of fabrication process flow of HD-GME-GAA-TFET (Brouzet et al. 2015; Vallett et al. 2010)

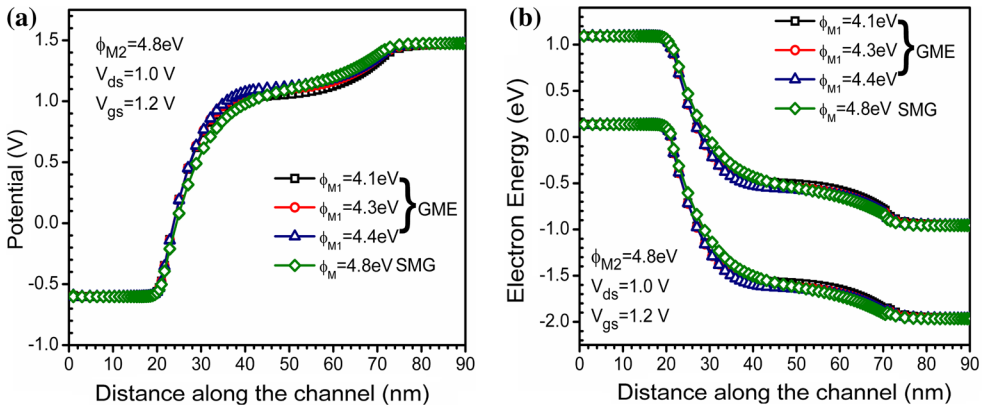

Fig. 4 **a** Surface potential profile. **b** Energy band profile along the channel of HD-GME-GAA-TFET and HD-GAA-TFET for various metal work function values at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V

feasibility of GAA-TFET has already been reported in several literatures such as (Chen et al. 2009) fabricated vertical silicon nanowire TFET, (Gandhi et al. 2011a, b) fabricated both vertical Si-nanowire n-type and p-type TFET. Furthermore, for realization of GME architecture various schemes have been reported such as tilt angle evaporation technique (Long et al. 1999), metal interdiffusion process (Polishchuk et al. 2001). Thus, the HD-GME-GAA-TFET can be fabricated using the above device design schemes, in which the benefits of HD and GME engineering scheme have been combined with GAA TFET for accomplishing improved characteristics.

4 Results and discussion

Figure 4a, b represent the surface potential and energy band profile for HD-GME-GAA-TFET and HD-GAA-TFET respectively, in the ON-state of both the devices. Along with this, the impact of metal work functions of HD-GME-GAA-TFET has also been shown. For analyzing the effect of GME, three metals (of different work functions) are used near source side (tunneling gate) keeping metal near drain side (auxiliary gate) same. It is evident from the plot of surface potential that for a tunneling gate with lower metal work function, the surface potential is higher, that is needed

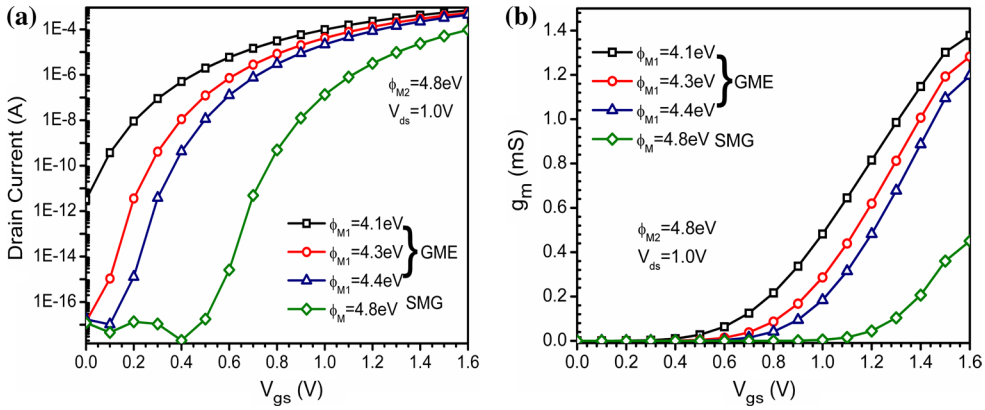

Fig. 5 **a** Transfer characteristics, **b** transconductance of HD-GME-GAA-TFET and HD-GAA-TFET for various metal work function values as a function of V_{gs}

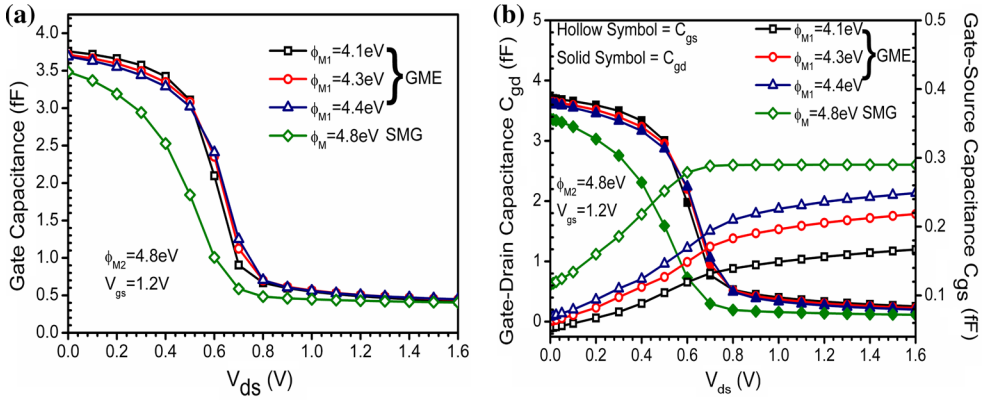

Fig. 6 **a** Gate capacitance. **b** gate-drain and gate-source capacitance of HD-GME-GAA-TFET and HD-GAA-TFET for various metal work function values as a function of V_{ds}

to enhance the band bending at the tunneling junction for achieving a high I_{ON}. In addition, the auxiliary metal with high metal work function used near drain side reduces the surface potential and thus improves the OFF-state characteristics and the ambipolar conduction. The energy band profile shown in Fig. 4b, reveals that for the presence of low metal work function near source side for the case of HD-GME-GAA-TFET, band bending at the tunneling junction increases that lowers the tunneling barrier width. This higher surface potential and lowered tunneling barrier width acquired by GME engineering scheme enhances the ON current, reduces the threshold voltage and the subthreshold swing of GAA-TFET.

Figure 5a compares the transfer characteristics of gate metal engineered TFET with single metal gate TFET of the same dimensions at a constant drain bias 1.0 V. It is evident from Fig. 5a, that I_{ON} of GME-TFET is many times greater than I_{ON} of SMG-TFET. It is clearly evident from Fig. 5a that the larger difference in metal work function (as in case 1 in comparison with case 3) leads to enhancement in I_{ON} by 2.68 times. Increase in I_{ON} is the main advantage of heterogate dielectric and gate metal engineering (Lee et al. 2012). The I_{ON} of case 4 which is the case of single metal gate (SMG) is much lower as compared to GME. The OFF-state current i.e. I_{OFF} is defined as the drain current at $V_{gs} = 0$ V and $V_{ds} = 1.0$ V. Variation of I_{OFF} for all the cases shows that I_{OFF} enhances from an order of 10^{-17}–10^{-11} A, as the metal work function difference of auxiliary and tunneling gate is increased to 0.7 eV. Thus we need to optimize the device for I_{ON}/I_{OFF} ratio for superior device performance.

An important device parameter that measures the device gain is the transconductance g_m, defined as the first order derivative of drain current w.r.t. gate voltage at a constant drain voltage. For a constant drain bias, g_m decides the current driving capability of the FET. Furthermore, higher g_m is desirable for acquiring higher gain. The transconductance g_m of HD-GME-GAA-TFET and HD-GAA-TFET are compared in Fig. 5b. It is found that g_m of HD-GME-GAA-TFET is superior in comparison with HD-GAA-TFET. The higher g_m of HD-GME-GAA-TFET is attributed to the improved driving current of HD-GME-GAA-TFET, obtained by GME architecture.

The switching speed in integrated circuits depends on the parasitic capacitances. For higher switching speed, parasitic capacitances should be as small as possible (Madan et al. 2015b). So, for the design of the circuits containing TFETs, the understanding of these capacitances is important. In this work, the reliance of parasitic capacitances of HD-GME-GAA-TFET on the drain bias, gate bias and the

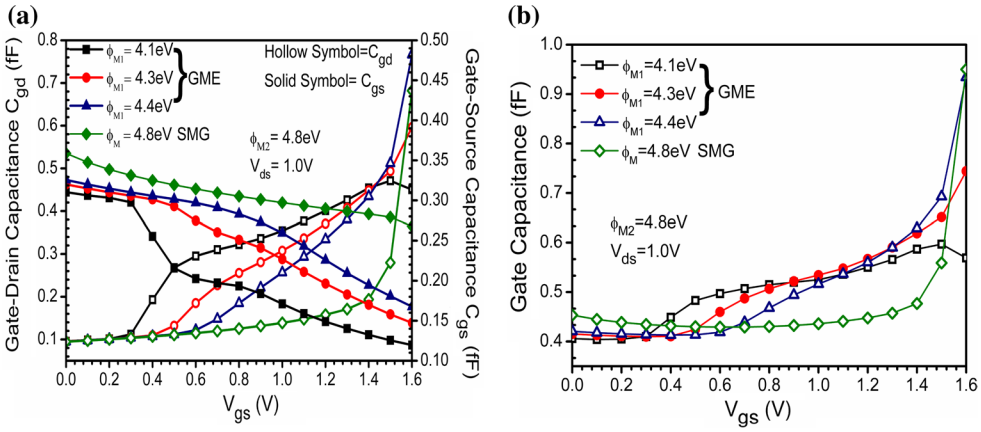

Fig. 7 **a** Gate drain and Gate-source capacitance. **b** Gate capacitance of HD-GME-GAA-TFET and HD-GAA-TFET for various metal work function values as a function of Vgs

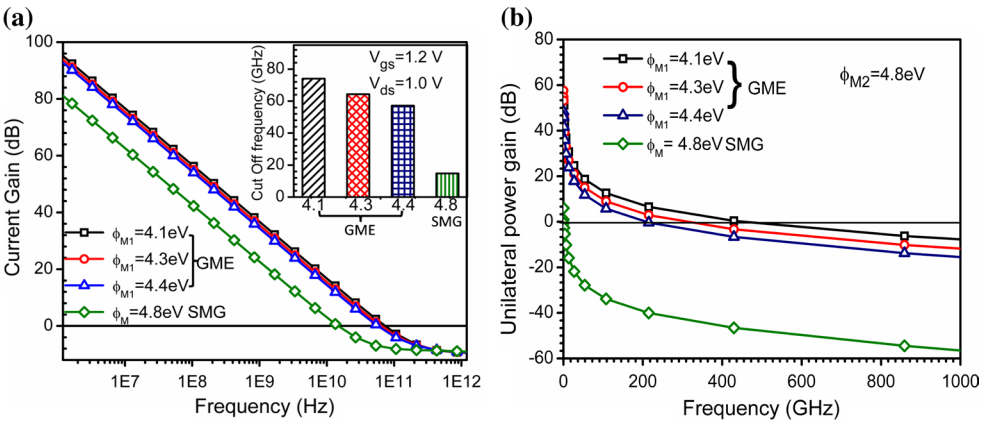

Fig. 8 **a** Current gain. **b** unilateral power gain of HD-GME-GAA-TFET and HD-GAA-TFET at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V for various metal work function values as a function of frequency

metal work function variation is studied using the physics based technology-aided design (TCAD) simulator.

In case of MOSFET, in the linear region, the C_{gg} is symmetrically apportioned between both the source and drain regions as both source and drain regions are connected to the inversion region formed underneath the gate dielectric region. But in case of TFET, only the drain is connected to inversion layer due to different inversion charge distribution and results in larger C_{gd} as compared to C_{gs} in both linear and saturation regions. As $C_{gg} = C_{gd} + C_{gs}$ so, a large fraction of C_{gg} is contributed by C_{gd} as compared to C_{gs} (Yang et al. 2010). For a constant gate bias in ON state, the formation of inversion layer starts from the drain side and an increase in drain bias pinches the inversion layer towards the source side (unlike as in case of MOSFET where pinch off occurs towards the drain side).

Figure 6a depicts the variation of gate to drain capacitance and gate to source capacitance with drain bias at a constant gate bias ($V_{gs} = 1.2$ V). As it is clearly evident that in linear region i.e. for lower drain bias, (in which the device is in on- state) the gate drain capacitance is comparatively large. As the drain bias is increased, the inversion layer shifts towards source side and hence the reduction in gate drain capacitance is obtained. Again in the region before inversion layer formation, the gate drain capacitance is more in case of gate metal engineered TFET as compared to single metal gate TFET, but for a higher drain bias, the gate drain capacitance is almost same for GME and SMG. Before inversion occurs, the gate source capacitance is very small because for lower drain bias, all the inversion charges are near the drain. As drain bias is increased, the inversion layer shifts towards the source side which leads to enhanced gate to source capacitance as clear from Fig. 6a. For GME, the gate source capacitances are small as compared to SMG. From Fig. 6a it is clear that as the difference between metal work function of GME TFET is enhanced, the gate source capacitance is reduced. Further, the order of C_{gs} are very much less than that of C_{gd} as evident from Fig. 6a. So a higher I_{ON} is obtained for gate metal engineered (GME) TFET and simultaneously the parasitic capacitances are not adversely affected, making GME a better candidate for future demands. Total gate capacitance C_{gg} which is basically equal to the sum of gate-source and gate-drain capacitance is shown in Fig. 6b. As the gate-source capacitance is very small as compared to gate-drain capacitance, so the total gate capacitance is almost same as that of gate-drain capacitance or the gate drain capacitance contributes dominantly to C_{gg}.

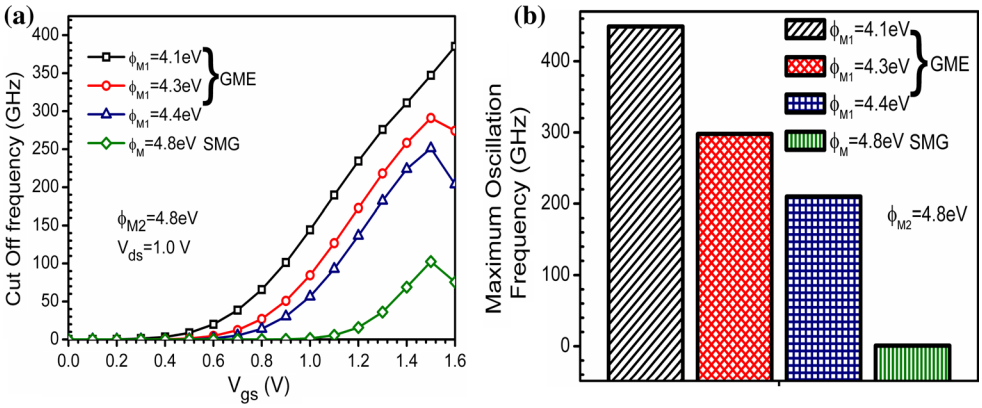

Fig. 9 **a** Cut off frequency as a function of gate bias. **b** Maximum oscillation frequency of HD-GME-GAA-TFET and HD-GAA-TFET at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V for various metal work function values

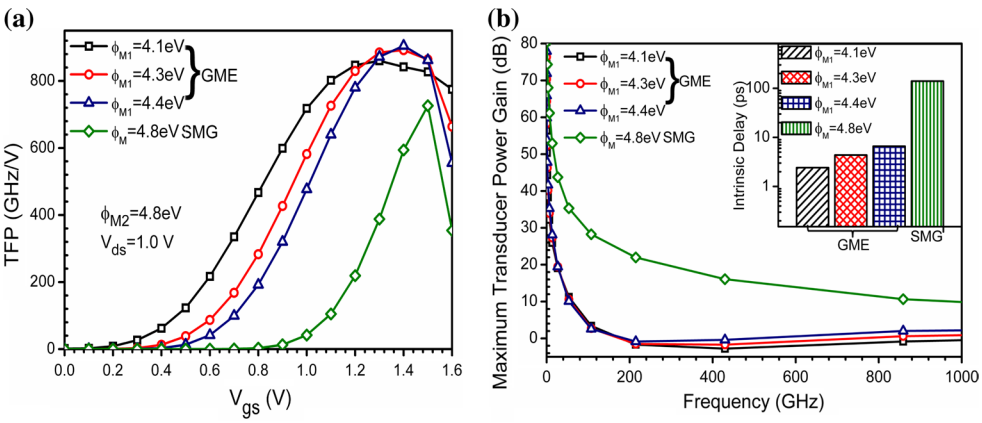

Fig. 10 **a** Transconductance frequency product at $V_{ds} = 1.0$ V as a function of gate bias. **b** Maximum transducer power gain of HD-GME-GAA-TFET and HD-GAA-TFET at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V for various metal work function values as a function of frequency. *Inset* intrinsic delay at $V_{ds} = 1.0$ V

The plot of gate to drain capacitance and gate to source capacitance of both GME and single metal gate as a function of V_{gs} at $V_{ds} = 1.0$ V is shown in Fig. 7a. The inversion layer moves from the drain side towards the source side with an increase in gate bias so the gate drain capacitance increases with gate bias at a constant drain bias. The coupling between gate and source decreases with the extension of inversion layer towards the source side. This decoupling of the source and gate results in a monotonically decrease in gate source capacitance with increase in gate bias as shown in Fig. 7a. Total gate capacitance for GME and SMG with respect to gate bias is shown in Fig. 7b. As the gate source capacitance contributes a little, so the total gate capacitance is almost same as gate drain capacitance. For higher gate bias, the parasitic capacitances are comparatively low in case of GME.

In addition, for investigation of RF performance, the RF figures of merits (FOM) are analyzed in terms of cut off frequency f_T and maximum oscillation frequency f_{Max}. Current gain and unilateral power gain are extracted for determining the values of f_T and f_{Max} respectively. Figure 8a illustrates the impact of GME and SMG on the current gain. The increase in difference between metal work function of GME leads to enhanced current gain. The cut off frequency of the device is an important parameter for RF application. The inset of Fig. 8a shows the cut off frequency f_T of all the cases. The cut off frequency plotted in the inset of Fig. 8a is extracted from the plot of current gain and is the frequency at which the current gain falls to 0 dB. It is clearly evident that the f_T of HD-GME-GAA-TFET is higher than the f_T of HD-GAA-TFET. The f_T enhances by 3.86, 4.34, and 5 times for the case 3, 2 and 1 respectively, in comparison to case 4. To analyze the high frequency performance of the device, the unilateral power gain is of prime importance. It is the highest achievable power gain. It is the gain from a device at which no reverse transmission occurs or good reverse isolation. Figure 8b shows the unilateral power gain for GME and SMG TFETs. Again with incorporation of GME, the unilateral power gain is enhanced.

Figure 9a compares f_T of GME and SMG TFET at various gate biases. f_T is increasing with increase in gate bias. The switching speed of the device depends on the f_T. It is clearly evident from Fig. 9a that as the difference between gate metal work function increases in case of GME, the cut off frequency increases, which leads to higher switching speed. Maximum oscillation frequency is a more useful FOM for microwave applications because microwave designers are typically concerned with power gain under conjugately matched conditions (Razavi 1998). Figure 9b

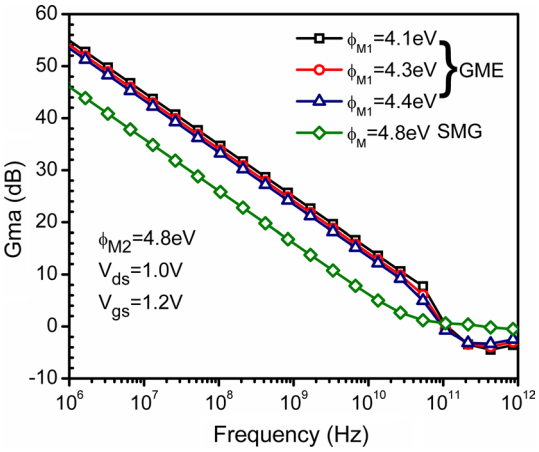

Fig. 11 Maximum available power gain of HD-GME-GAA-TFET and HD-SMG-GAA-TFET at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V

depicts the maximum oscillation frequency which is extracted from the unilateral power gain. f_{Max} is the highest frequency at which the power gain is unity. It is clear from the Fig. 9b that in case of GME, in which the metal work function difference between the tunneling and the auxiliary gate is high (case 1), the maximum oscillation frequency is almost double as compared to case 3. The f_{Max} in case of SMG is much smaller than GME.

Transconductance frequency product TFP is an important high frequency circuit design parameter. TFP is defined as the product of device efficiency g_m/I_d and f_T. TFP is used to tradeoff between power and bandwidth. As is clear from Fig. 10a, TFP is enhanced in case of GME-GAA-TFET by 1.52 times as compared to SMG-GAA-TFET. This is because of the enhancement of f_T and device efficiency with the amalgamation of GME scheme on HD-GAA-TFET. Moreover the peak of TFP is further enhanced with an increase in difference of gate metal work function difference. Further, intrinsic delay is an important figure of merit for evaluating the transistors speed. It is the reciprocal of intrinsic switching frequency f_i and is expressed as:

$$\tau = \frac{C_{gg} \times V_{dd}}{I_{ON}}$$

Where; C_{gg} is the total gate capacitance, V_{dd} is the drain voltage and I_{ON} is the saturation drain current. It is clearly evident from the bar graph shown in the inset of Fig. 10b that there is an intensive reduction in intrinsic delay with the integrity of GME engineering scheme on HD-GME-GAA-TFET as compared to HD-GAA-TFET. This reduction is caused by enhanced on-current and reduced parasitic capacitance, thus considerable reduction in intrinsic delay of the device, which further results into higher switching speed of the device (as $f_i = 1/\tau$). Moreover with an increase in gate metal work function difference in GME scheme, intrinsic delay is further reduced. As we increase the metal work function difference by 0.4–0.7 eV, the intrinsic delay is reduced by 63.34 %.

Figure 11 shows the improvement of high frequency maximum available power gain (Gma) of HD-GME-GAA-TFET over HD-SMG-GAA-TFET. This enhancement is due to the lowering of tunneling barrier width which is further a resultant of GME engineering scheme (Madan et al. 2016b), resulting into higher on current and reduced parasitic capacitances as shown in Fig. 7. Moreover with alteration of metal work function in GME scheme, such as increased metal work function difference also results into enhanced Gma, due to enhancement in drain current and reduction in parasitic capacitance at higher metal work function difference.

Under small-signal conditions, the transistor can be described by a small-signal equivalent circuit. MOSFET can be replaced by its Y-parameters equivalent circuit consisting of the four Y-parameters Y_{11}, Y_{12}, Y_{21} and Y_{22}. The Y parameters are defined under ac short-circuit conditions (either at the input or at the output). Values of Y-parameters depend on the dc bias conditions as well as on the operating frequency. At low frequencies, ac voltages and ac currents can be easily measured, but at high frequency the measurement of these parameters becomes exceptionally complicated. Then, another set of parameters scattering or S-parameters can be measured at such high frequencies. But as Y-parameters are more closely related to device physics and design, so S parameters are again converted into Y parameters. So, study of Y-parameters becomes necessary.

Y_{11} is the short circuit input admittance, Y_{22} is the short circuit output admittance, Y_{12} is the short circuit forward transfer admittance and Y_{21} is the short circuit reverse transfer admittance. Figure 12a–d compares the real and imaginary component of Y-parameters of HD-GME-GAA-TFET and HD-SMG-GAA-TFET. It is clearly evident that Y_{11} and Y_{22} are lower at low frequency and increases gradually as frequency increases, while Y_{12} and Y_{21} are higher at low frequency and decreases gradually with increase in frequency thus, giving useful information to the RF engineers.

5 Conclusion

In this work, the small signal parameters and RF performance of HD-GME-GAA-TFET such as parasitic capacitances, power gains, cut off frequency, maximum oscillation frequency, intrinsic delay and admittance parameters has been analyzed using TCAD device simulations. With

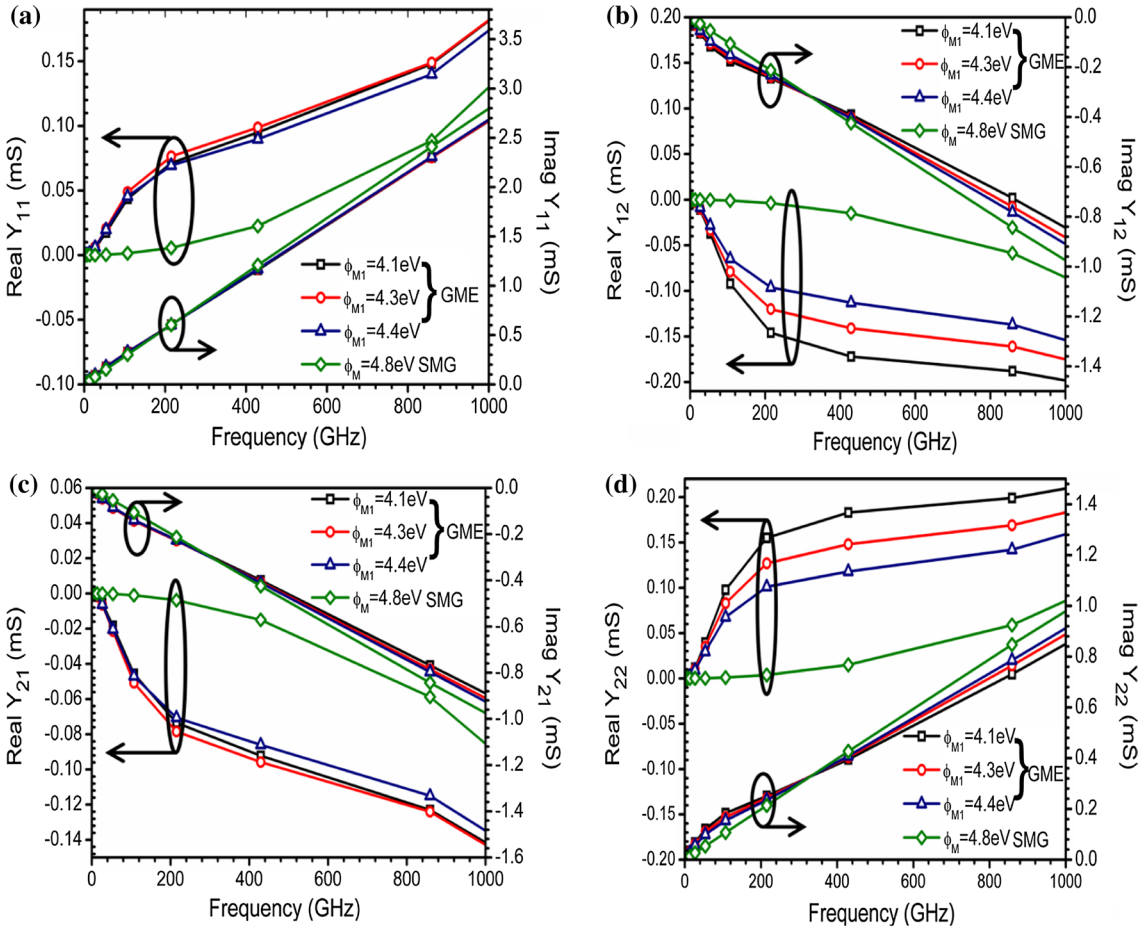

Fig. 12 Y-parameters of HD-GME-GAA-TFET and HD-GAA-TFET as a function of frequency at $V_{gs} = 1.2$ V and $V_{ds} = 1.0$ V. **a** Y_{11}, **b** Y_{12}, **c** Y_{21}, **d** Y_{22}

the implementation of GME, superior benefits of TFET are obtained. The parasitic capacitances are decreased, the cutoff frequency and the maximum oscillation frequency is manifold increased (better RF performance). Moreover it has been examined that with the amalgamation of GME scheme on HD-GAA-TFET on current is enhanced and parasitic capacitances are reduced, resulting into enhancement of numerous power gains thus makes it a suitable candidate for high frequency and microwave applications. Also the reduction in intrinsic delay and parasitic capacitances with GME architecture makes it applicable for analog and digital switching applications. In addition, the improvement in small signal Y parameters has been obtained with the GME architecture which is beneficial for the RF communication. So the HD-GME-GAA-TFET can find applications in high-switching-speed electronics.

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Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability

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***Abstract*—In this paper, we have investigated device reliability by studying the impact of interface traps, both donor (positive interface charges) and acceptor (negative interface charges), present at the Si/SiO_2 interface, on analog/RF performance and linearity distortion analysis of heterogeneous-gate-dielectric gate-all-around tunnel FET (HD-GAA-TFET), which is used to enhance the tunneling current of TFET. Various figures of merit such as cutoff frequency f_T, maximum oscillation frequency $f_{\max}$, transconductance frequency product, higher order transconductance coefficients (g_{m1}, g_{m3}), VIP2, VIP3, IIP3, IMD3, zero crossover point, and 1-dB compression point have been investigated, and the results obtained are simultaneously compared with a gate-all-around TFET (GAA-TFET). Simulation results indicate that HD-GAA-TFET is more immune toward the interface trap charges present at the Si/SiO_2 interface than the GAA TFET and hence can act as a better candidate for low power switching applications. All simulations have been done on an ATLAS device simulator.**

***Index Terms*—Band-to-band tunneling (BTBT), heterogeneous dielectric (HD), interface trap charges (ITCs), interface trap layer, parasitic capacitance, tunneling FET (TFET).**

I. Introduction

TFET works on band to band tunneling principle and have a subthreshold swing (SS) smaller than 60 mV/dec (overcome the limit of SS of MOSFET). Due to lower power dissipation, TFET has gained a lot of attraction and has become an attractive candidate for ultralow power applications. Further, TFET is immune to short channel effects and has very low OFF current, making it suitable for low power applications. However, TFET suffers from low ON state current (because of limited rate of tunneling of carrier), lower than the ITRS requirement. This makes it unsuitable for analog applications. Abundant techniques have been explored for resolving this issue such as using a smaller band gap material in the source region such as germanium [1], hetero gate dielectric TFET [2], double gate architecture [3], gate to source overlap [4], gate to drain underlap [5], dual material gate [6], n-pocket doping tunnel FET [7]. Other drawback of TFET is ambipolarity (conduction in both the directions) [8]. Many techniques were introduced to resolve this issue such as hetero gate dielectric [2], asymmetric source/drain doping [9] and hetero junction TFET [10].

The device reliability issue is always a major concern. During the device fabrication process, the process induced, stress induced and radiation induced damage results in conception of interface trap charges (ITC). It is known that the interface states causes reduction in device reliability and lifetime [11], [12]. Few works on the tunnel FET reliability have been reported yet [1], [13]–[15]. The interface defects which is attributed to the unsaturated fourth bond present at the interface, have energy level lying in the energy band gap of the silicon (unlike in the conduction and valence band). Electrons and holes that are present in these levels cannot move freely (or are localized) due to the larger distance between the neighboring interfacial trivalent silicon atoms. A donor type interface trap can act as a positive localized charge (when it is empty) or neutral localized charge (when it is filled with an electron). An acceptor type interface trap can act as a negative localized charge (when it is filled with an electron) or neutral localized charge (when it is empty). Donor traps usually lie near above the valence band and acceptor traps usually lies near below the conduction band.

In case of tunnel FET, higher electric field near the tunneling junction (the source channel junction) is needed for lowering of the tunneling barrier width but on the counterparts of lowering the tunneling barrier width, this high transverse field results into the generation of interface traps (donor and acceptor) and hence the localized charges (both positive and negative). Apart from the high electric field, hot carrier stress (HC) and positive bias temperature instability (PBTI) are also attributed to the generation of ITC [16]. The band to band tunneling rate is proportional to $\exp(-\mathrm{A/E_y})^6$, hence BTBT rate is very sensitive to electric field. But the presence of interface traps at the Si/SiO_2 interface results into degradation of electric field along the channel length at the tunneling junction and thus results in degradation of tunneling current and the analog performance of the device.

A lot of work has already been done to study the device reliability of MOSFET owed by the ITC. But there is a need to estimate the performance degradation due to the interface traps present at the Si-SiO_2 interface in TFET as the basic working principle of TFET is entirely different from that of the MOSFET. In this paper, the effect of ITC on two devices HD-GAA-TFET and GAA-TFET with cylindrical geometry has been compared.

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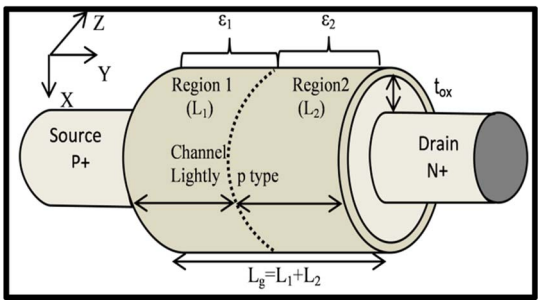

Fig. 1. Simulation structure of n-type heterogeneous-gate-dielectric GAA-TFET (HD-GAA-TFET).

II. Device Analysis and Simulation

Fig. 1 shows the simulation structure of HD-GAA-TFET. For HD-GAA-TFET region-1 consists of dielectric constant $\varepsilon_1 = 21$ HfO_2 (near the source) and region 2 consists of $\varepsilon_2 = 3.9$ (SiO_2) (near the drain) and for GAA TFET $\varepsilon_1 = \varepsilon_2 = 3.9$ (SiO_2). Silicon is used as source, drain and channel material. The radius (R), channel length $(L_g = L_1 + L_2)$, and gate oxide thickness $(t_{\rm ox})$ is 10 nm, 50 nm (10 nm + 40 nm) and 3 nm, respectively for both the cases HD-GAA-TFET and GAA-TFET. The source is p^+ type doped $(1 \times 10^{20}\ {\rm cm}^{-3})$, body is lightly p type doped $(1 \times 10^{16}\ {\rm cm}^{-3})$ and drain is n^+ doped $(5 \times 10^{18}\ {\rm cm}^{-3})$. To constrain the ambipolarity effect, (tunneling at drain and channel junction) source and drain are doped asymmetrically [9]. The optimum value of gate metal work function has been chosen for better OFF state characteristics. Metal work function is 4.3 eV for both the devices.

In this paper, to study the device reliability issue attributed to the interface charges, the effect of interface traps has been transmuted, into its equivalent positive localized charges (acceptor) and negative (donor) localized charges. The value of N_f is chosen on the basis of various experimental and simulation studies previously published incorporating the process damage, radiation damage and hot carrier damage resulting in trap density of $10^{11} - 10^{13}\ {\rm cm}^{-2}{\rm eV}^{-1}$ [17], [18]. To investigate the minimum change we have chosen positive and negative charge density as $N_f = \pm 1 \times 10^{12}\ {\rm cm}^{-2}$. Further, the effect of interface traps at the Si-SiO_2 interface is considered only near the source side for 10 nm, due to the presence of high transverse electric field at the tunneling junction. Although the interface traps are also present at the interface of dielectrics in HD GAA TFET and will be absent in case of GAA TFET, but in present work we have only considered the ITCs along the channel length at the silicon and oxide interface. The main reason for neglecting the ITCs at the HfO_2/SiO_2 interface is that in case of TFETs mainly the tunneling junction and the drain junction affects the device behavior majorly so in this work we haven't considered the ITCs at the HfO_2/SiO_2 interface [19]. INTERFACE statement is used during simulation to define the density of interface fixed charges and there position present at the interface of Si-SiO_2. The distribution of interface charges is assumed to be uniform during the entire stimulation. The device reliability (to study the behavior of ITCs on device performance) is studied in terms of analog, RF and linearity figure of merits.

III. Model Validation

A. Simulation Methodology

All simulations have been performed using the ATLAS device simulator [20]. The models invoked during simulation are concentration and field dependent mobility model, Shockley-Read-Hall for carrier recombination, non-local band to band tunneling, band gap narrowing and Fermi Dirac statistics. The most important model for Tunnel FET simulations is the band-to-band tunneling (BTBT) model. Non-local models have a more physical basis and don't depend on the electric field at the individual mesh points in the simulated device structure, but rather on band diagrams calculated along cross-sections through the device. According to BBT.NONLOCAL, the tunneling happens through 1D slice, at the tunnel junction, where each slice and the tunnel junction are perpendicular to each other. These slices are parallel to themselves. Fermi Dirac statistics, the use of Fermi-Dirac statistics are essential to account for certain properties of very highly doped (degenerate) materials. Such as reduced carrier concentrations in heavily doped regions (statistical approach). As we are using heavily doped source and drain, so Fermi Dirac statistics is used. For higher doping $(> 10^{18}\ {\rm cm}^{-3})$ experimental work has shown that the p-n product in silicon becomes doping dependent. As the doping level increases, a decrease in the bandgap separation occurs. Both the numerical methods Gummel (decoupled) together with Newton's (Fully coupled) has been incorporated to mathematically solve the carrier transport equation.

B. Calibration

Before simulating the device structure, the simulation models have been calibrated with the already published results [21]. To calibrate the models the GAA TFET has been designed with the same device parameters as shown in ref [21]. To calibrate the Non-local BTBT model, the tunneling masses were tuned from their default values i.e. me.tunnel $= 0.322\ {\rm m}_o$ and mh.tunnel $= 0.549\ {\rm m}_o$ to make it best fit with the experimental data. Where; mo is the rest mass of electron. The adjusted value of me.tunnel $= 0.22\ {\rm m}_o$ and mh.tunnel $= 0.52\ {\rm m}_o$. Inset of Fig. 2(a) shows the transfer characteristics of the extracted data from the reference and results obtained from the simulations. The results so obtained are in close proximity, thus validates the model parameters during the simulations.

IV. Results Analysis

A. Impact of ITC on Analog and RF Performance

Fig. 2(a) shows the effect of donor type traps (positive interface charges), acceptor type traps (negative interface charges) and absence of traps or interface charges on nonlocal band to band electron tunneling rate for both the aforementioned devices (GAA-TFET and HD-GAA-TFET). It is evident from the Fig. 2(a) that due to the presence of acceptor traps (negative interface charges), the band to band tunneling (BTBT) rate is decreased in both the devices and the donor traps (positive interface charges) increases the BTBT rate. This increase (decrease) is mainly attributed to the lowering (enhancing) of the flat band voltage $(V_{\rm fb})$, which in turn decreases (increases) the

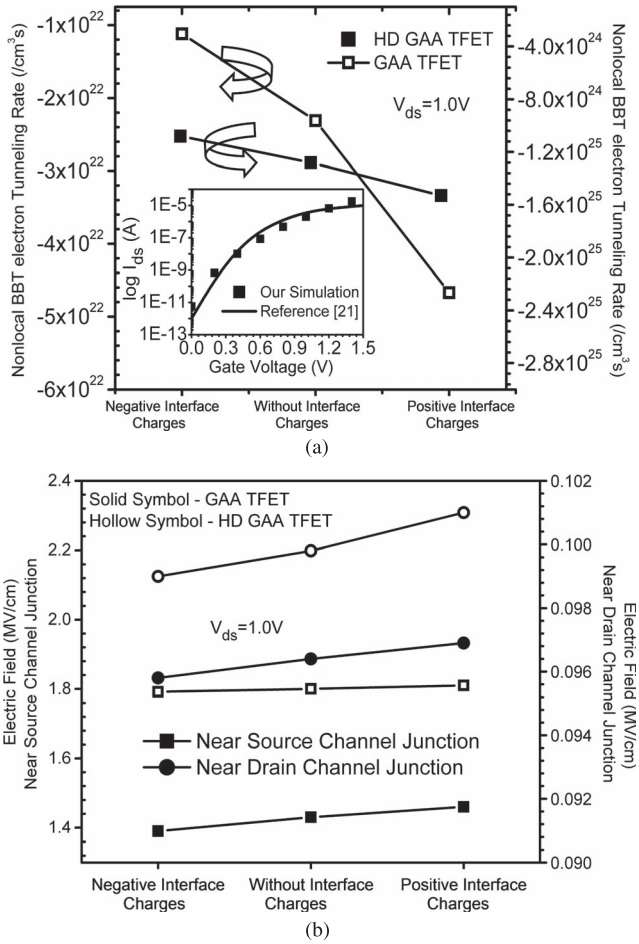

Fig. 2. (a) Nonlocal band-to-band tunneling rate at source–channel (tunneling) junction. (Inset) Calibration with the published result, $I_{\rm ds}-V_{\rm gs}$ characteristics of the 200-nm gate length SiNW-TFET at $V_{\rm ds} = 1.2$ V, $t_{\rm ox} = 4.5$ nm, and Diameter $= 70$ nm. (b) Electric field near source and drain side of HD-GAA-TFET and GAA-TFET for acceptor, donor, and absence of ITC.

band bending of conduction and valence band. This enhanced (reduced) band bending also results into lowering (higher) of tunneling barrier width. The increase in BTBT rate results into higher tunneling current. The BTBT is almost 1000 times greater in case of HD GAA TFET as compared to GAA TFET. It should be noted that as $\Delta V_{\rm fb} = {\rm qN_f}/C_{\rm ox}$, where $\Delta V_{\rm fb}$ is the change in flat band voltage, q is the electronic charge, N_f is the charge density and $C_{\rm ox}$ is the oxide capacitance. In case of HD GAA TFET, oxide capacitance in region 1 is increased thereby reducing the $\Delta V_{\rm fb}$. Thus BTBT is less influenced by the interface trap charges in case of HD GAA TFET in comparison with GAA TFET. The effect of interface traps on electric field near source and drain side for both the devices is shown in Fig. 2(b). The electric field is higher at the tunneling junction (near source side) for all the cases. In case of HD GAA TFET, the dielectric near source side is replaced by a high-k and the dielectric near drain is kept same. So the effect of HD is concentrated at the tunneling junction only and field near drain side is very less affected by the application of HD. Again due to higher (lower) band bending, the electric field is enhanced (reduced) for the donor (acceptor) traps near the source channel junction. Electric field near drain side is also

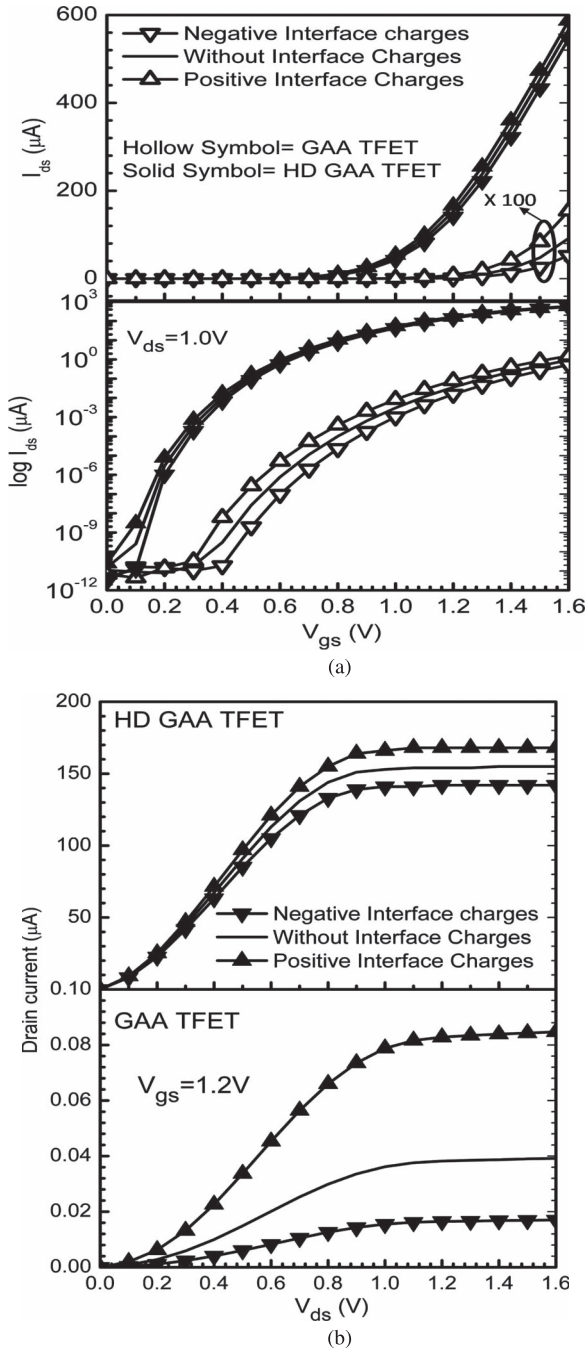

Fig. 3. (a) Transfer characteristics and (b) output characteristics of HD-GAA-TFET and GAA-TFET as a function of gate-to-source voltage for acceptor, donor, and absence of ITC.

enhanced (reduced) for positive (negative) interface charges for both the mentioned devices. The impact of interface charges on transfer-characteristics of both the devices is shown in Fig. 3(a). As mentioned before, the donor (acceptor) traps increases (decreases) the band bending. This increase (decrease) results in higher (lower) band to band generation rate, which finally leads to increase (decrease) in ON current. The donor (acceptor) interface traps increases (decreases) the ON current by 117% (57%) and 8.6% (8.2%) in case of GAA TFET and HD GAA TFET respectively. Furthermore the effect of interface traps is less in case of HD GAA TFET as compared to GAA TFET.

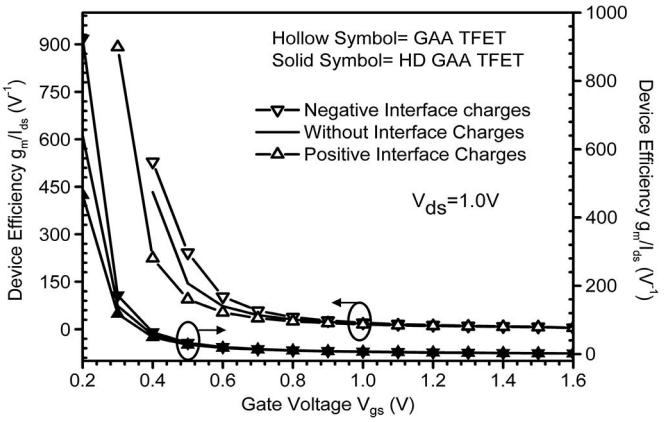

Fig. 4. Impact of ITCs on device efficiency of HD-GAA-TFET and GAA-TFET.

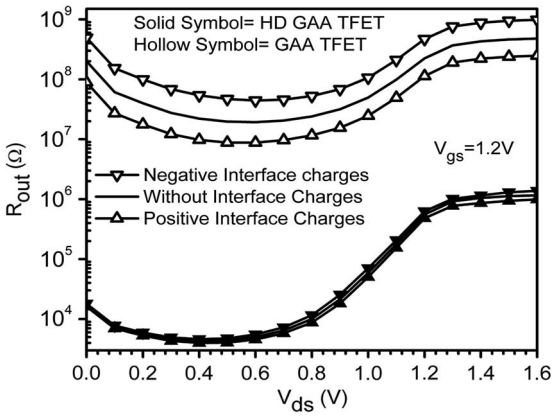

Fig. 5. Impact of ITCs on output resistance of HD-GAA-TFET and GAA-TFET.

This results into better device reliability in case of HD GAA TFET as compared to GAA TFET. The effect of interface traps (both donor and acceptor) on output characteristics of both the devices is shown in Fig. 3(b). It is clearly shown that the donor (acceptor) traps increases (decreases) the tunneling current. Again the effect of ITCs is comparatively less in case of HD GAA TFET as compared to GAA TFET. Thus, HD GAA TFET is more reliable in comparison to GAA TFET. Another vital device design parameter is transconductance to current ratio $(g_m/I_{\rm ds})$ or the device efficiency, which gives the measure of efficiency to convert current (power) into transconductance (speed). The impact of ITCs on device efficiency is shown in Fig. 4. Enhancement (reduction) in drain current and transconductance [see Fig. 3(a) and Fig. 9, respectively] due to positive (negative) ITCs, results into decrease (increase) in device efficiency for both the devices. The decrease (increase) in device efficiency due to presence of positive (negative) ITCs is mainly attributed to larger deviations in drain current in comparison to transconductance. The impact of ITCs on output resistance or the drain resistance with respect to the $V_{\rm ds}$ is shown in Fig. 5. $R_{\rm out}$ is numerically equal to inverse of drain conductance g_d, higher $R_{\rm out}$ is desirable for better analog performance in order to achieve higher voltage gain, $A_{\rm v} = g_m * R_{\rm out}$. It is clearly depicted in the graph that $R_{\rm out}$ of HD GAA TFET is many orders lower than $R_{\rm out}$ of GAA TFET. But the higher transconductance in case of HD GAA TFET (see Fig. 9) counterbalance the degradation of $R_{\rm out}$ and hence will stabilize the value of

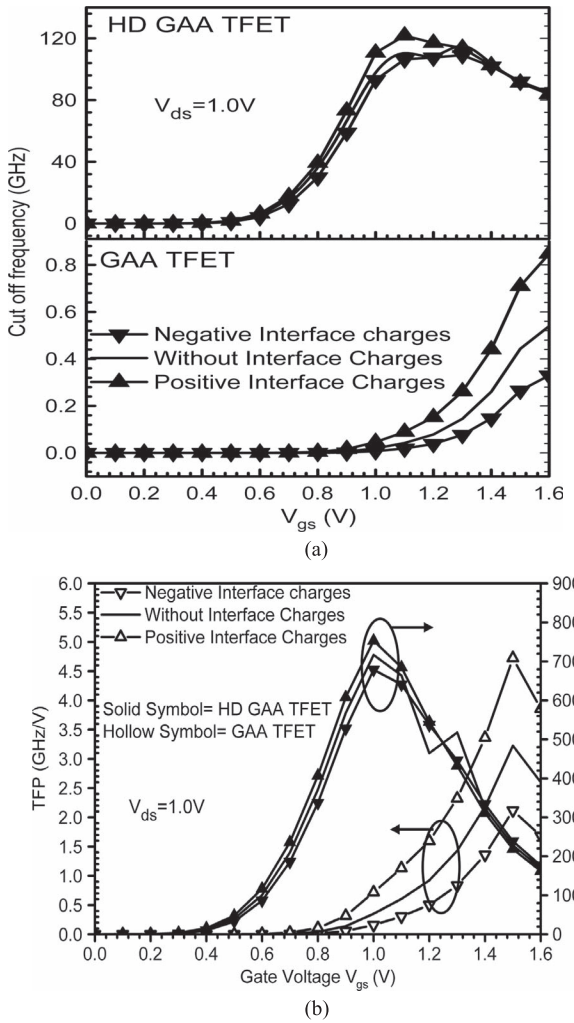

Fig. 6. (a) Cutoff frequency and (b) transconductance frequency product (TFP) as a function of gate voltage of HD-GAA-TFET and GAA-TFET.

intrinsic gain of the device. Moreover, the presence of acceptor (donor) ITCs results into increase (decrease) of $R_{\rm out}$, but again the increase/decrease in case of HD GAA TFET is very much less in comparison with GAA TFET.

After analyzing the effect of trap charges on analog performance, we have investigated their influence on high frequency performance of both the devices. Numerous RF figures of merits (FOMs) and high frequency (HF) gains such as cutoff frequency f_T, maximum oscillation frequency $f_{\rm Max}$, transconductance frequency product (TFP), unilateral power gain and maximum transducer power gain have been evaluated. f_T is a very vital parameter for evaluating and designing the RF performance of the device. f_T is also defined as the frequency at which short circuit current gain drops to unity (or the input and output currents are equal). f_T of both the devices has been presented in the Fig. 6(a). Numerically the cut off frequency is given by

$$f_T = \frac{g_m}{2\pi(C_{\rm gs} + C_{\rm gd})} \tag{1}$$

where; $C_{\rm gs}$ and $C_{\rm gd}$ are gate-to-source and gate-to-drain capacitance respectively. It is clearly evident that f_T of HD GAA TFET is several orders of magnitude greater than GAA TFET. Because of the increase (decrease) in transconductance due to

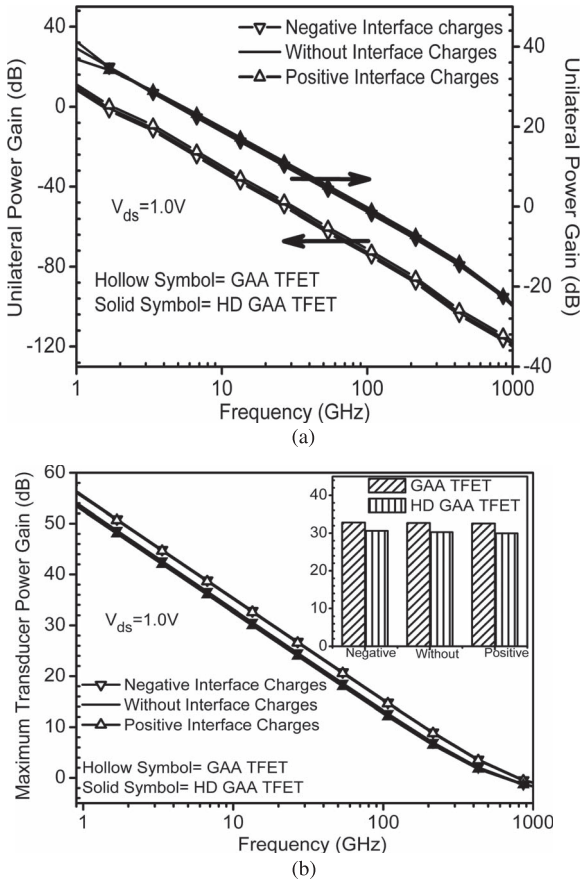

Fig. 7. (a) Unilateral power gain and (b) maximum transducer power gain as a function of frequency of HD-GAA-TFET and GAA-TFET.

donor (acceptor) traps, the f_T of both the devices increases (decreases) as shown in Figs. 6(a) and 9. At $V_{\rm gs} = 1.2$ V, donor (acceptor) traps results into an increase (decrease) of 93% (51%) and 12% (3%) of f_T for GAA TFET and HD GAA TFET respectively. A unique FOM for high frequency performance is the transconductance frequency product (TFP), given in Eq. (2) is plotted in Fig. 6(b) for donor, acceptor and absence of ITCs

$$\text{TFP} = \left(\frac{g_m}{I_{\rm ds}}\right) \times f_T. \tag{2}$$

TFP is basically the product of device efficiency and f_T. It represents a trade-off between power and bandwidth and is used for moderate to high speed designs [22]. It is clear from Fig. 6(b) that TFP of HD GAA TFET is almost 10 decades higher w.r.t TFP of GAA TFET. Further, TFP increases linearly before inversion region for both the device and after attaining a maximum value, it starts decreasing for the higher gate bias (after the inversion region is formed). Due to the presence of donor (acceptor) interface traps, TFP increases (decreases) in both the devices. At $V_{\rm gs} = 1.0$ V, the increase (decrease) in case of GAA TFET and HD GAA TFET is by 104% (54%) and 5% (5%) respectively. Further, unilateral power gain has been extracted for determining the value of maximum oscillation frequency $(f_{\rm max})$ and is defined as the power gain with no reverse transmission or nearly very minute reverse transmission. $F_{\rm Max}$ is the frequency at which the Mason's unilateral power gain drops to unity (corresponds to 0 dB). Fig. 7(a) shows the effect

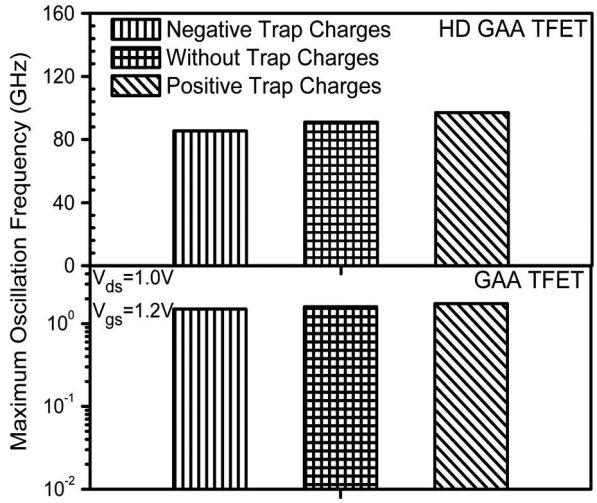

Fig. 8. Maximum oscillation frequency of HD-GAA-TFET and GAA-TFET.

of ITCs on unilateral power gain on both the devices. With the application of HD on GAA TFET, unilateral power gain is enhanced. The positive (negative) ITCs enhances (reduces) the unilateral power gain in case of GAA TFET, and the presence of high-k dielectric near source reduces (enhances) the unilateral power gain for positive (negative) ITCs. Moreover the effect of ITCs is very less in case of HD GAA TFET in comparison with GAA TFET. Maximum transducer power gain $(G_{\rm MT})$ is basically a measure of efficacy of the two ports. In case of a two port network $G_{\rm MT}$ is defined as the ratio of average power delivered to the load by a source to a maximum available power from the source. Fig. 7(b) shows the effect of ITCs on $G_{\rm MT}$ of both HD GAA TFET and GAA TFET. Faintly degradation in the performance of GMT in case of HD GAA TFET has been obtained in comparison to GAA TFET at high frequency beyond 100 GHz. The effect of ITCs is negligible less for frequency greater than 10 GHz, but at lower frequencies increase (decrease) in GMT due to negative (positive) ITCs has been found.

Fig. 8 compares the maximum oscillation frequency $f_{\rm max}$ of both the devices for the donor, acceptor and absence of trap charges acquired from unilateral power gains. It is clearly evident from both the bar graphs that $f_{\rm max}$ for HD GAA TFET is 49.2, 34.17, and 23.62 times greater than $f_{\rm max}$ of GAA TFET for positive, without and negative ITCs. For HD GAA TFET $f_{\rm max}$ increases (decreases) by 1.02% (2.97%) for acceptor (donor) trap charges. Thus, results indicate that with the application of HD engineering, analog as well as high frequency performance of TFET is enhanced, making it a better candidate for high switching speed electronics application.

B. Effect of ITCs on Linearity and Distortion Performance

Along with the high speed, modern communication systems must give assurance for minimum signal distortion to determine the suitability of the device for analog and RF applications. If the linearity is not maintained by a device, then the nonlinear parts at the output may swamp out the desired signal. For better linearity of a system, transconductance should be a constant over the input voltage but transconductance of a MOSFET as well as TFET depends on the input voltage, this reflects the

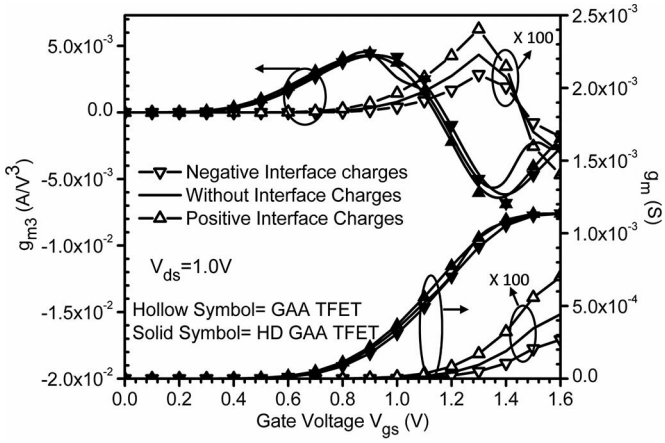

Fig. 9. g_m and g_{m3} as a function of gate bias of HD-GAA-TFET and GAA-TFET for various types of ITCs.

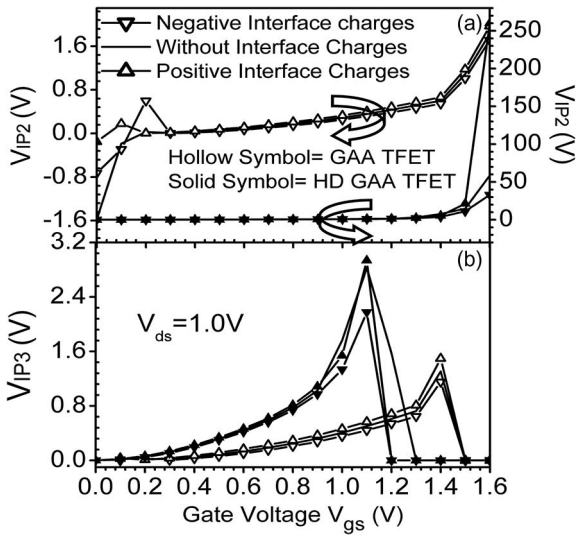

Fig. 10. (a) VIP2 and (b) VIP3 as a function of $V_{\rm gs}$ of HD-GAA-TFET and GAA-TFET for various types of ITCs.

nonlinear behavior of a MOSFET as well as TFET. In this work, effect of ITCs on linearity and RF distortion of TFET are analyzed by metrics $V_{\rm IP2}$, $V_{\rm IP3}$, IMD3, IIP3, g_{m3}, 1 dB compression point and zero-crossover point. Which are defined as:

$$\text{VIP2} = 4 \times \frac{g_{m1}}{g_{m2}} \qquad \text{VIP3} = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}} \tag{3}$$

$$\text{IIP3} = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_s} \quad g_{mn} = \frac{\partial^n I_{ds}}{\partial V_{gs}^n} \tag{4}$$

$$\text{IMD3} = \left[\frac{9}{2} \times (\text{VIP3})^3 \times g_{m3}\right]^2 \times R_s \tag{5}$$

$$\text{1-dB compression point} = 0.22\sqrt{\frac{g_{m1}}{g_{m2}}} \tag{6}$$

where $R_{\rm s} = 50\ \Omega$ for most of the RF applications and $V_{\rm IP2}$ represents the extrapolated input voltage at which first second-order harmonic voltages are equal; $V_{\rm IP3}$ represents the extrapolated input voltage at which first and third-order harmonic voltages are equal; and IIP3 represents the extrapolated input power at which first and third-order harmonic powers are equal.

For improved linearity performance and low distortion operations, these FOMs should be as high as possible [23]. Transconductance g_m is basically the gain of the device and it also decides the current driving capability of the device. The peak value of the curve ($g_m = g_{m|\max}$) gives the optimum bias point for which the device gives the maximum gain (used in case of amplifiers). Fig. 9 shows the impact of interface charges on transconductance of both the devices. As it is clearly shown that the presence of donor (acceptor) traps increases (decreases) the transconductance. Also at $V_{\rm gs} = 1.2$ V, transconductance is enhanced (reduced) by 94 % (51%) and 13% (2.4%) for donor (acceptor) traps w.r.t the case when there are no interface traps for GAA TFET and HD GAA TFET respectively. Thus, with the application of HD onto TFET, the device reliability is also improved along with the analog performance. The higher order transconductance coefficient g_{m3} is plotted with respect to $V_{\rm gs}$, as shown in Fig. 9. For better linear performance the amplitude of g_{m3} should be as low as possible. g_{m3} is mainly responsible for the distortion of fundamental amplitude via signals in the adjacent bands or the intermodulation distortions. It is clearly evident from Fig. 9 that peak of the g_{m3} is lower in case of HD GAA TFET and also shifted towards lower gate bias. Further the variation against ITCs are also less in case of HD GAA TFET.

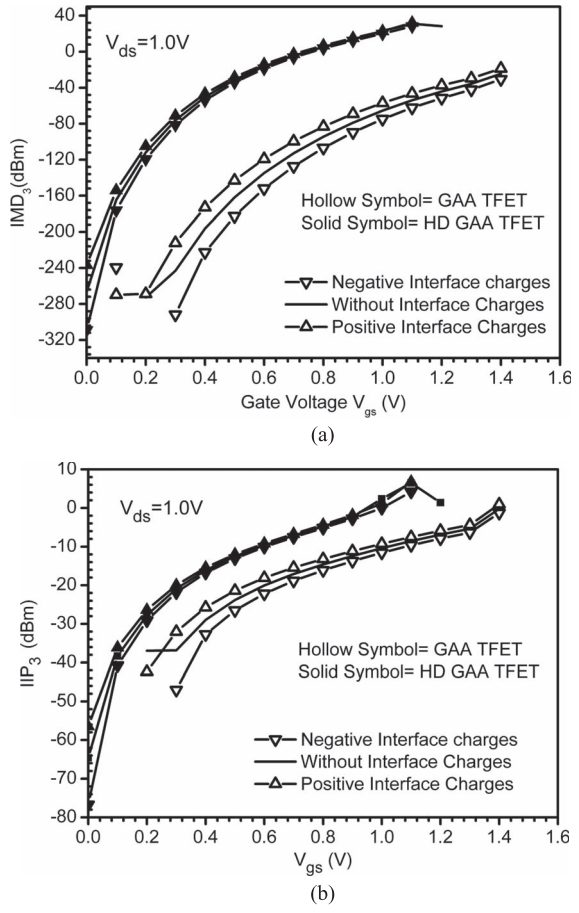

Fig. 11. (a) IMD3 and (b) IIP3 as a function of gate bias of HD-GAA-TFET and GAA-TFET for various types of ITCs.

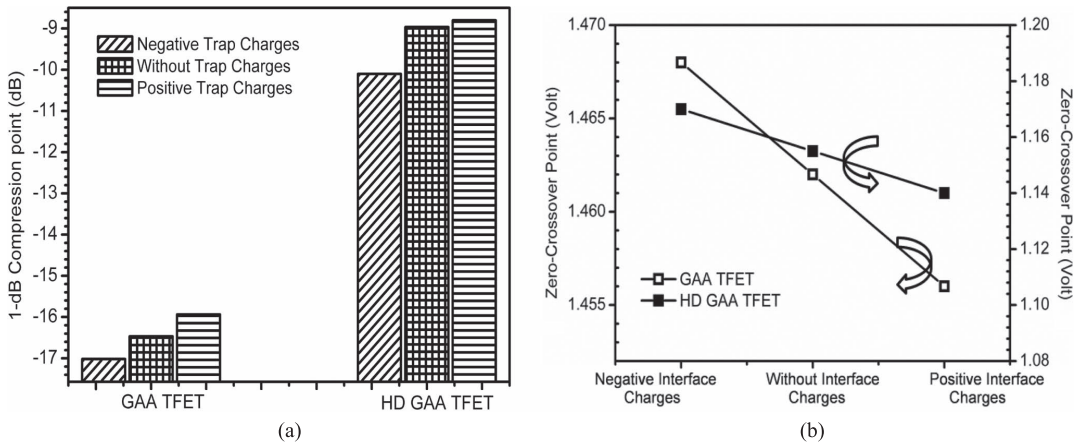

Fig. 12. Comparison of the (a) 1-dB compression point and the (b)zero crossover point as a function of gate bias of HD-GAA-TFET and GAA-TFET for various types of ITCs.

Fig. 10(a) and (b) shows the effect of ITCs on $V_{\rm IP2}$ and $V_{\rm IP3}$ with respect to the variation of $V_{\rm gs}$ at a constant $V_{\rm ds} = 1.0$ V for GAA TFET and HD GAA TFET. For high linearity and low distortion $V_{\rm IP2}$ and $V_{\rm IP3}$ should be as high as possible. The amplitude of $V_{\rm IP3}$ is higher for HD GAA TFET in comparison with GAA TFET, which shows that along with better analog performance (as shown in previous work [24]) HD engineering exhibits high linearity and low distortion in comparison with conventional TFET. Moreover the peak of the $V_{\rm IP3}$ is also shifted towards the lower gate bias; it implies that a lower gate drive is required to preserve linearity with the amalgamation of HD engineering onto TFET. Further, the peak value of VIP3 increases (decreases) with the presence of donor (acceptor) ITCs. $V_{\rm IP2}$ is used to determine the distortion characteristics for different DC parameters. As evident from graph that with the application of HD, $V_{\rm IP2}$ is enhanced, showing a better linearity of the device.

Fig. 11(a) and (b) illustrates the variation of third order intercept input power (IIP3) and third order intermodulation distortion power (IMD3) with $V_{\rm gs}$. The effect of ITCs is also included in the result. When the third order nonlinearity term is equal to the fundamental term in signal power, is called the IIP3. For high linearity and lower distortion operation, IIP3 should be as high as possible and IMD3 should be as low as possible.

As reported earlier in many papers, IIP3 increases with an increase in gate bias for both aforementioned devices. As evident from Fig. 11(b) that HD GAA TFET has higher IIP3 in comparison with GAA TFET, which indicates the potential of HD for better linearity and low distortions analog and RF applications. Moreover better immunity against ITCs is gained in case of HD GAA TFET as compared to GAA TFET. 1-dB compression point (P1 dB) is defined as the input power which causes the gain to drop by 1-dB (this can be considered as the onset of the distortion). P1 dB gives the estimate of maximum input power, after which the gain of an amplifier decreases. Fig. 12(a) presents the impact of ITCs on 1-dB compression point for both the devices. Thus, because of reduced signal distortion and high transconductance in case of HD GAA TFET, P1 dB is also enhanced in case of HD GAA TFET in comparison with GAA TFET as demonstrated in Fig. 12(a). Further, there is an increase (decrease) in P1 dB due the presence of positive (negative) ITCs. The nonlinearity possessed by g_{m3} can be suppressed by selecting the optimum biased point; determined by the zero crossover point (ZCP) of g_{m3}. Fig. 12(b) shows that a higher $V_{\rm gs}$ is needed in case of GAA TFET to achieve better linearity, in comparison with HD GAA TFET. Moreover for positive (negative) ITCs, ZCP shift towards lower (higher) gate voltages, which is desirable for better linearity and low distortion.

V. Conclusion

In this work, the impact of interface traps donor (positive interface charges) and acceptor (negative interface charges) is studied and is compared with the case when the interface traps are not present in terms of analog, RF and linearity analysis of the device through extensive simulations. The effect of interface charges on both GAA-TFET and HD-GAA-TFET is studied and it is found that HD-GAA-TFET is much immune to the ITCs present at the Si-SiO_2 interface in comparison to the GAA TFET. Moreover it is found that HD engineering improves the results in terms of analog, RF and linearity metrics of the device. The improvement in transconductance, with the amalgamation of HD results into enhancement of the high frequency gain of the device. It is observed that a shift of flatband voltage and thus the band bending in the channel, results into alteration of tunneling barrier width which eventually modifies the transfer characteristics and hence superior performance is obtained in terms of TFP, 1-dB compression point and zero crossover point. As these ITCs always exists in a real device, thus study of performance degradation due to these interface charges is always needed so that device can be optimized accordingly.

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Palladium Gate All Around - Hetero Dielectric -Tunnel FET based highly sensitive Hydrogen Gas Sensor

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ABSTRACT

The paper presents a novel highly sensitive Hetero-Dielectric-Gate All Around Tunneling FET (HD-GAA-TFET) based Hydrogen Gas Sensor, incorporating the advantages of band to band tunneling (BTBT) mechanism. Here, the Palladium supported silicon dioxide is used as a sensing media and sensing relies on the interaction of hydrogen with Palladium-SiO_2-Si. The high surface to volume ratio in the case of cylindrical GAA structure enhances the fortuities for surface reactions between H_2 gas and Pd, and thus improves the sensitivity and stability of the sensor. Behaviour of the sensor in presence of hydrogen and at elevated temperatures is discussed. The conduction path of the sensor which is dependent on sensors radius has also been varied for the optimized sensitivity and static performance analysis of the sensor where the proposed design exhibits a superior performance in terms of threshold voltage, subthreshold swing, and band to band tunneling rate. Stability of the sensor with respect to temperature affectability has also been studied, and it is found that the device is reasonably stable and highly sensitive over the bearable temperature range. The successful utilization of HD-GAA-TFET in gas sensors may open a new door for the development of novel nanostructure gas sensing devices.

1. Introduction

Hydrogen gas (H_2) participates as a clean energy in fuel cells and energy carrier and thus acts as a strong candidate to replace fossil fuels that are at the edge of exhaustion. But the smaller size of H-atoms attributes to the risk of leakage and thus creates a need for the detection of H_2 gas for fuel monitoring. Moreover, H_2 is an extremely flammable gas as it can burn at a concentration of 4% in air and have a large window (4–75% v/v H_2) of flammability in comparison with methane, ethane, natural gas, etc. Thus, H_2 gas sensors have perpetual demand for automotive, environmental monitoring, petroleum refining process, and medical industries [1,2]. These gas sensors mainly work as transducer devices that detect the presence of H_2 gas, measure its concentration, and produce an electrical signal that is further calibrated with the magnitude of H_2 gas concentration. Out of various gas sensors such as catalytic sensors, semiconductor sensors, electrochemical sensors and infrared sensors; semiconductor sensors have numerous benefits and can be used for an extensive range of gases including toxic, combustible, etc. Further, the low cost, high sensitivity, stability, fast response time, wide operation temperature range and reliability make it highly applicative for detection of variety of gases [3–5].

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Palladium (Pd) has a very high selectivity towards H_2 gas. Pd based gas sensor rely on the fact that after absorption of H_2 gas, a chemical species called palladium hydride is formed, which has a comparatively high electrical resistance. Apart from high selectivity, out of several catalytic metals, the sensitivity of Pd for hydrogen is highly appreciable because of the sites located at Pd–SiO_2 interface (in case of MOS architecture based FETs such as MOSFET and TFETs) along with the surface reactions, participating in the catalytic reactions. It is also reported that at room temperature and atmospheric pressure, Pd can absorb up to 900 times its volume of hydrogen [6,7]. When H_2 molecules interact with Pd surface, the H_2 molecules dissociate on the surface of metal to form atomic hydrogen and some of the dissociated H-atoms diffuse through the Pd surface. The probability of dissociation of H_2 on Pd is almost unity, or H_2 dissociates very meritoriously on Pd. Within few nanoseconds, the diffused H-atoms reaches to the interface of Pd and SiO_2 or the H-atoms gets adsorbed at the SiO_2–Pd interface. The H-atoms reaching the metal-insulator interface gets polarised and forms surface dipole layer. This dipole layer in turns modulates the work function, conductivity, etc. and thus affects the device electrical properties. The high sensitivity of Pd for H_2 is mainly attributed to the great polarisation of H-atoms at the Pd–SiO_2 interface rather than the large diffusion of H-atoms through Pd [8,9].

The key focus of earlier research work had been to enhance sensitivity and selectively (for a particular gas) and is done by either exploring suitable sensitive films or by various device design engineering schemes. For high sensitivity and selectivity, numerous films such as metal compounds [10–12], polymers [13], organic compounds [14], hydrated salts [15] and catalytic metals [16–18] were used. In the novel device design, dual gate MOSFET; nanowire MOSFET, conventional TFET, etc. has already been taken into consideration. Till now in order to fulfill the requirement of sensing H_2 gas, silicon nanowire based H_2 gas sensor was proposed by Cao A et al. [2]. Further, to obtain appreciable sensitivity, the surface of SiNW FET sensor was functionalised with catalytic layers of Pd nanoparticles by Bongsik Choi et al. [19], for enhancing the selectivity and thus the sensitivity. Moreover, various gas sensors using metal oxide nanowires such as SnO_2, ZnO and In_2O_3 have been reported previously. A lot of work in the field of semiconductor gas sensors has been carried out with MOSFETs. But there is a need to investigate TFET as a gas sensor, as TFET is highly suitable for low power digital CMOS applications. The novel properties of TFET such as low leakage current, lower subthreshold swing (lower than 60mV/decade); immunity against short channel effects makes it an outstanding candidate for low power devices in the semiconductor industry [20–23]. Apart from these remarkable features, TFET suffers from few shortcomings such as low I_{ON}, ambipolar current and high threshold voltage. So to overcome these drawbacks, various engineering schemes were introduced such as hetero gate dielectric engineering, gate metal work function engineering, heterojunction devices, gate drain underlap/overlap TFETs, etc. In heterogate-dielectric (HD) scheme, a high-k material is locally inserted (near the source side) in the gate dielectric to enhance the ON-current [24]. The presence of high-k dielectric results into a higher band bending due to increasing surface potential (at a constant gate bias) [25–27]. This boosted band bending leads to reduction in tunneling barrier width, which further increases the generation rate and hence, on-current. In this work, the concept of palladium gate based Tunnel FET for H_2 gas sensing applications has been proposed. In addition, hetero gate dielectric engineering scheme and gate all around architecture has also been incorporated to further enhance the sensitivity of the hydrogen gas sensor.

2. Structural descriptions and simulation methodology

Table 1 indicates the structural parameters of all four devices based gas sensor which are compared for the improved sensitivity. For GAA-TFET and HD-GAA-TFET, cylindrical geometry is considered. In the case of HD-GAA-TFET, the channel consists of two regions; region 1 (near the source $L_1 = 20$ nm) and region 2 (near the drain $L_2 = 30$ nm). Region 1 consists of high-k dielectric (optimized value is 21 corresponds to HfO_2) and region 2 is of low-k dielectric (SiO_2, $k = 3.9$) whereas, in the case of GAA TFET, the entire channel consists SiO_2. In both the cases, radius (R) is 10 nm. To reduce ambipolarity effect, source and drain are doped asymmetrically in the case of TFET. Uniform doping profile has been considered in each case. The source and drain junctions are abruptly doped for an effective BTBT and the interface of high-k and SiO_2 is taken as abrupt. (see Fig. 1)

All simulations have been performed using ATLAS device simulator. The models activated during simulation of TFET Gas Sensor are as follows: concentration and field dependent mobility model, Shockley-Read-Hall for carrier recombination, non-local BTBT, band gap narrowing and Fermi-Dirac statistics. For conventional MOSFET based gas sensor, models invoked for simulation are: - Shockley-Read-Hall for carrier recombination, Lombardi CVT mobility model, concentration and field dependent mobility model and boltzmann transport statistics. The most important model for Tunnel FET simulations is the band-to-band tunneling (BTBT) model. A non-local model is chosen in this work instead of local model, to incorporate the effect of electric field at each point in the tunneling path. In local models such as Kane's model the triangular barrier

Table 1
Default structural parameters for all the devices based gas sensors.

Device	Parameters			
	Channel length (nm)	Source doping (cm^{-3})	Drain doping (cm^{-3})	Channel/Substrate doping (cm^{-3})
Conventional MOSFET	50	$n^+ - 10^{19}$	$n^+ - 10^{19}$	$p - 10^{16}$
Conventional TFET		$p^+ - 10^{20}$	$n^+ - 5\times10^{18}$	$p - 10^{16}$
GAA TFET		$p^+ - 10^{20}$	$n^+ - 5\times10^{18}$	$p - 10^{16}$
HD-GAA- TFET	$50 = 20 + 30$ $L = L_1 + L_2$	$p^+ - 10^{20}$	$n^+ - 5\times10^{18}$	$p - 10^{16}$

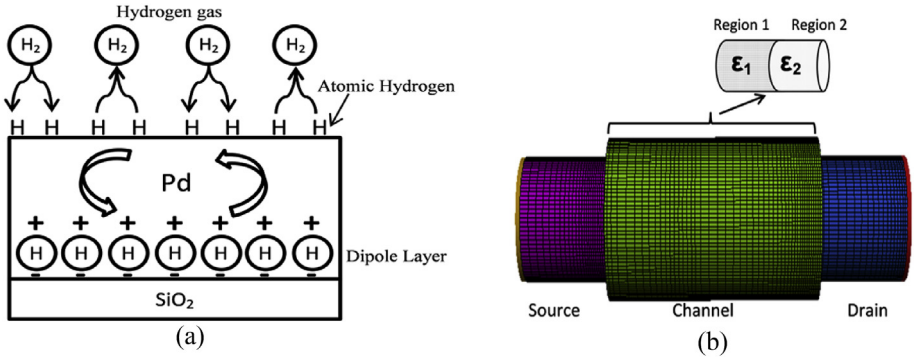

Fig. 1. (a) Schematic of adsorption of H_2 gas molecules, diffused through Pd films and formation of dipoles at the Pd–SiO_2 interface. (b) Meshed structure of HD-GAA-TFET gas sensor.

approximation of energy bands results into constant electric field at the entire tunneling path. But the non-local BTBT model have a more physical basis as the field changes at each point in the tunneling path. Both the numerical methods- Gummel (decoupled) together with Newton's (Fully coupled) have been incorporated to solve mathematically the carrier transport equation [28]. Pd with work function 5.1eV is used as the catalytic metal gate and gate oxide thickness is 2 nm for all the cases. The entire analysis has been performed at room temperature. For TFET, the calibration of non-local BTBT model is done with the experimental data [29]. The tunneling masses were tuned from their default values i.e. me.tunnel = $0.322m_o$ and mh.tunnel = $0.549m_o$ to make it best fit with the experimental data. Where; mo is the rest mass of electron. The adjusted value of me.tunnel = $0.22m_o$ and mh.tunnel = $0.52\ m_o$. The calibrated results are shown in Fig. 2(a). The fabrication feasibility of proposed gas sensor i.e. HD-GAA-TFET gas sensor is shown in Table 2. In addition, the gate all around TFET has already been fabricated by various researchers such as Chen et al., [29] fabricated vertical silicon nanowire TFET, Gandhi et al., [32,33] fabricated both vertical Si-nanowire n-type and p-type TFET. Therefore the proposed gas sensor can be fabricated using the above device design schemes, in which the advantages of hetero gate dielectric architecture has been incorporated onto GAA TFET for attaining higher sensitivity. In addition, the work function of the gate metal has been altered to incorporate the corresponding effect of change in hydrogen gas pressure as reported in Ref. [34].

3. Sensitivity analysis of proposed gas sensor

Sensitivity (S) is defined as;

$$S = \frac{I_{After\ gas\ adsortion} - I_{Before\ gas\ adsortion}}{I_{Before\ gas\ adsortion}}$$

Where; $I_{before\ gas\ adsorption}$ and $I_{after\ gas\ adsorption}$ are the drain current before the gas adsorption and the drain current after gas adsorption. In Fig. 2(b), sensitivity is plotted as a function of gas pressure for conventional MOSFET, conventional TFET, GAA-TFET, and HD-GAA-TFET. It is observed that the sensitivity of either of the TFET is higher in comparison with to conventional MOSFET over the entire pressure range.

The improved sensitivity in case of TFET is mainly attributed to the fact that TFET overcomes the limitation of subthreshold swing, which is limited to 60mV/decade in MOSFET. This limited SS of MOSFET bounds the sensitivity of the device as is clearly evident from Fig. 2. At a pressure of 1×10^{-10} Torr, the sensitivity of conventional TFET is 626 times greater with respect to conventional MOSFET. With the application of GAA structure, the sensitivity is further enhanced by almost three times in comparison to conventional TFET. It is due to the enhanced gate controllability of cylindrical GAA geometry. Further, it is observed that at a pressure of $1e^{-10}$ Torr, the sensitivity of HD-GAA-TFET is 3.5×10^4 times, 56 times and 30 times enhanced in comparison to the conventional MOSFET, conventional TFET, and GAA-TFET respectively. Thus, the amalgamation of HD scheme onto GAA architecture further improves the sensitivity. Enhanced sensitivity with the application of hetero gate dielectric scheme is mainly due to the higher band bending at the tunneling junction, and thus enhancement in the BTBT rate of electrons and drain current of the device is achieved. The reason for enhanced sensitivity from conventional TFET to GAA-TFET is due to higher surface to volume ratio of cylindrical architecture that enhances the probability of diffusion of H-atoms (which are dissociated) through the Pd, and hence increases the number of dipoles formed at the Pd–SiO_2 interface, thereby enhancing sensitivity of the design as a sensor.

3.1. Impact of temperature

In addition to the properties of the semiconductor, surface reactions between gas and catalytic metal are also dependent on temperature. So there is a need to study the effect of temperature in order to investigate the stability of the gas sensor. The

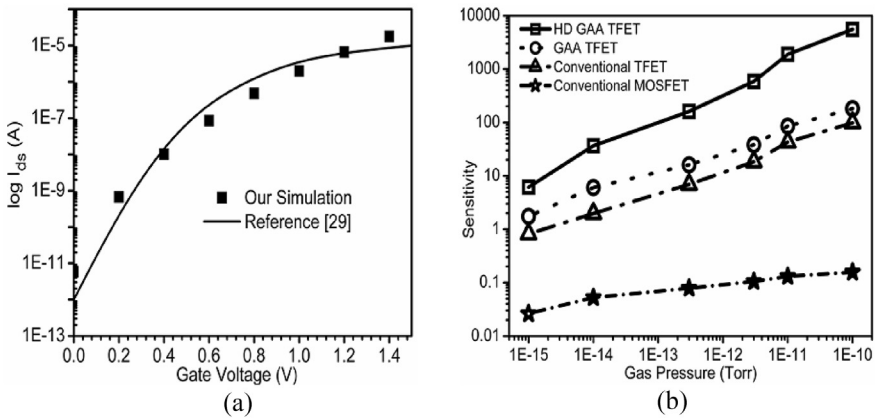

Fig. 2. (a) Calibration with the published result, transfer characteristics of 200 nm gate length SiNW-TFET at $V_{ds} = 1.2$ V, $t_{ox} = 4.5$ nm, Diameter = 70 nm. (b) Sensitivity comparison of conventional MOSFET, conventional TFET, GAA-TFET and HD-GAA-TFET as a function of gas pressure.

Table 2
Summary of Process Flow for HD-GAA-TFET Implementaion [30,31].

Starting material- SiNW Synthesized by • Au-catalyzed VLS method in LPCVD reactor • Silane as Si source gas, Trimethylboron (TMB) for p-type (Boron) and phosphine (PH_3) for n-type (Phosphorous) dopant sources. [30]
Axially doping of SiNW • Abrupt switching from TMB to second dopant PH3 during VLS growth- abrupt p-n junction. • P segment is grown first to avoid radial deposition of p-type shell along the length of SiNW. [30]
Thermal oxidation of SiNW • Dilute hydrofluoric acid (HF) – to etch the native oxide. • Wet etching – to remove Au Nanoparticles (used for the VLS growth of SiNW). • Thermal oxidation using Dry O_2 – at 800°C. [30]
Hetero gate dielectric layer is formed by etching SiO_2 followed by deposition of high-k material. [31]
Electron beam lithography and electron beam evaporation - to define and metallizing source and drain contacts [29]
Electron beam lithography and metal deposition-to define metal gate. [29]
Continue processing

results are studied only for HD-GAA-TFET as it is highly sensitive as evident from Fig. 2. Moreover, for stable operation of a sensor, the sensor should be least affected by the temperature. It is clear from Fig. 3 that at low pressure, the sensitivity is least affected by temperature but by an increase in pressure, the effect of temperature is comparatively large. Overall, the sensor has an endurable stable response to H_2 gas over an extensive temperature range. With an increase in temperature, the H_2 coverage over the catalytic metal (Pd) will decrease, and thus leads to a reduction in sensitivity. Moreover, the effect of temperature at constant pressure is plotted in the inset of Fig. 3, which illustrates that at low pressure, the sensitivity is less dependent of temperature.

3.2. Impact of radius

As the conduction path of the device in case of a cylindrical GAA MOSFET/TFET is mainly affected by the radius of the channel, there is a need to study the effect of radius on the sensitivity of proposed gas sensor. The effect of the radius of silicon pillar has been analyzed by taking three different radii such as 5 nm, 10 nm and 15 nm as shown in Fig. 4. As we reduce the

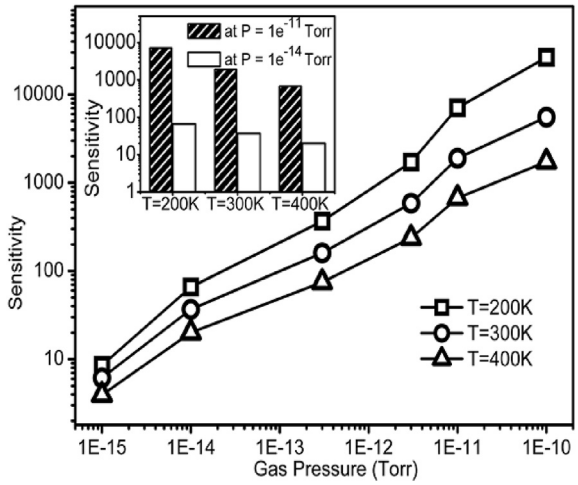

Fig. 3. Sensitivity comparison of HD-GAA-TFET as a function of gas pressure at various temperatures. Inset: - Sensitivity at constant pressures values at temperature = 200 K, 300 K and 400 K for HD-GAA-TFET.

radius from 10 nm to 5 nm, the sensitivity of the sensor reduces considerably by many orders. The reduction in sensitivity is mainly attributed to the reduced probability of surface reactions at the palladium surface (because of the reduction in surface area) with the hydrogen gas molecules. Moreover, the increase in channel radius from 10 nm to 15 nm does not enhance the sensitivity of the proposed sensor considerably. It is because the higher radius of the sensor enhances the surface area but on the other side, it reduces the gate controllability over the channel. So the results at 10 nm radius can be measured as optimized for a gas sensor with superior sensitivity.

4. Static performance analysis for proposed gas sensor

4.1. Impact of temperature

After investigating the sensitivity of the sensor, the effect of temperature on basic static performance parameters of sensor such as BTBT of electrons, threshold voltage and subthreshold swing is evaluated. Fig. 5(a–b) show the BTBT rate of electrons, threshold voltage and subthreshold swing of the HD-GAA-TFET based H_2 sensor. It is clearly shown in Fig. 5(a), that the BTBT rate is higher when gas is present, in comparison to the case when no gas molecules are there. In addition, for low pressure, less number of hydrogen-atoms are diffused through the Pd-gate, resulting in a lesser number of dipoles formations at the Pd–SiO_2 interface. Thus, comparatively less band bending will take place in the channel, and more tunneling barrier width is obtained, resulting in lowering of BTBT rate. Further, as the gas pressure increases, more number of H-atoms are diffused through the Pd surface and hence, enhances the number of dipoles formed at the Pd–SiO_2, thereby lowering the barrier width at the tunneling junction and resulting in enhanced BTBT rate. Further, as the temperature increases, the BTBT rate of electrons increases, because increase in temperature changes the properties of the semiconductor as well as the reaction rate between the gas and catalytic metal. Fig. 5(b) shows the effect of temperature on the threshold voltage and subthreshold swing of HD-GAA-TFET gas sensor. When no H_2 gas molecules are present, or the dipoles at the Pd–SiO_2 interface are not formed, the threshold voltage of the sensor is comparatively large. It is because of the lower BTBT rate of electrons when the gas is absent, as shown in Fig. 5(a). Further, as the pressure of the gas increases, the threshold voltage of the sensor decreases, because of the aforementioned reason. Lastly, the effect of temperature and gas pressure is studied on the SS of HD-GAA-TFET H_2 gas sensor. It must be noted that the SS of HD-GAA-TFET gas sensor has overcome the fundamental limit of the MOSFET, i.e. limitation of 60mV/decade, for entire temperature range and at any gas pressure. The SS increases with an increase in gas pressure which can be understood by the previously mentioned reasons. Moreover, with an increase in temperature, the SS of the sensor increases. Thus, there is a trade-off between improved sensitivity and improved static performance at high temperatures.

4.2. Impact of radius

After studying the effect of temperature, effect of channel radius of cylindrical GAA structure at constant gas pressures has been studied on the static performance of HD-GAA-TFET H_2-gas sensor. Effect of channel radius on BTBT rate of electrons for three cases can be seen in Fig. 6(a). It is clearly shown that with reduction in channel radius, the BTBT rate enhances significantly. This rise in BTBT rate of electrons is mainly attributed to higher band bending at lower channel radius, which enhances the probability of tunneling of electrons from the valence band of the source to conduction band of the channel, and

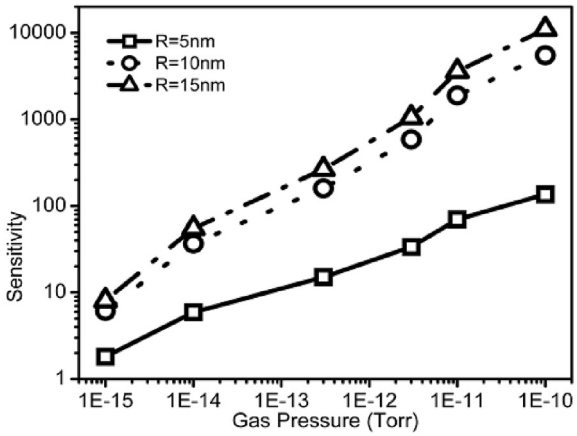

Fig. 4. Sensitivity comparison of HD-GAA-TFET as a function of gas pressure at a different radius.

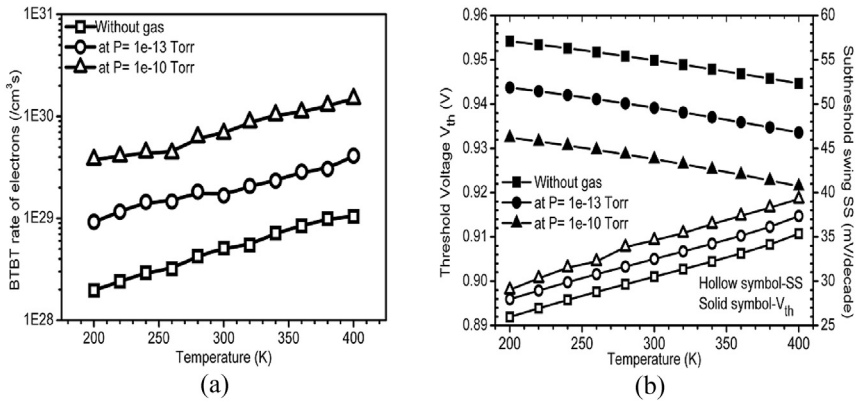

Fig. 5. Effect of temperature variations on (a) BTBT rate of electrons, (b) threshold voltage and subthreshold swing of HD-GAA-TFET gas sensor with radius R = 10 nm at constant gas pressures.

thus the BTBT rate of electrons. Moreover, it is illustrated that an increase in gas pressure results in remarkable enhancement in BTBT. As the pressure of the gas increases, more band bending occurs at the tunneling junction and thus results into an increase of BTBT rate of electrons at different radii. The effect of gas pressure and channel radius on the threshold voltage and subthreshold swing has also been plotted in Fig. 6(b). The increase in BTBT rate of electrons with pressure reduces the threshold voltage of the sensor, as higher BTBT rate of electrons turns the device ON at lower gate voltage. Further, the

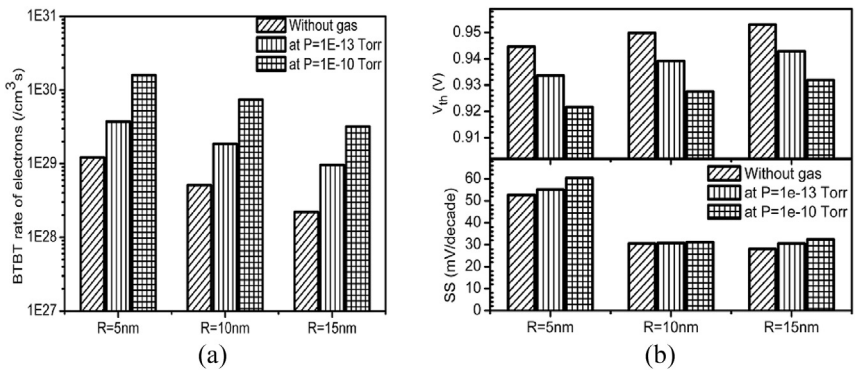

Fig. 6. Effect of radius variations on (a) band to band tunneling rate, (b) threshold voltage and subthreshold swing of HD-GAA-TFET gas sensor at T = 300 K and at constant gas pressures.

threshold voltage is higher for higher channel radius at any gas pressure. There is an increase (decrease) in SS with an increase in gas pressure (channel radius) respectively, because of the aforementioned reasons.

5. Conclusion

HD-GAA-TFET H_2 gas sensor unites the advantages of BTBT of electrons in case of tunnel FET along with hetero gate dielectric gate all around and provides substantially high sensitivity in comparison to conventional MOSFET, conventional TFET, GAA-TFET towards H_2 gas detection. Along with the high sensitivity, HD-GAA-TFET based H_2 gas sensor also has tolerable stability over wide temperature variations. Results have shown that for a radius of 10 nm, the sensor can be optimized in terms of high sensitivity. The stability of sensor with respect to temperature affectability has also been studied, and it is found that the device is reasonably stable over the bearable temperature range. After analysing the stability and sensitivity of the sensor, the temperature affectability and impact of radius has been considered on static performance parameters of the sensor such as BTBT rate of electrons, subthreshold swing and threshold voltage. This highly sensitive HD GAA TFET based hydrogen gas sensor may fulfill the everlasting demand for automotive, environmental monitoring, petroleum refining process, and medical industries.

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Applied Physics A
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Gate drain-overlapped-asymmetric gate dielectric-GAA-TFET: a solution for suppressed ambipolarity and enhanced ON state behavior

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Abstract The goal of this work is to overcome the major impediments of tunnel FET such as the inherent ambipolar current (I_{AMB}) and the lower ON current (I_{ON}). To suppress the I_{AMB}, gate drain overlap (GDO) engineering scheme has been incorporated over the cylindrical gate all around TFET (GAA-TFET). However, to enhance the I_{ON}, heterogate dielectrics (HD) are used in the gate oxide region. Results indicate that an appreciably reduced I_{AMB} and significantly enhanced I_{ON} has been obtained with the amalgamation of GDO and HD, respectively, onto GAA-TFET. Further, the effect of GDO length (L_{ov}) has also been studied. Quantitative analysis of ambipolarity factor "α" reveals that at large L_{ov}, "α" improves. It is found that GDO degrades the high-frequency (HF) performance such as cutoff frequency (f_T) of the device, because of the enhanced parasitic capacitances. To surpass the deterioration at HF caused by GDO, the dielectric over GDO region has been altered, and it has been analyzed that by inserting a material of low-dielectric constant ($k = 1$) and parasitic capacitances of the device reduces, resulting into enhancement in f_T. Moreover, the low-k dielectric inserted over L_{ov} reduces the I_{AMB} supplementary, along with enhanced f_T. Suppressed I_{AMB} and enhanced f_T of GDO–HD–GAA-TFET with low-k dielectric over L_{ov} make it adequate for application in HF and digital circuitry.

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1 Introduction

Lower subthreshold swing, lower OFF current, and immunity against short channel effects (SCEs) of tunnel field effect transistor (TFET) have marked it as one of the possible substitute devices for low-power applications. TFET uses different current conduction mechanisms (other than MOSFET), i.e., band-to-band tunneling (BTBT) of electrons from valence band of source to conduction band of channel other than thermionic emission of carriers over the barrier as in case of MOSFET. The presence of higher tunneling barrier width at the source channel junction (tunneling junction) for low gate bias results into lower I_{OFF}. Moreover, the intrinsic BTBT mechanism of electrons provides immunity against SCEs. The absence of thermionic emission delimits the TFET from thermal limit of 60 mV/decade on subthreshold swing (SS) (fundamental limit of MOSFET) [1–4]. In spite of these advantages, TFET has few shortcomings such as lower I_{ON} (caused by lower tunneling rate of electronics) and ambipolar behavior making it unsuitable for practical applications. Various techniques has been already proposed for enhancing the I_{ON} [5, 6], and for reducing the I_{AMB} [7, 8].

Ambipolarity is an intrinsic behavior of TFET that refers to the conduction for both positive and negative gate biases at a constant drain bias. In ambipolar region, conduction of holes (electrons) dominates for p-type (n-type) behavior of TFET. Ambipolarity is a serious issue for TFET. Although the ambipolar effect has been used for sensing application in [9], the ambipolar effect of the device limits its application for digital inverters. Schottky barrier (SB) transistors also suffer from the ambipolar conduction. But the solution to reduce ambipolarity for SB transistors is comparatively simple as to choose the appropriate contacts for source and drain [10]. In case of TFET, the ambipolarity is due to the

lowering of barrier width at the drain channel junction for negative gate bias. Various engineering schemes has been reported up to now to suppress the ambipolar current of TFET up to now such as: (a) heterogate dielectric [5, 11], (b) gate drain underlap or short gate [6], (c) heterojunction TFET [8], (d) asymmetric source/drain doping [7, 12], and (e) gate drain-overlapped TFET [13, 14].

In this work, cylindrical gate all around (GAA) architecture has been used that offers better device performance over their planar equivalents. GAA architecture with circular geometry provides confined volume body and excellent electrostatic control over channel and consequently boosts the tunneling probability that leads to improved I_{ON} [15]. In addition, gate drain overlap (GDO), asymmetric source/drain doping, and heterogate dielectric engineering scheme (HD) have been amalgamated onto GAA-TFET. GDO and asymmetric source/drain doping reduces the ambipolar current and HD enhances ON current of the device.

This paper is organized as follows: Sect. 2 demonstrates the device structure, simulation models, and calibration results. Section 3 consists of results and discussion, and Sect. 4 summarizes the result. Section 3 is composed of three subsections, i.e., 3.1 that shows the comparative analysis of GAA-TFET, GDO–GAA-TFET, HD–GAA-TFET, and GDO–HD–GAA-TFET, 3.2 that shows the effect of L_{ov} of GDO–HD–GAA-TFET, and 3.3 showing the improvement in HF parameters of GDO–HD–GAA-TFET has been analyzed.

2 Device structure and simulation models

The schematic cross-sectional view of the entire device architectures [i.e., GDO–HD–GAA-TFET (a), GAA-TFET (b), GDO–GAA-TFET (c), and HD–GAA-TFET (d)] considered in this work are shown in Fig. 1a–d. The device structure parameters and their values are stated in Table 1. Drain is intentionally lesser doped than source to reduce the tunneling at drain channel junction for negative gate bias and thus the ambipolarity effect [16]. All simulations have been performed using the ATLAS device simulator [17]. The models activated during simulation are: concentration- and field-dependent mobility model, Shockley–Read–Hall for carrier recombination, non-local BTBT, band gap narrowing, and Fermi–Dirac statistics. The reason of choosing the non-local band-to-band tunneling model (instead of local model) is to incorporate the effect of electric field at each point in the tunneling path. As in local models such as Kane's model, the electric field is constant at the entire tunneling path because of the triangular barrier approximation of energy bands. But non-local BTBT models have non-uniform electric field that changes at each point in the tunneling path, thus being more accurate [18]. To calibrate the non-local BTBT model, the tunneling masses were tuned from their default values, i.e., me.tunnel $= 0.322m_o$ and mh.tunnel $= 0.549m_o$ to make it best fit with the experimental data [19], where m_o is the rest mass of electron. In simulation, the value of effective tunneling mass has been set on the material statement for silicon material used in source, channel, and drain. The adjusted value of me.tunnel $= 0.22m_o$ and mh.tunnel $= 0.52m_o$.

The tuning of the effective tunneling masses is attributed to the fact that tunneling probability depends exponentially on electron and hole tunneling masses. Moreover, reduced electron tunneling mass enhances the tunneling probability and thus the drain current. The calibration of simulation models with experimental data for transfer characteristics shows close proximity as evident from Fig. 1b and thereby validates the choice of model parameters. In addition, the experimental realization of GDO–HD–GAA-TFET can be done by integration of various previously reported process

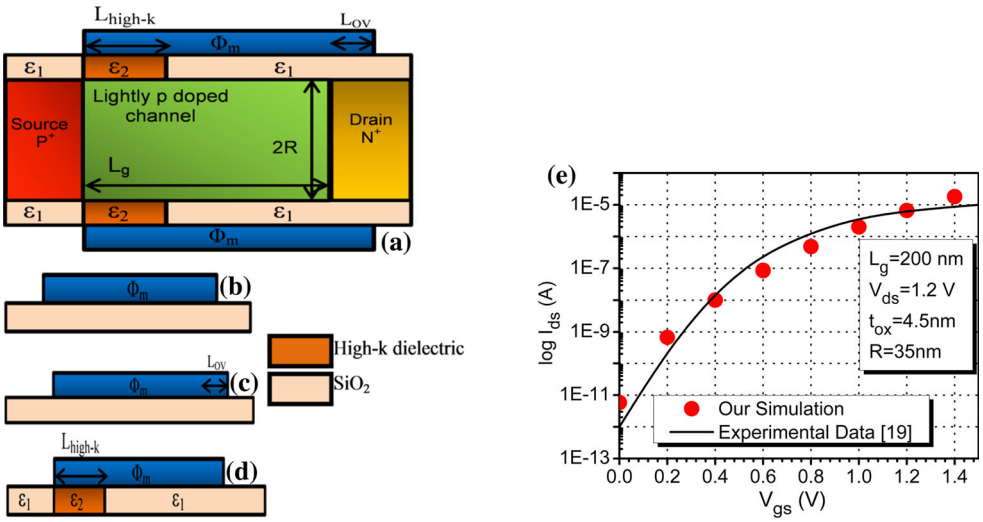

Fig. 1 Schematic structure of **a** gate drain-overlapped heterogate dielectric gate all around tunnel FET (GDO–HD–GAA-TFET) **b** GAA-TFET, **c** GDO-GAA-TFET, **d** HD-GAA-TFET **e** Calibration with the published result, I_{ds}–V_{gs} characteristics of 200-nm gate length SiNW-TFET at $V_{ds} = 1.2$ V, $T_{ox} = 4.5$ nm, Diameter = 70 nm

Table 1 Device parameters and values

Parameter	Value
Channel length L_g	50 nm
Channel radius R	10 nm
Gate oxide thickness T_{ox}	2 nm
Metal work function	4.3 eV
High-k dielectric ε_2	$HfO_2k = 21$
ε_1	$SiO_2k = 3.9$
Length of high-k dielectric $L_{high\text{-}k}$	10 nm
Source doping (p^+)	1×10^{20} cm^{-3}
Channel doping (lightly p-type)	1×10^{16} cm^{-3}
Drain doping (n^+)	1×10^{18} cm^{-3}

flow. The HD dielectrics can be formed by etching SiO_2 followed by the deposition of high-k material [5]. Thereafter, for processing of GDO, the electron beam lithography can be used for patterning of gate metal and then the electron beam evaporation can be used for gate metallization [20].

3 Results and discussion

3.1 Impact of GDO and HD engineering scheme

In this subsection, the effect of GDO and HD architectures on GAA-TFET is examined in terms of transfer characteristics, ambipolar conduction, threshold voltage (V_{th}), subthreshold swing (SS), transconductance (g_m), parasitic capacitances, cutoff frequency (f_T), and intrinsic delay (τ).

First and foremost, a comparative analysis of all the devices mentioned in Table 1 in terms of transfer characteristics is done as shown in Fig. 2a. Results thus obtained shows that GAA-TFET suffers from low I_{ON} along with large I_{AMB}. The low I_{ON} of GAA-TFET is due to the wide barrier width that reduces the tunneling rate and thus the I_{ON}. Both lower I_{ON} and large I_{AMB} limits GAA-TFET for practical applications. With incorporation of GDO architecture on GAA-TFET, i.e., for GDO-GAA-TFET, I_{AMB} reduces from an order of 10^{-13} to 10^{-15} A. The suppressed I_{AMB} for GDO-GAA-TFET is a consequence of the broadened barrier width at the drain–channel junction due to the overlapped gate over the drain. However, with application of GDO, the drain current is unaltered for positive V_{gs}. The unaltered I_{ds} for positive V_{gs} in case of GDO–GAA-TFET is due to the fact that barrier width at the tunneling junction remains unaltered with GDO architecture. The transfer characteristics of HD–GAA-TFET plotted in Fig. 2a shows a significantly large improvement in I_{ON} from an order of 10^{-10} to 10^{-5} A, without any change in I_{AMB}. The enhanced I_{ON} of HD–GAA-TFET is attributed to the steeper band bending caused by the presence of high-k material over the tunneling junction in HD engineering scheme [21, 22].

However, the drain channel junction is immune to the effects of high-k material being present over the source channel junction, thereby resulting in an unaltered I_{AMB} for HD-GAA-TFET. Consequently, for the case of GDO–HD–GAA-TFET, both I_{ON} (enhanced) and the I_{AMB} (reduced) have been improved. The I_{ON} and I_{AMB} of all the devices under considerations are plotted in Fig. 2b. The I_{AMB} is defined as the drain current at $V_{gs} = -1.0$ V and $V_{ds} = 1.0$ V. Consistent with above explanations, I_{AMB} is considerably suppressed for GDO–GAA-TFET and GDO–HD–GAA-TFET. Moreover, I_{ON} of HD–GAA-TFET and GDO–HD–GAA-TFET are appreciably improved. Thus, the GDO–HD–GAA-TFET has overcome the major obstacles of TFET such as lower I_{ON} and higher ambipolar current.

The threshold voltage (V_{th}) and subthreshold swing (SS) of aforementioned devices are illustrated in Fig. 3a, b, respectively. The consequence of large tunneling barrier width and lower tunneling rate of electrons for GAA-TFET and GDO–GAA-TFET results in higher V_{th} of these device architectures which is evident from Fig. 3a.

Further, the incorporation of HD scheme on GAA-TFET enhances the band bending at the tunneling junction that lowers the barrier width and thereby allows more electrons

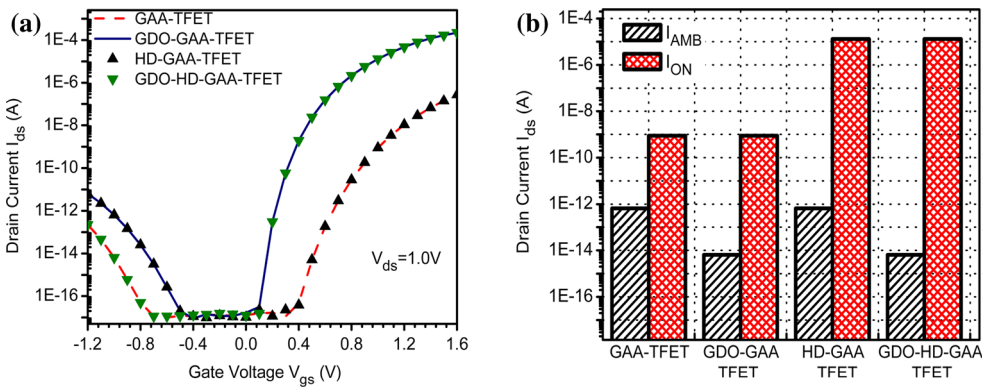

Fig. 2 **a** Transfer characteristics of GAA-TFET, HD-GAA-TFET, GDO-GAA-TFET and GDO–HD–GAA-TFET at constant drain bias $V_{ds} = 1.0$ V **b** Ambipolar current (I_{AMB}) and ON current (I_{ON}) of all the devices. For GDO architecture, $L_{ov} = 5$ nm; for HD scheme, HfO_2 is used as high-k gate dielectric $\varepsilon_2 = 21$

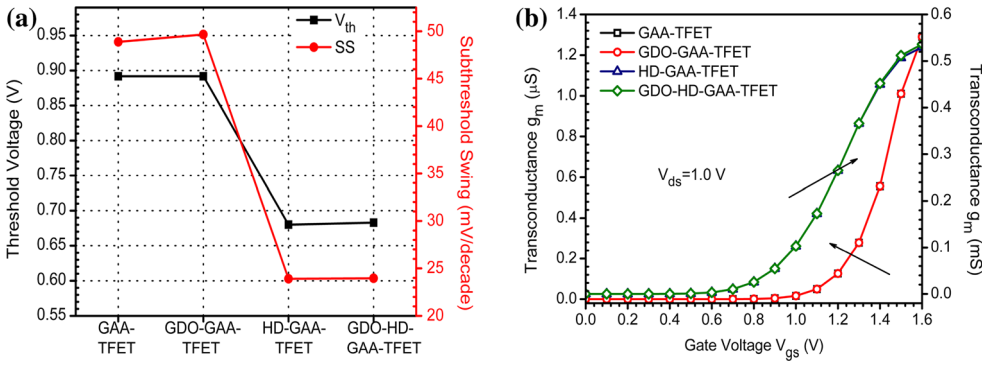

Fig. 3 **a** Threshold voltage (V_{th}) and Subthreshold swing (SS), **b** transconductance of GAA-TFET, HD-GAA-TFET, GDO-GAA-TFET, and GDO–HD–GAA-TFET. For GDO architecture, $L_{ov} = 5$ nm; for HD scheme, HfO_2 $\varepsilon_2 = 21$ is used as high-k gate dielectric

to tunnel through the source channel junction. Subsequently, the V_{th} of HD–GAA-TFET and GDO–HD–GAA-TFET reduces considerably in comparison with that of GAA-TFET and GDO–GAA-TFET as shown in Fig. 3a. Consistent with the above results, the lower I_{ON} of GAA-TFET and GDO–GAA-TFET results in large SS. However, the high-k material incorporated in HD engineering scheme, i.e., HD–GAA-TFET and GDO–HD–GAA-TFET, enhances the I_{ON} without any negotiation in I_{OFF}, contributing to lower SS. In TFETs, the gate voltage controls the drain current, and thus, the ratio of I_{ds} to the V_{gs} at constant drain bias defined as the transconductance or the mutual conductance g_m becomes an important performance parameter for TFET. For acquiring a high gain or large driving capability, the g_m should be high. The g_m of all the device architectures under consideration is shown in Fig. 3b. Significant improvement in g_m is achieved with incorporation of HD engineering scheme onto GAA-TFET as shown in Fig. 3b. In addition to this, the analogous profile of GAA-TFET/GDO–GAA-TFET and HD–GAA-TFET/GDO–HD–GAA-TFET is attributed to the similar transfer characteristics (in positive V_{gs} regime) of these architectures as explained for Fig. 2a.

The switching speed of device is affected by the parasitic capacitances. Further, in this work, the HD engineering scheme is incorporated to enhance the I_{ON} of TFET, and thus it is requisite to analyze the impact of both HD and GDO engineering on the parasitic capacitances. The parasitic capacitances of all the device architectures are analyzed in terms of gate-to-source capacitance C_{gs} and the total gate capacitance C_{gg} and are shown in Fig. 4. It must be noted that C_{gs} is significantly smaller than C_{gg} for all the device architectures.

The larger C_{gg} in each case is due to the fact of major contribution of C_{gd} to C_{gg} in case of TFET [23]. Results reveal degradation in C_{gg} and C_{gs} with the incorporation of HD architecture. Thus, there is a need to trade-off between the ON current and the parasitic capacitance of TFET, as per the application. The similar profile of C_{gs} for the case of GAA-TFET/GDO–GAA-TFET and HD–GAA-TFET/

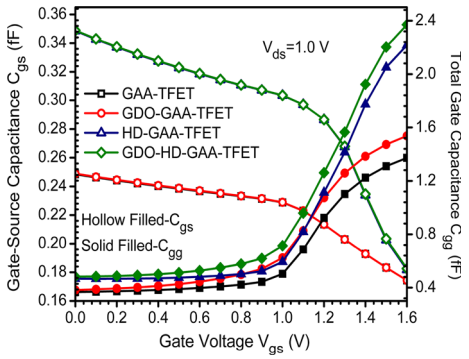

Fig. 4 Gate to source capacitance C_{gs} and total gate capacitance C_{gg} of all the devices at constant drain bias $V_{ds} = 1.0$ V. For GDO architecture, $L_{ov} = 5$ nm; for HD scheme, HfO_2 $\varepsilon_2 = 21$ is used as high-k gate dielectric

GDO–HD–GAA-TFET is due to the fact that GDO architecture (incorporated for reducing the I_{AMB}), is at the drain channel junction, and it thus does not affect the gate source capacitance.

In order to analyze the high-frequency HF performance, the cutoff frequency of all the devices is studied. Cutoff frequency f_T is defined as the frequency at which the short-circuit current gain drops to 0 dB, and mathematically it is expressed as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1}$$

where g_m is the transconductance, C_{gs} and C_{gd} are gate-to-source and gate-to-drain capacitances. As evident from Eq. 1, f_T depends directly on g_m and inversely on the parasitic capacitances. It is clearly evident from Fig. 5a that the degradation in C_{gg} has been overcome by the g_m. Thus, the dominated g_m results into superior f_T for GDO–HD–GAA-TFET and HD–GAA-TFET. The peak value of f_T, increases from 0.15 GHz to 38 GHz, with the amalgamation of HD engineering scheme. Another vital performance parameter for evaluation of the switching speed is the intrinsic delay τ, defined as:

$$\tau = \frac{C_{gg} V_{dd}}{I_{ON}} \tag{2}$$

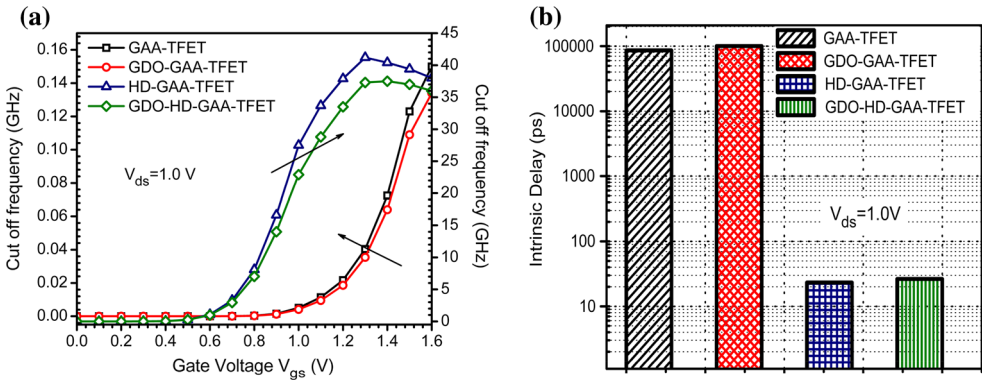

Fig. 5 **a** Cutoff frequency f_T, **b** intrinsic delay τ of GAA-TFET, HD-GAA-TFET, GDO-GAA-TFET and GDO–HD–GAA-TFET. For GDO architecture, $L_{ov} = 5$ nm; for HD scheme, HfO_2 $\varepsilon_2 = 21$ is used as high-k gate dielectric

Figure 5b shows the comparison of all the device architectures in terms of intrinsic delay. As is evident from the figure, there is a tremendous reduction in τ, with the incorporation of HD engineering scheme. The reduced τ for HD-GAA-TFET and GDO–HD–GAA-TFET is due to the presence of high-k that enhances I_{ON}.

It is analyzed that the enhanced I_{ON} dominates over the degraded parasitic capacitance, thereby improving the τ of HD–GAA-TFET and GDO–HD–GAA-TFET. Quantitatively, τ of HD–GAA-TFET and GDO–HD–GAA-TFET reduce to an order of 20 ps in comparison with τ of GAA-TFET and GDO-GAA-TFET for which τ is of order of 100 ns.

3.2 Impact of L_{ov} on GDO-GAA-TFET

After comparing GAA-TFET with HD–GAA-TFET, GDO–GAA-TFET, and GDO–HD–GAA-TFET, the effect of L_{ov} of GDO–HD–GAA-TFET has also been analyzed. The performance of GDO–HD–GAA-TFET for various L_{OV} is examined in terms of transfer characteristics, ambipolar current, ambipolarity factor α, energy band diagrams, electric field, band-to-band tunneling rate of electrons, parasitic capacitances, and cutoff frequency (f_T).

Figure 6a shows the transfer characteristics of GDO–HD–GAA-TFET for various overlapped lengths $L_{OV} = 0$, 5, 6, 7 and 8 nm. As clearly evident from the graph the ON state characteristic is immune to the variations of L_{OV} as explained previously.

The main advantage of variation of L_{OV} is for negative gate bias, i.e., reduction in the ambipolar current. It is clearly evident from Fig. 6a that ambipolar current reduces with increase in L_{OV}. The reduction in I_{AMB} with increase in L_{OV} is mainly attributed to the enhanced effective control over the barrier width at drain channel junction for negative gate biases for higher L_{OV}. Also for $L_{OV} = 0$ nm, i.e., when no gate drain overlapping is there, the ambipolar current is considerably large $\sim 10^{-11}$ A and is basically due to narrowing of barrier width at the drain channel junction for negative gate bias. Furthermore, to quantify the efficiency of GDO–HD–GAA-TFET, ambipolarity factor (α) is studied and is defined as [24].

$$\alpha = \log\left(\frac{I_{AMB}}{I_{OFF}}\right) \tag{3}$$

Figure 6b shows the ambipolar current and the ambipolarity factor of GDO–HD–GAA-TFET. Reduction in I_{AMB} from an order of 10^{-12} to 10^{-17} A has been found with an increase in L_{OV} from 0 nm to 8 nm as evident from Fig. 6b. Negative (or less value) of α illustrates minimized ambipolar conduction. As clearly illustrated in Fig. 6b, considerable reduction in α has been obtained with increase

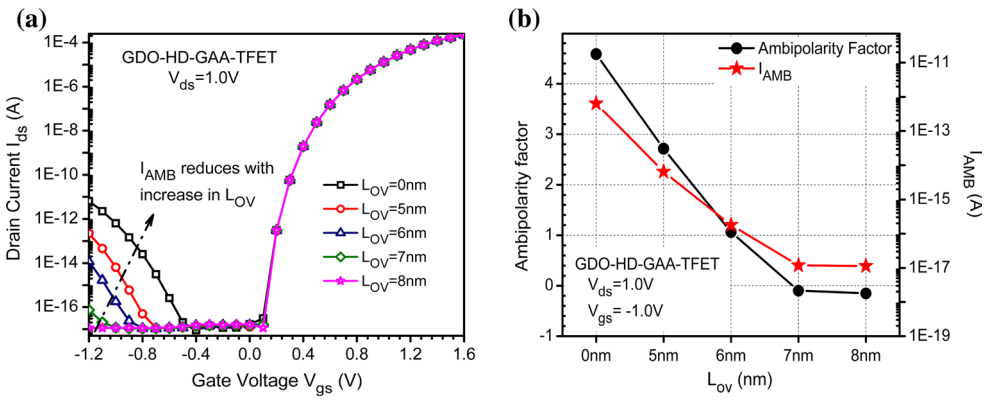

Fig. 6 **a** Transfer characteristics of GDO–HD–GAA-TFET at constant drain bias $V_{ds} = 1.0$ V for various $L_{OV} = 0$, 5, 6, 7 and 8 nm **b** Ambipolar current and ambipolarity factor for all the cases

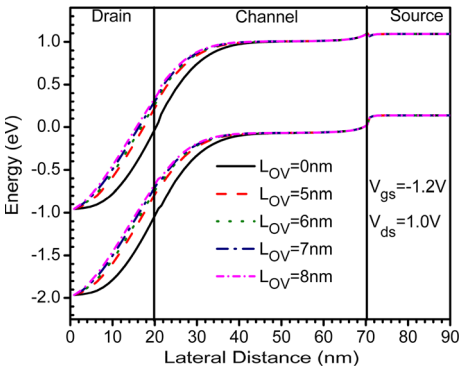

Fig. 7 Energy band diagram along the channel length of GDO–HD–GAA-TFET at constant $V_{ds} = 1.0$ V and $V_{gs} = -1.2$ V for various $L_{OV} = 0$, 5, 6, 7 and 8 nm

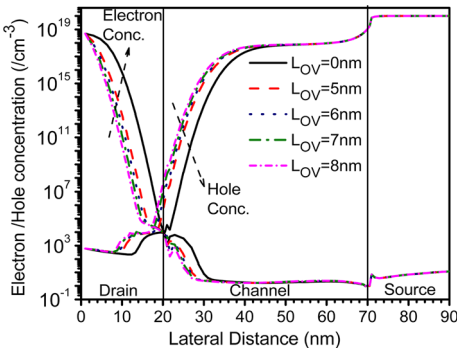

Fig. 9 Electron and hole concentration along the channel length of GDO–HD–GAA-TFET at $V_{ds} = 1.0$ V and $V_{gs} = -1.2$ V for various $L_{OV} = 0$, 5, 6, 7 and 8 nm

in L_{OV}. Furthermore, for $L_{OV} = 7$ nm and 8 nm, α becomes negative signifying that there is no effect of ambipolar conduction in the analog performance.

The reduction in I_{amb} with increase in L_{OV} can be better understood by studying the energy band diagram of GDO–HD–GAA-TFET at $V_{gs} = -1.2$ V and $V_{ds} = 1.0$ V as shown in Fig. 7. It should be noted that the effect of L_{OV} on energy bands are only at the drain channel junction and unaffected at the tunneling junction. For negative gate bias, the bands near the drain are moved upwards with an increase in L_{OV}, resulting into broadening of tunneling barrier width at the drain channel junction. This broadened barrier width at the drain channel junction reduces the probability of tunneling of electrons at the drain channel junction and thus reduces the ambipolar current as shown in Fig. 6a.

The plot of electric field at a constant $V_{gs} = -1.2$ V and $V_{ds} = 1.0$ V has also been studied and is shown in Fig. 8a. Because of the negative gate bias, the peak value at the drain channel junction is much higher than at the tunneling junction. Moreover, at the drain channel junction, the electric field is maximum for the case when no gate drain overlapping has been done or $L_{OV} = 0$ nm. Progressive reduction in peak value of electric field at the drain channel junction has been obtained with gradual increase in L_{OV}.

This reduced electric field at the drain channel junction is mainly responsible for the reduction in band-to-band tunneling BTBT of electrons at the drain channel junction as shown in Fig. 8b. Thus, the ambipolar current is reduced by increasing L_{OV}. The electron and hole concentration at a constant $V_{gs} = -1.2$ V and $V_{ds} = 1.0$ V is shown in Fig. 9. As for negative gate bias, the holes are majority carriers (as if TFET is working as a p-TFET for ambipolar conduction) in the channel region. With an increase in L_{OV}, the electric field near drain channel junction decreases resulting into increase (decrease) in hole (electron) concentration as evident from Fig. 9.

The circuit performance of TFET is appreciably affected by the parasitic capacitance that limits the upper switching speed of the device. The effect of parasitic capacitances cannot be ignored at HF operating regime. In addition to this, as gate is being overlapped over drain in GDO engineering scheme, and thus there is a need to examine the effect of drain-overlapped capacitance (C_{dov}) over the gate drain capacitance (C_{gd}) and thus the total gate capacitance (C_{gg}).

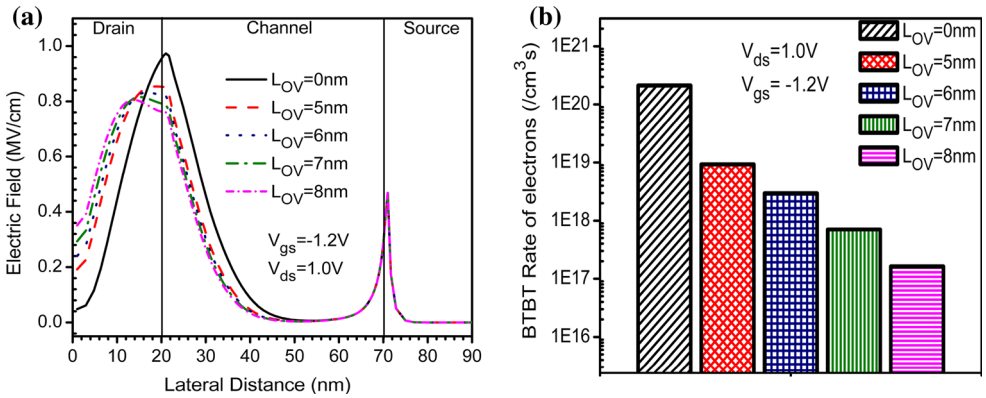

Fig. 8 **a** Electric field along the channel length of GDO–HD–GAA-TFET at $V_{ds} = 1.0$ V and $V_{gs} = -1.2$ V for various $L_{OV} = 0$, 5, 6, 7 and 8 nm **b** BTBT rate of electrons at the drain channel junction for all the cases

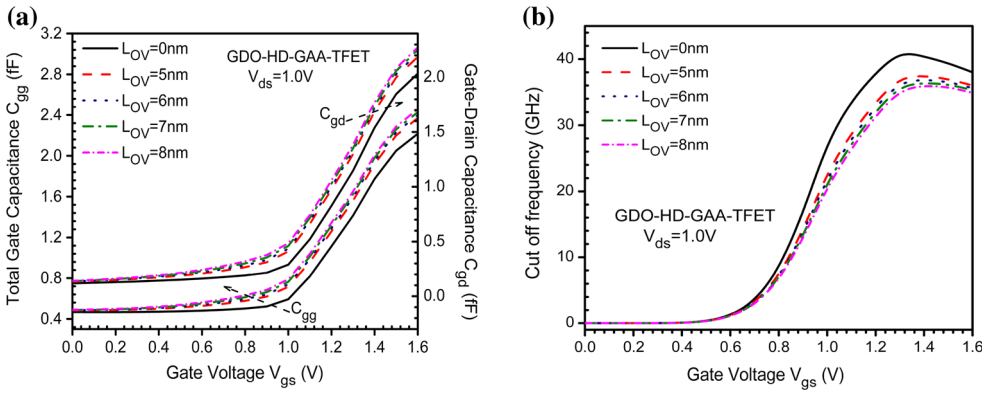

Fig. 10 **a** Total gate capacitance, gate drain capacitance and **b** Cutoff frequency of GDO–HD–GAA-TFET at $V_{ds} = 1.0$ V for various $L_{OV} = 0$, 5, 6, 7 and 8 nm

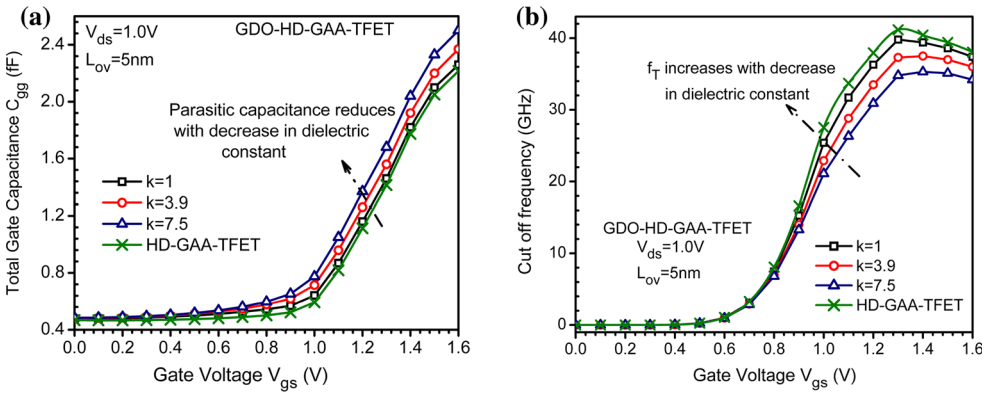

Fig. 11 **a** Total gate capacitance and **b** Cutoff frequency of GDO–HD–GAA-TFET at $V_{ds} = 1.0$ V for $L_{OV} = 5$ nm and various dielectric materials

$$C_{gd} = C_{of} + C_{dif} + C_{sif} + C_{dov} + C_{gd,inv} \quad (4)$$

where C_{of} is the outer fringing capacitance, C_{dif} and C_{sif} are the inner fringing capacitances at drain and source sides, respectively.Also another vital parameter for appraising the HF performance of the device is the cutoff frequency f_T. Thus, the effect of GDO on the parasitic capacitances and f_T has also been investigated. Effect of L_{ov} on C_{gg} and C_{gd} is shown in Fig. 10a for GDO–HD–GAA-TFET. The same profile and magnitude of both C_{gg} and C_{gd} is mainly attributed to the fact that for TFET large fraction of C_{gg} is contributed by C_{gd} as compared to C_{gs} [25]. Further, as the L_{ov} increases, the parasitic capacitances increases, thus resulting in decrease in cutoff frequency (f_T) of the device as shown in Fig. 10a,b. However, the decrease in f_T is only of 9 % and 12 % for $L_{ov} = 5$ nm and 8 nm, respectively.

3.3 Improving the HF performance of GDO–HD–GAA-TFET

To surpass the degradation on f_T caused by GDO, the dielectric over GDO region has been altered from SiO_2 to Si_3N_4 ($k = 7.5$) and vacuum dielectric ($k = 1$). Results thus obtained for total gate capacitance are shown in Fig. 11a. It is clearly evident from Fig. 11a that dielectric (inserted over L_{OV}) with higher dielectric constant enhances the C_{gg} and vice versa. Moreover, the insertion of vacuum dielectric over L_{ov} region reduces the parasitic capacitance. Thus, the degradation caused by GDO is replenished by inserting a vacuum dielectric over L_{OV}. In addition, the C_{gg} of GDO–HD–GAA-TFET with high-k over L_{OV} is also compared with that of HD-GAA-TFET. It is obtained that the integration of GDO scheme increases the C_{gg} insignificantly. However, this degradation in parasitic capacitances can be overlooked in comparison with the decrease in ambipolar conduction that blocks the application of TFET in digital circuitry. The effect of inserted dielectric over L_{OV} on f_T is shown in Fig. 11b. The f_T being inversely proportional to C_{gg} is thus enhanced due to the presence of vacuum dielectric over L_{OV} as shown in Fig. 11b. Peak value of f_T increases by 6.2 % in the presence of vacuum dielectric over L_{OV} in comparison with SiO_2. Moreover, to realize the effect of GDO more clearly, f_T of HD–GAA-TFET is also studied, and results thus obtained show marginal degradation in f_T with the integration of GDO architecture. This degradation in f_T with integration of GDO is attributed to the enhanced parasitic capacitances for GDO (as shown in Fig. 11a).

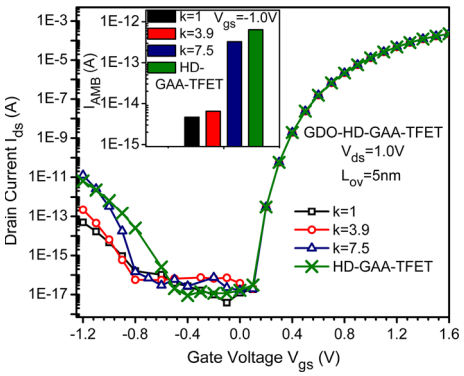

Fig. 12 Transfer characteristics of GDO–HD–GAA-TFET at $V_{ds} = 1.0$ V for $L_{OV} = 5$ nm and various dielectric materials

To determine the effect of inserted dielectric constant over L_{ov} region on the ambipolar characteristics, the transfer characteristics of GDO–HD–GAA-TFET with various dielectric constants over L_{ov} region is studied as shown in Fig. 12. It is clearly evident from Fig. 12 that for Si_3N_4 the ambipolar current is increased by 50.18 times and for the insertion of vacuum over L_{ov}, the ambipolar current is reduced by 1.39 times (in comparison with SiO_2). Moreover, to investigate the impact of GDO, the drain current of HD–GAA-TFET is also examined. It is analyzed that for HD–GAA-TFET the ambipolar conduction and thus the I_{AMB} are considerably enhanced in comparison with GDO–HD–GAA-TFET. The reduction in I_{AMB} is also shown in the inset of Fig. 12. It is evident from the inset that the I_{AMB} of HD-GAA-TFET is remarkably higher in comparison with GDO–GAA-TFET. Suppressed I_{AMB} and enhanced f_T of GDO–HD–GAA–TFET with low-k dielectric over L_{ov} make it eligible for application of digital circuitry.

4 Conclusion

This study proposed a device structure which overcomes the major shortcomings of tunnel FET. With the help of GDO architecture, the ambipolar behavior has been controlled and by amalgamation of HD scheme, the ON current of the device is enhanced. Reduced I_{AMB} and higher I_{ON} thus make it suitable for digital circuitry applications. It is revealed from the results that GDO improves the ambipolar characteristics, but it simultaneously degrades the HF performance of the device. Thus, to overcome the degradation caused by GDO, vacuum gate dielectric is inserted over the region of L_{OV}. The vacuum dielectric inserted over L_{OV} reduces the parasitic capacitances and the ambipolar current and enhances the cutoff frequency of the device, thereby resulting in an overall device improvement (analog and HF performance). Therefore, GDO–HD–GAA-TFET with vacuum dielectric over L_{ov} can be used for the development of better analog/low-power RF circuits.

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Analytical drain current formulation for gate dielectric engineered dual material gate-gate all around-tunneling field effect transistor

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In this work, an analytical drain current model for gate dielectric engineered (hetero dielectric)-dual material gate-gate all around tunnel field effect transistor (HD-DMG-GAA-TFET) has been developed. Parabolic approximation has been used to solve the two-dimensional (2D) Poisson equation with appropriate boundary conditions and continuity equations to evaluate analytical expressions for surface potential, electric field, tunneling barrier width and drain current. Further, the analog performance of the device is studied for three high-k dielectrics (Si_3N_4, HfO_2, and ZrO_2), and it has been investigated that the problem of lower I_{ON}, can be overcome by using the hetero-gate architecture. Moreover, the impact of scaling the gate oxide thickness and bias variations has also been studied. The HD-DMG-GAA-TFET shows an enhanced I_{ON} of the order of 10^{-4} A. The effectiveness of the proposed model is validated by comparing it with ATLAS device simulations.

1. Introduction

With steady downscaling of conventional CMOS devices to the nanometer domain, short channel effects and power management has become the most decisive issue for further scaling down the technology. Out of several short channel effects (SCE), high leakage current (I_{OFF}), high subthreshold slope (SS), and drain induced barrier lowering (DIBL) are of prime importance. Due to basic physics mechanism, SS is limited to 60 mV/decade resulting in increased leakage current (i.e., degradation of the off state characteristics) and enhanced static power consumption.[1,2] This dilemma can neither be resolved by using lower bandgap semiconductors, such as Ge and SiGe nor with novel gate structures such as double gate, tri gate and gate all around (GAA) due to the basic thermionic emission of carriers injected from the source to the channel region. Thus, the devices which use a new physics for carrier transport mechanism other than diffusion over a thermal barrier came into existence. Among these devices, tunnel field effect transistor (TFET) which relies on band to band tunneling (BTBT) mechanism, has established the potential to prevail the SS limit of MOSFETs and acts as a capable candidate for further extending the Moore's law.[3] Due to BTBT tunneling mechanism, TFETs are able to operate as steeper switches at lower supply voltages. Along with ultralow SS, TFETs also have very low I_{OFF} and lessened SCEs due to the built-in tunneling barrier width. Therefore, TFET has been regarded as the most promising candidate for low standby power applications.[4]

The major roadblock with TFET is lower I_{ON} (lower than the ITRS requirement), ambipolar conduction and a higher threshold voltage. Main cause of lower on-current (I_{ON}) of TFET is its small amount of BTBT at the source channel junction. Many architectures have been reported to enhance the tunneling current such as double gate architecture,[5] delta layer of SiGe at the edge of the source,[6] a high-k gate dielectric,[7] dual material gate,[8] a thin silicon body[9] and a p–n–p–n tunnel FET with a heavily doped fully depleted pocket region in between source and channel.[10] The major engineering challenge with TFET is to boost the lower I_{ON} without degrading the other device factors. Another leading problem with TFET is ambipolar conduction[11] which means conduction in two directions, both for positive and negative gate voltages. In order to overcome ambipolarity, many methods are reported such as: the hetero gate (HG) dielectric TFET proposed by Choi et al.,[12] asymmetric source/drain doping,[13] and gate drain underlap or short gate TFET,[14] and hetero-junction TFET.[15] To resolve the issue of high threshold voltage, many structures such as: tunnel bandgap modulation, gate work function engineering, vertical TFET with SiGe delta doped layer, and high-k gate dielectric with double gate, higher source doping and abrupt doping profile were proposed.[16]

In this work, we have studied a GAA geometry, which is already fabricated.[17–19] This nanowire TFET has better electrostatic control over the channel and provides a solution for SCEs. So the combine advantages of BTBT and GAA geometry improves the device characteristics. To improve I_{ON}, the high-k gate dielectric was introduced (over the entire gate length).[20] Although using high-k over the entire gate length improves I_{ON}, the major issue with high-k dielectric TFET was increase in I_{OFF} and the ambipolar current as well. Later, the hetero gate dielectric TFET was proposed by Choi et al. in which a high-k dielectric material is located near the source side and low-k dielectric near the drain side. By using a HG TFET, both ON current and ambipolarity can be improved.[12] Further, the optimization of high-k gate dielectric length is also done by Lee et al.[21] The concept of dual material gate (DMG) was proposed by,[22] to enhance the drain current of TFET. In DMG, a metal with high metal work function is used near drain side and a comparatively lower work function metal is used near source side. The DMG TFET improves the ON and OFF state characteristics simultaneously.

In this paper, in addition to the GAA geometry, the effect of DMG and HG dielectric is amalgamated, to develop an analytical model for the HD-DMG-GAA-TFET. Previously, a similar kind of work has been done in which only DMG on cylindrical GAA TFET was incorporated.[23] In this work along with DMG, the advantage of hetero gate dielectric in amalgamation has also been studied to evaluate the analog performance of the device. To study the advantage of HD configuration, the metal work functions of DMG is kept

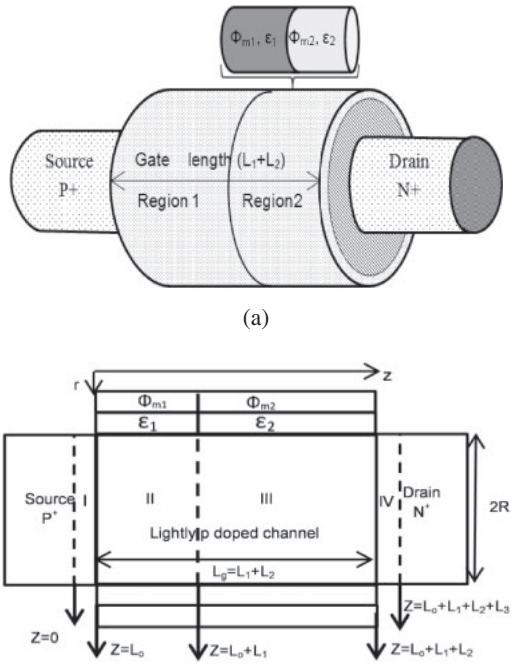

Fig. 1. (a) HD-DMG-GAA-TFET architecture. (b) 2D cross sectional view of HD-DMG-GAA-TFET.

constant throughout the work and different high-k dielectrics has been used to study the device analog performance.

2. Device structure: Parameters and simulation models

The simulation device structure, i.e., HD-DMG-GAA-TFET consisting of DMG and HG dielectric is shown in Figs. 1(a) and 1(b). The device parameters and their values are listed in Table I. To reduce the ambipolarity effect, source and drain are doped asymmetrically. All simulations have been performed using the ATLAS device simulator. The models activated during simulation are: concentration and field dependent mobility model, Shockley–Read–Hall for carrier recombination, non-local BTBT, band gap narrowing and Fermi Dirac statistics.[24)]

3. Model formulation for HD-DMG-GAA-TFET

Assuming that the influence of the charge carriers and fixed carriers are uniform in the channel, it can be neglected. The Poisson's equation can be written as

$$\frac{1}{r}\frac{d}{dr}\left[r\frac{d\psi_{si}(r,z)}{\partial r}\right]+\frac{\partial^2\psi_{si}(r,z)}{\partial z^2}=\frac{qN_i}{\varepsilon_{si}}, \tag{1}$$

where $\Psi_{si}(r,z)$ denotes the surface potential for each region. N_i is N_s, N_{ch}, N_{ch}, N_d for regions $i=1,2,3,4$, respectively. ε_{si} is the permittivity of silicon. The potential profile along the radial direction is assumed to be parabolic:

$$\psi_{si}(r,z)=A_{0i}(z)+A_{1i}(z)r+A_{2i}(z)r^2. \tag{2}$$

The following boundary conditions are applied to evaluate the coefficients A_{0i}, A_{1i}, and A_{2i}. The surface potential is only z dependent, the electric field at the center of the channel is zero, and electric field at Si/SiO_2 interface is continuous. After applying the boundary conditions, we get

Table I. Device geometrical parameters and the values used in the analysis.

Channel length L (nm)	50
Channel radius R (nm)	10
Gate oxide thickness t_{ox} (nm)	3
Source doping (p^+) N_s (cm^{-3})	10^{20}
Channel doping lightly p type N_{ch} (cm^{-3})	10^{17}
Drain doping (N^+) N_d (cm^{-3})	5×10^{18}
Dielectric constant of region 1 ε_1	21
Dielectric constant of region 2 ε_2	3.9
Metal work function of region 1 Φ_{m1} (eV)	4.1
Metal work function of region 2 Φ_{m2} (eV)	4.4
Length of region 1 L_1 (nm)	20
Length of region 2 L_2 (nm)	30

$$A_{0i}(z)=\psi_{si}(z)-A_{2i}(z)R^2, \tag{3a}$$

$$A_{1i}(z)=0, \tag{3b}$$

$$A_{2i}(z)=\frac{C_{fi}}{2R\varepsilon_{si}}[V_{gs}-\psi_{si}(z)-V_{FBi}]. \tag{3c}$$

Gate capacitance, flatband voltage, Si work function and Fermi potential of each region are given in Eqs. (4a)–(4d) as follows:

For $i=1$ (depletion region of source $0\le z\le L_0$),

$$C_{f1}=\frac{2}{\pi}\frac{\varepsilon_1}{R\ln\left(1+\frac{t_{ox}}{R}\right)},$$

$$V_{FB1}=\phi_{m1}-\phi_{s1},$$

$$\phi_{s1}=\chi_{si}+\frac{E_g}{2q}+\phi_{F1},$$

$$\phi_{f1}=\frac{k_BT}{q}\ln\left(\frac{N_s}{n_i}\right). \tag{4a}$$

For $i=2$ (tunneling region $L_0\le z\le L_1$),

$$C_{f2}=\frac{\varepsilon_1}{R\ln\left(1+\frac{t_{ox}}{R}\right)},$$

$$V_{FB2}=\phi_{m1}-\phi_{s2},$$

$$\phi_{s2}=\chi_{si}+\frac{E_g}{2q}+\phi_{F2},$$

$$\phi_{F2}=\frac{k_BT}{q}\ln\left(\frac{N_{ch}}{n_i}\right). \tag{4b}$$

For $i=3$ (remaining channel $L_1\le z\le L_2$),

$$C_{f3}=\frac{\varepsilon_2}{R\ln\left(1+\frac{t_{ox}}{R}\right)},$$

$$V_{FB3}=\phi_{m2}-\phi_{s2},$$

$$\phi_{s2}=\chi_{si}+\frac{E_g}{2q}+\phi_{F2},$$

$$\phi_{f2}=\frac{k_BT}{q}\ln\left(\frac{N_{ch}}{n_i}\right). \tag{4c}$$

For $i=4$ ($i=4$ depletion region of drain $L_2\le z\le L_3$),

$$C_{f4} = \frac{2}{\pi}\frac{\varepsilon_2}{R\ln\left(1+\frac{t_{ox}}{R}\right)},$$

$$V_{FB4} = \phi_{m2} - \phi_{s3},$$

$$\phi_{s3} = \chi_{si} + \frac{E_g}{2q} + \phi_{F3},$$

$$\phi_{F3} = \frac{k_B T}{q}\ln\left(\frac{N_d}{n_i}\right). \tag{4d}$$

Here V_{gs} is the gate to source voltage, n_i is the intrinsic carrier concentration, q is the electronic charge, T is the temperature, k_B is the Boltzmann constant, and χ_{si} is the electron affinity.

Solving Eqs. (1)–(4), we get

$$\frac{\partial^2\psi_{si}(z)}{\partial z^2} - k_i^2\psi_{si}(z) = \beta_i. \tag{5}$$

The general solution of Eq. (5) for region i is

$$\psi_{si}(z) = P_i\exp(k_i z) + Q_i\exp(-k_i z) - \frac{\beta_i}{k_i^2}, \tag{6}$$

where

$$k_i^2 = \frac{2C_{fi}}{R\varepsilon_{si}} \text{ and } \beta_i = \frac{qN_i}{\varepsilon_{si}} - k_i^2(V_{gs} - V_{FBi}). \tag{7}$$

Now using the continuity conditions (given below) at the interface of each region, coefficients P_i and Q_i can be determined. At the source depletion width end

$$\psi_{s1}(0) = -\frac{k_B T}{q}\ln\left(\frac{N_s}{n_i}\right) = V_{bi1}. \tag{8a}$$

At the tunneling junction

$$\psi_{s1} = \psi_{s2}|_{z=L_0} \text{ and } \frac{d\psi_{s1}}{dz} = \left.\frac{d\psi_{s2}}{dz}\right|_{z=L_0}. \tag{8b}$$

At the interface of region 1 and 2

$$\psi_{s2} = \psi_{s3}|_{z=L_0+L_1} \text{ and } \frac{d\psi_{s2}}{dz} = \left.\frac{d\psi_{s3}}{dz}\right|_{z=L_0+L_1}. \tag{8c}$$

At the channel and drain junction

$$\psi_{s3} = \psi_{s4}|_{z=L_0+L_g} \text{ and } \frac{d\psi_{s3}}{dz} = \left.\frac{d\psi_{s4}}{dz}\right|_{z=L_0+L_g}. \tag{8d}$$

At the drain depletion width end

$$\psi_{s4}(L_0+L_1+L_2+L_3) = \left(\frac{k_B T}{q}\right)\ln\left(\frac{N_d}{n_i}\right) + V_{ds} = V_{bi2} + V_{ds}, \tag{8e}$$

where L_0 and L_3 are the lengths of depletion width at the source and drain side respectively and given as

$$L_0 = \sqrt{\frac{2\varepsilon_{si}}{q}\frac{1}{N_{ch}}\frac{k_B T}{q}\ln\left(\frac{N_s N_{ch}}{n_i^2}\right)}, \tag{9a}$$

$$L_3 = \sqrt{\xi\left[\frac{k_B T}{q}\ln\left(\frac{N_d N_{ch}}{n_i^2}\right) + V_{ds}\right]} - \sqrt{\xi\left[\frac{k_B T}{q}\ln\left(\frac{N_d N_{ch}}{n_i^2}\right) - V_{gs}\right]}, \tag{9b}$$

where

$$\xi = 2\varepsilon_{si}/q(1/N_{ch} + 1/N_d), \tag{10}$$

$$P_1 = \frac{-V_{bi1}\gamma_2 - \gamma_2\frac{\beta_1}{k_1^2} + V_{bi2} + V_{ds} - \gamma_3}{\gamma_1 - \gamma_2}, \tag{11a}$$

$$Q_1 = \frac{V_{bi1}\gamma_1 - V_{bi2} - V_{ds} + \gamma_3 + \frac{\eta_1\gamma_1}{k_1^2}}{\gamma_1 - \gamma_2}. \tag{11b}$$

For $i = 2, 3, 4$

$$P_i = 0.5\left[P_{i-1}\left(1+\frac{k_{i-1}}{k_i}\right)\exp\left[(-k_i + k_{i-1})\left(\sum_{j=0}^{i-2}L_j\right)\right] + Q_{i-1}\left(1-\frac{k_{i-1}}{k_i}\right)\exp\left[(-k_i - k_{i-1})\left(\sum_{j=0}^{i-2}L_j\right)\right] + \left(\frac{\beta_i}{k_i^2} - \frac{\beta_{i-1}}{k_{i-1}^2}\right)\exp\left[-k_i\left(\sum_{j=0}^{i-2}L_j\right)\right]\right], \tag{11c}$$

$$Q_i = 0.5\left[P_{i-1}\left(1-\frac{k_{i-1}}{k_i}\right)\exp\left[(k_i + k_{i-1})\left(\sum_{j=0}^{i-2}L_j\right)\right] + Q_{i-1}\left(1+\frac{k_{i-1}}{k_i}\right)\exp\left[(k_i - k_{i-1})\left(\sum_{j=0}^{i-2}L_j\right)\right] + \left(\frac{\beta_i}{k_i^2} - \frac{\beta_{i-1}}{k_{i-1}^2}\right)\exp\left[k_i\left(k\sum_{j=0}^{i-2}L_j\right)\right]\right] \tag{11d}$$

where

$$\lambda_1 = e^{k_4(L_0+L_1+L_2+L_3)} \text{ and } \lambda_2 = e^{-k_4(L_0+L_1+L_2+L_3)}, \tag{12a}$$

$$\alpha_1 = 0.5e^{k_3(L_0+L_g)}\left[\lambda_1 e^{-k_4(L_0+L_g)}\left(1+\frac{k_3}{k_4}\right) + \lambda_2 e^{k_4(L_0+L_g)}\left(1-\frac{k_3}{k_4}\right)\right], \tag{12b}$$

$$\alpha_2 = 0.5e^{-k_3(L_0+L_g)}\left[\lambda_1 e^{-k_4(L_0+L_g)}\left(1-\frac{k_3}{k_4}\right) + \lambda_2 e^{k_4(L_0+L_g)}\left(1+\frac{k_3}{k_4}\right)\right], \tag{12c}$$

$$\alpha_3 = (0.5\lambda_1 e^{-k_4(L_0+L_1+L_2)} + 0.5\lambda_2 e^{k_4(L_0+L_1+L_2)})\left(\frac{\beta_4}{k_4^2} - \frac{\beta_3}{k_3^2}\right) - \frac{\beta_4}{k_4^2}, \tag{12d}$$

$$\sigma_1 = 0.5\left[\alpha_1 e^{(k_2-k_3)(L_0+L_1)}\left(1+\frac{k_2}{k_3}\right) + \alpha_2 e^{(k_2+k_3)(L_0+L_1)}\left(1-\frac{k_2}{k_3}\right)\right], \tag{12e}$$

$$\sigma_2 = 0.5\left[\alpha_1 e^{(-k_2-k_3)(L_0+L_1)}\left(1-\frac{k_2}{k_3}\right)+\alpha_2 e^{(-k_2+k_3)(L_0+L_1)}\left(1+\frac{k_2}{k_3}\right)\right], \tag{12f}$$

$$\sigma_3 = 0.5\left(\frac{\beta_3}{k_3^2}-\frac{\beta_2}{k_2^2}\right)(\alpha_1 e^{-k_3(L_0+L_1)}+\alpha_2 e^{k_3(L_0+L_1)})+\alpha_3, \tag{12g}$$

$$\gamma_1 = 0.5\left[\sigma_1\left(1+\frac{k_1}{k_2}\right)e^{(k_1-k_2)L_0}+\sigma_2\left(1-\frac{k_1}{k_2}\right)e^{(k_1+k_2)L_0}\right], \tag{12h}$$

$$\gamma_2 = 0.5\left[\sigma_1\left(1-\frac{k_1}{k_2}\right)e^{(-k_1-k_2)L_0}+\sigma_2\left(1+\frac{k_1}{k_2}\right)e^{(-k_1+k_2)L_0}\right], \tag{12i}$$

$$\gamma_3 = 0.5\left(\frac{\beta_2}{k_2^2}-\frac{\beta_1}{k_1^2}\right)(\sigma_1 e^{-k_2L_0}+\sigma_2 e^{k_2L_0})+\sigma_3. \tag{12j}$$

The obtained potential is then used to find the energy band diagram and electric field at the tunneling junction. The lateral electric field (2D) is given by

$$E_z(r,z) = -\frac{d\psi_{si}(r,z)}{dz}. \tag{13}$$

The lateral surface electric field is given by

$$E_{sz}(r,z) = k_i(P_i e^{K_i z}-Q_i e^{-K_i z}). \tag{14}$$

And transverse electric field (2D) is given as

$$E_{ri}(r,z) = 2rA_{2i}(z). \tag{15}$$

Kane's formulation is used for determining the drain current.[25] Drain current is obtained by integrating the generation rate over the volume $\pi r^2 W_T$, where W_T (tunneling barrier width) is the shortest distance (lateral) between valence band (VB) of the source and conductance band (CB) of the channel. W_T can be determined from the surface potential profile and is basically the difference between the points where the potential (Φ_s) falls $\sim E_g/q$ below the surface potential. The tunneling barrier width, thus, obtained is given as

$$W_T = \frac{1}{k_2}\ln\left[\left(\psi_{s2}(z)+\frac{E_g}{q}+\frac{\beta_2}{k_2^2}+\sqrt{\left(\psi_{s2}(z)+\frac{E_g}{q}+\frac{\beta_2}{k_2^2}\right)^2-4P_2Q_2}\right)\Big/\,2P_2\right]. \tag{16}$$

Further, with Kane's model, the generation rate can be evaluated as

$$G(E) = A\left(\frac{E^D}{E_g^{1/2}}\right)\exp\left(-\frac{BE_g^{3/2}}{|E|}\right), \tag{17}$$

where A and B are the parameters of Kane's model and depends on the effective mass of electron and hole in the CB and VB. The default value of $D = 2$.

$$A = \frac{q^2\sqrt{2m_{tunnel}}}{h^2E_g^{1/2}} \text{ and } B = \frac{\pi^2E_g^{3/2}\sqrt{0.5m_{tunnel}}}{qh}, \tag{18}$$

$$\frac{1}{m_{tunnel}} = \frac{1}{m_{ee}}+\frac{1}{m_{eh}}, \tag{19a}$$

where

$$m_{ee} = m_e m_0 \text{ and } m_{eh} = m_h m_0. \tag{19b}$$

Here m_e and m_h are the effective masses of electron and hole, respectively, and m_0 is the rest mass of an electron. The average electric field E_{avg} is calculated by integrating the total electric field E_{Tot} over the barrier width W_T as

$$E_{Tot} = \sqrt{|E_z|^2+|E_r|^2} \text{ and } E_{avg} = \left(\int_{W_T}E_{Tot}dz\right)\Big/\,W_T. \tag{20}$$

The expression for drain current (I_{ds}) is then given as:

$$I_{ds} = q\pi R^2 W_T G(E_{avg}) \tag{21}$$

4. Results verification and discussion

4.1 Impact of gate and drain bias

Figure 2(a) depicts the potential profile of the device for different gate bias. With an increase in gate bias, there is an increase in the channel potential which results in higher band bending of the energy bands in the channel. It is clearly shown that the model developed is in well agreement with the simulation data. Figure 2(b) illustrates the nonlocal BTBT electron tunneling rate at different V_{gs}. It is evident from the graph that at $V_{gs} = 0.0$ V, there is no tunneling of electrons from VB of source to CB of channel due to large W_T present at the tunneling junction. But, as we increase the gate bias, the higher band bending in the channel lowers W_T and allows more number of electrons to tunnel through the source–channel junction, which increases the tunneling rate to an order of approximately $10^{25}/cm^3{\cdot}s$.

The impact of V_{ds} on transfer characteristics is presented in Fig. 3(a). As is evident from the figure, the tunneling current increases as we increase V_{gs}. This enhanced drain current is due to the lowering of W_T with rise in V_{gs}, which in turn enhances the tunneling generation rate and hence, the drain current. A higher I_{ON} is observed for a higher V_{ds}.

The impact of V_{gs} on output characteristics is shown in Fig. 3(b). Again, tunneling current increases as the V_{ds} is increased. The device shows good saturation at higher V_{ds}. In addition, an increase in V_{gs} results in higher tunneling current.

Transconductance g_m, which is basically the first order derivative of the drain current with respect to the V_{gs} at constant V_{ds}, is shown in Fig. 4(a). The peak of g_m curve gives the optimum bias point if device is to be used as an amplifier. The g_m is obtained for three drain biases. It clearly shows that the peak of g_m is high for a higher drain bias. This enhancement is because of a high drain current at higher drain bias. Output-conductance g_d, which is first order

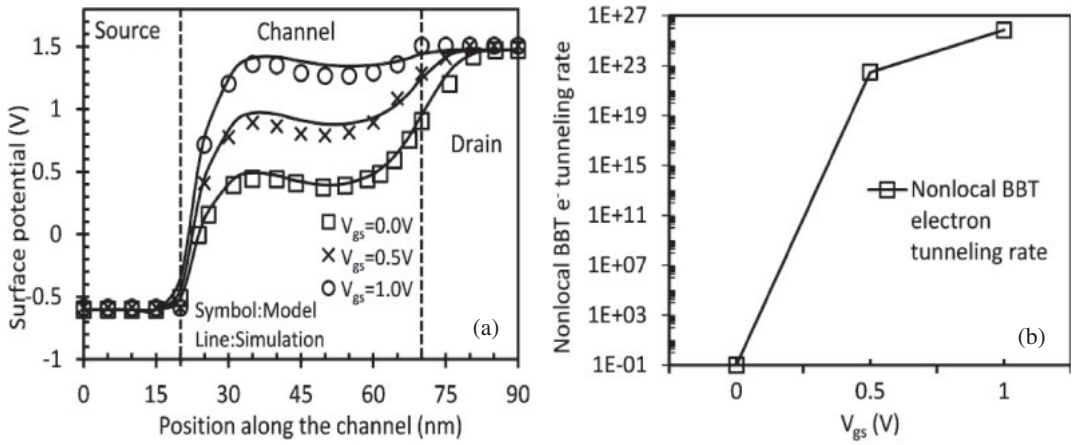

Fig. 2. (a) Surface potential along the length from source to drain, for $V_{gs} = 0.0$, 0.5, and 1.0 V at $V_{ds} = 1$ V. (b) Nonlocal BBT electron tunneling rate as a function of V_{gs}.

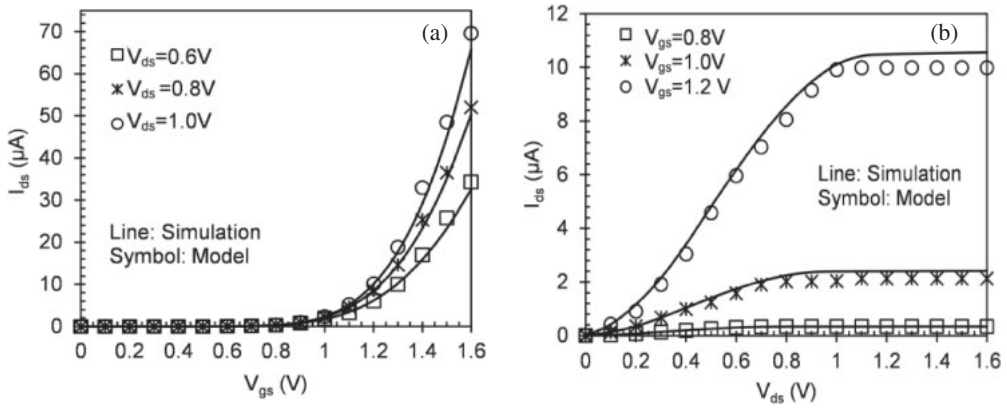

Fig. 3. Impact of drain and gate bias on (a) transfer and (b) output characteristics.

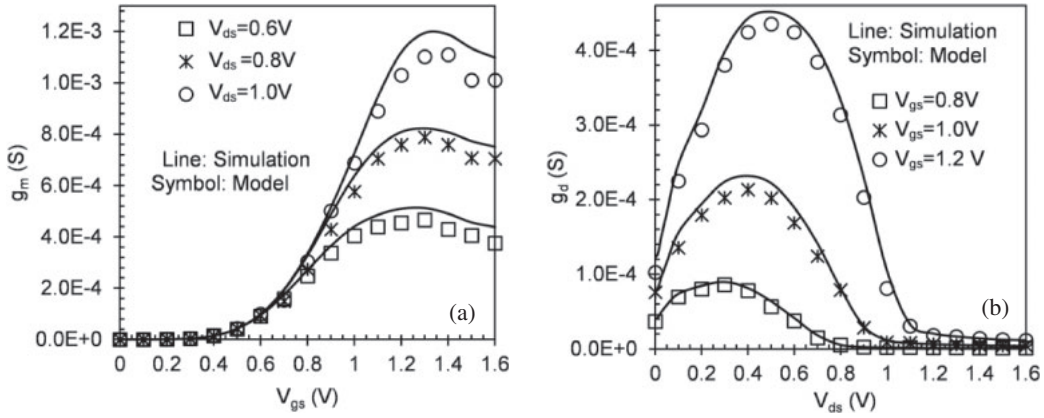

Fig. 4. (a) Impact of drain bias on g_m. (b) Impact of gate bias on g_d.

derivative of the drain current with respect to V_{ds} at a constant V_{gs}, is shown in Fig. 4(b). The output conductance is obtained for three gate biases. The curve gets shifted to a higher value of g_d for every increase in gate bias.

4.2 Impact of high-*k* gate dielectric

This section studies the impact of high-*k* dielectric on analog performance of the device. The electron velocity contour has been obtained for three high-*k* gate dielectric namely Si_3N_4 (7.5), HfO_2 (21), and ZrO_2 (29) shown in Figs. 5(a)–5(c), respectively. It is evident from the contours that the electron velocity is much lower at the drain side in case of ZrO_2 as compared to Si_3N_4, which leads to increase in the tunneling current (the solution for major roadblock of TFET). In hetero-gate-dielectric TFET, the presence of high-*k* near source side results into a higher band bending due to increase in surface potential (at a constant gate bias).[21)]

This higher band bending leads to reduction in tunneling W_T, which further increases the generation rate and hence the I_{ON}:

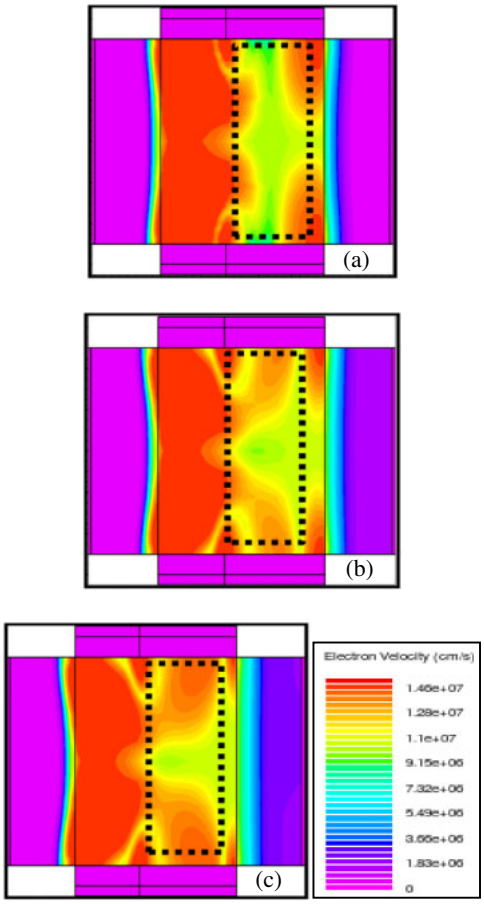

Fig. 5. (Color online) Electron velocity (cm/s) contour for different high-k dielectric. $k = 7.5$ (a), 21 (b), and 29 (c).

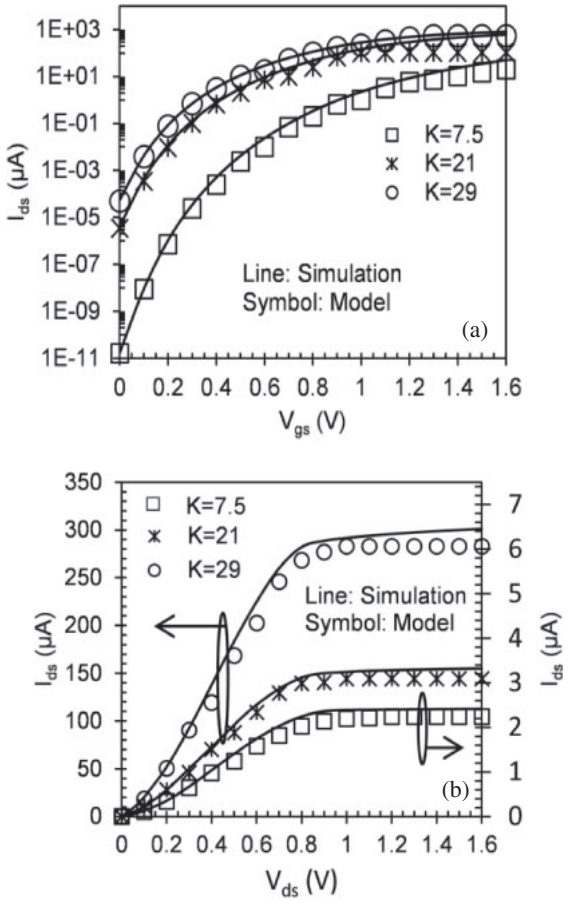

Fig. 6. (a) Drain current as a function of V_{gs} for different high-k dielectric at $V_{ds} = 0.8$ V. (b) Drain current as a function of V_{ds} for different high-k dielectric at $V_{gs} = 1.0$ V.

$$V_{gs} = \psi_s - \frac{Q_s t_{ox}}{\varepsilon_{ox}}, \tag{22}$$

where Q_s is the charge density per unit area, ε_{ox} is the permittivity of the insulator and ψ_s is the surface potential. The impact of high-k gate dielectric namely Si_3N_4, HfO_2, and ZrO_2 on transfer characteristics at constant $V_{ds} = 0.8$ V is shown in Fig. 6(a). It is evident from the graph that among the three dielectrics, the higher value of dielectric constant corresponds to higher current driving capability. This is because of the increase in band bending with higher dielectric constant, which reduces the tunneling barrier width and hence, enhances the generation rate. But the counter effect is the degradation of OFF characteristics owing to a higher band bending at higher gate dielectric resulting in tunneling of electrons at lower V_{gs}. This result in higher leakage current and, thus higher static power dissipation. Hence, we have to trade-off between I_{ON} and I_{OFF} to optimize the I_{ON}/I_{OFF} ratio and SS. The highest I_{ON}/I_{OFF} ratio is obtained for Si_3N_4 (7.5) as compared to other high-k's. The impact of high-k gate dielectric on output characteristics at a constant $V_{gs} = 1.0$ V is illustrated in Fig. 6(b). It is clear that the device predicts a qualitative agreement in linear regime and also shows drain current saturation for higher V_{ds}. It has been observed that the ZrO_2 has better output characteristics as compared to Si_3N_4 and HfO_2. Again good agreement between the model prediction and the device simulations are obtained in all regions.

Figure 7(a) illustrates the variation of barrier width lowering with respect to V_{gs} for different high-k dielectrics. W_T decreases with an increase in gate bias due to higher band bending for higher V_{gs} and the alignment of VB of source and CB of channel. The gate threshold voltage, V_{TG}, of TFET is the gate voltage for which the energy barrier narrowing starts to saturate with the applied V_{gs}.[26] Clearly, the barrier width for ZrO_2 is lower at each gate bias. Figure 7(b) indicates the drain current with respect to W_T. By using constant current method (at V_{gs} for which $I_{DS} = 10^{-7}$ A), the threshold voltage of TFET can be extracted.[27] It is clear from the figure that gate bias corresponding to barrier width of ~4.1 nm is the threshold voltage of the device. Impact of high-k dielectric on I_{ON} and I_{OFF} of the device is shown in Fig. 8(a). Among the three dielectrics, ZrO_2 has the maximum I_{ON}, but at the same time, I_{OFF} of the device is higher for the same dielectric and hence, an optimization has to be done depending on the application for I_{ON}/I_{OFF} ratio. The impact of high-k dielectric on threshold voltage and SS of the device is shown in Fig. 8(b). It is evident from the figure that threshold voltage decreases as we move from Si_3N_4 to HfO_2 and then to ZrO_2. But simultaneously, SS of the device enhances significantly from 34 to 53 mV/decade as we use higher dielectric constant. So an optimized value of high-k dielectric can be taken depending on the application. But it is clearly shown that the SS has been reduced considerably from the fundamental physical limit of $(k_B T/q)\ln 10$ on the subthreshold swing (~60 mV/decade) at normal room temperature of conventional MOSFET.

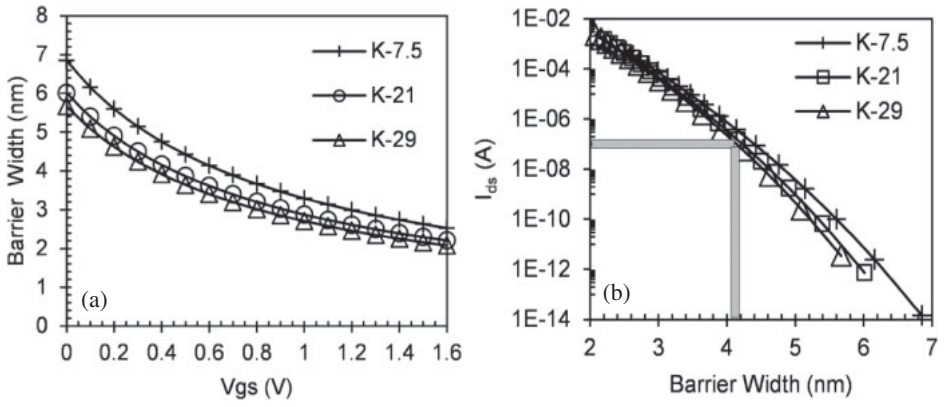

Fig. 7. (a) Barrier width as a function of V_{gs} for different high-k dielectric. (b) Drain current as a function of barrier width for different high-k dielectric.

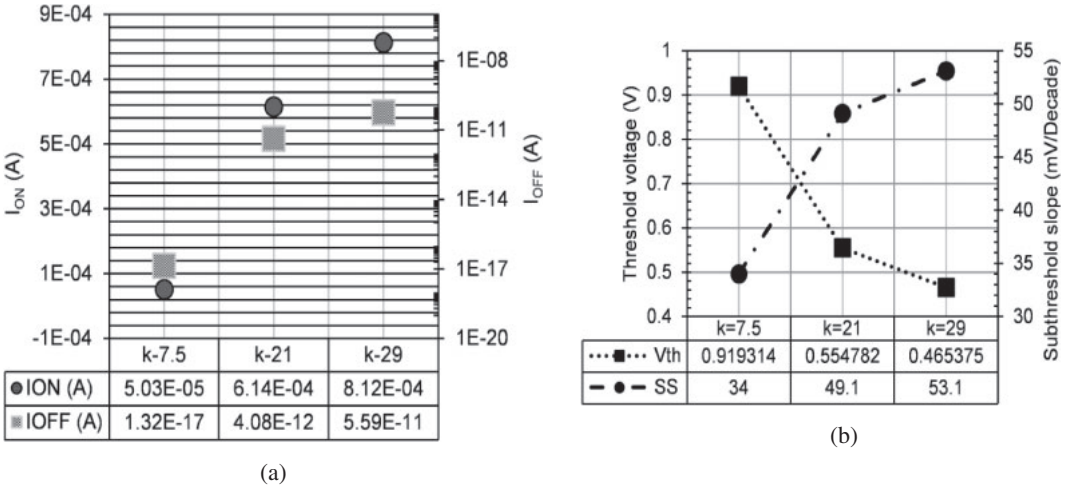

Fig. 8. (a) Tunneling current and (b) V_{th} and SS of HD-DMG-GAA-TFET for various high-k.

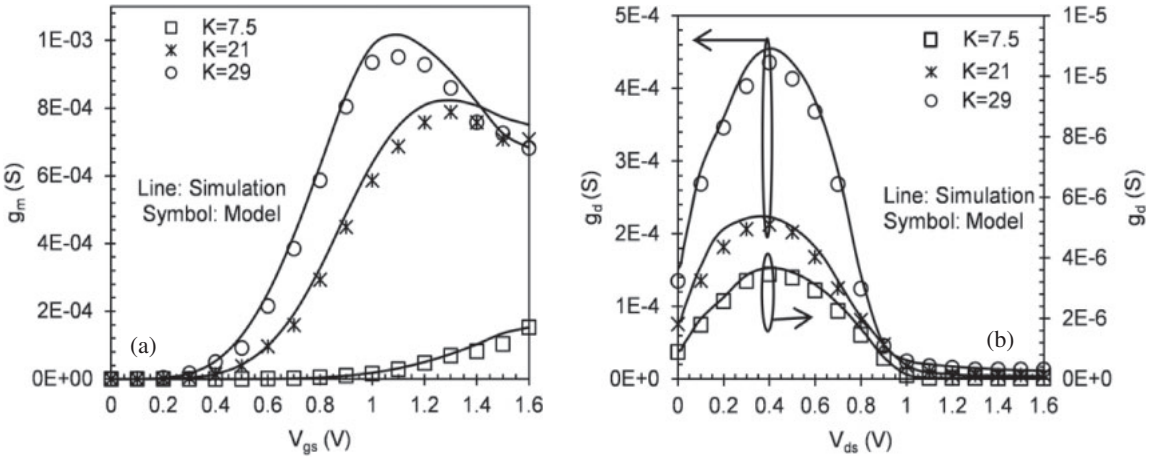

Fig. 9. (a) g_m as a function of gate bias for different high-k dielectric. (b) g_d as a function of V_{ds} for different high-k dielectric.

Variation of g_m for the three dielectrics with respect to V_{gs} at constant $V_{ds} = 0.8$ V, is shown in Fig. 9(a). By setting the DC bias close to V_{gs} (at $g_m = g_{mmax}$), a higher g_m can be achieved. This optimum bias point, shifts towards lower V_{gs} by 15.38% for higher gate dielectric (near source side) as compared to lower gate dielectric. This change is due to decrease in W_T lowering with an increase in high-k dielectrics. It is clearly shown that among the three dielectric constants, g_m of the device is higher for higher dielectric constant and is due to the enhanced electrical coupling between the gate and the tunneling junction, which further enhances the tunneling rate. Hence, more number of electrons tunnel through the barrier which eventually leads to enhanced drain current and g_m. The variation of output-conductance g_d, with respect to V_{ds} at a constant V_{gs}, is shown in Fig. 9(b). Again, the output conductance has a higher peak for ZrO_2 and is increased by an order of approximately 100 with respect to Si_3N_4.

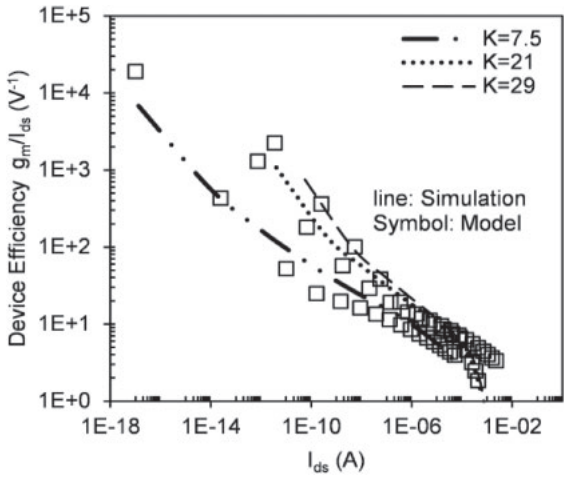

Fig. 10. Device efficiency as a function of tunneling current for different high-k dielectrics.

Another important parameter is the device efficiency (g_m/I_{ds}) which defines the capability to convert dc power into ac gain performance at a particular drain bias. Figure 10 illustrates the comparison of g_m/I_{ds} for three high-k dielectrics. For each case, the highest value of g_m/I_{ds} is obtained for the weak inversion region and an almost linear decrease in g_m/I_{ds} profile has been obtained with increase in tunneling current. Device having ZrO_2 as a high-k dielectric has better device efficiency as compared to the device which uses HfO_2 and Si_3N_4. Also for each case, the device efficiency has reached a value greater than 40 V^{-1} (the fundamental limit of conventional MOSFET) in subthreshold region.

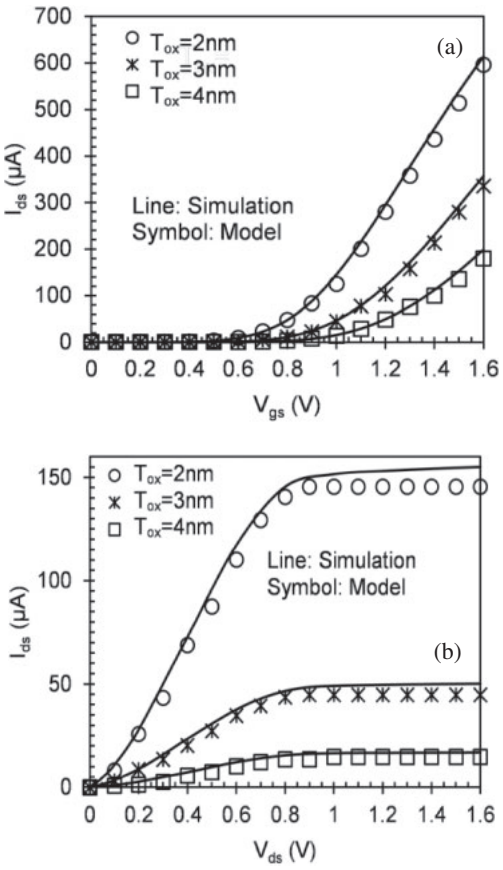

Fig. 11. (a) Drain current as a function of (V_{gs}) for different T_{ox} at $V_{ds} = 0.8$ V. (b) Drain current as a function of (V_{ds}) for different T_{ox} at $V_{gs} = 1.0$ V.

4.3 Impact of scaling oxide thickness

Further, the impact of scaling the gate oxide thickness has been studied on analog performance of the device. I_{ON} of the device increases by 2.3 times as we reduce the gate oxide thickness from 4 to 2 nm and is shown in Fig. 11(a). With scaling of T_{ox}, gate controllability over the tunneling junction improves, which results in increased electric field at the tunneling junction for lower oxide thickness and allows more number of charge carriers to tunnel through the junction (enhanced generation rate), which eventually resulted in enhancement of drain current. The impact of gate oxide thickness on output characteristics is shown in Fig. 11(b). Again the drain current is improved by 9.6 times with reduction in gate oxide thickness from 4 to 2 nm.

5. Conclusions

A 2D drain current model has been developed incorporating the effect of gate dielectric, gate bias, gate metal work function and oxide thickness for HD-DMG-GAA-TFET. The higher gate bias results into higher band bending and reduction in barrier width. By using a high-k dielectric near the source side; I_{ON} and transconductance is enhanced. The output characteristic shows a very good saturation for higher drain bias. As in most of the conventional amplifiers, MOSFET is operated in saturation region or in linear region; and therefore the device is well suited for analog applications. The counter effect of high-k is the degradation of OFF characteristics. Optimization of I_{ON}/I_{OFF} ratio depending on the application has to be done for sub nanometre devices. A SS less than 60 mV/decade have been obtained in each case. The improvement in SS and diminution in threshold voltage has been obtained by using higher-k dielectric. Additionally, the variation of oxide thickness on the analog performance has been investigated for better results. By using a thinner gate oxide TFET, the analog performance can be enhanced. The less static power dissipation, lower SS, higher device gain, better device efficiency and the higher I_{ON}/I_{OFF} ratio make the device an effective candidate for the analog applications.

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