A DISSERTATION ON

REALIZATION OF CONTINUOUS TIME FILTER USING OFCC

Submitted In partial fulfillment for the award of the degree

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In

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Submitted By

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CERTIFICATE

It is certified that the dissertation entitled **"REALIZATION OF CONTINUOUS TIME FILTER USING OFCC"** is a work of **ZUBAIR KHAN** Roll No. **2K11/VLS/13**, a student of Delhi Technological University. This work was completed under my direct supervision and guidance and forms a part of the Master of technology (VLSI Design and Embedded System) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted for the award of any other degree to the best of my knowledge.

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ABSTRACT

In this thesis operational floating current conveyor (OFCC), a current mode building block is studied and its application as continuous filter has been investigated. There modes of filter presented in this thesis using OFCC current mode, trans-impedance mode, voltage mode and TA mode. All these filters employ three OFCCs and two grounded capacitors. The current mode and trans-impedance mode filters use two grounded resistors whereas an additional grounded resistor is used in trans-admittance mode and voltage mode filters. The grounded resistor is implemented using MOS based structure thereby adding electronic tunability to filter parameters. Further low pass(LP) and band pass(BP) filters are also implemented using single OFCC block in multiple loop feedback topology. All the proposed filters functionality is verified through PSPICE simulation using 0.5µm mosis agilent technology parameters.

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CHAPTER 1: INTRODUCTION

As the technology in VLSI design is progressing , the sizes of electronic circuits are shrinking and consequently the voltage supply has also to be reduced in the same ratio in order to maintain appropriate power dissipation per area. However , designing of electronics circuits with low supply voltages and power dissipation becomes the limiting factor in the design, particularly when extreme speed or accurate signal processing is required. The concern to meet the simultaneous demands of two contradictory requirements has led to the evolution of trade-off solutions which sets the trend for modern era of VLSI. During the last two decades analog signal processing applications have found their place in so called current mode [1], where signals representing information are in the form of electric currents.

The current mode approach for analog signal processing has proved itself as a better alternate to traditional voltage mode circuits [2] due to their potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption and high operating speed. The current mode circuits are also advantageous for analog signal processing requirement because current addition/subtraction does not require additional circuit elements.

The current mode active elements are gaining wide acceptance as building blocks in analog circuit design which is evident from the availability of wide variety of current mode active elements. The initial set of current mode active elements are voltage feedback amplifier(VFA), , current feedback amplifier(CFA) [3] and current conveyor(CC) [4], operational transconductance amplifier(OTA) [5]. The initial set of active elements for analog signal processing is currently evolving in two directions. The first direction is represented by modifying the basic elements such as VFA, CFA, OTA and CC. Some of the modification of current conveyors are current conveyor first generation(CCI) [4], current conveyor second generation(CCII) [6], current conveyor third generation(CCIII) [7]. The second direction of the evolution of the active elements is characterized by appearance of entirely new elements which extend the original VFA-CFA-OTA-CC set [8]. Some of these types are operational transresistance amplifier(OTRA) [9], current differencing buffered amplifier(CDBA) [10], current differencing transconductance amplifier(CDTA) [11] and operational floating current conveyor(OFC) [12].

In this thesis the current mode active block used to implement continuous time filter is OFCC [14]. The operational floating current conveyor(OFCC) is a new two port general purpose

analog building block. Its interesting aspect is that of providing features of both the current conveyor(CCII) and the current feedback op-amp(CFOA)[13]. Literature survey on OFCC based circuits [14–21] shows that voltage mode filter [15–17], variable gain amplifier [18], wheat stone bridge [19], and instrumentation amplifier [20] and read out circuit [21] are available. The study of current mode filters [22, 25–43] shows that only OFCC based voltage mode filter is available in the literature. This thesis aims at presenting different modes of continuous time filters using OFCC.

The thesis is organised in 6 chapters. Chapter 2 presents the study of OFCC about its architecture, CMOS realizations and some existing applications.also simple. In Chapter 3 current mode and trans-impedance mode filter is presented and its operation is verified through simulations. Chapter 4 presents implementation of trans-admittance mode and voltage mode filter. Single OFCC based filters are presented in chapter 5. The thesis concludes in chapter 6.

All the results have been verified through SPICE simulation using 0.5μm mosis agilent technology parameters.

CHAPTER 2: OFCC CURRENT MODE BUILDING BLOCK

Operational floating current conveyor is one of the latest interests of researchers in domain of current mode blocks. The interesting aspect of OFCC lies in the fact that it provides the feature of both the current conveyor and the current feedback op-amp (CFOA). This chapter aims at familiarizing with the working of OFCC by describing its circuit and port relationship. The basic circuit applications are also described.

2.1. INTRODUCTION

Toumazou and Payne in 1991 proposed a versatile analogue building block and named it OFC (operational floating conveyor) having similar properties to a current feedback op-amp but with a differential current output which allows accurate current sampling [12]. The architecture [12] is based on current feedback op-amp (CFOA) and uses cross coupled current mirror circuit to provide additional current outputs. Another structure for OFC [13] is proposed which employs a tran- conductance amplifier sandwiched between two CCIIs. The realization based on CMOS is also given. Further a port was added and it was termed as OFCC (operational floating current conveyor) which enhanced the versatility of the block [14].

The implementation scheme found in literature is either current feedback amplifier with transistor array or CMOS structures having block architecture.

The circuit symbol of Operational Floating Current Conveyor (OFCC)[14] is shown in Fig.2.1. It has a low impedance current input port X and a high impedance voltage input port Y. It also has a low impedance voltage output port W and high impedance current output port Z. The output voltage at port W is multiplication of input current at port X and the open loop transimpedance gain Z_t. The port relationships of the OFCC is characterized by the following matrix

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_Z \end{bmatrix} \quad (2.1)$$

It may be noted that the voltage at port X is the same as input voltage at port Y so voltage tracking action is available at input port. The output current flowing through port W is copied to port Z, thereby offering current tracking at the output ports.

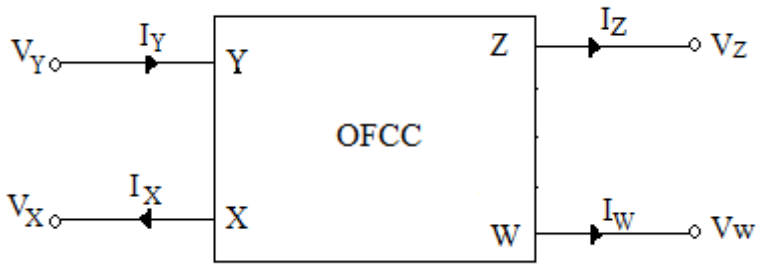


Fig. 2.1 OFCC Circuit symbol

2.2. OFCC BASIC ARCHITECTURE

The basic architectures for implementation of OFCC are described in [18]. The following section describes these architectures and their CMOS realizations.

2.2.1. FIRST REALIZATION

2.2.1.1. Architecture I

The first realization for implementing OFCC is shown in Fig. 2.2[18]. It comprises of a series connection of two 2nd generation current conveyors of the CCII+ type and one non-inverting transimpedance amplifier. The first CCII is used to perform the required voltage following action at the input port between terminals Y and X. The second CCII is used to perform the required current following action at the output port between terminals W and Z. The input current at terminal X is multiplied by the transimpedance amplifier gain to provide the output voltage at terminal W[18].

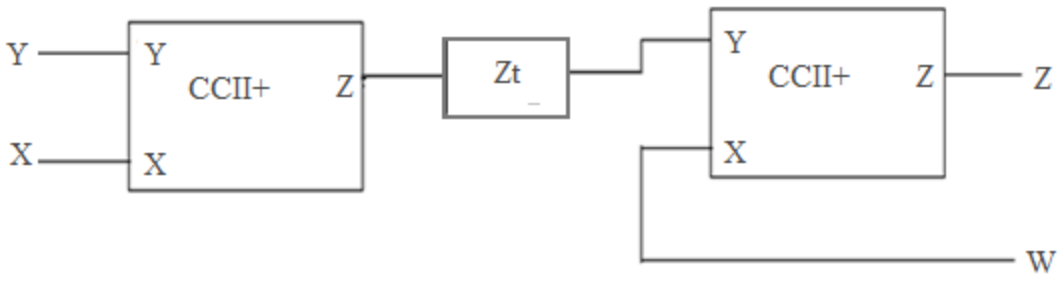


Fig. 2.2 Architecture I

2.2.1.2. Circuit Description

The first CMOS realization of the OFCC based on the block diagram shown in Fig. 2.2 is given in Fig. 2.3. The group of transistors (M1 and M2), (M3 and M4), (M14 and M15), (M16 and M17), (M5 and M18), (M6 and M19), (M11 and M12) as well as (M7 and M20) are matched. Assuming that all the transistors operate in saturation region, the operation of the circuit can be explained as follows. The first CCII+ (M1-M7) perform the voltage following action at the input port between terminals Y and X. The second CCII+ (M14-M20) perform the current following action at the output port between terminals W and Z. The transimpedance amplifier (M8-M13) multiply the input current at terminal X by large transimpedance gain Zt to produce the output voltage at terminal W. The transimpedance amplifier operation can be explained as follows. The input current at terminal X is mirrored by transistors M3,M4,M6 and M7, and the mirrored current will flow in the equivalent

parasitic impedance of the gate terminal of M8, producing a voltage on it. The voltage is then amplified to produce the output voltage at terminal W.

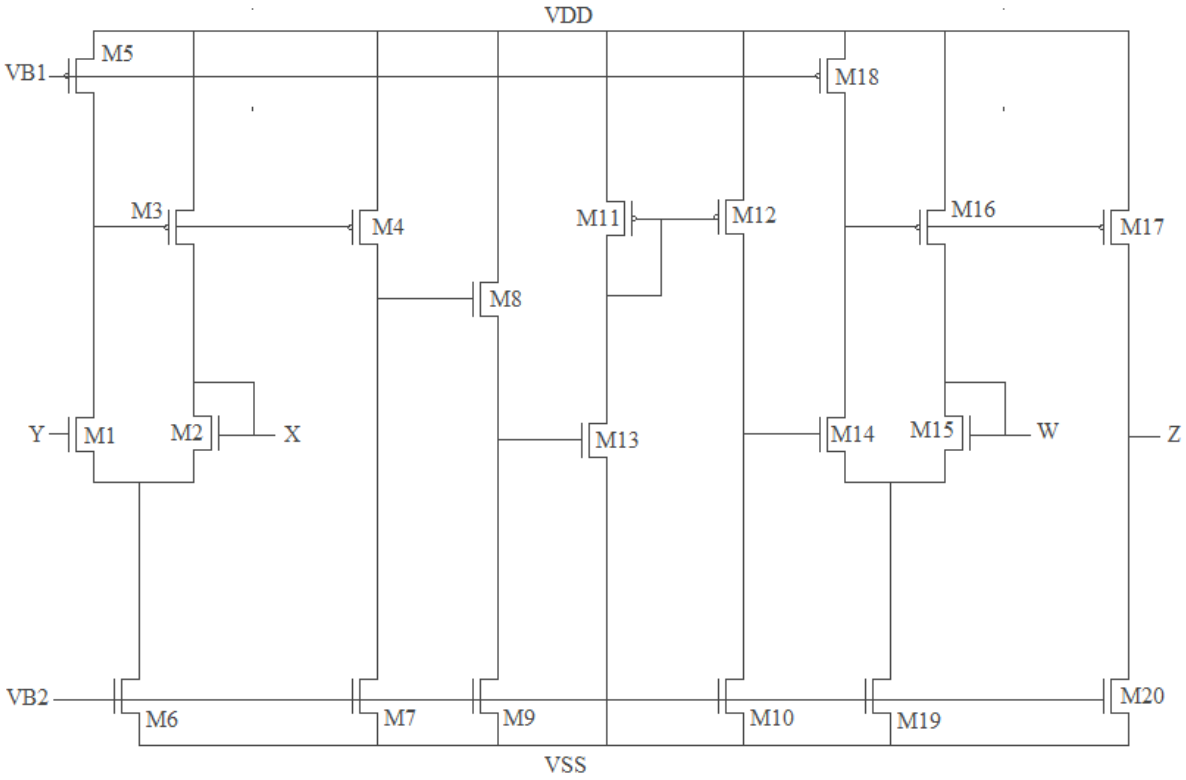


Fig. 2.3 CMOS realization of Architecture I

2.2.2. SECOND REALIZATION

2.2.2.1. Architecture II

The second realization of OFCC with block diagram is shown in Fig. 2.4 [18]. In this realization the second CCII+ of the first realization is replaced by a simple current follower to convey the terminal W current to terminal Z.

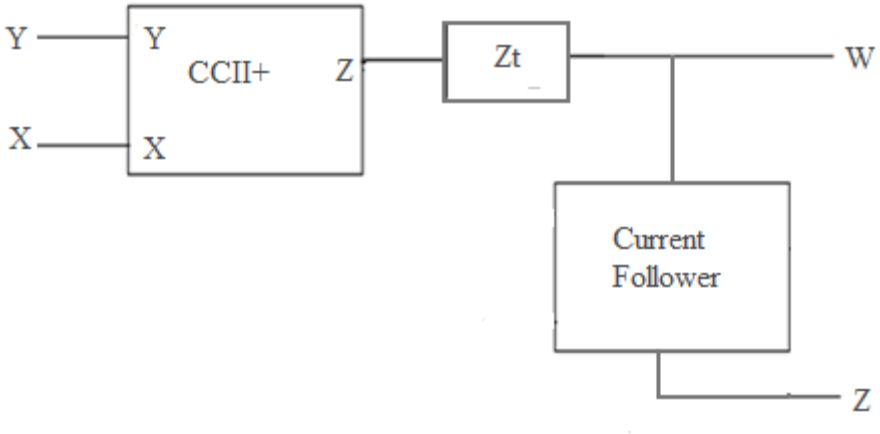


Fig. 2.4 Architecture II

2.2.2.2. Circuit Description

The second CMOS realization of the OFCC based on the block diagram shown in Fig. 2.4 is given in Fig. 2.5. The group of transistors (M1 and M2), (M3 and M4), (M10 and M15) as well as (M11, M12 and M14) are matched. Assuming that all the transistors operate in saturation region, the operation of the circuit can be explained as follows. The first CCII+ (M1-M7) perform the voltage following action at the input port between terminals Y and X. The positive current follower (M10, M12, M14 and M15) performs the current following action at the output port between terminals W and Z. The transimpedance amplifier (M8-M13) multiply the input current at terminal X by large transimpedance gain Zt to produce the output voltage at terminal W. The transimpedance amplifier operation can be explained as follows. The input current at terminal X is mirrored by transistors M3,M4,M6 and M7, and the mirrored current will flow in the equivalent parasitic impedance of the gate terminal of M8, producing a voltage on it. The voltage is then amplified to produce the output voltage at terminal W.

The implementation of OFCC in this thesis uses this architecture and its CMOS realization with additional Z copy terminals.

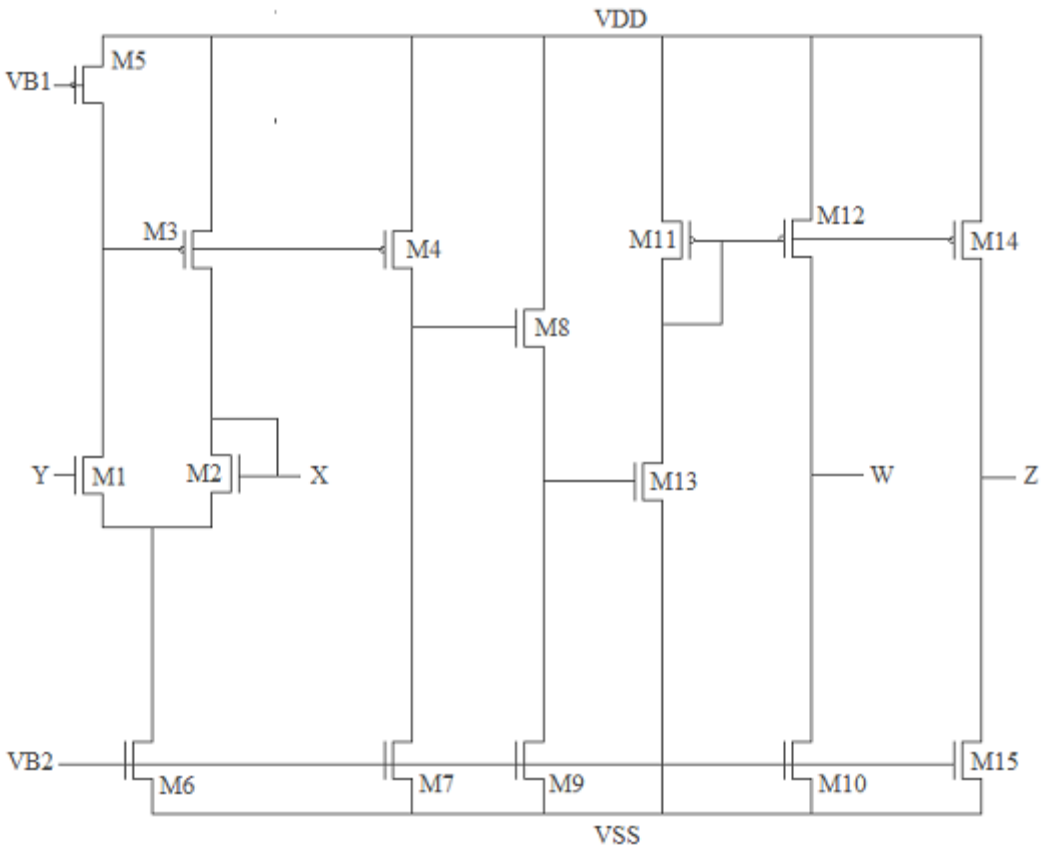


Fig. 2.5 CMOS realization of Architecture II.

2.2.3. THIRD REALIZATION

2.2.3.1. Architecture III

The third realization of OFCC with block diagram is shown in Fig. 2.6 [18]. In this realization the first CCII+ of the second realization is replaced by a CCII- and hence an inverting transimpedance amplifier is needed for proper operation.

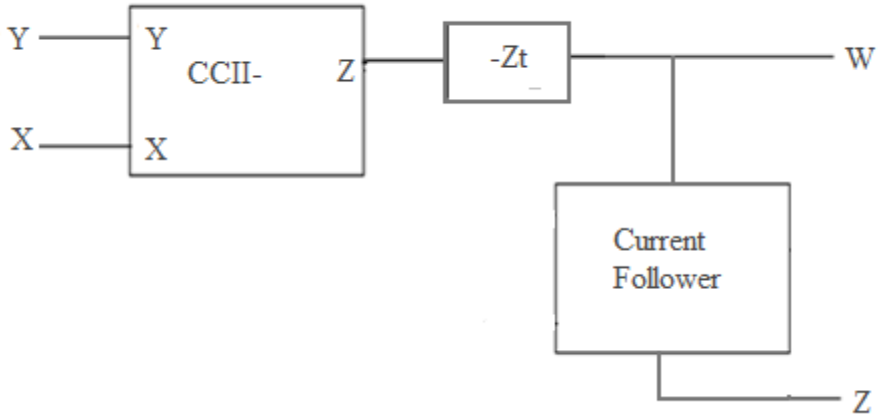


Fig. 2.6 Architecture III

2.2.3.2. Circuit Description

The third CMOS realization of the OFCC based on the block diagram shown in Fig. 2.6 is given in Fig. 2.7.The group of transistors (M1- M8), (M10 and M11), as well as (M12 and M13) are matched. Assuming that all the transistors operate in saturation region, the operation of the circuit can be explained as follows. The first CCII- (M1-M8) performs the voltage following action at the input port between terminals Y and X. It consists of two floating current source (FCS) blocks. The first FCS (M1-M4) produces two output-balanced currents Io1 and Io2 which are given by eqn. (2.1) where Vd =Vx-Vy. These two currents are forced to be zero by applying them to the input stage of the second FCS block and correspondingly from eqn. (2.1), the differential voltage Vd = 0. Hence, the voltage at terminal X will follow the voltage at terminal Y. The second FCS is responsible for conveying the X terminal current to the Z terminal. The positive current follower (M10-M13) performs the current following action at the output port between terminals W and Z. The transimpedance amplifier (M9 and M14) multiply the input current at terminal X with a large inverting transimpedance gain Zt to produce the output voltage at terminal W. The use of an inverting transimpedance amplifier is essential since the conveyed current at the gate terminal of M14 will be an inverted form of input current at terminal X. Hence, the inverting transimpedance amplifier is essential to provide an output voltage at terminal W directly proportional to the input current at terminal X. The transimpedance amplifier operation can be explained as follows. The input current at terminal X is conveyed by the CCII- to the gate terminal of M14. This current will flow in the equivalent parasitic impedance of this gate

terminal producing a voltage on it. The voltage is then amplified to produce the output voltage at terminal W.

$$I_{o1} = -I_{o2} = -\frac{1}{2} v_d \left(\sqrt{K_n}\sqrt{2I_B - \frac{K_n v_d^2}{4}} + \sqrt{K_P}\sqrt{2I_B - \frac{K_P v_d^2}{4}}\right) \quad (2.1)$$

Where,

$$K_n = \mu_n C_{ox} \frac{W_1}{L_1} \quad \text{and} \quad K_p = \mu_p C_{ox} \frac{W_3}{L_3} \quad (2.2)$$

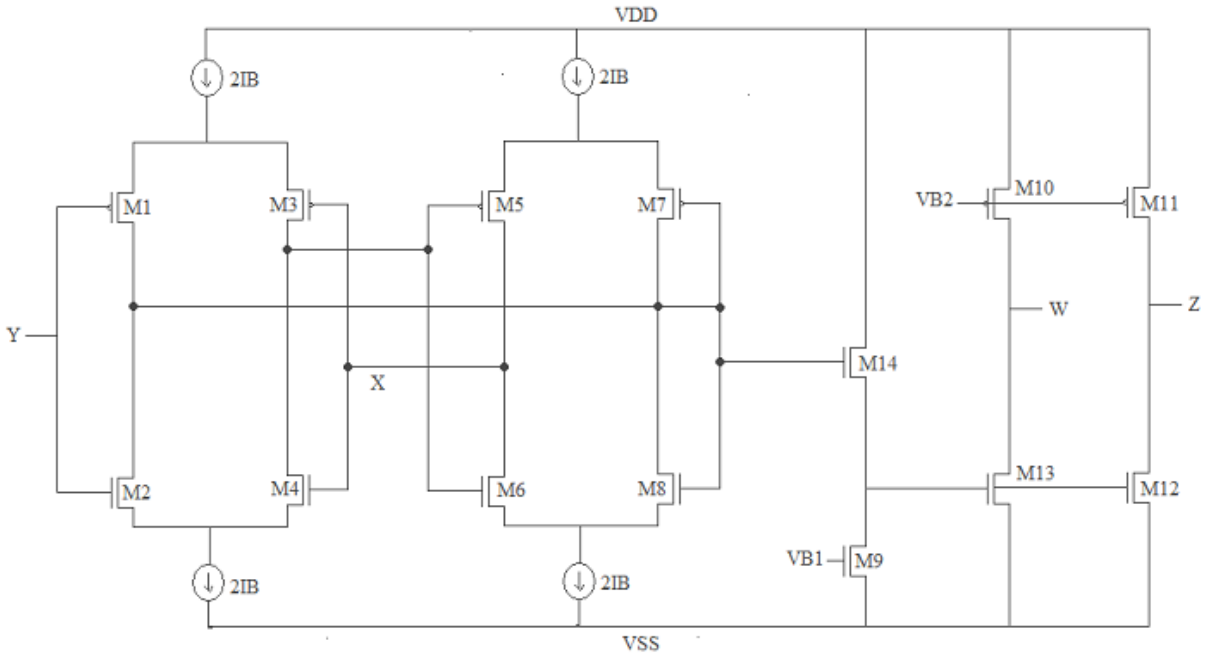


Fig. 2.7 CMOS realization of Architecture III

2.3. APPLICATIONS OF OFCC

In this work the OFCC with additional Z terminals is used. The block diagram is shown in Fig. 2.8.

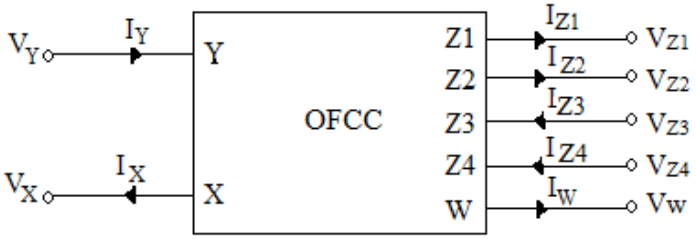


Fig. 2.8 OFCC block with additional Z terminals.

The port relations of the above mentioned block is explained by the following matrix.

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z1} \\ I_{Z2} \\ I_{Z3} \\ I_{Z4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z1} \\ V_{Z2} \\ V_{Z3} \\ V_{Z4} \end{bmatrix} \quad (2.4)$$

The current in terminal Iz1 and Iz2 is in phase with that of Iw whereas Iz3 and Iz4 are out of phase with Iw.

The CMOS implementation of OFCC is shown in Fig. 2.9 which is extension of Fig.2.5. The transistors M16-M17 are used to provide additional Z terminal whereas the cross coupled current mirror (M18 – M25) give negative current transfer. The aspect ratio of transistors are mentioned in Table 2.1. The OFCC applications given in the next section are simulated using this structure.

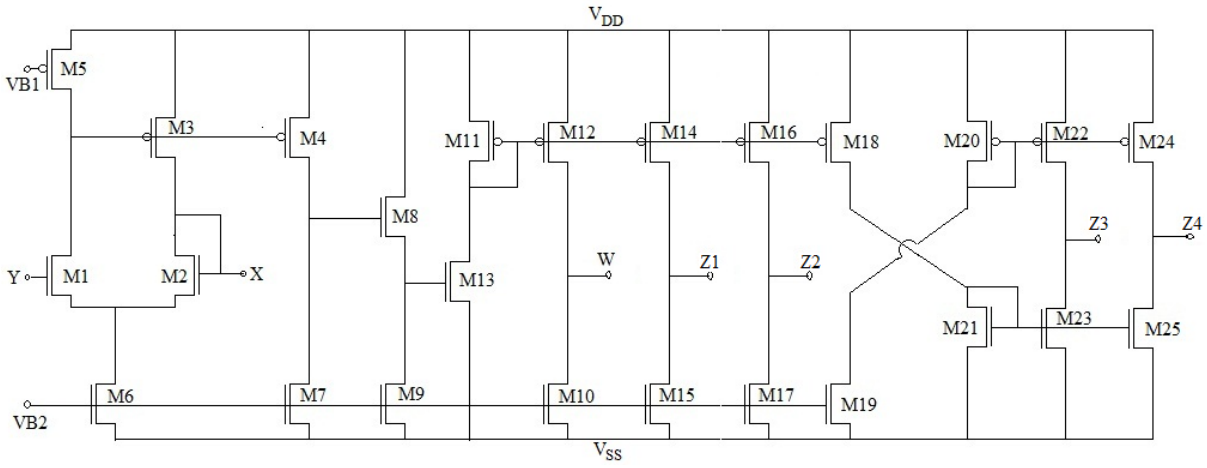


Fig 2.9 CMOS Schematic of OFCC

Table 2.1: Transistors aspect ratios of the circuit shown in Fig. 2.9[18]

Transistor	W (µm)/L (µm)
M1, M2	50/1
M3, M4, M11, M12, M14 M16, M18, M20, M22, M24	50/2.5
M5, M7, M10, M15, M17, M19 M21, M23, M25	20/2.5
M6, M8	40/2.5
M9, M13	100/2.5

2.3.1. TRANS-RESISTANCE AMPLIFIER

The trans- resistance amplifier configuration is shown in Fig. 2.10[18]. The trans- resistance gain can be obtained as follows:

$$Trans-resistance\ gain = \frac{V_{out}}{I_{in}} = -R1 \tag{2.5}$$

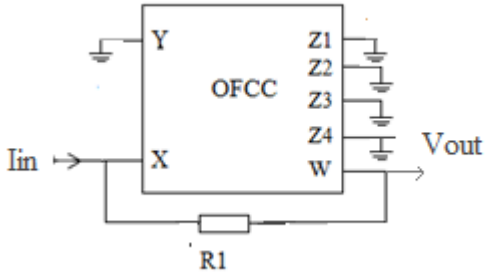


Fig. 2.10 Trans-resistance amplifier configuration using OFCC

Ideally the transimpedance gain Z_t is assumed to approach infinity. However, in practice, Z_t is a frequency dependent finite value. Using single pole model for transimpedance gain, Z_t (s) is expressed as [18].

$$Z_t(s) = \frac{Z_{to}}{1 + s/\omega_{tc}} \tag{2.6}$$

The parameter Z_{to} is the dc open loop transimpedance gain and ω_{tc} is the transimpedance cut off frequency. For high frequency applications, the transimpedance gain, Z_t (s) is approximated as

$$Z_t(s) \cong \frac{1}{sC_p} \tag{2.7}$$

Where

$$C_p = \frac{1}{Z_{to}\omega_{tc}} \tag{2.8}$$

Taking the effect of the finite transimpedance gain, Z_t, and using the finite transimpedance single pole model, the transresistance gain can be expressed as:

$$Trans-resistance\ gain = \frac{V_{out}}{I_{in}} = -R1\varepsilon(s) \quad (2.9)$$

Where, Ɛ(s) is the error function and it is given as

$$\varepsilon(s) = \frac{1}{1+sC_pR1} \quad (2.10)$$

Hence, for high frequency applications, compensation methods is needed for taking the error function into account A capacitor C =0.5pF (connected between the output terminal W and the input terminal Y) is used for compensating the error function

The trans-resistance amplifier is simulated for R1=1kΩ , 2kΩ , 5kΩ , 10kΩ and an input current of 1μA giving an output voltage of 1mV , 2mV, 5mV , 10mV respectively. The output frequency response of trans-resistance amplifier is shown in Fig. 2.11

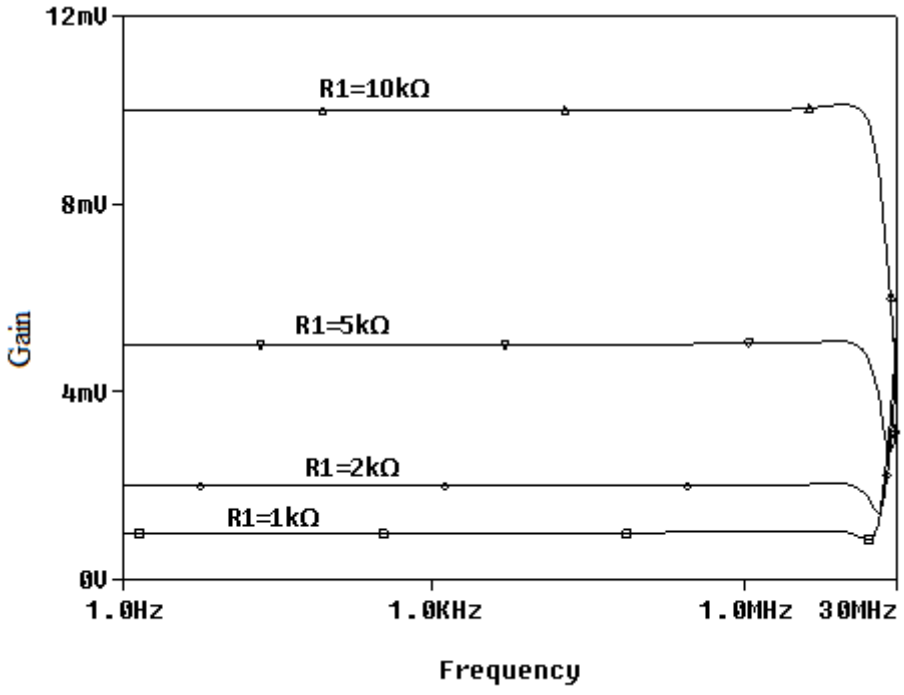


Fig. 2.11 Output frequency response of trans-resistance amplifier

2.3.2. TRANS-CONDUCTANCE AMPLIFIER

The trans- conductance amplifier configuration is shown in Fig. 2.12 [18]. The trans-conductance gain can be obtained as follows:

$$Trans-conductance\ gain = \frac{I_{out}}{V_{in}} = 1/R1 \tag{2.11}$$

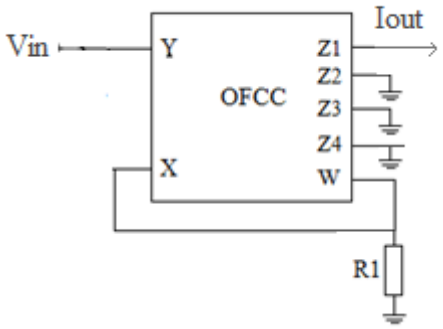


Fig. 2.12 Trans-conductance amplifier configuration using OFCC

Taking the effect of the finite transimpedance gain, Z_t, and using the finite transimpedance single pole model, the transconductance gain can be expressed as:

$$Trans-conductance\ gain = \frac{I_{out}}{V_{in}} = \frac{1}{R1}\varepsilon(s) \tag{2.12}$$

Where, Ɛ(s) is the error function and it is given as

$$\varepsilon(s) = \frac{1}{1+sC_pR1} \tag{2.13}$$

Hence, for high frequency applications, compensation methods is needed for taking the error function into account A capacitor C =0.5pF (connected between the output terminal W and the input terminal Y) is used for compensating the error function

The trans- conductance amplifier is simulated for R1=1kΩ , 2kΩ , 5kΩ , 10kΩ and an input voltage of 1mV giving an output current of 1µA , 0.5µA, 0.2µA , 0.1µA respectively. The output frequency response of trans- conductance amplifier is shown in Fig. 2.13

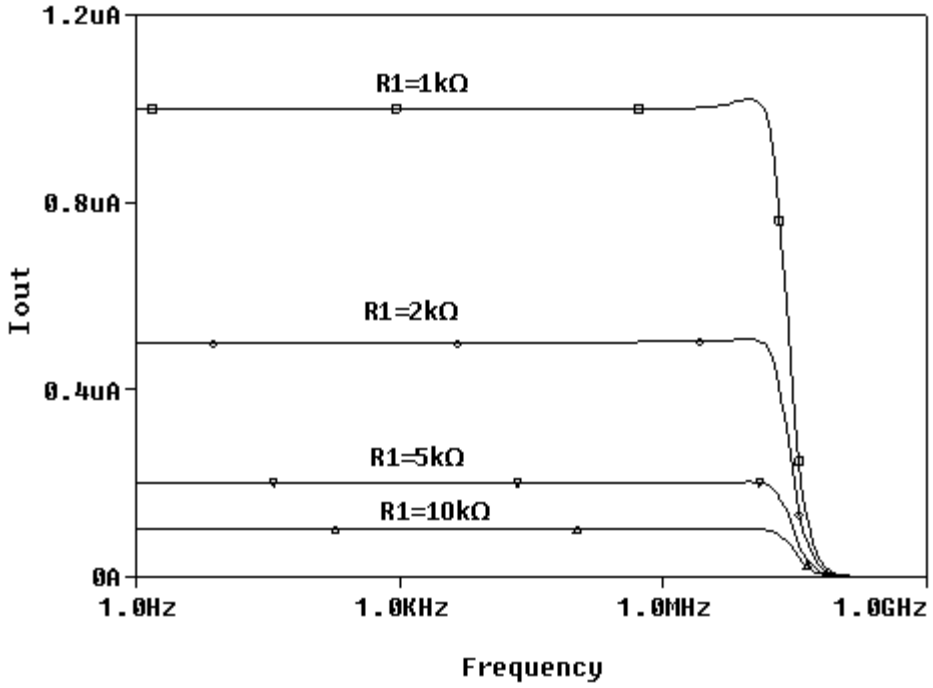


Fig. 2.13 Output frequency response of trans-conductance amplifier

2.3.3 CURRENT AMPLIFIER

The Current amplifier configuration is shown in Fig. 2.14. The gain of the amplifier can be obtained as follows:

$$gain = \frac{I_{out}}{I_{in}} = \frac{R1}{R2} \tag{2.14}$$

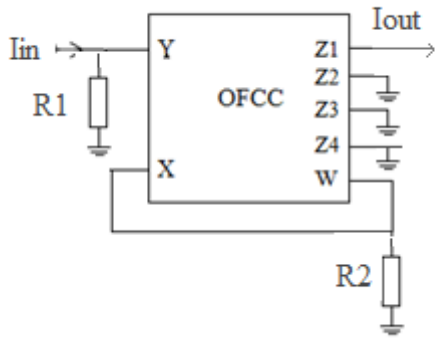


Fig. 2.14 Current amplifier configuration using OFCC

Taking the effect of the finite transimpedance gain, Z_t, and using the finite transimpedance single pole model, the transconductance gain can be expressed as:

$$gain = \frac{I_{out}}{I_{in}} = \frac{R1}{R2}\varepsilon(s) \tag{2.15}$$

Where, Ɛ(s) is the error function and it is given as

$$\varepsilon(s) = \frac{1}{1 + sC_pR2} \tag{2.16}$$

Hence, for high frequency applications, compensation methods is needed for taking the error function into account A capacitor C =0.5pF (connected between the output terminal W and the input terminal Y) is used for compensating the error function

The Current amplifier is simulated for R2=1kΩ and R1=1kΩ , 2kΩ , 5kΩ , 10kΩ and an input current of 1μA giving a gain of 1 , 2, 5 ,10 respectively. The output frequency response of current amplifier is shown in Fig. 2.15. Generally we find two configurations of an amplifier namely inverting and non-inverting and both having different architectures according to their configuration. Here the discussed OFCC structure has both the configurations in single architecture. As discussed above we have obtained the gain of amplifier for non-inverting configuration while taking output with Z1 terminal. The inverting configuration can be achieved by taking output from Z3 or Z4 terminal. Thus the above OFCC architecture proves its usefulness by allowing us to have two configurations in single structure.

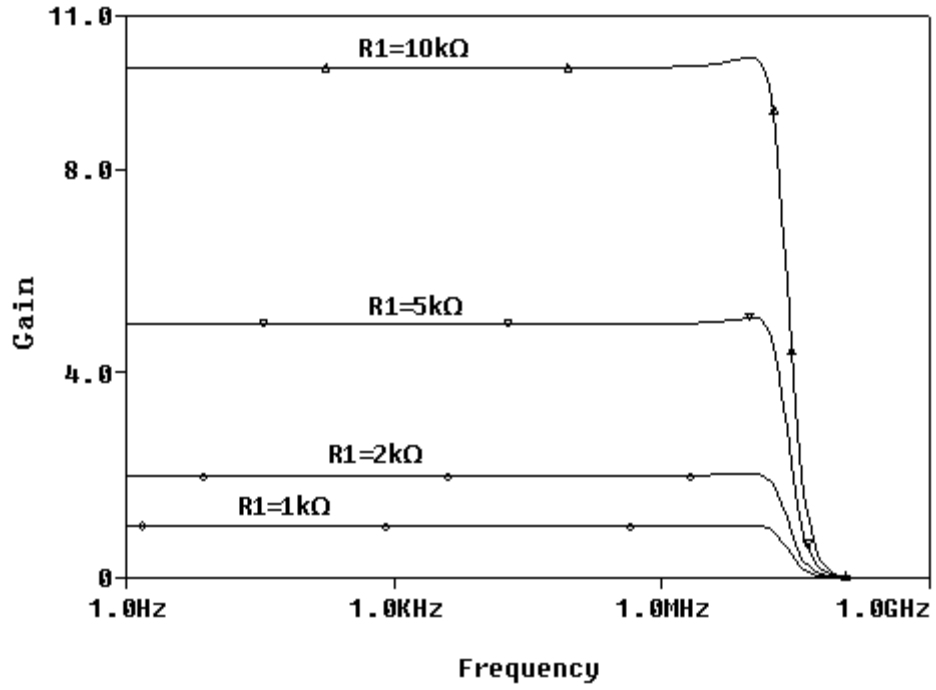


Fig. 2.15 Output frequency response of current amplifier

2.3.4. VOLTAGE AMPLIFIER

The voltage amplifier configuration is shown in Fig. 2.16. The gain of the amplifier can be obtained as follows:

$$gain = \frac{V_{out}}{V_{in}} = 1 + \frac{R2}{R1} \tag{2.17}$$

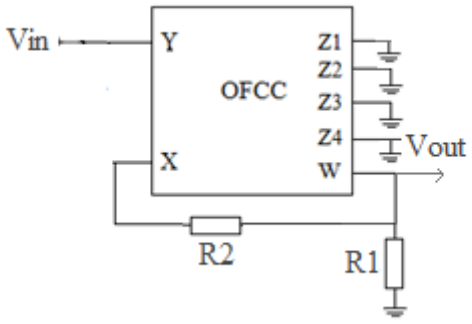


Fig. 2.16 Voltage amplifier configuration using OFCC

Taking the effect of the finite transimpedance gain, Z_t, and using the finite transimpedance single pole model, the transconductance gain can be expressed as:

$$gain = \frac{V_{out}}{V_{in}} = \left(1 + \frac{R2}{R1}\right)\varepsilon(s) \tag{2.18}$$

Where, Ɛ(s) is the error function and it is given as

$$\varepsilon(s) = \frac{1}{1 + sC_p R2} \tag{2.19}$$

Hence, for high frequency applications, compensation methods is needed for taking the error function into account A capacitor C =0.5pF (connected between the output terminal W and the input terminal Y) is used for compensating the error function

The voltage amplifier is simulated for R1=1kΩ and R2=1kΩ , 2kΩ , 5kΩ , 10kΩ and an input voltage of 1mV giving a gain of 2 , 3, 6 and 11 respectively. The output frequency response of voltage amplifier is shown in Fig. 2.17

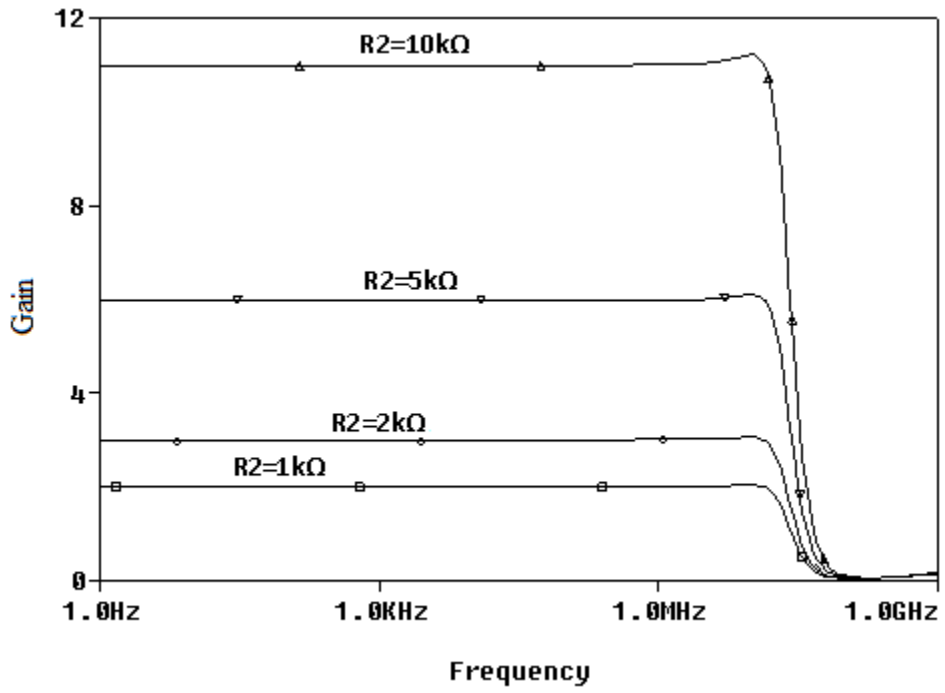


Fig. 2.17 Output frequency response of voltage amplifier.

2.3.5 INTEGRATOR

The integrator configuration is shown in Fig.2.18. The gain of integrator can be obtained as follows:

$$gain = \frac{I_{out}}{I_{in}} = \frac{R1/R2}{sC1R1 + 1} \tag{2.20}$$

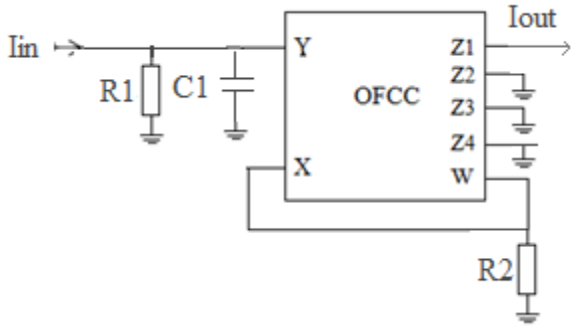


Fig. 2.18 Integrator configuration using OFCC

Taking the effect of the finite transimpedance gain, Z_t, and using the finite transimpedance single pole model, the transconductance gain can be expressed as:

$$gain = \frac{I_{out}}{I_{in}} = \frac{R1/R2}{sC1R1 + 1}\varepsilon(s) \tag{2.21}$$

Where, $\varepsilon(s)$ is the error function and it is given as

$$\varepsilon(s) = \frac{1}{1 + sC_pR2} \tag{2.22}$$

Hence, for high frequency applications, compensation methods is needed for taking the error function into account A capacitor C =0.5pF (connected between the output terminal W and the input terminal Y) is used for compensating the error function

The integrator configuration is simulated for an input current of 10µA , R1=10kΩ, R2=1kΩ and C1=1nF. The frequency response of integrator is shown in Fig. 2.19. From the frequency response we can observe that the output decreases as frequency increases which validates the expression obtained for gain and also the phase response shows that phase is approaching -90 degrees as expected.

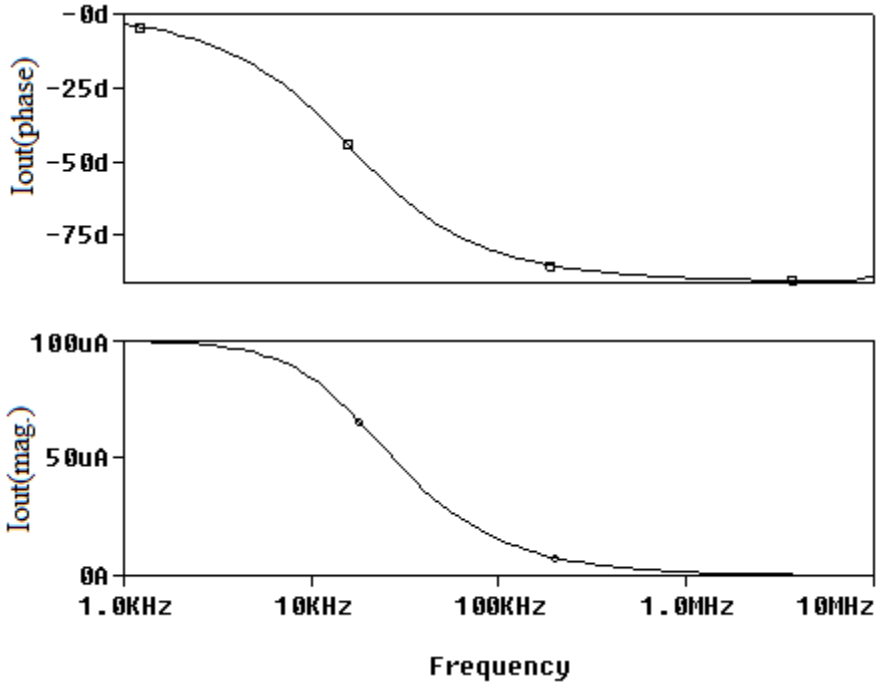


Fig. 2.19 Frequency response of integrator configuration

CHAPTER 3: OFCC BASED CURRENT MODE & TRANS-IMPEDANCE MODE FILTER

This chapter aims at presenting operational floating current conveyor (OFCC) based current mode universal filter and trans-impedance mode LP & BP filter. It employs only three OFCCs and two grounded capacitors and resistors each. The MOS based grounded resistors implementation is used, which adds feature of electronic tunability to the filter parameters. The chapter proceeds first with review of different current mode filters available and then the proposed filter architecture is given with transfer function of the various filter responses. Further, implementation of trans-impedance filter is shown and its responses are verified. The results are verified through PSPICE simulation.

3.1. INTRODUCTION

The development of current mode continuous time filters has received growing interest due to its applications in sampled data systems, communications, and control systems [22, 23]. This interest is also gaining strength with the requirement of circuits to operate at lower supply voltages and hence uses the current mode concept. Owing to the advantages of current mode filters, considerable research has directed towards the realization of single-input multiple output filters. A variety of current mode building blocks [25–31], namely, current follower trans-conductance amplifier [25], current conveyor [26–28], operational transconductance amplifier [29], Z copy current follower transconductance amplifier [30], and Z-Copy Current Inverter Transconductance amplifier [26], have been used to implement these filters [22, 25–43]. The structures—use excessive number of elements [27, 28, 34, 36] some of the references cited in [38], do not present low input impedance [22, 29, 34–37, 39]which is necessary for a current mode filter, employ multiple inputs to provide output responses [36, 37], put matching constraint [28, 31,36, 37] to obtain all five responses of universal filter, has less than three simultaneous output responses [25, 29, 36, 37,42], employ different type of active blocks [33, 40, 41]. Literature survey on OFCC based circuits [15–21] shows that voltage mode filter [15–17], variable gain amplifier [18], Wheatstone bridge [19], and instrumentation amplifier [20] and read out circuit [21] are available. The study of current mode filters [22, 25–43] shows that no OFCC based current mode filter is available in the literature. Therefore, this paper aims at presenting a single input four-output OFCC based current mode filter. The proposed filter uses three OFCCs, two grounded capacitors and two

grounded resistors. The resistors are implemented using MOSFETs so as to achieve electronic tunability of filter parameters. The filter enjoys low component spread and low sensitivity performance.

The proposed current mode filter can be used as trans-impedance mode filter which can provide low pass and band pass responses. The filter has electronic control of filter parameters and enjoys low sensitivity performance

3.2. CURRENT MODE FILTER

3.2.1. CIRCUIT DESCRIPTION

In this section the implementation of OFCC based current mode universal filter, as shown in Fig. 3.1 is proposed. It employs three OFCCs, two grounded capacitors and resistors each. The analysis of the circuit gives the following transfer functions

$$T_{LPF} = \frac{I_{LPF}}{I_{in}} = \frac{-1}{D(s)} \tag{3.1}$$

$$T_{BPF} = \frac{I_{BPF}}{I_{in}} = \frac{-sC_2R_2}{D(s)} \tag{3.2}$$

$$T_{HPF} = \frac{I_{HPF}}{I_{in}} = \frac{-s^2C_1C_2R_1R_2}{D(s)} \tag{3.3}$$

$$T_{NOTCH} = \frac{I_{NOTCH}}{I_{in}} = \frac{s^2C_1C_2R_1R_2 + 1}{D(s)} \tag{3.4}$$

Where,

$$D(s) = s^2C_1C_2R_1R_2 + sC_2R_2 + 1 \tag{3.5}$$

Thus the proposed circuit provides low pass, high pass, band pass and notch (band stop) response simultaneously without any modification in the circuit or connection of output currents. There is no matching constraint for realization of filter responses. It may be noted that the current I_{HPF} is not explicitly available at high impedance and therefore cannot be directly used. However, by connecting I_{NOTCH} and I_{LPF} the high pass response can be made available at high output impedance. Similarly, the all pass function can easily be obtained by

connecting band pass and notch output currents, i.e. $I_{AP} = I_{BP}+I_{NOTCH}$ and the corresponding transfer function is obtained as

$$T_{AP} = \frac{I_{AP}}{I_{in}} = \frac{s^2 C_1 C_2 R_1 R_2 - sC_2 R_2 + 1}{D(s)} \tag{3.6}$$

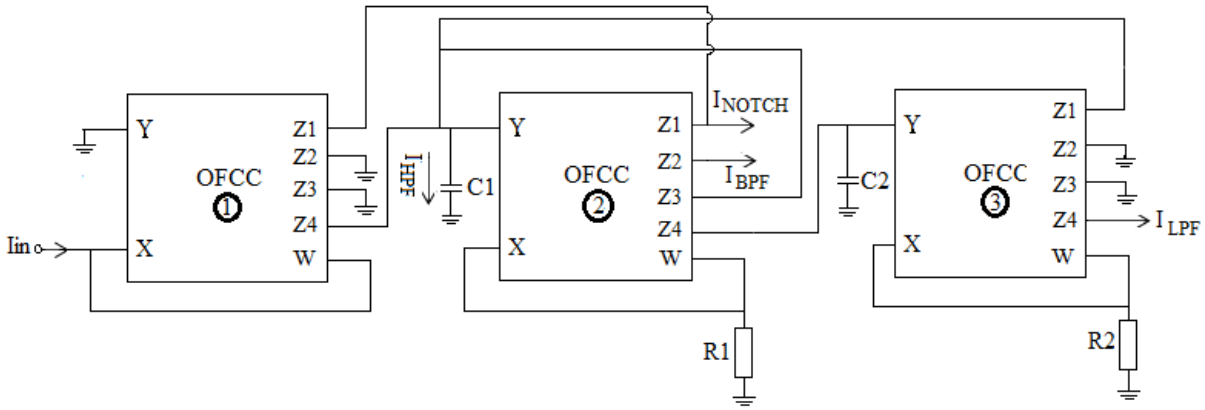


Fig. 3.1 Proposed OFCC based single input four output current mode filter.

All the responses are characterized by pole frequency (ω_0), bandwidth (ω_0/Q_0) and quality factor (Q_0) given as:

$$\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \tag{3.7}$$

$$BW = \frac{\omega_0}{Q_0} = \frac{1}{R_1 C_1} \tag{3.8}$$

$$Q_0 = \sqrt{\frac{R_1 C_1}{R_2 C_2}} \tag{3.9}$$

Equations (3.7)-(3.9) reveals that the pole frequency (ω_0) and quality factor (Q_0) can be adjusted by R_2, without disturbing (ω_0/Q_0). The orthogonal adjustability of (ω_0) and (Q_0) can be achieved by simultaneous adjustment of R_1 and R_2 such that the product R_1R_2 remains constant and the quotient R_1/R_2 varies and vice versa. With moderate values of ratios of component values ((R_1/R_2) = (C_1/C_2) = Q_0) i.e. from low component spread [45], high values of Q-factor can be obtained. Hence the component spread is of the order of$\sqrt{Q_0}$.

The proposed filter uses grounded resistors which can easily be implemented using the MOS based structure given in Fig.3.2 [44]. It uses two diode connected matched transistors, operating in saturation region. Assuming $V_1 = - V_2$, the value of resistor is given by:

$$R = \frac{\mathrm{L}}{2\mu C_{ox} W (V_1 - V_T)} \tag{3.10}$$

Where, μ is carrier mobility, C_{ox} is gate capacitance per unit area, V_T is threshold voltage and W, L are the channel length and width respectively.

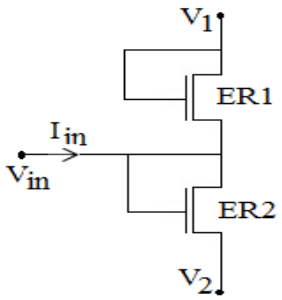


Fig. 3.2 MOS realization of a resistor

3.2.2. SIMULATION RESULTS

3.2.2.1. Frequency Domain

To verify the functionality of the proposed OFCC based current mode filter, SPICE simulations have been carried out using 0.5 μm CMOS process model provided by MOSIS (AGILENT) and CMOS schematic of Fig. 2.9 with power supply voltage of $V_{DD} = -V_{SS} = 1.5$ V and $V_{B1} = -V_{B2} = 0.8$ V. The aspect ratios of the transistor are reported in Table 2.1[18].

The simulations have been performed for a pole frequency of 1.59 MHz with component values as $C_1 = C_2 = 100$ pF and MOS based resistors of value 1 kΩ by selecting bias voltages as ± 1.310V. Figure 3.3 shows the simulation results for low pass, band pass and high pass responses. The phase and magnitude plots for notch and all pass responses are depicted in Fig. 3.4 and 3.5 respectively. The responses confirm the theoretical predictions.

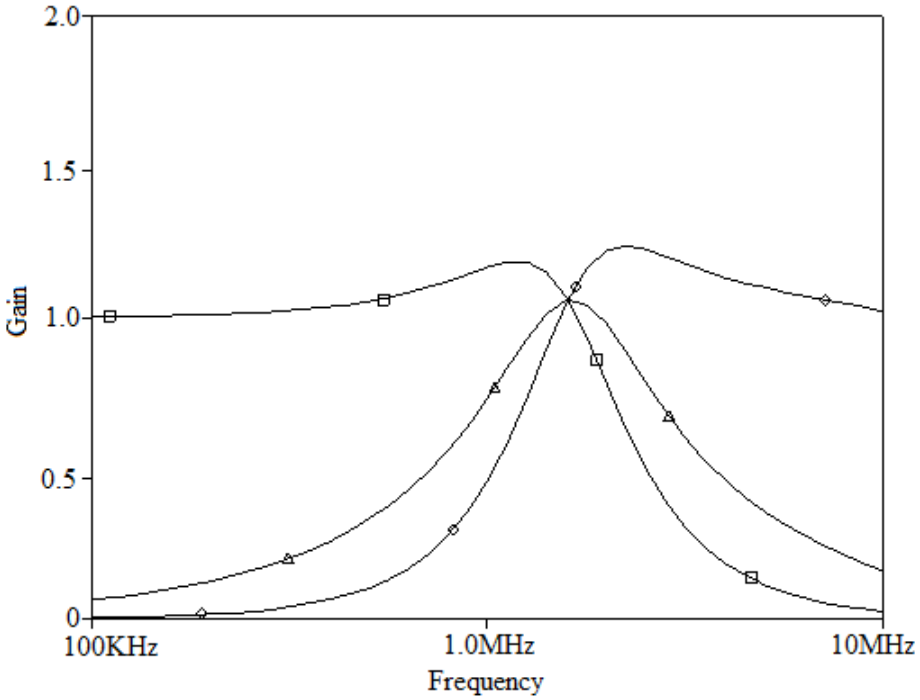


Fig. 3.3 Simulated low pass, band pass and high pass responses

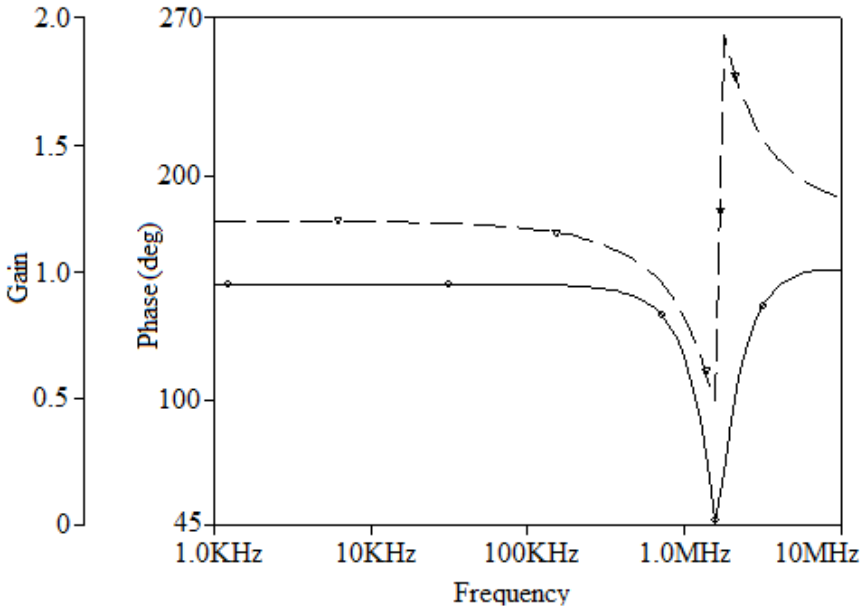


Fig. 3.4 Magnitude and phase plot for notch response

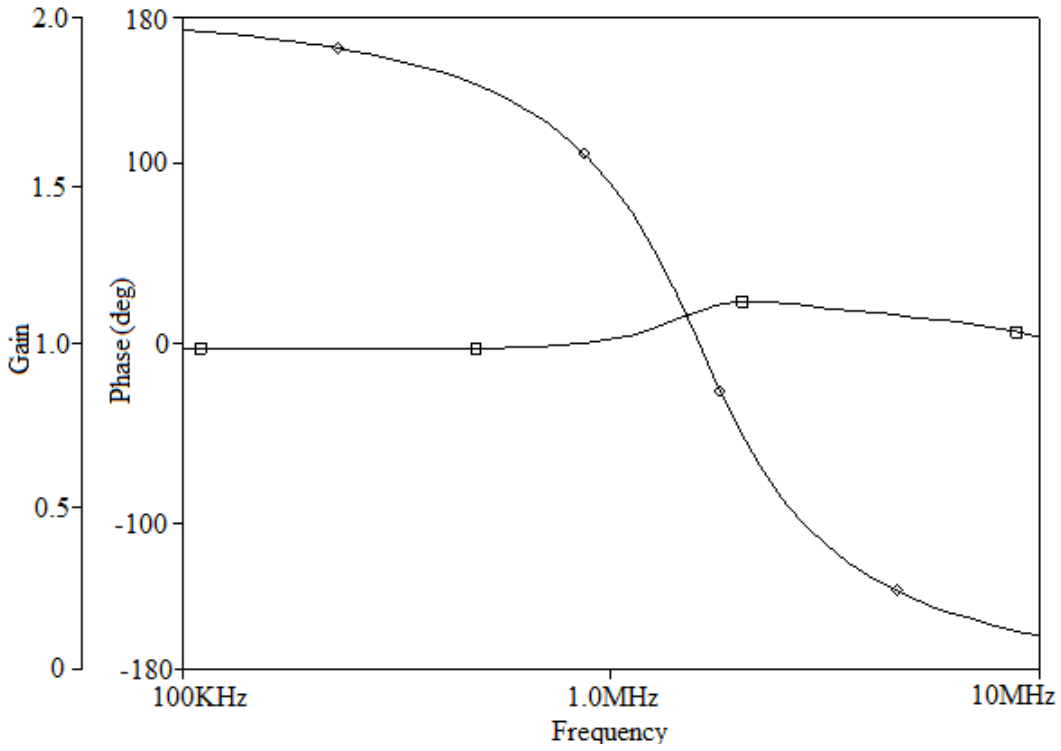


Fig. 3.5 Magnitude and phase plots for allpass response

The orthogonal adjustment of f_0 with Q_0 is depicted in Fig. 3.6 where the value of $Q_0 = 1$ is considered. The capacitors C_1 and C_2 are taken as 100 pF and the bias voltages along with the resistor values for different values of f_0 as given in Table 3.1. Figure 3.7 shows orthogonal adjustment of Q_0 with f_0 = 800 kHz. The values of Q_0 for constant value of f_0 as obtained with $C_1 = C_2$ = 100 pF and bias voltages and resulting resistor values are listed in Table 3.2.

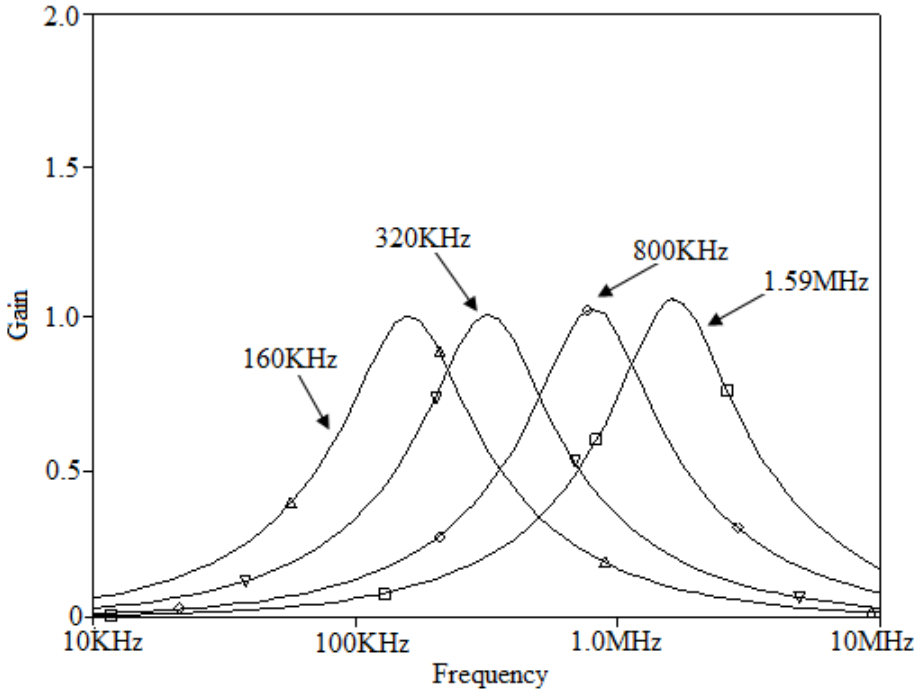


Fig. 3.6 Tuning of f_0

Table 3.1: Bias voltages/ Resistor values for orthogonal adjustment of f_0 with Q_0

V_{11}^*(V)	V_{21}^*(V)	R1(KΩ)	V_{12}^*(V)	V_{22}^*(V)	R2(KΩ)	Q	F(KHz)
1.310	-1.310	1	1.310	-1.310	1	1	1590
0.869	-0.869	2	0.869	-0.869	2	1	800
0.726	-0.726	5	0.726	-0.726	5	1	320
0.711	-0.711	10	0.711	-0.711	10	1	160

* V_{1i} and V_{2i} refer to bias voltages corresponding to resistance R_i

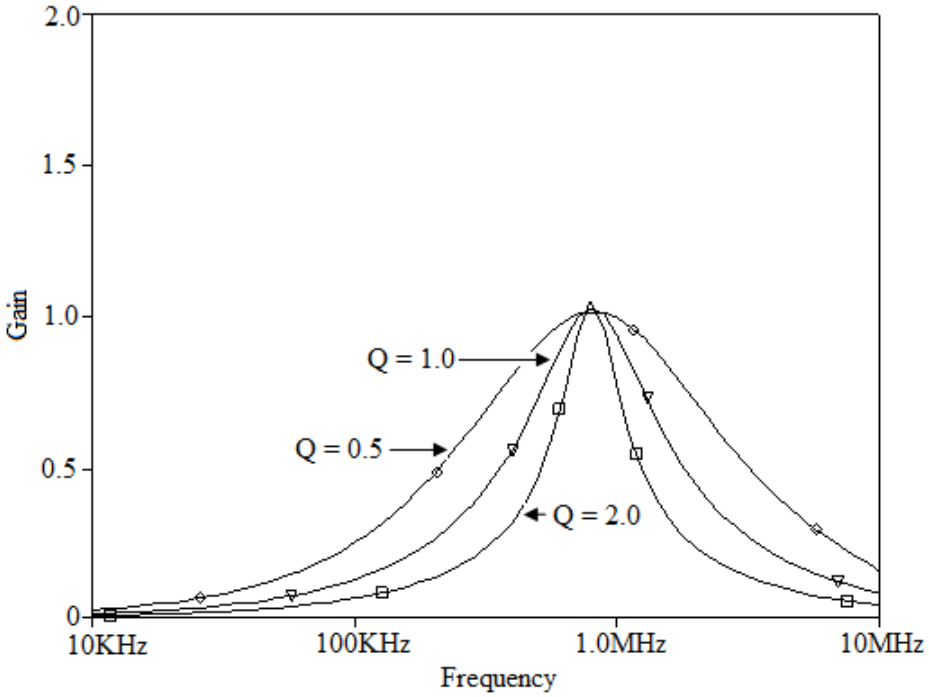


Fig. 3.7 Tuning of Q_0

Table 3.2: Bias voltages/ Resistor values for orthogonal adjustment of Q_0 with f_0

V_{11}^*(V)	V_{21}^*(V)	R1(KΩ)	V_{12}^*(V)	V_{22}^*(V)	R2(KΩ)	C1(nF)	C2(nF)	Q	F(KHz)
1.310	-1.310	1	0.869	-0.869	2	0.1	0.2	0.5	800
0.869	-0.869	2	0.869	-0.869	2	0.1	0.1	1	800
0.869	-0.869	2	1.310	-1.310	1	0.2	0.1	2	800

* V_{1i} and V_{2i} refer to bias voltages corresponding to resistance R_i

3.2.2.2. Time Domain

To study the time domain behaviour of the proposed filter, an input sinusoidal signal of 159 KHz frequency and amplitude 2 µA is applied to the low pass filter with pole frequency 1.59MHz. The transient response for low pass output is shown in Fig. 3.8. To show the effectiveness of proposed filter a mixed sinusoidal signals of frequencies of 30 KHz, 300 KHz and 3 MHz having amplitude of 2 µA each is applied at the input of the filter. The transient response with its spectrum for input and output signals is shown in Fig. 3.9 (a) and (b). It is clear that the 300 KHz signal is significantly attenuated and 3 MHz signal is completely filtered.

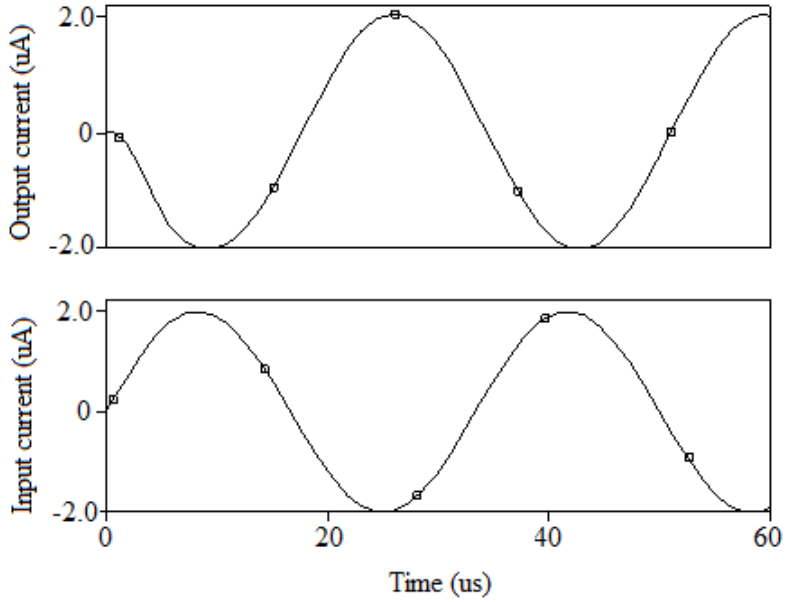
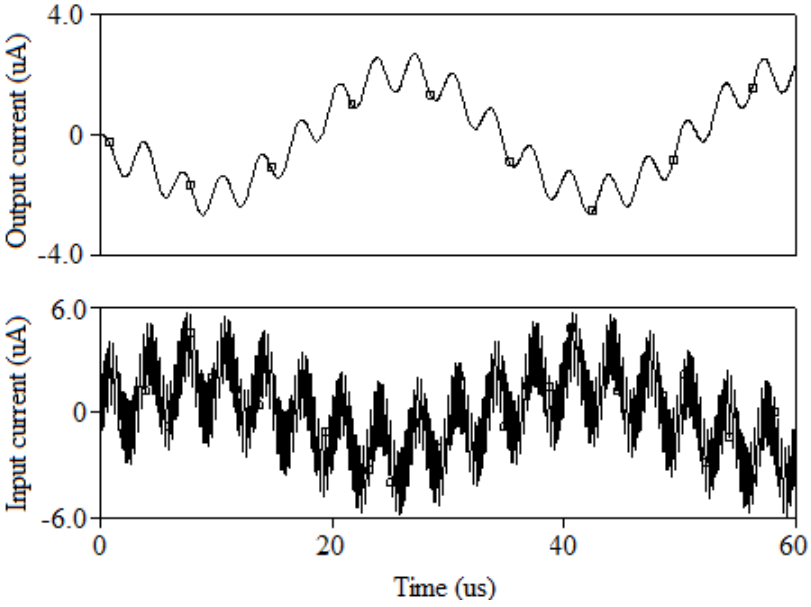
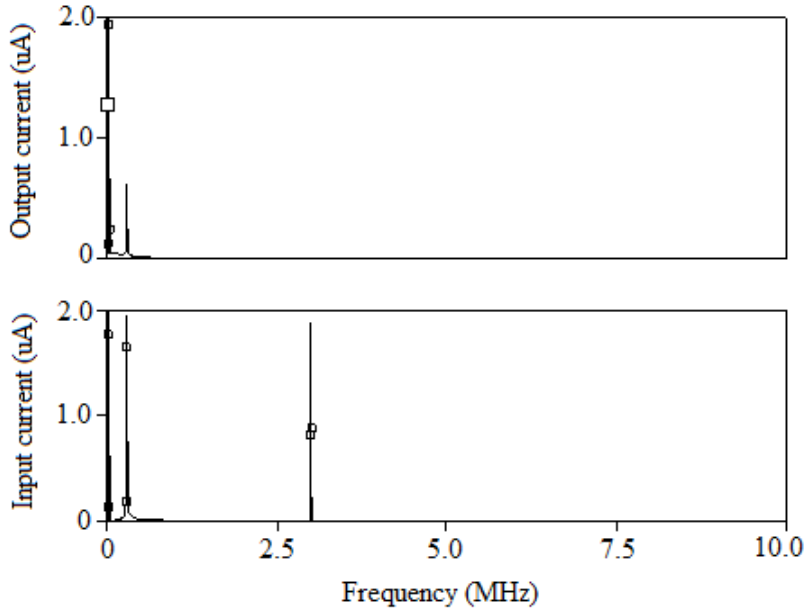


Fig. 3.8 Transient response for low pass output



(a)



(b)

Fig. 3.9 (a) Transient response of input and output signals

(b) Spectrum of input and output signals

3.2. 3.SENSITIVITY ANALYSIS

The sensitivity analysis of the proposed circuit is as follows:

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_2}^{Q} = S_{C_2}^{Q} = -\frac{1}{2},$$

$$S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{R_2}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}$$

Thus the all passive sensitivities are not more than unity in magnitude. So the proposed filter circuit can be classified as insensitive.

3.3 TRANS-IMPEDANCE MODE FILTER

3.3.1. CIRCUIT DESCRIPTION

In this section the implementation of OFCC based trans-impedance mode filter, as shown in Fig. 3.10 is proposed. It employs three OFCCs, two grounded capacitors and resistors each. The analysis of the circuit gives the following transfer functions

$$T_{LPF} = \frac{V_{LPF}}{I_{in}} = \frac{-R_2}{D(s)} \tag{3.11}$$

$$T_{BPF} = \frac{V_{BPF}}{I_{in}} = \frac{-SC_2R_2R_1`}{D(s)} \tag{3.12}$$

Where,

$$D(s) = s^2C_1C_2R_1R_2 + sC_2R_2 + 1$$

Both the responses are characterized by same pole frequency (ω_0), bandwidth (ω_0/Q_0) quality factor (Q_0) obtained for current mode filter and given in eqn. (3.7), (3.8) and (3.9) respectively.

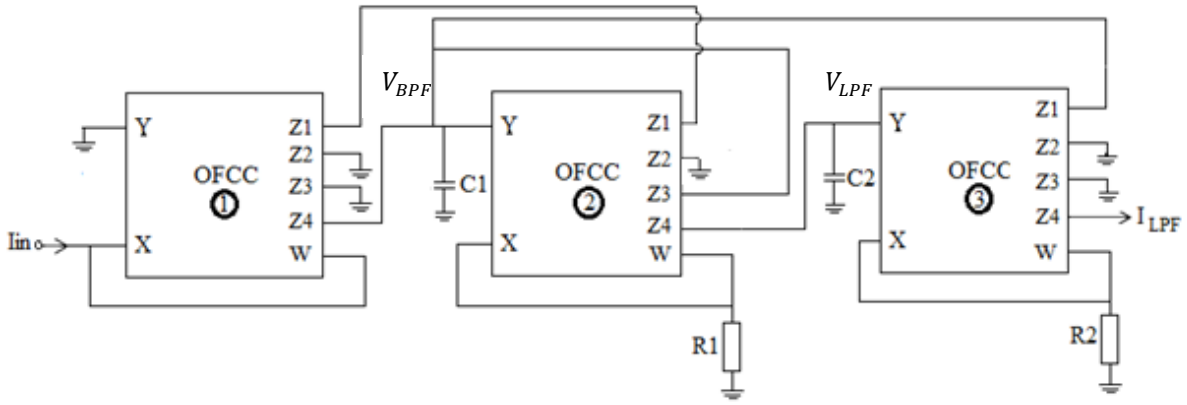


Fig. 3.10 Proposed OFCC based single input two output trans-impedance filter

The above proposed filter also has grounded resistors which can be implemented using MOS based structure as discussed in 3.2.

The filter also enjoys the same performance characteristics of current mode filter proposed in section 3.2 regarding orthogonal adjustment of ω_0 and Q_0 and low component spread giving high Q factor.

3.3.2. SIMULATION RESULTS

The simulations have been performed for a pole frequency of 1.59 MHz with component values as $C_1 = C_2 = 100$ pF and MOS based resistors of value 1 kΩ by selecting bias voltages as ± 1.310V. Figure 3.11 shows the simulation results for low pass response, and the band pass response is shown in Fig. 3.12. The responses confirm the theoretical predictions.

3.3. 3.SENSITIVITY ANALYSIS

The sensitivity analysis of the proposed circuit is as follows:

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_2}^{Q} = S_{C_2}^{Q} = -\frac{1}{2},$$

$$S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{R_2}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}$$

Thus the all passive sensitivities are not more than unity in magnitude. So the proposed filter circuit can be classified as insensitive.

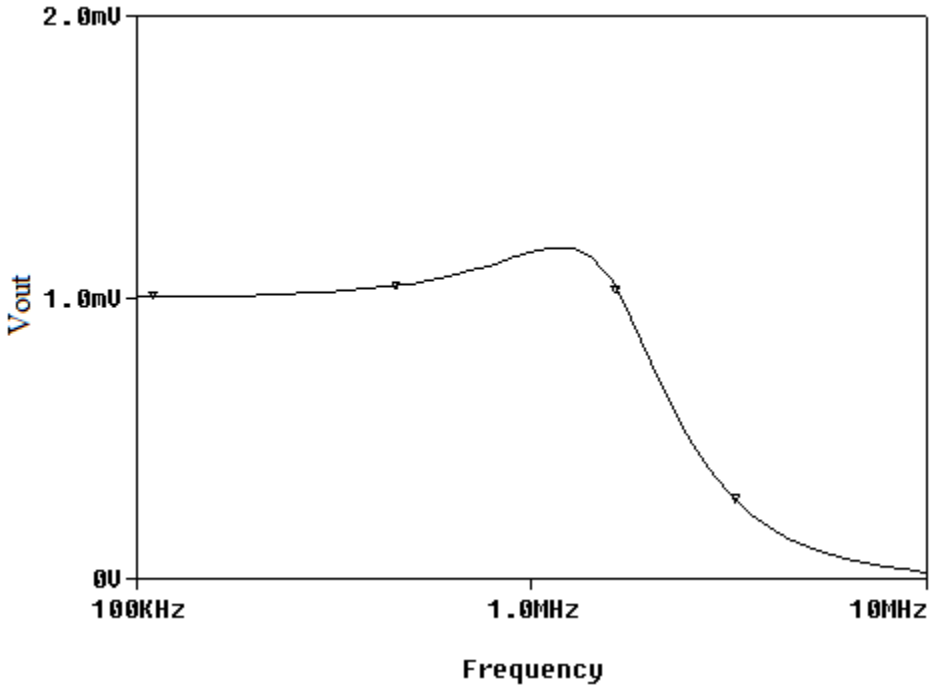


Fig. 3.11 Simulated low pass response of trans-impedance filter

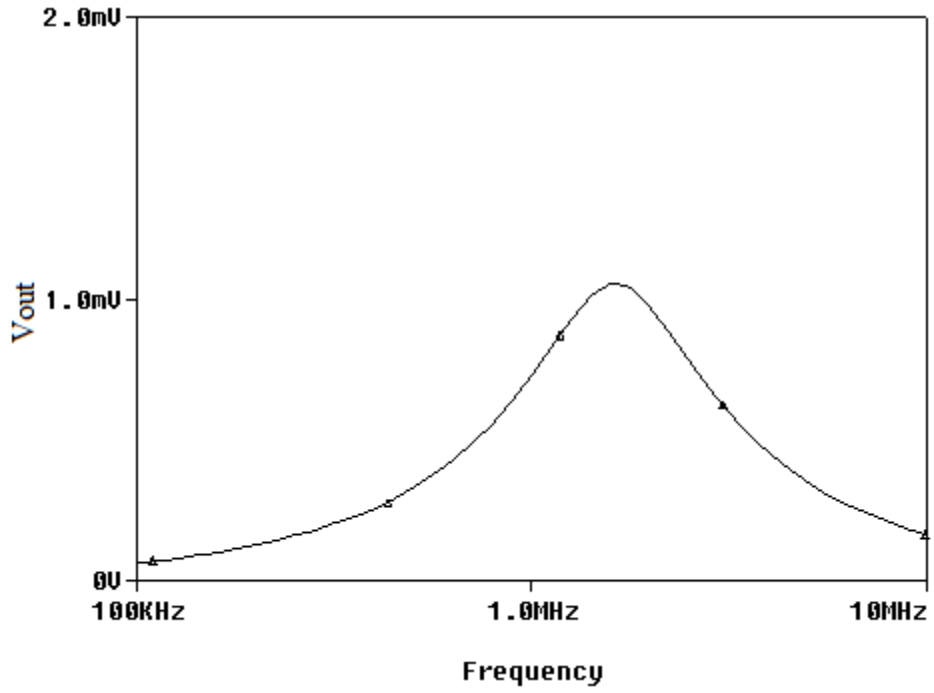


Fig. 3.12 Simulated band pass response of trans-impedance filter

CHAPTER 4: OFCC BASED TRANS-ADMITTANCE MODE & VOLTAGE MODE FILTER

This chapter aims at presenting operational floating current conveyor (OFCC) based trans-admittance mode universal filter and voltage mode LP & BP filter. It employs only three OFCCs, two grounded capacitors and three resistors. The MOS based grounded resistors implementation is used, which adds feature of electronic tunability to the filter parameters. The chapter proceeds first with review of different trans-admittance mode filters available and then the proposed filter architecture is given with transfer function of the various filter responses. Further, implementation of voltage mode filter is shown and its responses are verified. The results are verified through PSPICE simulation.

4.1. INTRODUCTION

The trans-admittance mode filter , where input is voltage and the output is taken in current form , is an important filter configuration. Its useful aspect is that, when we have a voltage mode filter and its output is to be fed to a current input device then we need extra circuitry to perform this operation. But the availability of trans-admittance mode filter obviates this need of extra circuitry and can be directly connected to such device [46]. A variety of current mode building blocks[46-54], namely current conveyors[46, 49, 50, 51, 52], positive four terminals floating nullors (PFTFN) [47], op-amp[48], current differencing transconductance amplifier[50] and modified current backward transconductance amplifier (MCBTA) [54] have been used to implement the trans-admittance mode filter.

In this chapter we present an OFCC based trans-admittance mode filter. The filter architecture comprises of three OFCC blocks, three resistors and two capacitors each being grounded. The resistors can be implemented with mos structure as they are grounded which adds electronic tunability to the circuit[44].

The proposed trans-admittance mode filter can be used as voltage mode filter which can provide low pass and band pass responses. The filter has electronic control of filter parameters and enjoys low sensitivity performance

4.2. TRANS-ADMITTANCE MODE FILTER

4.2.1. CIRCUIT DESCRIPTION

In this section OFCC based trans-admittance mode (voltage input and current output) universal filter is proposed. The architecture of the proposed filter is as shown in Fig. 4.1. It employs three OFCCs, two capacitors and three resistors while each capacitor and resistor is grounded. The analysis of the circuit gives the following transfer functions:

$$T_{LPF} = \frac{I_{LPF}}{V_{in}} = \frac{1/R_x C_1 C_2 R_1 R_2}{D(s)} \tag{4.1}$$

$$T_{BPF} = \frac{I_{BPF}}{V_{in}} = \frac{s/R_x C_1 R_1}{D(s)} \tag{4.2}$$

$$T_{HPF} = \frac{I_{HPF}}{V_{in}} = \frac{(s^2)/R_x}{D(s)} \tag{4.3}$$

$$T_{NOTCH} = \frac{I_{NOTCH}}{V_{in}} = -\frac{(s^2 + 1/C_1 C_2 R_1 R_2)/R_x}{D(s)} \tag{4.4}$$

Where,

$$D(s) = s^2 + s/C_1 R_1 + 1/C_1 C_2 R_1 R_2 \tag{4.5}$$

Thus the proposed circuit provides low pass, high pass, band pass and notch (band stop) response simultaneously. It may be noted that the current I_{HPF} is available through the capacitor and therefore cannot be directly used. However, by connecting I_{NOTCH} and $I_{LPF}$the high pass response can be made available at high output impedance. Similarly, the all pass function can easily be obtained by connecting band pass and notch output currents, i.e. $I_{AP} = I_{BP} + I_{NOTCH}$ and the corresponding transfer function is obtained as

$$T_{AP} = \frac{I_{AP}}{V_{in}} = -\frac{\frac{\left(s^2 - \frac{s}{C_1 R_1} + \frac{1}{C_1 C_2 R_1 R_2}\right)}{R_x}}{D(s)} \tag{4.6}$$

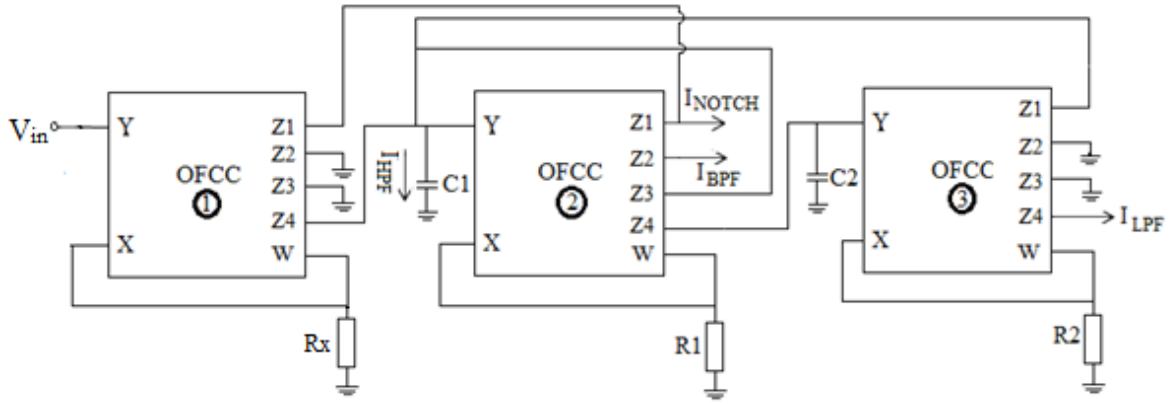


Fig. 4.1 Proposed OFCC based Trans-admittance mode filter

All the responses have characteristic pole frequency (ω_0), bandwidth (ω_0/Q_0) and quality factor (Q_0) given as:

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}} \tag{4.7}$$

$$BW = \frac{\omega_0}{Q_0} = \frac{1}{C_1 R_1} \tag{4.8}$$

$$Q_0 = \sqrt{\frac{C_1 R_1}{C_2 R_2}} \tag{4.9}$$

The above proposed filter also has grounded resistors which can be implemented using MOS based structure as discussed in 3.2.1.

The filter also enjoys the same performance characteristics of current mode filter proposed in chapter 3 regarding orthogonal adjustment of ω_0 and Q_0 and low component spread giving high Q factor.

4.2.2. SIMULATION RESULTS

4.2.2.1. Frequency Domain

To verify the functionality of the proposed OFCC based trans-admittance mode mode filter, SPICE simulations have been carried out using 0.5 µm CMOS process model provided by MOSIS (AGILENT) and CMOS schematic of Fig. 2.9 with power supply voltage of V_{DD} = -V_{SS} = 1.5 V and V_{B1} = -V_{B2} = 0.8 V. The aspect ratios of the transistor are reported in Table2.1[18].

The simulations have been performed for a pole frequency of 1.59 MHz with component values as C_1 = C_2 = 100 pF and MOS based resistors of value 1 kΩ by selecting bias voltages as ± 1.310V. Figure 4.2 shows the simulation results for low pass and high pass responses. The response of notch and band pass filter is depicted in Fig. 4.3. The magnitude and phase plots of all pass filter is shown in Fig. 4.4. The responses confirm the theoretical predictions.

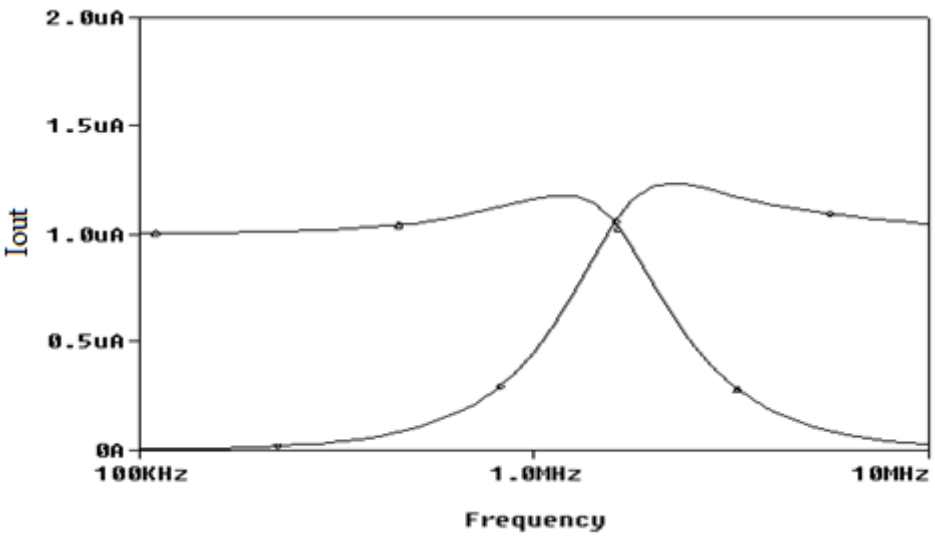


Fig. 4.2 Simulated low pass and high pass responses

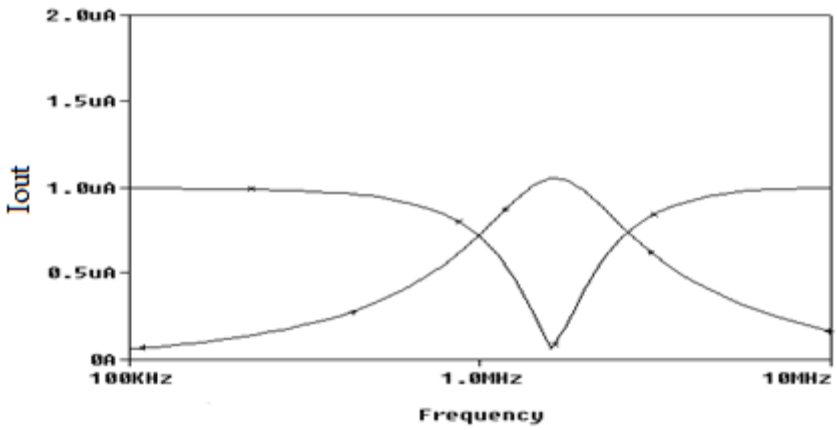


Fig. 4.3 Simulated band pass and notch responses

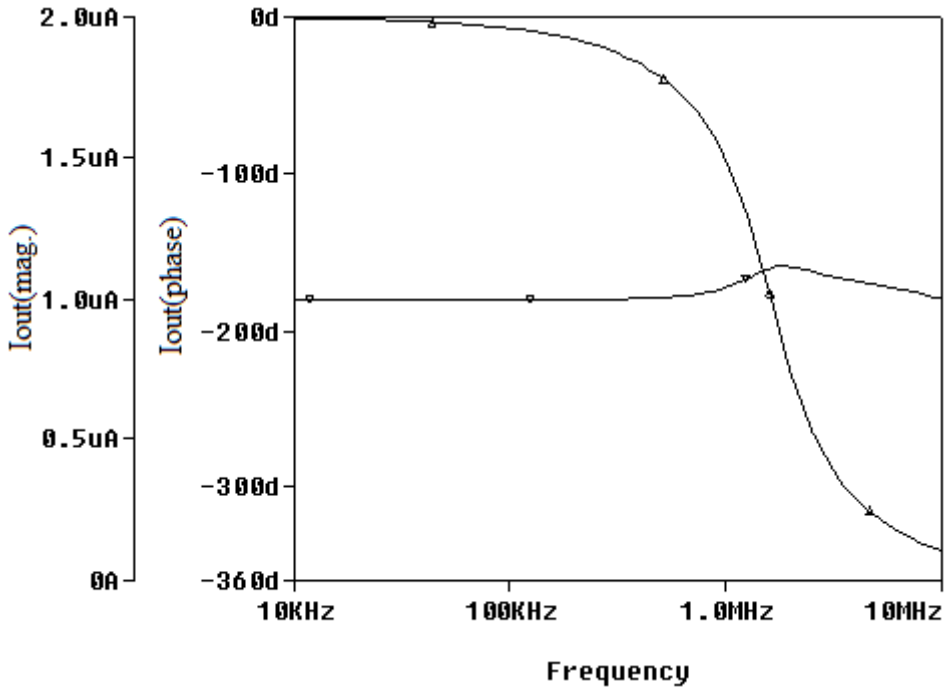


Fig. 4.4 Magnitude and phase plots for all pass response

The orthogonal adjustment of f_0 with Q_0 is depicted in Fig. 4.5 where the value of $Q_0 = 1$ is considered. The capacitors C_1 and C_2 are taken as 100 pF and the bias voltages along with the resistor values for different values of f_0 as given in Table 3.1. Figure 4.6 shows orthogonal adjustment of Q_0 with f_0 = 800 kHz. The values of Q_0 for constant value of f_0 as obtained with $C_1 = C_2$ = 100 pF and bias voltages and resulting resistor values are listed in Table 3.2.

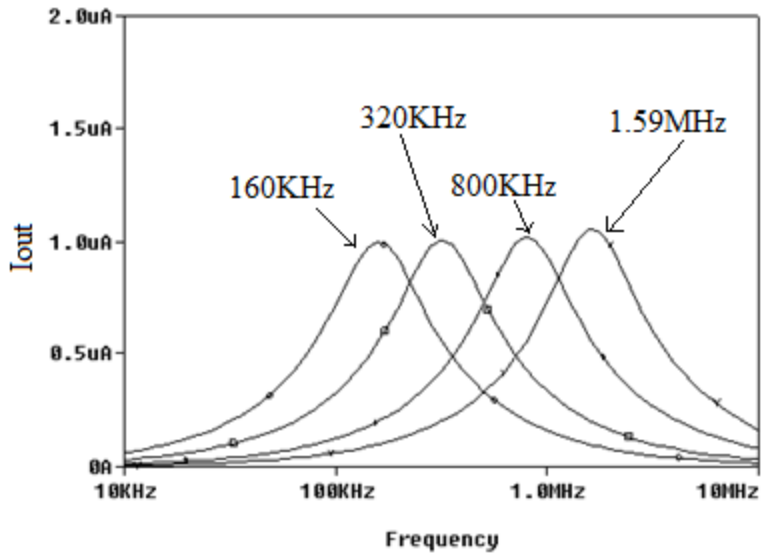


Fig. 4.5 Tuning of f_0

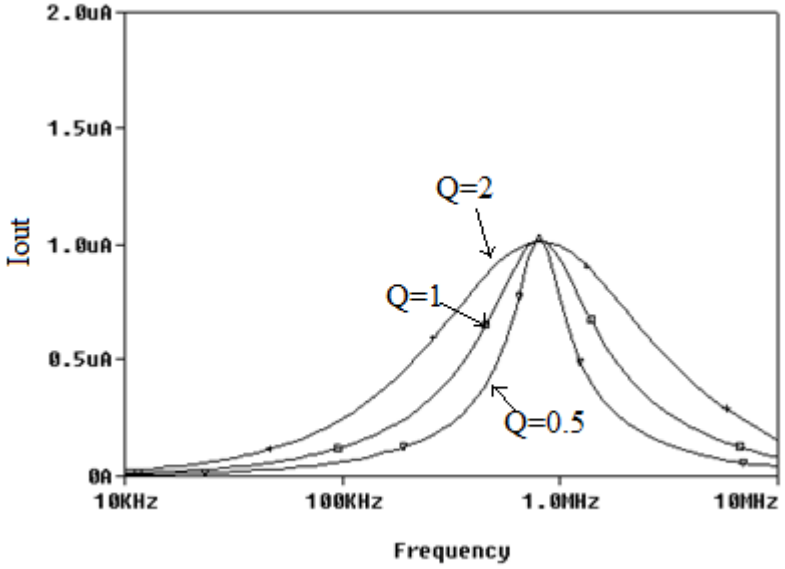


Fig. 4.6 Tuning of Q_0

4.2.2.2. Time Domain

To study the time domain behaviour of the proposed filter, an input sinusoidal signal of 159 KHz frequency and amplitude 2 µA is applied to the low pass filter with pole frequency 1.59MHz. The transient response for low pass output is shown in Fig. 4.7. To show the effectiveness of proposed filter a mixed sinusoidal signals of frequencies of 30 KHz, 300 KHz and 3 MHz having amplitude of 2 µA each is applied at the input of the filter. The transient response with its spectrum for input and output signals is shown in Fig. 4.8 (a) and

(b). It is clear that the 300 KHz signal is significantly attenuated and 3 MHz signal is completely filtered.

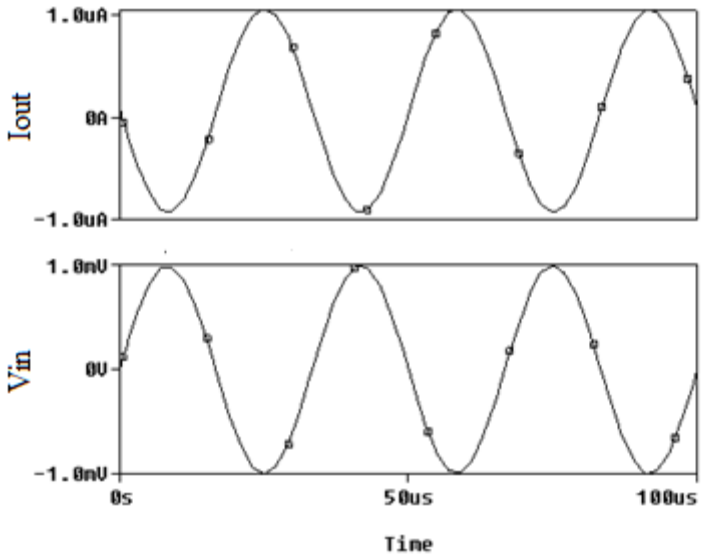
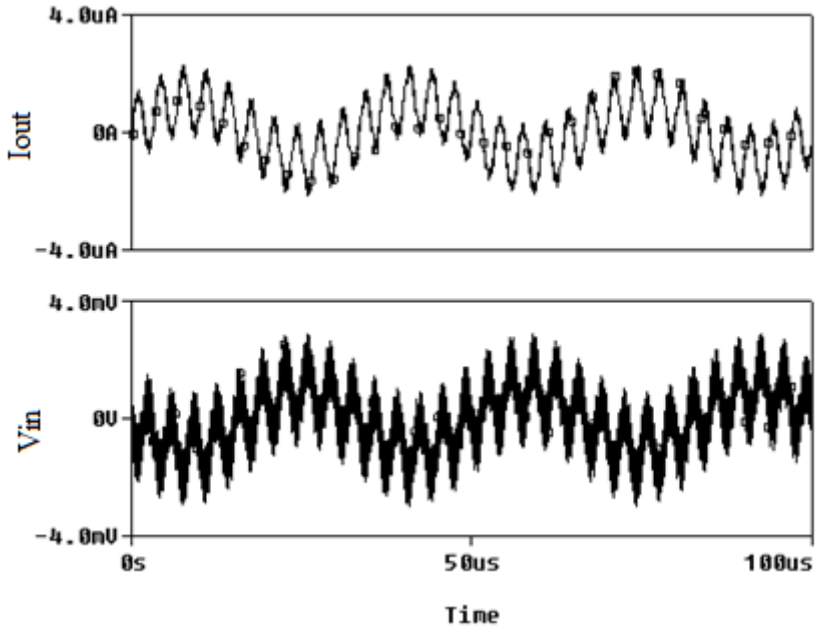
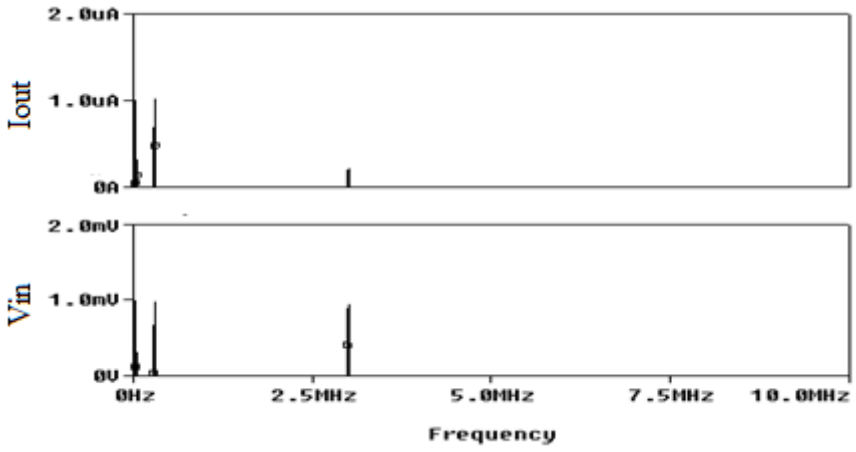


Fig. 4.7 Transient response for low pass output



(a)



(b)

Fig. 4.8 (a) Transient response of input and output signals

(b) Spectrum of input and output signals

4.2.3. SENSITIVITY ANALYSIS

The sensitivity analysis of the proposed circuit is as follows:

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_2}^{Q} = S_{C_2}^{Q} = -\frac{1}{2},$$

$$S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{R_2}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}$$

Thus the all passive sensitivities are not more than unity in magnitude. So the proposed filter circuit can be classified as insensitive.

4.3 VOLTAGE MODE FILTER

4.3.1. CIRCUIT DESCRIPTION

In this section the implementation of OFCC based voltage mode filter, as shown in Fig. 4.9 is proposed. It employs three OFCCs, two grounded capacitors and three grounded resistors. The analysis of the circuit gives the following transfer functions

$$T_{LPF} = \frac{V_{LPF}}{V_{in}} = \frac{1/R_x C_1 C_2 R_1}{D(s)} \tag{4.10}$$

$$T_{BPF} = \frac{V_{BPF}}{I_{in}} = \frac{s/R_x C_1}{D(s)} \tag{4.11}$$

Where,

$$D(s) = s^2 C_1 C_2 R_1 R_2 + s C_2 R_2 + 1 \tag{4.12}$$

Both the responses are characterized by same pole frequency (ω_0), bandwidth (ω_0/Q_0) quality factor (Q_0) obtained for current mode filter and given in eqn. (4.7), (4.8) and (4.9) respectively.

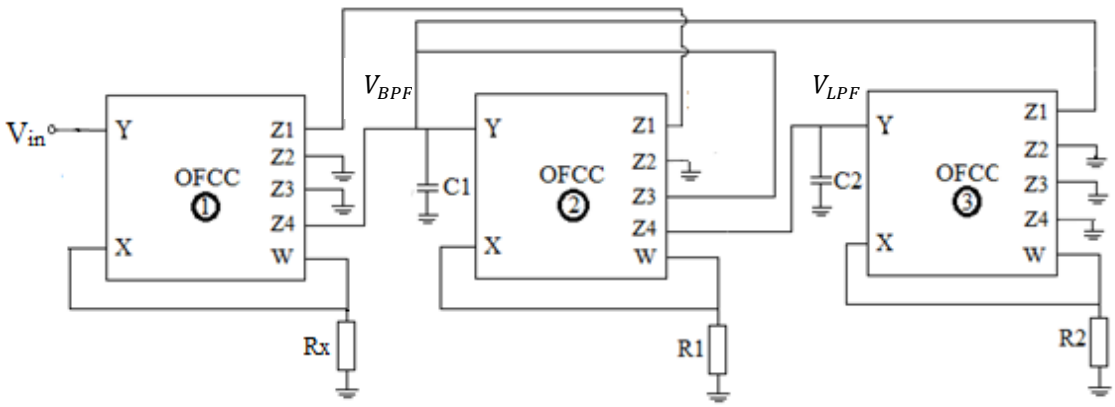


Fig. 4.9 Proposed OFCC based single input two output voltage mode filter

The above proposed filter also has grounded resistors which can be implemented using MOS based structure as discussed in 3.2.

The filter also enjoys the same performance characteristics of current mode filter proposed in section 3.2 regarding orthogonal adjustment of ω_0 and Q_0 and low component spread giving high Q factor.

4.3.2. SIMULATION RESULTS

The simulations have been performed for a pole frequency of 1.59 MHz with component values as $C_1 = C_2 = 100$ pF and MOS based resistors of value 1 kΩ by selecting bias voltages as ± 1.310V. Fig. 4.10 shows the simulation results for low pass response, and the band pass response is shown in Fig. 4.11. The responses confirm the theoretical predictions.

4.3. 3.SENSITIVITY ANALYSIS

The sensitivity analysis of the proposed circuit is as follows:

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_2}^{Q} = S_{C_2}^{Q} = -\frac{1}{2},$$

$$S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{R_2}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}$$

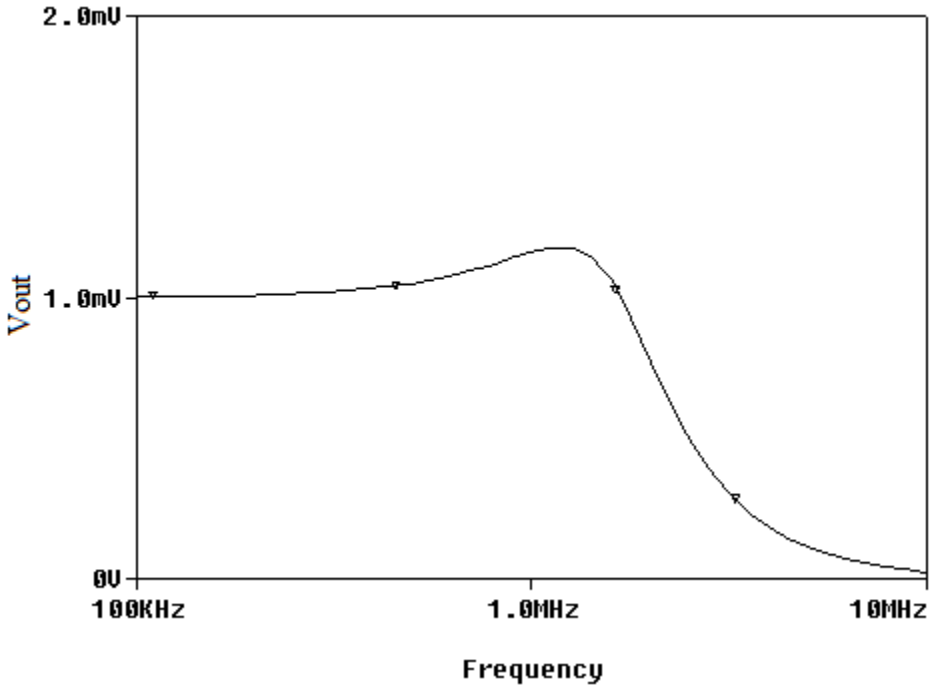


Fig. 4.10 Simulated low pass response of voltage mode filter

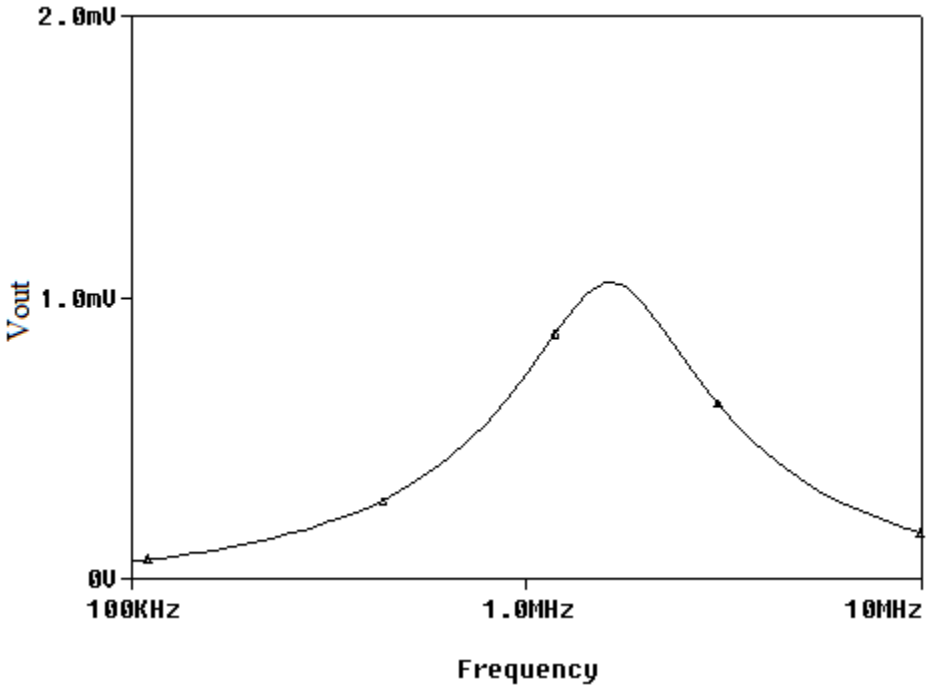


Fig. 4.11 Simulated band pass response of voltage mode filter

CHAPTER 5: LP & BP FILTER USING SINGLE OFCC

This chapter presents the realization of low pass and band pass filter using single OFCC in multiple loop feedback topology. The multiple loop feedback topology is widely used because of its low sensitivity in the domain of single active element networks [55]. In the proposed topology only one type of response is available. However, the topology can provide other responses by taking suitable selection of component values.

5.1. CIRCUIT DESCRIPTION

The general architecture for realizing continuous time filter using single OFCC in multiple loop feedback topology is shown in Fig. 5.1[56]. It is a general architecture and can realize low pass and band pass responses depending upon proper selection of components Y1, Y2, Y3, Y4 and Y5 which is given in table 5.1.

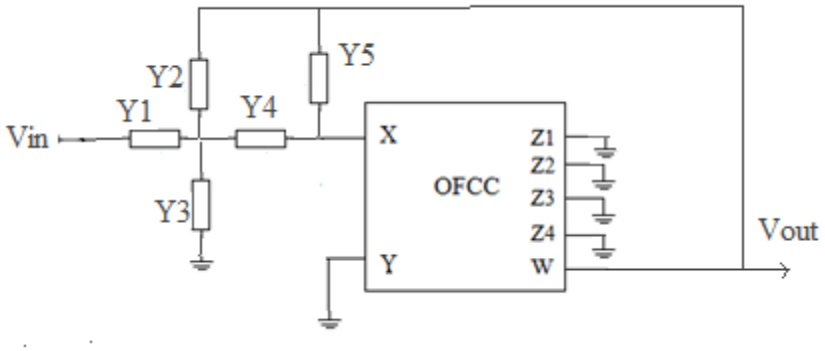


Fig. 5.1 General structure for filter using OFCC in multiple feedback topology.

The transfer function for above structure is obtained as follows:

$$T.F. = \frac{V_{out}}{V_{in}} = \frac{Y_1 Y_4}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_2 Y_4} \tag{5.1}$$

Table 5.1 Component values for realization of LP/BP filter

Type of	Component values				
Filter	Y1	Y2	Y3	Y4	Y5
LP	G1	G2	sC3	G4	sC5
BP	G1	sC2	G3	sC4	G5

5.2. LOW PASS FILTER

Using table 5.1, the transfer function for low pass filter is obtained as

$$T_{LP} = \frac{G_1 G_4 / C_3 C_5}{s^2 + \frac{G_1 + G_2 + G_4}{C_3} s + \frac{G_2 G_4}{C_3 C_5}} \tag{5.2}$$

The response is characterized by pole frequency (ω_0) and quality factor (Q_0) given as:

$$\omega_0 = \sqrt{\frac{G_2 G_4}{C_3 C_5}} \tag{5.3}$$

$$Q = \frac{1}{G_1 + G_2 + G_4} \sqrt{\frac{G_2 G_4 C_3}{C_5}} \tag{5.4}$$

To verify the functionality of the proposed single OFCC based filter, SPICE simulations have been carried out using 0.5 µm CMOS process model provided by MOSIS (AGILENT) and CMOS schematic of Fig. 2.2 with power supply voltage of V_{DD} = -V_{SS} = 1.5V and V_{B1} = -V_{B2} = 0.8 V. The aspect ratios of the transistor are reported in Table 2.1[18].

The simulations have been performed for a pole frequency of 15.9 KHz with component values as C_3 = C_5 = 1nF and $G_2 = G_4 = 0.1\ m℧$. Figure 5.2 shows the simulation results for low pass response. The responses confirm the theoretical predictions.

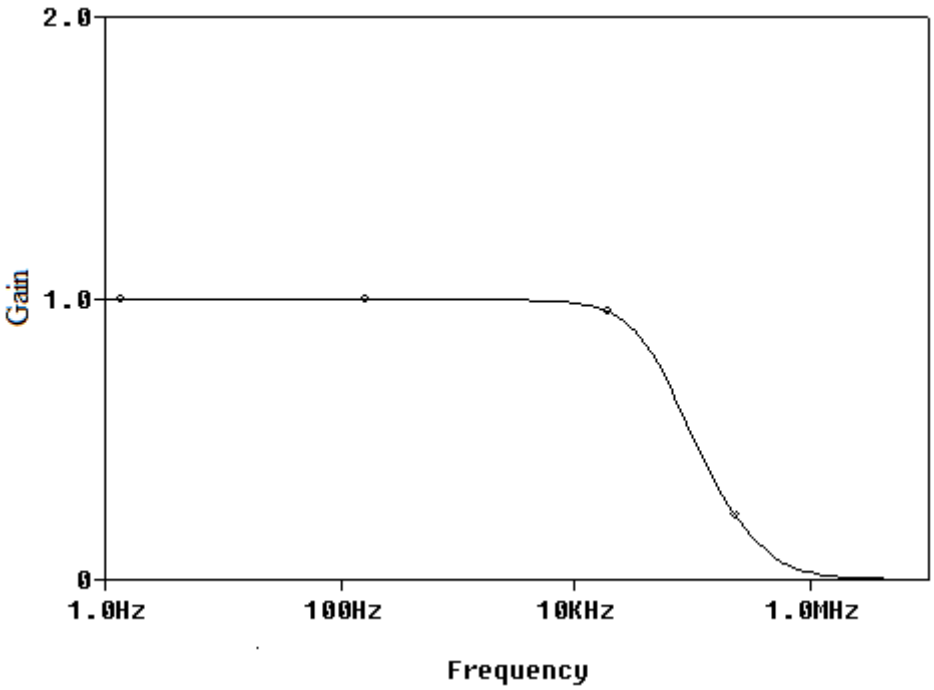


Fig. 5.2 Low pass response using single OFCC

5.3. BAND PASS FILTER

The transfer function for band pass filter using table 5.1 can be written as

$$T_{BP} = \frac{sG_1/C_2}{s^2 + \frac{C_1 + C_3}{C_2C_4}G_5 s + \frac{G_1 + G_3}{C_2C_4}G_4} \tag{5.5}$$

The response is characterized by pole frequency (ω_0) and quality factor (Q_0) given as:

$$\omega_0 = \sqrt{\frac{(G_1 + G_3)G_5}{C_2C_4}} \tag{5.6}$$

$$Q = \frac{1}{C_2 + C_4}\sqrt{\frac{(G_1 + G_3)C_2C_4}{G_5}} \tag{5.7}$$

The simulation has been performed for a pole frequency of 22.5 KHz with component values as C_2 = C_4 = 1nF and $G_1 = G_3 = G_5 = 0.1\ m\mho$. Fig. 5.3 shows the simulation results for band pass response. The response confirms the theoretical predictions.

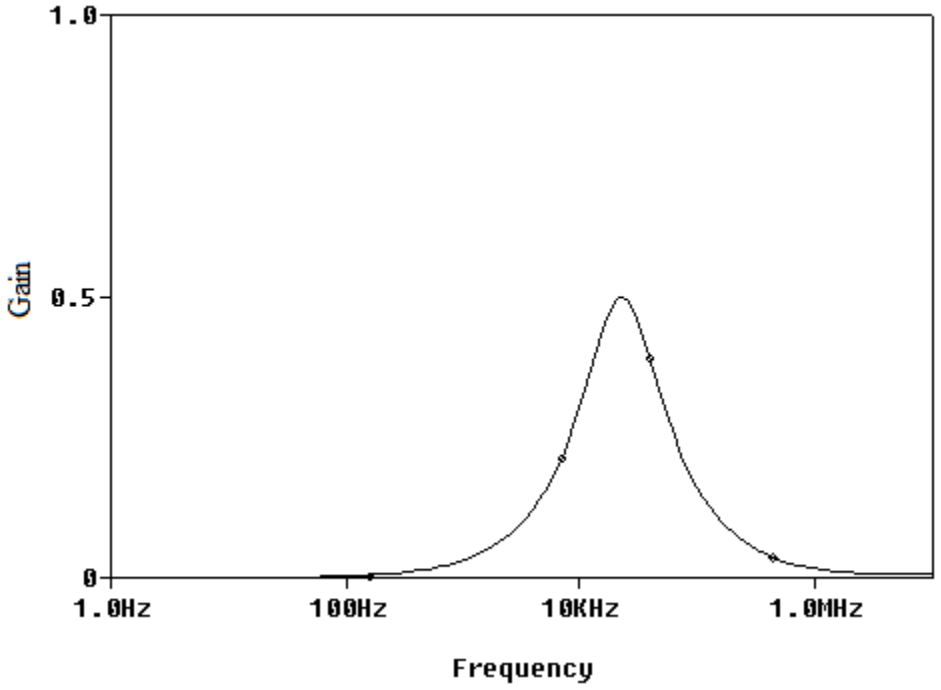


Fig. 5.3 Band pass response using single OFCC

CHAPTER 6

CONCLUSION

In this thesis , operational floating current conveyor (OFCC), a current mode building block is studied with its architectures, CMOS realizations and some existing applications.

A current mode filter and a trans-admittance mode filter is presented. The above filter responses are available at high impedance nodes with three responses at a time. Moreover, trans-impedance mode and voltage mode filters are also presented and they use similar topology of current mode and trans-admittance mode filter respectively. The filter parameters of above mentioned filters are tuned electronically via MOS based grounded resistors. These filters are also found to have low component spread and a sensitivity of less than unity.

Further low pass and band pass filters are also implemented using single OFCC block in multiple loop feedback topology.

PUBLICATIONS

A research article titled " **Single-input Four-output Current Mode filter Using Operational floating current conveyor**", has been published in **Hindawi** Publishing Corporation, Active And Passive Electronic Components, Vol. 2013.

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APPENDIX (I)

0.5μm Mosis Agilent Technology Parameter

NMOS

LEVEL=3 UO=460.5 TOX=1E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417
RSH=2.73 LD=4E-8 ETA=0 VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=.905
THETA=.129 GAMMA=.69 KAPPA=0.1 AF=1 WD=1.1E-7 CJ=76.4E-5 MJ=.357
CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
KF=3.07E-28 DELTA=0.42 NFS=1.2E11

PMOS

LEVEL=3 UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=.1E-6 RS=886 RSH=1.81
LD=3E-8 ETA=0 VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=.905 THETA=.12
GAMMA=.76 KAPPA=2 AF=1 WD=1.4E-7CJ=85E-5 MJ=.429 CJSW=4.67E-10
MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29
DELTA=0.81 NFS=.52E11