Implementation of Analog Blocks Using Current Mirror

Project Report submitted in partial fulfillment of the requirements for the degree of

MASTERS of TECHNOLOGY (M. Tech.)

In

VLSI AND EMBEDDED SYSTEMS

Submitted by:

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(Session: 20015-2017)

CERTIFICATE

This is to certify that the report titled **"Implementation of analog blocks using current mirror"** is a bonafide record of Major-2 submitted by Sapna Yadav(Roll no: 2K15/VLS/14) as the record of the work carried out by her under my guidance. The said work has not been submitted anywhere else for the award of any other degree or diploma.

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DECLARATION

This is to certify that dissertation entitled **"Implementation of analog blocks using current mirror"** which is submitted by me in partial fulfillment of the requirement for the award of M.Tech degree in **VLSI and EMBEDDED SYSTEMS** from Delhi Technological University, Delhi, INDIA comprises only my own work and due acknowledgement has been made to all other material used.

I hereby, further declared that in case of legal dispute in relation to my M.Tech dissertation, I will be solely responsible for the same.

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ABSTRACT

A current mode signal processing circuit is quite attractive for low power supply and high frequency applications. The current mirror is an active element of this circuit. In current mode techniques the current mirrors have wider dynamic range and extended bandwidth as compared to other active elements. The project involves study of current mirrors, their comparison between input and output resistances and compliance voltage. Further the project includes the basic like adder, subtractor blocks using CMOS based cascode current mirror and implementation of filters using this building block. Project also includes studies of sinusoidal to square waveform. Results will be verified on PSPICE using CMOS 350 nm technology parameters.

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LIST OF ABBREVIATION

AC	Alternating Current
ADC	Analog-to-digital converter
APF	All Pass Filter
BJT	Bipolar Junction Transistor
BPF	Band Pass Filter
BSF	Band Stop Filter
CM	Current Mode
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-analog converter
DC	Direct Current
HPF	High Pass Filter
IC	Integrated Circuit
LPF	Low Pass Filter
LT	Linear Transformation
MOS	Metal Oxide Semiconductor
SIMO	Single Input Multi Output
VM	Voltage Mode

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Chapter 1

INTRODUCTION

Digital signal processing has become one of the preferred signal processing for past few decades because of compact and efficient implementation. As per Moore's law in every 18 months number of transistors on a chip become double but this limit of transistors has been crossed. So complementary metal oxide semiconductor (CMOS) technology helps us to design a smaller size circuit.

However there are some issues with digital signal processing. They are as:

I. Every natural signal is analog in nature. So at input side of digital signal processing analog-to-digital converter(ADC) and at output digital-to-analog converter(DAC) is required. Leading to larger chip area.
II. It uses anti-aliasing filter. So only limited frequency analog signals pass through this. Rest of the frequencies are eliminated.
III. Clock skew is one of the main issue in digital signal process.
IV. There is always a tradeoff between power dissipation, cost, area and speed of digital system

Thus, Analog signal processing has gained a renewed interest due to the designs catering high frequency applications.

There are two types of analog signal processing i.e. voltage mode(VM) and current mode(CM) signal processing. In VM signal processing, information is processed in voltage form. Output voltage is the function of input voltage. In CM signal processing, information is carried through branch currents.

1.1Voltage and current mode signal processing

Analog system design has historically been viewed as a voltage dominated form of signal processing. However, the evolution of submicron technologies necessitates the use of low power supply voltage. Thus, it has become very difficult to design the VM circuit with high linearity and dynamic range. This problem can be resolved either by using CMOS technologies with lower threshold voltage or by using standard CMOS technology with low voltage circuit techniques. The CMOS technologies with lower threshold are costly therefore over last few decades CM processing has emerged as an alternative design technique for low voltage applications. The CM circuits are characterized by low terminal impedances, therefore, are suitable for fast response. If instead of current, voltage is used as signal, there will be a reduction in the output swing and hence the CM circuits can operate under low supply voltage. Thus, a CM circuit, for a fixed supply voltage, has a larger dynamic range than the VM circuit. In CM circuits by joining terminals at a single point, addition/subtraction operations can be performed resulting in simple architecture.

Thus, higher bandwidth, low operating voltage, better linearity, low power consumption, and simple architecture are some of the key advantages of CM over VM processing [1.1].

1.2 Motivation

Research and development in the field of analog electronics has revolutionized human life. Because of developments in IC technology isolated circuits are almost obsolete. The need of scaling down of chip area is increasing very rapidly. It seems that high speed; less complexity; high density; low power consumption; price etc. will be the major factor of apprehension in the ultramodern device designing. These motivate us to do research on most basic and essential building block of processor. since Unique property of this device opened the door to efficient use of current mirrors Current mode circuits, which process the active signal as current offers a number of advantages.

Advantages of current mode circuits over voltage mode circuits:

There are various advantage of current mode circuits over voltage mode circuits and they are as follows:

A. Delay:

As technology is shrinking, interconnect delays are increasing even they are dominating transistor gate delays. But as current mode circuits have low output impedence this delay is reduced [1.2].

B. Supply voltage reduction:

In voltage mode circuits output is directly proportional to the input voltage so adverse effect due to supply voltage and ground fluctuations. But in current mode circuits reduction in supply voltage minimize these effects.

C. Bandwidth improvement:

Current mode interconnects provide high bandwidth. Improvement in bandwidth increases the speed of the circuit. Signal can be transmitted fast over.

D. High output resistance:

Current mirror has high output resistance so high gain is achieved and it is electronically controllable.

Applications:

1) Due to reduction in voltage supply, power consumption is also less so it is very important feature, especially in biomedical application where battery life of implantable devices should be more.
2) It is used in biasing circuits. Every analog circuit needs biasing.
3) As chip size is getting reduced it is very difficult to mount a bulky inductor so designers started replacing passive RLC circuit into active RC circuit.
4) Short range electronic devices for wireless communication.

1.3 Objective

Main objective of the work done in this dissertation is to implement the analog circuits using cascode current mirror.

To achieve this, dissertation concentrated on following areas:

- Literature survey.
- Study and implementation of various existing current mirror.
- Study and implementation of existing application based on current mirror.
- Design and development of new applications.

To meet these objectives all analog circuits are designed and simulated using pspice on 350nm technology. Simulated results are compared with theoretical results. Performance of the proposed circuit's results also compared with existing ones.

1.4 Report Organization

In this work current mirror and its based applications are discussed and simulated results are compared with theoretical results. Work is distributed in five chapters as follows:

Chapter 1: This chapter presents brief introduction about the digital and analog signal processing. Advantages of analog signal processing over digital signal processing. Comparison between CM and VM signal processing. This chapter also discuss the motivation and objective of the work done.

Chapter 2: Survey of the different structures of the current mirror and comparison between them on different structure and technology. Cascode current mirror, DC and AC characterization of this current mirror is presented in this chapter. Various performance parameters are also extracted in this chapter.

Chapter 3: Some existing CM applications are implemented using this cascade current mirror. First order and second order low pass filter, first order high pass filter, KHN filter, Linear Transformation (LT) filter are implemented and verified using pspice simulator.

Chapter 4: This chapter records the summary of the work presented in this dissertation and the further scope of this technique.

Chapter 2

LITERATURE SURVEY

2.1 Introduction

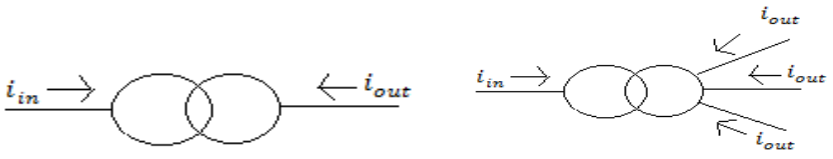
In past few decades CM signal processing has gain interest which was explained in chapter 1. Advantages of CM signal processing has offered various analog building blocks. In these building blocks current mirror is one of them.

Current mirror circuits are widely used, especially in integrated circuit technology. Generally it consists of two transistor but for better performance number of transistors can be increased. The current mirror circuit called current mirror because it copies the input current at the output section, keeping the output current constant regardless of load because it has high output resistance. Also it has a low input resistance which keeps the input current constant regardless of drive conditions.

An ideal current mirror is a current amplifier also called current controlled current source has unity gain.

Current mirror is used as an active load because it has high output resistance so gain will be high and also to provide bias current.

Current mirror can have many input and many output. Fig 2.1.1(a) shows single input single output (SISO) type current mirror. And Fig2.1.1 shows single input multiple output (SIMO) current mirror. These are used for filter designing with less component.



(a) (b)

Fig 2.1.1(a): Single output current mirror.(b): Multi output current mirror

There are two types of current mirrors on basis of direction of output current.

1) Current sink
2) Current source

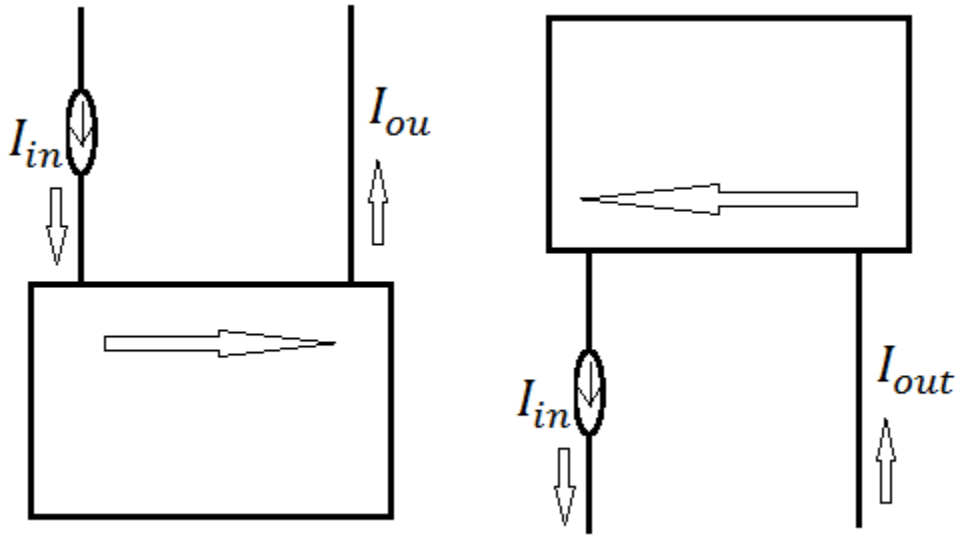


Fig. 2.1.2: Current Mirror (a) Sink (b) Source.

In current sink if input is given as current then it is converted into voltage, this voltage is used to control the exiting current and we would obtain a current sink. Conversely output current of current sink is given at input that current is converted into voltage and this voltage control the output current of current source.

2.2 Review on Current Mirror

Vast literature available about various structure of the current mirror and its analysis. And advantages and disadvantages of various structure is discussed later. Detail of various structures discussed in following subsections:

Current mirrors are important block in analog applications. They are widely used as an active load and current mirroring. They come in different varieties:

- Simple current mirror
- Wildar current mirror
- Wilson current mirror
- Cascode current mirror

2.2.1 Simple current mirror :

Basic current mirror consists of a diode connected reference transistor and output transistor whose drain and gate are connected with the reference transistor.

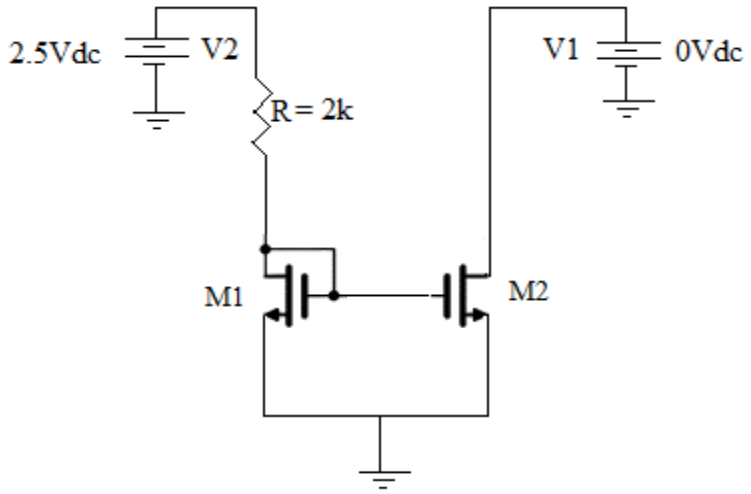


Fig 2.2.1: Simple current mirror

Current through M1 is given by [2.1],

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{TN})^2$$

Assuming M2 is also in saturation, so current through M2 can be given by,

$$I_{D2} = I_0 = \frac{\beta_2}{2}(V_{GS2} - V_{TN})^2$$

From above these equations, drain current dependency on supply voltage (because gate and drain voltage are equal), processes parameters, temperature.

Since $V_{GS1} = V_{GS2}$ then ratio of I_{D1} and I_{D2}will be

$$\frac{I_{D2}}{I_{D1}} = \frac{\beta_2}{\beta_1} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}}$$

Output current is proportional to the input current multiplied with the ratio of output aspect ratio to the input transistor aspect ratio. If aspect ratio of second transistor is greater than first it acts as current amplifier whose gain is directly proportional to the ratio of their aspect ratios.

Its accuracy also depends upon the channel length modulation and drain to source voltage in case of MOSFET[2.2 ref]

$$\frac{i_0}{i_1} = \frac{L_1 W_2}{L_2 W_1}(1 + \lambda V_{DS})$$

In case of short channel MOS devices used to design smaller high frequency, low power consumption device error due to channel length effect further increases. In short channel devices transconductance increases but output resistance decreases and decrement in output resistance is more prominent than increase in transconductance. Hence simple current mirror has lower accuracy and has low output resistance.

For best performance, transistors should be matched, temperature should be same for all devices and drain-gate voltage should be matched. This will provide equal currents on both sides of the current mirror.

Output resistance of current mirror is equal to resistance of M2,

$$r_0 = \frac{1}{\lambda I_0}$$

Transfer characteristics of basic current mirror is not exactly linear but a curved shape due to small scale effect. Output resistance is also low.

2.2.1(a). Input resistance

Small signal model for calculating input resistance[2.2] is shown in Fig 2.2.2. For small signal analysis all DC currents act as open circuit and voltages act as short circuit. A voltage source is applied at the input terminal and ratio of input voltage and input current gives the input resistance.

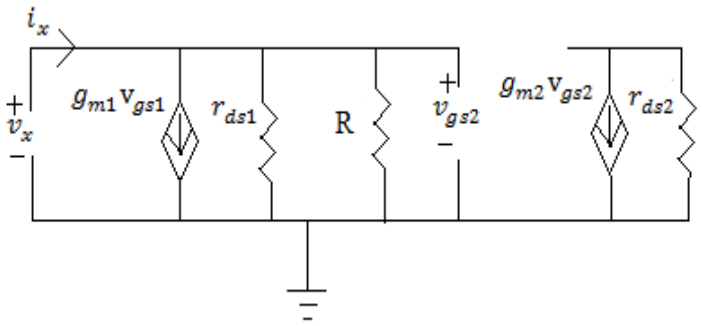


Fig 2.2.2: Small signal model of simple current mirror for input resistance

To calculate input resistance, apply KCL at the input terminal,

$$\frac{v_x}{r_{ds1}} + g_{m1}v_{gs1} + \frac{v_x}{R} = i_x \quad \text{.....(1)}$$

As we can see from equation (1) we don't need output circuit to calculate input resistance.

$v_{gs1} = v_x$, putting this into equation (1), we get

$$\frac{v_x}{i_x} = \frac{1}{\frac{1}{r_{ds1}} + g_{m1} + \frac{1}{R}} \quad \text{.....(2)}$$

If we neglect channel length modulation, M1 is in saturation because gate and drain is shorted so r_{ds1} will have very high value so we can neglect it. So input resistance becomes the parallel combination of R and $\frac{1}{g_{m1}}$.

$$\boxed{R_{in} = R \| \frac{1}{g_{m1}}}$$

2.2.1(b). Output resistance

Small signal model for output resistance of simple current mirror is shown in Fig 2.2.3.

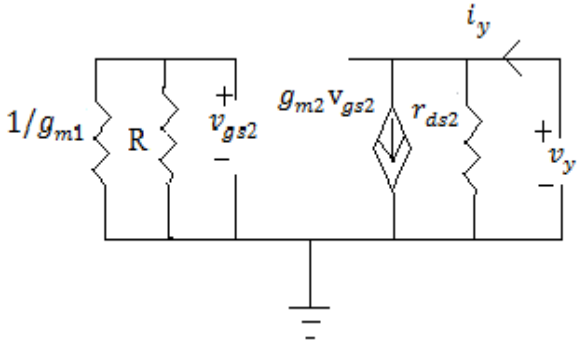


Fig 2.2.3: Small signal model for output resistance

Input transistor is replaced by only $\frac{1}{g_{m1}}$ because input terminal gets open circuited because of silicon dioxide layer which is present between gate and channel. And that oxide layer does not allow any current from gate to flow into channel side. So input current that is gate current is zero and only voltage exist at source side. If channel length modulation is neglected M1 is replaced by $\frac{1}{g_{m1}}$.

As it can be seen from FIG that no current flowing into $\frac{1}{g_{m1}}$. So value of v_{gs2} will be equal to zero.

As $v_{gs2} = 0$, $g_{m2}v_{gs2}$ becomes open circuit. So output resistance of M2 which is output resistance of current mirror is r_{ds2}.

$$\boxed{R_o = r_{ds2}}$$

2.2.1(c). Minimum output voltage

Output voltage of simlple current mirror is volatge across drain to source. For proper operation of simple current mirror M1 and M2 must be in saturation . M1 is in saturation because gate and drain are shorted. But problem is with M2. We must ensure that M2 should operate in saturation region.

From current mirror diagram

$V_{DS1} = V_{GS1} = V_{GS2}$

But $V_{DS2} \neq V_{GS2}$

For proper operation of current mirror both transistor should operate in saturation region .

Codition to keep M2 in saturation is

$$V_{DS2} \geq V_{GS2} - V_T$$

$$V_O \geq V_{GS2} - V_T$$

Minimum voltage to keep M2 in saturation is

$$\boxed{V_{Omin} = V_{GS2} - V_T}$$

2.2.2 Wildar current source

Wildar current mirror is variation of simple current mirror. It was invented by Bob Wildar in mid 1960s. the only difference between simple current mirror and Wildar current mirror is the introduction of the source resistance of M2. This additional component forces the unequal current in the two branches of the circuit. So this circuit is also called current source rather than current mirror. Application of this circuit is in operational amplifiers.

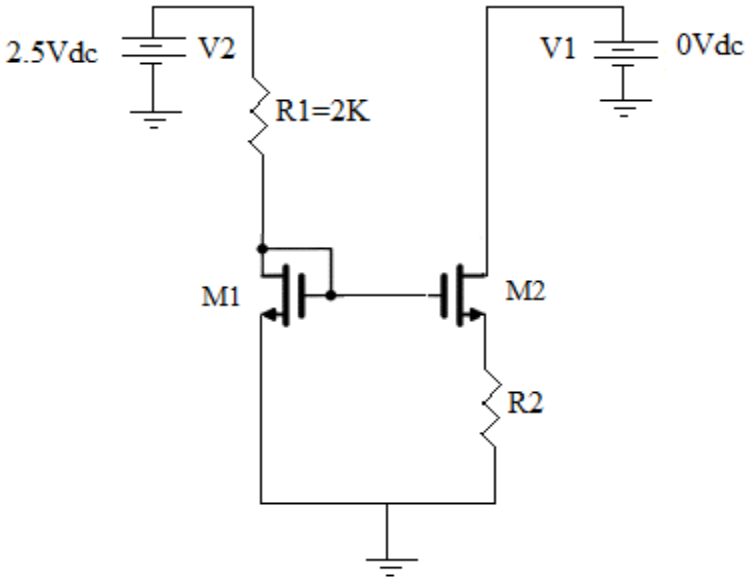


Fig 2.2.4: Wildar current mirror

2.2.2(a). Input resistance

Input resistance of wildar current mirror is same as simple current mirror. Small signal model of wildar current mirror is shown in Fig 2.2.5.

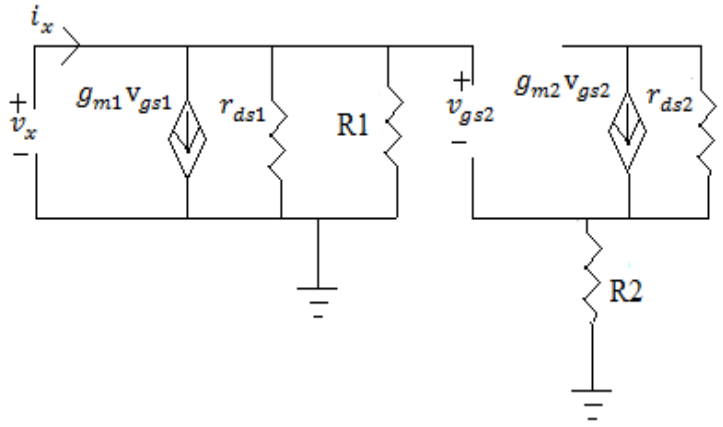


Fig 2.2.5: Small signal model of wildar current mirror for input resistance

We don’t need output section to calculate input resistance and input section is same as input resistance of simple current mirror.

$$R_{in} = R1 || \frac{1}{g_{m1}}$$

2.2.2(b). Output resistance

Small signal model of wildar current mirror to calculate output resistance is shown in Fig 2.2.6.

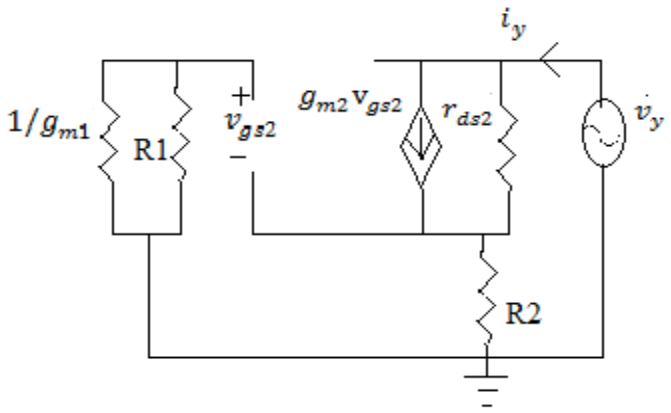


Fig 2.2.6: Small signal model for output resistance.

As discussed above input transistor M1 is replaced by $\frac{1}{g_{m1}}$. Apply an AC voltage signal at the output and calculate the current across that voltage signal. Ratio of these two quantities give the output resistance.

Applying KCL at the output section, assuming v_x voltage at source of M2.

$$\frac{v_y - v_x}{r_{ds2}} + g_{m2}v_{gs2} = i_y \quad \text{.....(3)}$$

Also applying KCL at source of M2,

$$\frac{v_x - v_y}{r_{ds2}} + \frac{v_x}{R2} = g_{m2}v_{gs2} \quad \text{.....(4)}$$

As no current flowing across $\frac{1}{g_{m1}}$ and R1 so gate volatge will be zero.

$v_{gs2} = v_{g2} - v_{s2} = 0 - v_{s2} = -v_x$, putting this into equation(3) and (4) and taking ratio of v_y and i_y. We get

$$\frac{v_y}{i_y} = R_o = r_{ds2} + R2 + r_{ds2}g_{m2}R2$$

$$\boxed{R_o = r_{ds2} + R2 + r_{ds2}g_{m2}R2}$$

2.2.2(c). Minimum output voltage

Minimum output voltage of wildar currrent source is volatge across drain to source of M2 transistor plus volatge across R2.

$$V_{Omin} = V_{DS2} + I_D R2$$

$$\boxed{V_{Omin} = V_{GS2} - V_T + I_D R2}$$

This is the minimum output voltage that can keep M2 transistor into saturation.

2.2.3 MOSFET implementation of the Wilson current mirror

MOSFET implementation of Wilson current mirror will look like as shown in Fig 2.2.7. Wilson current mirror is having negative feedback and drain current is stabilized. There are four types of feedback. Series sampling is used here to increase the output impedence.

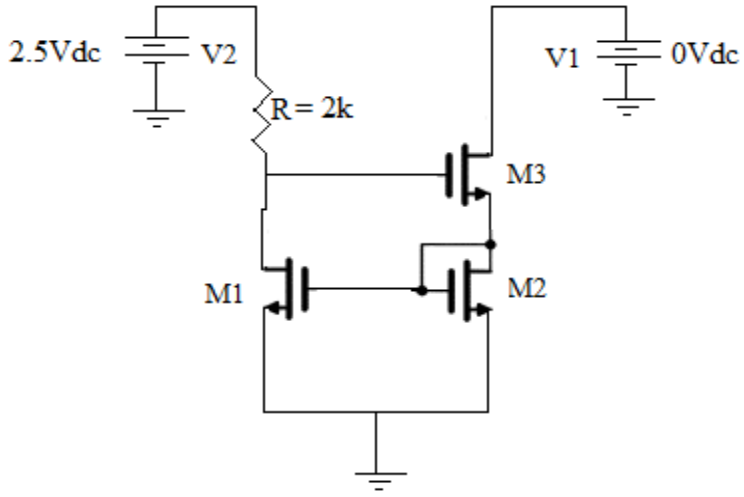


Fig 2.2.7: Wilson current mirror[2.3]

2.2.3(a). Existence of negative feedback :

M2 is in saturation because of gate and drain shorted. As drain current of M2 will be equal to drain current of M1 because they form simple current mirror. Output current making influence of input current that is nothing but feedback. Feedback is a part of output which is fed back to the inpput side.

2.2.3(b). Stabilisation of output current against variation in output voltage:

Even though output voltage change, output current should not change, it should be stable.

As output voltage increases, output current increases due to channel length modulation. For the given value of V_{GS}, if V_{DS} is increased, output current increases which makes I_{D1} increases. When I_{D1} increases at that time V_{DS1} decreases. Because when I_{D1} increases but we are getting a constant current through R1 that forces V_{DS1} reduces.

2.2.3(c). Input resistance:

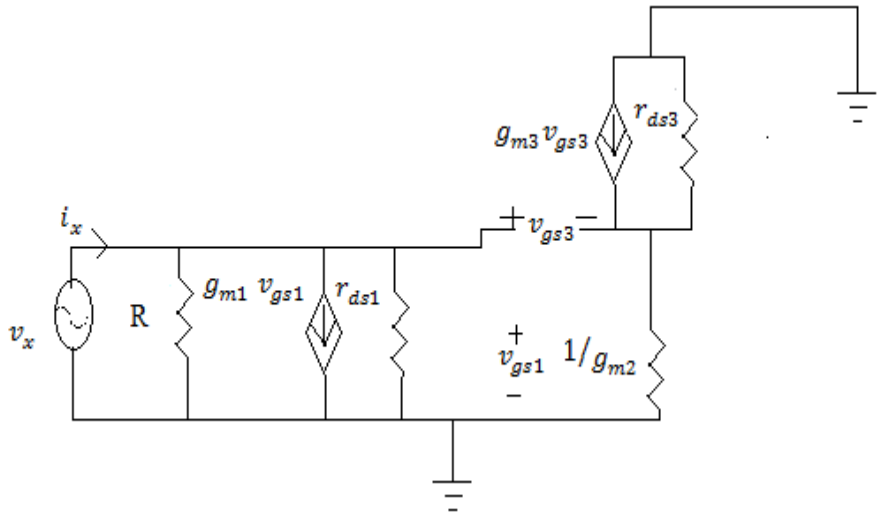


Fig 2.2.8: Small signal model of wilson current mirrorof input resistance.

Input resistance of wilson current mirror is

$$R_{in} = \frac{g_{m2}+g_{m3}}{(R||g_{m1})g_{m3}}$$

2.2.3(d).Output resistance

To calculate output resistance, apply test voltage at output which causes a test current in the circuit. Ratio of test voltage and test current gives the output resistance. For which small signal diagram is shown in Fig 2.2.9.

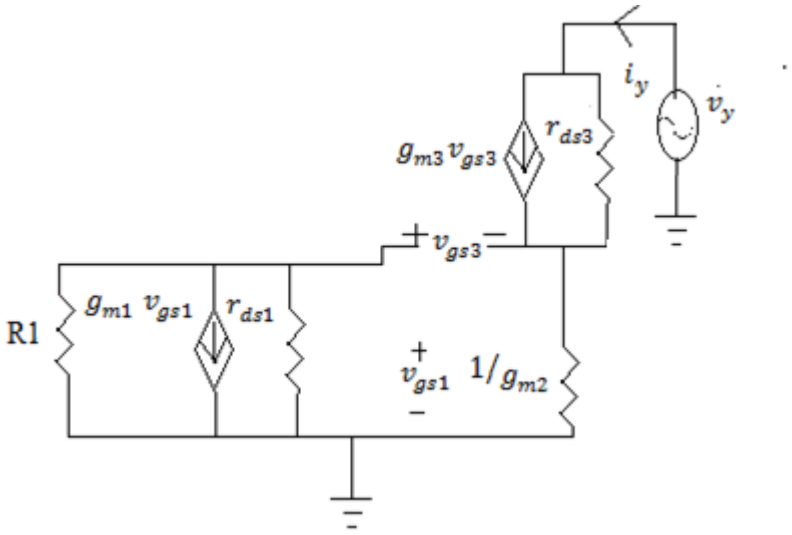


Fig 2.2.9: Small signal model for output resistance

M1 is replaced by $\frac{1}{g_{m1}}$. Here

$v_{gs1} = i_y \frac{1}{g_{m2}}$ and $v_{gs3} = v_{g3} - v_{s3} = (r_{ds1} g_{m1} v_{gs1} R1) - v_y$

Applying KCL at drain of M3,

$\frac{v_y - v_{gs1}}{r_{ds3}} + g_{m3} v_{gs3} = i_y$ .....(5)

Putting expression of v_{gs3} and v_{gs1} into equation(5), and solving for $\frac{v_y}{i_y}$.

$\frac{v_y}{i_y} = R_o = \left[\frac{1}{g_{m2}} + r_{ds3} + \frac{g_{m3} r_{ds3} r_{ds1} g_{m1} R1}{(R1 + r_{ds1}) g_{m2}}\right]$

Assuming $r_{ds1} = r_{ds3} = r_o$, $g_{m1} = g_{m2} = g_{m3} = g_m$ and neglecting first two terms, final output resistance is

$$\boxed{R_o = \frac{g_m^2 r_o^2 R1}{(R1 + r_o) g_m}}$$

Now it is square of r_o, wilson current mirror has an output resistance similar to the cascode current mirror.

2.2.3(e). Minimum output voltage:

Minimum output voltage to keep M2 and M3 into saturation is

$V_{Omin} = V_{GS2} + V_{DS3}$. But $V_{DS3} = V_{GS3} - V_T$. So V_{Omin} becomes

$V_{Omin} = V_{GS2} + V_{GS3} - V_T$. If $V_{GS2} = V_{GS3}$ then

$$\boxed{V_{Omin} = 2V_{GS2} - V_T}$$

2.2.4 Cascode current mirror

Current mirror has high output resistance. Disadvantage of simple current mirror is output resistance is not that much high. Cascode current mirror has two advantages over simple current mirror is that

1. It supress the effect of channel length modulation.
2. It increases the output impedence.

In simple current mirror $V_{DS1} \neq V_{DS2}$ because of channel length modulation. So $I_{REF} \neq I_{OUT}$.

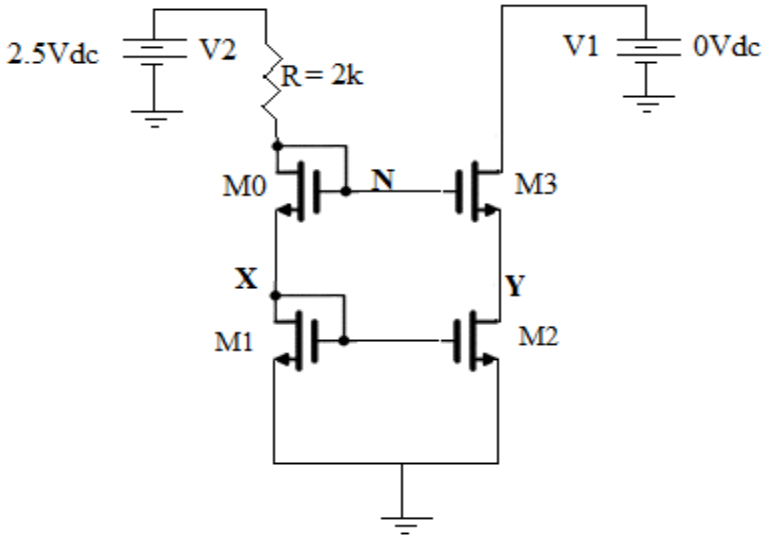


Fig 2.2.10: Cascode current mirror[2.4]

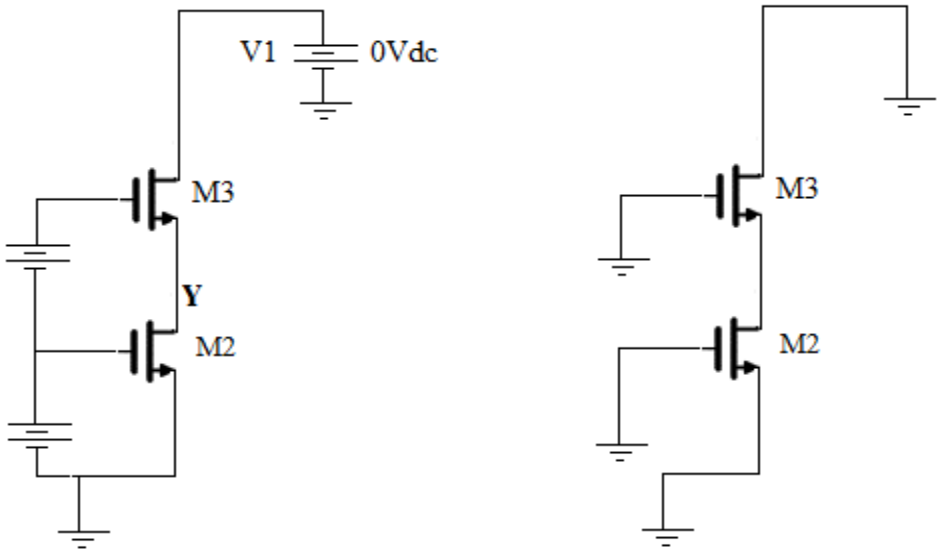
At node N,

$V_{GS0}+V_X = V_{GS3} + V_Y$. Proper choice of dimensions results in $V_{GS0} = V_{GS3}$.

And then $V_X = V_Y$. And hence channel length modulation is neglected.

2.2.4(a). Output resistance:

A diode connected MOSFET being fed by a constant current behaves as a constant DC potential which is shown in Fig 2.2.11(a) and it AC equivalent circuit is shown in Fig 2.2.11(b).



(a) (b)

Fig 2.2.11: (a) Cascode current mirror when two transistor replaced by DC potential. (b)small signal reprentation.

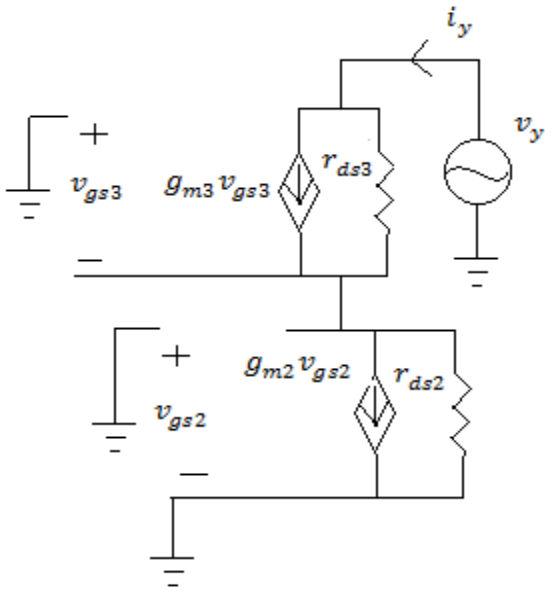


Fig 2.2.12: Small signal model for output resistance[2.5]

$v_{gs2} = 0$, so $g_{m2}v_{gs2} = 0$ i.e. it acts as open circuit. And i_y only flows through the r_{ds2}.

$$i_y = g_{m3}v_{gs3} + \frac{v_1-(-v_{gs3})}{r_{ds3}} \quad \text{.....(6)}$$

Where $v_{gs4} = -i_y r_{ds2}$

Putting this into equation(6), we get

$$R_0 = r_{ds3}(1 + g_{m3}r_{ds2}) + r_{ds2}$$

Assuming $r_{ds2} = r_{ds3} = r_o$,

$$\boxed{R_0 = g_{m3}r_o^2}$$

2.2.4(b). Minimum output voltage

Requied minimum output voltage to keep M2 and M3 in saturation is

$V_{Omin} = V_{DS2} + V_{DS3}$, which is equal to

$V_{Omin} = V_{GS2} - V_T + V_{GS3} - V_T = 2(V_{GS} - V_T)$ if $(V_{GS2} = V_{GS3} = V_{GS})$ which is large enough.

Assuming all transistor are identical and they are in saturation then exact V_{Omin} to keep the transistors in saturation is

$$\boxed{V_{Omin} = 2V_{GS} - V_T}$$

2.3 PSPICE simulation of all current mirrors

All current mirrors are simulated through PSPICE using 350nm technology process parameters. Supply voltage used is $\pm$2.5V. Table 2.1 shows the aspect ratio used for different transistors of cascode current mirror. All current mirrors are characterized for its DC and AC responses. Various aspect parameters are calculated using PSPICE simulation. It is observed that simulated results are very close to calculated results.

2.3.1 DC characteristics

2.3.1(a). I_{out} and I_{ref} versus output voltage of all current mirror.

DC simulation of all current mirror is shown in Fig 2.3.1 to Fig 2.3.4. They show the minimum output voltage required to copy the input current at the output to keep all the transistors in saturation for proper working of current mirror.

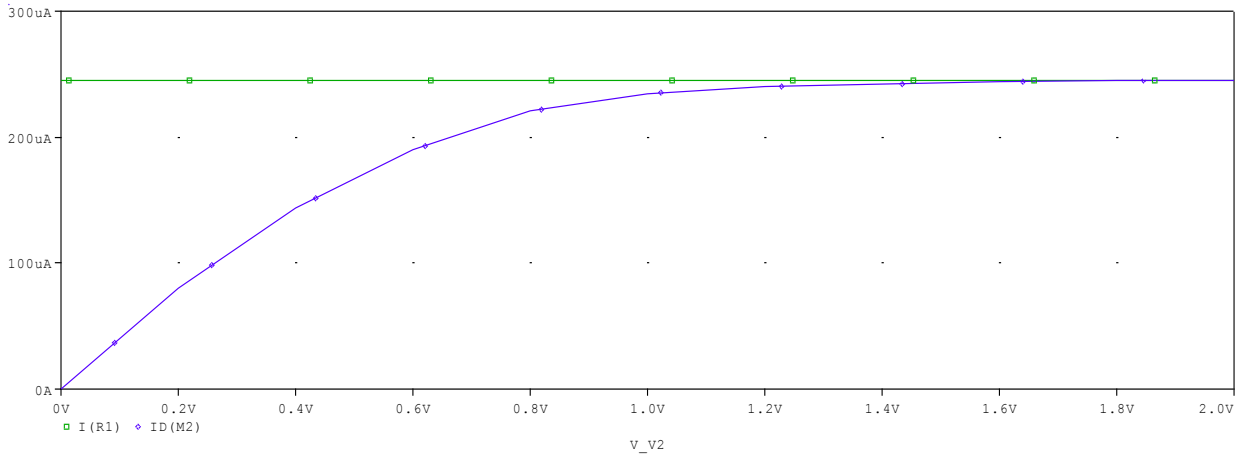


Fig 2.3.1: I_{out} and I_{ref} versus compliance voltage of simple current mirror.

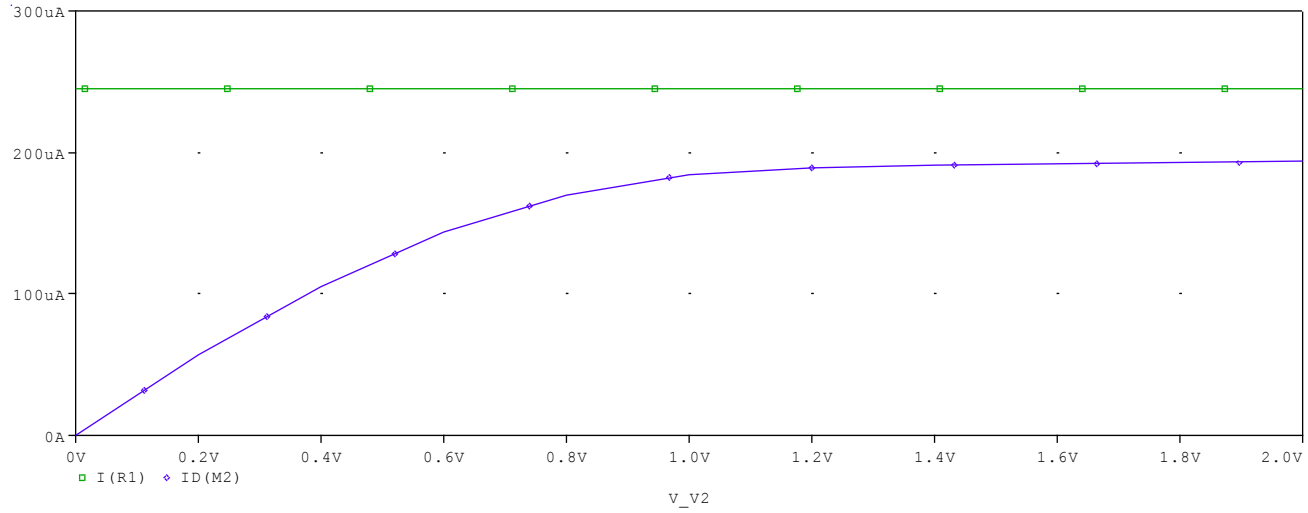


Fig 2.3.2: I_{out} and I_{ref} versus compliance voltage of wildar current mirror.

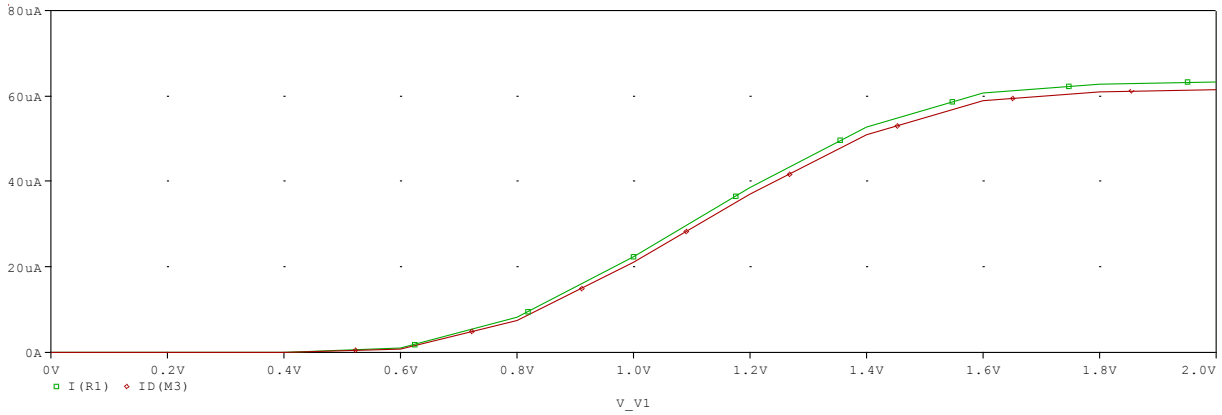


Fig 2.3.3: I_{out} and I_{ref} versus compliance voltage of wilson current mirror.

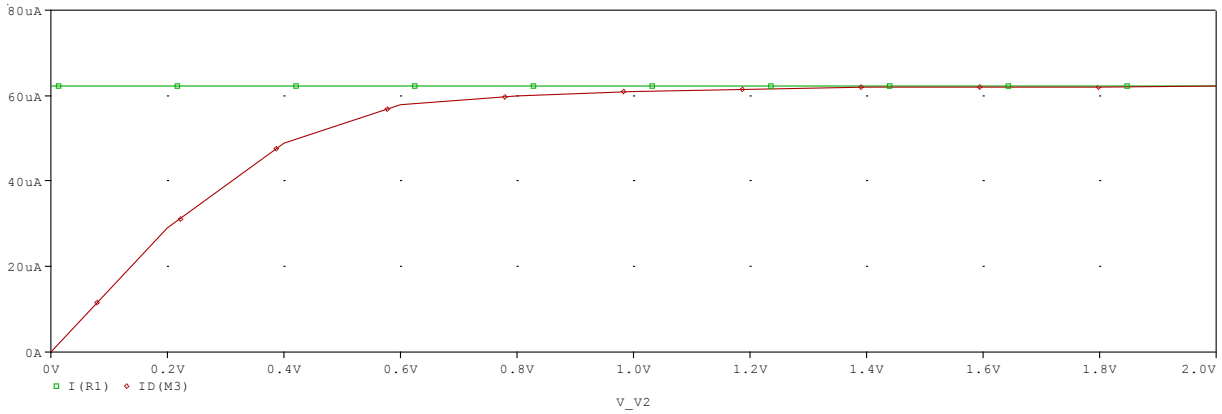


Fig 2.3.4: I_{REF} and I_{out} vs compliance voltage of cascode current mirror.

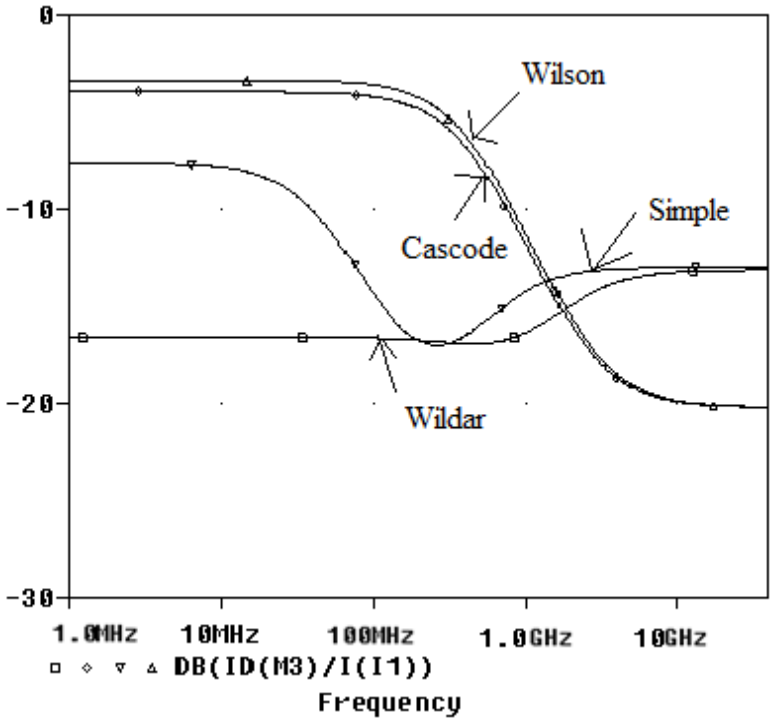


Fig 2.3.5: i_{out}/i_{in}(db) of all current mirrors versus frequency.

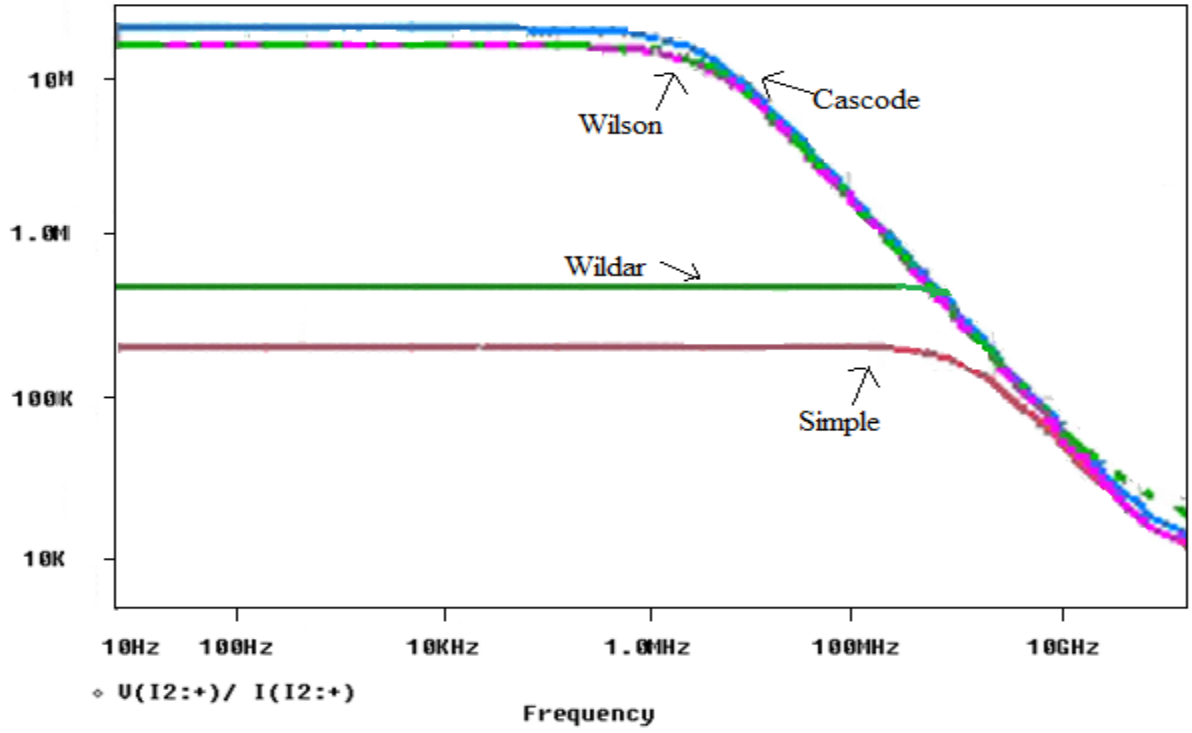


Fig 2.3.6: Output resistance of all current mirror.

2.4. Comparison

Comparison of different current mirror in terms of technology, supply voltage, number of transistors, power dissipation, input resistance, output resistance etc. presented in Table 2.1.

Table 2.1: Comparison of different Current Mirror structures

Parameter	**Simple**	**Wildar**	**Wilson**	**Cascode**
Technology	350nm	350nm	350nm	350nm
Mirroring accuracy	Very poor	Poor	poor	Very good
Bias current	……	……	……	……
$i_{out}/i_{in}(-3db)bandwidth$	5.425GHz	4.29GHz	776.49MHz	789.6MHz
R_{in}(in ohm)	5.024E+2	1.0E+2	3.356E+4	1.005E+3
R_{out}(in ohm)	298.7E+3	576.4E+3	24.8E+6	29.3E+6
Accuracy error	.38	.58	.22	.18`
Power consumption (in Watts)	9.8E-12	9.9E-12	2.32E-11	3.8E-11
Minimum output voltage(in V)	1.47	1.945	3.2	3.2

2.8 CMOS based cascode current mirror

Recently CM technique provides higher advantages as compare to VM techniques. CMOS based cascode current mirror is used for high output resistance and also suppress the channel length modulation. Higher the output resistance of current mirror higher will be the accuracy of the current mirror. Output voltage across cascode current mirror is larger than the simple current mirror. CMOS based current mirror structure is shown in Fig 2.5.1. This is the block which is used further to implement analog blocks.

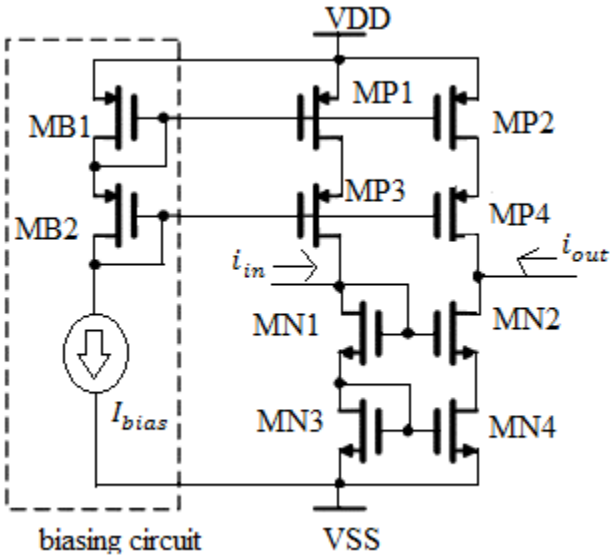


Fig 2.5.1: CMOS based cascode current mirror[2.6].

Main feature of the current mirror is that current is independent of the voltage. Biasing circuit in the circuit provide the constant reference current to the circuit. This I_{bias} current is independent or insensitive to temperature [3.1]. As drain and gate of MB1, MB2 are shorted. So they are in saturation and MB1, MB2, MP1,MP2, MP3, MP4 form PMOS current mirror for CMOS technology current mirror. Whatever current will be at the input of MN1 will flow at the output. Because gate and source voltage MN3, MN4 is same. So current at output node will be equal to the current at the input node.

2.5.1 Effect of non-idealities on current mirror:

Effect of non-idealities on current mirror is evaluated by calculating their transfer function. A small signal model of this current mirror is shown in Fig 2.5.2 where the small signal transconductance, output conductance and gate to source capacitance of each transistor have been taken into consideration. The derived expression of the transfer function is given by equation as[2.7].

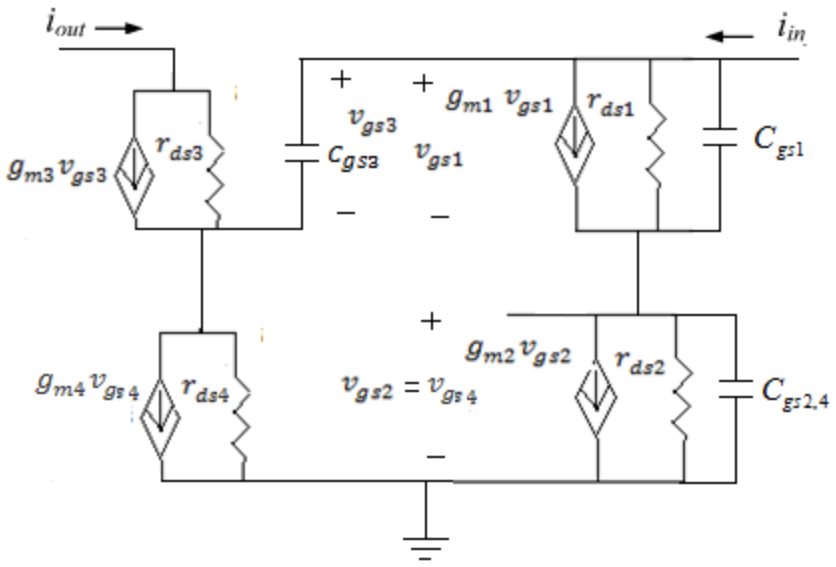


Fig 2.5.2 : AC equivalent of CMOS based cascode current mirror[2.8].

$$\frac{i_{out}}{i_{in}} = \frac{g_{m3}}{g_{m4}}\left(\frac{s\frac{c_{gs1}}{g_{m1}}+1}{s^2\frac{c_{gs2,4}\,c_{gs1}}{g_{m2}g_{m1}}+s\frac{c_{gs2,4}}{g_{m2}}+1}\right) \quad \text{.....(7)}$$

Where $c_{gs2,4} = c_{gs2} + c_{gs4}$ is the total gate to source capacitance of Mn2 and Mn4.

Bandwidth from equation (7) is

$$\text{BW} = \sqrt{\left(\frac{g_{m2}g_{m1}}{C_{gs1}C_{gs2,4}}\right)}$$

The pole of the second order equation are obtained from equation (7) as

$$p1 = \frac{g_{m1}}{2C_{gs1}}\left[-1 \pm \sqrt{1-4\left(\frac{g_{m2}}{g_{m1}}\right)\left(\frac{C_{gs1}}{C_{gs2,4}}\right)-1}\right] \quad \text{.....(8)}$$

Equation (8) conclude that it has three different case of root location:

1) If

$$\left(\frac{g_{m2}}{C_{gs2,4}}\right) < \frac{1}{4}\left(\frac{g_{m1}}{C_{gs1}}\right)$$

The current mirror has two different negative real poles,

2) If

$$\left(\frac{g_{m2}}{C_{gs2,4}}\right) = \frac{1}{4}\left(\frac{g_{m1}}{C_{gs1}}\right)$$

It has two equal negative real poles $p1 = p2 = -\frac{g_{m1}}{2C_{gs1}}$. In this case the bandwidth is two times the bandwidth of basic current mirror.

3) If

$$\left(\frac{g_{m2}}{C_{gs2,4}}\right) > \frac{1}{4}\left(\frac{g_{m1}}{C_{gs1}}\right)$$

Then it has complex conjugate pole pair

$$p1 = \frac{g_{m1}}{2C_{gs1}}\left[-1 \pm j\sqrt{4\left(\frac{g_{m2}}{g_{m1}}\right)\left(\frac{C_{gs1}}{C_{gs2,4}}\right) - 1}\right]$$

Bandwidth is, $BW = \left(\frac{g_{m2}}{C_{gs2,4}}\right)\sqrt{2}$, that is 1.4 times the basic current mirror.

2.6 Characterization of cascode current mirror through PSPICE simulation

CMOS realisation of cascode current mirror is simulated through PSPICE using 350nm technology process parameters. Supply voltage used is $\pm$2.5V. Table 2.2 shows the aspect ratio used for different transistors of cascode current mirror. Cascode current mirror is characterized for its DC and AC responses. Various aspect parameters are calculated using PSPICE simulation.

Table 2.2: Aspect ratio of cascode current mirror used[2.9]

Element	W/L ratio	Element	W/L ratio
MB1	8.6u/.85u	MP4	8.6u/.85u
MB2	8.6u/.85u	MN1	2u/.85u
MP1	8.6u/.85u	MN2	2u/.85u
MP2	8.6u/.85u	MN3	2u/.85u
MP3	8.6u/.85u	MN4	2u/.85u

2.6.1 DC characteristics

The general PSPICE schematic of cascode current mirror is shown in Fig 2.6.1. To verify the current mirroring accuracy, DC curve between I_{in} and I_{out} is plotted in Fig 2.6.2.

DC curve between Iin and Iout while keeping I_{bias} = 20uA is shown in Fig 2.6.3.

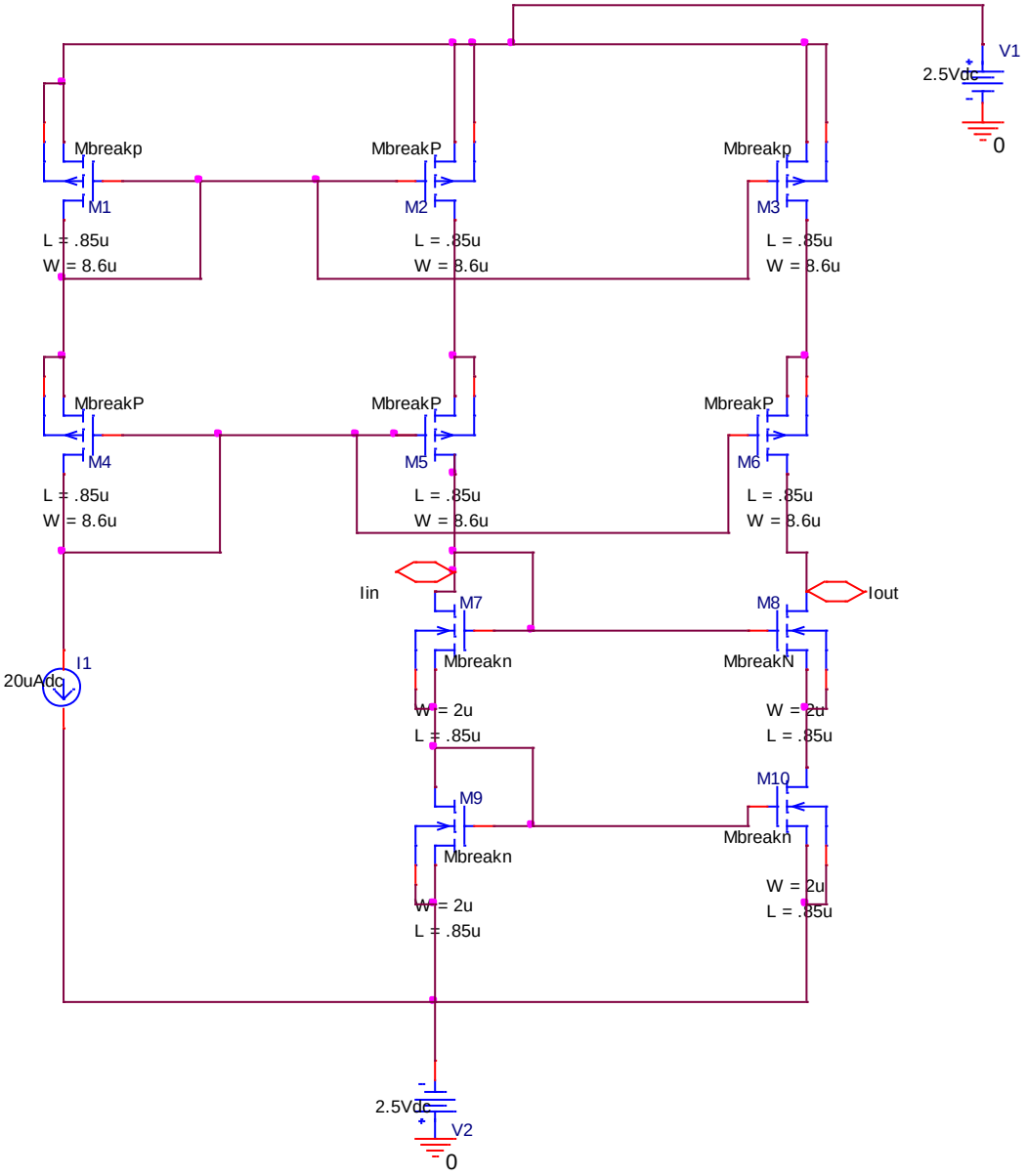


Fig 2.6.1: SPICE simulation of cascode of current mirror.

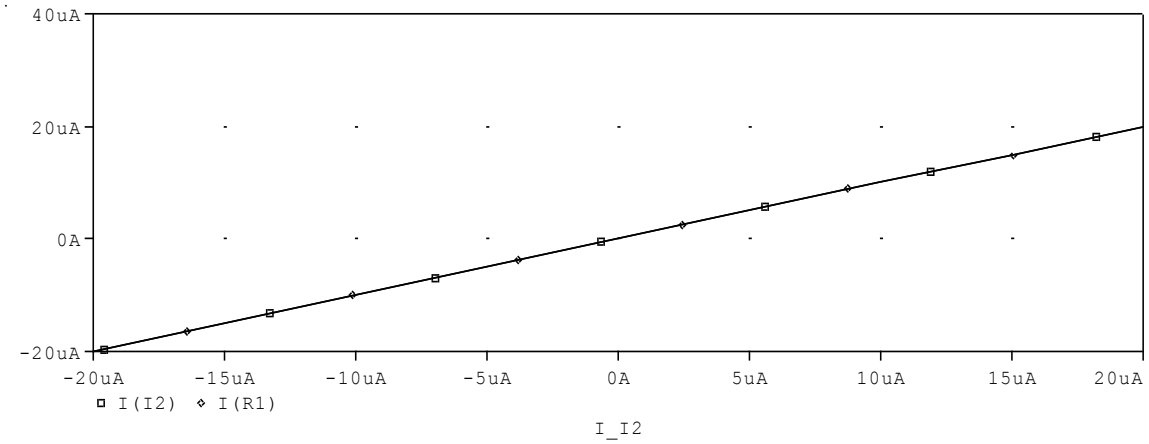


Fig 2.6.2: I_{in} versus I_{out}

Current mirroring accuracy also depends upon the biasing current. Because proper biasing keep all the transistors in active/saturation region. And for proper working of cascode current mirror this is necessary condition. Graph of I_{out} versus I_{in} for different biasing current is shown in Fig 2.6.3.

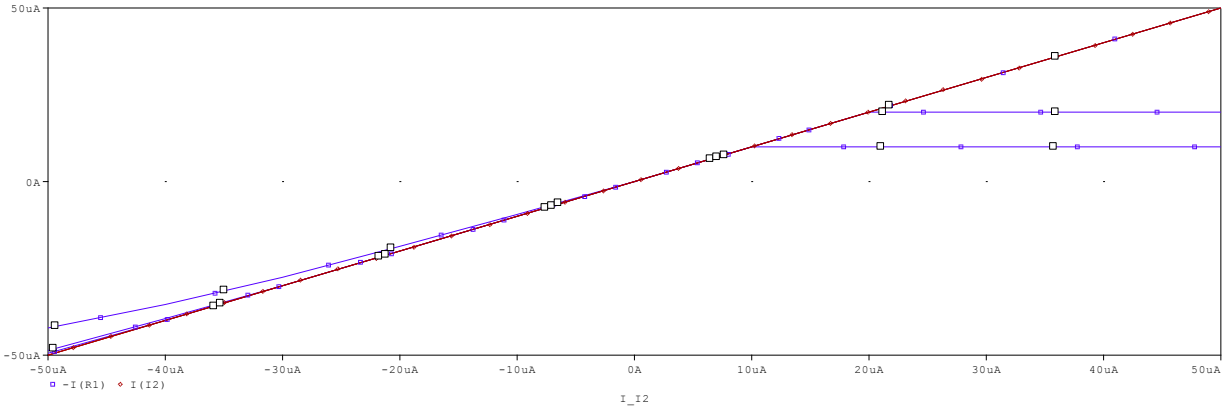


Fig 2.6.3: I_{in} versus I_{out} for different biasing current (I_{bias})

2.6.2 AC characteristics:

For AC characteristics of the cascode current mirror, an AC signal of 1mA is applied at the input. Current at output terminal is obtained to be exactly 1mA. The simulation curve is shown in Fig 2.6.4

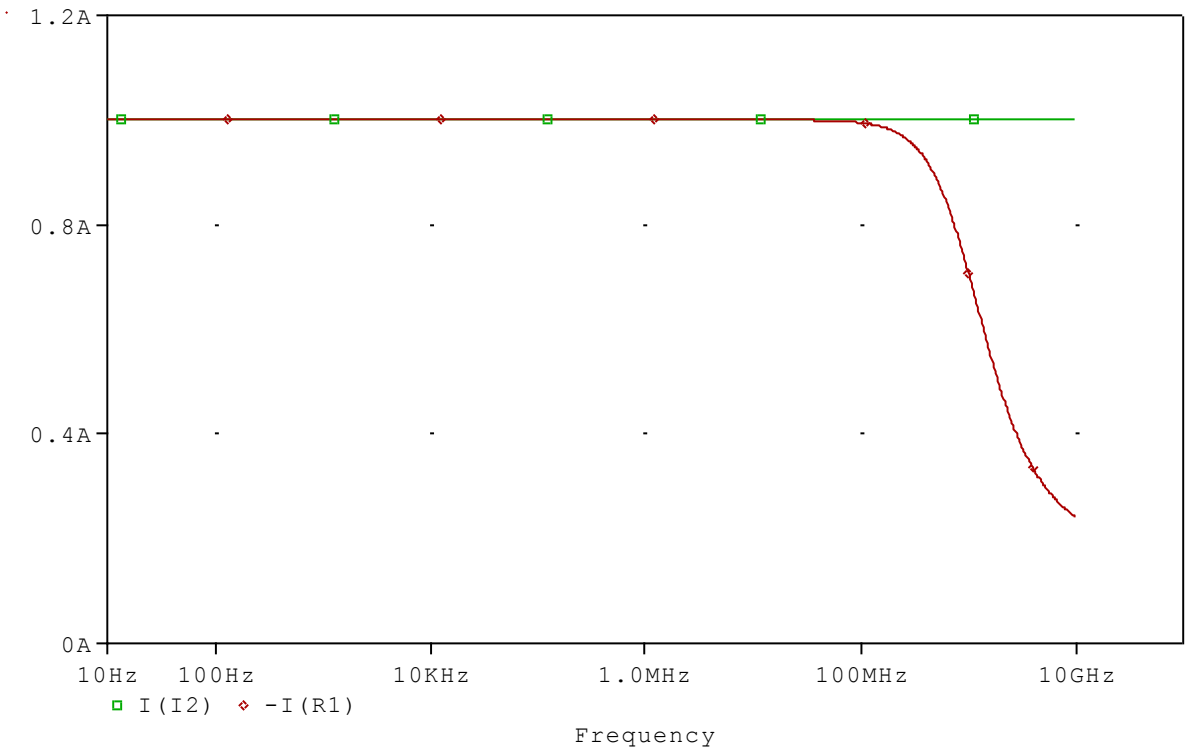


Fig 2.6.4: i_{out} and i_{in} versus frequency.

As it can be seen from the fig that Iout follows completely to the Iin till 71.79MHz.

The 3-db bandwidth of the cascode current mirror is 1.03GHz. Up to 1.03GHz it acts as perfect current mirror i.e. its current mirroring accuracy is very good.

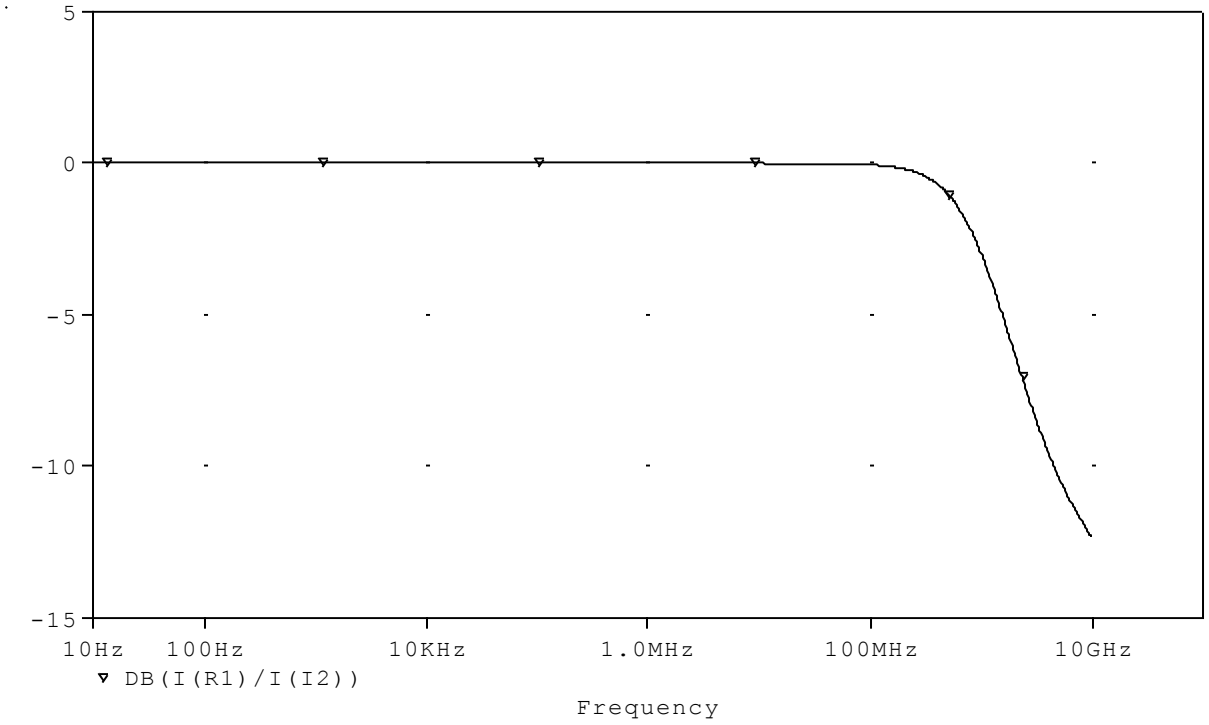


Fig 2.6.5: I_{in}/ I_{out} (db) versus frequency

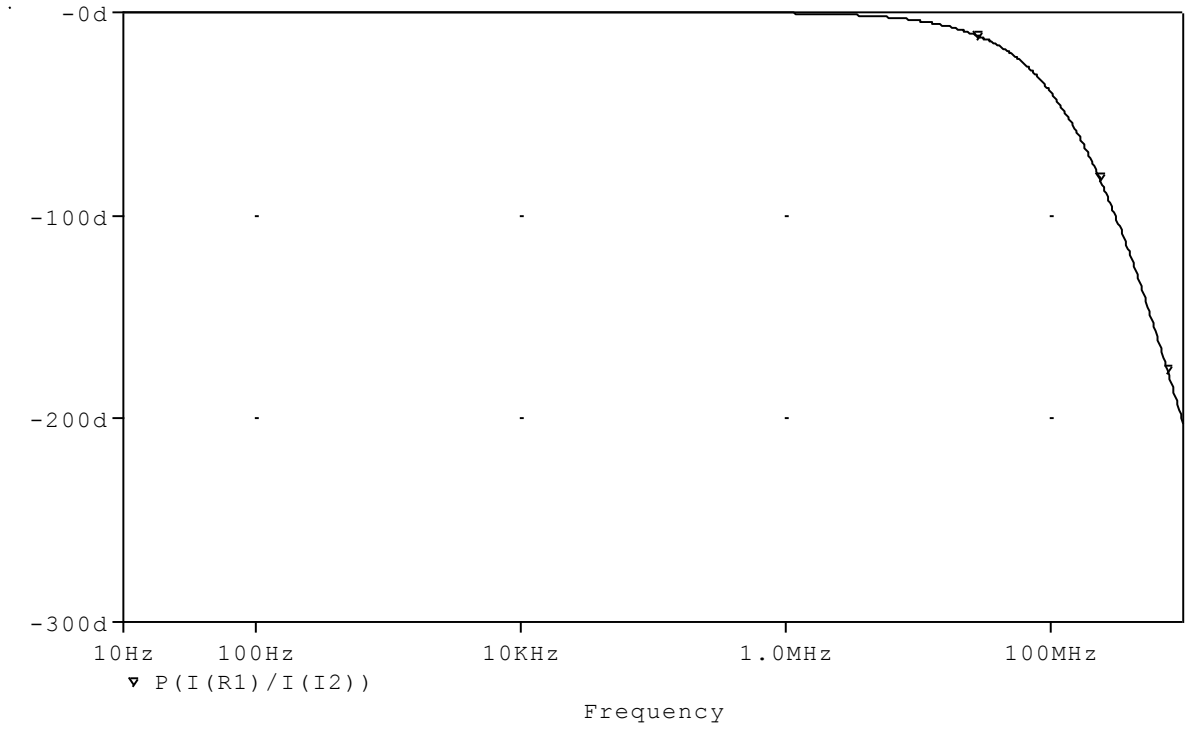


Fig 2.6.6: Phase response of current mirror

To determine the input impedence at input terminal, other terminal i.e. output terminal is kept open. AC current source is applied at the input terminal and corresponding voltage across that terminal is obtained. The input impedence obtained is 18.40k ohm as shown in Fig 2.6.7.

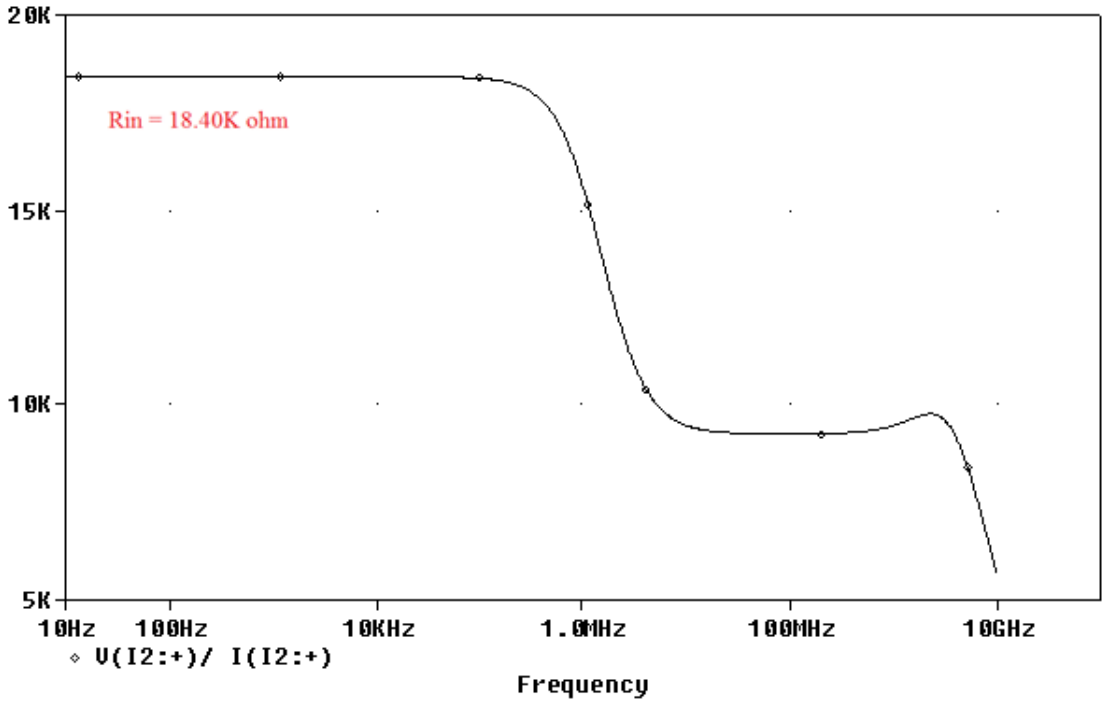


Fig 2.6.7: Input resistance obtained at input terminal

Similarly to see the output resistance at the output terminal, open circuit the input terminal and apply an AC current signal at the output terminal . Get the voltage across that AC current signal.

Take the ratio of output voltage to the output current. Output resistance obtained is 86.13M ohm as shown in Fig 2.6.8. Output resistance of this cascode current mirror is highest as compare to other structure of the current mirror except few.

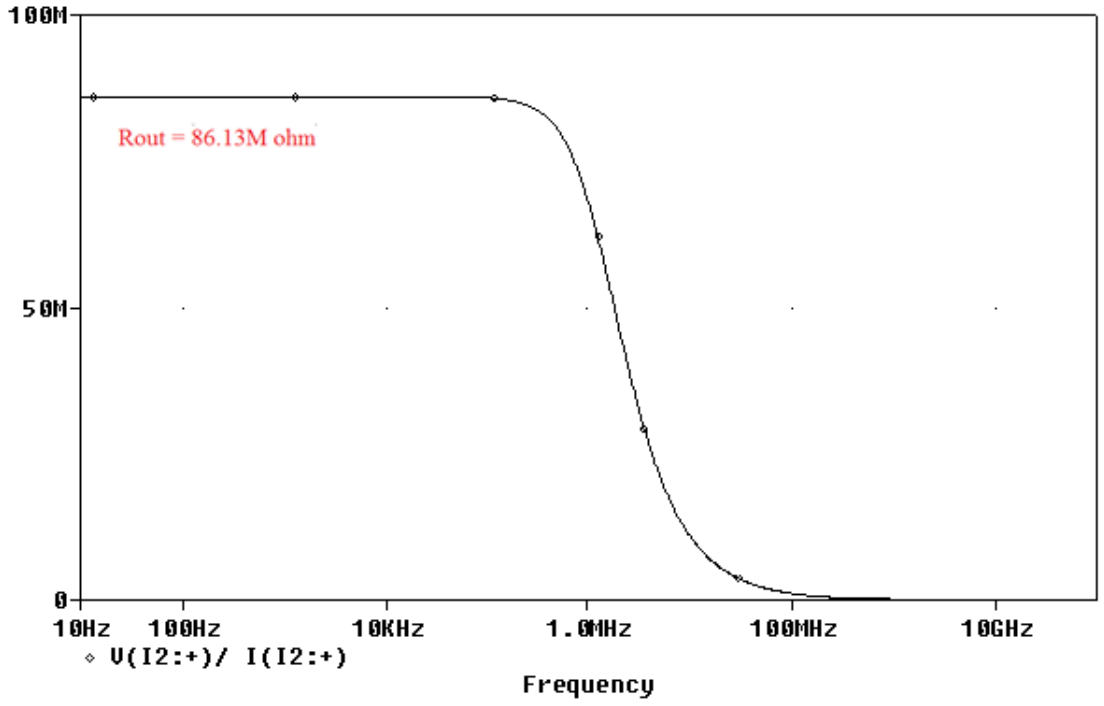


Fig 2.6.8: Output resistance obtained at the output terminal

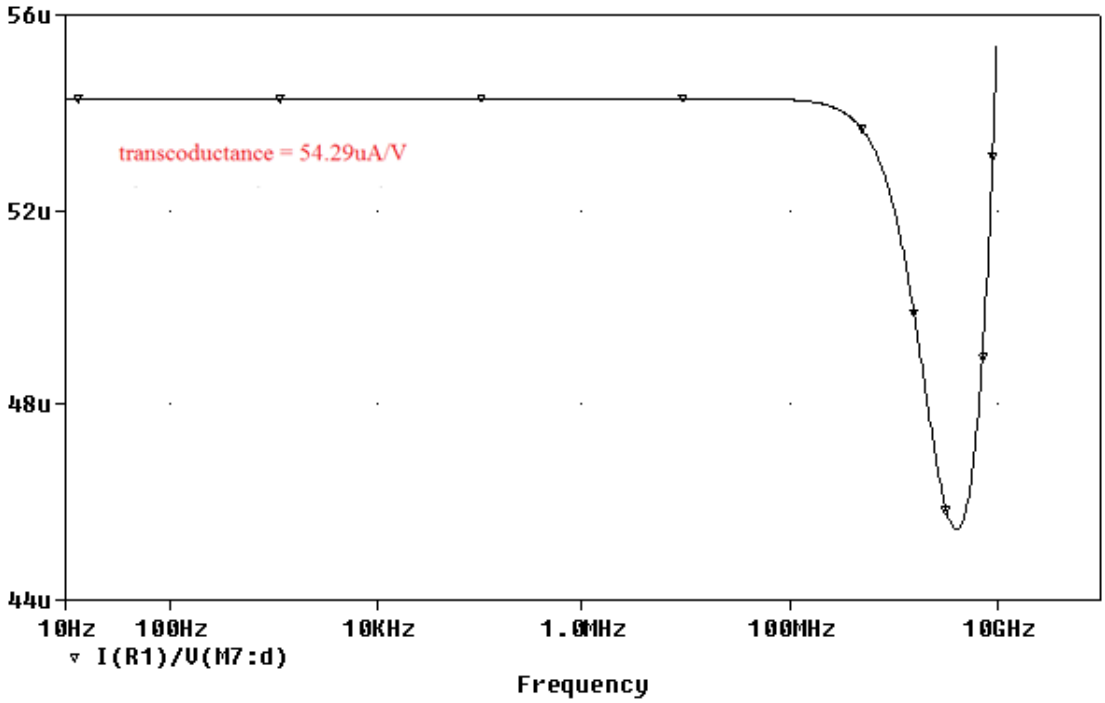


Fig 2.6.9: Transconductance versus frequency.

To determine the α variation of output current with frequency for biasing current 20uA was plotted. And the curve is shown in Fig 2.6.10. The value of α was obtained to be 0.999 which is approximately equal to unity.

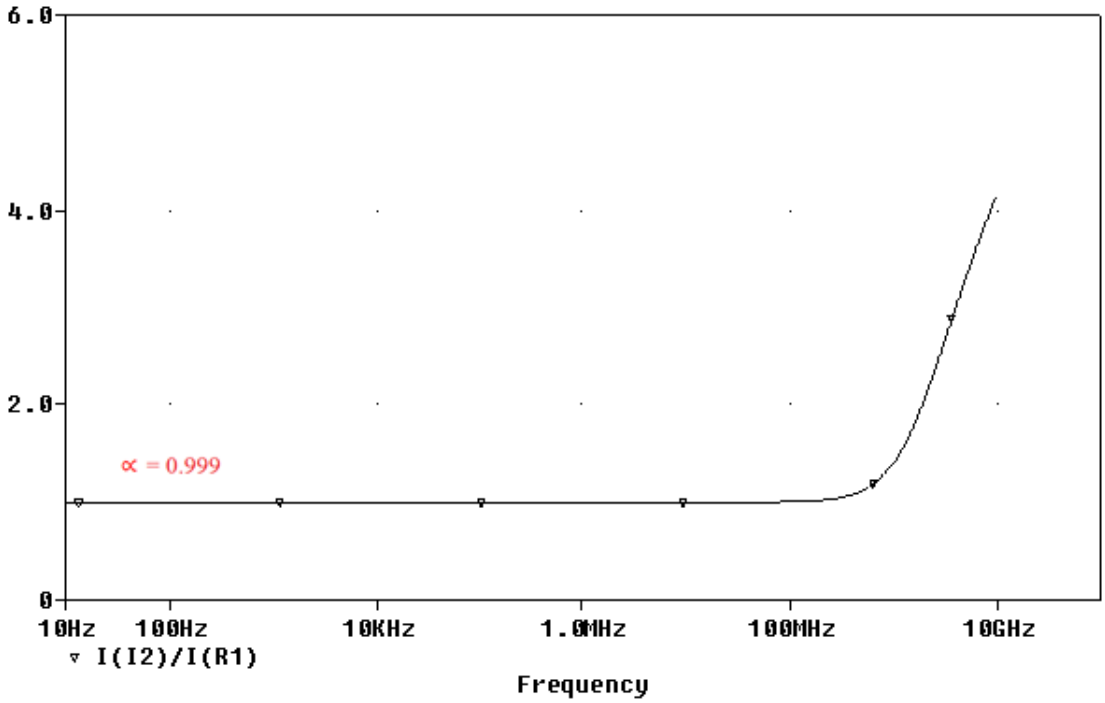


Fig 2.6.10: I_{out}/I_{in} with frequency keeping (I_{in} = 1mA)

Total power dissipation of the cascode current mirror block is 0.3m Watts. Which is large as compare to the other current mirrors because as number of the transistors increase, power dissipation also increases.

The performance parameters obtained through simulation are listed in Table 2.3.

Table 2.3: Performance parameters of CMOS cascode current mirror

Parameter	**Value**
Technology	350nm
Supply voltage	2.5V
Bias current	20u A
Transconductance	54.29u A/V
Iout/Iin(-3db) bandwidth	1.03G Hz
Input resistance	18.4K ohm
Output resistance	86.13M ohm
$\propto$	0.999
Power consumption	0.3m Watts

2.7 Conclusion:

After analyzing all current mirrors, it is concluded that CMOS based cascode current mirror has high output resistance, larger bandwidth, high accuracy. But it is also observed that it has maximum number of transistors so power dissipation is maximum which is quite obvious. Characteristics for which current mirror is used are (a) it should have high output resistance. (b) channel length modulation should be negligible. These characteristics fulfills only cascode current mirror. Also it has high accuracy of mirroring an input current at the output.

Chapter 3

APPLICATIONS OF CURRENT MIRROR

In this chapter few analog basic building blocks such as current inverter, adder, subtractor are implemented using current mirror. First order, second order low pass filter, SIMO filter, LT filter, sinusoidal to square wave generator are also implemented using CMOS based cascode current mirror. These all simulation are done using SPICE simulation. In these applications theoretical and experimental results are checked and then verified.

3.1 Basic Building blocks

In this section current mirror based basic analog building blocks which are used for CM analog circuits. The workability of these analog building blocks are verified using SPICE simulation. The supply voltage of$\pm$2.5 V and in biasing circuit biasing current is 20 µA are used.

3.1.1 Current Adder

Current mirror can be used for addition of two current signals. In the Fig 3.1.1, two current signals are added and result can be expressed as

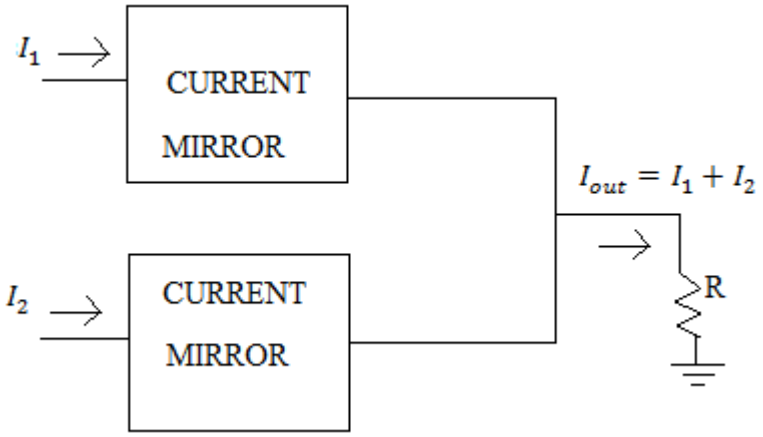


Fig 3.1.1: Block diagram of adder using current mirror.

Current adder circuit's functionality can be verfied by taking two current signals of same frequency at an input terminal of having $I_1 = 5\ \mu A\ and\ I_2 = 15\ \mu A$ current mirror. So output current I_{out} obtained to be $I_{out} = 20\ \mu A$ as shown in Fig 3.1.2.

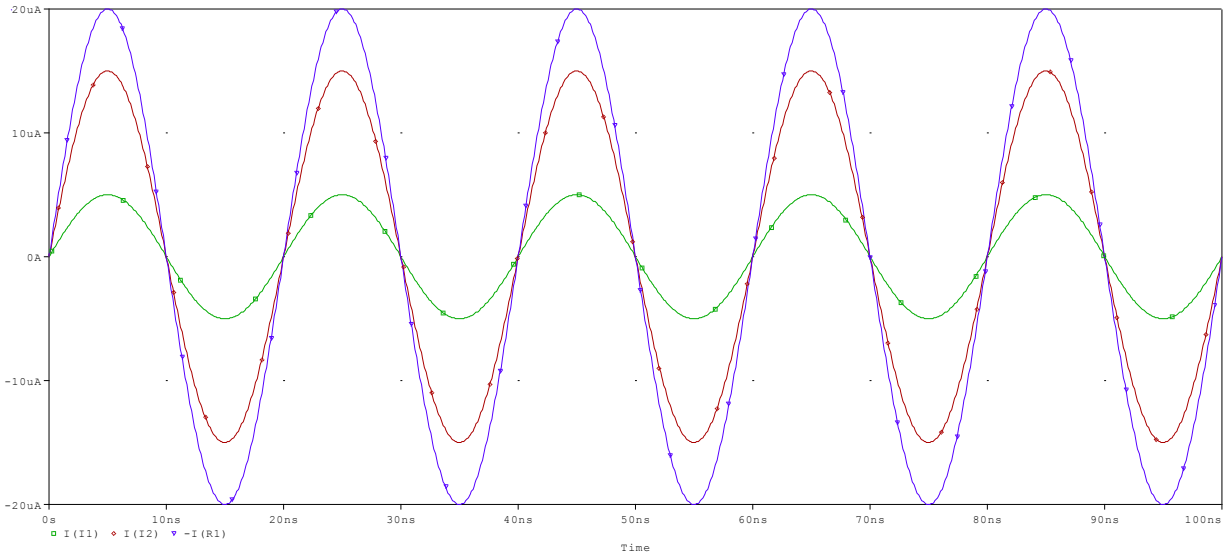


Fig 3.1.2: Transient response of adder block

3.1.2 Current Inverter

Whatever current signal is applied at the input terminal this block invert that input signal as shown in Fig 3.1.3. We can say when a current signal is passed by this block we get the same signal but 180 degree phase shift as shown in Fig 3.1.4.

$$I_{out} = -I_{in}$$

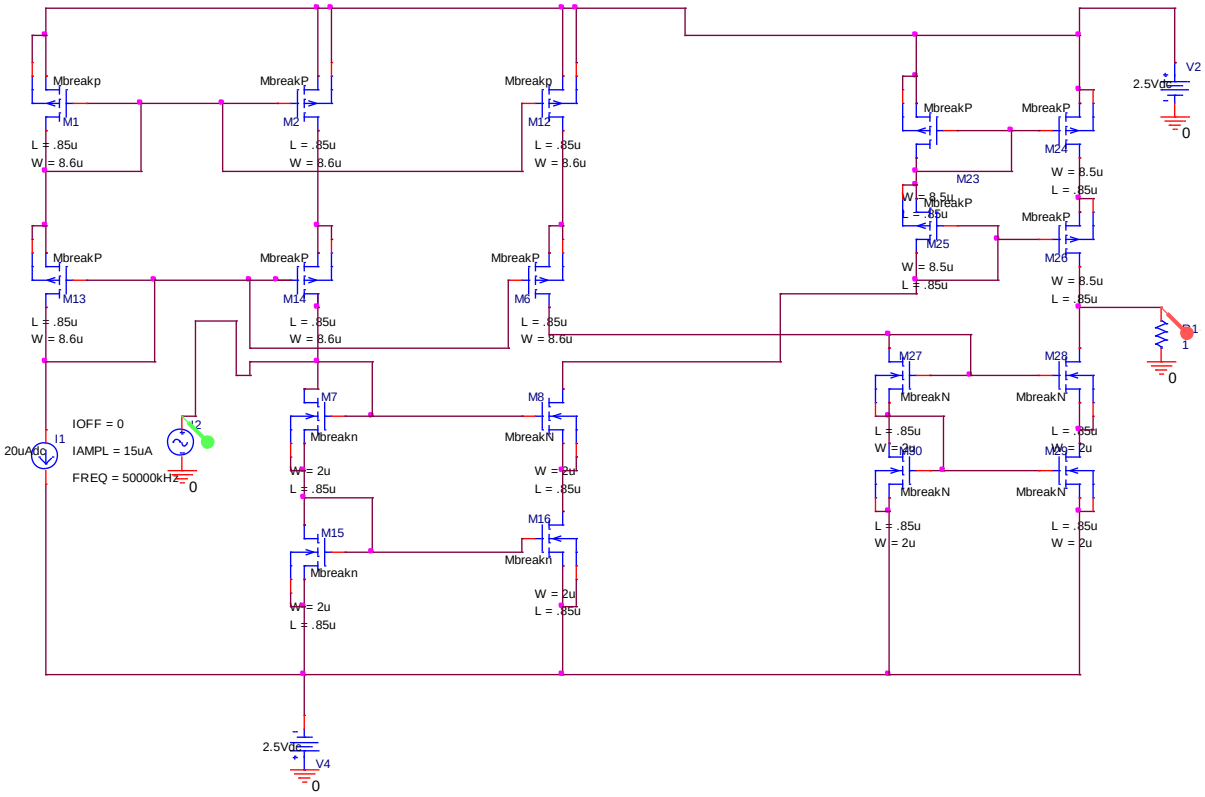


Fig 3.1.3: Schematic of current inverter.

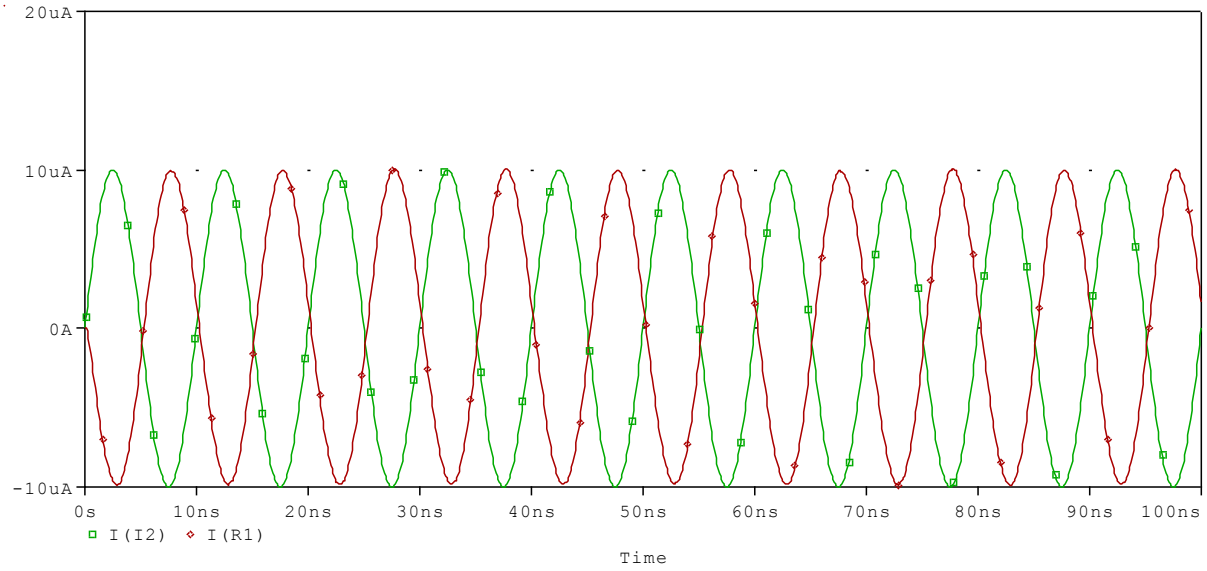


Fig 3.1.4: Time response of current inverter block.

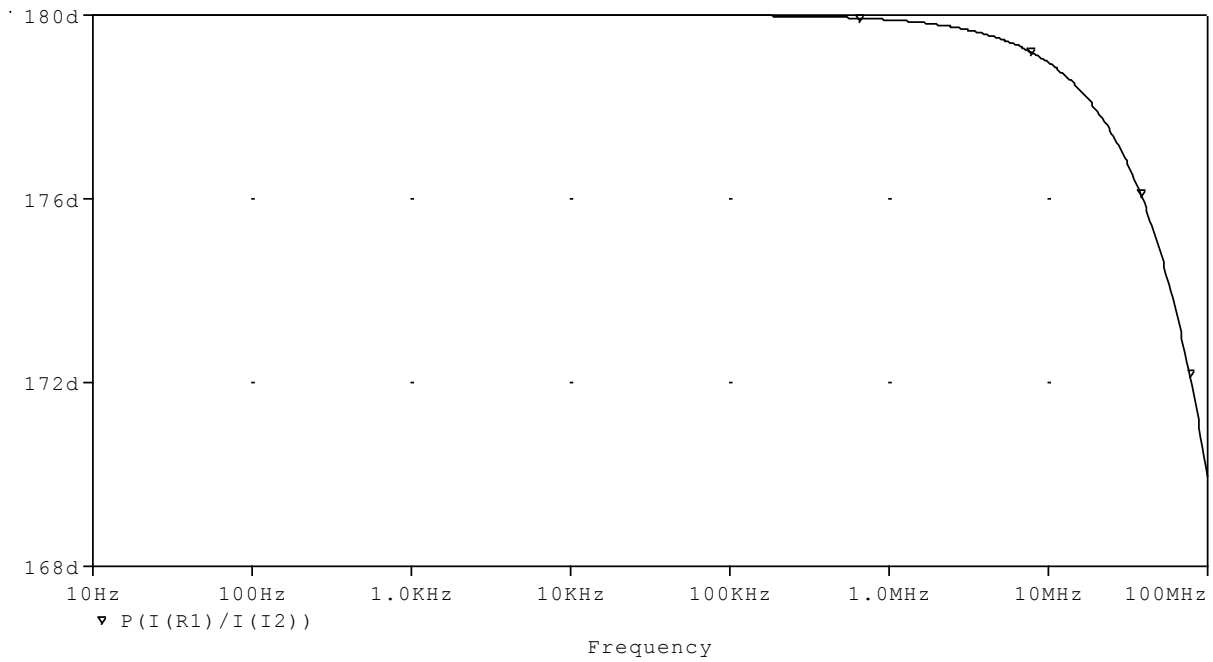


Fig 3.1.5: Phase response of current inverter.

3.1.3 Current subtractor

When first current signal applied to current mirror and second current signal to the current inverter, output of these block are joint and output taken through the resistance. Output is the difference of the two current signal as shown in Fig 3.1.6.

$$(I_{out} = I_1 - I_2)$$

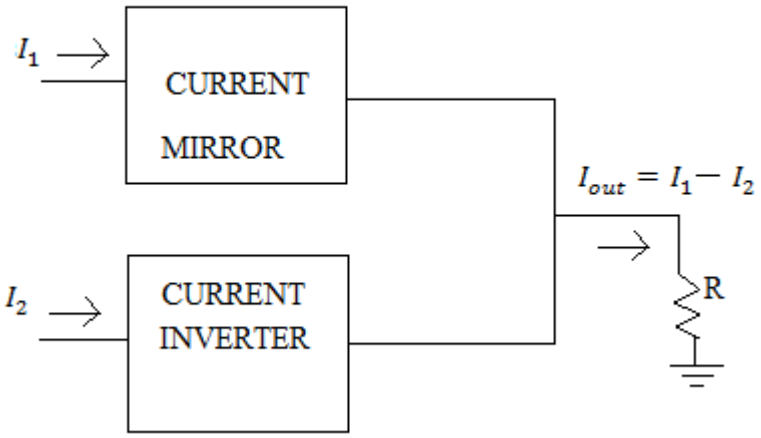


Fig 3.1.6: Block diagram of current subtractor

Current subtractor circuit's functionality can be verfied by taking two current signals of same frequency at an input terminal of having $I_1 = 15\ \mu A$ *and* $I_2 = 10\ \mu A$ current mirror. So output current I_{out} obtained to be $I_{out} = 5\ \mu A$. But due to some offset current it is not exactly 5 μA but little bit larger than 5 μA as shown in Fig 3.1.7.

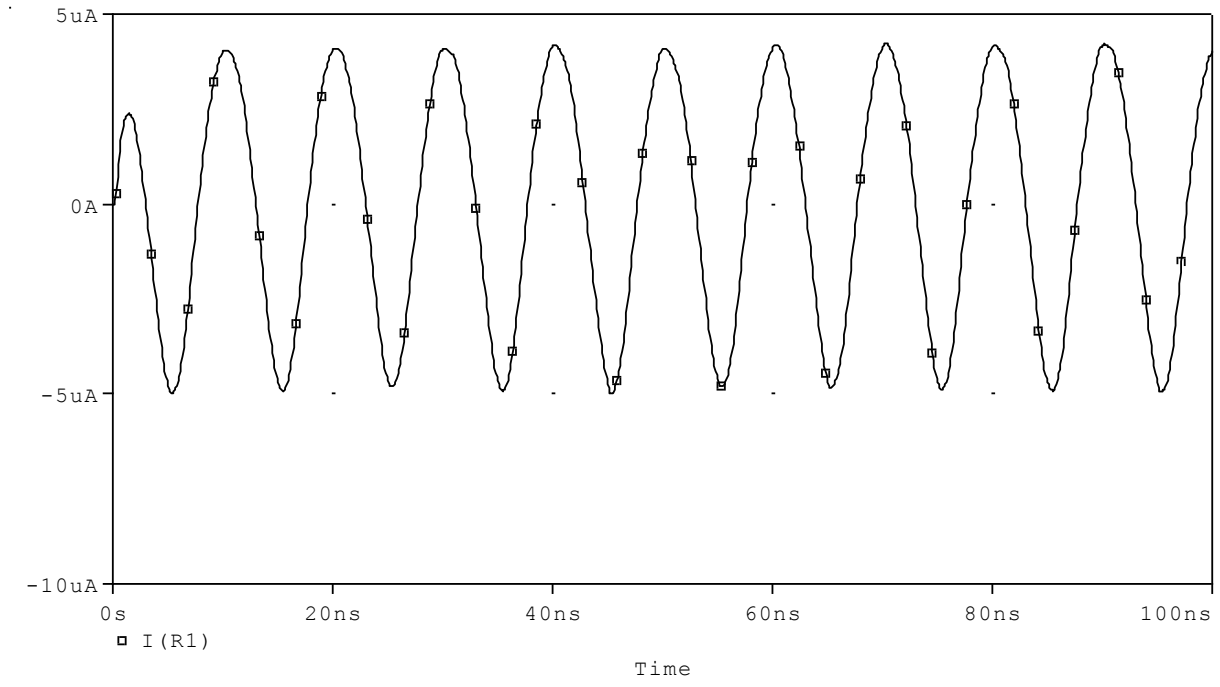


Fig 3.1.7: Transient response of subtractor block.

3.2 Filters

3.2.1 First order low pass filter

Implementation of the first order low pass filter is shown in Fig 3.2.1. How it is designed it is shown in Fig 3.2.2, this is the core of the filter in which a lossy integrator used which works as loss pass filter.

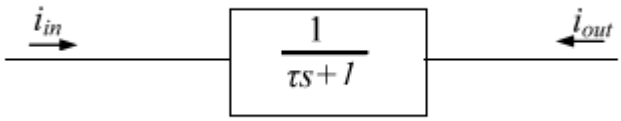


Fig 3.2.1: Core of the filter[3.1].

Transfer function of the low pass filter using core diagram is

$$\frac{i_{0ut}}{i_{in}} = \frac{1}{1+\tau s}$$

Where τ is the time constant of the filter which is equal to

$$\tau = \frac{C}{g_{m.\ Mn1}}$$

Where $g_{m.\ Mn1}$ is the small signal transconductance of the transistor Mn1.

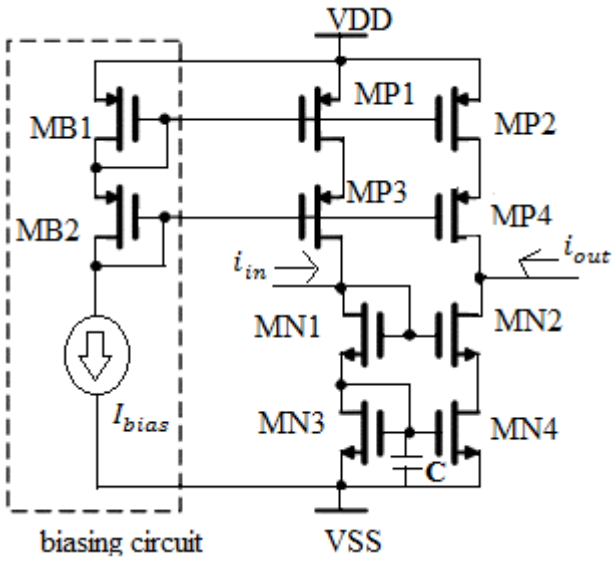


Fig 3.2.2: Low pass filter using current mirror.

The workability of the LPF is verified through SPICE simulation. The values of the components used are 60 nF, $I_{bias} = 20\ \mu A$.AC magnitude and phase response of the lpf is shown in Fig 3.2.3 and Fig 3.2.4 respectively. -3 db frequency (3-db bandwidth) of the filter is 120 Hz.

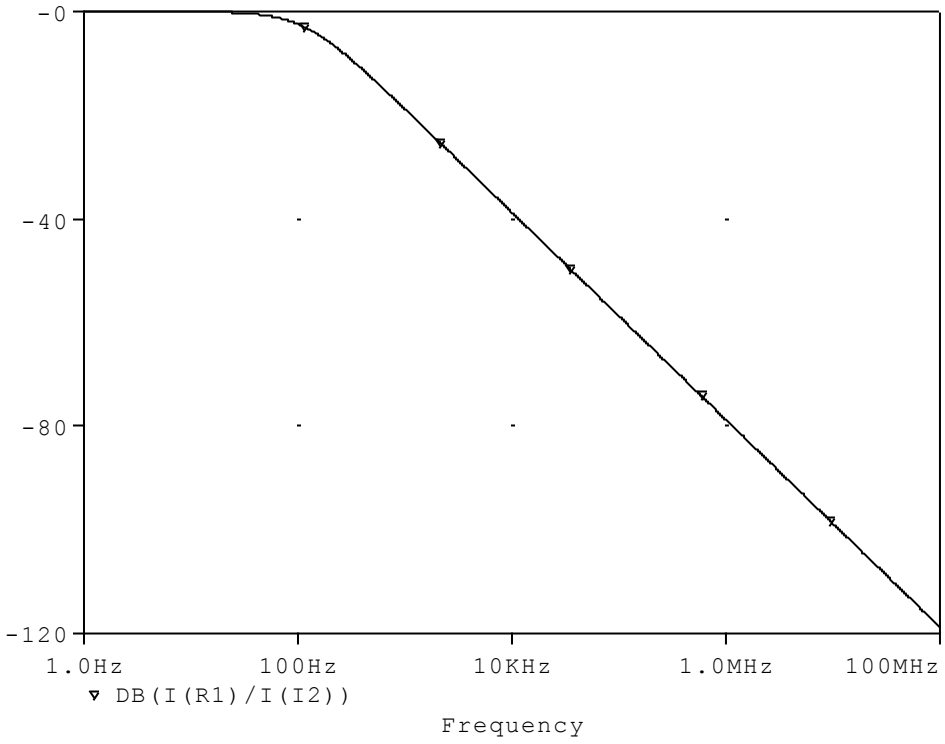


Fig 3.2.3: AC magnitude response of the low pass filter

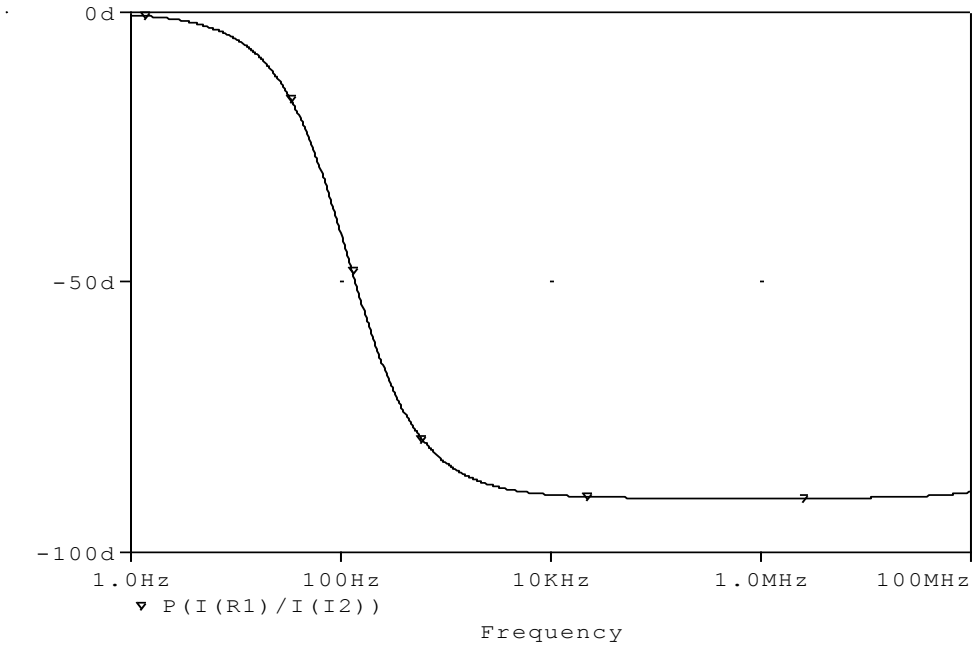


Fig 3.2.4: AC Phase response of the low pass filter

3.2.2 Second order low pass filter

Cascading of lossy and lossless integrator, we get a second order LPF as shown in Fig 3.2.5. Through this cascding method , any type of transfer function can be generated.

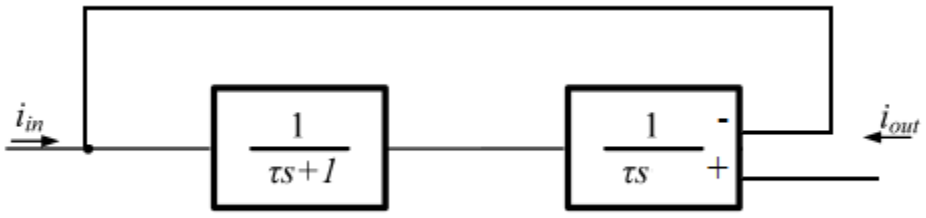


Fig 3.2.5: Block diagram of the second order filter[3.2].

Transfer function of the second order LPF is

$$\frac{i_{out}}{i_{in}} = \frac{1}{1 + (1 + \tau s)(\tau s)}$$

AC magnitude and phase respose of the second order LPF is shown in Fig 3.2.6 and Fig 3.2.7 respectively.

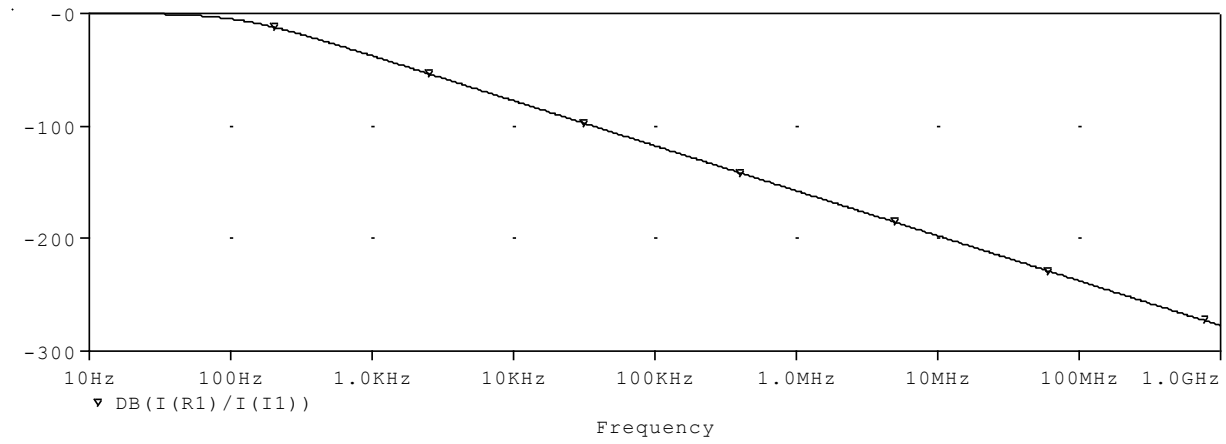


Fig 3.2.6: AC magnitude response of second order LPF

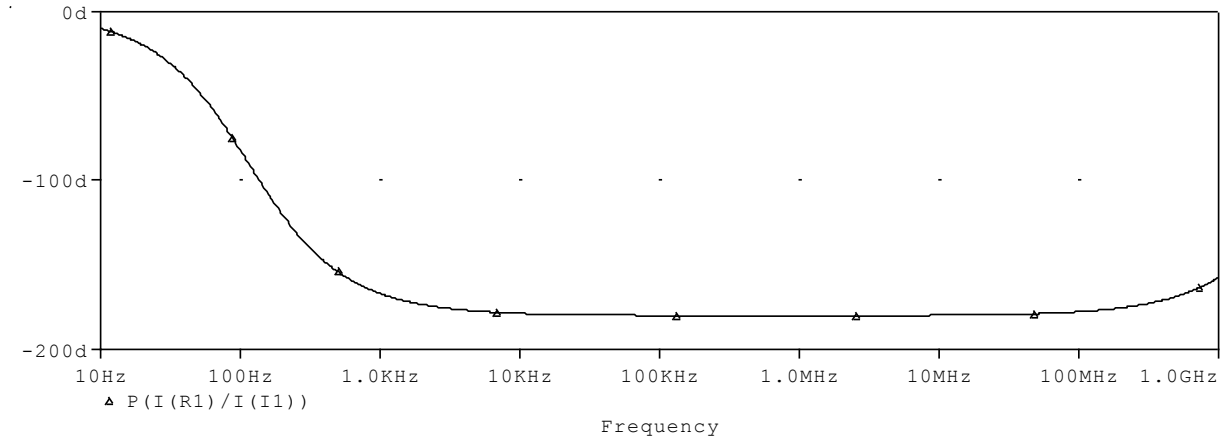


Fig 3.2.7: AC phase response of the filter

3.2.3 LT FILTER

In this filter, two port V-I domain is converted into new x-y domain. There are three different section: input, output and middle. To simplify the complexities of transformation matrix take α_{ji} and δ_{ji}=0 for shunt arms, and β_{ji} and γ_{ji} = 0 for series arms. To reduce the SI cells choose either α_{ji} or $\gamma_{ji} = \pm G$ and either β_{ji} or $\delta_{ji} = \pm 1$[3.3].

Relationship between input, output current and voltage in terms of transmission parameter is

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \text{.....(3.1)}$$

Where both I_1 and I_2 are assumed to flow into the network.
Consider the new port variable can be defined in terms of two nonsingular transformation matrices as

$$\begin{bmatrix} x_1 \\ y_1 \end{bmatrix} = \begin{bmatrix} \alpha_1 & \beta_1 \\ \gamma_1 & \delta_1 \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \text{.....(3.2)}$$

$$\begin{bmatrix} x_2 \\ y_2 \end{bmatrix} = \begin{bmatrix} \alpha_2 & \beta_2 \\ \gamma_2 & \delta_2 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \text{.....(3.3)}$$

From above the three equation

$$\begin{bmatrix} x_1 \\ y_1 \end{bmatrix} = \begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} x_2 \\ y_2 \end{bmatrix}$$

Where

$a = \{\alpha_1 (\delta_2 A - \gamma_2 B) + \beta_1(\delta_2 C - \gamma_2 D)\}/\Delta_2$
$b = \{\alpha_1 (\alpha_2 B - \beta_1 A) + \beta_1(\alpha_2 D - \beta_2 C)\}/\Delta_2$
$c = \{\gamma_1(\delta_2 A - \gamma_2 B) + \delta_1(\delta_2 C - \gamma_2 D)\}/\Delta_2$
$d = \{\gamma_1(\alpha_2 B - \beta_2 A) + \delta_1(\alpha_2 D - \beta_2 C)\}/\Delta_2$

$\Delta_2 = \alpha_2 \delta_2 - \beta_2 \gamma_2$

Now transpose of $[y_1\ y_2]$ can be found from the above equation in terms of transpose of $[x_1\ x_2]$ as

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} d/b & -(ad - bc)/b \\ \frac{1}{b} & -\frac{a}{b} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

For series and shunt arms

$\begin{bmatrix}1 & -Z\\ 0 & -1\end{bmatrix}$ and $\begin{bmatrix}1 & 0\\ Y & -1\end{bmatrix}$

For both matrices

A=1, D= -1, and BC=0

Interconnection matrix is

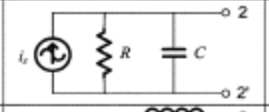
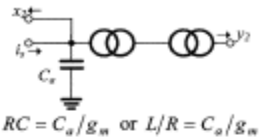
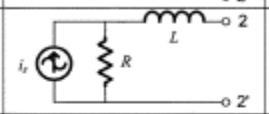
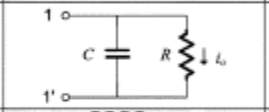
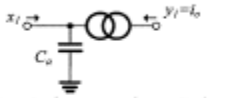
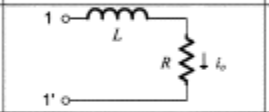
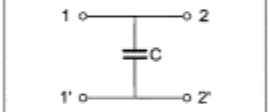
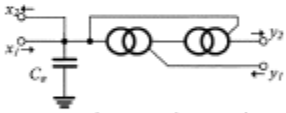
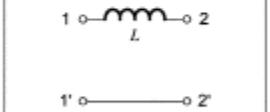
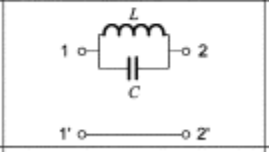
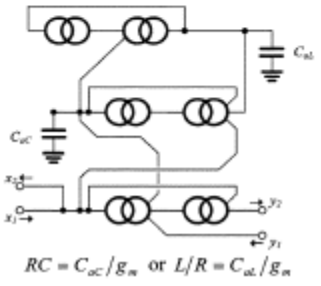
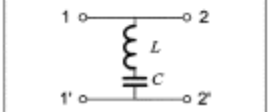
$\begin{bmatrix}V_1\\ I_1\end{bmatrix}=\begin{bmatrix}1 & 0\\ 0 & -1\end{bmatrix}\begin{bmatrix}V_2\\ I_2\end{bmatrix}$.

Let us consider the input terminal of the ladder filter connected to the current source i_s. From the Table 3.1. if we choose the transformation matrix as

$\begin{bmatrix}\alpha_2 & \beta_2\\ \gamma_2 & \delta_2\end{bmatrix}=\begin{bmatrix}0 & 1\\ G & 0\end{bmatrix}$ then the expression for y_2 is

$y_2=\frac{i_s-x_2}{\tau s+1}$ where $\tau = RC$ is the time constant and R = 1/G and this relationship can be realized by a two input CM based lossy integrator as shown in table

Table 3.1 CM based substitution scheme[3.4]

	Passive filter section	Transformation matrix and transfer function	Current mirror based LT equivalent
1		$\begin{bmatrix}0 & 1\\ G & 0\end{bmatrix}$ $y_2=\frac{i_s-x_2}{\tau s+1}$ $\tau=RC$	 $RC=C_a/g_m$ or $L/R=C_a/g_m$
2		$\begin{bmatrix}G & 0\\ 0 & 1\end{bmatrix}$ $y_2=\frac{i_s-x_2}{\tau s+1}$ $\tau=L/R$	
3		$\begin{bmatrix}0 & 1\\ G & 0\end{bmatrix}$ $y_1=\frac{x_1}{\tau s+1}$ $\tau=RC$	 $RC=C_a/g_m$ or $L/R=C_a/g_m$
4		$\begin{bmatrix}G & 0\\ 0 & 1\end{bmatrix}$ $y_1=\frac{x_1}{\tau s+1}$ $\tau=L/R$	
5		$\begin{bmatrix}0 & 1\\ G & 0\end{bmatrix}\begin{bmatrix}0 & 1\\ G & 0\end{bmatrix}$ $y_2=-y_1=\frac{x_1-x_2}{\varpi}$ $\tau=RC$	 $RC=C_a/g_m$ or $L/R=C_a/g_m$
6		$\begin{bmatrix}G & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}G & 0\\ 0 & 1\end{bmatrix}$ $y_2=-y_1=\frac{x_1-x_2}{\varpi}$ $\tau=L/R$	
7		$\begin{bmatrix}G & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}G & 0\\ 0 & 1\end{bmatrix}$ $y_2=-y_1=\frac{\tau_1\tau_2 s^2+1}{\tau_2 s}(x_1-x_2)$ $\tau_1=RC,\tau_2=L/R$	 $RC=C_{ac}/g_m$ or $L/R=C_{aL}/g_m$
8		$\begin{bmatrix}0 & 1\\ G & 0\end{bmatrix}\begin{bmatrix}0 & 1\\ G & 0\end{bmatrix}$ $y_2=-y_1=\frac{\tau_1\tau_2 s^2+1}{\tau_2 s}(x_1-x_2)$ $\tau_1=RC,\tau_2=L/R$	

The fifth order elliptic filter is shown in Fig 3.2.8. The workability of the filter is shown in Fig 3.2.9. The values of the capacitors of the active filter are C_{a1}=11.89pF, C_{ac2}=21.10pF, C_{aL2}=4.23pF, $C_{a3}=19.11pF$, C_{aC4}=6.24pF, C_{aL4}=8.22pF and C_{a5}=7.40pF. And its -3db bandwidth is 812k Hz.

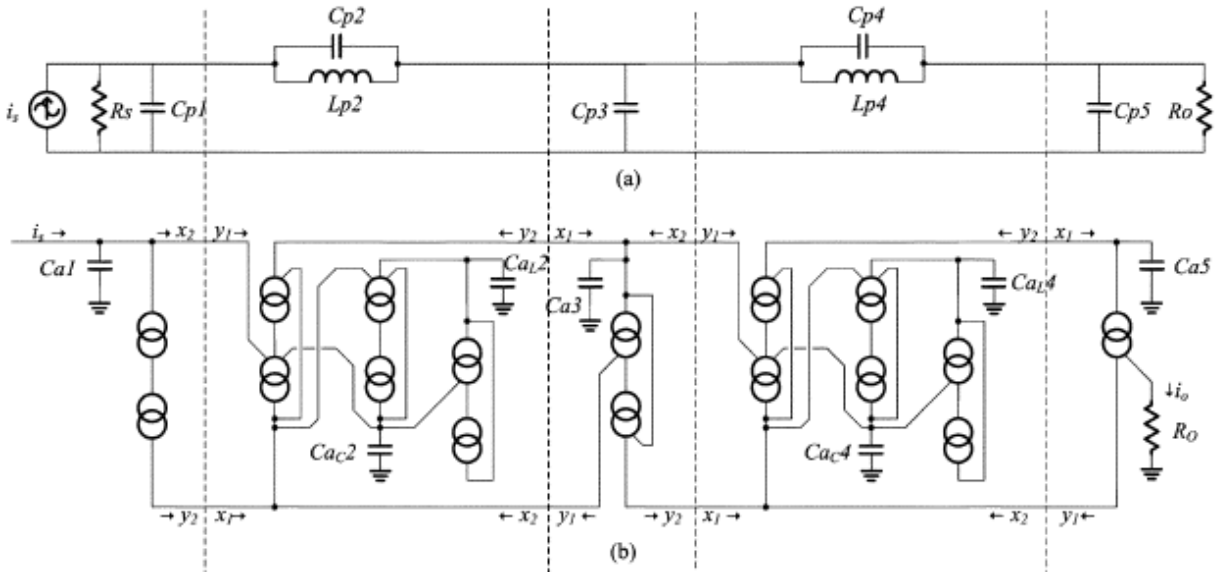


Fig 3.2.8:Block diagram of fifth order ellptic filter[3.5]

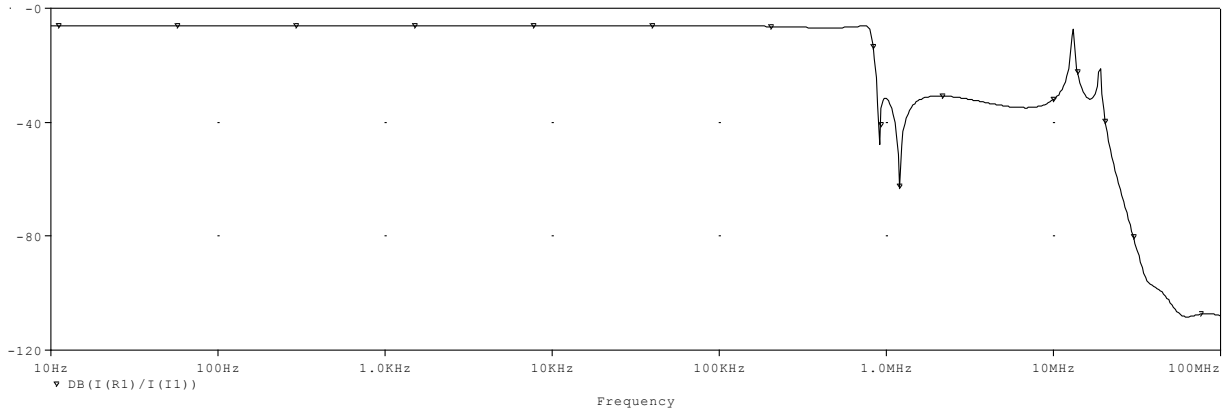


Fig 3.2.9 : Frequency response of fifth order elliptic filter

3.2.4 SIMO filter

This is universal biquad filter topology and block diagram of SIMO filter is shown in Fig 3.2.10. in which SIMO current mirror is used. Five standard filter can be desribed as:

Table 3.2: Transfer function of second order filter.

Filter type	Input	Transfer function
LPF	$i_{in1} = i_{in}$	$\frac{i_{out}}{i_{in}} = \frac{w_0^2}{s^2 + Bs + w_0^2}$
BPF	$i_{in2} = i_{in}$	$\frac{i_{out}}{i_{in}} = \frac{Bs}{s^2 + Bs + w_0^2}$
BSF	$i_{in2} = i_{in3} = i_{in}$	$\frac{i_{out}}{i_{in}} = \frac{s^2 + w_0^2}{s^2 + Bs + w_0^2}$
HPF	$i_{in2} = i_{in}$	$\frac{i_{out}}{i_{in}} = \frac{s^2}{s^2 + Bs + w_0^2}$
APF	$i_{in2} = i_{in3} = i_{in4} = i_{in}$	$\frac{i_{out}}{i_{in}} = \frac{s^2 - Bs + w_0^2}{s^2 + Bs + w_0^2}$

Where natural frequency $w_0 = \frac{g_m}{\sqrt[2]{C_1 C_2}}$, bandwidth(B) = $\frac{1}{g_m \sqrt[2]{C_1 C_2}}$ and quality factor(Q) = $\sqrt[2]{\frac{C_1}{C_2}}$

The workability of this filter can be verified through SPICE simulation. This multifunction filter is designed for 1.8MHz frequency for which capacitance choose are $C_1 = 2.8\,pF$ *and* $C_2 = 3\,pF$.

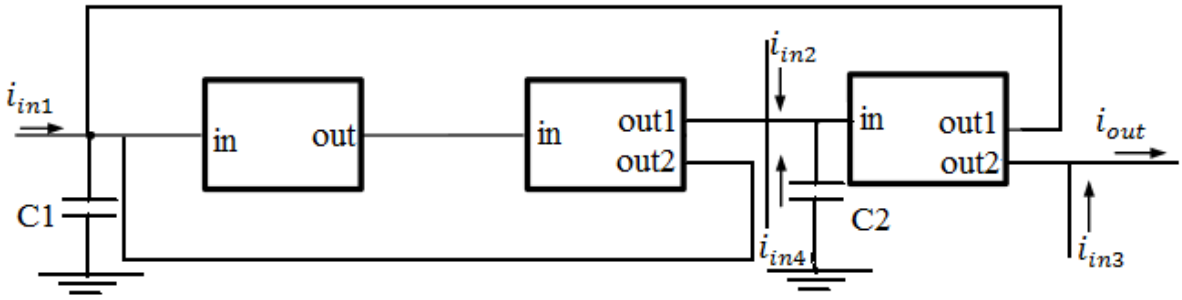


Fig 3.2.10: Block diagram of SIMO biquad filter[3.6].

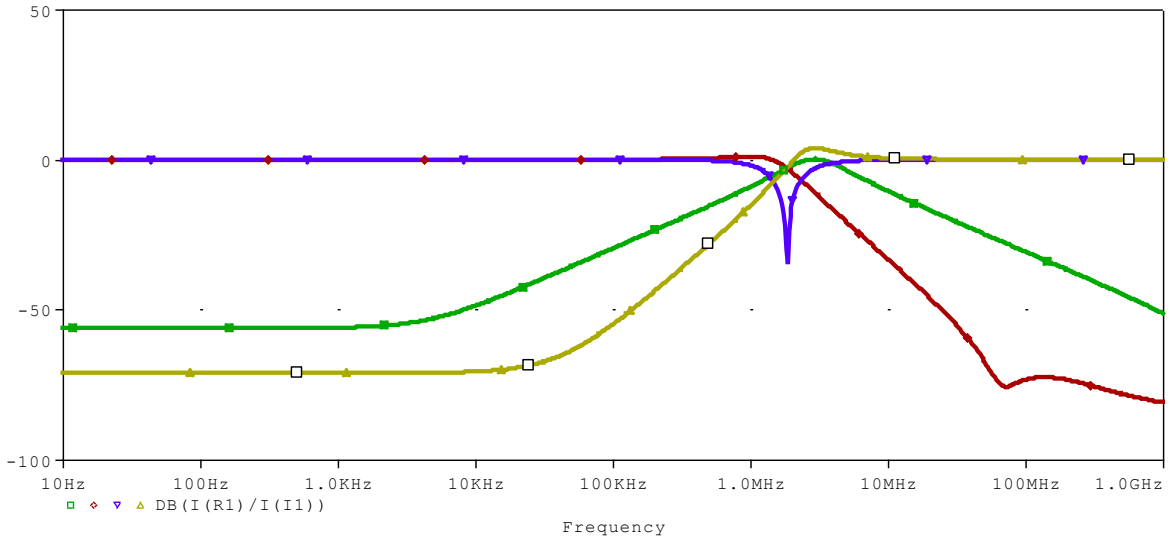


Fig 3.2.11: AC response of all filters

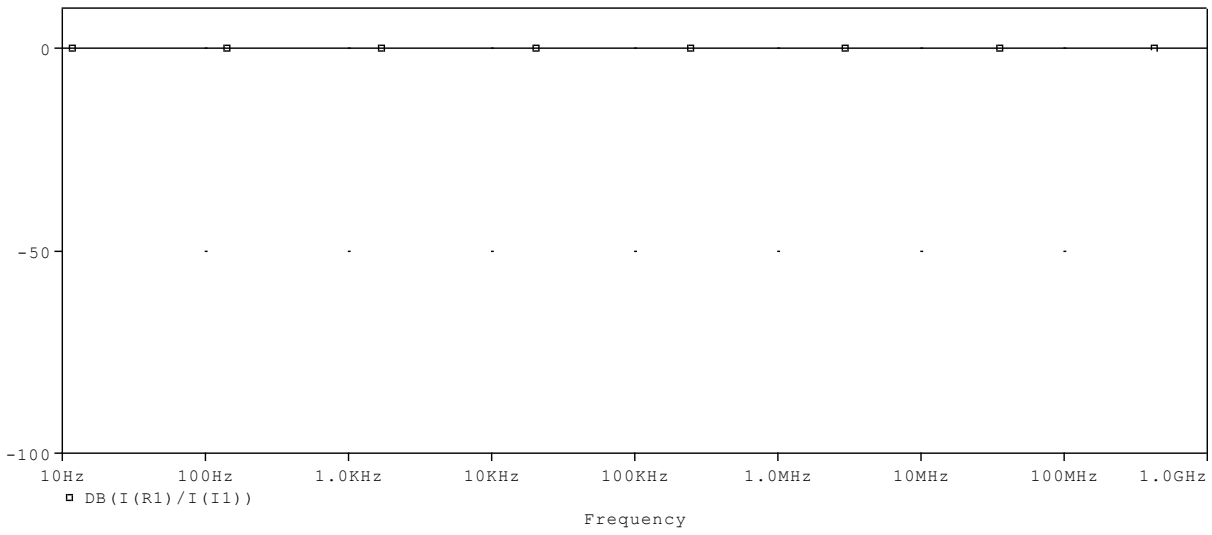


Fig 3.2.12: AC magnitude response of all pass filter

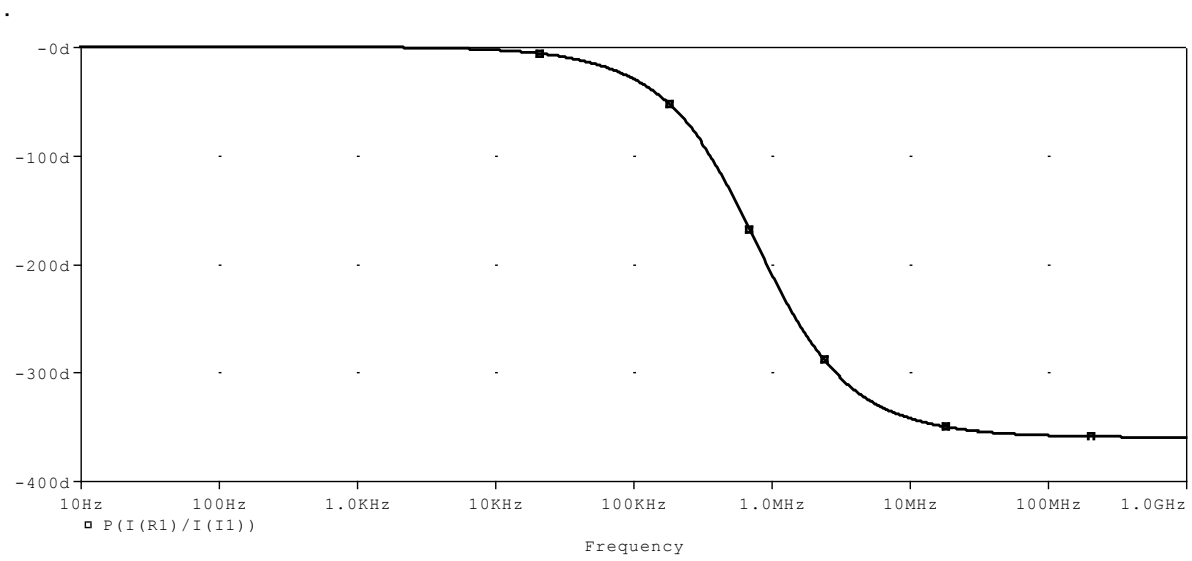


Fig 3.2.13: Phase response of all pass filter

3.3 Square wave generator

Square wave generator is a device which convert sinusoidal wave to a square wave. When current of a sinusoidal wave goes above or below from $\pm$0.5uA, output of square wave generator goes to $\pm$354uA. Workablity of the generator is shown in Fig 3.3.1.

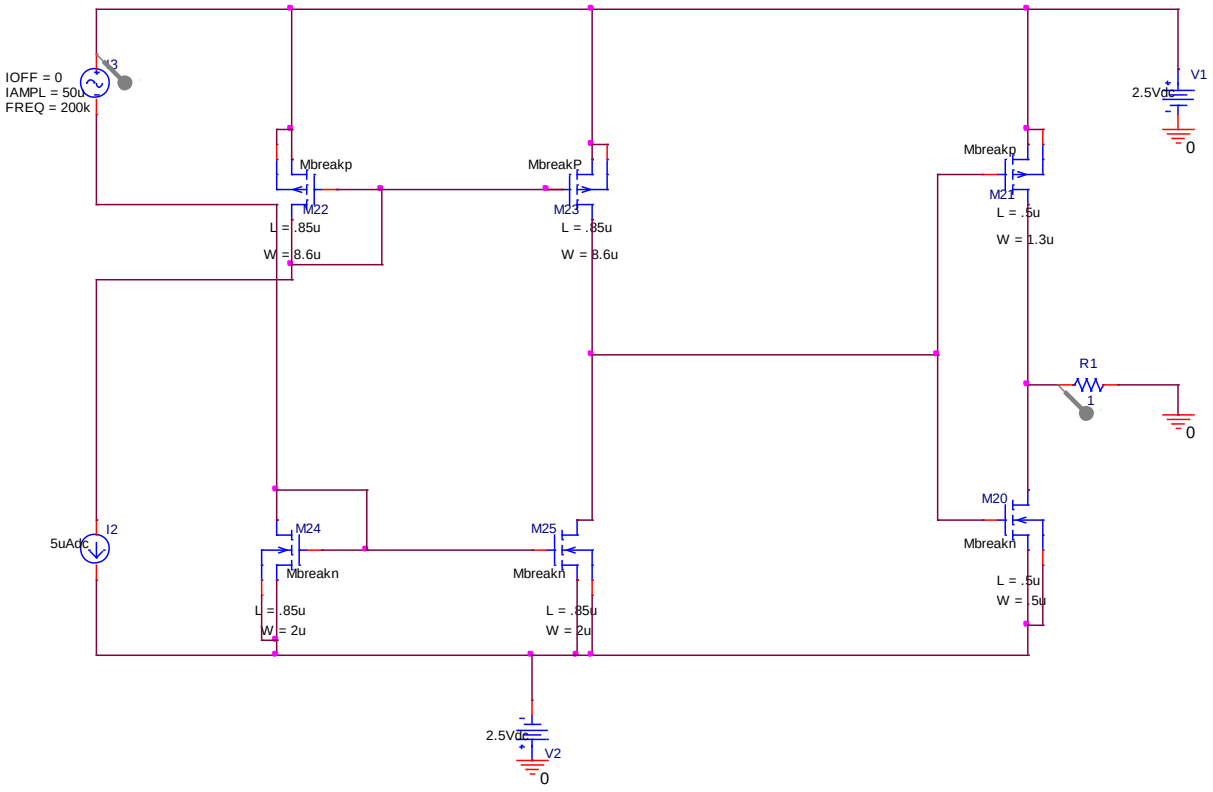


Fig 3.3.1: Schematic of square wave generator[3.7].

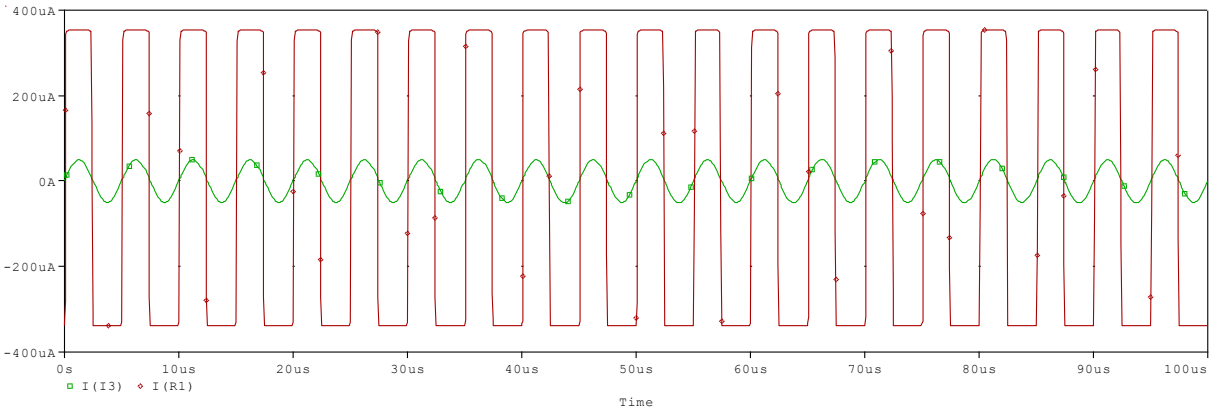


Fig 3.3.2: Waveform of square wave generator

Chapter 4

CONCLUSION AND FUTURE SCOPE

This chapter presents whatevere work carried out in this dissertation. This dissertation presents study of various current mirror, their comparision and then application based on CMOS based cascode current mirror. In first chapter, evavlution of current signal processing and how current signal processing is better than voltage signal processing is presented which leads to motivation for the work done in this thesis. Objective of the thesis is also discussed in this chapter.

Literature review on the various current mirror is shown in chapter 2. Current mirror can be designed using both BJT and MOSFET which is obsereved in this review chapter. Then comparison of various current mirror is done on the basis of their performance pararmeter. Further it includes CMOS based cascode current mirror study. DC and AC characterisation of this current mirror is also done in this chapter through SPICE simulation using 350nm technology. Various performance parameters have been observed through simulation.

In chapter 3 some basic analog building blocks such as current inverter, current adder and subtractor are implemented using CMOS based cascode current mirror. Further implementation of first order LPF, second order LPF is done. This is followed by impementation of KHN and LT filter. Further application of current mirror includes conversion of sinusoidal to square wave. Workability of all these applications is verified through SPICE simulation.

Last chapter of this dissertation contains the summary of the thesis in chronological order.

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