SIMULATION AND ANALYSIS OF VARIOUS APPLICATIONS OF STATIC POWER DISSIAPTION TECHNIQUE

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by

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CERTIFICATE

This is to certify that the dissertation titled "**SIMULATION AND ANALYSIS OF STATIC POWER DISSIAPTION TECHNIQUE**" is a bona-fide record of work done by **KISHAN GOPAL, Roll No. 2K15/VLS/10** at **Delhi Technological University** for partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI and Embedded systems Engineering. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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DECLARATION

I hereby declare that the project entitled **"SIMULATION AND ANALYSIS OF VARIOUS APPLICATIONS OF STATIC PWER DISSIAPTION TECHNIQUES"** being submitted by me is a authentic work carried out under the supervision of **Dr. N.S Raghava (Professor) ,** Electronics and Communication Engineering Department, Delhi Technological University, Delhi.

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Generally, individuals set aims, but more often than not, their conquest are by the efforts of not just one but many determined people. This complete project could be accomplished because of contribution of a number of people. I take it as a privilege to appreciate and acknowledge the efforts of all those who have, directly or indirectly, helped me achieving my aim.

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ABSTRACT

The speed of operation has increased to a greater extent by properly scaling of the CMOS technology, still the issue of leakage currents are leftover as a contrary issue. The issue has taken a severe shift as the scaling enhances into ultra-deep-submicron (UDSM) region. And as the process technology turns into the better state with increment in the device density, it also contributed a lot in increasing the leakage power. As the value of supply voltage decreases, gate oxide thickness reduces which further decrease the value of threshold voltage which contributed in preserving the performance of the circuit. But the main drawback of decreasing the threshold voltage is that the value of leakage power dissipation increases significantly. These unwanted leakage current must be lowered down for proper working of the circuit. So, the proper designing of those nano- CMOS Circuits which provides leakage current free performance advantage and this is the most difficult designing strategy in present era. In this work, we address the issue of leakage power and presents a circuit technique to mitigate the leakage power which in turns reduces the static power dissipation to a greater extent. In the proposed circuits, the static power dissipation is reduced to a greatest extent In popular circuits like SRAM, flip flops by using various techniques like forced stack technique, sleepy stack technique, sleep transistor technique and LECTOR technique. The circuits are implemented using the SymicaDE and LTspice software at PTM models 45nm, and 90nm and the result is compared with the existing techniques, which finally concluded that by using these techniques the leakage power can be decreased to a noteworthy degree.

CHAPTER 1
INTRODUCTION

In the past, Power dissipation was not a major concern in the VLSI chips design because the device density and operating frequency were quite low that it was not a restraining component in the chips.

As per the Moore's law, the device density is continuously increasing, as it states that the growth rate of Integrated circuits is 2 times in every 18 months. Therefore, with the advancement in the scale of integration, large number of faster and smaller transistors, are being integrated into a chip. It is for this reason, the operating frequency and the processing capacity per chip keeps on increasing and further results in increased power dissipation. So, in the present era, reducing power consumption has become very important as more and more transistors are integrated onto a single chip with a continuous increment in the clock frequency along with the continuous demand of better performance and portable applications in the present era.

1.1 MOTIVATION:

As the circuit design in VLSI requires the proper balance between the area, performance and power according to the desired application. For devices which are handy and are small in size, needs lesser power dissipation as the battery power is limited. In CMOS design the different power dissipations are as follows:

1. Dynamic power dissipation.
2. Static power dissipation.

Dynamic power dissipation is the power required to charge and discharges the load capacitance of the CMOS circuits while static power dissipation is generated due to different leakage in CMOS circuit that is regardless of transition. Dynamic power consumption was the dominant concern at and above 180nm technology node which contributed to approximately 90% of the total circuit power. Therefore, the previous techniques to reduce the power dissipation were based on voltage and frequency scaling.

As we are moving towards the deep sub-micron regime e.g. to 90nm and 65nm, static power grow into a matter of tremendous concern for current and future technologies. According to the International Technology Roadmap for Semiconductors (ITRS), Kim *et al.* report that at the technology node 65nm, the value of static power dissipation is far more than that of dynamic power dissipation.

1.2 RESEARCH OBJECTIVE:

The basic idea to begin this thesis is to lessen the static power dissipation in the circuit without affecting the other performance parameters. As in the technology lesser than 65nm, the static power dissipation dominates, so the need for minimizing the power is the important concern nowadays.

Dynamic power can be easily eliminated up to considerable extent by various approaches like the technique which lessen the power consumption of idle sections of synchronous circuits known as the clock gating technique. However, while dynamic power loss has been prevailing offender in the previous era, static power loss has developed into a ample contributor to power consumption in nano-scale technologies [4,8] because of the leakage currents present in the circuit.

There are Variety of approaches drafted to lower down the value of leakage currents in the circuit[1,2,8]. The best techniques comprising power gating circuits — basically cuts off the pull-up network (PUN) and pull-down network (PDN) draw up system (PUN) from either one or both power rails all along the "sleep" period. While, all along the active period, the circuit is again connected to the power rails and this process is called “active” or power up.

The leakage power reduction technique like the forced stack technique, sleepy stack technique, sleep transistor logic and the LECTOR technique is basically used in this thesis work to find the best applications in SRAM and flip flops circuits.

1.3 ORGANISTION OF THESIS

The whole thesis is categorized into 6 main chapters. Here in the chapter 1, i.e. the INTRODUCTION chapter gives the brief introduction about the main problem in implementing the circuits, along the types of power dissipations and how thesis is helpful in solving the presently prevailed problem in the circuits of VLSI design.

Chapter 2 examines the leakage mechanism of CMOS transistor. A thorough understanding of such mechanism is crucial to develop techniques to mitigate static power consumption in various VLSI design circuits.

Chapter 3 briefly explores the common techniques that are used to reduce static power consumption at different stages of design process.

Chapter 4 presents the proposed circuits which in turns reduces the leakage power with its best applications in the SRAM and the flip flops circuits along with the comparison of the proposed circuits with other existing circuits in terms of basic performance parameters like power, delay etc.

Chapter 5 finally concluded the thesis work along with the future scope in which the proposed work can be used and is useful for the use in future aspects.

CHAPTER 2
COMPONENTS OF LEAKAGE CURRENTS

The exponential increment of the number of transistors on the chips, increases the circuit density which in turn reduces the threshold Voltage (Vth) and gate oxide thickness (Tox) which further results in considerable amount of static power dissipation in the circuit. The main cause of static power dissipation is the leakage current which flows over the circuit when the total current through the circuit is 0A. The major concern that needs to be addressed earlier is the increment in the leakage power, especially for circuits that have low duty cycles, and which depend on batteries for extended span of time. There are numerous situations which are responsible for the production of leakage current in the circuit, and recognizing such conditions is significant in understanding how to lessen them. This part outlines the principle short-channel CMOS devices for the transistor leakage system. Despite a large portion of argument in this section is accomplished for a n-type MOS transistor, a closely resembling examination can be delivered for a p-type MOS transistor also[1,3].

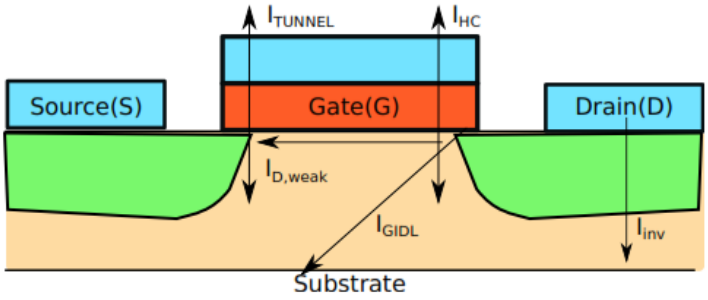


Figure 2.1: Leakage current representation in the Traversal view of a MOSFET device[1].

The total leakage current not only depend on one single component, but it also depends upon addition of different parasitic current. These parasitic currents can be divided into two fundamental classifications: i) drain leakage current that moves from the drain to the source of the circuit(I_{OFF}); and ii) leakage current that drizzles through the gates of the transistor (I_{GATE}).

I_{OFF} and I_{GATE} are the compound of currents created by various physical impacts under distinct conditions. Figure 2.1 demonstrates the leakage current in the transverse view of the n- type

MOSFET device. The remaining portion of this chapter shortly depicts the circumstances that permits static power utilization in computerized digital circuits.

Table 2.1:Types of Leakage currents in a MOSFET device[1]

I_{OFF}	Sub-threshold drain current ($I_{D;WEAK}$) Reverse biased current (I_{INV}) Gate Induced drain leakage (I_{GIDL})
I_{GATE}	Gate tunnelling (I_{TUNNEL}) Hot Carrier Injection (I_{HC})

2.1 Sub-threshold leakage current (I_{OFF}):

The subthreshold leakage current of a transistor is abbreviated as IOFF. The value of drain current when |Vg|- |Vs|= 0 and Vd ≥ 0 is known as IOFF. The value of IOFF in the circuit confides on the circuit topology along with the circuit parameters like supply voltage, threshold voltage, doping concentration of the MOSFET device, and T_{ox}.. T_{ox} stands for gate oxide thickness. The subthreshold leakage current comprises of a lot of sub-components as illustrated in Fig. 2.2, and the expression of subthreshold leakage current is shown in Eq. 2.1[3,5].

$$I_{OFF} = I_{INV} + I_{D,WEAK} + I_{GIDL} \quad \text{....(2.1)}$$

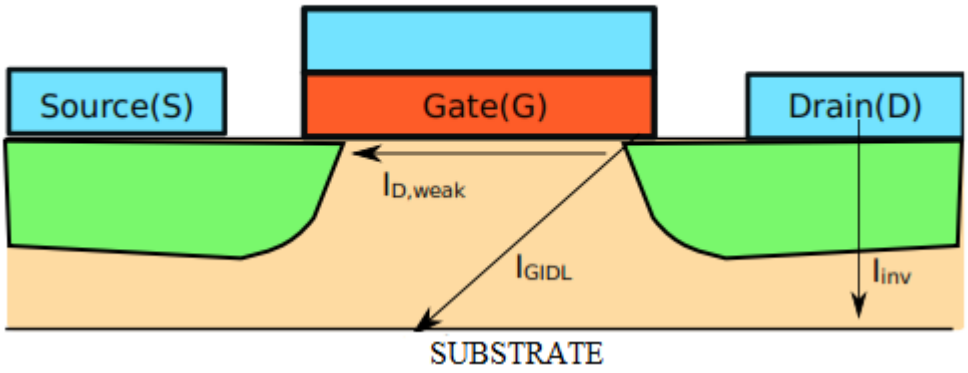


Figure 2.2: Subthreshold leakage Currents representation in the traversal view of a transistor

2.1.1 Reverse biased diode current (I_{INV})

The current that moves in the device via the reverse biased diode amid the drain (n-region) and the p-region of the transistor is known as IINV, and it is highly vulnerable on the junction in between the Source and the body terminal or Drain and the body terminal and exponentially rely on the value of temperature also [7].

The leakage current representation for a reversed biased diode is depicted in Eq. 2.2, where V_T stands for thermal Voltage.I_s stands for reverse saturation current and it is an intrinsic parameter for the device. V_d is the voltage difference in between the drain and the body of the transistor. As a consequence of exponential reliance on the voltage, just small disorder will approximately equate the value of reverse saturation current and the saturation current. Once in a while, electric data sheets just give the information of saturation current density Jinv, in that case the value of reverse biased diode current can be calculated by multiplying the value of current density and diffusion area (Ad) as depicted by equation 2.3.

$$I_{INV} = I_s \left(e^{(V_d/V_T)} - 1\right) \quad \text{.... (2.2)}$$

$$I_{INV} = A_d \times Jinv \quad \text{.... (2.3)}$$

2.1.2 Sub-threshold drain current ($I_{D,WEAK}$)

The condition for the transistor to be in weak inversion region is Vg < Vth, |Vd| ≥ 0:1 and Vs = Vb= 0. A transistor is said to be in weak inversion when it has a constant voltage beyond the channel and the value of electric field in the longitudinal direction across the channel is also 0. Thus, there is no drift current in the circuit. Rather, the $I_{D,WEAK}$ current is created by the dispersion of majority carriers across the channel [36]. $I_{D,WEAK}$ can be demonstrated in Eq. 2.4, where V_T stands for thermal voltage and I0 is the initial DC offset in the I_D. It is vital to take note of the exponential reliance of $I_{D,WEAK}$ on Vgs and additionally a direct offset in view of V_{DS}.[6,7]

$$I_{d,weak} = \frac{W}{L} \times I_0 \times e^{(V_{gs}-V_{th})(mV_T^{-1})} \times (1 - e^{-V_{DS}(mV_T^{-1})}) \quad \text{....(2.4)}$$

2.1.3 Gate-induced drain current (I_{GIDL})

When high gate to drain voltage is enforced, then it results in electron tunnelling effect adjacent to the interface of gate oxide and drain and due to this reason Gate-induced drain leakage, IGIDL is induced in the circuit.

2.2 Gate Leakage (I_{GATE})

The gate leakage manifests itself as current that dribbles across the gate to and from the channel, substrate, and diffusion terminals. This current disallows the treatment of the gate of a device as an ideally insulated electrode. The gate leakage is compounded by two main elements [4].

i) Gate tunnelling (I_{TUNNEL})

ii) Hot Carrier injection (I_{HC})

2.2.1 Gate tunnelling (I_{TUNNEL}):

This current is created due to carriers tunnelling through the gate of the transistor. There are two ways carriers can tunnel through the gate: i) into the conduction band of the dielectric (commonly Silica: SiO_2), this is known as Fowler-Nordheim tunnelling and it manifests itself as an electron emission caused by the intense high electric field; and ii) directly to/from the gate through the for-bidden band gap of the dielectric[4,7].

2.2.2 Hot Carrier injection (I_{HC}):

This current is known as hot carrier leakage, this current is generated whenever a carrier gains sufficient kinetic energy to conquer the effect of gate potential barrier. This effect is more likely for the electron since the voltage barrier and effective mass of an electron is less than the one for holes.

2.3 The impact of CMOS device scaling in leakage currents:

For the past 40 years, because of the Moore's law, circuit designers have the luxury of doubling the number of transistors every two years, which further results in the greater advancement in the area of faster speed of operation, larger device density, with a better response time devices. While this trend is slowing down, it will continue (at least) for the near future. The main problem rises as transistor miniaturization reaches atomic levels: photolithography, manufacturing costs, increased power density and the I_{ON} : $I_{LEAKAGE}$ current ratio are just some of the challenges that scientists face. While the trend of some leakage currents are to shrink (I_{INV}), some others significantly increased (I_{TUNNEL}, I_{DWEAK}), this section explores the trends of device miniaturization and their impact on the leakage currents described above.

2.3.1 Gate Oxide Thickness (T_{ox}) scaling:

Gate oxide thickness in SiO_2 CMOS devices is one of the most important parameters on a FET device. Traditionally the T_{ox} has scaled such that $L_{eff} = 45\ T_{ox}$. This relationship usually leads to good V_G-I_d transfer behaviour [26]. As the channel scales under the 100m this scale is not feasible, since the T_{ox} reaches its minimum limit. Previous work has set the barrier limit from 12Å to 16Å, which is the limit where dynamic gate leakage power equals $1Acm^2$ for large MOS capacitors [3].

There are two leakage currents directly affected by reducing T_{ox}: GIDL (Sec. 2.1) and Gate Direct Tunnelling. GIDL currents increase, since the voltage required to generate electron tunnelling decreases as gate oxide thickness shrinks. Although GIDL could impose a limit on scaling the T_{ox}, its effect is expected to be less relevant for digital applications as the voltage reduces below the energy band gap of the silicon. Direct tunnelling and hot carrier injection is expected to increase significantly as the thin oxide layers become smaller than 20Å. Despite the industry hesitation to discontinue Silica as the insulator of gate terminal, the use of other dielectrics will allow more aggressive reduction of the oxide thickness in the near future.

2.3.2 Channel Miniaturization:

Short-channel effects are expected to worsen when channel length is reduced. Drain Induced Barrier Lowering (DIBL) is one of such effects, in which the depletion region of the source/drain extends into the channel of a MOSFET device, effectively reducing the channel length. This reduction on the depletion region lowers the potential barrier for electrons, which results in an observable lowering of V_{th}, and hence in an increase on the I_{DWEAK} current as seen in Eq 2.4. On the other hand, channel miniaturization reduces the junction area between the substrate and the Source/Drain, effectively reducing the (I_{INV}) Channel miniaturization is also closely related to scaling of the T_{ox}, since both channel and gates are engineered for optimum performance and low power consumption.

2.3.3 V_{dd} and V_{th} Scaling:

Two of the most important transistor characteristics are the nominal V_{dd} and V_{th}. Process engineers typically scale the supply voltage (V_{dd}) to control dynamic power consumption and power density. This reduction in V_{dd} forces a reduction in V_{th} in order to get performance gains. This reduction in V_{th} typically causes a relatively large increase in I_{OFF}, while the reduction of V_{dd} reduces the leakage currents substantially. The effects of GIDL in technologies that have a nominal V_{dd} 1:1 (energy band gap of Silicon) decay drastically, becoming less of a concern in digital circuits [3].

2.3.4 Doping Concentration:

The electric field at a p-n junction strongly depends on the junction doping [30]. When device engineers scale-down transistors, the doping concentration is generally increased, incrementing the overall I_{inv} and I_{TUNNEL}. However, device scientist's engineers are trying to develop smart doping profiles for the channel and the transistor terminals to maximize active current drive while minimizing idle-current.

2.3.5 Source-Drain Punch-through:

In an overly simplistic way, punch-through happens when the depletion regions from the source and the drain join in the absence of a depletion region induced by gate [36]. Punch-trough happens when voltages between the source and the body are above the nominal range of V_{dd}, since this is not the common case for digital circuits, this is usually not a concern for ASIC designers.

CHAPTER 3
STATIC POWER REDUCTION TECHNIQUES

The basic techniques for the Static power reduction can be categorized into three principle classifications relying upon the granularity at which it can be applied:

1. Device Engineering. It included the methods that are realized at the underlying transistor level in the circuit designing.

2. Circuit Engineering. It indicates the techniques that are directly incorporated to the gates, like NAND, NOR or on the other part of the circuit designing.

3. System Engineering. It alludes to methods that can are implemented to big macro blocks which are the subset of microchip.

This chapter briefly describes the most common techniques on each of the categories and discusses the advantages and disadvantages of each one of them.

3.1 Device Engineering

Specialists have created designing procedures to lessen the leakage power in CMOS circuits. But disastrously, these procedures normally have trade-offs in other performance parameters and area. With a specific end goal to control static power, circuit designers can adjust certain dimensions of the circuit (e.g., Leff ,Tox, substrate depth, Source and Drain cover), the theoretical estimations of Vdd and Vth, the type of materials utilized , the type of FET devices depending upon the depleted devices, bulk devices or the multiple gate devices along with the doping profile [8].

The benefits of tuning transistors are tremendous since leakage current diminished is generally noteworthy and devices are rationalist to circuit standards and logic families. The fundamental inconvenience of implementing device engineering is that periodically the circuit designer has no authority over the choice of devices and no doubt does not have the mastery, time, and proper budget to alter the basic transistors that adjust circuits. However, it is not uncommon for a design team to be presented with a portfolio of technologies and manufacturing processes, it is their responsibility to choose the one that fits the needs of the application. If the main

concern is leakage power consumption, an educated decision when choosing a technology can be done by analysing parameters like the ones discussed in Chapter 2.

3.2 Circuit Engineering

There exists a collection of techniques that assist the circuit designer to reduce leakage power at the gate level. Probably the most known technique is forced transistor stacking, which exploits the dependence of the sub-threshold current Id;weak on Vth and Vgs as described by Eq. 2.4. Transistor stacking also attenuates the effect of DIBL. To understand the effect of transistor stacking consider the circuit in Fig.3.2[B] and the value of input c set to 0V, the gate source voltage of transistor M_6, V_{gs6}= 0V ,V_{m2}= 0V, effectively decreasing the $I_{d;weak}$ current. DIBL effect is also attenuated because the drain source voltage of transistor M_6.There are two flavours of transistor stacking, the first flavour comprises on exploiting the common transistor stacks like the ones found in NAND and NOR gates by setting proper input vectors to build the quantity of off transistors in a series of transistors. The second flavor is to strongly add additional transistors in series to the gate to diminish the leakage power dissipation. The disadvantage of forced stack technique is that the gate delay is increased to a greater extent in the active region. Figure 3.2[A] demonstrates a case of normal transistor stacking on a NAND gate. The fundamental issue of low-level circuit design engineering is that it normally needs a great deal of manual designing of the gates and circuit designers for the most part need to work truly difficult to accomplish a critical reduction on the leakage power dissipation.

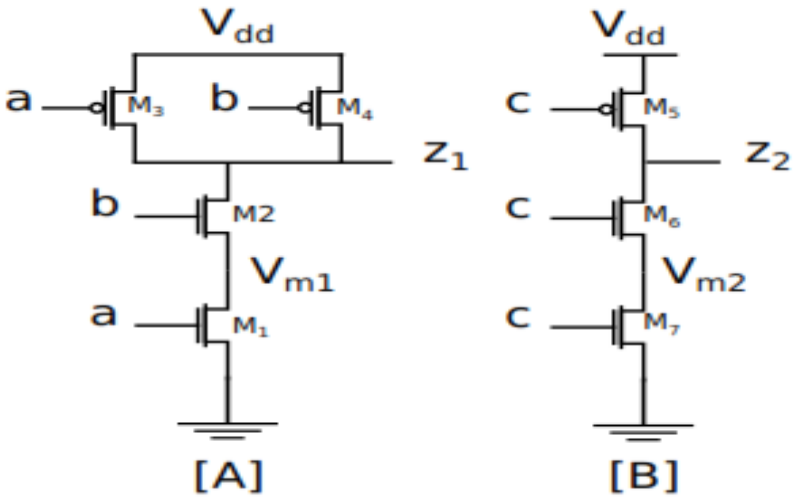


Figure 3.1: [A]Natural stacks found in a NAND gate. [B]Forced stacking on the pull-down network of an inverter.

The leakage power reduction techniques at circuit level can be broadly classified into two groups:

1. State destructive technique
2. State saving technique

3.2.1 State Destructive Technique

State Destructive techniques also called gated- V_{dd} and gated- GND techniques , cuts off either the pull-up or pull-down or both transistor networks from supply voltage or ground using sleep transistors. Sleep transistor technique is the example of State destructive technique[15].

3.2.1.1 Sleep Transistor Technique

Sleep transistor technique use the sleep transistor to isolate the logic network form power supply and ground during the sleep mode and hence reduce the leakage power reduction. This sleep transistor technique frequently uses high-Vth sleep transistors (the transistors controlled by S (Sleep Signal) and S'(Sleep Bar Signal)) to achieve larger leakage power reduction. During sleep mode S =1and S'= 0 are asserted and both of the transistor are turned off [9,10]. And the Output of the circuit is floating and hence this Technique is State-Destructive technique. During active mode of operation S =0 and S'= 1and both sleep transistor is turned on and the output of the circuit is evaluated according to the input. Fig 3.2 shows the sleep transistor technique applied in CMOS inverter.

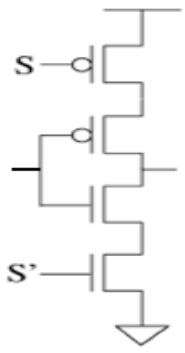


Fig 3.2 Sleep Transistor Technique[10]

3.2.2. State Saving Technique

In State Saving technique, number of transistors between V_{dd} and GND path are increased (in pull-down as well as in pull-up network) in such a way that logic operation performed by the circuit will not change. Due to this, leakage current flowing in the circuit is reduced which in turn further reduces the leakage power in the circuit. Forced stack and Sleepy stack techniques are the example of state saving techniques.

3.2.2.1 Forced Stack Technique:

It is one of the simple techniques to reduce leakage power. Forced stack technique shown in Fig 3.3. uses the transistor stacking for the proper decrement of leakage power. It is based on the stack effect; stack effect reduces the sub-threshold leakage current by turning off two or more stack transistors. It will increase the effective channel length of the transistor, which indirectly increase the threshold voltage of the transistor and reduce the leakage power dissipation in the circuit[10,36].

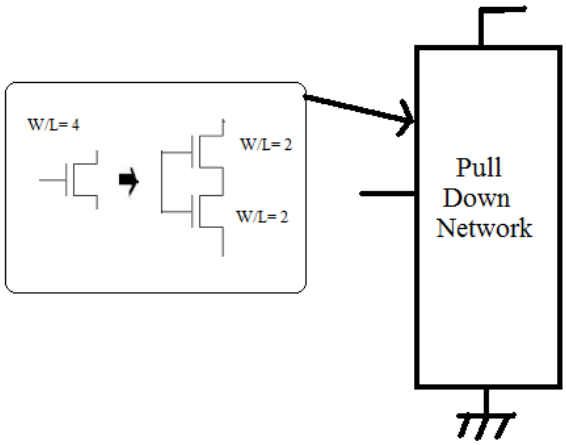


Fig 3.3. Forced Stack Technique[10]

In this technique, single transistor is resolved into two transistors of size half of the original transistor. When these two transistors are turned on or off simultaneously it reduces the sub-threshold leakage current but on the other hand it also increases the delay because the number of transistor between output and GND increases [20,24] Advantage of the forced stack technique are:-

1). Easy application in the digital logic circuit.

2). Output state is saved at every instance of time.

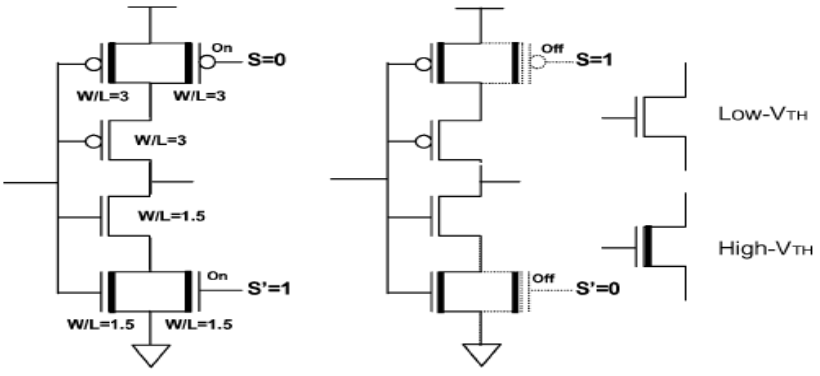
Disadvantages of this technique are:-

1). It increases the area-overhead in the circuit.

2). It decreases the speed of operation and further makes the circuit slower.

3.2.2.2 Sleepy Stack Technique

Sleepy Stack technique is the combination of both forced stack and sleep transistor technique in order to utilize the advantages of both technique without adding large delay penalties [11,15,28].It is a state saving technique and can be used to achieve the ultra-power saving in digital circuits. In sleepy stack technique, a transistor is resolved into two transistor of width half of the original transistor and a sleep transistor is placed in parallel with the stack transistor so that the delay of the circuit is minimize and the state of the circuit is also save. The mode of operation of sleepy stack technique is similar to the operation of sleep transistor technique. During the active mode of operation S =0 and S'= 1 and both sleep transistor is turned on and the output of the circuit is evaluated according to the input [fig3(a)]. Sleepy stack technique give the faster switching operation than the forced stack technique in the active mode by reducing the resistance of the discharge path from output to ground. During the sleep mode of operation signals S =1and S'= 0[fig3(b)] such that both the sleep transistor is off but the sleepy stack structure can maintain the exact logic state.



(a (b)

Fig 3.4. Sleepy Stack Technique (a) Active Mode of operation

(b) Sleep Mode of operation[11]

Advantages of the Sleepy Stack technique are as follows: -

1) Ultra power saving techniques is achieved when compared to forced stack technique and sleep transistor technique.
2) No need to regenerate the state at any instance of time because it is a state saving technique.
3) It can use the multi-threshold transistor in order to manage the power and delay trade-off in the circuit where it is employed.

Although Sleepy stack technique is better when compared to Forced stack and Sleep transistor in the terms of power saving and delay but it has some disadvantages which are as follows: -

1) It Increases the Area-overhead in the circuit.
2) Manufacturing cost of the chip increases.

3.2.2.3 LECTOR Technique

The basic idea behind lector technique is the lowering of leakage power by properly stacking of transistor in the midway from supply voltage to ground, because a state with greater than one transistor off in the path from supply voltage to ground is far less leaky than a state with only one transistor off in any supply to ground path. In this technique two leakage control transistors (PMOS between pull-up network and output; NMOS between output and pull-down network). The gate terminal of PMOS(MP) transistor is controlled by source of NMOS (MN) and the gate terminal of NMOS (MN) is controlled by source of PMOS(MP)[12,16,26]. One of the leakage control transistor (LCT) always work near cut-off region which reduces the leakage current.

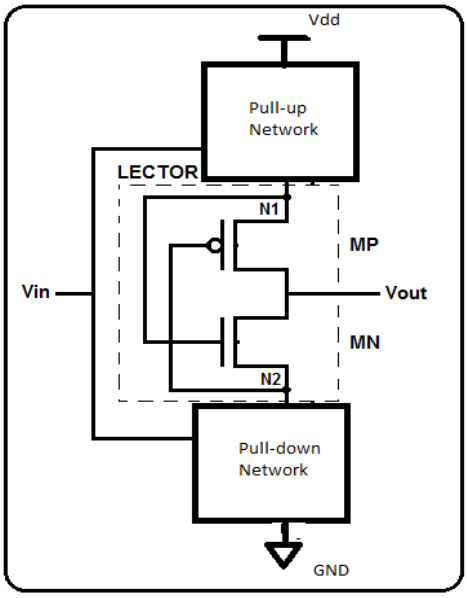


Fig 3.5. Lector technique[12].

3.3 System Engineering

At last, there exist a few strategies that can be incorporated system wide to diminish leakage power and typically render a great deal of static power saving. Some of these implementations are design particular, for instance the decision of a SRAM cell or the particular execution of a data path unit.

Nonetheless, there are two general techniques that can be implemented to (nearly) any circuit: Clock Gating and Power Gating. Asynchronous circuits are data driven in nature, implementing an equivalent fine grain clock gating design. Hence, power gating is the unrivalled systematic technique to reduce static power in an asynchronous pipeline.

CHAPTER 4

APPLICATION OF STATIC POWER DISSIPATION TECHNIQUES

Static power dissipation techniques are not applicable on each and every CMOS circuit because each static power dissipation technique has its own pros and cons. So, the main challenge is to find a circuit in which these power dissipation techniques can be applied, so that the circuit performance is improved to a greater extent in terms of power.

In this chapter, the application of these techniques in flip flops and SRAM is shown. As there are various advantages of using those devices which have a brighter side of reducing the static power dissipation without affecting other parameters to a greater extent. So, by using these techniques the energy efficient flip flops and SRAM circuits are proposed for the application in various VLSI design circuits like in memory units, delay units, registers etc.

4.1 Pulse Trigger D Flip-Flops

Depending on the operation and structures, D-flip-flop are categorized into various classes which are as follows: -

1. Conditional Discharge flip-flop (CDFF)
2. Clocked pair share flip-flop (CPSFF)
3. Low power clocked pass transistor flip-flop (LPCTFF) etc [17]

The power consumed by the flip-flops are categorised into two main components- the Clock Power and Data Power [28]. The first component i.e. the clock power, is the power which is dissipated when the flip-flop is clocked while the data of the flip-flop is unchanged. The second component i.e. the data power, is the additional power required to write the different data value into the flip-flop. In typical flip-flop the low power components are comparable. However, in most of the system, the data rate of the flip-flop is typically much lower than its clock rate. So, the power saving techniques in the flip-flop is mostly concentrated on reducing the clock power. But these power saving techniques add the delay penalties to the flip-flop, therefore every power saving techniques cannot be applied in all the circuit design.

4.1.1 Low power clocked pass transistor flip-flop (LPCTFF)

Clock power of the transistor can be saved by reducing the unwanted switching due to clock signal while the data is unchanged or by reducing the number of clock MOSFET. LPCTFF is the one of the low power structure of D-flip-flop in which clock power is saved by reducing the number of clock transistor. LPCTFF uses only one clocking transistor as compare to 7 clocking transistors in CDMFF and 4 clocking transistors in CPSFF. The structure of the LPCTFF is shown in Fig 4.1 The complete structure of this D-flip-flop use 5 transistors to generate output Q and an additional CMOS inverter for generating the complement of output Q i.e Qb.

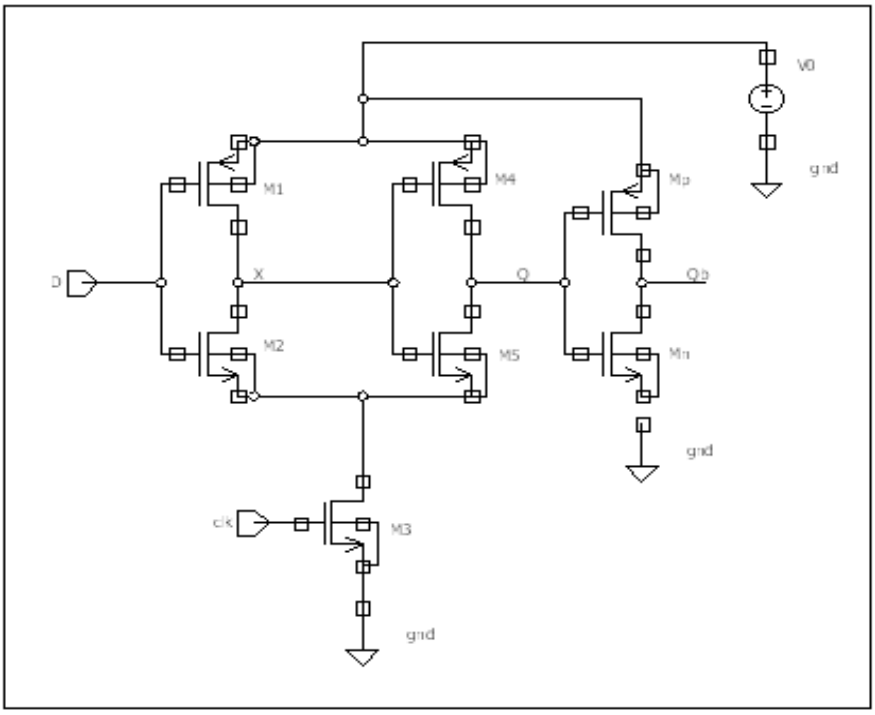


Fig 4.1 Low power clocked pass transistor flip-flop (LPCTFF)[17]

Operation of LPCTFF :-

When "CLk = 0" the transistor M3 is off and the output Q remains in memory state [5]. When the CLk make 0 to 1 transition, the transistor M3 is ON and the output of the circuit is determined by the value of D. If "D=1" then the transistor M2 is on and M1 is off as a result

the node X discharge through the ground hence transistor M4 is on and output Q reach at logic level 1. If "D=0" then the transistor M2 is off and M1 is on, so the node X is charged to Vdd by M1 and in turn it turns off the transistor M4 and transistor M5 is ON and the output Q discharges through ground.

4.1.2 Forced Stack Low power clocked pass transistor flip-flop (FS-LPCTFF)

LPCTFF is one of the most power efficient structure of D-flip-flop but its performance can be further improved by applying the static power reduction technique such as forced stack, sleep transistor and sleepy stack at the cost of little increase of area overhead. The LPCTFF structure with forced stack technique is shown in the Fig 4.2. Operation of this flip-flop is similar to that of LPCTFF except there are two CLK transistor connected in series which on and off simultaneously by the clock signal it reduces the sub-threshold current in the flip-flop and hence reduces the static power dissipation.

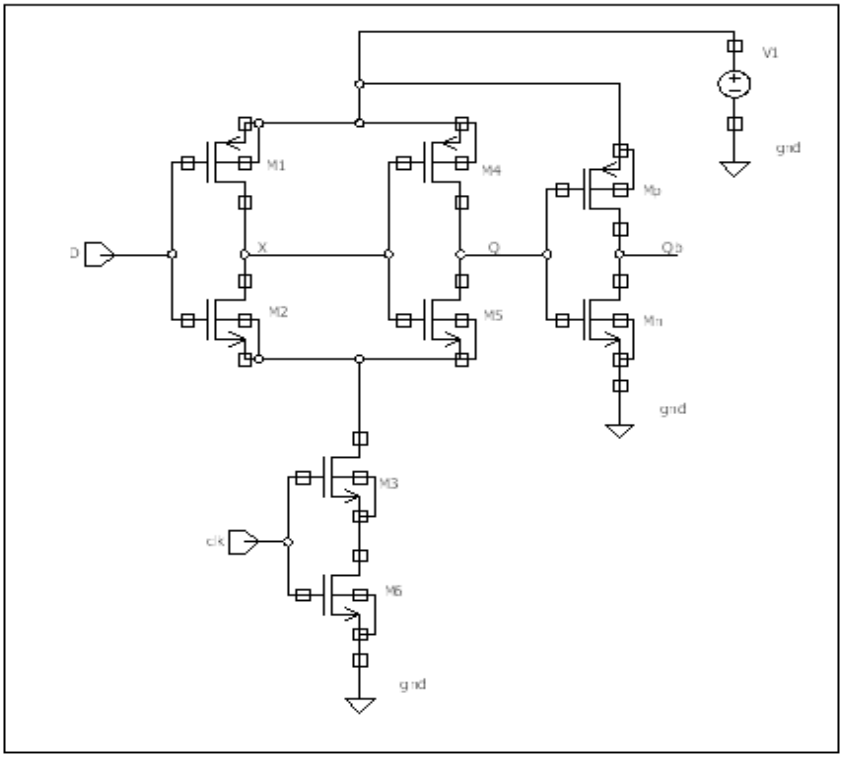


Fig 4.2. Forced Stack Low power clocked pass transistor flip-flop (FS-LPCTFF)[17]

4.1.3 Sleep Transistor Low power clocked pass transistor flip-flop (ST-LPCTFF)

The Structure of the Low power clocked pass transistor flip-flop (LPCTFF) with Sleep transistor technique is shown in Fig 4.3. In this structure, a transistor M6 is connected in series with the clock transistor M3, which is controlled by the Sbar (Sleep Bar).

This D-flip-flop operate in the two modes: -

1. Sleep mode

2. Active mode.

In sleep mode "Sbar = 0" and transistor M6 is off, which reduces the sub-threshold current flowing through the transistor M3 and hence reduces the static power dissipation in the flip-flop. As Sleep Transistor technique is State destructive technique Output Q loses its actual logic level during the sleep mode and hence require the output restoration time in the active mode. It increases the delay in the flip-flop although it save the large amount of power dissipation. During the Active mode of operation the signal "Sbar = 1" and transistor M6 is ON and output of the flip-flop is computed depending on the values of signals D and CLK.

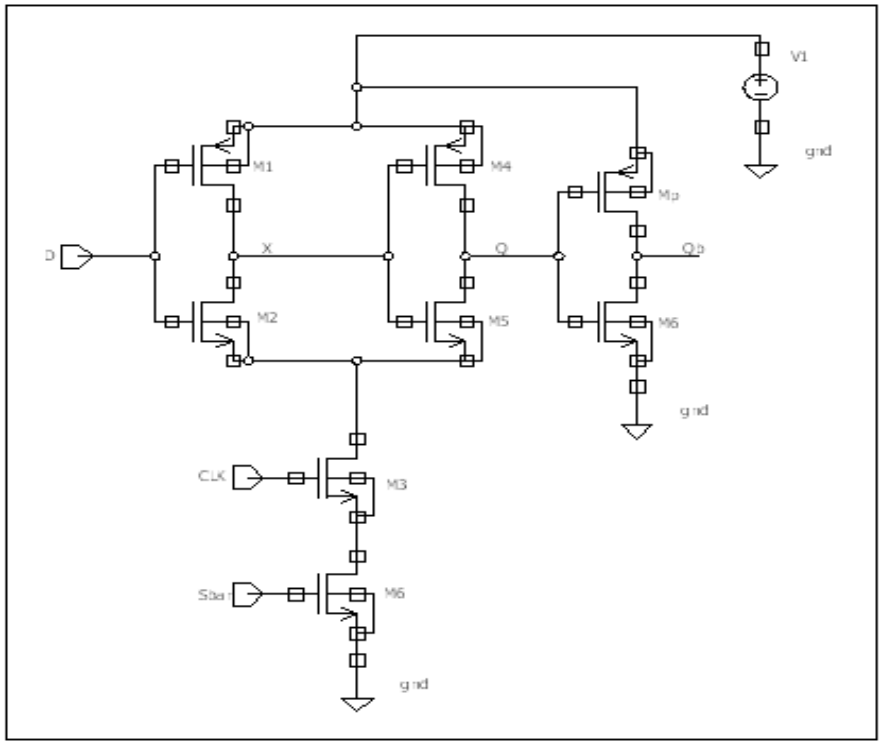


Fig 4.3 Sleep Transistor Low power clocked pass transistor flip-flop (ST-LPCTFF)

4.1.4 Sleepy Stack Low power clocked pass transistor flip-flop (SS-LPCTFF) :

The Structure of the Low power clocked pass transistor flip-flop (LPCTFF) with Sleepy Stack technique is shown in Fig4.4.In this Structure two transistor M6 and M7 are connected in such a way that these are in series with clock transistor M3 and Parallel to each other. Transistor M6 is a stack transistor which is controlled by the CLK signal and transistor M7 is the sleep transistor which is controlled by the Sbar (Sleep Bar) signal. Like Sleep transistor model it also has two mode of operation Sleep mode and Active mode. During sleep mode "Sbar = 0" and when clock is low transistors M3, M6 and M7 all are OFF So that sub-threshold current flowing in the flip-flop is reduced by the larger amount and static power is saved upto a greater extent. During the Active mode "Sbar = 1" therefore transistor M7 is kept ON and only M6 reduces the sub-threshold current when clock signal is low and thus saves power. If clock signal is high during sleep mode, both M6 and M7 are ON which reduces the overall resistance of the discharge and hence reduces the delay compared to Sleep Transistor LPCTFF and Forced Stack LPCTFF. Sleepy Stack LPCTFF Structure use 9 transistors which is more than the Simple LPCTFF, Forced Stack LPCTFF and Sleep transistor LPCTFF structure. Along with this it gives the Ultra Static power saving compared to simple structure and have less delay compared to forced stack and sleep transistor structure.

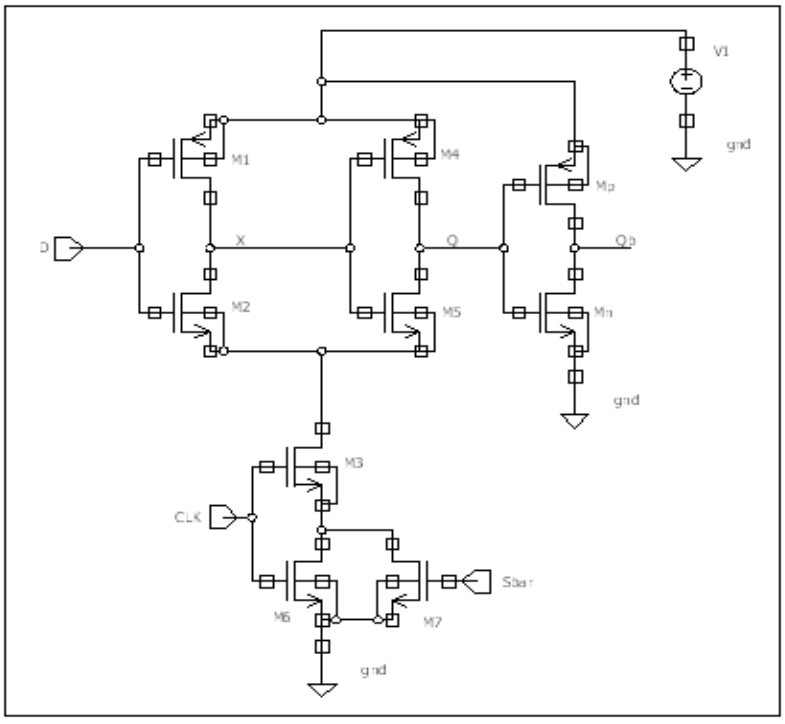


Fig 4.4 Sleepy Stack Low power clocked pass transistor flip-flop (SS-LPCTFF)

4.1.5 Low Power Pulse Triggered D Flip-Flop structure (LPTDFF)

The static power dissipation of LPCTFF can be reduced by replacing the simple CMOS inverter with a lector inverter. Lector inverter improves the performance of LPCFF by reducing the sub-threshold leakage current. The low power pulse triggered D flip-flop structure (LPTDFF) is shown in fig. 4.5.

Operation of LPTDFF is as follows:-

When clk ='1' and D='0' the transistor M1, M5,M4 and LCT MN1 and MP2 are ON and LCT MP1 and MN2 are ON near cut-off region, while the transistor M2 and M3 are off ,hence the output Q discharges to GND. When clk='1' and D='1' the transistor M2,M3,M5 and LCT MP1 and MN2 are ON and LCT MN1 and MP2 are ON near cut-off region, while the transistor M1 and M4 are off hence the output Q is charge to Vdd.

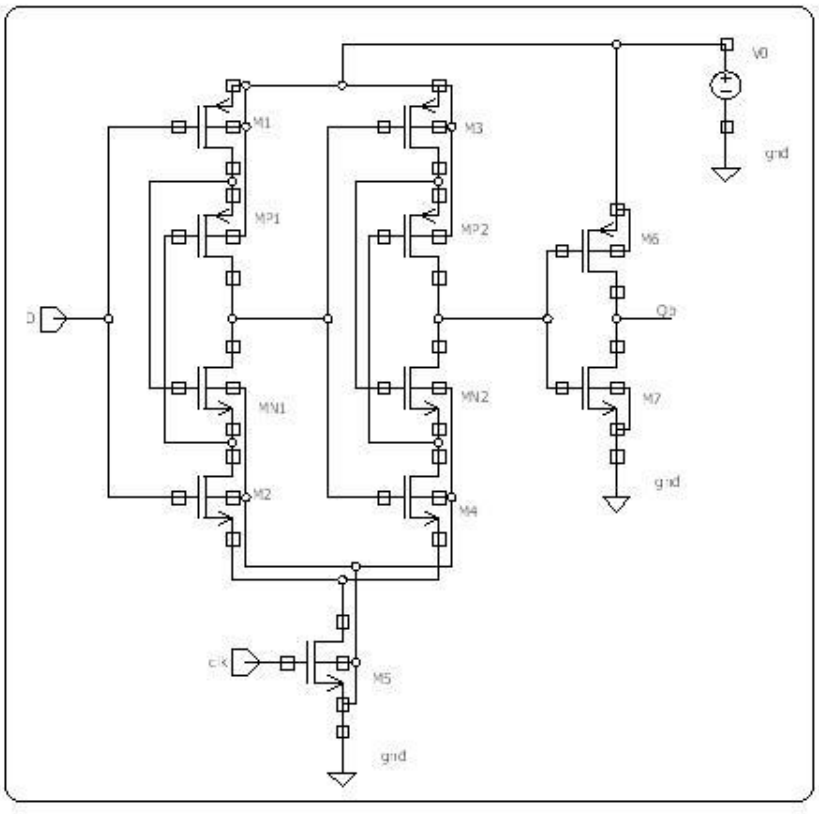


Fig 4.5 Low power pulse triggered D flip-flop structure (LPTDFF)

4.2 Static Random Access Memory (SRAM)

SRAM Utilizes a large portion of the chip area and have its applications in wide range of devices like in the cache memory of CPU. As the technology is continuously evolving and the number of transistors used is increasing day by day, the leakage power is continuously increasing which further adversely affect the operating frequency and the power consumption of the SRAMs circuit [33,34,40]. The leakage power is inversely proportional to the threshold voltage because the leakage current increases exponentially as the value of threshold voltage decreases. To overcome this problem, the threshold voltage can be increased to a greater extent but increasing the threshold voltage will slow down the operating speed of SRAMs. Therefore, the SRAM circuit which has lower leakage current with the lower power dissipation and faster devices are a good candidate in today's application.

SRAM makes up a large portion of a system-on-chip area, and commands the overall system power and performance. Additionally, there is a massive growth in the domain of smaller mobile devices, bioelectronics and emerging applications such as wireless body sensing network and implanted medical instrument which requires low power circuit design which further improves the performance of the system. It is for this reason there is a need for low power and low voltage SRAM design.

Basically, there are two important flavours of SRAM topology; Double- ended SRAM topology and Single- ended SRAM topology. In double- ended SRAM topology, THE BIT LINES (BL) along with the BL BAR is used, which increases the speed of the circuit but add power penalty in the circuit [32] .To overcome this demerit, the Single- ended SRAM Topology is used. In single- ended SRAM topology, only BL is used, which has the advantage that the overall power consumption is reduced up to one half of the active power because the switching and the leakage power is reduced and it is for this reason it is used in power- constrained applications. And also, the use of Single- ended SRAM topology reduces the total chip area of the device. However, the disadvantage is that the read write access time is increased and this is the only limitations of single- ended SRAM topology. But for the low power application, the Single- ended SRAM topology is the best candidate. To overcome the demerits of Single-ended SRAM topology different kinds of SRAM circuits were proposed in the literature of VLSI design, which overcome the demerits but they have their own individual disadvantages.

4.2.1 Conventional 6T SRAM

6T SRAM memory shown in Fig 4.6 will be an sort of semiconductor memory that employments bi-stable latching meandering will store every touch [34]. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered. The operation of this SRAM is divided into three modes, which are as follows: -

1. Stand By Mode
2. Read Mode
3. Write Mode

In standby mode word line is not asserted (wl=0), so pass transistors, which connect 6T cell from bit lines are turned off. Hence the two cross coupled inverters in the cell will continue to feedback each other as long as they are connected to the supply, and data will hold in the latch. In read mode word line is asserted (wl =1), Word line enables both the access transistor which will connect cell from the bit lines. Now values stored in nodes are transferred to the bit lines which are initially pre-charge to $V_{dd}/2$. Similarly, in write mode word line is asserted (wl =1) and the data from bit lines is transferred to latch.

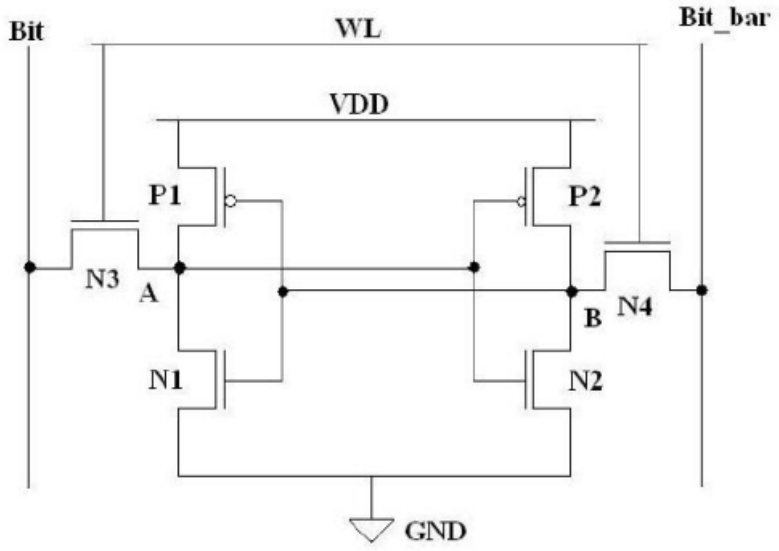


Fig 4.6 6T SRAM Cell [43]

4.2.2 Forced Stack SRAM:

The performance of the 6T SRAM cell can be improved by replacing the CMOS inverter in the latch by Forced stack inverter [41,44]. Forced Stack SRAM cell is shown in Fig 4.7. It reduces the static power dissipation of the existing cell by a greater extent but on the other hand it also increases the delay of the cell. The basic operation of the cell is remains same.

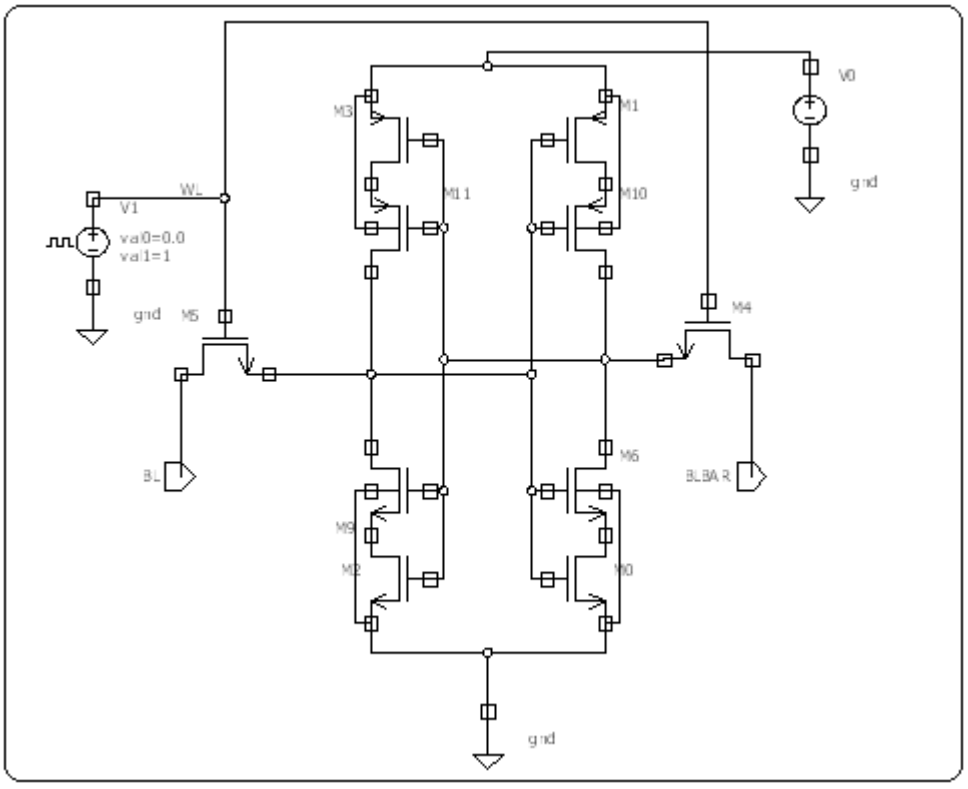


Fig 4.7 Forced Stack SRAM Cell [43]

4.2.3 Lector inverter SRAM:

Static power dissipation of the 6T SRAM cell can be improved without affecting its dynamic power dissipation, if the CMOS inverter in the latch part the SRAM is replaced by lector inverter. Operation of the cell is same as the Basic SRAM cell. Circuit diagram of lector inverter SRAM cell is shown in Fig. 4.8 [42].

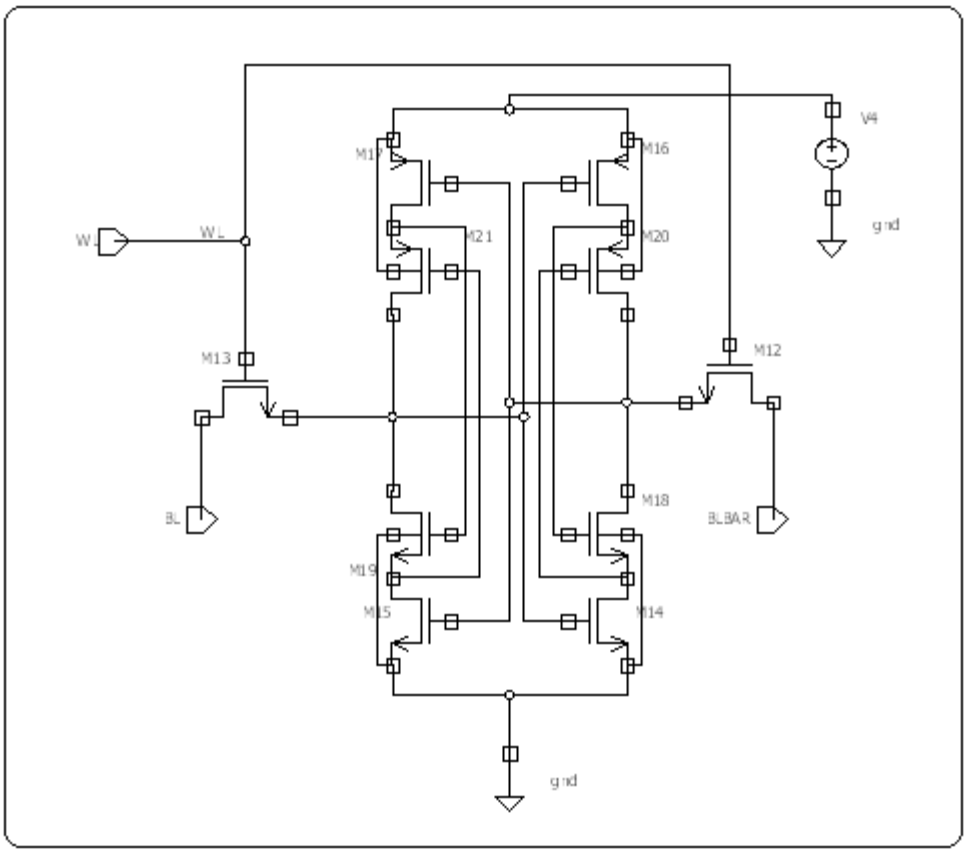


Fig 4.8 Lector Inverter SRAM Cell [42]

4.2.4 Single Ended Schmitt Trigger SRAM Cell (ST11T SRAM):

Single-ended SRAM topology is one of the exceptionally valuable methodologies for those applications which have power constraint factor. The main principal behind this is to decrease the value of leakage power or switching power ad also contributed a lot in maintaining the chip area as smaller devices are in major trends in the present era. Fig 4.10 illustrates the ST11T SRAM cell which is the extremely powerful single ended SRAM cell structure [32,38]. The SRAM cell shown comprises of a cell core (cross-coupled ST inverter), a read path comprising of two transistors, and a write-access transistor. The write-access transistor MAL is totally disciplined by row-based WL, and the read-access transistor MAR1 is completely in control of a row-based read WL (RWL). The internal storage nodes Q and QB are responsible for controlling the

feedback transistors of ST, MNFL, and MNFR respectively, and the drains of these transistors are interconnected with a control signal Word-line bar (WLB).

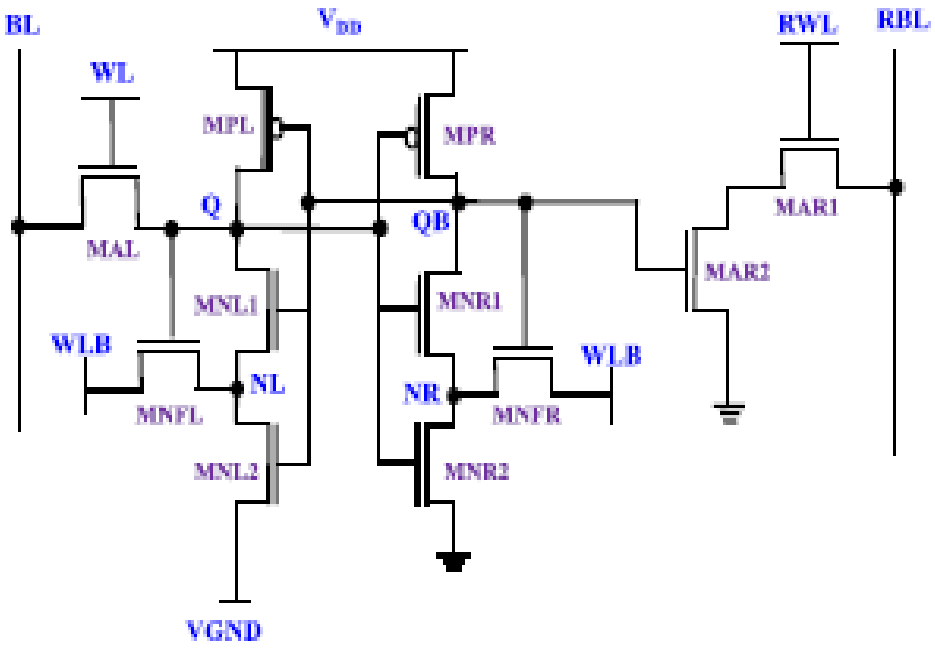


Fig. 4. 9 ST11T SRAM Cell [32]

4.2.5 Single Ended Forced Stack SRAM Cell

Schmitt-trigger-based single-ended 11T SRAM cell [32] is one of the most efficient SRAM structure but its performance can be further improved by replacing Schmitt-trigger inverter in the cell by forced stack inverter. Single-ended SRAM cell with Forced stack inverter is shown in Fig 4.11.The raw based WL signal is use to control the write access transistor and RWL is used to control the read access transistor. During hold mode both signal WL and RWL are disable and data-bit is stored in the cross-coupled inverter. IN read mode RWL is enable, whereas WL is disable, which provides a discharge path for RBL depending on the data at node QB. To write the data in the cell WL signal is enable and VGND is kept floating, which transfer the data of BL to storage node of the cell.

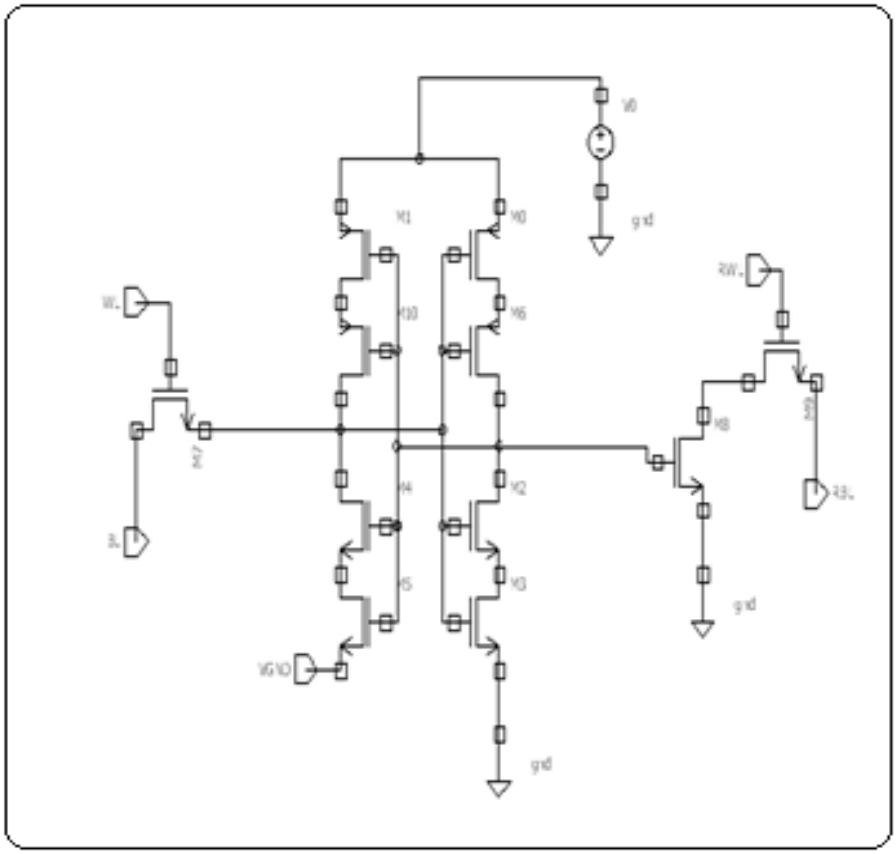


Fig 4.10 Single-Ended Forced Stack SRAM.

4.2.6 Single Ended Lector Inverter SRAM Cell

Schmitt-trigger-based single-ended 11T SRAM cell is one of the most efficient SRAM structure but its performance can be further improved by replacing Schmitt-trigger inverter in the cell by lector inverter. Single-ended SRAM cell with Lector inverter is shown in Fig 4.12.The raw based WL signal is use to control the write access transistor and RWL is used to control the read access transistor. During hold mode both signal WL and RWL are disable and data-bit is stored in the cross-coupled inverter. IN read mode RWL is enable, whereas WL is disable, which provides a discharge path for RBL calculated on the data at node QB. To write the data in the cell WL signal is enable and VGND is kept floating, which transfer the data of BL to storage node of the cell.

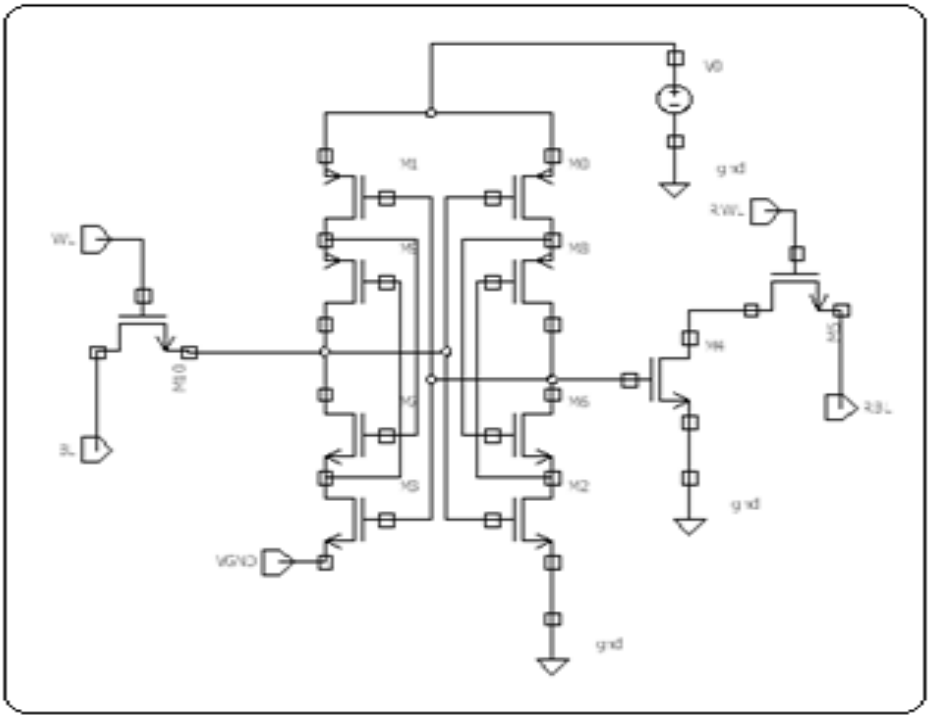


Fig 4.11 Single Ended Lector Inverter SRAM

CHAPTER 5

SIMULATION AND ANALYSIS

Various circuits of D Flip-Flops and SRAM shown in chapter 4 are simulated using SymicaDE and LT spice tool at 90nm and 45nm PTM technology parameters. Delay, static power dissipation and total power consumed by different circuits are calculated at different temperature with a voltage supply of 1 volt.

5.1 Schematic and Results of various D Flip-Flops

5.1.1 Low power clocked pass transistor flip-flop (LPCTFF)

Schematic of LPCTFF is shown in Fig 5.1 and output wave form is shown in Fig 5.2, along with different performance parameter which are shown in Table 5.1

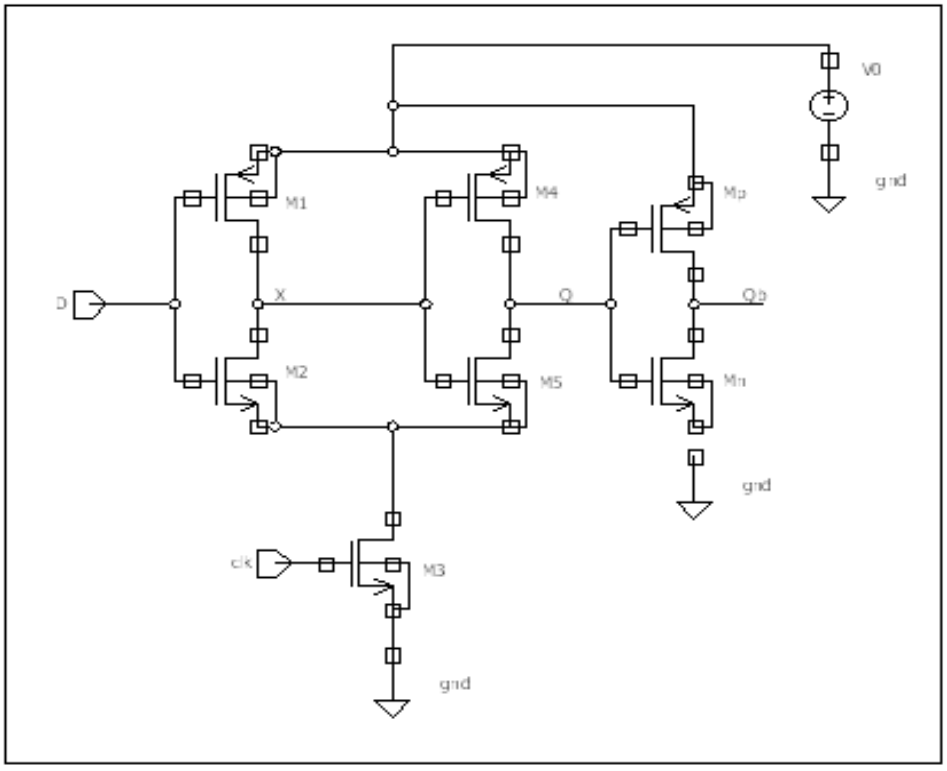


Fig 5.1 Schematic of Low power clocked pass transistor flip-flop (LPCTFF)

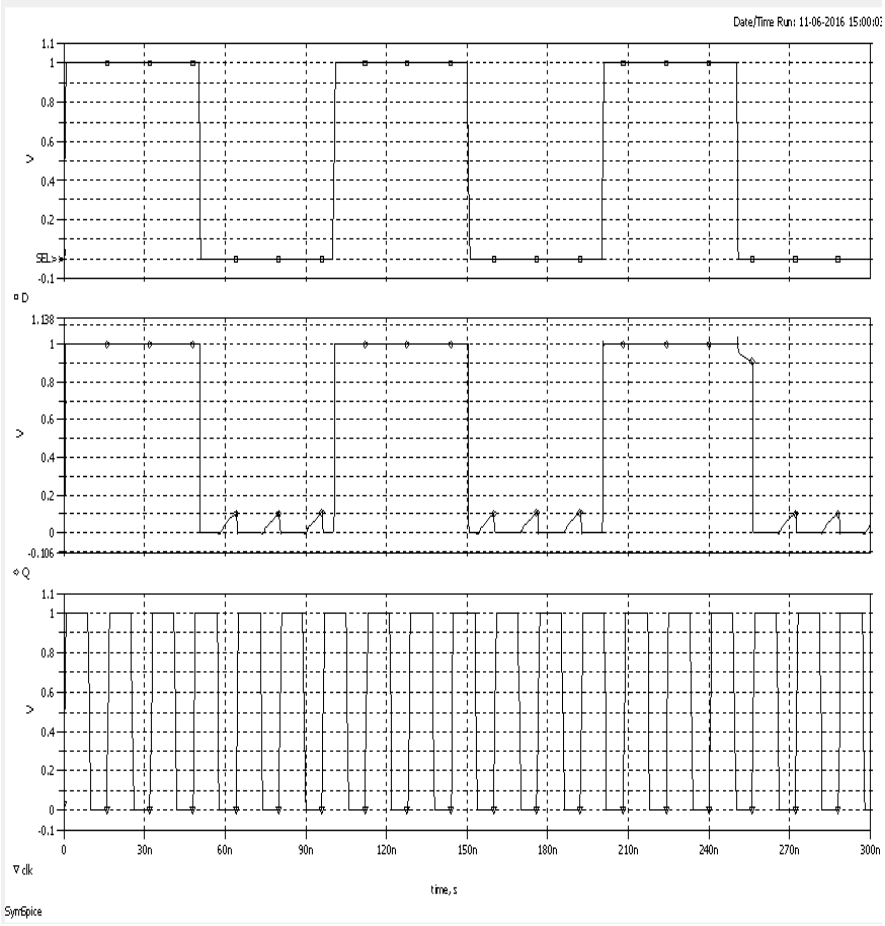


Fig 5.2 Output waveform of LPCTFF

Table 5.1 performance Parameters of LPCTFF

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Temperature(℃)
1.	45nm	11.2	28.7	27
2.		18.5	45.4	55
3.		24.8	70.5	120
4.	90nm	57.8	13.07	27
5.		64.3	19.49	55
6.		81.03	57.08	120

5.1.2 Forced Stack Low power clocked pass transistor flip-flop (FS-LPCTFF)

Schematic of Forced Stack-LPCTFF is shown in Fig 5.3,along with different performance parameter which are shown in Table 5.2

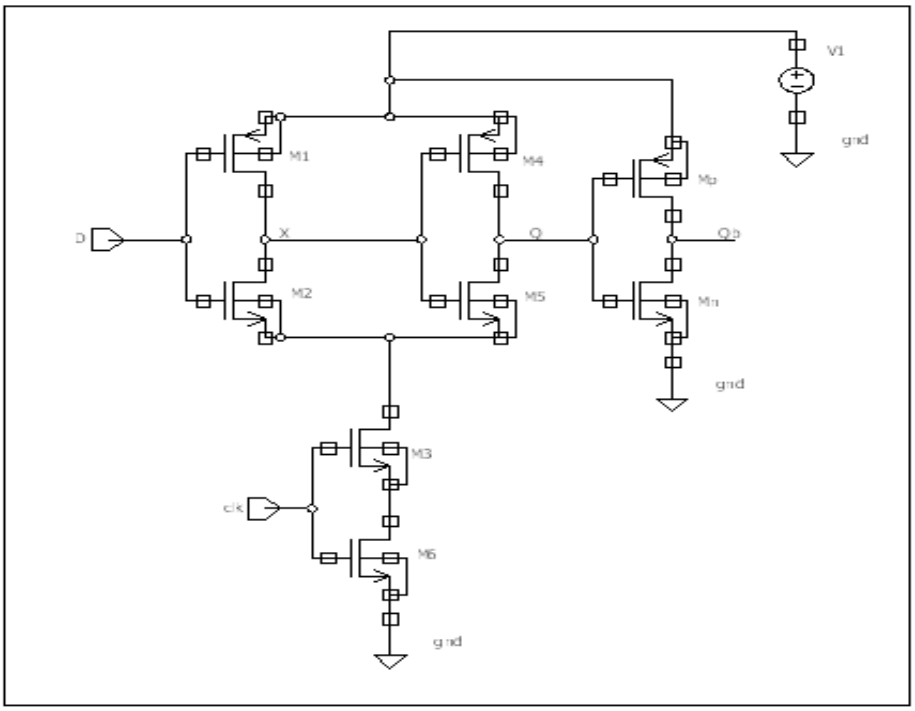


Fig 5.3.Schematic of Forced Stack Low power clocked pass transistor flip-flop (FS-LPCTFF)

Table 5.2 Performance Parameters of FS-LPCTFF

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Temperature (°C)
1.	45nm	45.42	22.9	27
2.		49.67	36.09	55
3.		63.85	56.6	120
4.	90nm	71.8	8.8	27
5.		79.73	13.6	55
6.		98.49	45.2	120

5.1.3 Sleep Transistor Low power clocked pass transistor flip-flop (ST-LPCTFF)

Schematic of Sleep Transistor-LPCTFF is shown in Fig 5.4,along with different performance parameter which are shown in Table 5.3

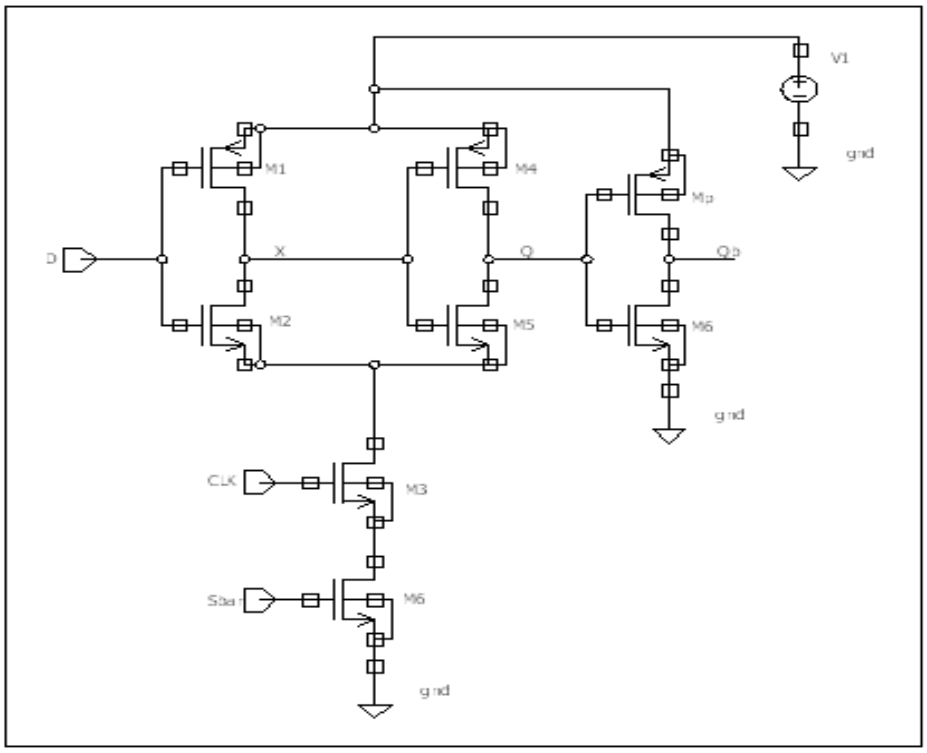


Fig 5.4 Schematic of Sleep Transistor Low power clocked pass transistor flip-flop (ST-LPCTFF)

Table 5.3 performance Parameters of ST-LPCTFF

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Temperature(℃)
1.	45nm	136.8	2.51	27
2.		158.4	9.68	55
3.		164.78	45.15	120
4.	90nm	161.9	9.1	27
5.		179.6	11.7	55
6.		198.4	28.5	120

5.1.4 Sleep Stack Low power clocked pass transistor flip-flop (SS-LPCTFF)

Schematic of Sleep Transistor-LPCTFF is shown in Fig 5.5, along with different performance parameter which are shown in Table 5.4.

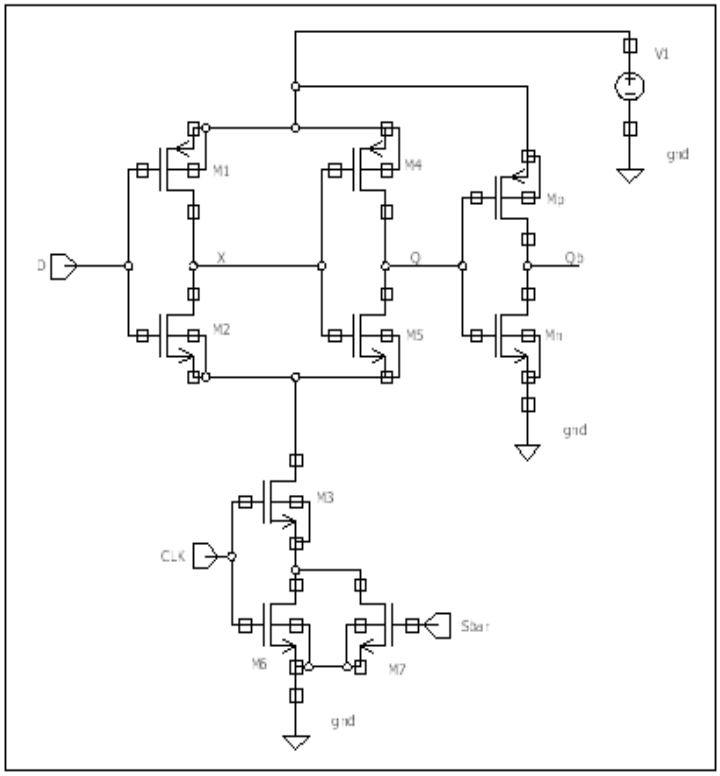


Fig 5.5 Schematic of Sleepy Stack Low power clocked pass transistor flip-flop (SS-LPCTFF)

Table 5.4 performance Parameters of SS-LPCTFF

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Temperature(°C)
1.	45nm	41.36	15.14	27
2.		46.3	33.4	55
3.		60.05	45.5	120
4.	90nm	67.8	4.68	27
5.		72.7	14.5	55
6.		92.48	42.7	120

5.1.5 Low Power Pulse Triggere D Flip-flop structure (LPTDFF)

Schematic of Low Power Pulse Triggere D Flip-flop structure (LPTDFF) is shown in Fig 5.6, along with different performance parameter, which are shown in Table 5.5.

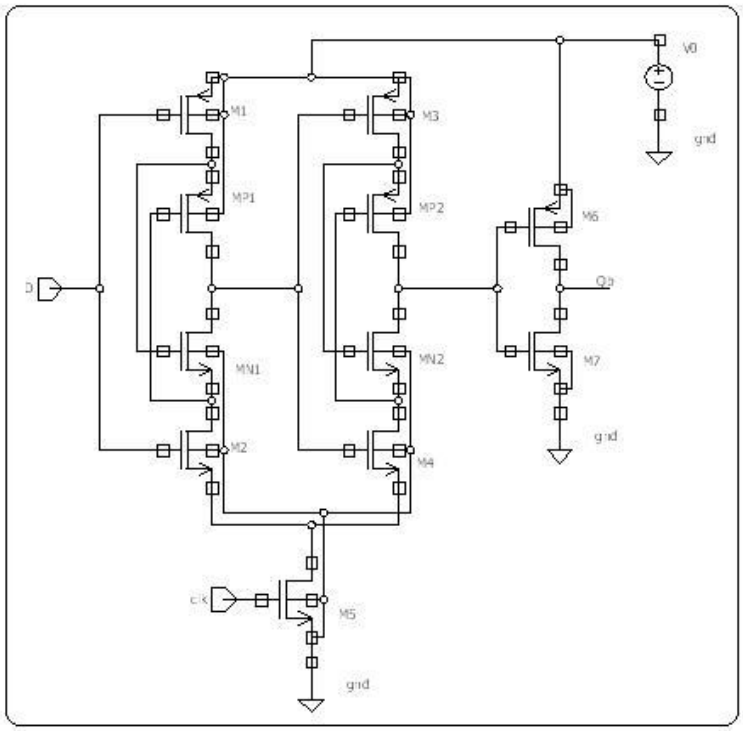


Fig 5.6 Schematic of Low power pulse triggere D flip-flop structure (LPTDFF)

Table 5.5 performance Parameters of LPTDFF

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Temperature(°C)
1.	45nm	42.937	8.88	27
2.		50.786	13.25	55
3.		70.141	30.91	120
4.	90nm	66.427	11.6	27
5.		78.019	16.41	55
6.		106.185	34.07	120

5.1.6 Comparison of Proposed D Flip-Flops with LPCTFF

Comparison of static power dissipation of various D Flip-Flops using 45nm PTM models is shown in Fig. 5.7 and using 90nm PTM models is shown in Fig 5.8.

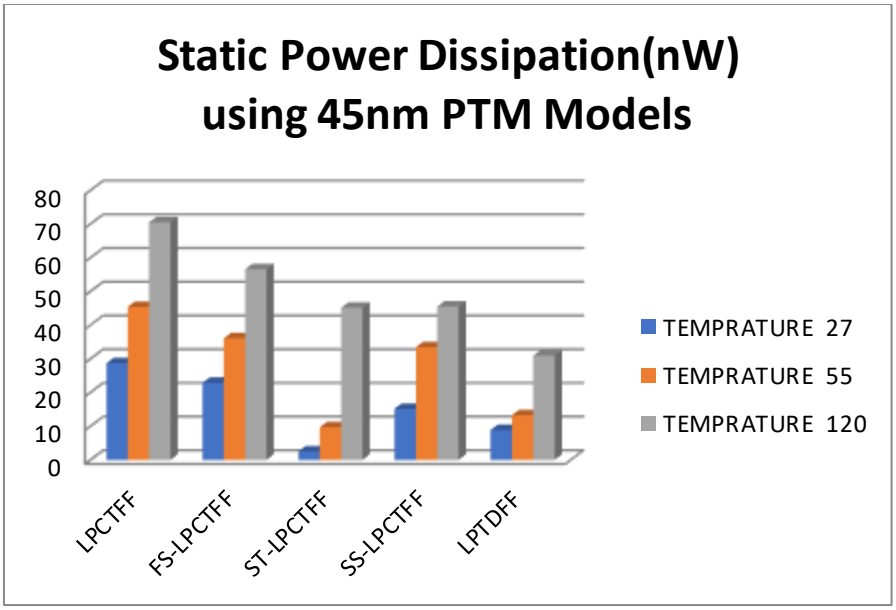


Fig. 5.7 Static Power Dissipation of Various D Flip-Flops at 45nm.

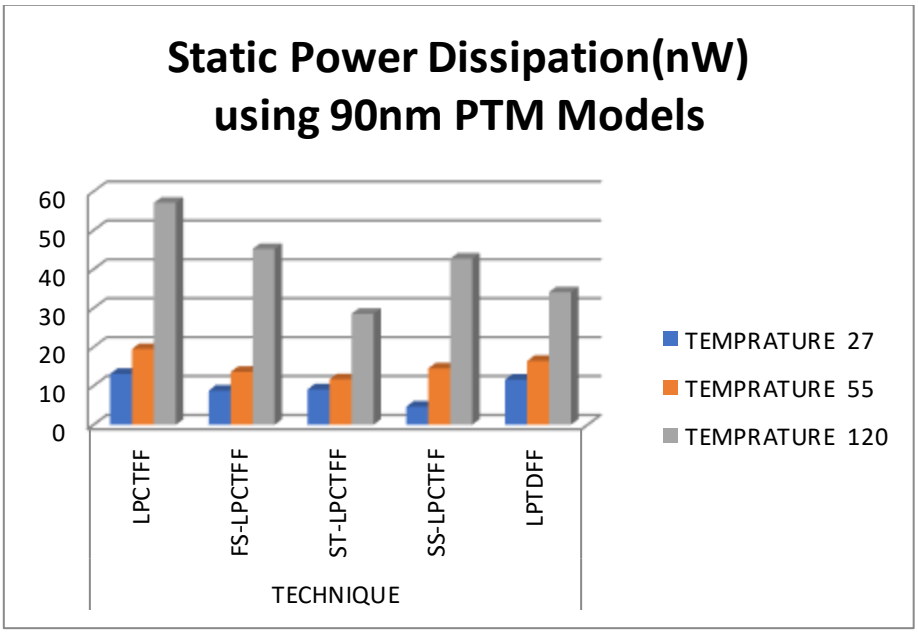


Fig. 5.8 Static Power Dissipation of Various D Flip-Flops at 90nm.

Comparison of Delay of various D Flip-Flops using 45nm PTM models is shown in Fig. 5.9 and using 90nm PTM models is shown in Fig 5.10.

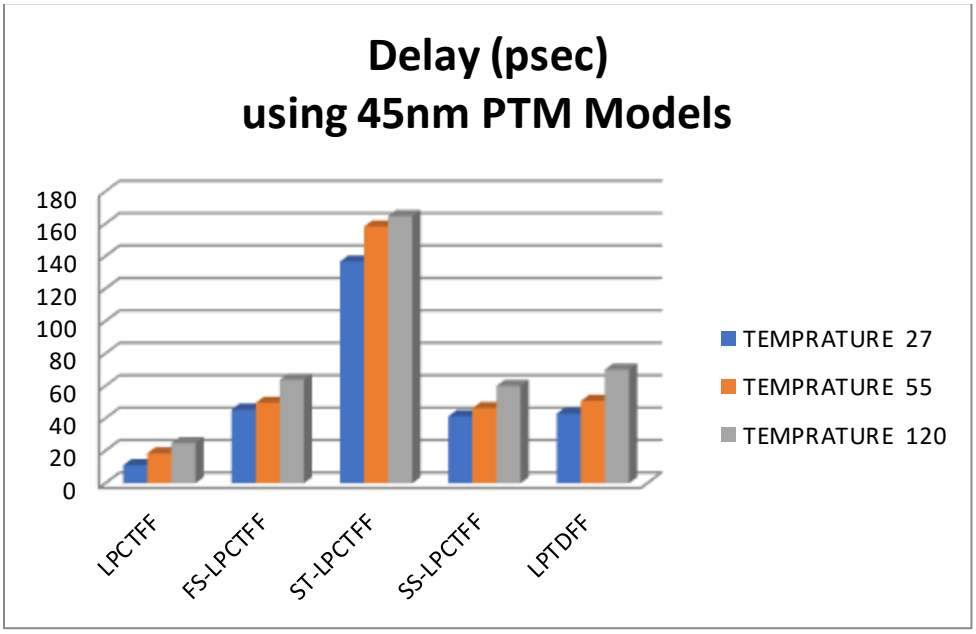


Fig. 5.9 Delay of Various D Flip-Flops at 45nm.

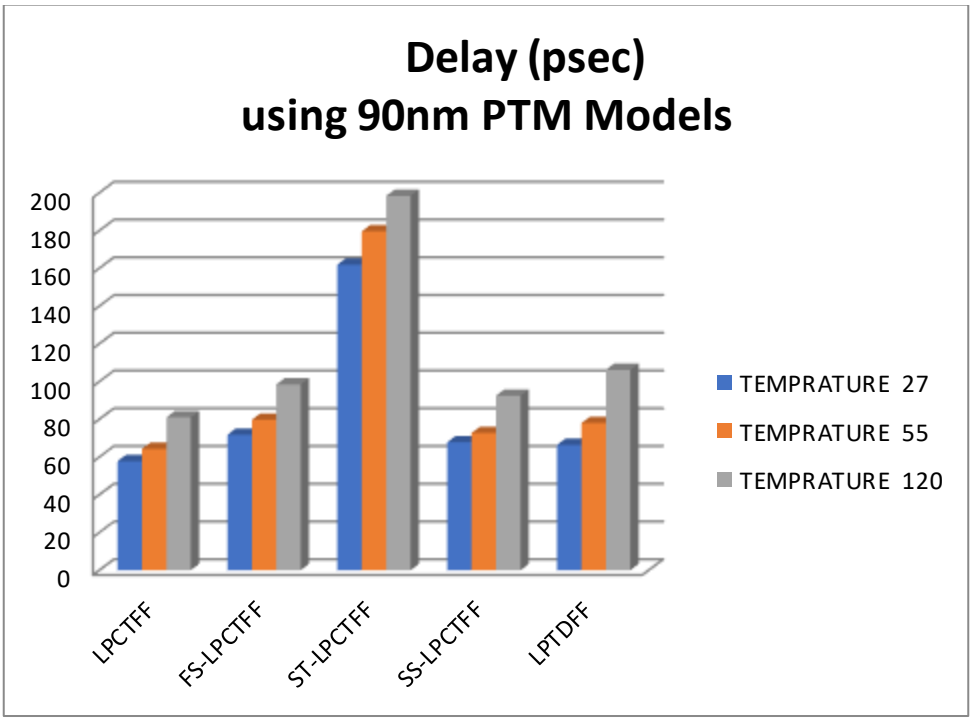


Fig. 5.10 Delay of Various D Flip-Flops at 45nm.

5.2 Schematic and Result of Various SRAM

5.2.1 Conventional 6T SRAM

Schematic of conventional 6T SRAM is shown in Fig 5.11 and output is shown in Fig 5.12, along with different performance parameter, which are shown in Table 5.6.

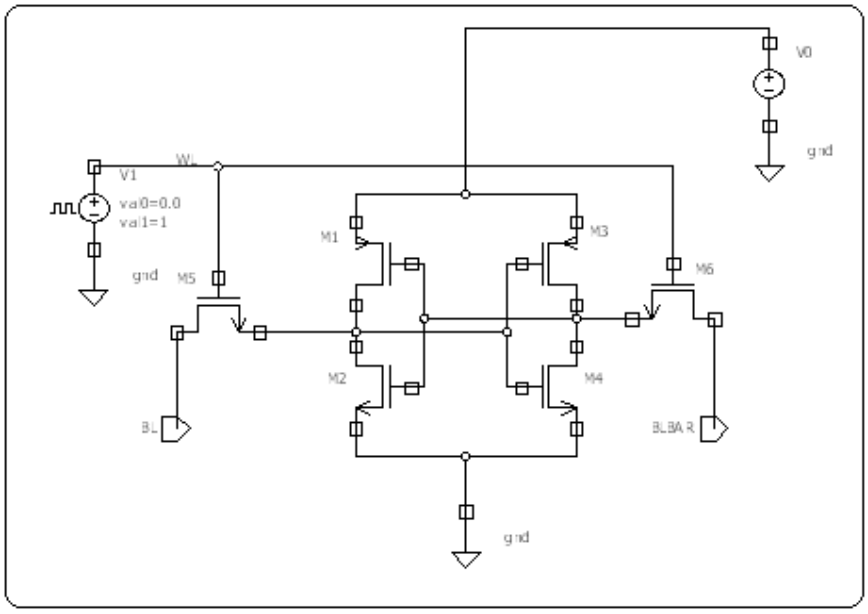


Fig 5.11 Schematic of Conventional 6T SRAM

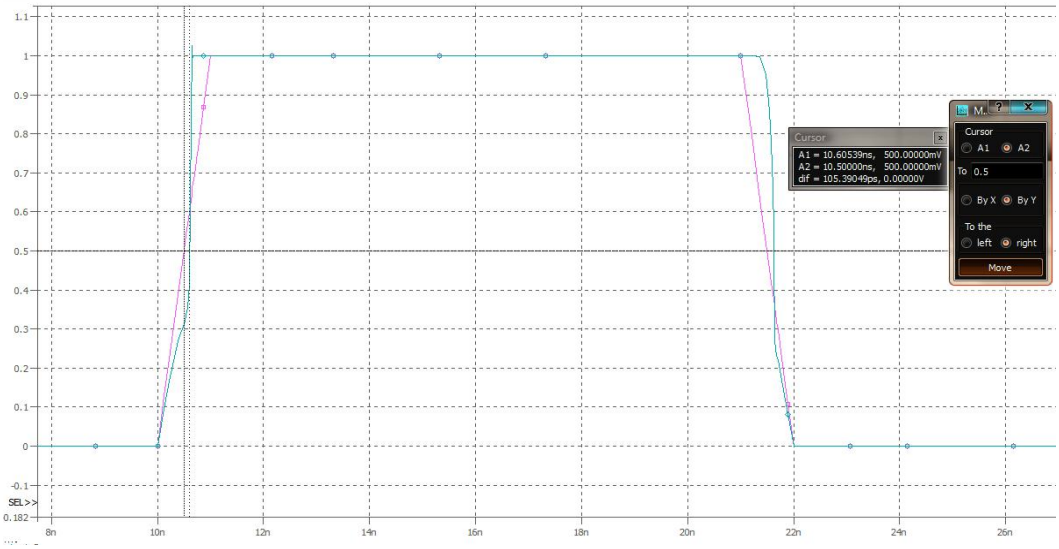


Fig 5.12 output of SRAM

Table 5.6 Performance Parameters of Conventional 6T SRAM

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Total Power Diss. (µWatt)	Temperature(°C)
1.	45nm	108.85	420.72	1.52	27
2.		115.4	489.61	1.79	55
3.		129.76	534.71	2.17	120

5.2.2 Forced Stack SRAM

Schematic of Forced Stack-SRAM is shown in Fig 5.13,along with different performance parameter which are shown in Table 5.7

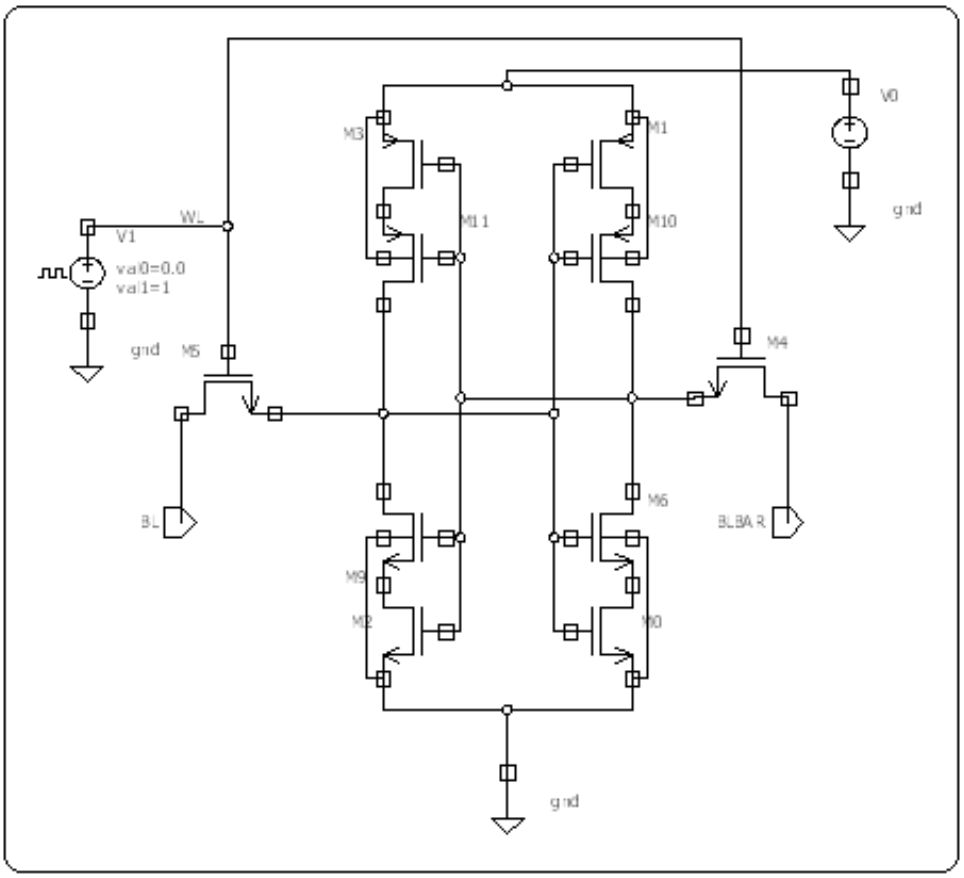


Fig.5.13.Schematic of Forced Stack SRAM

Table 5.7 Performance Parameters of Forced Stack SRAM

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Total Power Diss. (µWatt)	Temperature(°C)
1.	45nm	547.8	268.09	0.889	27
2.		593.2	285.1	0.962	55
3.		615.7	298.5	1.084	120

5.2.3 Lector Inverter SRAM

Schematic of Forced Stack-SRAM is shown in Fig 5.14,along with different performance parameter which are shown in Table 5.8

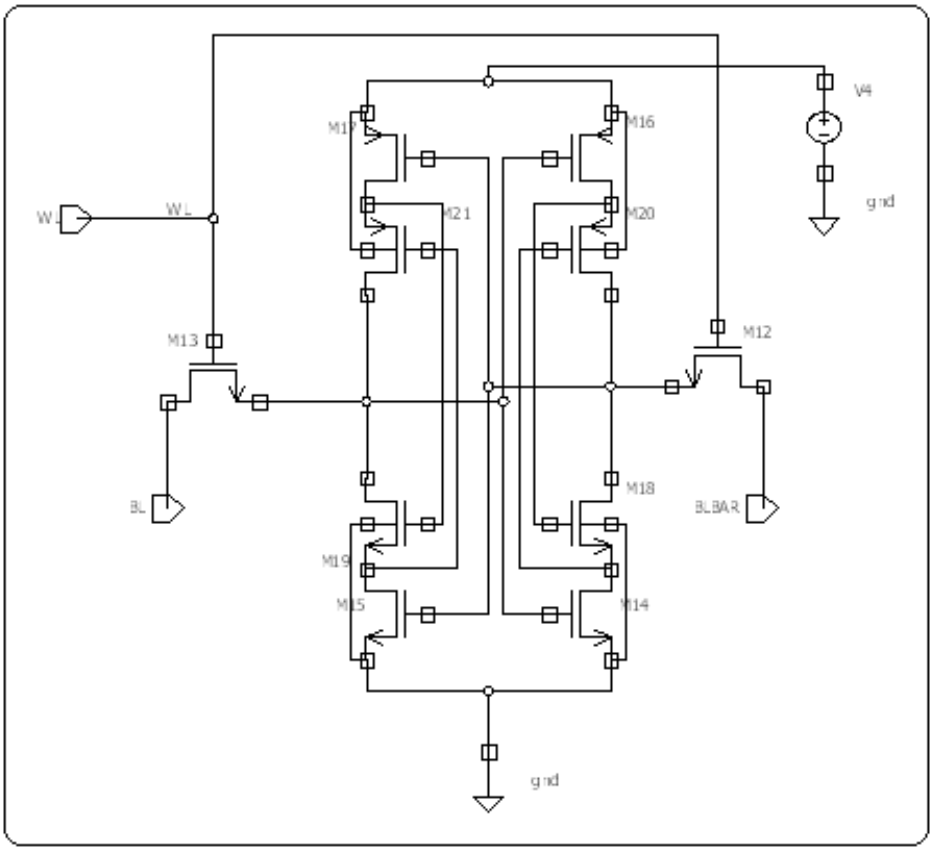


Fig.5.14. Schematic of Lector Inverter SRAM

Table 5.8 Performance Parameters of Lector Inverter SRAM

S.No	Technology Node	Delay (psec)	Static Power Diss. (nwatt)	Total Power Diss. (µWatt)	Temperature(℃)
1.	45nm	670.58	359.57	0.993	27
2.		689.3	371.9	1.067	55
3.		704.7	396.6	1.172	120

5.2.4 Comparison of 6T SRAM and Other modified 6T SRAM

Comparison of static power dissipation of various 6T SRAM using 45nm PTM models is shown in Fig. 5.15

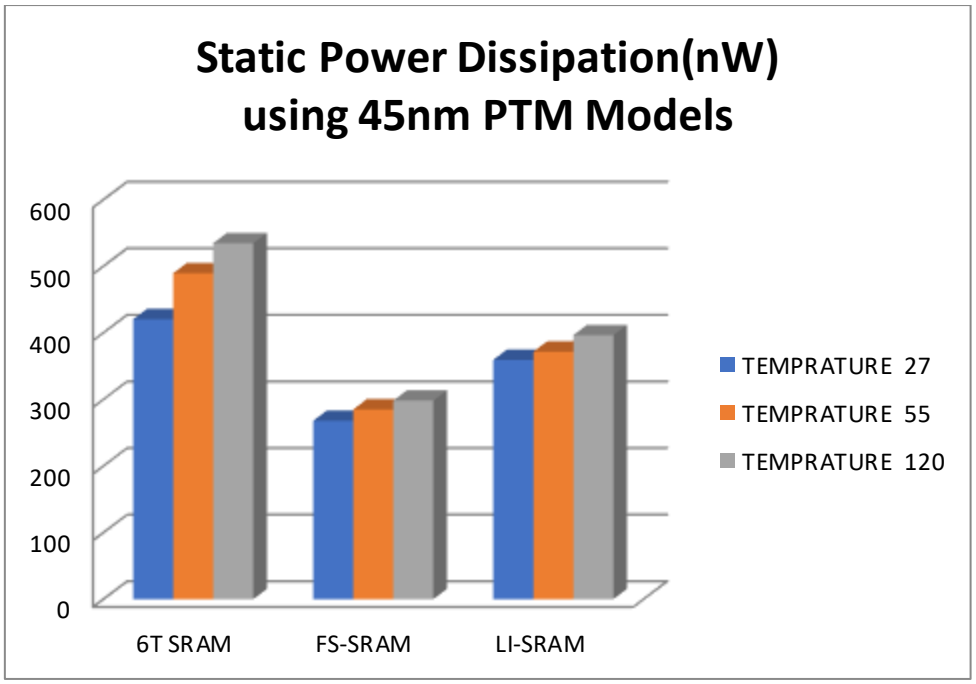


Fig. 5.15 Static Power Dissipation of Basic SRAMs

Comparison of Delay of various 6T SRAM using 45nm PTM models is shown in Fig. 5.16

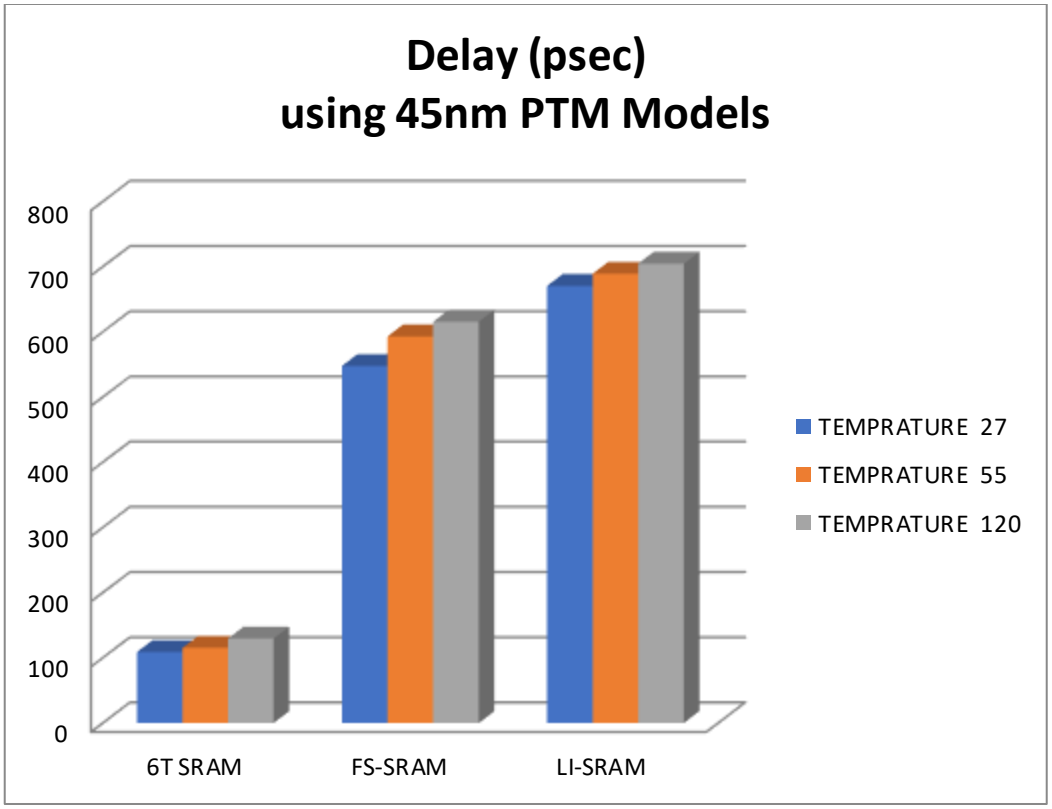


Fig. 5.16 Delay of Basic SRAMs

Comparison of Average power dissipation of various 6T SRAM using 45nm PTM models is shown in Fig. 5.17

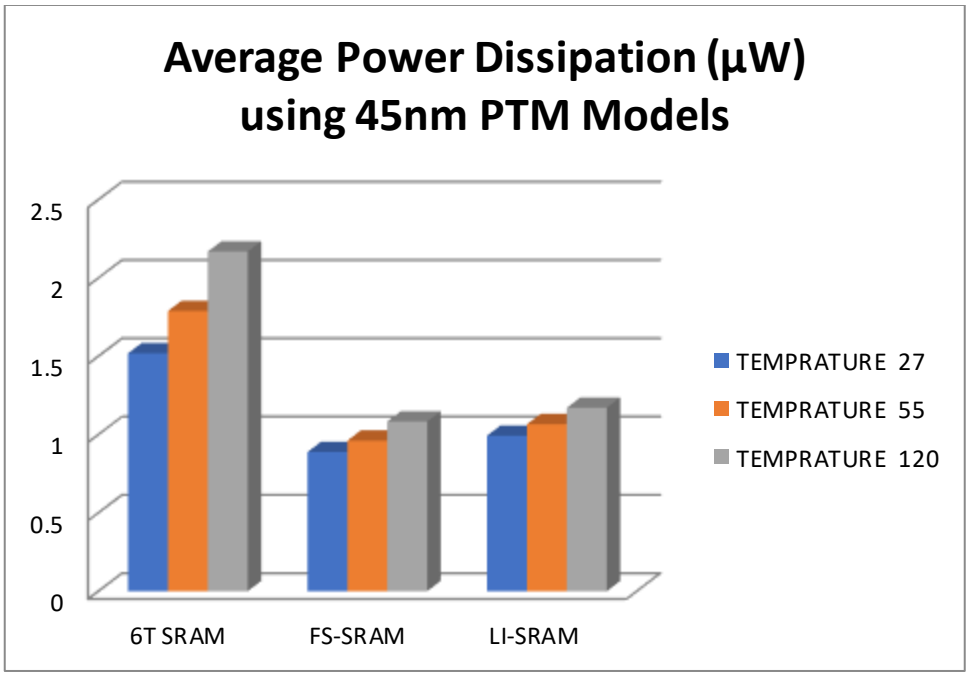


Fig. 5.17 Average Power Dissipation of Basic SRAMs

5.2.5 Various Single Ended SRAM Cell

Schematic of Single Ended Schmitt Trigger SRAM (ST11T SRAM) , Single Ended Forced Stack SRAM cell and Single Ended Lector Inverter SRAM cell is shown in Fig 5.18, Fig 5.19 and Fig. 5.20 respectively along with different performance parameter which are shown in Table 5.9.

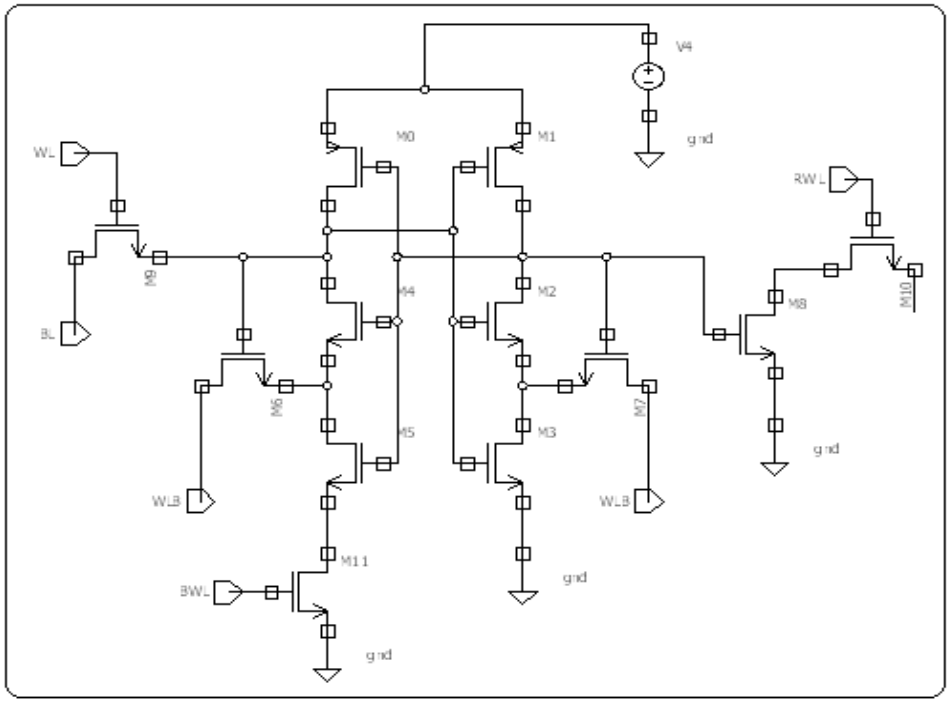


Fig. 5.18 Schematic of ST11T SRAM

Table 5.9 Performance Parameters of various Single Ended SRAM

SRAM CELL	P_{static} (Hold Mode) (µW)	P_{static} (Read Mode) (µW)	P_{static} (Write Mode) (µW)	$P_{Average}$ (µW)	Total Energy (fJ)
ST11T SRAM	1.72	1.65	4.28	3.41	341.19
FS11T SRAM	1.43	1.39	0.98	2.10	210.16
LI11T SRAM	1.40	1.48	0.826	1.13	113.31

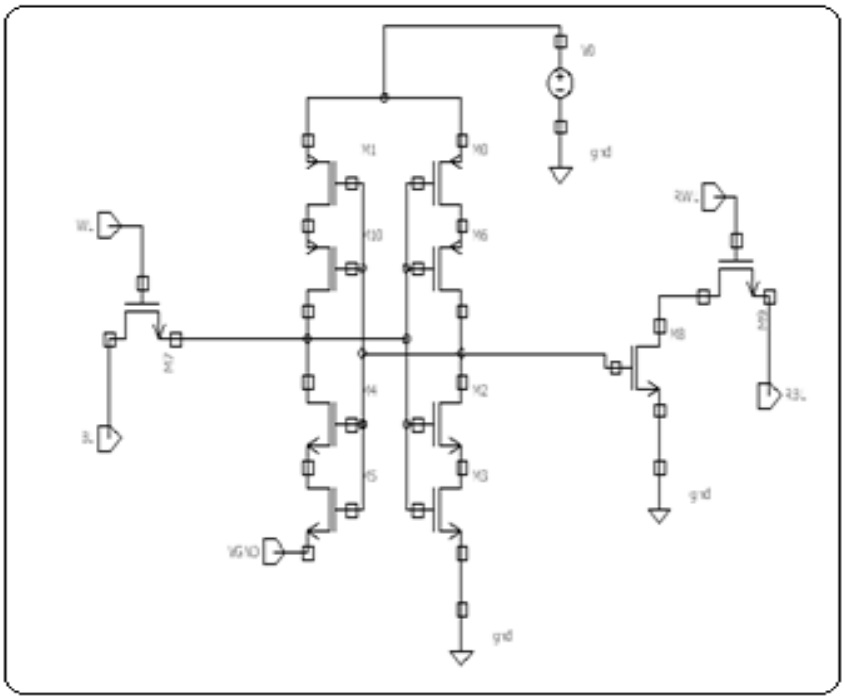


Fig 5.19 Schematic of FS11T SRAM

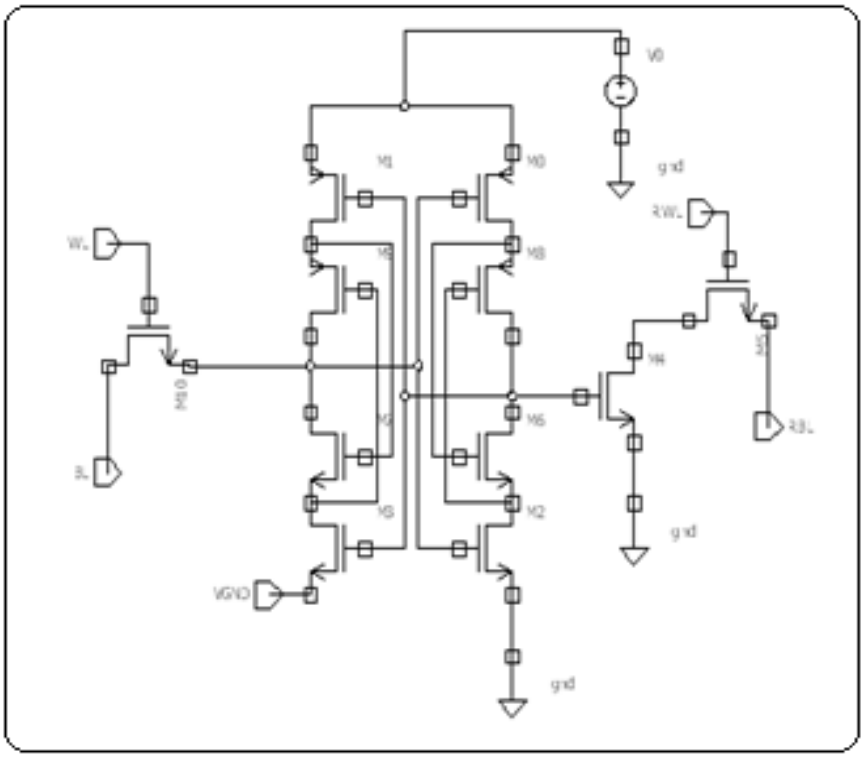


Fig.5.20 Schematic of LI11T SRAM

5.2.6 Comparison of Various Single Ended SRAMs

A comprehensive comparison of proposed Single Ended SRAM cells with Schmitt-trigger-based single-ended 11T SRAM cell shown in Fig. 5.21, Fig 5.22and Fig. 5.23.

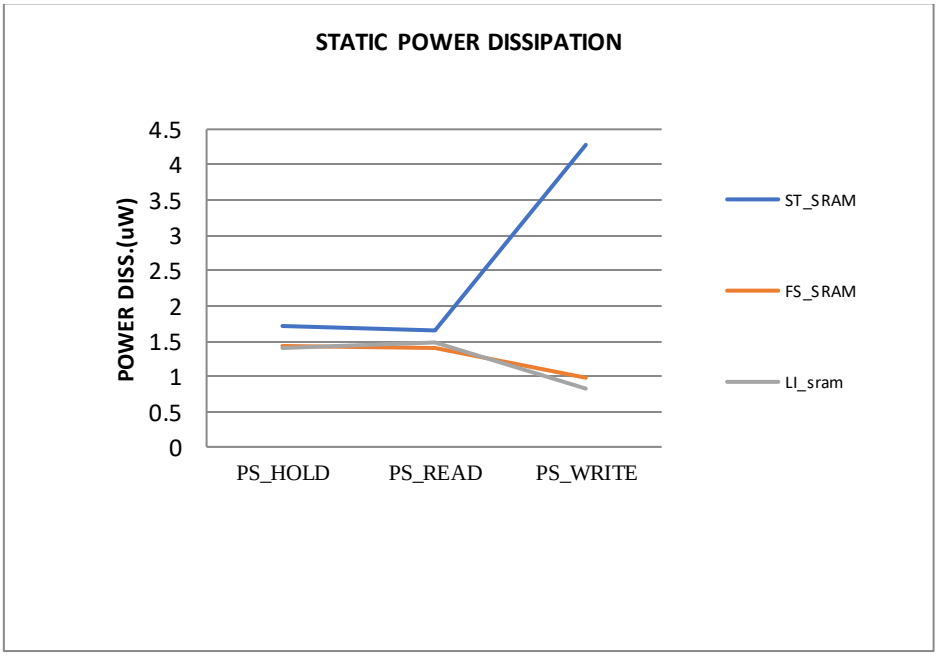


Fig5.21 Static power Dissipation in hold, read and write mode for various SRAM Cells

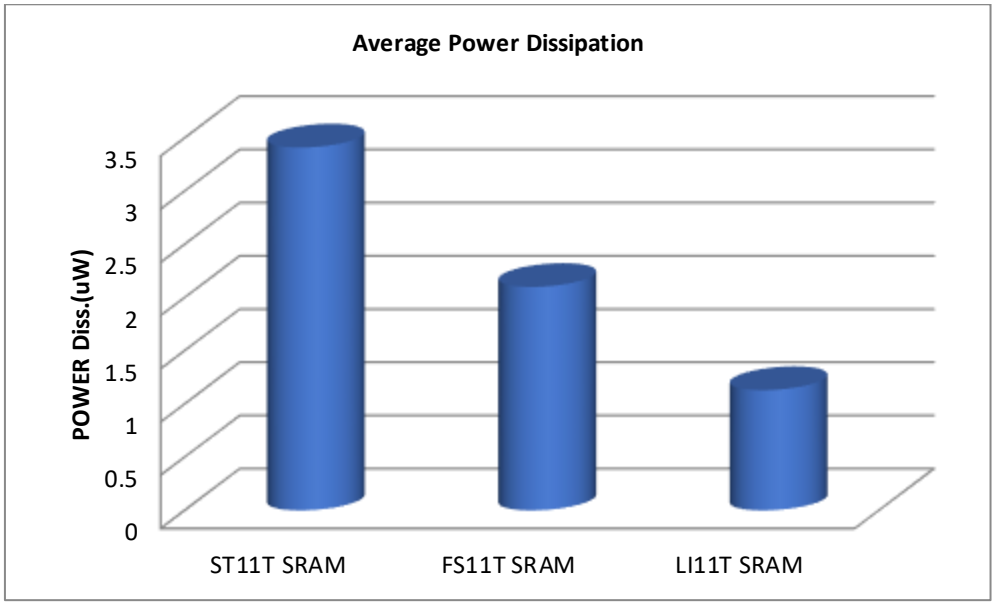


Fig5.22 Average Power Dissipation in various SRAM cells

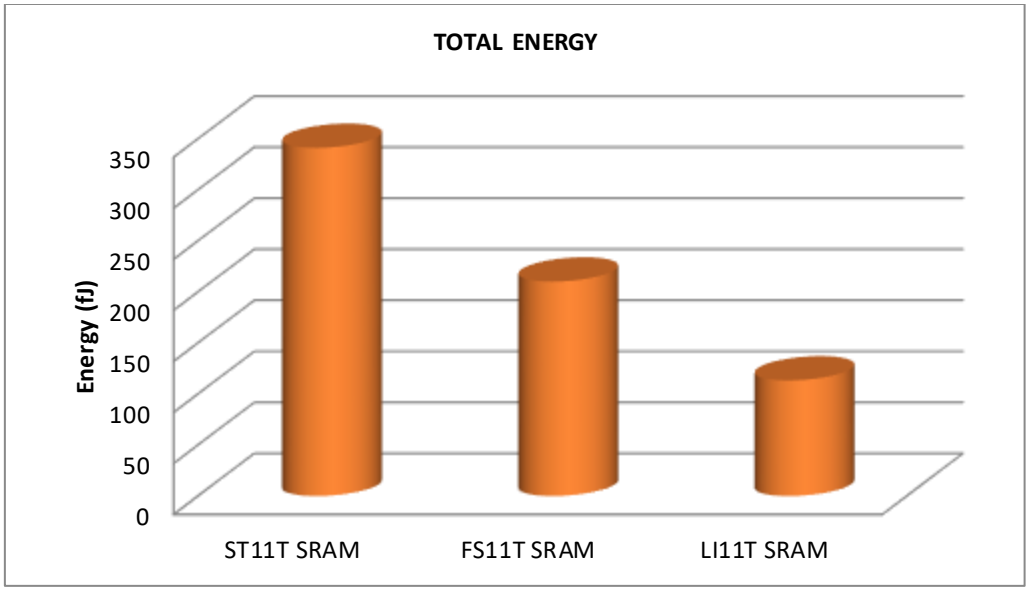


Fig 5.23 Total energy consumption in various SRAM Cells

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

In this work, the performance parameters of proposed D-flip-flop structures are calculated in terms of static power dissipation and delay. Sleepy Stack LPCTFF flip-flop give the optimum performance over all other structure of LPCTFF flip-flop. It reduces the static power dissipation by 47.2% and 64.19 % using 45nm and 90nm PTM models respectively. Sleepy Stack and forced Stack structure also have the power-delay products lower than the simple LPCTFF structure. The power-delay product for Sleepy stack LPCTFF and Forced Stack LPCTFF structures is 42% and 83.6% of the simple LPCTFF structure. Along with this, It has been concluded that the proposed LPTDFF circuit, gives an effective advantage of reduction in both static and dynamic power dissipation The static power dissipation of LPTDFF is reduced by 69.78%,and 11.2% by using for 45nm and 90nm PTM models respectively as compared to simple LPCTFF. On the contrary, there is increase in delay of LPTDFF by using lector inverter.

The performance parameters of SRAM structures are also calculated in terms of static and dynamic power dissipation.. Modified SRAM using forced stack technique reduced the static power dissipation by 36.27% and the average power dissipation by 41.5%. While, the modified SRAM using LECTOR technique reduces the static power dissipation by 14.53% and the average power dissipation by 34.67%.

The proposed single ended forced stack SRAM cell and LECTOR inverter SRAM cell improves the performance parameter to a greater extent as compared to the previous research work.

In the proposed single ended forced stack SRAM cell, the static power dissipation in hold mode, read mode and write mode is reduced by 16.8%, 15.7% and 77.1% respectively and the total power dissipation by 41.5%. And the proposed single ended LECTOR SRAM cell, the static power dissipation in hold mode, read mode and write mode is reduced by 18.6%, 10.3% and 80.6% respectively and the total power dissipation is reduced by 66.8%.

6.2 Future Scope

The proposed circuit gives an advantage of highly improved power reduction but on the contrary the delay is also increased. So, the circuit can be further improved so that the delay can also be reduced without affecting other performance parameters.