IMPLEMENTATION OF ANALOG CIRCUITS USING CDTA AND CDDITA

Project Report submitted in partial fulfillment of the requirements for the degree of

MASTER of TECHNOLOGY (M. Tech.)

In

VLSI AND EMBEDDED SYSTEMS

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CERTIFICATE

This is to certify that the report titled **"Implementation of analog circuits using CDTA and CDDITA"** is a bonafide record of Major-2 submitted by **Ambatkar Harshal Sureshrao (Roll no: 2K15/VLS/02)** as the record of the work carried out by him under my guidance. The said work has not been submitted anywhere else for the award of any other degree or diploma.

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CANDIDATE DECLARATION

This is to certify that dissertation entitled **"Implementation of analog circuits using CDTA and CDDITA"** which is submitted by me in partial fulfillment of the requirement for the award of M.Tech. degree in **VLSI and Embedded Systems** from Delhi Technological University, Delhi, INDIA comprises only my own work and due acknowledgement has been made to all other material used.

I hereby, further declared that in case of legal dispute in relation to my M.Tech. dissertation, I will be solely responsible for the same.

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M. Tech. (VLSI)

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Date:

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M. Tech. (VLSI)

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
i/p-o/p	Input-Output
IC	Integrated Circuit
IVI	Current-Voltage-Current
VIV	Voltage-Current-Voltage
SFG	Signal Flow Graph
AC	Alternating Current
DC	Direct Current
VLSI	Very Large Scale Integration
VCCS	Voltage Controlled Current Source
DVCCS	Differential Voltage Controlled Current Source
SR	Slew Rate
ADC	Analog to Digital Convertor
DAC	Digital to Analog Convertor
ASP	Analog Signal Processing
ABBs	Active Building Blocks
CM	Current Mode
VM	Voltage Mode
MM	Mixed Mode
CFA	Current Feedback Amplifier
VFA	Voltage Feedback Amplifier
CDU	Current Differencing Unit

FVF	Flip Voltage Follower
OTA	Operational Transconductance Amplifier
DO-OTA	Dual Output OTA
CDTA	Current Differencing Transconductance Amplifier
MO-CDTA	Multiple Output CDTA
CCCDTA	Current Control CDTA
CD-DITA	Current Differencing Differential Input Transconductance Amplifier
ZC-CDTA	Z-copy CDTA
CC	Current Conveyor
CCII	2nd generation Current Conveyor
CCCII	2nd generation Current Controlled Current Conveyor
CCTA	Current Conveyor Transconductance Amplifier
DDCC	Differential Difference Current Conveyor
OTRA	Operational Transresistance Amplifier
DVCC	Differential Voltage Current Conveyor
FTFN	Four Terminal Floating Nuller
CDBA	Current Differencing Buffered Amplifier
VDTA	Voltage Differencing Transconductance Amplifier
VD-DIBA	Voltage Differencing – Differential input Buffered Amplifier
APF	All Pass Filter
BPF	Band Pass Filter
BRF	Band Reject Filter
KHN	*Kerwin-Huelsman-Newcomb*
MISO	Multiple Input Single Output
B.W	Bandwidth

ABSTRACT

A new CMOS realization of the current differencing differential input transconductance amplifier (CD-DITA) and CD-DITA based voltage mode MISO-type universal biquad filter are proposed. CD-DITA is an extension of CDTA having extra voltage input than CDTA increasing its usability of differential inputs. For a suitable CMOS based implementation of CD-DITA, several CDTA realizations are studied and the suitable one is modified to implement the proposed CD-DITA block. A FVF based DO-CDTA is characterized and its applications in analog signal processing circuits such as basic amplifiers, signal generators such as Schmitt Trigger and KHN filter are also studied. The proposed CD-DITA based voltage mode MISO-type universal biquad filter is realized with two resistors and two capacitors with independent electronic control of natural frequency and quality factor. The proposed filter can implement all five second order low pass, high pass, band pass, band stop, and all pass filter responses without altering the circuit topology. The proposed filter also offers low active and passive sensitivities. In addition, the effects of parasitics and errors on the proposed filter are also investigated. The characteristics CDTA and its applications are verified by PSPICE simulations using TSMC 0.25μm CMOS technology. The characteristics of CD-DITA and validity of proposed universal biquad filter is verified by SPICE simulation using TSMC 180nm technology.

Chapter

1. Introduction

The advancement in IC technology provides compact and efficient implementation of the different types of digital signal processing applications on silicon chip. CMOS technique generates digital most efficient and smaller sized circuits with high performance.

However digital signal processing also have some issues such as

- Every naturally occurring signal is analog. So ADC/ DAC are required at the interface of two worlds.
- Long distance transmission of digital signal using cables causes attenuation and distortion because of their limited bandwidth.
- Distribution of large data and timing of clock over a large chip may result in clock skew
- A trade-off between, noise, level of interferer, operating frequency, power dissipation and cost of digital systems.

Therefore, despite of the advancement made in digital signal processing, many crucial analog domain functions such as signal amplification, time varying signal rectification, continuous time filtering, analog-to-digital (A/D) and digital-to-analog (D/A) conversions cannot be carried out by digital circuits[1]. The need for analog circuits with extreme speed of operation with high precision signal processing, low supplies and low power dissipation has been increased [2]. Thus, analog signal processing (ASP) circuits are necessitous in several practical operations such as amplification and conditioning of signals in communication applications, modulation in both analog and digital communication, processing of optical signals. In conclusion, despite of the whole world going digital, analog designs and circuits are not outdated rather; they are evolving to face new challenges and to make it go concurrent with digital technology.

1.1. Voltage and current mode signal processing

Since two decades, in VLSI design the development of latest analog signal processing applications has been following the buzz of so-called current mode (CM)[3] due to the advantages it offers. The application is said to be working in CM when signals (information) being processed, are in the form of currents rather than the conventional voltage mode (VM), which uses voltages. The reason behind using the current mode circuits is it being exhibiting

large bandwidth and superior signal linearity. Another advantage of using circuits CM is use of smaller supply voltages since the design of CM circuits deals in the processing of current which can be achieved with lower voltage swings. Simultaneously, the mixed-mode (MM) circuits are also analyzed and synthesized along with the development of CM applications. This is because of the necessity effective interface between the sub-blocks working in different modes. It is known from a boundless literature on CM circuits published in the recent past, that these techniques have provided number of significant ASP and signal generating circuits. Due to tremendous progress made in IC technology in last two decades, CM analog techniques have quite often been exploited by circuit designers providing efficient solutions to multiple circuit design problems. As an outcome, the CM approach to analog signal processing has been claimed to offer one or more of the following advantages: higher operating frequency range, lower power consumption, larger slew rates (SR), better linearity and high precision and accuracy.

1.2.Motivation

Since many years, traditional VM op-amps are believed to be performing almost all ASP functions. All linear integrated and discrete circuits such as the voltage/current controlled sources, integrators, differentiators, summers and differencing amplifiers, instrumentation amplifiers with variable-gain, filters and oscillators etc., can be realized using op-amps. Op-amps can also perform many non-linear operations such as voltage comparators, Schmitt trigger, high precision rectifiers, multi-vibrators, log-exponential amplifiers and oscillators. Till 1990 or so, the designing of analog electronic circuits was heavily subjugated by op-amps. But due to its limitations the popularity of op-amps has been receding lately. Many op-amp circuits require excessive number of external components and also the number of matched components or constraints to be met for implementing the required circuit functions is more than necessary. A most important shortcoming of the several controlled voltage/current sources employing the conventional op-amps is the ‘gain-bandwidth-conflict’ which essentially means the product of gain-bandwidth remain constant and cannot be tuned independently. Another crucial limitation, which restrains the usage of op-amp circuits in high frequency range, is its finite slew rate (SR)

CM circuits give intriguing choices and solutions over their VM counterparts in giving several advantages such as realizing circuit functions with less external components, no conditions on component-matching or constraints, less complex circuit structures, better

linearity with higher dynamic range, accuracy in its input-output characteristics and higher operating frequency range.

The primitive set of active building blocks (ABBs) for ASP and signal generating is currently developing in two ways. The first is the modification in the basic blocks such as transconductance Amplifier, Current mirrors, Voltage Feedback Amplifier, current conveyors, and Current Feedback Amplifier. The important boost for such modifications is to increase the application capability of the element. Another requirement is that the active element should have simpler internal structure for high-speed operation along with low power consumption. Another crucial motivation to revamp the circuit is the electronic control of gain or other parameters. The second way of the progress is characterizing the active elements by extending the original OTA-VFA-CC-CFA set leading to entirely new elements. In a Search of Novel ABBs, we seek few rational motivation factors:

- To increase the universality of an ABB while keeping the simpler topology.
- Elimination or reduction of parasitic effects
- Need for electronic control of inherent parameters.
- To design circuits applications with a minimum number of these ABBs with a minimum external passive components
- To find solutions to trade-off between required operating speed and accuracy.

The current differencing transconductance amplifier (abbreviated as CDTA) and current differencing differential input transconductance amplifier (abbreviated CD-DITA) which is an extension to CDTA are one among those. These elements are characterized by low i/p and high o/p impedances, which is suitable for implementation of signal processing applications in CM operation. The universality of CD-DITA leads to the realizations using lesser active components and are therefore structurally simpler.

1.3. Objective

In view of the above discussions, the dissertation has concentrated on the following basic objectives to be achieved for CDTA:

- Literature survey for identifying research gaps
- Design and development of CDTA block
- Study and implementation of existing CDTA based applications

For the discussion of CD-DITA, the main objectives are to design a new CMOS based CD-DITA and propose a new application. To achieve this, the dissertation has concentrated on the following areas to narrow down the broad objective:

- Design of new CD-DITA block
- Design of universal biquadratic filter employing a single CD-DITA

The objective of CD-DITA based filter is to design MISO-type VM universal biquad filter employing a single CD-DITA, two capacitors and two resistors with three voltage i/p's and one o/p; realizing all five standard filter transfer functions by appropriate selection of i/p voltages from the same circuit configuration without the requirement of inversion of i/p signal and altering the circuit topology. To meet the objectives, the existing and proposed designs will be simulated using PSPICE software in 250nm (for CDTA) and 180nm (for CD-DITA) TSMC technology nodes to test their functionality. The simulated results will be compared with the theoretical results.

1.4. Organization of Thesis

Chapter 1: Presents brief introduction of current scenario in analog circuit design and salient features of CM processing. This chapter also discusses the motivation and objective of the work undertaken.

Chapter 2: An extensive survey of CDTA literature on CDTA structures and survey of several MISO-type VM universal biquad circuits using CM ABBs.

Chapter 3: FVF based CDTA is realized and its non-idealities are studied and simulated. It is also characterized for DC and AC responses and various performance parameters are extracted through sumlations.

Chapter 4: Some existing signal generation and processing applications are implemented using FVF based CDTA to verify the functionality of this structure in various applications. The applications include few basic amplifier configurations, Schmitt Trigger and CM-KHN biquad.

Chapter 5: A new structure of CD-DITA is proposed and Various performance parameters of non-ideal CD-DITA that could affect filter performance were simulated along with the measurement of parasitics to use them in filter analysis.

Chapter 6: A new CD-DITA based VM-MISO type universal filter is proposed. Deep analysis of filter responses considering the non-idealities of CD-DITA is presented and simulated to

verify the simulation results with the theoretical values. The filter responses are simulated to validate the workability of the proposed filter.

Chapter 7: This chapter records chronological summary of the work presented in this dissertation and future work also has been discussed.

Chapter

2. Literature Survey

2.1.Introduction

In past few decades the CM analog signal processing has received considerable interest owing to the advantages offered by CM techniques which have been elaborated in chapter 1. This has resulted in emergence of various CM analog building blocks and CDTA is one among those. The CDTA block was first reported by D. Biolek [4] in 2003. The block diagram of CDTA is shown in Fig. 2.1(a)

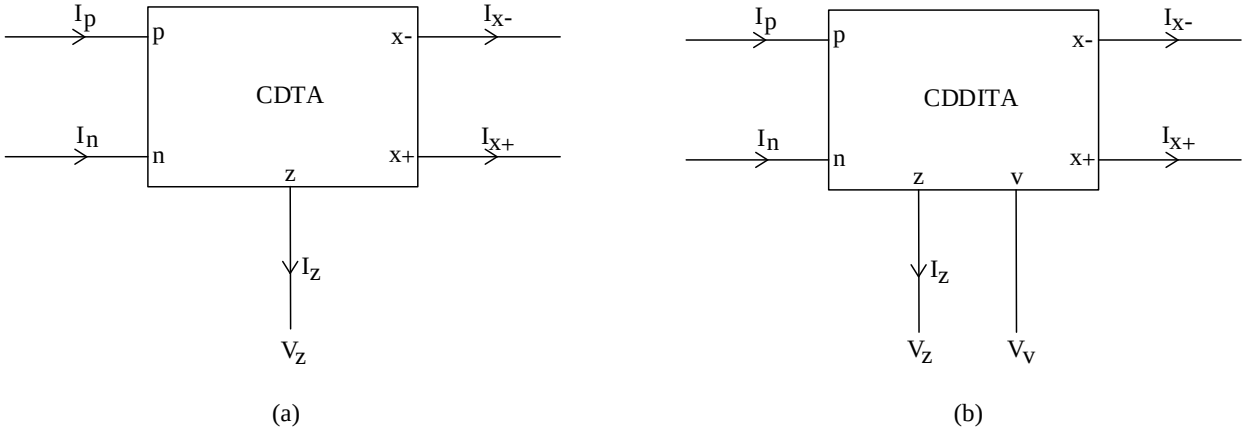


Fig. 2.1 Block diagrams (a) CDTA (b) CD-DITA

CDTA can be viewed as a cascade of current differencing unit (CDU) and an operational transconductance amplifier (OTA). It has two low-impedance terminals p and n. The difference of the currents I_p and I_n at these terminals flow out of the *z*-terminal which, in turn develops a voltage V_z across an external load if connected at *z*-terminal. The OTA block converts this V_z into currents I_{x+} and I_{x-} at $x\pm$ terminal with the gain of g_m. As the input terminals of the CDTA are low impedance nodes, it finds many applications where circuits are insensitive to stray capacitances. This makes CDTA an appropriate choice for high frequency applications. Also in literature this block has been referred as a true CM block since it is a current input current output device. The universality of the CDTA block can be augmented by using the availability and accessibility of differential i/p or o/p OTAs which is the output stage in CDTA. CD-DITA (Current Differencing Differential Input Transconductance Amplifier) is such an example which

is modified version of CDTA and utilizes a differential-i/p OTA instead of a single-i/p OTA employed in the traditional CDTA as shown in Fig 2.1(b). This active element can provide various applications with enthralling features, such as providing the electronic controllability, usage of minimum passive elements and multi-mode operation.

A vast literature is available on CDTA which includes various realization of CDTA [5-15] and wide variety of CDTA based signal processing and generation applications [12-22]. However it is evident from the literature survey that, CD-DITA has a single application, i.e. a VM first-order APF reported in [23]. This work presents the development of new CD-DITA structure and its application in VM-Universal biquad filter therefore a detailed review of reported CDTA architectures has been dealt with in this chapter such that the appropriate structure can be modified to use it as a CD-DITA and apply it in the VM filter application. This work also includes comparison of various VM universal biquads to get the essence of crucial points in designing the required filter.

2.2. Review of CDTA Implementations

Extensive literature review suggests that both bipolar [5-7] and CMOS [8-16] technologies are used for CDTA implementation. One of the CDTA realizations using bipolar technology is reported in [5]. The advantages of these circuits are high overall gain compared to CMOS based implementations. But along with high gain these CDTA structures also produce high power dissipation due to use leakages in BJT. Another bipolar implementation which is an extension of CDTA known as ZC-CDTA is presented in [6]. In this structure an extra *z*-terminal termed as *z*-copy, is included to provide design flexibility. A current controlled CDTA (CCCDTA) based on BJT technology is presented in [7]. In this structure the input voltages of p and n terminals are not zero and therefore these terminals have a finite resistance which can be controlled through bias currents.

Few CMOS technology based CDTA structures have also been reported in literature. One such structure is reported in [8] which have an advantage of high impedance at the *z*-terminal. A low power CMOS realization of the CDTA is reported in [9]. In this structure the input stages are constructed using FVF, due to which this CDTA has very low input resistances. The modification of CDTA in [2.6] known as MO-CDTA is reported in [10] which has advantage of better OTA gain and multiple outputs can be drawn out of CDTA. Another CMOS based CDTA is reported in [11]. This circuit exhibit very low impedance at the inputs and high (typically in

$G\Omega$). A comparison of available CDTA structures in terms of supply voltage, technology and number of transistors, gain, power dissipation and terminal impedances is presented in table 2.1

Table 2.1 Comparison of several CDTA structures

Ref	Technology	Supply Voltage	Bias current	Transconductance gain	Power dissipation	Impedances at p,n and z
[5]	Bipolar	±3V	100 μA	2 mS	-	-
[6]	Bipolar	±2.5V	50 μA	0.96 mS	-	-
[7]	Bipolar	±1.5V	100 μA	-	8.11 mW	
[8]	0.25 μ CMOS	±1.2V	150 μA	624.9 μS	-	-
[9]	0.35 μ CMOS	±0.75V	54 μA	210 μS	0.37 mW	-
[10]	0.35 μ CMOS	±1.5V	100 μA	673 μS	3.61 mW	812 Ω, 348 Ω, 1.08 MΩ
[11]	0.5 μ CMOS	±2.5V	125 μA	670 μS	1.4 mW	654 Ω, 506 Ω, 1GΩ

2.3.Review of voltage mode universal filters

Analog active filter is commonly exploited block for analog signal processing. It finds applications in many fields, such as wireless communications, control systems, signal measurement and instrumentation [24]. The design and synthesis of analog active filter circuits using electronically controllable ABBs, taking several criteria into account, such as minimum number of active and passive elements or others, has been receiving significant attention. Such ABBs provides versatility, convenience and flexibility for analog circuit designer. Recently, the filters namely the universal or multifunction biquadratic filters, performing several functions and having single topology have been receiving significant attention.

One of the most popular universal analog filters topology is a MISO type VM filters. By simply switching on or off the i/p voltages or by doing the same along with their different combinations, various filter functions is realized simultaneously. The selection of inputs is done digitally with the usage of microcontroller or microprocessor.

Several VM-MISO type universal biquadratic filter configurations employing different ABBs have been designed and implemented in past twenty years. Such as CCII [25,26], CCCII [27,28], CCTA [29], DDCC[30,31], OTA[32,33], OTRA [34], DVCC [35,36], FTFN[37], CDBA[38], CFA[27,37], VDTA[39] and VD-DIBA [40]. The comparison of these blocks is listed in table 2.2. The proposed CD-DITA based MISO-VM filter is compared with these filters and its advantages and disadvantages are also discussed in the subsequent chapters.

Table 2.2 Comparison of various VM-MISO universal filters

Ref	**No. of ABB**	**No. of R &C**	**High i/p imped -ance**	**Low o/p imped -ance**	**No matching constraints**	**No need of inverting i/p**	**Electronic tune**	**Grounded C only**
[25]	3	3&3	No	Yes	No	No	No	No
[26]	2	2&2	No	No	Yes	No	No	No
[27]	1	1&2	Yes	No	No	No	Yes	No
[28]	2	0&2	Yes	No	No	Yes	No	No
[32]	3	0&2	Yes	Yes	No	Yes	No	No
[33]	6	0&2	Yes	Yes	No	Yes	Yes	Yes
[38]	2	4&2	No	No	Yes	Yes	Yes	No
[37]	2	3&2	No	No	Yes	No	Yes	No
[30]	2	2&2	No	No	Yes	Yes	Yes	Yes
[31]	3	2&2	No	Yes	Yes	Yes	Yes	Yes
[34]	1	4&4	No	No	Yes	No	Yes	No
[29]	1	2&2	Yes	No	No	Yes	Yes	Yes
[35]	1	2&2	Yes	No	No	No	No	No
[36]	3	4&2	No	Yes	No	No	Yes	Yes
[39]	1	0&2	Yes	No	No	No	Yes	Yes
[40]	1	1&2	Yes	No	No	Yes	Yes	No

Chapter

3. Realization of CDTA

3.1.Introduction

3.1.1. Ideal CDTA

Fig. 3.1(a) shows a simple model of ideal CDTA, it has two current inputs *p* and *n*, z is an intermediate terminal where the difference of currents through p and n flows through. A voltage is developed across z terminal when an outside load is connected to it. This voltage is transferred to two currents by a transconductance g_m that are taken out at current pair (x+ an x-) terminals.

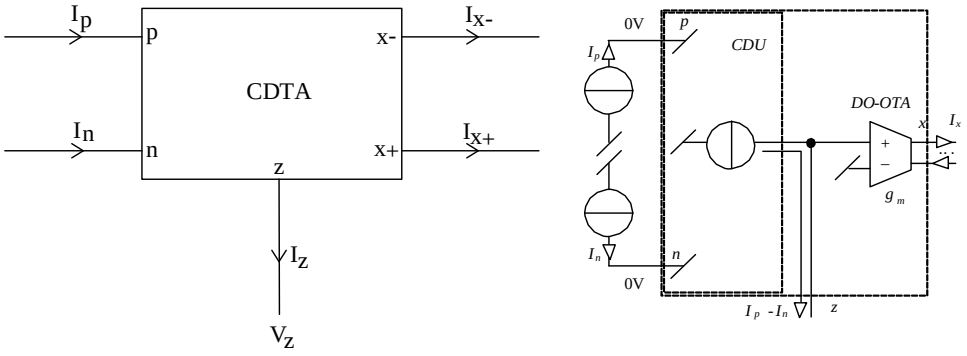


Fig. 3.1 CDTA (a) Schematic symbol (b) Behavioral model

As shown in Fig. 3.1(a), the two output currents from the $\pm x$ terminals, can be extended to n number of current terminals with any of the 3 types of combinations of directions: 1) all currents can flow out, 2) all currents flowing inside CDTA, 3) currents having different directions. Then the current directions can be marked in the circuit symbol by the signs '+' for the currents flowing outside and '–' for currents flowing inside. CDTA can be constructed with an input stage of current differencing unit (CDU) followed by an output stage of operational transconductance amplifier with dual outputs (DO-OTA) as shown in Fig. 3.1(b) [41].

The CDTA element can sense two currents I_p and I_n at its inputs, thus the impedances at these terminals has to be low (ideally zero) and the voltage across these terminals should also be very low (ideally zero). CDTA's outputs are also currents I_{x+} and I_{x-} thus, the impedances seen from these terminals has to be very high (ideally infinite). The current o/p of CDU section I_z is the difference of i/p currents I_p and I_n. The z terminal which is an o/p terminal of CDU

section and also an i/p to DO-OTA stage, acts as an intermediate terminal through which the difference of I_p and I_n flows and is converted into voltage V_z when loaded with an external impedance Z_z. The DO-OTA can be assumed as an ideal VCCS where the difference of i/p voltages is converted to o/p currents via its transconductance g_m, where g_m can be controlled with bias current of DO-OTA. When DO-OTA is used in CDTA, its inverting voltage terminal is grounded the z terminal of CDU section act as a noninverting voltage i/p and this voltage converted to currents I_{x+} and I_{x-}. These are the o/p currents CDTA which flow in opposite direction but, their magnitudes are equal. Following equations depict the behavior of CDTA:

$$V_p = V_n = 0 \tag{3.1}$$

$$I_z = I_p - I_n \tag{3.2}$$

$$I_{x+} = g_m V_z \tag{3.3}$$

$$I_{x-} = -g_m V_z \tag{3.4}$$

Therefore, the overall working of CDTA can be described by following equations matrix:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \tag{3.5}$$

In most of the applications, the *z* terminal of a CDTA element connected by grounded load impedance *Z*. Special signal flow graphs (SFGs) can be used in such circuits for their analysis and synthesis; these are called “IVI” (Current-Voltage-Current) SFGs. As introduced in [42] it is an analogy of the “VIV” (Voltage-Current-Voltage) SFGs. Fig. 3.2(a) shows the “IVI” SFG of CDTA element. As shown in Fig. 3.2(b). SFG can be simplified by removing intermediate voltage node.

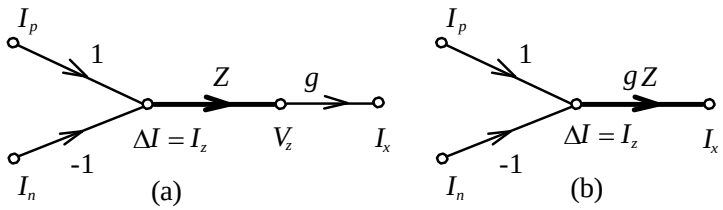


Fig. 3.2 (a) “IVI” SFG of CDTA with z terminal loaded by grounded impedance Z, (b) simplified SFG

3.1.2. Non Ideal CDTA

This section deals with the non-ideal case of CDTA element. It is necessary to consider the active block's non-idealities as the frequency performance of its applications in filter circuit may deviate from its ideal counterpart. These non-ideal conditions on CDTA element result from two effects: the CDTA's finite parasitic resistances and capacitances and error in current transfers. Fig. 3.3 shows the non-ideal CDTA structure as reported in [43].

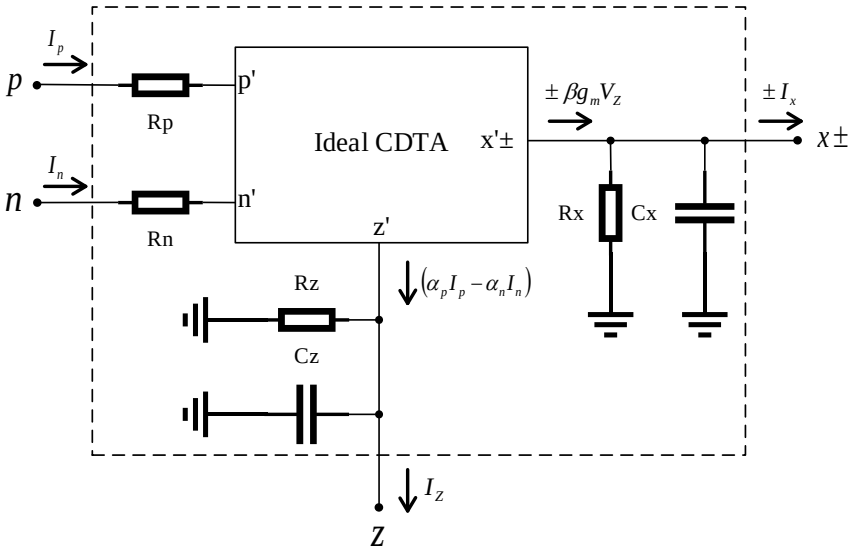


Fig. 3.3 Non ideal CDTA

As shown in the Fig. 3.3, R_p and R_n are floating parasitic resistances at current input terminals p and n, respectively. Shunt parasitic resistances and capacitances R_z, C_z and R_x, C_x are present at the output ports z and $x\pm$, respectively. The unity gain current transfer from p and n terminals to z terminal may deviate from its ideal unity value and these parasitic current gains between $p-z$ and $n-z$ are represented by α_p and α_n. These parasitic gains in CDU, which usually are deflected from their ideal unity value, are due to current-tracking errors in the CDU section of CDTA. These errors has absolute values much lesser than unity and are related to parasitic gains by following equations

$$\alpha_p = 1-\varepsilon_p;\ \alpha_n = 1-\varepsilon_n \text{ and } |\varepsilon_p| << 1;\ |\varepsilon_n| << 1 \tag{3.6}$$

Where ε_p and ε_n are the errors in current tracking in CDU from p to z and n to z terminals, respectively. In the DO-OTA section of CDTA, the error in transconductance gain

from z to $x\pm$ ports can be modeled by βg_m factor. Therefore, in a non-ideal case, the terminal equations of CDTA are modified as follows

$$V_p = V_n = 0 \tag{3.7}$$

$$I_z = \alpha_p I_p - \alpha_n I_n \tag{3.8}$$

$$I_{x+} = \beta g_m V_z \tag{3.9}$$

$$I_{x-} = -\beta g_m V_z \tag{3.10}$$

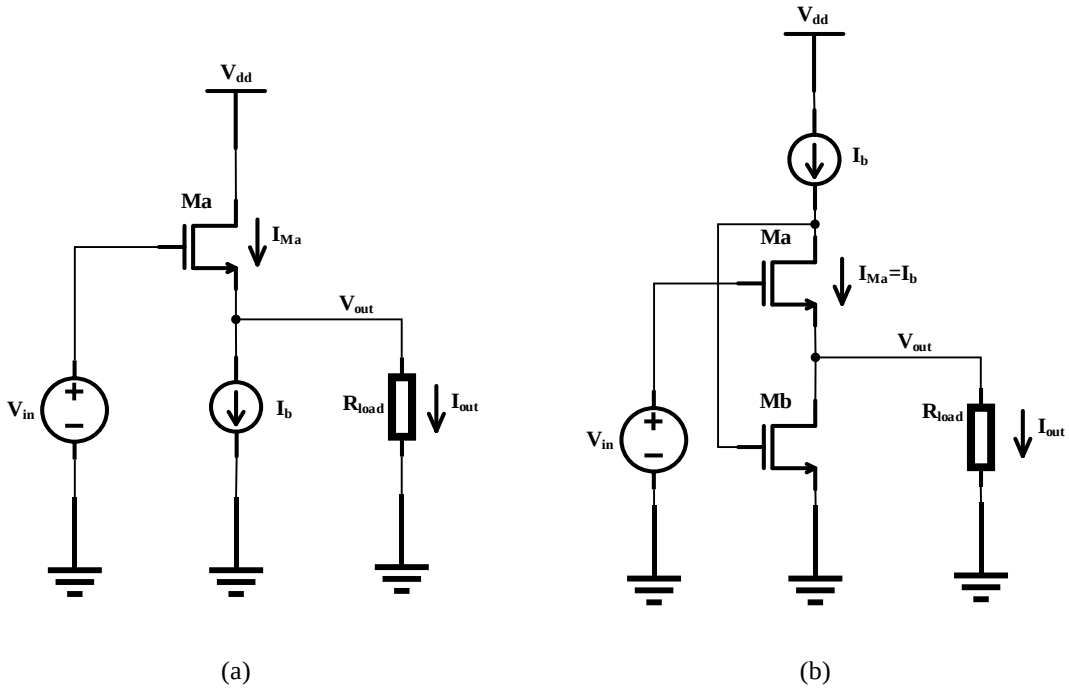
Therefore the Non-ideal CDTA without considering the effects of parasitics, is characterized as:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 \\ 0 & 0 & 0 & \pm\beta g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \tag{3.11}$$

3.2. Realization of FVF based CDTA

3.2.1. Flipped voltage follower

MOS based Common drain (CD) amplifier as shown in Fig. 3.4(a), is one of the most frequently used circuit in ASP for its voltage buffering operation.



(a) (b)

Fig. 3.4 (a) Source Follower, (b) Flipped Voltage Follower

If the body effect of M_a transistor is ignored, then the o/p voltage of the circuit follows i/p voltage with a dc level shift of V_{GS} of M_a. Therefore the relation between i/p and o/p voltages is expressed as

$$V_{out} = V_{in} - V_{GS} \tag{3.12}$$

The DC analysis of this circuit depicts that it can sink huge current to the load, but I_b i.e. biasing current limits its sourcing capability from output node. Another drawback of the CD amplifier circuit is that there is a dependence of o/p current I_{out} on current through M_a transistor I_{Ma}, such that its V_{GS} varies with the variation of transistor current and, hence the voltage gain is not constant and du to the DC shift it is also less than unity. In the case of capacitive loads similar limitations exists but at relatively higher frequencies. The impedance at o/p node is given as:

$$r_{out} = \frac{1}{g_m} \tag{3.13}$$

Where g_m is the transconcductance of M_a. The typical value of r_{out} ranges from $1k\Omega$ to $5k\Omega$

The circuit shown in Fig. 3.4(b) is a negative-shunt-feedback cascade amplifier which also acts as source follower. Here M_a transistor is used for buffering i/p to o/p. Here current through M_a transistor I_{Ma} is kept constant by bias current I_b, making it independent of the o/p current I_{out} and hence V_{GS} of M_a remains constant. Therefore unlike conventional CD amplifier here the variations in I_{out} are absorbed by M_a which is basically a current sensing transistor. Thus the voltage variations at o/p remain low even at higher frequencies. This circuit shows very low impedance at o/p node, due to the transistor M_b which provides shunt feedback. The power consumption of this circuit is very low due to low power supply requirement (almost equal to threshold voltage V_t of M_a). The bias current source in this circuit is connected on drain terminal of M_a rather than the source terminal, therefore this circuit has a name flipped voltage follower (FVF). Unlike conventional CD amplifier, FVF can source large currents due to low impedance at o/p node [44]. The output resistance this circuit is given as:

$$r_{out} = \frac{1}{g_{ma} g_{mb} r_{oa}} \tag{3.14}$$

Where r_{oa}, g_{ma} and g_{mb} are o/p resistance of M_a and transconductance of M_a and M_b respectively. The typical value of r_{out} ranges from 10Ω to 100Ω.

3.2.2. FVF based current mirror

The voltage buffer circuit can be used as a current mirror by modifying it to operate as a current follower. Considering FVF circuit, its o/p can be used as an i/p of the required current mirror, as it shows very low impedance at this node. Thus, this modified FVF can be called as a current sensing cell, thus a name FVF current sensor (FVFCS) is given to this circuit. One such circuit is shown in Fig. 3.5.

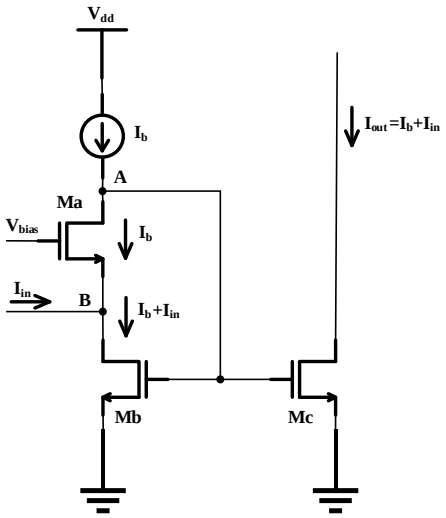


Fig. 3.5 FVF based current mirror

In this circuit, the low impedance node B acts as an i/p current sensing node, the shunt feedback provided by M_b. I/p current signal variations at B are transformed to voltage variations at node A. M_c transistor is used to utilize these variations and produce the copy of i/p current. The o/p and the i/p currents are related through the expression:

$$I_{out} = I_{in} + I_b \tag{3.15}$$

The bias current I_b can be easily eliminated by using current mirroring techniques if it is needed for a specific application. The voltage level required at node A is just V_{DSsat}, which is smaller than the levels required for traditional low-voltage current mirrors. The i/p impedance of this mirror is very low (10Ω-100Ω), the minimum voltage supply required at node A is expressed as:

$V_{dd(\min)} = 2V_{DSsat} - V_t$. Thus this mirror has very low power supply requirements.

3.2.3. Current differencing unit

As shown in Fig. 3.6, CDU can be realized using FVFCS [9], where transistors M_1-M_3 and M_4-M_6 form two FVF based current mirrors and transistor pairs M_7 and M_8 are used to realize simple current mirror. Both FVF based mirrors are biased with same current I_b, therefore the currents through M_1 and M_6 transistors will be equal to I_b.

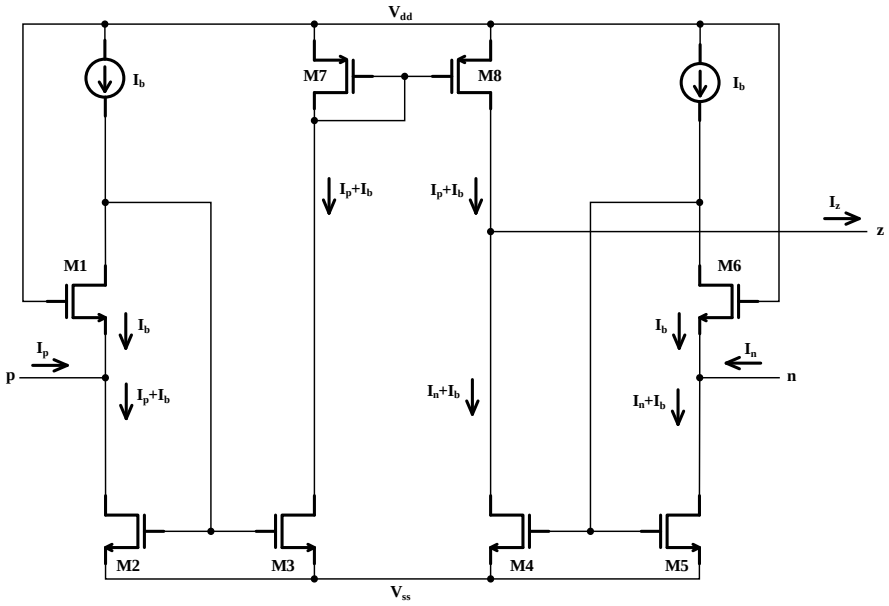


Fig. 3.6 FVF based CDU

The i/p currents I_p and I_n are applied at p and n terminals of CDU respectively. Therefore the currents through M_2 and M_5 may be expressed as

$$I_{M2} = I_p + I_b \tag{3.16}$$

$$I_{M5} = I_n + I_b \tag{3.17}$$

The current through M_2 and M_5 will be mirrored into M_3 and M_4 respectively. The current through M_3 is further mirrored into M_8 by simple mirror. Therefore, the currents through M_8 and M_4 may be expressed as

$$I_{M8} = I_p + I_b \tag{3.18}$$

$$I_{M4} = I_n + I_b \tag{3.19}$$

This difference of currents through M_8 and M_4 is either sourced or sunk by z terminal and may be expressed as

$$I_z = I_p - I_n \tag{3.20}$$

Therefore, z terminal can be considered as o/p terminal of CDU and thus the current differencing operation is realized. External impedance is added at z terminal of CDU when used in CDTA to convert I_z into voltage drop V_z. This voltage drop is further used as an i/p in a DO-OTA section.

3.2.4. Dual output OTA (DO-OTA)

As shown in Fig. 3.7, DO-OTA block is realized with a differential pair amplifier using M_9 and M_{10} which is biased through current I_b; along with few PMOS and NMOS based simple current mirrors for obtaining dual current outputs.

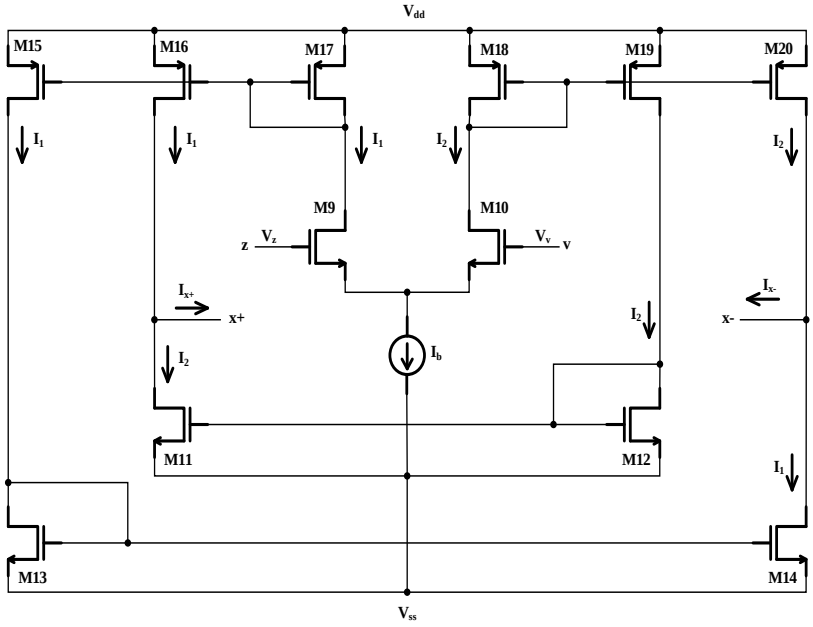


Fig. 3.7 DO-OTA [45]

The i/p voltages V_z and V_v are applied at z and v (voltage)terminals respectively. These voltages produce currents I_1 and I_2 through M_9 and M_{10} respectively. When I_1 is mirrored using M_{16} and M_{17} along with the mirroring of I_2 using M_{11}, M_{12}, M_{18} and M_{19}, a positive difference of I_1 and I_2 can be obtained by taking an o/p terminal $x+$. Thus the current through this terminal may be expressed as

$$I_{x+} = I_1 - I_2 \tag{3.21}$$

When I_2 is mirrored using M_{18} and M_{20} along with the mirroring of I_1 using M_{13}, M_{14}, M_{15} and M_{17}, a negative difference of I_1 and I_2 can be obtained by taking an o/p terminal $x-$. Thus the current through this terminal may be expressed as

$$I_{x-} = -(I_1 - I_2) \tag{3.22}$$

Thus, dual o/p currents can be obtained when differential input voltage $(V_z - V_v)$ is applied. The o/p currents are related to differential input by the transconductance gain g_m of DO-OTA and these currents may be expressed as

$$I_{x\pm} = \pm(I_1 - I_2) = \pm g_m(V_z - V_v) \tag{3.23}$$

Where g_m is expressed as

$$g_m = \sqrt{I_b\left[\mu_n C_{ox}\left(\frac{W}{L}\right)\right]_{M9,M10}} \tag{3.24}$$

Where the parameters $\mu_n, C_{ox}, \frac{W}{L}$ are of differential pair transistors M_9 or M_{10}. Consequently, g_m can be varied by bias current I_b.

When DO-OTA is clubbed with CDU to realize CDTA, z terminal of DO-OTA block is driven by z terminal of CDU and the v terminal is grounded. The complete schematic of FVF based CDTA block is shown in Fig. 3.8 which consists of CDU followed by DO-OTA block. The aspect ratios of transistors used in CDTA implementation are listed in table 3.1

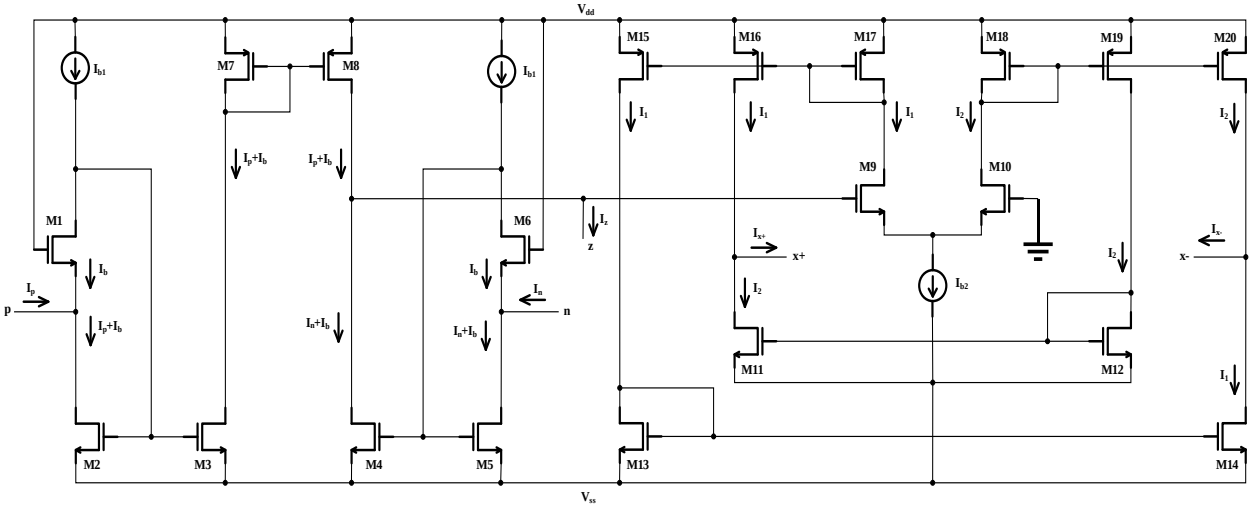


Fig. 3.8 FVF based CDTA

Table 3.1 Aspect ratios of transistors for FVF based CDTA

Transistors	W (μm)	L (μm)
$M_1 - M_8$	24	1
M_9, M_{10}	8	1
$M_{11} - M_{14}$	5	1
$M_{15} - M_{20}$	8	1

3.3. Characterization of CDTA

The CMOS realization of FVF based CDTA block as shown in Fig 3.8 is simulated using PSPICE simulations with 0.25um process parameters. The power supply rails are $\pm 1.2V$. The CDTA is characterized for its large signal (DC response) and small signal (Frequency response) behavior.

3.3.1. Large signal analysis (DC characteristics)

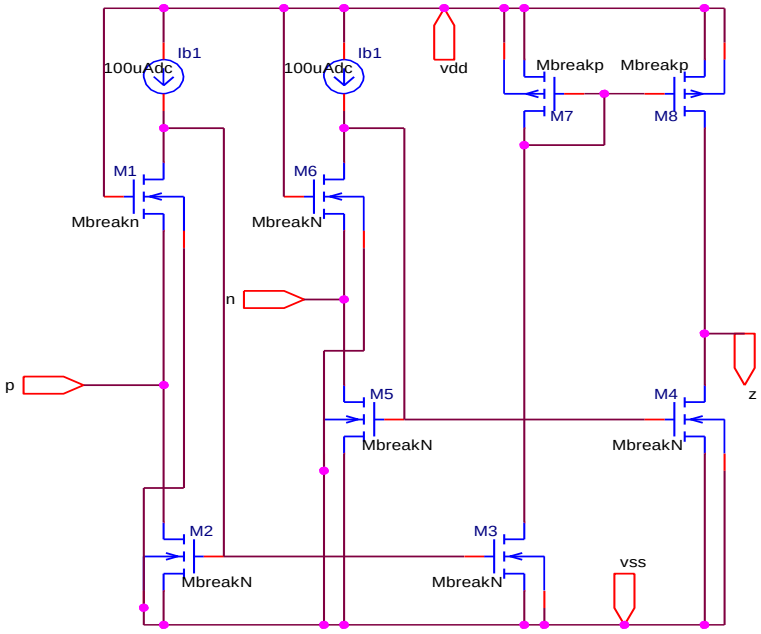


Fig. 3.9 PSPICE schematic of CDU

The PSPICE schematic of CDU is shown in Fig. 3.9. Bias current I_{b1} is chosen as $100\mu A$ .To verify the current dynamic range at i/p terminals p and n along with the verification of current tracking from p to z and n to z, DC curves I_z vs I_p (with $I_n = 0$) and I_z vs I_n (with $I_p = 0$

)respectively, are plotted as shown in Fig. 3.10 and 3.11. To obtain these plots, current at z terminal I_z is varied from $-100\mu A$ to $100\mu A$.

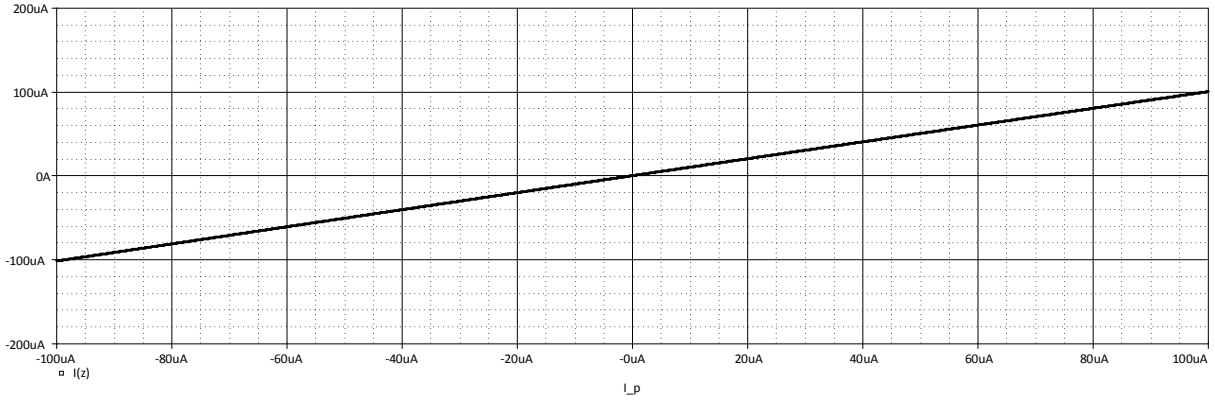


Fig. 3.10 Current transfer from p -terminal to z -terminal with $I_n = 0$ (I_z vs I_p)

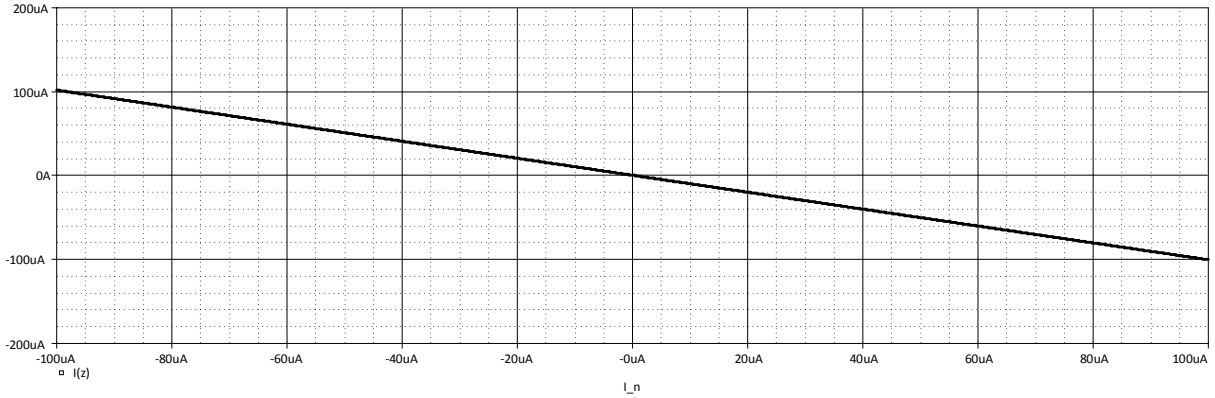


Fig. 3.11 Current transfer from n -terminal to z -terminal with $I_p = 0$ (I_z vs I_n)

The DC curves in Fig. 3.12 show variation of n terminal current I_n on I_z vs I_p plot, similarly Fig. 3.13 show variation of p terminal current I_p on I_z vs I_n plot. To obtain these plots current at z terminal I_z is varied from $-100\mu A$ to $100\mu A$ with a parametric sweep of I_p or I_n ranging from $-60\mu A$ to $60\mu A$ with $30\mu A$ interval.

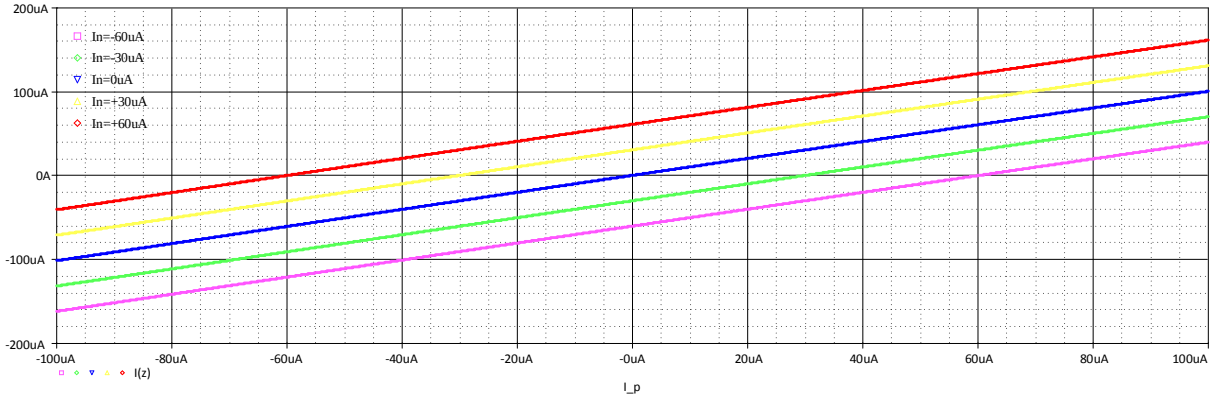


Fig. 3.12 Current transfer from p -terminal to z -terminal with I_n as parametric sweep (I_z vs I_p)

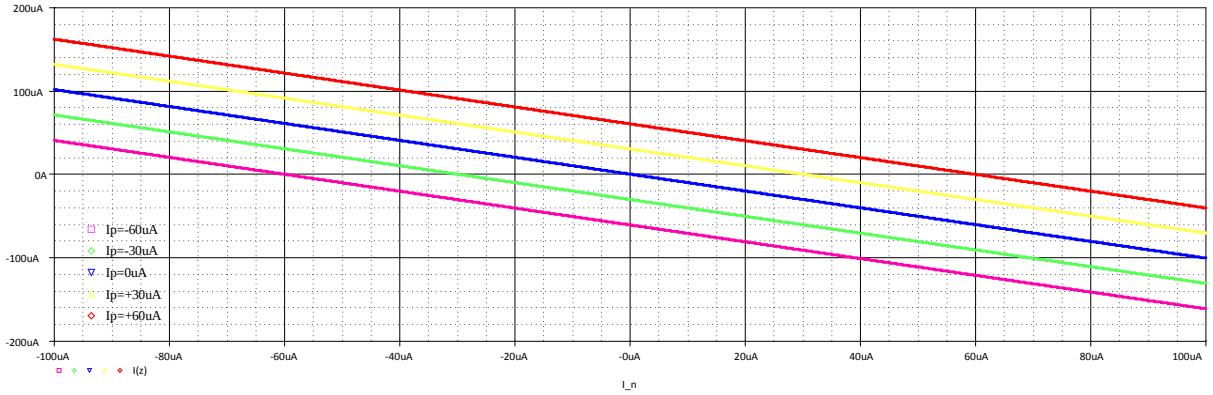


Fig. 3.13 Current transfer from n -terminal to z -terminal with I_p as parametric sweep (I_z vs I_n)

From the PSPICE simulations of CDU, it can be concluded that i/p-o/p characteristics remain linear for the dynamic range $-100\mu A$ to $100\mu A$ which can be theoretically confirmed by bias currents I_{b1} which limits dynamic range of CDU.

The PSPICE schematic of DO-OTA block is shown in Fig. 3.14. Bias current I_{b2} is chosen as $100\mu A$. To verify the voltage dynamic range at i/p terminal z along with the verification of trasnconductance transfer from z to $x\pm$ terminals, DC curves $I_{x\pm}$ vs V_z is plotted as shown in Fig. 3.15. To obtain these plots voltage at z terminal V_z is varied from $-1.2V$ to $1.2V$

.

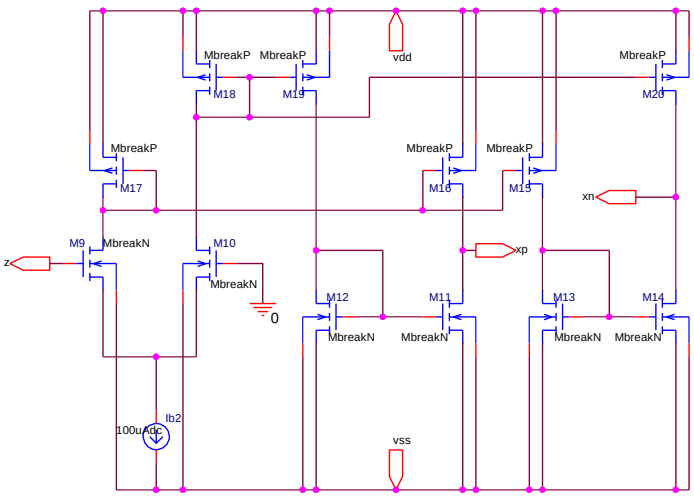


Fig. 3.14 PSPICE schematic of DO-OTA

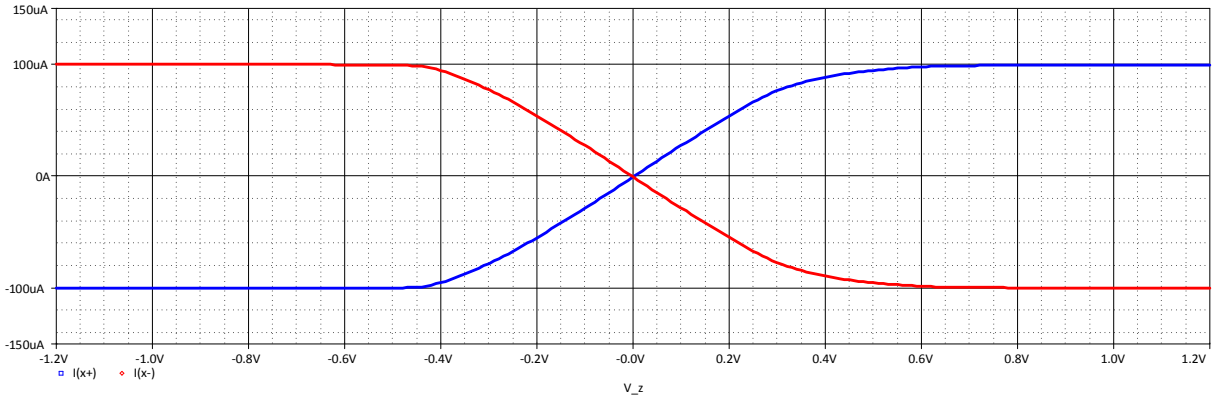


Fig. 3.15 Transconductance transfer from z -terminal to $x\pm$ terminals with $I_{b2}=100\mu A$ ($I_{x\pm}$ vs V_z)

The DC curves in Fig. 3.16 show variation of bias current I_{b2} on $I_{x\pm}$ vs V_z plot. To obtain these plots, V_z is varied from $-1.2V$ to $1.2V$ with a parametric sweep of I_{b2} with values $20\mu A$, $40\mu A$, $80\mu A$ and $100\mu A$.

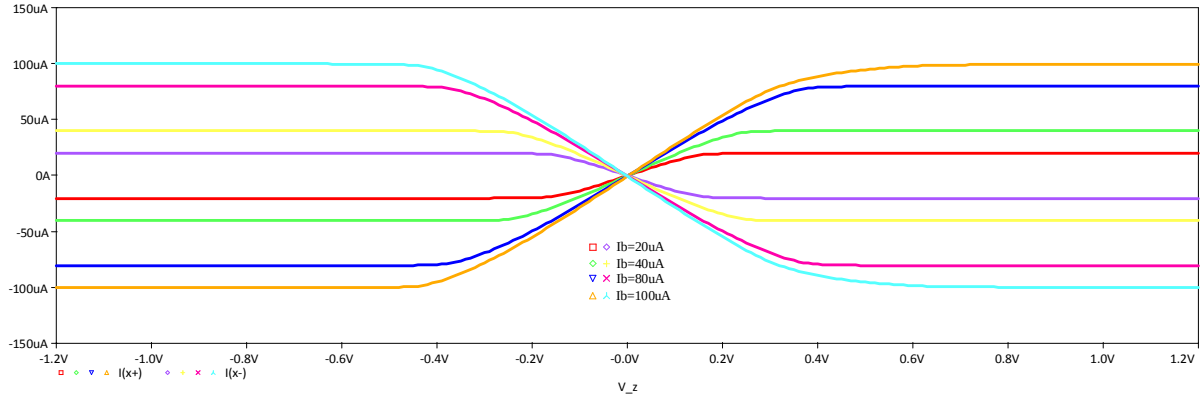


Fig. 3.16 Transconductance transfer from z -terminal to $x\pm$ terminals with I_{b2} as parametric sweep ($I_{x\pm}$ vs V_z)

From the PSPICE simulations of DO-OTA, it can be concluded that i/p-o/p characteristics remain linear for the i/p dynamic range $-300mV$ to $300mV$ which is limited by bias current I_{b2} of DO-OTA. CDU and DO-OTA blocks are cascaded to form CDTA block. The PSPICE schematic of CDTA is shown in Fig. 3.17. Bias current I_{b1} and I_{b2} are chosen as $100\mu A$.

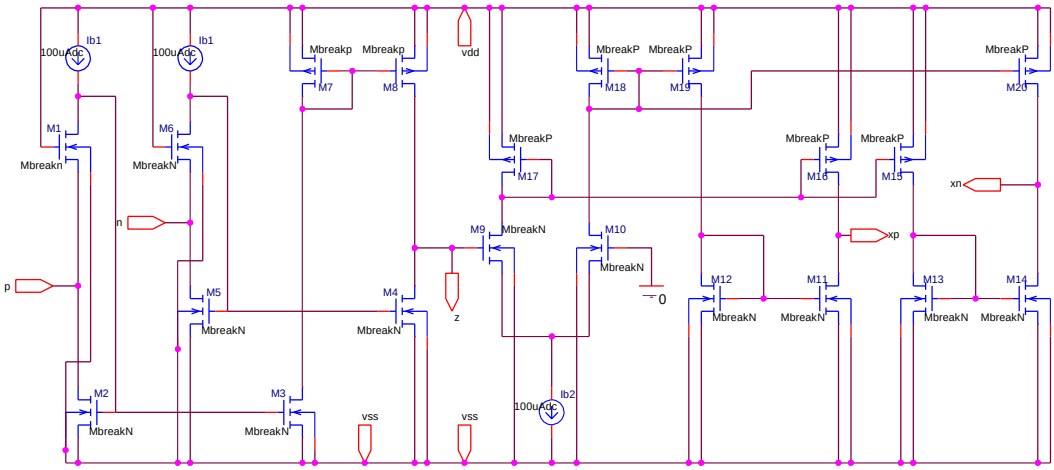


Fig. 3.17 PSPICE schematic of CDTA block

To verify the unity current gain transfer from p terminal to $x\pm$ terminal, DC curves I_{x+} vs I_p with varying external resistance R_z at z -terminal is plotted. The DC curves in Fig. 3.18 show variation of external resistance R_z at z terminal on I_{x+} vs I_p plot. To obtain these plots, current at p terminal I_p is varied from $-60\mu A$ to $60\mu A$ with a parametric sweep of R_z with values $1k\Omega, 3k\Omega, 5k\Omega$ & $7k\Omega$. From these plots the value of R_z to obtain unity gain of CDTA comes out to be $3.55k\Omega$ which is verified from I_{x+} vs I_p graph, plotted at $R_z = 3.55k\Omega$ as shown in Fig. 3.19.

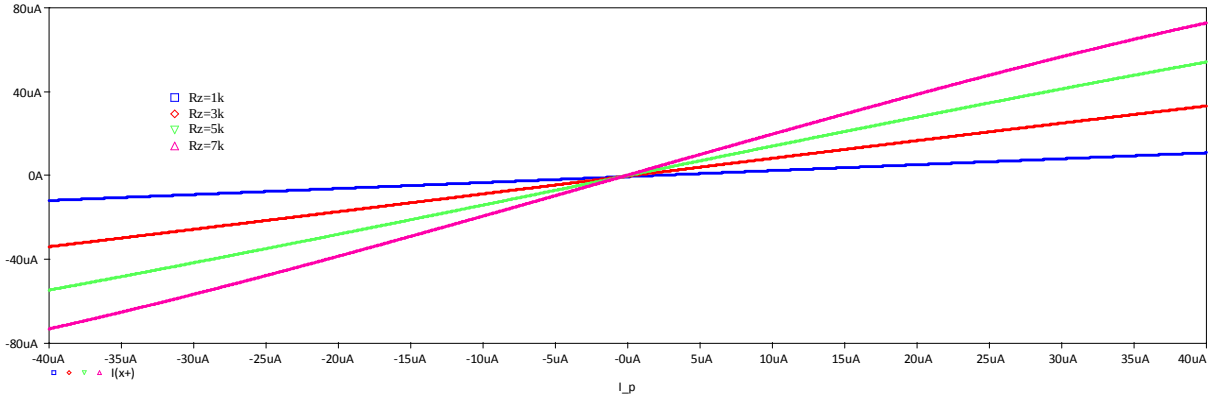


Fig. 3.18 Current transfers from p terminal to $x+$ terminal with $I_n = 0$ & R_z as parametric sweep (I_{x+} vs I_p)

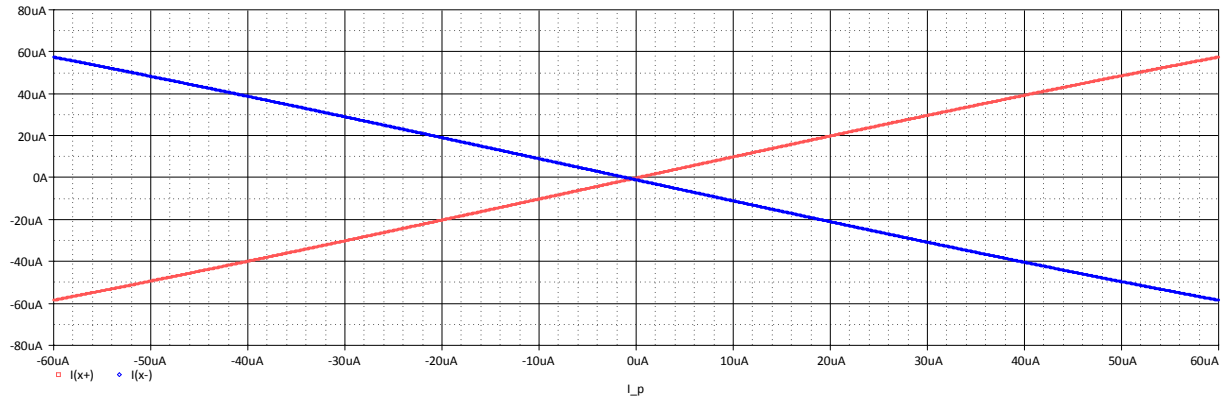


Fig. 3.19 Current transfers from p terminal to $x\pm$ terminal with $I_n = 0$ and $R_z = 3.55k\Omega$ ($I_{x\pm}$ vs I_p)

The DC curves in Fig. 3.20 show variation of bias current I_{b2} on I_{x+} vs I_p plot with $I_n = 0$ and $R_z = 3.55k\Omega$. To obtain these plots, I_p is varied from $-50\mu A$ to $50\mu A$ with a parametric sweep of I_{b2} with values $50\mu A, 100\mu A, 150\mu A$ and $200\mu A$.

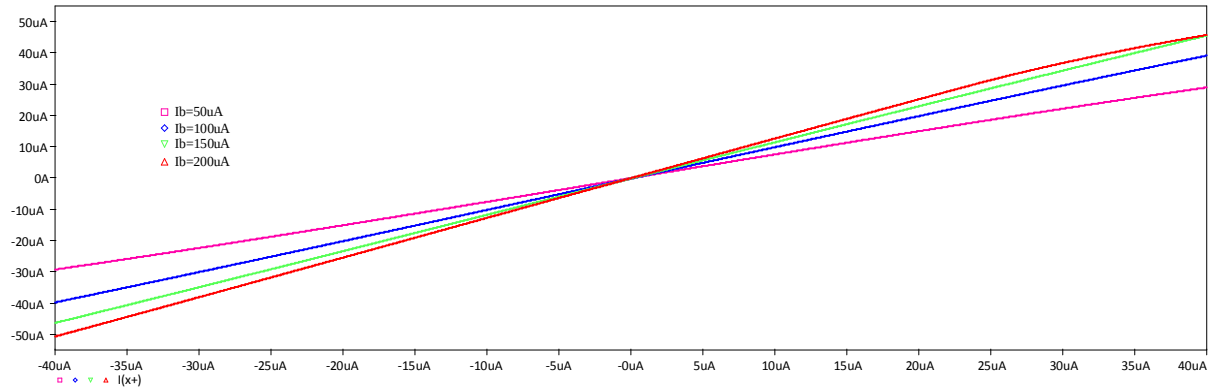


Fig. 3.20 Current transfers from p terminal to $x+$ terminal with $I_n = 0$, $R_z = 3.55k\Omega$ and I_{b2} as parametric sweep ($I_{x\pm}$ vs I_p)

3.3.2. Small signal analysis (AC characteristics)

For AC characterization, AC signals are applied as inputs to simulated by plotting frequency responses of its outputs. Bias current I_{b1} and I_{b2} are chosen as $100\mu A$. The frequency response of I_z/I_p is shown in Fig. 3.21 from which the parasitic gain α_p and current tracking error ε_p from p terminal to z terminal and its bandwidth are measured and found to be:

$$\alpha_p = \frac{I_z}{I_p} = 108.42mdB = 1.012 \qquad (3.25)$$

$$\therefore \varepsilon_p = 1 - \alpha_p = -0.012 \tag{3.26}$$

$$\text{B.W.} = 197.246MHz \tag{3.27}$$

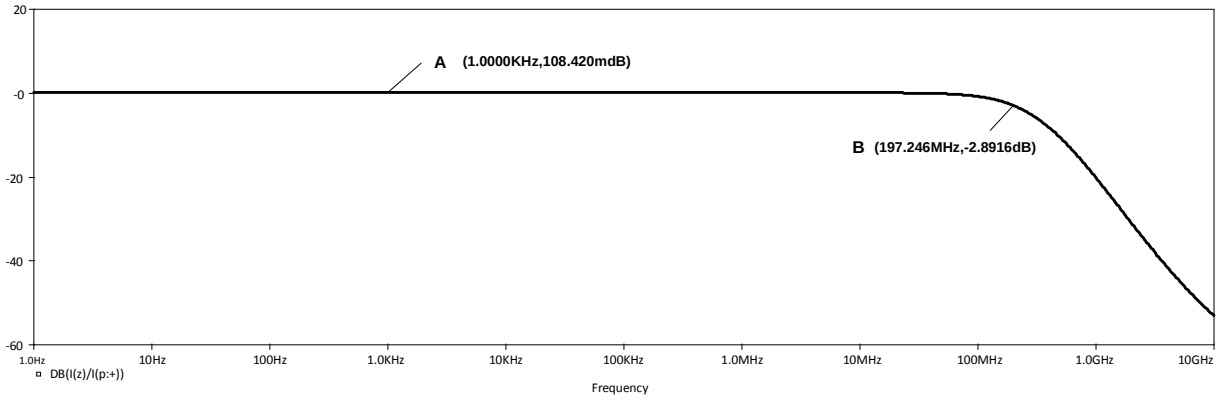


Fig. 3.21 Parasitic Current gain from p terminal to z terminal with $I_n = 0$ (I_z / I_p vs frequency)

Similarly parasitic gain, current tracking error from n terminal to z terminal and bandwidth from frequency response of I_z / I_n (as shown in Fig. 3.22) is measured and found to be:

$$\alpha_n = \frac{I_z}{I_n} = 118.516mdB = 1.013 \tag{3.28}$$

$$\therefore \varepsilon_n = 1 - \alpha_n = -0.013 \tag{3.29}$$

$$\text{B.W.} = 374.81MHz \tag{3.30}$$

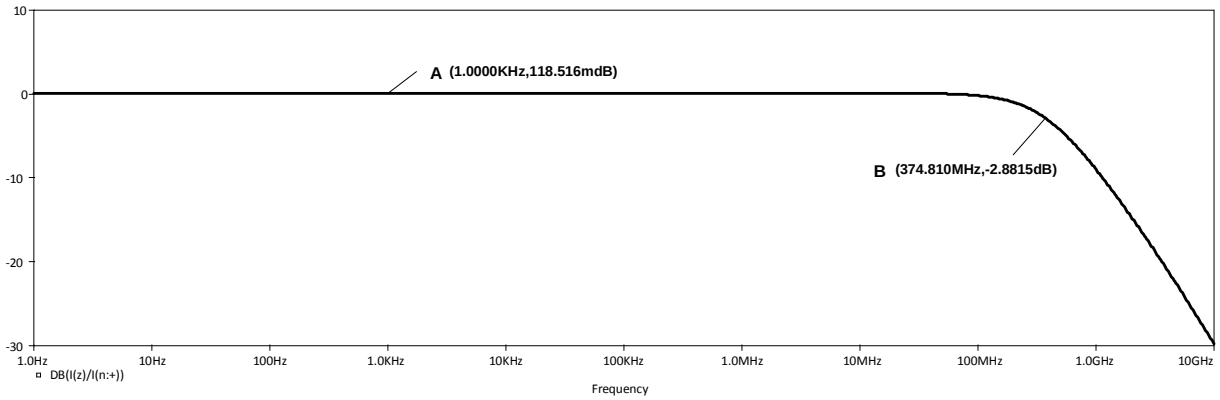


Fig 3.22 Parasitic Current gain from n terminal to z terminal with $I_p = 0$ (I_z / I_n vs frequency)

Fig. 3.23 shows the simulated frequency response of transconductance gain g_m from z - terminal to $x\pm$ terminals. The transconductance gain and its bandwidth is measured for $I_{b2} = 100\mu A$ and can found out from points A and B as:

$$g_m = -71.004dB = 281.708\,\mu A/V \tag{3.31}$$

$$\text{B.W.} = 236.323MHz \tag{3.32}$$

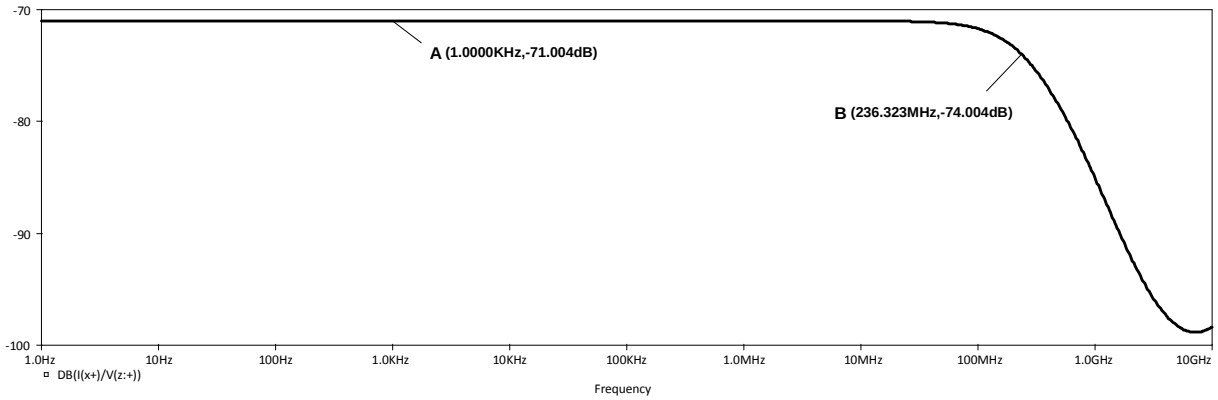


Fig. 3.23 Transconductance gain g_m from z -terminal to $x\pm$ terminals with $I_{b2} = 100\mu A$ (I_{x+}/V_z vs frequency)

Fig. 3.24 shows the simulated frequency response of transconductance gain by varying bias current I_{b2} with values $20\mu A, 40\mu A, 80\mu A$ and $100\mu A$, the transconductance gain obtained are $213.176\,\mu A/V$, $281.709\,\mu A/V$, $325.914\,\mu A/V$ and $356.184\,\mu A/V$ respectively.

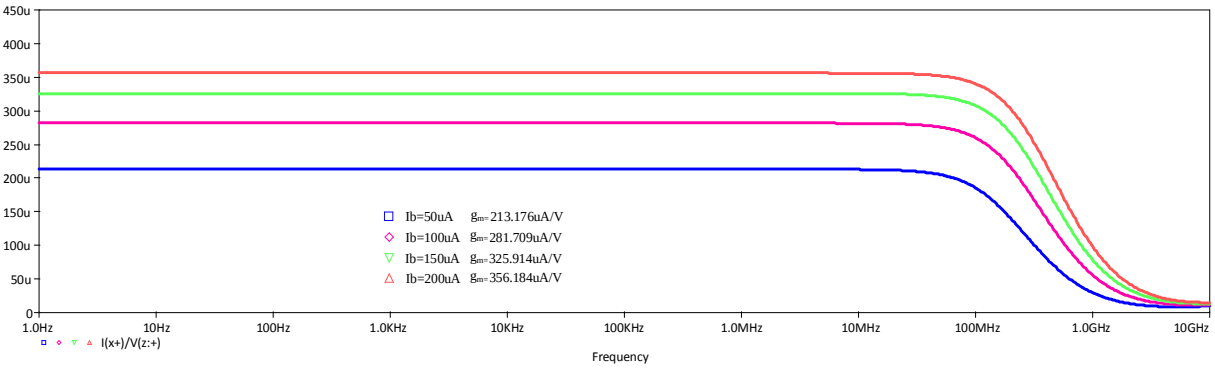


Fig. 3.24 Transconductance gain g_m from z -terminal to $x+$ terminals with I_{b2} as parametric sweep (I_{x+}/V_z vs frequency)

Fig. 3.25 shows the simulated frequency response of total gain of CDTA from p terminal to $x+$ terminal with $I_{b2} = 100\mu A$ ($g_m = 281.709\,\mu A/V$)and $R_z = 17.74k\Omega$ which theoretically gives the gain($g_m R_z$) of 5 or $14dB$. Thus, CDTA's gain and bandwidth can found out from points A and B as:

$$\text{Gain} = 13.729dB \tag{3.33}$$

$$\text{B.W.} = 83.66MHz \tag{3.34}$$

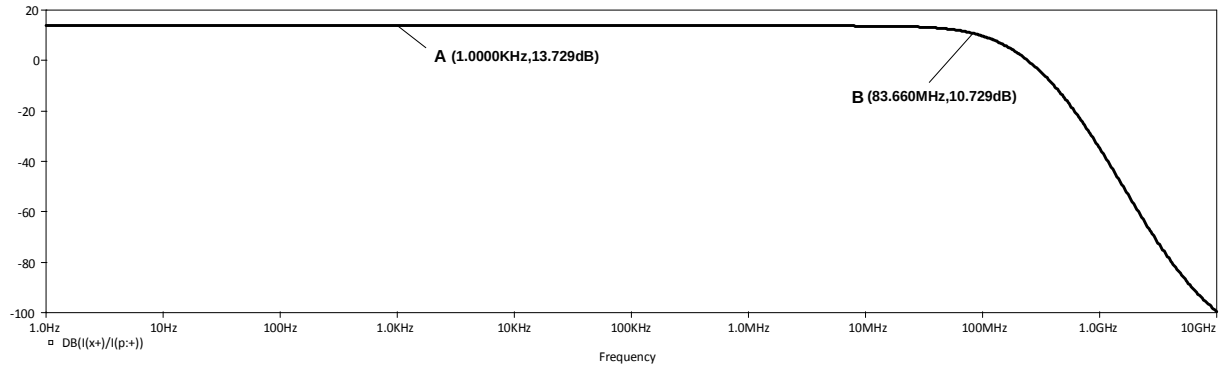


Fig. 3.25 Gain of CDTA from p terminal to $x+$ terminal with $I_n = 0$, $I_{b2} = 100\mu A$ and $R_z = 17.74k\Omega$ (I_{x+}/I_p vs frequency)

Similarly CDTA's gain and bandwidth from n terminal to $x+$ terminal can found out using points A and B respectively from I_{x+}/I_p vs frequency plot as

$$\text{Gain} = 13.741dB \tag{3.35}$$

$$\text{B.W.} = 92.118MHz \tag{3.36}$$

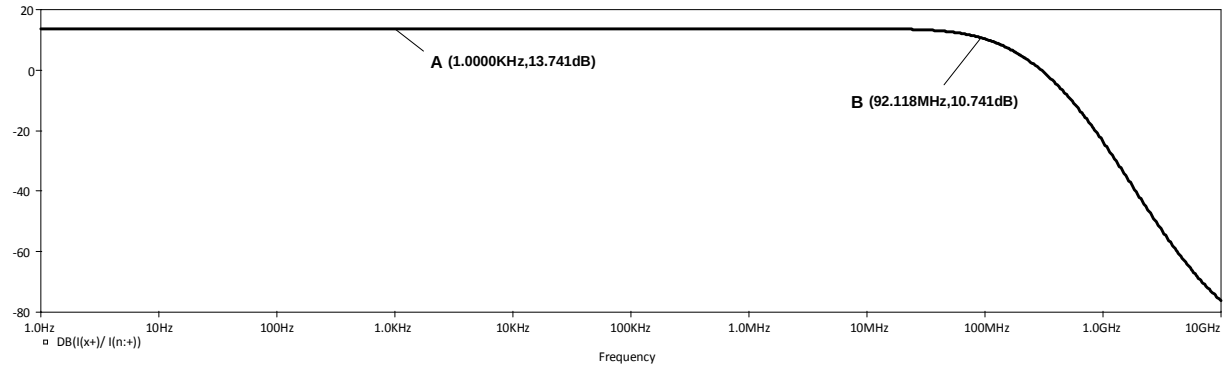


Fig. 3.26 Gain of CDTA from n terminal to $x+$ terminal with $I_p = 0$, $I_{b2} = 100\mu A$ and $R_z = 17.74k\Omega$ (I_{x+}/I_n vs frequency)

To measure impedance at i/p and o/p terminals other terminals are kept open and a test AC input signal is applied to the terminal at which the impedance is required. Then the ratio of voltage and current of this test signal is plotted w.r.t. to frequency.

From the Fig. 3.27 and Fig. 3.28, the impedances seen through p and n terminals are found out to be very low and equal as they are required to be, theoretically. The values of these impedances measured using point A from their corresponding frequency responses are as follows

$$Z_p = Z_n = 35.105\Omega \tag{3.37}$$

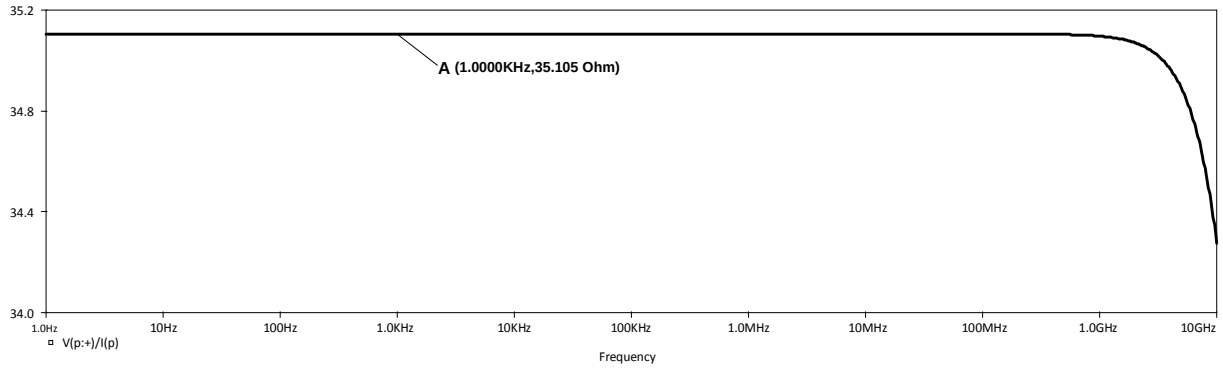


Fig. 3.27 Impedance seen through p -terminal (Z_p vs frequency)

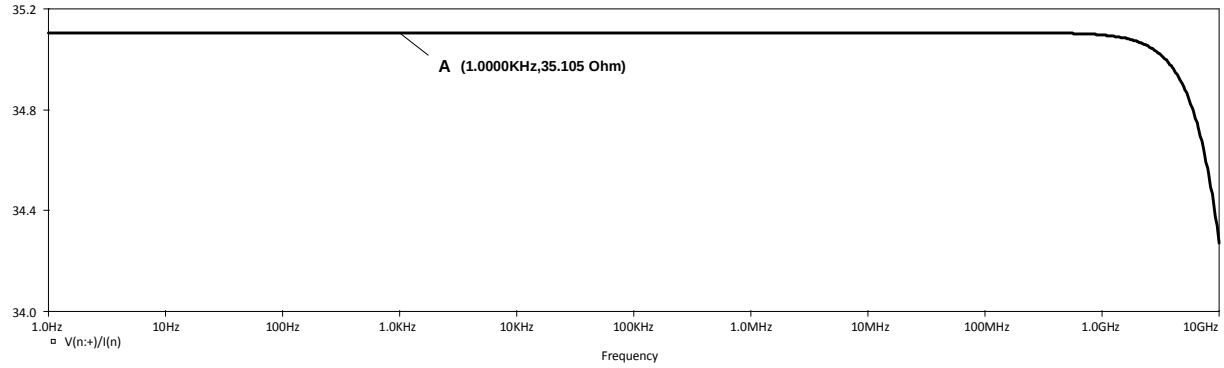


Fig. 3.28 Impedance seen through n -terminal (Z_n vs frequency)

From the Fig. 3.29 and Fig. 3.30, the impedances seen through z and $x\pm$ terminals are found out to be very high as they are required to be, theoretically because these o/p current terminals are high impedance terminals. The values of these impedances measured using point A from their corresponding frequency responses are as follows

$$Z_z = 411.274k\Omega \tag{3.38}$$

$$Z_{x\pm} = 971.48k\Omega \tag{3.39}$$

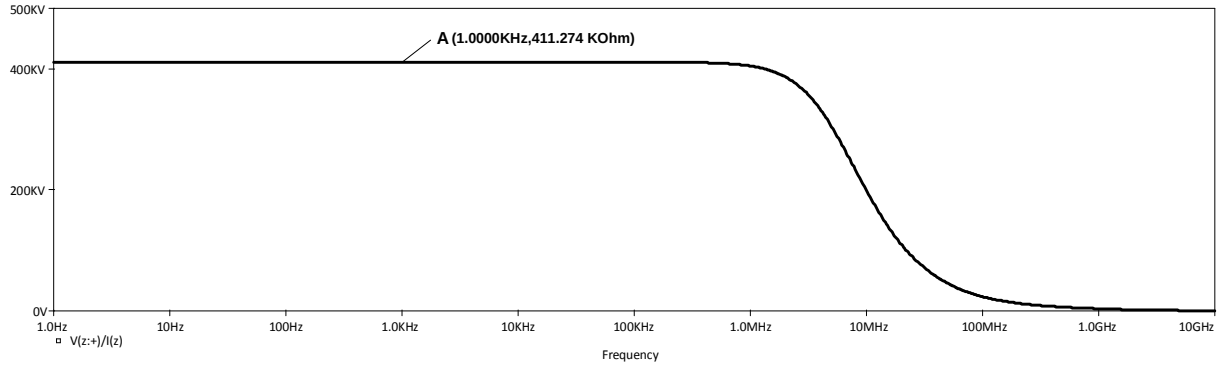


Fig. 3.29 Impedance seen through z -terminal (Z_z vs frequency)

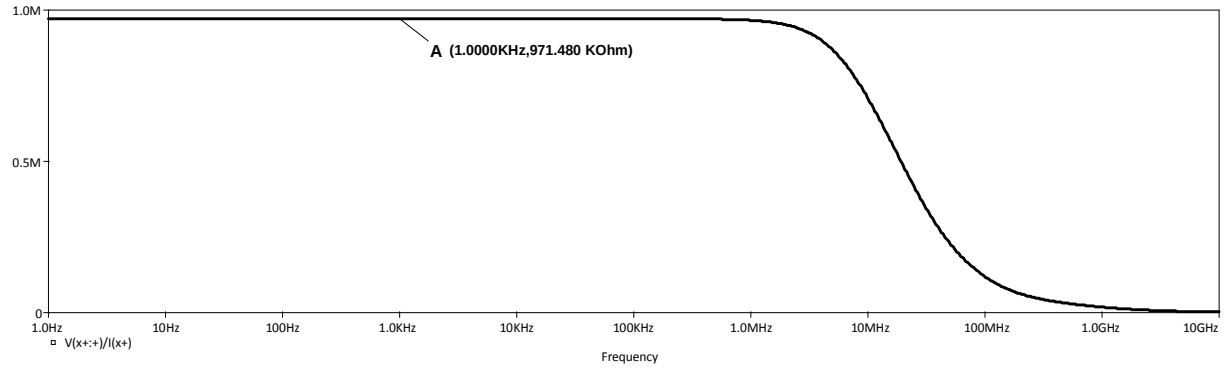


Fig. 3.30 Impedance seen through $x\pm$ terminal ($Z_{x\pm}$ vs frequency)

The simulated total power dissipation of the FVF based CDTA block comes out to be 1.57 milli watts. The summary of AC and DC performance parameters of CDTA are listed in Table 3.2.

Table 3.2 Performance parameters of CDTA

Parameter	**Value**	**Condition**
Power supplies	$\pm 1.2V$	-
Process parameters	TSMC $0.25\mu m$	-
Input current dynamic range (I_p and I_n)	$-100\mu A$ to $100\mu A$	$I_{b1} = I_{b2} = 100\mu A$
Input voltage dynamic range(V_z)	$-300mV$ to $300mV$	-
Parasitic gains(α_p, α_n)	$1.012, 1.013$	z terminal grounded
Bandwidth (I_z/I_p , I_z/I_n)	$197.246MHz$, $374.81MHz$	z terminal grounded
Transconductance gain(g_m)	$281.708\,\mu A/V$	$x\pm$ terminals grounded
Bandwidth(I_{x+}/V_z)	$236.323MHz$	$x\pm$ terminals grounded
Overall Gain ($g_m R_z$)(from p , n)	$13.729dB$, $13.741dB$	$R_z = 17.74k\Omega$ for $14dB$ gain
Bandwidth(I_{x+}/I_p , I_{x+}/I_n)	$83.66MHz$, $92.118MHz$	$R_z = 17.74k\Omega$ for $14dB$ gain
Input impedances at p and n (Z_p, Z_n)	35.105Ω	z and $x\pm$ terminals open circuit
Output impedances at z (Z_z)	$411.274k\Omega$	p , n and $x\pm$ terminals open circuit

Output impedances at $x\pm$ ($Z_{x\pm}$)	$971.48k\Omega$	p, n and z terminals open circuit
Static Power dissipation	$1.57mW$	$I_p = I_n = 0A$, z and $x\pm$ terminals open circuit

Chapter

4. CDTA based applications

4.1. Basic building blocks

In this chapter few basic circuit applications of CDTA such as simple current amplifier, adder, subtractor and lossless integrator are implemented. This is followed by implementation of CM-Schmitt Trigger and CM-KHN filter. The working of these circuits is validated using FVF based CDTA through PSPICE simulation. The theoretical and the observed results are found to be in close agreement hence verifying the functionality of CDTA based applications.

4.1.1. Simple current mirror

CDTA can function as a simple CM amplifier as shown in Fig. 4.1.The i/p signal is applied to the terminal *p* and o/p is taken from either $x+$ or $x-$ terminal depending upon the required o/p (inverting or non-inverting). The gain is obtained from the total gain of CDTA $(g_m R_z)$

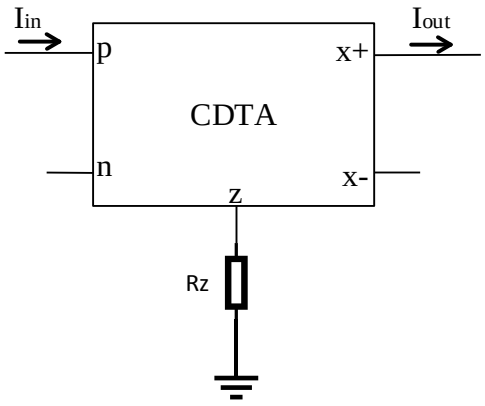


Fig. 4.1 Circuit Schematic of Simple current amplifier based on CDTA.

The o/p current is expressed as

$$I_{out} = I_{x\pm} = \pm g_m R_z I_{in} \qquad (4.1)$$

For PSPICE simulations the bias current I_b of DO-OTA section of CDTA is set to $100\mu A$, which leads to $g_m = 281.324\,\mu A/V$. To obtain a gain of 2 or 6.0023dB R_z is set to the value of $7k\Omega$.To obtain a transient response, a sinusoidal current signal is applied as an i/p having range from $-30\mu A$ to $+30\mu A$. Its frequency is fixed to $10kHz$. As shown in Fig. 4.2 transient analysis result

shows the amplified output and its gain and 3dB bandwidth are obtained from points A and B in frequency response as shown in Fig. 4.3. Therefore,

$$Gain = 5.98dB \text{ and } B.W. \approx 61MHz \quad (4.2)$$

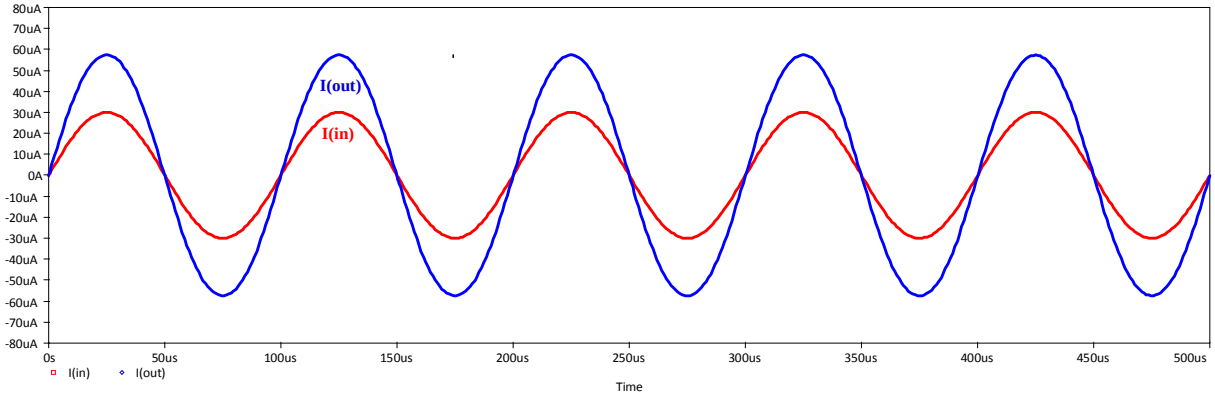


Fig. 4.2 Simulated o/p waveform of simple current amplifier corresponding to sinusoidal i/p

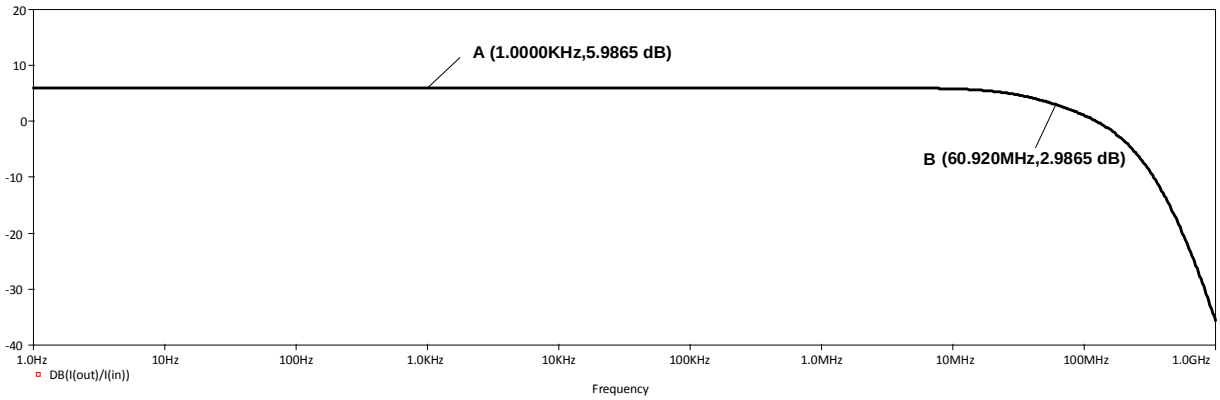


Fig. 4.3 Simulated frequency response of a simple current amplifier

4.1.2. Adder or summing amplifier

Summing amplifiers a.k.a. mixers are the most useful circuits in analog domain. These circuits are used for both ac and dc voltage/current signals processing. These circuits provide an o/p voltage or current proportional to or equal to the sum of multiple i/p's. As these circuits are implemented using at least one active block, the output can be amplified by constant gain along with the summation of each i/p. For the designing of summing voltage signals op-amp circuits are the first choice of any designer. Its current counterpart can be implemented by any CM-ABB. In this work, for the designing of summing amplifier a single CDTA is used and the two inputs

are applied at the positive terminal as shown in Fig. 4.4. The gain of this circuit is obtained by the gain of CDTA i.e. $(g_m R_z)$

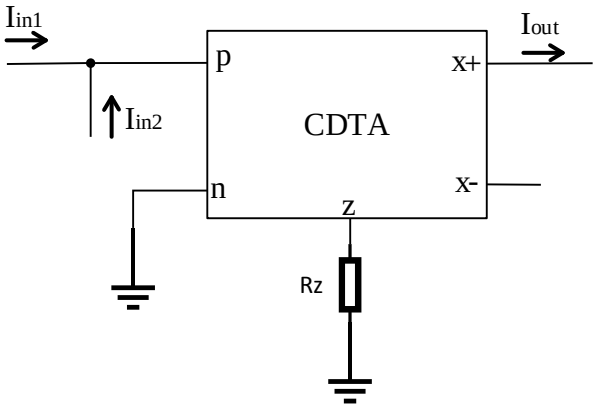


Fig. 4.4 Circuit Schematic of a summing amplifier based on CDTA.

The o/p current of the circuit is expressed as

$$I_{out} = I_x = g_m R_z \left(I_{in1} + I_{in2}\right) \tag{4.3}$$

For PSPICE simulations, the setup is same as used in current amplifier except for the value of R_z. Here, to obtain a gain of 1 or 0dB R_z is set to the value of $3.55k\Omega$.For transient analysis, two sinusoidal current signals are applied one with the range of $\pm 30\mu A$ and another with $\pm 20\mu A$. As shown in Fig. 4.5 transient analysis result shows the output which is the summation of 2 i/p's. Its gain can be adjusted using g_m or R_z which give amplification along with summation at the o/p. The gain and 3dB bandwidth are obtained from points A and B in frequency response as shown in Fig. 4.6. Therefore,

$$Gain \approx 0dB \text{ and } B.W. \approx 46MHz \tag{4.4}$$

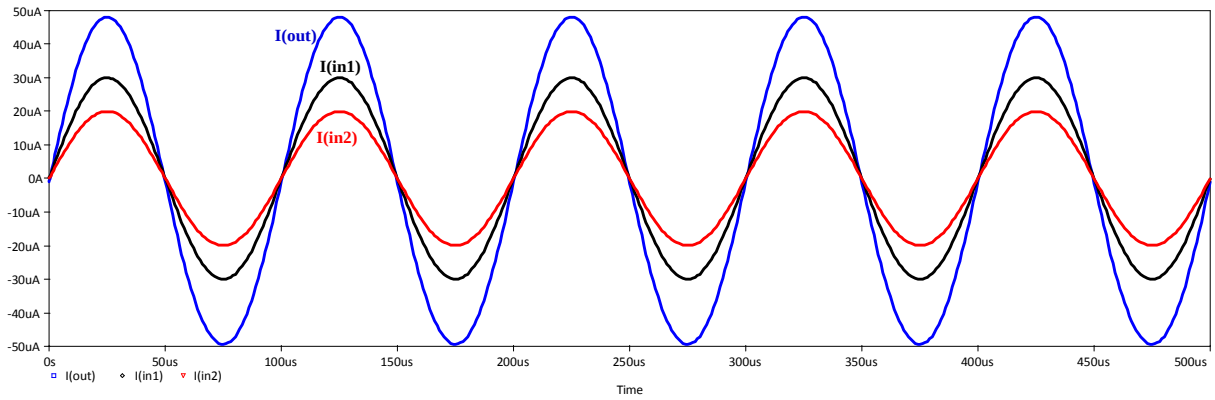


Fig. 4.5 Simulated o/p waveform of summing amplifier corresponding to two sinusoidal i/p's

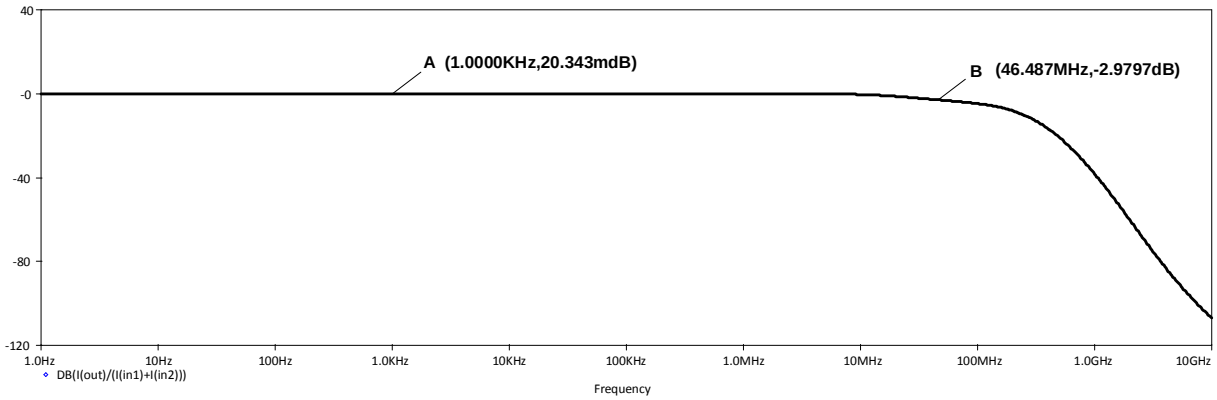


Fig. 4.6 Simulated frequency response of a summing amplifier

4.1.3. Subtractor or differential amplifier

Subtractors or differential amplifiers provide an o/p voltage or current proportional to or equal to the difference of multiple i/p's. VM differential amplifiers are usually designed and implemented using op-amps. Its CM counterpart can be implemented by CDTA, in which one of the i/p's is applied at the negative terminal and another i/p at positive terminal as shown in Fig. 4.7.

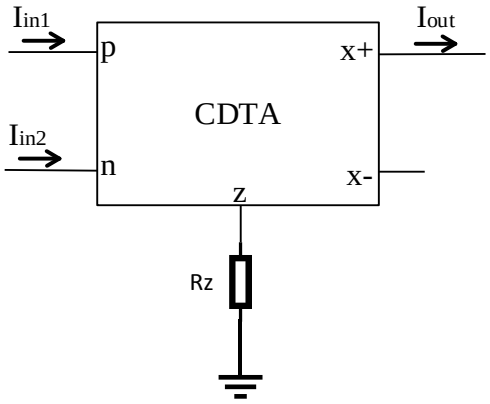


Fig. 4.7 Circuit Schematic of a current differential amplifier based on CDTA.

The o/p current of CDTA based differential amplifier can be expressed as

$$I_{out} = I_x = g_m R_z \left(I_{in1} - I_{in2} \right) \tag{4.5}$$

For PSPICE simulations, here the value of R_z is set to the value of $25k\Omega$ to get the gain of 7 or 16.9dB. As shown in Fig. 4.8, the transient analysis result shows the o/p which is the subtraction of 2 i/p's with an amplification of factor 7. The gain and 3dB bandwidth are obtained from points A and B in frequency response as shown in Fig. 4.9. Therefore,

$$Gain \approx 0dB \text{ and } B.W. \approx 46MHz \tag{4.6}$$

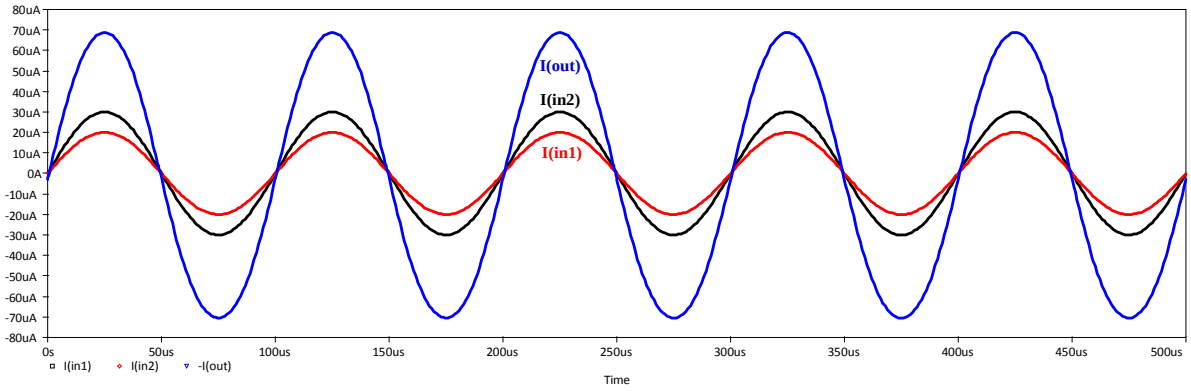


Fig. 4.8 Simulated o/p waveform of current differential amplifier corresponding to two sinusoidal i/p's

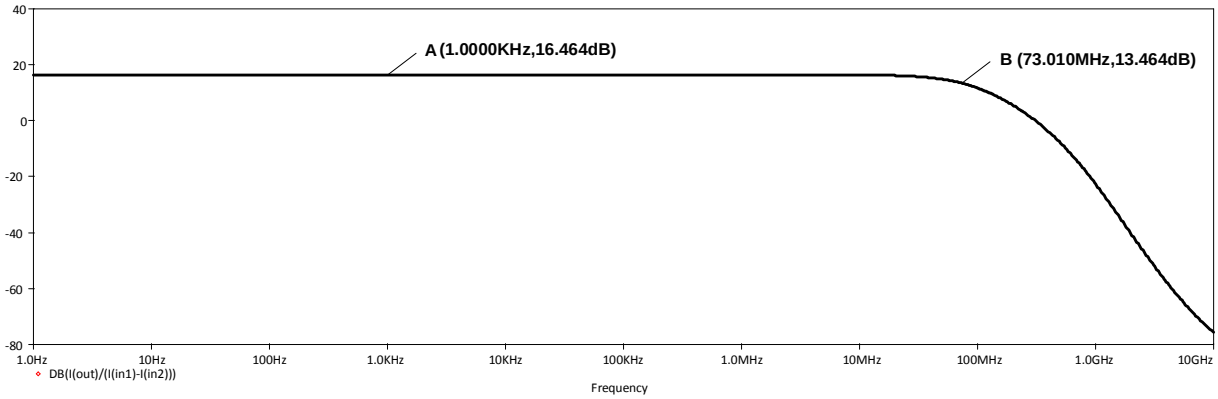


Fig. 4.9 Simulated frequency response of a current differential amplifier

4.1.4. Lossless integrator

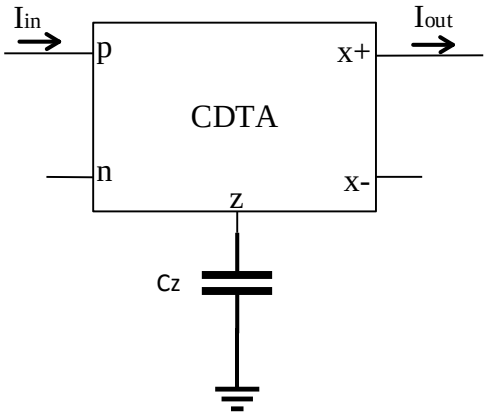


Fig. 4.10. Circuit Schematic of a lossless integrator based on CDTA.

A simple CM $g_m C$ lossless integrator can be designed and implemented using single CDTA and the circuit to implement the same is shown in Fig. 4.10 and the integrating action is achieved by connecting a grounded capacitor at terminal z . The o/p current of this integrator is expressed as

$$I_{out} = I_x = \frac{g_m}{sC_z}(I_{in}) \tag{4.7}$$

For PSPICE simulations, C_z is set to the value of $0.5nF$ .For transient analysis, a sinusoidal current signal is applied with the range of $\pm 50\mu A$. As shown in Fig. 4.11, the transient analysis result shows the o/p signal has the phase difference of 90^0 w.r.t. its i/p signal.

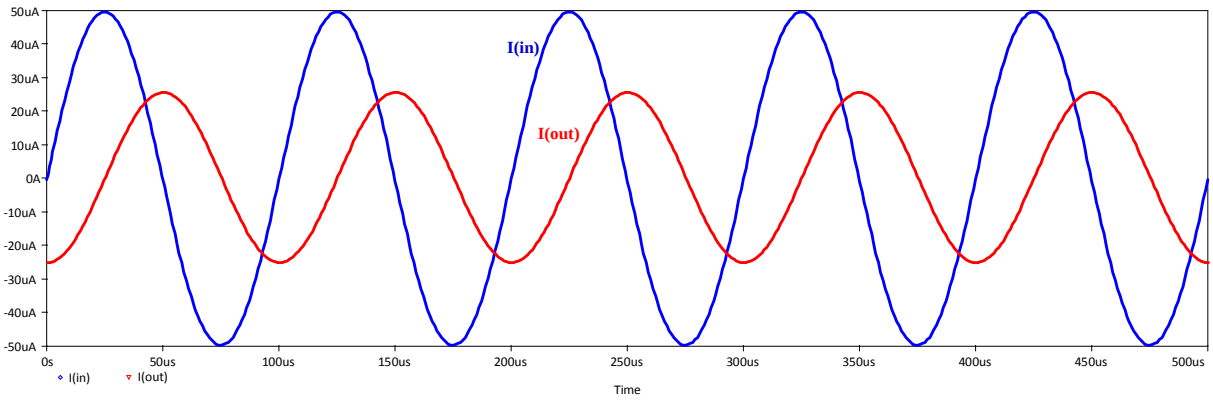


Fig. 4.11 Simulated o/p waveform of lossless integrator corresponding to sinusoidal i/p's

4.1.5. Impedance inverter

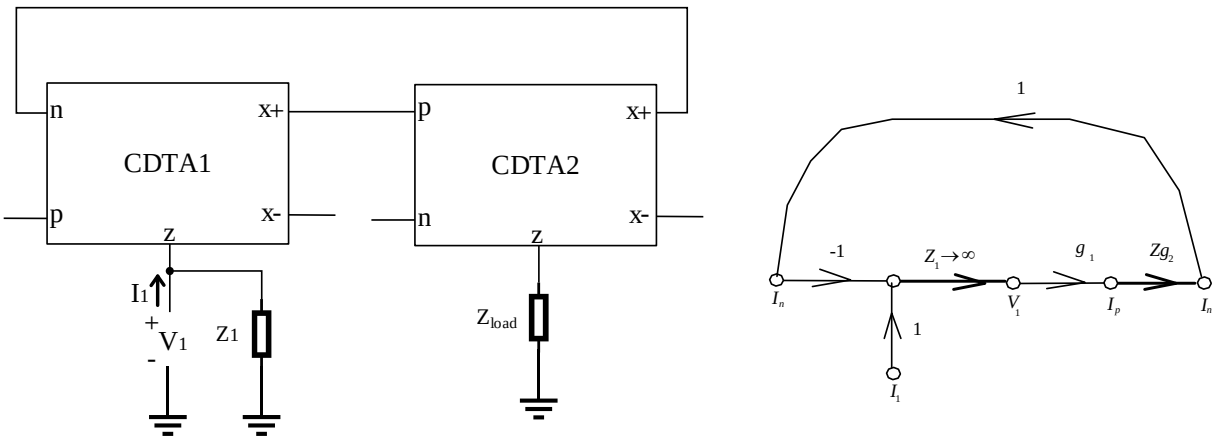


Fig. 4.12 Impedance inverter: (a) Implementation using two CDTAs, (b) "IVI" SFG.

By using a couple of traditional OTAs [46] the impedance inverters can be designed and realized. By exploiting similar principle it can be implemented by using CDTAs as shown in Fig. 4.12(a)[4]. The corresponding "IVI" SFG is given in Fig. 4.12(b), where Z_1 is an auxiliary grounded impedance. By evaluating the SFG, we can obtain the formula for the input impedance which is the inverse of Z_1.

$$Z_{in} = \frac{V_1}{I_1} = \frac{Z_1}{1 + g_{m1} g_{m2} Z_1 Z} \xrightarrow{Z_1 \to \infty} \frac{1}{g_{m1} g_{m2} Z} \tag{4.8}$$

PSPICE simulations of this circuit shows inductive impedance across the input terminal i.e. Z terminal of 1st CDTA, when a capacitive load is connected at Z terminal of 2nd CDTA. Fig. 4.13 shows the AC response of the impedance inverter circuit in which the input impedance is inductive in nature with phase of 90^0 in a passband when a capacitor is connected at the load end which has phase -90^0

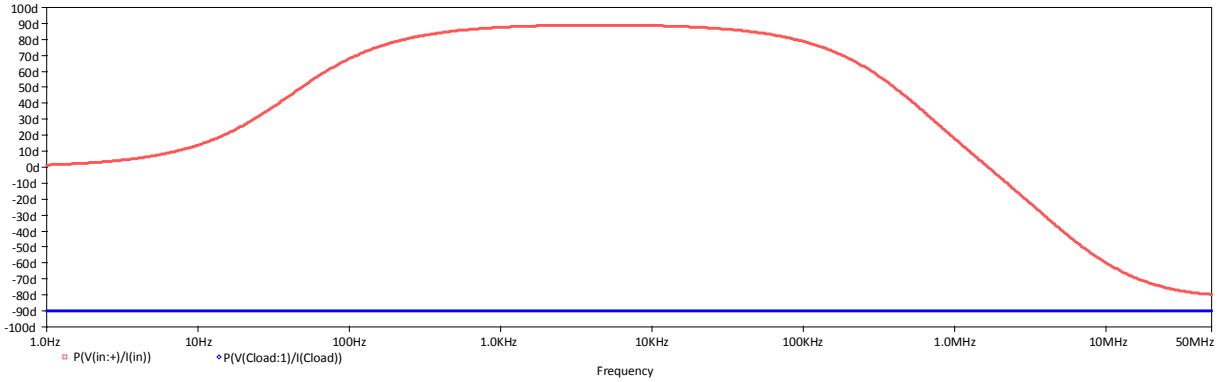
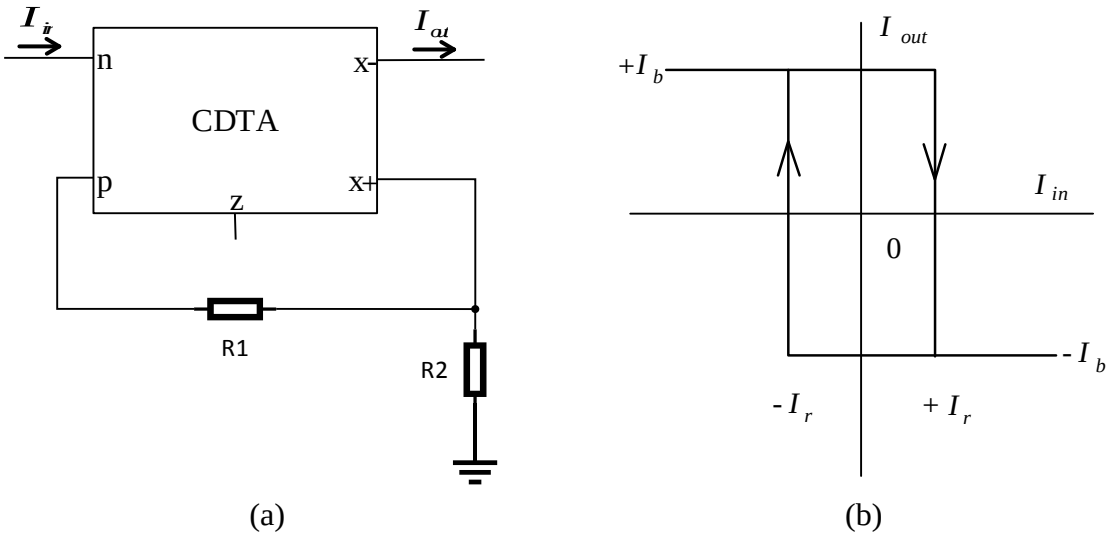


Fig. 4.13 Frequency response of Impedance Inverter using CDTAs: Inductor simulation

4.2. CM-Schmitt Trigger

Schmitt trigger holds a property of converting a time varying voltage/current signal into a stable logical signal (zero or one). This exclusive property of Schmitt Trigger is useful in both analog and digital applications. Some of its applications are comparators, function generators, triangular and square wave generators etc. Basically Schmitt trigger is a special comparator with a supplemental property of hysteresis. This is achieved by implementing any amplifier with positive feedback. Usually VM Schmitt Trigger were designed and implemented by traditional op-amps due its high voltage gain. Recently Schmitt Triggers have been implemented in CM by using wide range of current mode ABBs. Fig 4.14(a) shows the CM Schmitt Trigger implemented using single CDTA element [47].



(a) (b)

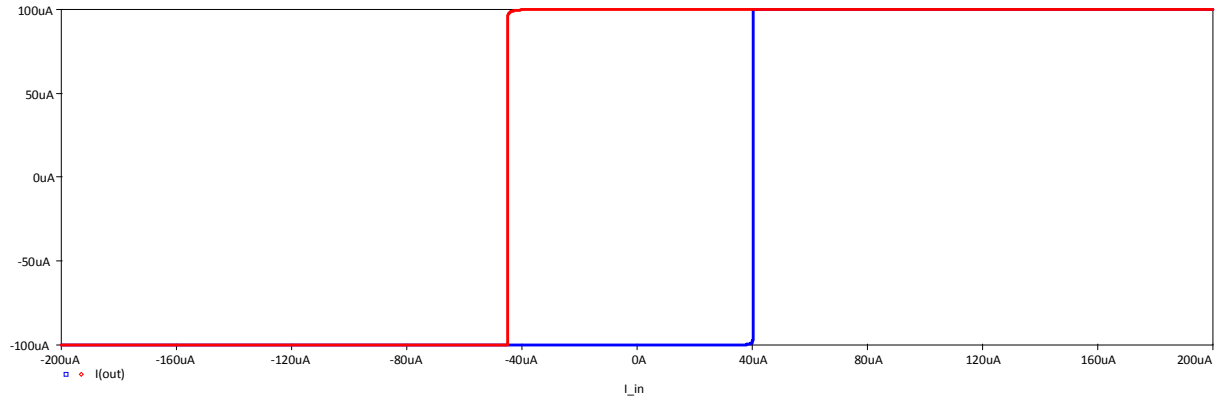
Fig. 4.14 CM-Schmitt Trigger based on CDTA: (a) Circuit schematic (b) Current transfer characteristics

CDTA has high current gain which is comparable to voltage gain of a traditional op-amp. By applying a proper positive feedback to CDTA the required hysteresis can be achieved. When the z terminal is not loaded with any external impedance, the potential drop across this terminal is due to its internal resistance formed by high impedance o/p node of CDU and very high impedance of i/p node of DO-OTA, which is very high (typically in mega Ohms). The product of this internal resistance and transconductance of DO-OTA g_m constitutes the overall current gain of the CDTA which comes out to be very high. As the value of o/p currents I_{x+} and I_{x-} are limited by internal bias current I_b of DO-OTA. When the product of $I_p - I_n$ and the overall current gain of CDTA is out of the interval $\notin (-I_b, I_b)$, the o/p currents I_{x+} and I_{x-} will be clipped. The hysteresis as shown in Fig.4.14(b), can be implemented by positive feedback designed using the current divider formed by R_1 and R_2. The following relation is obtained between output current saturation levels $\left(I_{out} = \pm I_b\right)$ and the input current levels $\left(I_{in} = \pm I_r\right)$ at which the output current toggles.

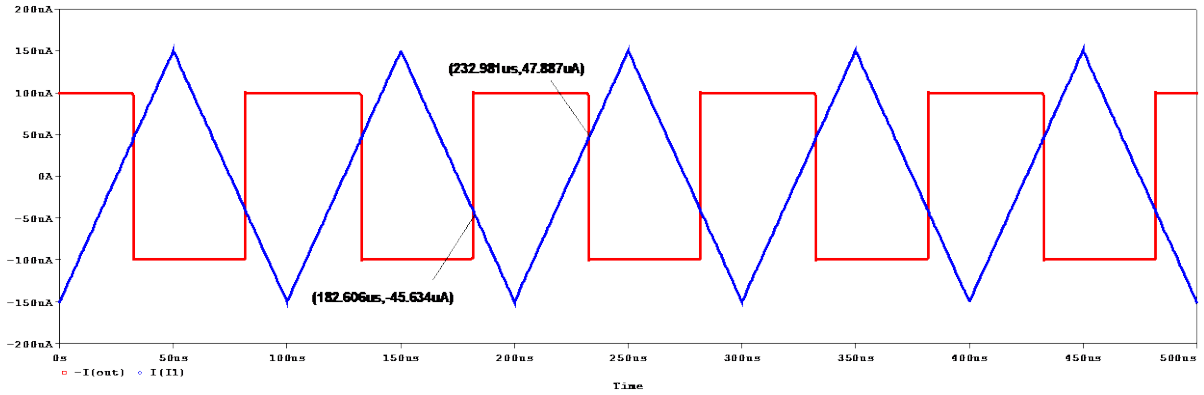
$$I_b = \frac{R_1}{R_1 + R_2} I_r \tag{4.8}$$

Simplest CM Schmitt trigger is obtained by short circuiting R_1 and disconnecting R_2. Then the toggling levels of input current are equal to saturation levels of output current $\left(\pm I_b = \pm I_r\right)$.

For PSpice simulations of the circuit shown in Fig 4.14(a) the bias current I_b is set to $100\mu A$, $R_1 = R_2 = 1k\Omega$.For transient analysis a triangular wave with the range of $-150\mu A$ to $+150\mu A$. Its frequency is fixed to $10kHz$. As shown in Fig 4.15(a), the transient analysis gives $I_r \approx +48\mu A, -46\mu A$ (ideally $= \pm 50\mu A$) and $I_{out} = \pm I_b = 100\mu A$. Fig 4.15(b) gives the hysteresis curve.



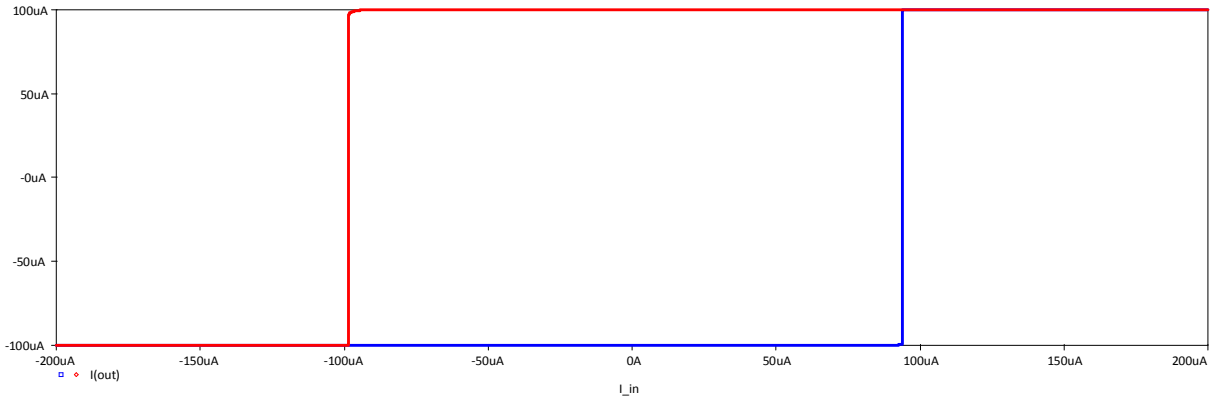
(a)



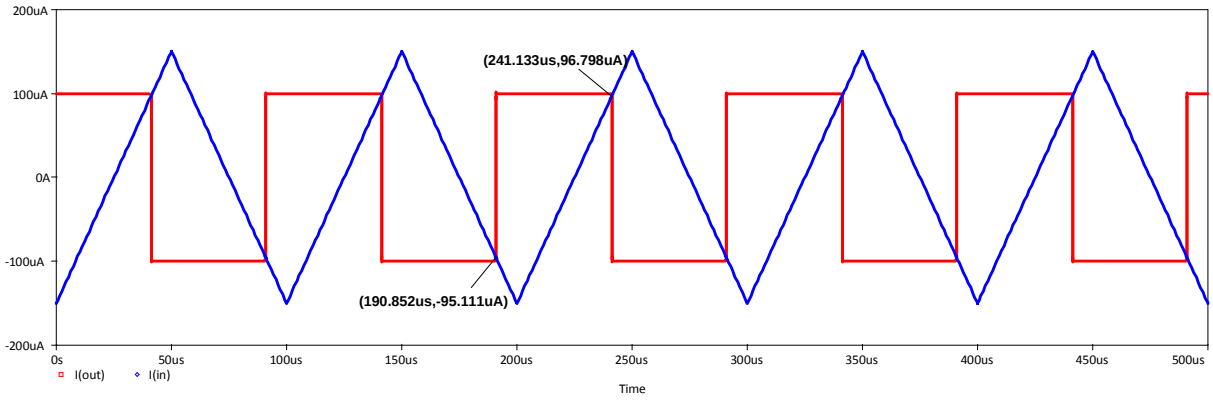
(b)

Fig. 4.15 (a) Simulated o/p waveform corresponding to sinusoidal i/p (b) Simulated transfer characteristics (Hysteresis curve)

For PSPICE simulations of the simplest Schmitt Trigger, the circuit shown in Fig 4.14(a) is modified by short circuiting R_1 and disconnecting R_2, the rest of the setup remains same. As shown in Fig 4.16(a), the transient analysis gives $I_r \approx +97\mu A, -95\mu A$ (ideally $= \pm 100\mu A$) and $I_{out} = \pm I_b = 100\mu A$. Fig 4.16(a) shows the hysteresis curve which has larger hysteresis area than of the original circuit.



(a)

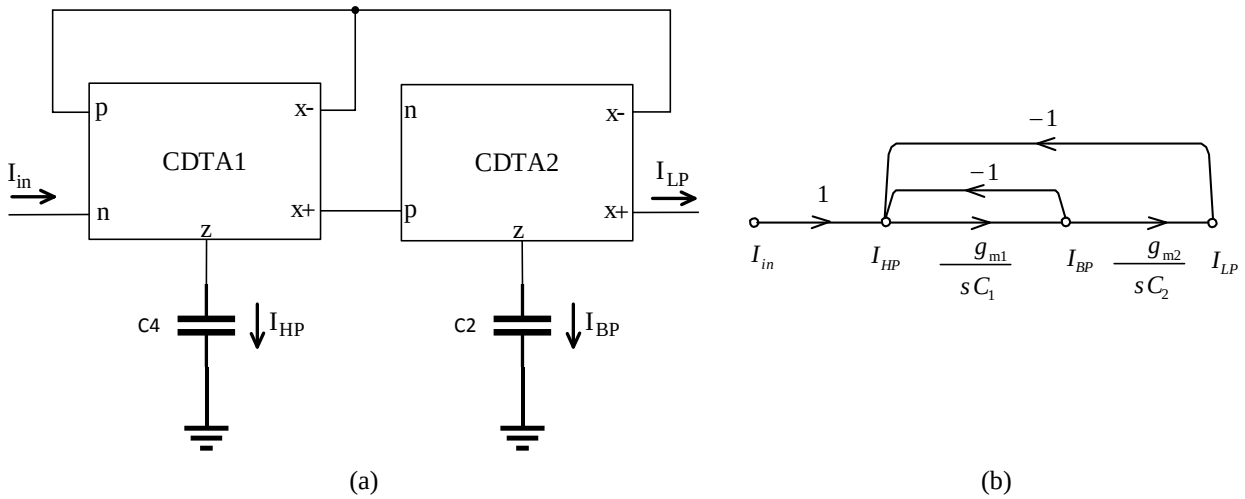


(b)

Fig. 4.16 (a) Simulated o/p waveform corresponding to sinusoidal i/p (b) Simulated transfer characteristics (Hysteresis curve) for modified Schmitt trigger.

4.3. CM-KHN biquad filter

OpAmp-based VM-KHN filter has bandwidth limitation. CM-KHN filters overcome op-amp's limitation using CM-ABBs as reported in [48-51]. But, many of these require excess number of ABBs. Fig. 4.17(a) shows CM-KHN filter implemented using two CDTAs [52]. This filter circuit can be implemented using two lossless $g_m - C$ integrators in feedback loop as depicted form its SFG in Fig. 4.17(b). Three basic filters, i.e., LPF, BPF and HPF can be implemented simultaneously without modifying the circuit structure. It also has an advantage of independent tuning of natural frequency and quality factor Therefore, due to advantages of CDTA, it can used to implement KHN filter.



(a) (b)

Fig. 4.17 CDTA based CM-KHN filter: a) circuit schematic b) SFG

The following current transfer functions can be for CM-KHN filter:

$$\frac{I_{HP}}{I_{in}} = \frac{-s^2}{D_r(s)} \tag{4.9}$$

$$\frac{I_{BP}}{I_{in}} = \frac{-s}{D_r(s)} \tag{4.10}$$

$$\frac{I_{LP}}{I_{in}} = \frac{-1}{D_r(s)} \tag{4.11}$$

$$\text{Where } D_r(s) = s^2 + s\frac{g_{m1}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2} \tag{4.12}$$

The natural angular frequency and Q-factor is given as

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \text{ and } Q_0 = \sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}} \tag{4.13}$$

Considering non-ideal CDTA, natural frequency and Q-factor become

$$\omega_0 = \sqrt{\alpha_{p1}\alpha_{p2}\frac{g_{m1}g_{m2}}{C_1C_2}} \text{ and } Q_0 = \sqrt{\frac{\alpha_{p2}}{\alpha_{p1}}\frac{g_{m2}C_1}{g_{m1}C_2}} \tag{4.14}$$

If tracking errors are equal for both CDTAs then the Q-factor remains unaltered and the deviation in natural frequency can be compensated by adjusting the values of capacitances C_1 and C_2

For the validation of KHN filter, the CDTA based CM-KHN is simulated using PSPICE software. Bias currents for both CDTAs are chosen as $I_{b1} = I_{b2} = 100\mu A$. Corresponding transconductances are $g_{m1} = g_{m2} = 281.709\,\mu A/V$. Values of capacitances are kept as $C_1 = C_2 = 1nF$ .Theoretical value of f_0 comes out to be $44.835kHz$. Fig 4.18 shows all three simulated filter responses viz. LPF, HPF and BPF. Simulated value of f_0 can be measured using point A from the BPF response as shown in the Fig. 4.19

The measured natural frequency is

$$f_0 = 44.668kHz \qquad (4.15)$$

Therefore, the results obtained from simulation are in agreement with theoretical calculations.

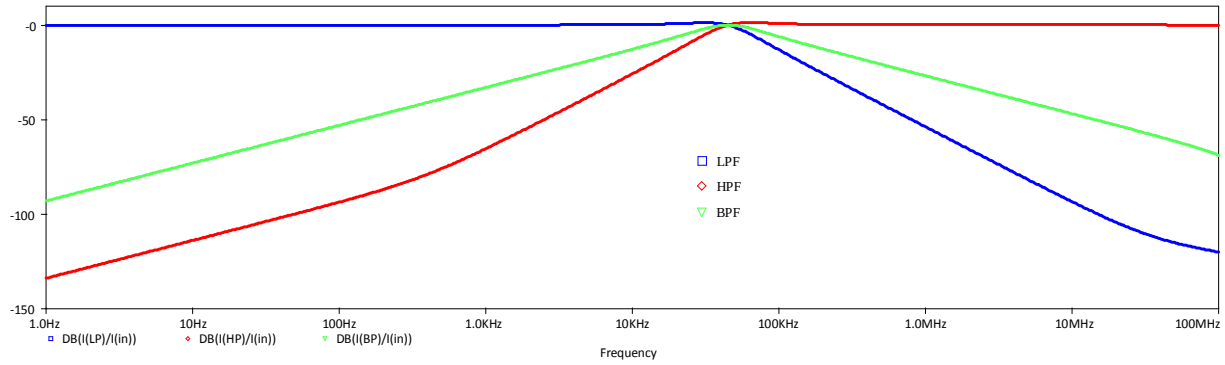


Fig. 4.18 Simulated filter responses of CDTA based CM-KHN biquad circuit: LPF, HPF and BPF

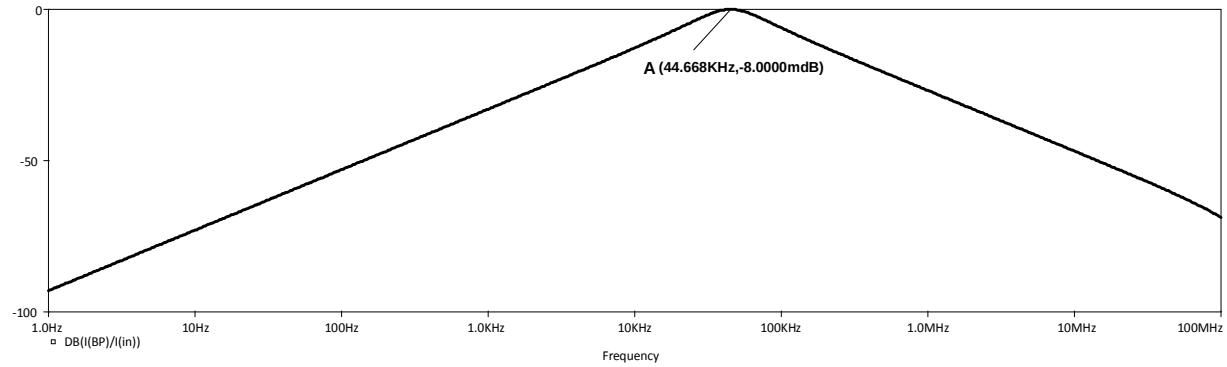


Fig. 4.19 Simulated BPF response for the calculation of natural frequency

Chapter

5. Realization of CD-DITA

5.1.Introduction

Current differencing differential input transconductance amplifier (CD-DITA) is one of the ABBs for designing and implementing analog circuits. In contrast to the traditional op-amps, CD-DITA not only supports VM but also CM and multi-mode operation. CD-DITA is surfacing as a flexible, universal and versatile ABB for analog signal processing. Its advantageous features and usefulness have been recognized in Biolek's paper on active elements [41].

5.1.1. Ideal CD-DITA

CD-DITA is a new six-terminal active block with electronic control. The circuit schematic of CD-DITA and its behavioral model [41] are shown in the Fig. 5.1(a) and (b), respectively. CD-DITA has two low-impedance (ideally zero) current input terminals p and n, and four high-impedance (ideally infinite) terminals, out of which two are the intermediate terminals namely output current terminal z and input voltage terminal v and the remaining two includes output current terminals $x+$ and $x-$.

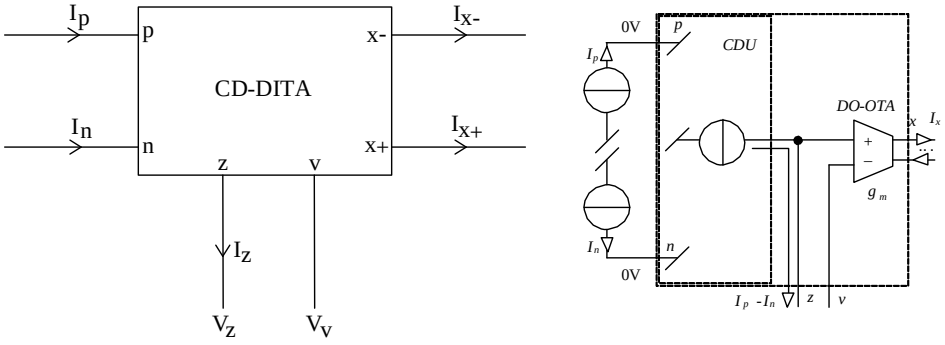


Fig. 5.1 CD-DITA (a) Schematic symbol (b) Behavioral model

The CD-DITA model includes two stages which are essentially controlled sources: differential current controlled current source (DCCCS) with unity current gain, and differential voltage controlled current source (DVCCS) with the transconductance gain. The input stage of CD-DITA can be easily designed by a differential i/p single-o/p CDU, which produces the difference of i/p currents I_p and I_n which flows through the z terminal. This current I_z will

produce an appropriate voltage drop, if any external load impedance is connected to it. The output stage can be implemented by differential input-dual output OTA (DO-OTA). The z terminal of CD-DITA is also internally connected to the non-inverting i/p of DO-OTA. The inverting terminal of the DO-OTA is brought out as a terminal v.The voltage difference between z and v terminals are transformed via DO-OTA's transconductance gain g_m into the currents I_{x+} and I_{x-} flowing through $x+$ and $x-$ terminals. These currents flow in opposite direction but, their magnitudes are equal. The transconductance gain of DO-OTA can be electronically varied with bias currents. The relations between the inputs and outputs terminals of CD-DITA can be given by following terminal equations:

$$V_p = V_n = 0 \tag{5.1}$$

$$I_v = 0 \tag{5.2}$$

$$I_z = I_p - I_n \tag{5.3}$$

$$I_{x+} = g_m\left(V_z - V_v\right) \tag{5.4}$$

$$I_{x-} = -g_m\left(V_z - V_v\right) \tag{5.5}$$

Therefore, Equation matrix is given as

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \\ I_v \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 & \mp g_m \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_x \\ V_v \end{bmatrix} \tag{5.5}$$

5.1.2. Non ideal CD-DITA

This section deals with the non-ideal case of CD-DITA element. As shown in Fig. 5.2 the non-ideal equivalent of CD-DITA is similar to that of CDTA, except for the addition of error in transconductance transfer β_v from v terminal which is grounded in case of CDTA. These errors from z and v terminals are defined as

$$\beta_z = 1 - \varepsilon_z;\ \beta_v = 1 - \varepsilon_v \text{ and } |\varepsilon_z| << 1;\ |\varepsilon_v| << 1 \tag{5.6}$$

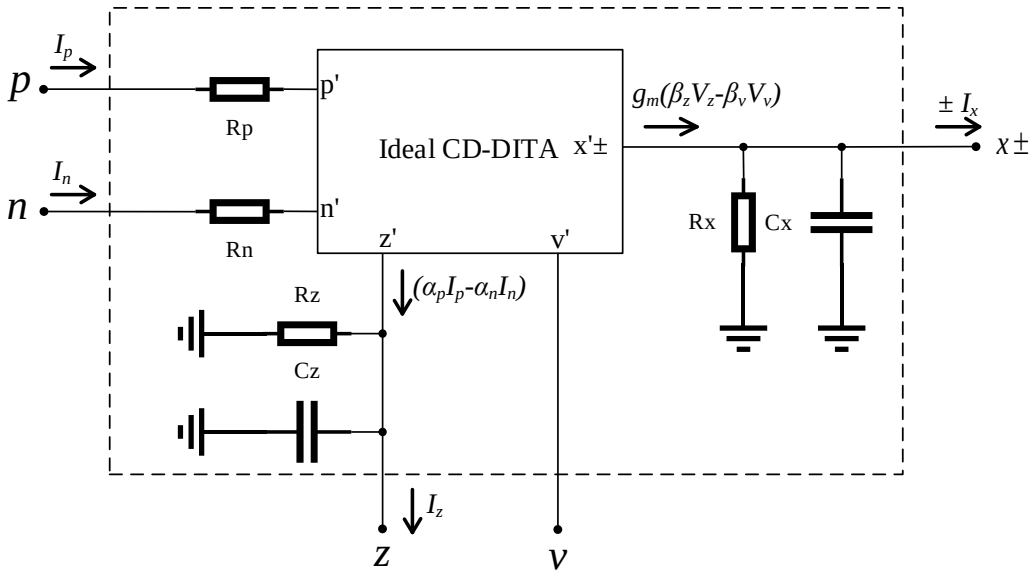


Fig. 5.2 Non ideal CD-DITA

Where ε_z and ε_v are the transconductance tracking errors from z to $x\pm$ and v to $x\pm$ terminals, respectively. In a non-ideal case, the terminal equations of CD-DITA are modified as follows

$$V_p = 0 \tag{5.7}$$

$$V_n = 0 \tag{5.8}$$

$$I_z = \alpha_p I_p - \alpha_n I_n \tag{5.9}$$

$$I_{x+} = +g_m\left(\beta_z V_z - \beta_v V_v\right) \tag{5.10}$$

$$I_{x-} = -g_m\left(\beta_z V_z - \beta_v V_v\right) \tag{5.11}$$

Therefore the Non-ideal CD-DITA in absence of parasitics is represented by following equations matrix

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \\ I_v \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 \\ 0 & 0 & \pm\beta_z g_m & 0 & \mp\beta_v g_m \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_x \\ V_v \end{bmatrix} \tag{5.12}$$

5.2.New realization of CMOS based CD-DITA

The BJT implementation of CD-DITA has already been proposed in [39]. In this work the proposed CMOS implementation of CD-DITA used for the simulations its characteristics and

applications is shown in Fig. 5.3, where the CDU is realized by transistors M1-M12 and M13-M16 form the DO-OTA.

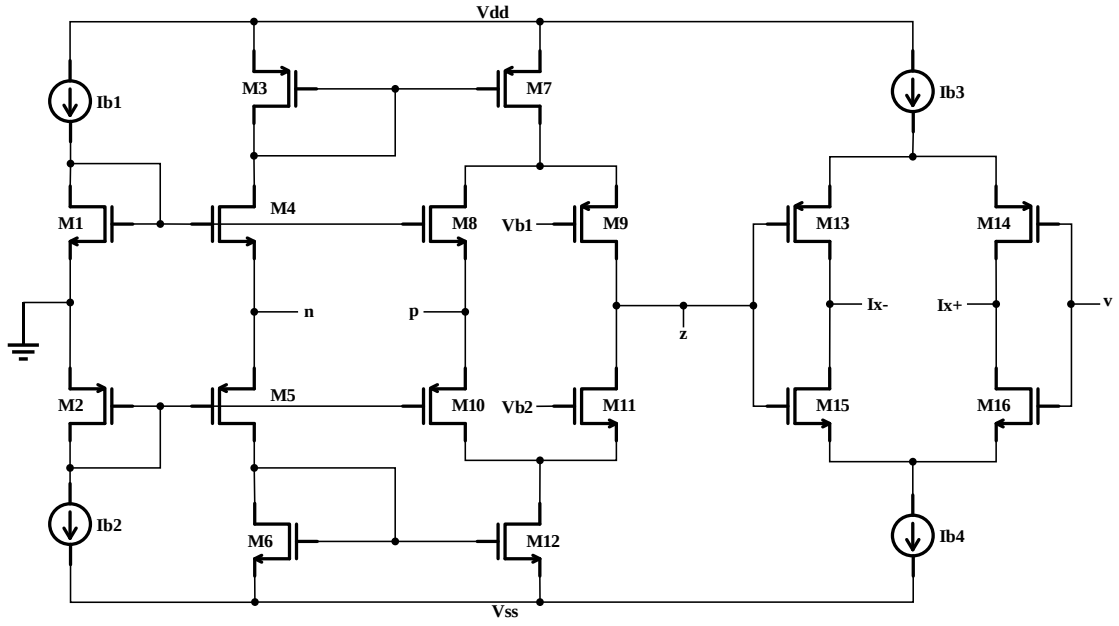


Fig. 5.3 New CMOS implementation of CD-DITA

This CMOS implementation of CD-DITA is the modification of CDTA circuit, which was first proposed in [53] and modified for its application in [54]. The i/p terminal of DO-OTA which is usually grounded in the case of CDTA is replaced with a voltage terminal v. In CDU section M2, M5 and M6 are the transistors constitutes floating current source [53,55]. The transistors M3 and M4are used for positive feedback in the CDU section to reduce the P terminal i/p resistance. To reduce N terminal i/p resistance, M4 and M6 are used. The DO-OTA stage employs an Arbel-Goldminz OTA [56]. The aspect ratios of transistors used in CD-DITA implementation are enumerated in table 5.1

Table 5.1 Aspect ratios of MOS transistors used in CD-DITA implementation

Transistors	$\mathbf{W}(\mu m)$	$\mathbf{L}(\mu m)$
$M_1 - M_3$	18	0.18
M_4, M_5	36	0.18
$M_6 - M_{12}$	18	0.18
$M_{13} - M_{16}$	6	0.18

Transconductance g_m parameter of DO-OTA section of CD-DITA element can be determined by the transconductance of outputs transistors (M13-M16). The approximated value can be calculated as

$$g_m = \frac{(g_{m13} + g_{m15})}{2} \text{ or } g_m = \frac{(g_{m14} + g_{m16})}{2} \tag{5.13}$$

where g_{mi} is the transconductance of ith transistor which is defined by

$$g_{mi} = \sqrt{I_{bi}\mu_{n/p}C_{ox}\left[\frac{W}{L}\right]_i} \tag{5.14}$$

where $\mu_{n/p}$ is the carrier mobility of the for NMOS (n) and PMOS (p) transistors, C_{ox} is the silicon oxide capacitance per area, $[W/L]_i$ and I_{bi} are the W/L ratio and bias current of ith transistor respectively.

5.3. Characterization of CD-DITA

The CMOS realization of CD-DITA block as shown in Fig. 5.3 is simulated using PSPICE with 180nm process parameters. The aspect ratios of MOS transistors are given in Table 5.1. The power supply rails are $\pm 0.9V$. Both CDTA and CD-DITA are characterized by same AC & DC behavior. Small signal (Frequency response) behavior of CD-DITA will be dealt here as these analyses will provide the parameters related to the non-idealities of CD-DITA which can be useful in verification of filter characteristics of non-ideal CD-DITA

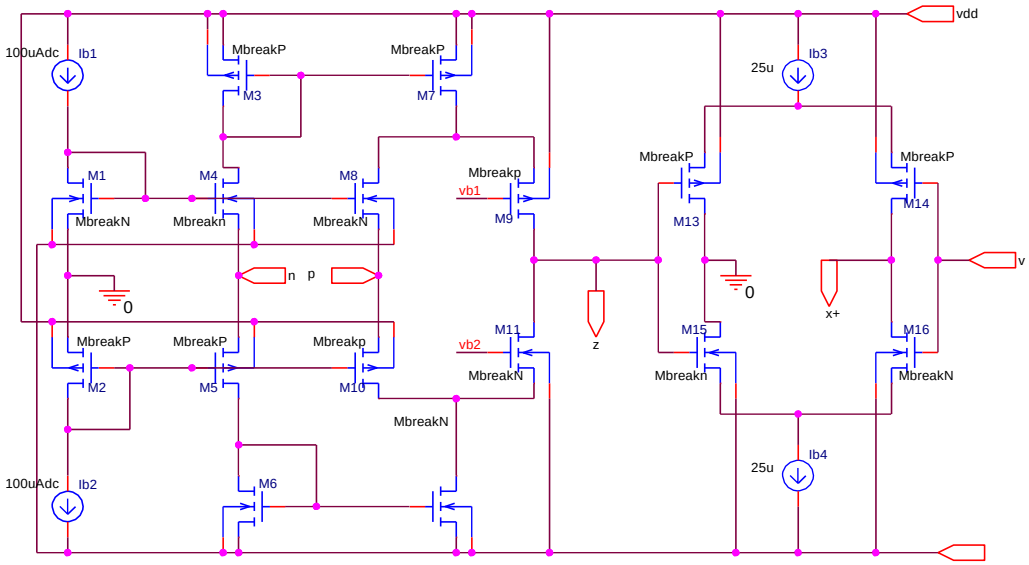


Fig. 5.4 PSPICE schematic of CD-DITA block

The PSPICE schematic of CDTA is shown in Fig. 5.4. Bias currents and voltages I_{b1}, I_{b2}, $I_{b3}, I_{b4}, V_{b1}, V_{b2}$, are chosen as $100\mu A, 100\mu A, 25\mu A, 25\mu A, -400mV$ and $300mV$ respectively. The frequency response of I_z/I_p is shown in Fig. 5.5 from which the parasitic gain α_p from p terminal to z terminal is measured and found to be:

$$\alpha_p = \frac{I_z}{I_p} = -173.806mdB \approx 0.98 \qquad (5.15)$$

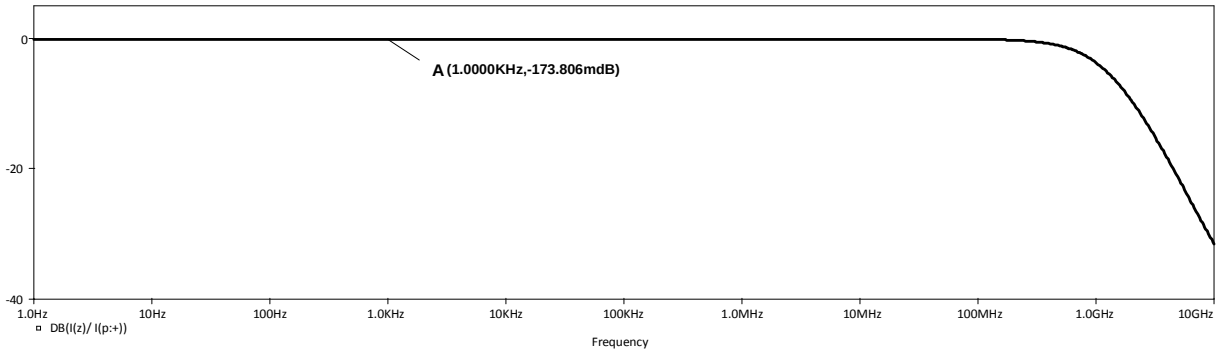


Fig. 5.5 Parasitic Current gain from p terminal to z terminal with $I_n = 0$ (I_z/I_p vs frequency)

The frequency response of I_z/I_n is shown in Fig. 5.6 from which the parasitic gain α_n from n terminal to z terminal is measured and found to be:

$$\alpha_n = \frac{I_z}{I_n} = -388.787mdB \approx 0.96 \qquad (5.16)$$

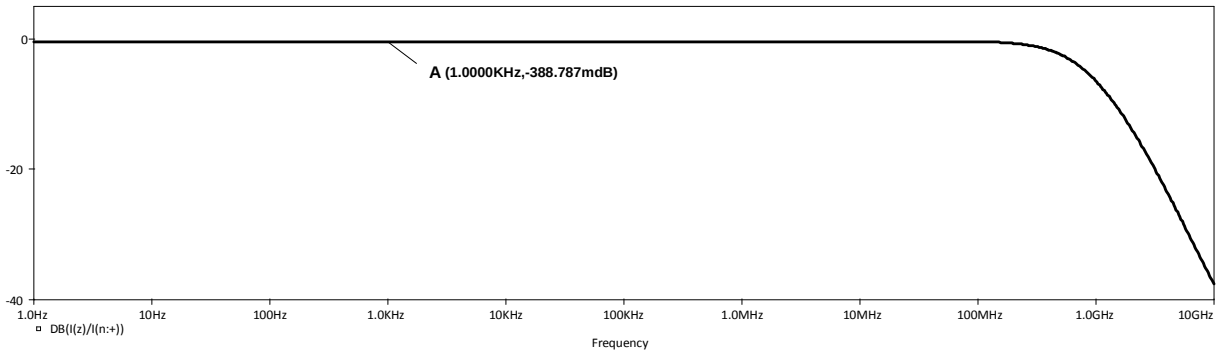


Fig 5.6 Parasitic Current gain from n terminal to z terminal with $I_p = 0$ (I_z/I_n vs frequency)

Fig. 5.7 shows the simulated frequency response of transconductance gain by varying bias current I_{b3} and I_{b4} simultaneously with values $15\mu A$ $20\mu A, 25\mu A$ and $30\mu A$, the

transconductance gain obtained are $154.612\,\mu A/V$, $197.114\,\mu A/V$, $236.658\,\mu A/V$ and $273.722\,\mu A/V$ respectively.

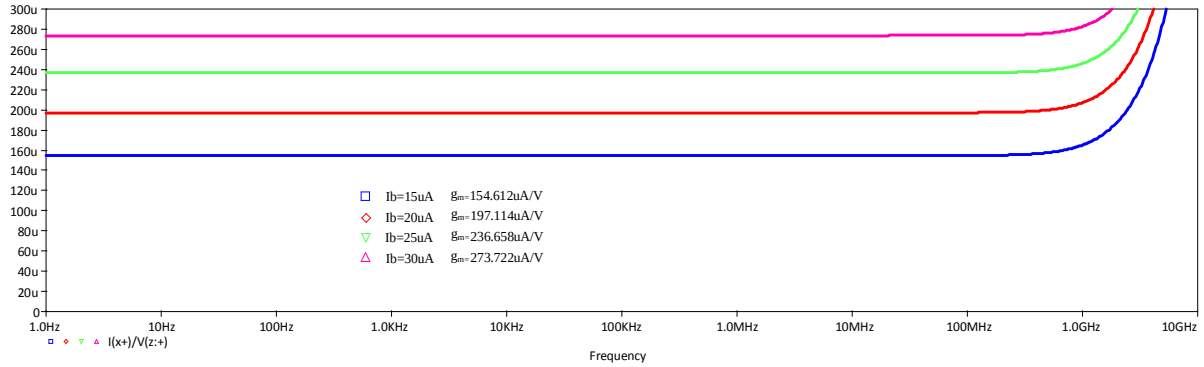


Fig. 5.7 Transconductance gain g_m from z -terminal to $x+$ terminals with I_{b3} and I_{b4} as parametric sweep (I_{x+}/V_z vs frequency)

From Fig. 5.8 and Fig. 5.9 the impedances seen through p and n terminals are found out to be very low as they are required to be, theoretically. The values of parasitic resistances R_p and R_n can be measured using point A from their corresponding frequency responses, where the parasitic capacitance at these terminals has negligible effect.

$$R_p \approx 322\Omega \tag{5.17}$$

$$R_n \approx 166\Omega \tag{5.18}$$

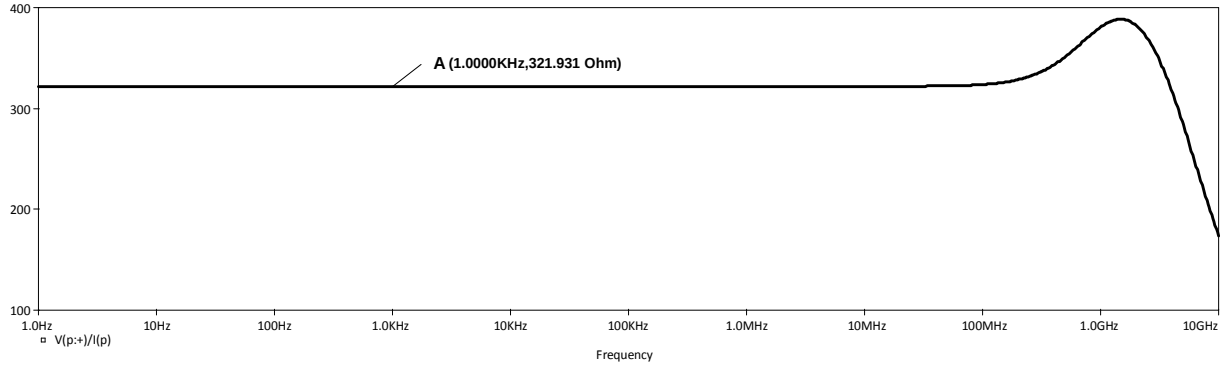


Fig. 5.8 Impedance seen through p -terminal (Z_p vs frequency)

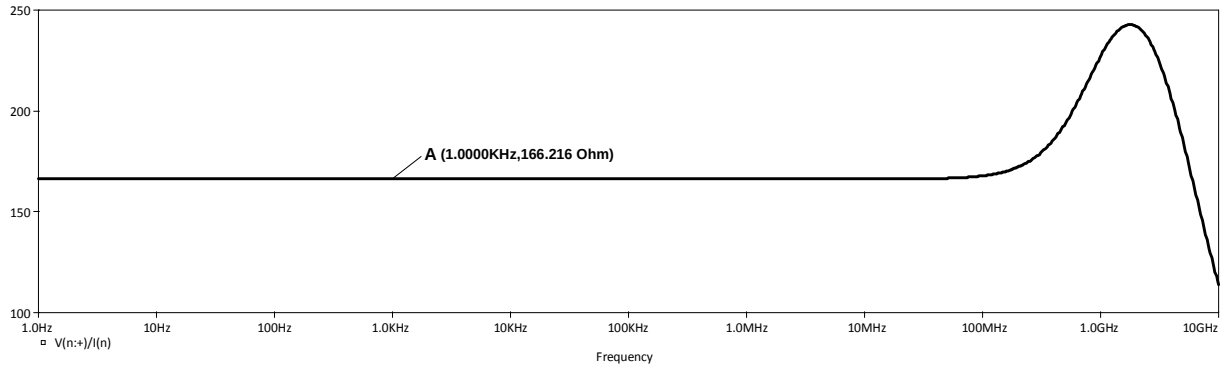


Fig. 5.9 Impedance seen through n -terminal (Z_n vs frequency)

The values of parasitic resistances R_z and R_x can be measured using point A from their corresponding frequency responses(Fig. 5.10 and Fig. 5.11), where the parasitic capacitance at these terminals has negligible effect and using these values parasitic resistances C_z and C_x are measured at high frequencies (Point B) where their effect is predominant.

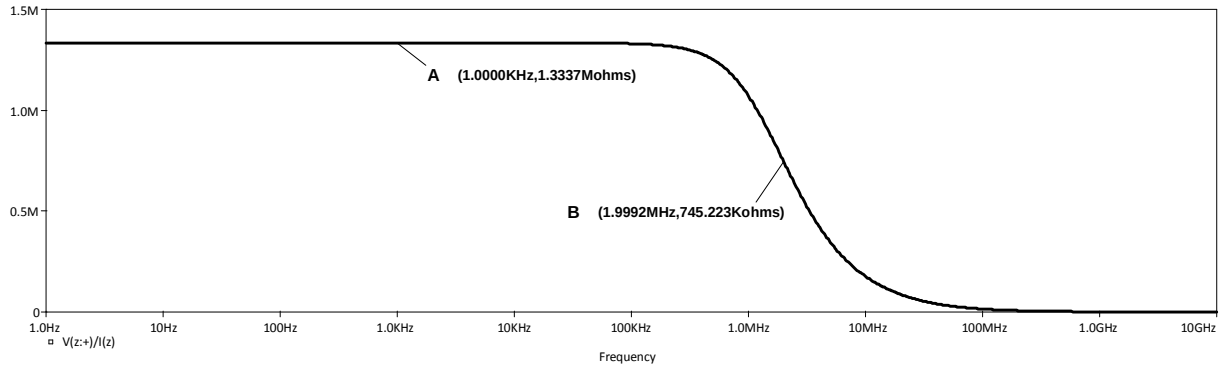


Fig. 5.10 Impedance seen through z -terminal (Z_z vs frequency)

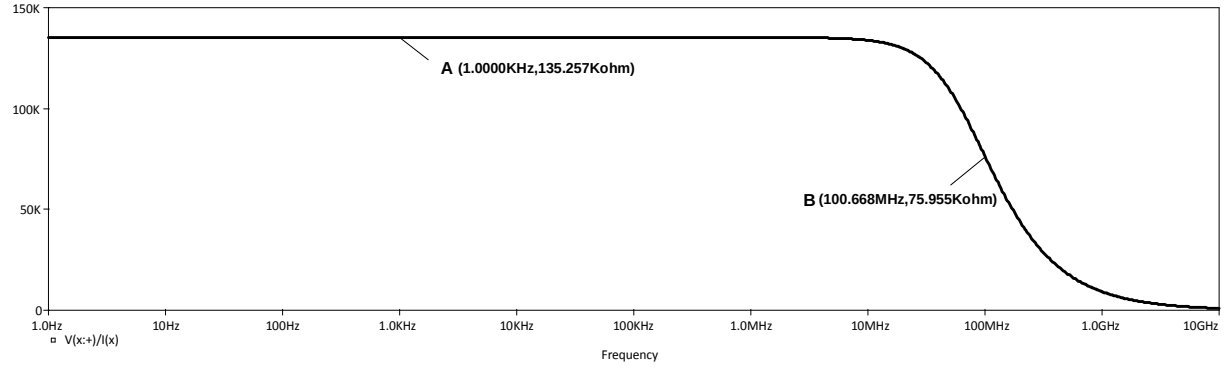


Fig. 5.11 Impedance seen through $x\pm$ terminal ($Z_{x\pm}$ vs frequency)

$$\therefore R_z = 1.3337 M\Omega \tag{5.19}$$

$$Z_z = \frac{R_z}{1 + sC_z R_z} \therefore |Z_z| = \frac{R_z}{\sqrt{1 + \omega^2 C_z^2 R_z^2}} \tag{5.20}$$

From the graph, at $f = 2MHz$, $|Z_z| = 745.223k\Omega$

$$\therefore C_z = 88.6\, fF \tag{5.21}$$

Similarly,

$$R_x = 135.257k\Omega \tag{5.22}$$

$$Z_x = \frac{R_x}{1 + sC_x R_x} \therefore |Z_x| = \frac{R_x}{\sqrt{1 + \omega^2 C_x^2 R_x^2}} \tag{5.23}$$

From the graph, at $f = 100MHz$, $|Z_x| = 75.955k\Omega$

$$\therefore C_x = 17.23\, fF \tag{5.24}$$

Therefore, the impedances seen through z and $x\pm$ terminals are found out to be very high as they are required to be high, theoretically for it to work in filtering applications.

Chapter

6. Proposed CD-DITA based VM-MISO type universal filter

6.1.Introduction

Universal filters can be classified based on their topology is: variable and fixed topology type. The latter is further divided into VM, CM and MM types, each of which is further subdivided based on how responses are obtained w.r.t. combinations of i/p's and o/p's: i) single-i/p multiple-o/p (SIMO) type filters, ii) multiple-i/p single-o/p (MISO) type filters, and iii) multiple-i/p multiple-o/p (MIMO) type filters. The biquad circuits working in mixed-mode can be operated in voltage, current, transimpedance, and transadmittance modes. One of the most widely used universal analog filters topology is a MISO type VM filters. By simply switching on or off the i/p voltages or by doing the same along with their different combinations, various filter functions is realized simultaneously. The selection of inputs is done digitally with the usage of microcontroller or microprocessor. One such filter based on single CD-DITA is proposed in this work.

6.2. Proposed filter circuit employing single CD-DITA

The proposed MISO-type VM universal biquad filter employing single CD-DITA as an ABB is shown in Fig. 6.1. It consists of single CD-DITA, two resistors and two capacitors.

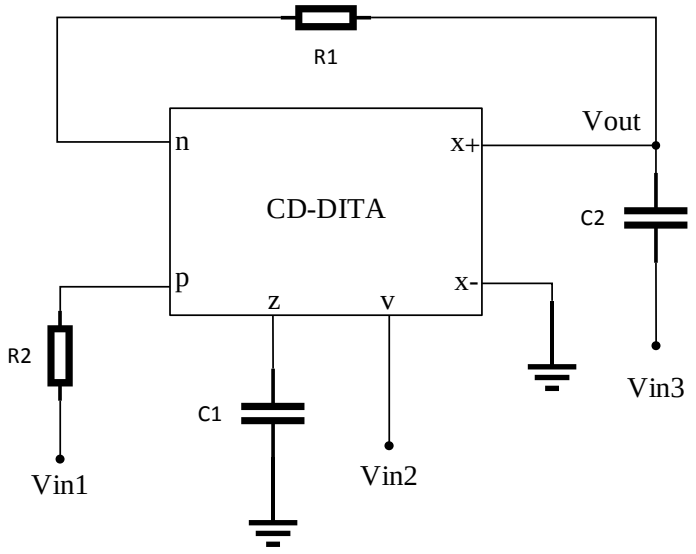


Fig. 6.1 The proposed CD-DITA based universal MISO-type VM-biquad filter circuit.

Considering the ideal CD-DITA, circuit analysis of the proposed filter yields following relation between o/p voltage and i/p voltages

$$V_{out} = \frac{s^2 C_1 C_2 V_{in3} - s g_m C_1 V_{in2} + g_m G_2 V_{in1}}{s^2 C_1 C_2 + s G_1 C_1 + g_m G_1} \tag{6.1}$$

Using equation 6.1, various filter functions are realized as follows

1. If $V_{in2} = V_{in3} = 0$ and $V_{in1} = V_{in}$, then LPF is realized as

$$\frac{V_{LP}}{V_{in}} = \frac{G_2}{G_1} \frac{g_m G_1}{s^2 C_1 C_2 + s G_1 C_1 + g_m G_1} \tag{6.2}$$

2. If $V_{in1} = V_{in2} = 0$ and $V_{in3} = V_{in}$, then HPF can realized as

$$\frac{V_{HP}}{V_{in}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s G_1 C_1 + g_m G_1} \tag{6.3}$$

3. If $V_{in1} = V_{in3} = 0$ and $V_{in2} = V_{in}$, then (inverting) BPF is realized as

$$\frac{V_{BP}}{V_{in}} = \frac{g_m}{G_1} \frac{-s G_1 C_1}{s^2 C_1 C_2 + s G_1 C_1 + g_m G_1} \tag{6.4}$$

4. If $R_1 = R_2$, $V_{in2} = 0$ and $V_{in1} = V_{in3} = V_{in}$, then notch filter(BRF) is realized as

$$\frac{V_{BR}}{V_{in}} = \frac{s^2 C_1 C_2 + g_m G_1}{s^2 C_1 C_2 + s G_1 C_1 + g_m G_1} \tag{6.5}$$

4. If $R_1 = R_2 = \frac{1}{g_m}$ and $V_{in1} = V_{in2} = V_{in3} = V_{in}$, then APF is realized as

$$\frac{V_{AP}}{V_{in}} = \frac{s^2 C_1 C_2 - s g_m C_1 + g_m^2}{s^2 C_1 C_2 + s g_m C_1 + g_m^2} \tag{6.6}$$

From equations 6.2 to 6.6, it is observed that there is no necessity of inverting i/p to realize an APF response.

From equation 6.1 the filter pole frequency or natural frequency (ω_0) and quality factor (Q_0) are expressed as

$$\omega_0 = \sqrt{\frac{g_m}{R_1} \cdot \frac{1}{C_1 C_2}} \text{ and } Q_0 = \sqrt{g_m R_1 \cdot \frac{C_2}{C_1}} \tag{6.7}$$

If $R_1 = R_2 = \frac{1}{g_m}$ then,

$$\omega_0 = g_m \sqrt{\frac{1}{C_1 C_2}} \text{ and } Q_0 = \sqrt{\frac{C_2}{C_1}} \tag{6.8}$$

From equation 6.8, it follows that after adjusting Q_0, ω_0 can be tuned independently by DO-OTA's g_m.

The voltage gains of the filters are expressed as

$$G_{LP} = \frac{G_2}{G_1} \tag{6.9}$$

$$G_{BP} = \frac{g_m}{G_1} \tag{6.10}$$

$$G_{HP} = G_{BR} = G_{AP} = 1 \tag{6.11}$$

From equation 6.7, the sensitivities due to variation of active and passive elements are found as:

$$S_{R_2}^{\omega_0} = S_{R_2}^{Q_0} = 0 \tag{6.12}$$

$$S_{g_m}^{\omega_0} = \frac{1}{2}; S_{R_1}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2} \tag{6.13}$$

$$S_{g_m}^{Q_0} = S_{R_1}^{Q_0} = S_{C_2}^{Q_0} = \frac{1}{2}; S_{C_1}^{Q_0} = -\frac{1}{2} \tag{6.14}$$

From equations 6.12 to 6.14, it is observed that all of the sensitivities are less than unity.

6.3.Effects of non-idealities on filter performance

The performance of the CD-DITA based universal filter may deflect from the ideal one due to the nonidealities of CD-DITA block. The equivalent circuit of CD-DITA in presence of nonidealities has been discussed in one of the previous sections. The tracking errors in CDU, transfer error in transconductace of DO-OTA and parasitics at the terminals of CD-DITA will affect the filter performance especially when used in VM.

The parasitics at z and $x\pm$ terminals of CD-DITA may or may not affect the filter performance depending upon how they appear with external filter passive elements. Either these parasitics are absorbed by the external grounded impedances when they are shunt with them or they could only affect the center frequency and quality factor but also can add parasitic zeros to

some of the filter responses. In the proposed filter circuit parasitic capacitances C_z and C_x at z and x terminals appear in parallel with external capacitance C_1 and C_2, respectively. The external resistance R_1 between the o/p and the n terminal of CD-DITA is increased by R_n, and similarly the external resistance R_2 between the i/p and the p terminal of CD-DITA is increased by R_p .Therefore, the parasitic resistance at x terminal R_x appears parallel with $R_1 + R_n$. This increase in resistances can cause deviation for relatively high i/p resistances of CD-DTAs. Parasitic resistance R_z at z terminal neither appear parallel or series with any of the external impedances it causes considerable deflections in filter responses. Considering these non-idealities into account the relation of o/p and i/p voltages can be modified as

$$V_{out} = \frac{V_{in3}(s^2 C_1^* C_2 + sC_2 G_z) - V_{in2}(sC_1^* g_m \beta_v + g_m \beta_v G_z) + V_{in1}(g_m \beta_z \alpha_p G_2^*)}{s^2 C_1^* C_2^* + s\left(C_1^* G_x + C_1^* G_1^* + C_2^* G_z^*\right) + \left(G_1^* \alpha_n \beta_z g_m + G_x G_z + G_1^* G_z\right)} \tag{6.15}$$

Where

$$C_1^* = C_1 + C_z \text{ and } C_2^* = C_2 + C_x \tag{6.16}$$

$$G_z = \frac{1}{R_z} \text{ and } G_x = \frac{1}{R_x} \tag{6.17}$$

$$G_1^* = \frac{1}{R_1 + R_n} \text{ and } G_2^* = \frac{1}{R_2 + R_p} \tag{6.18}$$

For simplicity, we can ignore R_x as it is a large valued (typically in mega ohms) parasitic resistance and appears in shunt with $R_1 + R_n$ which has typical values in kilo ohms. Therefore, the modified expression for V_{out} is given as

$$V_{out} = \frac{V_{in3}(s^2 C_1^* C_2 + sC_2 G_z) - V_{in2}(sC_1^* g_m \beta_v + g_m \beta_v G_z) + V_{in1}(g_m \beta_z \alpha_p G_2^*)}{s^2 C_1^* C_2^* + s\left(C_1^* G_1^* + C_2^* G_z^*\right) + \left(G_1^* \alpha_n \beta_z g_m + G_1^* G_z\right)} \tag{6.19}$$

From equation 6.19, it can be observed that R_z adds a zero in BPF transfer function which gives finite low-frequency attenuation. This attenuation can be increased by keeping $R_z \rangle\rangle R_1 + R_n$. This can be achieved by designing CDU section of CD-DITA for high o/p resistance. The natural frequency ω_0 and quality factor Q_0 are also affected by R_z and are expressed as

$$\omega_0 = \sqrt{\frac{\beta_z \alpha_n g_m G_1^* + G_1^* G_z}{C_1^* C_2^*}} \tag{6.20}$$

$$\therefore \omega_0 = \sqrt{\frac{\beta_z \alpha_n g_m R_z + 1}{(C_1 + C_z)(C_2 + C_x) R_z (R_1 + R_n)}} \tag{6.21}$$

$$Q_0 = \sqrt{\frac{C_1^* C_2^* (\beta_z \alpha_n g_m G_1^* + G_1^* G_z)}{C_1^* G_1^* + C_2^* G_z}} \tag{6.22}$$

$$\therefore Q_0 = \sqrt{\frac{(C_1 + C_z)(C_2 + C_x)(\beta_z \alpha_n g_m R_z + 1)}{R_z (C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)}} \tag{6.23}$$

From above equations, it can be conclude that if the values of R_p and R_n are much lower than R_1 and R_2 then these parasitic resistances don't have much effect on ω_0 and Q_0. The effect of C_z and C_x is absorbed by C_1 and C_2 therefore, can be neglected.

There non-ideal sensitivities are found as

$$S_{\beta_v}^{\omega_0} = S_{R_p}^{\omega_0} = S_{\alpha_p}^{\omega_0} = S_{R_2}^{\omega_0} = S_{\beta_v}^{Q_0} = S_{R_p}^{Q_0} = S_{\alpha_p}^{Q_0} = S_{R_2}^{Q_0} = 0 \tag{6.24}$$

$$S_{C_1}^{\omega_0} = -\frac{1}{2}\frac{C_1}{C_1 + C_z}; S_{C_2}^{\omega_0} = -\frac{1}{2}\frac{C_2}{C_2 + C_x} \tag{6.25}$$

$$S_{Cz}^{\omega_0} = -\frac{1}{2}\frac{C_z}{C_1 + C_z}; S_{C_x}^{\omega_0} = -\frac{1}{2}\frac{C_x}{C_2 + C_x} \tag{6.26}$$

$$S_{R_1}^{\omega_0} = -\frac{1}{2}\frac{R_1}{R_1 + R_n}; S_{R_n}^{\omega_0} = -\frac{1}{2}\frac{R_n}{R_1 + R_n} \tag{6.27}$$

$$S_{R_z}^{\omega_0} = -\frac{1}{2}\frac{R_z}{(\beta_z \alpha_n g_m R_z + 1)} \tag{6.28}$$

$$S_{\beta_z}^{\omega_0} = S_{g_m}^{\omega_0} = S_{\alpha_n}^{\omega_0} = S_{\beta_z}^{Q_0} = S_{g_m}^{Q_0} = S_{\alpha_n}^{Q_0} = \frac{1}{2}\frac{\beta_z \alpha_n g_m R_z}{(\beta_z \alpha_n g_m R_z + 1)} \tag{6.29}$$

$$S_{C_1}^{Q_0} = \frac{1}{2}\frac{C_1}{C_1 + C_z}\frac{(R_1 + R_n)(C_2 + C_x)}{[R_z (C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)]} \tag{6.30}$$

$$S_{C_2}^{Q_0} = \frac{1}{2}\frac{C_2}{C_2 + C_x}\frac{(R_1 + R_n)(C_2 + C_x)}{R_z (C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)} \tag{6.31}$$

$$S_{Cz}^{Q_0} = \frac{1}{2}\frac{C_z}{C_1 + C_z}\frac{(R_1 + R_n)(C_2 + C_x)}{[R_z (C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)]} \tag{6.32}$$

$$S_{C_x}^{Q_0} = \frac{1}{2}\frac{C_x}{C_2 + C_x}\frac{(R_1 + R_n)(C_2 + C_x)}{[R_z(C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)]} \tag{6.33}$$

$$S_{R_z}^{Q_0} = \frac{1}{2}\frac{R_z}{(\beta_z \alpha_n g_m R_z + 1)}\frac{\beta_z \alpha_n g_m (R_1 + R_n)(C_2 + C_x) - (C_1 + C_z)}{[R_z(C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)]} \tag{6.34}$$

$$S_{R_1}^{Q_0} = -\frac{1}{2}\frac{R_1(C_2 + C_x)}{R_z(C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)} \tag{6.35}$$

$$S_{R_n}^{Q_0} = -\frac{1}{2}\frac{R_n(C_2 + C_x)}{[R_z(C_1 + C_z) + (C_2 + C_x)(R_1 + R_n)]} \tag{6.36}$$

From above equations, it is clear that all sensitivities are less than $1/2$ in magnitude for the proposed CD-DITA based VM-MISO universal filter.

6.4. Simulation results of proposed filter

To verify the working of the proposed CD-DITA based universal biquad filter, it is simulated using CMOS based CD-DITA (as shown Fig. 5.3). For this purpose the simulation is done using PSPICE software with 180nm process technology. The filter is designed for center frequency $f_0 = 7Mhz$ with quality factor of 1. To achieve $Q_0 = 1$, C_1 and C_2 are chosen as $5pF$ .Now to get $f_0 = 7Mhz$ using $C_1 = C_2 = 5pF$ the value of required transconductance comes out to be $g_m = 221.236\mu A/V$ and therefore the values of R_1 and R_2 are set to $1/g_m$ which is equal to $4.52k\Omega$. Theoretically the value of transconductance is related to MOS process parameters and bias current by the relation given by equations 5.13 and 5.14. If the values of parameters $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 12$, $\mu_p = 112.51 cm^2/V\sec$, $\mu_n = 296.84\, cm^2/V\sec$, $t_{ox} = 4.1\times10^{-9} m$ and $\varepsilon_{ox} = 3.9\varepsilon_0$ are put into equation 5.14, along with the required value of $g_m = 221.236\mu A/V$, then the bias currents required to design this filter turn out to be $I_{b3} = I_{b4} \approx 25\mu A$. Fig. 6.2 shows the responses of proposed filter: LPF, HPF, BPF and Notch. Fig. 6.3 shows the APF responses of proposed filter.

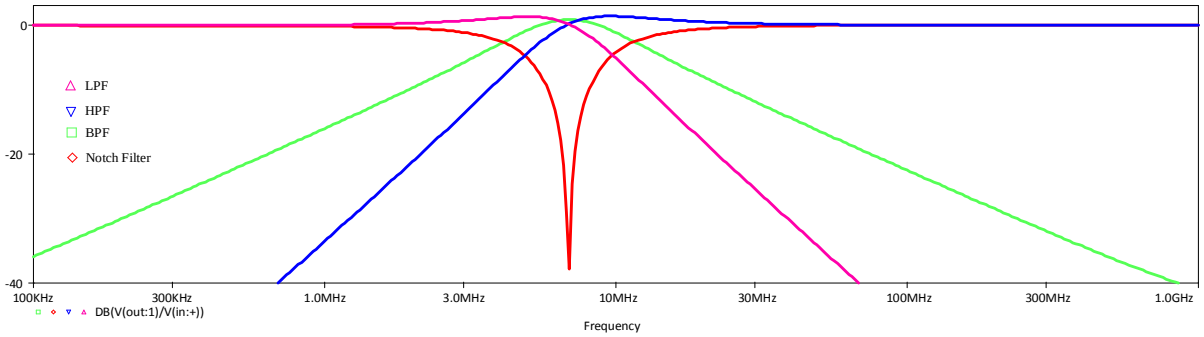
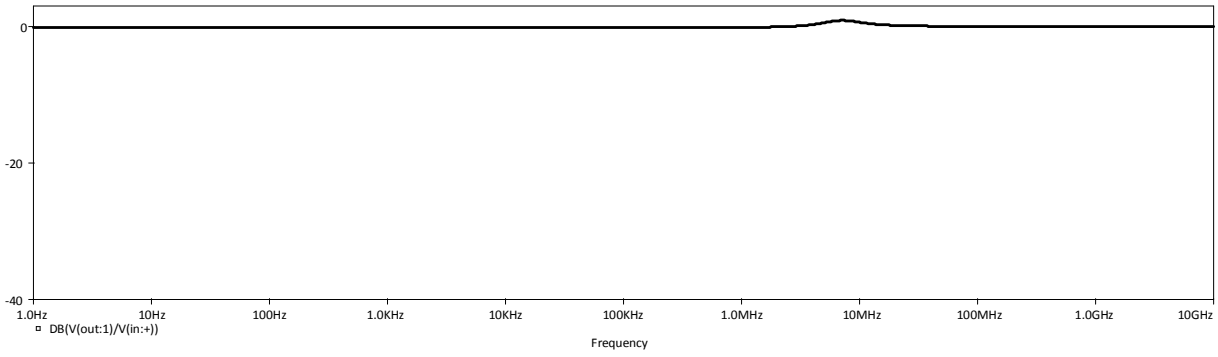
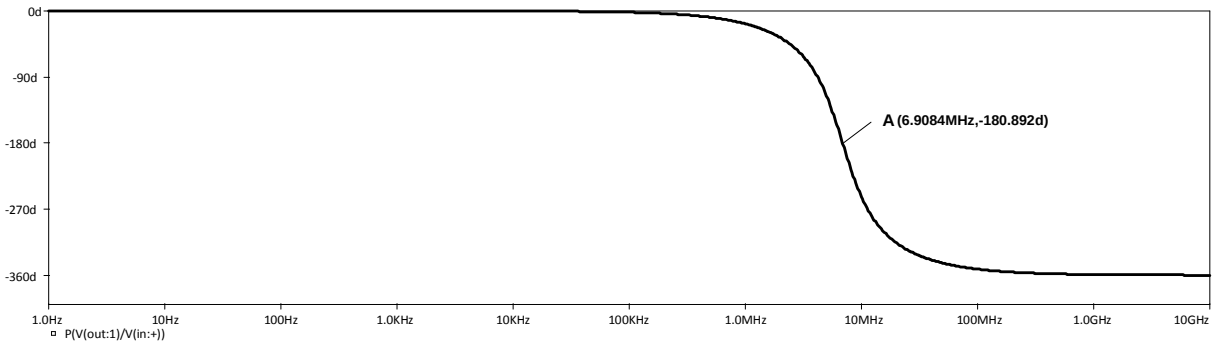


Fig. 6.2 Simulated filter responses of proposed CD-DITA based universal filter: LPF, HPF, BPF and Notch

Simulated center frequency can be measured using phase response of APF by measuring frequency at phase $= -180^0$. The measured center frequency using point A in phase response of APF is $f_0 = 6.9083MHz$ which is close to theoretical frequency.



(a)



(b)

Fig. 6.3 Simulated APF: (a) magnitude and (b) phase response of proposed CD-DITA based universal filter

Simulated BPF responses with the variation of bias currents I_{b3} and I_{b4} are shown in Fig. 6.4 Bias currents I_{b3} and I_{b4} are adjusted concurrently for the values of $15\mu A$ $20\mu A$, $25\mu A$ and $30\mu A$ thus having corresponding transconductance gain values $154.612\,\mu A/V$, $197.114\,\mu A/V$, $236.658\,\mu A/V$ and $273.722\,\mu A/V$. Due to this variation the center frequency is also varied. The values of variation in center frequency can be measured from Fig 6.4

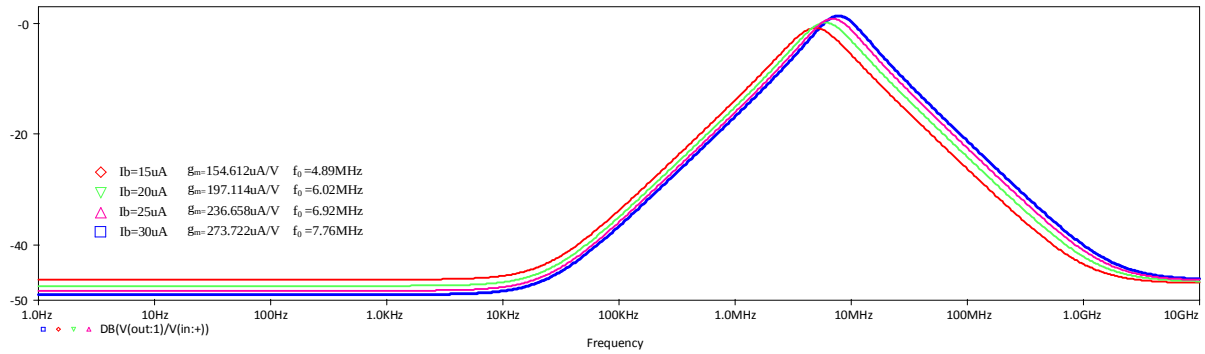


Fig. 6.4 Simulated multiple BPF responses with the variation of bias currents I_b

These simulated values of f_0 are slightly different from the theoretical values due to non-ideal nature of CD-DITA. Therefore if the simulated values of parasitic impedances and gains are considered for calculating f_0 (using equation 6.21), then it can be observed that the simulated values of f_0 are almost equal to those calculated considering non-ideal case of CD-DITA. The comparison results of these frequencies are enumerated in Table 6.1.

Table 6.1 Summary of comparisons of center frequencies

Bias current $I_b(\mu A)$	**Theoretical** $g_m(\mu A/V)$	**Simulated** $g_m(\mu A/V)$	**Theoretical** $f_0(MHz)$	**Simulated** $f_0(MHz)$	**Non-ideal CD-DITA** $f_0(MHz)$
15	171.369	154.612	5.454	4.897	5.132
20	197.879	197.114	6.274	6.025	6.213
25	221.236	236.658	7.042	6.908	6.947
30	242.352	273.722	7.714	7.762	7.597

Chapter

7. Conclusion and future work

This dissertation presents realization of a new CMOS based CD-DITA and its filtering application. In introductory chapter a brief on evolution of current mode signal processing is presented which leads to motivation for the work undertaken in this thesis. Detailed objective of the work is presented thereafter. A review of existing literature on design of CDTA block and voltage mode MISO type universal filters has been presented in second chapter. It is observed that both bipolar and CMOS technologies have been used for designing CDTA. A detailed review on CDTA structures is presented to lay background for new realization of CD-DITA presented in this work. FVF based CDTA block is realized and characterized in chapter 3 through PSPICE simulations. CDTA based applications are presented in Chapter 4 from which it can be concluded that CDTA true to its name, is an ideal current mode block. A new CMOS realization of CD-DITA has been presented in chapter 5. Various performance parameters of non-ideal CD-DITA that could affect filter performance were simulated along with the measurement of parasitics to use them in filter analysis. In chapter 6 a 2^{nd} order CD-DITA based VM-MISO-type universal filter has been proposed. The proposed filter provides the following advantages which are not exhibited simultaneously by few of the single ABB-based universal filters realizing all five filter responses:1) no need of inversion of i/p's, 2)independent electronic tuning of natural frequency and Q factor, 3) low sensitivities and 4)simultaneous realization of all filter responses without altering its topology. For validating the responses of proposed filter, it is simulated using new CD-DITA realization using 180nm technology and the results agree with the theoretical values.

The future work includes the generalization of CD-DITA universal filter to make it work in all possible modes: CM, VM and Mixed mode. Mixed mode enables user to select all kind of filter operations namely transadmittance mode, transconductance mode along with the conventional voltage and current modes. CD-DITA can also overcome the issues of usage of excess ABB and passive elements in realizing analog circuits, due to the availability of both current and voltage differential pairs. Apart from universal biquads, the future applications of CD-DITA can be in designing oscillators and other analog signal processing circuits.

RFERENCES

[1] R. Senani et al., Current Feedback Operational Amplifiers and Their Applications, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-5188-4_2,

[2] FERRI, G., GUERRINI, N.C. Low-Voltage Low-Power CMOS Current Conveyors. Cluwer Academic Publishers, 2003.

[3] TOUMAZOU, C., LIDGEY, F.J., HAIGH, D.G. *Analogue IC Design: The current mode approach*. IEE Circuits and Systems Series 2. Peter Peregrinus Ltd., 1990.

[4] D. Biolek, "CDTA – Building Block for Current- Mode Analog Signal Processing," Proc. European Conference on Circuit Theory and Design (ECCTD), 2003, Vol. III , pp. 397-400.

[5] W. Tanjaroen, T. Dumawipata, S. Unhavanich, W. Tangsrirat, W. Surakampontorn, "Design of current differencing transconductance amplifier and its application to current-mode KHN biquad filter," Proceedings of the ECTI-CON 2006, vol.2, Thailand, pp.497-500, 2006.

[6] A. Lahiri, A. Chowdhury, "A novel first-order current-mode all-pass filter using CDTA,"

[7] W. Jaikla, and M. Siripruchyanun, "Current Controlled Current Differencing Transconductance Amplifier (CCCDTA): A New Building Block and Its Applications," the proceedings of ECTI con 2006, Ubon-ratchathani, Thailand pp.348-351, May 2006.

[8] M. Kumngern, P. Phatsornsiri, K. Dejhan, "Four Inputs and One Output Current-Mode Multifunction Filter Using CDTAs and All-Grounded Passive Components,"

[9] A. Uygur, H. Kuntman, "Low -Voltage Current Differencing Transconductance Amplifier in a Novel Allpass Configuration," IEEE MELECON 2006, May 16-19, Benalmadena (Malaga), Spain

[10] Somdunyakanok M. et al. "CMOS multiple-output CDTA and its Applications" Proceedings of the 1st International Conference on Technical Education (ICTE2009) January 21-22, 2010 Bangkok, Thailand

[11] A. Uygur, H. Kuntman, A. Zeki, "Multi-input multi-output CDTA-based KHN filter," In Proc. of ELECO: The 4th International Conference on Electrical and Electronics. 2005, p. 46-50

[12] N. Pandey, R. Pandey, R. Choudhary, A. Sayal, M. Tripathi, “Realization of CDTA Based Frequency Agile Filter,”

[13] F. Kacar, H. Kuntman, “New CMOS Current Differencing Transconductance Amplifier (CDTA) and its Biquad Filter application”

[14] N. Pandey and S. K. Paul, “Single CDTA-Based Current Mode All-Pass Filter and Its Applications,” Hindawi Publishing Corporation Journal of Electrical and Computer Engineering Volume 2011, Article ID 897631, 5 pages doi:10.1155/2011/897631

[15] P. Singh, M. Dehran, I. Prabha Singh, R. K. Singh, “Universal Transadmittance Filter Using CMOS MOCDTA”

[16] M. Kumngern and K. Dejhan, “Current-Mode Multifunction Biquad Filter with Three Inputs Five Outputs Using ZC-CDTAs”

[17] A. R. Nasir & S. N. Ahmad, “Single CDTA Based Current-Mode Universal Filter with grounded Capacitors” International Journal of Electronics Engineering, 4 (1), 2012, pp. 73– 75

[18] D. Biolek, V. Biolkova & Z. Kolka, “Current mode biquad employing single CDTA,” Indian journal of Pure and Applied physics, vol. 47, july 2009, pp. 535-537

[19] W. Tanjaroen, W. Tangsrirat, “Resistorless current-mode first-order all pass filter using CDTAs,” Proceedings of ECTI-CON 2008

[20] A. Uygur, H. Kuntman, “Design of a Current Differencing Transconductance Amplifier (CDTA) and Its Application on Active Filters” (accepted). SIU'2005: IEEE 13th Signal Processing and Communication Applications Conference, 16-18 Mayıs 2005, Kayseri.

[21] D. Biolek, E. Hancioglu, and U. Keskin, “High-performance current differencing transconductance amplifier and its application in precision current-mode rectification,” AEU International Journal of Electronics and Communications, vol. 62, no. 2, pp. 92–96, 2008.

[22] A. Uygur, H. Kuntman, “CDTA-based quadrature oscillator design”, 14th European Signal Processing Conference (EUSIPCO 2006), Florence, Italy, September 4-8, 2006, copyright by EURASIP

[23] Prasad D., Panwar K., Bhaskar D. and Srivastava M. (2015) “CDDITA-Based Voltage-Mode First Order All Pass Filter Configuration”. *Circuits and Systems*, **6**, 252-256.

[24] SEDRA, A. S., SMITH, K. C. Microelectronic Circuits. 3rd ed. Florida: Holt, Rinehart and Winston, 1991.

[25] Horng JW. High input impedance voltage-mode universal biquadratic filters with three inputs using plus-type CCIIs. Int J Electron 2004;91(8): 465-75.

[26] Horng JW. Voltage-mode universal biquadratic filters using CCIIs. IEICE Trans Fundam 2004;87A:406-9.

[27] Sagbas M, Koksal M. Voltage mode three input single output multifunction filters employing minimum number of components. Frequenz 2007;61:87-93.

[28] Ranjan A. Paul SK. Voltage mode universal biquad using CCCII. Active Passive Electron Compon 2011 [Article ID 439052].

[29] Herencsar N, Koton J, Vrba K Single CCTA-based universal biquadratic filters employing minimum components. Int J Comput Electr Eng 2009;1(3): 309-12.

[30] Chang CM, Chen HP. Universal capacitor-grounded voltage-mode filter with three inputs and a single output. Int J Electron 2003:90(6):401-6.

[31] Horng JW. High-input and low-output impedance voltage-mode universal biquadratic filter using DDCCs. IEEE Trans Circuits Syst II 2007;54(8):649-52.

[32] Horng JW. High input impedance voltage-mode universal biquadratic filter using two OTAs and one CCII. Int J Electron 2003;90(3):153-7.

[33] Kumngern M, Somdunyakanok M, Prommee P. High-input Impedance voltage-mode multifunction filter with three-Input single-output based on simple CMOS OTAs. Int Symp Commun Inf Technol 2008:426-31.

[34] Kılınç S, Keskin AÜ, Çam U. Cascadable voltage-mode multifunction biqu.ad employing single OTRA. Frequenz 2007;61 :84-6.

[35] Tangsrirat W, Channumsin 0. Voltage-mode multifunctional biquadratic filter using single DVCC and minimum number of passive elements. Indian J Pure Appl Phys 2011;49:703-7.

[36] Horng JW, Hsu CH, Tseng CT. High input impedance voltage-mode universal biquadratic filters with three inputs using three CCs and grounding capacitors. Radioengineering 2012;21(1):290-6.

[37] Shah NA, Malik MA. Voltage/current-mode universal filter using FTFN and CFA. Analog lntegr Circuits Signal Process 2005;45: 197-203.

[38] Pathak JK, Singh AK, Senani R. New voltage mode universal filters using only two CDBAs. ISRN Electron 2013 [Article ID 987867].

[39] Satansup J, Tangsrirat W. Single VDTA-based voltage-mode electronically tunable universal filter. In: The 27th International Technical Conference on Circuits Systems, Computers and Communications. 2012.

[40] Pushkar KL, Bhaskar DR, Prasad D. A new MISO-type voltage-mode universal biquad using single VD-DIBA. ISRN Electron 2013 [Article ID 478213].

[41] BIOLEK, D. CDTA – Building block for current-mode analog signal processing. In *Proceedings of the ECCTD03*. Krakow (Poland), 2003, vol. III, p. 397-400.

[42] D. Biolek, V. Biolková, "Modelling and Optimization of Active Filters by Hybrid "VIVMMC"- graphs", Systems and Control: Theory and Applications, World Scientific, Electrical and Computer Engineering Series, 2000, pp. 381-386.

[43] W. Tangsrirat, W. Tanjaroen, and T. Pukkalanun, "Current mode multiphase sinusoidal oscillator using CDTA-based all-pass sections," *AEU—International Journal of Electronics and Communications*, vol. 63, no. 7, pp. 616–622, 2009.

[44] Carvajal, R.G. et al, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Regular Papers Vol. 52, Issue 7, July 2005 pp.1276 - 1291.

[45] P.E. Allen and D.R. Holberg, "CMOS Analog circuit design," Holt Rinehart and Winston, Inc., 1987.

[46] R. Schaumann, M. S. Ghausi, K. R. Laker, "Design of Analog Filters", Prentice Hall, 1990.

[47] D. Biolek and V. Biolkova, "Current-mode CDTA based comparators", *in proc. the 13th International Conference on Electronic Devices and Systems (EDS)*, pp.6-10, 2006.

[48] Senani R, Singh VK. KHN-equivalent biquad using current conveyors. Electron Lett 1995;31:626–8.

[49] Khaled NS, Soliman AM. Voltage mode Kerwin–Huelsman– Newcomb circuit using CDBAs. Frequenz 2000;54:90–3.

[50] Ibrahim MA, Kuntman H. Transadmittance-type KHN-biquad employing DO-DDCC with only grounded passive elements. In: Proceedings of the ECCTD'03, vol. 1, Krakow, Poland; 2003. p. 279–82.

[51] Sanchez-Sinencio E, Geiger RL, Nevarez-Lozano H. Generation of continuous-time two integrator loop OTA filter structures. IEEE Trans Circuits Systems 1988;35(8):936–46.

[52] Keskin, A..U., Biolek, D., Hancioglu, E., and Biolkova, V.: 'Current mode KHN filter employing current differencing transconductance amplifiers', AEU- Int. J. Electron. Commun. Accepted for publication, 2005

[53] E. Alaybeyoglu, A. Guney, M. Altun, and H. Kuntman, "Design of positive feedback driven current-mode amplifiers Z-Copy CDBA and CDTA, and filter applications," Analog Integrated Circuits and Signal Processing, vol. 81, no. 1, pp. 109-120, 2014.

[54] Atasoyu, Mesut, et al. "Design of current-mode class 1 frequency-agile filter employing CDTAs." *Circuit Theory and Design (ECCTD), 2015 European Conference on*. IEEE, 2015.

[55] Armağan, E., & Kuntman, H. (2012). Design of balanced differential pair based CCCII circuit and configurable frequency agile filter application in 28 nm process. In Proceedings of ELECO 2012: Conference on Electrical and Electronics Engineering. (pp. 257–261) 29 Nov–01 Dec 2012, Bursa

[56] ARBEL, A. F., GOLDMINZ, L. Output stage for current-mode feedback amplifiers, theory and applications. *Analog Integrated Circuits and Signal Procesing*, 1992, vol.2, no. 3, p. 243 – 255.