IMPEMENTATION AND ANALYSIS OF ADDER CIRCUITS USING MODIFIED GLITCH FREE CASCADABLE ADIABATIC LOGIC

Submitted in
partial fulfilment of the requirements
for the award of the degree of

Master of Technology
in
VLSI Design and Embedded Systems
by

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Certificate

This is to certify that the work done in the thesis entitled **"Implementation and Analysis of Adder Circuits using Modified Glitch Free Cascadable Adiabatic Logic**" has been carried out by **Ms. Neha Raghav, Roll No. 2K15/VLS/11** under my supervision, in partial fulfilment of the requirements for the award of the degree of Master of Technology (M.Tech.) in VLSI Design and Embedded systems, at **Delhi Technological University, Delhi.**

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Candidate's Declaration

The work in this thesis entitled "**Implementation and Analysis of Adder Circuits using Modified Glitch Free Cascadable Adiabatic Logic"** is a record of original research work carried out by me under the guidance of Dr. Malti Bansal, Assistant Professor , Department of Electronics and Communication Engineering, Delhi Technological University, in partial fulfilment of the requirements for the award of the degree of Master of Technology in VLSI Design and Embedded systems at Delhi Technological University, Delhi. Neither this thesis nor any part of it has been submitted for the award of any other degree or diploma elsewhere.

Date:

Neha Raghav
(2K15/VLS/11)

Acknowledgement

To be candid, this project would never have been successful without the good wishes and hard work of few people. My primary debt of thanks is to my mentor **Dr. Malti Bansal,** Assistant Professor, Department of Electronics and Communication Engineering, Delhi Technological University, for giving me complete freedom to express my views and for her challenging questions and thoughtful feedback, as it clarified and strengthened the ideas. Also, for providing me a unique environment to conduct my thesis research work and for providing encouragement and institutional support from the start, allowing us to closely entwine into our project.

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Last but not the least, my parent's constant trust and faith on my abilities was like a giant shadow that sheltered me to complete this project successfully. This has been one of the greatest experiences of my life.

Neha Raghav

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Refereed Publications arising from this Thesis

1. Malti Bansal, Neha Raghav, "Flexible & Dry ECG Electrodes based on Carbon Nanotubes for Long- Term & Continuous Recording of Bio- signals," in *Proceedings of 3rd International Conference on Emerging Electronics (ICEE),* IIT Bombay.

2. Neha Raghav, Malti Bansal, "Analytical Study of High Performance Flip-flop Circuits Based on Performance Measurements*.", International Conference on Computing, Communication and Automation (ICCCA 2017),* pp. 1574- 1579.

3. Neha Raghav, Malti Bansal, "Analysis of Power Efficient 6-T SRAM Cell with Performance Measurements.", *accepted in International Conference on Innovations in Control and Information Systems (ICICCI), 2017.*

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MGFCAL : Modified Glitch Free Cascadable Adiabatic Logic

LPFA : Low Power Full Adder

LPHBF : Low Power Half Adder based Full Adder

LPRCA : Low Power Ripple Carry Adder

LPLCA : Low Power Look ahead Carry Adder

LPCSA : Low Power Carry Select Adder

LPHA : Low Power Hybrid Adder

TIPS : Tera Instructions per second

IC : Integrated Circuits

CMOS : Complementary Metal Oxide Semiconductor Field Effect Transistors

Ni-MH : Nickel- Metal Hydride

NiCd : Nickel Cadmium

ULSI : Ultra Large-Scale Integration

C_L : Load Capacitance

CPU : Central Processing Unit

GND : Ground

IoT : Internet of Things

RFID : Radio Frequency Identification

MUX : Multiplexer

ABSTRACT

Nowadays, power dissipation is among the most dominant concerns in designing VLSI circuits. Endless improvement in technology has points to an increased requirement for devices which have the basic characteristic of low power consumption. Hence, power has turned into a demanding design parameter in low power and high-performance applications. The Adiabatic logic technique is becoming a solution to the dilemma of power dissipation. The expression 'Adiabatic' indicates to the change of state that takes place without any loss or gain of heat. The power dissipation at the time of switching events can be reduced to a greater extent by using the adiabatic switching technique. Adiabatic logic is a promising design paradigm for low power circuits since the energy which is to be dissipated is recycled and reused back. In most of the digital circuits, digital signal processing and communication systems, multipliers play a major role where adders constitute the basic blocks. Adders with huge power consumption affect the overall efficiency of the system.

The research in this thesis unfolds the rising gravity of the issue of the power dissipation and explores different ways to curtail the problem.

This thesis includes in depth study of causes of power dissipation, ways of removing a power dissipation in the circuit by using modified GFCAL circuits, along with the proposed application of modified GFCAL technique in various adder circuits. Then, the comparison is made between the conventional CMOS circuit and the modified GFCAL circuit. The functionality and effectiveness of all proposed architectures are confirmed through intensive simulations on SYMICA Development Environment at 90nm technology parameters. All the above introduced circuits are simulated with supply voltage = 0.9 V, 1.2 V and 1.8 V to analyse the pattern followed with supply variation. Similarly, the calculation of delay is performed for temperature values of 27˚C, 55˚C and 120˚C at 90nm technology. Effect of proposed applications on the delay of the circuit has been analysed as well.

CHAPTER - 1

1 INTRODUCTION

1.1 Motivation

In this generation of digital world, electronic gadgets with fast applications are in incredible demand. Combined with this is the demand of compact gadgets like cell phone and tablet. In these devices, there is limited power budget. The recent approach to deal with this requirement is to move towards the lower technology node called scaling but this is not so straightforward and needs lot of optimization. According to Moore law, the number of transistors doubles almost every 18 months [1]. The current pattern of expanding the quantity of transistors within the same area prompts complex circuits, which is having conflicting impact on power and performance of a given circuit.

In the previous couple of decades, the electronics industry has been encountering an unpredictable spurt in the growth, because of the utilization of incorporated circuits in processing, broadcast communications and customer electronics gadgets. We have made some amazing progress from the single transistor period in 1958 to the present day ULSI (Ultra Large-Scale Integration) frameworks with more than 50 million transistors in a solitary chip [2].

The steadily growing number of transistors coordinated on a chip and the continuous increasing transistors exchanging speed in recent decades has empowered awesome performance changes in computer system by a few orders. On the contrary, such amazing execution changes have been joined by an expansion in power and increase in energy dissipation of the digital circuits. Higher power dissipation in digital VLSI circuits require more costly bundling and cooling techniques along with a significant increase in cost, and thus makes the system less reliable. In any case, the power and energy dissipation of highly reliable systems with better performance will be a basic plan requirement [3].

There are basically 2 significant types of power dissipation present in VLSI domain: -

(i) Static power dissipation

(ii) Dynamic power dissipation [1].

Static Power dissipation is mainly due to the internal leakage that is present in the device, when the circuit is in OFF state [4]. Dynamic power dissipation occurs when switching takes place in the circuit and is mainly due to the energy loss at the time of charging and discharging of the output node capacitance of a transistor. Therefore, static power dissipation and dynamic power dissipation have been the dominant matter for the designers [5] For the proper power reduction in the circuits, various divergent technologies have been popularised over the years which are sub-threshold logic technique [6], multi-threshold logic technique [7] and adiabatic logic technique [8]. For instance, high end microprocessors in 2010 are anticipated to utilize 100 crores of transistors at clock rates more than 30GHz to accomplish TIPS (Tera Instructions per seconds) execution [2]. These high number of transistors, influence the power dissipation to thousands of Watts. This thesis explores the power dissipation in various CMOS adder circuits and proposes and analyse the techniques to reduce the power dissipation to a greater extent.

The basic component behind the VLSI designing is the digital CMOS based ICs for better performance and other different operations related to science and innovation. But right now, with the development of energy efficient gadgets [9] and biomedical field related applications that desires extremely low power consumption without affecting the other performance parameters to a greater extent, so a modern and different way need to be investigated so that the need for power saving is fulfilled [10].

Thus, nowadays, the requirement for decreasing the power dissipation is the significant matter for advanced digital devices. Also, utilization of adiabatic logic technique is the appealing answer for the most common issue of the advanced digital circuits for decreasing the dynamic power, which utilizes ramping supply voltage sources to recuperate the energy which would somehow or another be dissipated as a loss [11-12]

1.2 Demand of Low Power VLSI Design:

In VLSI chip design, power dissipation is customarily a disregarded subject. Earlier, the functional frequency as well as the device density were sufficiently low that it was not an obliging aspect in the chips. As the device density enhances, more transistors, speedier and littler than their antecedents, are being integrated onto a chip, which further prompt increment in power dissipation of the device [1]. The multiplication in Transistor count in Intel microprocessors is shown in fig 1.1[13] Further, it is estimated the leakage power is going to increment 32 times for each device by the year 2020 in view of the present situation [14].
The rate of energy delivered from the source to the device is known as the power dissipation of the device. Nowadays, Power dissipation is turning into an imperative limitation in a design. A few reasons underline the developing of this issue. Among them some are exhibited here:

The demand for battery powered systems such as laptop, computers, etc. desires that they have extended battery life. Numerous versatile applications for the small size portable devices utilize the rechargeable Nickel Cadmium (NiCd) batteries. Despite the fact that the battery business has been trying endeavours to create batteries with higher energy limit than that of NiCd, a fast increment does not appear to be impending. The normal change expectation of the energy density is 40% by the turn of approximately 100 years. Indeed, even with the new innovations in the battery, for example, Nickel-Metal Hydride (Ni-MH) which give energy density qualities (30 Watt-hour/pound), the average lifespan of battery is still considerably on the lower side. Since battery innovation has offered a restricted change, low power design procedures are basic for versatile portable gadgets and devices [2]. Low power is required for compact applications as well as to diminish or considerably lower the power of superior performance circuits. With huge number of transistors on a single chip and enhanced speed of operation, designs with larger clock frequencies are rising. These efficient designs are utilizing fast processors and related circuits which increment the power utilization. The cost related with cooling, bundling and fans required by these modules or design to expel the heat because of increased power dissipation, is expanding fundamentally. Thus, a need for low power devices is the major requirement in today's era.

As shown in Figure 1.1, the power utilization of the lead Intel microchips has been expanding fundamentally for approximately every generation in the course of recent years. The changes amid this period in terms of frequency is from a few MHz to 3 GHz. So, the figure shown below states that at higher frequencies, the power dissipation is excessive.

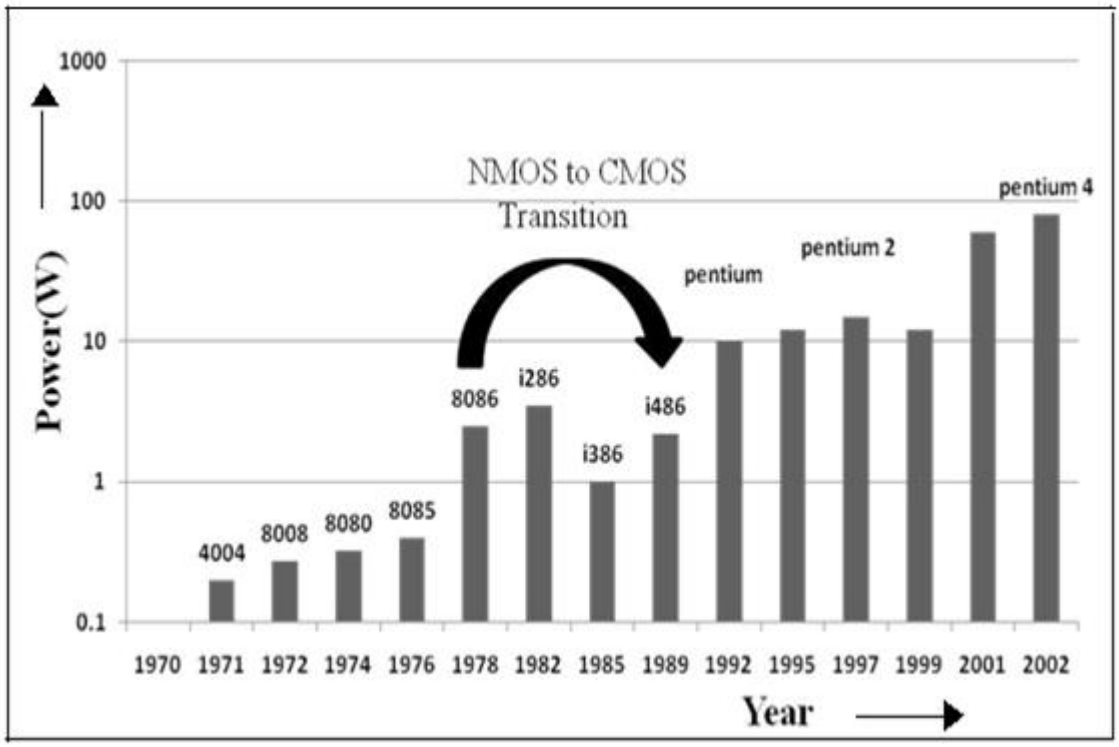

Figure - 1.1 Maximum power consumption of lead Intel Microprocessor [15]

Ultra Large- Scale Integration (ULSI) unwavering quality is yet another worry which focuses to the need of low power plan. There is a very great relationship between the power dissipation of circuits and reliability issues, for example, electro migration, heating problem in the device, requirement of excess cooling pads, etc Therefore, it can be stated the lowering of energy consumption is additionally urgent for reliable quality improvement. Fig 1.2 shows the total number of transistors in Intel microprocessors within a long span of time. The figure shows that there is great increment in the total number of transistors used as the years pass by. And with the ever-increasing number of transistors, further results in increase in total power dissipation of the circuits, it is for this reason power reduction in the device module is the main concern nowadays.

But the practices which are utilized to accomplish low power utilization in compact portable digital systems traverse an ample field, from device level to process level to algorithm level, device components used, sizing of transistors, interconnects used, voltage supply used along with the other parameters plays a vital role in minimizing the total power dissipated from the circuit. Circuit level and architecture level outline measures are basically utilized to accomplish low power utilization in the digital design circuits.

So certainly, a total power consumption by the digital circuits can be lessened by an appropriate choice of information handling algorithms, particularly to limit the quantity of switching in the given design.

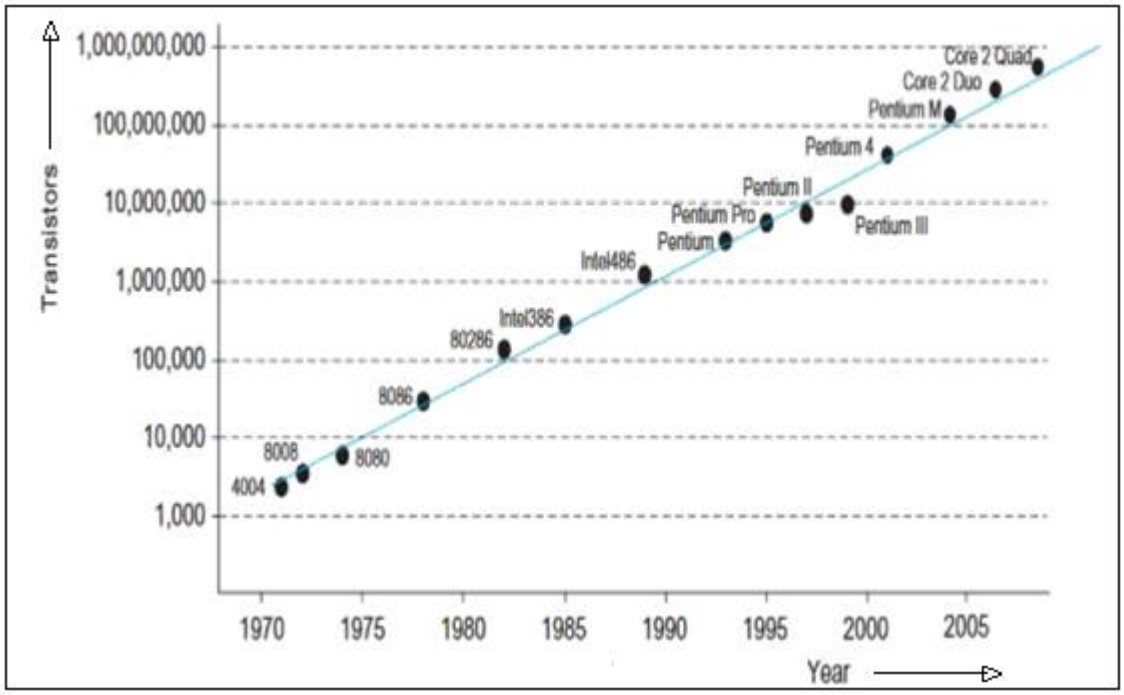

Fig 1.2:-_Total number of Transistors in Intel microprocessors [16]

1.3 Research Objective:

The fundamental inspiration to continue with this specific research is to execute a significant examination of circuit level techniques to balance the ever-increasing Power dissipation in the circuit with better advances and technologies and finally came up with a Modified Glitch Free Cascadable Adiabatic Logic Technique-A Technique of the adiabatic logic family and shows its applications in different VLSI design adder circuits. Adiabatic circuits are low power circuits which utilize "reversible logic" to preserve energy, it is for this reason it offers certain

points of interest over logic implementation utilizing ordinary CMOS logic style and consequently is on the brighter side. Limiting the power dissipation is the fundamental concern these days, it is for this reason designing those circuits which save power to a greater extent serves the purpose. This thesis is an endeavour to unfurl the power dissipation issue in digital adder circuits and propose new adder circuits which can be utilized as a part of advanced VLSI configuration circuits and save the power to a greater extent as compared to the conventional CMOS circuits. The goals of doing this thesis work are as follows:

- To cautiously study the patterns of dissipated power with fast innovation progress of technology.
- In depth study of several circuit level power reduction adiabatic logic technique.
- Appropriately applying the knowledge of CMOS Technique in various full adder circuits.
- In depth analysis of modified glitch free cascadable adiabatic logic.
- To analyse various logic gates circuit based upon MGFAL so that the power is reduced to the greater extent in the circuit.
- To introduce various adders like full adder, half adder based full adder, parallel adder, look ahead carry adder, carry select adder and the hybrid adder using MFCAL.
- Authentication of proposed adder structures by performing in depth simulation on SYMICA development environment at 180nm, 90nm, 65nm and 45nm technologies.
- Performing temperature variations and voltage supply variation for the proposed adder structures.

1.4 Organization of Thesis

The essential objective of this thesis is to establish a circuit level approach, for adoption in those designs which request outrageous low power dissipation. The content of this thesis is wrapped into seven major parts:

Chapter 1 i.e., the **Introduction**

This chapter introduces power consumption issues in the area of VLSI. This chapter also summarizes the need of low power design in the today's era of scaling down of technologies and nanotechnology. Finally, this chapter concludes with the research objective behind this thesis followed by the brief organisation of thesis.

Chapter 2 i.e., the **Power Consumption in VLSI Circuits** introduces about the types of power dissipation in the circuit along with the already existing techniques to mitigate or lessen that power dissipation in a circuit.

Chapter 3, i.e**., the Adiabatic Logic Technique** explains about the adiabatic logic technique along with merits and demerits of already existing quasi or partially adiabatic logic.

Chapter 4, i.e., **the Modified Glitch Free Cascadable Adiabatic Logic (MGFCAL)**, gives the brief introduction about the MGFCAL technique used in the proposed application for a power reduction in a circuit to a greater extent.

Chapter 5, i.e., **The Application of MGFCAL in various circuits**. This chapter explains the proposed adder circuits implemented through the MGFCAL technique.

Chapter 6, i.e**., Simulation and Analysis**. This chapter presents the proposed adder circuits which in turns reduces the total power dissipation in the circuit up to a greater extent along with this the comparison of the proposed circuits with the conventional CMOS circuit is also shown in terms of basic performance parameters like power, delay etc.

Chapter 7, i.e., the C**onclusion and Future Scope**, this chapter finally concluded the thesis work along with the future scope in which the proposed work can be used and is useful for the use in future aspects.

CHAPTER - 2

2 POWER CONSUMPTION IN VLSI CIRCUITS

2.1 Power dissipation in CMOS Circuit

In this chapter, the essential components of power dissipation in CMOS circuits is reviewed, which is followed by the techniques that were earlier used for the power reduction in the circuit. Excessive power consumption is an essential confinement to the further improvement in semiconductor industry. Distinguishing between the causes of power consumption is basic for creating power reduction methods at the manufacture fabrication technology, circuit level or at architecture level. There are fundamentally three sources of power dissipation in digital CMOS circuits.

- Dynamic Power
- Short- circuit Power
- Leakage power

So, the total power consumption of a CMOS circuit is shown in eq. 2.1:

$$P_{total} = P_{dynamic} + P_{leakage} + P_{short\text{-}circuit} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2.1)$$

2.1.1 Dynamic Power

The main cause dynamic power in the VLSI circuits is due to charging and discharging of the C_L (load capacitance). This capacitance comprises of gate internal capacitance, capacitance of the gate terminal of the transistor being disciplined by the fanout net and the value of capacitance of wire of the fanout net. The dynamic switching power does not depend on the type of switching gates, type of input waveform, neither on the rise and fall time of the input signal. On the contrary, it only depends on the voltage supply, the switching frequency of the circuit, and on the value of capacitance of a switching node [17].

The dynamic power can be determined by the equation shown below [18- 19].

$$P_{dynamic} = \frac{1}{2} C_{load} V_{dd}^2 f D \quad \text{.....(2.2)}$$

where,

$P_{dynamic}$= Total dynamic power dissipation

C_{load} = Capacitance of the load Terminal

f= Clock frequency

D = Transition density of the output

V_{dd}= Supply voltage

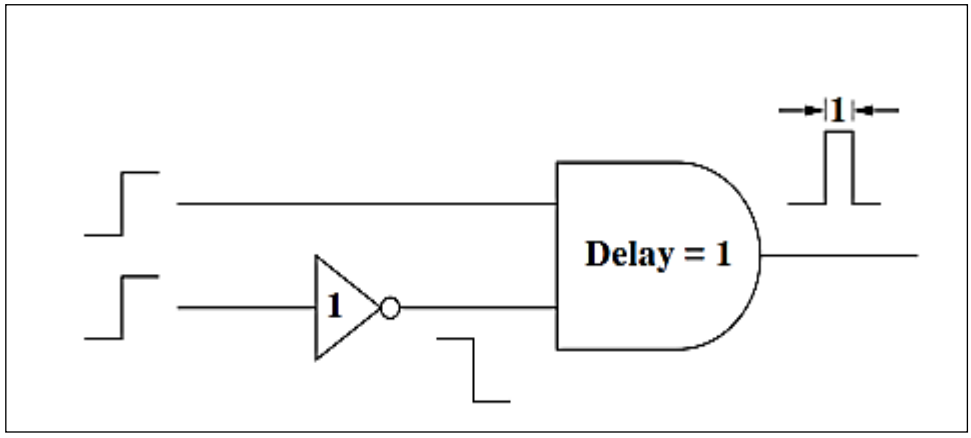

Fig 2.1: Static hazard example

All the while along a clock cycle, the average number of transitions is termed as Transition Density [20]. Thus, we can say that the total dynamic power dissipation present in the circuit is directly proportional to the total number of transitions present in the circuit. Earlier, the dynamic power contributed to majority of portion of power dissipation in the circuit but with the advancement in the deep sub- micron technology, the leakage current or we can say the static power dissipation is also considered as the important aspect [21]. The transition occurs in the circuit because of two main reasons:

(i) Switching activity which is quite essential for the correct working of the circuit.

(ii) Due to unnecessary transitions. The main cause of unnecessary transitions in the circuits is basically due to the unbalanced paths present in the circuit, and this is known as the glitching power.

2.1.2 Hazard and Glitch Power:

As depicted in equation 2.1, power consumption is increased to a greater extent by the increment in the count of transitions in the circuit and the resulted power consumption is termed as glitch power. These unwanted transitions are known as glitches. The basic cause of glitches in the circuit is due to the variation or we can say difference in the reaching time of the input signals at the input of any logic. Glitch power in the circuit ranges from 20% to as large as 70% present in the circuits like combinational adder circuits [22].

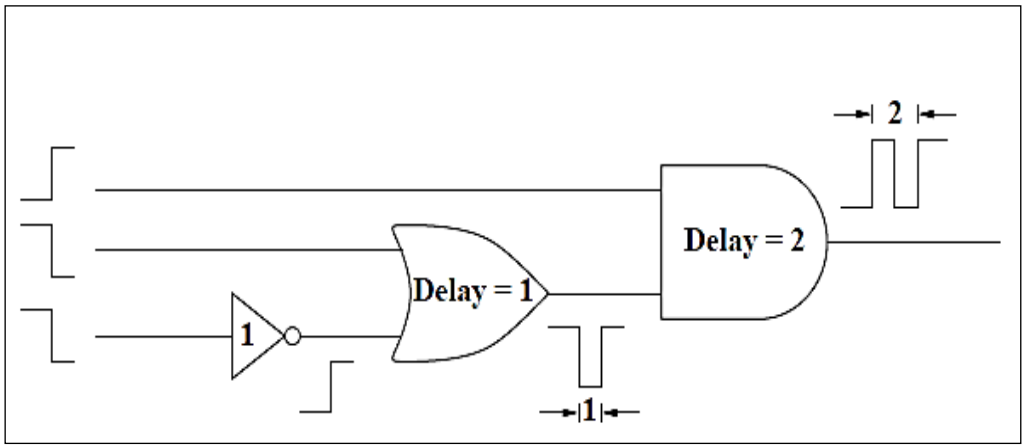

Figure 2.2: Dynamic hazard example

Because of the variation in the timing of the signal reaching the input of the AND gate, a sudden glitch is observed in the output which is of 1-unit width, which is equivalent to the delay of inverter and this is called as static hazard. As depicted in figure 2.2, the outcome of OR gate produces a static hazard of 1 unit. The transient at the output comprises of 2 rising and one falling edge, that is a sum total of three edges. And thus, we can say that it is a dynamic hazard with a width of 2 units.

A gate which is producing the hazard has greater than 1 input and has a non-zero greatest variation in the arrival time of the inputs of the gate. The amount of time in which the output changes after the change in the input is known as Inertial delay and it is contributed as a noteworthy part in altering the glitch that is produced in the circuit [23].

2.1.3 Short circuit power dissipation:

In static CMOS circuits, there is a period amid the transition of the input signals when both the pull up as well as the pull-down system transistors are all the while ON, subsequently it results

in a DC current path between the power supply and ground. The conduction of DC current by a CMOS circuit amid an input signal transient just because of non-zero value of rise time and fall times of the input signal is known as the short circuit current [24-25].

The short circuit power dissipation at the input of inverter is given by:

$$P_{short-circuit} = \frac{\beta}{12}(V_{dd} - 2V_T)^3 \frac{\tau}{T} \quad \ldots\ldots\ldots\ldots\ldots\ldots(2.3)$$

where,

V_{dd} = Supply voltage.

V_T = Absolute threshold temperature of NMOS and PMOS transistors

τ = Rise time or fall time of the input

T = Period of the signal

β = Gain factor of the inverter

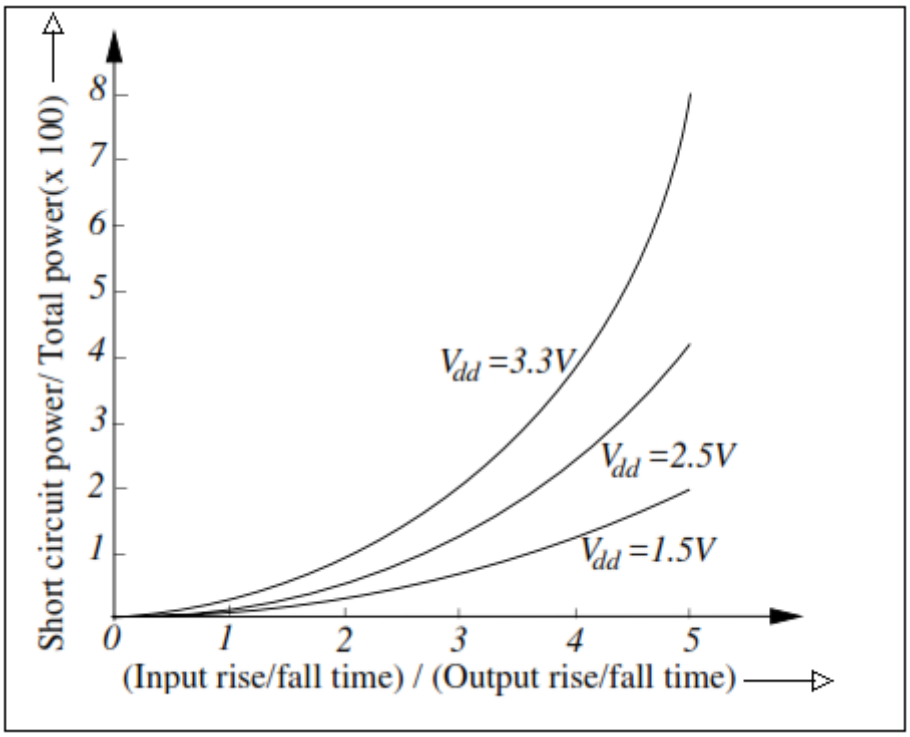

Fig. 2.3: Short circuit power dissipation versus input rise/ fall time [1].

Figure shown above depicts the graph between the short circuit power dissipation and the ratio of input rise/ fall time to the output rise/ fall time. [26.] Larger the value of ratio on the x- axis,

higher the value of short circuit power (average) incremented in the circuit.

2.1.4 Leakage Power Dissipation:

Leakage currents are mainly categorized into two parts:

(i) Reverse biased leakage current

(ii) Sub- threshold leakage current

The leakage current that flows through the parasitic diode amid the source and the body terminal is termed as reverse biased leakage current. On the contrary, the leakage current which flows through the channel of the device is termed as sub threshold leakage current [1]. Furthermore, added objection such as that of process variation, leads to tremendous increment in the leakage power [27-29].

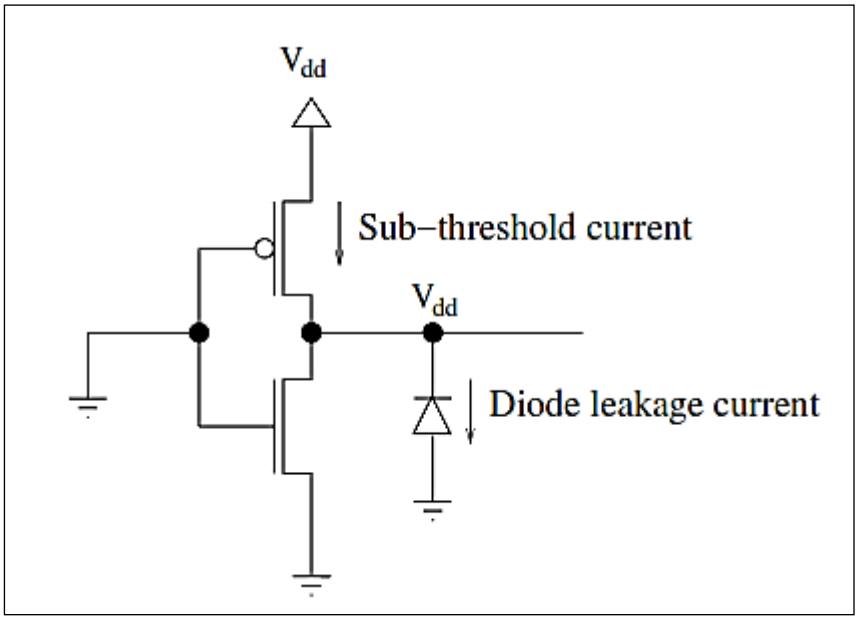

Fig 2.4: Leakage current in an inverter [28].

Diode leakage current occurs when the transistor is turned OFF, and another active device charge up or discharges the drain with respect to the former's bulk potential. Let us consider the above figure, when the input applied is low, then the PMOS is turned ON While the NMOS is turned OFF. And output charges to V_{dd}. The parasitic diode from output to the NMOS bulk is reverse biased with voltage V_{dd}.

This diode has a current to the substrate given by:

$$I_{leakage} = I_s \left(e^{\frac{qV}{kT}} - 1 \right) \quad \text{.....(2.4)}$$

where,

I_s= Reverse saturation current n the diode

V = Reverse biased voltage

q = charge on electron (1.602 ×10-19 C)

k = Boltzmann's constant

T = Temperature in Kelvin

So, as presented in Figure 2.3, leakage current will turn into the main cause of power dissipation in the coming years.

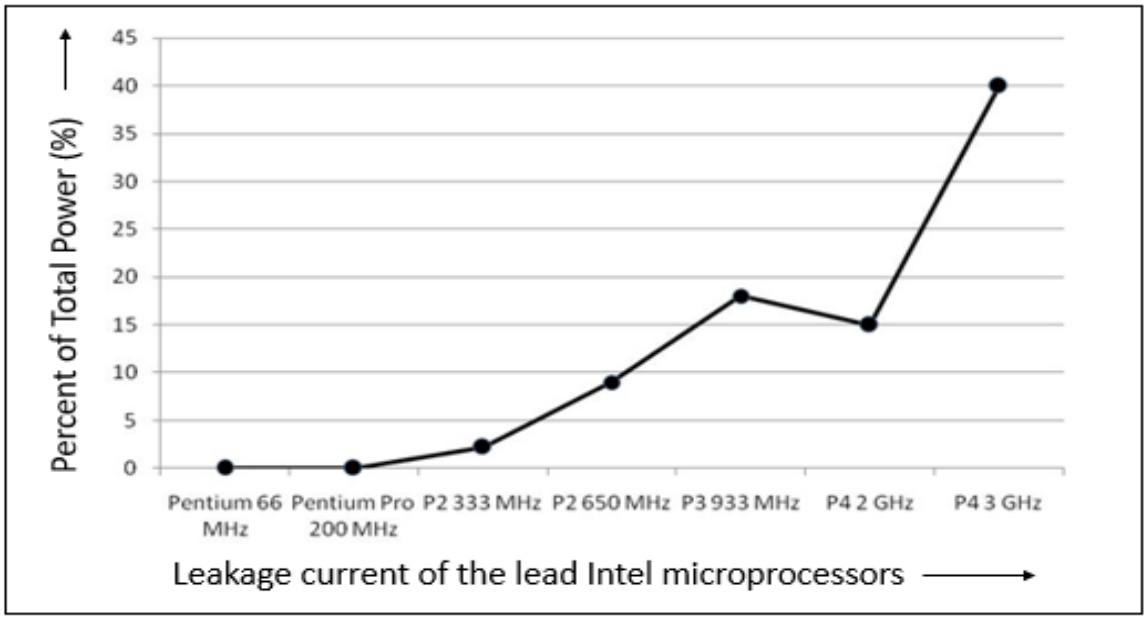

Fig.: 2.5 Increasing contributions of leakage currents to the total power consumption of the lead Intel microprocessors [30]

Also, the decrement in the threshold voltage results in increment in leakage power [31-34].

2.2 Low Power Design Techniques:

The low power design of the circuit can be realized at either at the circuit level by changing the circuit configuration without changing the desired result, or at the architecture level or at the programming level, where the programming of the whole circuit module is optimized. Sometimes a blend of one or more of these of approaches are utilized to save the overall power dissipation of the circuit design. The circuit level optimization for low power in the circuit includes lowering any one of the components as shown in eq. (2.1) and this is the most difficult task at circuit level for low power optimization. In the coming section, a concise study on various strategies used to get low power configuration are shown. The power per operation can also be lowered down by reducing the supply voltage, as the value of capacitance and threshold voltage still remains constant in the circuit, but on the contrary, it has one drawback that by increasing the value of supply voltage the value of delay is decreased. It has been shown in [35] that the relation between the delay, threshold voltage and the output capacitance is as follows:

$$t_d = \frac{k(CV)}{(V - V_{th})^2} \quad \text{.....(2.5)}$$

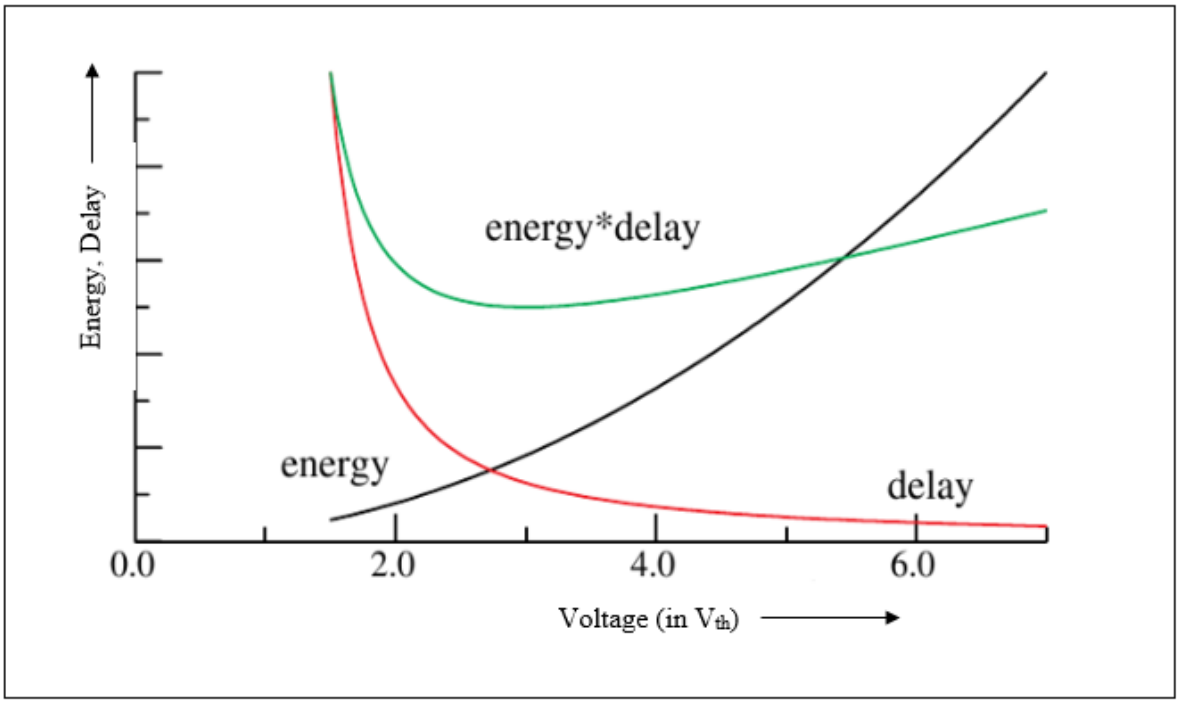

Fig 2.6: Energy, delay vs. Voltage [1]

By properly scaling of voltage, Figure 2.6, demonstrates a plot among energy, delay and energy delay product. At voltage level, much greater than the threshold voltage, decreasing the supply voltage decreases the overall power dissipation of the circuit without affecting the delay to much greater extent. On the contrary, at voltage level near the threshold of the device, even with a slight shift in the supply voltage, leads to great variation in the delay value along with the modest revision in the value of total power dissipation. At $V_{dd} = 3V_{th,}$ a minima is noticed and varying the value of supply voltage at this point does not disturb the energy- delay product to a greater extent. From the value $V_{dd} = 1.5V_{th}$ toward $V_{dd} = 6V_{th}$ there is a change of 8 in energy element that can be traded for delay without affecting the energy delay product largely.

2.2.1 Transistor Sizing:

By properly reducing the device size in the circuit, the value of the total power dissipation in the circuit can be decreased and by decreasing the dimensions of the device in the circuit, the value of capacitance due to gates of transistors is also decreased which further reduces the overall power consumption of the circuit. But scaling of the device size results in reduction in the current driving capability of the logic gates, which reduces the response time of the circuit to a greater extent along with increasing the delay of the circuit. But like in [35], using circuits which have smaller device size, contribute to low power design but on the contrary, it does not guarantee the energy efficient design as it affects other parameters also.

2.2.2. Technology Scaling:

One different way to correct the energy- delay product can be done by the technology enhancement process. In ideal scaling; by a scaling factor of $\gamma(<1)$, all the dimensions which are linear along with all voltages are decreased [36- 37]. As the scaling does not affect the electric field along with the wires present in the device, so the total current in the device as well as the capacitances of wire are also scaled by a factor of γ. As the scaling factor of γ is applied in voltage also, so the switching energy (CV^2) per transition also scaled by γ^3. So, the delay of individual logic gate enhances by γ ($td \approx CV/i$) . It is for this reason, there is the reduction by factor γ^4 in the energy-delay product. This concludes that if a scaling of 0.7 is introduced, then a chip can give the same performance at $(0.7)\ 4 \approx 0.25$ of the previous power consumption. But in ideal scaling, the threshold voltage V_{th} does not scale in tune with the supply voltage. Static power dissipation caused by leakage current through the off transistors

will limit how low the threshold voltage can be scaled. Even with constant voltage scaling, the reduced capacitance improves both the energy and delay, so their product scales as γ^2.

2.3 Dynamic Power Reduction:

There are two methods of reducing active power or dynamic power. They are:

2.3.1. Activity Reduction:

The total energy consumed is directly proportional to the frequency and the value of capacitance. This signifies that the power consumption in the circuit can be reduced by reducing the number of transitions that is there must be minimum switching activity in the circuit. For example: In the processor, a unit named program counter generally utilizes the binary code; that is on an average two bits are changed for each and every state transition. On the contrary, if gray codes are used in place of binary codes, then with each state transition only a single bit is changed. this result is energy saving in the circuit. Many such coding strategies have been accounted for in literature that yield different power saving in the circuit [38]. To reduce activity in synchronous logic, click gating [39] is used. Clock signal to a logic block is gated by a control signal, disabling clock when the particular logic block is not in use, thereby reducing the click signal activity and thus the overall active power consumption.

2.3.2 Supply Voltage Reduction:

Since power utilization decreases quadratically along the supply voltage, supply voltage cut back can bring about generous power saving in the circuit. There are mainly two approaches for the supply voltage cutback without trading off other performance parameters of the circuit; they are the static approach and dynamic approach [40]. In dynamic approach, the chip is intended to convey greatest performance at maximum value of supply voltage. For some applications, the performance parameter need not to be up to the mark, in those applications the chip can be operated at lower voltage which further results in reduction of power consumption by the circuit. The frequency and supply voltage can also be varied accordingly in respect to the performance need by the chip [41]. Let's consider an example of a mobile microprocessor unit. It identifies peaks in the waveform and according to the performance requirement it adjust the frequency and supply voltage to deliver the necessary performance parameter and in this way, saves power.

2.4 Leakage Reduction:

This commits finally to the total power dissipation of the circuit. As the leakage current is present in the circuit even when the device is turned OFF or is in idle state. With the advancement in the newer technologies in the present era, the leakage power is becoming a significant part in the total power dissipation of the circuit. Some of the techniques for decreasing leakage power are as follows:

2.4.1 Dual Threshold Voltage Technique:

The main motive behind using this technique is to minimize the sub threshold leakage power [42]. In this, the process technology adds 2 categories of transistors like:

(i) High threshold voltage (High V_t)

(ii) Low threshold voltage (Low V_t).

The high V_t transistors provide slower logic with minimal value of leakage. On the other hand, the low V_t transistors provide faster logic, but higher (about 10 times the slower ones) leakage. Thus, a proper use of low and high V_t transistors will provide better performance with lower leakage.

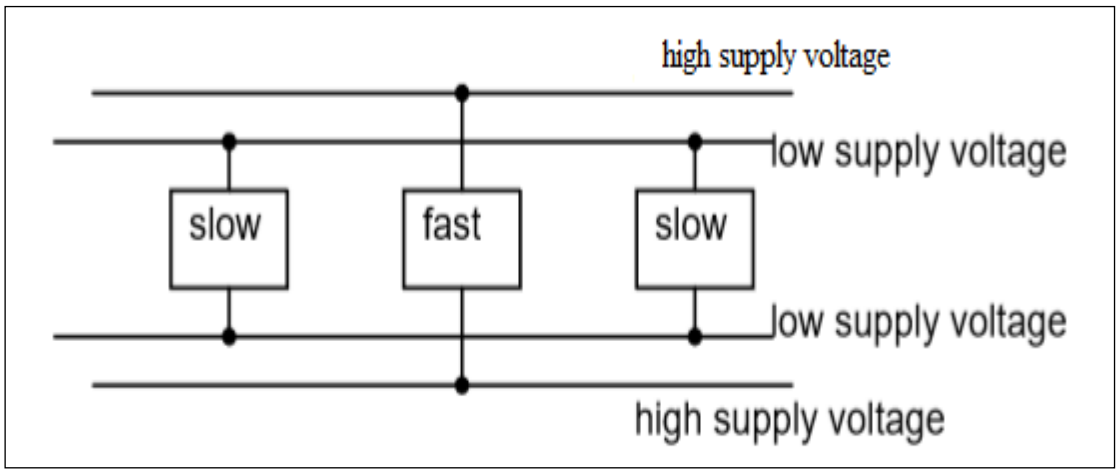

Fig 2.7: Scaling of static voltage using multiple supplies [42]

2.4.2 Stacking Technique:

This strategy is utilized to decrease the standby leakage power. It utilizes the evidence that an "off" transistor stack has lower sub threshold leakage magnitude in comparison to the individual transistor. To accomplish stack effect in standby mode, the logic block need to be placed in a state where all stacked transistors are turned OFF. This should be possible physically by the future tools improvements. A 1.5X to 2.5X dimensions has been accounted for utilizing this procedure [43].

2.4.3. Supply Gating:

This technique is also termed as “sleep transistor” technique. This method is utilized for the reduction of both active and standby leakage power [44]. This technique is quite comparable to the clock gating in which the power supply is “gated” by employing a high V_t transistor, so that the power can be cut off in a logic block. This method can lower the leakage currents by 1000X; along with the disadvantage of numerous unwanted issues in the circuit. First, the high V_t transistor in series with the supply causes performance degradation. Second, the noise immunity is also reduced to a greater extent in the circuit.

2.4.4. System and Architecture Level Power Reduction:

The previously mentioned circuit design techniques for power decrements in the circuit attempt to limit any one or more components of power dissipation as illustrated in eq. (2.1). The other approach for the power reduction can be done at the system level, where by properly altering the algorithm and data encoding, the power dissipation can be reduced to a greater extent. [45] For example, in reading a data block from the memory, requires signals to be sent from the CPU to the main memory. This signalling is decreased by implementing altered algorithms and employing cache memory structures which try to get the data as far as possible from the CPU registers or from the cache.

2.5. Adiabatic or Charge Recovery based Circuit Design:

Aside from the previously mentioned circuit level approaches, one especially fascinating method is the Adiabatic Circuit Design Technique [46]. Here the primary concern is the reusing of the charge that has been stored on the capacitive nodes at the output. Normally in ordinary CMOS circuits, the output capacitance either charged to power supply level V_{dd} at the logic 1

state or at the ground level at logic 0 state. Switching from logic 1 to logic 0 or vice versa during the discharging or charging of output capacitive node is merely a wastage of power in the circuit. Each time an output capacitance C is discharged from voltage V_{dd} to GND, an energy equivalent to $\frac{1}{2}CV^2$ is lost. Adiabatic circuits attempt to reuse this stored charge that in-spite of discharging to ground, is sent back to the power supply. The basic principle behind adiabatic logic is the charge recycling the charging procedure and the charge recovery process are efficient just when the charging voltage is gradually or slowly changing one. In the following chapter, the essentials of adiabatic circuits viz., The charging and releasing procedure of a capacitor in RC circuit and the power calculations are examined. Later a short depiction on the effectively existing adiabatic logic styles with their benefits and negative marks is given.

CHAPTER - 3

3 ADIABATIC LOGIC: AN INTRODUCTION

Adiabatic technique can be considered as a thermodynamic method which implies there is no gain and no loss of energy in the circuit. Adiabatic circuits utilize trapezoidal power clock unlike CMOS which has very short fall time and rise time [47]. In adiabatic logic, the energy can again be used in the power supply with the help of capacitors. The basic logic behind adiabatic technique is that it never allows both NMOS and PMOS to turn ON or OFF simultaneously. The term originates from the way that an adiabatic procedure is one in which the total heat or energy remains consistent in the system. For perfectly implementing adiabatic logic in CMOS structure, two essential principles are as follows:

1) The condition for the transistor to be ON is when both drain and source are at the same potential level.

2) When a current is flowing through the transistor, it never turns OFF the transistor [48].

The above mentioned two rules are realized to ensure that step variations of current are absent and in this way irrelevant energy dissipation can be avoided to a greater extent in the circuit. Energy stored in transistor switch is given by $\frac{1}{2} C_L V_{dd}^2$ [49- 51].

where,
V_{dd} = constant voltage supply
C_L = load capacitance

For power dissipation, this is the minimal limit in the CMOS circuit, although adiabatic technique works on lower limit. Power clock is an oscillatory voltage supply which is charging and discharging by ramp voltage so that the voltage drop is decreased across the switching transistor.

Adiabatic Techniques are basically categorized into two main types:

(i) Fully adiabatic logic
(ii) Quasi adiabatic logic or Partially adiabatic logic

In quasi or partially adiabatic logic, some portion of power is sent to the ground which implies some heat is disseminated from the circuit and some piece of the energy is reusable by sending it back to the power supply [52]. On the contrary, in fully adiabatic logic, no part of energy is wasted and all energy of the circuit is fed back to the power supply as all charges are recovered on capacitor and this saves the mere wastage of energy in the circuit and these types of logics are termed as fully adiabatic logic. The disadvantages of fully adiabatic logic are that the speed of operation of circuit is slower and it contributes to the more complex circuitry as compared to the partially adiabatic logic. Basically, adiabatic circuits works on the principle of "reversible logic" to conserve power and it is for this reason they are used in the circuit where low power is the major requirement [53].

In conventional CMOS level-restoring logic, with rail-to-rail output voltage swing the switching event of circuits results in an energy transfer from the power supply to the output node or from the output node to the ground which results in increased value of power dissipation in the circuit. On the contrary, it is not in the case of adiabatic logic, so we can say that Adiabatic Logic have accomplished noteworthy power saving as compared with traditional CMOS circuits [54].

Tremendous circuit designs based upon adiabatic logic have been proposed throughout the years [55- 69]. At the circuit nodes, to reuse the energy, adiabatic techniques use AC control clock as the power clock, which has four distinct periods of operation. In these adiabatic circuits, the charge flows back to the power supply rather than flowing from output capacitance to ground. In this manner, the charge or energy can be reused in the circuit [59], [70].

3.1 Adiabatic Principle:

The basic operation of adiabatic logic gate is partitioned into two specific stages: one phase is utilized for logic evaluation or assessment; while the other stage is utilized to reset the gate output logic value [71]. In the following section, conventional switching and adiabatic switching are discussed in detail.

3.1.1 Conventional Switching:

The two- noteworthy source of power scattering in traditional CMOS circuits are static power dissipation and dynamic power dissipation. The main cause of dynamic power dissipation in the circuit is due to the switching in the circuit from high to low and low to high. On the contrary, static power dissipation is administered by the logic states of the circuit. Switching in the circuit has no effect on the static power dissipation of the circuit. Static power dissipation arises in the circuit because of diode leakage currents, gate oxide leakage currents and subthreshold leakage currents.

Controlling Leakage power is a critical issue as it is dominating active leakage power components in deep submicron technology. The equation for leakage power is as follows:

$$P_{lkg} = I_{lkg} \times V_{dd} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3.1)$$

where,

P_{lkg} = Leakage power

I_{lkg} = Leakage Current

V_{dd} = Supply Voltage

The switching depicted in Fig. 3.1, illustrates about the conventional CMOS switching.

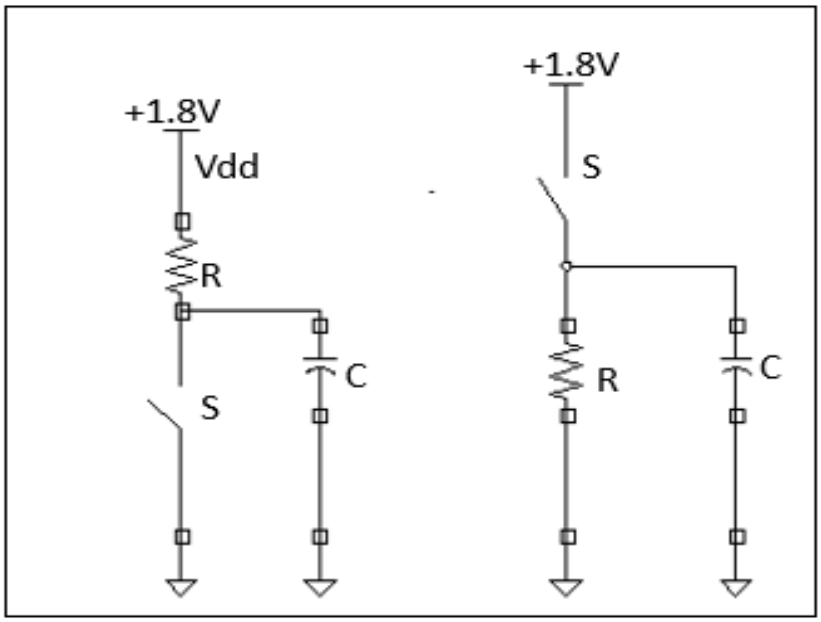

Fig 3.1: Conventional CMOS switching [72].

Dynamic power dissipation occurs due to switching in the circuit because of the charging and discharging of capacitance. At the time of charging the energy drawn from the power supply is equivalent to CV_{dd}^2. Half of this is dissipated instantly in the PMOS transistors and its interconnect and the other half is stored at the load capacitance C which gets dissipated over the NMOS and its interconnect. The main cause of short circuit is the slow transition of input signal from 0 to V_{dd} and V_{dd} to 0 volts. Subsequently, this results in the flow of short circuit current between the V_{dd} supply and the ground terminal [72]. The equivalent circuits of CMOS logic for charging and discharging is illustrated in Figure 3.1. The expression for total power dissipation is shown in eq. 3.2

$$P_{total} = \alpha C V_{dd}^2 f_{clk} + I_{sc} V_{dd} + I_{lkg} V_{dd} \ldots\ldots\ldots\ldots\ldots\ldots (3.2)$$

3.1.2 Adiabatic Switching:

An adiabatic technique is another appropriate answer to the biggest problem of power dissipation in the digital logic. The energy stored in the output capacitance is send back to the power in case of discharging in this way it saves the circuit power to a greater extent. The adiabatic switching circuit is illustrated in fig. 3.2.

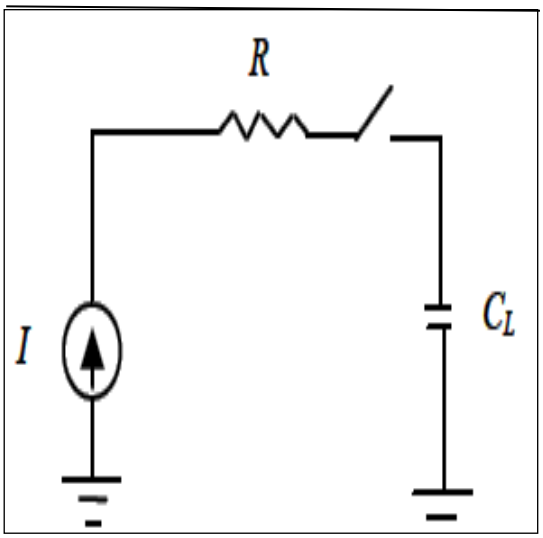

Fig 3.2: Adiabatic switching circuit [73].

Let RC be the time constant of the circuit, T be the voltage ramp period. The value of time constant of the circuit is kept much smaller than the voltage ramp period i.e., RC << T.

So, the voltage at the capacitor strictly follows the supply voltage, so the potential difference measured across the resistor R is very close to zero. So, it implies that the voltage at the capacitor V_c is also a constant ramp signal with slope V/T.

where,

V= Supply voltage swing

T = Power- clock phase period.

The charging current of the adiabatic circuit can be given as

$$I_c = C\frac{dV_c}{dt} = \frac{CV}{T} \quad \text{……..……..…(3.3)}$$

And the energy dissipated in the resistor can be evaluated using equation 3.4.

$$E = i_c^2 RT = (\frac{CV}{T})^2 RT = \left(\frac{RC}{T}\right) CV^2 \quad \text{……(3.4)}$$

The equivalent circuit for discharging is also completely same as that of the charging circuit, the only difference is that the supply voltage ramps down in the discharging circuit.

As we know that, RC << T, so we have

$$E = \left(\frac{RC}{T}\right) CV^2 \ll \frac{1}{2} CV^2 \quad \text{……(3.5)}$$

The equation (3.5) signifies that the energy dissipated by the resistor during charging and discharging is less than the energy stored in the capacitor. So, this concludes that at the time of discharging, some part of energy which is stored in the capacitor is actually send back to the energy source. [72]

3.2 Power Clock used for Adiabatic Switching:

The noteworthy part of the entire adiabatic system is the structure of its power clock generator. The power clock utilized here is a mixture of power supply and a clock. This signifies that it comprises of both frequency and voltage levels. In adiabatic circuits, the power clock is multi-phase in nature [74.].

The power clock of the adiabatic process is broadly classified into four phases. These phases signifies a different levels used for the specific operations performed in the circuit. The basic structure of the power clock is illustrated in fig. 3.3.

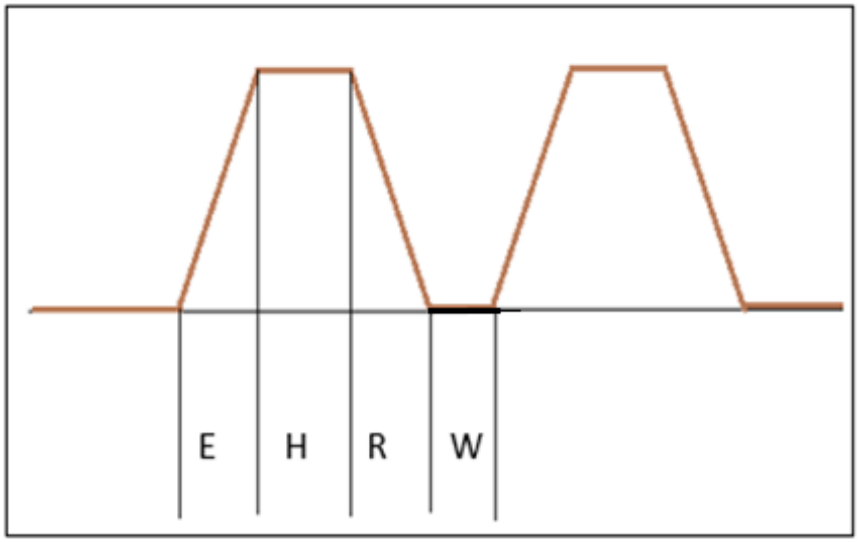

Fig 3.3: One cycle of power clock in adiabatic technique. [73]

Power clock used in adiabatic technique shown in figure 3.3, comprises of four different phases. These are:

(i) Evaluate (E)
(ii) Hold (H)
(iii) Recovery (R)
(iv) Wait (W)

In E interval, i.e., in the evaluation phase, the outputs get evaluated from the stable input signal.

During H interval, i.e., the Hold phase, the output is kept stable to provide input to the next stage.

During R interval, i.e., the recovery phase, the energy gets recovered and

W interval, i.e., the wait interval provides symmetry.

3.3 Classification of Adiabatic Logic Families:

There are basically two types of adiabatic logic families:

(i) Partially Adiabatic or quasi adiabatic logic family.

(ii) Fully Adiabatic logic families.

In partially adiabatic or quasi adiabatic circuits, a portion of charge is sent to the ground, that is some heat is dissipated in the circuit. And the other portion of energy is recovered and is sent back to the supply. The advantage of using the partially or quasi adiabatic logic circuit is that the implementation of circuits is easy as compared to the fully adiabatic logic families.

On the contrary, in fully adiabatic logic, no part of energy is wasted and all energy of the circuit is fed back to the power supply as all charges are recovered on capacitor and fed back to the power supply and this saves the mere wastage of energy in the circuit and these types of logics are termed as fully adiabatic logic. The disadvantages of fully adiabatic logic are that the speed of operation of circuit is slower and it contributes to the more complex circuitry as compared to the partially adiabatic logic.

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A few partially or quasi adiabatic logic families are as follows: -

(i) 2N-2P Adiabatic logic

(ii) 2N-2N 2D Adiabatic Logic

(iii) Efficient Charge Recovery Logic (ECRL)

(iv) Complementary Energy Path Adiabatic Logic (CEPAL)

(v) Two Phase Adiabatic Static Clocked Logic (2PASCL)

(vi) Quasi- Static Energy Recovery Logic (QSERL)

(vii) Glitch Free Cascadable Adiabatic Logic (GFCAL)

A few fully adiabatic logic families are as follows: -

(i) Pass Transistor Adiabatic Logic (PAL)

(ii) Two Phase Adiabatic Static CMOS Logic (2PASCAL)

(iii) Split-Rail Charge Recovery Logic (SCRL)

Some of the already existing quasi or partially adiabatic logic techniques are discussed here

3.3.1 2N- 2P Logic:

This 2N- 2P adiabatic logic was proposed by Denker et. al[75] . The name of the technique is derived from the total number of transistors in a gate. Each input needs 2 NMOS and the overhead for each complete gate is 2 PMOS transistors. Both differential input and differential output are used in tis circuit. So, both polarity of input is required at the input of the gate and the output of the gate produces both the logic function as well as its complement.
The basic circuit for an inverter-buffer is shown in figure 3.4.

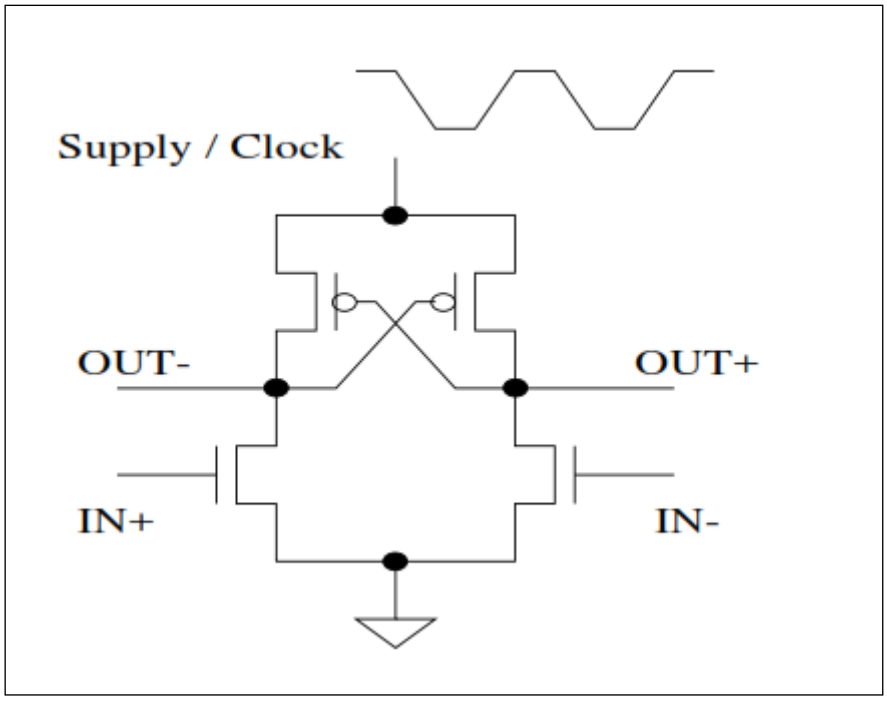


Fig 3.4: Basic 2N- 2P differential inverter/ buffer [76].

Each NMOS input gets the corresponding positive and negative polarity inputs and the cross-coupled PMOS are connected to the power clock. The timing and logical operation of fig. 3.4 is illustrated here. The basic circuit operation can be sub- categorized into 4 phases depending on the clock and input conditions. The NMOS inputs gets the positive and the negative polarity inputs and the PMOS are connected to the power supply. The timing diagram for the 2N- 2P buffer/ inverter is illustrated in the fig 3.5

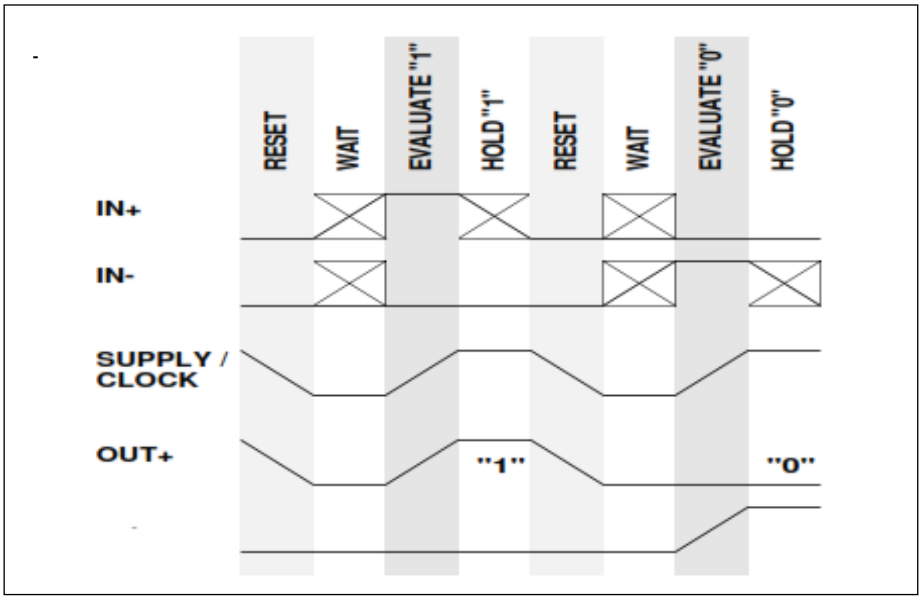


Fig. 3.5 : Timing for 2N- 2P inverter/ buffer [76]

Phase-1: RESET PHASE

The inputs are low, the outputs are in the manner that one output is low and other output is high and the power supply ramps down. As the PMOS is held in ON state by the low output, so the high output, will follow the clock down so that at the end of the reset phase both outputs will be low or at logic 0.

Phase- 2: WAIT PHASE

Power-supply is at the low level or at logic 0, so the output is kept low (as it is the crucial condition for the next logical gate, which suffer a delay by a quarter cycle, so that the reset operation is performed for the next logical gate and the inputs are evaluated. Because the gate is “powered down", so the evaluation of the inputs has no consequence on the state of the gate.

Phase- 3: EVALUATE PHASE

In this phase, the power supply ramps up and the outputs will evaluate to a complementary state. The half-gate with its input as logic 1 will have its output held low while the half-gate which have their input as low or at logic 0, will follow the ramp up. At the end of this phase, the outputs will always be complementary. This situation is assured by the inverse logic of the two half gates and their cross coupled PMOS’s and this is the main reason behind the 2N- 2P logic to be differential.

Phase- 4: HOLD PHASE

This is the last phase. In this complete phase, the power supply clock is high while the inputs ramp down to logic 0 and the gate outputs continues to be valid for the entire phase. Because there are four phases to the timing, there must be four quadrature clocks in a complete system, each clock 90 degrees in advance of the previous clock. In this way, each logic phase in the system holds its outputs valid while its successor is evaluating (ramping up) and its predecessor is resetting (ramping down) and waits with its outputs both low while its successor is resetting (down) and its successor is evaluating (up) [76].

3.3.2 2N 2N-2D Logic:

This 2N 2N- 2D logic utilizes differential signalling and it is for this reason each signal is represented in two forms- its normal form and its complemented form. Downward pulse on c signifies logic 0 and downward pulse on d signifies logic 1. This technique also utilize the four stage power clock cycle. Fig 3.6, illustrates the 2N 2N - 2D inverter/ buffer circuit. At the start of the cycle the clock is at V_{dd}. When the clock changes from 0 to V_{dd}, the circuit starts operating in the evaluation phase. During the evaluation phase, the inputs must be held constant. Let us assume the case when a= 0 and b =1. Since a=0, no current flows in that branch and the output c remains high. But as both b and c are 1, so all transistors in the right evaluation made are ON. And signal d follows the clock down. The next phase is the HOLD PHASE. In this phase, the output is a valid logic signal and in this phase the value of input needs not to be constant as both and the signal are at the lower value in this phase and the condition of the right evaluation branch whether ON or OFF, does not affect the output. In the same manner, as signal d is low, it turns OFF the left evaluation branch and output d is set at 1, no matter what the value of the inputs are. Then the circuit operate in the recharge phase when the clock ramps up to V_{dd} and due to the presence of diodes, whichever output was low follows the clock to a logical high. Cascading such logic gates requires the second gate to be operated from a different clock as the output is valid only during the hold phase while the inputs are required to be valid during the evaluation phase [77 – 78].

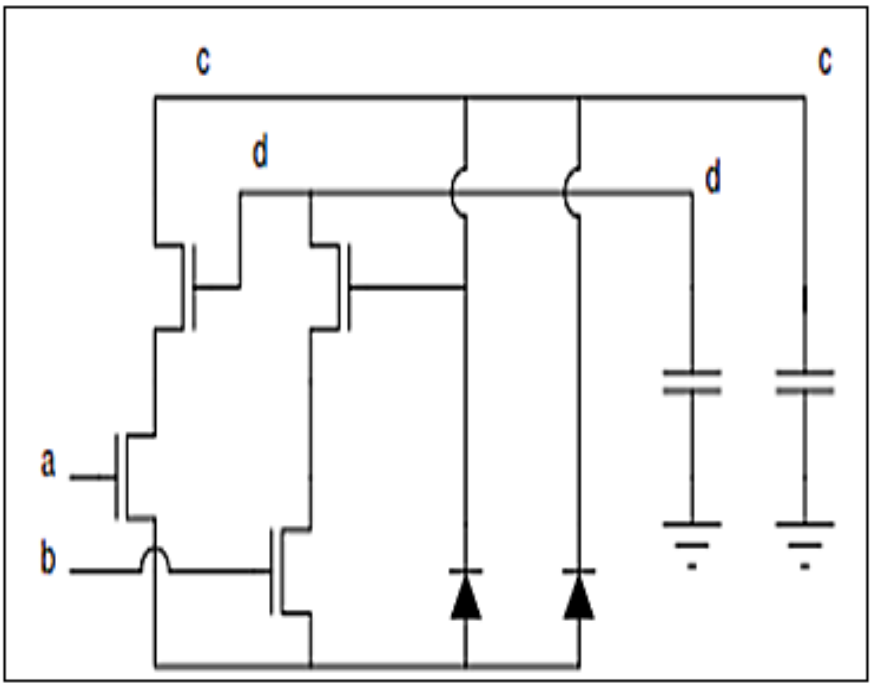


Fig 3.6: 2N2N-2D inverter/buffer [77].

3.3.3 Efficient Charge Recovery Logic (ECRL):

The ECRL adiabatic logic style was proposed by Yong Moon et. al [79-80]. A simple inverter circuit implementation using the ECRL adiabatic logic is shown in the figure 3.7. ECRL Technique also utilizes differential signalling, that is at the input terminal both the normal input as well as its complimented form is required. Let us consider a situation when the input "in" is at logic 1, so the compliment of the input "inb" is at logic 0, at the start of a cycle, when the clock phi ascends, the output terminal "out" stays at logic 0 level since "in" turn on MN2.So, "outb" follows phi1 through Mp1. The output will hold the valid logic as long as the phi1 is high for the utilization of these values in the next stage. While phi1 get back down to a ground level, charge on 'outb' send back its energy to phil. As there is no utilization of diodes, but still 4 phase clocking power is used for the appropriate pipelining of different stages.

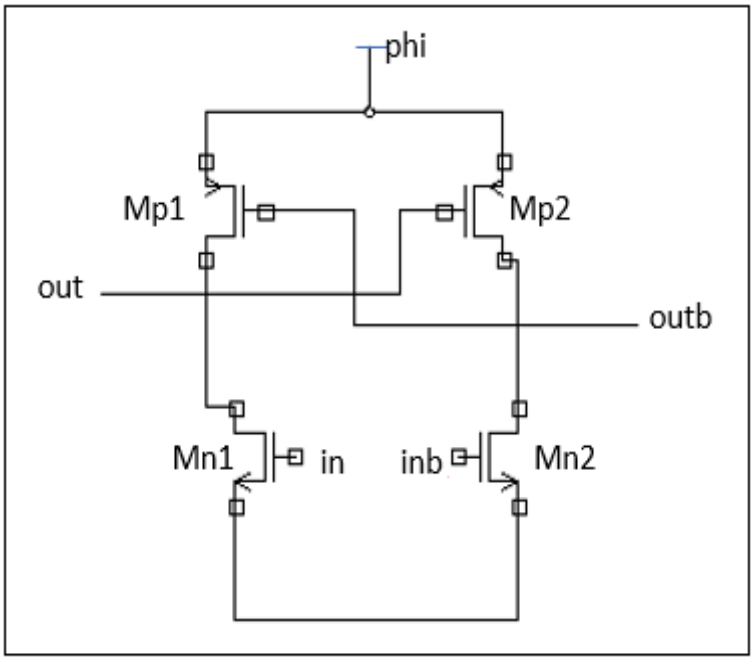


Fig 3.7: ECRL inverter/buffer [80]

3.3.4 Complementary Energy Path Adiabatic Logic (CEPAL):

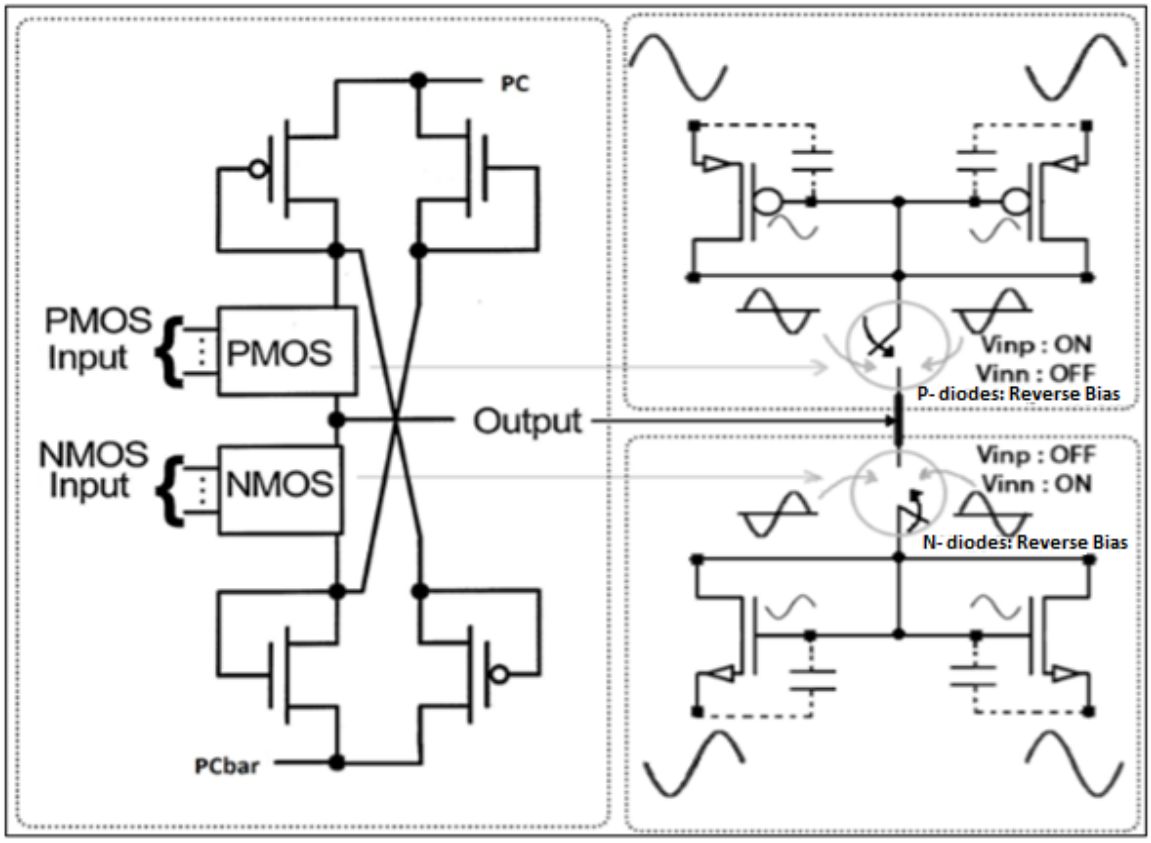


Fig 3.8: Complementary Energy Path Adiabatic logic[81].

The basic Structure and working of the CEPAL is shown in figure 3.8 [82- 83]. As illustrated in figure 3.8, it basically comprises of a pair of charging and discharging transistors; A pull up network (p-network) and a pull-down network (n-network).

This CEPAL logic utilizes two sinusoidal power clocks, PC and PC bar, that are just complementary of one another. Let us assume a condition when V_{in} is low, i.e. logic 0 at the input terminal makes the P- network ON and turns OFF the N- network, V_{out} follows the power clock PC or PC bar which ever swings to the high level. As the power clock used in the CEPAL Adiabatic Logic is sinusoidal in nature, so when it ramps down, it makes the V out to follow it and in this way a floating node is generated in the circuit. This condition can be avoided by the complementary clock which swings high, thus eliminating this weak high signal and also eliminating the hold state seen in two phase clock operated circuits. Similarly, the weak low signal is also eliminated by the complementary clock [84- 86].

Assume the other case in which V out is high with the P-network ON and the N-network is OFF. So, the value of Vout will remain high until there is some change in the input. In comparison to the QSERL technique, CEPAL technique has two extra diodes, but the two extra diodes do not affect the power dissipation adversely, as they are only meant for the charging and the discharging purpose and turning ON of these diodes takes place only at a particular instant of time. The advantages of the CEPAL logic over the QSERL logic is that the driving capability as well as the robustness is reduced to a greater extent in the circuit. The throughput of the CEPAL logic is not affected by the frequency ratio and the throughput is twice as better as the QSERL circuit. The disadvantages of using the CEPAL logic over the QSERL logic is that the two extra diodes in the charging discharging path, results in larger area on the chip [87].

3.3.5 Two Phase Adiabatic Static Clocked Logic (2PASCL):

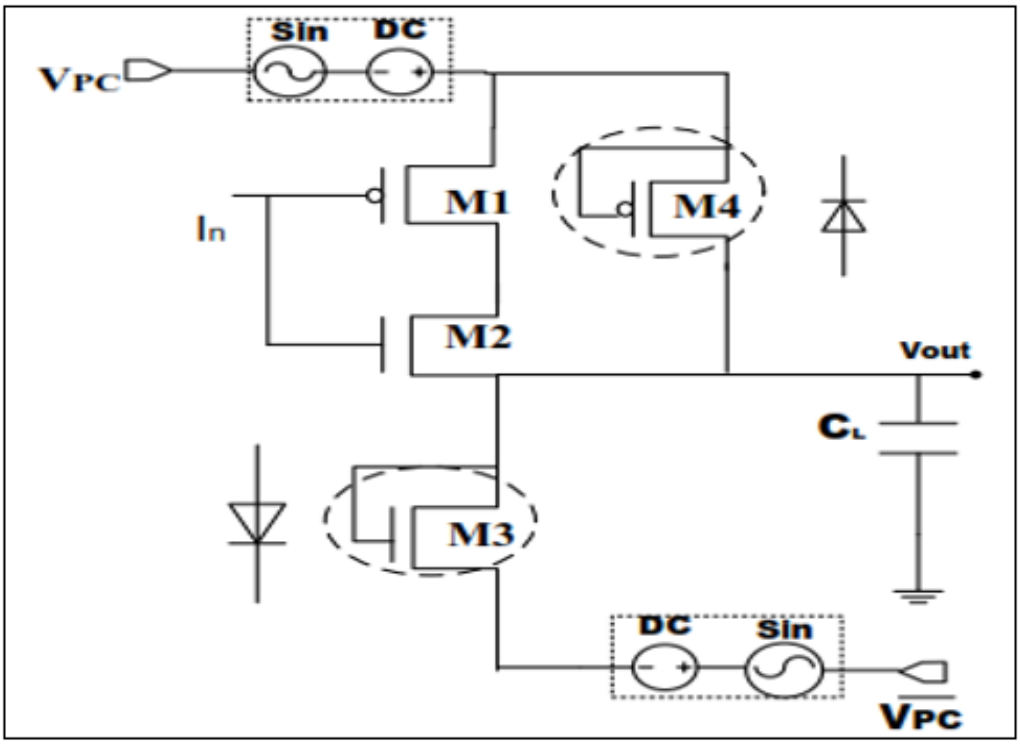


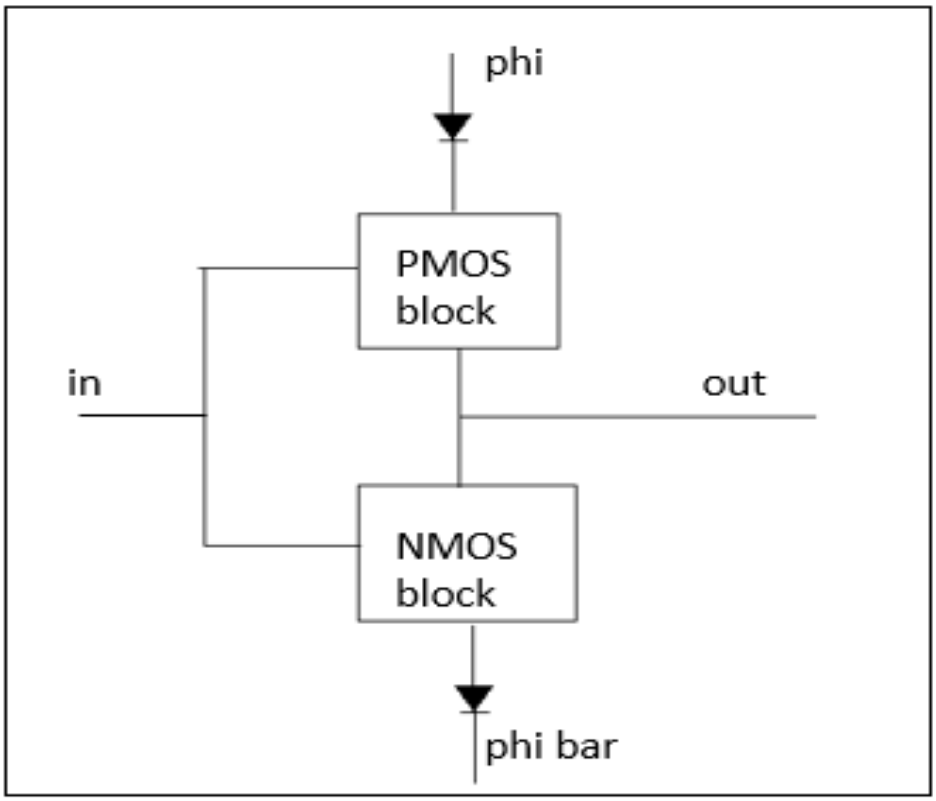
Fig 3.9: Inverter Circuit using 2PASCL [84].

The inverter circuit using 2PASCL is illustrated in figure 3.9. [84] In 2PASCL, at the time of charging, the flow of current is only via the PMOS transistor as there is no diode in the charging path. This will lower down the nun-adiabatic losses because of the cut in voltage of diodes. 2PASCL discussed here is quite different from the other quasi or partially adiabatic logic because in normal partially adiabatic logic ramp or sinusoidal power clocks are used. On the contrary, in the 2PASCL logic two split level sinusoidal power clocks are used.

The advantage of using this clock is that it results in the decrement in the voltage difference between the electrodes, which further results in decrement of the dissipated power. But the main disadvantage of this technique is that the performance is very much degraded by using this technique because the diodes are connected in parallel with the PMOS device and in series below the NMOS transistors for the purpose of recycling of charge [88- 89].

3.3.6 Quasi Static Energy Recovery Logic (QSERL):

QSERL proposed by K.Roy [90- 91] is similar to the conventional CMOS design along with the two extra diodes as illustrated in figure 3.10. Two diodes are basically used in the circuit for the charging and the discharging paths. One diode regulates the PMOS tree (P- Network) charging path while the other diode controls the NMOS tree (N- network) discharging path. QSERL is different from 2N2N-2D and 2N-2P in a way that, in QSERL technique two complimentary sinusoidal clocks are used. QSERL gates are totally identical to the conventional CMOS logic gates, the only difference is that of the two diodes; the diode on the top of PMOS block controls the charging path. The diode on the top of PMOS block is for the charging path, on the contrary the diode below the NMOS block is utilized for the discharging path. The power clock consists of two stages: the evaluation phase and the hold phase. In the evaluation phase, the clock phi swings up and as the clock phi and phi bar are complement of each other, so this makes the clock phi bar to swing down in the evaluation phase. And only one path is kept ON, that is either the PMOS pull up network (P- Network) or the NMOS pull down network (N- Network). Depending upon the present state of the gate, we have 4 cases which are helpful in determining the next state of the output [84], [91].



3.10: QSERL logic block [91]

Let the output node “out” be named as “X”. The 4 cases which are helpful in determining the next stage of the output are as follows:

1. If the node “X” is at logic 0 and the PMOS network is ON, then the present “X” will follow phi clock, as it swings HIGH.

2. If the node “X” is at logic 0 and the NMOS network is ON, then the present “X” will remain low and no transition takes place in the circuit.

3. If the node “X” is at logic 1 and the PMOS network is ON, then the present “X” will remain HIGH and no transition takes place in the circuit.

4. If the node “X” is at logic 1 and the NMOS network is ON, then the X follows complementary clock phi- bar as it swings down to LOW.

3.3.7 Glitch-Free and Cascadable Adiabatic Logic (GFCAL):

This was proposed by N.S Reddy [92] and the GFCAL Technique is the modified version of the QSERL explained earlier. The main advantage of using GFCAL Technique is that in this logic, just a single clock pulse is used in place of two complimentary clocks, Φ1 and Φ1bar which are used in most of the adiabatic logic technique. So, this logic utilizes a single triangular clock waveform. The complete process of charging is controlled by the diode D1 and the complete process of discharging is controlled by the diode D2.
The basic operation of the GFCAL Technique is illustrated in figure 3.11 using a simple inverter circuit. Likewise, QSERL, based upon the input and output condition, a total of four cases arise:

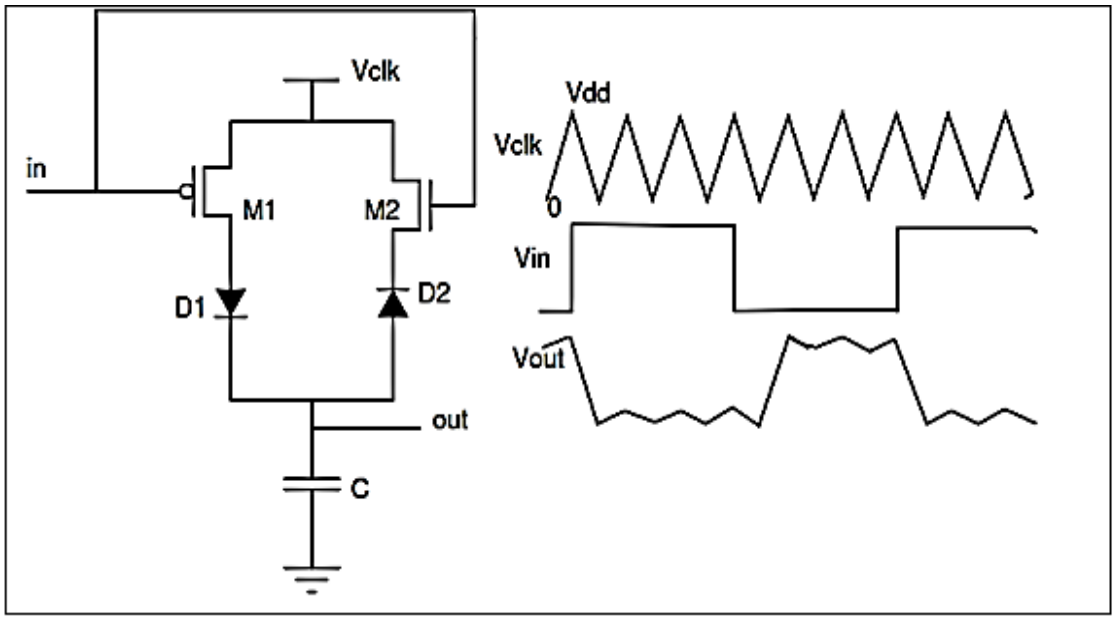


Fig 3.11: GFCAL inverter [92]

1. Rising Vclk and input LOW.

In this case, the transistor M1 is ON, M2 is OFF and the output capacitor is charged through M1 and D1 and this makes the complete charging of the output capacitor to Vclk and in this way logic HIGH is created at the output nude.

2. Falling Vclk and input LOW.

Because of the presence of diode in the circuit, there is no discharging in the circuit even when the clock pulse is falling. And the capacitor at the output node still remains charged. Thus, a LOW input is still giving a HIGH at the output.

3. Rising Vclk and input HIGH.

When the input is at logic 1, then it turns on M2 transistor and M1 transistor is turned OFF. And via M2- D2, discharging of output capacitor takes place in the circuit when the output is higher Vclk(t) at any point. This does not affect much change in the output, as this discharging occurs for a small interval of time in the circuit.

4. Falling Vclk and input HIGH.

In this situation, if the output capacitance is charged, then this situation makes the output capacitor to get discharged. Thus, logic 1 at the input, gives logic 0 at the output [93].

3.4 Overview:

The above reviewed quasi or partially adiabatic logic techniques have their own points of interest and drawbacks.

The 2N-2P and its modifications like 2N2P-2D,2N2P-2N have an advantage of lower power consumption. It has necessities like of differential inputs and multi-stage clock inputs, which are the disadvantages of the 2N- 2P logic block. The ECRL technique also suffers from lots of disadvantages like it also requires four-stage clocking. And use of Multi-stage clocking in the circuit, makes the clock circuit more complex and the power dissipation using the ECRL logic is also on the higher side in the clocking circuit. Also, it suffers from a major drawback of increased area. As for implementing a particular gate, quite larger number of transistors are used. Increased area problem is also in 2N- 2P logic. For example, for a M-input logic gate, the 2N2P-2N technique want 6M transistors, which are quite high in number which increase the area of the circuit to a greater extent. In adiabatic inverters, as the frequency increases, the power dissipation is also increased to a greater extent. But as compared to others, in QSERL and GFCAL circuit, has lower power dissipation up to a certain frequency level of 100MHz . Among all the techniques discussed, the QSERL technique has an positive point of lowest power dissipation among all the adiabatic techniques but the QSERL circuits suffers from floating node problem. So, GFCAL is the best choice for the power efficient circuits, where lower power is the major concern. The advantage of GFCAL logic is that it utilizes a single clock for its operation and also comparatively lesser number of transistors are used in GFCAL as compared to other adiabatic logic techniques and in this way, it conserves the area on the chip also. For any logic operation of N inputs, it needs 2N transistors along with two extra diodes. The diodes are used in the circuit for the charging and discharging operation in the circuit at the load capacitance. It also suffers from a smaller demerit of increased power dissipation, due to voltage drop across diode due to the cut in voltage of the diode and this increase the power dissipation whenever the current flows through the diode. The reported efficiency of 50% in the GFCAL circuit, [94] compared to conventional CMOS circuit can be more enhanced by some other technique which consumes comparatively lesser energy. By replacing the diodes by MOS transistors results in decrement of the power dissipation and this modified technique is shown in the next chapter. And the application of these MGFCAL in the field of adder designing is the basis of this thesis. In the next chapter, a modified GFCAL inverter is discussed.

3.5 Application of Adiabatic Logic:

The development of Internet of Things (IoT) has expanded the research exploration for the designing of energy efficient circuit, which saves more power and along with the energy efficient they must be secure design of Radio Frequency Identification (RFID) and smart cards [94], the real major uses of smart cards and RFIDs are in the areas of finance, communication, electronics, data security, and so forth. With the rise of IoT, there is a pressing need to outline energy efficient and secure IoT based gadgets, for example, RFID, smart card etc. The change in the security of these gadgets prompts the decrease in its battery life. Battery life is regarded as an imperative parameter in ultralow-power devices. So, adiabatic logic is a better substitute approach to design secure and energy efficient circuits [94]. However, the disadvantage of adiabatic technique is that it can work properly in the frequency range from Hz to few MHz And the adiabatic logic techniques can work effectively at low frequency range. And adiabatic logic technique can be relevant in the applications where operation is done at lower frequency like RFIDs, smart card etc. in a properly energy efficient and secure manner. Let us consider an example of RFID tag which can operate effectively at 13.56 MHz frequency, which is in the range of the adiabatic logic for its proper functioning [95]. Adiabatic logic technique can also be used in the field of biomedical engineering, where low power devices are the major concern incorporated with the slower circuitry [96].

The interest for implementing those systems which have very low power dissipation in various modern applications like mobile systems, sensor networks, and implanted biomedical systems has expanded the significance of designing such logic circuits which can work at low power [96]. Low power multipliers with better performance parameters are important for high computational applications. At the multiplier level, the power advancement can additionally prompt tremendous power saving for the whole system [97].

CHAPTER – 4

4 MODIFIED GLITCH FREE CASCADABLE ADIABATIC LOGIC

The GFCAL logic talked about in the past section has its own disadvantages. Due to the existence of diode in the charging and the discharging path, when the current flows through the diode, the loss of energy takes place. Even, from a basic perspective, if a charge q passes through a forward biased diode having a cut in voltage of V; at that point an energy of qV is used.

On the contrary, this diode path for current flow is modified, which results in noticeable change in energy reduction. There are a few procedures to acknowledge adiabatic logic however most of them need compliment forms. So, another adiabatic logic system has been advanced which is capable of working with a single time varying supply voltage. The most tempting aspect of this MGFCAL procedure is that complementary inputs are not required.

The Modified Glitch Free Cascadable Adiabatic logic has been executed by including charging and discharging paths in the current standard CMOS logic, utilizing diodes and capacitors. Also, considerable improvement in the power dissipation is seen in different applications utilizing this MGFCAL Technique. The power supply is a trapezoidal waveform fluctuating in between 0 and V_{dd} [98].

4.1 Basic Structure of Modified Glitch Free Cascadable Adiabatic Logic (MGFCAL):

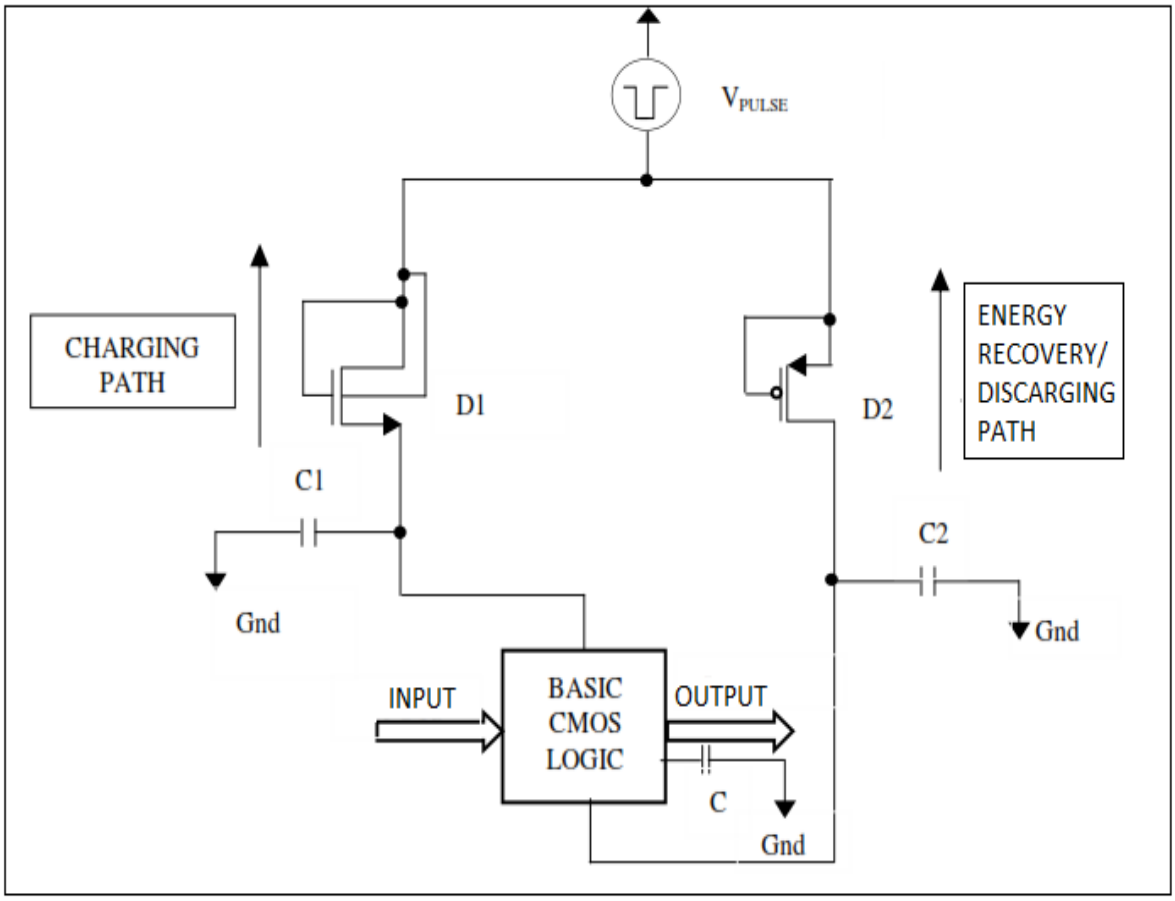


Fig 4.1: Modified Glitch Free Cascadable Adiabatic Logic Block [98].

The Modified GFCAL utilizes a single trapezoidal pulse power supply. Two MOS diodes are utilized in this technique, named D1 and D2. D1 is NMOS transistor along the charging path while D2 is PMOS transistor along the energy recovery path. This circuit is fundamentally an altered form of diode based adiabatic logic in which the power supply is accepted to be almost triangular in nature. However, the fundamental constraint of diode based adiabatic logic is that it results in degraded amplitude of output and the value of noise is quite high due to leakage current flowing in the diode.

To solve this problem, Modified Glitch Free Cascadable Adiabatic Logic technique is used which utilizes capacitors C1 and C2 in charging and discharging path along with MOS diodes. These capacitors absorb fluctuations and henceforth fluctuations are lessened to incredible degree in the circuit. Furthermore, in charging circuitry, dynamic body bias technique is used in the MOS based diode D1 [99]. This benefits in boosting the output swing

and lower the fluctuations at the output level. The conventional static CMOS logic circuit is connected between D1 and D2.

4.2 Operation of MGFCAL Circuit:

The operation of the circuit using Modified Glitch Free Cascadable Adiabatic Logic is depicted in fig 4.2, with the help of the inverter block.

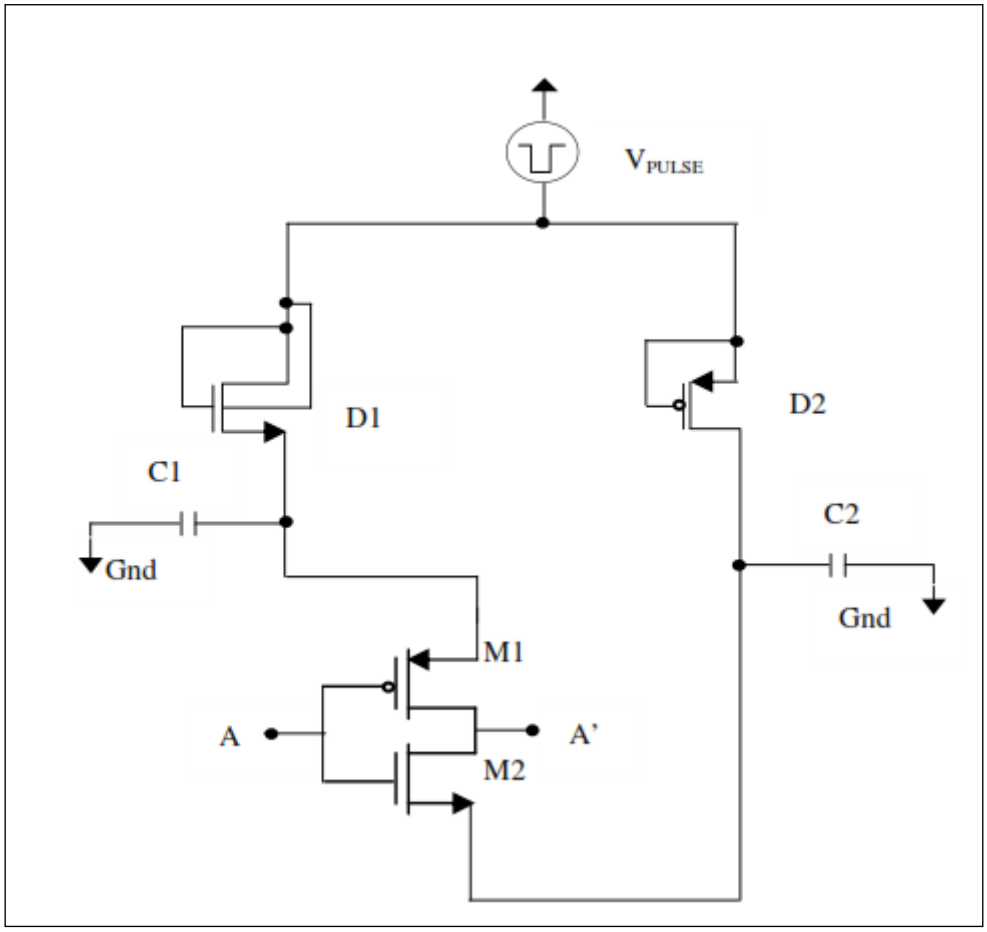


Fig 4.2: Low Power Inverter block using MGFCAL. [98]

The adiabatic inverter circuit depicted in fig. 4.2 is powered by a trapezoidal power supply and in between the charging transistor D2 and the discharging diode D1, the static CMOS inverter is connected. Let at output node A', the capacitance is not charged and the input at node A is logic '0'. Due to logic '0' at the input, as M1 transistor is a PMOS, so it turns on and as the supply surpass the cutin voltage V_{tn} of diode D1, it turns on and inverter output node A' charges via D1 and M1. Thus, a logic 0 at the input gives logic 1 at the output. Now, when at output node A' the capacitance is in charged state and the input at node A is logic '1'. The high input

level will turn on transistor M2 and D2 turns on as soon as the supply exceeds the cutin voltage V_{tp} of the diode D2. Thus the output node capacitance discharges through M2 and D2 and the charge is sent back to the power supply.

When the output capacitance at node A' is charged and the input is at logic low level '0'. Here M2 transistor will not turn on and thus the discharge path for output node back to the power supply is cut through M2 and hence the output capacitance does not discharge and the high output level is maintained. When the output capacitance node A' is uncharged and the input at node A is logic '1', transistor M1 will not turn on and the charging path via D1 is not completed, thus the output node remains at logic low level.

In the last two cases, it can be realized that dynamic switching does not take place, it is for this reason, the value of power dissipation is decreased to a greater extent [98].

4.3 Mathematical Model Of The Inverter Circuit Using Modified Glitch Free Cascadable Adiabatic Logic (MGFCAL):

The energy dissipated in the inverter block is calculated as follows:

(a) ENERGY DISSIPATED DURING CHARGING:

During the ON duration of the PMOS transistor in static CMOS inverter, since V_{dd} increases from 0 to V_0, the load capacitor C is charged through the capacitor C_1 and diode D_1 in the charging path shown in Fig.4.2. The voltage reaches a peak value V_0 in a time period T and its value $V_{dd}(t)$ at any time 't' is therefore given by Eq.(4.1) and Eq.(4.2).

$$V_{dd}(t) = V_o \frac{t}{T} \; when \; 0 \leq t \leq T \quad \text{.....(4.1)}$$

$$V_{dd}(t) = V_o \left[1 - \frac{(t-T)}{T}\right] when \; T \leq t \leq 2T \quad \text{.....(4.2)}$$

The voltage $V_{dd}(t)$ reaches a value V_B in a period T_{ch}, when the conduction of the diode starts. Let R_{ch} be the total resistance in the charging path.

The voltage V_C across the load capacitor 'C' for $t>T_{ch}$, is given as:

$$\frac{V_o}{T}t = V_B + R_{ch}\frac{C_1C}{C_1+C}\frac{dV_c}{dt} + V_c \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.3)$$

Assuming that :

$$T_{ch} > \frac{C_1C}{C_1+C}R_{ch}$$

On solving eq. 4.3, energy dissipated over the period 0 – T in the diode, capacitor C_1 and the transistor is obtained as:

$$E_{ch} \approx V_o\frac{C_1C}{C_1+C}\left(R_{ch}\frac{C_1C}{C_1+C}\frac{V_o}{T} + V_B\right)\left(1 - \frac{V_B}{V_o}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.4)$$

(b) ENERGY DISSIPATION DURING DISCHARGING:

When the PMOS is OFF and NMOS transistor in static CMOS inverter is ON, charging of the load capacitance is prevented and it starts discharging through the diode and capacitance C_2 in the discharge path till t_{dc} i.e. till V_c is higher than the supply voltage by at least V_B, when V_{dd} increased from 0 to V_o. The capacitance then stops discharging at t_{dc} and again continues discharging from 2T – t_{dc} until V_C= V_B.

Let R_{dis} be the total resistance in the discharging path. Assuming $CR_{dis} < t_{dc}$, the energy E_{dc} dissipated during discharging is the sum of energy dissipated during 0 to t_{dc} and (2T- t_{dc}) to 2T which is obtained as [99]:

$$E_{dis} \approx t_{dc}\left(2\frac{V_o^2}{T^2}\left\{\frac{C_2C}{C_2+C}\right\}^2 R_{dis}\right) - 2\,\frac{C_2C}{C_2+C}\frac{V_o}{T}B\frac{C_2C}{C_2+C}R_{dis} + V_BB\frac{C_2C}{C_2+C} + \frac{B^2}{2}\frac{C_2C}{C_2+C} \ldots(4.5)$$

where,

$$B = V_{CO} - V_B + R_{dis}\frac{C_2C}{C_2+C}\frac{V_o}{T}$$

The total energy $E_{dissipated}$ during one cycle of charging and discharging is given as

$$E_{dissipated} = E_{ch} + E_{dc} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.6)$$

Now putting the value of E_{ch} and E_{dc} in the above equation (4.6), we get

$$E_{dissipated} = V_o \frac{C_1 C}{C_1+C}\left(R_{ch}\frac{C_1 C}{C_1+C}\frac{V_o}{T} + V_B\right)\left(1 - \frac{V_B}{V_o}\right) + t_{dc}\left(2\frac{V_o^2}{T^2}\left\{\frac{C_2 C}{C_2+C}\right\}^2 R_{dis}\right) - 2\frac{C_2 C}{C_2+C}\frac{V_o}{T}B\frac{C_2 C}{C_2+C}R_{dis} + V_B B\frac{C_2 C}{C_2+C} + \frac{B^2}{2}\frac{C_2 C}{C_2+C} \quad \text{.....(4.7)}$$

where t_{dc} is given by:

$$t_{dc} = R_{dis}\left(\frac{C_2 C}{C_2+C}\right)\ln\left[\frac{V_{co} - V_B + \left(R_{dis}\frac{C_2 C}{C_2+C}\frac{V_o}{T}\right)}{R_{dis}\left(\frac{C_2 C}{C_2+C}\right)\frac{V_o}{T}}\right. \quad \text{.....(4.8)}$$

Thus Eq. (4.7), gives the theoretical expression for energy dissipation during charging and discharging cycles for the Modified Glitch Free Cascadable Adiabatic Logic circuit, it can therefore be implied from this equation that as T increases, the energy dissipation decreases. Here, T indicates the rate of variation of the supply. Also, this equation indicates that the power dissipation generally changes with capacitance values,V_o, slowly varying supply voltages and the equivalent series resistance due to MOS and diode.

4.4 Cascadabiity:

The fundamental prerequisite for an advanced digital logic gate to be cascadable is that the input voltage levels and the output voltage levels are identical. But in spite of this necessity not being fulfilled in this logic technique, the circuit is cascadable. For one stage the outputs are degraded from 1 to $V_{dd} - V_{tn}$ .But this voltage level rely totally on the supply voltage. On the assumption that the inverter circuit is given $V_{dd} + V_{tn}$ as logic 1 , then it is noticed that output logic levels are also identical as that of input. So, the circuits can be effectively cascaded.

CHAPTER - 5

5 APPLICATION OF MGFCAL IN VARIOUS CIRCUITS

Adiabatic system is a thermodynamic technique which means that there is no gain or no loss of energy in the circuit. As in this digital world, because of increment in requirement of handy and portable electronic equipment, low power VLSI design plays the major role.

So, implementing the circuits through Modified Glitch Free Cascadable Adiabatic logic serves the purpose of reducing the power dissipation to a greater extent in the circuit. As the adiabatic technique is not relevant for each and every CMOS circuit as every adiabatic logic technique has its own particular advantages and disadvantages. In this way, the fundamental challenge is to find a circuit in which these power dissipation reduction techniques can be enforced, so that the circuit performance is enhanced to a more prominent degree with respect to power dissipation without influencing alternative process parameters to a more noteworthy degree.

In this chapter, the application of various full adder circuits using Modified Glitch Free Cascadable Adiabatic Logic is shown. These power efficient circuits can be used in those VLSI design circuits where addition operation is to be performed and power efficient circuit is required like in ALU, microprocessors, combinational circuits, memory elements, etc.

5.1Basic Inverter Block using MGFCAL:

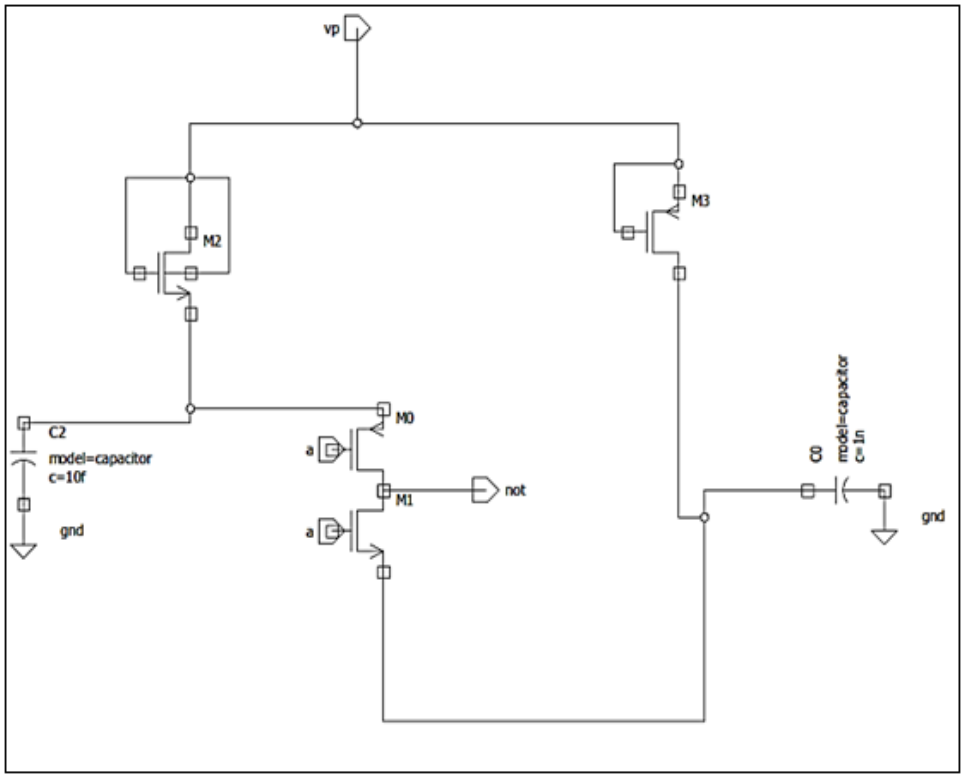


Fig 5.1: Low Power Inverter block using MGFCAL.

The MGFCAL based inverter circuit is controlled by a trapezoidal power supply and the static CMOS inverter is linked between the charging transistor M2 and the discharging transistor M3.

Suppose the output capacitance at node 'NOT' is uncharged and the input at node A is logic '0'. Due to logic '0' at the input, M0 transistor turns on and as the supply exceeds the cut in voltage Vtn of diode M2, transistor M0 turns on and inverter output node 'NOT' charges through M2 and M0. Thus, a low input gives a high output. When the output capacitance at node 'NOT' is in charged state and the input at node A is logic '1'. The high input level will turn on transistor M1 and M3 as soon as the supply exceeds the cut in voltage Vtp of the transistor M3. Thus, the output node capacitance discharges through M1 and M3 and the charge is sent back to the power supply.

When the output capacitance at node 'NOT' is charged and the input is at logic low level '0'. Here M1 transistor will not turn on and thus the discharge path for output node back to the power supply is cut through M1 and hence the output capacitance does not discharge and the high output level is maintained. When the output capacitance node 'NOT' is uncharged and

the input at node A is logic ‘1’, transistor M0 will not turn on and the charging path via M2 is not completed, thus the output node remains at logic low level.

So, in the last two cases it can be observed that dynamic switching does not take place hence power dissipation is reduced.

5.2 Basic AND Gate Block using MGFCAL:

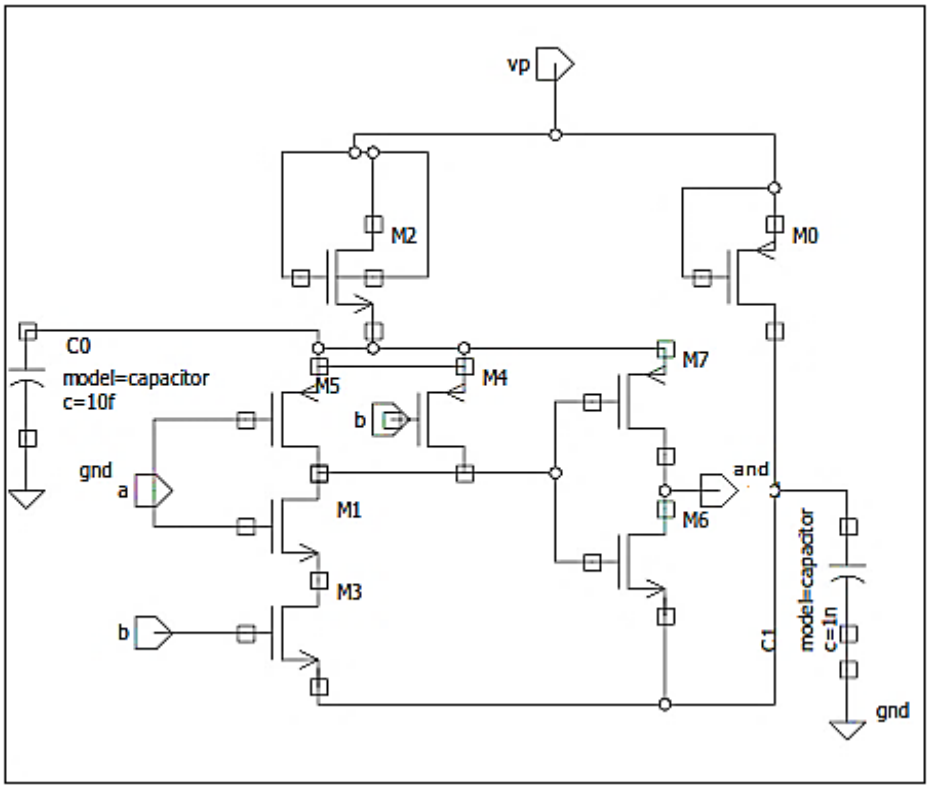


Fig 5.2: Low Power AND gate block using MGFCAL.

The MGFCAL based AND gate circuit is controlled by a trapezoidal power supply and the static CMOS AND gate structure is linked between the charging transistor M2 and the discharging transistor M0. The whole charging discharging operation is same as described for the Inverter block.

When the output transition is made from logic 1 to logic 0, then it results in discharging of the output capacitance and the energy while discharging the capacitance , the charge is not wasted out, on the contrary it is sent back to the power supply. In fig 5.2, a and b are the inputs and the output terminal named ‘ AND’ is the output node from where the output of the AND gate is taken . The output of the Low Power AND gate block is high only if both the input a and b are 1, in all the other cases the value of the output is 0.

5.3 Basic OR Gate Block using MGFCAL:

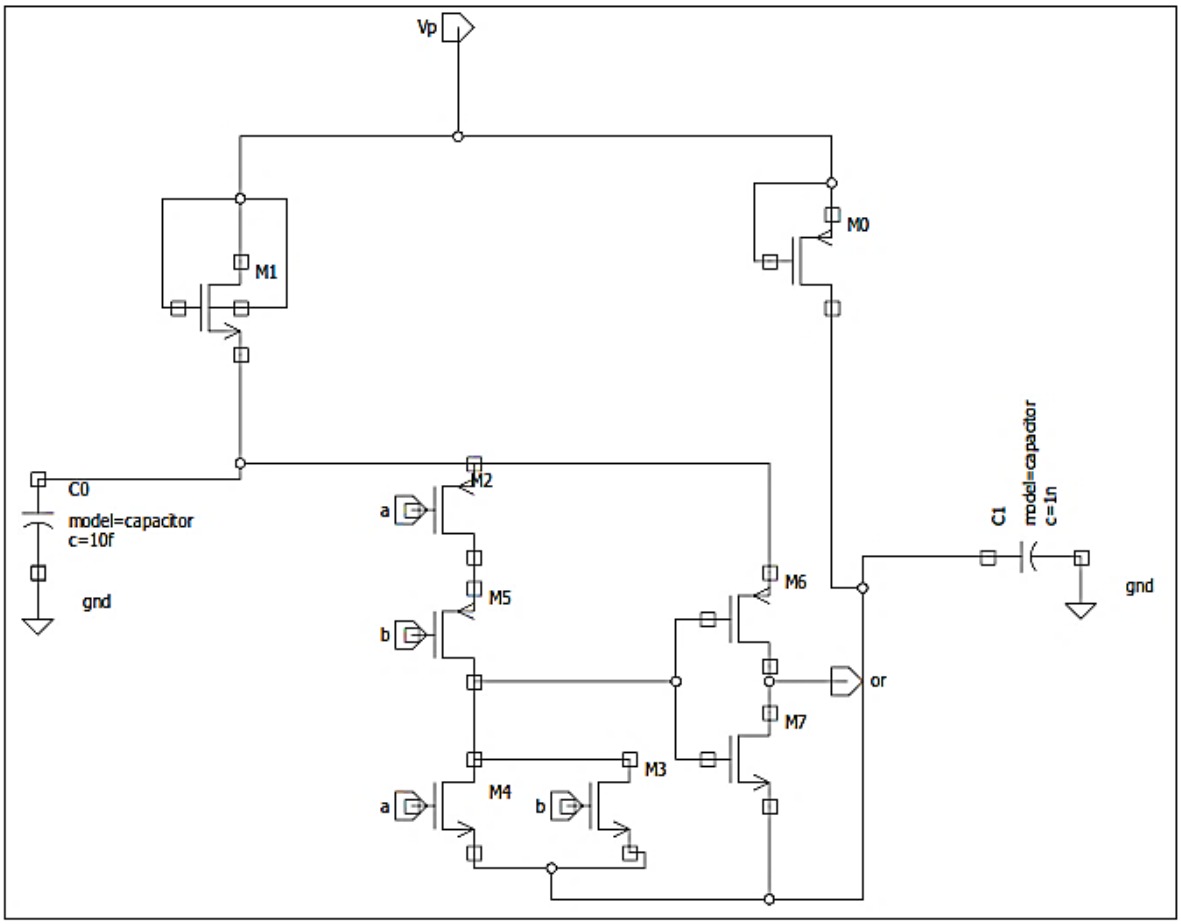


Fig 5.3: Low Power OR gate block using MGFCAL

The MGFCAL based OR gate circuit is also controlled by a trapezoidal power supply and the static CMOS OR gate structure is linked between the charging transistor M1 and the discharging transistor M0. Both transistors M1 and M0 are basically the diodes, one is used for charging and the other for discharging. So, we can say that basically M1 and M0 are basically the transistor based diode.

In fig 5.3, a and b are the inputs and the output terminal named ‘OR’ is the output node from where the output of the OR gate is taken from. The output of the Low Power OR gate block is LOW only if both the input a and b are 0, in all the other cases the value of the output is HIGH or we can say at logic 1.

5.4 Basic NAND Gate Block using MGFCAL:

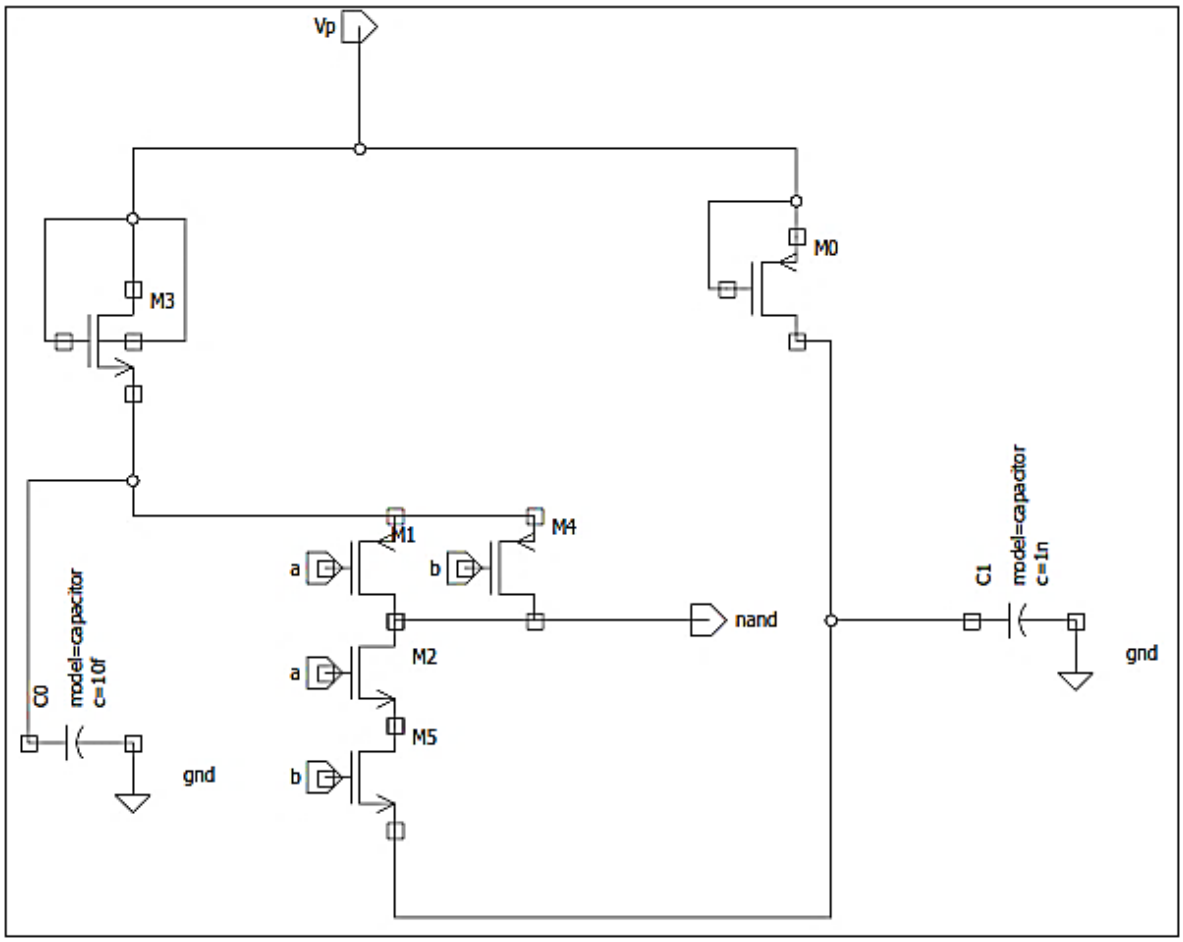


Fig 5.4: Low Power NAND gate block using MGFCAL

The MGFCAL based NAND gate is basically controlled by V_p. V_p is the trapezoidal power supply that is the V_{pulse}. V_{pulse} is quite different from the supply voltage used in the conventional CMOS logic. That is V_{dc}, which is the dc voltage supply. The conventional CMOS NAND gate structure is connected between the transistors M3 and M0 which are the charging and the discharging transistors respectively.

a and b are the input terminal, while NAND is the output terminal from where the output of the circuit is taken from. NAND logic circuit produces the output 0, when both input a and b are 1. In all other cases, the output is always high or at logic '1' in the NAND gate.

5.5 Basic NOR Gate Block using MGFCAL :

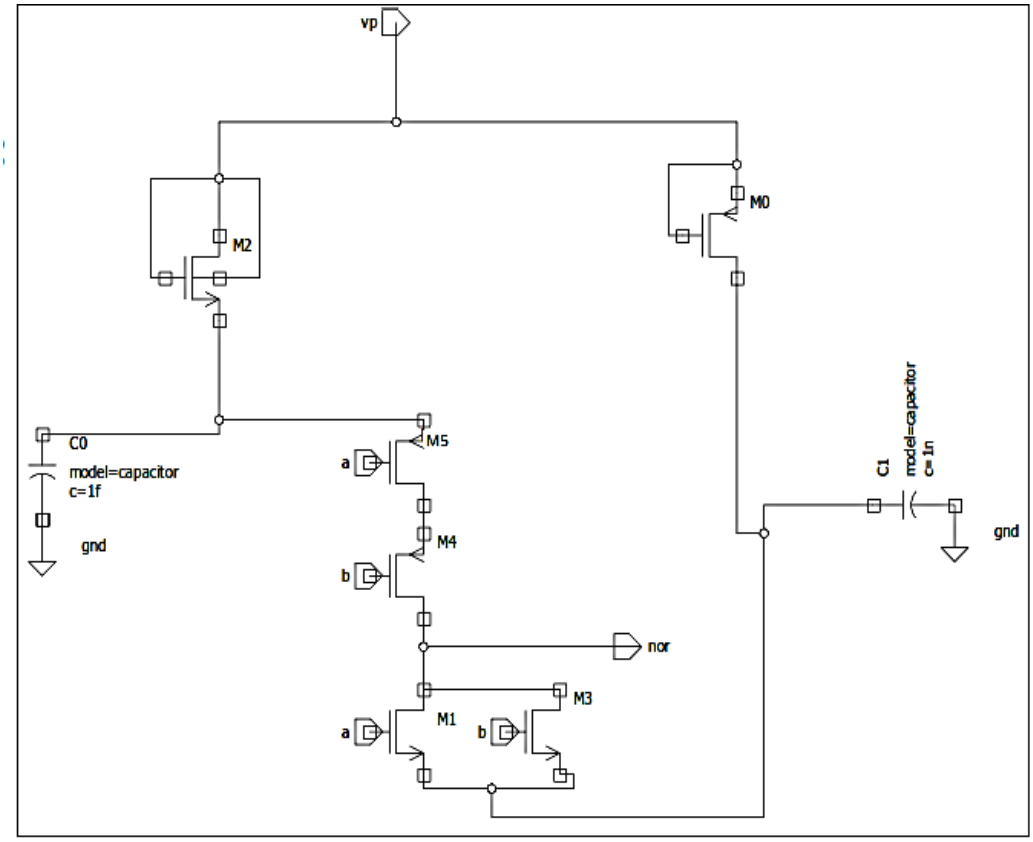


Fig 5.5: Low Power NOR gate block using MGFCAL

The conventional CMOS NOR gate structure is connected between the transistors M2 and M0 which are the charging and the discharging transistors respectively. The advantage of using this Low power NOR gate block is that the power is reduced to a greater extent than the conventional CMOS structure. The output of the conventional NOR gate is (a + b) bar that is the output is set at logic 1, if and only if all the inputs are at logic'0'. Otherwise in all other circumstances, the value of output is low that is at the logic 0 level.

When the output makes transition from logic 1 to logic 0, then in spite of the charge wastage, the charge is fed back to the power supply. In this way, energy is not lost in the circuit.

5.6 Basic XOR Gate Block using MGFCAL:

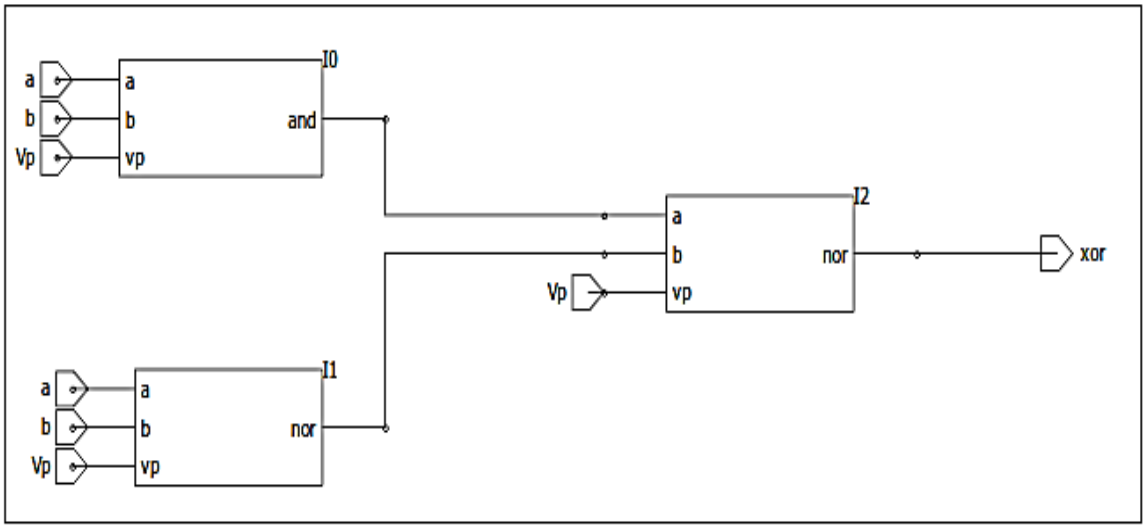


Fig 5.6: Low Power XOR gate block using MGFCAL

The low power XOR gate block using MGFCAL is made through combining three blocks as discussed earlier; two nor gate and one and gate. The output of the XOR gate is same as in the convention XOR implementation through CMOS. The only difference is that by using MGFCAL technique the power is reduced to a greater extent.

As illustrated in fir 5.6, a and b are the inputs of the XOR gate and output node termed as 'XOR' is the output of the block. V_p is the trapezoidal power supply used to control the circuit. The output XOR of the logic block is A XOR B and is given by:

$$XOR = A\overline{B} + \overline{A}B$$

The output of the XOR gate is 1 if and only if both the input a and b are different, on the contrary when both the inputs a and b are same, the output of the XOR gate is 0 or low output.

5.7 Basic Half Adder Block using MGFCAL Logic:

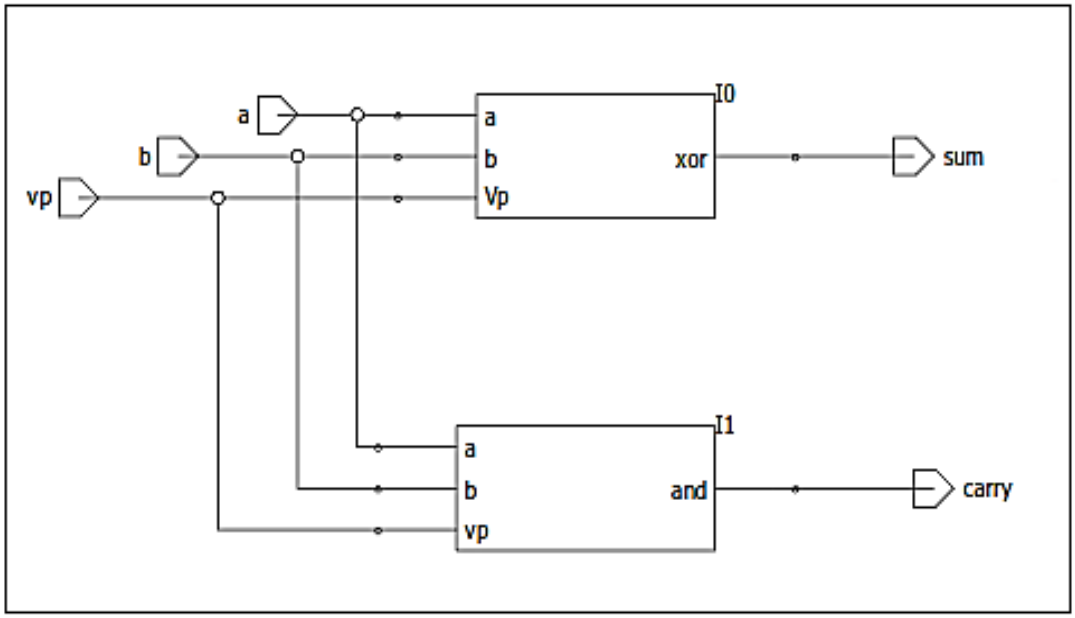


Fig 5.7: Low Power Half Adder block using MGFCAL

The half adder block implementation using MGFCAL requires two different blacks discussed earlier, one is XOR gate and one AND gate. The output of the half adder is sum and the carry output. The basic aim behind using this half adder block arises when addition of two bits is required in the circuit. Previously generated carry has no role in the next sum output thus produced. The output of the half adder are as follows:

Sum = A XOR B

Carry = A.B

Table 5.1: Truth Table of Half Adder

Input		**Output**	
A	**B**	**SUM**	**CARRY**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

5.8 Proposed Adder Circuits Applications using MGFCAL:

Adders are one of the basic logic circuits intended to carry out faster arithmetic operations and are one of the fundamental block in outlining of any digital circuit on account of their broad use in a few essential operations, for example, subtraction, division and multiplication. The convergence of research amid the time is a mission of planning low power and quicker speed adder [100-101].

In numerous PCs and different sort of processors, adders are utilized not only in the ALU, but also in the different modules of the processor to calculate addresses, table records, etc. The fundamental operation of adder is the addition of two binary digits i.e. bits. A combinational circuit that includes two bits is named as half adder, while the module which is utilized to add 3 bits, where the third bit is produced from the past addition is named as Full adder [102- 103].

Addition is one of the essential pertain that is utilized as a part of numerous VLSI design frameworks like DSP design, microchip, microcontroller and data process unit. Along these lines, these days for better execution parameter with the principle advantage of low power utilization, the new VLSI framework in this era demand power effective adders which change the complete performance of the system [104- 107]. Adder structure is grouped in different approaches based upon their execution strategy, for example, serial process or parallel process. Different adder structure implemented through MGFCAL technique are Full adder, half adder based full adder, Ripple Carry Adder (RCA), Look- ahead Carry Adder (LCA), Carry select Adder (CSA) and the hybrid adder. The positive point of using this MGFCAL technique is that the power is reduced to a greater extent in the circuit.

5.8.1 Application Of Full Adder Structure using MGFCAL :

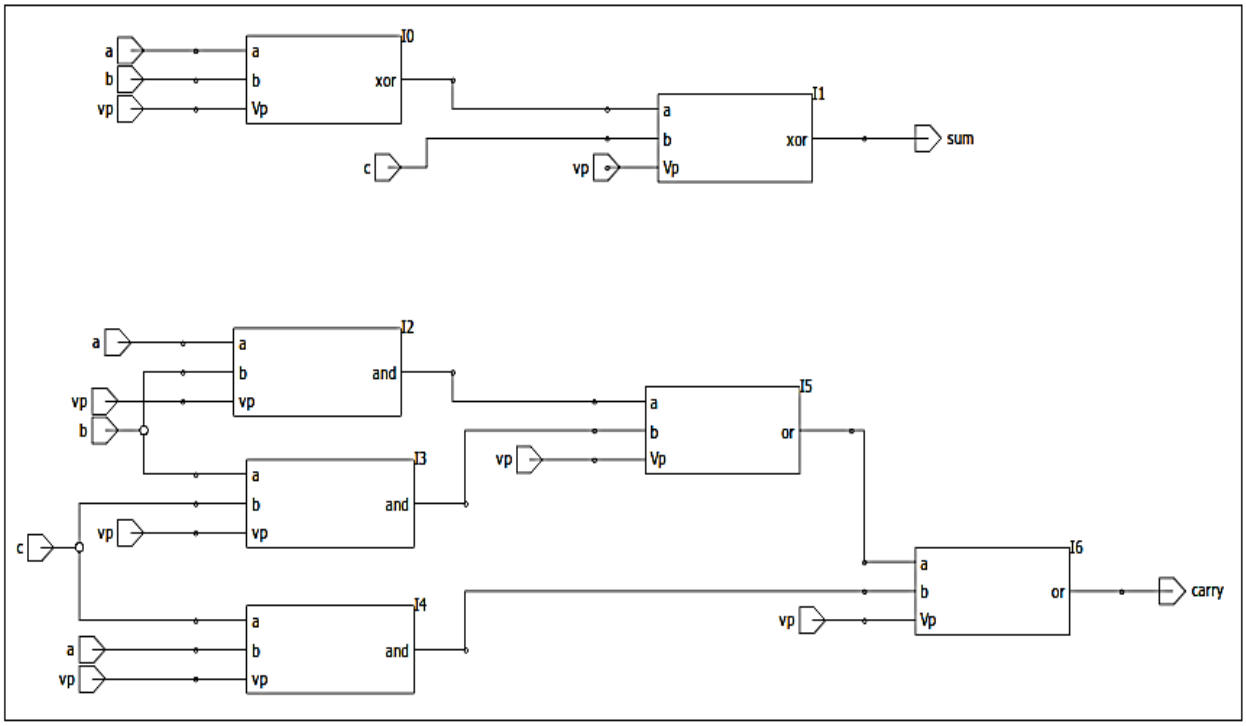


Fig 5.8: Low Power Full Adder block using MGFCAL

Different arithmetic circuits, for example, multipliers demand Full Adder (FA) as the fundamental module for the circuit to work. The advantage of full adder over the half adder is that in the half adder only two bits are added together, while in full adder, two input bits along with the carry from the previous addition is also added with the two inputs, to get the carry output and the sum. The logic expression of sum and the carry out for the full adder is as follows:

$$SUM = A \text{ XOR } B \text{ XOR } C$$

$$C_{out} = AB + C (A \text{ XOR } B)$$

Where, C represents the input carry generated when the previous lower two bits are added together [103].

TABLE 5.2: Truth table of full adder

A	**B**	**C_{in}**	**C_{out}**	**SUM**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

5.8.2 Application of Half Adder Based Full Adder Structure using MGFCAL :

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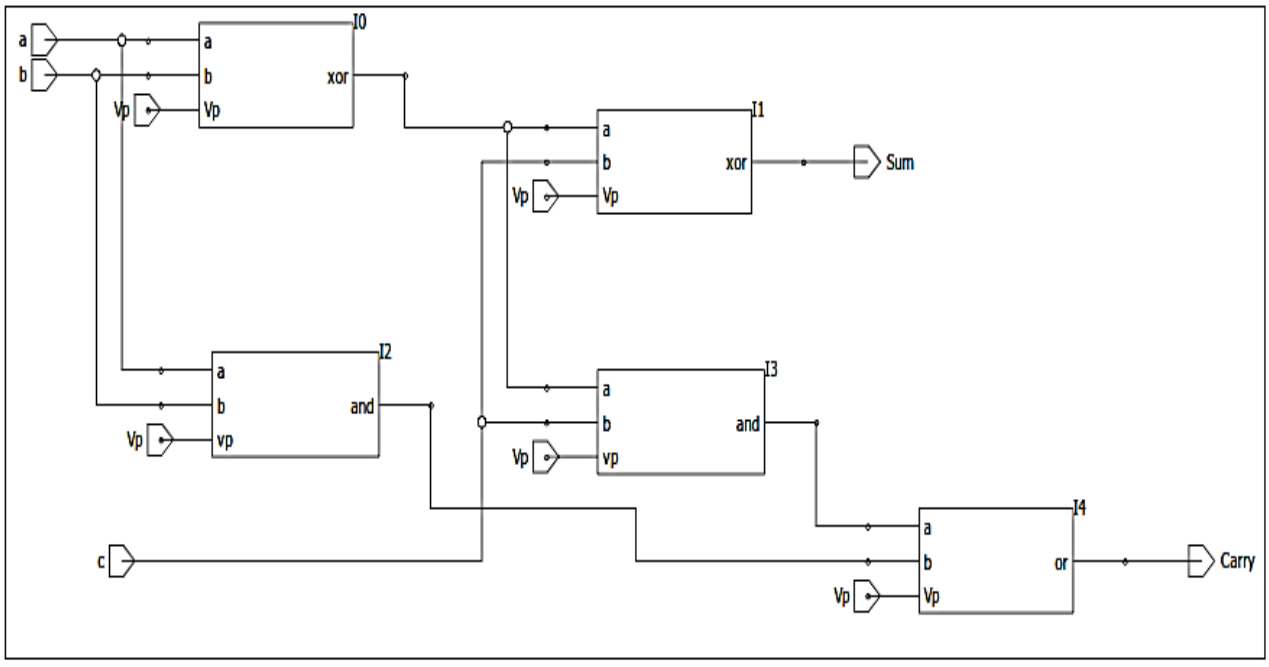

Fig 5.9 : Low Power Half adder based Full Adder block using MGFCAL

The main advantage of using half adder based full adder over the usual full adder circuit described above is that the total number of blocks in the half adder based full adder is reduced from 7 to 5. That is instead of two XOR, three AND gates and two OR gates, only two XOR gate, two AND gate and one OR gate is used in the half adder based full adder.

The advantage of lesser blocks in the circuit is that the overall chip area is reduced to a greater extent along with that it results in lesser power dissipation in the circuit. This is the basic requirement of the circuit in the present era.

Implementing one full adder using half adder, require two half adders blocks along with one OR gate. The expression of output SUM and CARRY remains the same.

5.8.3 Application of Ripple Carry Adder using MGFCAL :

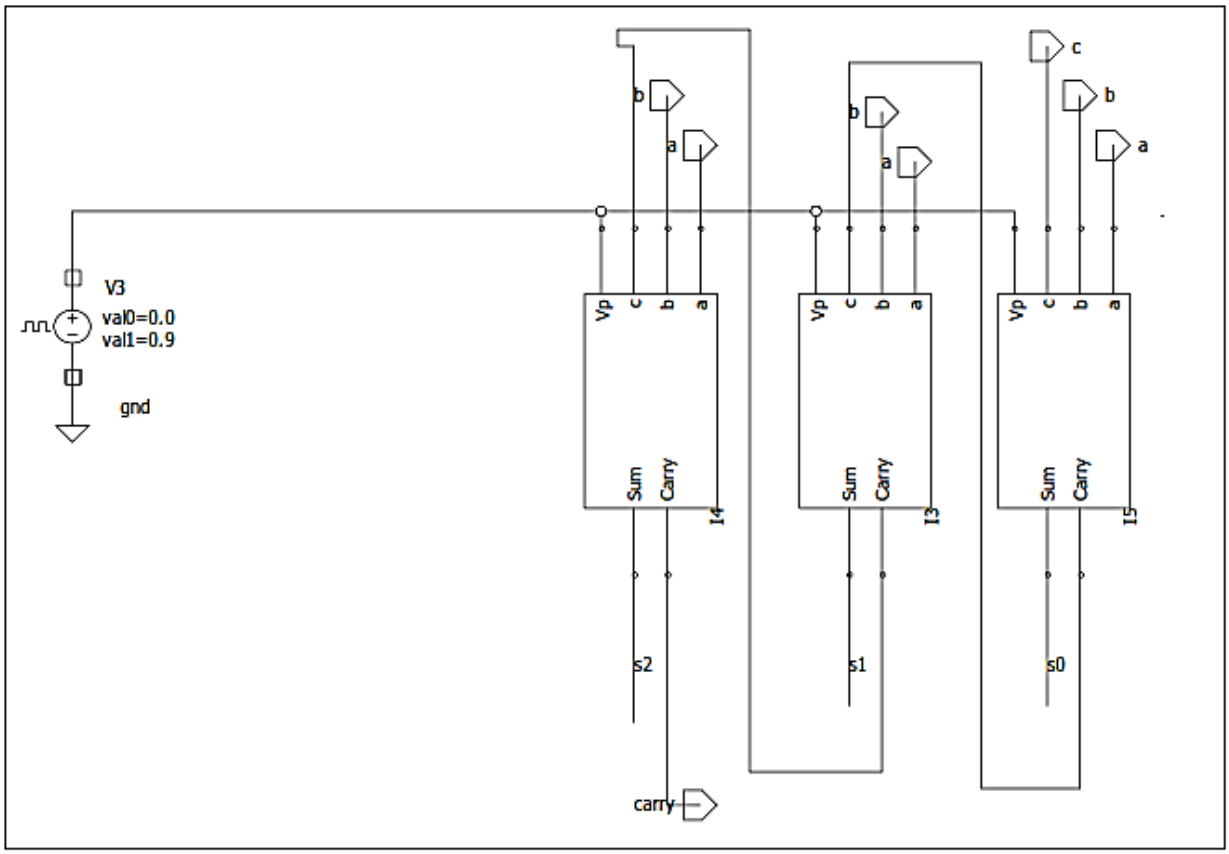

Fig 5.10: Low Power Ripple Carry Adder using MGFCAL

Ripple Carry Adder is essentially an array of full adders associated in series arrangement so that the carry must propagate over every full adder just before the addition is finished. One of the input of each full adder is the carry input (C_{in}), which is the output carry (C_{out}) of the previous adder. This sort of adder is termed as ripple carry adder, since carry bit ripples to the

next full adder. Ripple Carry Adder is constantly favoured regarding power and area. Ripple Carry Adder requires the least amount of hardware compared to all other adders, but it is the slowest because of the ripple of carry in each full adder [109- 110]. So, the final carry thus generated at the output is named as CARRY as depicted in above figure 5.10.

5.8.4 Application Of Look Ahead Carry Adder using MGFCAL:

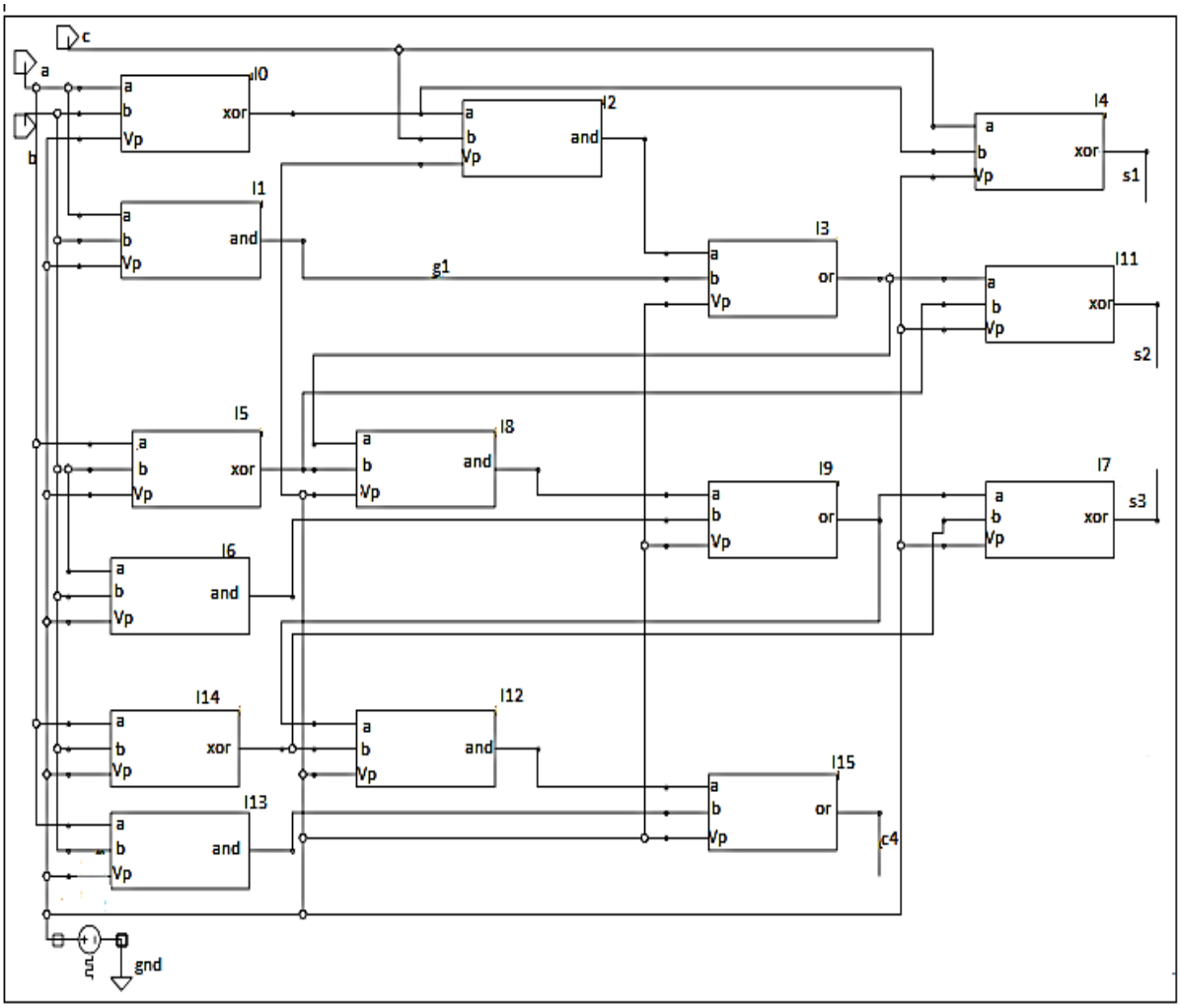

Fig 5.11 : Low Power Look Ahead Carry Adder using MGFCAL

To defeat the disadvantage of Ripple Carry Adder, Look Ahead Carry Adder has been outlined. A quick technique for adding two numbers is called as carry look ahead adder. The computational strategy for this adder is quite fast since it doesn't require the carry signal to propagate stage by stage. Rather it utilizes extra logic to speed up the propagation and

generation of carry information, permitting quick addition at the expense of more hardware necessity [111 - 112].

As illustrated in fig. 5.11, a, b, c are the inputs and the c_4 is the final carry generated after the addition. And the output of the three XOR gates named I4, I7 AND I11 give the sum output s_1, s_2 and s_3. All the basic gates in fig. 5.11 are implemented through the GFCAL technique, which results in the power reduction in the circuit to a greater extent.

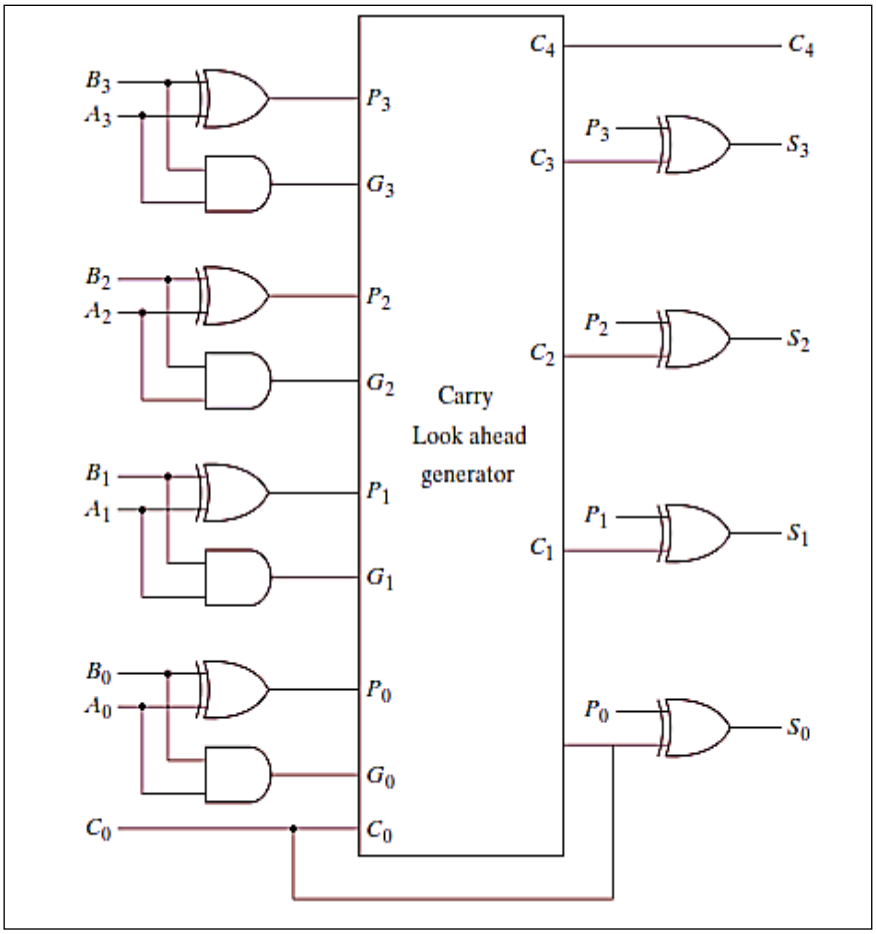

Fig 5.12: Basic Logic diagram of 4- bit Look Ahead Carry Adder [113].

Fig 5.12, depict the basic logic diagram of 4- bit look Ahead Carry Adder, here C_4 is the final carry thus generated and S_0, S_1, S_2, S_3 are the output SUM bits.

Where,

$$S_i = P_i \text{ XOR } C_i$$

$$\text{And output Carry } C_{i+1} = G_i + P_iC_i$$

So,

$$C_2 = G_1 + P_1C_1$$

$$C_3 = G_2 + P_2C_2$$

$$C_3 = G_2 + P_2 (G_1 + P_1C_1)$$

$$C_3 = G_2 + P_2G_1 + P_1P_2C_1$$

Similarly, $C_4 = G_3 + P_3C_3$

Therefore, $C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1C_1$

5.8.5 Application of Carry Select Adder using MGFCAL :

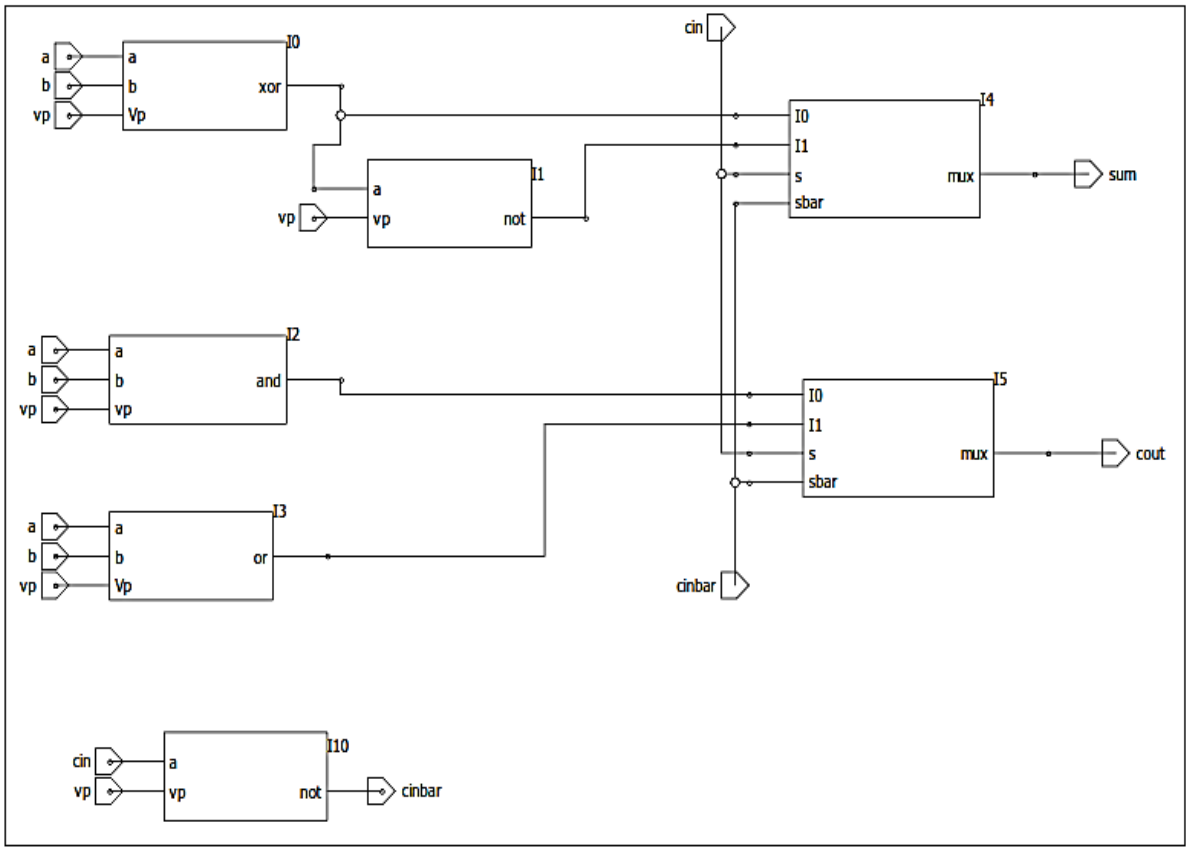

Fig 5.13 : Low Power Carry Select Adder using MGFCAL

There are various ways of implementing the carry select adder like the conventional RCA based Carry Select Adder [114], D- latch based carry select adder [115] but to obtain the lower power dissipation, MUX based carry select adders are used [116].

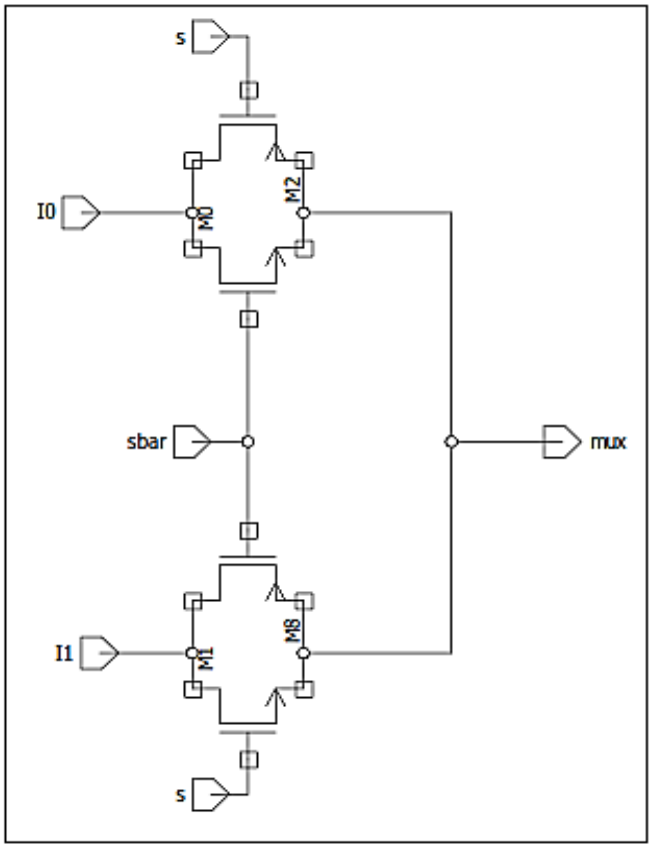

Fig 5.14: Logic Diagram of MUX used in Low Power Carry Select Adder using MGFCAL

The advantage of using proposed circuit in which MUX based CSA using MGFCAL technique is that the power is further reduced to a greater extent in the circuit. As depicted in fig 5.13, when $C_{in} = 0$, then the sum is obtained through the XOR gate of inputs (A and B) and the carry is obtained by the AND pertain between A and B. On the contrary, when value of $C_{in} = 1$, then the sum is obtained by the XNOR operation between the inputs(A and B) and the carry is obtained by the OR operation between the input A and B.

TABLE 5.3: Low Power Carry Select Adder Truth Table

Cin	A	B	SUM	SUM OPERATION	CARRY OUTPUT	CARRY OPERATION
0	0	0	0	XOR	0	AND
0	0	1	1		0	
0	1	0	1		0	
0	1	1	0		1	
1	0	0	1	XNOR	0	OR
1	0	1	0		1	
1	1	0	0		1	
1	1	1	1		1	

5.8.6 Application of Hybrid Adder using MGFCAL:

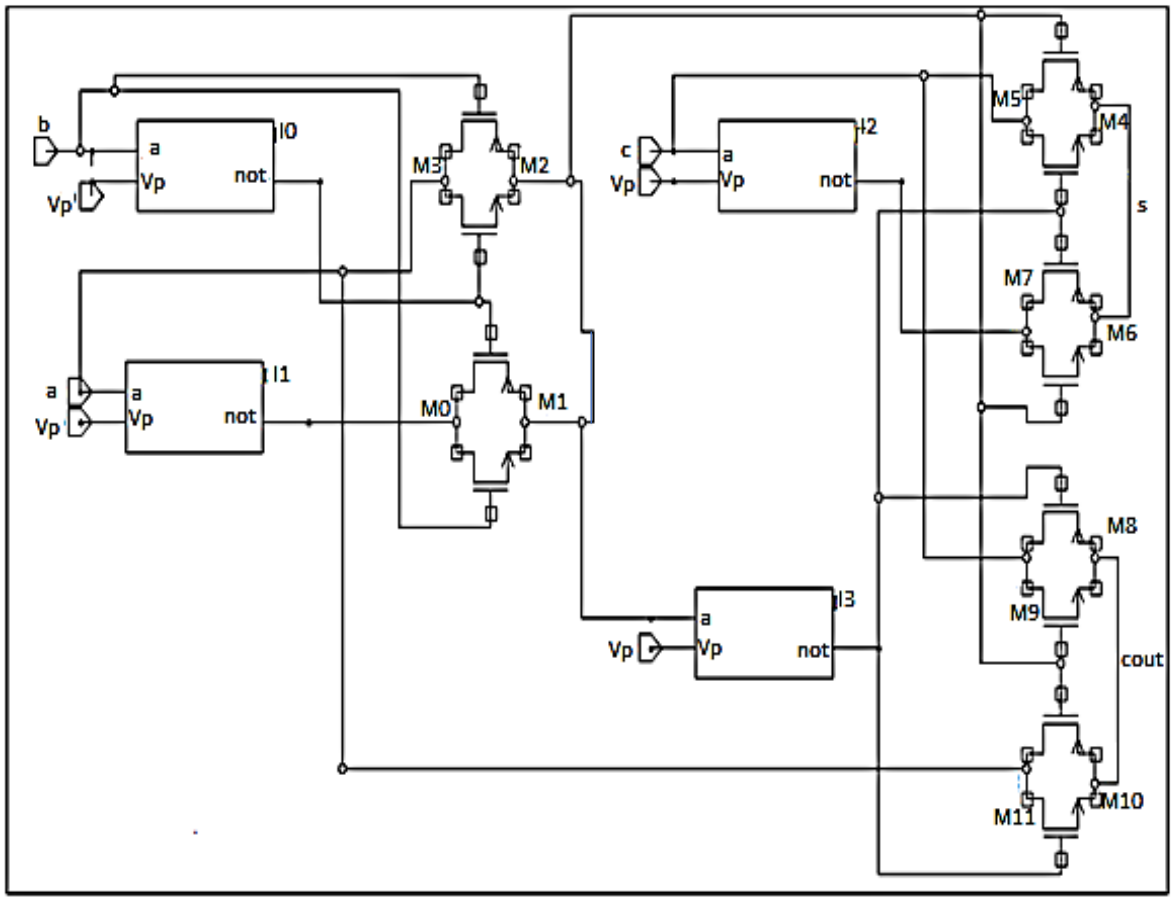

Fig 5.15 : Low Power Hybrid Adder using MGFCAL

The hybrid adder is employed with the help of inverters and the transmission gates. As the transmission gate is another very popular designing style for the CMOS circuit. The only difference between the transmission gates and the pass transistors is that in transmission gate logic both n- type and p- type MOSFET are used on the contrary in the pass transistor approach, either p- type or n- type transistors are used [117].

And the implementation of hybrid adder using MGFCAL technique is that it proves to be at the advantageous side as it has advantages of both the MGFCAL technique as well as the transmission gates. The four inverters used in the circuit are implemented through the MGFCAL technique as depicted in fig 5.1 and it is for this reason the power dissipation is reduced to a greater extent when the implementation is done with the help of MGFCAL technique. Thus, the proposed hybrid adder is at the positive side as far as the power dissipation of the circuit is concerned.

CHAPTER - 6

6 SIMULATION AND ANALYSIS

Different circuits of adders as depicted in chapter 5 are simulated with the help of Symica DE Software and LT spice tool at 90nm PTM model using three different power supply viz 0.9V, 1.2V, 1.5V at different temperature of 25˚C, 55˚C and 125˚C. Different performance parameters like delay, total power dissipation, along with the total energy is calculated in the proposed adder circuits. The analysis of basic gates, along with half adder, is also simulated for the better understanding of the MGFCAL technique.

6.1 Low Power NOT Gate Block using MGFCAL :

Schematic of NOT gate block is depicted in fig 6.1 and the output waveform of the NOT gate block is illustrated in fig 6.2 along with all the performance parameters of the low power NOT gate which are shown in table 6.1. And performance parameters of NOT gate using conventional CMOS logic is shown in table 6.2.

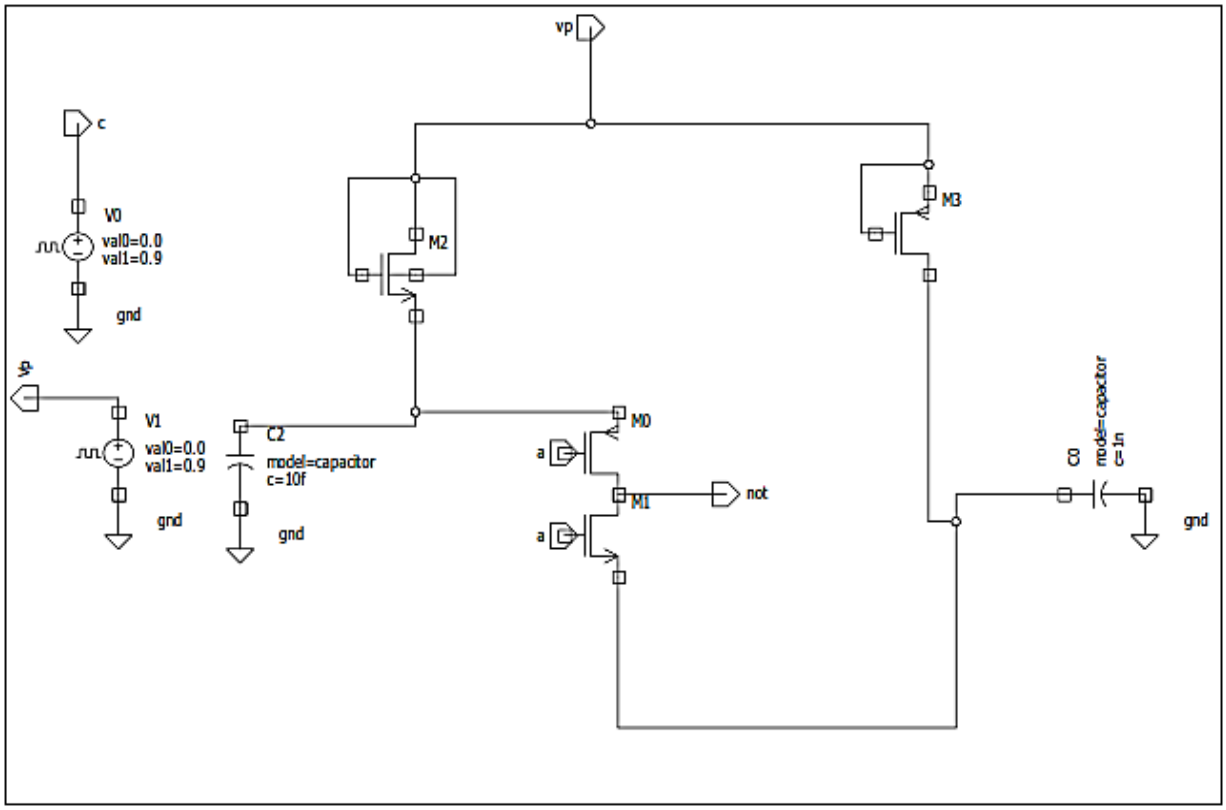

Fig 6.1: Schematic of Low Power NOT gate block

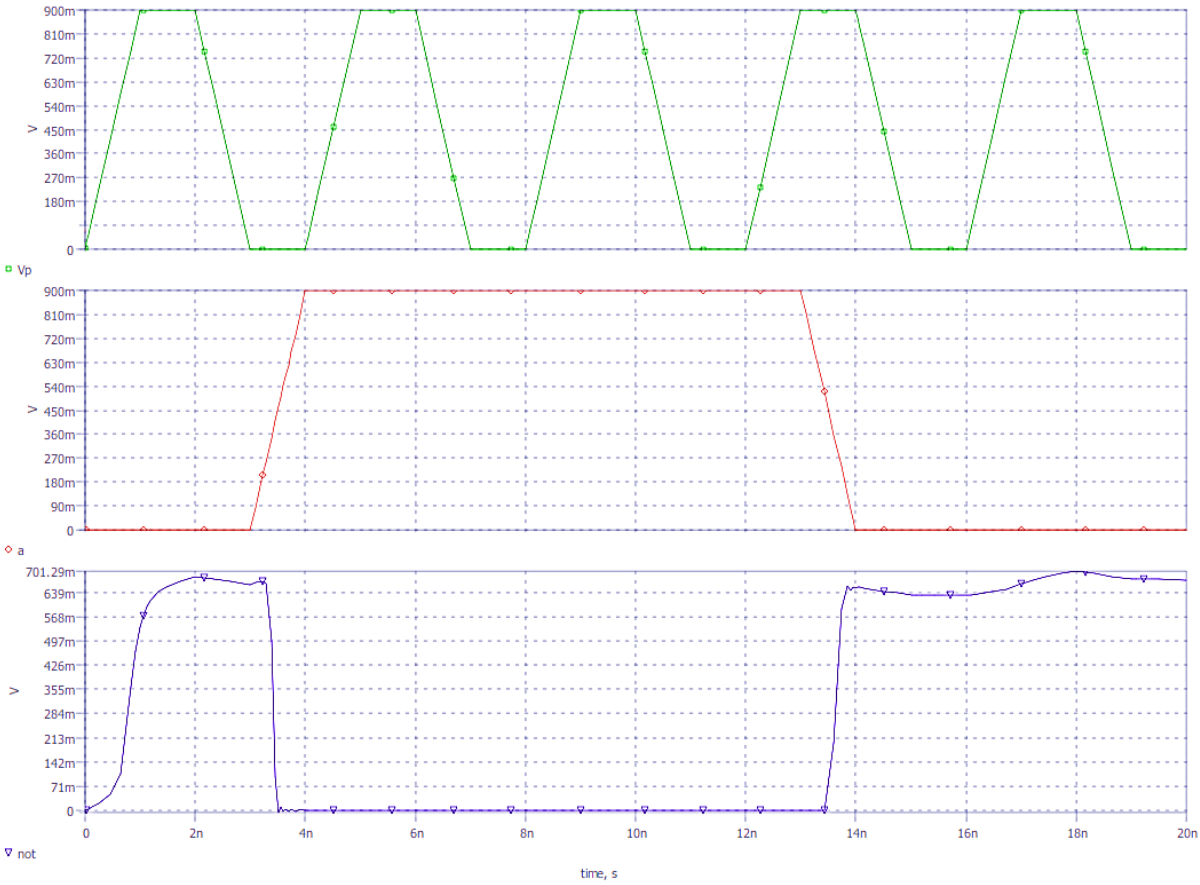

Fig 6.2: Output waveform of Low Power NOT gate block

Table 6.1 (a): Delay calculation of NOT gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Voltage Supply(V)	Temperature (˚C)
1	90nm	156.66	0.9	27
2		166.05		55
3		173.32		120
4		104.83	1.2	27
5		165.99		55
6		170.09		120
7		100.40	1.5	27
8		154.74		55
9		162.27		120

Table 6.1 (b): Performance parameter of NOT gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply(V)	Temperature (˚C)
1	90nm	156.66	102.95	1.87	0.9	27
2		104.83	150.47	3.95	1.2	
3		100.40	198.34	4.82	1.5	

Table 6.2 (a): Delay calculation of NOT gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	12.36	0.9	27
2		17.29		55
3		20.52		120
4		10.124	1.2	27
5		11.86		55
6		15.86		120
7		9.26	1.5	27
8		10.42		55
9		13.65		120

Table 6.2 (b): Performance parameter of NOT gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply(V)	Temperature (˚C)
1	90nm	12.36	350.28	6.24	0.9	27
2		10.12	412.47	7.05	1.2	
3		9.26	462.81	7.93	1.5	

6.2 Low Power AND Gate Block using MGFCAL :

Schematic of low power AND gate block is depicted in fig 6.3 and the output waveform of the AND gate block is illustrated in fig 6.4 along with all the performance parameters of the low power AND gate which are shown in table 6.3. And performance parameters of AND gate using conventional CMOS logic is shown in table 6.4.

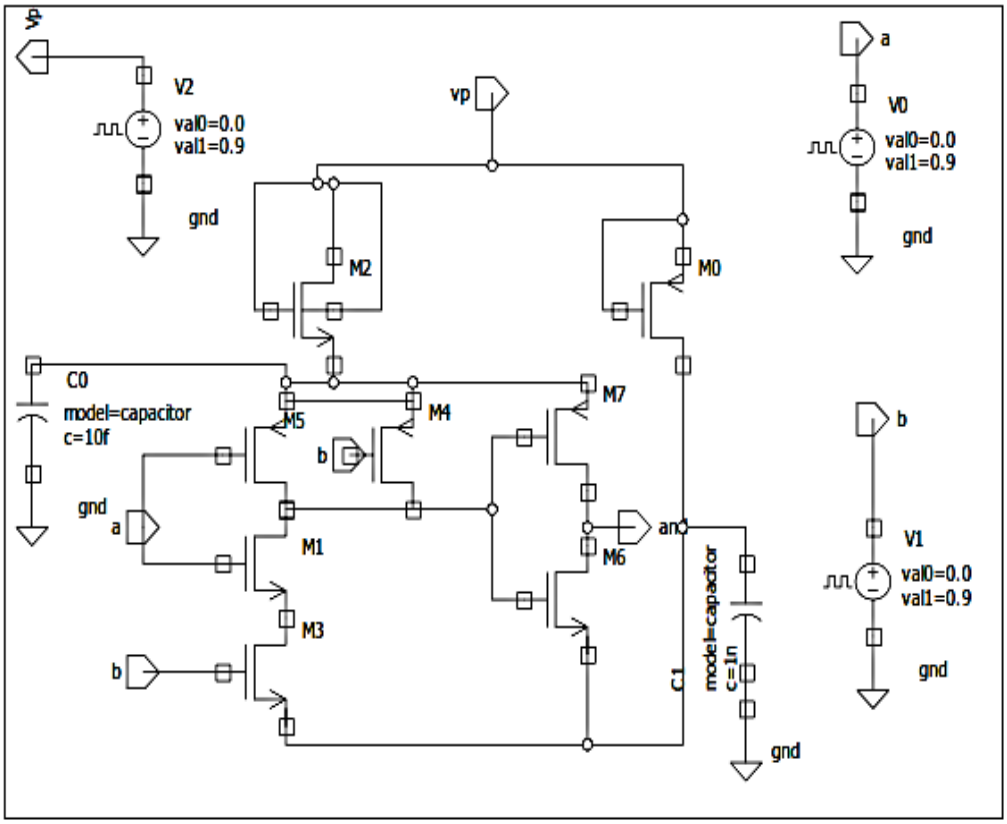

Fig 6.3: Low Power AND gate block using MGFCAL.

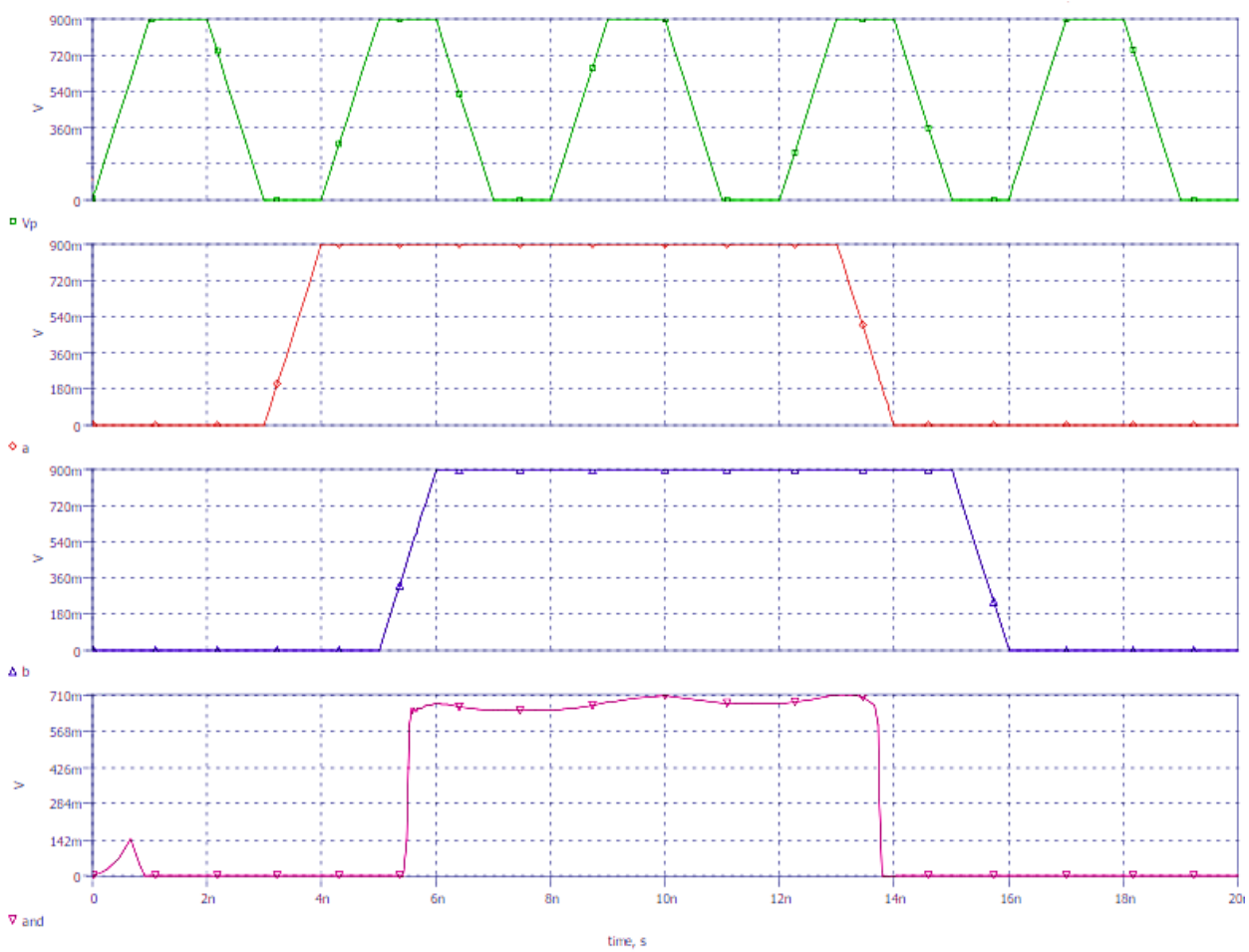

Fig 6.4: Output waveform of Low Power AND gate block.

Table 6.3 (a): Delay calculation of AND gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature(˚C)
1	90nm	243.86	0.9	27
2		247.61		55
3		251.10		120
4		191.67	1.2	27
5		198.74		55
6		206.21		120
7		178.95	1.5	27
8		183.27		55
9		187.37		120

Table 6.3 (b): Performance parameter of AND gate block using MGFCAL.

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply	Temperature (˚C)
1	90nm	243.86	285.73	5.14	0.9	27
2		191.67	305.48	6.97	1.2	
3		178.95	386.95	8.16	1.5	

Table 6.4 (a): Delay calculation of AND gate block using conventional CMOS logic.

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	35.30	0.9	27
2		37.89		55
3		40.73		120
4		26.09	1.2	27
5		27.63		55
6		30.279		120
7		24.09	1.5	27
8		29.17		55
9		29.52		120

Table 6.4 (b) : Performance parameter of AND gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply	Temperature (˚C)
1	90nm	35.30	622.46	12.44	0.9	27
2		26.09	691.53	14.76	1.2	
3		24.09	715.82	17.83	1.5	

6.3 Low Power OR Gate Block using MGFCAL:

Schematic of low power OR gate block is depicted in fig 6.5 and the output waveform of the OR gate block is illustrated in fig 6.6 along with all the performance parameters of the low power OR gate which are shown in table 6.5. And performance parameters of OR gate using conventional CMOS logic is shown in table 6.6.

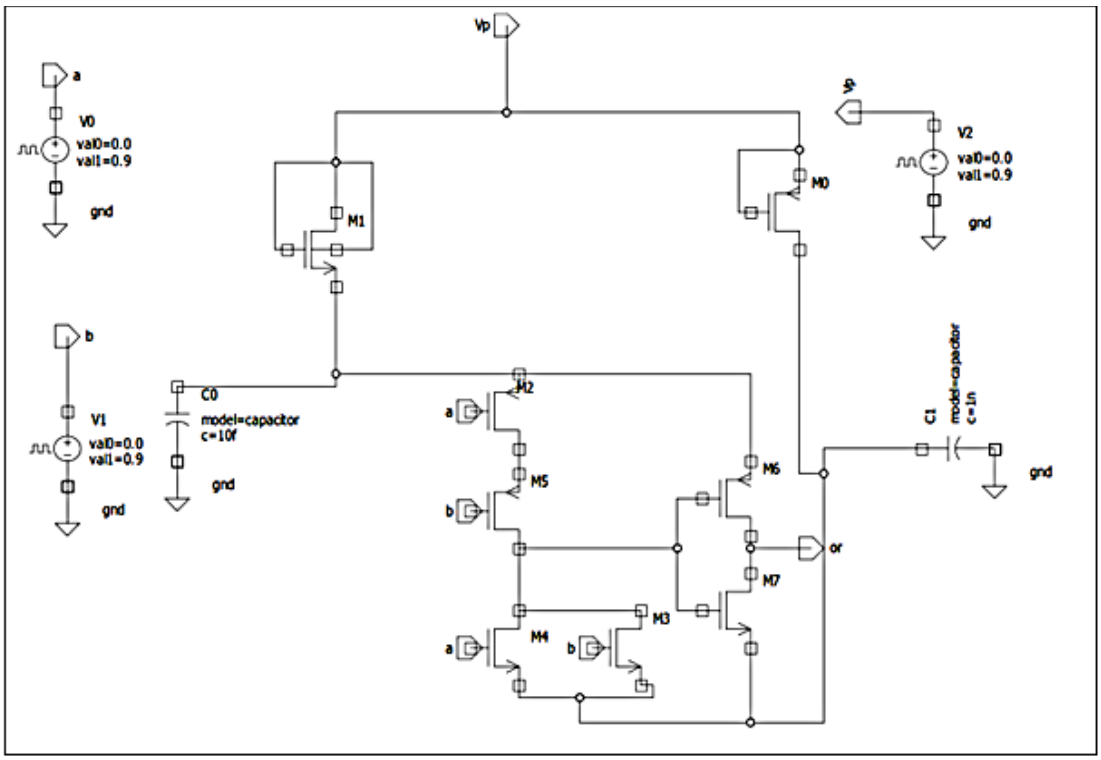

Fig 6.5: Low Power OR gate block using MGFCAL.

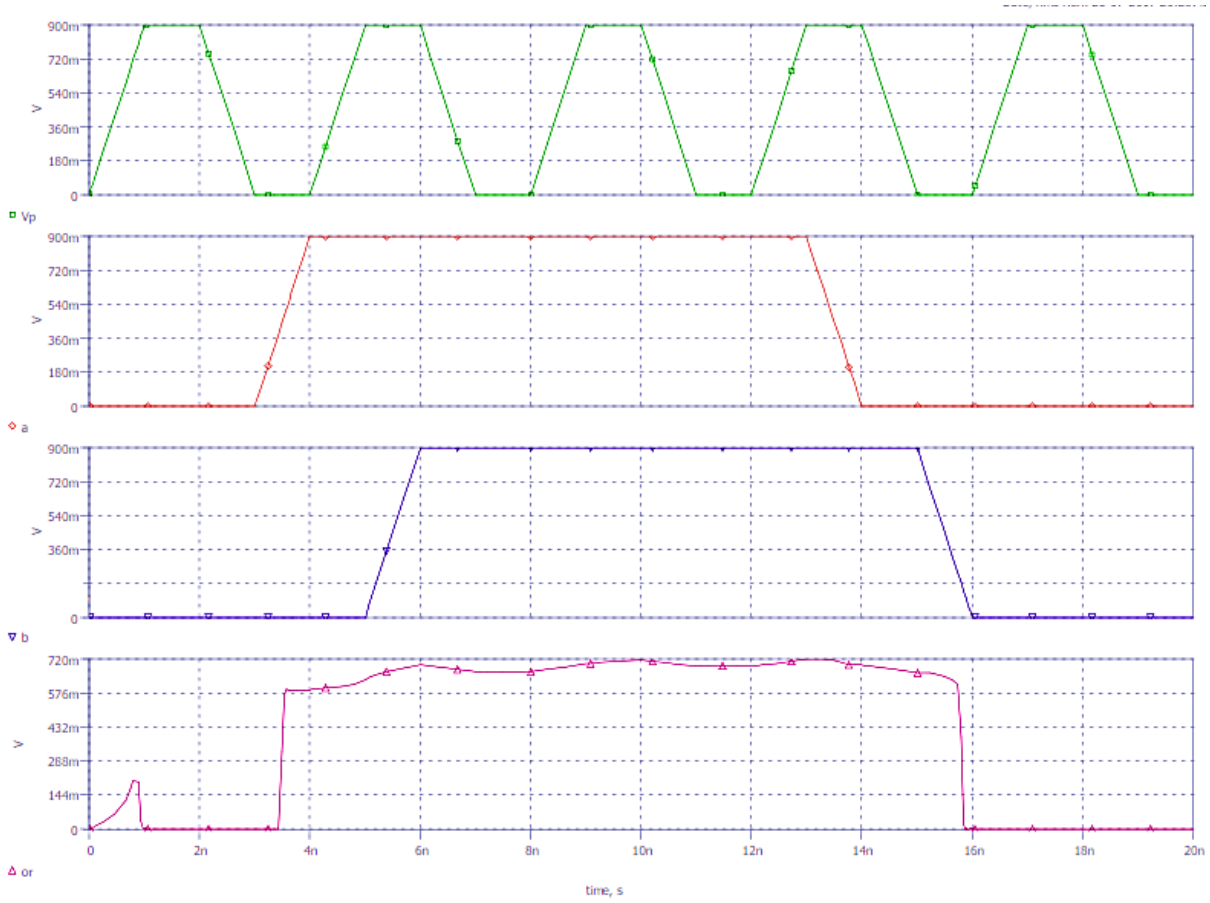

Fig 6.6: Output waveform of Low Power OR gate block.

Table 6.5 (a): Delay calculation of OR gate block using MGFCAL

S.No.	Technology Node	Delay(ps)	Voltage Supply (V)	Temperature(˚C)
1	90nm	223.84	0.9	27
2		229.40		55
3		247.23		120
4		215.02	1.2	27
5		223.71		55
6		245.30		120
7		178.95	1.5	27
8		183.27		55
9		187.37		120

Table 6.5 (b): Performance parameter of OR gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	223.84	351.62	5.67	0.9	27
2		215.02	320.26	7.58	1.2	
3		178.95	295.67	9.26	1.5	

Table 6.6 (a): Delay calculation of OR gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	88.76	0.9	27
2		100.45		55
3		101.40		120
4		86.71	1.2	27
5		99.32		55
6		100.97		120
7		83.84	1.5	27
8		96.61		55
9		98.11		120

Table 6.6 (b) : Performance parameter of OR gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply(V)	Temperature (˚C)
1	90nm	88.76	593.65	11.87	0.9	27
2		86.17	619.52	15.78	1.2	
3		83.84	678.67	19.27	1.5	

6.4 Low Power NOR Gate Block using MGFCAL:

Schematic of low power NOR gate block is depicted in fig 6.7 and the output waveform of the NOR gate block is illustrated in fig 6.8 along with all the performance parameters of the low power NOR gate which are shown in table 6.7. And performance parameters of NOR gate using conventional CMOS logic is shown in table 6.8.

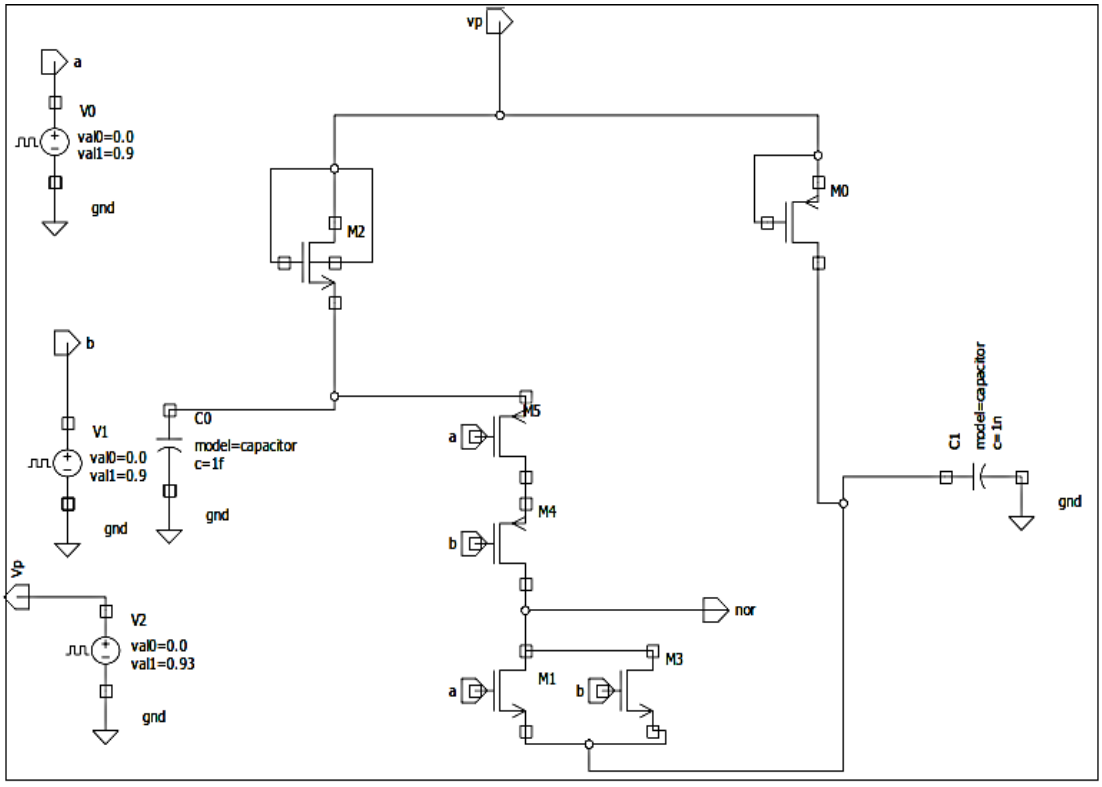

Fig 6.7: Low Power NOR gate block using MGFCAL.

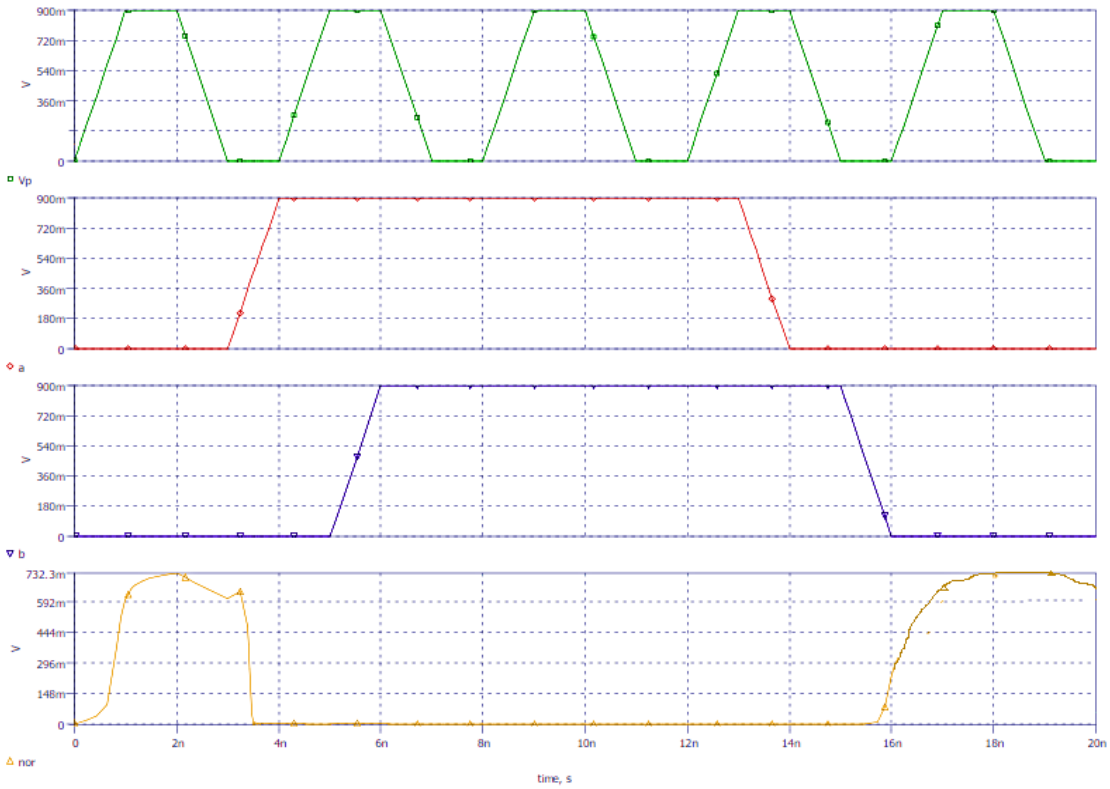

Fig 6.8: Output waveform of Low Power NOR gate block.

Table 6.7 (a): Delay calculation of NOR gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	201.38	0.9	27
2		205.98		55
3		210.36		120
4		186.75	1.2	27
5		191.33		55
6		205.68		120
7		180.38	1.5	27
8		185.58		55
9		202.59		120

Table 6.7 (b): Performance parameters of NOR gate block using MGFCAL.

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply	Temperature (˚C)
1	90nm	201.38	247.59	4.36	0.9	27
2		186.75	296.83	5.89	1.2	
3		180.38	316.27	8.57	1.5	

Table 6.8 (a): Delay calculation of NOR gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	51.25	0.9	27
2		61.52		55
3		69.21		120
4		49.32	1.2	27
5		60.35		55
6		62.29		120
7		47.57	1.5	27
8		65.15		55
9		96.72		120

Table 6.8 (b) : Performance parameters of NOR gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	51.25	453.07	9.061	0.9	27
2		49.32	537.15	13.06	1.2	
3		47.57	589.62	16.28	1.5	

6.5 Low Power NAND Gate Block using MGFCAL:

Schematic of low power NAND gate block is depicted in fig 6.9 and the output waveform of the NAND gate block is illustrated in fig 6.10 along with all the performance parameters of the low power NAND gate which are shown in table 6.9. And performance parameter of NAND gate using conventional CMOS logic is shown in table 6.10.

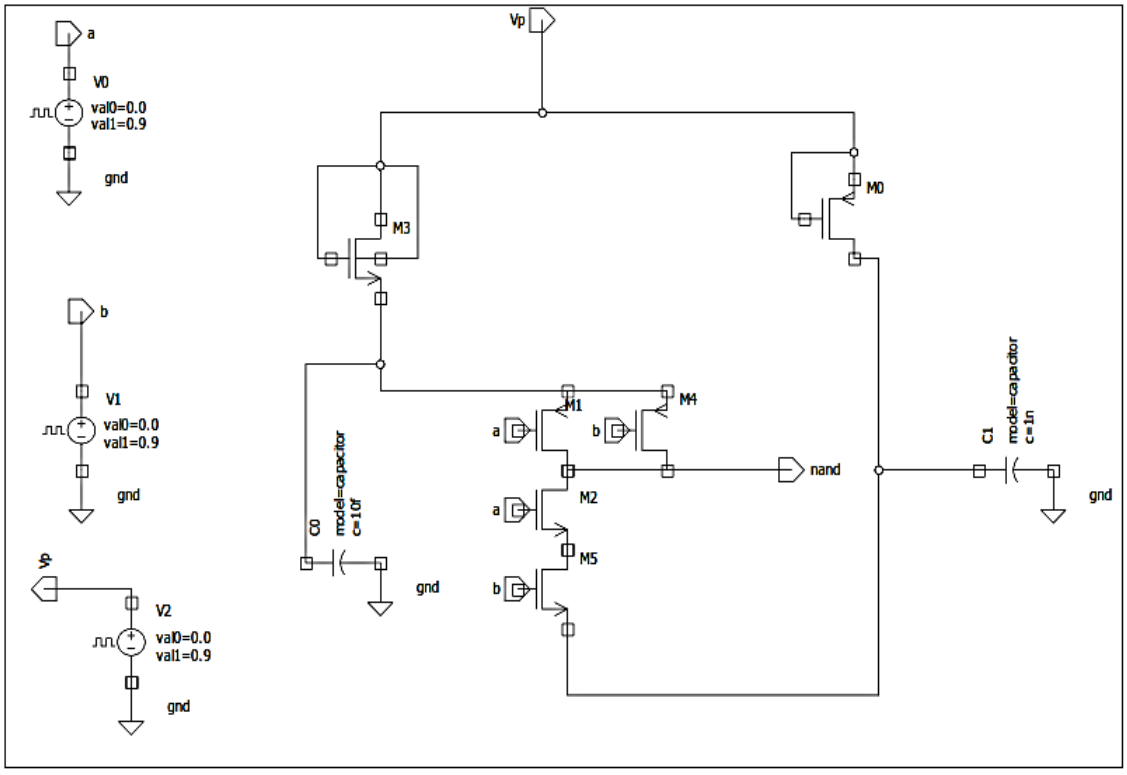

Fig 6.9: Low Power NAND gate block using MGFCAL.

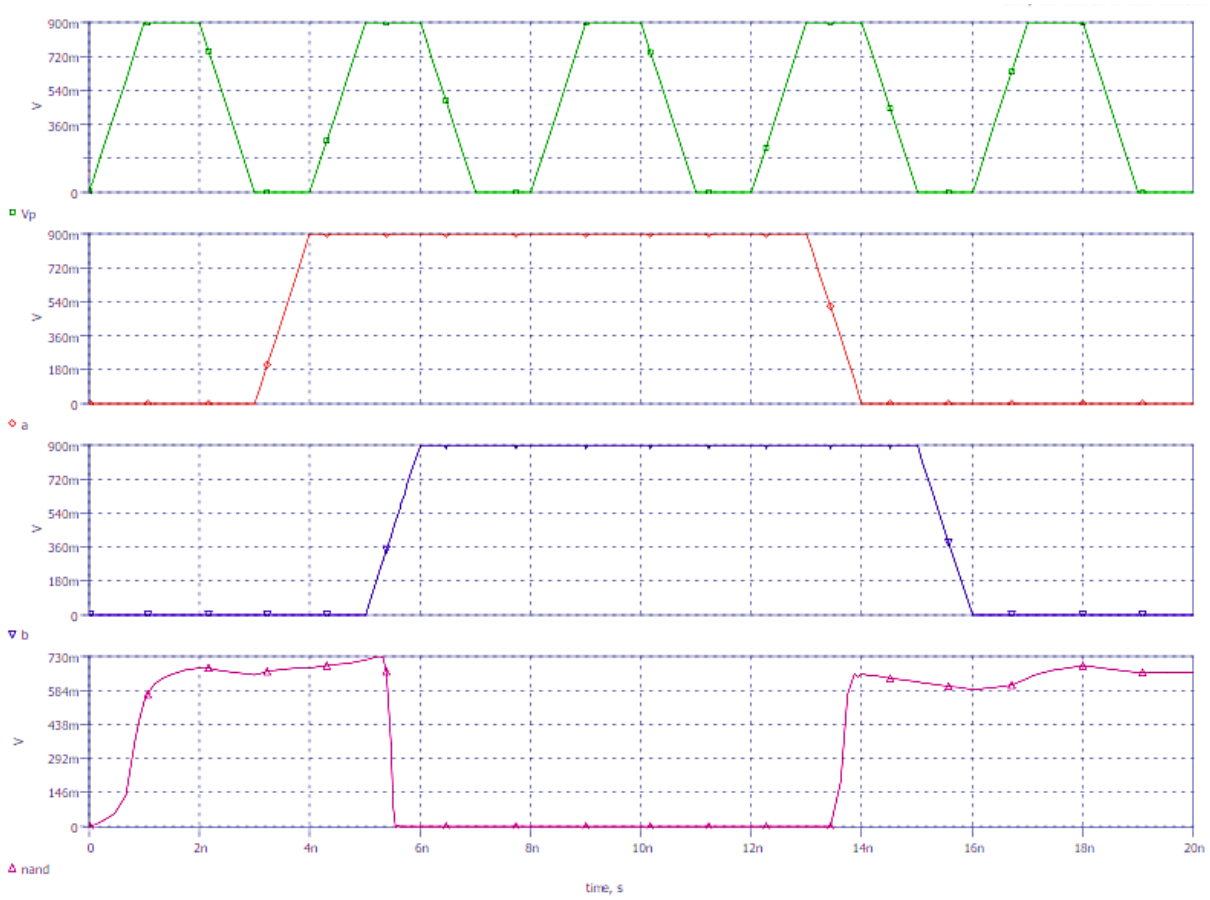

Fig 6.10: Output waveform of Low Power NAND gate block.

Table 6.9 (a): Delay calculation of NAND gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	171.05	0.9	27
2		175.95		55
3		179.98		120
4		170.41	1.2	27
5		172.36		55
6		175.52		120
7		161.89	1.5	27
8		168.76		55
9		180.58		120

Table 6.9 (b): Performance parameter of NAND gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	171.05	261.92	4.67	0.9	27
2		170.41	310.65	6.03	1.2	
3		161.89	363.87	9.65	1.5	

Table 6.10 (a): Delay calculation of NAND gate block using conventional CMOS logic

S.No.	Technology Node	Delay	Voltage Supply	Temperature
1	90nm	40.54	0.9	27
2		59.84		55
3		69.92		120
4		38.48	1.2	27
5		49.68		55
6		59.54		120
7		34.92	1.5	27
8		45.84		55
9		58.54		120

Table 6.10 (b): Performance parameter of NAND gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (nW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	40.54	481.82	9.63	0.9	27
2		38.48	547.12	13.16	1.2	
3		34.92	601.23	16.92	1.5	

6.6 Low Power XOR Gate Block using MGFCAL:

Schematic of low power XOR gate block is depicted in fig 6.11 and the output waveform of the XOR gate block is illustrated in fig 6.12 along with all the performance parameters of the low power XOR gate which are shown in table 6.11. And performance parameter of XOR gate using conventional CMOS logic is shown in table 6.12.

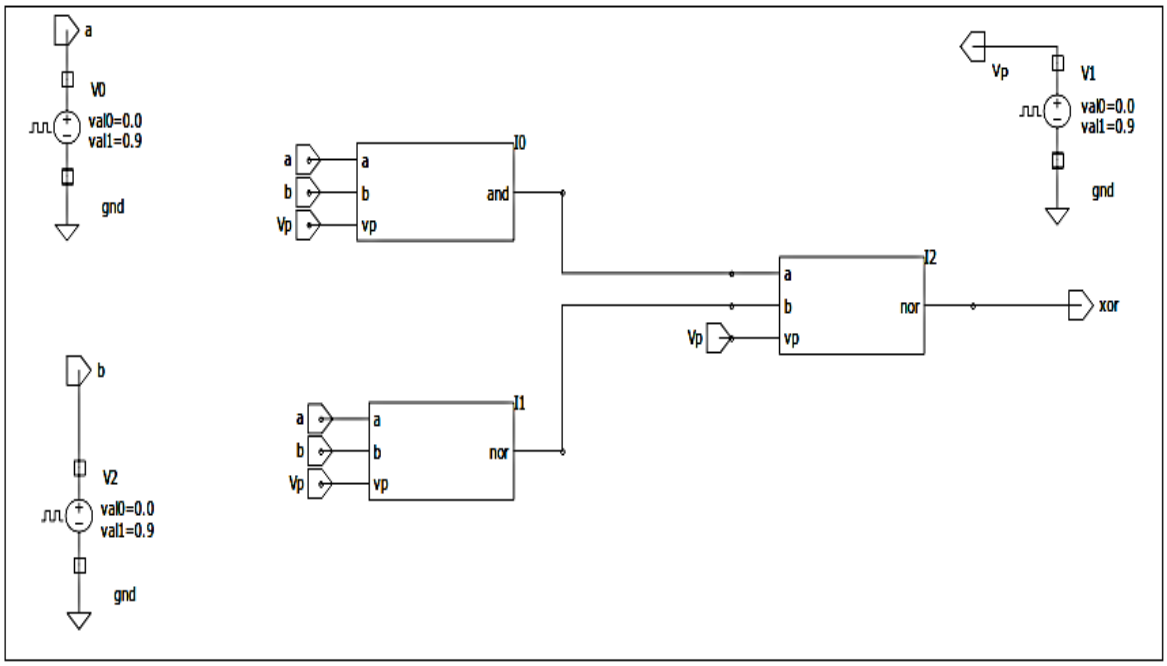

Fig 6.11: Low Power XOR gate block using MGFCAL.

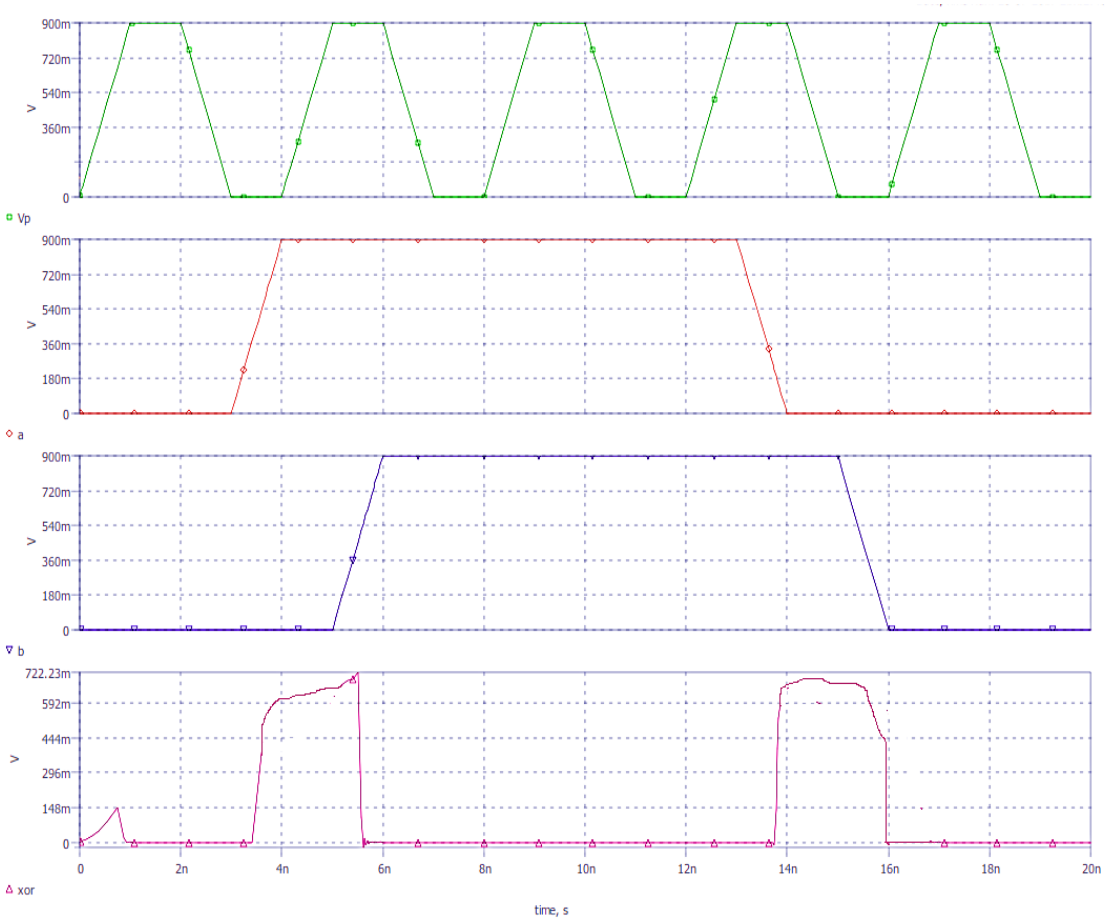

Fig 6.12: Output waveform of Low Power XOR gate block

Table 6.11 (a): Delay calculation of XOR gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	319.48	0.9	27
2		323.18		55
3		326.71		120
4		234.96	1.2	27
5		252.54		55
6		272.96		120
7		230.61	1.5	27
8		245.35		55
9		266.70		120

Table 6.11 (b): Performance parameter of XOR gate block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	319.48	0.247	10.275	0.9	27
2		234.96	0.651	18.636	1.2	
3		230.61	0.814	25.175	1.5	

Table 6.12 (a): Delay calculation of XOR gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Voltage Supply (V)	Temperature (˚C)
1	90nm	90.25	0.9	27
2		104.51		55
3		105.47		120
4		86.00	1.2	27
5		97.77		55
6		104.45		120
7		71.91	1.5	27
8		84.99		55
9		101.36		120

Table 6.12 (b) : Performance parameter of XOR gate block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	90.25	1.411	28.214	0.9	27
2		86.00	1.729	37.265	1.2	
3		71.91	2.062	45.921	1.5	

6.7 Low Power Half Adder Block using MGFCAL:

Schematic of low power HALF ADDER block is depicted in fig 6.13 and the output waveform of the SUM and CARRY of the half adder block is illustrated in fig 6.14 along with all the performance parameters of the low power Half adder block which are shown in table 6.13. And performance parameter of Half adder block using conventional CMOS logic is shown in table 6.14.

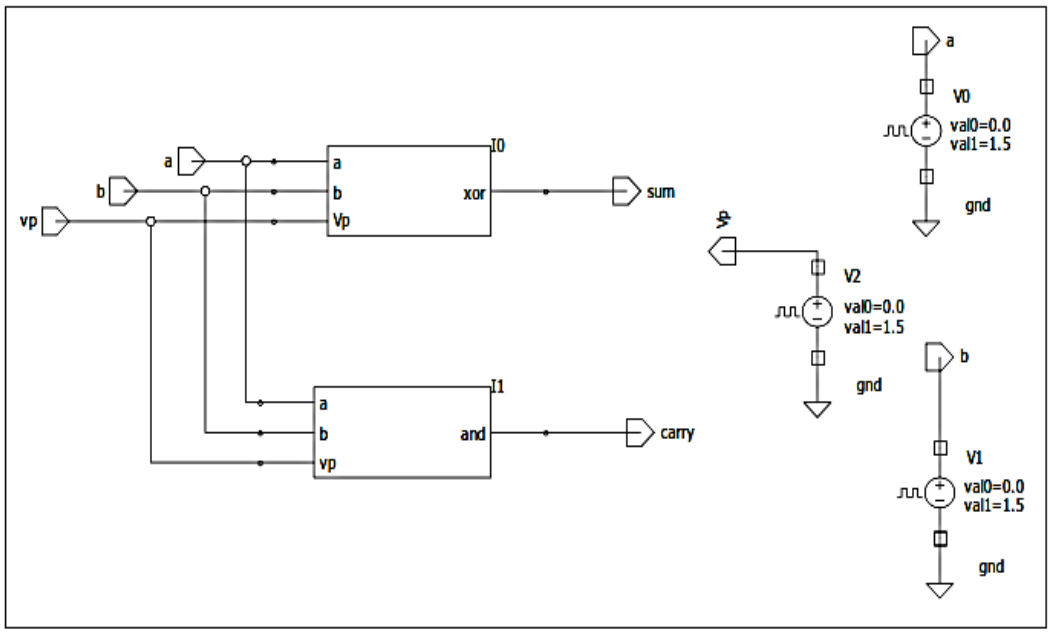

Fig 6.13: Low Power Half Adder block using MGFCAL.

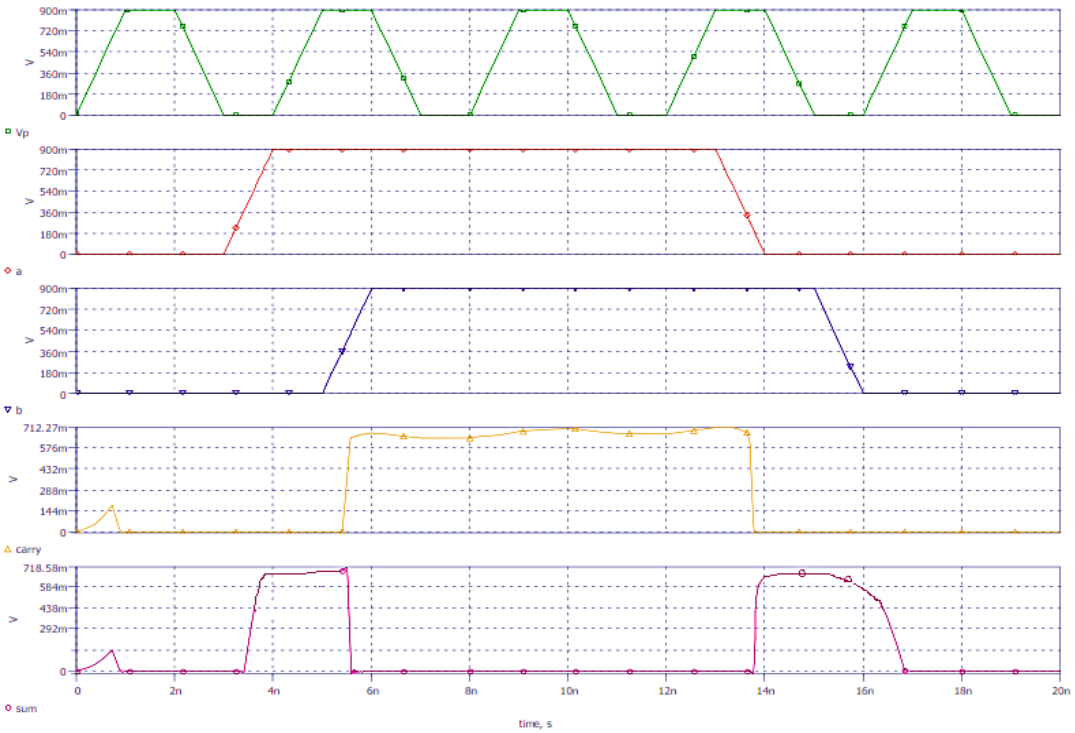

Fig 6.14: Output waveform of Low Power Half Adder block

Table 6.13 (a): Delay calculation of Half Adder block using MGFCAL

SUM			CARRY		
Delay (ps)	**Voltage (V)**	**Temperature (˚C)**	**Delay (ps)**	**Voltage (V)**	**Temperature (˚C)**
319.48	0.9	27	243.86	0.9	27
323.18		55	247.61		55
326.71		120	251.10		120
234.96	1.2	27	191.67	1.2	27
252.54		55	198.74		55
272.96		120	206.21		120
230.61	1.5	27	178.95	1.5	27
245.35		55	183.27		55
266.70		120	187.37		120

Table 6.13 (b): Performance parameter of Half Adder block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	319.48	2.412	68.47	0.9	27
2		234.96	4.927	234.82	1.2	
3		230.61	14.524	406.84	1.5	

Table 6.14 (a): Delay calculation of Half Adder block using conventional CMOS logic

SUM			CARRY		
Delay (ps)	Voltage (V)	Temperature (˚C)	Delay (ps)	Voltage (V)	Temperature (˚C)
90.25	0.9	27	35.30	0.9	27
104.51		55	37.89		55
105.47		120	40.73		120
86.00	1.2	27	26.09	1.2	27
97.77		55	27.63		55
104.45		120	30.279		120
71.91	1.5	27	24.09	1.5	27
84.99		55	29.17		55
101.36		120	29.52		120

Table 6.14 (b) : Performance parameter of Half Adder block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	90.25	9.784	125.79	0.9	27
2		86.00	18.276	460.71	1.2	
3		71.91	36.134	821.73	1.5	

6.8 Proposed Adders using MGFCAL Technique:

6.8.1 Low Power Full Adder (LPFA) Block using MGFCAL:

Schematic of low power Full Adder block is depicted in fig 6.15 and the output waveform of the SUM and CARRY of the Full Adder block is illustrated in fig 6.16 along with all the performance parameters of the low power Full Adder block which are shown in table 6.15. And performance parameters of Full Adder block using conventional CMOS logic is shown in table 6.16.

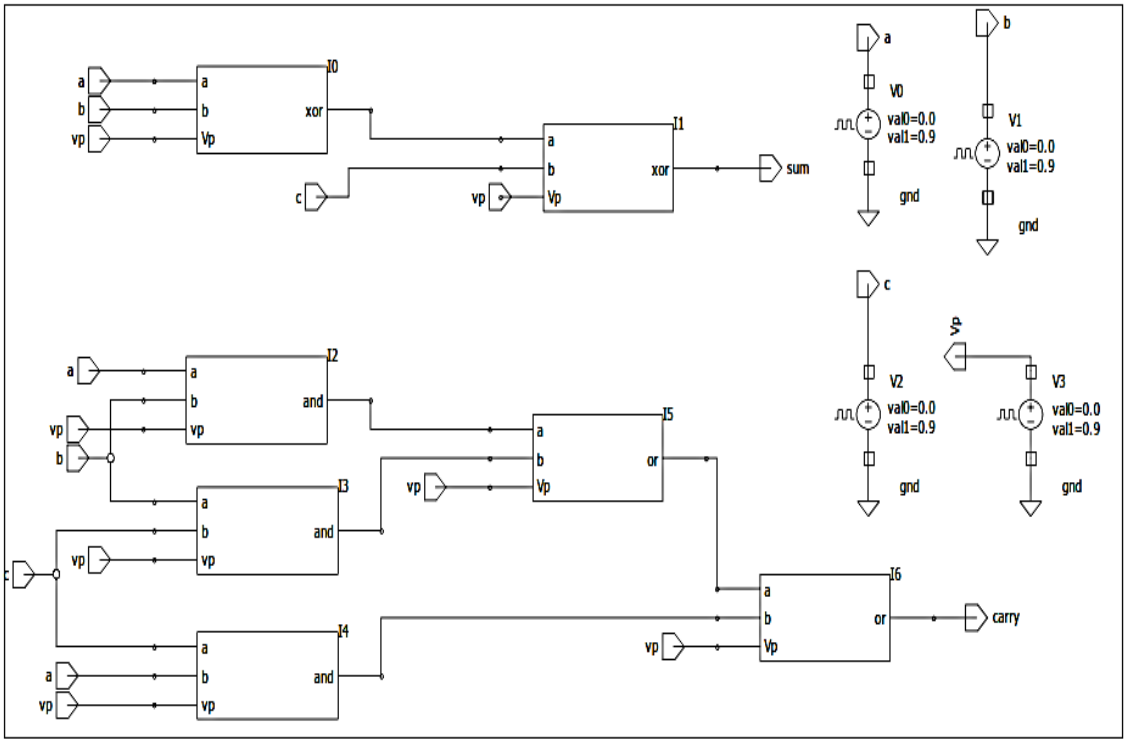

Fig 6.15: Low Power Full Adder block using MGFCAL

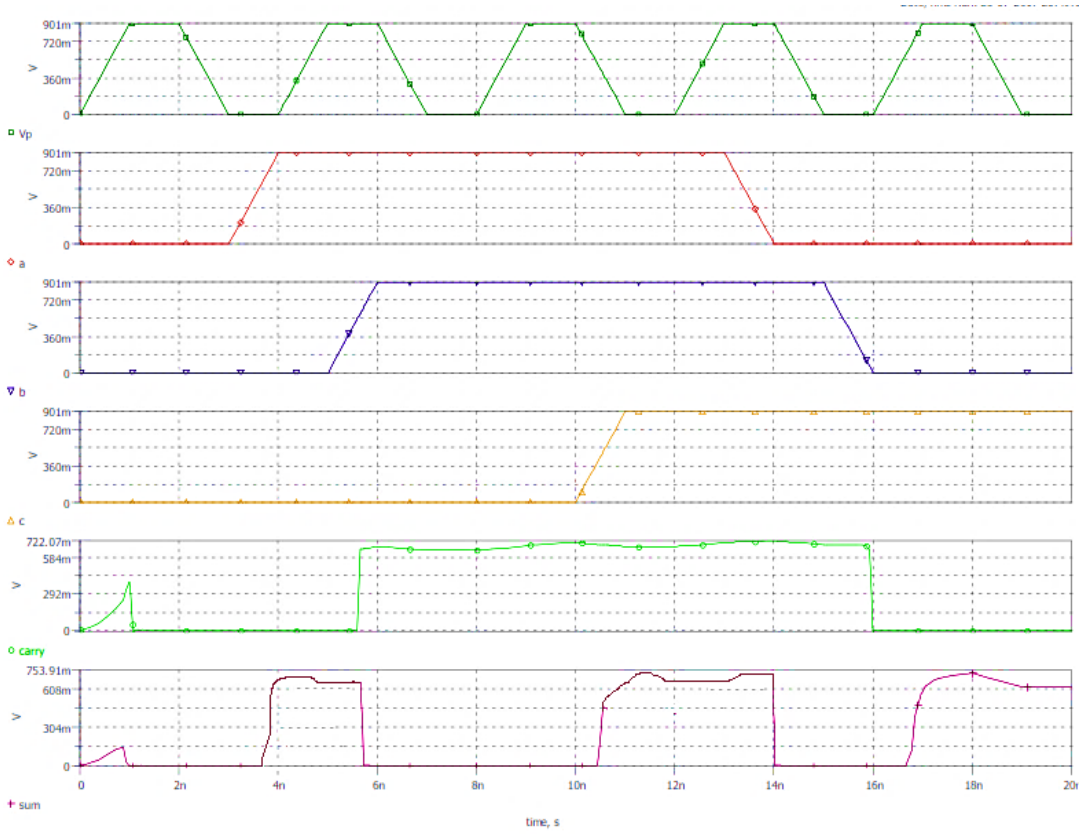

Fig 6.16: Output waveform of Low Power Full Adder block

Table 6.15 (a): Delay calculation of Full Adder block using MGFCAL

SUM			CARRY		
Delay (ps)	**Voltage (V)**	**Temperature (˚C)**	**Delay (ps)**	**Voltage (V)**	**Temperature (˚C)**
429.34	0.9	27	432.93	0.9	27
459.04		55	468.23		55
543.39		120	560.27		120
326.15	1.2	27	333.25	1.2	27
332.01		55	348.15		55
376.66		120	399.08		120
263.34	1.5	27	300.62	1.5	27
283.59		55	347.27		55
328.46		120	273.32		120

Table 6.15 (b): Performance parameter of Full Adder block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	432.93	4.513	90.261	0.9	27
2		333.25	12.601	252.01	1.2	
3		300.62	26.082	521.64	1.5	

Table 6.16 (a): Delay calculation of Full Adder block using conventional CMOS logic

SUM			CARRY		
Delay (ps)	Voltage (V)	Temperature (˚C)	Delay (ps)	Voltage (V)	Temperature(˚C)
140.20	0.9	27	45.17	0.9	27
160.26		55	50.89		55
165.21		120	55.70		120
66.85	1.2	27	41.57	1.2	27
81.05		55	43.25		55
110.62		120	45.67		120
55.86	1.5	27	40.23	1.5	27
71.23		55	42.25		55
104.23		120	43.77		120

Table 6.16 (b) : Performance parameter of Full Adder block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply(V)	Temperature (˚C)
1	90nm	140.20	31.778	635.57	0.9	27
2		66.85	87.833	1756.7	1.2	
3		55.86	173.68	2932.9	1.5	

6.8.2 Low Power Half Adder based Full Adder (LPHBF) Block using MGFCAL:

Schematic of low power Half Adder based Full Adder block is depicted in fig 6.17 and the output waveform of the SUM and CARRY of the Half Adder based Full Adder block is illustrated in fig 6.18 along with all the performance parameters of the low power Half Adder based Full Adder block which are shown in table 6.17. And performance parameters of Half Adder based Full Adder block using conventional CMOS logic is shown in table 6.18.

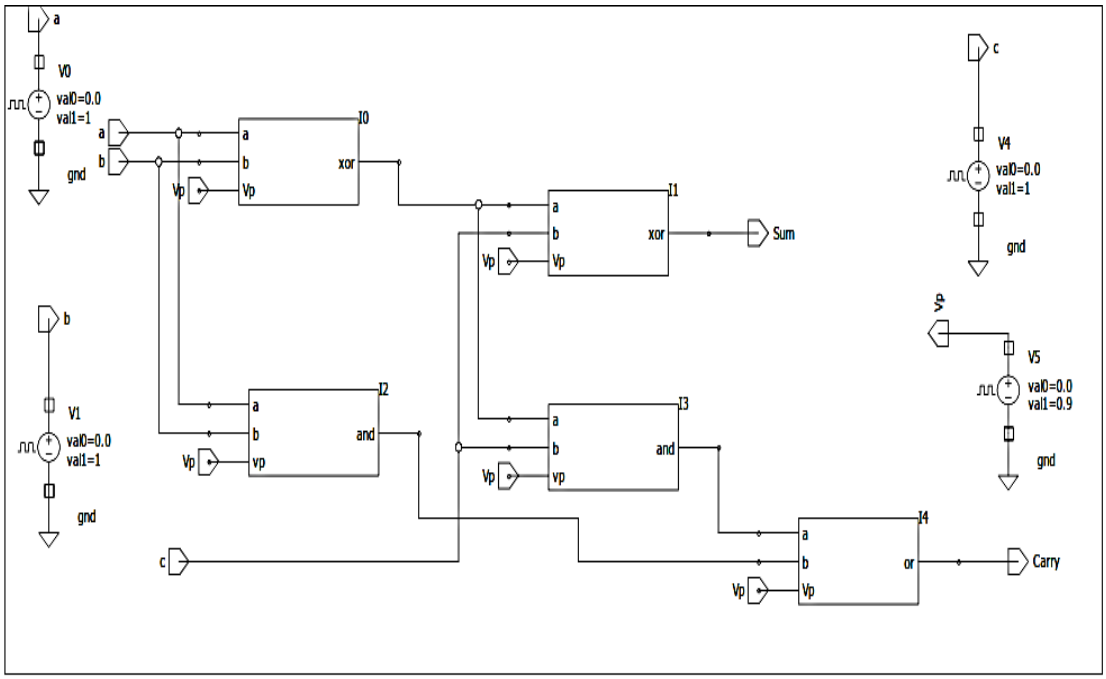

Fig 6.17: Low Power Half Adder based Full Adder block using MGFCAL

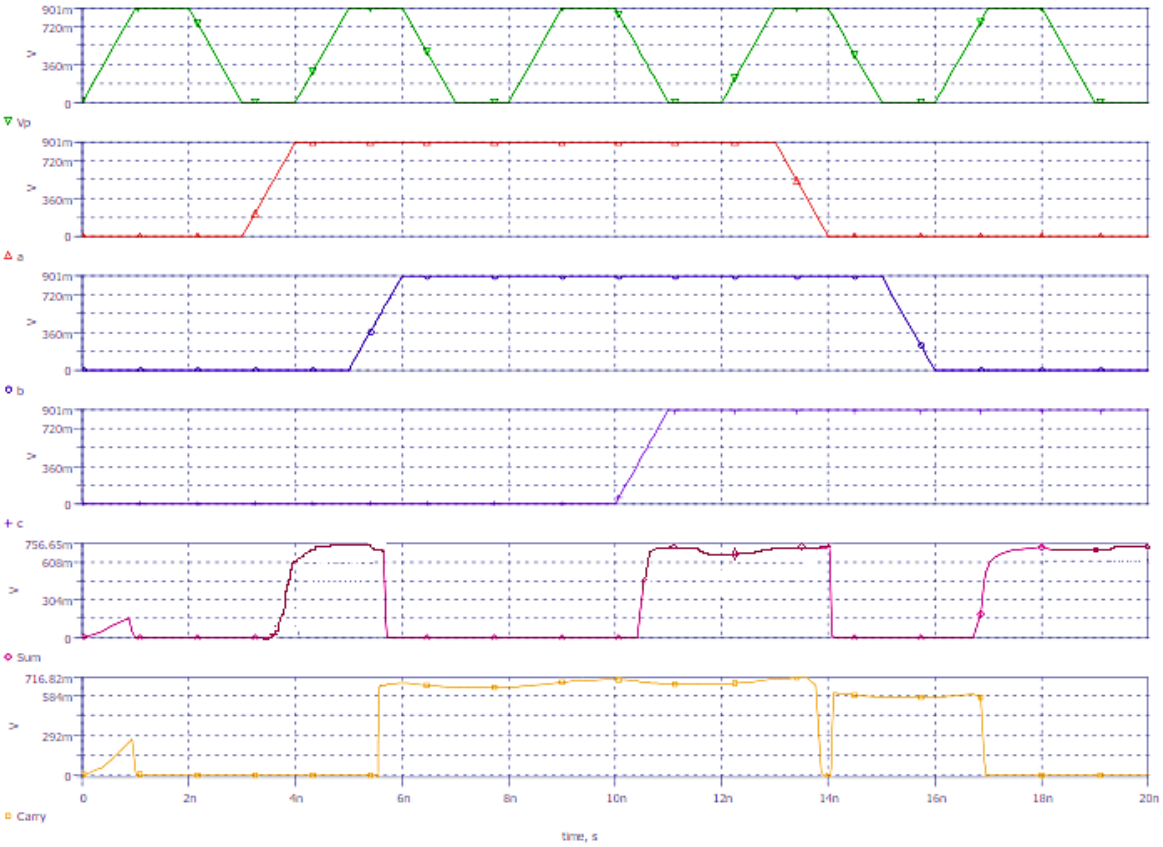

Fig 6.18: Output waveform of Low Power Half Adder based Full Adder block

Table 6.17 (a): Delay calculation of Half Adder based Full Adder block using MGFCAL

SUM			CARRY		
Delay (ps)	**Voltage (V)**	**Temperature (˚C)**	**Delay (ps)**	**Voltage (V)**	**Temperature (˚C)**
344.35	0.9	27	269.41	0.9	27
358.65		55	274.70		55
403.02		120	305.04		120
340.95	1.2	27	257.78	1.2	27
355.03		55	262.64		55
400.18		120	302.24		120
326.58	1.5	27	253.16	1.5	27
340.27		55	260.47		55
380.51		120	300.08		120

Table 6.17 (b): Performance parameter of Half Adder based Full Adder block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	344.35	4.459	89.144	0.9	27
2		340.95	12.437	248.74	1.2	
3		326.58	25.028	500.56	1.5	

Table 6.18 (a): Delay calculation of Half Adder based Full Adder block using conventional CMOS logic

SUM			CARRY		
Delay (ps)	Voltage (V)	Temperature (˚C)	Delay (ps)	Voltage (V)	Temperature(˚C)
61.42	0.9	27	101.25	0.9	27
101.34		55	119.65		55
105.23		120	120.35		120
56.69	1.2	27	98.45	1.2	27
63.70		55	100.73		55
76.17		120	115.38		120
40.25	1.5	27	95.25	1.5	27
56.94		55	99.65		55
74.80		120	110.35		120

Table 6.18 (b): Performance parameter of Half Adder based Full Adder block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	101.25	12.078	241.56	0.9	27
2		98.45	35.532	710.64	1.2	
3		95.28	81.674	1560	1.5	

6.8.3 Low Power Ripple Carry Adder (LPRCA) Block using MGFCAL:

Schematic of Low Power Ripple Carry Adder block is depicted in fig 6.19 and the output waveform of the SUM and CARRY of the Ripple Carry Adder block is illustrated in fig 6.20 along with all the performance parameters of the Low Power Ripple Carry Adder block which are shown in table 6.19. And performance parameters of Ripple Carry Adder block using conventional CMOS logic is shown in table 6.20.

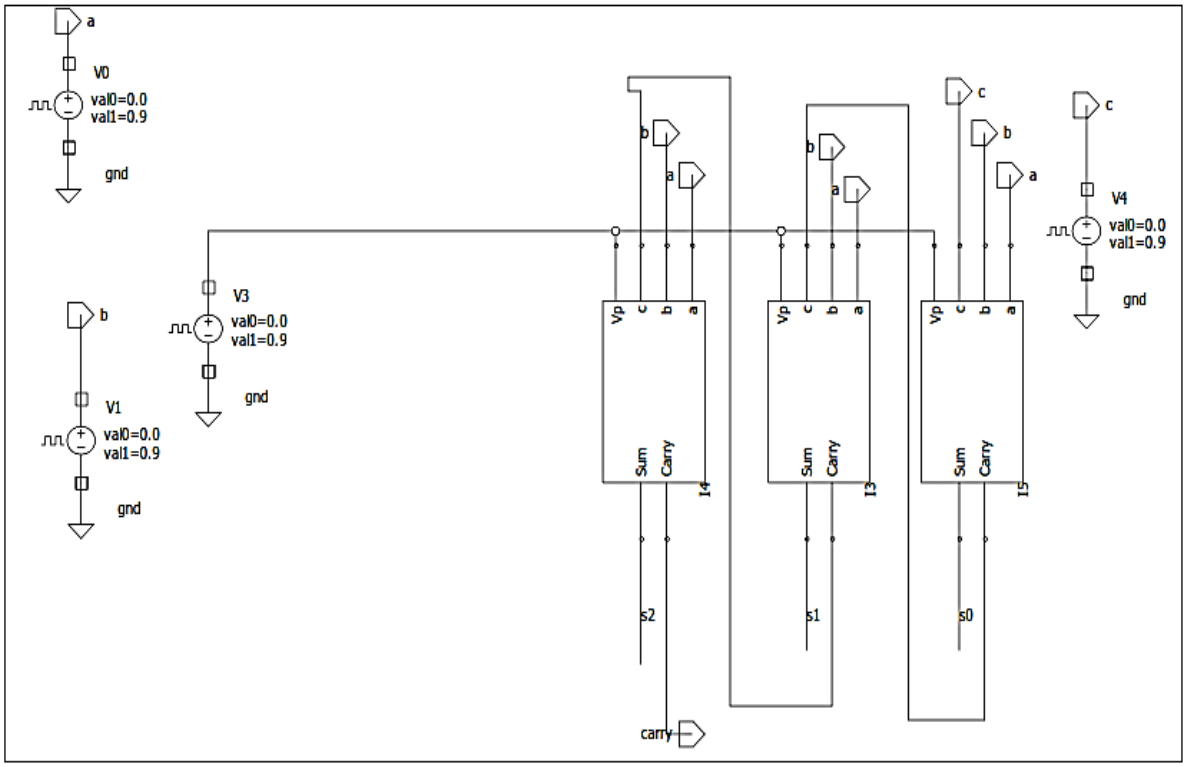

Fig 6.19: Low Power Ripple Carry Adder block using MGFCAL

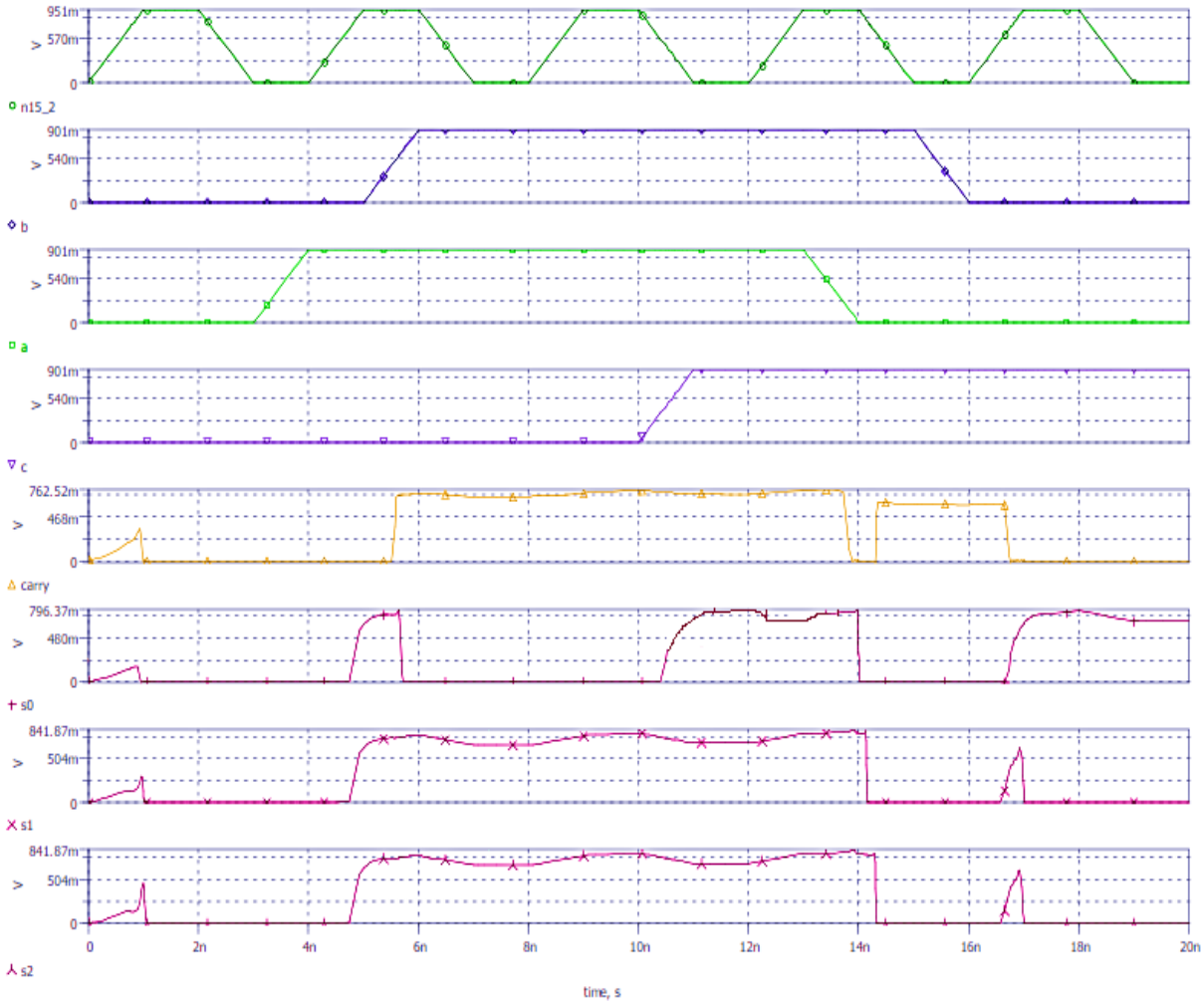

Fig 6.20: Output waveform of Low Power Ripple Carry Adder block

Table 6.19 (a): Delay calculation of Ripple Carry Adder block using MGFCAL

SUM			CARRY		
Delay (ps)	**Voltage (V)**	**Temperature (˚C)**	**Delay (ps)**	**Voltage(V)**	**Temperature (˚C)**
836.84	0.9	27	531.96	0.9	27
931.06		55	588.46		55
1200.32		120	697.10		120
495.84	1.2	27	411.86	1.2	27
544.71		55	426.23		55
682.34		120	451.62		120
400.57	1.5	27	367.55	1.5	27
439.24		55	406.28		55
551.23		120	449.34		120

Table 6.19 (b): Performance parameter of Ripple Carry Adder block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	836.84	36.284	204.75	0.9	27
2		495.63	62.472	379.43	1.2	
3		400.57	105.874	563.57	1.5	

Table 6.20 (a): Delay calculation of Ripple Carry Adder block using conventional CMOS logic

SUM			CARRY		
Delay (ps)	Voltage (V)	Temperature (˚C)	Delay (ps)	Voltage (V)	Temperature (˚C)
79.49	0.9	27	82.21	0.9	27
81.37		55	95.74		55
90.26		120	108.32		120
56.25	1.2	27	56.52	1.2	27
65.32		55	62.61		55
79.29		120	86.01		120
38.79	1.5	27	43.59	1.5	27
55.05		55	49.56		55
77.64		120	65.45		120

Table 6.20 (b) : Performance parameter of Ripple Carry Adder block using conventional CMOS logic.

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (pJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	82.21	91.625	1.236	0.9	27
2		56.52	175.783	1.952	1.2	
3		43.59	296.256	3.441	1.5	

6.8.4 Low Power Look Ahead Carry Adder (LPLCA) Block using MGFCAL :

Schematic of Low Power Look Ahead Carry Adder block is depicted in fig 6.21 and the output waveform of the SUM and CARRY of the Look Ahead Carry Adder block is illustrated in fig 6.22 along with all the performance parameters of the low power Look Ahead Carry Adder block which are shown in table 6.21. And performance parameter of Look Ahead Carry Adder block using conventional CMOS logic is shown in table 6.22.

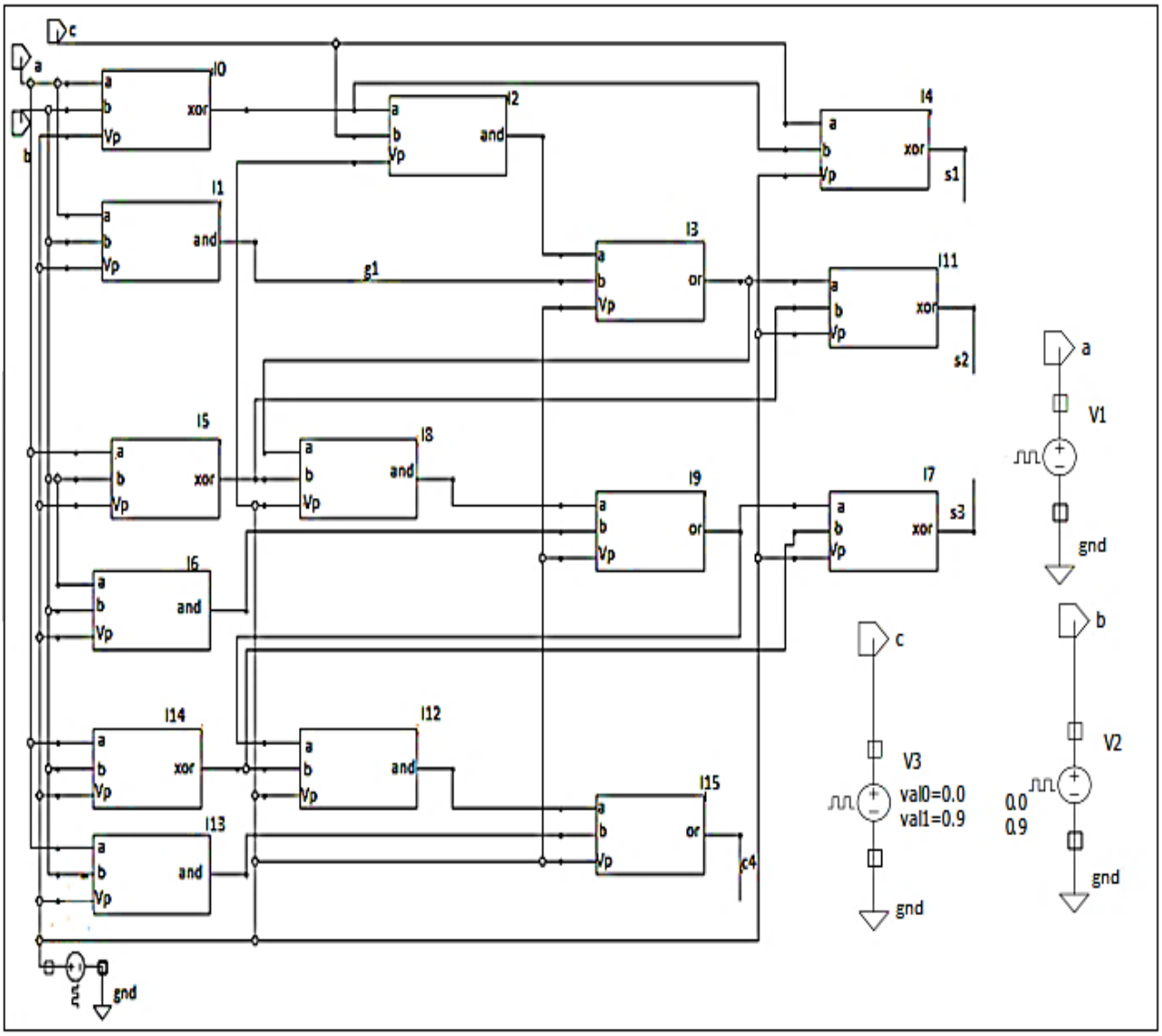

Fig 6.21: Low Power Look Ahead Carry Adder block using MGFCAL

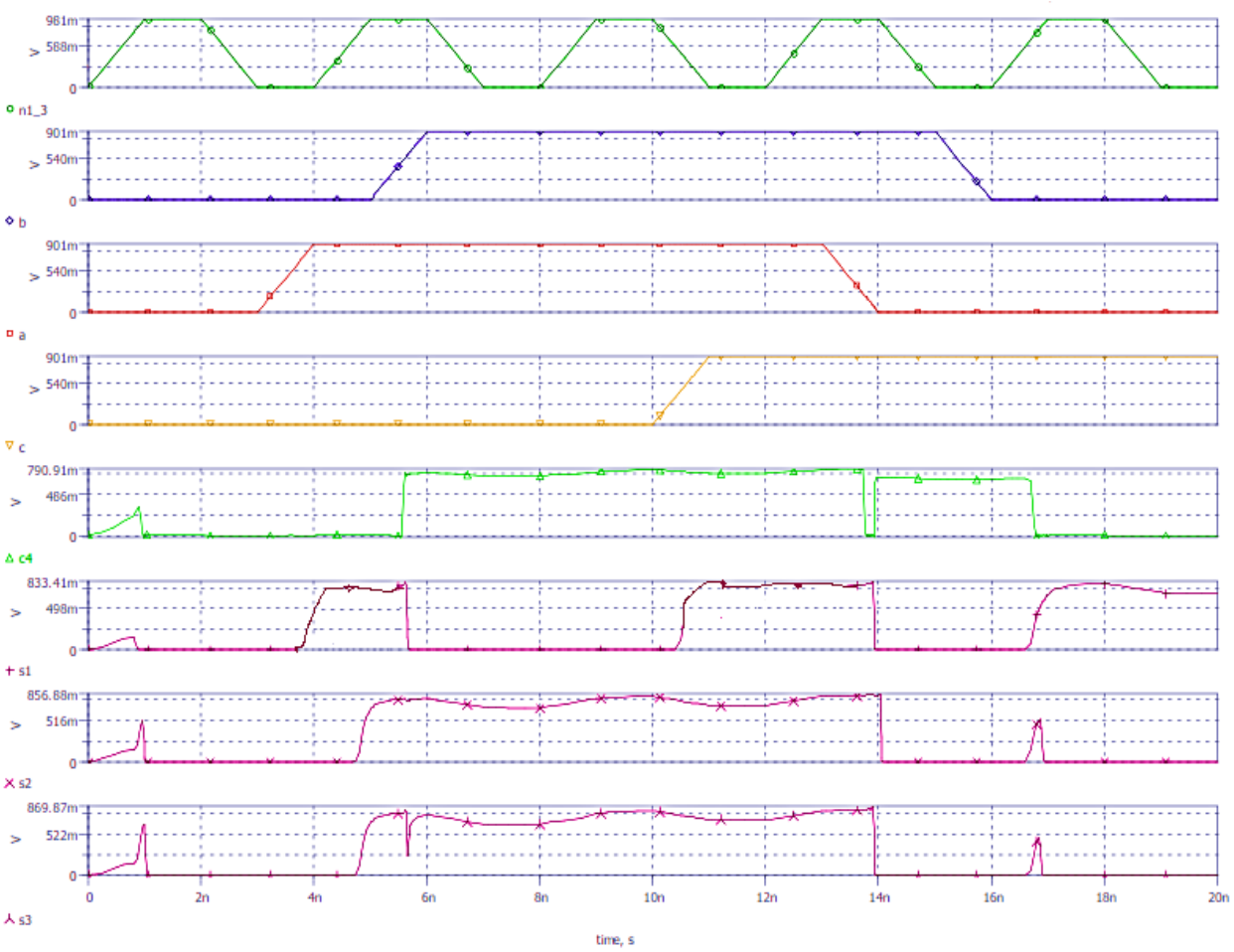

Fig 6.22: Output waveform of Low Power Look Ahead Carry Adder block

Table 6.21 (a): Delay calculation of Look Ahead Carry Adder block using MGFCAL

SUM			CARRY		
Delay (ps)	**Voltage (V)**	**Temperature(˚C)**	**Delay (ps)**	**Voltage (V)**	**Temperature(˚C)**
468.57	0.9	27	552.46	0.9	27
515.33		55	584.75		55
600.71		120	684.42		120
318.64	1.2	27	466.58	1.2	27
340.95		55	414.84		55
400.79		120	469.82		120
269.31	1.5	27	411.25	1.5	27
289.27		55	416.59		55
338.72		120	450.32		120

Table 6.21 (b): Performance parameter of Look Ahead Carry Adder block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply	Temperature (˚C)
1	90nm	552.46	25.246	784.92	0.9	27
2		466.58	71.582	2211.7	1.2	
3		411.25	93.679	5073.4	1.5	

Table 6.22 (a): Delay calculation of Look Ahead Carry Adder block using conventional CMOS logic

SUM			CARRY		
Delay (ps)	Voltage (V)	Temperature (˚C)	Delay (ps)	Voltage (V)	Temperature (˚C)
120.58	0.9	27	138.65	0.9	27
134.35		55	145.17		55
149.54		120	150.89		120
105.65	1.2	27	125.47	1.2	27
122.52		55	138.35		55
136.22		120	145.87		120
95.45	1.5	27	113.49	1.5	27
110.52		55	120.41		55
123.73		120	129.38		120

Table 6.22 (b) : Performance parameter of Look Ahead Carry Adder block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (pJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	138.65	67.25	1.142	0.9	27
2		125.47	162.89	2.317	1.2	
3		113.49	247.335	2.985	1.5	

6.8.5 Low Power Carry Select Adder (LPCSA) Block using MGFCAL:

Schematic of low power Carry Select Adder block is depicted in fig 6.23 and the output waveform of the SUM and CARRY of the Carry Select Adder block is illustrated in fig 6.24 along with all the performance parameters of the low power Carry Select Adder block which are shown in table 6.23. And performance parameters of Carry Select Adder block using conventional CMOS logic is shown in table 6.24.

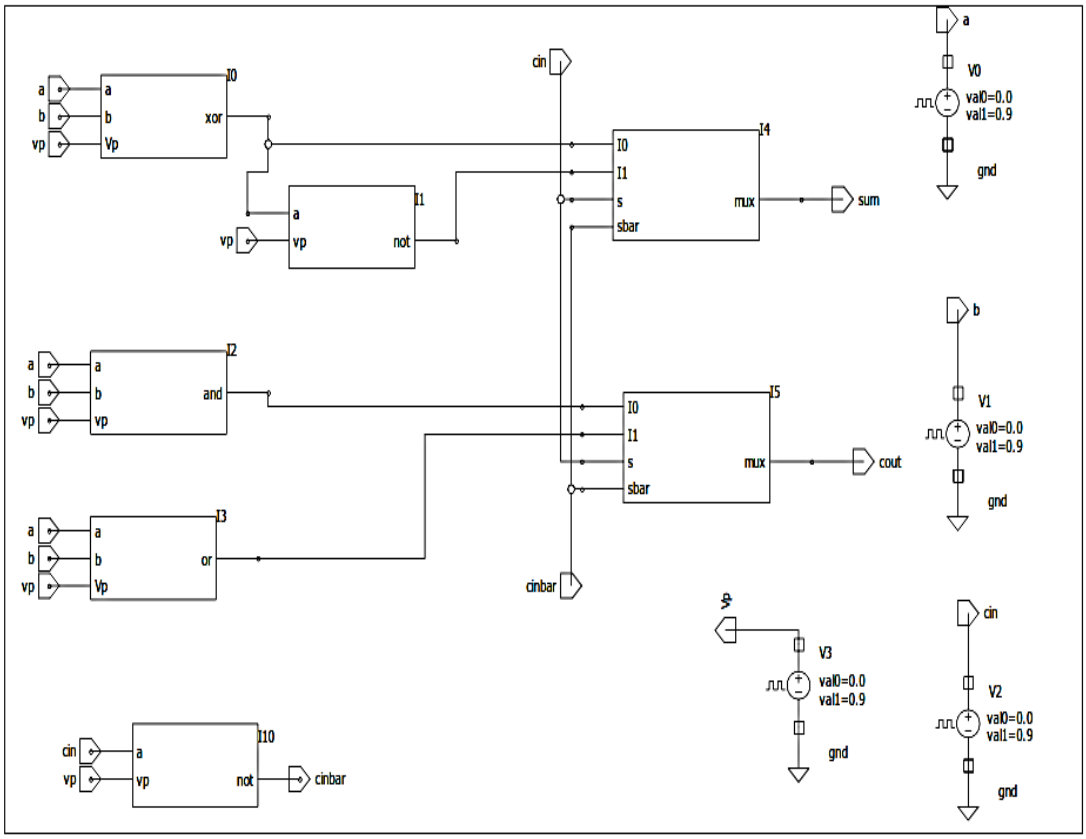

Fig 6.23: Low Power Carry Select Adder block using MGFCAL

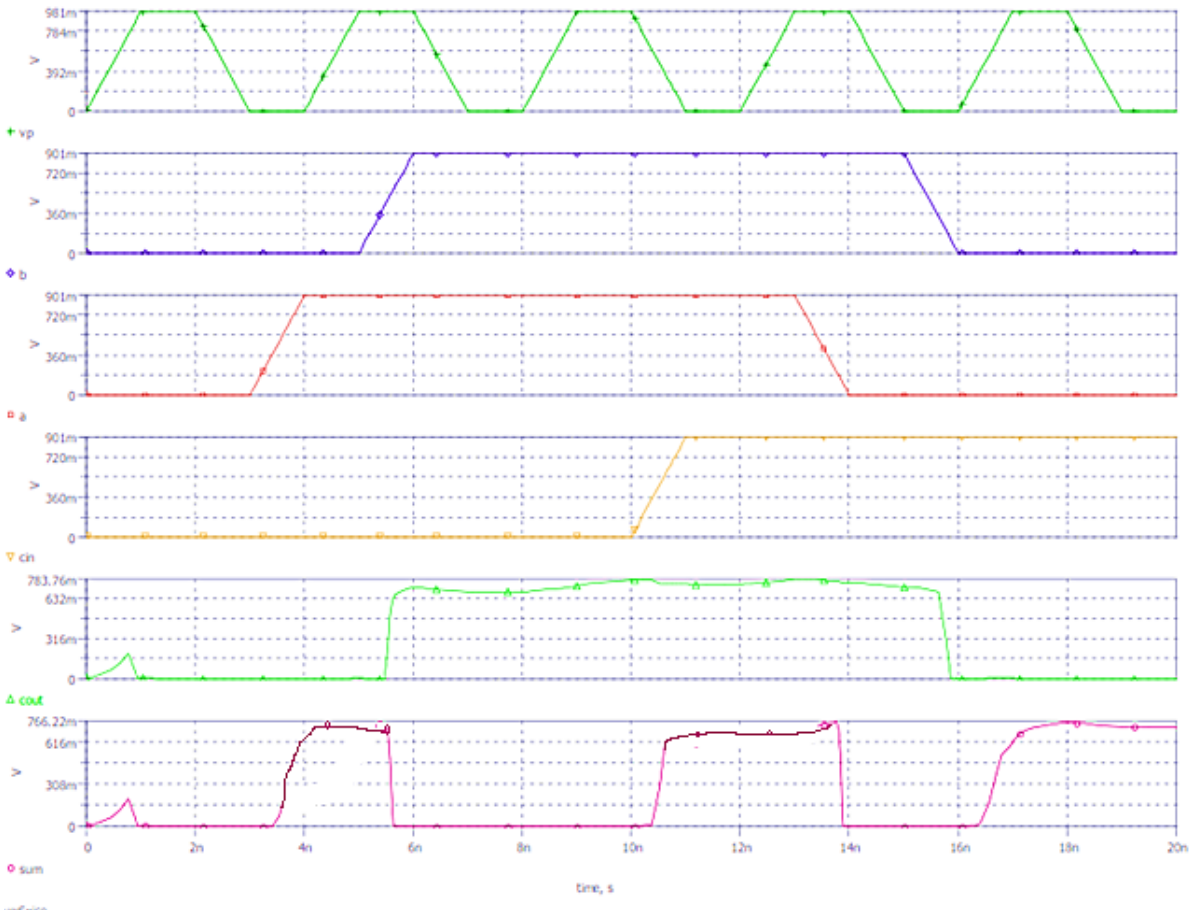

Fig 6.24: Output waveform of Low Power Carry Select Adder block

Table 6.23 (a): Delay calculation of Carry Select Adder block using MGFCAL

SUM			CARRY		
Delay (ps)	**Voltage (V)**	**Temperature (˚C)**	**Delay (ps)**	**Voltage (V)**	**Temperature (˚C)**
367.54	0.9	27	333.68	0.9	27
406.59		55	339.56		55
451.51		120	366.09		120
274.57	1.2	27	228.70	1.2	27
286.89		55	274.35		55
328.80		120	346.28		120
243.45	1.5	27	218.95	1.5	27
255.41		55	263.71		55
280.99		120	298.25		120

Table 6.23 (b): Performance parameter of Carry Select Adder block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	367.54	0.991	19.824	0.9	27
2		274.57	3.774	75.493	1.2	
3		243.45	10.477	209.55	1.5	

Table 6.24 (a): Delay calculation of Carry Select Adder block using conventional CMOS logic

SUM			CARRY		
Delay (ps)	Voltage (V)	Temperature (˚C)	Delay (ps)	Voltage (V)	Temperature (˚C)
108.81	0.9	27	35.51	0.9	27
124.04		55	42.45		55
135.95		120	43.09		120
45.20	1.2	27	32.52	1.2	27
65.45		55	41.50		55
81.61		120	42.43		120
32.74	1.5	27	15.87	1.5	27
35.24		55	21.34		55
66.45		120	40.31		120

Table 6.24 (b) : Performance parameter of Carry select Adder block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	108.81	12.098	241.96	0.9	27
2		45.20	31.582	630.57	1.2	
3		32.74	65.337	1362.72	1.5	

6.8.6 Low Power Hybrid Adder (LPHA) Block using MGFCAL:

Schematic of low power Hybrid Adder block is depicted in fig 6.25 and the output waveform of the SUM and CARRY of the Hybrid Adder block is illustrated in fig 6.26 along with all the performance parameters of the low power Hybrid Adder block which are shown in table 6.25. And performance parameters of Hybrid Adder block using conventional CMOS logic is shown in table 6.26.

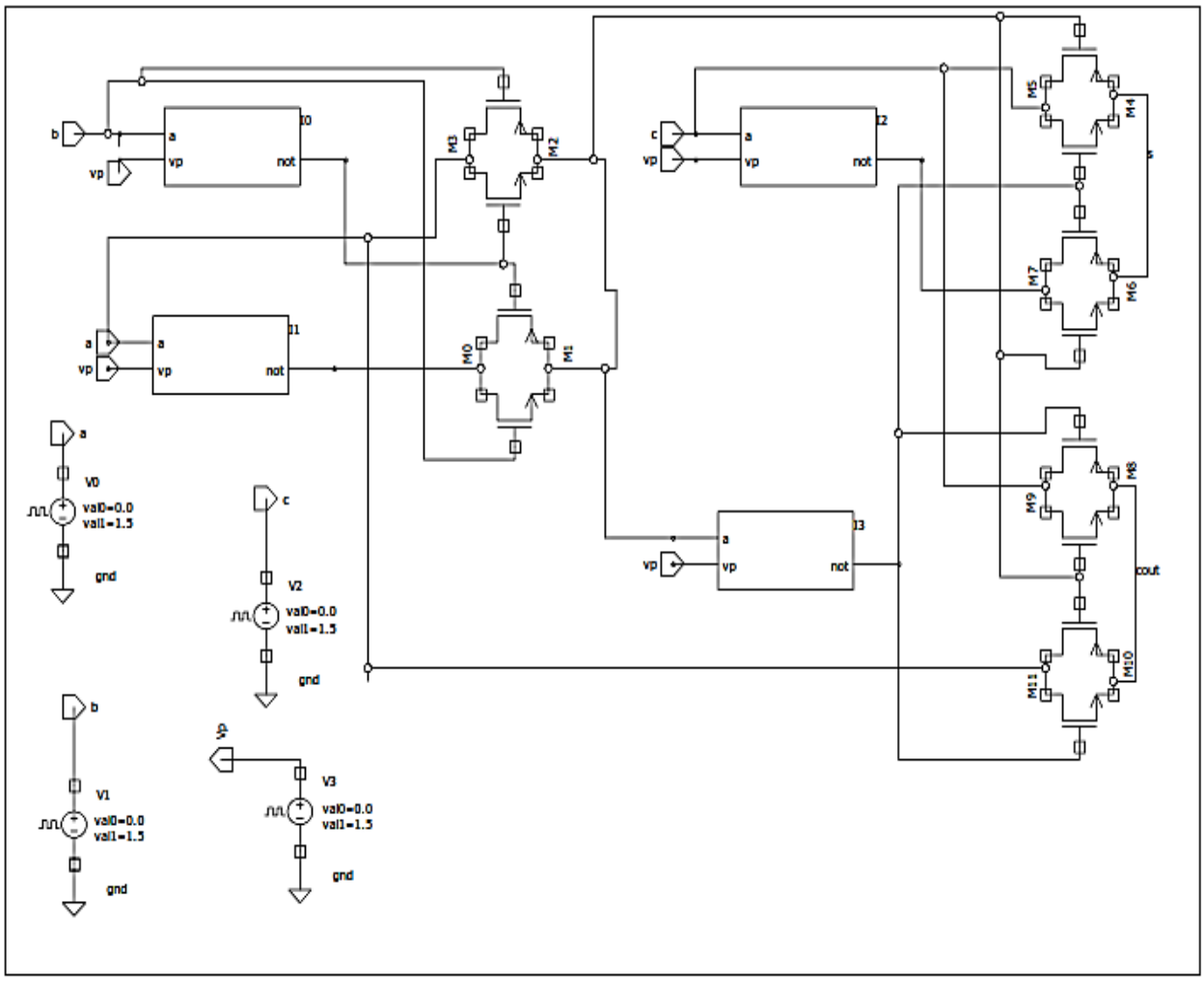

Fig 6.25 Low Power Hybrid Adder block using MGFCAL

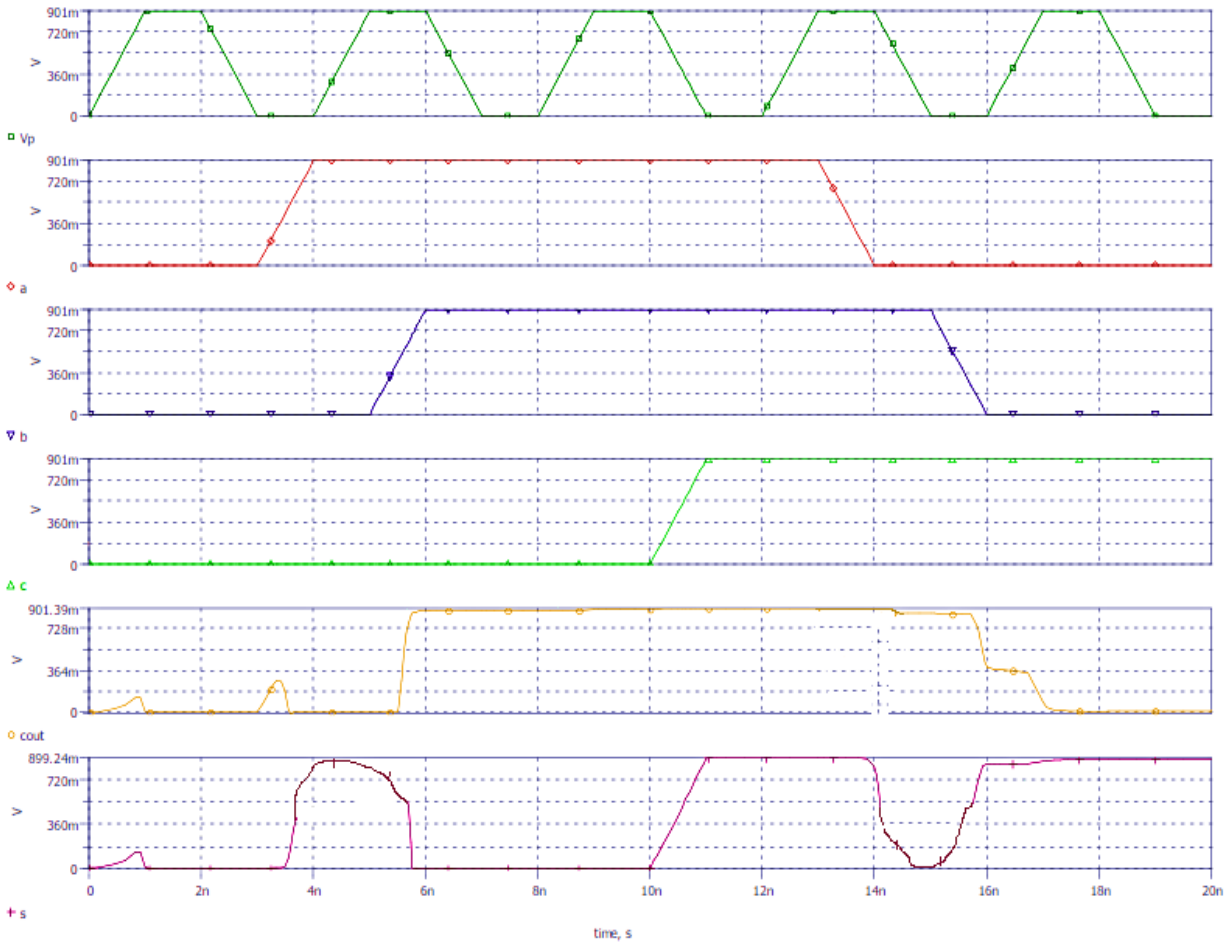

Fig 6.26: Output waveform of Low Power Hybrid Adder block

Table 6.25 (a): Delay calculation of Hybrid Adder block using MGFCAL

SUM			CARRY		
Delay (ps)	**Voltage (V)**	**Temperature (˚C)**	**Delay (ps)**	**Voltage (V)**	**Temperature(˚C)**
655.23	0.9	27	492.95	0.9	27
711.13		55	535.49		55
735.25		120	598.25		120
420.42	1.2	27	393.59	1.2	27
450.89		55	459.35		55
517.70		120	485.89		120
400.91	1.5	27	380.59	1.5	27
449.33		55	436.95		55
458.62		120	452.58		120

Table 6.25 (b): Performance parameter of Hybrid Adder block using MGFCAL

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	655.23	0.00576	9.612	0.9	27
2		420.42	2.539	30.814	1.2	
3		400.91	8.914	83.189	1.5	

Table 6.26 (a): Delay calculation of Hybrid Adder block using conventional CMOS logic

SUM			CARRY		
Delay (ps)	Voltage (V)	Temperature (˚C)	Delay (ps)	Voltage (V)	Temperature (˚C)
178.11	0.9	27	128.50	0.9	27
197.14		55	130.24		55
214.21		120	145.55		120
127.06	1.2	27	120.09	1.2	27
141.83		55	125.69		55
188.97		120	138.37		120
112.59	1.5	27	101.49	1.5	27
135.68		55	105.17		55
172.54		120	120.93		120

Table 6.26 (b) : Performance parameter of Hybrid Adder block using conventional CMOS logic

S.No.	Technology Node	Delay (ps)	Power Dissipation (µW)	Energy (fJ)	Voltage Supply (V)	Temperature (˚C)
1	90nm	178.11	4.862	97.252	0.9	27
2		127.06	17.532	350.63	1.2	
3		112.59	36.251	728.68	1.5	

CHAPTER – 7

7 CONCLUSION AND FUTURE SCOPE

7.1 Conclusion:

In this work, the performance parameters of proposed adder circuit structures are calculated in terms of power dissipation delay and energy at three different voltage levels. And the delay is calculated for three different voltages at three different temperatures.

The calculated power dissipation for the proposed low power full adder (LPFA) circuit is decreased by 85.79% at 0.9V, 85.65% at 1.2V and 84.98% at 1.5V as compared to the CMOS logic, for the proposed low power full adder based Half Adder (LPHBF) circuit is decreased by 63.08% at 0.9V, 64.99% at 1.2V and 69.35% at 1.5V as compared to the CMOS logic, for the proposed low power Ripple Carry Adiabatic (LPRCA) circuit is decreased by 60.39% at 0.9V, 64.46% at 1.2V and 64.28% at 1.5V as compared to the CMOS logic, for the proposed low power Look ahead carry adder (LPLCA) circuit is decreased by 62.45% at 0.9V, 56.05% at 1.2V and 62.12% at 1.5V as compared to the CMOS logic, for the proposed low power Carry select adder (LPCSA) circuit is decreased by 91.80% at 0.9V, 88.05% at 1.2V and 83.96% at 1.5V as compared to the CMOS logic and for the proposed low power hybrid adder (LPHA) circuit is decreased by 99.88% at 0.9V, 85.51% at 1.2V and 75.41% at 1.5V as compared to the CMOS logic .

Thus, the power dissipation can be reduced to a greater extent in the proposed circuit without affecting the other parameters to a much extent. Although the value of delay is increased in the MGFCAL circuit, but still the amount of decrement of power dissipation in the circuit is quite good, for the better applications in the low power VLSI devices. This is the plus point of using the Modified Glitch Free Cascadable Adiabatic Logic, which provides excellent reduction in the power dissipation to a greater extent.

7.2 Future Scope:

This work was an attempt to analyse the demand for reducing the power dissipation in the circuit, as need for low power devices are increasing day by day in the present era. The proposed circuit gives an advantage of highly improved power reduction in which the power is reduced to a greater extent. The proposed circuit can also be improved in the future in terms of delay. Thus, a pathway has been paved for future researchers to exploit the MGFCAL benefits of power reduction and other bigger applications can also be structured by using these circuits and the proposed adder can be utilized in various applications like ALU circuits, multipliers, computational devices, etc. where power reduction is the main issue.

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Appendices

Appendix I:
Comparison in Terms of Power Dissipation

The comparison of the power dissipation between proposed adder design using MGFCAL and the conventional CMOS at voltage level 0.9V is shown in the below fig.6.27.

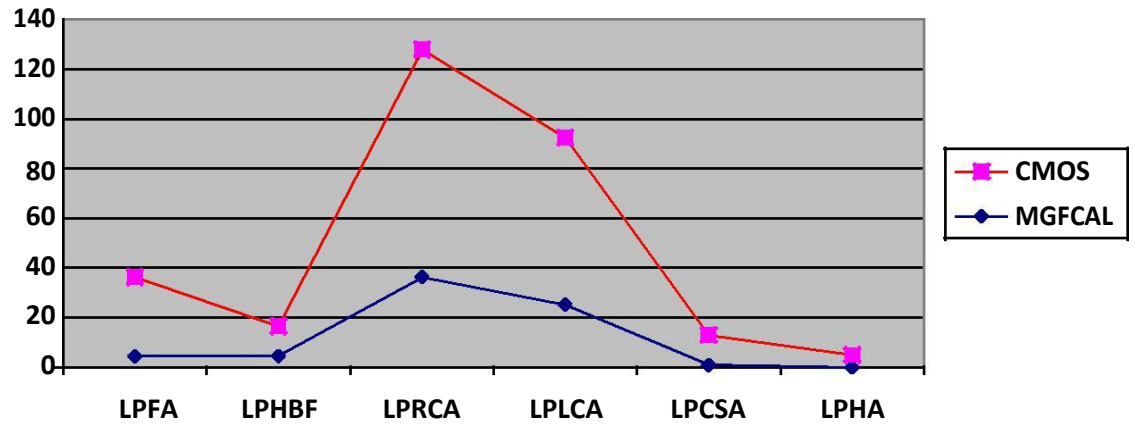

Fig 6.27: Comparison of power dissipation (µW) of proposed adder circuits at 0.9V.

The comparison of the power dissipation between proposed adder design using MGFCAL and the conventional CMOS at voltage level 1.2 V is shown in the below fig.6.28.

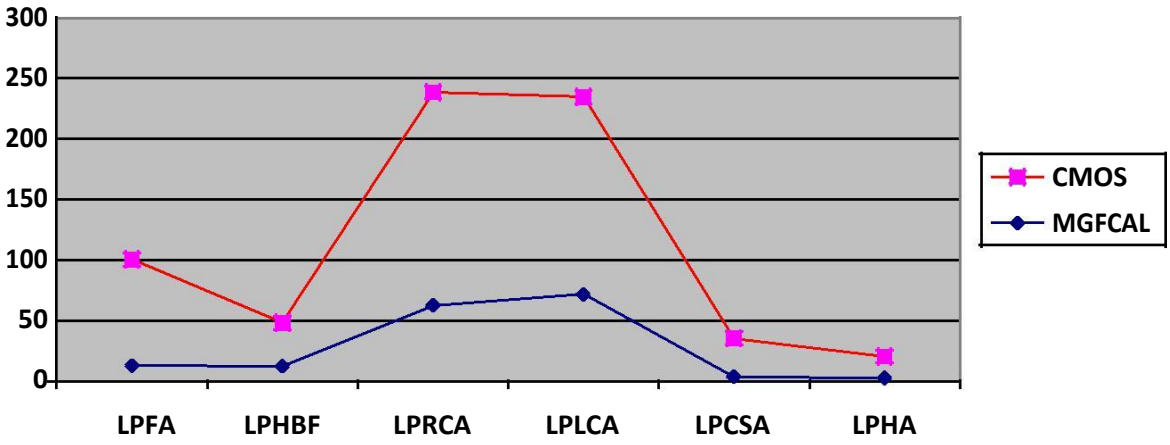

Fig 6.28: Comparison of power dissipation (µW) of proposed adder circuits at 1.2V.

The comparison of the power dissipation between proposed adder design using MGFCAL and the conventional CMOS at voltage level 1.5 V is shown in the below fig.6.29.

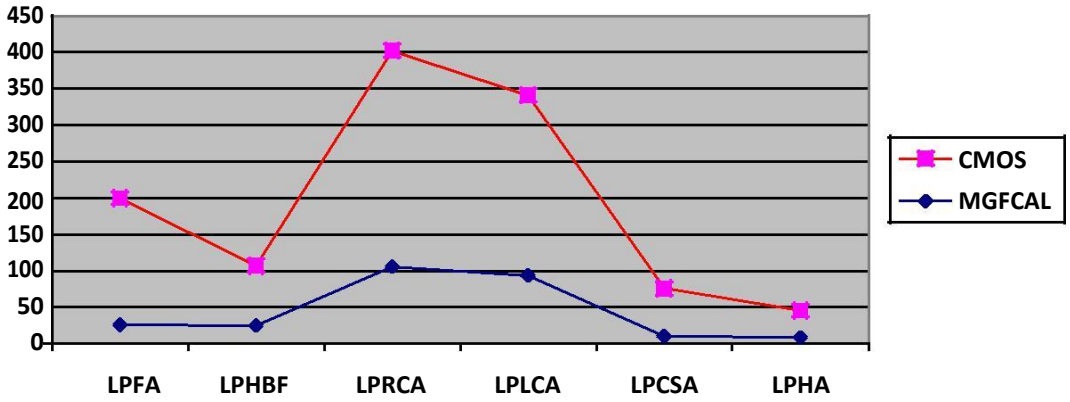

Fig 6.29: Comparison of power dissipation (µW) of proposed adder circuits at 1.5V

Appendix- II:
Published Paper

Flexible & Dry ECG Electrodes based on Carbon Nanotubes for Long-Term & Continuous Recording of Bio-signals

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***Abstract*— Carbon Nanotubes (CNTs) have attractive features for implementation as Electrocardiogram (ECG) electrode because of their small size, low density, high flexibility, good electrical conductivity, high aspect ratio and high elasticity. In this paper, we review the recent developments in the area of carbon nanotube based dry and flexible electrodes, for long- term and continuous recording of bio- signals. Also, we compare the performance of these CNT based electrodes with the conventional wet electrode (Ag/ AgCl).**

***Keywords*— Carbon Nanotubes (CNTs), Electrocardiogram (ECG), Dry, Flexible, Electrode, Bio-signals.**

I. INTRODUCTION

In 1991, Sumio Iijima, discovered the spectacular nanostructures called Carbon nanotubes [1] and very soon there was a boom of research papers related to the synthesis, properties, characteristics and the applications of this wonderful nano material for e.g. in OLEDs [2], diodes [3], field-effect transistors [4] etc. The amalgamation of two very ponderous fields (biomedical electronics and carbon nanotubes) brings very blossoming settlement when both are serviced well together. And thus, results in remarkable application. In the area of biomedical electronics, carbon nanotubes are bountifully used in- fashioning numerous electrodes for measurement of electrocardiogram (ECG) and Electroencephalography (EEG) signals.

II. ECG

ECG plays a very significant role in gathering meaningful and important information about a person's heart and performance. In the current cardiac medicine field, among all vital signs that keep record and track an individual's health, ECG is the standard and the primary diagnostic procedure for the persons suffering from cardiac diseases. Recently, great efforts have been made to make ECG monitoring an easy, efficient and easily available approach for people with cardiac problems and; especially, for those who are having severe cardiac problems and are at the risk of heart attack or stroke [5]. On the basis of 2011 death rate data, due to cardiovascular diseases (CVD), each day >2150 Americans die. That is an average of approximately 1 death in every 40 seconds. Americans who died of CVD in the year 2011 were approximately 1, 55,000 and aged < 65 years. In 2011, according to the report, 34% of deaths due to CVD occurred before the age of 75 years, which is less than 78.7 years, which is the current average life expectancy [6]. ECG is one of the commonly used diagnostic tests, which can be easily recorded. The basic aim of ECG monitoring in hospital settings includes simple heart rate and basic rhythm determination, diagnosis of complex arrhythmias, prolonged QT interval and myocardial ischemia [7]. The important factors that are affecting health and safety in modern society basically include fatigue, sleepiness and disturbed sleep [8]. But traditionally, the measurement of ECG signals outside laboratories, with the maintained robustness and quality, is difficult and rather impossible [9], [10].

III. CNT & ITS FLAVOURS

Carbon nanotubes are hollow cylinders of graphite sheets which have length-to-diameter ratio of up to $(1.32 \times 10^8):1$, which is quite greater than any other material [11]. Structurally, carbon nanotubes exhibit two flavours i.e., single-wall carbon nanotubes (SWNTs) and multiwall carbon nanotubes (MWNTs). CNTs have very good optical, electrical, mechanical and electrochemical properties, apart from high aspect ratio. They have high electrical conductivity (about 1000 times higher than copper wire) and high thermal conductivity (=2000 W Mk^{-1}) [12-16]. A tube made of a single graphite layer rolled up into a hollow cylinder is called a single-wall nanotube (SWNT). A tube comprising several, concentrically arranged graphite sheet cylinders is referred to as a multi-wall nanotube (MWNT) [17]. Multi-wall carbon nanotubes generally exhibit diameters from two to several hundred nanometers, lengths up to several microns and inter-tube spacing of around 0.34–0.35 nm. Depending on how the tube is rolled up, a carbon nanotube can be a metal or a semiconductor, [18]. Also it is somewhat easier to process MWNTs as compared to SWNTs [19].

IV. CONVENTIONAL ECG ELECTRODES

The most commonly regularly used bio electrodes in the clinical fields are of the gel type silver/silver chloride (Ag/ AgCl) , and these electrodes have the advantage that they are simple, lightweight, reliable, easy to use and cost effective. But, these electrodes have the drawbacks that the long-term use of these gel type electrodes may cause irritation to the skin [20] and cause allergic reactions and deterioration of signal quality due to drying of the gel with time and due to motion sensitivity and motion artifacts [21]. Conventional ECG sensors can lead to skin irritation, since they are in- direct contact with the patient's body. And also they can make monitoring an inconvenient process, if they are not convenient for the person using them. Finally, the main drawback is that, the signal quality degrades with time, that is, the constant

desirable signal quality is delivered for a limited period of time [5]. Due to the interface between the skin and electrolyte paste, signal noise is boosted up by the space charge layer present between the skin and electrolyte. Sweat is another cause of signal degradation. Noise is the prime cause which reduces resolution of wet surface electrodes. However, the combination of electrolyte drying and skin removal causes skin irritation and degrades signal level during long-term recording of the ECG signals [22]. In addition, the main reason for reduction of performance of wet electrodes is motion artifacts, because of the relative motion of electrodes with the body as well as drying of conductive gel [23].

V. FLEXIBLE & DRY ECG ELECTRODES BASED ON CNT

To clear up these complications and drawbacks of Ag/AgCl electrodes, dry surface electrodes have been employed. Thin-skin- like electrodes are also a modern advancement in the field of material sciences that uniformly laminate onto the surface of skin, without producing skin irritation [24], [25]. Even though several dry electrodes have been developed using metallic materials, but there are some limitations in their practicable use due to high electrode- to- skin impedance, poor biocompatibility, and abnormalities in the contact area at the time of motion. Soft polymer-based ECG dry electrodes are superior than metallic material based dry electrodes, as their use results in inconvenience-free long-term wear ability without any ill effects [26]. In some studies, it has been shown that to get a flexible, stretchable and conductive polymer based ECG electrode , polydimethylsiloxane (PDMS) is mixed with conductive materials such as silver microspheres, silver nanowires and CNTs. Silver micro particle based electrodes demonstrate good electrical conductivity and mechanical fidelity and reliability [27]. But the drawback is that, they are quickly non-contacted when the polymer is stretched, bent or twisted. When PDMS is used with silver nanowires, the thin film electrodes commonly suffer poor resistance to tearing and inadequate compliance to curved surface, which restrict their application. In other words, we can say that it is less flexible [28].

The PDMS on mixing with the CNTs fiber shows a great advantage that under numerous stretching- and- releasing cycles, there is very little deviation in the resistance (= 1%), up to a pre-strain level of 40%, which, as stretchable conductor signifies impressive stability, support and repeatability in performance [29]. Additionally, the CNTs are tangled, twisted, mixed up and assembled randomly, which allows them to have a better contact with each other even when the polymer is bent or stretched. Therefore, for analysis of bio-signals, the CNTs are a preferred choice when compared with silver microspheres or silver nanowires, for application with conductive polymer [30]. Dry electrodes made of CNTs offer a lot of advantages such as great electrical conductivity, tremendous bio-compatibility, high flexibility; and the value of electrode- to- skin impedance is quite low. S. M. Lee et al [30] reported the fabrication of a self-adhesive carbon nanotube based electrode that can record ECG signals without damaging the skin. They developed an ECG patch which is self-adhesive and long-term wearable, on which a scheme of measurement and wireless communication system is integrated. The advantage of the patch is that it is also useful for a person with wrinkled skin as it can conformally laminate even into the wrinkles of skin, without any drawback. It also provides robust contact, and sticks itself very fast onto skin, without any additional accessories [30]. By well-dispersed blending of CNTs in adhesive Polydimethylsiloxane (aPDMS), the ECG patch was fabricated as it has impressive stability and repeatability in performance as stretchable conductor.

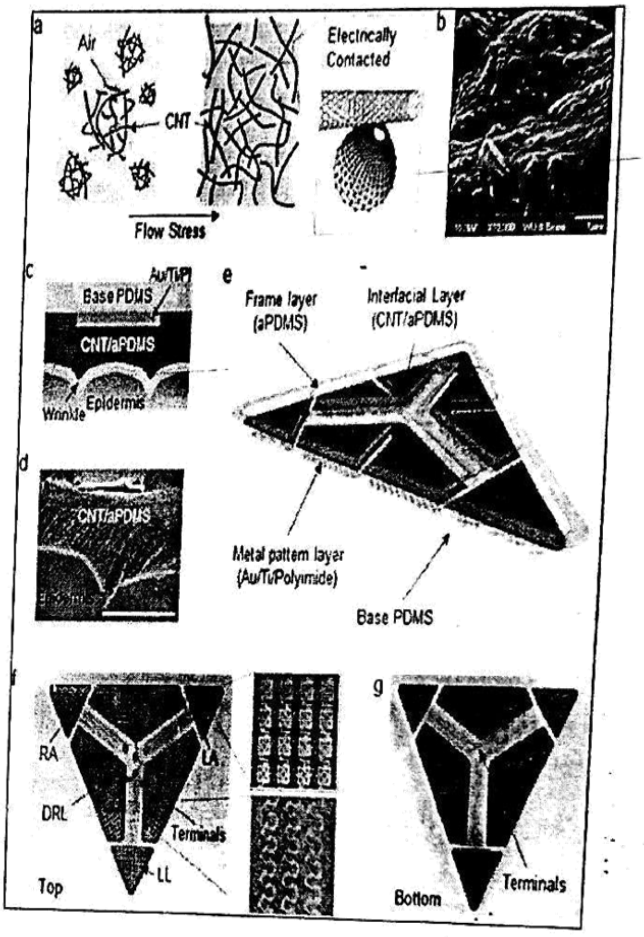

Fig.1: ECG electrode based on CNT/aPDMS.

(a) The aggregated CNTs are mixed with aPDMS by using flow stress. (b) SEM image of CNT/aPDMS after removal of some aPDMS with THF solution. (c) Conformal contact of CNT/aPDMS with wrinkles and rough skin (d) SEM image of a CNT/aPDMS electrode attached to a PDMS skin replica. (e) Structure of an ECG electrode composed of a PDMS base, a metal-patterned layer (Au/Ti/PI), a frame layer (aPDMS), and a CNT/aPDMS interfacial layer. (f) Upper surface of the ECG electrode and serpentine lines. (g) Bottom surface of the ECG electrode, which is the surface attached to the chest (Reproduced from [30])

Due to high conductivity property of CNTs, they are used to fabricate the conductive interfacing layer, through their complete dispersion in aPDMS with a mechanism known as

wetting and flow stress process (Fig. 1a). This turns the CNT/ aPDMS into highly conductive layer as the dissolved CNTs are in electrical contact with one another. The well-dispersed CNTs in CNT/ aPDMS were observed by scanning electron microscopy (SEM) and the image is shown (Fig. 1b). Then a polymide (PI) electrode which is metal- patterned is concealed with CNT/aPDMS layer and hence, electrode was fabricated which is based on epidermal CNT type. The CNT/ aPDMS layer has superior qualities like softness and adhesiveness, it is for this reason that it penetrates into the skin and shows very positive results on even wrinkled skin, and manages robust contact (Fig. 1c). The end shape of the electrode is that of an equilateral triangle. The placement of these three ECG lead-electrodes (ELEs) laminated with CNT/ aPDMS is completed at each corner of left arm (LA), right arm (RA), and left leg (LL), which is same as the conventional gel type ECG electrode measurement method. The CNT/aPDMS layer is conductive, self-adhesive, has low Young's modulus, thin and managed attractive conformal contact disregarding the skin surface (Fig. 1d) [30]. Also similar to conventional gel, CNT/aPDMS can drill into the valleys of the skin, which outcome in enlarging the contact area and lowers the contact impedance significantly and also its impedance is powerful with respect to stretching, bending and twisting; so it can smoothly fit to body motion like sitting, running and so without any modification in its impedance. And also its adhesion force was incredibly boosted up as compared to other conformal electrodes, which depend on van der Waals force alone or other adhesives like silicone membranes or silicon tapes, which results in a completely waterproof electrode, and this make recording of the bio signals much easier in the day to day life [30]. By spin coating speed and the flow property of the fluid, the thickness of the fluid was controlled which further affects the electrical property of the film. Based on these experiments, it was found that CNT/aPDMS ECG electrodes require less than 1.5wt% CNT for the desired achievement. And the signal quality was as good as the commercial conventional ECG electrodes. On increasing the percentage of CNTs in the ECG electrode, the value of electrical conductance was found to increase but it further resulted in deterioration of the mechanical properties. [31].

In one more study [32], as reported by G. Ruffini et al, a different approach was adopted whereby a CNT array was grown on top surface of electrode and because of this, the CNT array architecture was selected to penetrate only the outer layer of the stratum corneum (SC). The outer layer of the epidermis, which is known as SC has a thickness of 10 to 20 μm. Electrolytic gels and skin scrubbing are obligatory in electrophysiology as the SC works as an ideal fluid barrier. The SC must be bypassed, removed, detached or its electrical properties must be changed, to get a good contact between the electrolytic tissue and the electrode. Penetration of only the outer parts of the SC is achieved using the CNT array architecture [32]. To overcome the measured noise in the conventional electrode, a SC gel based electrode was used. In this SC based electrode technique, the conductive layer below the SC was reached by bypassing the SC layer at nanoscales without any pain to the patient, and the outcome of this technique was the painless approach for recording of bio signals, with minimum value of measured noise; and the quality of the recorded signals was maintained without the use of any gel [33]. The head of the SC based electrode was covered with a wide range of multi-walled carbon nanotubes at nanoscales and then was painted with Ag/ AgCl. Ionic-electronic transduction was contributed by painting this with Ag/AgCl. In the SC based electrode, the width of the CNT is very small and the structure is chosen to be brush like structure, so that it can smoothly penetrate the outer layer of the skin This results in advantages such as the contact surface area increases, electrical conductance is improved, a low noise electrical interface is induced; which is stable, pain free penetration, quite comfortable to the wearer, and the diameter is small so the probability of any infection is also reduced to a greater extent. And the signal quality is maintained in the whole process of the CNT array and the measured noise is also low as compared to the conventional ECG electrode process. [32], [33]. The first human trials of the prototype were also reported and the results thus obtained were better as compared to the conventional Ag/AgCl wet electrode. Also, the subject did not report any ill effects such as pain, irritation, burning sensation, redness etc. while and even after six months after using the CNT coated electrode [34]. Thus, we can conclude that the CNT array has several advantages over the conventional electrode and dry electrode to skin interface is easily possible using this CNT array. But for use in practical applications, a wireless transmission module must be used side by side with the flexible dry electrode, which provides a total solution for the practical usage also along with the great advantage of the low noise circuit [35].

In another research work done on CNT based ECG electrodes, screen printing process was used. By using the screen printing process, dry ECG electrode was fabricated, in which the silver (Ag) ink was accumulated on polyethylene terephthalate (PET) substrate, which is highly flexible. Then a multi-walled carbon nanotube (MWCNT)/ PDMS composite was made and then was further bar coated on the screen printed electrode. An observation was made which says larger the area of dry electrodes, larger the peak to peak amplitude of the ECG bio signals. So, for the better performance in measurement of ECG signal, the dry electrode area must be chosen comparatively larger [36], [37]. The major advantage of employing this screen printing technique was that cost was reduced to a great extent because the manufacturing temperature as well as the material wastage during the process of fabrication was quite low and the substrate was highly flexible, which is quite useful in measurement of ECG signal, but it has a disadvantage that the skin-electrode contact impedance is high [38], [39]. In one more study, as reported by H. L. Peng et al [40], the flexible dry electrode based on CNT, with micro pillar array, was designed and the fabrication was done by MEMS process. And, the advantages of this electrode were that the skin-electrode contact impedance was reduced when used with micro pillar array structure [40]. C. L. Lam et al [41] reported a different approach, whereby using

MWCNTs, a textile based electrode for measurement of ECG signals, was developed. The advantage of this type of electrode was that it in terms of comfortability level, this electrode came out as the best candidate. In this scheme, for the substrate material, cotton fabric was used and for the conductive material, MWNTs were used. The structure of the electrode thus fabricated is shown in Fig. 2. The performance of this MWCNT/Cotton based flexible electrode was found to be better than conventional electrode (Ag/AgCl) [41].

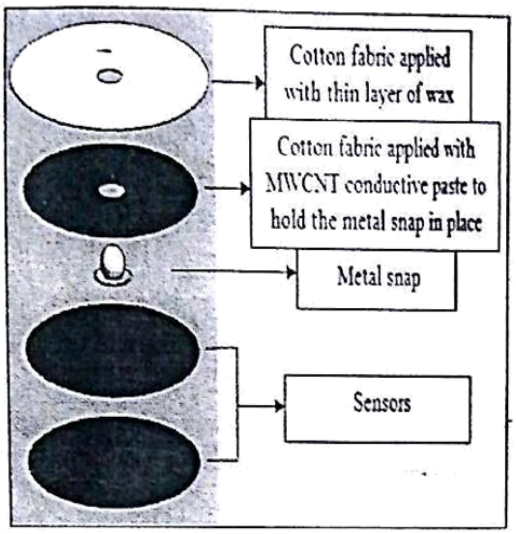

Fig 2: Configuration of the electrode [reproduced from 41]

Another electrode was developed, in which PDMS and conductive additives of CNTs were used for the fabrication of composite electrodes for ECG. A three-step dispersion process consisting of ultra-sonication, stirring, and in situ polymerization was advanced to turn out homogenous CNTs-PDMS mixtures. The CNTs PDMS mixtures were used to fabricate CNTs-PDMS composite electrodes by the replica technique. This approach is cost effective when the production is done in larger quantity. Also it is comfortable to the wearer. As compared to commercial Ag/AgCl electrodes, CNT content of 5 wt. % was comparable. And the fabrication process was also simpler [42].

VI. CONCLUSION & FUTURE SCOPE

A lot of research work has been done in the area of MWNT based electrodes for ECG signals. MWNT based electrodes are dry electrodes and hence they overcome the disadvantages associated with conventional wet electrodes (Ag/ AgCl), such as degradation of the signal quality due to drying of the gel over time, irritation and allergic reactions to skin, non-suitability for long-term monitoring of signals, etc. MWNT based electrodes have the added advantages of low electrode-to-skin impedance, flexibility, excellent bio- compatibility and very low levels of motion artifacts— something which is not observed in other dry electrodes. Hence, MWNT based ECG electrodes have emerged as the front runner amongst the various electrodes available for long-term and continuous recording of ECG signals. Long term and continuous recording of ECG signals is critical to the early diagnosis of cardiovascular diseases and subsequent prevention of deaths due to them. Also, these electrodes are a big leap in the direction of wearable electronics— the technology of today.

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Analytical Study Of High Performance Flip-flop Circuits Based On Performance Measurements

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Abstract— **In designing synchronous circuits and memory elements, Flip-flops (FF) play an integral role. In the present era, the demand of area efficient, lesser delay, and faster devices are the major concern. This paper present the comparative study of Flip Flops in terms of area and delay. The problem of device size is very dominant today because the demand for small device size along with lesser number of transistors is increasing. And also for implementing a circuit, comparatively less number of transistors are preferred in comparison to conventionally used number of transistors, as it results in lesser number of switching activities. And smaller delay is preferred as it results in faster device along with faster response time of device. Hence, in this paper, the comparative study of various flip flops using The Clocked CMOS (C^2MOS) register, True Single-Phase Clocked Register (TSPCR), Self-Gating Flip Flop, Static Flip Flop is done. The reduction in the delay is done by properly changing the size of transistor and alteration in the value of voltage. The circuits are simulated and correlated using 45nm technology.**

Keywords—Flip-flops, circuit optimization, delay, transistors

I. INTRODUCTION

Nowadays, as the demand of high speed computation devices is growing continuously, there is an urgency for designing such circuits which are power efficient along with faster response time [1] and have smaller delay and lesser area requirement.

Among the most commonly used sequential type of logic circuits, flip- flops plays a very important role as a memory element. In flip-flops, the output not only rely totally on the present inputs but also depends on the past inputs. In response to a rising edge of the clock signal in the positive edge triggered registers, a flip flop stores the logical state of the input data or signal [2] and works as a memory element. On the contrary, in negative edge triggered flip- flop the whole process of storing the logic state of the input by the flip- flop is done at the falling edge of the clock signal.

As there is tremendous demand for designing such devices which can operate at high speed and have less delay, so in this paper, a comparative study of D flip flop using four techniques is done. On the basis of the result, the technique with the minimum delay will be useful in implementing faster Phase Frequency Detector (PFD) circuits [3], in various portable applications used in day to day life where lesser delay is required [4], in the applications which requires shift registers [5], microprocessors, buffers, etc. [6].

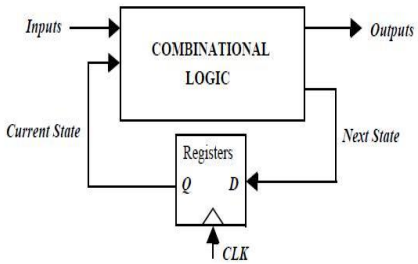

Fig 1: Block diagram of a sequential circuit block using positive edge-triggered registers [18]

The block in figure 1 shows the finite state machine implemented using sequential circuit block, that includes Combinational Logic, Register, Inputs and outputs. Basically, registers can be sub divided into two flavors: Positive Edge Triggered Register and Negative Edge Triggered Register. When the input data or input signal is duplicated on the positive edge of the clock signal, then the register is known as positive edge triggered. And when the input signal or input data is duplicated on the negative edge of the clock signal, then it is known as negative edge triggered register, and it is denoted by small circle at the clock input.

The current state along with the current inputs are used to resolve the next state, which is then deliver to the register inputs. The output of the finite state machine implemented through sequential circuit block totally depends on current inputs and current states. As the block shown in figure 1 has a positive edge triggered registers, so after some propagation delay, the next state bit is copied to the output of the register on the rising edge of the clock, which subsequently results in initialization of new cycle. And as the register is positive edge triggered; so, until the next rising edge, the register will hold the previous value and doesn't allow any change in the signal.

II. FLIP-FLOPS

Flip-flops are basically a sequential circuit logic, which are used as a sub module of data part architecture and is used for the compilation of data prepared by the combinational circuits and also for proper synchronization operation of level signal flip-flops are used [7]. In terms of the speed, delay and the response time of the circuit, the further improvement can be

made by changing and varying the voltage and by significantly increasing the size of the transistor [2].

Basically, there are two criteria through which delay can be determined: First is the delay between data and the output and the second is the delay between the clock signal and the output.

The transistor sizing between master stage and slave stage is used in high speed computational design as sizing increases the speed of flip flop [7] and speed further increases the response time of the flip-flop. When the differently type of inputs are used; the low-power, high-speed flip-flops have been described and reported [8-10].

And by the proper alteration in the voltage range and sizing in the transistors, the delay can be further cut down [2].

III. TIMING BEHAVIOUR

Timing behavior of FF can be further subdivided into two main categories:

I. Data to clock
II. Clock to output [2].

The setup time is defined as the minimum time between a data change and the trigger of the clock for which the data signal should be held steady before the clock pulse; if the clock pulse is high, the output will surely change and become equal to the new value [13].

Hold Time is that minimal amount of time that the data signal must be held consistent after the triggering edge of the clock signal [13].

If setup time be T_{setup} for a flip-flop, and if the data is not stable before this T_{setup} time from the active edge of clock pulse then it results in setup violation. And if the hold time be T_{hold} for a flip-flop; and if the data is not kept stable after the T_{hold} time, then it results in hold time violation.

In section IV, the simulation and analysis of flips flops using different techniques is done. And the paper is concluded in section V. The comparison of results is done using 45 nm technology, for the simulation of flip flops using various techniques.

IV SIMULATION AND ANALYSIS

1. Static D Flip Flops

The D flip-flops are commonly classified into two types:

I. Static D flip-flops
II. Dynamic D flip-flops [14]

The main distinction between dynamic and static DFFs is that the Dynamic DFFs have a decreased setup time than static DFFs. And the dynamic DFFs are faster and has better speed along with better response time. The signal value is stored as a charge on parasitic capacitor in Dynamic DFFs. And as the value charge on capacitors reduce in value with time, dynamic DFFs can only be used when the module has a constantly running system clock. On the other hand, for the implementation of the memory function, the positive feedback is used in static D flip-flops and it is for this reason, it can store value endlessly without the regular refreshing. That is the circuit does not require continuous refreshing. It is for this reason, the static D flip-flop proves to be better candidate among the two, as in low power application this property is very useful, where circuit is partially or sometimes fully idled [15]

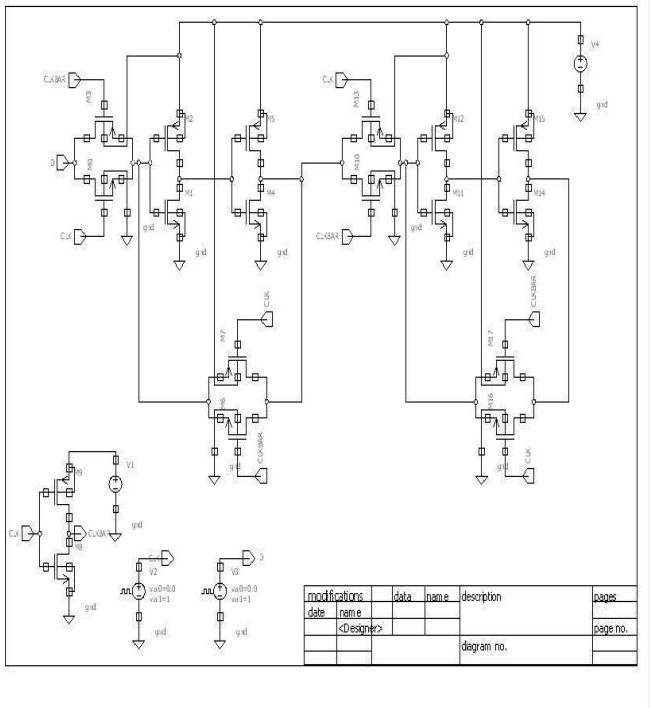

Fig 2: Schematic Diagram of Static D Flip Flop [14]

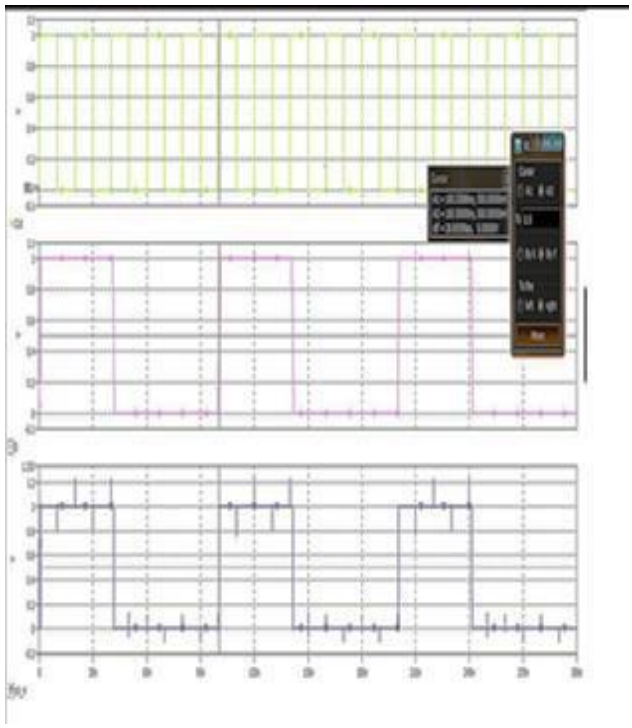

Fig 3: Output Waveform of Static D Flip Flop

2. C^2MOS Register

In C^2MOS based D flip- flops, the clock gating transistors are used in place of transmission gates[2] and the value of delay can be varied by varying the value of rise time and fall time; that is the delay depend on the rise time and the fall time.

The working of the C^2MOS Register module is basically done in two phases:

1. When Clock Bar = 0 (Clock signal = 1): In this phase, master stage evaluates the data and thus in Evaluation mode and the slave stage holds the data and it for this reason it is said to be in high impedance or we can say hold mode. The first tristate driver is on, and the master stage operates as an inverter which provide the inverted D signal on the internal node X (after the master stage). So, in this phase, the output maintains its past value saved on the output capacitor [18].

2. The second phase is when Clock Bar= 1 (Clock signal = 0). In this phase, the master stage is in high impedance or hold mode and the phase stage is in evaluation mode. In this phase, the slave stage acts as an inverter and the value stored on Capacitor node propagates to the output node through the slave stage [18].

In C^2MOS register, when the master stage is ON or in conduction phase, the slave stage is OFF or in non- conducting phase. And when slave stage is ON, the master stage is in OFF state.

A C^2MOS register with *CLK-CLK* clocking is unresponsive to overlap, as long as the rise and fall times of the clock edges are adequately small [2].

In summary, it can be stated that the C^2MOS latch is unresponsive to clock overlaps because those overlaps never activate both the pull-up and the pull-down networks of the latches together. When the pull up network is in ON state, pull down network is in OFF state and vice versa.

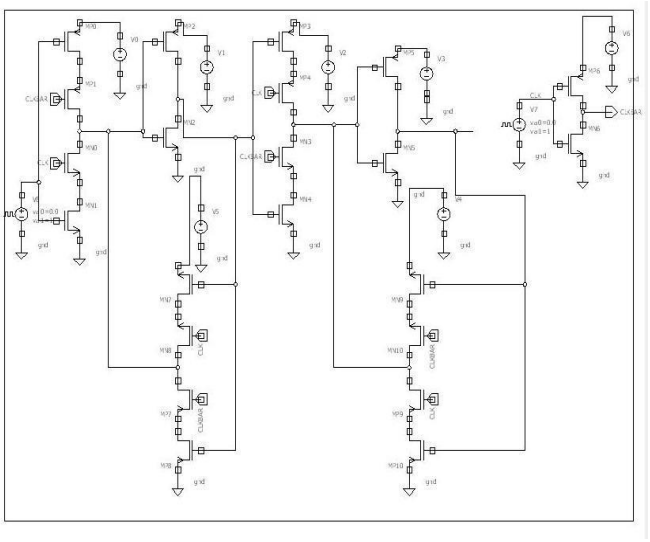

Fig 4: Schematic diagram of C^2MOS [2]

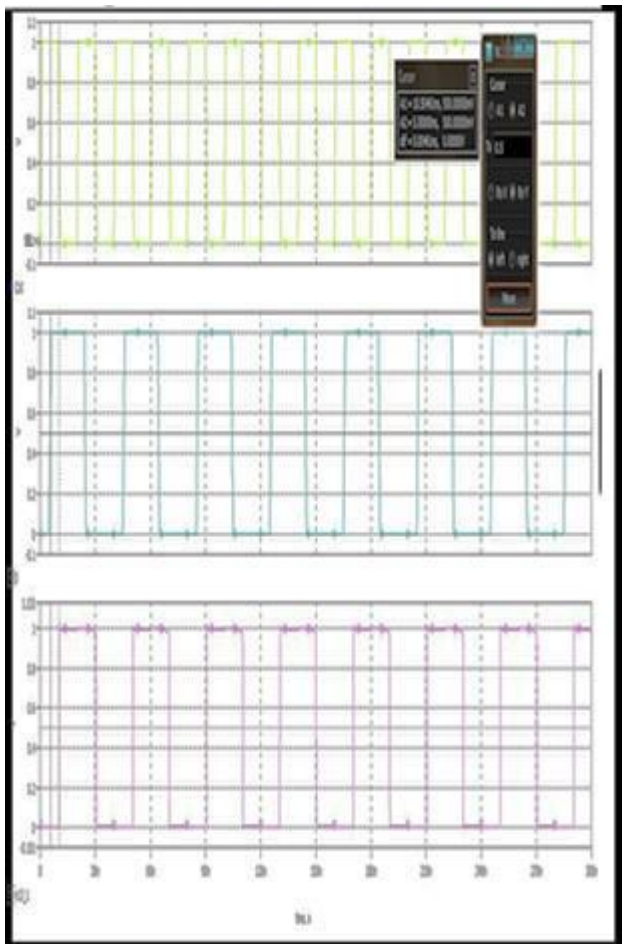

Fig 5: Output waveform of C^2MOS

3. Self-gated D Flip-Flop

The main concept behind the self-gating flip flops is identical as that of the clock gating technique. The clock signal's switching activity can be abolished, if the input of the flip-flop is totally same as that to its output, and in this way, the power can be conserved to a much greater extent. But the circuit acquires larger area in terms of number of transistors as it requires comparative large number of transistors which in turn results in slight degradation of the delay because of a longer way from Clock to Q output.

The total power that is dissipated is calculated on the relative transition frequencies of the data input T_{DI} and clock signal T_{clock}. When $T_{DI} / T_{clock} \ll 1$, the internal clock signals can be disabled again and again, as there are less transition frequencies between the data input and the clock and in this way the self-gating flip-flop consumes lesser power than the regular flip-flop. On the contrary, when the ratio outpaces a certain amount less than 1.0, the self-gating flip-flop will consume more power [18].

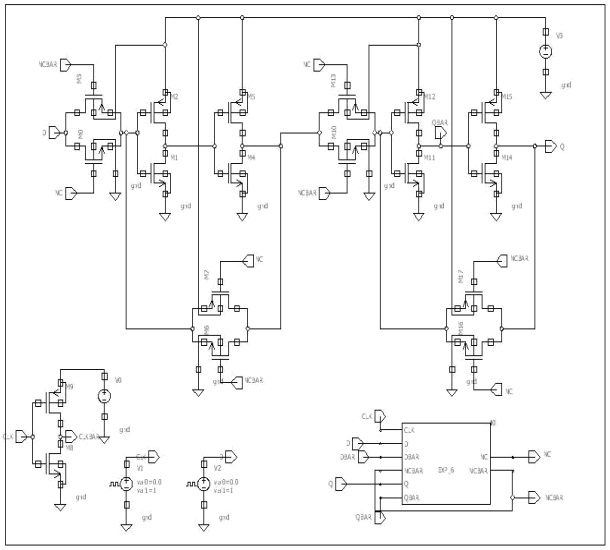

Fig 6: Schematic Diagram of Self Gated D Flip Flops [14]

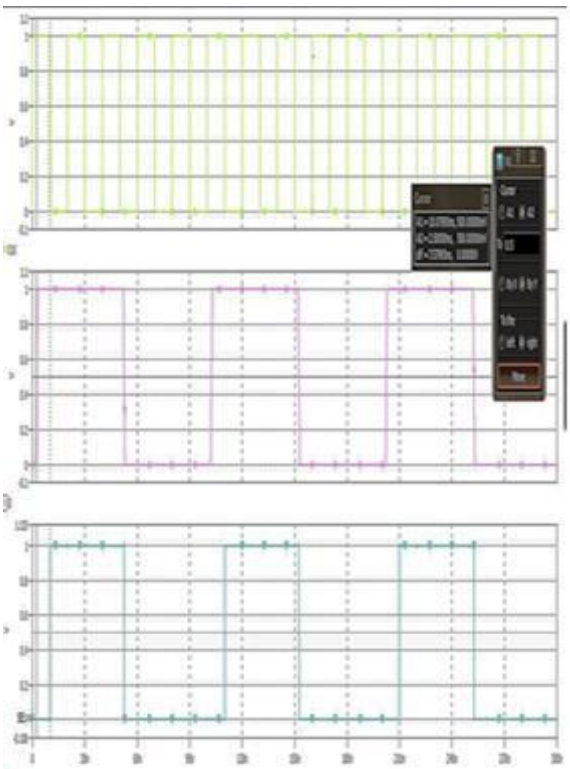

Fig 7: Output waveform of Self Gated D Flip-Flop

4. TSPC

The TSPC based dynamic logic technique was popularized by [19] so that the complexity which arise due to multiple clock cycles can be easily conquered and properly eliminated. Multiple clock cycles in the circuit results in higher power dissipation and more delay in the circuit which further reduces the response time and makes the circuit slower. So, to overcome this disadvantage, TSPCL is used, as it uses a single clock cycle.

TSPCL technique includes positive and negative edge triggered D flip flop [20].

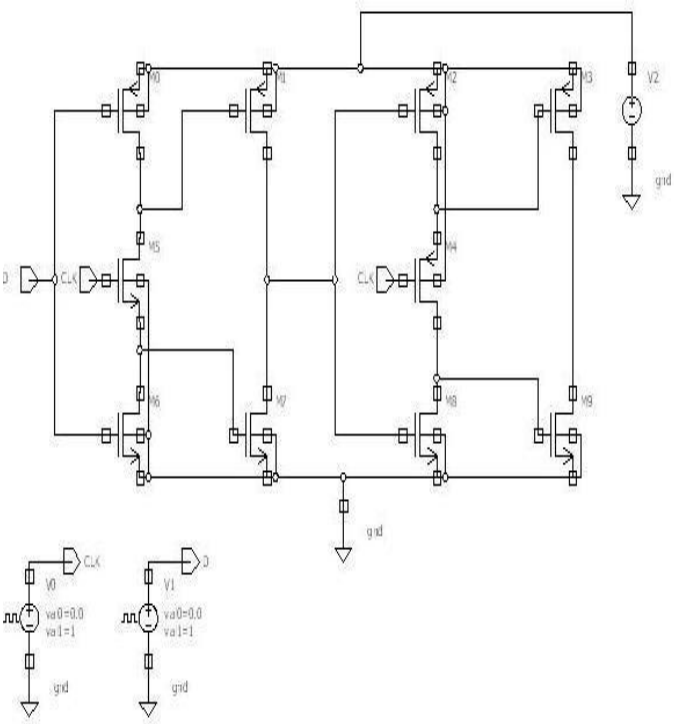

Fig 8: Schematic Diagram of TSPCL[22]

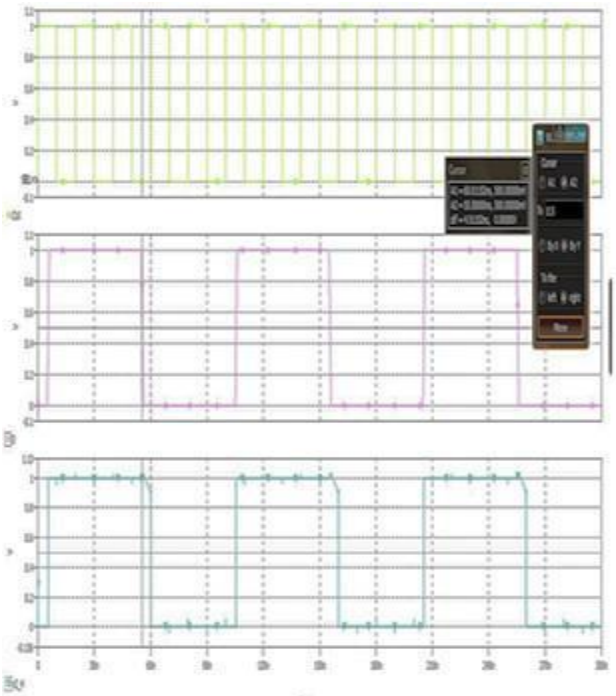

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Fig 9: Output waveform of TSPCL

TABLE I. DELAY CALCULATION (USING 45 NANO METER TECHNOLOGY)

Circuit Technology	Delay(ns)
Static D Flip Flop	28.855
Self-Gated Flip Flop	7.58
C^2MOS	5.00
TSPC	4.51

TABLE II. TRANSISTORS COUNT (WITH ALMOST SAME ASPECT RATIO) (USING 45 NANO METER TECHNOLOGY)

CIRCUIT TECHNOLOGY	NUMBER OF TRANSISTORS
Static D Flip Flop	16
Self-Gated Flip Flop	16
C^2MOS	20
TSPC	10

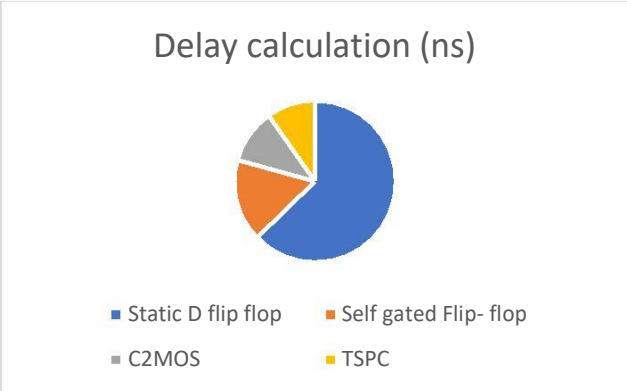

Fig 10 : Comparison based on delay calculation by four different techniques using 45 nm technology.

Along with the advantages of less hardware and low power, TSPC logic also manages design having lower phase noise margin. Along with less transistors and faster device capability, TSPC techniques point to low phase noise in the module and can be efficiently used in various applications such as in frequency divider, phase/ frequency detector (PFD) circuits, etc. [23]. In terms of faster devices, TSPC stands better than the SVL Technique as the delay calculation of D flip flop using SVL technique is 112.86 ns while in case of TSPC, it is 4.51 ns [*24*]. The delay of the C2MOS technique is comparably equal when comparing the result with C2MOS designed in paper entitled design of high performance power efficient flip flops using transmission gates [2]. Therefore, TSPC is the best candidate among the four techniques used, as it offers faster device with minimum delay in the circuit.

V. CONCLUSION

In this paper, the comparative study of performance measurements of various flip-flops is done using four different techniques and the result is compared. As in today's era, there is requirement of faster switching along with smaller devices, so the implementation of D flip flop is most effectively done by TSPC technique as it offers smaller delay along with lesser number of transistors. As the transistors used in all techniques have almost same aspect ratio, so we can say that devices with lesser number of transistors are more area efficient devices. Smaller delay results in faster devices with faster response time. So, TSPC is the best candidate for area efficient and faster circuits among these four techniques because as the delay increases the speed of device decreases and as the area overhead increases, it results in bigger circuit size.

ACKNOWLEDGMENT

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Appendix III:
Accepted Paper

Analysis of Power Efficient 6-T SRAM Cell with Performance Measurements

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Abstract— Among all the semiconductor memory modules available today, SRAM is considered to be the most critical and highly demanding semiconductor memory in the gamut of microelectronics applications as it does not require the need of regular refreshing. As the technology is continuously scaling down, it results in reduction of feature size along with the miniaturization at chip level. But along with this, the need of low power devices has also increased. But the genuine dilemma, especially for SRAM, is the leakage power. To solve leakage power problems, a large number of power reduction techniques are used. There are various advantages of using low power devices for example, the use of low power makes the device more portable with easy handling, improved battery life along with great improvement in the performance parameters. In processing as well as in memories and in data handling applications, devices with low power dissipation are in great demand. In this paper, the comparative study of various leakage power reduction techniques like Schmitt trigger, forced stack technique and LECTOR technique with SRAM architecture has been done. Simulation and analysis results show that the SRAM cell using forced stack technique attains lowest static power dissipation and total power dissipation along with all the advantages of the existing SRAM Cell. The simulation is done on the Symica DE and LT spice with 45 nm PTM technology.

Keywords— **SRAM, Leakage Power, Forced Stack Technique, LECTOR Technique, Schmitt Trigger.**

I. INTRODUCTION

Power consumption is among one of the dominant burden of VLSI circuit design, and for the designing of VLSI circuits, CMOS is the fundamental technology used. All battery-operated mobile devices desire primary memory that acknowledges fast. So for that we need SRAM's which don't require regular refreshment along with faster speed of operation. It is for this reason, SRAM's occupy most of the area and influence the performance and power of a device [1].

The leakage power dissipation contributes a lot in the total power dissipation of the circuit. The leakage power is continuously increasing which further adversely affects the operating frequency and the power consumption of the SRAMs circuit [2]- [5]. The threshold voltage is inversely proportional to the leakage power because the leakage current increments exponentially as the amount of threshold voltage reduces [6]-[8].

Therefore, to minimize the overall power dissipation, the supply voltage has to be reduced further since the threshold voltage and the transistor has to be scaled to obtain great performance [9]. Most of the time, large portion of the chip area is occupied by SRAM and; SRAM also influences the performance of the system. Simultaneously, the astounding advancement in the prominent area of mobile devices and other developing applications, such as implanted medical equipment and wireless body sensing networks, and wireless sensors, constrains the demand for low-power SRAMs [10]. Therefore, implementation of a low-power SRAM circuit design has drawn booming research attention [11-13]. Mobile applications also require SRAM memories, like in smartphones or mobile phones streaming HD videos and pictures or virtual-reality headsets rendering 3D landscapes and images or motion video; that when used in low power state can result in extended battery life [14] along with the proper functioning of the circuit and high-performance results
[15]. Therefore, SRAM circuit which has lower leakage current with lower power dissipation and faster devices, is a good candidate for today's applications. For the low power devices, various low power techniques are used like forced stack technique, sleepy stack technique, sleep transistor logic, LECTOR technique, etc. [16- 17]. This paper includes the following sections: Section II presents the conventional 6T SRAM cell, Section III presents the simulation, Section IV presents the analysis results; finally, Section V concludes the paper.

II. CONVENTIONAL 6T SRAM CELL

The conventional 6T SRAM cell is shown in Fig. 1. It comprises of two inverters (M1-M4) combined to one another in the cross coupled pattern. M5 and M6 are access transistors. M5 and M6 are known as access transistors because whenever their gates are triggered by the duration of read and write operation signal WL, nodes Q and QB are connected to BL and BLB respectively [18].

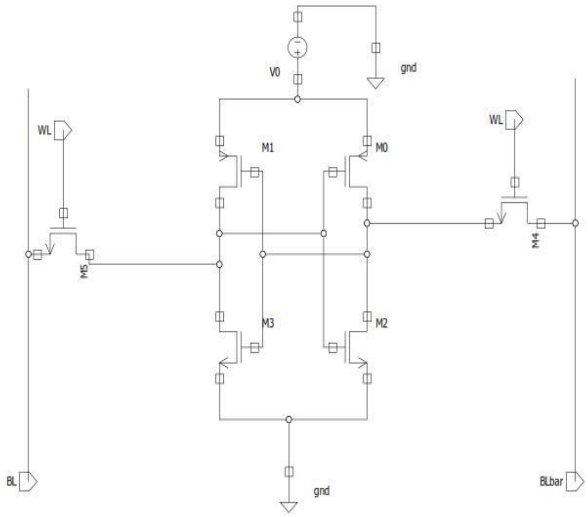

Fig 1: Conventional 6T SRAM Cell [18]

III. SIMULATION

As the need of small size, mobile devices with lower power dissipation is increasing, there comes the necessity to make the devices which have lower power dissipation, like using Schmitt trigger, forced stack technique, LECTOR technique, etc. [16], [18], [19]. In this paper, the performance comparison of SRAM is done with the CMOS, Schmitt Trigger, LECTOR Technique and forced stack technique. The inverter in the SRAM cell is replaced by the inverter implementation by forced stack and LECTOR technique, which further reduces the power dissipation up to a great extent. For the implementation of let's say 34k× 8 SRAM, there are numerous smaller SRAM cells required. So, reducing the power of these smaller SRAM cells can further result in great improvement in the bigger circuits. Also, the delay is also comparably same, as the inverters are in latch. Nowadays, static power dissipation is one of the major concerns and with the help of forced stack and LECTOR technique, static power dissipation is reduced to a great extent. On the other hand, the Schmitt Trigger helps in lowering the dynamic power dissipation.

The circuit implementation of 6 T SRAM using CMOS, Schmitt trigger, LECTOR technique and forced stack technique is shown in Fig 2, Fig 3, Fig 4, Fig 5 respectively.

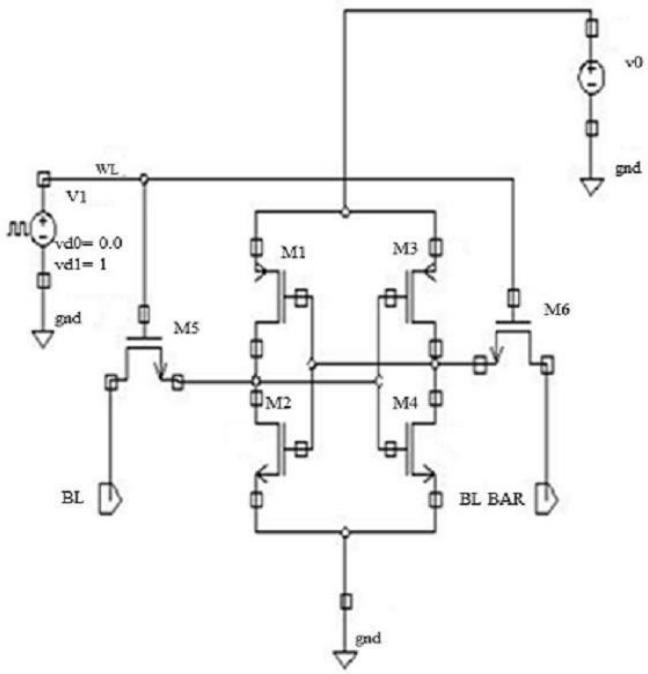

Fig 2 : 6T SRAM using simple CMOS circuit.

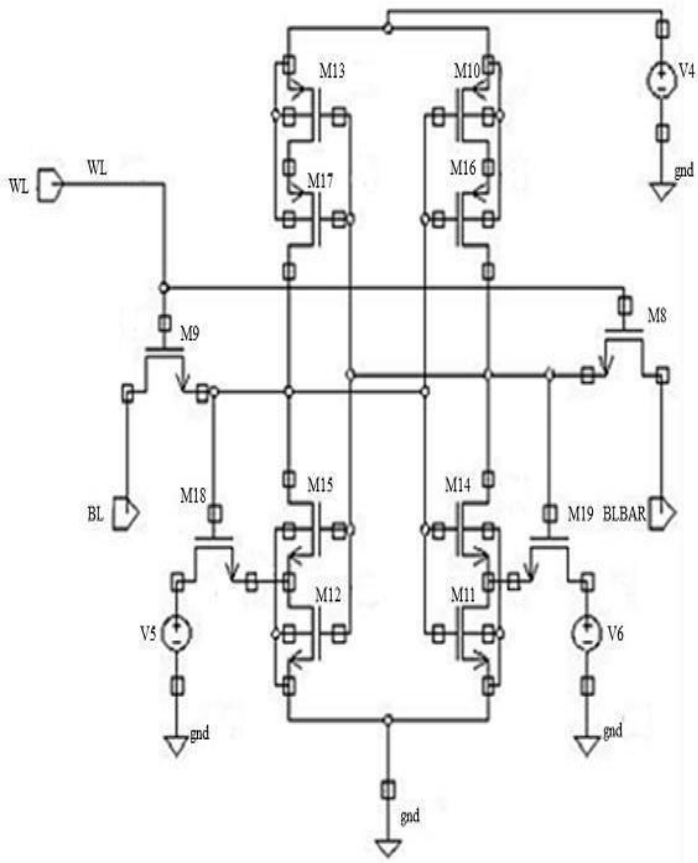

Fig 3: 6T SRAM using Schmitt Trigger

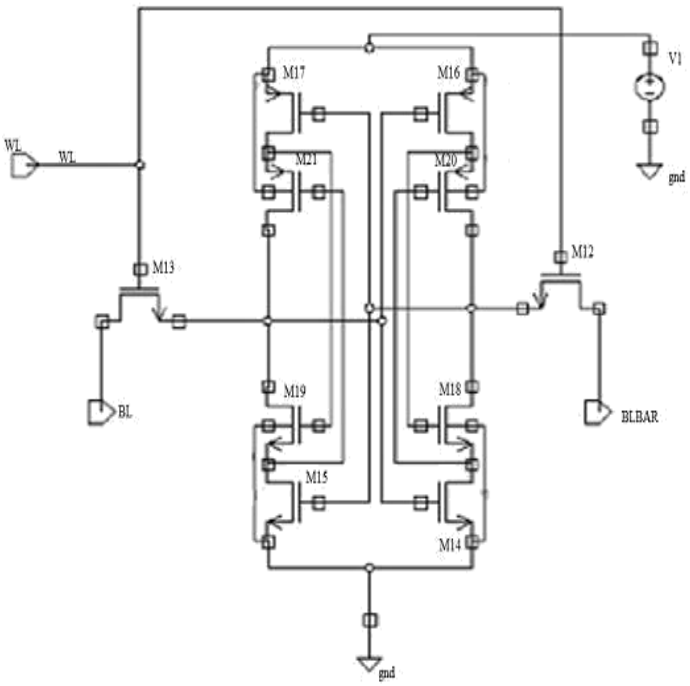

Fig 4: 6T SRAM using LECTOR technique

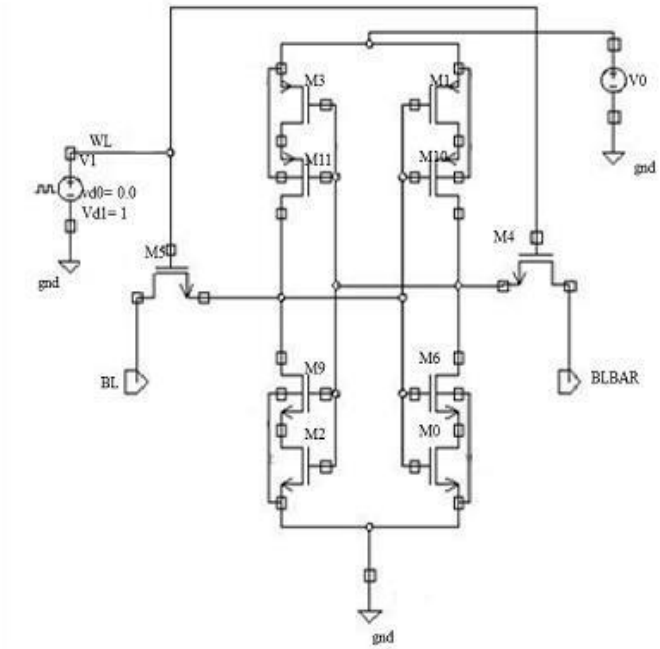

Fig 5: 6T SRAM using Forced Stack Technique

IV. ANALYSIS

The 6T SRAM cell shown in Fig 2, Fig 3, Fig 4 and Fig 5 has been implemented using LT SPICE and SYMICA DE software and simulated using 45nm Predictive Technology Model (PTM). Table 1 shows total power dissipation and static power dissipation and Table 2 shows the overall delay. A comprehensive comparison of SRAM cells with simple CMOS, forced stack technique, LECTOR Technique and Schmitt-trigger-based SRAM cell is shown in Fig 6(a), Fig 6(b) and Fig 6(c).

TABLE I. POWER DISSIPATION OF 6T SRAM CELL USING VARIOUS TECHNIQUES

TECHNIQUE	POWER DISSIPATION	
	Static (nW)	Total (nW)
Simple CMOS	420.72	1521.1
Schmitt Trigger	326.05	796.14
Forced stack	268.09	889.47
LECTOR	359.57	993.05

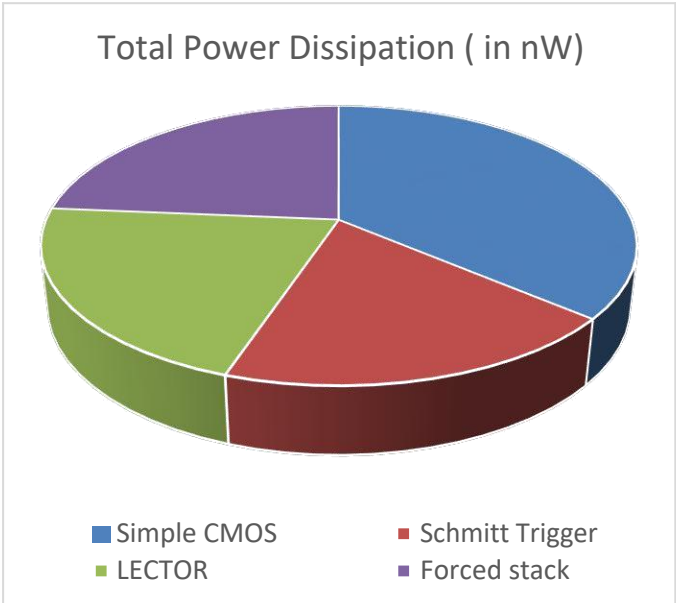

Fig 6(a): Comparison of 6T SRAM using various techniques, for total power dissipation

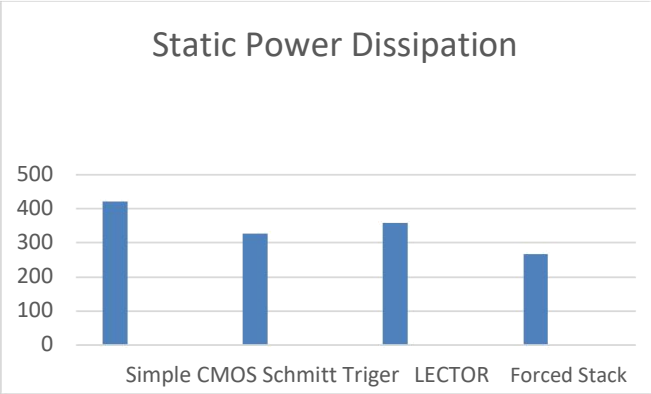

Fig 6(b): Comparison of 6T SRAM using various techniques, for static power dissipation.

TABLE II. DELAY CALCULATION OF 6T SRAM CELL USING VARIOUS TECHNIQUES

TECHNIQUE	DELAY (n sec)
Simple CMOS	0.1088
Schmitt Trigger	0.15
Forced stack	0.54
LECTOR	0.670

V. CONCLUSION

By virtue of broad progress in technology scaling, the low power and faster on chip memory is the best candid. This can be easily achieved through SRAM, as SRAM works as a cache memory element. As the technology is scaling continuously, so need for those devices with low static power dissipation is the major concern. An efficient low power SRAM cell is shown in this paper, which reduces the power dissipation to a great extent and thereby can be used in various low power devices. The static power dissipation is highly reduced without affecting the other parameters to a great extent. The low power devices so formed can be used in various portable electronic devices like mobile devices and other low power devices where power dissipation is the main concern. The results show that the static power dissipation is minimum in case of 6T SRAM using forced stack technique, without affecting the other parameters such as delay to a great extent. The comparison of 6T SRAM using simple CMOS, Schmitt Trigger, LECTOR, forced stack technique is shown in Fig 7 with respect to parameters like Total Power dissipation, Static Power Dissipation and the overall delay of the circuit. The comparison shows that the static power dissipation is reduced by 36.2% when the forced stack technique is used in the SRAM cell as compared to the SRAM implementation through simple CMOS circuit. Thus, we can say that for implementation of low power SRAM, forced stack technique is the good candidate as the major static power is reduced to a greater extent in this technique.

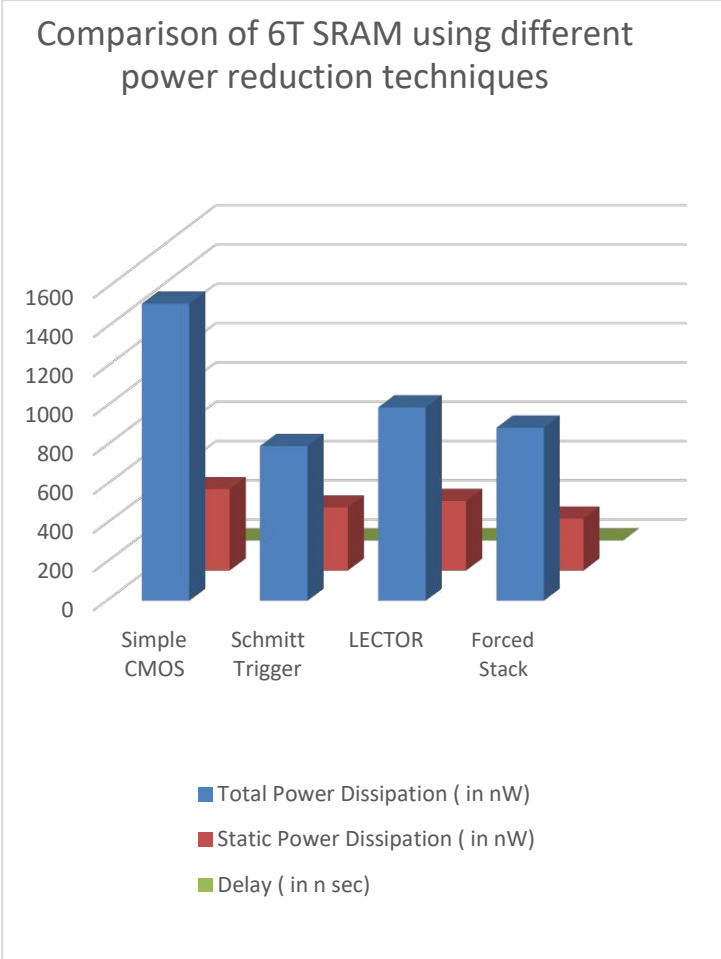

Fig 7: Comaprison of various performance parameters of 6T SRAM using different power reduction techniques.

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