Design and Analysis of LNA for 2.4 GHz ISM Band using 0.13 µm CMOS Technology

Submitted in partial fulfillment of the requirements for the award of the degree of
Master of Technology
In
Microwave and Optical Communication Engineering (MOCE)

by
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Certificate

This is to certify that the work done in the thesis entitled '**Design and Analysis of LNA for 2.4 GHz ISM Band using 0.13 µm CMOS technology**' has been carried out by Ms. Aditi, under my supervision in partial fulfillment of the requirements for the award of the degree of Master of Technology (M.Tech) in Microwave and Optical Communication Engineering (MOCE) at Delhi Technological University, Delhi.

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Candidate's Declaration

The work in the thesis entitled '**Design and Analysis of LNA for 2.4 GHz ISM Band using 0.13 µm CMOS technology**' is a record of original research work carried out by me under the guidance of Dr. Malti Bansal, Assistant Professor, Department of Electronics and Communication, Delhi Technological University, in partial fulfillment of the requirement for the award of the degree of Master of Technology in Microwave and Optical Communication Engineering (MOCE), at Delhi Technological University, Delhi. Neither this thesis nor any part of it has been submitted for the award of any other degree or diploma elsewhere.

Date:

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I would also like to acknowledge people with whom I made this gracious journey of two years: my college colleagues who contributed to the ideas, provided intellectual boost and energy.

Last but not the least, my parent's constant trust and faith on my abilities was like a giant shadow that sheltered me to complete this project successfully. This has been one of the greatest experiences of my life.

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Abstract

Due to rapid developments in communication industry, the requirement of more and different kinds of wireless communication systems has increased. It is desired that these wireless communication systems have characteristics such as low noise figure, low input/output return losses, a high IIP3 and, low power consumption. The main aim of the manufacturers of the wireless communication systems is to achieve low power. In these wireless communication systems, the RF front-end circuit is LNA which is one of the crucial elements of RF receivers. They amplify RF signal to a particular level so that the sensitivity requirements of other components in RF receivers such as filters are met by RF signal as the signal received by the antenna is very small. Hence, it is important to amplify the signal as much as possible without noise addition and also; attaining good linearity, high gain and low power consumption at the same time. For designing of LNA, the most optimum tradeoff between various parameters has to be achieved. Also, the size of communication devices and power consumption should be as minimum as possible, which is possible nowadays because of advancements in integrated circuit (IC) technology. In this thesis, low noise amplifier topologies have been proposed to achieve high linearity while keeping the noise performance as good as possible and gain as high as possible. To achieve input impedance matching of 50 Ω, a pi-matched circuit is used at input. The proposed low noise amplifier topologies are designed for 2.4 GHz frequency. The circuits are implemented using 0.13 µm CMOS technology and is simulated using Advanced Design Simulation Software.

Refereed Publications arising from this Thesis

1. Malti Bansal, Aditi, "Mobile and Real-Time Sensing Electronic Nose based on Carbon Nanotubes," in *Proceedings of 3rd International Conference on Emerging Electronics (ICEE)*, IIT Bombay, 2016, pp. 326-331.
2. Aditi, Malti Bansal, "A High Gain and Moderate Linearity Inductively Degenerated Cascode CMOS LNA for 2.4GHz ISM Band," in *Proceedings of International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS)*, Coimbatore, 2017, vol. 5, no. 71, pp. 382-385.
3. Aditi, Malti Bansal, "A High Linearity and Moderate Gain LNA for Receiver Front-End Applications in 2.4GHz ISM Band," *accepted in International Conference on Innovations in Control and Information Systems (ICICCI)*, 2017.
4. Aditi, Malti Bansal, "A High Gain, High Linearity and Low Noise LNA for IEEE 802.15.4 ZigBee Standard in 2.4 GHz ISM Band," *accepted in International Conference on Innovations in Control, Communication and Information Systems (ICICCI)*, 2017.
5. Aditi, Malti Bansal, "High Linearity and Low Noise Shunt Resistive Feedback CMOS LNA in 2.4GHz ISM Band," *accepted in Recent Developments in Control, Automation and Power Engineering (RDCAPE)*, 2017.
6. Aditi, Malti Bansal, "High Linearity and High Input Impedance Matching Common Gate CMOS LNA in 2.4GHz ISM Band," *accepted in Recent Developments in Control, Automation and Power Engineering (RDCAPE)*, 2017.
7. Aditi, Malti Bansal, "Design, Analysis and Comparison of LNA topologies for IEEE 802.15.4 Zigbee Standard," *accepted in Conference on Information and Communication Technology (CICT), 2017.*
8. Aditi, Malti Bansal, "A High Linearity and Low Noise Shunt Resistive Feedback UWB LNA*," accepted in Conference on Information and Communication Technology (CICT), 2017.*
9. Frequency Dependent LNA Design: A Review *(Communicated).*

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List of Abbreviations

SNR	Signal to noise ration
F	Noise Factor
NF	Noise Figure
IIP3	Input third order intercept point
OIP3	Output third order intercept point
LNA	Low Noise Amplifier
RF	Radio Frequency
CS	Common Source
CG	Common Gate
GSM	Global System for Mobile
GPS	Global Positioning System
LAN	Local Area Network
WLAN	Wireless Local Area Network
IM	Intermodulation Distortion
MIM	Metal Insulator Metal
CMOS	Complementary Metal Oxide Semiconductor
Si	Silicon
GHz	Giga-Hertz
MHz	Mega-Hertz
KHz	Kilo-Hertz
µm	Micrometer

nm	Nanometer
ADS	Advanced Design Simulation Software
EDA	Electronic Design Automation
TSMC	Taiwan Semiconductor Manufacturing Company
Bi-CMOS	Bipolar Complementary Metal-Oxide Semiconductor

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Chapter-1

INTRODUCTION

1.1 Motivation

The electromagnetic spectrum's part that covers high frequencies in GHz range is the radio frequency range. Signals received by and transmitted from the antenna are RF signals. People's demand for wireless applications has become more sophisticated i.e., requiring a small power of radiation, large converging area, and higher speed because of the rapid development of communication technology.

Wireless telecommunication systems are used in reception and transmission of radio waves, which includes Wi-Fi, mobile phones, and two-way radios. Because of the communication industry's rapid developments, the requirement of more and different kinds of wireless communication systems has increased. It is desired that these wireless communication systems have characteristics such as low noise figure, low input/output return losses, a high IIP3 and, low power consumption. The main aim of the manufacturers of the wireless communication systems is to achieve low power. The demand of small radiation power, large converging area, and high speed are fulfilled due to the low-cost, low-rate, and low-power network; IEEE 802.15.4 ZigBee standard.

The license free frequency bands are 2400 MHz, 920 MHz, and 860 MHz, used by IEEE 802.15.4 ZigBee standard. The design in this thesis is mainly concentrated on the 2.4GHz band because of global operation in this band as is used by router, cordless phone, Bluetooth device, baby monitor and etc.

1.2 S-parameter

A two port networks performance can be described in many different ways such as using Y parameters, Z parameters, ABCD parameters and T parameters for low frequency. Linear electrical network behavior is described by these parameters by using open circuit and short circuit conditions. However, at high frequency it is difficult to realize these terminations and hence, cannot be used for high frequency analysis. Therefore, S parameter is used for high frequency analysis i.e. also for RF range.

Load termination measurement and matching is achieved by S-parameter by utilizing incident wave and reflected wave at the input port and the output port. A two port network is shown in figure 1.1.

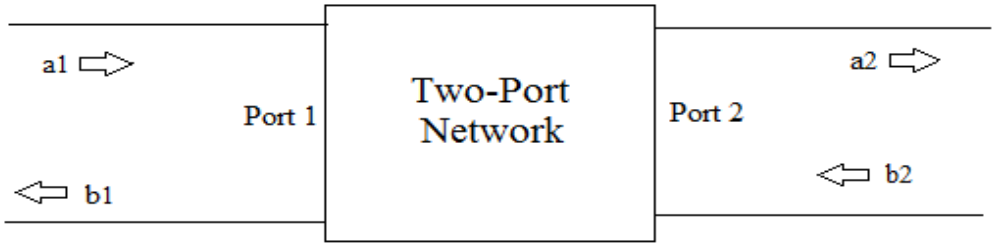

Fig 1.1 Two port network [1]

where,
a1 and a2 are incident wave
b1 and b2 are reflected wave

The relationship between a1, a2, b1 and b2 is described by s parameter as follows:

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a1 \\ a2 \end{bmatrix} = [S] \begin{bmatrix} a1 \\ a2 \end{bmatrix} \quad (1.1)$$

The matrix [S] is called the scattering matrix. Its parameters are as follows:

1.2.1. S_{11}

S_{11} is input reflection coefficient or input return loss. In order to measure S_{11}, a signal is injected at input port and its reflected signal is measured. In this case, no signal is injected into output port. So, it represents the measure of matching of the input impedance to the reference impedance. It is given by:

$$S_{11} = \frac{b1}{a1}\Big|_{\,a2 = 0} \quad (1.2a)$$

1.2.2 S_{12}

S_{12} is reverse transmission coefficient or reverse isolation as it measures how much the input signal is reflected back. In S_{12}, a signal is injected into output port, and signal power leaving port is measured.

$$S_{12} = \frac{b1}{a2}\Big|_{\,a1 = 0} \quad (1.2b)$$

1.2.3 S_{21}

S_{21} is forward transmission coefficient or forward gain. If S_{21} is to be measured, a signal is injected at the input port, and the resulting signal power exiting output port is measured. It measures how well the signal goes from input to output.

$$S_{21} = \frac{b2}{a1}\Big|_{\,a2 = 0} \quad (1.2c)$$

1.2.4 S_{22}

S_{22} is output reflection coefficient or output return loss. For S_{22} measurement, a signal at output port is injected and its reflected signal is measured. So, it represents the measure of matching of the output impedance to load impedance.

$$S_{21} = \frac{b2}{a2}\Big|_{a1=0} \tag{1.2d}$$

1.3 Low Noise Amplifier

In these wireless communication systems, the RF front-end circuit is low noise amplifier which is one of the crucial elements of RF receivers. They amplify RF signal to a particular level so that the sensitivity requirements of other components in RF receivers such as filters are met by RF signal.

Since, the low-noise amplifier (LNA) is the first stage of receiver and is an important component of wireless telecommunication systems. Firstly, its main function is to overcome the noise of subsequent stages (such as mixers) by providing enough gain, i.e., it should have high gain. Secondly, minimize the effect of the overall noise performance by adding as little noise as possible, i.e., it should have low noise figure itself. Thirdly, large signals should be accommodated without distortion by an LNA, i.e., it should provide good linearity. A specific impedance of 50 ohms must be provided by LNA to the input source and output load. Also, low power consumption should be there especially in portable systems.

1.4 Low Noise Amplifier Design Parameters

The low noise amplifier is the first active and also, an essential block in the receiver chain of communication system. It is used at the front end of the receiver, is connected directly to the antenna. So, the noise performance of low noise amplifier directly impacts the overall noise performance of the receiver. Crucial design specification i.e., noise figure (NF) has trade-offs with other design specifications such as gain, power consumption and third order intercept point (IIP3). So, LNA design consists of trade-offs between gain, noise figure, linearity, input and output matching, and power consumption. However, to achieve good overall system performance, several desired parameters are required such as low power consumption, high gain, high third order intercept point, low noise figure and good input and output impedance matching.

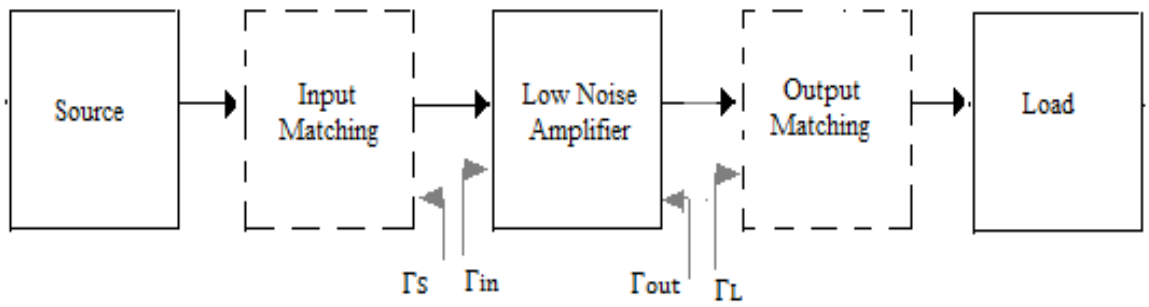

Fig. 1.2 Basic Components of Amplifier with input/output of amplifier (two-port network)

where,
Γ_s is reflection coefficient of source of two-port network,
Γ_L is reflection coefficient of load of two-port network,
Γ_{in} is reflection coefficient at input of the amplifier and,
Γ_{out} is reflection coefficient at output of amplifier.

Combination of following three stages form low noise amplifier

1.4.1 Input matching network.

The input matching network is present so that the input return loss or input reflection coefficient (S_{11}) is minimum without additional noise introduction. The ideal value of the input impedance is infinite if the low noise amplifier is considered as voltage amplifier. So, to obtain minimum noise figure, a transformation network is required before low noise amplifier, if viewed from noise point of view while conjugate matching between antenna and low noise amplifier is required, if viewed from signal point of view. Each of the above choices has its own advantages and disadvantages however, the latter is commonly used in today's systems. Therefore, LNA is designed such that it has input impedance equal to 50 Ω resistance.

The LNA is designed to make gain and linearity as high as possible and make noise figure as low as possible. However, gain and linearity are the two parameters which are poles apart and it is difficult to balance them i.e., gain will be affected while trying to improve the linearity and vice versa. Gain is enhanced in pi-matching when compared to T-matching. So, in order to obtain reasonable linearity at low power, pi-matching is used and hence, is adopted in this thesis.

1.4.2 Main amplifier section

Amplifier section ensures maximum gain and linearity and also, minimum noise figure and power consumption. It also provides input impedance matching at the same time.

1.2.4.1 Power Gain

In figure 1.2, the input/output power gain of low noise amplifier i.e. a two port network is shown. Power gain is defined as the ratio of the power dissipated in the load i.e., output power to the power supplied to the amplifier i.e., input power. The power gain mathematically, can be expressed as:

$$G = \frac{P_{out}}{P_{in}} \tag{1.3}$$

$$G = \frac{(1-|\Gamma_L|^2)|S_{22}|^2}{(1-S_{22}|\Gamma_L|^2)(1-|\Gamma_L|^2)} \tag{1.4}$$

1.2.4.2 Noise Figure

The basic definition of noise is everything except the desired signal. All the communication systems are sensitive to the noise. The signal to noise ratio (SNR) is used for measurement of the noise present in the system.

The degradation of SNR by the circuit is indicated by the noise factor. Noise performance of the system is measured by noise figure. Noise Factor is the ratio of the signal to noise ratio of the input port to that of output port and is larger than 1 dB and is given by:

$$F = \frac{SNR_{out}}{SNR_{in}} \tag{1.5}$$

Noise factor expressed in dB unit is called noise figure and is given by:

$$NF = 10\log\frac{SNR_{out}}{SNR_{in}} \tag{1.6}$$

For the single-stage amplifier, its noise figure is seen as follows:

$$F = F_{min} + \frac{4r_n|\Gamma_S-\Gamma_{opt}|}{(1-|\Gamma_S|^2)|1+\Gamma_{opt}|^2} \tag{1.7}$$

In the formula, Fmin is the minimum noise figure. Γopt, r_n and Γs are the best source reflection coefficient, the equivalent noise resistance of the transistor and the input reflection coefficient of the transistor when Fmin is obtained.

For multi-stage amplifier, the entire system noise is contributed by each stage. So, the total noise factor of the system is given by the Friis formula:

$$NF = F_1 + \frac{F_2-1}{G_{A1}} + \frac{F_3-1}{G_{A2}} + \ldots \tag{1.8}$$

where,
Fn is the noise figure of the first n-amplifier and Gn is the gain of the first n-amplifier.

1.2.4.3 Linearity

The highest value of signal that can accepted at the input of the system is defined as linearity of that system. LNA along with amplification of signal and good noise performance, should be linear even when the signal is strong. Hence, during designing of LNA, linearity is an important consideration. Several methods are used to find the linearity of the system. However, the most commonly used methods are:

A. 1 dB Compression Point (P1dB)

For a specified frequency range the linear amplifier have a fixed gain. The slope of the line in the output power vs input power plot is called gain. However, after some point the gain decreases as the input power is increasing continuously and the point at where the output power is not increased further when input power is increasing, the amplifier enters into compression i.e. becomes saturated. Hence, distortion occurs due to non-linear response. The input signal is restricted to the point where compression begins to occur to avoid distortion. The value of the point is the input power where the gain is decreased by 1 dB from the normal linear gain or the output power where the 1 dB decreased gain drop occurs.

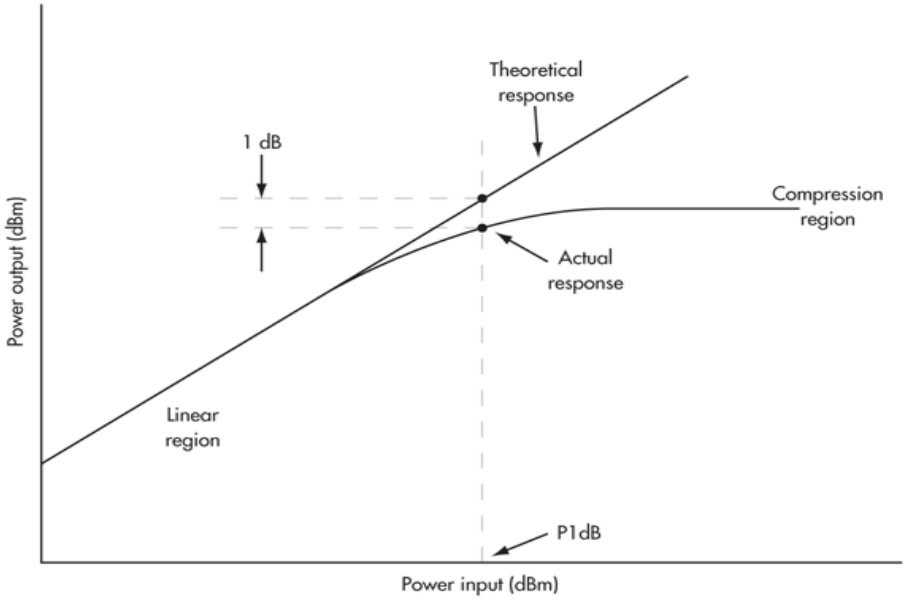

Fig 1.3 P1 dB (logarithmic scale)

B. Third Order Intercept Point (IP3)

The amplified input produces harmonics when the amplifier becomes non-linear. All the harmonics except the first or fundamental harmonic is present outside the bandwidth of the amplifier. Moreover, if the signal harmonics are close in the frequency then their sum and difference frequencies are also present in the bandwidth and are difficult to filter out. These frequencies are called intermodulation products.

If the graph between output power and input power is plotted then a graph similar to 1 dB is obtained and is the first order plot. Third order product signal's graph is also plotted in the same plot. The point at which gain flattens in both the graph is called compression point and if the linear region of both the graphs are extended then they meet at a point where third order signal to the first order signal. This point is called third order intercept point. It is called IIP3 if the third order point is read from input axis and is called OIP3 if the third order point is read from output axis.

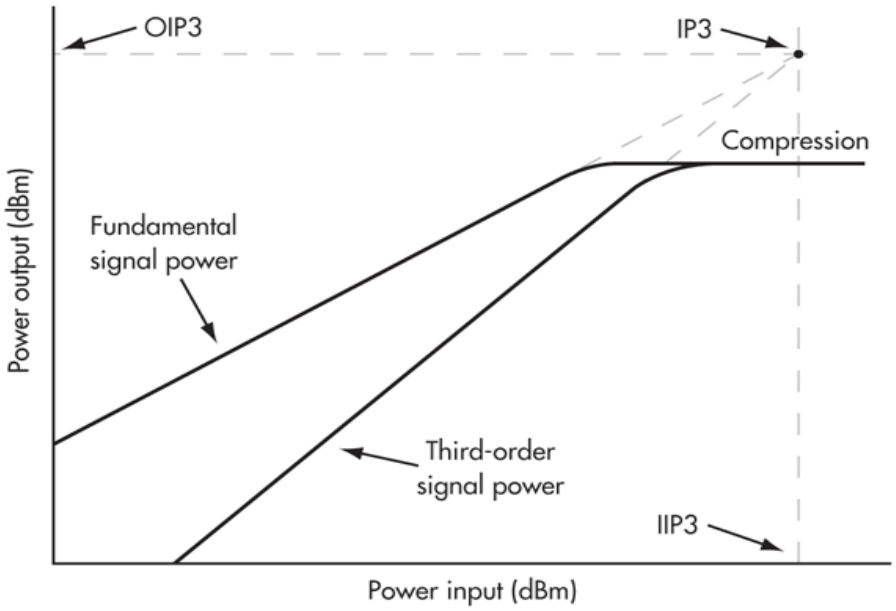

Fig 1.4 Third order intercept (logarithmic scale)

1.4.3 Output matching network

The output matching network is present to guarantee that the output impedance is 50 Ω.

1.3 Low Noise Amplifier Basic Topologies

The important goals in the designing of LNA are low NF, high gain, low power consumption, and 50 Ω input impedance. For achieving all these goals, different LNA architectures are available as follows: Common-Source (CS) stage with resistive termination, Common-Gate (CG) LNA, Common-Source with shunt feedback, Common-Source with inductive source degeneration and Common-Source with cascode inductive source degeneration.

1.5.1 Common Source with Resistive Termination

For termination at the input port a resistor is used, to provide 50 Ω input impedance in the resistive termination CS amplifier. In order to realize input matching, a resistor of 50 Ω is connected in parallel to the input, leading to a high NF. This architecture is undesirable where good input matching as well as low noise is desired.

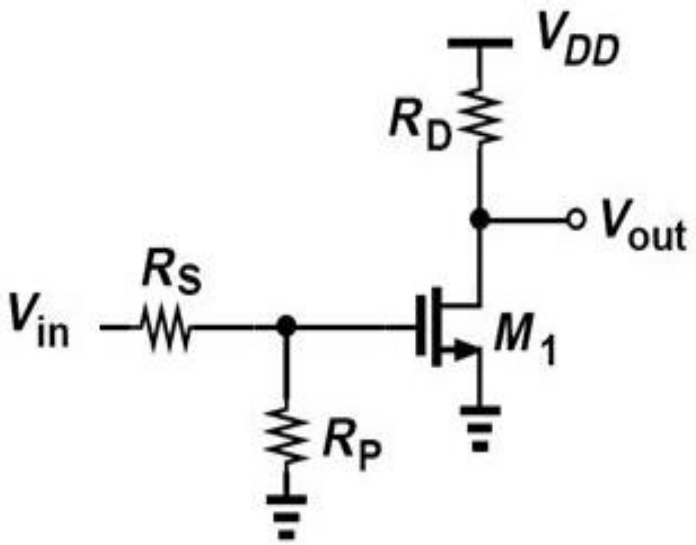

Fig. 1.5 Common Source with Resistive Termination LNA [1]

1.5.2 Common Gate

The transconductance (gm) value should be fixed at $\frac{1}{R_S}$ for the input matching in the Common Gate LNA, therefore, the only design variable is RL. The input transistor's transconductance of cannot be high due to the input matching. However, this topology is well known for wideband applications and also, the noise factor is quite reasonable and acceptable.

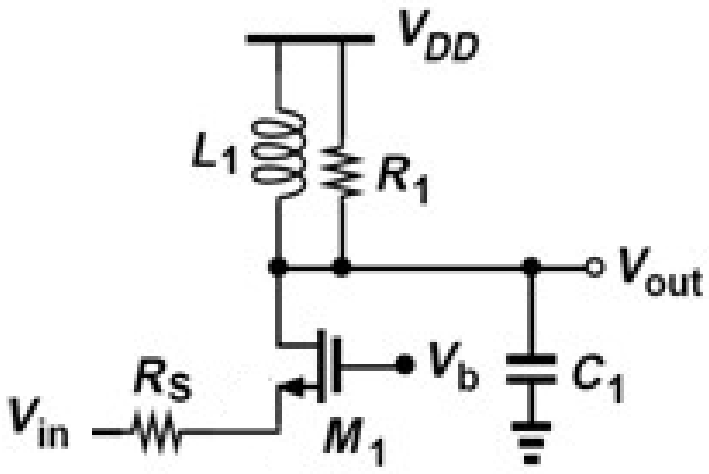

Fig 1.6 Common Gate LNA [1]

1.5.3 Common Source with Shunt Feedback

The Common Source stage with shunt feedback, as compared to the conventional Common Gate LNA, achieves lower noise figure and higher power dissipation.

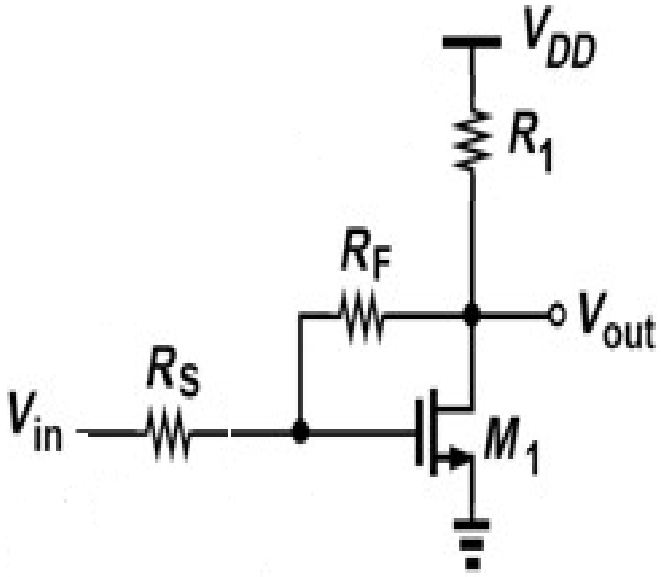

Fig. 1.7 Common Source with Shunt Feedback LNA [1]

1.5.4 Common Source with Inductive Source Degeneration

In Common Source with inductive source degeneration LNA, thermal noise is not generated like an ordinary resistor. So, the input matching requirement is achieved without introduction of the additional noise due to real resistor. Also, compared to

other architectures, this topology consumes less power, making it suitable for low power applications. However, this topology has disadvantages like low gain, low linearity and high noise figure.

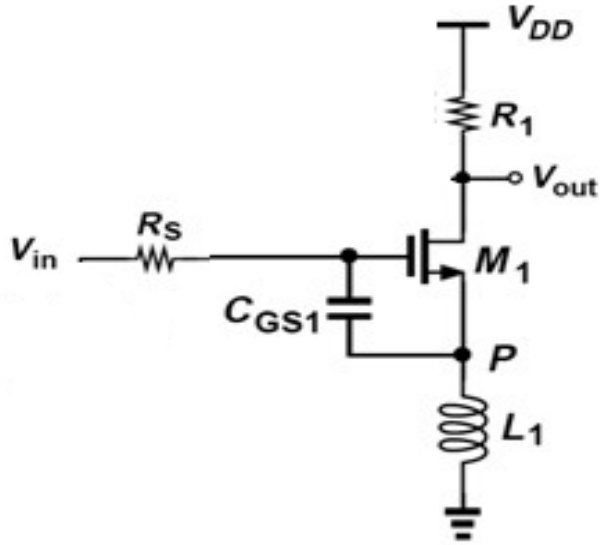

Fig. 1.8 Common Source with Inductive Source Degeneration LNA [1]

1.5.5 Cascode Common Source with Inductive Source Degeneration

The Common Source with cascode inductive source degeneration LNA has high reverse isolation and high stability. However, the inductors L_S and L_G have to be adjusted to keep the input impedance to 50 Ω as the generated noise power from the cascode stage increases when the width of the cascode stage increases.

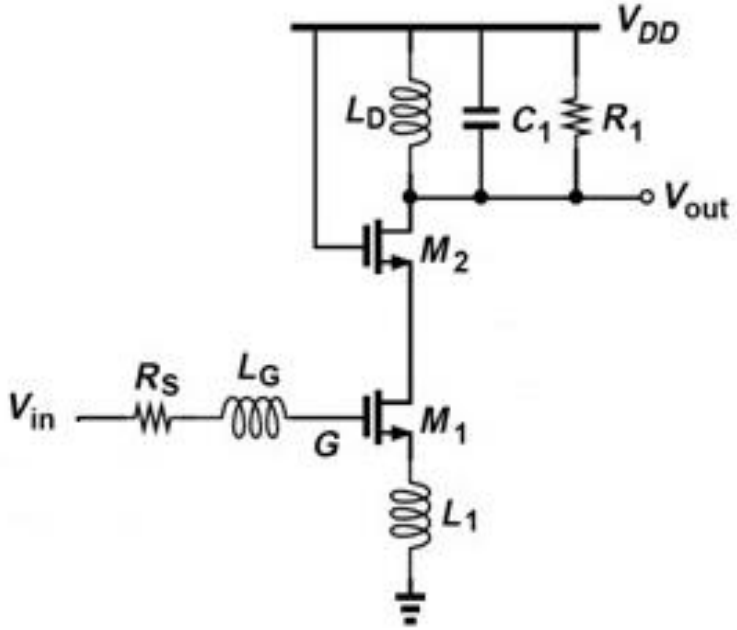

Fig. 1.9 Cascode Common Source with Inductive Source Degeneration LNA [1]

The various LNA topologies are compared in table 1.1 shown below.

TABLE 1.1 COMPARISON OF BASIC LNA TOPOLOGIES

Topology	Advantages	Disadvantages
Resistive termination common source LNA	Broadband amplifier. Good input matching.	Addition of noise from the resistor. High noise figure.
Common gate LNA	Well known for wide band applications. Low power consumption.	Weak noise performance.
Common source with shunt feedback	Broadband amplifier. Has good input and output characteristics.	High power dissipation.
Common source with inductive source degeneration	Suitable for low power applications.	Low gain, low linearity and high noise figure.
Cascode Common source with inductive source degeneration	High reverse isolation and high stability.	The noise power generated from cascode stage increases when the width of cascode stage increases.

Chapter-2

HISTORY

Almost, 20 years ago, the most valuable device present to function as low noise amplifier at high frequency were only travelling wave tubes or vacuum tubes which were fabricated in various laboratories [2]. However, the noise temperature of travelling wave tube was around 3000K. Thus, making its amplification limited by noise in the circuit [3]. The tunnel diode was also used as low noise amplifier which provides amplification by using negative conductance effect but shot noise is present in the dc current that flows during the amplification operation and is major source of noise, contributing as the drawback of using tunnel diode for amplification [4]. The maser standing for microwave amplification by stimulated emission of radiation, having extremely low noise figure replaced vacuum tubes and tunnel diodes but unfortunately it had its own drawback of working at low temperature environment, resulting in use of costly and highly complicated equipment. Therefore, could be used only in sophisticated systems for specialized applications [5]. Parametric amplifier formed from semiconductor diode was also a low noise amplifier because is purely reactive ideally and hence, no noise is present. Low bandwidth is the shortcoming if a single diode is used so, to increase the bandwidth multiple pair of identical diodes are used. Requiring high quality identical diodes is the serious disadvantage of the above technique [6]. Large size and unable to fabricate the device on chip made the above discussed devices less favorable to be used for low noise amplification. So, transistors such as bipolar junction transistor (BJT) or field effect transistor (FET) were used as a low noise amplifier [7][8]. However, the tradeoffs between noise figure, gain, linearity and stability in both the above transistors were different. So, the design of low noise amplifier depends on the transistor technology which is incorporated such as if Gallium arsenide high-mobility electron transistor (GaAs HEMT) is used, excellent linearity and noise figure is obtained compared to Silicon Germanium Heterojunction bipolar transistor (SiGe HBT) but on the other hand, low power consumption, high gain and good noise figure is obtained by SiGeHBT. Since, the area on chip required by BJT and FET is large, CMOS technology are used being used. The complementary MOS (CMOS) transistor is used in low noise amplifiers because of its good characteristics. High immunity against noise and static power are two of the important characteristics of CMOS transistors. Moreover, CMOS technology are used to fabricate in-chip low noise amplifiers because of high level of integration [9]. The internal structure of CMOS contains a NMOS and PMOS transistor in series. So, the power is drawn by the series combination momentarily when there is switching between ON and OFF states, because one of the transistor in the series connection is always OFF. Hence, the heat produced by CMOS devices is less as compared to other logic families such as transistor transistor logic (TTL), NMOS, etc.

Number of new devices capable of giving better performance substantially is present during these recent times. So, from the past 20 years and more, there are continuous and rapid development of low noise amplifiers due to discovery of new and advanced devices for fabrication of low noise amplifier. Moreover, the advancement in technique to reduce noise is also responsible for low noise amplifier development. Therefore, for implementation of low noise amplifier, CMOS is one of the competitive technology because of high level of integration, low cost and technology scaling. Furthermore, ultra-high level of integration (UHI) is achieved due to advancement in technology scaling. Currently, most of the low noise amplifier are designed using 0.18 μm or 0.13 μm technology.

Chapter-3

LITERATURE SURVEY

Our knowledge in the field of low noise amplifier cannot be updated without studying the earlier work done by the researchers/scientists because the earlier concepts and techniques given are helpful to study and analyze present technology concepts and techniques as there is increasing and constant demand to make the devices smaller, portable, consuming less power and operating for large frequency band. A brief review of the earlier work done in the designing of low noise amplifier by simple current reuse technique, common source cacode amplifier topology, common sou5rce inductive degeneration amplifier topology, cross couple capacitor technique and, etc. in various CMOS technology (90 nm, 35 nm, 0.18 µm, 0.13 µm) for microwave frequency i.e. frequency ranging from 300 MHz unto 300 GHz is discussed in the following literature review.

3.1 Narrowband LNA

3.1.1 900 MHz

This paper [10] proposes and designed first CMOS LNA that integrates input and output matching network for 900 MHz ISM Band. The LNA is formed by two stage amplifier, the first stage of which is a cascaded amplifier having inductor-capacitor resonator as load so as to improve gain and noise performance while the second stage is a CS amplifier having capacitor transformer and resistor as a load. Therefore, improved reverse isolation and simplifying the matching because of input and output decoupling are the advantages of using two stage amplifier. It also includes series inductive feedback, bias circuit and capacitive transformer. The LNA is designed on a chip of size 0.74x0.72 mm^2 using 0.8 µm CMOS technology. A supply of 3 V is used for drawing current of 8.6 mA from first stage and 2 mA from second stage. Maximum power gain of 14.3 dB, minimum noise figure of 4.5 dB and P_{1dB} of +5 dBm is observed.

A LNA for 900 MHz is designed using 0.5 µm CMOS technology. Current reuse technique is used to increase overall LNA gain. The LNA design approach utilizes two stage amplifier. The forward gain is achieved from stage 1 of the amplifier and unity buffer is achieved from stage 2. Also, each stage employs bias feedback amplifier to establish Q point for each stage by setting dc output voltage of each stage to bias reference. Output of first stage is directly coupled to input of second stage. A minimum noise figure of 1.9 dB, gain of 15.6 dB, IIP3 of -3.2 dB and power consumption of 20 mW is obtained when a supply of 2.7 V is given to LNA. Chip of size 0.7 mm x 0.4 mm is designed [11].

In the paper [12], broadband inductorless LNA design at 900 MHz is explored as LC tanks which are highly tuned and have high Q value are not used i.e. on chip

providing overdrive capabilities are not exploited. The LNA consists of three NMOS gain stages in cascode. Also, multistage topology is used by the LNA so that at low or zero intermediate frequency the circuit has critical reverse isolation. To reduce power consumption, current reuse technique is used and to improve linearity the last two LNA stages are degenerated. For the input stage, open loop structure is used to avoid noise generated by the feedback system and the output buffer is degenerated cascode amplifier. A 9 dB gain, 2.3-3.3 dB NF, >-41 dB S_{21} and -4.7 dBm IIP3 has been observed by 900 MHz designed using 0.5 µm CMOS process while current of 3.4 mA is drawn from 3 V supply. A die area of 1.0 x 1.2 mm^2 has been used in total and the largest part occupied only by de-coupling capacitors while die are of 0.4x0.3 mm^2 is occupied only by active core.

A 900 MHz LNA is implemented in the paper [13] fabricated using three level metal 0.8 µm CMOS process and SOIC like package used for packing. Amplifier design topology is cascode topology having only single stage for improvement of linearity, 1 dB compression point and minimization of power dissipation and also uses inductive degeneration at the source. The cacsode stage is used to improve reverse isolation and eliminate Miller effect and source inductive degeneration is used to achieve input matching and noise matching simultaneously. Only one external inductor is required. The area occupied by the chip is 720x720 µm2. The LNA provides NF of 1.2 dB at 30 mW, 1.5-dB at 13.5 mW, and 2-dB at 6.3 mW. Also, a NF of less than 2 dB is provides at less than 10 mW power. Moreover, an IIP3's of -1 dBm is obtained at 30 mW and -3.8 dBm at 6.3 mW. A high S_{11}, S_{22} is below -10 dB and S_{12} is more than 42 dB.

A full integrated 900 MHz CMOS LNA has been fabricated with 0.35 µm minimum channel length. To provide wide dynamic range and low noise a single stage cascoded inductive degeneration configuration is used. Single stage is used in order to limit power consumption and improve reverse isolation of the LNA. Also, LC networks is used to achieve 50 Ω matching. The CMOS LNA of three different version is fabricated in [14] with the main transistor width (W) of 225µm, 450µm, and 675µm, are C225, C450, C675 respectively and is mounted of TQFP48 package. C225 is measure on dedicated application board and packed components are soldered on the board while C675 is measured on test board and packaged chip is plugged in Johnstech socket. C450 is measured on dedicated application and test board. The best configuration is C450 having 16 dB NF at 12 mA and 1.5 dB NF at 20 mA, along with VSWRin less than or equal to 2.5. For good matching conditions i.e. for VSWRin less than or equal to 2, the NF≤1.75 dB, IIP3≤3 dBm and gain equal to 10 dB.

A 900 MHz LNA using 0.35 µm CMOS process has been fabricated. A single stage cascode LNA configuration is used. Here, to reduce power consumption single stage is used and to reduce Miller effect and to improve reverse isolation cacscode configuration is used. Transistor of width (W) of 450 mm is used. The LNA is housed into TQFP48 package. A power gain of 14 dB, NF of 0.9 dB, S_{11} of -10 dB, S_{22} of -27 dB and IIP3 0f 0 dBm is obtained at 18 mW power while a NF of 1.05

dB is also obtained at 9 mW power along with power gain of 12 dB, S_{11} of -8.7 dB, IIP3 of -2 dBm [15].

The LNA working at 900 MHz and to be used as mobile CDMA receiver, that works on 824-894 MHz has been proposed and fabricated in the paper [16]. The LNA circuit uses the current reuse technique so as to achieve transconductance of that of device but by using less current. The inductors in LC network that is used as the load and are tuned at operating frequency, has high quality factor. The quality of inductor is high if the substrate resistivity is higher. This, the performance of inductor depends on the doping of substrate. The LNA is implemented using 0.35 µm CMOS process. The dimensions of the LNA are 1541 µm x 850 µm and the total area occupied is 1.31 mm^2. A NF of 1.8 dB, gain of 15 dB, IP3 of -3 dBm and compression point of -11 dBm is obtained.

TABLE 3.1 COMPARISON OF LNA AT 900 MHZ

	[10]	[11]	[12]	[13]	[14]	[15]	[16]
Technology (µm)	0.8	0.5	0.5	0.8	0.35	0.35	0.35
Supply (V)	3	2.7	3	-	-	-	-
S_{21} (dB)	14.3	15.6	9	-	10	14 @18mW	15
NF (dB)	4.5	1.9	2.3-3.3	1.2 @ 30mW	≤1.75	0.9 @ 18mW	1.8
IIP3 (dBm)	-	-3.2	-4.7	-1 @ 30mW	≤3	0 @18mW	-3

3.1.2 1 GHz

Single ended two 1 GHz LNAs has been designed in the paper [17] with and without ac coupled inductor. Both the LNAs utilizes single stage cascode topology along with pull up resistive load without no chip inductor. However, the second LNA topology uses an additional ac coupled inductive load. Thus, forming inductive degeneration cascode topology. The active inductor working in GHz is built from CMOS gyrator as it can form large value inductor (20-40 nH) on chip using an area less than used by on chip spiral inductor. However, has poor linearity compared to on chip spiral inductor. A 0.5 µm CMOS technology is used in designing of the LNA. The circuit uses 2 V supply. The active inductor LNA provides a gain of 12.2 dB, IIP3 of -21 dB and NF of 2-2.3 dB for long channel model and 2.7-3.1 dB for short channel model consuming a power 17 mW while the inductorless LNA provides a gain of 10.7 dB, IIP3 of -3.8 dBm and NF of 2-2.2 dB for long channel model and 2.6-2.9 dB for short channel model consuming a power of 16 mW. The input return loss is -10 dB and reverse isolation is higher

than 45 dB for the both the LNA while the output matching is less than -10 dB for active inductor LNA. Therefore, out of both the LNA design, active inductor LNA is more selective and image reject filter requirements are relaxed with the help of series resonance.

A 0.5 µm RF CMOS LNA using current reuse technology and CS inductive degeneration topology is proposed in [18]. The first stage of LNA has a PMOS and a NMOS, CS amplifier in cascode configuration followed by a CG stage. Another transistor in CS configuration is present before the cascode to set the dc bias of transistor in cascode stage while a transistor in CG configuration is present at the end as buffer stage to provide output matching of LNA. The on chip inductor i.e. the degenerated inductor have quality factor of 5 while the off chip inductors i.e. input and output inductors have quality factor of 50. The proposed LNA at 1GHz gives a S_{11} of -31.8 dB, S_{21} of 21.6 dB, S_{12} of 42 dB, S_{22} of 42.1 dB, NF of 2.7 dB and IIP3 of 18.8 dB. Also, a current of 20.3 mW is consumed from 2.2 V supply.

A 1 GHz CMOS LNA which uses cascode configuration but in modified form is proposed in the [19]. Here, the LNA circuit uses a CS amplifier which is inductively degenerated in the first stage of LNA followed by CG amplifier, which forms a cascode configuration. A CS amplifier before stage 1 is used to bias the amplifier in first stage and a CG amplifier is used at the end as a buffer stage to achieve output matching. The inductor on chip is a degenerated inductor having quality factor of 5 and the input and output inductors are off chip inductor having a quality factor of 50. 0.5 µm CMOS technology is used to design the LNA circuit. An input reflection coefficient of -33.64 dB, forward gain of 18.6 dB, reverse isolation coefficient of -45.5 dB, output reflection coefficient of -35.22 dB, NF of 1.62 dB and IIP3 of -23 dBm is observed. A power of 12.5 mW is consumed from 1 V supply.

TABLE 3.2 COMPARISON OF LNA AT 1 GHZ

	[17]		[18]	[19]
Technology (µm)	0.5		0.5	0.5
Supply (V)	2		2.2	1
	Active inductor	Inductorless	21.6	18.6
S_{21} (dB)	12.2	10.7		
NF (dB)	2-2.3	2-2.2	2.7	1.62
IIP3 (dBm)	-21	-3.8	18.8	-23

3.1.3 1.5 GHz/GPS

For GPS receiver a 1.5 GHz LNA is implemented in 0.6 µm CMOS technology by employing inductive source degeneration topology along with input tuning so that 50 Ω narrow band input impedance is achieved, to convert the MOS device reactive

input impedance into real resistance. Although, dual-feedback and resistive termination could also have been used but each have its own drawback; of being used when loop gain requirement can be satisfied easily at low frequency and on the NF lower bound of 3dB is placed respectively. A gain of 22 dB, NF of 3.5 dB and IIP3 of -9.3 dB is obtained while from 1.5 V, a power of 30mW is consumed [20].

A 1.5 GHz LNA for GPS receiver, front-end applications has been designed with one poly and two metal layers only in 0.35 µm CMOS process. For better on chip rejection, a differential architecture is selected but consumes twice the power consumed by single ended architecture to achieve same noise figure. The architecture of LNA consists of two stage, the stage 1 is cascoded so that reverse isolation improves, stability is maintained as spiral inductor is used to tune stage 1 output and the influence gate to drain overlap capacitance is reduced on input impedance i.e. Miller effect is mitigated. Moreover, by reusing the bias current of stage 2 in the stage 1, the power factor is decreased by a factor of two. So, a common mode feedback technique is used. At the source of two transistors the inductive degeneration is employed so that output of the RF filter present before the LNA is properly matched to input impedance of LNA. Baluns are used to interface to single ended test instrumentation since, the circuit is differential. A total die area of 0.84 mm^2 is used to fabricate a LNA and a mixer on a single chip. The gain of LNA is 17 dB, NF is 3.8 dB and IIP3 is -6 17 dBm and reverse gain is 52 17 dB, while dissipating a power of 12mW and using 1.5 V supply [21].

A 0.35 µm differential CMOS LNA has been fabricated for GPS application in [22]. Inductive degeneration topology in differential form is used at the input stage and LC network is used as load where the quality factor of the inductor is 7. Transistor in cascode also present between input stage and LC load to reduce Miller effect and increase reverse isolation. At the gate of the input stage transistor, the spiral inductor is integrated in series so that level of integration is increased. Since, the telecommunication signal is narrowband, narrowband RF signal processing is required. Here, the input stage is intrinsically narrowband because maximum power transfer occurs at carrier frequency because at carrier frequency only the source and input impedance match and, out of band signal components is filtered out and in band thermal noise is minimized because of LC feedback. The LNA has been realized by 5 metal layer while spiral inductor itself is realized by upper thicker metal layer. The simulated LNA has 26 dB gain, NF of 3.6 dB, IIP3of -3 dBm and current of 5 mA flows from 2.8 V supply.

A two stage LNA has been designed using 0.6 µm CMOS for 1.57 GHz. The LNA is design consists of cascode configuration in first stage so that input resonant circuit and output resonant circuit are decoupled followed by source follower present in the second stage. A coupling capacitor is used to separate the two stages. Current mirror is used to bias the input transistor so that minimum noise is coupled between the biasing resistor and the signal path. A separate circuit is used to bias the second stage. So, power consumption is less. The results observed for 1.8 V

power supply is that the circuit dissipates a power of 17 mW with a NF of 2 dB, gain of 19 dB, S_{11} of -30 dB, S_{22} of -32 dB, S_{12} of -57 dB and IIP3 of 10 dB. Moreover, in paper [23] noise rejection behavior of proposed design's single ended and differential LNA has been studied and it is indicated that for the same gain differential LNA produces more noise compared to single ended LNA but is less prone to common mode noise.

A LNA for GPS receiver has been designed using 0.25 µm CMOS process in [24]. The LNA circuit uses two stage differential structure, in the stage 1 two CS amplifier are present in cascode configuration to reduce Miller effect and to improve reverse isolation, and also degenerated inductor is employed at the source to achieve stable input impedance. Spice using level 49 CMOS parameter is used for simulation of LNA, giving a NF of -5.6 dB and gain of 22 dB. The LNA circuit dissipates a power of 35 mW and uses 3 V supply. The LNA layout is designed using Cadence and area of the layout is 0.27x0.33 mm^2.

A two stage LNA has been designed using 0.18 µm CMOS process in [25]. The first and second stage of the LNA consists of CS amplifier with inductively degenerated inductors at the source. The output of the first stage is provided at the gate of the amplifier in the second stage. Another CS configuration transistor is present before the first stage to bias the in the amplifier in the first stage. Inductors are used as load for the two stages. The circuit is simulated using Cadence Spectre RF and uses 1 V supply. A NF of 2.0 dB, gain of 28.7 dB and IIP3 of -16.0599 dBm is obtained.

A LNA based on noise optimization technique has been designed [26] for 1.5 GHz. The LNA circuit has single stage having two CS amplifier. Also having 1 nH bond wire inductor as the degenerated inductor at the source of the first amplifier. LC network is used at the load so that is optimized at the operating frequency. The circuit is designed using 0.13 µm CMOS process. The simulated LNA has input reflection coefficient of about -17 dB, gain of 12.9 dB and NF of 0.55 dB. A current of 1 mA is drawn from a supply of 1 V.

A cascode CS inductive degeneration topology is used in designing of the LNA using 90 nm CMOS technology. The gate inductor and degenerated source inductor is used for input impedance matching as at the resonant frequency are acted like series resonant circuit. Another transistor is present in current mirror formation with the CS stage transistor in cascode configuration. The load of cascode architecture is LC circuit which is used to achieve output impedance matching. Cadence spectre RF is used for simulation of the LNA circuit. The input return loss, reverse isolation, power gain, NF and IIP3 are -9.9 dB, -35.68 dB, 30.942 dB, 0.533 dB and 2.9140 dB respectively. The circuit uses a supply of 1.5 V and dissipates a power of 8.7 mW [27].

TABLE 3.3 COMPARISON OF LNA AT 1.5 GHZ

	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]
Technology (µm)	0.6	0.35	0.35	0.6	0.25	0.18	0.13	90 nm
Supply (V)	1.5	1.5	2.8	1.8	3	1	1	-
S_{21} (dB)	22	17	26	19	22	28.7	12.9	30.942
NF (dB)	3.5	3.8	3.6	2	-5.6	2	0.55	0.533
IIP3 (dBm)	-9.3	-6.17	-3	10	-	-16.0599	-	2.9

3.1.4 1.8 GHz/ Direct Conversion Radio Receiver

A 1.8 GHz LNA for direct conversion radio receiver, that can drive a capacitive input mixer, has been designed in the paper [28]. In the front–end subsampling, aliasing problem is reduced by limiting LNA noise band with output resonator and integrated passive component's extracted models is used for optimizing the resonator, including on chip coupling capacitor to overcome the problem of second order non-linarites in down conversion of direct conversion receiver. Also, to optimize system noise figure output resonator is used, by limiting input noise bandwidth of mixer. The LNA uses cascaded input and inductive degeneration topology. A high quality factor of 4 is used in designing of circuit, else small change in component value will increase the NF significantly. A 0.5 µm CMOS technology is used to design LNA. DC coupling which has low sensitivity to parasitic effect is realized with an on chip structure as is an essential function of direct conversion. A gain of 17 dB, S_{11} of -11 dB, IIP3 of +9 dBm and NF of 3.4 dB is obtained while consuming a power of 48mW from a 3 V supply. Therefore, a method to implement modern integrated receiver having CMOS LNA in GHz range using capacitor inputs instead of 50 Ω resistor matching is designed.

A two stage LNA is designed in [29] which is based on LC resonance that uses spiral inductor on chip. The LNA uses differential structure so that even order distortion gets eliminated and also uses common mode inductive coupling because it is desired for direct conversion receivers. The common mode inductive coupling can be assumed as the extension of CS topology with a spiral inductors present on chip for applications in narrowband frequency and current source for biasing. The cascode structure is also used. The inductive load are used instead of resistive load and is of 7 nH having a quality factor of 4.5. Positive feedback circuit is also present to generate negative resistance which cancels out the series resistance present in the inductive load. A 0.8 µm with two poly and two metal CMOS process is used for designing of the LNA. The LNA exhibit a power gain of 18 dB, NF of 2.1 dB and IIP3 of -5 dBm wile dissipating a power of 48 mW from 3 V supply.
A LNA working at 1.8 GHz, using double poly triple metal 0.35 µm CMOS technology is designed and is presented in [30]. The LNA circuit uses a two stage

cascaded configuration to provide good gain and isolation between input port and output port simultaneously. In the stage 1, CS inductive degeneration topology is used to match input impedance to 50 Ω followed by stage 2 which is a buffer stage present to match output to 50 Ω. The LNA layout occupies an area of 1025 x 1345 μm^2. The S-parameter is measured using HP 8719ES network analyzer and a resultant S_{11} parameter value is -8.4 dB, S_{12} is -41.7 dB, S_{21} is 10.5 dB and S_{22} is -6.6 dB. A NF of 4 dB and IIP3 of -2.4 dB is also observed. The circuit is operated using 2.5 V supply dissipates a power of 40 mW.

A two stage architecture LNA circuit having input stage as the first stage uses CG amplifier so as to achieve lower NF and uses CS stage as the second stage so as to achieve high gain along with good reverse isolation is designed in [31]. A capacitor present for dc blocking and an inductor is present between CG and CS amplifiers to provide biasing network to CS amplifier and for matching AC power so as to achieve maximum power transfer. Therefore, the capacitor and the inductor act as interstage matching network. Spectre RF is used for the simulation of the LNA. The resultant input reflection coefficient value is -6.4 dB, output reflection coefficient is -31.8 dB, power gain is 17.4 dB, reverse isolation of -66 dB, NF is 1.07 dB and IIP3 is -9 dBm while OIP3 is 8.1 dBm. The LNA circuit is designed using 0.35 µm CMOS process and a power supply of 1.2 V.

TABLE 3.4 COMPARISON OF LNA AT 1.8 GHZ

	[28]	[29]	[30]	[31]
Technology (µm)	0.5	0.8	0.35	0.35
Supply (V)	3	3	1.8	1.2
S_{21} (dB)	17	18	10.5	17.4
NF (dB)	3.4	2.1	4	1.07
IIP3 (dBm)	9	-5	-2.4	-9

3.1.5 1.9 GHz/GSM

A spiral inductor of high quality has been employed in the paper [32] having 8.5-12.5 quality factor along with optimized active device layout and bias condition. The LNA is a two-stage amplifier, CS with inductive source degeneration is present in the stage-1so as to match noise and power gain. For high linearity and gain, the second stage's bias condition is chosen. A 0.8 µm CMOS technology LNA, fabricated on high resistivity Si substrate. Using on-wafer RF probes and HP8510C Network Analyzer measurements are carried out and a chip area of 0.93x0.93 mm2 is occupied. Linear simulator is used to simulate the LNA and ATN setup is used to measure noise parameters for 0.3-3 GHz, giving a NF of 2.8 dB at 1.9 GHz. Also, a gain of 15 dB, input reflection coefficient of -16.4 dB and output reflection

coefficient of -7 dB is observed at 1.9GHz, while consuming 15 mA from 3.6 V supply.

A quantitative analysis of LNA in cascode configuration is done in [33] in 0.35 µm CMOS process. A single stage LNA having two transistor namely M1 and M2 is present in cascode. Degenerated inductor is present at the source of M1 and also input is applied to the gate of M1. The cascode structure is present to achieve input impedance matching and to avoid thermal noise. The noise performance of the LNA is dominated by the first MOSFET transistor i.e. M1 while the more linarites are contributed by second MOSFET transistor i.e. M2. So, using 0.35 µm CMOS process the M1 is designed such that it gives optimum noise performance and M2 is designed to optimize linearity. The simulation of 1.9 GHz LNA is conducted in Agilent Advanced Design System (ADS) giving a minimum NF of 1.6 dB, gain of 17.5 dB, OIP3 of 10.7 dBm using a supply of 1.5 V and dissipating a power of 9 mW. Therefore, from both theoretical analysis and simulation results it is shown that the noise performance is dominated by the first MOSFET and more linaerites are contributed by second MOSFET for the LNA in cascode configuration.

A 1.9 GHz LNA has been designed in [34] using 0.35 µm CMOS technology. In the two stage LNA design, the first stage is in cascode configuration and LC tank circuit is present as the load of the cascode architecture so as to tune to 1.9 GHz. Moreover, another inductor is present at the source of the first transistor. This stage is followed by an output stage consisting of one transistor, also having LC circuit as load. Also, a current mirror is formed with before the cascode stage with first transistor of cascode stage. Inductors are placed on chip if have value lesser than 10 nH while are placed off chip if the inductor have value greater than 10 nH. For TSMC CMOS 0.35 µm, BSIM3 transisitor model is used. The circuit is simulated using HSPICE and Cadence giving a gain of 21 dB, NF of 1.4 dB at 1.9 GHz and OIP3 of -14dBm, input reflection coefficient of -35dBm and output reflection of -32dBm. A supply of 1.5 V is used and power dissipated is 6.5 mW. A die of active area 5 10 µm x 250 µm is also formed.

TABLE 3.5 COMPARISON OF LNA AT 1.9 GHZ

	[32]	[33]	[34]
Technology (µm)	0.8	0.35	0.35
Supply (V)	3.6	1.5	1.5
S_{21} (dB)	15	17.5	21
NF (dB)	2.8	1.6	1.4
OIP3 (dBm)	-	10.7	-14

3.1.6 2 GHz

A 2 GHz LNA has been designed using 0.6 µm CMOS process in [35]. The LNA circuit design is based on two stage cascode topology which is narrowband LC tuned. The first stage uses CS cascode inductive degeneration topology followed by CS configuration which has LC network as load because in wireless communications RF signals are narrowband usually. The cascode architecture is used to improve reverse isolation and also to provide forward gain. The circuit uses 3.3 V supply. A NF of 2.3 dB, gain of 18 dB, reverse isolation of -44.79 dB and IIP3 of -4.94 dBm is observed as the simulation results. Also, power of 33.94 mW is dissipated.

A 0.35 µm CMOS LNA is designed in [36]. The LNA design is a two stage amplifier design, it uses conventional cascode topology. An inductor is present between the CS amplifier and CG amplifier in the cascode stage. So, inductor is used as the interstage matching network. The cascode stage is succeeded by a CS stage which along with resistors are used to bias the amplifiers in the cascode stage. The inductors used have quality factor around 5. The simulation of 2 GHz LNA using an interstage inductor is done in Agilent Advanced Design System (ADS). The simulated results are, NF of value 1.97 dB, gain of 13.7 dB. Dissipating a power of 7.5 mW from 1.5 V supply.

A 2 GHz LNA designed using 0.18 µm CMOS process has been implemented in [37]. The LNA circuit has three parts, the first part uses CS inductively degenerated topology, the second part is realized using differential pair acting as a low pass filter and the last part is the biasing circuit formed by using pn junction of PMOS as it provides steady voltage because of the large width of the transistor. The circuit uses 1 V supply and is implemented using 0.18 µm CMOS process. A LNA of size 175 µm x 50 µm is obtained. Moreover, the simulated results shows that the input reflection coefficient is -25 dB, gain is 11 dB, NF is 1.8 dB and IIP3 is 0 dBm.

A high linearity LNA circuit has been designed using 0.25 µm CMOS technology in [38]. The LNA circuit utilizes inductively degenerated topology in balanced differential mode. A superior noise performance is obtained from inductively degenerated topology because of signal swing and hence is used. However, because of the signal swing the linearity is degraded. Thus, the linearity improvement technique is required. For differential signals two balun transformers are used. The LNA circuit uses a supply voltage of 2.5 V. At 2 GHz a maximum gain obtained is 15.2 dB, NF obtained is 2.8 dB and IIP3 obtained is 14.7 dBm and the maximum IIP3 of 16 dBm is obtained at 2.2 GHz. The size of the fabricated chip is 900 µm x 900 µm.

TABLE 3.6 COMPARISON OF LNA AT 2 GHZ

	[35]	[36]	[37]	[38]
Technology (µm)	0.6	0.35	0.18	0.25
Supply (V)	3.3	1.5	1	2.5
S21 (dB)	18	13.7	11	15.2
NF (dB)	2.3	1.97	1.8	2.8
IIP3 (dBm)	-4.94	-	0	16

3.1.7 2.4 GHz/Wireless Sensor Network/Bluetooth

A two stage 2.4 GHz LNA is presented in the paper [39][40]. The first stage has transistors in cascode configuration with resistor in parallel to capacitor as load. Here, resistor is present to set bias circuitry current to generate bias voltage at gate of first transistor in second stage; in second stage transistors are present in cascode having matching inductor between the stage such that the transistors in cascode are considered as different individual stage. So, the inter stage inductor is added between CS and CG stage. Inductor is added to increase the gain and decrease the noise of the system. The capacitor is used to provide AC ground at the gate of second transistor in second stage. A LNA using 0.5 µm CMOS technology is designed using a 3 V supply. A power gain of 19 dB, NF of 2.4 dB and input reflection coefficient of -10 dB is observed while drawing a current of 3mA.

A 2.4 GHz two stage cascade topology LNA using 0.35 µm CMOS process has been proposed in the paper [41]. The LNA using cascade topology uses series inter-stage resonance. So, it is a current sharing amplifier. Here, the two common source amplifiers are not cascaded directly but an inductor in series resonance with capacitor is present. The series resonance provides low impedance at the drain of the first transistor in the cascade stage so that common source stage of the first transistor does not experience Miller effect. A supply of 2 V is and a power gain of 21 dB along with NF of 1.24 dB has been observed. A current of 2.5 mA is drawn by the circuit.

Two CMOS LNA has been designed in the paper [42] one is single ended LNA while the other is differential LNA and fully integrated without off chip components. In the single ended LNA cascode topology is used and a degenerative inductor is also present at the source of the first amplifier in cascode architecture. Here, the input matching is obtained by the two inductor present at the gate of first amplifier present in cascode topology while the output matching is obtained by tuning of the load inductor and output capacitor. The simulation results of single ended LNA is input reflection coefficient of -17 dB, reverse isolation of -24 dB, gain of 15 dB, output reflection coefficient of -23 dB, NF of 2.2 dB. Also, a power dissipation of 4.8 mW is obtained from 3.3 V supply. In the differential LNA

architecture, the single ended LNA architecture is present in differential form. The differential LNA architecture is studied because the single ended LNA architecture is sensitive to ground parasitic inductance while the differential LNA is not affected by the common mode interference. The simulation results of differential LNA is input reflection coefficient of -19 dB, reverse isolation of -35 dB, gain of 20 dB, output reflection coefficient of -21 dB, NF of 2.4 dB. A power of 7.2 mW is dissipated from 3.3 V supply. The layout is designed using 0.25 µm CMOS process and the layout area of single ended LNA is 2.05 mm x 1.28 mm while the layout area of differential LNA is 1.62 mm x 1.28 mm, which is smaller than the single ended LNA.

The LNA designed using 0.35 µm CMOS uses the conventional cascode LNA topology with degenerated inductor in differential form [43]. Since, the mismatch occurs at CS and CG amplifier present in cascode topology the spiral inductor is present between the amplifiers in the cascode stage so as to improve the matching. At the output two source follower namely (M6 and M7) transistor along with a resistor form a current source and also, current mirror is formed by another transistor (M5) with M6. The LNA circuit is simulated for 2.4GHz and using a supply of 2 V. A power gain of 19.9 dB, reverse isolation of -47.8 dB, NF of 2.5 dB and IIP3 of 2 dBm is obtained with a power dissipation of 14.7 mW.

A 2.4 GHz fully differential LNA is proposed in [44]. The LNA circuit core has a cascode design so as to remove the Miller effect and improve the reverse isolation. The linearity of the LNA is required such that if the user is close to the transmitter the linearity from minimum detectable signal to -12 dBm is achieved. However, the LNA is able to meet these specifications but the signals overdrive the subsequent stage. So, to overcome this problem the LNA in this paper is designed to have a low gain so that it could suppress input signals that have large level to desired level. Moreover, so that linearity is improved and current is reduced. A network of NMOS devices are used which acts as bypass switches along with cascode architecture to implement low gain stage and to avoid feedback that causes unstable condition. A 0.25 µm CMOS process is used to design the LNA architecture. NF, gain, input return loss, output return loss, reverse isolation and IIP3 observed are 2.88 dB, 14.7 dB, >7 dB, >10 dB, >25 dB and -1.5 dBm respectively for a high gain mode whereas for low gain or for bypass mode the NF, gain, input return loss, output return loss, reverse isolation and IIP3 observed are 14.2 dB, -14.2 dB, >9 dB, >10 dB, 14.2 dB and 19 dBm. A current of 11.4 mA is consumed in high gain mode while no current is consumed in low gain mode.

A conventional cascode LNA with degenerated inductor is used in the LNA circuit to be operated at 2.4 GHz [45][46]. The circuit also contains additional capacitor in parallel to the gate capacitor of the CS amplifier present in cascode topology so that low power is dissipated and noise performance is optimized. An additional interstage inductor is present between CS and CG stage so that matching is improved and also gain is increased. This circuit is implemented using TSMC 0.18 µm CMOS process. 1.2 V power supply is used in the circuit and power dissipation

of 2.4 mW is observed. Also, S_{11} = -22.4 dB, S_{12} = -48.9 dB, S_{21} = 12.9 dB, S_{22} = -21.6 dB and a NF of 0.76 dB is observed.

A two stage LNA using 0.18 µm CMOS process has been designed in the paper [47]. The first stage is in CS inductively degenerated cascode configuration followed by second stage which is source follower. In the first stage the input transistor is the main noise contributor while the second transistor contributes to the linearity more than first transistor or input transistor. The circuit uses a supply of 1 V and dissipates a power of 13 mW. The S_{11} obtained is -16.8 dB, S_{12} obtained is -51.7 dB, S_{21} obtained is 23 dB, S_{22} obtained is -10.2 dB, NF obtained is 3.8 dB and IIP3obtained is -9.1 dBm.

A LNA operated at 2.4 GHz, with improved matching has been proposed in the paper [48]. The LNA circuit utilizes conventional cascode topology with degenerated inductor at the input. Here, to improve the input matching a capacitor is placed at the gate of the first MOS device present in cascode topology. The circuit is implemented using 0.18 µm CMOS process. The value of the degenerated inductor is 0.17 nH if capacitor is not present i.e. the circuit is not improved while the value of inductor reduces to 0.5 nH is the circuit is improved. The gain and NF of the circuit with traditional input stage is 24 dB and 0.24 dB while of the modified circuit is 21 dB and 0.39 dB.

A switched LNA used for Bluetooth applications i.e. at 2.4 GHz has been fabricated in [49] using 0.18 µm CMOS process. The switched LNA circuit has CS cascode inductively degenerated topology as the core and for attenuation and switching function has an additional circuitry. The switching logic and attenuation network are the main parts of the switched LNA. Large isolation is provided between input and output so that at all frequency unconditional stability is achieved because the LNA performance should not be influenced by the attenuation path when the circuit is operated in the gain mode. By using the inverter the LNA core is switched off in the attenuation mode. The bypass switch consists of two MOSFETS in the series combination having there gate controlled by the gate voltage. An area of 0.79 mm^2 is required by the device. A gain of 7 dB, NF of 3 dB and attenuation of -17 dB is obtained by the circuit using 1.8 V supply. Also, 7.6 mW power is consumed.

A LNA is designed to be used at 2.4 GHz, using 0.18 µm CMOS technology in [50]. A cascode LNA structure have been used in the LNA design with first amplifier in the CS configuration and second amplifier in the CG configuration and LC network as the load used for tuning the output. The bias circuit consists of diode connected transistor and for the first transistor it generates the bias voltage. The LNA circuit using 1.8 V supply is simulated in Winspice3. A voltage gain of 51 dB and NF of 1.65 dB and power dissipation of 3.15 mW is obtained.

A low voltage LNA amplifier working at 2.4 GHz have been proposed and designed in the [51]. To reduce the voltage, folded cascode architecture is used. The CS stage and CG stage of the cascoded topology is folded into two paths. The RF traps are

also added in the circuit as at DC they act as short circuit and at operating frequency they act as open circuit. LC tank circuit is present at the drain of Cs stage and at the source of the CG stage so that they act as RF trap when they resonate at frequency of operation. Between the two paths a capacitor is added and is called as coupling capacitor as couples RF between the two stages. The LNA requires only 0.6 V supply and is designed using 0.18 µm CMOS technology. The input reflection coefficient is -43 dB, power gain is 13.8 dB, reverse isolation is -36.5, output reflection coefficient is -30.8, NF is 1.56 dB and IIP3 is -2 dBm. The chip size is 1.1 mm x 1.1 mm.

A fully integrated CMOS LNA working at 2.4 GHz is designed in [52]. So, that inductors values are fully integrated and input loss is minimum even if the on chip inductors are used that have low quality factor than off chip inductor. This is achieved by pi-matching the input. Active device sizing method and lossless feedback is also used to achieve low NF and 50 Ω impedance at the input. The LNA core uses cacsode topology with a degenerated inductor at source as the feedback. 0.28 µm CMOS foundry design kit is used to design the LNA circuit. A NF of 3 dB, a voltage gain of 31 dB and input reflection coefficient of -30 dB is obtained along with a power consumption of 10 mW when a supply of 2.5 V is used.

CMOS LNA is designed using CS cascode configuration having a degenerated source inductor which along with the gate inductor which is used to control resonant frequency, is used to achieve input impedance matching. A biasing circuit uses another transistor forming a current mirror with CS amplifier stage in cascode structure for biasing the cascode stage. CS amplifier is used in output stage. A 3.3 V of power supply is used in the circuit designed in 0.25 µm CMOS technology and a current of 5 mA is consumed. Hence, dissipating a power of 16.5 mW. An input reflection coefficient of -13.4 dB, output reflection coefficient of -18.3 dB, gain of 21.63 dB, NF of 1.8 dB and 1 dB compression point is obtained at -19 dBm for 2.4 GHz frequency. Layout of the circuit is formed using Cadence Virtuoso Editing tools and thus, an area of 0.8 mm x 0.6 mm is occupied by the chip [53].

In the paper [54] a CG LNA circuit is designed which at input matching network adds additional degree of freedom and at low power consumption improves the NF. So, a differential CG LNA has been designed that uses g_m technique. To increase the value of transconductance of the transistor, a capacitor in series with inductor is placed at the two differential input stage. Thus, producing series resonance to increase the gain of the LNA. The circuit is designed using 0.18 µm CMOS process and consumes a power of 0.98 mW from a supply of 1 V. The circuit requires a total chip size of 0.98 mm x 1.2 mm and gives a value of -11 dB for input reflection coefficient, 15.5 dB for gain, 5.2 dB for NF and -19 dBm for IIP3.

A two stage LNA is designed using 0.13 µm CMOS process for 2.4 GHz frequency. The LNA consists of a core part and a buffer stage. A self-biased cell is present in the core LNA stage and a 3 bit DAC is used to control its supply voltage, varying from 0.4 V to 0.6 V. Also, between the two transistor's gates a decoupling capacitor

is used to reduce the supply voltage further. The buffer stage is used to provide output impedance matching. A maximum gain of 15.7 dB and a minimum NF of 4.6 dB is obtained at 0.6 V. IIP3 is -12.2 dBm for 0.4 V and -12.6 dBm for 0.5 V. The circuit consumes a power of 60 mW from 0.4 V supply and a chip area of 0.63 mm^2 is required for the circuit [55].

A LNA is designed using 0.13 µm CMOS technology for wireless sensor network application. The designed LNA circuit is of two stage. The first stage consists of cascode topology with degenerated inductor at the source which provides matching of input impedance and high stability. The second stage consists of a CS amplifier which is used for increasing the gain of the system. The load of the first stage is RLC network which act as RF choke and hence, is used to select the output frequency. The load of second stage is an inductor. The supply voltage is 1.2 V. The circuit is simulated in Cadence Spectre RF giving value of input reflection coefficient, output reflection coefficient, gain, NF and IIP3 as -26.9 dB, -20.6 dB, 23.6 dB, 5.6 dB and -1 dBm respectively. Chip area is 0.89 mm x 0.72 mm. Also, a power of 8.1 mW is consumed [56].

A CG LNA is designed using 0.18 µm CMOS process [57]. The proposed LNA consists of two NMOS CG stage transistor and two PMOS CG stage transistors. Two capacitors and large resistors forms CCC topology. PMOS transistors has resistors as load which provide amplified signal which is cross coupled to the gates of NMOS transistors forming g_m boosting topology. The circuit requires 1.8 V power supply and consumes a power of 0.58 mW. It is observe that input reflection coefficient is less than -18 dB, gain is 14.7 dB, NF is 4.8 dB and IIP3 is 2 dBm. An area of 0.62 mm x 0.63 mm is required by the LNA.

A CS cascode inductive degenerated topology using current reuse technique is proposed in [58]. The degenerated inductor along with input inductor is used to achieve input impedance matching. The CS amplifier's output is cascaded to the CG amplifier so as to decrease Miller effect and thus are present in cacsode configuration. Output of CG amplifier goes to another CS amplifier's gate through a capacitor and an inductor is also present between CG amplifier stage and another CS amplifier stage for current reuse. A 0.18 µm CMOS technology is used to design the LNA circuit. A supply of 1.8 V is used and 10.08 mW of power is consumed. The simulated results show that the input matching is less than -10 dB, gain is 26.5 dB, NF is 3.8 dB and IIP3 is -10.3 dB for 2.4 GHz frequency.

A CS inductive degeneration topology using complementary current reuse technique is used in designing of the LNA along with transformer coupled at both the input and the output. On the top of a PMOS amplifier a NMOS amplifier is placed symmetrically so that DC current is shared between them. Inductors are used as load to increase the operating frequency and also to bias NMOS output at supply voltage and PMOS output at the ground. Thus, removing feedback circuit which is used in traditional current reuse technique. A 90 nm CMOs technology is used in fabrication of the LNA and requires a chip size of 1.0 mm x 0.75 mm. 1.2 V power

supply is used in fabrication of the LNA and a power of 3 mW is consumed. The input and output reflection coefficient is less than -10 dB, gain is 13 dB, NF is 1.8 dB and IIP3 is -8.9 dBm [59].

The proposed LNA uses CS inductive degeneration topology for 2.4 GHz frequency. The LNA circuit uses transformer as the load. The circuit is designed using 0.18 µm technology. The simulated graph shows that the value of input reflection coefficient is -2.625 dB, reverse isolation is -57.166 dB, gain is 15.71 dB, output reflection coefficient is -47.36 dB, NF is 2.447 dB and IIP3 is -20 dBm. A power of 6.5 mW is consumed from a supply of 1.8 V [60].

TABLE 3.7 COMPARISON OF LNA AT 2.4 GHZ

	[39]/ [40]	[41]	[42]	[43]	[44]		[45]/ [46]	[47]	[48]
Technology (µm)	0.5	0.35	0.25	0.35	0.25		0.18	0.18	0.18
Supply (V)	3	2	3.3	2			1.2	1	-
	19	21	20	19.9	High gain mode	Low noise mode	12.9	23	21
S_{21} (dB)					14.7	-14.2			
NF (dB)	2.4	1.24	2.4	2.5	2.88	14.2	0.76	3.8	0.13
IIP3 (dBm)	-	-		2	-1.5	19	-	-9.1	-

	[49]	[50]	[51]	[52]	[53]	[54]	[55]
Technology (µm)	0.18	0.18	0.18	0.28	0.25	0.18	0.13
Supply (V)	1.8	1.8	0.6	2.5	3.3	1	0.4-0.6
S_{21} (dB)	7	51	13.8	31	21.63	15.5	15.7 @ 0.6 V
NF (dB)			1.56	3	1.8	5.2	4.6 @ 0.6 V
IIP3 (dBm)	3	1.65	-2	-	-	-19	-12.2 @ 0.4 V

	[56]	[57]	[58]	[59]	[60]
Technology (µm)	0.13	0.18	0.18	90 nm	0.18
Supply (V)	1.2	1.8	1.8	1.2	1.8
S_{21} (dB)	23.6	14.7	26.5	13	15.71
NF (dB)	5.6	4.8	3.8	1.8	2.447
IIP3 (dBm)	-1	2	-10.3	-8.9	-20

3.1.8 5 GHz/Wireless LAN

A 5 GHz LNA circuit is designed using 0.25 µm CMOS process in [61]. The LNA circuit utilizes differential design formed by pair of single stage cascode amplifiers. The amplifier in CS configuration in cascode topology has an inductor is that is used as degenerated inductor at source so as to increase linearity. At the gates of the CS amplifiers input signal is applied through inductor. This inductor along with degenerated source inductor forms input matching. Moreover, inductor is also used as load at the drain of CG amplifier present in cascode topology which along with output capacitors form output matching. The gates of CG amplifiers when connected to 3 V supply is used to bias the circuit. The LNA circuit area on chip is 830 µm x 390 µm. A gain and NF is 16.6 dB and 2.38 dB respectively is obtained if power dissipation is 48 mW and, is 14.4 dB and 2.8 dB if power dissipation is 24 mW. For a power dissipation as low as 12 mW power gain is 11.6 dB and NF is 3.5 dB. The circuit also provides reverse isolation of -26 dB and IIP3 of -1.5 dBm.

A 5 GHz LNA to be used in wireless LAN receiver has been fabricated in the paper [62] using 0.18 µm CMOS technology. The proposed LNA circuit consists of an amplification stage followed by an output buffer. The amplification stages utilizes cascode topology that uses two n-channel MOSFET, of which one of the NMOS is in CS stage while other NMOS is in CG stage. The input is applied at the gate of the CS stage and a source degenerated inductor formed by parallel combination of the three bond wires is connected at the source of the CS stage. The output buffer is used to convert amplified signal to differential. Also, a VGA cell is present in parallel to LNA input so as to adjust gain to increase the dynamic range. The simulated S_{21} parameter of LNA is 25 dB, NF is 1.5 dB and the amplification stage consumes a current of 6 mA from 1.5 V.

A LNA using FDC has been designed for 5 GHz, using 0.25 µm CMOS technology in [63]. The original LNA circuit is same as conventional cascode LNA circuit with load as inductor. Two large resistive dividers are used as couplers for simplification of the circuit and noise minimization while unit gain CS amplifier having inductor

as load is used as time delayers. So, for cancellation performance to be best the delay constant and coupler coefficient should be optimized. Also, a multiplier is formed by two MOS namely M1 and M2. The output of the original LNA is coupled to M2 acting as source follower while the M1 is in saturation and coupled signal is fed into it. The simulation is carried out in Agilent ADS. A power gain of 17.4 dB, NF of 1.22 dB, reverse isolation of -32 dB, input reflection coefficient and output reflection coefficient both of -23 dB is provided by the whole LNA. Without degrading any noise and gain the IIP3 is boosted from 5 dBm to 21 dBm.

A RF CMOS LNA performance at 5 GHz has been analyzed using 90 nm technology for designing. The LNA architecture uses a CS cascode topology with source degenerated inductor. The input signal is applied to the gate of CS amplifier in cascode topology through inductor and inductor is also used as load. A gain of 13 dB along with NF of 2.7 dB is obtained by the circuit using 1.2 V power supply and consuming power of 9.7 mW [64].

The LNA is proposed for 5 GHz frequency in [64] designed using 90 nm CMOS process. The proposed LNA design consists of a cascoded amplifier using gm enhanced technique which is followed by feedback transistor in source follower configuration. A capacitor is used to DC block the feedback resistor. Another source follower is used which form transconductance with the mixer. A 42 mW of power is consumed from 2.7 V power supply. The simulation results shows that the S11, gain, NF and IIP3 is -13 dB, 25 dB, 2 dB and -14 dBm respectively [65].

A differential LNA having variable gain have been designed for WLAN application. The core of LNA circuit is cascoded CS inductive degenerated differential topology. Another set of transistors, known as cascoded transistor is cascoded with the input stage and forms CG stage. They are also implemented in differential pair and are present between input transconductor and the load giving rise to variable gain characteristic. The circuit is designed using 0.18 µm technology and 1.5 V supply. The simulation results of the circuit simulated in Cadence Spectre RF is -11.8 dB input reflection coefficient, -17.75 dB reverse isolation, 12.34 dB gain, 3.98 dB NF and -1.24 dBm IIP3 for high gain mode and have -25 dB input reflection coefficient, -23.9 dB reverse isolation, 6 dB gain, 4.25 dB NF and 1.71 dBm IIP3 for low gain mode. LNA circuit requires an area of 1.3 mm x 1.9 mm [66].

In [67] LNA using ultra low voltage supply of 0.6 V is designed using 0.13 µm technology. The LNA utilizes CS amplifier along with darlington pair. Darlingtion pair is implemented using resistive degeneration as improves linearity and the noise. The gate source voltage of the common source stage is provided by the quiescent current of darlington pair transistor, flowing through the degenerated resistor. The circuit is simulated in spectre giving value of input reflection coefficient less than -10 dB, voltage gain of 25 dB, minimum NF of 1.8 dB and IIP3 of 10 dBm while consuming a power of 0.85 mW.

TABLE 3.8 COMPARISON OF LNA AT 5 GHZ

	[61]	[62]	[63]	[64]	[65]	[66]		[67]
Technology (µm)	0.25	0.18	0.25	90 nm	90 nm	0.18		0.13
Supply (V)	-	1.5		1.2	2.7	1.5		0.6
	16.6	25	17.4	13	25	High gain mode	Low gain mode	25
S_{21} (dB)						12.34	6	
NF (dB)	2.38	1.5	1.22	2.7	2	3.98	4.25	1.8
IIP3 (dBm)	-1.5		21	-	-14	-1.24	1.71	10

3.1.9 5.2 GHz

A 5.2 GHz LNA is implemented using interstage series technique in [68]. The LNA circuit consists of two stages, the stage 1 consists of a CS amplifier (M1) and a diode connected transistor (M4) which is used for voltage drop and to decrease the quality factor of the inductor so as to increase stability. The stage 2, uses the cascode architecture consisting of two transistor and a degenerated inductor to improve the linearity. The inductor used as load and output capacitor is used for output matching. An inductor is present between the two stages thus acting as interstage inductor. The circuit is designed using 0.18 µm CMOS technology and uses 2.7 V supply. A gain of 18.9 dB, NF of 1.7 dB and OIP3 of 12.9 dBm is obtained. Also, a power of 22.3 mW is consumed.

A LNA having two stage which uses current reuse technology and interstage series resonance is designed in [69]. A CS amplifier and a cascode stage is used having an inductor between them. Another inductor is present as a load and uses capacitive interstage coupling having an inductor in series. The value of inductor and capacitor are adjusted for series resonance. The interstage series resonance technique is used as is less affected by substrate effect and high gain is provided along with less stability issues. The LNA circuit is designed using 0.35 µm CMOS process with a power supply of 3.3 V for 5.2 GHz. A power gain of 19.3 dB is observed along with NF of 2.45. Also, OIP3 of 13.2 dB is observed while consuming a current of 8 mA.

A 5.2 GHz LNA is designed and implemented using 0.25 µm technology [70]. A common source inductively degenerated topology is used. CS cascode transistor having inductor at the source of value 0.516 nH with quality factor of 10.5 is used so that the gate drain capacitance effect of CG transistor is reduced and also, interaction between tuned output and tuned input is reduced. Resistors are used to

form the bias circuit. The circuit is designed using ADS. The simulated value of S_{11}, S_{12}, S_{21}, S_{22} and NF is -10.04 dB, -25.2 dB, 11.04 dB, -11.05 dB and 3.249 dB.

TABLE 3.9 COMPARISON OF LNA AT 5.2 GHZ

	[68]	[69]	[70]
Technology (µm)	0.18	0.35	0.25
Supply (V)	2.7	3.3	-
S_{21} (dB)	18.9	19.3	11.04
NF (dB)	1.7	2.45	3.249
OIP3 (dBm)	12.9	13.2	-

3.1.10 5.8 GHz

A 5.8 GHz LNA that can control gain and frequency is designed in [71] using 0.18 µm CMOS technology. The proposed circuit uses folded cascode configuration that uses NMOS and PMOS for reduction of supply voltage. Here, gate voltage of PMOS is controlled to attain gain control i.e. adjusting overall gain of the LNA without affecting its input noise and input matching which depends on NMOS. Moreover, varactor is added at resonant tank circuit for achieving the frequency tuning. S_{11}, S_{21}, S_{22}, NF, power dissipation and gain tuning are -5.3 dB, 13.2 dB, -10.3 dB, 2.5 dB, 22.2 mW and 12.8 dB respectively for a supply of 1V and are -7.1 dB, 7 dB, -12.3 dB, 2.68 dB, 12.5 mW and 7 dB respectively for 0.7 V supply. The frequency tuning for both 1 V and 0.7 V supply is 360 MHz. Also, the total chip area is 0.9 mm x 0.8 mm including bonding pads.

A two stage LNA circuit is designed in [72] using 0.35 µm 1P4M (one poly layer for gate and four metal layers for interconnection) CMOS technology. The first stage is a CS architecture with degenerated inductor at its source while the second stage is a CG architecture. The two stages have an inductor between them. The voltage is applied to the gate of CS amplifier through inductor. The value of input reflection coefficient is -11dB, gain is 7.2 dB, output reflection coefficient is -17dB, NF is 3.2 dB and IIP3 is 6.7 dB. The circuit uses 1.3 V and dissipates a power of 20 mW. The area required for the circuit without on chip pads is 0.63 mm x 0.46 mm.

Cascode architecture is employed in designing of the LNA at 5.8 GHz. The cascode configuration uses two transistor along with degenerated inductor and the gate of these transistors are connected to gate of other transistors that are also in cascode. The circuit design uses 1.5 V power supply and is designed using 0.18 µm CMOS process. A chip of area 0.9 mm^2 is used. When the power dissipation is 15 mW then the minimum NF is 1.5 dB and when the power dissipation is 8 mW then the

minimum NF is 1.8 dB. However, if power dissipation is 15 mW then the gain is 28 dB if LNA is followed by super source follower buffer and is 14 dB if output is matched to 50 Ω impedance while if the power dissipation is 8 mW then the gain is 23 dB if LNA is followed by supreme source follower buffer and is 13 dB if output is matched to 50 Ω impedance [73].

TABLE 3.10 COMPARISON OF LNA AT 5.8 GHZ

	[71]		[72]	[73]
Technology (µm)	0.18		0.35	0.18
Supply (V)	0.7	1	1.3	1.5
S_{21} (dB)	7	13.2	7.2	28
NF (dB)	2.68	2.5	3.2	1.5

3.1.11 24 GHz/ K Band

A simple topology is chosen to design the LNA in 0.18 µm technology for 24GHz. The transistor uses three stages of common stage amplifier with inductive source degeneration. In the first stage of the circuit topology the transistor is scaled and the gate inductance is used for shifting of noise optimizing impedance to 50 Ω. Each stage output is loaded using high pass combination of inductor and capacitor so as to increase the gain and obtain parallel resonance. An input return loss of 11 dB, output return loss of 22 dB, reverse isolation of -33.18 dB, gain of 12.78 dB, NF of 5.6 dB and IIP3 of 2.04 dBm is obtained. Also, a current of 30 mA is consumed from 1.8 V supply. The chip size is 1.05 x 0.7 mm^2 [74][75].

Cascoded two stage CS architecture is used in designing of LNA using 0.18 µm technology and to be operated at 24 GHz [76]. Here, for the noise, the first stage is designed and for the gain, the second stage is designed. The CS amplifier has degenerated inductor which is connected to the source and series combination of inductor and capacitor is used as load. A high pass combination of inductor and capacitor is used to as the interstage network. The simulated design has input return loss of 18 dB, output return loss of 23 dB, gain of 13.1 dB, NF of 3.9 dB and IIP3 of -12.3 dBm, a supply voltage of 1 V is used for operation consuming a power of 14 mW. 0.57 x 0.6 mm2 is the chip area.

TABLE 3.11 COMPARISON OF LNA AT 24 GHZ

	[74]/[75]	[76]
Technology (µm)	0.18	0.18
Supply (V)	1.8	1
S_{21} (dB)	12.78	13.1
NF (dB)	5.6	3.9
IIP3 (dBm)	2.04	-12.3

3.2 Ultra-wideband LNA

The ultra-wide band (UWB) has been approved in US by the Federal Communication Commission (FCC), ranging from 3.1-10.6 GHz, for use for commercial applications recently [77]. In the recent years, significant interest has been developed in Ultra-wideband (UWB) technology for wireless communication, since a wide frequency band spectrum, transmission of data at very low power, high data rate and low cost is provided by it provides [78]. So, majority of LNA topologies for UWB is defined for frequency ranging from 3.1-10.6 GHz.

The LNA for UWB has been designed in the paper [79] using 0.13 µm CMOS technology. The proposed LNA circuit is divided into two stages and three sub-circuits, the first stage is CG as its input impedance is $1/g_m$ so as to achieve the input impedance at 50 Ω. The second stage is CS amplifier stage. A matching circuit is present between the first and the second. The gain is of value 14.73 dB, S_{11} is below -10 dB, NF is less than 4 dB.

A two stage LNA based inverter is designed in [80] using 0.18 µm CMOS technology. The NMOS transistor reuses the current of PMOS transistor. Therefore, for NMOS additional driving current is not required. Pi-matching is used to achieve input impedance matching. The LNA circuit uses 1.8 V power supply and consumes a power of 18 mW. The input reflection coefficient value is less than -10.7 dB, gain is 13.7 dB, NF is 2.3 dB and IIP3 is -0.2 dBm. The power dissipated is 18 mW. The chip area is 0.39 mm^2.

Two stage cascode LNA topology with degenerated inductor is designed using 0.18 µm process. Between the CS and CG device an inductor is present The CG amplifier uses a resistor for feedback and hence, is called current reuse topology. Three section band pass Chebyshev filter is used at input to achieve wideband input matching and flat gain. The simulated results are 20 dB maximum gain, -28 dB input return loss, -25 dB reverse isolation, -9.7 dB output return loss, NF ranging from 2.89 to 6.5 dB and IIP3 of 10 dBm. The power consumed is 12 mW from 1.8 V supply [81].

A LNA to be operated from 3.1 GHz to 10.6 GHz is designed using 0.18 µm process. The first stage consists of a CS transistor and CG transistor in cascode configuration having a degenerated inductor and an inductor between the two amplifier stages. Also, shunt

feedback topology is used in the first stage. It is followed by two transistor in cascode of which one transistor is used as current source to bias the other transistor. The circuit is simulated in Agilent ADS. Gain of 19.982 dB, NF of 1.27 dB, input reflection coefficient of -31.670 dB, output return loss of -7.449 dB is obtained [82].

A noise cancelling LNA is designed in [83]. The LNA designed has two stage where the first stage or the input stage uses a current reuse circuit to save power and noise cancelling topology is utilized in the second stage of the LNA. The CMOS LNA is designed using TSMC 0.18 µm process and is simulated using Agilent ADS tool. The input and output return loss is less than -10 dB, gain is 15.33 dB, NF is 2.65 dB and IIP3 is -5.5 dB. The LNA circuit using a voltage of 1.3 V and dissipates a power of 9.1 mW.

A CS amplifier using inductor for degeneration at source is present at the first stage of the LNA and at the second stage a CS amplifier is present. At the gate of the two amplifier two series peaking inductor is used. Resistive shunt shunt feedback is applied to the first stage. A supply of 0.8 V is used in the circuit and a current of 11 mA is consumed. The gain of 13.1 dB, reverse isolation of -25 dB, input return loss of less than -10 dB and NF of 3.25 dB is achieved. The circuit uses a chip area of 0.6 mm x 0.75 mm [84].

A 90 nm CMOS low noise amplifier is designed in paper [85]. An inductively degenerated inverter cell is used as the first stage of the low noise amplifier design to operate over large bandwidth having high pass filter at the input to obtain low value of input reflection coefficient and desired low cutoff characteristics. The self-biased resistive shunt shunt feedback amplifier is present is second stage to decrease the consumption of power. The self forward bias technique is used to bias the first stage to achieve low power consumption goal. The simulated results shows that the input reflection coefficient is less than -10 dB, gain is 13.9 dB, NF is 1.35 dB and IIP3 is -3 dBm. A power of 13.5 mW is consumed from 0.9 power supply.

TABLE 3.12 COMPARISON OF LNA FOR 3.1-10.6 GHZ

	[79]	[80]	[81]	[82]	[83]	[84]	[85]
Technology (µm)	0.13	0.18	0.18	0.18	0.18	0.18	90 nm
Supply (V)		1.8			1.3	0.8	0.9
S_{21} (dB)	14.73	13.7	20	19.982	15.33	13.1	13.9±1.42
NF (dB)	4	2.3	2.89-6.5	1.27	2.65	3.25	1.35
IIP3 (dBm)	-	-0.2	10	-	-5.5	-	-3

Chapter-4

EXPERIMENTAL WORK

4.1 Cascode Common Source LNA topology with FDC

4.1.1 Circuit Design

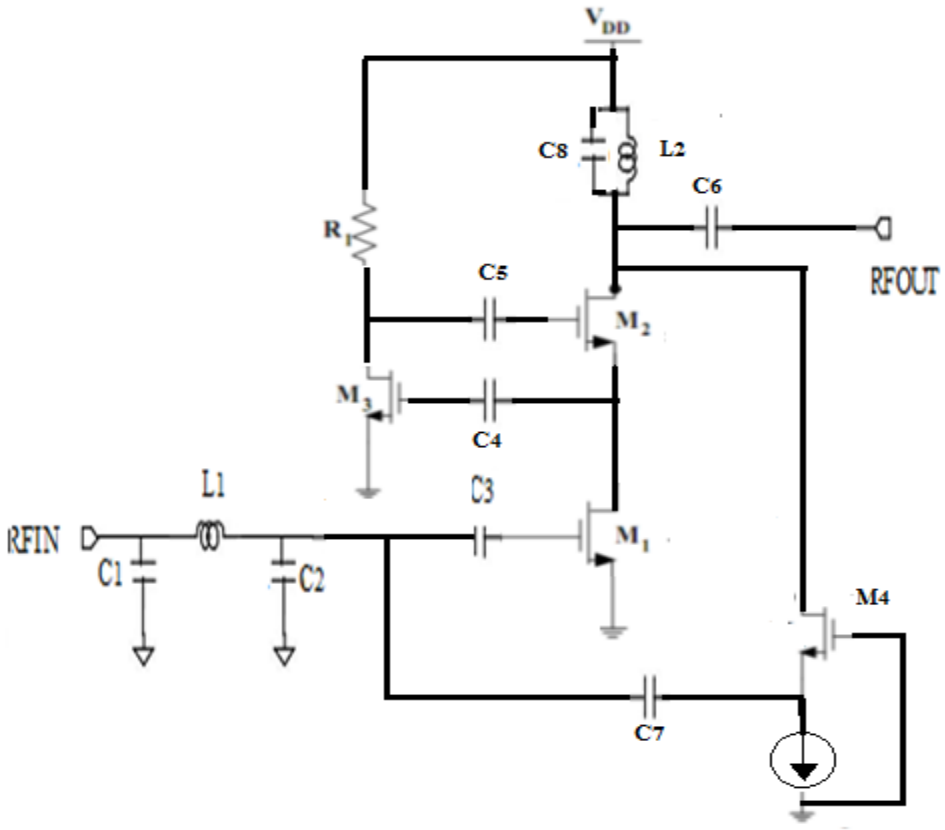

Fig 4.1 Proposed Cascode Common Source CMOS LNA with FDC

The M1 transistor is used as common source (CS) stage; cascode structure is formed by M1 and M2. Gate of M3 and drain of M1 are connected and M3 transistor's output is given to base of M2; for boosting the gain by increasing the drain resistance of M2. M3 and R1 form another CS amplifier. To improve input third order intercept point (IIP3), M4 transistor is used in common gate (CG) mode as an auxiliary transistor. C8 and L2 are used as load and C1, C2, and L1 are forming pi -matching network.

The input capacitance is increased and because of Miller effect, the input and output terminals capacitance is amplified in the input stage of CS, hence reducing the gain. A CG transistor (M2) is inserted at the output of M1 as a current buffer, forming a cascode, to outdo this problem. This cascode configuration also increases the bandwidth of LNA. In the feed forward path, M4 acts as an auxiliary amplifier and nonlinear current is generated, and at the drain of M2, subtracts the current of M2. Therefore this is a single-ended LNA. At the drain of M2, main amplifier (M1, M2) and auxiliary amplifier (M4) currents are added in 180º. So, at the output, currents of the auxiliary amplifier and the main amplifier subtract from each other. Although the linearity is improved, but the gain is decreased. Hence, M3 is used to boost the gain.

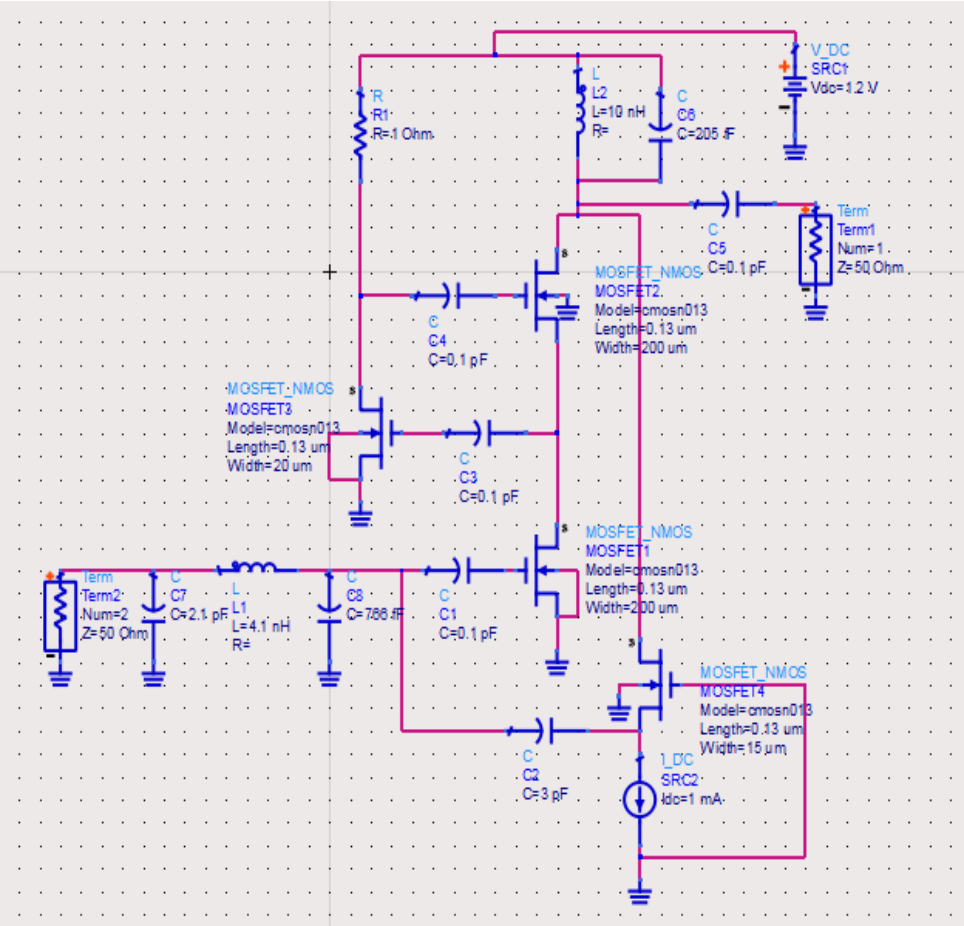

Fig. 4.2 Schematic of Proposed Cascode Common Source CMOS LNA with FDC in ADS

4.1.2 Simulation and results

Simulations of the LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S_{21}) of 10.976 dB as shown in figure 4.5. The input reflection coefficient (S_{11}) is -5.562 dB as shown in figure 4.3 and the output reflection coefficient (S_{22}) is -8.707 dB as shown in figure 4.6. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S_{12}) as shown in figure 4.4 is -22.063 dB and a minimum noise figure of 10.26 dB is obtained as shown in figure 4.7. The simulated IIP3 result is shown in figure 4.8 and IIP3 of 17.0 dBm is obtained. From the result, it can be concluded that very high gain and moderate linearity have been achieved.

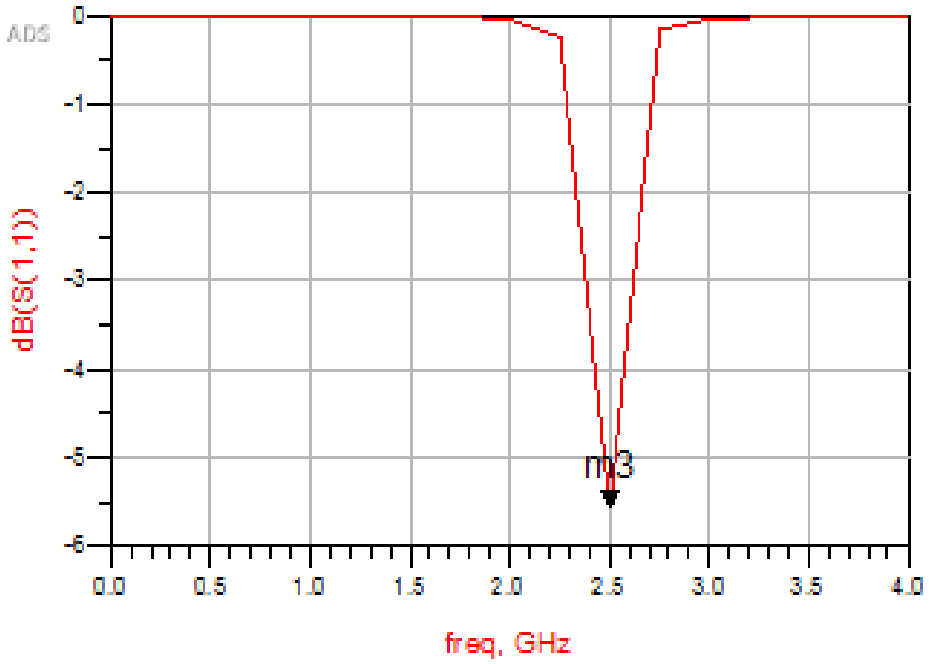

Fig. 4.3 Input return loss (S_{11})

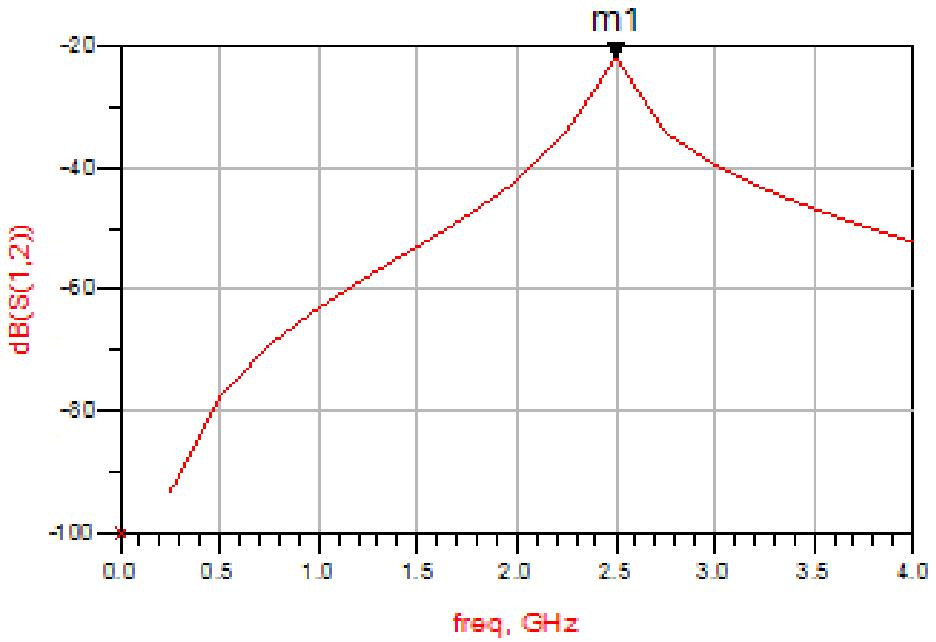

Fig. 1.4 Reverse Isolation (S_{12})

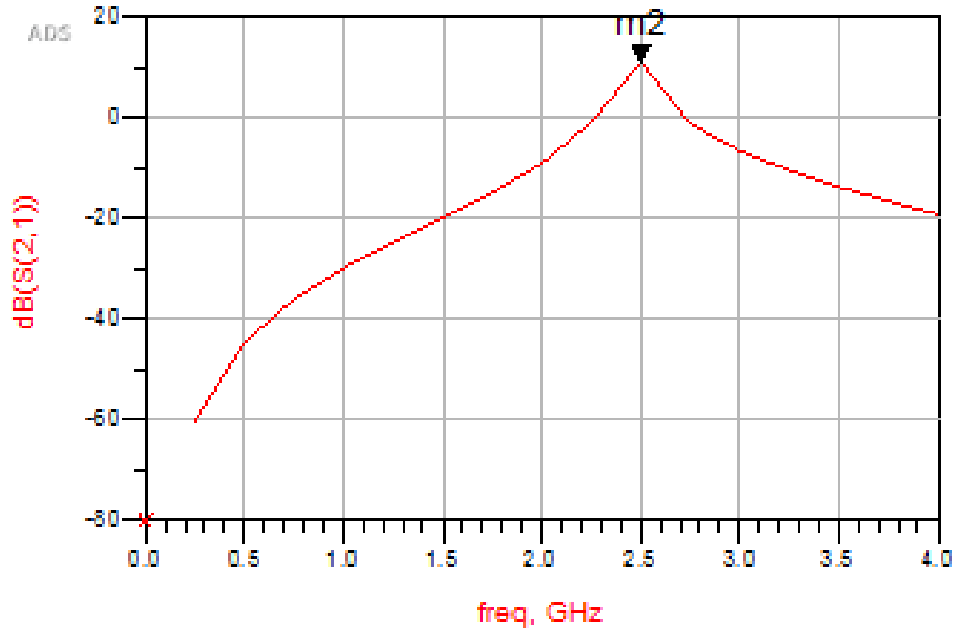

Fig. 4.2. Forward gain (S_{22})

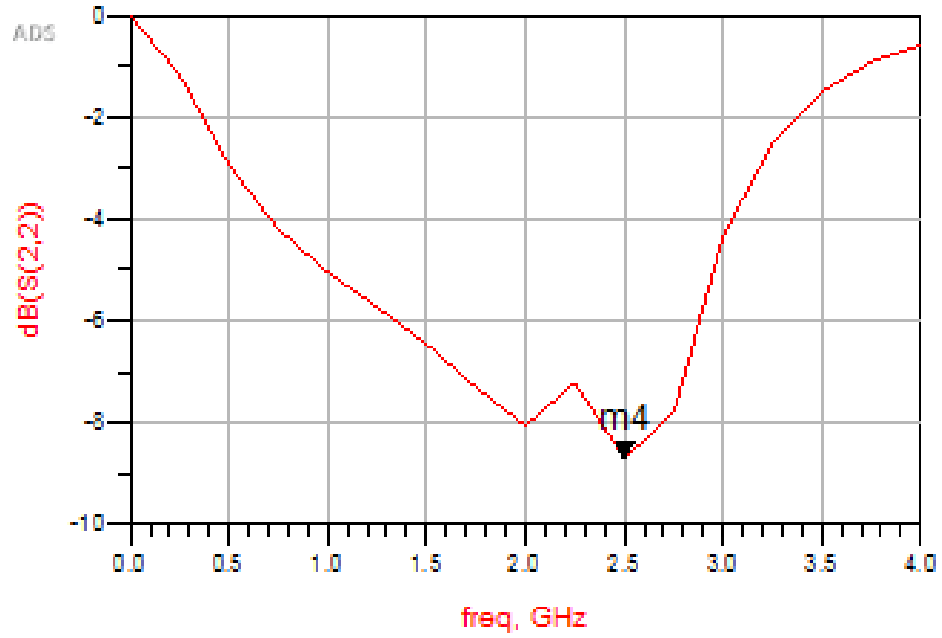

Fig. 4.3. Output reflection coefficient (S_{22})

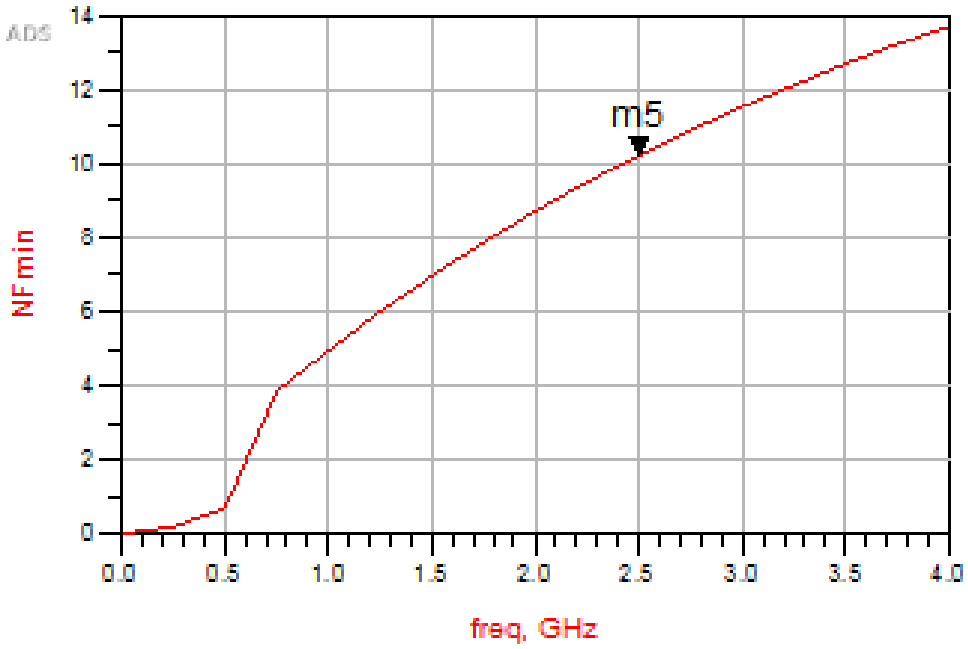

Fig. 4.4 Noise figure

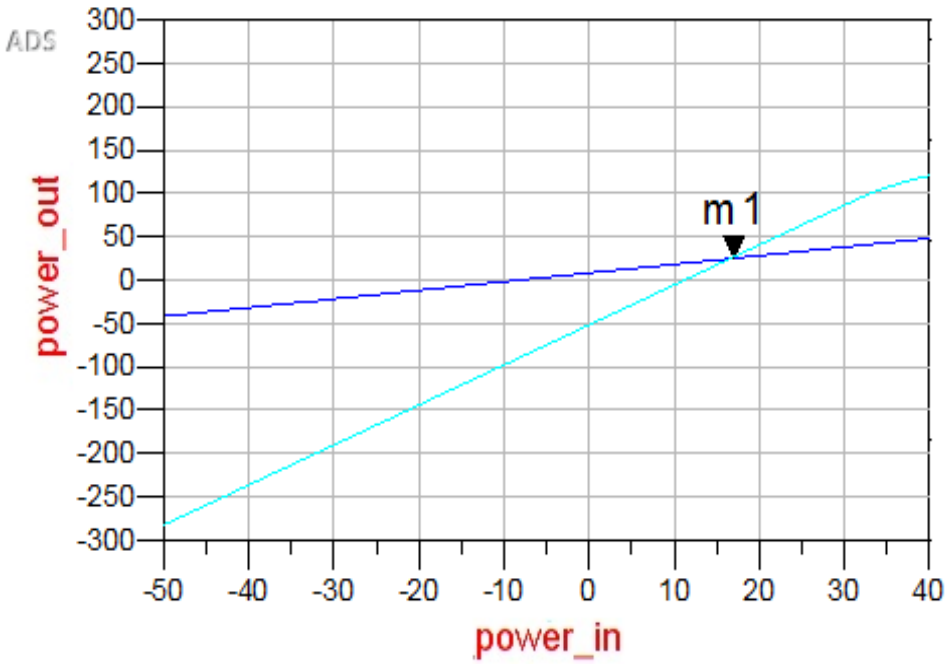
ADS
300
250
200
150
100
50
0
-50
-100
-150
-200
-250
-300
power_out
m1
-50
-40
-30
-20
-10
0
10
20
30
40
power_in

Fig. 4.5. IIP3

4.2 Cascode Common Source Inductive Degenerated LNA topology

4.2.1 Circuit Design

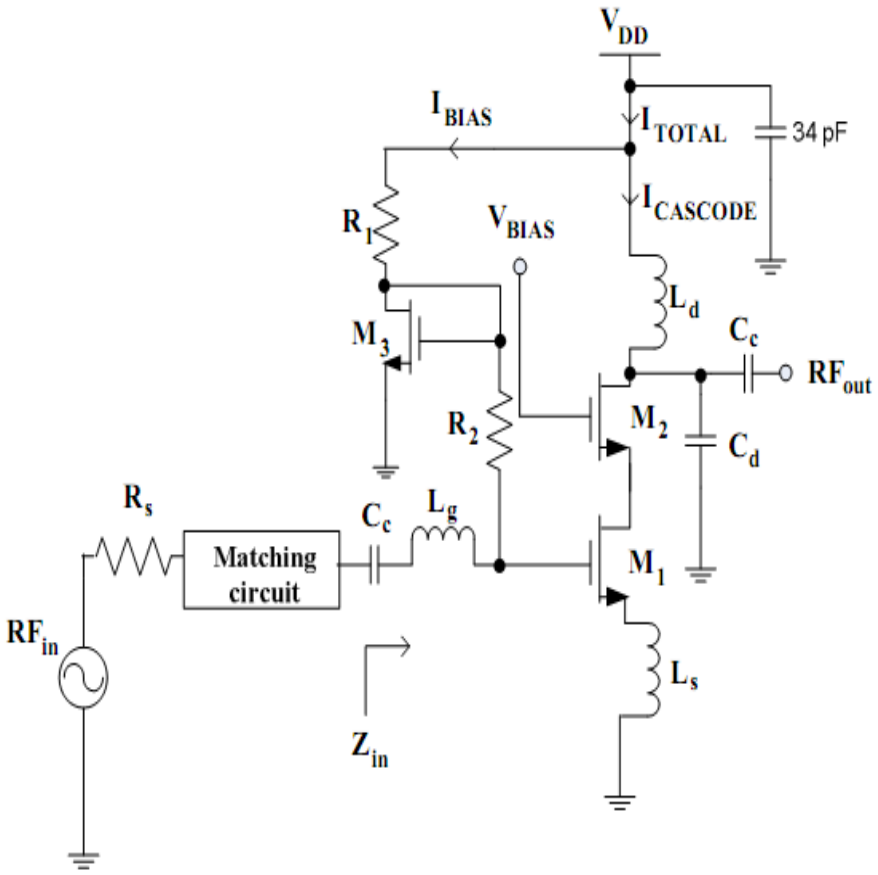

Fig. 4.9 Proposed Cascode Common Source Inductively-Degenerated CMOS LNA

A current mirror circuit is formed by M3 and R1. The input signal is enforced into the input of LNA because the signal path is isolated from the biasing circuit by M1. If the value of R2 is not greater than the input impedance of the stage before it, then the R2 value is critical. M3 is the biasing transistor in the circuit which forms current mirror with M1. To avoid heavy current consumption, the W/L ratio of M3 should not be large.

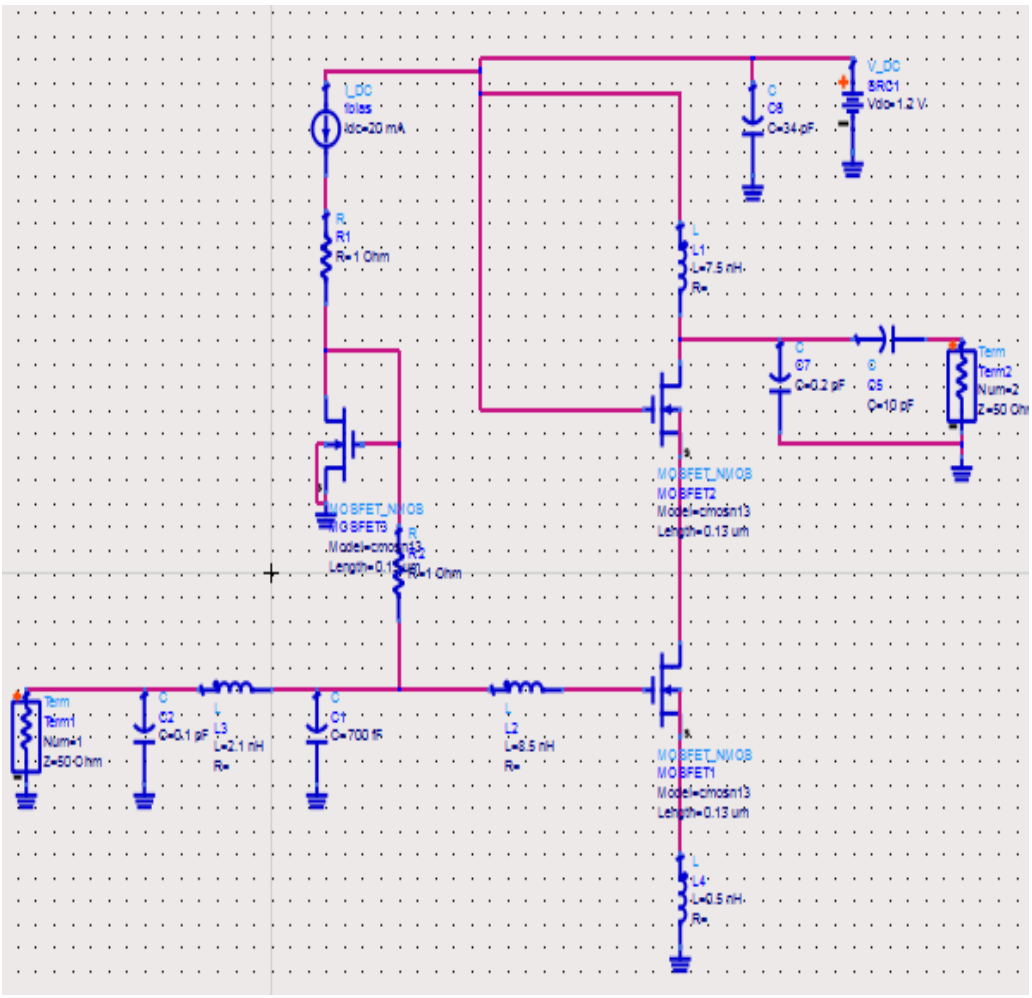

Fig. 4.10. Schematic of proposed Cascode Common Source Inductively degenerated LNA in ADS

4.2.2 Simulation and Results

Simulations of the LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S_{21}) of 24.227 dB as shown in figure 4.13. To make the input matching impedance (Z_{in}) equal to 50 Ω, Cgs and gm are selected properly. The input reflection coefficient (S_{11}) is -7.375 dB as shown in figure 4.11 and the output reflection coefficient (S_{22}) is -0.28 dB as shown in figure 4.14. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S_{12}) as shown in figure 4.12 is -41.478 dB and a minimum noise figure of 2.109 dB is obtained as shown in figure 4.15. The simulated IIP3 result is shown in figure 4.16 and IIP3 of 4 dBm is obtained. From the result, it can be concluded that very high gain and moderate linearity have been achieved.

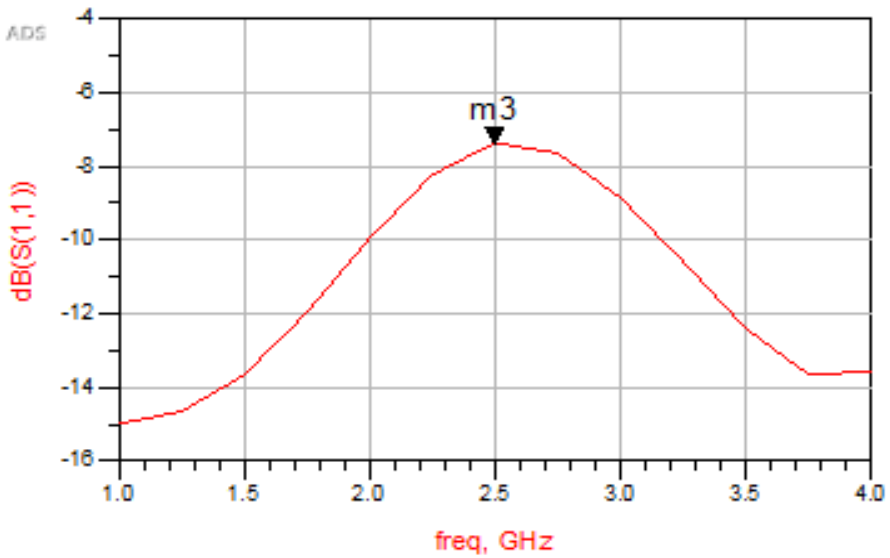

Fig. 4.11 Input Reflection Coefficient (S_{11})

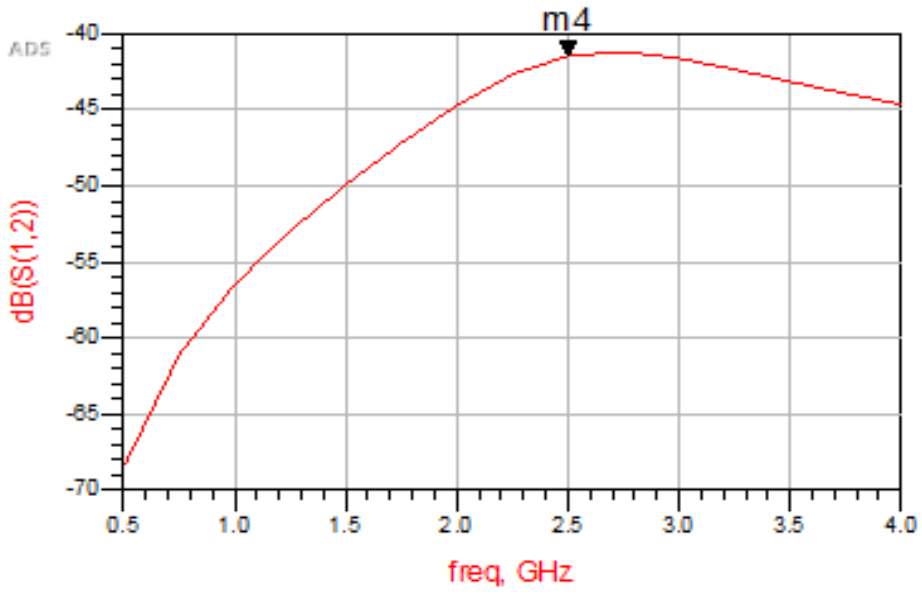

Fig. 4.12 Reverse Isolation (S_{12})

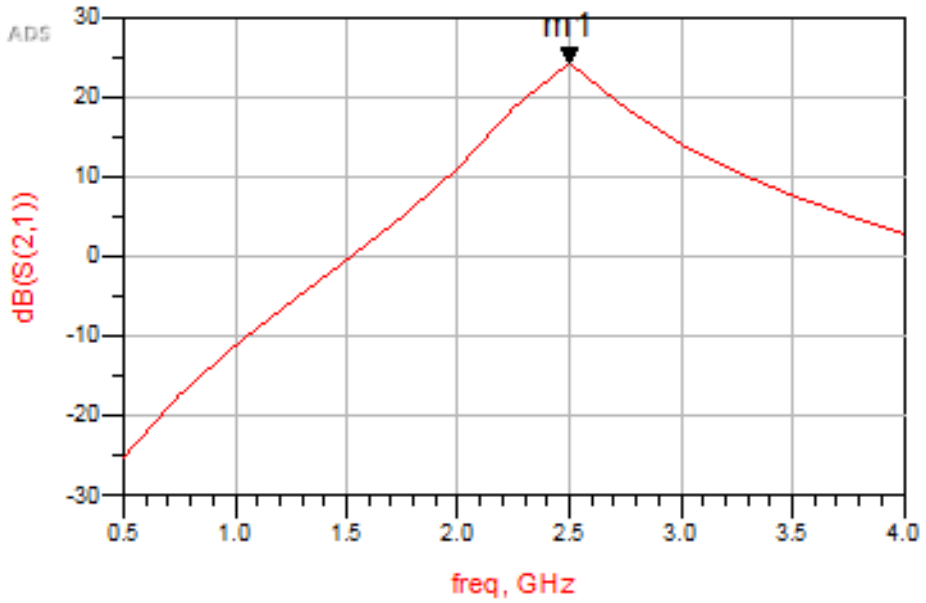

Fig. 4.13 Forward Gain (S_{21})

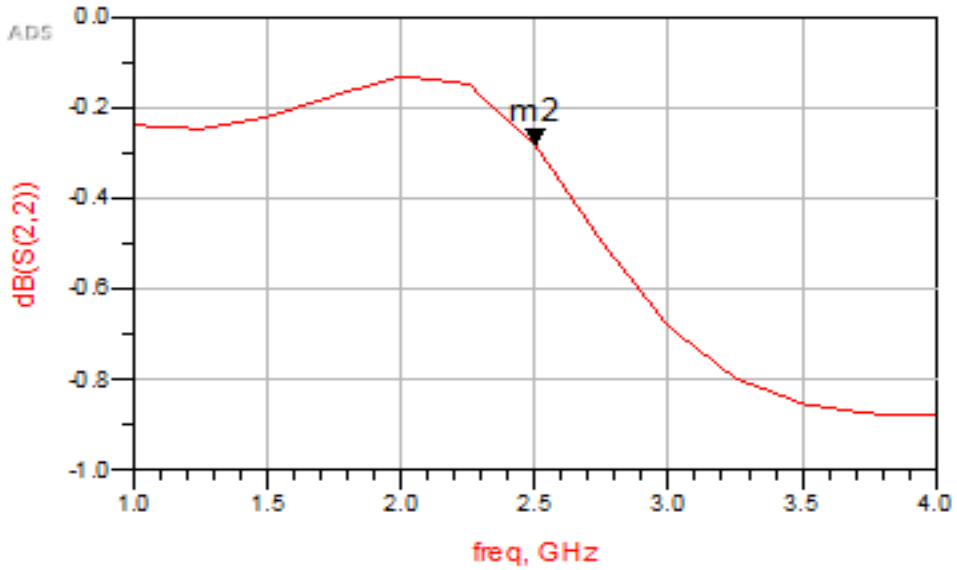

Fig. 4.14 Output Reflection Coefficient (S_{22})

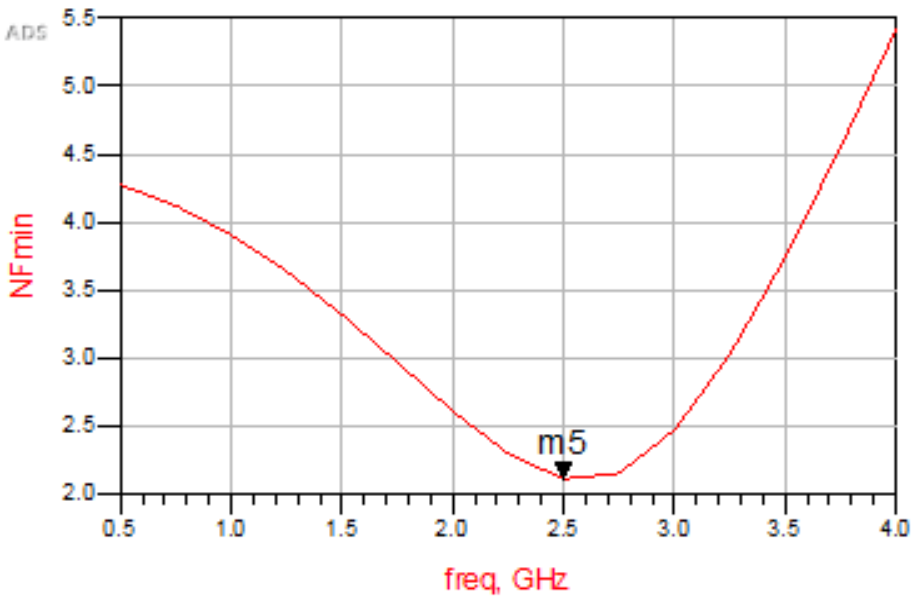

Fig. 4.15 Noise Figure (NF)

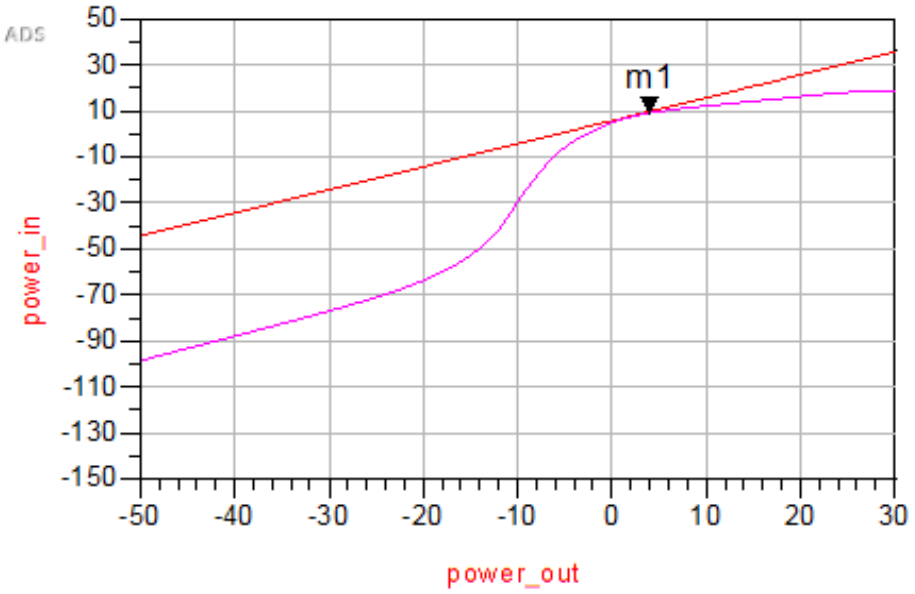

Fig. 4.16. IIP3

4.3 Cascode Common Source inductive degenerated LNA topology with FDC

4.2.3 Circuit Design

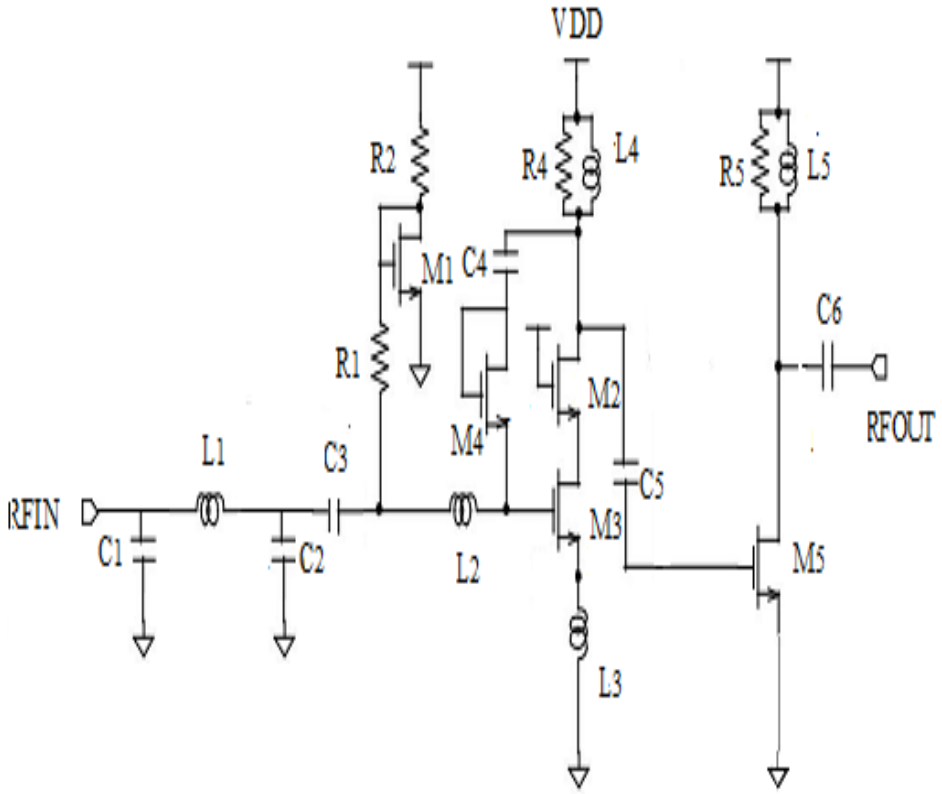

Fig. 4.17 Proposed Cascode Common Source Inductively-Degenerated CMOS LNA with FDC

Figure 4.19 presents the proposed LNA having basic cascode structure comprising of M2 and M3. However, due to capacitance amplification between the input and output terminals, the equivalent input capacitance of an inverting voltage amplifier increases. The main reason for the low gain is Miller effect. A common gate transistor (M2) is used as a current buffer at the output of M3 to overcome this problem. Further, R4 and L4 serve as cascode stage (M2-M3) load. The feed-forward distortion cancellation is provided by transistor M4 and capacitor C4, to improve linearity. To maintain DC voltage at the drain of M2, C4 is used. So, basically C4 is a blocking capacitor. Pi-matching network is used to obtain input impedance matching while R5, L5 and C6 are used to obtain output matching. The M5 transistor is a common source stage which along with the load facilitates output matching and also increases the gain of the LNA. R5-L5 serve as the load M5. The schematic of the proposed circuit in ADS is shown in figure 4.20.

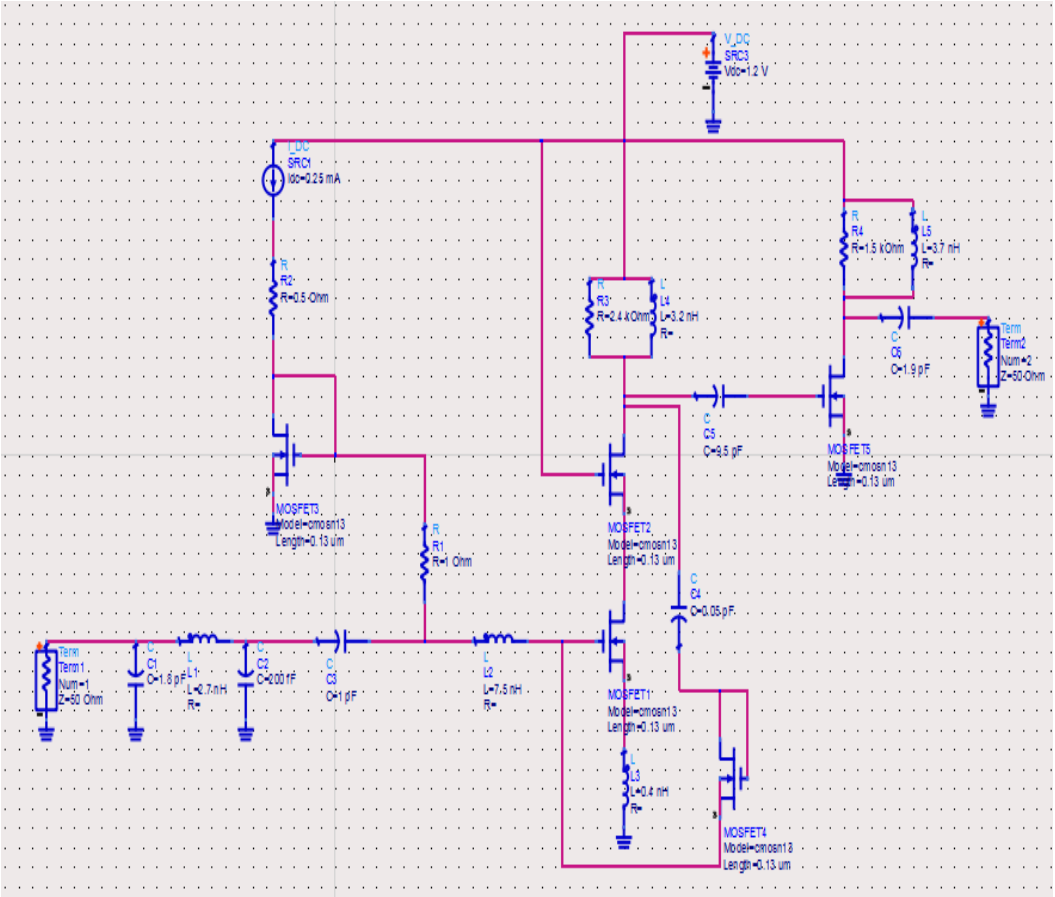

Fig. 4.18 Schematic of proposed Cascode Common Source Inductively Degenerated LNA with FDC in ADS

4.2.4 Simulation and Results

Simulations of the LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S_{21}) of 23.023 dB as shown in figure 4.21. The input reflection coefficient (S_{11}) is -9.403 dB as shown in figure 4.19 and the output reflection coefficient (S_{22}) is -4.730 dB as shown in figure 4.22. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S_{12}) as shown in figure 4.20 is –21.732 dB and a minimum noise figure of 0.988 dB is obtained as shown in figure 4.23. The simulated IIP3 result is shown in figure 4.24, and IIP3 of 14 dBm is obtained. From the result, it can be concluded that very high gain and a high linearity with low noise figure have been achieved.

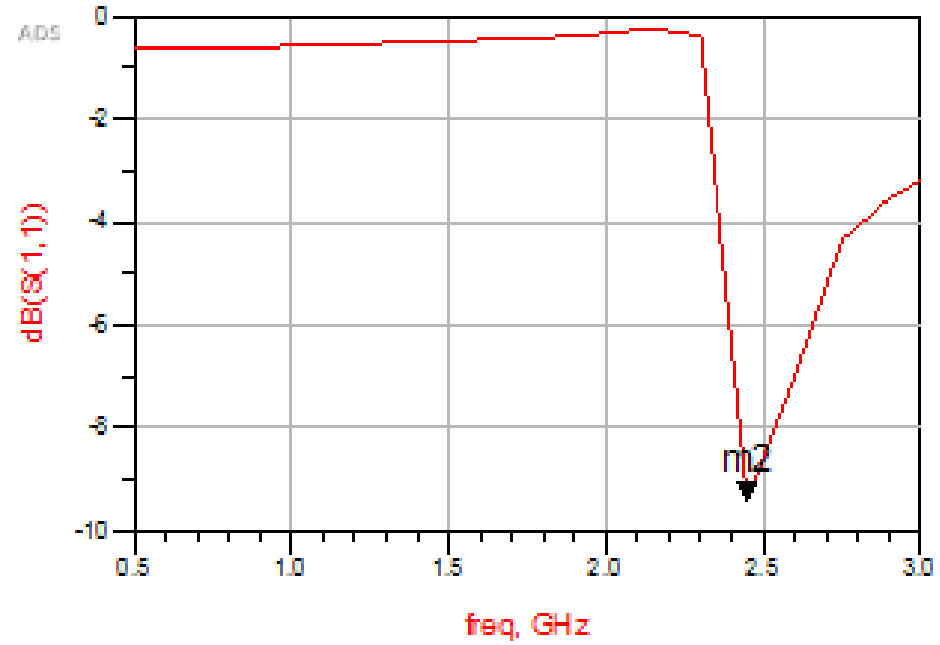

Fig. 4.19 Input Reflection Coefficient (S_{11})

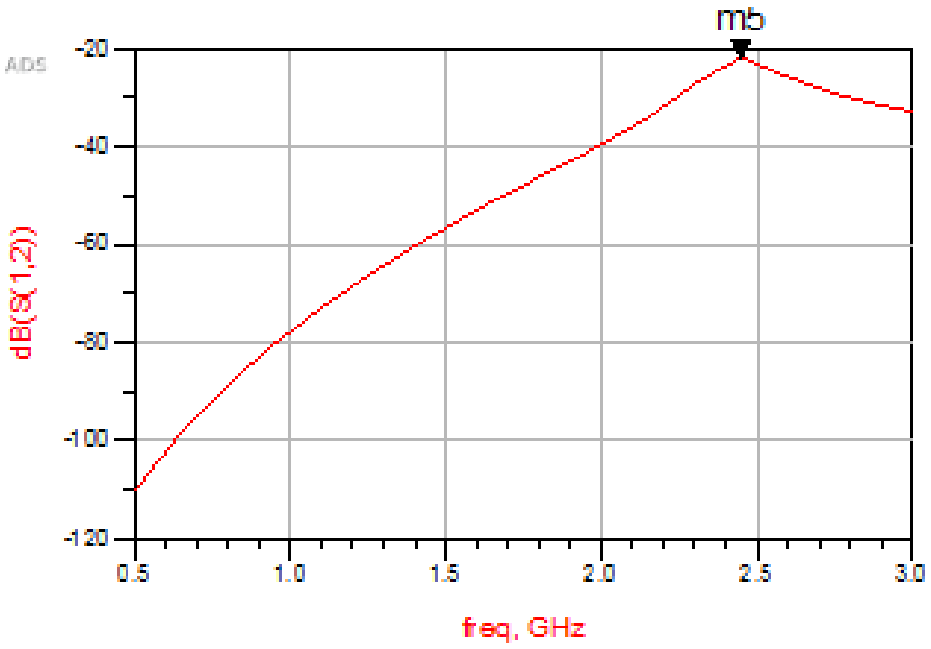

Fig. 4.20 Reverse Isolation (S_{12})

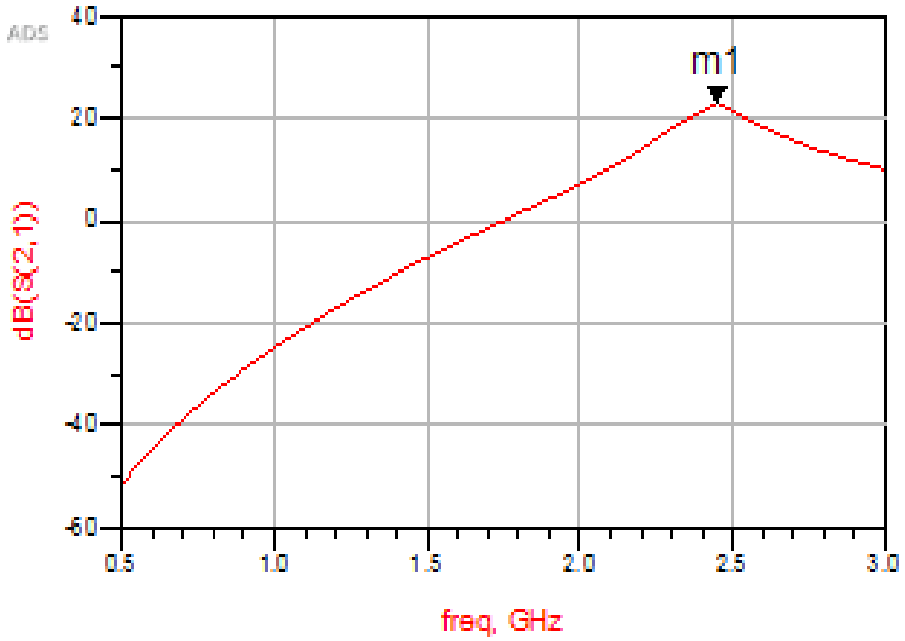

Fig. 4.21 Forward Gain (S_{21})

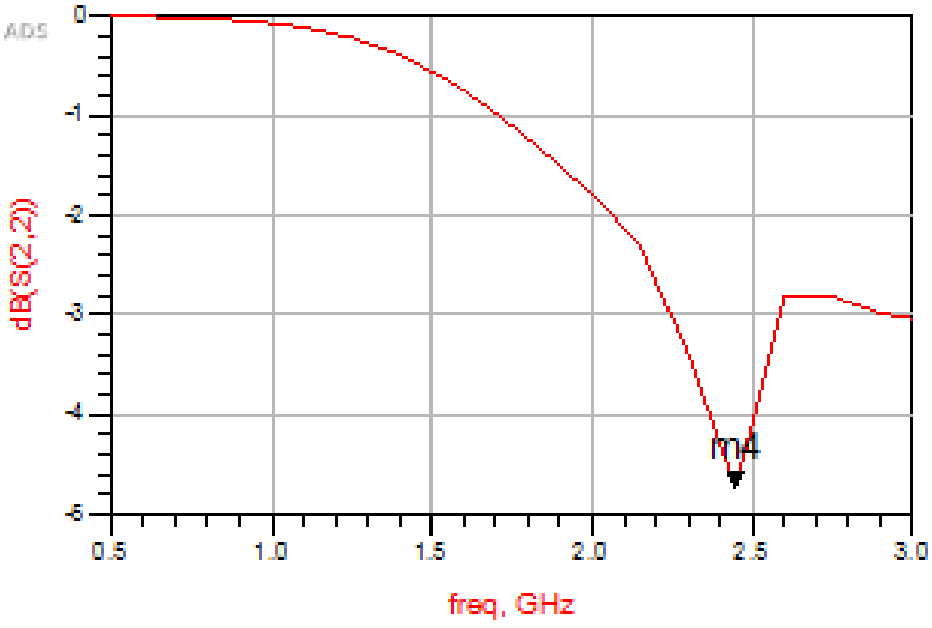

Fig. 4.22 Output Reflection Coefficient (S_{22})

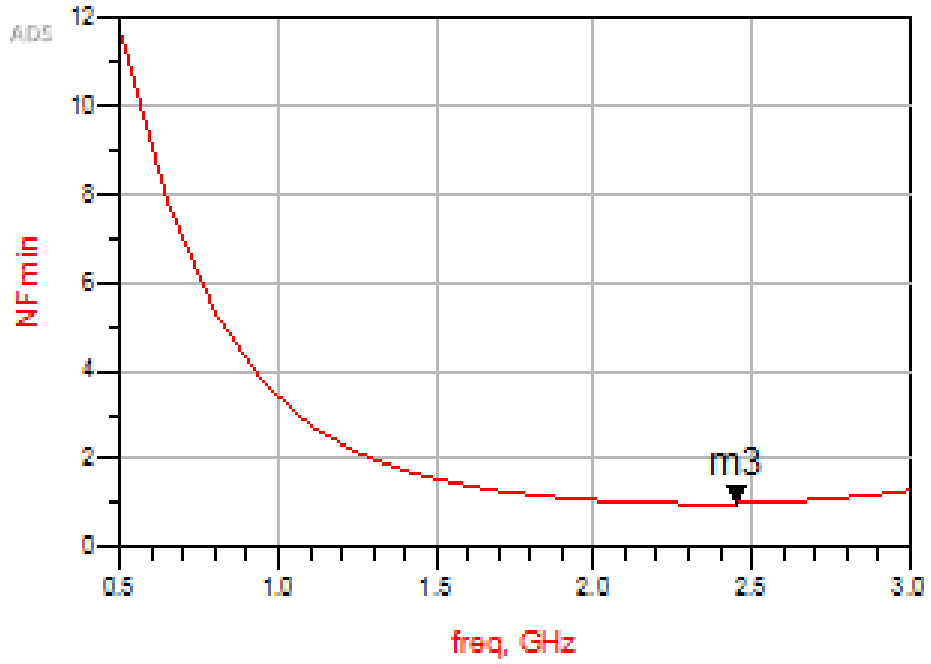

Fig. 4.23 Noise Figure (NF)

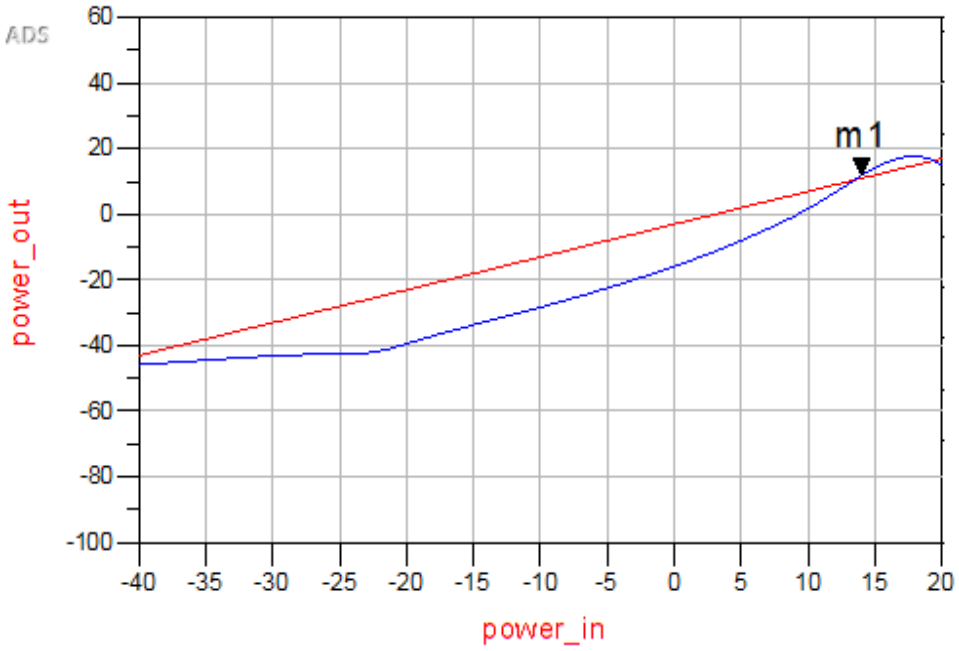

Fig. 4.24 IIP3

4.4 Common Source Shunt Resistive Feedback LNA topology

4.2.5 Circuit Design

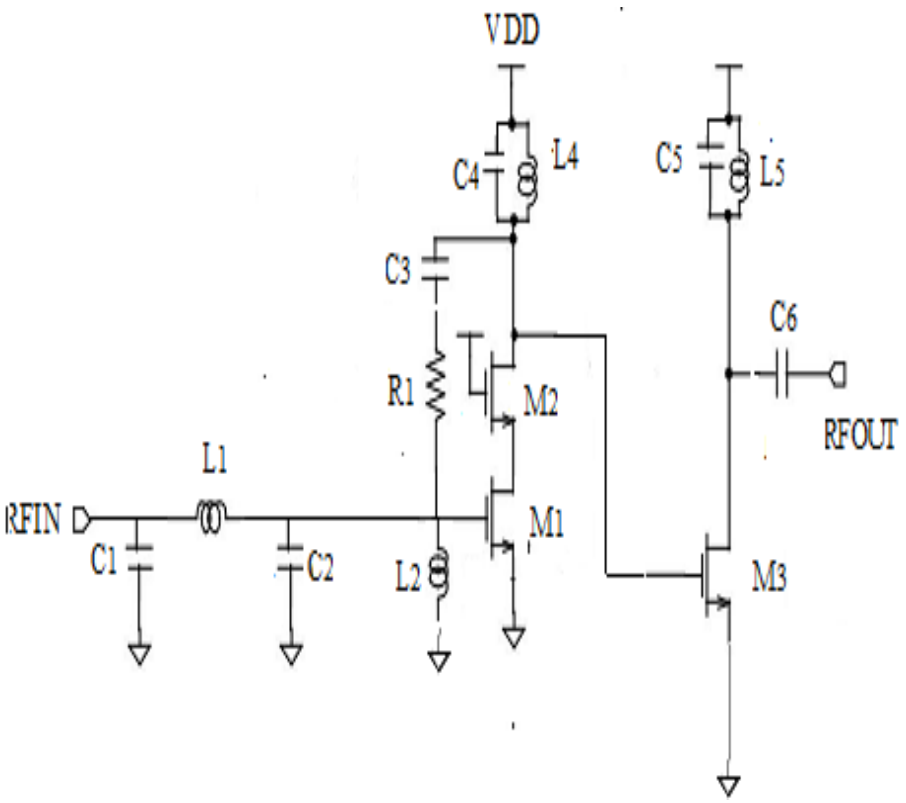

Fig. 4.25 Proposed Common Source Shunt Resistive Feedback CMOS LNA

This is a very simple low noise amplifier topology making it suitable for low cost LNA applications (ideally). The first stage consists of two transistors, one is a common source stage and other is a common gate stage. The two transistors are connected in cascode configuration. Although, the gain of the common source stage is not large in cascaded configuration, but its benefit is that it has negligible Miller effect on M1 transistor. Here, R1 is used as the feedback resistor and C3 is used as the blocking capacitor. The feedback resistor is placed in shunt to achieve broadband matching of input and also to get negative feedback so as to improve stability factor,that provides unconditional stability of the amplifier and reduces the gain sensitivity. L4 and C4 serve as cascode stage loading elements, formed by the inductor in parallel with a capacitor. The second stage is a source follower stage which is used to extend the bandwidth further and to achieve high gain. This stage also provides matching of the output impedance. L1, C1 and C2 form pi – matching

network which is used at input to improve linearity of the circuit and to achieve input impedance matching.

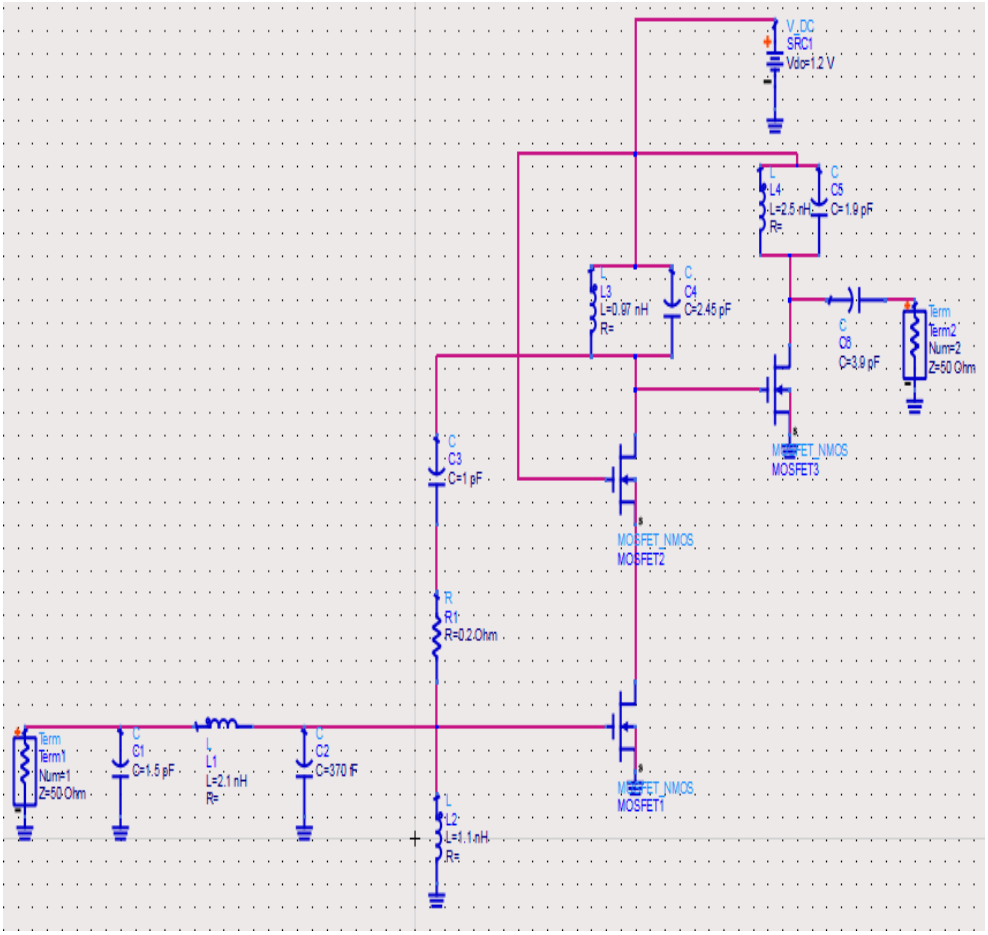

Fig. 4.26 Schematic of proposed Common Source Shunt Resistive Feedback CMOS LNA in ADS

4.2.6 Simulation and Results

Simulations of the proposed LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S_{21}) of 15.417 dB as shown in figure 4.29. The input reflection coefficient (S_{11}) is -9.170 dB as shown in figure 4.27 and the output reflection coefficient (S_{22}) is -6.024 dB as shown in figure 4.30. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S_{12}) as shown in figure 4.28 is –18.909 dB and a minimum noise figure of 1.182 dB is obtained as shown in figure 4.31. The simulated IIP3 result is shown in figure 4.32, and IIP3 of 8 dBm is obtained. From the result, it can be concluded that very high gain and a high linearity with low noise figure have been achieved.

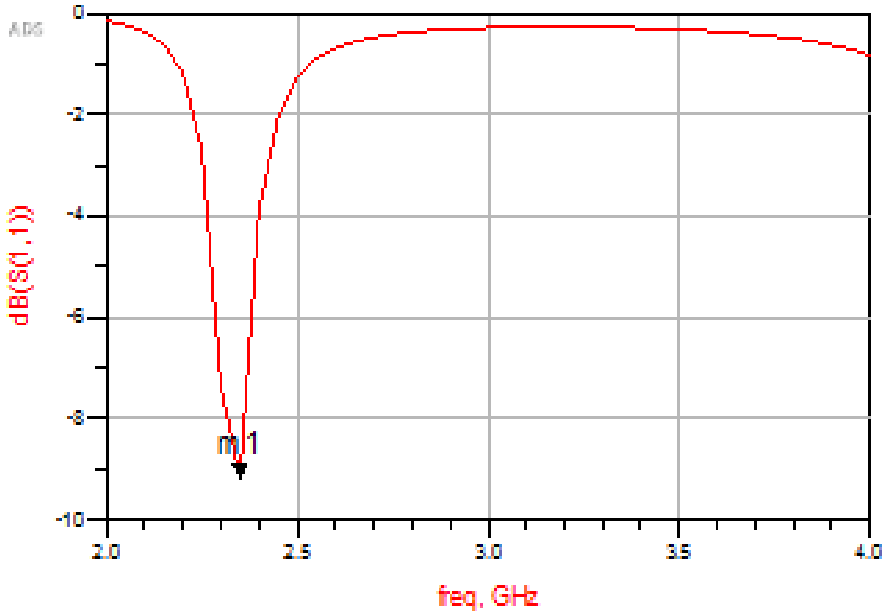

Fig. 4.27 Input return loss (S_{11})

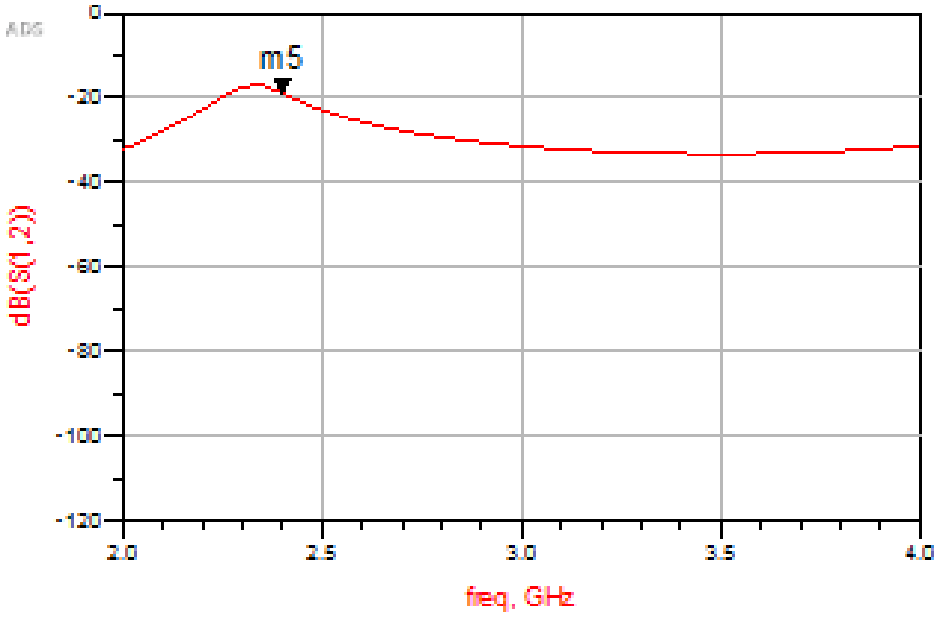

Fig. 4.28 Reverse Isolation (S_{12})

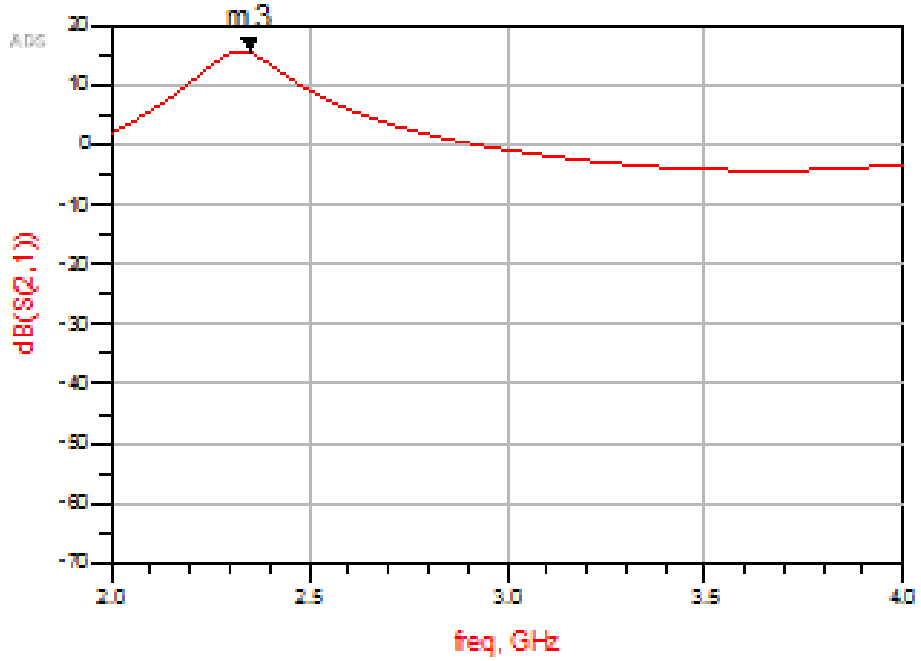

Fig. 4.29 Forward Gain (S_{21})

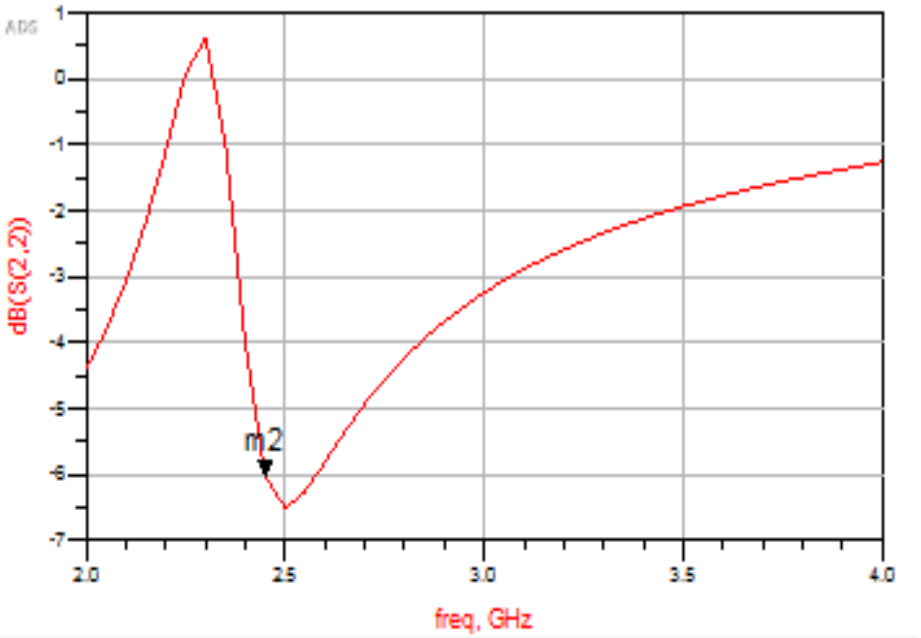

Fig. 4.30 Output Reflection Coefficient (S_{22})

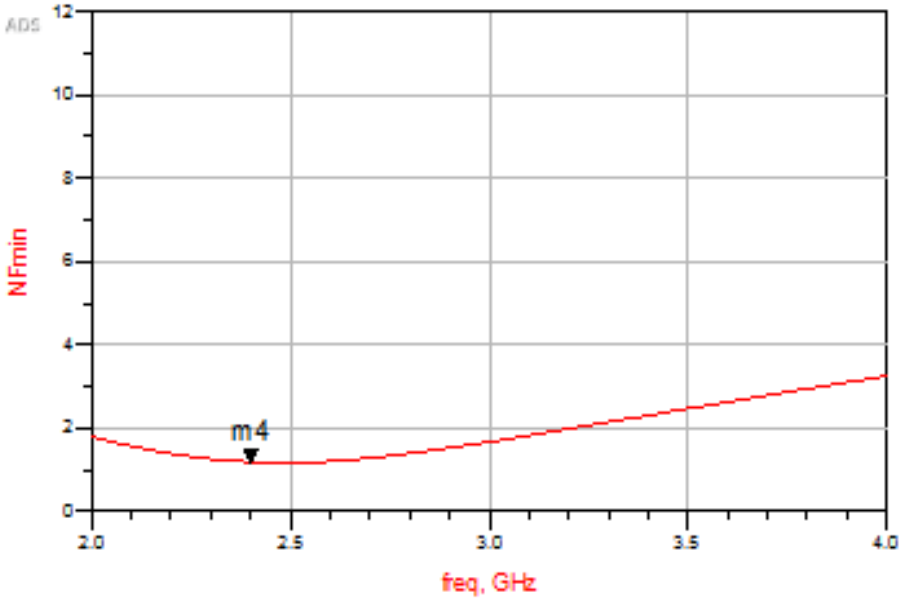

Fig. 4.31 Noise Figure (NF)

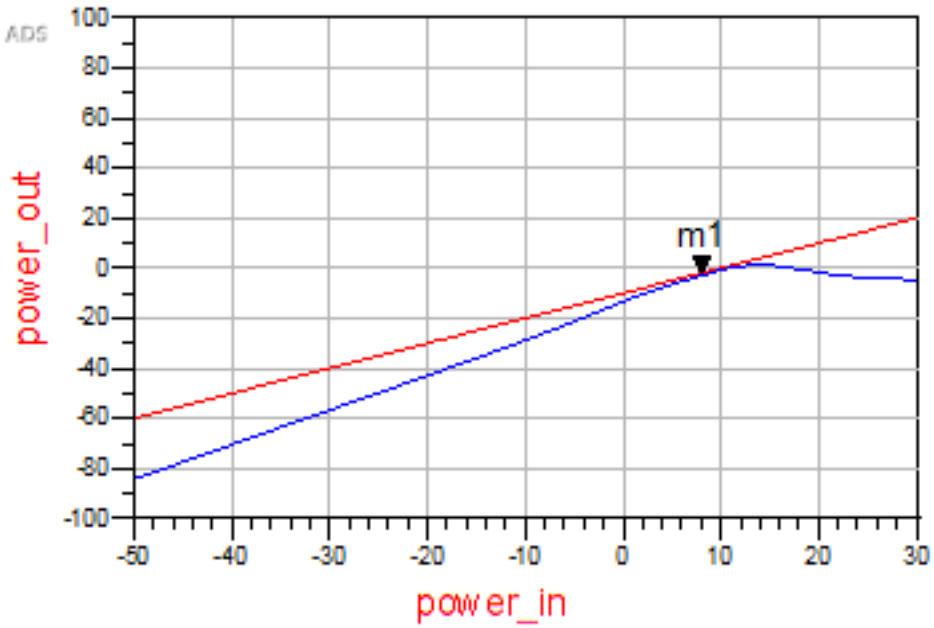

Fig. 4.32 IIP3

4.5 Common Gate LNA topology

4.2.7 Circuit Design

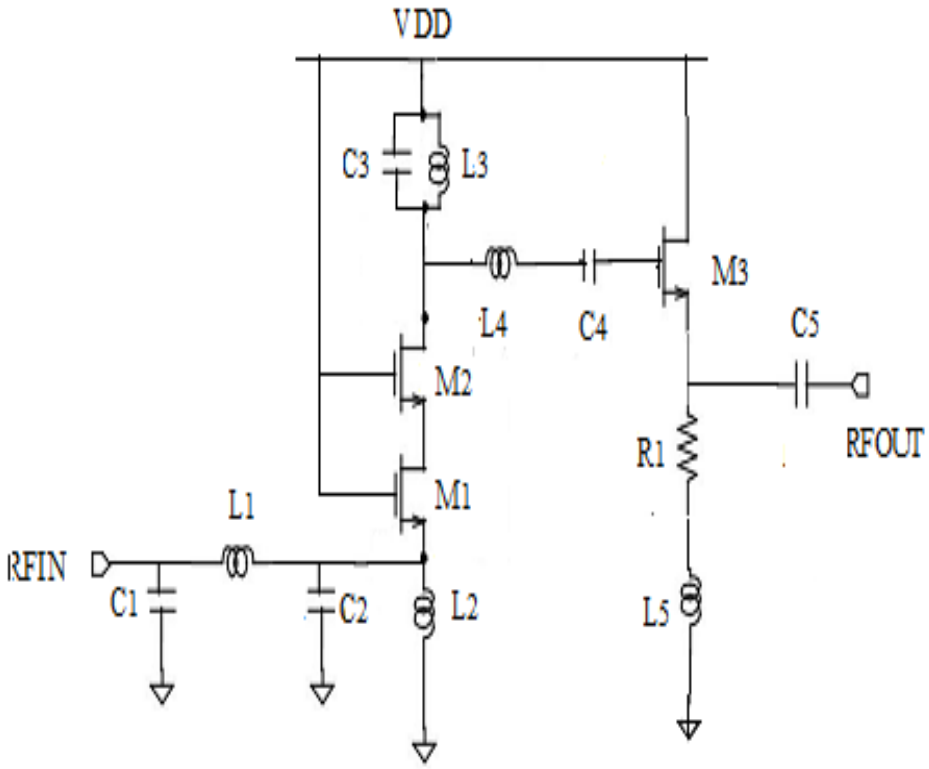

Fig. 4.33 Proposed Common Gate CMOS LNA

The proposed LNA consists of common gate and common source stages, of which at the first stage, for the input matching, the common gate topology is adopted. Parallel resonance is present instead of series resonance for the input matching of common gate amplifier.

$$Q_{CG} = \omega_o \frac{C_{gs}}{g_m} \tag{4.1}$$

where,

$$\omega_0 = \frac{1}{L_s C_{gs}} \tag{4.2}$$

However, the power gain of common gate amplifier is lower than common source amplifier. So, a common source amplifier is used in second stage of our circuit to compensate for the power gain. To ensure that the circuit is optimized, the LC tank

circuit is matched for the center frequency. To block RF current leakage to ground, inductor L2 is used. As compared to common source amplifier, the value of L2 for common gate amplifier is higher. C1, L1 and C2 form pi-matching network at input and C5 is the DC blocking capacitor.

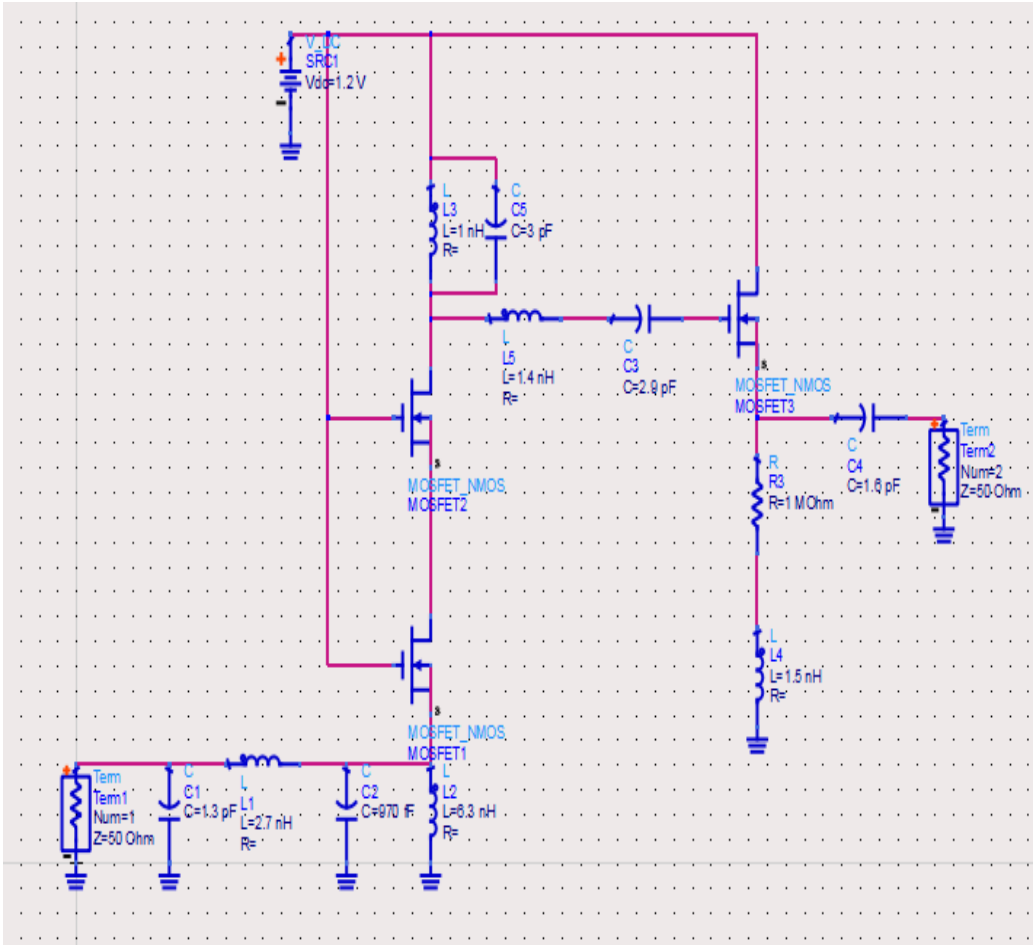

Fig 4.34 Schematic of proposed Common Gate CMOS LNA in ADS

4.2.8 Simulation and Results

Simulations of the proposed LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S_{21}) of 7.526 dB as shown in figure 4.37. The input reflection coefficient (S_{11}) is -26.894 dB as shown in figure 4.35 and the output reflection coefficient (S_{22}) is -12.246 dB as shown in figure 4.38. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S_{12}), as shown in figure 4.36, is –18.604 dB and a minimum noise figure of 3.513 dB is obtained as shown in figure 4.39. The simulated IIP3 result is shown in figure 4.40, and IIP3 of 12 dBm is obtained. From the result, it can be concluded that high linearity and good input matching have been achieved.

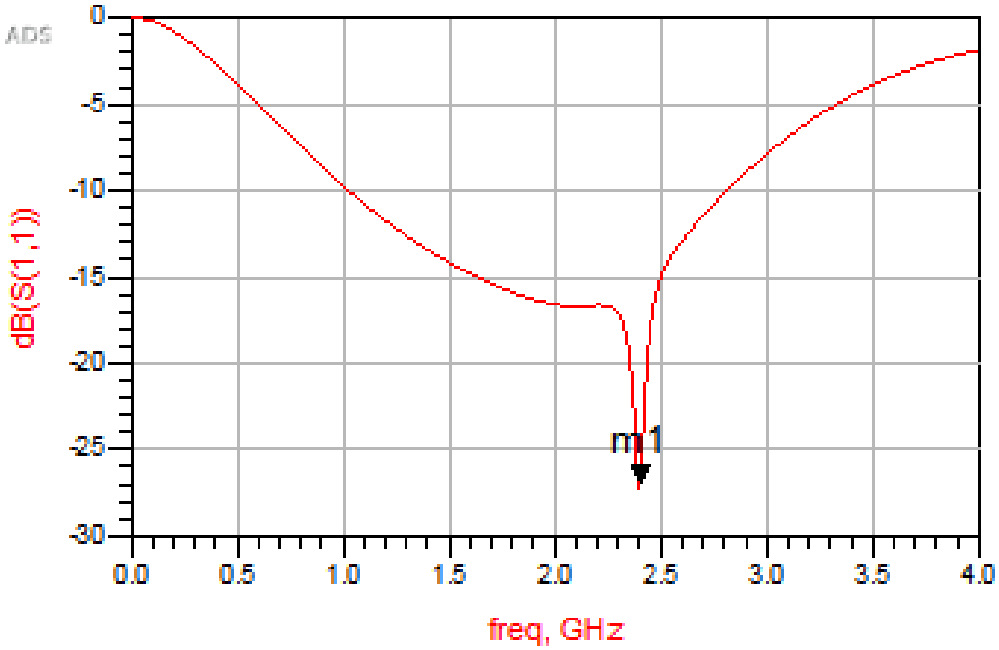

Fig. 4.35 Input Reflection Coefficient (S_{11})

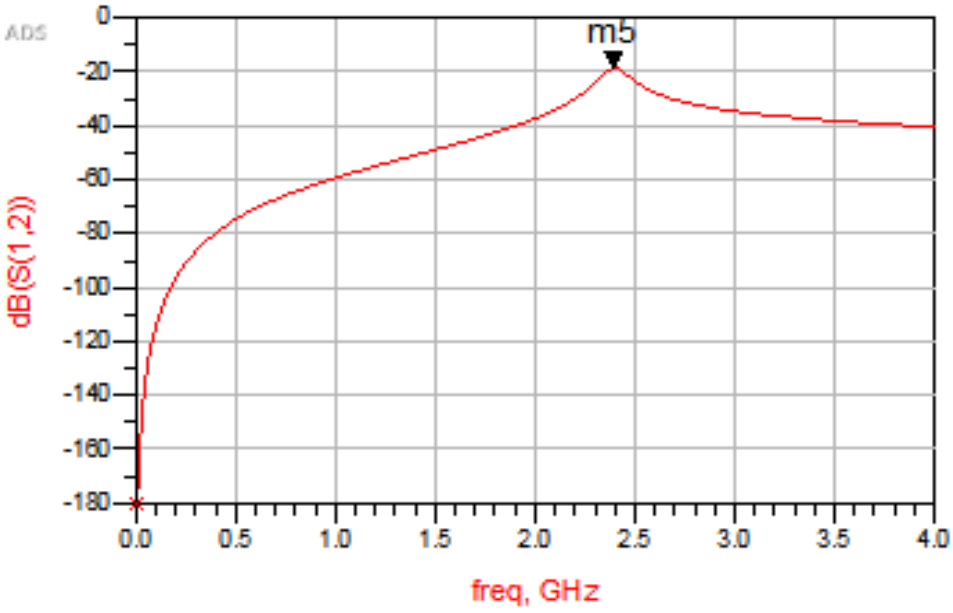

Fig. 4.36 Reverse Isolation (S_{12})

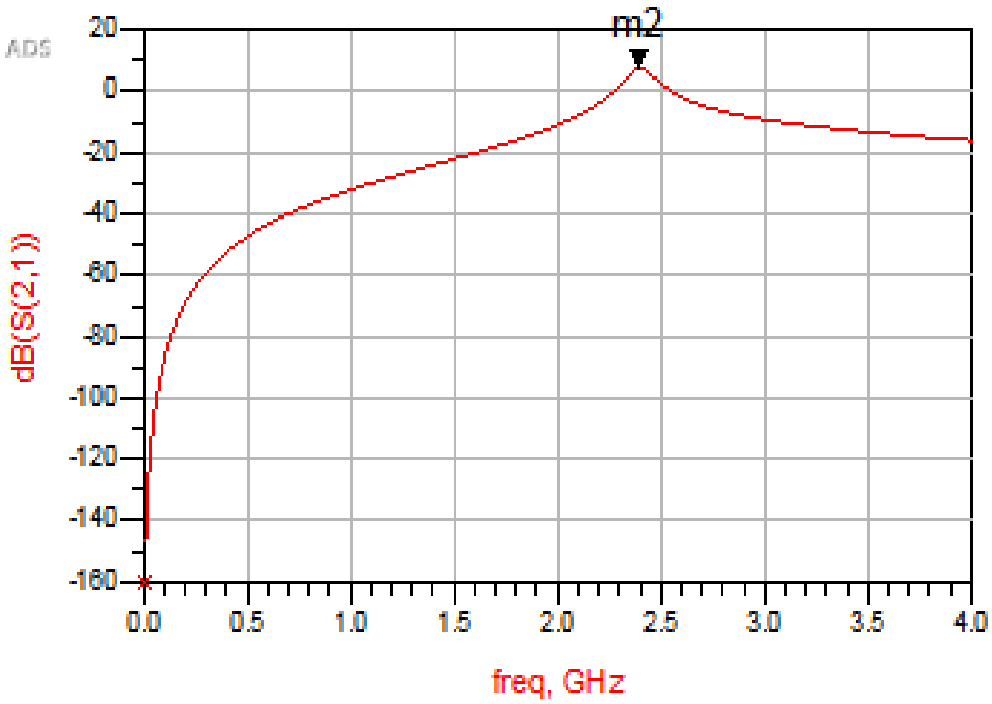

Fig. 4.37 Forward Gain (S_{21})

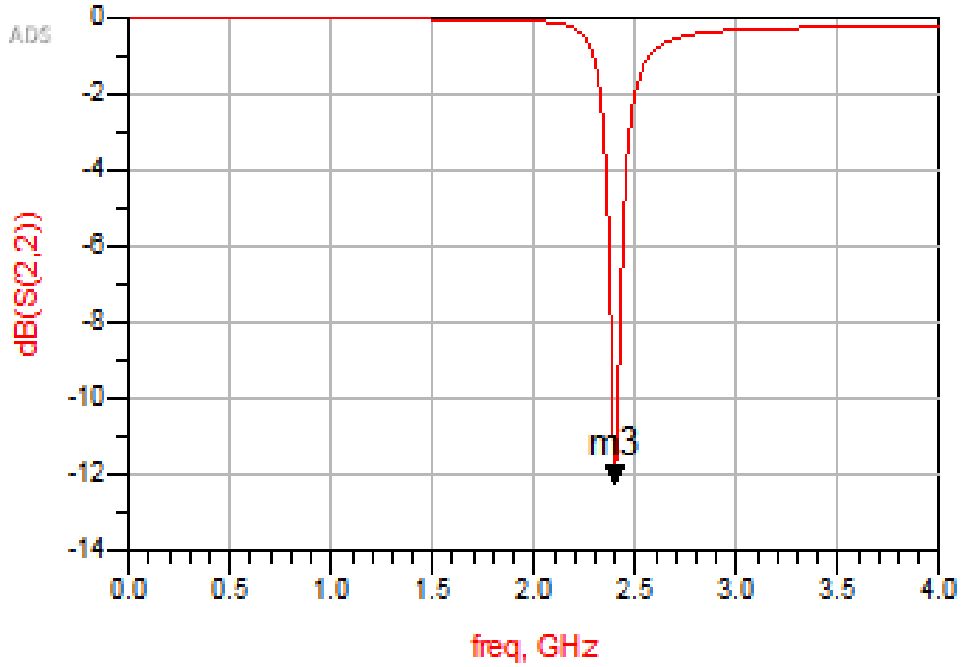

Fig. 4.38 Output Reflection Coefficient (S_{22})

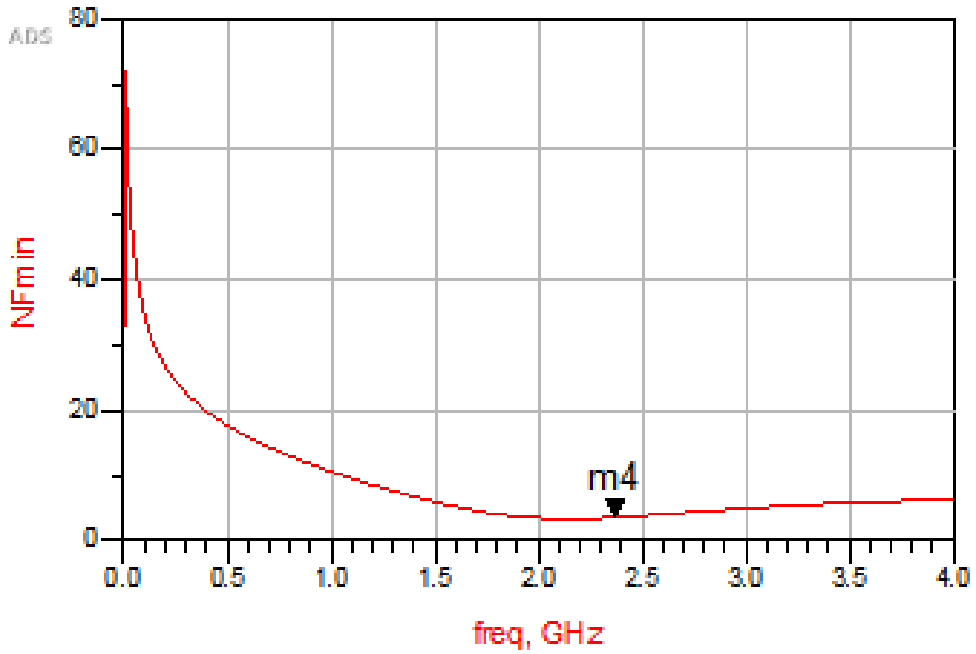

Fig. 4.39 Noise Figure (NF)

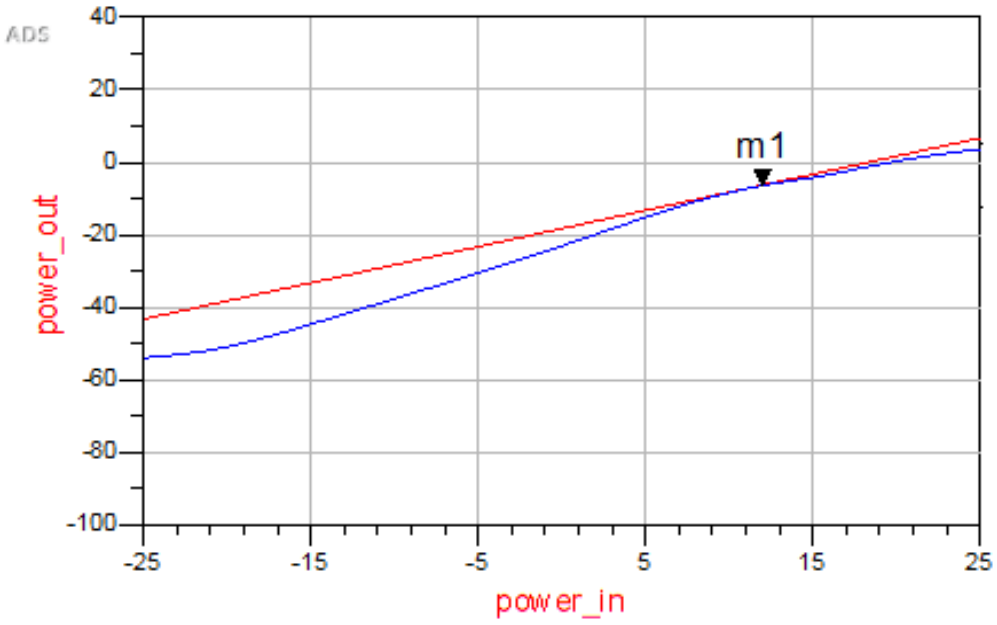

Fig. 4.40 IIP3

Chapter-5

RESULT AND CONCLUSION

In this thesis, the designs are implemented in ADS using 0.13µm RF CMOS technology for 2.4 GHz frequency. All the designs operate with the 1.2 V supply voltage. These LNAs give high gain, low noise figure with proper input and output matching. These LNAs can be used in applications where high gain, high linearity and low noise figure are needed.

TABLE 5.1 COMPARISON OF EXPERIMENTAL WORK

TOPOLOGIES / PARAMETER	CS Cascode with FDC	CS Inductive Degeneration LNA [86]	CS Inductive Degeneration LNA with FDC	CS Shunt Resistive Feedback LNA	CG LNA
S_{11} (dB)	-5.562	-7.375	-9.408	-9.170	-26.894
S_{12} (dB)	-22.06	-41.47	-21.732	-18.909	-18.604
S_{21} (dB)	10.976	24.227	23.032	15.417	7.526
S_{22} (dB)	-8.707	-0.28	-4.730	-6.204	-12.264
NF (dB)	10.26	2.109	0.988	1.182	3.513
IIP3 (dBm)	17.0	4.0	14.0	8.0	12.0

From table 5.1, it can be concluded that highest gain is obtained from common source inductive degenerated LNA while common source inductively degenerated LNA with FDC provides the lowest noise figure. Highest linearity is achieved by common source cascode LNA with FDC; and for highest input impedance matching, common gate LNA should be preferred.

Overall performance of the common source inductively degenerated LNA with FDC is good as it has a high gain of 23.032 dB, high linearity of 14 dBm, low noise figure of 0.988 dB and good input impedance matching ≈ 10 dB. Therefore, it can be concluded that inductively degenerated LNA with FDC is the best LNA topology as compared to others, for IEEE 802.15.4 Zigbee standard i.e. at 2.4 GHz.

Chapter-6

FUTURE DIRECTIONS

In the future, this work can be further optimized by using multiple low noise amplifiers that have their degenerated inductors shared with each other in common source inductively degenerated low noise amplifier so that the area is reduced and the circuit is also operated for multiple standards and frequency. Moreover, a differential pair topology of all the above discussed topology can be used to further improve the performance and their results can be observed. Instead of resistor, inductor or can be used in common source shunt feedback topology. Also, various other topologies can be explored such as shunt series feedback, shunt-shunt feedback and series-series feedback topologies. Feedforward techniques, current-reuse techniques and forward body bias techniques can be used along with the topologies discussed in thesis for increasing the performance of the low noise amplifier. The topologies discussed in the thesis can be used for different frequencies, more than one frequencies and also for a wide frequency bands but with modifications which could be the next step.

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Appendices

Appendix I:
Published Papers

Mobile and Real-Time Sensing Electronic Nose based on Carbon Nanotubes

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***Abstract*—Composites/blends of conducting polymers with carbon nanotubes have caught the increasing attention of the scientific community in the last few years because of their potential applications in new devices such as in electronic nose. We aim here to review the different types of electronic nose based on carbon nanotubes as sensing material. Based on principal component analysis (PCA), portable electronic nose is applied in classification of various alcoholic beverages, sea foods, volatile components, milk and dairy products etc. and also further in determining their quality.**

***Keywords*—Carbon nanotubes, electronic nose, multiple sensor array, data acquisition system, pattern recognition algorithm, real time detection**

I. INTRODUCTION

Ecstasy in the world of science was felt because of miraculous re-discovery [1] of carbon nanotubes (CNTs) captivating realm by Sumio Ijima in 1991 and this breakthrough further kicked off with synthesis of carbon nanotubes [2,3] study of properties of both multiwall [4,5] and single walled [6,7,8] carbon nanotubes and their application in every known field. Moreover, worldwide CNT production capacity has increased at least 10-fold since 2006, and the annual number of CNT-related journal publications and issued patents continues to grow [9]. From the explored search under the topic ‘‘carbon nanotubes’’, for the period of 1990–2003 (14 years) the total number of publications was 351,824 papers and 48,448 patents, with a patent/paper ratio of 0.13 and for the period of 2000–2010 at a recorded date and time, the total number of publications, was 52,224 papers and the total number of accepted patents was 5746 items; the ratio of published patents to papers for this period is 0.11. An annual increase of 8.09% for research papers and 8.68% for patents has resulted for CNT research in the given period [10]. The domain of sensors is not ostracized and is being embraced in the bewitching and fascinating world of “nano”. An amalgam of two different worlds of carbon nanotubes and sensors has led to quantum leaps of gizmos such as carbon nanotubes based force sensors [11], thermal accelerometer based on CNT [12] ,wireless sensor based on CNT [13] , etc. These devices have shown properties far more superior compared to those without carbon nanotubes. Carbon nanotubes (CNTs) are seamless cylinders of one (single walled carbon nanotubes denoted by SWNT) or more (multiwalled carbon nanotubes denoted by MWNT) layers of graphene with open or closed ends [14]. Diameters of SWNTs and MWNTs are typically 0.8 to 2 nm and 5 to 20 nm, respectively, although MWNT diameters can exceed 100 nm. CNT lengths range from less than 100 nm to several centimeters, thereby bridging molecular and macroscopic scales. Unorganized CNTs have limited properties and are re-used in bulk composite and thin films while organized CNT architecture such as vertically aligned forests, yarns and sheets, scales up the properties and brings about new functionalities such as shape recovery [15] ,dry adhesion [16], high damping [17,18], terahertz polarization [19], large-stroke actuation [20], near-ideal black-body absorption [21], and thermo-acoustic sound emission [22,23] but thermal, mechanical, and electrical properties of CNT macrostructures such as yarns and sheets remain lower than those of individual CNTs. Moreover, CNTs are used in fabrication of various devices such as organic light emitting diodes [24], thin film transistors [25], FETs [26], etc. In the field of sensors, the above two (CNTs and sensors) are brought together to bear the sensing elements of sensors, ergo the term “nano” is affixed to sensors-nanosensors. According to Business Communication Company Inc. (BCCI), the global nanosensor market in 2004 was worth $190 million and was forecasted to reach $592 million by 2009 at an average annual growth rate (AAGR) of 25.2 per cent [27]. Many companies attempting to exploit nanosensors for health-care are targeting new applications, particularly to detect chemical molecules and agents such as proteins [28], nucleic acid [29] ,etc. and homeland security industries is making electronic nose as one of the significant candidate of this category.

II. ELECTRONIC NOSE AND ITS MODULES

A biomimetic system comprising an array of electronic chemical sensors with partial specificity and appropriate pattern recognition system and which is capable of recognizing odors is an E-nose, a term coined by Gardner and Barlett in 1988 [30,31]. After being first developed in 1987, it is being used in wide variety of applications. However, not everything that has smell or odor can be measured with the help of e-nose, thus more justly it is construed as a chemical array sensor system that emulates mammalian olfactory system. The e-nose is both more and less at the same time, because it is not adapted to detect substances of daily importance in mammalian life such as the scent of other animals, foodstuff, or spoilage, while it offers the capability to detect some important non-odorant gases, thus making e-nose application specific and ergo; all-purpose electronic nose is not

available. Therefore it can be concluded that electronic nose is technical equivalent of mammalian nose but when compared between the two, the natural olfactory system i.e., mammalian nose outshines the advantages offered by artificial nose/e-nose. Nevertheless, there are many strong drivers to apply it in the field of olfaction because alternatives either are not practicable or are too costly and time-consuming, e.g., human test panels [32]. Detriment of existing e-nose is that they usually work offline and are not fully portable; and target gas samples have to be brought where equipment is set. Hence, a fully portable electronic gas measurement sensor with high sensitivity is needed in the market [33]. To meet these requirements, further advances have been made to obtain a mobile battery operated electronic nose which has measurement circuit on it; making it easy to operate.

In principle, E-nose consists of three main elements, namely:

(i) Multiple sensor array (MSA)

The electronic integration of various sensors inside one set constitutes an array of sensors called multiple sensor. These sensors transduce chemical interactions into signals that can be measured after processing them. The sensing elements depending on type of analyte (gas that is required to be detected) are chosen. Most commonly, different sensors are required for cross verification of data and identical sensors are required to improve precision.

(ii) Data Acquisition System

System responsible for ensnaring the signals provided by the multiple sensor array; and conveying them to the computing system that processes the information. Also, it must be able to handle and store data from multiple sensors and this data is used to prepare data bank. This system is integrated in single devices such as microcontroller, microprocessor, DSP, etc. The data is usually acquired through a USB DAQ device/data acquisition card (NI USB-6008).

(iii) Pattern Recognition Algorithm

The pattern recognition algorithm (PRA) classifies, identifies the vapor or odors of concern based on the data stored in data-bank. To construct a database and train a pattern recognition system, patterns or finger prints from known analytes are used so that the unknown analytes can subsequently be classified and identified. There are various methods used to aid this process but the commonly used one is Principal Component Analysis (PCA). PCA is statistical technique and allows an easy visualization of all information. However, preprocessing or feature extraction from the acquired sensor signal prior to the use of PCA is necessary to get the better separation. PCA is most useful when no known sample is available or when it is suspected that relationships between samples or variables are veiled [34].

The applicability of electronic noses has been tested in every imaginable field where odor or odorless volatiles and gases are thought to play a role, some of such fields include food freshness, quality, ripeness and shelf-life [35, 36, 37], milk and dairy products [38,39], meat products [40], fish and seafood products [41], agricultural plant production [42], plant pathology [43], medical pathology [44, 45, 46], chemistry and chemical detection [47, 48], alcohol beverage detection [49, 50, 51] ,etc.

III. Carbon nanotubes and its flavors

Carbon nanotubes (CNTs) are an allotrope of carbon comprised of graphene sheets rolled up into cylinders of sp2 hybridized atoms, hence tubular in shape. CNTs are typically microns long; and when combined with their narrow diameter, lead to excellent material properties such as a high aspect ratio and large surface area. The electrical properties of a CNT are determined by the tube helicity and diameter. CNTs can be approximated to one-dimensional nanostructures [52]. Structurally, carbon nanotubes exhibits 2 flavors, single walled nanotubes [53] and multi-walled nanotubes in which former is made of single graphite layer rolled into hollow cylinder and latter is made of concentric arrangement of these cylinders.

A. Multi-walled carbon nanotubes (MWNTs)

Multi-walled carbon nanotubes, which were the first to be discovered, consist of concentric cylinders around a common central hollow with a constant separation between the layers close to the graphite interlayer spacing (0.34 nm) [54]. Each individual cylinder is characterized by a different helical angle and has a diameter ranging from 2 to 25 nm and a length of several microns [55].

B. Single walled carbon nanotubes (SWNTs)

Single walled carbon nanotubes were observed about two years later after the discovery of MWNT [56]. Compared to the multiwall tubes, the single-walled nanotubes are generally narrower with diameters typically in the range 1-2 nm, and tend to be curved rather than straight [57].

IV. Mobile And Real-Time Sensing E-Nose based on CNT

A. Sensors

Sensors are the heart of the system and can be divided according to the type of sensitive material used: inorganic crystalline materials (e.g. semiconductors and metal oxides) [58], organic material and polymers (carbon nanotubes) [59], and biologically derived material (immobilized biologic molecule (enzymes, cellules or antibodies)) [60]. So, the sensors such as metal oxide semiconductors (MOS) [61], organic conducting polymers (CP) [62], chemo-capacitors, MOS field effect transistors (MOSFET) [63], quartz crystal microbalance (QCM) [64, 65], surface acoustic wave (SAW) [66,67] etc. are used as e-nose sensors for the analysis of gases . Fabrication of sensor array by carbon nanotubes can be further divided into two categories: one made of MWNTs and the other made of SWNTs.

a) MWNT

i) MWNT-SnO_2

The gas sensors were fabricated by E-beam evaporation [68]. Under a vacuum pressure of $\sim 10^{-4}$ Torr, the substrates were cleaned by oxygen-ion bombardment; to improve the adhesion of the film to the substrates, then Cr/Au interdigitated electrodes on alumina substrates were prepared and through electroplated-Ni shadow masks, Cr and Au layers were then successively E-beam evaporated over the alumina substrates. The resulted thickness of Cr and Au layers were ~50nm and ~200 nm, respectively and the spacing, width, and length of the interdigitated electrodes were approximately 100 μm, 100 μm, and 1 mm, and respectively. In a lab- made horizontal tube furnace, MWNT powder was synthesized by thermal chemical vapor deposition (CVD). By mixing 15g of SnO_2 powder with 0.075g and 0.15g of CNT powders, respectively, CNT–SnO_2 mixed powders were prepared with 0.5 wt% and 1 wt% concentrations. The mixed powders were thoroughly mixed for 30 min by grinding in a mortar and at a pressure of 15 tons, the pure SnO2 and mixed powders were compressed into cylindrical pellets in a hard steel mold by a hydraulic compressor. Next, the mixed CNT–SnO_2 materials (0.5 wt% and 1wt% CNTs) and compressed SnO_2 were loaded in E-beam chamber and evaporated over the interdigitated electrodes through an electroplated shadow mask with square window pattern that aligned to the interdigitated area at an operating vacuum of$\sim 10^{-5}$ Torr. The film thickness of sensing materials was ~300 nm. For 3 hours, the evaporated film was then annealed at 500 ˚C. Finally, at the backside of substrate, a NiCr layer with (Ni 80% and Cr 20%) was also E-beam evaporated to perform as a heating unit as the NiCr heater can perform heating up to 350˚C. Fig 1 shows the photograph of fabricated sensor [68].

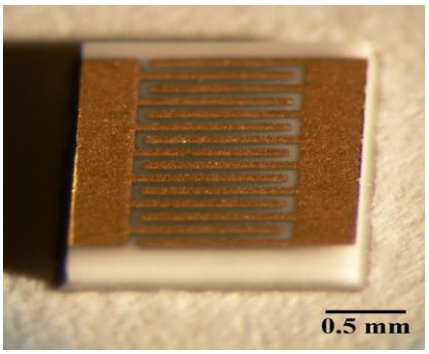

Fig. 6. Fabricated sensor

(Taken from C. Wongchoosuk, A. Wisitsoraat, A. Tuantranont, T. Kerdcharoen, "Portable electronic nose based on carbon nanotube-SnO2 gas sensors and its application for detection of methanol contamination in whiskeys", Sensors and Actuators B: Chemical, vol. 147, no 2, pp. 392-339, 2010)

ii.) MWNT polymer sensor array

To form MWNT-polymer gas-sensor array chip, twelve independent sensing areas were present [69] on a single silicon substrate of which ten sensor array chip each of size 34mm x 20mm were fabricated using the batch process on 4-inch wafer, eight of which were coated with sensing components while remaining were reserved for future addition. To minimize heat loss from silicon substrate each of the sensing elements contained a circular membrane with diameter 2 mm.

The selection of polymer was performed according to two processes: the linear solvation energy relationship (LSER) theory and physical absorption bonding. In the former process, to enhance the device recognition capability for different odours, LSER theory was applied. Using series of LSER coefficients related to the polymer solubility properties, LSER equations correlate the log of the partition coefficient of a vapor in a polymer with the vapor solvation parameter. It was scrutinized that a smaller solvation coefficient corresponds to larger interaction between ethanol gas and polymer, resulting in larger resistance variation. However, physical as well as chemical characteristics of film can be changed by carbon nanotubes, making solvation energy insufficient for sensor-analyte interaction. To use the sensors repetitively with a short recovery time, the interaction between gas and polymer membrane was usually the latter process of physical adsorption bonding, namely: hydrogen-bond acidic (HBA), hydrogen-bond basic (HBB), dipolar and hydrogen-bond basic (D-HBB), moderately dipolar and weakly H-bond basic or acidic (MD-HB), and weakly dipolar with weak or no hydrogen-bond properties (WD). Methods adopted to fabricate the gas sensing films for these sensors:

1. One-layer film-making method: in methyl ethyl ketone (MEK) solvent, the selected polymers were dissolved and MWNTs (1 wt.%) were added. Under ultrasonic oscillation, the mixture was magnetically stirred to achieve uniform dispersion. Using an HPLC syringe, the uniformly mixed composite precursor was injected onto the chip. The solvent was removed and by baking in a vacuum oven for 24 hrs, the composite membrane was formed
2. Two-layer film-making method: by drop-casting 1 mg/ml MWNTs (1 wt.%) dispersed in MEK onto the surface of an interdigitated microelectrode (IME) device, a MWNT-modified electrode layer was prepared. To yield the MWNT film, the MEK solvent was evaporated in air, at room temperature. To form the multilayer films [70] ,the polymer films were deposited by drop casting their solutions onto the MWNT layer, followed by drying in vacuum.
3.

b) SWNT

By E-beam evaporation of Cr/Au over alumina substrates through electroplated-Ni shadow masks, interdigitated electrodes (IDE) were fabricated. The thickness of Cr and Au layers were ~50 nm and ~200 nm, respectively and the width, spacing, and length of the IDE were approximately 100 μm, 100 μm, and 1 mm, respectively. The SWNTs were dispersed in the polymer solution such as PVP, cumene-PSMA, etc. Each composited material was dropped onto the interdigitated electrodes and was heated at 150 °C for 1 hour to remove the residual solvent and impurities leading to formation of sensors. The resistances of fabricated sensors were approximately between 500Ω - 20kΩ under ambient condition [71].

Chemical compounds used for sensing volatile organic components generated from human's axillary skin, as a polymer on SWNT-COOH are cumene terminated polysterene-co-maleic anhydride (cumene-PSMA), poly(styrene- co-maleic acid) partial isobutyl/ methyl mixed ester (PSE), polyvinylpyrrolidonn (PVP), and on SWNT-OH are Cumene terminated polystyrene-co-maleic anhydride (Cumene-PSMA), Poly(styrene-co-maleic acid) partial isobutyl/ methyl mixed ester (PSE), Polyvinylpyrrolidon (PVP) [72] while for sensing proteins such as amino proteins, as a polymer on SWNT-COOH, are polyvinhyl chloride (PVC) in THF, cumene terminated polysterene-co-maleic anhydride (cumene-PSMA) in the acetone, poly(styrene- co-maleic acid) partial isobutyl/ methyl mixed ester (PSE) in acetone, polyvinylpyrrolidonn (PVP) in ethanol, and on SWNT-OH are polyvinhyl chloride (PVC) in THF, cumene terminated polysterene-co-maleic anhydride (cumene-PSMA) in the acetone, poly(styrene- co-maleic acid) partial isobutyl/ methyl mixed ester (PSE) in acetone, polyvinylpyrrolidonn (PVP) in ethanol [73] where, SWNT-COOH is carboxylic-functionalized single walled carbon nanotubes and SWNT-OH is hydroxyl functionalized SWNTs purchased from manufacturers containing 90wt% carbon with 1-2 nm diameter and 0.5-2.0 μm length and degree of functionalization is 2.73% and 3.96% for SWNT-COOH and SWNT-OH, respectively. Here, the polymers are varied to introduce the difference of physical and chemical properties for generating the specific patterns of activation across the sensor array. For the same reason, two types of functionalized single-walled carbon nanotubes were used to disperse in each of the polymer matrix.

V. Conclusion and future Scope

Sensor array based on CNT-SnO2 are designed and the doping of CNTs enhances the sensitivity of SnO2 sensors and the amount of doping affects the selectivity of gases while in the sensor array based on polymer/SWNT nanocomposites, specific pattern were generated by using polymer matrix and functionalized CNT (SWNT-COOH and SWNT-OH). The fabricated sensors show good sensitivity, specific to some components such as ammonia, amines while show very low response to organic solvents. The combination of MWNT and polymer has further enhanced the sensitivity making it pertinent as microarray gas-sensing elements and uses fast adaptive readout circuitry that first responds to the odor then adapts the odor. The present era is trending towards the advancement of electronic noses for particular purposes or a fairly narrow range of applications. The efficiency of electronic nose can be increased by reducing instrument costs, and allowing easy data analysis by wireless electronic nose and highly sensitive to the gas to be detected. New potential discoveries in this new sector of sensor technology will continue to expand as new products, machines, and industrial processes are being developed. These developments will lead to the recognition of new ways to exploit the electronic nose to solve many new problems for the benefit of mankind. New emerging technologies are continuously providing means of improving e-noses' capabilities by interfacing and combining classical analytical systems for rapid discrimination of individual chemical species within aroma mixtures. Future appears to be brighter for electronic nose based on carbon nanotubes.

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A High Gain and Moderate Linearity Inductively Degenerated Cascode CMOS LNA for 2.4 GHz ISM Band

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Abstract—**A high gain and moderate linearity inductively degenerated cascode CMOS LNA has been fabricated in this paper using 0.13um CMOS technology. The low noise amplifier is optimized for working in the 2.4 GHz band range. The inductive degeneration topology with pi-matched input used in the LNA provides low noise, very high gain and an acceptable IIP3. Advanced Design System (ADS) software is used for simulation. The fabricated LNA uses 1.2V supply voltage and it exhibits a gain of 24.227 dB, noise figure of 2.109 dB, input reflection coefficient (S11) of -11.11 dB, reverse gain (S12) of -41.478 dB and an IIP3 of 4.**

***Index Terms*—ADS (Advanced Design Simulation Software); LNA (Low Noise Amplifier); RF (Radio Frequency); CMOS (Complementary MOSFET); Inductively degenerated cascode; IIP3 (Third Order Intercept Point)**

I. Introduction

Because of the communication industry's rapid developments, the requirement of more and different kinds of wireless communication systems has increased. It is desired that these wireless communication systems have characteristics such as low noise figure, low input/output return losses, a high IIP3 and, low power consumption. The main aim of the manufacturers of the wireless communication systems is to achieve low power. In these wireless communication systems, the RF front-end circuit is LNA which is one of the crucial elements of RF receivers [1][2][3]. They amplify RF signal to a particular level so that the sensitivity requirements of other components in RF receivers such as filters are met by RF signal.

In this paper, a 2.4GHz band CMOS LNAs is proposed which uses an inductive degeneration cascode topology to provide low noise and high gain and also implements pi-matching network to provide better gain because compared to T-matching, pi- matching has good power gain because of introducing additional degree of freedom [4][5]. The purpose of the proposed LNA is to improve the performance of receiver by reducing the power consumption of the CMOS LNA while still retaining acceptable noise performance, good input/ output match, and moderate linearity. The LNA offered NF of 2.109 dB and input return loss of -7.375dB, output return loss of -0.28 dB, and IIP3 of 4 dBm

II. Circuit Topology

For IEEE 802.15.4 ZigBee standard, inductively degenerated cascode LNA topology is chosen because this topology is the basis of the varieties of LNA topologies which are available presently. Under low power constraint, the topology maximizes the gain and good input and output isolation is provided. Stability is improved by good reverse isolation and also input port matching is simplified [6]. The simplified schematic of the CMOS LNA is given in Fig 1.

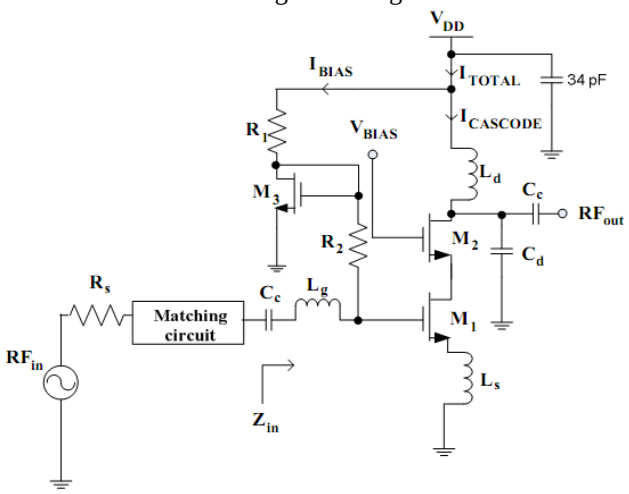

Fig. 2 Inductively-Degenerated Cascode CMOS LNA

In the circuit shown above, output matching is provide by Ld & Cd. Moreover, at output during resonance additional filtering is enabled by them. The circuit is very suitable for low power design because the series resistance contributes the voltage drop across the inductor.

The transistor and degeneration inductor combination provides input matching. The impedance at the input is given by:

$$Z_{in}=s(L_g+L_s)+\frac{1}{(sC_{gs})}+\frac{g_m L_s}{C_{gs}} \quad (1)$$

where,

$$\text{Input resistance= Rin}=R_e[Z_{in}]=\frac{g_m L_s}{C_{gs}} \quad (2)$$

Gain of LNA is given by:

$$\frac{V_{out}}{V_{in}} = \frac{-g_m s L_d}{1-\omega^2 C_{gs}(L_g+L_s)+sL_s g_m} \quad (3)$$

Also at resonant frequency,

$$\omega^2 = (L_g + L_s)C_{gs} = 1 \quad (4)$$

Therefore, by substituting (4) in (3)

$$\frac{V_{out}}{V_{in}} = \frac{-g_m s L_d}{sL_s g_m} = \frac{-L_d}{L_s} \quad (5)$$

Hence, the ratio of inductor at drain to inductor at source is the gain. If Ld is greater than Ls, then gain is high but the series resistance of inductor causes trade-off between Ld's size and output of the circuit [7].

III. Circuit Design

Figure 2. shows the schematic of the inductively degenerated cascode topology LNA using pi-matching at input.

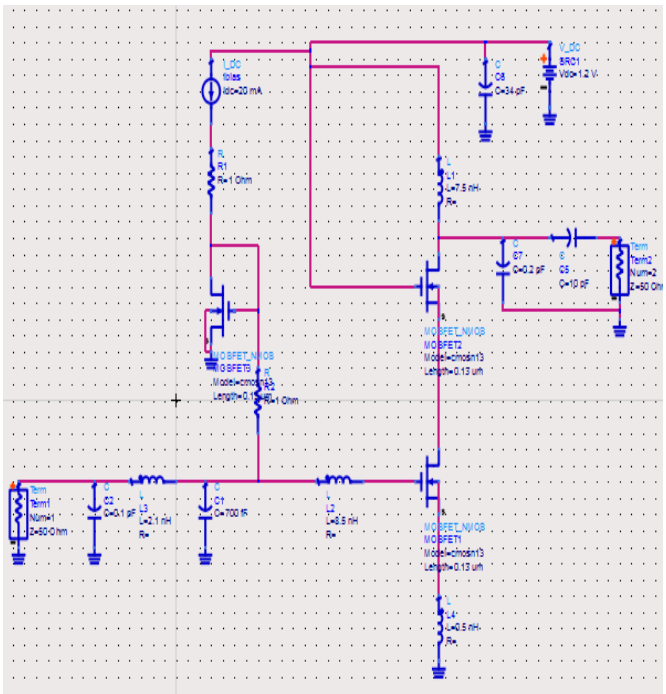

Fig. 2. Proposed LNA

A current mirror circuit is formed by M3 and R1. The input signal is enforced into the input of LNA because the signal path is isolated from the biasing circuit by M1. If the value of R2 is not greater than the input impedance of the stage before it, then the R2 value is critical. M3 is the biasing transistor in the circuit which forms current mirror with M1. To avoid heavy current consumption, the W/L ratio of M3 should not be large.

IV. Simulation and Results

Simulations of the LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S21) of 24.227 dB as shown in figure 5. To make the input matching impedance (Zin) equal to 50 Ω, Cgs and gm are selected properly according to (1). The input reflection coefficient (S11) is -7.375 dB as shown in figure 3 and the output reflection coefficient (S22) is -0.28 dB as shown in figure 6. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S12) as shown in figure 4 is -41.478 dB and a minimum noise figure of 2.109 dB is obtained as shown in figure 7. The simulated IIP3 result is shown in figure 8 and IIP3 of 4 dBm is obtained. From the result, it can be concluded that very high gain and moderate linearity have been achieved. The simulated amplifier's characteristics summary is presented in Table I. From Table I, compared with other LNA's, the performance of our proposed CMOS LNA is much better as it has the best reported value of gain at 2.4GHz.

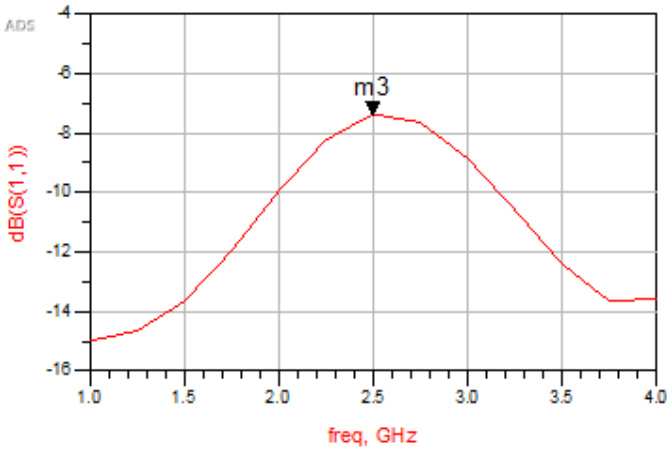

Fig. 3. Input Reflection Coefficient (S_{11})

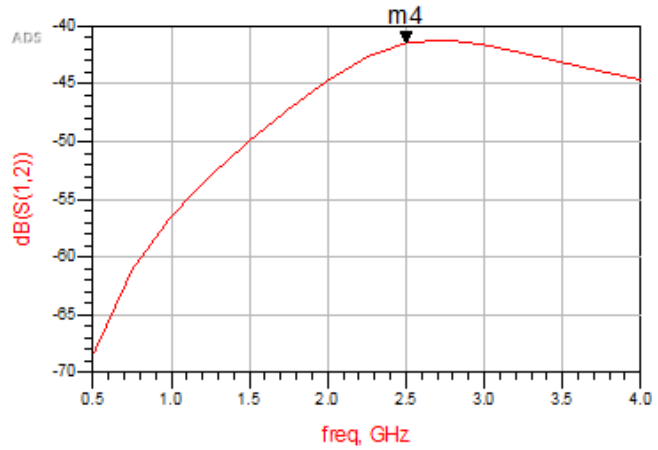

Fig. 4. Reverse Gain/ Reverse Isolation (S_{12})

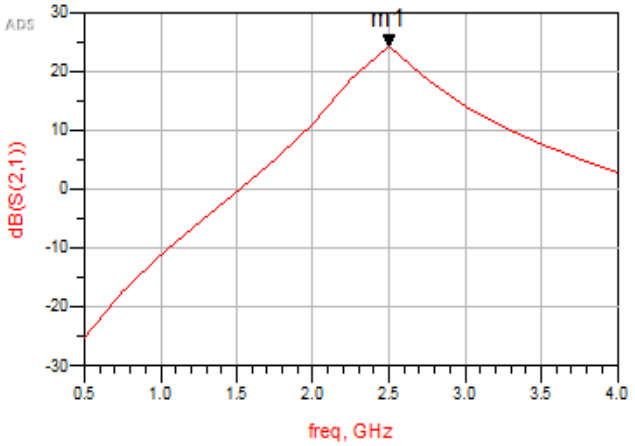

Fig. 5. Forward Gain (S_{21})

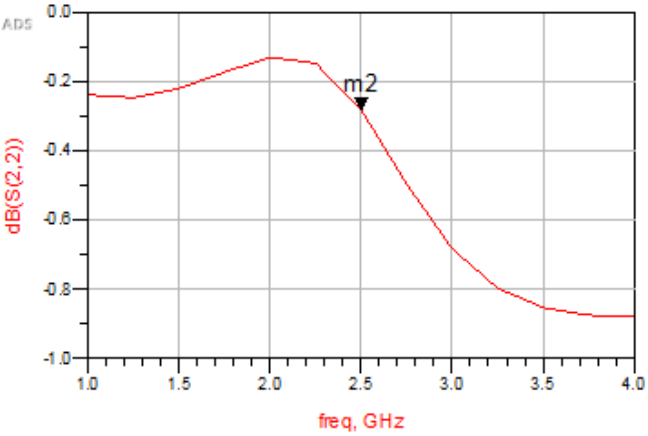

Fig. 6. Output Reflection Coefficient (S_{22})

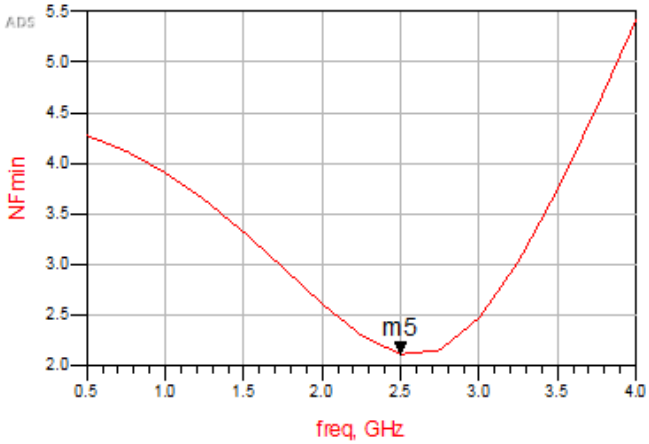

Fig. 7. Noise Figure (NF)

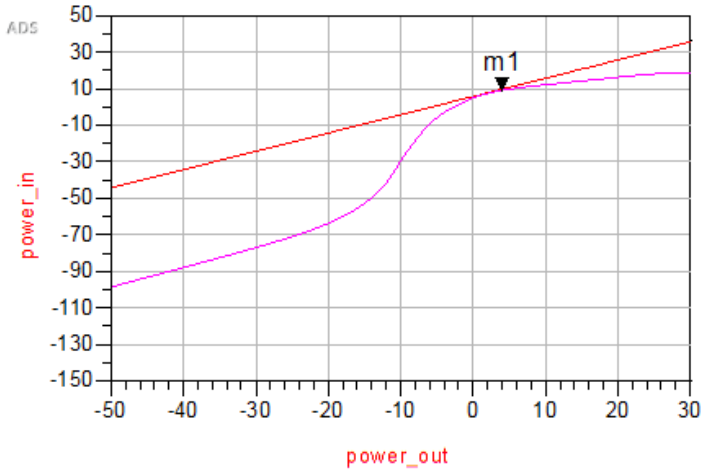

Fig. 8. IIP3

TABLE I. COMPARISON OF DIFFERENT CMOS LNA

	[7]	[8]	[9]	This Work
Frequency (GHz)	2.14	2.4-2.5	2.4	2.4
Technology (μm)	0.13	0.13	0.13	0.13
Supply (V)	1.2	1.2	1	1.2
Gain (dB)	18.24	20.343	18.5	24.227
Noise Figure (dB)	1.362	1.98	4.38	2.109
IIP3 (dBm)	–	5	0.7	4

V. CONCLUSION

In this paper, a 2.4GHz CMOS LNA for IEEE 802.15.4 ZigBee standard is proposed. Good noise figure of value 2.109 dB and very high gain of 24.227 dB are obtained at 1.2V power supply. Also, a moderate IIP3 of 4 dBm is obtained which shows that the proposed circuit has acceptable stability.

ACKNOWLEDGMENT

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Appendix II:
Accepted Papers

A High Linearity and Moderate Gain LNA for Receiver Front-End Applications in 2.4GHz ISM Band

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***Abstract*—Using EDA tool for simulation and designing of the low noise amplifier (LNA) has resulted in the acceleration of the design and production of RF low noise amplifier. In this paper, LNA is designed using BSIM3 0.13µm technology for 2.4 GHz ISM band using ADS tool, based on cascode topology using feed forward cancellation (FDC) technique. Feed forward cancellation technique has been used to improve linearity. The designed low noise amplifier (LNA) has excellent linearity, moderate gain and considerable matching of input impedance. The designed LNA is having S_{11}=-5.562 dB, S_{21}=10.976 dB, NF=10.26 dB and IP_3=17.0 dBm.**

Keywords—Advanced Design Simulation (ADS) software, Low Noise Amplifier (LNA), EDA, Cascode, Common Gate (CG), Feedforward Cancellation (FDC), Common Source (CS)

I. INTRODUCTION

The electromagnetic spectrum's part that covers high frequencies in GHz range is the radio frequency range. Signals received by and transmitted from the antenna are RF signals. People's demand for wireless applications has become more sophisticated i.e., requiring a small power of radiation, large converging area, and higher speed because of the rapid development of communication technology. Wireless telecommunication systems are used in reception and transmission of radio waves, which includes Wi-Fi, mobile phones, and two-way radios [1]. The demand of small radiation power, large converging area, and high speed are fulfilled due to the low-cost, low-rate, and low-power network; IEEE 802.15.4 ZigBee standard [2]. The license free frequency bands are 2400 MHz, 920 MHz, and 860 MHz, used by IEEE 802.15.4 ZigBee standard [3]. This design is mainly concentrated on the 2.4GHz band because of global operation in this band.

An important component of the wireless telecommunication system is a LNA [4] [5] [6] which is placed on the front end of the receiver to improve the linearity and noise figure and provide amplification of the signal by adding as little distortion and noise as possible [7] in the circuits of ultra-wide band receivers. So, metrics of good LNA are high gain, high linearity, low power consumption, low noise figure (NF), and high input isolation but also there are tradeoffs in these metrics while designing [8].

The LNA is operated in RF band so, for RF path especially, the LNA circuit should be as simple as possible otherwise, the noise in the circuit becomes too high. Moreover, amplified signal may get distorted due to parasitic effects in the complicated circuits [9]. The important goals in the designing of LNA are low NF, high gain, low power consumption, and 50 Ω input impedance. For achieving all these goals, different LNA architectures are available as follows: Common-Source (CS) stage with resistive termination, Common-Gate (CG) LNA, Common-Source with shunt feedback, Common-Source with inductive source degeneration and Common-Source with Cascode inductive source degeneration.

For termination at the input port a resistor is used, to provide 50 Ω input impedance in the resistive termination CS amplifier. In order to realize input matching, a resistor of 50 Ω is connected in parallel to the input, leading to a high NF. This architecture is undesirable where good input matching as well as low noise is desired. The transconductance (gm) value should be fixed at $\frac{1}{R_S}$ for the input matching in the Common Gate LNA, therefore, the only design variable is RL. The input transistor's transconductance of cannot be high due to the input matching. However, this topology is well known for wideband applications and also, the noise factor is quite reasonable and acceptable. The Common Source stage with shunt series feedback, as compared to the conventional Common Gate LNA, achieves lower noise figure and higher power dissipation. In Common Source with inductive source degeneration LNA, thermal noise is not generated like an ordinary resistor. So, the input matching requirement is achieved without introduction of the additional noise due to real resistor. Also, compared to other architectures, this topology consumes less power, making it suitable for low power applications. However, this topology has disadvantages like low gain, low linearity and high noise figure. The Common Source with cascode inductive source degeneration LNA has high reverse isolation and high stability. However, the inductors LS and LG have to be adjusted to keep the input impedance to 50Ω as the generated noise power from the cascode stage increases when the width of the cascode stage increases. The various LNA topologies are compared in table I shown below.

TABLE I. COMPARISON OF LNA TOPOLOGIES

Topology	Advantages	Disadvantages
Resistive termination common source LNA [10][11]	Broadband amplifier. Good input matching.	Addition of noise from the resistor. High noise figure.
Common gate LNA [11] [12][17][18]	Well known for wide band applications. Low power consumption.	Weak noise performance.
Common source with shunt feedback [10][12][13]	Broadband amplifier. Has good input and output characteristics.	High power dissipation.
Common source with inductive source degeneration [11][13][14] [15][16]	Suitable for low power applications.	Low gain, low linearity and high noise figure.
Common source with cascode inductive source degeneration [19][20][21][22]	High reverse isolation and high stability.	The noise power generated from cascode stage increases when the width of cascode stage increases.

Gain and linearity are two opposite parameters and hence, are difficult to balance; gain will be degraded automatically while trying to improve the linearity and vice versa [23]. Compared to T-matching, power gain is enhanced in Pi-matching, so that reasonable linearity is obtained at low power and hence, is adapted in this paper. The feed forward technique generates distortion (by using an additional path) which cancels the distortion of original LNA at the output. This paper shows designing and implementation of LNA in 130nm technology. The paper is arranged into four sections. In section I, an introduction to design is summarized. In section II, the circuit design is analyzed and in section III, circuit simulation result graphs are shown, and comparison of different types of single-ended LNAs has been done. Section IV gives conclusion and future scope of this work.

II. CIRCUIT DESIGN

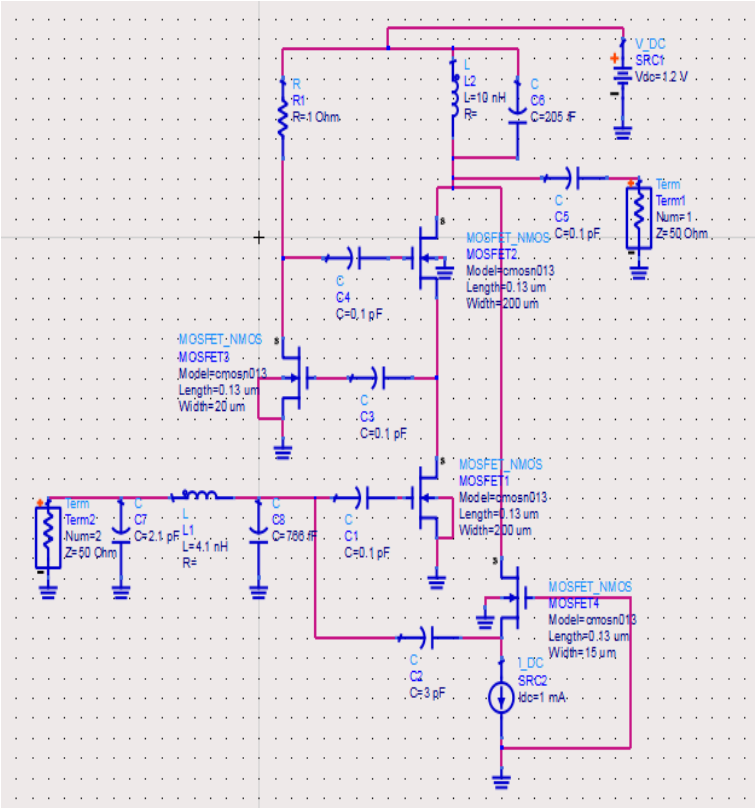

Fig. 7 Schematic of LNA

The M1 transistor is used as common source (CS) stage; cascode structure is formed by M1 and M2. Gate of M3 and drain of M1 are connected and M3 transistor's output is given to base of M2; for boosting the gain by increasing the drain resistance of M2. M3 and R1 form another CS amplifier. To improve input third order intercept point (IIP3), M4 transistor is used in common gate (CG) mode as an auxiliary transistor. C6 and L2 are used as load and C7, C8, and L1 are forming π -matching [23].

In LNA, input matching is needed for maximum power transfer from the antenna to LNA, so π- matching is adapted. Small signal circuit of CS stage with π -matching is shown below in fig. 2 [24].

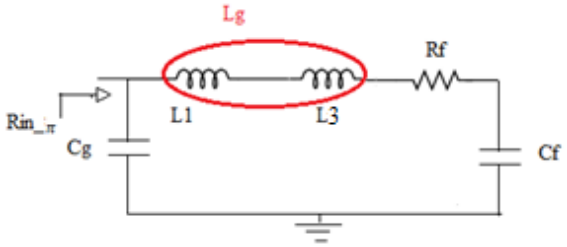

FIG. 8 SMALL SIGNAL EQUIVALENT OF CS WITH PI-MATCHING (REPRODUCED FROM [24])

The input impedance is equal to 50Ω i.e., it is purely resistive at resonance. The Lg splits into L1 and L3, in the small

signal equivalent circuit, resonating with Cg and Cf (feedback capacitor). The input impedance is given by:

$$R_{in-\pi} = \left(\frac{1}{\omega_0^2 C_g^2 R_f}\right) \approx \left(\frac{\omega_0^2 L_1^2}{R_f}\right) \quad (5)$$

ωo is operating frequency (radians).

The input capacitance is increased and because of Miller effect, the input and output terminals capacitance is amplified in the input stage of CS, hence reducing the gain. A CG transistor (M2) is inserted at the output of M1 as a current buffer, forming a cascode, to outdo this problem. This cascode configuration also increases the bandwidth of LNA. In the feed forward path, M4 acts as an auxiliary amplifier and nonlinear current is generated, and at the drain of M2, subtracts the current of M2. Therefore this is a single-ended LNA. At the drain of M2, main amplifier (M1, M2) and auxiliary amplifier (M4) currents are added in 180º. So, at the output, currents of the auxiliary amplifier and the main amplifier subtract from each other. Although the linearity is improved, but the gain is decreased. Hence, M3 is used to boost the gain [23].

III. Simulation Results and Comparison

The LNA is simulated using Advanced Design Simulation (ADS) software. A maximum gain of 10.976 dB is provided by the low noise amplifier as shown in figure 5. 1.2 V supply voltage is required to operate this circuit. A minimum noise figure of 10.26 dB and the third intercept point of -17.0dBm is achieved at the desired frequency (2.4 GHz) for the LNA.

A. S-Parameters

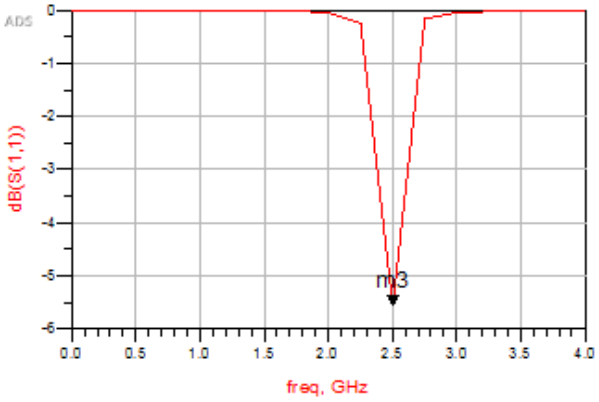

Fig. 9 Input return loss

S_{11} (input reflection coefficient) represents how much power is reflected from the antenna 1. Therefore, it is also known as input return loss. It represents the measure of matching of the input impedance to the reference impedance. The input reflection coefficient (S_{11}) for 2.4 GHz frequency is -5.562 dB as shown in figure 3.

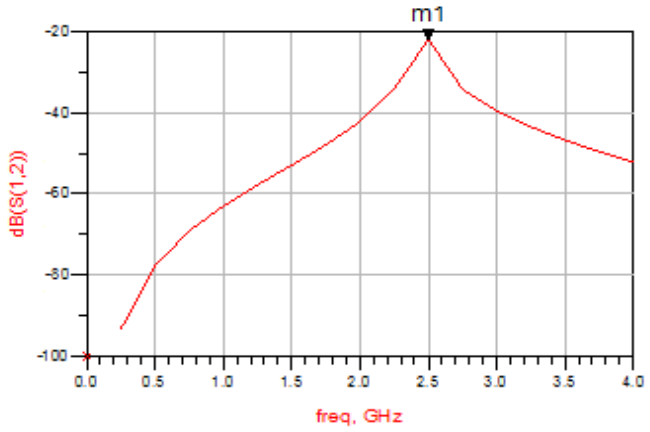

Fig. 10. Reverse transmission coefficient

S_{12} (reverse transmission coefficient) is also, known as reverse isolation, it measures how much the input signal is reflected back. The reverse transmission coefficient (S_{12}) at 2.4 GHz frequency is -22.063 dB as shown in figure 4.

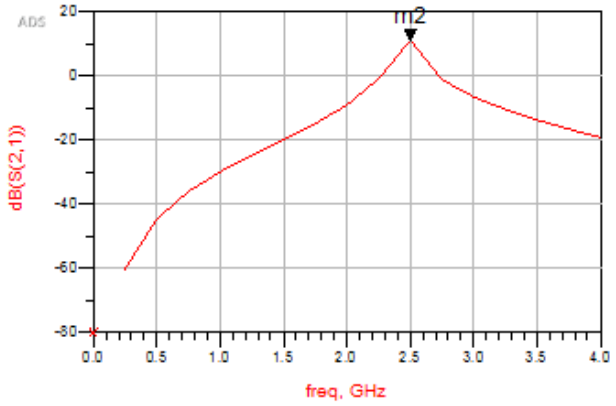

Fig. 11. Forward Gain

S_{21} (forward transmission coefficient) is also, known as forward gain, it measures how well the signal goes from input to output. The forward transmission coefficient (S_{21}) at 2.4 GHz frequency is 10.976 dB as shown in figure 5.

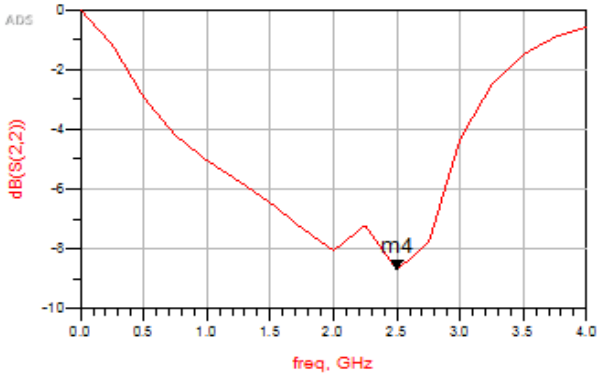

Fig. 12. Output reflection coefficient

S_{22} (output reflection coefficient) represents power reflected from antenna 2. Also, known as output return loss, it represents the measure of matching of the output impedance to load impedance. The output reflection coefficient (S_{22}) at the 2.4 GHz frequency is -8.707 dB as shown in figure 6.

B. Noise Figure

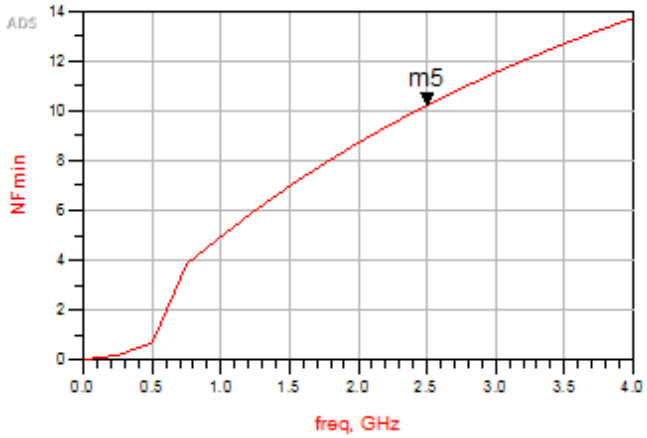

Fig. 13 Noise figure

The noise performance of device at high frequency is indicated by NF. The minimum NF of 10.26 dB has been obtained at 2.4 GHz, as shown in figure 7.

C. Third order intercept point

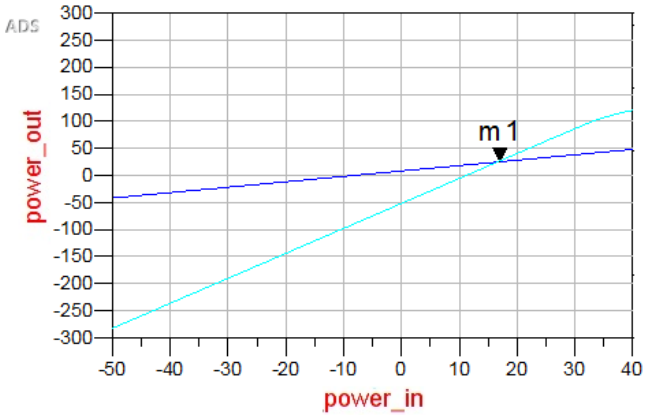

Fig. 14. Third order intercept point

LNA along with amplification of signal and good noise performance, should be linear even when the signal is strong. Hence, during designing of LNA, linearity is an important consideration. The third order intercept point (IIP3) is the most typical measure of linearity [26]. The third intercept point is illustrated in figure 8 that was achieved at 17.0 dBm, showing that the LNA achieves good gain and noise performance without affecting its linearity. In fact, the linearity of the LNA is quite high.

D. Stability

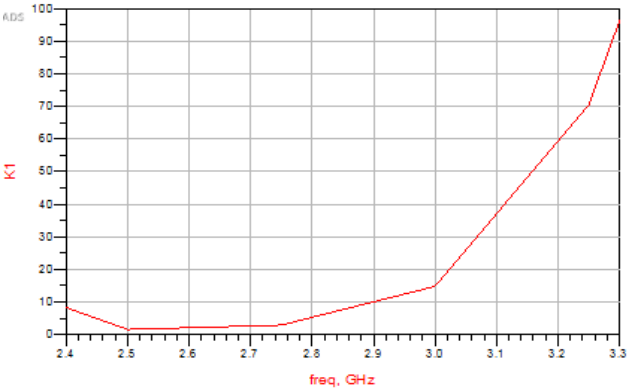

Fig. 9 Stability

At K1 > 1, the designed circuit is stable unconditionally, and the stability factor is defined as:

$$K1=\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}$$

where, $\Delta= |S_{11}S_{22} - S_{12}S_{21}|$

The decrease in the absolute value of S_{12} is observed when input and output matching is good and hence, stability factor K1 increases. The designed LNA is stable unconditionally, as shown in figure 9.

TABLE 2. COMPARISON OF REPORTED SINGLE ENDED CMOS LNAS WITH CURRENT LNA DESIGN

Ref. No.	[24]	[21]	[26]	This work
Technology (µm)	0.18	0.13	0.13	0.13
S_{11} (dB)	-13.9	-26.9	-27.63	-5.562
S_{21} (dB)	20.98	23.9	18.56	10.976
NF (dB)	4.2	5.6	1.85	10.26
IP_3 (dBm)	-5.17	-5.8	-7.75	17.0
Frequency (GHz)	2.4	2.4	2.4	2.4
Supply (V)	1	1.2	1.2	1.2

From table II, it can be observed that compared to 0.18µm technology LNA, gain of the designed LNA is moderately reduced but linearity is highly increased. Also, the noise figure of the circuit degrades. Among 0.13µm technology LNAs, the linearity of our designed LNA has increased significantly. Although, gain and linearity are two opposite parameters and hence, are difficult to balance; gain will be degraded automatically while trying to improve the linearity and vice versa [23]. Still we are able to obtain moderate gain (10dB) along with high linearity (17dBm), as compared to other 0.13µm technology LNAs.

IV. CONCLUSION

This paper describes the design of a single-ended CMOS LNA with 0.13µm technology, operating at 2.4 GHz. As compared to the already reported LNAs designed using the technology of 0.13µm, the designed LNA's linearity is increased substantially. High third intercept point and moderate value of gain are achieved by making use of π-matching network (to realize the input matching).

ACKNOWLEDGMENT

One of the authors (Aditi) acknowledges the fellowship support she is receiving from Delhi Technological University (DTU), for carrying out this work, as a part of her Master of Technology Thesis work in the domain of Microwave and Optical Communication. She also acknowledges the guidance support from her thesis mentor, Dr. Malti Bansal, Assistant Professor, Department of Electronics and Communication Engineering, DTU, for carrying out this research work.

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A High Gain, High Linearity and Low Noise LNA for IEEE 802.15.4 ZigBee Standard in 2.4 GHz ISM Band

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***Abstract*— A high gain, high linearity and low noise figure inductively degenerated cascode CMOS LNA with feedforward distortion cancellation (FDC) technique has been fabricated in this paper using 0.13µm CMOS technology. The low noise is optimized for working in the 2.4 GHz frequency band range. The inductive degeneration topology with pi-matched input and using FDC technique provides low noise figure, very high gain and high IIP3. Advanced Design System (ADS) software is used for simulation. The fabricated LNA uses 1.2V supply voltage and it exhibits a gain of 23.032 dB, noise figure of 0.988 dB, input reflection coefficient (S11) of -9.403 dB, reverse gain (S12) of -21.732 dB and an IIP3 of 14.**

***Index Terms*—ADS (Advanced Design Simulation Software); LNA (Low Noise Amplifier); FDC (Feedforward Distortion Cancellation); NMOS (N-Type MOSFET), CMOS (Complementary MOSFET); Inductively degenerated cascode; IIP3 (Third order intercept point);**

I. INTRODUCTION

Low-noise amplifier (LNA) is the first stage of receiver and is an important component of wireless telecommunication systems [1] [2]. Firstly, its main function is to overcome the noise of subsequent stages (such as mixers) by providing enough gain, i.e., it should have high gain. Secondly, minimize the effect of the overall noise performance by adding as little noise as possible, i.e., it should have low noise figure itself. Thirdly, large signals should be accommodated without distortion by an LNA, i.e., it should provide good linearity. A specific impedance of 50 ohms must be provided by LNA to the input source and output load. Also, low power consumption should be there especially in portable systems [3]. However, LNA design consists of trade-offs between gain, noise figure, linearity, input and output matching, and power consumption. Also, there is also a constant desire of keeping the size of the communication devices and the power consumption to as minimum as possible. Fortunately because of advancements in integrated circuit (IC) technology, low-cost and compact implementation is possible [4]. One of the widely used LNA topology to optimize circuit performance is conventional cascode topology. The common source (CS) stage and common gate (CG) stage are connected in series in cascode configuration [5]. It offers high gain and low DC power consumption since its two gain stages have same DC path and also, common gate stage provides good isolation and common source stage provides better noise figure, but fails to deliver the linearity required by the system [6].

LNA design where common source transistor in cascode topology employs inductive degeneration technique is used to fulfill this requirement. The proposed schematic of inductive degeneration topology is shown in figure 1.

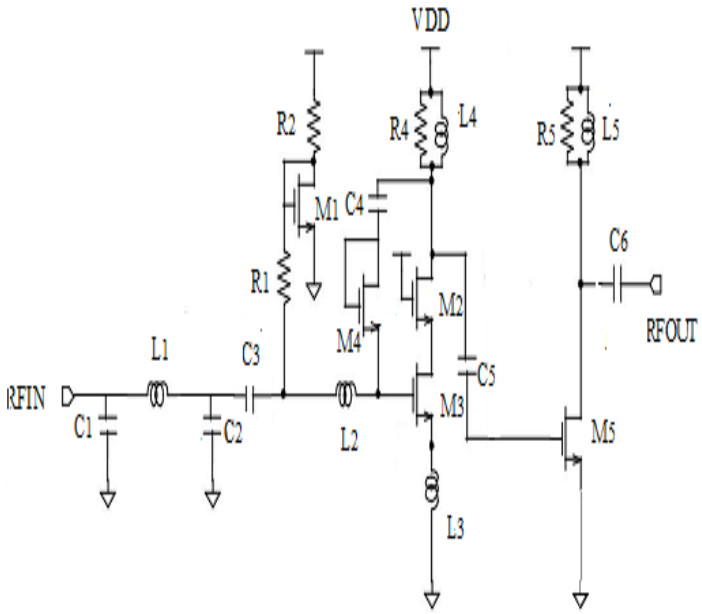

Fig. 1 Proposed Inductively-Degenerated CMOS cascode LNA

The transistor and degeneration inductor combination provides input matching. The impedance at the input is given by:

$$\text{Zin}=s(L_g + L_s) + \frac{1}{(sC_{gs})} + \frac{g_m L_s}{C_{gs}} \quad (1)$$

where,

$$\text{Input resistance= Rin}=R_e[Z_{in}] = \frac{g_m L_s}{C_{gs}} \quad (2)$$

Gain of LNA is given by:

$$\frac{V_{out}}{V_{in}} = \frac{-g_m s L_d}{1-\omega^2 C_{gs}(L_g+L_s)+sL_s g_m} \quad (3)$$

Also, at resonant frequency,

$$\omega^2 = (L_g + L_s)C_{gs} = 1 \quad (4)$$

Therefore, by substituting (4) in (3)

$$\frac{V_{out}}{V_{in}} = \frac{-g_m s L_d}{sL_s g_m} = \frac{-L_d}{L_s} \quad (5)$$

Hence, the ratio of inductor at drain to inductor at source is the gain. So far, most of the distortion cancelling LNA, to overload main circuit, employ complex architecture (as reported) which requires large area and additional components, and hence consumes more power [7][8]. A simple feed forward distortion cancellation (FDC) technique is used which uses a simple capacitor and diode connected transistor without any additional DC path to improve linearity, without degrading noise figure (NF) and input matching; FDC uses additional path, to improve linearity, by generating distortion which cancels initial LNA's distortion [9]. However, linearity and gain are two opposite poles which are difficult to balance as while improving gain, linearity gets degraded and vice versa. So, pi-matching is used to enhance the forward gain of LNA by providing additional degree of freedom [10].

II. CIRCUIT DESIGN

Figure 1, presents the proposed LNA having basic cascode structure comprising of M2 in common source amplifier configuration and M3 in common gate amplifier configuration. However, due to capacitance amplification between the input and output terminals, the equivalent input capacitance of an inverting voltage amplifier increases. The main reason for the low gain is Miller effect. Therefore, a common gate transistor (M2) is used as a current buffer at the output of M3 to overcome this problem. So, the cascode configuration is used to increase the reverse isolation of the circuit and provide high gain by reducing Miller effect. Furthermore, R4 and L4 serve as cascode stage (M2-M3) load. The feed-forward distortion cancellation is provided by the diode connected NMOS transistor (M4) based on weak inversion region and capacitor C4, to improve linearity. At the gate of M3, the M4 transistor senses the signal and at the cascode pair output, the M4 transistor generates the negative third order non-linearity coefficient. Hence, cancelling the distortion generated by the cascode pair which is positive third order non-linearity coefficient as the M2 and M3 transistor are based on strong inversion region. To maintain DC voltage at the drain of M2, C4 is used. So, basically C4 is a blocking capacitor. Pi-matching network formed by C1, L1 and C2 is used to obtain input impedance matching while R5, L5 and C6 are used to obtain output matching. The M5 transistor is a common source stage which along with the load facilitates output matching and also increases the gain of the LNA further. R5-L5 serve as the load M5. The schematic of the proposed circuit in ADS is shown in figure 2.

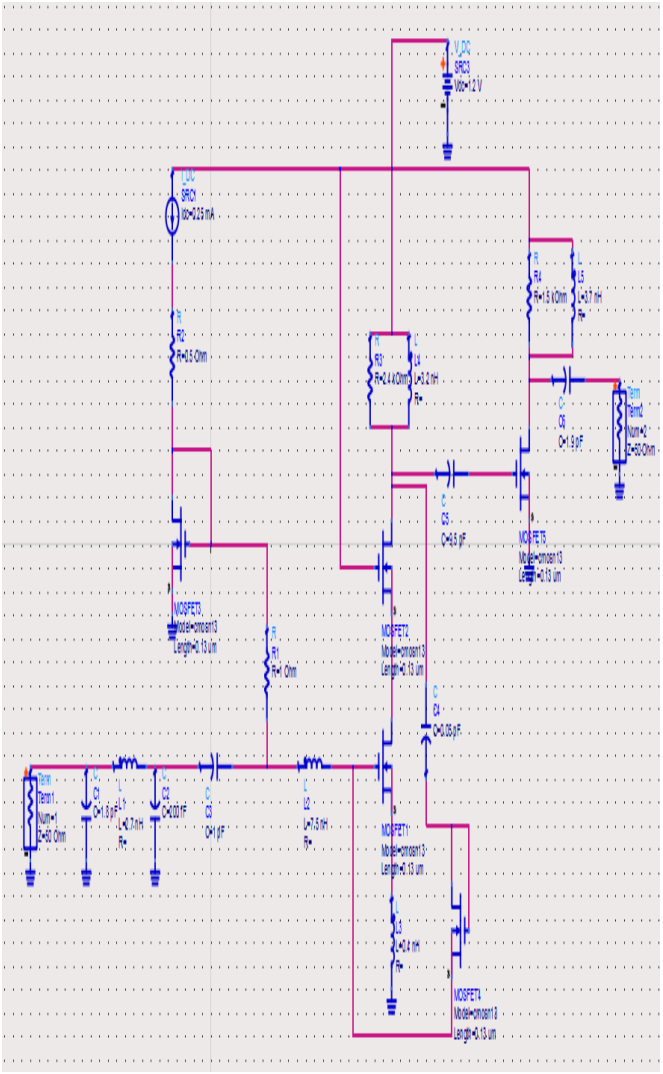

FIG. 2 SCHEMATIC OF PROPOSED CIRCUIT IN ADS

III. SIMULATION AND RESULTS

Simulations of the LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S21) of 23.023 dB as shown in figure 5. The input reflection coefficient (S11) is -9.403 dB as shown in figure 3 and the output reflection coefficient (S22) is -4.730 dB as shown in figure 6. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S12) as shown in figure 4 is –21.732 dB and a minimum noise figure of 0.988 dB is obtained as shown in figure 7. The simulated IIP3 result is shown in figure 8, and IIP3 of 14 dBm is obtained. From the result, it can be concluded that very high gain and a high linearity with low noise figure have been achieved. The simulated amplifier's characteristics summary is presented in Table I. From Table I, compared with other LNA's, the performance of our proposed CMOS LNA is much better as it has the best reported value of NF and linearity at 2.4GHz.

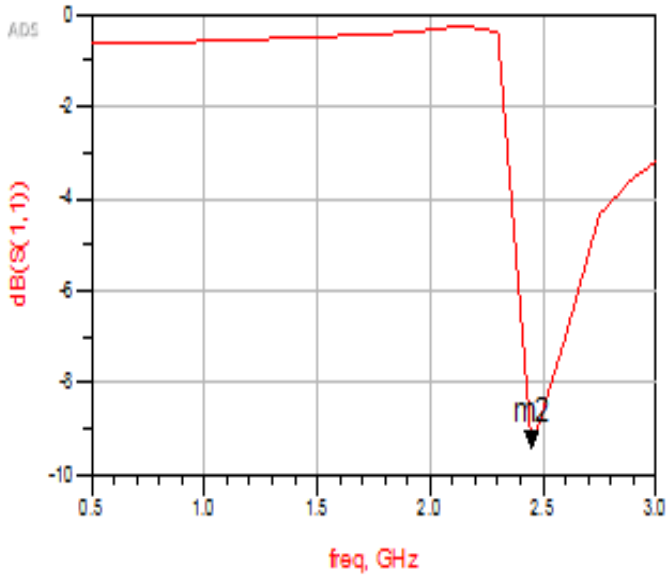

Fig. 3 Input Reflection Coefficient (S_{11})

S_{11} (input reflection coefficient) represents how much power is reflected from the antenna 1. Therefore, it is also known as input return loss. It represents the measure of matching of the input impedance to the reference impedance. For 2.4 GHz, as shown in figure 3, the value of S11 is -9.408 dB. Since, the value of input reflection coefficient is less than -9 dB, the input impedance is approximately matched to 50 Ω impedance.

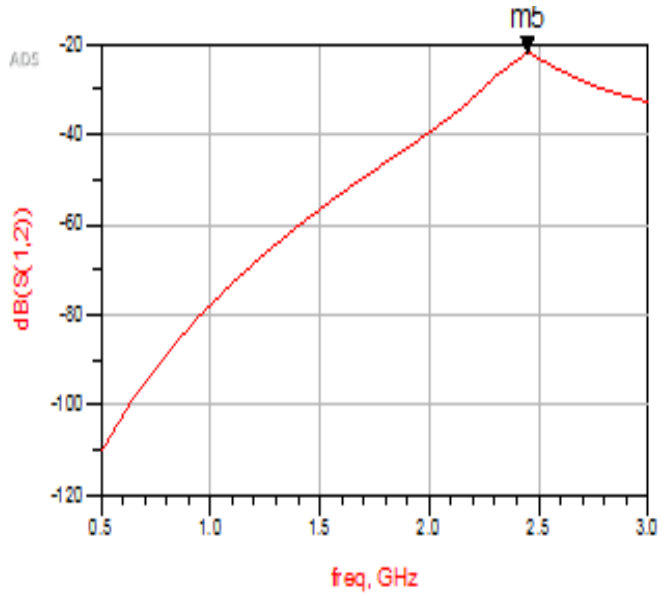

Fig. 4 Reverse Gain/ Reverse Isolation (S_{12})

S_{12} (reverse transmission coefficient) represents power received at antenna 1 relative to power input at antenna 2. Also, known as reverse isolation, it measures how much the input signal is reflected back. For 2.4 GHz, as shown in figure 4, the value of S12 is -21.732 dB indicating that a very high isolation is present between the input and the output.

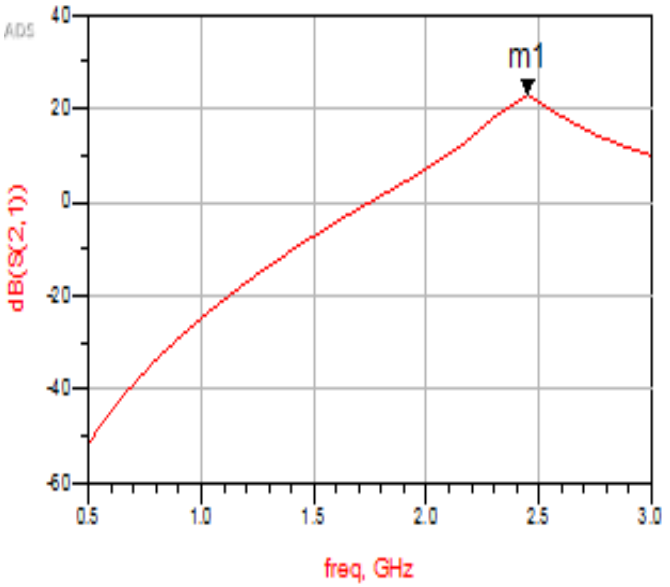

Fig. 5 Forward Gain (S_{21})

S_{21} (forward transmission coefficient) represents power received at antenna 2 relative to power input at antenna 1. Also, known as forward gain, it measures how well the signal goes from input to output. For 2.4 GHz, as shown in figure 5, the value of S21 is 23.032 dB. Therefore, a high output voltage is obtained even for a small value of input voltage.

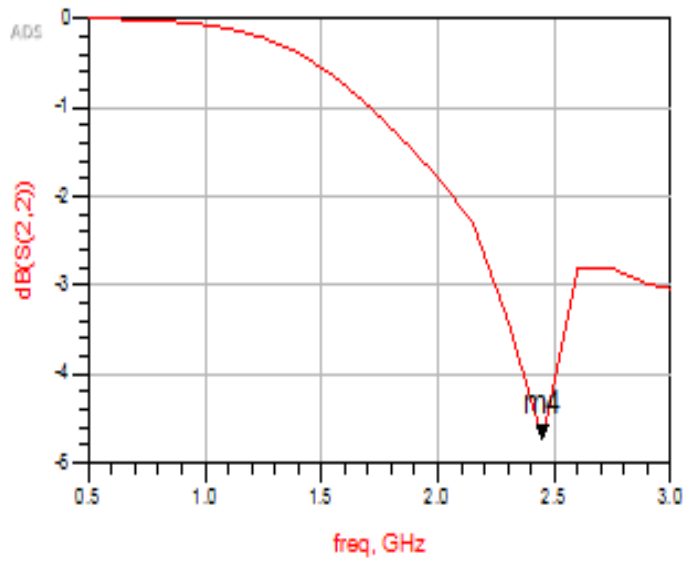

Fig. 6 Output Reflection Coefficient (S_{22})

S_{22} (output reflection coefficient) represents power reflected from antenna 2. Also, known as output return loss, it represents the measure of matching of the output impedance to load impedance. For 2.4 GHz, as shown in figure 6, the value of S22 is -4.730 dB indicating that a considerable matching of the output impedance to 50 Ω is obtained.

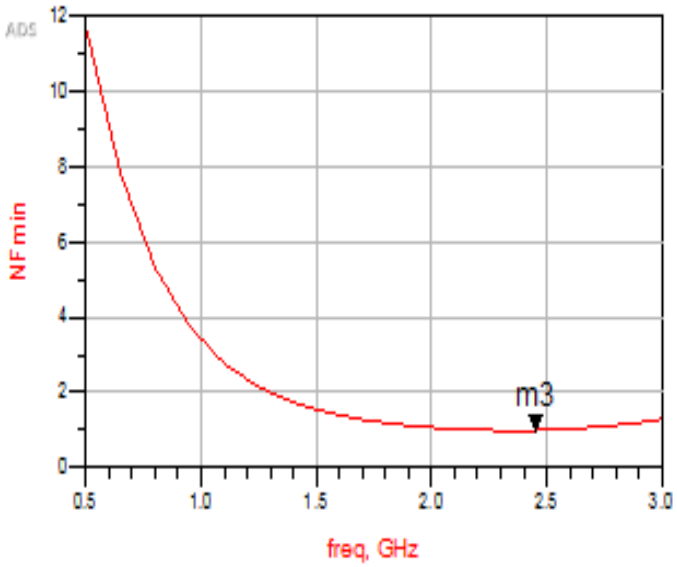

Fig. 7 Noise Figure (NF)

The noise performance of device at high frequency is indicated by noise figure. The minimum noise figure of 0.988 dB has been obtained at 2.4 GHz, as shown in figure 7. This value indicates that the noise performance of the circuit is very high as the value of noise figure of the circuit is very low.

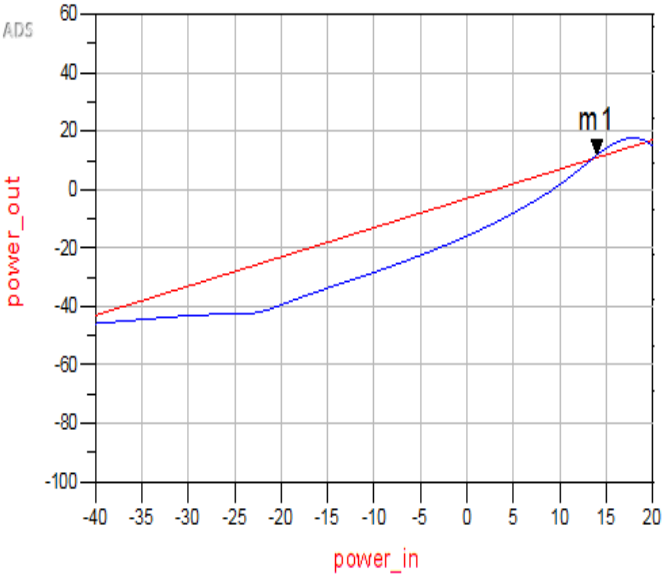

Fig. 8 IIP3

LNA along with amplification of signal and good noise performance, should be linear even when the signal is strong. Hence, during designing of LNA, linearity is an important consideration. The third order intercept point (IIP3) is the most typical measure of linearity [11]. The third intercept point is illustrated in figure 8 that was achieved at 14.0 dBm, showing that the LNA achieves good gain and noise performance without affecting its linearity. In fact, the linearity of the LNA is quite high.

TABLE II. COMPARISON OF DIFFERENT CMOS LNAS

	[12]	**[13]**	**[14]**	**This Work**
Frequency (GHz)	2.4	2.44	2.45	2.4
Technology (µm)	0.13	0.13	0.13	0.13
Supply (V)	1.5	1.2	1	1.2
Gain (dB)	10	23	18.5	23.032
Noise Figure (dB)	1.66	3	4.38	0.988
IIP3 (dBm)	11.1	-11.5	0.7	14

From table I, it can be concluded that for 2.4 GHz frequency using 0.13µm CMOS technology, compared to other 0.13 µm CMOS LNAs operating at 2.4 GHz, the designed LNA has least noise figure of value 0.988 dB and maximum linearity of value 14 dBm, with a good value of gain (23.032 dB). So, our designed LNA is much better as compared to other LNAs at 2.4 GHz.

IV. CONCLUSION

In this paper, a 2.4 GHz CMOS LNA for IEEE 802.15.4 ZigBee standard is proposed. A conventional cascode common source inductive degeneration topology is used in designing of the low noise amplifier along with extremely simple feed forward cancellation technique to improve the linearity of the circuit. The measurement results of the proposed low noise amplifier is given in table I and is compared with the other low noise amplifier operating at 2.4 GHz frequency. Good noise figure value of 0.988 dB and high linearity of 14 dBm is achieved which shows that the proposed circuit has good stability as obtained at 1.2V power supply. Also, a high gain value of 23.032 dB is obtained.

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High Linearity and Low Noise Shunt Resistive Feedback CMOS LNA in 2.4GHz ISM Band

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***Abstract*—A shunt resistive feedback CMOS low noise amplifier (LNA) using a pi-matching network has been fabricated in this paper using 0.13µm CMOS technology. The low noise amplifier is optimized for working in the 2.4 GHz frequency band range. The shunt resistive feedback topology with pi-matched input provides low noise figure, moderate gain and high linearity. Advanced Design System (ADS) software is used for simulation. The fabricated LNA uses 1.2V supply voltage and it exhibits a gain of 15.417 dB, noise figure of 1.182 dB, input reflection coefficient (S_{11}) of -9.170 dB, reverse gain (S_{12}) of -18.909 dB and an IIP3 of 8 dBm.**

***Index Terms*—Advanced Design Simulation (ADS) Software, Low Noise Amplifier (LNA), Complementary MOSFET (CMOS), Common Source (CS), Common Gate (CG), Noise Figure (NF), Resistive Feedback.**

I. INTRODUCTION

The demand for highly integrated radio frequency circuits having low noise, high gain and low power dissipation is increasing due to tremendous growth of wireless communication technology. An important block of RF receivers is Low noise amplifier (LNA) which is also the first block of RF receiver [1]. The signal received by the antenna is very small. So, it is important to amplify the signal as much as possible without noise addition and also; attaining good linearity, high gain and low power consumption at the same time [2][3]. For designing of LNA, the most optimum tradeoff between various parameters has to be achieved. Also, the size of communication devices and power consumption should be as minimum as possible, which is possible nowadays because of advancements in integrated circuit (IC) technology [4].

Many structures have been developed for wideband CMOS LNA to achieve desired values of parameters, in which the first stage of LNA is common source or common gate configuration. Common gate configuration is commonly used as compared to inductively degenerated common source configuration for wideband application because the input matching network has low value of quality factor and hence, leading to good wideband input matching [5][6], low power consumption and less reverse transmission and high linearity. However, the transconductance of the input transistor is limited because of low noise performance. So, an alternate and most widely used topology for wideband application is the shunt resistive feedback topology. Flat gain and input impedance matching is provided by resistive feedback [7]. The proposed common-source cascode amplifier using shunt feedback topology is shown in figure 1. The advantage of high gain and wide bandwidth, of the cascode is utilized by this amplifier; and more stability in wide band application is obtained due to shunt resistive feedback [8].

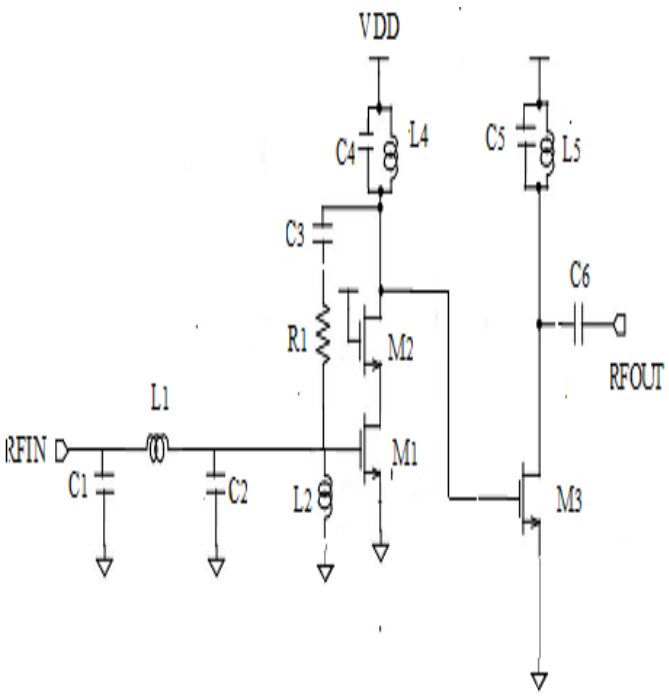

Fig. 15 Proposed Common Source Shunt Resistive Feedback CMOS LNA

The impedance at the input is given by [9]:

$$Z_{IN} = sL_G + \left[\frac{1}{sC_{gs}} // \frac{R_f + R_L}{1 + g_m R_l}\right]$$

$$= sL_G + \frac{1}{sC_{gs}\left(1+\frac{1}{{Q_L}^2}\right)} + \frac{R_f+R_L}{(1+g_m R_L)(1+{Q_L}^2)}$$

At resonant frequency (ωo),

$$Z_{IN} = \frac{R_f+R_L}{(1+g_m R_L)(1+{Q_L}^2)} \quad (1)$$

where,

$$Q_L = \frac{\omega_o L_G}{R_s} \quad (2)$$

The noise factor for the proposed LNA topology is

$$F = 1 + \frac{\gamma}{\alpha}\left[\frac{1}{g_m R_s} + 2|c|\sqrt{\frac{\alpha^2\delta}{5\gamma}}\left(\frac{\omega_o}{\omega_T}\right) + \frac{\alpha^2\delta}{5\gamma} g_m R_s \left(\frac{\omega_o}{\omega_T}\right)^2\right] \quad (4)$$

Linearity and gain are two opposite poles which are difficult to balance as while improving gain, linearity gets degraded and vice versa. So, pi-matching is used to enhance the forward gain of LNA, by providing additional degree of freedom [10].

II. Circuit Design

The schematic for the proposed low noise amplifier topology is shown in figure 2. This is a very simple low noise amplifier topology making it suitable for low cost LNA applications (ideally). The first stage consists of two transistors, one is a common source stage and other is a common gate stage. The two transistors are connected in cascode configuration. Although, the gain of the common source stage is not large in cascaded configuration, but its benefit is that it has negligible Miller effect on M1 transistor. Here, R1 is used as the feedback resistor and C3 is used as the blocking capacitor. The feedback resistor is placed in shunt to achieve broadband matching of input and also to get negative feedback so as to improve stability factor, that provides unconditional stability of the amplifier and reduces the gain sensitivity. L4 and C4 serve as cascode stage loading elements, formed by the inductor in parallel with a capacitor. The second stage is a source follower stage which is used to extend the bandwidth further and to achieve high gain. This stage also provides matching of the output impedance. L1, C1 and C2 form pi – matching network which is used at input to improve linearity of the circuit and to achieve input impedance matching.

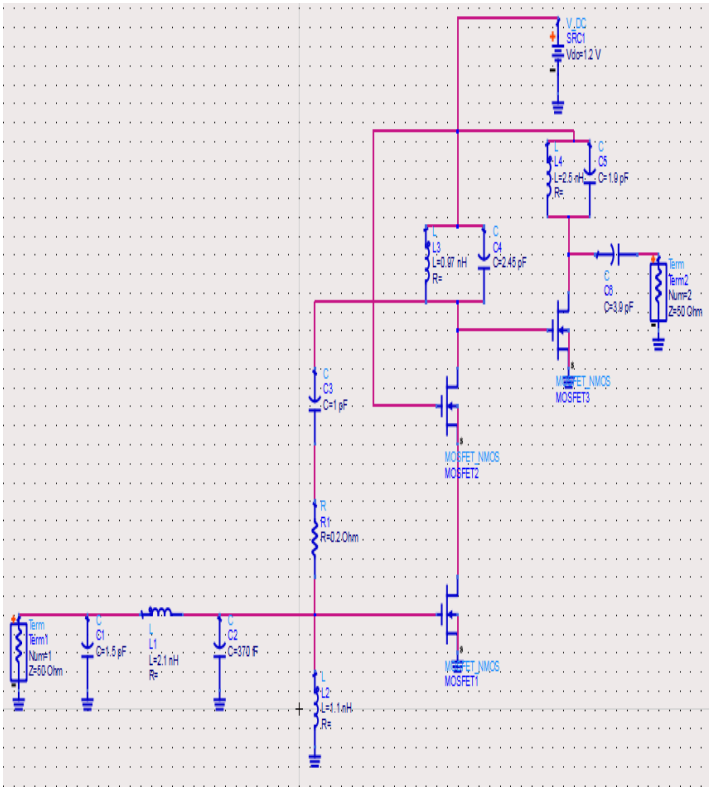

Fig. 16 Schematic of proposed circuit in ADS

III. Simulation and Results

Simulations of the proposed LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S21) of 15.417 dB as shown in figure 5. The input reflection coefficient (S11) is -9.170 dB as shown in figure 3 and the output reflection coefficient (S22) is -6.024 dB as shown in figure 6. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S12) as shown in figure 4 is –18.909 dB and a minimum noise figure of 1.182 dB is obtained as shown in figure 7. The simulated IIP3 result is shown in figure 8, and IIP3 of 8 dBm is obtained. From the result, it can be concluded that very high gain and a high linearity with low noise figure have been achieved. The simulated amplifier's characteristics summary is presented in Table I. From Table I, compared with other LNA's, the performance of our proposed CMOS LNA is much better as it has the best reported value of NF at 2.4GHz.

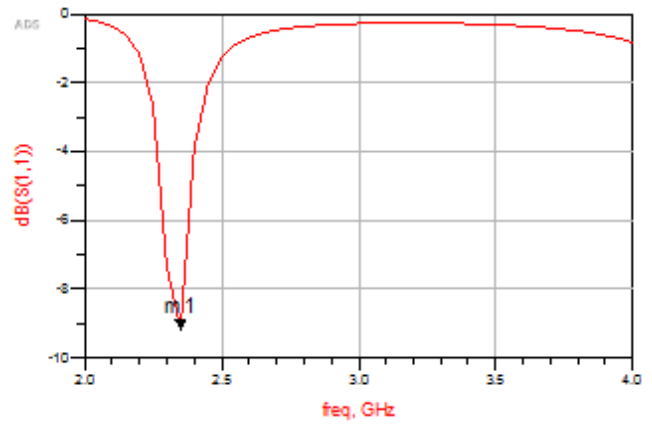

Fig. 3 Input Reflection Coefficient (S_{11})

S_{11} (input reflection coefficient) represents how much power is reflected from the antenna 1. Therefore, it is also known as input return loss. It represents the measure of matching of the input impedance to the reference impedance. For 2.4 GHz, as shown in figure 3, the value of S11 is -9.170 dB.

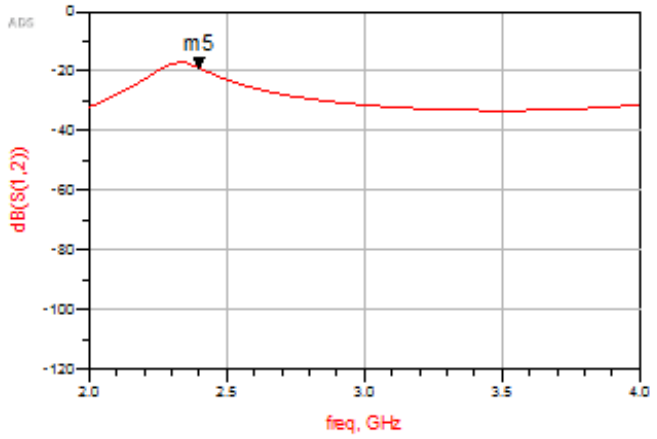

Fig. 4 Reverse Gain/ Reverse Isolation (S_{12})

S_{12} (reverse transmission coefficient) represents power received at antenna 1 relative to power input at antenna 2. Also, known as reverse isolation, it measures how much the input signal is reflected back. For 2.4 GHz, as shown in figure 4, the value of S12 is -18.909 dB.

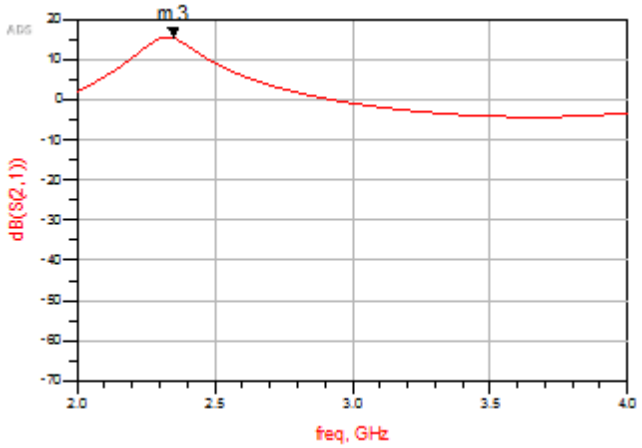

Fig. 5 Forward Gain (S_{21})

S_{21} (forward transmission coefficient) represents power received at antenna 2 relative to power input at antenna 1. Also, known as forward gain, it measures how well the signal goes from input to output. For 2.4 GHz, as shown in figure 5, the value of S_{21} is 15.417 dB.

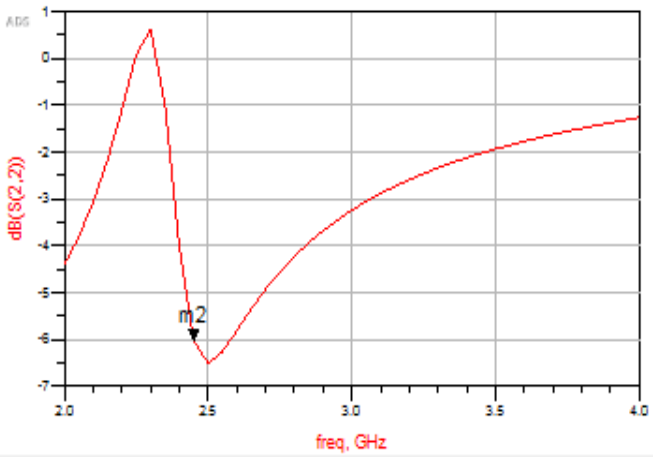

Fig. 6 Output Reflection Coefficient (S_{22})

S_{22} (output reflection coefficient) represents power reflected from antenna 2. Also, known as output return loss, it represents the measure of matching of the output impedance to load impedance. For 2.4 GHz, as shown in figure 6, the value of S22 is -6.204 dB.

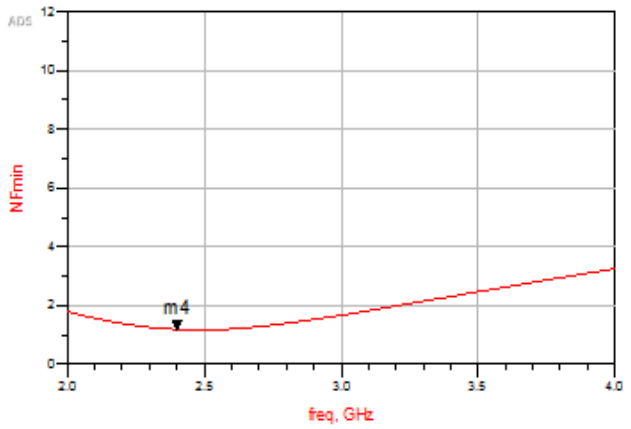

Fig. 7 Noise Figure (NF)

The noise performance of device at high frequency is indicated by noise figure. The minimum noise figure of 1.182 dB has been obtained at 2.4 GHz, as shown in figure 7.

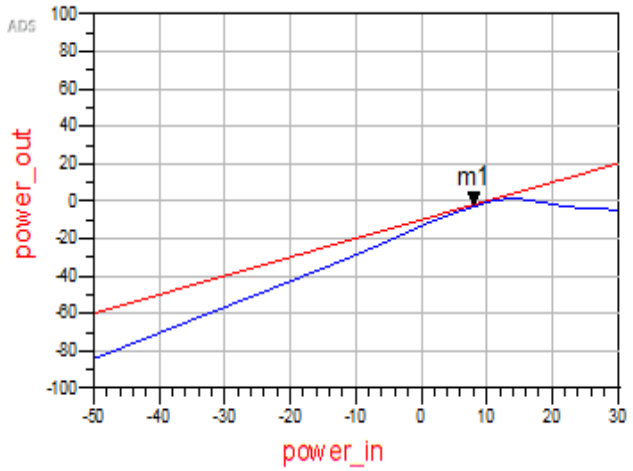

Fig. 8 IIP3

LNA along with amplification of signal and good noise performance, should be linear even when the signal is strong. Hence, during designing of LNA, linearity is an important consideration. The third order intercept point (IIP3) is the most typical measure of linearity [11]. The third intercept point is illustrated in figure 8 that was achieved at 8.0 dBm, showing that the LNA achieves good gain and noise performance without affecting its linearity. In fact, the linearity of the LNA is quite high.

TABLE I. COMPARISON OF DIFFERENT CMOS LNAS

	[9]	[12]	This Work
Frequency (GHz)	2.4	3.4	2.4
Technology (µm)	0.13	0.13	0.13
Supply (V)	1.2	1.2	1.2
Gain (dB)	28.3	20.8	15.417
Noise Figure (dB)	2.0	2.2	1.182
IIP3 (dBm)	-22.4	-11.5	8

From the table I, it can be concluded that for 2.4GHz frequency at 0.13µm technology, compared to other LNAs, the designed LNA has least noise figure (of value 1.182 dB) and maximum linearity (of value 8 dBm), with a good value of gain (15.417 dB). So, our designed LNA, in terms of linearity and noise, is much better as compared to other reported LNAs at 2.4 GHz.

IV. CONCLUSION

In this paper, a 2.4GHz CMOS LNA for IEEE 802.15.4 ZigBee standard is proposed. Good noise figure value of 1.182 dB and high linearity of 8 dBm is achieved which shows that the proposed circuit has good stability, as obtained at 1.2V power supply. Also, a reasonably good gain value of 15.417 dB is obtained.

ACKNOWLEDGMENT

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High Linearity and High Input Impedance Matching Common Gate CMOS LNA in 2.4GHz ISM Band

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***Abstract*— A high linearity and low input reflection coefficient (<-10 dB) common gate CMOS LNA has been fabricated in this paper using 0.13µm CMOS technology. The low noise amplifier is optimized for working in the 2.4 GHz frequency band range. The common gate topology with pi-matched input provides high IIP3 and best input matching characteristics. Advanced Design System (ADS) software is used for simulation. The fabricated LNA uses 1.2V supply voltage and it exhibits a linearity of 12 dBm, input reflection coefficient (S11) of -26.894 dB, reverse gain (S12) of -18.604 dB, noise figure of 3.513 dB, and gain of 7.526.**

***Index Terms*— ADS (Advanced Design Simulation) Software; LNA (Low Noise Amplifier); CMOS (Complementary MOSFET); Common Gate (CG); Noise Figure (NF), IIP3 (Third order intercept point)**

I. Introduction

The front-end of wireless communication receivers are becoming sophisticated day-by-day as they employ complex functionalities and provide high flexibility, which is demanded by the consumers and moreover, the standards are continuously evolving. The major block present in the front end of the RF receiver is the low noise amplifier (LNA). The performance of low noise amplifier affects the performance of complete RF receiver system as by knowing the specification of low noise amplifier, we can estimate the overall noise performance of wireless receivers [1]. In the receiver, the noise figure of the stages following low noise amplifier is decreased when the low noise amplifier has high gain and low noise figure. Hence, low noise amplifier's important characteristics is to amplify the received signal without adding internal noise. However, due to constant demand of reduction in the sizes of devices and low supply voltage, it is difficult to achieve low noise figure at advanced technology while having linearity, as dictated by wireless standards. Also, specifications of low noise amplifier such as noise figure, linearity, gain and input matching trade amongst each other [2]. Low noise amplifiers are used in variety of applications. RF communication systems, two way radio, personal digital assistant (PDA) and laptops etc., are some of the examples in which low noise amplifiers are used. The inductively degenerated common-source (CS) low noise amplifier topology is commonly used for narrowband applications as higher gain and lower noise figure is provided by this topology but it is difficult to achieve impedance matching at the input when compared to common gate (CG) low noise amplifier topology, below 10 GHz. Moreover, the number of inductors required by inductively degenerated common source LNA topology (4 or 6 for differential amplifier) is more as compared to common gate low noise amplifier topology. Hence, area on chip occupied by inductively degenerated common source low noise amplifier topology is more [3] [4]. Therefore, the common gate (CG) low noise amplifier topology has been proposed in this paper and proposed circuit as shown in figure 1, is utilized for input matching. However, due to impedance matching constraint, common gate low noise amplifier has low gain and high noise figure [5] [6].

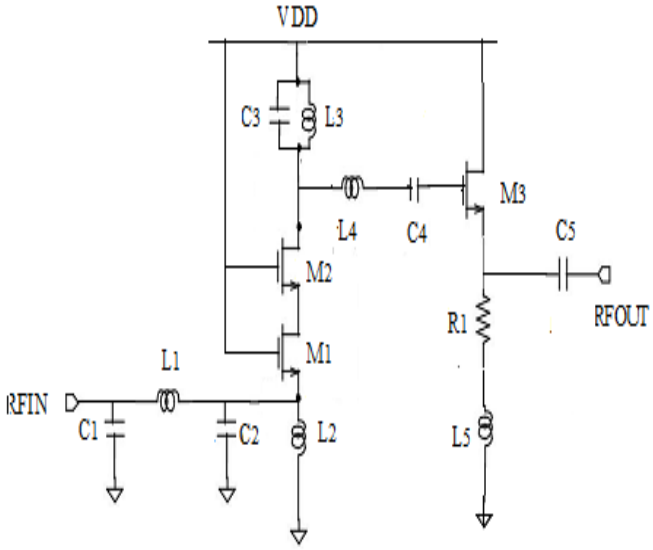

Fig. 1 Proposed Common Gate CMOS LNA

In conventional common gate (CG) low noise amplifier topology, the transconductance of the main transistor should be inverse of source resistance i.e. 1/gm = Rs, for input matching. For the entire frequency range of operation, this condition should hold true.

The transconductance of short channel devices is given by [7]:

$$g_m = \left[\frac{\mu C_{ox}}{2}\right] * \left[\frac{W}{L}\right] * \left[\frac{1}{\theta}\right] \quad (1)$$

where,

W and L are the channel width and length of main transistor respectively, and θ is a fitting parameter.
From equation (1), it can be observed that the transconductance (gm) of main transistor is independent of biasing current [7]. Therefore, channel width of main transistor (W) depends on the technology and its value is given by:

$$W_{0pt} = \left[\frac{2}{\mu C_{ox}}\right] * [\theta * L * g_m] \quad (2)$$

Since, linearity and gain are two opposite poles which are difficult to balance, as while improving gain, linearity gets degraded and vice versa. So, pi-matching is used to enhance the forward gain of LNA by providing additional degree of freedom [8].

II. Circuit Design

The complementary MOS (CMOS) transistor is used in low noise amplifiers because of its good characteristics. High immunity against noise and static power are two of the important characteristics of CMOS transistors. The internal structure of CMOS contains a NMOS and PMOS transistor in series. So, the power is drawn by the series combination momentarily when there is switching between ON and OFF states, because one of the transistor in the series connection is always OFF. Hence, the heat produced by CMOS devices is less as compared to other logic families such as transistor transistor logic (TTL), NMOS, etc.

The proposed LNA consists of common gate and common source stages, of which at the first stage, for the input matching, the common gate topology is adopted. Parallel resonance is present instead of series resonance for the input matching of common gate amplifier. The quality factor (Q) of common gate amplifier is given as [9]:

$$Q_{CG} = \omega_o \frac{C_{gs}}{g_m} \quad (3)$$

where,

$$\omega_0 = \frac{1}{L_s C_{gs}} \quad (4)$$

However, the power gain of common gate amplifier is lower than common source amplifier. So, a common source amplifier is used in second stage of our circuit to compensate for the power gain. To ensure that the circuit is optimized, the LC tank circuit is matched for the center frequency. To block RF current leakage to ground, inductor L2 is used. As compared to common source amplifier, the value of L2 for common gate amplifier is higher. C1, L1 and C2 form pi-matching network at input and C5 is the DC blocking capacitor.

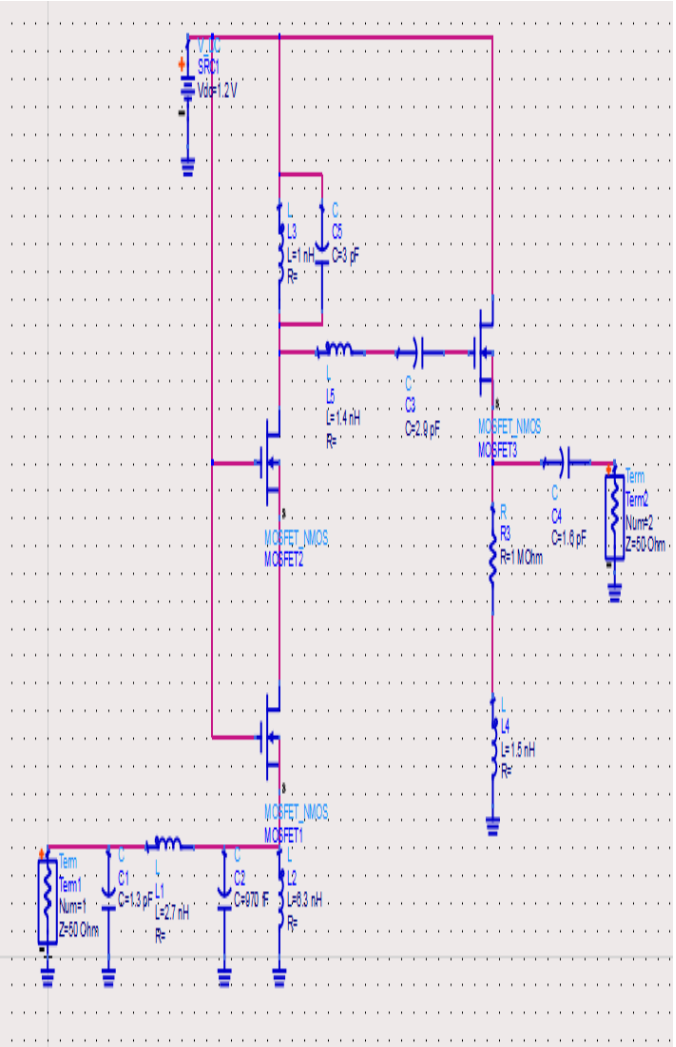

Fig 2. Schematic of Proposed Common Gate LNA

III. Simulation and Results

Simulations of the proposed LNA for 0.13 um CMOS process were performed using ADS. The low noise amplifier provides a gain (S21) of 7.526 dB as shown in figure 5. The input reflection coefficient (S11) is -26.894 dB as shown in figure 3 and the output reflection coefficient (S22) is -12.246 dB as shown in figure 6. The circuit operation requires 1.2 V power supply. The value of reverse isolation (S12), as shown in figure 4, is –18.604 dB and a minimum noise figure of 3.513 dB is obtained as shown in figure 7. The simulated IIP3 result is shown in figure 8, and IIP3 of 12 dBm is obtained. From the result, it can be concluded that high linearity and good input matching have been achieved. The simulated amplifier's characteristics summary is presented in Table I. From Table I, compared with other LNA's, the performance of our proposed CMOS LNA is much better it terms of linearity and input matching, as it has the best reported value of linearity and input reflection coefficient at 2.4GHz.

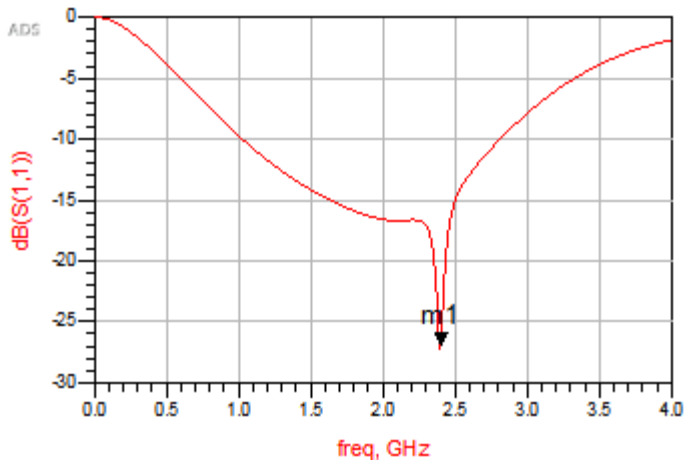

Fig. 3 Input Reflection Coefficient (S_{11})

S_{11} (input reflection coefficient) represents how much power is reflected from the input antenna. Therefore, it is also known as input return loss. It represents the measure of matching of the input impedance to the reference impedance. For 2.4 GHz, as shown in figure 3, the value of S11 is -26.894 dB.

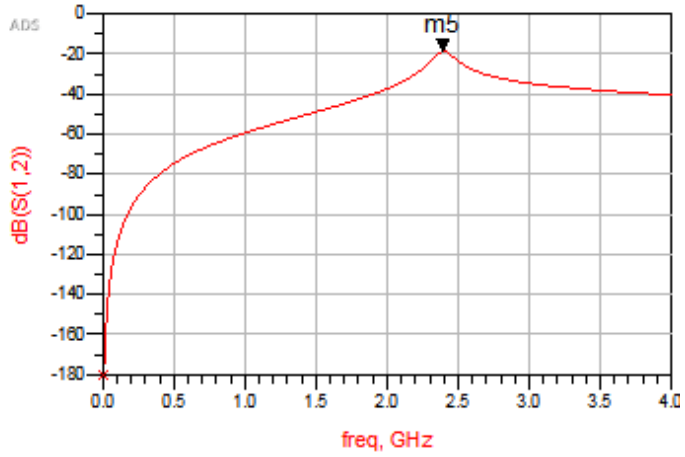

Fig. 4 Reverse Gain/ Reverse Isolation (S_{12})

S_{12} (reverse transmission coefficient) represents power received at input antenna relative to power input at output antenna. Also, known as reverse isolation, it measures how much the input signal is reflected back. For 2.4 GHz, as shown in figure 4, the value of S12 is -18.604 dB.

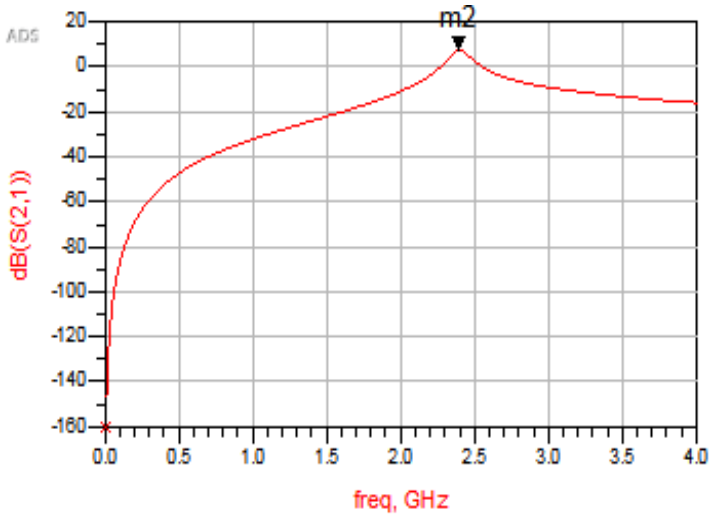

Fig. 5 Forward Gain (S_{21})

S_{21} (forward transmission coefficient) represents power received at output antenna relative to power input at input antenna. Also known as forward gain, it measures how well the signal goes from input to output. For 2.4 GHz, as shown in figure 5, the value of S21 is 7.526 dB.

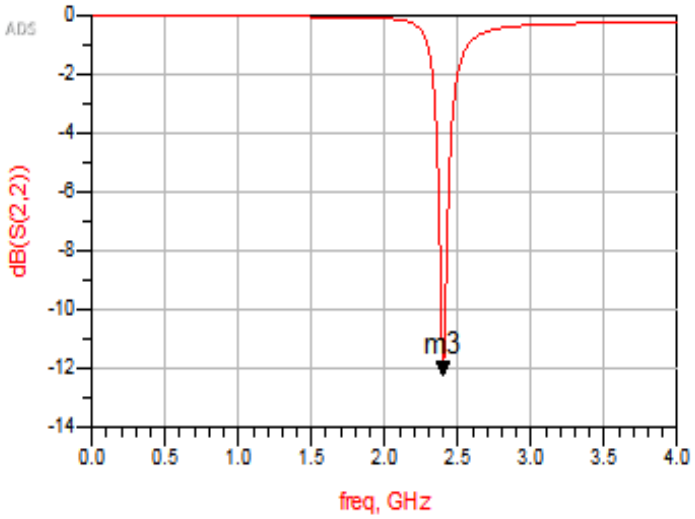

Fig. 6 Output Reflection Coefficient (S_{22})

S_{22} (output reflection coefficient) represents power reflected from output antenna. Also known as output return loss, it represents the measure of matching of the output impedance to load impedance. For 2.4 GHz, as shown in figure 6, the value of S22 is -12.246 dB.

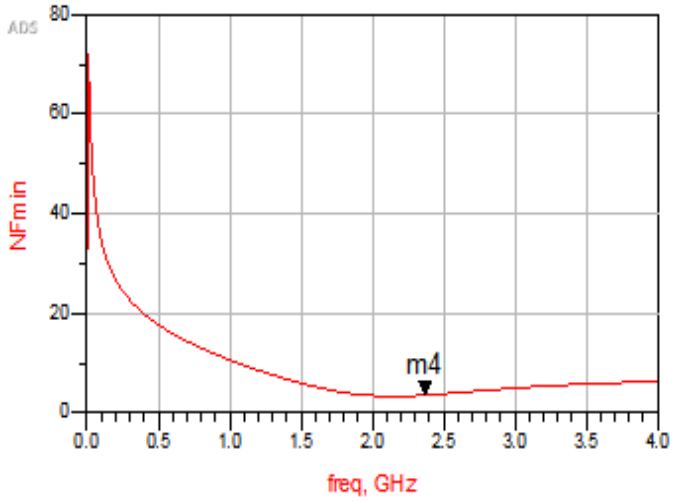

Fig. 7 Noise Figure (NF)

The noise performance of device at high frequency is indicated by noise figure. The minimum noise figure of 3.513 dB has been obtained at 2.4 GHz, as shown in figure 7.

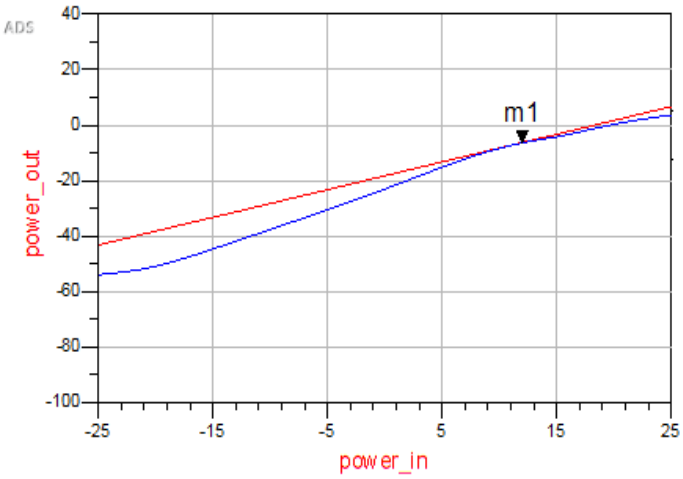

Fig. 8 IIP3

LNA along with amplification of signal and good noise performance, should also exhibit linearity, even when the signal is strong. Hence, during designing of LNA, linearity is an important consideration. The third order intercept point (IIP3) is the most typical measure of linearity [8]. The third intercept point is illustrated in figure 8 that was achieved at 12.0 dBm, showing that the LNA achieves good gain and noise performance without affecting its linearity. In fact, the linearity of the LNA is quite high.

TABLE I. COMPARISON OF DIFFERENT CMOS LNAS

	[10]	**[11]**	**This Work**
Frequency (GHz)	2.44	2.1	2.4
Technology (µm)	0.18	0.13	0.13
Supply (V)	1.8	1.2	1.2
Input reflection coefficient (dB)	-16.7	-14	-26.894
Gain (dB)	-2 ~ 12.5	5.2	7.526
Noise Figure (dB)	3.9	3	3.513
IIP3 (dBm)	-1	10.5	12

From table I, it can be concluded that for 2.4GHz frequency at 0.13µm technology, compared to other LNAs, our designed LNA has higher linearity, better noise performance and high input impedance matching. So, our designed LNA is much better in terms of linearity and input impedance matching as compared to other LNAs at 2.4 GHz.

IV. CONCLUSION

In this paper, a 2.4GHz CMOS LNA using common gate topology for IEEE 802.15.4 ZigBee standard is proposed. Best matching at input is achieved as the value of input refection coefficient (S11) is -26 dB (< -10 dB), because a common gate amplifier is used at input stage, and maximum linearity of 12 dBm is obtained due to pi-matching circuit used at input, at 1.2V power supply.

ACKNOWLEDGMENT

One of the authors (Aditi) acknowledges the fellowship support she is receiving from Delhi Technological University (DTU), for carrying out this work, as a part of her Master of Technology Thesis work in the domain of Microwave and Optical Communication. She also acknowledges the guidance support from her thesis mentor Dr. Malti Bansal, Assistant Professor, Department of Electronics and Communication Engineering, DTU, for carrying out this research work.

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Design, Analysis and Comparison of LNA topologies for IEEE 802.15.4 Zigbee Standard

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***Abstract*— We have designed common source cascode low noise amplifier with feedforward distortion cancellation, common source inductive degeneration low noise amplifier, common source inductive degeneration low noise amplifier with feedforward distortion cancellation, common source shunt resistive feedback low noise amplifier, common gate low noise amplifier in this paper using 0.13um CMOS technology. The low noise amplifier has been optimized for working in the 2.4 GHz band. All the above low noise amplifiers are having pi-matching at input for improving gain. Advanced Design System (ADS) software is used for simulation. The fabricated low noise amplifiers use 1.2V supply voltage. The performance target is to achieve high gain and low noise figure without degrading the overall linearity**

***Index Terms*— Advanced Design Simulation (ADS) software, Low Noise Amplifier (LNA), Cascode, Common Gate (CG), Feedforward Cancellation (FDC), Common Source (CS), Inductively Degenerated Cascode, Shunt Resistive Feedback, Third Order Intercept Point (IIP3), Noise Figure (NF)**

I. INTRODUCTION

Nowadays, RF transceivers which utilize low-power and have good noise performance are in great demand for operating in ISM band; and significant developments in this domain have been possible due to advancements in wireless sensor networks (WSN) [1]. It is now possible to integrate all elements of RF transceiver on a single chip, because of the rapid advancement and acceleration in scaling of CMOS and in the designing techniques of RF CMOS circuits in the past few years. Moreover, to implement all the necessary RF functions for existing and emerging ISM band applications, inexpensive CMOS technologies can be successfully used [2]. However, the transmitter and receiver comprising communication systems will not only experience attenuation but will also experience the interference at the receiver end. Hence, the operation of the demodulator circuit, is hindered, making it necessary to increase the signal strength before it is fed into the demodulator circuit, but the desired signal along with the noise is also amplified by the amplifier. Therefore, it is important to use amplifier which adds as minimum noise as possible and such type of amplifier is called low noise amplifier (LNA). The low noise amplifier is therefore, the first active and also, an essential block in the receiver chain of communication system [3][4][5]. It is used at the front end of the receiver, is connected directly to the antenna and the noise performance of low noise amplifier directly impacts the overall noise performance of the receiver. Crucial design specification i.e., noise figure (NF) has trade-offs with other design specifications such as gain, power consumption and third order intercept point (IIP3). So, LNA design consists of trade-offs between gain, noise figure, linearity, input and output matching, and power consumption. However, to achieve good overall system performance, several desired parameters are required such as low power consumption, high gain, high third order intercept point, low noise figure and good input and output impedance matching.

Combination of three stages form low noise amplifier [6][7]:

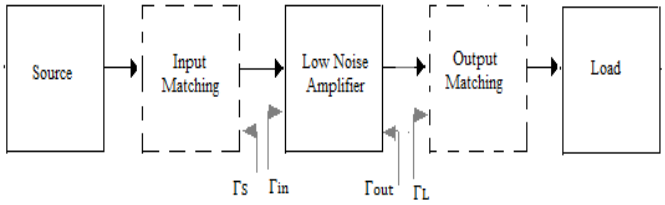

Fig. 3 Basic Components of Amplifier with input/output of amplifier (two-port network)

Where,
Γs is reflection coefficient of source of two-port network , ΓL is reflection coefficient of load of two-port network, Γin is reflection coefficient at input of the amplifier and Γout is reflection coefficient at output of amplifier

A. Input matching network.

The input matching network is present so that the input return loss or input reflection coefficient (S11) is minimum without additional noise introduction. The ideal value of the input impedance is infinite if the low noise amplifier is considered as voltage amplifier. So, to obtain minimum noise figure, a transformation network is required before low noise amplifier, if viewed from noise point of view while conjugate matching between antenna and low noise amplifier is required, if viewed from signal point of view. Each of the above choices has its own advantages and disadvantages however, the latter is commonly used in today's systems. Therefore, LNA is designed such that it has input impedance equal to 50Ω resistance.

The LNA is designed to make gain and linearity as high as possible and make noise figure as low as possible. However,

gain and linearity are the two parameters which are poles apart and it is difficult to balance them i.e., gain will be affected while trying to improve the linearity and vice versa [8][9]. Gain is enhanced in Pi-matching when compared to T-matching. So, in order to obtain reasonable linearity at low power, pi-matching is used and hence, is adopted in this paper.

B. Main amplifier section

Amplifier section ensures maximum gain and linearity and also, minimum noise figure and power consumption. It also provides input impedance matching at the same time.

1) Power Gain

In figure 1, the input/output power gain of low noise amplifier i.e. a two port network is shown. Power gain is defined as the ratio of the power dissipated in the load i.e., output power to the power supplied to the amplifier i.e., input power. The power gain mathematically, can be expressed as:

$$G = \frac{P_{out}}{P_{in}} \quad (1)$$

$$G = \frac{(1-|\Gamma_L|^2)|S_{21}|^2}{(1-S_{22}|\Gamma_L|^2)(1-|\Gamma_L|^2)} \quad (2)$$

2) Noise Figure

Noise Figure is the ratio of the signal to noise ratio of the input port to that of output port and is larger than 1 dB and is given by:

$$NF = \frac{SNR_{out}}{SNR_{in}} \quad (3)$$

For the single-stage amplifier, its noise figure is seen as follows:

$$F = F_{min} + \frac{4r_n|\Gamma_S-\Gamma_{opt}|}{(1-|\Gamma_S|^2)|1+\Gamma_{opt}|^2} \quad (4)$$

In the formula, Fmin is the minimum noise figure. Γopt, rn and Γs are the best source reflection coefficient, the equivalent noise resistance of the transistor and the input reflection coefficient of the transistor when Fmin is obtained.

For multi-stage amplifier, the noise figure is decided by the Friis formula:

$$NF = F_1 + \frac{F_2-1}{G_{A1}} + \frac{F_3-1}{G_{A2}} + \dots \quad (5)$$

where,

Fn is the noise figure of the first n-amplifier and Gn is the gain of the first n-amplifier.

C. Output matching network

The output matching network is present to guarantee that the output impedance is 50Ω.

In this paper, LNA having common source cascode with feed forward distortion calculation, common source inductive degeneration, common source inductive degeneration with feed forward distortion cancellation, common source with shunt resistive feedforward and common gate, working at 2.4GHz frequency have been designed at 0.13um technology.

II. Circuit Designs for Different LNA Topologies

A. Common Source Cascode Low Noise Amplifier with Feed Forward Distortion cancellation (FDC) technique.

The M_1 transistor is used in CS stage, forming cascode structure with M_2. Gate of M_3 and drain of M_1 are connected and M_3 transistor's output is given to base of M_2; for boosting the gain. M_3 and R_1 form another CS amplifier. M_4 transistor is used in common gate (CG) mode as an auxiliary transistor. C_6 and L_2 are used as load and C_7, C_8, and L_1 are forming pi – matching at input.

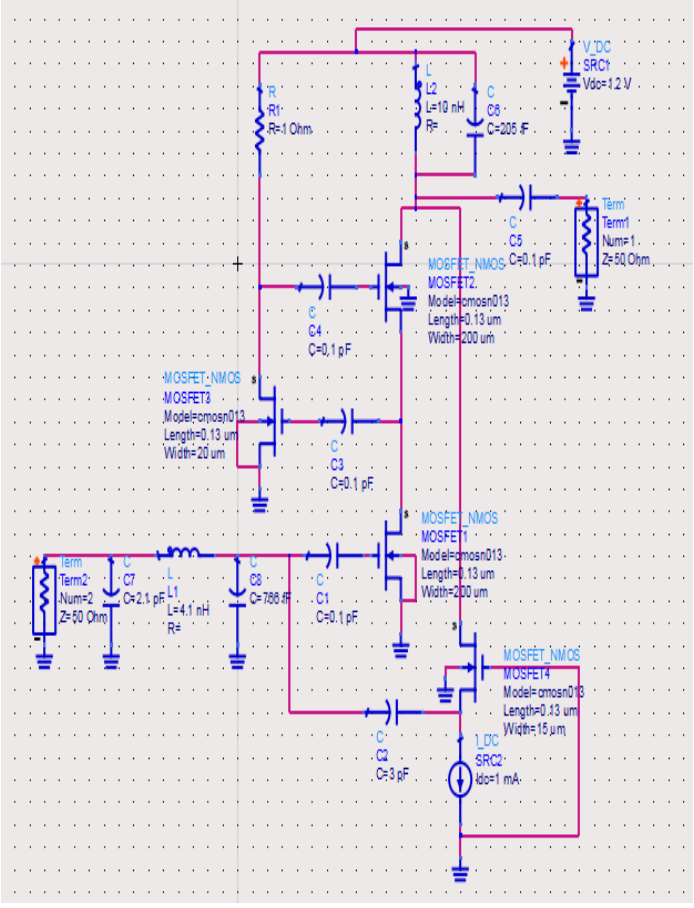

Fig. 2 Schematic of CS Cascode LNA with FDC

B. *Common Source Inductive Degeneration Low Noise Amplifier*

M_1 and M_2 are in CS stage forming cascode structure and degenerative inductor L_4 is present at the source of M_1. M_3 and R_1 form current mirror circuit. The signal path is isolated from the biasing circuit by M_1. M_3 is the biasing transistor in the circuit which forms current mirror with M_1. To avoid heavy current consumption, the W/L ratio of M_3 should not be large.

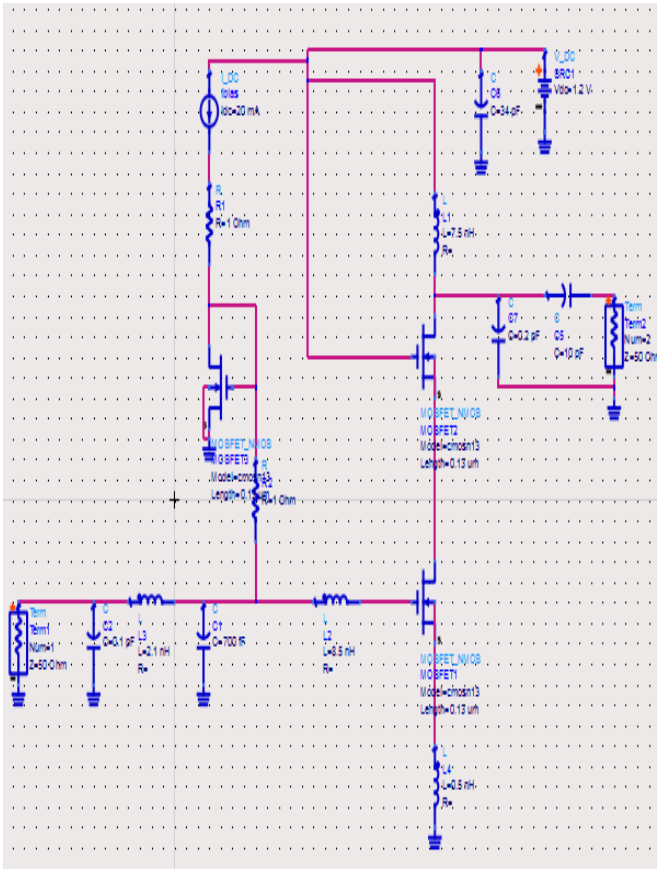

Fig. 3 Schematic of CS Inductive Degeneration LNA

C. *Common Source Inductive Degeneration Low Noise Amplifier with Feed Forward Distortion cancellation (FDC) technique*

M_2 and M_3 forms the basic cascode structure. A common gate transistor (M_2) is used as a current buffer at the output of M_3 to overcome the Miller effect. R_4 and L_4 serve as cascode stage (M_2-M_3) load. The feed-forward distortion cancellation is provided by transistor M_4 and capacitor C_4. C_4 is a blocking capacitor. L_1, C_1 and C_2 form pi-matching network. The M_5 transistor is in common source stage and R_5-L_5 serve as the load M_5.

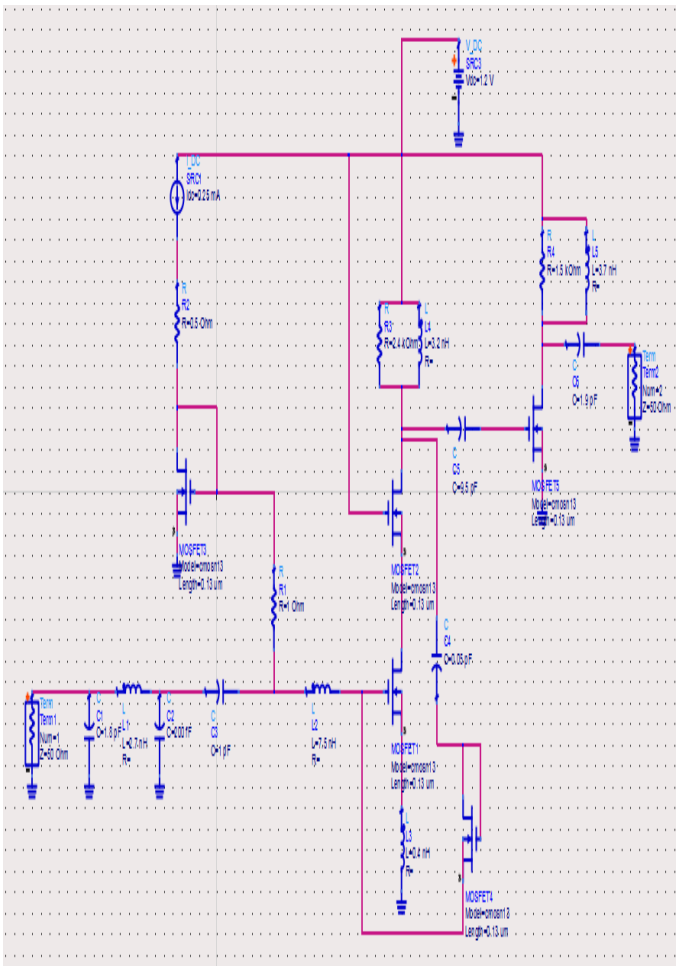

Fig.4 Schematic of CS Inductive Degeneration LNA with FDC

D. *Common Source Shunt Resistive Feedback Low Noise Amplifier*

A CS and CG transistor is present in the first stage and are connected in cascode configuration. R_1 is used as the feedback resistor and is in shunt configuration to achieve broadband matching of input and also to get negative feedback. C3 is the blocking capacitor. L_4 in parallel configuration with C_4 serves as cascode stage loading element. The second stage is a source follower stage and M_3 transistor is present in this stage. L_1, C_1 and C_2 form pi – matching network.

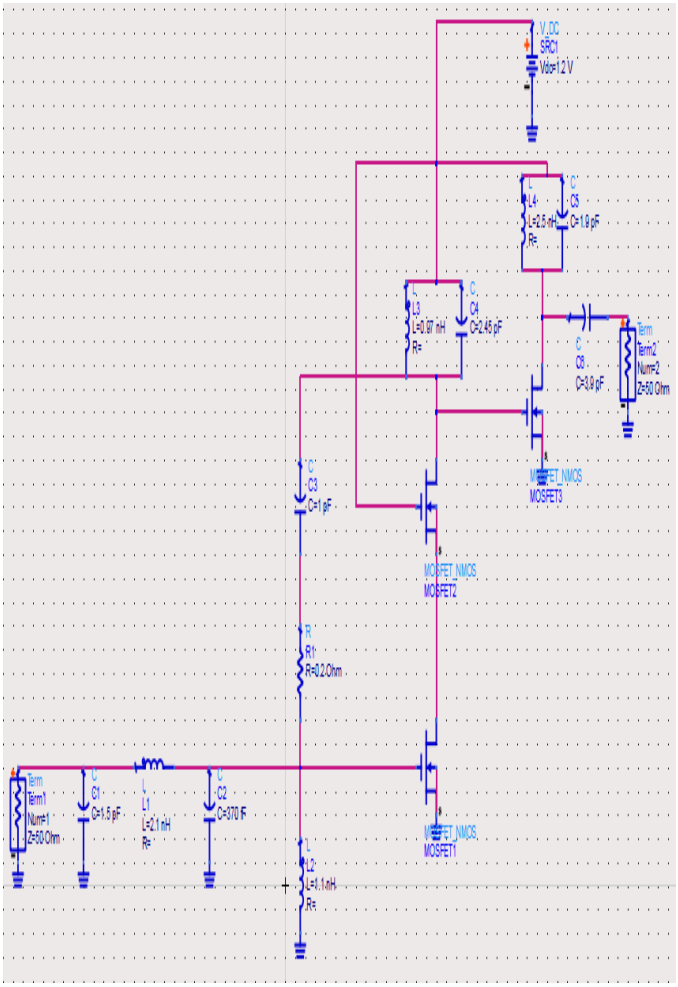

Fig. 5 Schematic of CS Shunt Resistive Feedback LNA

E. Common Gate Low Noise Amplifier

A common source amplifier is used in second stage of this circuit to compensate for the power gain, as the power gain of common gate amplifier is lower than common source amplifier. To ensure that the circuit is optimized, the LC tank circuit is matched for center frequency and to block RF leakage to ground, the inductor L_2 is present. Compared to common source amplifier, the value of L_2 for common gate amplifier is higher. C_1, L_1 and C_2 form pi-matching network at input and C_5 is the DC blocking capacitor.

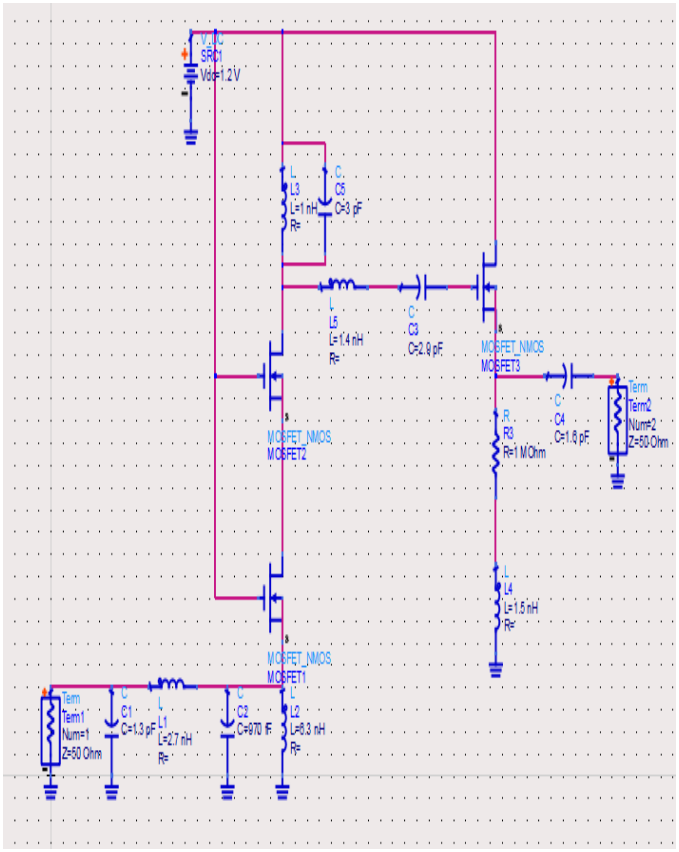

Fig. 6 Schematic of CG LNA

III. SIMULATION RESULTS AND COMPARISON

Simulations of the LNA for 0.13 um CMOS process were performed using ADS. The circuit operation requires 1.2 V power supply. The simulated results of the above circuits are shown below:

A. S-Parameters and Noise Figure

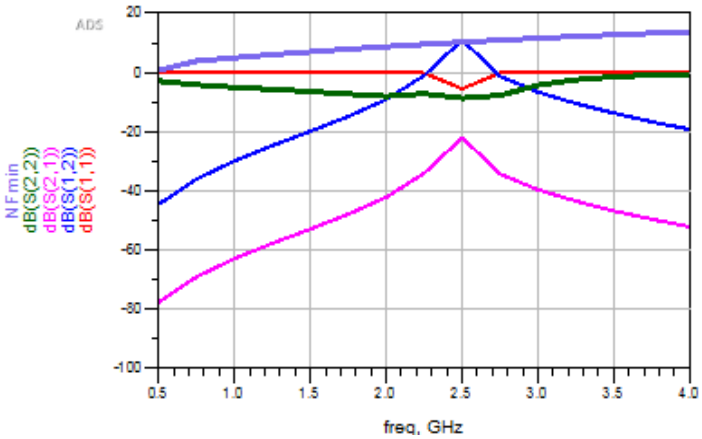

Fig. 7 CS Cascode LNA with FDC

From the above graph, we can observe that S11 is -5.562 dB, S12 is -22.06 dB, S21 is 10.976 dB, S22 is -8.707 dB and NF is 10.26 dB for common source cascode LNA configuration with FDC.

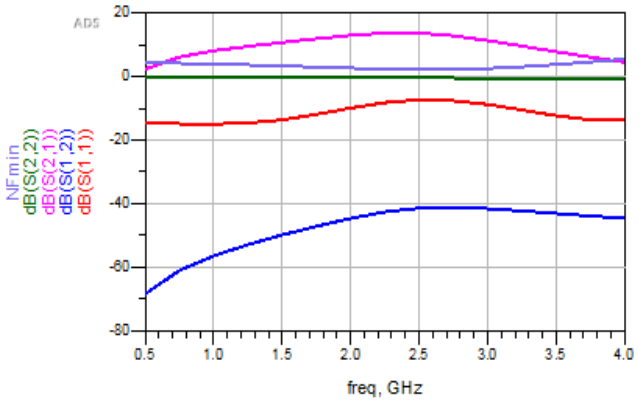

Fig. 8 CS Inductive Degeneration LNA

From the above graph, we can observe that S_{11} is -7.375 dB, S_{12} is -41.47 dB, S_{21} is 24.227 dB, S_{22} is -0.28 dB and NF is 2.109 dB for common source inductive degeneration LNA configuration.

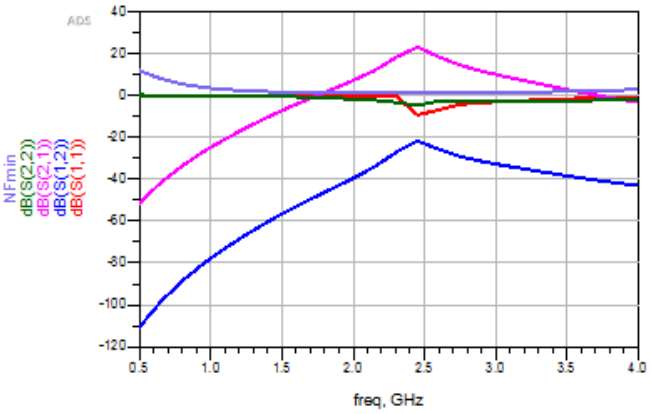

Fig. 9 CS Inductive Degeneration LNA with FDC

From the above graph, we can observe that S_{11} is -9.408 dB, S_{12} is -21.732 dB, S_{21} is 23.032 dB, S_{22} is -4.730 dB and NF is 0.988 dB for common source inductive degeneration LNA configuration with FDC.

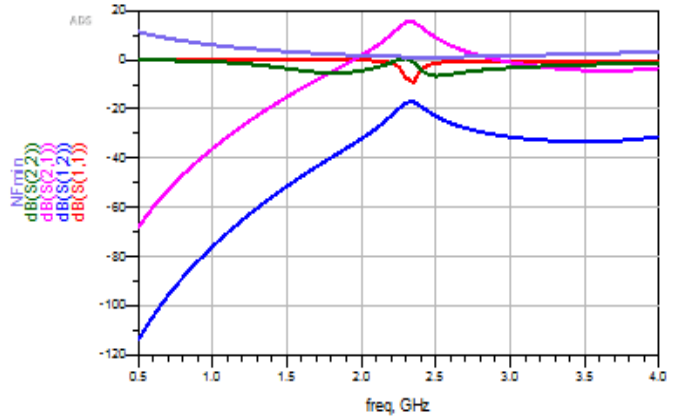

Fig. 10 CS Shunt Resistive Feedback LNA

From the above graph, we can observe that S_{11} is -9.170 dB, S_{12} is -18.909 dB, S_{21} is 15.417 dB, S_{22} is -6.204 dB and NF is 1.182 dB for common source shunt resistive feedback LNA configuration.

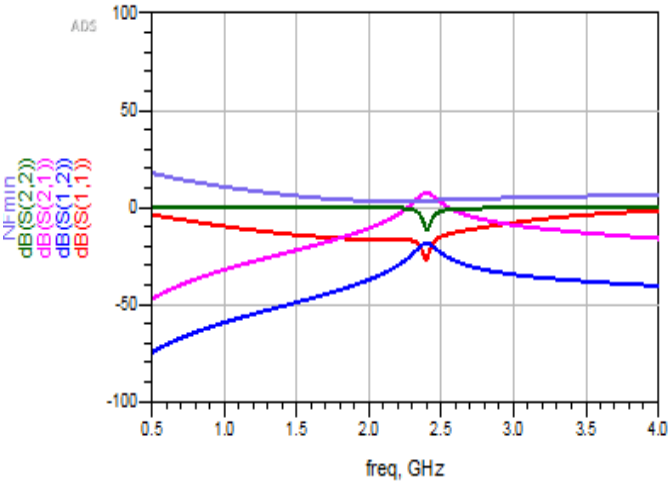

Fig. 11 CG LNA

From the above graph, we can observe that S_{11} is -26.894 dB, S_{12} is -18.604 dB, S_{21} is 7.526 dB, S_{22} is -12.264 dB and NF is 3.513 dB for common gate LNA configuration.

B. Third-Order Intercept Point (IIP3)

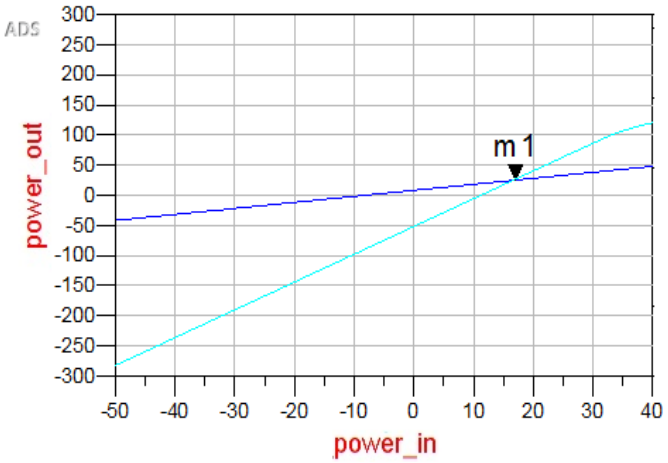

Fig. 12 CS Cascode LNA with FDC

From the above graph we observe that IIP3 point is 17 dBm for common source cascode LNA configuration with FDC.

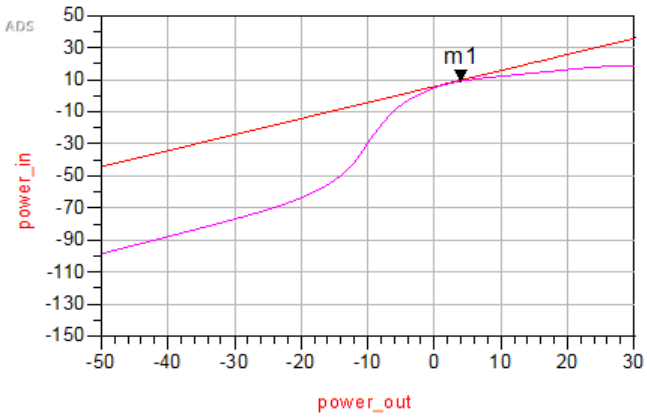

Fig. 13 CS Inductive Degeneration LNA

From the above graph we observe that IIP3 point is 4 dBm for common source inductive degeneration LNA configuration.

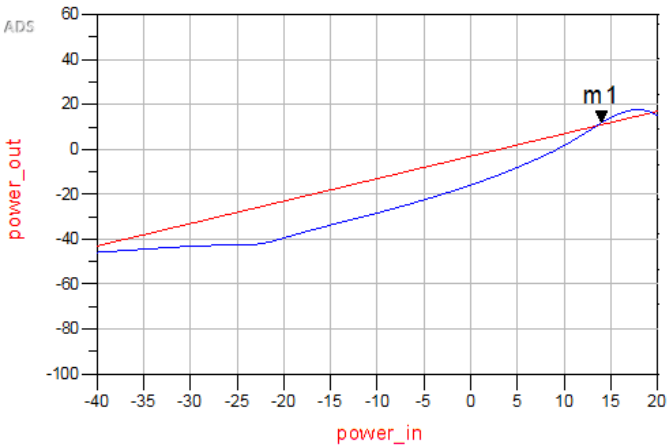

Fig. 14 CS Inductive Degeneration LNA with FDC

From the above graph we observe that IIP3 point is 14 dBm for common source inductive degeneration LNA configuration with FDC.

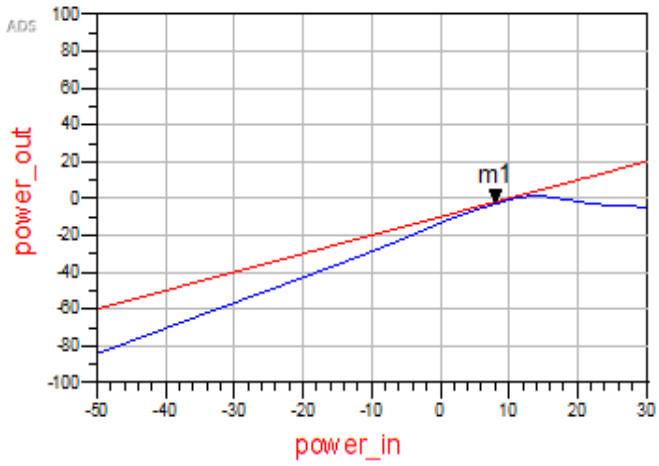

Fig. 15 CS Shunt Resistive Feedback LNA

From the above graph we observe that IIP3 point is 8 dBm for common source shunt resistive feedback LNA configuration.

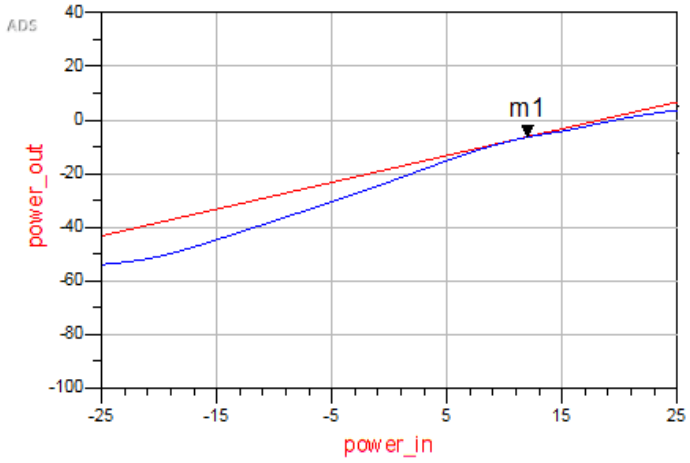

Fig. 11 CG LNA

From the above graph we observe that IIP3 point is 12 dBm for common gate LNA configuration.

TABLE III. COMPARISON OF LNA TOPOLOGIES

	CS Cascode with FDC	CS Inductive Degenerat -ion LNA [11]	CS Inductive Degenerat - ion LNA with FDC	CS Shunt Resistive Feedback LNA	CG LNA
S_{11} (dB)	-5.562	-7.375	-9.408	-9.170	-26.894
S_{12} (dB)	-22.06	-41.47	-21.732	-18.909	-18.604
S_{21} / Gain (dB)	10.976	24.227	23.032	15.417	7.526
S_{22} (dB)	-8.707	-0.28	-4.730	-6.204	-12.264
Noise Figure (dB)	10.26	2.109	0.988	1.182	3.513
IIP3 (dBm)	17.0	4.0	14.0	8.0	12.0

From table I, it can be concluded that highest gain is obtained from common source inductive degenerated LNA while common source inductively degenerated LNA with FDC provides the lowest noise figure. Highest linearity is achieved by common source cascode LNA with FDC; and for highest input impedance matching, common gate LNA should be preferred.

IV. Conclusion

In this paper, a 2.4GHz CMOS LNA for IEEE 802.15.4 ZigBee standard has been designed and analyzed using various LNA topologies. The common source inductively degenerated LNA with FDC has a high gain of 23.032 dB, high linearity of 14 dBm, low noise figure of 0.988 dB and good input impedance matching ≈ 10 dB. So, inductively degenerated LNA with FDC is the best LNA topology as compared to others, for IEEE 802.15.4 Zigbee standard.

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A High Linearity and Low Noise Shunt Resistive Feedback UWB LNA

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***Abstract*— A shunt resistive feedback CMOS low noise amplifier (LNA) using a pi-matching network has been fabricated in this paper using 0.13µm CMOS technology for applications in ultra-wideband (UWB) systems is presented. Minimum stimulated noise figure is of 1.811 dB value and the maximum linearity of 3 dBm with moderate gain of 11.0037 dB is achieved simultaneously, when operated at 1.2 V power supply, with a 3-dB bandwidth ranging from 3.1 GHz to 10.6 GHz.**

***Index Terms*— Advanced Design Simulation (ADS) Software, Low Noise Amplifier (LNA), Wideband, Complementary MOSFET (CMOS), Common Source (CS), Common Gate (CG), Noise Figure (NF), Resistive Feedback.**

I. INTRODUCTION

The Federal Communication Commission (FCC) in US has approved the ultra-wide band (UWB) in the range of 3.1-10.6 GHz, for use for commercial applications recently [1]. For wireless communication, significant interest has been developed in Ultra-wideband (UWB) technology as it provides, over a wide frequency band spectrum, transmission of data at very low power, high data rate and low cost [2]. It is envisioned that in the ultra-wide band technology, wireless connections will be all home and office cable networks, by featuring hundreds of megabits per seconds. So, this technology is being applied in sensor networks, wireless personal area networks, imaging systems, etc. Since, it relays data within area by providing cost effective, power efficient and large bandwidth circuits, it is specifically most suitable for short-range radios and wireless personal area networks. The multiband OFDM and the direct sequence (DS) are the two ultra-wide band technology approaches, of which, in multiband OFDM, 3.1-10.6 GHz spectrum is divided into 528MHz sub-bands and to transmit data at high data rate (480 Mb/s), OFDM is employed while in the direct sequence technique, the 3.1-10.6 GHz spectrum is covered in pulses. Low noise amplifier is required by both the techniques [3] and is the first block of the receiver as it comes directly after the antenna. However, several challenges such as low noise figure (to increase receiver sensitivity), low power consumption (to increase battery life), 50 Ω wide-band input impedance matching (to minimize return loss), high gain, etc. are encountered in the designing of low noise amplifier for ultra-wide band, so designing of low noise amplifier is not an easy job. Hence, to achieve desired parameters, many topologies have been explored and developed to design ultra-wide band CMOS low noise amplifier in the recent years, of which inductively degenerated common source low noise amplifier, common gate low noise amplifier and common source resistive feedback low noise amplifier are the popular low noise topologies. The first stage of all the low noise amplifier structures is either common source or common gate configuration but in wide band applications common gate low noise amplifier is preferred over common source inductively degenerated low noise amplifier because common gate low noise amplifier has low power consumption, high linearity, high reverse transmission and good wideband input impedance matching due to low quality factor of input resonant matching network [4][5]. But it also has high noise figure i.e., poor noise performance. So, common source resistive feedback is an alternative as it provides input impedance matching for broad-band. But it is difficult to achieve input matching, low noise figure and low power consumption simultaneously [6][7]. The proposed common-source cascode amplifier using shunt feedback topology is shown in figure 1.

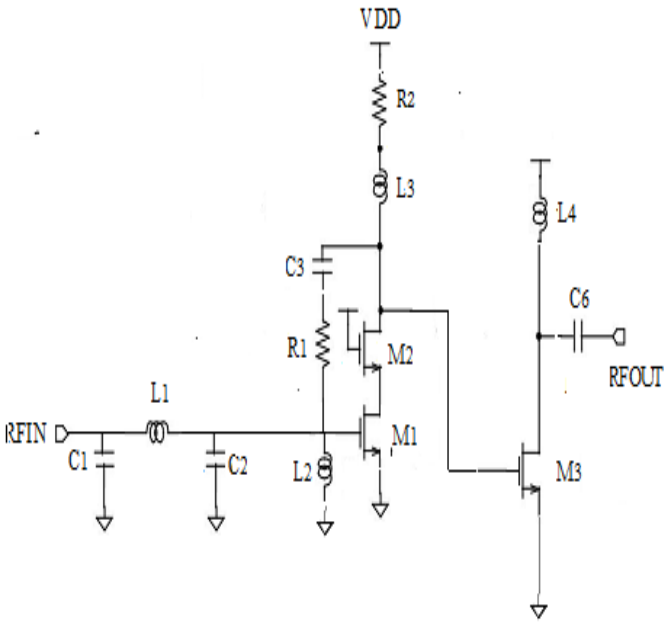

Fig. 1 Proposed Common Source Shunt Resistive Feedback UWB LNA

In general, linearity and gain are two different poles and to balance them is difficult because while improving gain, linearity gets degraded and vice versa. So, pi-matching is used to enhance the forward gain of LNA, by providing additional degree of freedom [8].

II. Circuit Design

The proposed low noise amplifier topology's schematic is shown in figure 2. One common source transistor and other following common gate transistor, connected in cascode configuration, are present in the first stage of the low noise amplifier. The common source load impedance can be approximated to input impedance which is parallel to parasitic capacitance and the common source stage's gain is not large. Cascoded topology is used because it has negligible Miller effect on M_1 transistor. Here, R_1 and C_3 are used as the feedback resistor and the blocking capacitor respectively. The feedback resistor is in shunt configuration so as to obtain negative feedback and also for broadband matching of input. The negative feedback improves the stability factor and hence, unconditional stability is provided by the amplifier and gain sensitivity of the amplifier is reduced. L_3 and R_2 in series act as loading elements of the cascode stage. For further extending the bandwidth and for achieving high gain, the second stage is is used which is a source follower stage. Pi-matching network is formed by L_1, C_1 and C_2 at input for improvising linearity of the circuit. Furthermore, it also helps to achieve input impedance matching. Since, this is a very simple low noise amplifier topology, therefore, it is suitable for low cost LNA applications (ideally).

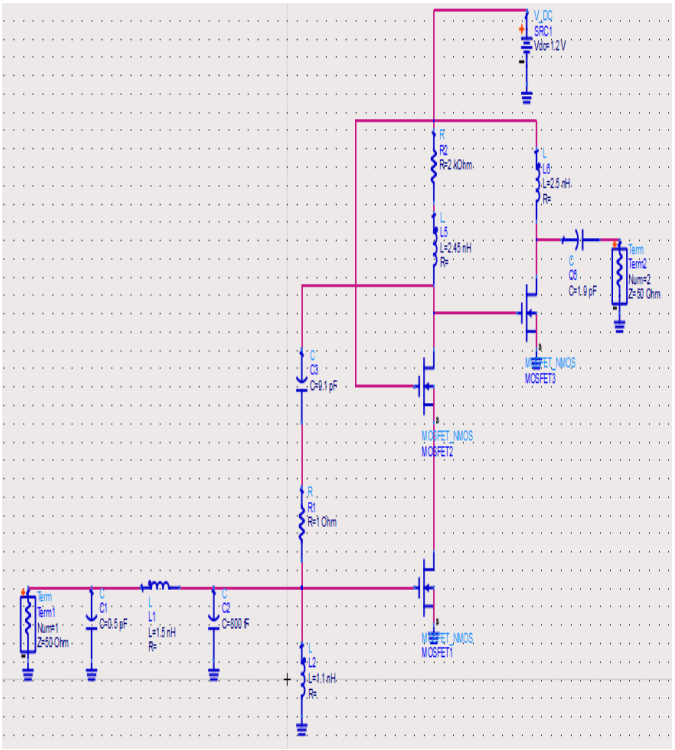

Fig 2. Schematic of Common Source shunt resistive feedback UWB LNA

III. Simulation and Results

The proposed LNA has been designed in a 0.13µm CMOS process and the simulations of the designed LNA were performed using ADS. The circuit operates at 1.2 V power supply. In figure 3, the input reflection coefficient (S_{11}) is shown and in figure 5, the power gain (S_{21}) is shown. The circuit has maximum power gain of 11.037 dB over 3.1-10.6 GHz frequency range. The reverse isolation (S_{12}) is shown in figure 4. The measured reverse isolation is from -14.265 dB to -31.897 dB in the range from 3.1-10.6 GHz. The output reflection coefficient (S_{22}) is shown in figure 6 and is less than -10 dB. The noise figure of proposed low noise amplifier, shown in figure 7, is about 1.811 dB. The simulated third order intercept point (IIP3) result for UWB LNA is shown in figure 8, and IIP3 of 3 dBm is obtained. From the result, it can be concluded that good value of gain and high linearity with low noise figure have been achieved. The simulated amplifier's characteristics summary is presented in Table I. From Table I, compared with other LNA's, the performance of our proposed CMOS LNA is much better as it has the best reported value of noise figure and linearity, in both 0.18µm and 0.13µm technology, in the range of 3.1-10.6 GHz.

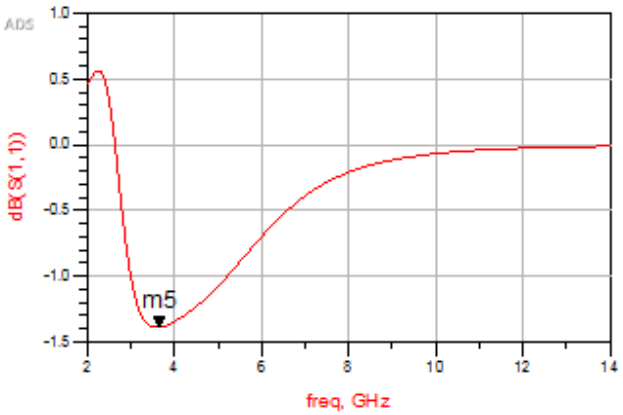

Fig. 3 Input Reflection Coefficient (S_{11})

S_{11} is input reflection coefficient or input return loss. In order to measure S_{11}, a signal is injected at input port and its reflected signal is measured. In this case, no signal is injected into output port. So, it represents the measure of matching of the input impedance to the reference impedance. For 3.1-10.6 GHz frequency range, the S_{11} parameter obtained is -1.390 dB, as shown in figure 3.

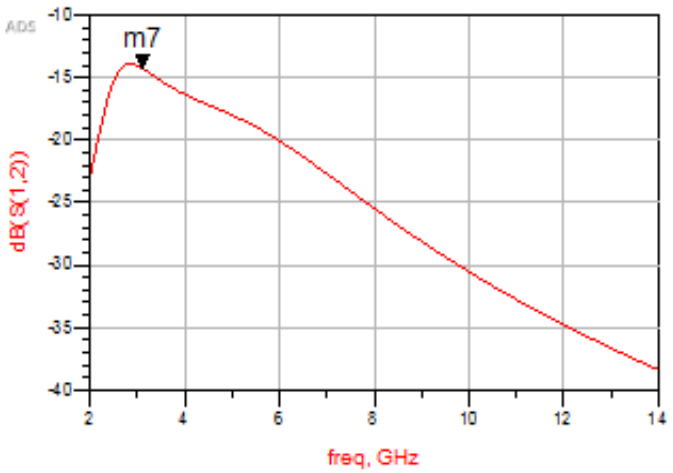

Fig. 4 Reverse Gain/ Reverse Isolation (S_{12})

S_{12} is reverse transmission coefficient or reverse isolation as it measures how much the input signal is reflected back. In S_{12}, a signal is injected into output port, and signal power leaving port is measured. For 3.1-10.6 GHz, the minimum value of S_{12} is less than -10 dB i.e., -14.265 dB, as shown in figure 4.

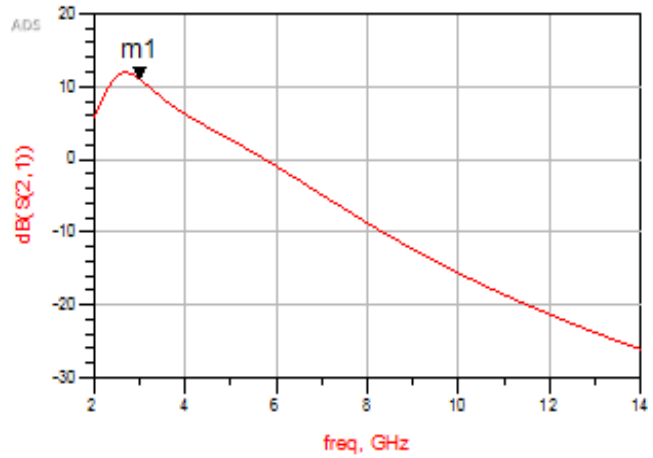

Fig. 5 Forward Gain (S_{21})

S_{21} is forward transmission coefficient or forward gain. If S_{21} is to be measured, a signal is injected at the input port, and the resulting signal power exiting output port is measured. It measures how well the signal goes from input to output. For 3.1-10.6 GHz, the value of maximum gain obtained is 11.037 dB, as shown in figure 5.

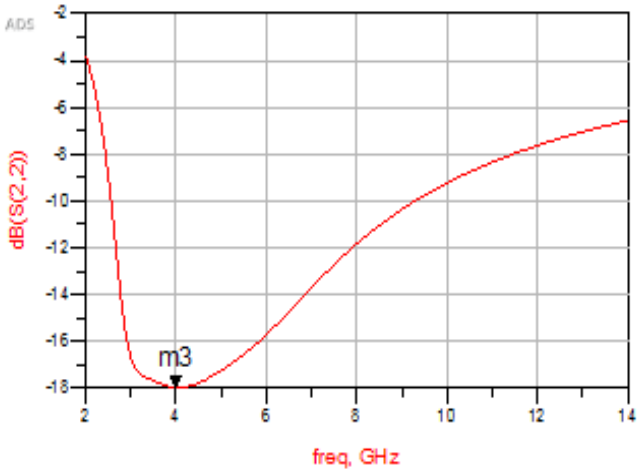

Fig. 6 Output Reflection Coefficient (S_{22})

S_{22} is output reflection coefficient or output return loss. For S_{22} measurement, a signal at output port is injected and its reflected signal is measured. So, it represents the measure of matching of the output impedance to load impedance. For 3.1-10.6 GHz, the S_{22} is less than -10 dB i.e., -17.980 dB, as shown in figure 6.

Fig. 7 Noise Figure (NF)

The noise performance of device at high frequency is indicated by noise figure. Noise figure is a figure-of-merit, the amount of excess noise present in a system is described by it. The system impairments resulting from the noise can be reduced by minimizing the noise in the system. The minimum noise figure of 1.811 dB has been obtained for 3.1-10.6 GHz, as shown in figure 7.

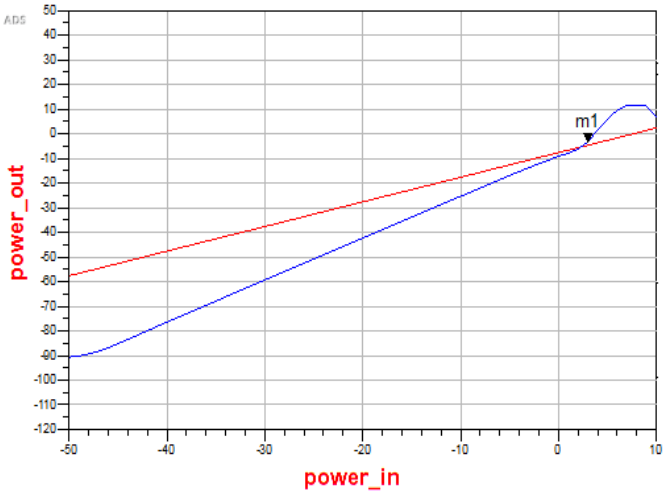

Fig. 8 IIP3

LNA along with amplification of signal and good noise performance, should be linear, even when the signal is strong. Hence, during designing of LNA, linearity is an important consideration. The third order intercept point (IIP3) is the most typical measure of linearity [9]. The value of third order intercept point is 3 dBm as shown in figure 8.

TABLE I COMPARISON OF DIFFERENT CMOS LNAS

	[10]	[11]	[12]	This work
Frequency (GHz)	3.1-10.6	3.1-10.6	3.1-10.6	3.1-10.6
Technology (µm)	0.18	0.13	0.13	0.13
Supply (V)	0.8	1.2	1.2	1.2
Gain (dB)	13.1	15.1	13	11.037
Noise Figure (dB)	3.25	2.1	2.9	1.811
IIP3 (dBm)	-16.2	-8.5	-4.8	3

From the table I, it can be concluded that for the range of frequency from 3.1-10.6 GHz, at 0.13µm technology, operating at 1.2 V, compared to other LNAs, the designed LNA has least noise figure (of value 1.811 dB) and maximum linearity (of value 3 dBm), with a good value of gain (11.037 dB). So, our designed LNA, in terms of linearity and noise, is much better as compared to other reported LNAs for 3.1-10.6 GHz frequency range.

IV. CONCLUSION

The design for an UWB LNA based on a simple resistive shunt feedback technique is reported in this paper, that can perform well over the entire range of 3.1-10.6 GHz i.e., in ultra-wide band. More importantly, decent gain, low noise figure and good IIP3 is achieved simultaneously over ultra-wide bandwidths using a relatively simple resistive shunt feedback topology for LNA at 1.2V power supply. Because of the simplicity in the design, it is possible to achieve low noise figure and high linearity; and most importantly, provides an alternative as well as attractive design to realize high performance and low-cost CMOS UWB receivers and systems.

ACKNOWLEDGMENT

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Appendix III:
Communicated Papers

Frequency Dependent LNA Design: A Review

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***Abstract*— Literature review of various low noise amplifier (LNA) design (LNA) is presented in this paper which is used to improve the NF, gain, linearity, stability and also, to reduce power dissipation. Low noise amplifier having high performance and lower noise performance have crucial importance in wireless technologies and is an active research area. So, several recent architecture is explored in this paper.**

***Index Terms*— ADS (Advanced Design Simulation Software); LNA (Low Noise Amplifier); CMOS (Complementary MOSFET); IIP3 (Third order intercept point); GSM (Global System for Mobile); GPS (Global Positioning System); LAN (Local Area Network); IM (Intermodulation Distortion), MIM (Metal Insulator Metal); UWB (Ultra-wide Band)**

I. INTRODUCTION

The recent development in wireless technology due to scaling of the transistor and development of low power, low noise and high gain circuit has led to diversion of attention to design a wireless high gain, low noise, low power and highly stable transceiver. The main and essential component of RF receiver system is low noise amplifier (LNA). It is also the first stage of the receiver. The low noise amplifier is used to provide enough gain to overcome noise by the other stages of the receiver system and to add minimum noise as possible in the system while amplifying the signal. So, the receiver noise performance mainly depends on the LNA noise performance. More importantly is used to provide good linearity to the system by accommodating large signal without signal distortion. This paper presents brief review of research work done by the various researchers in designing and simulating the LNA by using various topologies such as common source (CS) cascode, common gate (CG), common source shunt feedback and etc. and also, various techniques such as forward body bias technique, current reuse techniques and etc. for improving the gain, noise figure (NF), linearity, stability and power consumption.

II. HISTORY

Almost, 20 years ago, the most valuable device present to function as low noise amplifier at high frequency were only travelling wave tubes or vacuum tubes which were fabricated in various laboratories [1]. However, the noise temperature of travelling wave tube was around 3000K. Thus, making its amplification limited by noise in the circuit [2]. The tunnel diode was also used as low noise amplifier which provides amplification by using negative conductance effect but shot noise is present in the dc current that flows during the amplification operation and is major source of noise, contributing as the drawback of using tunnel diode for amplification [3]. The maser standing for microwave amplification by stimulated emission of radiation, having extremely low noise figure replaced vacuum tubes and tunnel diodes but unfortunately it had its own drawback of working at low temperature environment, resulting in use of costly and highly complicated equipment. Therefore, could be used only in sophisticated systems for specialized applications [4]. Parametric amplifier formed from semiconductor diode was also a low noise amplifier because is purely reactive ideally and hence, no noise is present. Low bandwidth is the shortcoming if a single diode is used so, to increase the bandwidth multiple pair of identical diodes are used. Requiring high quality identical diodes is the serious disadvantage of the above technique [5]. Large size and unable to fabricate the device on chip made the above discussed devices less favorable to be used for low noise amplification. So, transistors such as bipolar junction transistor (BJT) or field effect transistor (FET) were used as a low noise amplifier [6][7]. However, the tradeoffs between noise figure, gain, linearity and stability in both the above transistors were different. So, the design of low noise amplifier depends on the transistor technology which is incorporated such as if Gallium arsenide high-mobility electron transistor (GaAs HEMT) is used, excellent linearity and noise figure is obtained compared to Silicon Germanium Heterojunction bipolar transistor (SiGe HBT) but on the other hand, low power consumption, high gain and good noise figure is obtained by SiGeHBT. Since, the area on chip required by BJT and FET is large, CMOS technology are used being used. The complementary MOS (CMOS) transistor is used in low noise amplifiers because of its good characteristics. High immunity against noise and static power are two of the important characteristics of CMOS transistors. Moreover, CMOS technology are used to fabricate in-chip low noise amplifiers because of high level of integration [8]. The internal structure of CMOS contains a NMOS and PMOS transistor in series. So, the power is drawn by the series combination momentarily when there is switching between ON and OFF states, because one of the transistor in the series connection is always OFF. Hence, the heat produced by CMOS devices is less as compared to other logic families such as transistor transistor logic (TTL), NMOS, etc.

III. Study of Existing Techniques

Our knowledge in the field of low noise amplifier cannot be updated without studying the earlier work done by the researchers/scientists because the earlier concepts and techniques given are helpful to study and analyze present technology concepts and techniques as there is increasing and constant demand to make the devices smaller, portable, consuming less power and operating for large frequency band. A brief review of the earlier work done in the designing of low noise amplifier by simple current reuse technique, common source cacode amplifier topology, common sou5rce inductive degeneration amplifier topology, cross couple capacitor technique and, etc. in various CMOS technology (90 nm, 35 nm, 0.18 µm, 0.13 µm) for microwave frequency i.e. frequency ranging from 300 MHz unto 300 GHz is discussed in the following literature review.

A. Narrowband

1. 900 MHz

This paper [9] proposes and designed first CMOS LNA that integrates input and output matching network for 900 MHz ISM Band. The LNA is formed by two stage amplifier, the first stage of which is a cascaded amplifier having inductor-capacitor resonator as load so as to improve gain and noise performance while the second stage is a CS amplifier having capacitor transformer and resistor as a load. Therefore, improved reverse isolation and simplifying the matching because of input and output decoupling are the advantages of using two stage amplifier. It also includes series inductive feedback, bias circuit and capacitive transformer. The LNA is designed on a chip of size 0.74x0.72 mm^2 using 0.8 µm CMOS technology. A supply of 3 V is used for drawing current of 8.6 mA from first stage and 2 mA from second stage. Maximum power gain of 14.3 dB, minimum noise figure of 4.5 dB and P_{1dB} of +5 dBm is observed.

A LNA for 900 MHz is designed using 0.5 µm CMOS technology. Current reuse technique is used to increase overall LNA gain. The LNA design approach utilizes two stage amplifier. The forward gain is achieved from stage 1 of the amplifier and unity buffer is achieved from stage 2. Also, each stage employs bias feedback amplifier to establish Q point for each stage by setting dc output voltage of each stage to bias reference. Output of first stage is directly coupled to input of second stage. A minimum noise figure of 1.9 dB, gain of 15.6 dB, IIP3 of -3.2 dB and power consumption of 20 mW is obtained when a supply of 2.7 V is given to LNA. Chip of size 0.7 mm x 0.4 mm is designed [10].

In the paper [11], broadband inductorless LNA design at 900 MHz is explored as LC tanks which are highly tuned and have high Q value are not used i.e. on chip providing overdrive capabilities are not exploited. The LNA consists of three NMOS gain stages in cascode. Also, multistage topology is used by the LNA so that at low or zero intermediate frequency the circuit has critical reverse isolation. To reduce power consumption, current reuse technique is used and to improve linearity the last two LNA stages are degenerated. For the input stage, open loop structure is used to avoid noise generated by the feedback system and the output buffer is degenerated cascode amplifier. A 9 dB gain, 2.3-3.3 dB NF, >-41 dB S_{21} and -4.7 dBm IIP3 has been observed by 900 MHz designed using 0.5 µm CMOS process while current of 3.4 mA is drawn from 3 V supply. A die area of 1.0 x 1.2 mm^2 has been used in total and the largest part occupied only by de-coupling capacitors while die are of 0.4x0.3 mm^2 is occupied only by active core.

A 900 MHz LNA is implemented in the paper [12] fabricated using three level metal 0.8 µm CMOS process and SOIC like package used for packing. Amplifier design topology is cascode topology having only single stage for improvement of linearity, 1 dB compression point and minimization of power dissipation and also uses inductive degeneration at the source. The cacsode stage is used to improve reverse isolation and eliminate Miller effect and source inductive degeneration is used to achieve input matching and noise matching simultaneously. Only one external inductor is required. The area occupied by the chip is 720x720 µm2. The LNA provides NF of 1.2 dB at 30 mW, 1.5-dB at 13.5 mW, and 2-dB at 6.3 mW. Also, a NF of less than 2 dB is provides at less than 10 mW power. Moreover, an IIP3's of -1 dBm is obtained at 30 mW and -3.8 dBm at 6.3 mW. A high S_{11}, S_{22} is below -10 dB and S_{12} is more than 42 dB.

A full integrated 900 MHz CMOS LNA has been fabricated with 0.35 µm minimum channel length. To provide wide dynamic range and low noise a single stage cascoded inductive degeneration configuration is used. Single stage is used in order to limit power consumption and improve reverse isolation of the LNA. Also, LC networks is used to achieve 50 Ω matching. The CMOS LNA of three different version is fabricated in [13] with the main transistor width (W) of 225µm, 450µm, and 675µm, are C225, C450, C675 respectively and is mounted of TQFP48 package. C225 is measure on dedicated application board and packed components are soldered on the board while C675 is measured on test board and packaged chip is plugged in Johnstech socket. C450 is measured on dedicated application and test board. The best configuration is C450 having 16 dB NF at 12 mA and 1.5 dB NF at 20 mA, along with VSWRin less than or equal to 2.5. For good matching conditions i.e. for VSWRin less than or equal to 2, the NF≤1.75 dB, IIP3≤3 dBm and gain equal to 10 dB.

A 900 MHz LNA using 0.35 µm CMOS process has been fabricated. A single stage cascode LNA configuration is used. Here, to reduce power consumption single stage is used and to reduce Miller effect and to improve reverse isolation cacscode configuration is used. Transistor of width (W) of 450 mm is used. The LNA is housed into TQFP48 package. A power gain

of 14 dB, NF of 0.9 dB, S_{11} of -10 dB, S_{22} of -27 dB and IIP3 0f 0 dBm is obtained at 18 mW power while a NF of 1.05 dB is also obtained at 9 mW power along with power gain of 12 dB, S_{11} of -8.7 dB, IIP3 of -2 dBm [14].

The LNA working at 900 MHz and to be used as mobile CDMA receiver, that works on 824-894 MHz has been proposed and fabricated in the paper [15]. The LNA circuit uses the current reuse technique so as to achieve transconductance of that of device but by using less current. The inductors in LC network that is used as the load and are tuned at operating frequency, has high quality factor. The quality of inductor is high if the substrate resistivity is higher. This, the performance of inductor depends on the doping of substrate. The LNA is implemented using 0.35 µm CMOS process. The dimensions of the LNA are 1541 µm x 850 µm and the total area occupied is 1.31 mm^2. A NF of 1.8 dB, gain of 15 dB, IP3 of -3 dBm and compression point of -11 dBm is obtained.

TABLE I. COMPARISON OF LNA AT 900 MHZ

	[9]	[10]	[11]	[12]	[13]	[14]	[15]
Technology (µm)	0.8	0.5	0.5	0.8	0.35	0.35	0.35
Supply (V)	3	2.7	3	-	-	-	-
S_{21} (dB)	14.3	15.6	9	-	10	14 @18mW	15
NF (dB)	4.5	1.9	2.3 - 3.3	1.2 @ 30mW	≤1.75	0.9 @ 18mW	1.8
IIP3 (dBm)	-	-3.2	-4.7	-1 @ 30mW	≤3	0 @18mW	-3

2. *1 GHz*

Single ended two 1 GHz LNAs has been designed in the paper [16] with and without ac coupled inductor. Both the LNAs utilizes single stage cascode topology along with pull up resistive load without no chip inductor. However, the second LNA topology uses an additional ac coupled inductive load. Thus, forming inductive degeneration cascode topology. The active inductor working in GHz is built from CMOS gyrator as it can form large value inductor (20-40 nH) on chip using an area less than used by on chip spiral inductor. However, has poor linearity compared to on chip spiral inductor. A 0.5 µm CMOS technology is used in designing of the LNA. The circuit uses 2 V supply. The active inductor LNA provides a gain of 12.2 dB, IIP3 of -21 dB and NF of 2-2.3 dB for long channel model and 2.7-3.1 dB for short channel model consuming a power 17 mW while the inductorless LNA provides a gain of 10.7 dB, IIP3 of -3.8 dBm and NF of 2-2.2 dB for long channel model and 2.6-2.9 dB for short channel model consuming a power of 16 mW. The input return loss is -10 dB and reverse isolation is higher than 45 dB for the both the LNA while the output matching is less than -10 dB for active inductor LNA. Therefore, out of both the LNA design, active inductor LNA is more selective and image reject filter requirements are relaxed with the help of series resonance.

A 0.5 µm RF CMOS LNA using current reuse technology and CS inductive degeneration topology is proposed in [17]. The first stage of LNA has a PMOS and a NMOS, CS amplifier in cascode configuration followed by a CG stage. Another transistor in CS configuration is present before the cascode to set the dc bias of transistor in cascode stage while a transistor in CG configuration is present at the end as buffer stage to provide output matching of LNA. The on chip inductor i.e. the degenerated inductor have quality factor of 5 while the off chip inductors i.e. input and output inductors have quality factor of 50. The proposed LNA at 1GHz gives a S_{11} of -31.8 dB, S_{21} of 21.6 dB, S_{12} of 42 dB, S_{22} of 42.1 dB, NF of 2.7 dB and IIP3 of 18.8 dB. Also, a current of 20.3 mW is consumed from 2.2 V supply.

A 1 GHz CMOS LNA which uses cascode configuration but in modified form is proposed in the [18]. Here, the LNA circuit uses a CS amplifier which is inductively degenerated in the first stage of LNA followed by CG amplifier, which forms a cascode configuration. A CS amplifier before stage 1 is used to bias the amplifier in first stage and a CG amplifier is used at the end as a buffer stage to achieve output matching. The inductor on chip is a degenerated inductor having quality factor of 5 and the input and output inductors are off chip inductor having a quality factor of 50. 0.5 µm CMOS technology is used to design the LNA circuit. An input reflection coefficient of -33.64 dB, forward gain of 18.6 dB, reverse isolation coefficient of -45.5 dB, output reflection coefficient of -35.22 dB, NF of 1.62 dB and IIP3 of -23 dBm is observed. A power of 12.5 mW is consumed from 1 V supply.

TABLE II. COMPARISON OF LNA AT 1 GHZ

	[16]		[17]	[18]
Technology (µm)	0.5		0.5	0.5
Supply (V)	2		2.2	1
	Active inductor	Inductorless	21.6	18.6
S_{21} (dB)	12.2	10.7		
NF (dB)	2-2.3	2-2.2	2.7	1.62
IIP3 (dBm)	-21	-3.8	18.8	-23

3. *1.5 GHz/GPS*

For GPS receiver a 1.5 GHz LNA is implemented in 0.6 µm CMOS technology by employing inductive source degeneration topology along with input tuning so that 50 Ω narrow band input impedance is achieved, to convert the MOS device reactive input impedance into real resistance. Although,

dual-feedback and resistive termination could also have been used but each have its own drawback; of being used when loop gain requirement can be satisfied easily at low frequency and on the NF lower bound of 3dB is placed respectively. A gain of 22 dB, NF of 3.5 dB and IIP3 of -9.3 dB is obtained while from 1.5 V, a power of 30mW is consumed [19].

A 1.5 GHz LNA for GPS receiver, front-end applications has been designed with one poly and two metal layers only in 0.35 µm CMOS process. For better on chip rejection, a differential architecture is selected but consumes twice the power consumed by single ended architecture to achieve same noise figure. The architecture of LNA consists of two stage, the stage 1 is casoded so that reverse isolation improves, stability is maintained as spiral inductor is used to tune stage 1 output and the influence gate to drain overlap capacitance is reduced on input impedance i.e. Miller effect is mitigated. Moreover, by reusing the bias current of stage 2 in the stage 1, the power factor is decreased by a factor of two. So, a common mode feedback technique is used. At the source of two transistors the inductive degeneration is employed so that output of the RF filter present before the LNA is properly matched to input impedance of LNA. Baluns are used to interface to single ended test instrumentation since, the circuit is differential. A total die area of 0.84 mm^2 is used to fabricate a LNA and a mixer on a single chip. The gain of LNA is 17 dB, NF is 3.8 dB and IIP3 is -6 17 dBm and reverse gain is 52 17 dB, while dissipating a power of 12mW and using 1.5 V supply [20].

A 0.35 µm differential CMOS LNA has been fabricated for GPS application in [21]. Inductive degeneration topology in differential form is used at the input stage and LC network is used as load where the quality factor of the inductor is 7. Transistor in cascode also present between input stage and LC load to reduce Miller effect and increase reverse isolation. At the gate of the input stage transistor, the spiral inductor is integrated in series so that level of integration is increased. Since, the telecommunication signal is narrowband, narrowband RF signal processing is required. Here, the input stage is intrinsically narrowband because maximum power transfer occurs at carrier frequency because at carrier frequency only the source and input impedance match and, out of band signal components is filtered out and in band thermal noise is minimized because of LC feedback. The LNA has been realized by 5 metal layer while spiral inductor itself is realized by upper thicker metal layer. The simulated LNA has 26 dB gain, NF of 3.6 dB, IIP3of -3 dBm and current of 5 mA flows from 2.8 V supply.

A two stage LNA has been designed using 0.6 µm CMOS for 1.57 GHz. The LNA is design consists of cascode configuration in first stage so that input resonant circuit and output resonant circuit are decoupled followed by source follower present in the second stage. A coupling capacitor is used to separate the two stages. Current mirror is used to bias the input transistor so that minimum noise is coupled between the biasing resistor and the signal path. A separate circuit is used to bias the second stage. So, power consumption is less. The results observed for 1.8 V power supply is that the circuit dissipates a power of 17 mW with a NF of 2 dB, gain of 19 dB, S_{11} of -30 dB, S_{22} of -32 dB, S_{12} of -57 dB and IIP3 of 10 dB. Moreover, in paper [22] noise rejection behavior of proposed design's single ended and differential LNA has been studied and it is indicated that for the same gain differential LNA produces more noise compared to single ended LNA but is less prone to common mode noise.

A LNA for GPS receiver has been designed using 0.25 µm CMOS process in [23]. The LNA circuit uses two stage differential structure, in the stage 1 two CS amplifier are present in cascode configuration to reduce Miller effect and to improve reverse isolation, and also degenerated inductor is employed at the source to achieve stable input impedance. Spice using level 49 CMOS parameter is used for simulation of LNA, giving a NF of -5.6 dB and gain of 22 dB. The LNA circuit dissipates a power of 35 mW and uses 3 V supply. The LNA layout is designed using Cadence and area of the layout is 0.27x0.33 mm^2.

A two stage LNA has been designed using 0.18 µm CMOS process in [24]. The first and second stage of the LNA consists of CS amplifier with inductively degenerated inductors at the source. The output of the first stage is provided at the gate of the amplifier in the second stage. Another CS configuration transistor is present before the first stage to bias the in the amplifier in the first stage. Inductors are used as load for the two stages. The circuit is simulated using Cadence Spectre RF and uses 1 V supply. A NF of 2.0 dB, gain of 28.7 dB and IIP3 of -16.0599 dBm is obtained.

A LNA based on noise optimization technique has been designed [25] for 1.5 GHz. The LNA circuit has single stage having two CS amplifier. Also having 1 nH bond wire inductor as the degenerated inductor at the source of the first amplifier. LC network is used at the load so that is optimized at the operating frequency. The circuit is designed using 0.13 µm CMOS process. The simulated LNA has input reflection coefficient of about -17 dB, gain of 12.9 dB and NF of 0.55 dB. A current of 1 mA is drawn from a supply of 1 V.

A cascode CS inductive degeneration topology is used in designing of the LNA using 90 nm CMOS technology. The gate inductor and degenerated source inductor is used for input impedance matching as at the resonant frequency are acted like series resonant circuit. Another transistor is present in current mirror formation with the CS stage transistor in cascode configuration. The load of cascode architecture is LC circuit which is used to achieve output impedance matching. Cadence spectre RF is used for simulation of the LNA circuit. The input return loss, reverse isolation, power gain, NF and IIP3 are -9.9 dB, -35.68 dB, 30.942 dB, 0.533 dB and 2.9140 dB respectively. The circuit uses a supply of 1.5 V and dissipates a power of 8.7 mW [26].

TABLE III. COMPARISON OF LNA AT 1.5 GHZ

	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]
Techn-ology (µm)	0.6	0.35	0.35	0.6	0.25	0.18	0.13	90 nm
Sup-ply (V)	1.5	1.5	2.8	1.8	3	1	1	-
S21 (dB)	22	17	26	19	22	28.7	12.9	30.942
NF (dB)	3.5	3.8	3.6	2	-5.6	2	0.55	0.533
IIP3 (dBm)	-9.3	-6.17	-3	10	-	-16.0599	-	2.9

4. 1.8 GHz/Direct Conversion

A 1.8 GHz LNA for direct conversion radio receiver, that can drive a capacitive input mixer, has been designed in the paper [27]. In the front–end subsampling, aliasing problem is reduced by limiting LNA noise band with output resonator and integrated passive component's extracted models is used for optimizing the resonator, including on chip coupling capacitor to overcome the problem of second order non-linarites in down conversion of direct conversion receiver. Also, to optimize system noise figure output resonator is used, by limiting input noise bandwidth of mixer. The LNA uses cascaded input and inductive degeneration topology. A high quality factor of 4 is used in designing of circuit, else small change in component value will increase the NF significantly. A 0.5 µm CMOS technology is used to design LNA. DC coupling which has low sensitivity to parasitic effect is realized with an on chip structure as is an essential function of direct conversion. A gain of 17 dB, S_{11} of -11 dB, IIP3 of +9 dBm and NF of 3.4 dB is obtained while consuming a power of 48mW from a 3 V supply. Therefore, a method to implement modern integrated receiver having CMOS LNA in GHz range using capacitor inputs instead of 50 Ω resistor matching is designed.

A two stage LNA is designed in [28] which is based on LC resonance that uses spiral inductor on chip. The LNA uses differential structure so that even order distortion gets eliminated and also uses common mode inductive coupling because it is desired for direct conversion receivers. The common mode inductive coupling can be assumed as the extension of CS topology with a spiral inductors present on chip for applications in narrowband frequency and current source for biasing. The cascode structure is also used. The inductive load are used instead of resistive load and is of 7 nH having a quality factor of 4.5. Positive feedback circuit is also present to generate negative resistance which cancels out the series resistance present in the inductive load. A 0.8 µm with two poly and two metal CMOS process is used for designing of the LNA. The LNA exhibit a power gain of 18 dB, NF of 2.1 dB and IIP3 of -5 dBm wile dissipating a power of 48 mW from 3 V supply.

A LNA working at 1.8 GHz, using double poly triple metal 0.35 µm CMOS technology is designed and is presented in [29]. The LNA circuit uses a two stage cascaded configuration to provide good gain and isolation between input port and output port simultaneously. In the stage 1, CS inductive degeneration topology is used to match input impedance to 50 Ω followed by stage 2 which is a buffer stage present to match output to 50 Ω. The LNA layout occupies an area of 1025 x 1345 μm^2. The S-parameter is measured using HP 8719ES network analyzer and a resultant S_{11} parameter value is -8.4 dB, S_{12} is -41.7 dB, S_{21} is 10.5 dB and S_{22} is -6.6 dB. A NF of 4 dB and IIP3 of -2.4 dB is also observed. The circuit is operated using 2.5 V supply dissipates a power of 40 mW.

A two stage architecture LNA circuit having input stage as the first stage uses CG amplifier so as to achieve lower NF and uses CS stage as the second stage so as to achieve high gain along with good reverse isolation is designed in [30]. A capacitor present for dc blocking and an inductor is present between CG and CS amplifiers to provide biasing network to CS amplifier and for matching AC power so as to achieve maximum power transfer. Therefore, the capacitor and the inductor act as interstage matching network. SpectreRF is used for the simulation of the LNA. The resultant input reflection coefficient value is -6.4 dB, output reflection coefficient is -31.8 dB, power gain is 17.4 dB, reverse isolation of -66 dB, NF is 1.07 dB and IIP3 is -9 dBm while OIP3 is 8.1 dBm. The LNA circuit is designed using 0.35 µm CMOS process and a power supply of 1.2 V.

TABLE IV. COMPARISON OF LNA AT 1.8 GHZ

	[27]	[28]	[29]	[30]
Technology (µm)	0.5	0.8	0.35	0.35
Supply (V)	3	3	1.8	1.2
S_{21} (dB)	17	18	10.5	17.4
NF (dB)	3.4	2.1	4	1.07
IIP3 (dBm)	9	-5	-2.4	-9

5. 1.9 GHz/GSM

A spiral inductor of high quality has been employed in the paper [31] having 8.5-12.5 quality factor along with optimized active device layout and bias condition. The LNA is a two-stage

amplifier, CS with inductive source degeneration is present in the stage-1so as to match noise and power gain. For high linearity and gain, the second stage's bias condition is chosen. A 0.8 µm CMOS technology LNA, fabricated on high resistivity Si substrate. Using on-wafer RF probes and HP8510C Network Analyzer measurements are carried out and a chip area of 0.93x0.93 mm2 is occupied. Linear simulator is used to simulate the LNA and ATN setup is used to measure noise parameters for 0.3-3 GHz, giving a NF of 2.8 dB at 1.9 GHz. Also, a gain of 15 dB, input reflection coefficient of -16.4 dB and output reflection coefficient of -7 dB is observed at 1.9GHz, while consuming 15 mA from 3.6 V supply.

A quantitative analysis of LNA in cascode configuration is done in [32] in 0.35 µm CMOS process. A single stage LNA having two transistor namely M1 and M2 is present in cascode. Degenerated inductor is present at the source of M1 and also input is applied to the gate of M1. The cascode structure is present to achieve input impedance matching and to avoid thermal noise. The noise performance of the LNA is dominated by the first MOSFET transistor i.e. M1 while the more linarites are contributed by second MOSFET transistor i.e. M2. So, using 0.35 µm CMOS process the M1 is designed such that it gives optimum noise performance and M2 is designed to optimize linearity. The simulation of 1.9 GHz LNA is conducted in Agilent Advanced Design System (ADS) giving a minimum NF of 1.6 dB, gain of 17.5 dB, OIP3 of 10.7 dBm using a supply of 1.5 V and dissipating a power of 9 mW. Therefore, from both theoretical analysis and simulation results it is shown that the noise performance is dominated by the first MOSFET and more linaerites are contributed by second MOSFET for the LNA in cascode configuration.

A 1.9 GHz LNA has been designed in [33] using 0.35 µm CMOS technology. In the two stage LNA design, the first stage is in cascode configuration and LC tank circuit is present as the load of the cascode architecture so as to tune to 1.9 GHz. Moreover, another inductor is present at the source of the first transistor. This stage is followed by an output stage consisting of one transistor, also having LC circuit as load. Also, a current mirror is formed with before the cascode stage with first transistor of cascode stage. Inductors are placed on chip if have value lesser than 10 nH while are placed off chip if the inductor have value greater than 10 nH. For TSMC CMOS 0.35 µm, BSIM3 transistor model is used. The circuit is simulated using HSPICE and Cadence giving a gain of 21 dB, NF of 1.4 dB at 1.9 GHz and OIP3 of -14dBm, input reflection coefficient of -35dBm and output reflection of -32dBm. A supply of 1.5 V is used and power dissipated is 6.5 mW. A die of active area 5 10 µm x 250 µm is also formed.

TABLE V. COMPARISON OF LNA AT 1.9 GHZ

	[31]	[32]	[33]
Technology (µm)	0.8	0.35	0.35
Supply (V)	3.6	1.5	1.5
S_{21} (dB)	15	17.5	21
NF (dB)	2.8	1.6	1.4
OIP3 (dBm)	-	10.7	-14

6. 2 GHz

2 GHz LNA has been designed using 0.6 µm CMOS process in [34]. The LNA circuit design is based on two stage cascode topology which is narrowband LC tuned. The first stage uses CS cascode inductive degeneration topology followed by CS configuration which has LC network as load because in wireless communications RF signals are narrowband usually. The cascode architecture is used to improve reverse isolation and also to provide forward gain. The circuit uses 3.3 V supply. A NF of 2.3 dB, gain of 18 dB, reverse isolation of -44.79 dB and IIP3 of -4.94 dBm is observed as the simulation results. Also, power of 33.94 mW is dissipated.

A 0.35 µm CMOS LNA is designed in [35]. The LNA design is a two stage amplifier design, it uses conventional cascode topology. An inductor is present between the CS amplifier and CG amplifier in the cascode stage. So, inductor is used as the interstage matching network. The cascode stage is succeeded by a CS stage which along with resistors are used to bias the amplifiers in the cascode stage. The inductors used have quality factor around 5. The simulation of 2 GHz LNA using an interstage inductor is done in Agilent Advanced Design System (ADS). The simulated results are, NF of value 1.97 dB, gain of 13.7 dB. Dissipating a power of 7.5 mW from 1.5 V supply.

A 2 GHz LNA designed using 0.18 µm CMOS process has been implemented in [36]. The LNA circuit has three parts, the first part uses CS inductively degenerated topology, the second part is realized using differential pair acting as a low pass filter and the last part is the biasing circuit formed by using pn junction of PMOS as it provides steady voltage because of the large width of the transistor. The circuit uses 1 V supply and is implemented using 0.18 µm CMOS process. A LNA of size 175 µm x 50 µm is obtained. Moreover, the simulated results shows that the input reflection coefficient is -25 dB, gain is 11 dB, NF is 1.8 dB and IIP3 is 0 dBm.

A high linearity LNA circuit has been designed using 0.25 µm CMOS technology in [37]. The LNA circuit utilizes inductively degenerated topology in balanced differential mode. A superior noise performance is obtained from inductively degenerated topology because of signal swing and hence is used. However, because of the signal swing the linearity is degraded. Thus, the

linearity improvement technique is required. For differential signals two balun transformers are used. The LNA circuit uses a supply voltage of 2.5 V. At 2 GHz a maximum gain obtained is 15.2 dB, NF obtained is 2.8 dB and IIP3 obtained is 14.7 dBm and the maximum IIP3 of 16 dBm is obtained at 2.2 GHz. The size of the fabricated chip is 900 µm x 900 µm.

TABLE VI. COMPARISON OF LNA AT 2 GHZ

	[34]	[35]	[36]	[37]
Technology (µm)	0.6	0.35	0.18	0.25
Supply (V)	3.3	1.5	1	2.5
S21 (dB)	18	13.7	11	15.2
NF (dB)	2.3	1.97	1.8	2.8
IIP3 (dBm)	-4.94	-	0	16

7. 2.4 GHz/WSN/Bluetooth

A two stage 2.4 GHz LNA is presented in the paper [38][39]. The first stage has transistors in cascode configuration with resistor in parallel to capacitor as load. Here, resistor is present to set bias circuitry current to generate bias voltage at gate of first transistor in second stage; in second stage transistors are present in cascode having matching inductor between the stage such that the transistors in cascode are considered as different individual stage. So, the inter stage inductor is added between CS and CG stage. Inductor is added to increase the gain and decrease the noise of the system. The capacitor is used to provide AC ground at the gate of second transistor in second stage. A LNA using 0.5 µm CMOS technology is designed using a 3 V supply. A power gain of 19 dB, NF of 2.4 dB and input reflection coefficient of -10 dB is observed while drawing a current of 3mA.

A 2.4 GHz two stage cascade topology LNA using 0.35 µm CMOS process has been proposed in the paper [40]. The LNA using cascade topology uses series inter-stage resonance. So, it is a current sharing amplifier. Here, the two common source amplifiers are not cascaded directly but an inductor in series resonance with capacitor is present. The series resonance provides low impedance at the drain of the first transistor in the cascade stage so that common source stage of the first transistor does not experience Miller effect. A supply of 2 V is and a power gain of 21 dB along with NF of 1.24 dB has been observed. A current of 2.5 mA is drawn by the circuit.

Two CMOS LNA has been designed in the paper [41] one is single ended LNA while the other is differential LNA and fully integrated without off chip components. In the single ended LNA cascode topology is used and a degenerative inductor is also present at the source of the first amplifier in cascode architecture. Here, the input matching is obtained by the two inductor present at the gate of first amplifier present in cascode topology while the output matching is obtained by tuning of the load inductor and output capacitor. The simulation results of single ended LNA is input reflection coefficient of -17 dB, reverse isolation of -24 dB, gain of 15 dB, output reflection coefficient of -23 dB, NF of 2.2 dB. Also, a power dissipation of 4.8 mW is obtained from 3.3 V supply. In the differential LNA architecture, the single ended LNA architecture is present in differential form. The differential LNA architecture is studied because the single ended LNA architecture is sensitive to ground parasitic inductance while the differential LNA is not affected by the common mode interference. The simulation results of differential LNA is input reflection coefficient of -19 dB, reverse isolation of -35 dB, gain of 20 dB, output reflection coefficient of -21 dB, NF of 2.4 dB. A power of 7.2 mW is dissipated from 3.3 V supply. The layout is designed using 0.25 µm CMOS process and the layout area of single ended LNA is 2.05 mm x 1.28 mm while the layout area of differential LNA is 1.62 mm x 1.28 mm, which is smaller than the single ended LNA.

The LNA designed using 0.35 µm CMOS uses the conventional cascode LNA topology with degenerated inductor in differential form [42]. Since, the mismatch occurs at CS and CG amplifier present in cascode topology the spiral inductor is present between the amplifiers in the cascode stage so as to improve the matching. At the output two source follower namely (M6 and M7) transistor along with a resistor form a current source and also, current mirror is formed by another transistor (M5) with M6. The LNA circuit is simulated for 2.4GHz and using a supply of 2 V. A power gain of 19.9 dB, reverse isolation of -47.8 dB, NF of 2.5 dB and IIP3 of 2 dBm is obtained with a power dissipation of 14.7 mW.

A 2.4 GHz fully differential LNA is proposed in [43]. The LNA circuit core has a cascode design so as to remove the Miller effect and improve the reverse isolation. The linearity of the LNA is required such that if the user is close to the transmitter the linearity from minimum detectable signal to -12 dBm is achieved. However, the LNA is able to meet these specifications but the signals overdrive the subsequent stage. So, to overcome this problem the LNA in this paper is designed to have a low gain so that it could suppress input signals that have large level to desired level. Moreover, so that linearity is improved and current is reduced. A network of NMOS devices are used which acts as bypass switches along with cascode architecture to implement low gain stage and to avoid feedback that causes unstable condition. A 0.25 µm CMOS process is used to design the LNA architecture. NF, gain, input return loss, output return loss, reverse isolation and IIP3 observed are 2.88 dB, 14.7 dB, >7 dB, >10 dB, >25 dB and -1.5 dBm respectively for a high gain mode whereas for low gain or for bypass mode the NF, gain, input return loss, output return loss, reverse isolation and IIP3 observed are 14.2 dB, -14.2 dB, >9 dB, >10 dB, 14.2 dB and 19 dBm. A current of 11.4 mA is consumed in high gain mode while no current is consumed in low gain mode.

A conventional cascode LNA with degenerated inductor is used in the LNA circuit to be operated at 2.4 GHz [44][45]. The circuit also contains additional capacitor in parallel to the gate capacitor of the CS amplifier present in cascode topology so that low power is dissipated and noise performance is optimized. An additional interstage inductor is present between CS and CG stage so that matching is improved and also gain is increased. This circuit is implemented using TSMC 0.18 µm CMOS process. 1.2 V power supply is used in the circuit and power dissipation of 2.4 mW is observed. Also, S_{11} = -22.4 dB, S_{12} = -48.9 dB, S_{21} = 12.9 dB, S_{22} = -21.6 dB and a NF of 0.76 dB is observed.

A two stage LNA using 0.18 µm CMOS process has been designed in the paper [46]. The first stage is in CS inductively degenerated cascode configuration followed by second stage which is source follower. In the first stage the input transistor is the main noise contributor while the second transistor contributes to the linearity more than first transistor or input transistor. The circuit uses a supply of 1 V and dissipates a power of 13 mW. The S_{11} obtained is -16.8 dB, S_{12} obtained is -51.7 dB, S_{21} obtained is 23 dB, S_{22} obtained is -10.2 dB, NF obtained is 3.8 dB and IIP3obtained is -9.1 dBm.

A LNA operated at 2.4 GHz, with improved matching has been proposed in the paper [47]. The LNA circuit utilizes conventional cascode topology with degenerated inductor at the input. Here, to improve the input matching a capacitor is placed at the gate of the first MOS device present in cascode topology. The circuit is implemented using 0.18 µm CMOS process. The value of the degenerated inductor is 0.17 nH if capacitor is not present i.e. the circuit is not improved while the value of inductor reduces to 0.5 nH is the circuit is improved. The gain and NF of the circuit with traditional input stage is 24 dB and 0.24 dB while of the modified circuit is 21 dB and 0.39 dB.

A switched LNA used for Bluetooth applications i.e. at 2.4 GHz has been fabricated in [48] using 0.18 µm CMOS process. The switched LNA circuit has CS cascode inductively degenerated topology as the core and for attenuation and switching function has an additional circuitry. The switching logic and attenuation network are the main parts of the switched LNA. Large isolation is provided between input and output so that at all frequency unconditional stability is achieved because the LNA performance should not be influenced by the attenuation path when the circuit is operated in the gain mode. By using the inverter the LNA core is switched off in the attenuation mode. The bypass switch consists of two MOSFETS in the series combination having there gate controlled by the gate voltage. An area of 0.79 mm^2 is required by the device. A gain of 7 dB, NF of 3 dB and attenuation of -17 dB is obtained by the circuit using 1.8 V supply. Also, 7.6 mW power is consumed.

A LNA is designed to be used at 2.4 GHz, using 0.18 µm CMOS technology in [49]. A cascode LNA structure have been used in the LNA design with first amplifier in the CS configuration and second amplifier in the CG configuration and LC network as the load used for tuning the output. The bias circuit consists of diode connected transistor and for the first transistor it generates the bias voltage. The LNA circuit using 1.8 V supply is simulated in Winspice3. A voltage gain of 51 dB and NF of 1.65 dB and power dissipation of 3.15 mW is obtained.

A low voltage LNA amplifier working at 2.4 GHz have been proposed and designed in the [50]. To reduce the voltage, folded cascode architecture is used. The CS stage and CG stage of the cascoded topology is folded into two paths. The RF traps are also added in the circuit as at DC they act as short circuit and at operating frequency they act as open circuit. LC tank circuit is present at the drain of Cs stage and at the source of the CG stage so that they act as RF trap when they resonate at frequency of operation. Between the two paths a capacitor is added and is called as coupling capacitor as couples RF between the two stages. The LNA requires only 0.6 V supply and is designed using 0.18 µm CMOS technology. The input reflection coefficient is -43 dB, power gain is 13.8 dB, reverse isolation is -36.5, output reflection coefficient is -30.8, NF is 1.56 dB and IIP3 is -2 dBm. The chip size is 1.1 mm x 1.1 mm.

A fully integrated CMOS LNA working at 2.4 GHz is designed in [51]. So, that inductors values are fully integrated and input loss is minimum even if the on chip inductors are used that have low quality factor than off chip inductor. This is achieved by pi-matching the input. Active device sizing method and lossless feedback is also used to achieve low NF and 50 Ω impedance at the input. The LNA core uses cacsode topology with a degenerated inductor at source as the feedback. 0.28 µm CMOS foundry design kit is used to design the LNA circuit. A NF of 3 dB, a voltage gain of 31 dB and input reflection coefficient of -30 dB is obtained along with a power consumption of 10 mW when a supply of 2.5 V is used.

CMOS LNA is designed using CS cascode configuration having a degenerated source inductor which along with the gate inductor which is used to control resonant frequency, is used to achieve input impedance matching. A biasing circuit uses another transistor forming a current mirror with CS amplifier stage in cascode structure for biasing the cascode stage. CS amplifier is used in output stage. A 3.3 V of power supply is used in the circuit designed in 0.25 µm CMOS technology and a current of 5 mA is consumed. Hence, dissipating a power of 16.5 mW. An input reflection coefficient of -13.4 dB, output reflection coefficient of -18.3 dB, gain of 21.63 dB, NF of 1.8 dB and 1 dB compression point is obtained at -19 dBm for 2.4 GHz frequency. Layout of the circuit is formed using Cadence Virtuoso Editing tools and thus, an area of 0.8 mm x 0.6 mm is occupied by the chip [52].

In the paper [53] a CG LNA circuit is designed which at input matching network adds additional degree of freedom and at low power consumption improves the NF. So, a differential CG LNA has been designed that uses g_m technique. To increase the value of transconductance of the transistor, a capacitor in series with inductor is placed at the two differential input stage. Thus,

producing series resonance to increase the gain of the LNA. The circuit is designed using 0.18 µm CMOS process and consumes a power of 0.98 mW from a supply of 1 V. The circuit requires a total chip size of 0.98 mm x 1.2 mm and gives a value of -11 dB for input reflection coefficient, 15.5 dB for gain, 5.2 dB for NF and -19 dBm for IIP3.

A two stage LNA is designed using 0.13 µm CMOS process for 2.4 GHz frequency. The LNA consists of a core part and a buffer stage. A self-biased cell is present in the core LNA stage and a 3 bit DAC is used to control its supply voltage, varying from 0.4 V to 0.6 V. Also, between the two transistor's gates a decoupling capacitor is used to reduce the supply voltage further. The buffer stage is used to provide output impedance matching. A maximum gain of 15.7 dB and a minimum NF of 4.6 dB is obtained at 0.6 V. IIP3 is -12.2 dBm for 0.4 V and -12.6 dBm for 0.5 V. The circuit consumes a power of 60 mW from 0.4 V supply and a chip area of 0.63 mm^2 is required for the circuit [54].

A LNA is designed using 0.13 µm CMOS technology for wireless sensor network application. The designed LNA circuit is of two stage. The first stage consists of cascode topology with degenerated inductor at the source which provides matching of input impedance and high stability. The second stage consists of a CS amplifier which is used for increasing the gain of the system. The load of the first stage is RLC network which act as RF choke and hence, is used to select the output frequency. The load of second stage is an inductor. The supply voltage is 1.2 V. The circuit is simulated in Cadence Spectre RF giving value of input reflection coefficient, output reflection coefficient, gain, NF and IIP3 as -26.9 dB, -20.6 dB, 23.6 dB, 5.6 dB and -1 dBm respectively. Chip area is 0.89 mm x 0.72 mm. Also, a power of 8.1 mW is consumed [55].

A CG LNA is designed using 0.18 µm CMOS process [56]. The proposed LNA consists of two NMOS CG stage transistor and two PMOS CG stage transistors. Two capacitors and large resistors forms CCC topology. PMOS transistors has resistors as load which provide amplified signal which is cross coupled to the gates of NMOS transistors forming g_m boosting topology. The circuit requires 1.8 V power supply and consumes a power of 0.58 mW. It is observe that input reflection coefficient is less than -18 dB, gain is 14.7 dB, NF is 4.8 dB and IIP3 is 2 dBm. An area of 0.62 mm x 0.63 mm is required by the LNA.

A CS cascode inductive degenerated topology using current reuse technique is proposed in [57]. The degenerated inductor along with input inductor is used to achieve input impedance matching. The CS amplifier's output is cascaded to the CG amplifier so as to decrease Miller effect and thus are present in cacsode configuration. Output of CG amplifier goes to another CS amplifier's gate through a capacitor and an inductor is also present between CG amplifier stage and another CS amplifier stage for current reuse. A 0.18 µm CMOS technology is used to design the LNA circuit. A supply of 1.8 V is used and 10.08 mW of power is consumed. The simulated results show that the input matching is less than -10 dB, gain is 26.5 dB, NF is 3.8 dB and IIP3 is -10.3 dB for 2.4 GHz frequency.

A CS inductive degeneration topology using complementary current reuse technique is used in designing of the LNA along with transformer coupled at both the input and the output. On the top of a PMOS amplifier a NMOS amplifier is placed symmetrically so that DC current is shared between them. Inductors are used as load to increase the operating frequency and also to bias NMOS output at supply voltage and PMOS output at the ground. Thus, removing feedback circuit which is used in traditional current reuse technique. A 90 nm CMOs technology is used in fabrication of the LNA and requires a chip size of 1.0 mm x 0.75 mm. 1.2 V power supply is used in fabrication of the LNA and a power of 3 mW is consumed. The input and output reflection coefficient is less than -10 dB, gain is 13 dB, NF is 1.8 dB and IIP3 is -8.9 dBm [58].

The proposed LNA uses CS inductive degeneration topology for 2.4 GHz frequency. The LNA circuit uses transformer as the load. The circuit is designed using 0.18 µm technology. The simulated graph shows that the value of input reflection coefficient is -2.625 dB, reverse isolation is -57.166 dB, gain is 15.71 dB, output reflection coefficient is -47.36 dB, NF is 2.447 dB and IIP3 is -20 dBm. A power of 6.5 mW is consumed from a supply of 1.8 V [59].

TABLE VII. COMPARISON OF LNA AT 2.4 GHZ

	[38]/ [39]	[40]	[41]	[42]	[43]		[44] / [45]	[46]	[47]
Tech. (µm)	0.5	0.35	0.25	0.35	0.25		0.18	0.18	0.18
Supply (V)	3	2	3.3	2			1.2	1	-
S_{21} (dB)	19	21	20	19.9	High gain mode 14.7	Low gain sm ode -14.2	12.9	23	21
NF (dB)	2.4	1.24	2.4	2.5	2.88	14.2	0.76	3.8	0.13
IIP3 (dBm)	-	-		2	-1.5	19	-	-9.1	-

	[48]	[49]	[50]	[51]	[52]	[53]	[54]
Technology (µm)	0.18	0.18	0.18	0.28	0.25	0.18	0.13
Supply (V)	1.8	1.8	0.6	2.5	3.3	1	0.4-0.6
S_{21} (dB)	7	51	13.8	31	21.63	15.5	15.7 @ 0.6 V
NF (dB)			1.56	3	1.8	5.2	4.6 @ 0.6 V
IIP3 (dBm)	3	1.65	-2	-	-	-19	-12.2 @ 0.4 V

	[55]	[56]	[57]	[58]	[59]
Technology (µm)	0.13	0.18	0.18	90 nm	0.18
Supply (V)	1.2	1.8	1.8	1.2	1.8
S_{21} (dB)	23.6	14.7	26.5	13	15.71
NF (dB)	5.6	4.8	3.8	1.8	2.447
IIP3 (dBm)	-1	2	-10.3	-8.9	-20

8. 5 GHz/WLAN

A 5 GHz LNA circuit is designed using 0.25 µm CMOS process in [60]. The LNA circuit utilizes differential design formed by pair of single stage cascode amplifiers. The amplifier in CS configuration in cascode topology has an inductor is that is used as degenerated inductor at source so as to increase linearity. At the gates of the CS amplifiers input signal is applied through inductor. This inductor along with degenerated source inductor forms input matching. Moreover, inductor is also used as load at the drain of CG amplifier present in cascode topology which along with output capacitors form output matching. The gates of CG amplifiers when connected to 3 V supply is used to bias the circuit. The LNA circuit area on chip is 830 µm x 390 µm. A gain and NF is 16.6 dB and 2.38 dB respectively is obtained if power dissipation is 48 mW and, is 14.4 dB and 2.8 dB if power dissipation is 24 mW. For a power dissipation as low as 12 mW power gain is 11.6 dB and NF is 3.5 dB. The circuit also provides reverse isolation of -26 dB and IIP3 of -1.5 dBm.

A 5 GHz LNA to be used in wireless LAN receiver has been fabricated in the paper [61] using 0.18 µm CMOS technology. The proposed LNA circuit consists of an amplification stage followed by an output buffer. The amplification stages utilizes cascode topology that uses two n-channel MOSFET, of which one of the NMOS is in CS stage while other NMOS is in CG stage. The input is applied at the gate of the CS stage and a source degenerated inductor formed by parallel combination of the three bond wires is connected at the source of the CS stage. The output buffer is used to convert amplified signal to differential. Also, a VGA cell is present in parallel to LNA input so as to adjust gain to increase the dynamic range. The simulated S_{21} parameter of LNA is 25 dB, NF is 1.5 dB and the amplification stage consumes a current of 6 mA from 1.5 V.

A LNA using FDC has been designed for 5 GHz, using 0.25 µm CMOS technology in [62]. The original LNA circuit is same as conventional cascode LNA circuit with load as inductor. Two large resistive dividers are used as couplers for simplification of the circuit and noise minimization while unit gain CS amplifier having inductor as load is used as time delayers. So, for cancellation performance to be best the delay constant and coupler coefficient should be optimized. Also, a multiplier is formed by two MOS namely M1 and M2. The output of the original LNA is coupled to M2 acting as source follower while the M1 is in saturation and coupled signal is fed into it. The simulation is carried out in Agilent ADS. A power gain of 17.4 dB, NF of 1.22 dB, reverse isolation of -32 dB, input reflection coefficient and output reflection coefficient both of -23 dB is provided by the whole LNA. Without degrading any noise and gain the IIP3 is boosted from 5 dBm to 21 dBm.

A RF CMOS LNA performance at 5 GHz has been analyzed using 90 nm technology for designing. The LNA architecture uses a CS cascode topology with source degenerated inductor. The input signal is applied to the gate of CS amplifier in cascode topology through inductor and inductor is also used as load. A gain of 13 dB along with NF of 2.7 dB is obtained by the circuit using 1.2 V power supply and consuming power of 9.7 mW [63].

The LNA is proposed for 5 GHz frequency in [64] designed using 90 nm CMOS process. The proposed LNA design consists of a cascoded amplifier using gm enhanced technique which is followed by feedback transistor in source follower configuration. A capacitor is used to DC block the feedback resistor. Another source follower is used which form transconductance with the mixer. A 42 mW of power is consumed from 2.7 V power supply. The simulation results shows that the S11, gain, NF and IIP3 is -13 dB, 25 dB, 2 dB and -14 dBm respectively [64].

A differential LNA having variable gain have been designed for WLAN application. The core of LNA circuit is cascoded CS inductive degenerated differential topology. Another set of transistors, known as cascoded transistor is cascoded with the input stage and forms CG stage. They are also implemented in differential pair and are present between input transconductor and the load giving rise to variable gain characteristic. The circuit is designed using 0.18 µm technology and 1.5 V supply. The simulation results of the circuit simulated in Cadence Spectre RF is -11.8 dB input reflection coefficient, -17.75 dB reverse isolation, 12.34 dB gain, 3.98 dB NF and -1.24 dBm IIP3 for high gain mode and have -25 dB input reflection coefficient, -23.9 dB reverse isolation, 6 dB gain, 4.25 dB NF and 1.71 dBm IIP3 for low gain mode. LNA circuit requires an area of 1.3 mm x 1.9 mm [65].

In [66] LNA using ultra low voltage supply of 0.6 V is designed using 0.13 µm technology. The LNA utilizes CS amplifier along with darlington pair. Darlingtion pair is implemented using resistive degeneration as improves linearity and the noise. The gate source voltage of the common source stage is provided by the quiescent current of darlington pair transistor, flowing through the degenerated resistor. The circuit is simulated in spectre giving value of input reflection coefficient less than -10 dB, voltage gain of 25 dB, minimum NF of 1.8 dB and IIP3 of 10 dBm while consuming a power of 0.85 mW.

TABLE VIII. COMPARISON OF LNA AT 5 GHZ

	[60]	[61]	[62]	[63]	[64]	[65]		[66]
Technology (µm)	0.25	0.18	0.25	90 nm	90 nm	0.18		0.13
Supply (V)	-	1.5		1.2	2.7	1.5		0.6
S_{21} (dB)	16.6	25	17.4	13	25	High gain mode	Low gain mode	25
						12.34	6	
NF (dB)	2.38	1.5	1.22	2.7	2	3.98	4.25	1.8
IIP3 (dBm)	-1.5		21	-	-14	-1.24	1.71	10

9. 5.2 GHz

A 5.2 GHz LNA is implemented using interstage series technique in [67]. The LNA circuit consists of two stages, the stage 1 consists of a CS amplifier (M1) and a diode connected transistor (M4) which is used for voltage drop and to decrease the quality factor of the inductor so as to increase stability. The stage 2, uses the cascode architecture consisting of two transistor and a degenerated inductor to improve the linearity. The inductor used as load and output capacitor is used for output matching. An inductor is present between the two stages thus acting as interstage inductor. The circuit is designed using 0.18 µm CMOS technology and uses 2.7 V supply. A gain of 18.9 dB, NF of 1.7 dB and OIP3 of 12.9 dBm is obtained. Also, a power of 22.3 mW is consumed.

A LNA having two stage which uses current reuse technology and interstage series resonance is designed in [68]. A CS amplifier and a cascode stage is used having an inductor between them. Another inductor is present as a load and uses capacitive interstage coupling having an inductor in series. The value of inductor and capacitor are adjusted for series resonance. The interstage series resonance technique is used as is less affected by substrate effect and high gain is provided along with less stability issues. The LNA circuit is designed using 0.35 µm CMOS process with a power supply of 3.3 V for 5.2 GHz. A power gain of 19.3 dB is observed along with NF of 2.45. Also, OIP3 of 13.2 dB is observed while consuming a current of 8 mA.

A 5.2 GHz LNA is designed and implemented using 0.25 µm technology [69]. A common source inductively degenerated topology is used. CS cascode transistor having inductor at the source of value 0.516 nH with quality factor of 10.5 is used so that the gate drain capacitance effect of CG transistor is reduced and also, interaction between tuned output and tuned input is reduced. Resistors are used to form the bias circuit. The circuit is designed using ADS. The simulated value of S_{11}, S_{12}, S_{21}, S_{22} and NF is -10.04 dB, -25.2 dB, 11.04 dB, -11.05 dB and 3.249 dB.

TABLE IX. COMPARISON OF LNA AT 5.2 GHZ

	[67]	[68]	[69]
Technology (µm)	0.18	0.35	0.25
Supply (V)	2.7	3.3	-
S_{21} (dB)	18.9	19.3	11.04
NF (dB)	1.7	2.45	3.249
OIP3 (dBm)	12.9	13.2	-

10. 5.8 GHz

A 5.8 GHz LNA that can control gain and frequency is designed in [70] using 0.18 µm CMOS technology. The proposed circuit uses folded cascode configuration that uses NMOS and PMOS for reduction of supply voltage. Here, gate voltage of PMOS is controlled to attain gain control i.e. adjusting overall gain of the LNA without affecting its input noise and input matching which depends on NMOS. Moreover, varactor is added at resonant tank circuit for achieving the frequency tuning. S_{11}, S_{21}, S_{22}, NF, power dissipation and gain tuning are -5.3 dB, 13.2 dB, -10.3 dB, 2.5 dB, 22.2 mW and 12.8 dB respectively for a supply of 1V and are -7.1 dB, 7 dB, -12.3 dB, 2.68 dB, 12.5 mW and 7 dB respectively for 0.7 V supply. The frequency tuning for both 1 V and 0.7 V supply is 360 MHz. Also, the total chip area is 0.9 mm x 0.8 mm including bonding pads.

A two stage LNA circuit is designed in [71] using 0.35 µm 1P4M (one poly layer for gate and four metal layers for interconnection) CMOS technology. The first stage is a CS architecture with degenerated inductor at its source while the second stage is a CG architecture. The two stages have an inductor between them. The voltage is applied to the gate of CS amplifier through inductor. The value of input reflection coefficient is -11dB, gain is 7.2 dB, output reflection coefficient is -17dB, NF is 3.2 dB and IIP3 is 6.7 dB. The circuit uses 1.3 V and dissipates a power of 20 mW. The area required for the circuit without on chip pads is 0.63 mm x 0.46 mm.

Cascode architecture is employed in designing of the LNA at 5.8 GHz. The cascode configuration uses two transistor along with degenerated inductor and the gate of these transistors are connected to gate of other transistors that are also in cascode. The circuit design uses 1.5 V power supply and is designed using 0.18 µm CMOS process. A chip of area 0.9 mm^2 is used. When the power dissipation is 15 mW then the minimum NF is 1.5 dB and when the power dissipation is 8 mW then the minimum NF is 1.8 dB. However, if power dissipation is 15 mW then the gain is 28 dB if LNA is followed by super source follower buffer and is 14 dB if output is matched to 50 Ω impedance while if the power dissipation is 8 mW then the gain is 23 dB if LNA is followed by supreme source follower buffer and is 13 dB if output is matched to 50 Ω impedance [72].

TABLE X. COMPARISON OF LNA AT 5.8 GHZ

	[70]		[71]	[72]
Technology (µm)	0.18		0.35	0.18
Supply (V)	0.7	1	1.3	1.5
S_{21} (dB)	7	13.2	7.2	28
NF (dB)	2.68	2.5	3.2	1.5

11. 24 GHz/K Band

A simple topology is chosen to design the LNA in 0.18 µm technology for 24GHz. The transistor uses three stages of common stage amplifier with inductive source degeneration. In the first stage of the circuit topology the transistor is scaled and the gate inductance is used for shifting of noise optimizing impedance to 50 Ω. Each stage output is loaded using high pass combination of inductor and capacitor so as to increase the gain and obtain parallel resonance. A input return loss of 11 dB, output return loss of 22 dB, reverse isolation of -33.18 dB, gain of 12.78 dB, NF of 5.6 dB and IIP3 of 2.04 dBm is obtained. Also, a current of 30 mA is consumed from 1.8 V supply. The chip size is 1.05 x 0.7 mm^2 [73][74].

Cascoded two stage CS architecture is used in designing of LNA using 0.18 µm technology and to be operated at 24 GHz [75]. Here, for the noise, the first stage is designed and for the gain, the second stage is designed. The CS amplifier has degenerated inductor which is connected to the source and series combination of inductor and capacitor is used as load. A high pass combination of inductor and capacitor is used to as the interstage network. The simulated design has input return loss of 18 dB, output return loss of 23 dB, gain of 13.1 dB, NF of 3.9 dB and IIP3 of -12.3 dBm, a supply voltage of 1 V is used for operation consuming a power of 14 mW. 0.57 x 0.6 mm2 is the chip area.

TABLE XII. COMPARISON OF LNA AT 24 GHZ

	[73]/[74]	[75]
Technology (µm)	0.18	0.18
Supply (V)	1.8	1
S_{21} (dB)	12.78	13.1
NF (dB)	5.6	3.9
IIP3 (dBm)	2.04	-12.3

B. Ultra-wideband

The ultra-wide band (UWB) has been approved in US by the Federal Communication Commission (FCC), ranging from 3.1-10.6 GHz, for use for commercial applications recently [76]. In the recent years, significant interest has been developed in Ultra-wideband (UWB) technology for wireless communication, since a wide frequency band spectrum, transmission of data at very low power, high data rate and low cost is provided by it provides [77]. So, majority of LNA topologies for UWB is defined for frequency ranging from 3.1-10.6 GHz.

The LNA for UWB has been designed in the paper [78] using 0.13 µm CMOS technology. The proposed LNA circuit is divided into two stages and three sub-circuits, the first stage is CG as its input impedance is $1/g_m$ so as to achieve the input impedance at 50 Ω. The second stage is CS amplifier stage. A matching circuit is present between the first and the second. The gain is of value 14.73 dB, S_{11} is below -10 dB, NF is less than 4 dB.

A two stage LNA based inverter is designed in [79] using 0.18 µm CMOS technology. The NMOS transistor reuses the current of PMOS transistor. Therefore, for NMOS additional driving current is not required. Pi-matching is used to achieve input impedance matching. The LNA circuit uses 1.8 V power supply and consumes a power of 18 mW. The input reflection coefficient value is less than -10.7 dB, gain is 13.7 dB, NF is 2.3 dB and IIP3 is -0.2 dBm. The power dissipated is 18 mW. The chip area is 0.39 mm^2.

Two stage cascode LNA topology with degenerated inductor is designed using 0.18 µm process. Between the CS and CG device an inductor is present The CG amplifier uses a resistor for feedback and hence, is called current reuse topology. Three section band pass Chebyshev filter is used at input to achieve wideband input matching and flat gain. The simulated results are 20 dB maximum gain, -28 dB input return loss, -25 dB reverse isolation, -9.7 dB output return loss, NF ranging from 2.89 to 6.5 dB and IIP3 of 10 dBm. The power consumed is 12 mW from 1.8 V supply [80].

A LNA to be operated from 3.1 GHz to 10.6 GHz is designed using 0.18 µm process. The first stage consists of a CS transistor and CG transistor in cascode configuration having a degenerated inductor and an inductor between the two amplifier stages. Also, shunt feedback topology is used in the first stage. It is followed by two transistor in cascode of which one transistor is used as current source to bias the other transistor. The circuit is simulated in Agilent ADS. Gain of 19.982 dB, NF of 1.27 dB, input reflection coefficient of -31.670 dB, output return loss of -7.449 dB is obtained [81].

A noise cancelling LNA is designed in [82]. The LNA designed has two stage where the first stage or the input stage uses a current reuse circuit to save power and noise cancelling topology is utilized in the second stage of the LNA. The CMOS LNA is designed using TSMC 0.18 µm process and is simulated using Agilent ADS tool. The input and output return loss is less than -10 dB, gain is 15.33 dB, NF is 2.65 dB and IIP3 is -5.5 dB. The LNA circuit using a voltage of 1.3 V and dissipates a power of 9.1 mW.

A CS amplifier using inductor for degeneration at source is present at the first stage of the LNA and at the second stage a CS amplifier is present. At the gate of the two amplifier two series peaking inductor is used. Resistive shunt shunt feedback is applied to the first stage. A supply of 0.8 V is used in the circuit and a current of 11 mA is consumed. The gain of 13.1 dB, reverse isolation of -25 dB, input return loss of less than -10 dB and NF of 3.25 dB is achieved. The circuit uses a chip area of 0.6 mm x 0.75 mm [83].

A 90 nm CMOS low noise amplifier is designed in paper [85]. An inductively degenerated inverter cell is used as the first stage of the low noise amplifier design to operate over large bandwidth having high pass filter at the input to obtain low value of input reflection coefficient and desired low cutoff characteristics. The self-biased resistive shunt shunt feedback amplifier is present is second stage to decrease the consumption of power. The self forward bias technique is used to bias the first stage to achieve low power consumption goal. The simulated results shows that the input reflection coefficient is less than -10 dB, gain is 13.9 dB, NF is 1.35 dB and IIP3 is -3 dBm. A power of 13.5 mW is consumed from 0.9 power supply.

TABLE XII. COMPARISON OF LNA FOR 3.1-10.6 GHZ

	[78]	[79]	[80]	[81]	[82]	[83]	[84]
Tech. (µm)	0.13	0.18	0.18	0.18	0.18	0.18	90 nm
Supply (V)		1.8			1.3	0.8	0.9
S_{21} (dB)	14.73	13.7	20	19.982	15.33	13.1	13.9± 1.42
NF (dB)	4	2.3	2.89 -6.5	1.27	2.65	3.25	1.35
IIP3 (dBm)	-	-0.2	10	-	-5.5	-	-3

IV. CONCLUSION

From the above literature survey it can be concluded that for improving the performance of the LNA several techniques and topologies have been proposed. Out of the four basic topologies i.e. the CS with resistive termination, series shunt feedback, CG and, CS inductive degeneration topology; the commonly used and most efficient topology used as the LNA core is CS with inductive degeneration. It is the topology used for both narrowband and UWB. It is also most commonly used in differential form. Here, cacsode configuration is preferred to reduce miller and improves the reverse isolation. Secondly, CG topology is used if high input impedance matching is required. Most commonly used software for simulation of the LNA is Cadence Spectre RF and ADS.

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Appendix IV:
ADS
(Advanced Design Simulation Software)

In the field of radio frequency, microwave and high speed applications the leading automation design software is using EDA (Electronic Design Automation) software tool for simulation and designing and that software is Agilent ADS (Advanced Design System). A division of Keysight Technologies, Keysight EEsofEDA produces the ADS. An environment for integrated design is provided by ADS to radio frequency electronic product like satellite communications system, radar system and mobile phones designers. Each and every step of designing process such as schematic design, design checking, time and frequency domain circuit simulation and layout is supported by ADS for optimizing and characterizing radio frequency design. Therefore, the key benefits of the ADS system:

- Complete schematic and complete layout environment.
- Direct and full access to 3D EM field solvers.
- Integration of design flow with Cadence, Mentor and Zuken.
- Wireless libraries are up to date.
- Process designing kits are developed in large number.

Appendix V:
802.15.4 and Zigbee

IEEE 802.15.4

In the open system interconnection (OSI) model, 802.15.4 standard defines the communication layer at level 2 i.e. data link layer. It allows the two devices to communicate with each other. Institute of Electrical and Electronics Engineering (IEEE) created the 802.15.4, which sets standards so that technological developments have same sets of rule. In the data link layer, information units i.e. bits are organized to become electromagnetic pulses in the lower level i.e. physical layer. The frequencies are distributed in 27 different channels which are divided into three main bands as follows:

Frequency	**868.0 - 868.6 MHz**	**902.0 - 928.0 MHz**	**2.40 - 2.48 GHz**
Geographical Region	Europe	America	Worldwide
Number of Channels	1	10	16
Channel Bandwidth	600 KHz	2 MHz	5 MHz
Symbol Rate	20K symbols/s	40K symbols/s	62.5K symbols/s
Data Rate	20K bits/s	40K bits/s	250K bits/s
Modulation	BPSK	BPSK	Q-QPSK

Zigbee

In the open system interconnection (OSI) model, Zigbee standard defines the communication layer at level 3 and the upper layer. It allows communication between numbers of device by creating network topology and also provides communication features such as authentication, encryption and association. Zigbee Alliance is the set of companies that created the standard.