A DISSERTATION

on

VOLTAGE DIFFERENCING TRANSCONDUCTANCE AMPLIFIER (VDTA) AND ITS APPLICATIONS

Submitted in partial fulfillment of the requirement for the award of Degree of

MASTER OF TECHNOLOGY

in

VLSI Design and Embedded Systems

Submitted by

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CERTIFICATE

This is to certify that the dissertation titled "**Voltage Differencing Transconductance Amplifier (VDTA) and its Applications**" has been completed by me**,** submitted in partial fulfillment of the requirement for the award of degree of **Master of Technology** in **VLSI Design and Embedded Systems**. Further it is declared that the work done in this thesis has not been published/submitted earlier in any conference, publication or in any institution and is my own original and authentic work.

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This is a record of his own work carried out by him under my supervision and support. He has completed his dissertation work with utmost sincerity and diligence.

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ABSTRACT

Analog VLSI is playing an important part in technology now a days. A vast range of circuits (Amplifers, Filters, Comparators, Oscillators, Multipliers, PLL, Voltage/Current References, Sample-And-Hold Circuits, A/D and D/A Converters, High speed IO Interface etc.) are being introduced now a days for new applications for the purpose of information processing like speech recognition, integrated sensors, handwriting recognition, image processing etc.

In this report an Analog Building Block, Voltage Differencing Transconductance Amplifier (VDTA). The realization of which is given in 2011 is simulated using TSMC 0.18 µm CMOS Technology process parameters. VDTA has two different values of transconductances which eliminate the need of external resistors for most of the applications based on VDTA. Also, the application of VDTA as filter, parallel R-L impedance, controller and oscillator has been simulated and presented in this report.

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LIST OF ABBREVIATIONS

AC	Alternating Current
BOCCII	Balanced Output Current Conveyor Second Generation
CCI	First Generation Current Conveyor
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
CCTA	Curent Conveyor Transconductance Amplifier
CDTA	Current Differencing Transconductance Amplifier
CMOS	Complementary Metal Oxide Semiconductor
CTTA	Current Through Transconductance Amplifier
dB	Decibel
DCCII	Differential Current Conveyor Second Generation
DDCC	Differential Difference Current Conveyor
DDCCTA	Differential Difference Current Conveyor Transconductance Amplifier
DOICCII	Dual Output Inverting Current Conveyor Second Generation
DXCCII	Dual X Current Conveyor Second Generation
FDCCII	Fully Differential Current Conveyor Second Generation
FD Op-Amp	Fully Differential Operational Amplifier
FD OFA	Fully Differential Operational Feedback Amplifier
FD OTA	Fully Differential Operational Transconductance Amplifier
FD OTRA	Fully Differential Operational Transresistance Amplifier
FDVCCII-	Fully Differential Voltage Second Generation Inverting Current Conveyor
IC	Integrated Circuit
MHz	Mega Hertz
MOCCCA	Current Controlled Current Amplifier with Multi Outputs

MOCCI	Multiple Output First Generation Current Conveyor
MOCCII	Multiple Output Second Generation Current Conveyor
MOCCIII	Multiple Output Third Generation Current Conveyor
NMOS	N- Channel Metal Oxide Semiconductor
OFA	Operational Feedback Amplifier
OFCC	Operational Floating Current Conveyor
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
OTRA	Operational Transresistance Amplifier
PMOS	P- Channel Metal Oxide Semiconductor
PSPICE	Personal Simulated Program with Integrated Circuit Emphasis
QO	Quadrature Oscillator
VDTA	Voltage Differencing Transconductance Amplifier

CHAPTER 1

INTRODUCTION

Analog circuit design is one of the important areas of the present day research and development. For designing an analog circuit two modes are commonly used which are current mode and voltage mode. In the case of voltage mode circuits, the state variables used in the equation that is used to define the circuit is always a voltage. Thus, it can be said that signal states of a voltage mode circuit is determined completely and without any ambiguity by its node voltage. In a similar way, currents are used as state variables in case of current mode circuits. Thus, it can again be said that signal state of a current mode circuit is determined completely without any ambiguity using its branch currents. Theoretically, it is said that voltage mode and current mode circuits are dual of each other [1]. So realising a function in voltage mode or current mode is almost the same thing. Due to certain constraints it may not be possible to fulfil every practical requirement. Thus using a single topology for designing all applications is not possible. Further, high performance supplies are designed using the voltage mode designs. Later in this chapter both the advantage and disadvantage of current and voltage mode designs are discussed. These can be used to find a topology, either voltage or current or mixed topology to satisfy the requirements of the design in the best possible way.

1.1 VOLTAGE MODE CIRCUITS

Earlier all the circuits used voltage mode topology or only the voltage signals were used for the processing purposes. For the ease of understanding of the voltage mode circuits let us take the case of voltage power supply. Voltage power supply is required to maintain a constant output voltage irrespective of load current that is allowed to vary from zero to full rated current of the supply, which means the concern here is the voltage of the output terminals not the current. It is quite clear that in practical scenario, no circuit operates in ideal fashion. For this operation of supplying constant output voltage switched capacitor circuits and charge coupled devices are used whose performance are quite close to the required one. From the basic definition of the voltage we can say that it is the ratio of energy and charge. Since the

energy needed for taking an electron out of the valence band to the conduction band and the charge of electron both are constant. Thus voltage has invariant value providing reliable voltage reference, for a given technology.

ADVANTAGES:

- AC dynamic range in case of voltage mode circuits is determined by internal noise voltage which is generated by Noise currents. The WB NSD is dependent on device parameters and biasing. Total noise is dependent on the absolute frequency range and bandwidth [2].
- Measurement of voltage by different instruments and its accurate display can easily be done without creating any kind of disturbance for circuit elements. These circuits have a finite impedence but they can easily drive compatible circuits with only a very small effect on magnitude. That is the reason these circuits are of great importance both for digital circuit design and analog circuit design [2].
- These circuits provide a very good cross regulation and the reason for this quality is that these circuits offer low impedences at output terminals in case of supply with multiple output.
- Design and Analysis in case of these circuits is easier as these circuits use single feedback loop.

DISADVANTAGES:

When any kind of changes in the output are sensed, then for the sake of correction a feedback loop is used that result in slowing down of the circuit. The requirement of dominant pole or a zero is added to compensate for the filter output that results in addition of 2 poles in control loop. It also results in complication of compensation as the loop gain varies with the variation in the input.

1.2 CURRENT MODE CIRCUITS

Historically the signal processing was dominated by voltage signals, but with development of submicron power technologies, there emerges the need of using low power voltage supply.

But meeting this requirement using voltage mode circuits poses the constraint of linearity and dynamic range as it becomes difficult at submicron technology to design a circuit with high linearity and dynamic range. To resolve this problem either we have to use CMOS technology having the low threshold voltage and also as another option we can opt for standard CMOS technology along with low voltage circuit techniques. These suggested methods are quite expensive, so current mode processing emerged over last few decades as an alternative design technique. The characterisation of current mode circuit is done by low terminal impedence, which makes these circuits suitable for fast response. With the use of current as a signal in current mode circuits we increase the output swing and hence making these circuits to be a better choice for using them under low supply voltage. Thus it can be said that for a fixed supply current mode circuit's dynamic range is larger than the voltage mode circuits. In terms of applications like addition/subtraction, these circuits provide a simplicity over voltage mode circuits as these operations in current mode can simply be performed by joining the terminals at a single point.

ADVANTAGES:

- One of the most significant benefits that the current mode design provides is wide Bandwidth.
- Even at high frequencies the power requirement is low.
- It allows us to shrink the feature size.
- Speed is high.
- Some applications may require current mode interfaces such as in power measurement system in fiber-optics, the input required from photodiode is current [2].
- Without components in the feedback path controlled gain can be achieved.
- Switching Noise is low and the dynamic range is large.

DISADVANTAGES:

- Distortion is high.
- Gain variation is high.

Thus, after looking at advantages and disadvantages of both the voltage mode and current mode circuits we can decide that which circuit is fulfilling our practical requirements to the best possible level and depending on that we can decide the mode to be used in our design.

1.3 ANALOG BUILDING BLOCKS

The demand for analog building blocks is increasing because of advancements in technology which poses new practical requirements, hence motivating towards the development of new building blocks. Some of those blocks are named as follows.Op-Amp, OFA, OTA, OTRA, COA etc. are the operational amplifiers of different types and CCI, CCII, CCIII, DOCCI, DOCCII, DOCCIII are the current conveyors of different types and have been reported in [3]. VDTA, CDTA are again important active elements. The discussion regarding the behavioural models of FD Op-Amp, FD OFA, FD OTRA, FD OTA, FD OCA, FD OFC, DCCII, DXCCII, DDCC etc. is done in [4]. The representation of BOCCII, DOICCII, DDCC and FDCCII by nuller-floating mirror elements.

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CHAPTER 2

LITERATURE REVIEW

In the past few years, analog building blocks have been proved to be one of the most important circuit elements to be used. Since the modern analog building blocks are CMOS based structures, so they meet two most important requirements of present day circuits which are power consumption and limitation of space. CMOS structures reduce the power consumption to a large extent. Along with this they reduce the space utilised in designing the circuit as the passive elements can be implemented using the CMOS design only. Continuous developments are being made in the field of CMOS technology which further helps in achieving the present time motives i.e integration of as many circuit elements as possible on a single chip.

A lot of analog building blocks have been proposed, implemented and used in various applications till now. However this report deals with VDTA which was proposed by Yesil as shown in the literature [18]. This report also shows the simulation of some of its applications as filter, oscillator and parallel R-L inductance. Prior to the proposal of VDTA, a lot of active blocks have been proposed. A review of some of those along with the reference of the literature in which they were proposed is being given in this chapter.

Current Conveyor, which proved to be one of the most important active blocks introduced in [1] and it proved to be an important element especially in instrumentation applications [2], [3]. [1] introduces the current conveyor as the three port network and gives the circuit implementation for the same.

In [4], CCII is introduced. CCII has a different terminal relationship as compared to CCI as introduced in [1]. This also presents the way CCII can be used for the applications namely current amplifier, differentiator, integrator, summer and the weighted current summer. The text also says that if the current is taken as the variable for the computation in an analog signal computer, then current conveyor is going to prove to be a fundamental unit of such computer.

In continuation with [4], Fabre proposed CCIII as given in [5]. This was proposed with the change in terminal relationships current conveyors as given in [1], [4] but still the number of

terminals remained three only. The usefulness of this block as a floating current sensing device is given in [5]. An implementation of CCIII using two CCII's is also given.

In [6], a new block DDCC has been introduced. The paper also presents a CMOS circuit for the implementation of DDCC. It also shows the implementation of block DDCC as frequency selective circuit, multiplier, square rooter and squarer.

In [7], a new realization using CMOS technology for DVCC is given. It is also referred to be an important building block for applications like impedance converter and an instrumentation amplifier operating in the current mode.

In [8], positive and negative floating resistors which are electronically tunable are developed using an OTA designed using CMOS. The circuit have used two OTAs which are balanced and a fully differential OTA. Thus in total it uses three OTAs and the resistance which is realised in this paper has a linear control by the external biasing current and that too over a range greater than three decades.

In [9], CDBA is proposed. It is explained as an active block with two inputs and two outputs. It is implemented practically using CFA which is available in the market as AD844.

In [10], a FDCCII is introduced. The blocks finds its utility in the applications which require mixed mode operation along with a fully differential signal processing.

In [11], a DXCC is proposed and its usefulness for filtering in continuous time domain is also given. The linearity of the device is also high when the input applied to the device is a large signal. This also helps in reducing the total number of MOSFET resistors and total number of active devices in MOSFET-C filters which operates in continuous time domain.

In [12], CDTA is introduced and an implementation of this block using two CCIIs and one OTA is given. This device is introduced with two current inputs and two current outputs.

In [13], a survey is presented for the elements that are used for the current mode signal processing. All the elements surveyed in this paper are implemented using CDTA and CTTA.

In [14], CCTA is proposed and its implementation using CMOS technology is given. This element can be used not only in the current mode circuits but also in voltage mode and mixed mode circuits.

In [15], an active block FB-VDBA is proposed. In the input stage of this element a fully differential OTA is present and to each output of OTA, a voltage buffer is connected.

In [16], three different realisations using the CMOS technology for FDVCCII- are proposed. The realisation which is given first has a limitation of the input range and rest of the two realizations are provided with a rail to rail input range and they are very good in terms of Bandwidth and linearity. A floating gyrator as an application for FDVCCII- is also proposed in this paper, which is used to realize a floating inductor which in turn is used to realize a second order low pass filter.

In [17], an analysis of active elements that are used in voltage mode, current mode and mixed mode analog signal processing applications is given. It also refers to problems involved in utilising these elements in linear applications. It also proposes a method to generate various new active elements having utilization in signal processing.

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CHAPTER 3

VDTA

3.1 INTRODUCTION

Analog signal processing that forms the base of modern day technology widely uses active elements and the example of which can be seen in filters, oscillators etc. Many of the active elements have been proposed [1] - [13] because every active element have some important and unique features as compared to the other one such as input or output terminals. In [14] all the active elements are reviewed and many new elements are introduced whose realisations have not been given yet.

VDTA is an acronym used for Voltage Differencing Transconductance Amplifier. In case of VDTA, voltage at the differential input (V_{VP},V_{VN}) results into the current leaving the terminal Z by one transconductance gain and the voltage at Z results into the current at the terminals X+ and X- by another transconductance gain. The external bias current is capable of electronically controlling both the transconductance gains. If we compare VDTA with other active blocks [1] – [8], the advantageous feature that VDTA shows is that it has 2 different transconductance values , so a lot of applications such as oscillator, inductance, biquad filters can be realised with a single active block used in addition to one or two capacitors. One other important feature is the capability of this block to be used in transconductance mode applications because of the reason that voltage is at input terminals and on the other hand current is at the output terminals.

3.2 DESCRIPTION OF CIRCUIT

The symbol that is used to represent the circuit of VDTA [15] is given in Figure 1. Here V_P and V_N are the terminals at which input is applied and Z, X+, X- are the terminals where output is obtained. A high impedence value is exhibited by all these terminals. For an ideal VDTA, the terminal relationship can be described by the matrix given below.

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_Z \end{bmatrix}$$

Matrix equation representing the terminal relationship of VDTA [15]

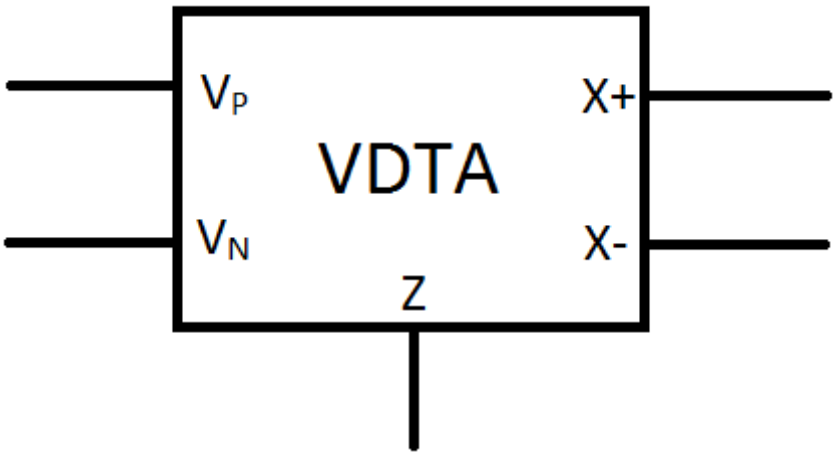

Figure 1: Circuit symbol of VDTA[15]

Using the above matrix equation the terminal relations in simple mathematical equations can be expressed as

$$I_z = g_{m1}(V_{VP} - V_{VN}) \quad (3.1)$$

$$I_{X+} = g_{m2}V_Z \quad (3.2)$$

$$I_{X-} = -g_{m2}V_Z \quad (3.3)$$

The implementation of input and output stage can be done using floating current sources. The voltage applied at the input terminals results into an output current at terminal Z. The voltage present at the terminal Z further results into output current at terminals X+ and X-. CMOS realisation of VDTA [15] is given in Figure 2. The transconductance at input and output terminals of VDTA element described in the circuit in Figure 2 is given by output transistors transconductances. The approximated expressions for the transconductances are

$$g_{m1} = \frac{g_3+g_4}{2} \tag{3.4}$$

$$g_{m2} = \frac{g_5+g_8}{2} \tag{3.5}$$

or

$$g_{m2} = \frac{g_6+g_7}{2} \tag{3.6}$$

Here g_i represents the value of transconductance for i^{th} transistor .

The value of the transconductance for a transistor is given by

$$g_i = \sqrt{I_{Bi}\mu_i C_{ox}\left(\frac{W}{L}\right)_i} \tag{3.7}$$

Here,

μ_i represents the carrier mobility for NMOS or PMOS transistor depending on whether i is p or n , where p is for PMOS and n is for NMOS transistor.

C_{ox} is the gate capacitance per unit area.

W is the value of effective channel width.

L is the value of effective channel length.

I_{Bi} is the bias current for the i^{th} transistor.

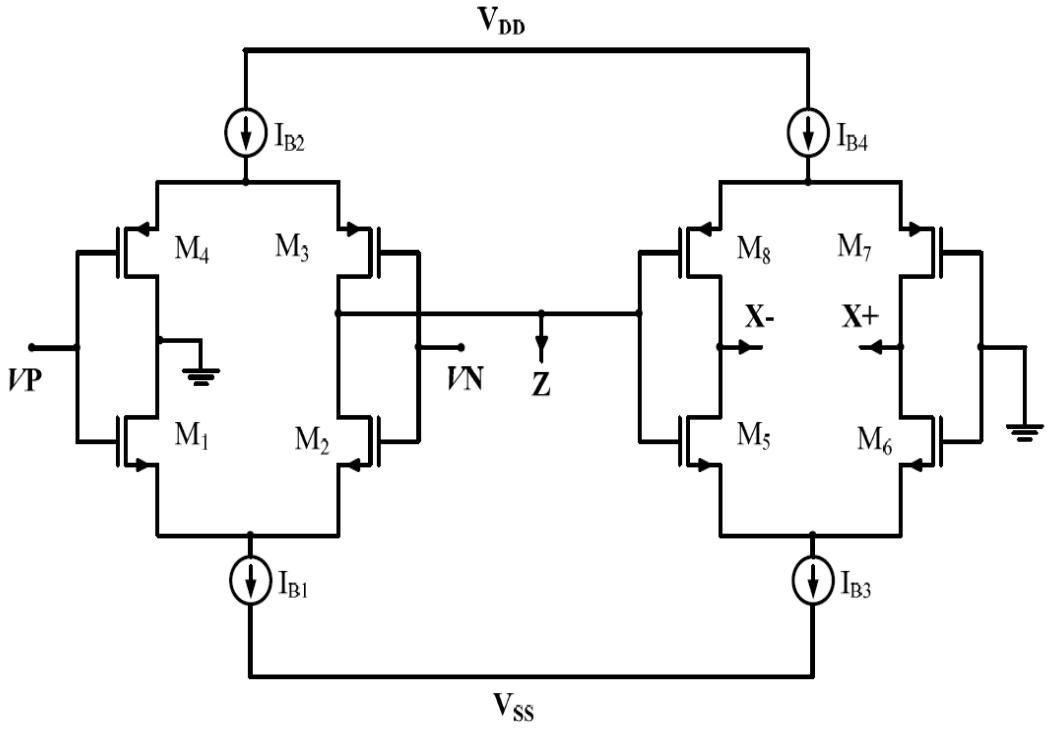

Figure 2 : CMOS implementation of VDTA [15]

The CMOS implementation of VDTA shown above when used in practical applications, sometimes have a different looking structure which uses few more MOSFET's, the reason

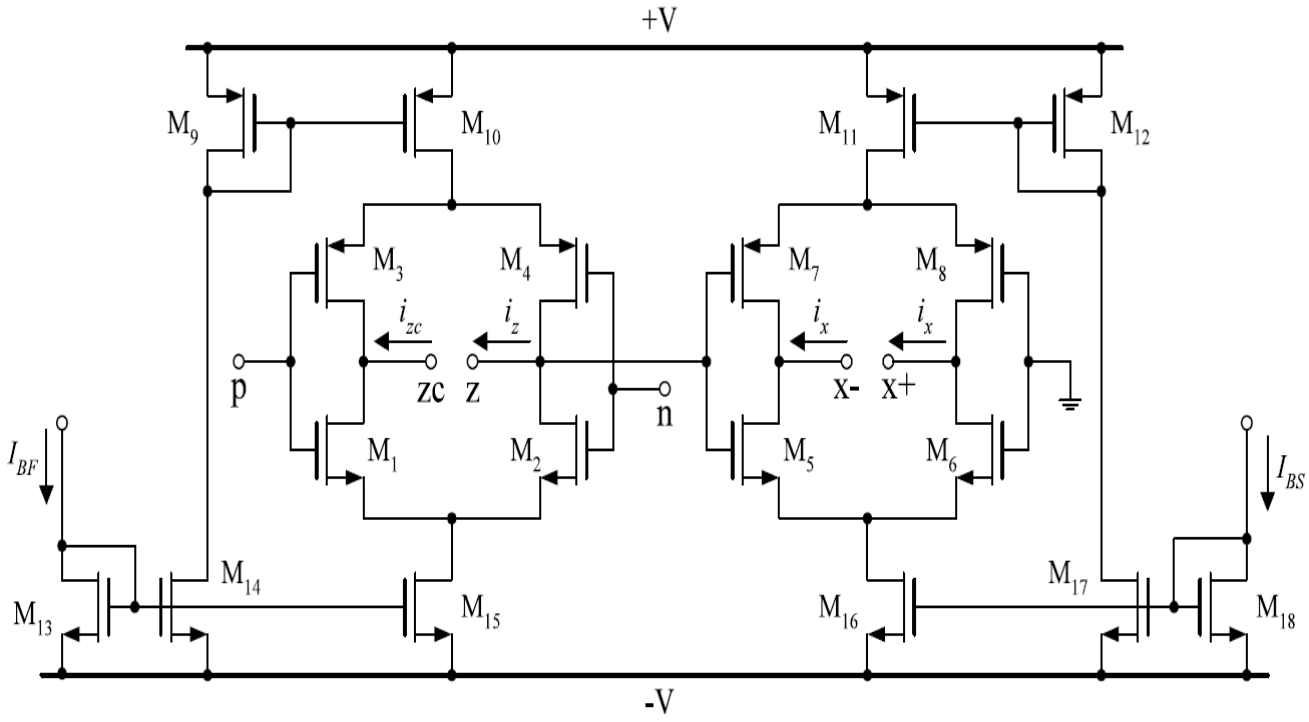

Figure 3 : CMOS implementation of VDTA showing current mirrors in place of current sources [16]

being the current sources shown in the above figure are replaced by the current mirror structures. The design using the MOSFET's instead of current sources is shown in Figure 3.

In Figure 3, we can easily see that M_9 and M_{10} are forming a current mirror and M_{13} and M_{14} as well as M_{13} and M_{15} also form a current mirror. IBF acting as a driving current for these current mirrors and these pair of current mirrors fulfil the requirement of current sources I_{B1} and I_{B2} in Figure 2. Similarly the functioning of I_{B3} and I_{B4} of Figure 2 is done in Figure 3 with the help of current mirrors formed using the MOSFETs M_{11}, M_{12}, M_{16}, M_{17} and M_{18}.

When it comes to the practical implementation of VDTA [17], it can easily be implemented using an already available IC LM13700 [18]. LM13700 is an IC manufactured by Texas Instruments. It consists of two current controlled transconductance amplifiers, each having differential inputs and push-pull outputs, it also provides a feature of adjustable transconductance. The implementation of VDTA using LM13700 is shown in Figure 4.

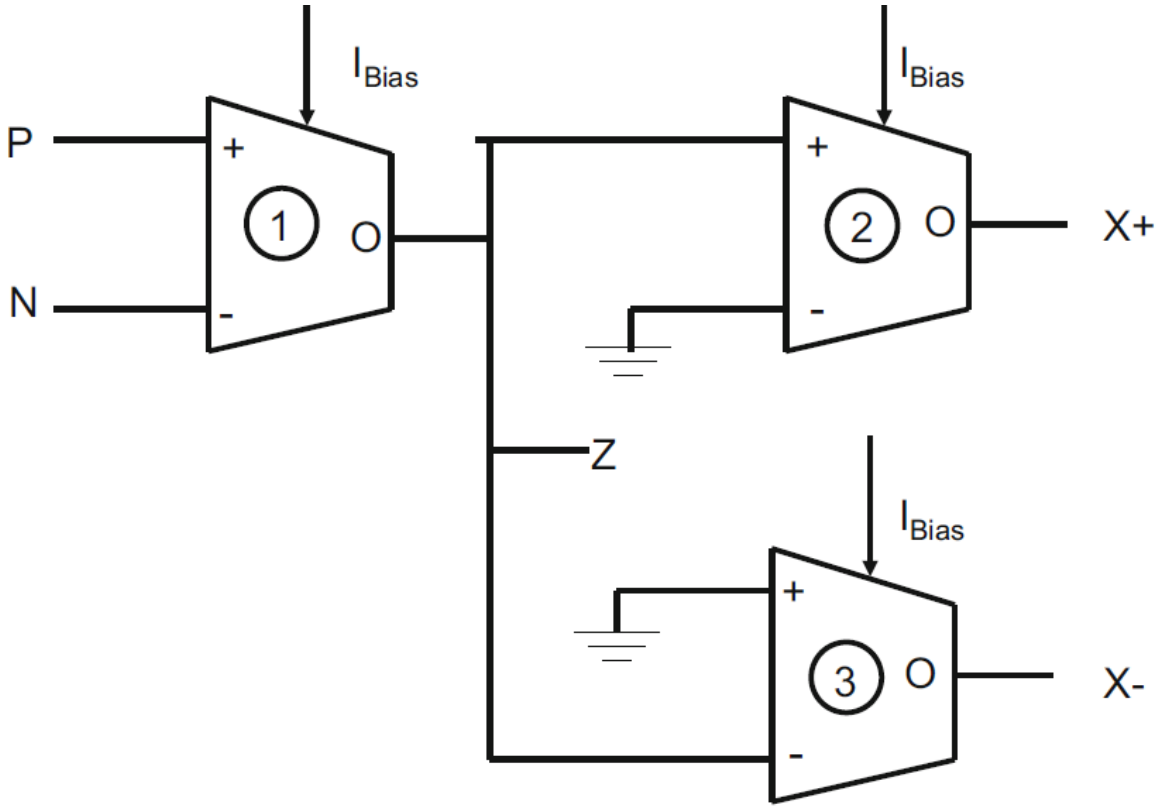

Figure 4 : Implementation of VDTA using OTA [17]

3.3 SIMULATION RESULTS

CMOS implementation of VDTA as described above in Figure 2 is simulated using PSPICE software with TSMC CMOS 0.18µm process parameters. Different Aspect ratios for NMOS and PMOS have been used. These aspect ratios for the different transistors are shown in Table 1.

Transistors	**Width (µm)**	**Length (µm)**
M_1, M_2, M_5, M_6	3.6	0.36
M_3, M_4, M_7, M_8	16.64	0.36

Table 1 : Aspect ratios of Transistors for VDTA [15]

The supply voltage shown in Figure 2 as V_{DD} and V_{SS} are taken to be $V_{DD} = -V_{ss} = 0.9$ V and the bias currents are taken to be $I_{B1} = I_{B2} = I_{B3} = I_{B4} = 150\mu A$. The value of the biasing current and the aspect ratios of the transistors that have been chosen here results in the transconductance values of VDTA which were represented by g_{m1}, g_{m2} to be both equal to 636.3µA/V.

VDTA is here simulated for obtaining both the DC and the AC characteristics of the active block.

The circuit diagram of VDTA used in PSPICE for plotting the DC Characteristics is as given in Figure 5.

The DC characteristics of VDTA that have been obtained after simulation are given in Figure 6. DC characteristics is a plot showing the variation of I_{X+} and I_{X-} with respect to V_Z.

The circuit diagram of VDTA used in PSPICE for plotting the AC Characteristics is as given in Figure 7.

The AC Characteristics of VDTA that have been obtained after simulating the circuit in Figure 7 are given in Figure 8. The AC characteristics show the variation of transconductance gain with respect to the frequency. The simulation results show that transconductance gain drops by 3db at 2.163GHz.

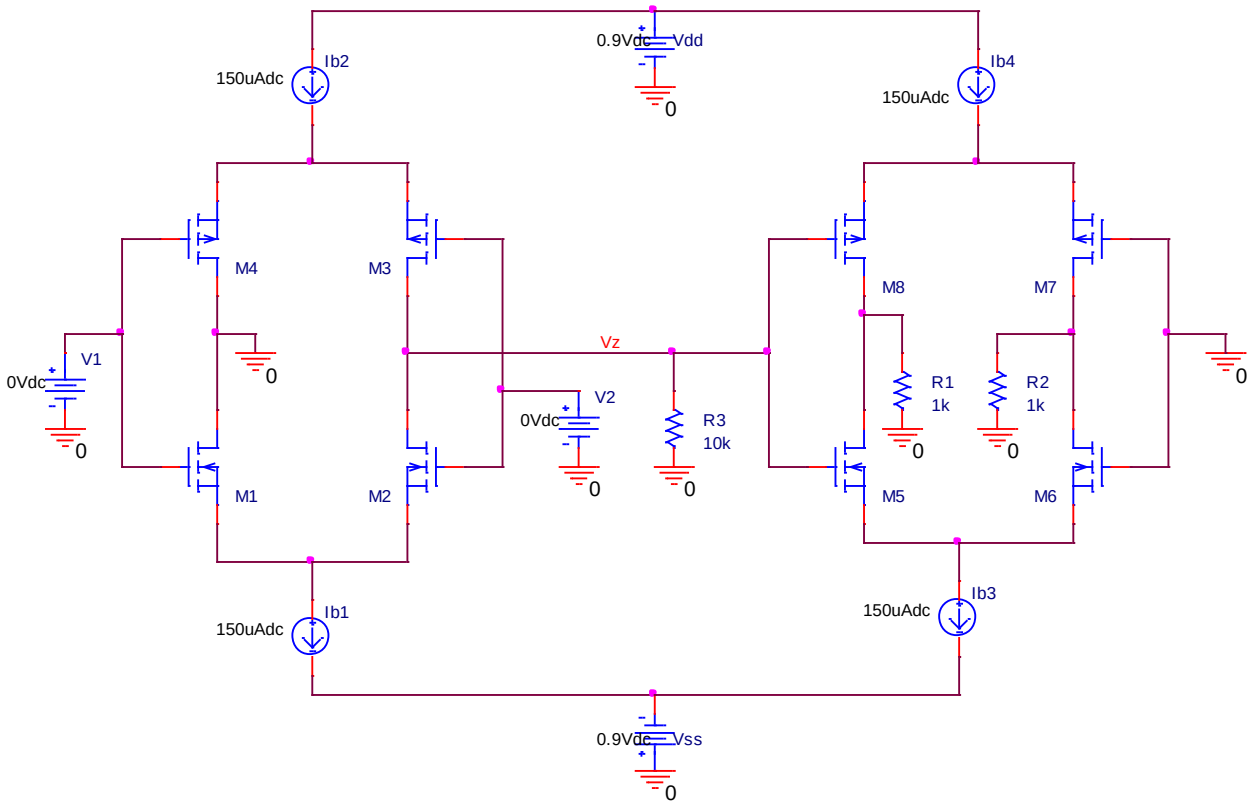

Figure 5 : PSPICE circuit diagram of VDTA to plot DC characteristics

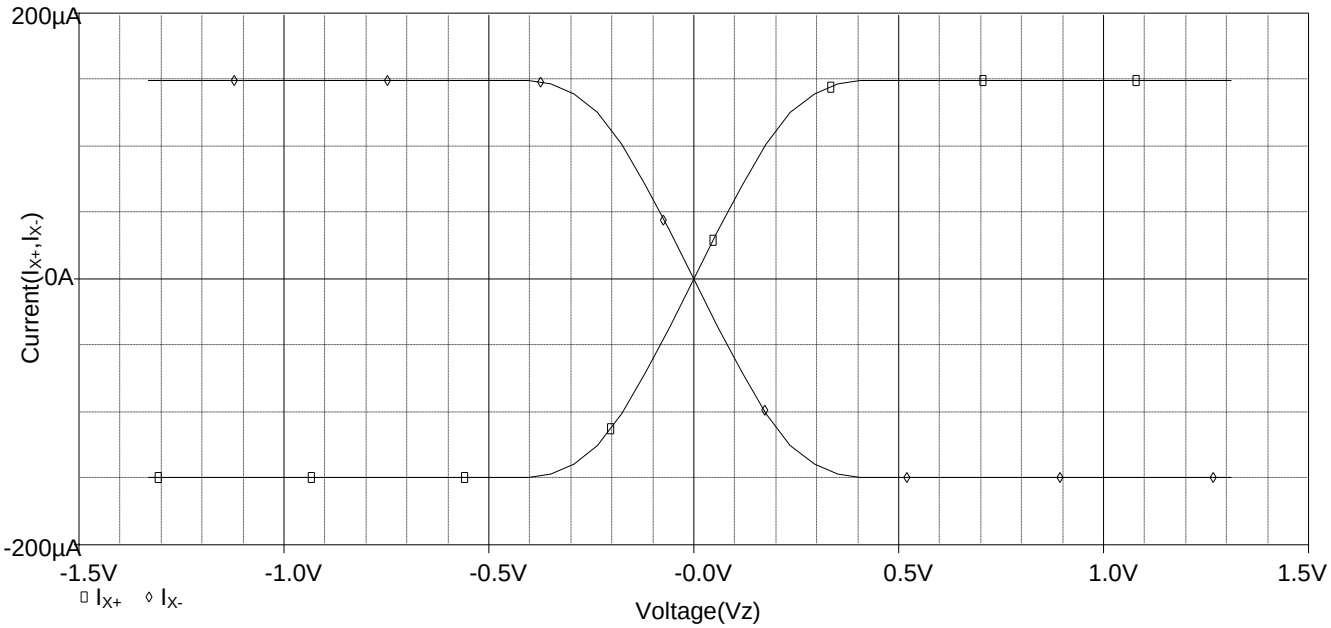

Figure 6 : DC characterstics of VDTA

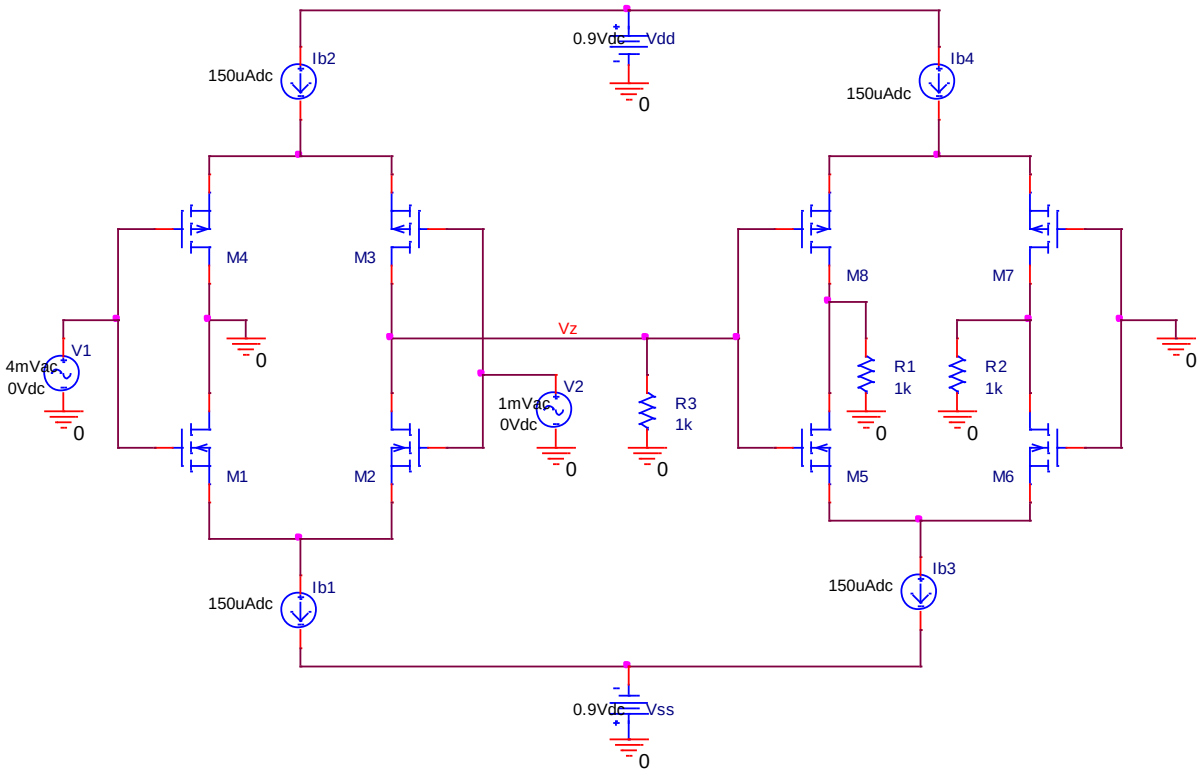

Figure 7 : PSPICE circuit diagram of VDTA to plot AC characteristics

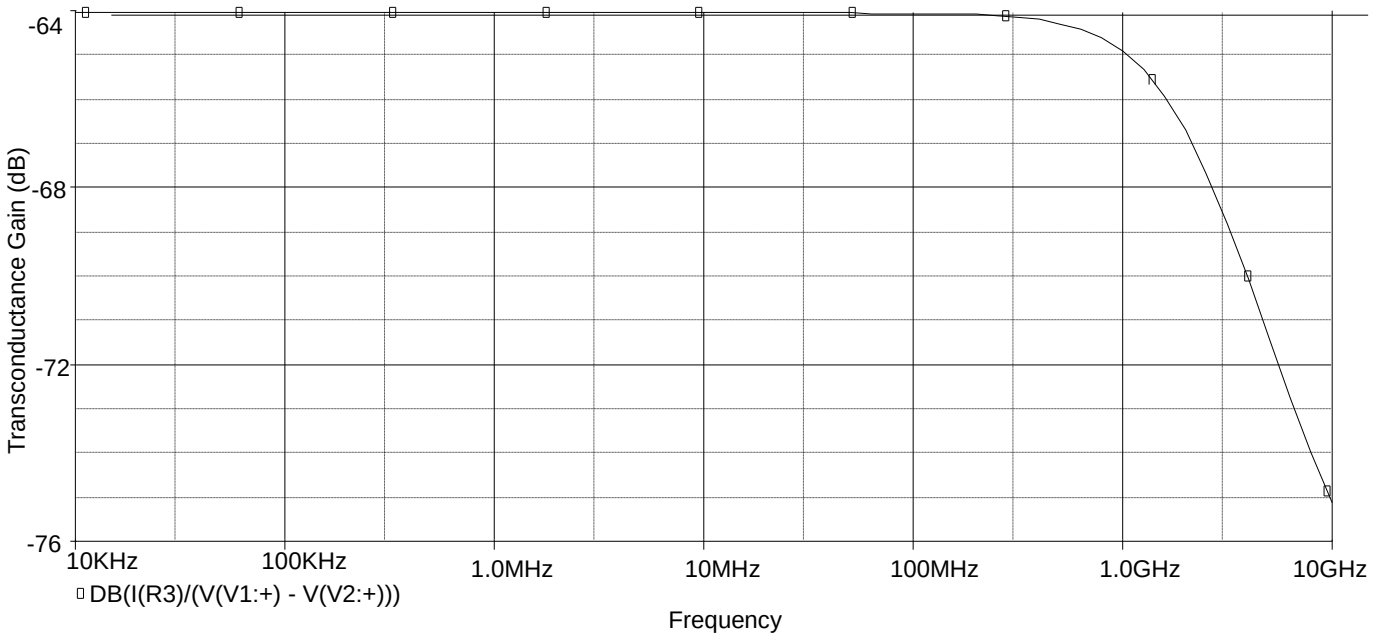

Figure 8 : AC characteristics of VDTA

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CHAPTER 4

FILTERS USING VDTA

4.1 INTRODUCTION

The networks that are used to process the signals taking into consideration the frequency of a signal are known as filters. The explanation of the filters can be given simply by explaining the variation in impedence of capacitors and inductors. If we consider the example of voltage divider in which the element present in shunt leg is a reactive impedence. As soon as there arises a change in frequency, there occurs a change in reactive impedence, so as a result of this the ratio appearing across the voltage divider also changes. This process results into a change in the transfer function at input/output depending on the frequency and this variation of transfer function with frequency is defined as the frequency response.

There are a lot of practical applications of filters. One of the application is the stabilisation of Amplifiers at high frequencies by rolling off gain because at such high frequencies oscillations may occur as a result of excessive phase shift. For this purpose low pass filter is used. Other general application of the filter is to improve response of high gain amplifiers and this is done by blocking the dc offset. For this purpose a high pass filter is used. Filters have the capability to separate the signals on the basis of frequency or in other words they have the capability to pass the signals of interest and block the unwanted frequencies.

A radio receiver can be considered as one of the above said application of filters, it passes the frequencies which we want to process and block the rest of the frequencies or the unwanted frequencies. In data conversion, the elimination of the aliasing effect is done using the filters in A/D systems. At the output of D/A converter, the elimination of higher frequency components which are mainly in this case harmonics of sampling frequency is done using filters, thus filters help in signal reconstruction at output of D/A converter.

If we consider the case of an ideal filter, the amplitude response in the pass band is one or unity and it is zero in the stop band. The point where pass band and stop band of a filter intersect is cut-off frequency. In practical filters, the cut-off frequency is defined as the frequency where the amplitude response of a filter falls below 3-dB point or becomes less than 0.707 times of the maximum value. The variation or changes in the pass band response

are said to be pass band ripples. The steepness or the slope of line joining the pass band and stop band depends on the order of the filter. Order of a filter is equal to the number of poles or number of roots of the denominator of the transfer function.

To represent the filter's frequency domain behaviour mathematically, we define the ratio of output voltage to input voltage in s-domain and it is called as voltage transfer function and is given by

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} \tag{4.1}$$

Here $V_{OUT}(s)$ is laplace transform of output voltage signal and $V_{IN}(s)$ is laplace transform of input voltage signal.

Now if we replace s by jω in the equation 4.1 then we can represent the ratio in terms of magnitude and phase response, Magnitude response is written as

$$\left|H(\mathrm{j}\omega) = \frac{V_{OUT}(\mathrm{j}\omega)}{V_{IN}(\mathrm{j}\omega)}\right| \tag{4.2}$$

And phase response can be written as

$$\arg H(\mathrm{j}\omega) = \arg \frac{V_{OUT}(\mathrm{j}\omega)}{V_{IN}(\mathrm{j}\omega)} \tag{4.3}$$

The quality factor of a circuit is also represented sometimes by α and it is given as

$$\alpha = \frac{1}{\mathrm{Q}} \tag{4.4}$$

4.2 VDTA BASED FILTER TOPLOGIES

Filters have been designed using all the active building blocks defined so far. VDTA proves to be a flexible active block in the realisation of different mode filters. The advantage that we have here is that transconductance can be adjusted with the help of bias currents so we do not rely on external resistors for this purpose. Here in this part of the chapter seven different topologies of filters are presented some of them being in current mode and some of them being in Voltage mode. Some of them are capable of realizing all the filters i.e Band Pass, Low Pass, High Pass, All Pass and Notch filters and some on the other hand are capable of realizing only the Low Pass, Band Pass and High Pass filters. After presenting these filter the

transfer functions of all the filters that are being realised using that topology is given and later on the results of all the simulations that have been done for that particular topology are presented.

4.2.1 TOPOLOGY A

The filter topology presented as topology 1 was introduced in 2011 [1]. This circuit is using only one VDTA and two capacitors and is capable of realizing High Pass, Low Pass and Band Pass filters. The filter presented by this topology is a voltage mode biquad filter. The circuit of this filter is shown in Figure 9.

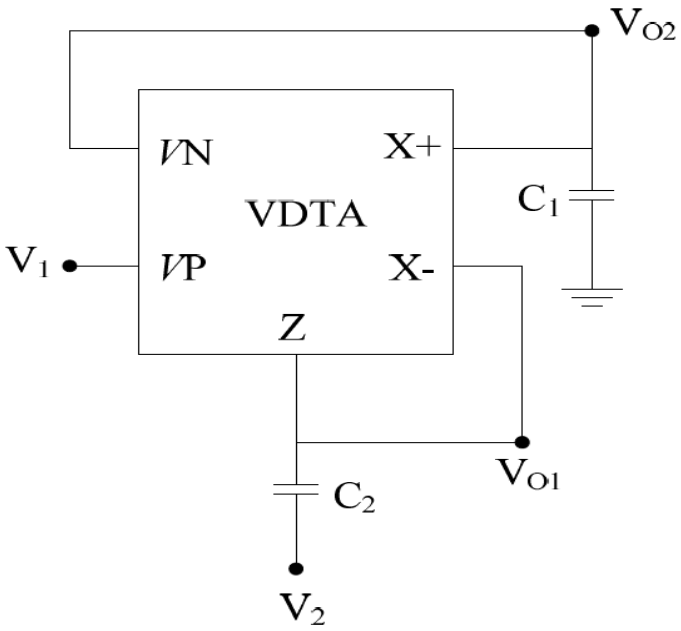

Figure 9 : Biquad Filter (Topology A) [1]

As we can see in figure 9 , input can be supplied at the terminals named as V_1 and V_2 and the output is taken from the terminals indicated by V_{01} and V_{02}. The transfer functions that are obtained after the analysis clearly show the way in which these filters can be implemented. When V_2 terminal is grounded and input is supplied at V_1, then Band Pass and Low Pass filter topologies can be realized. The Band Pass output is obtained at V_{out1} terminal and Low Pass output is obtained at V_{out2} terminal . The transfer functions are written as given in the equations 4.5 and 4.6.

If $V_1 = V_{in}$ and $V_2 = 0$, then

$$\text{Band Pass} \rightarrow \quad \frac{V_{out1}}{V_{in}} = \frac{s\, C_1\, g_{m1}}{s^2\, C_1\, C_{2T} + s\, C_1 g_{m2} + g_{m1} g_{m2}} \tag{4.5}$$

$$\text{Low Pass} \rightarrow \frac{V_{out2}}{V_{in}} = \frac{g_{m1}g_{m2}}{s^2\, C_1\, C_{2T} + s\, C_1 g_{m2} + g_{m1}g_{m2}} \tag{4.6}$$

When V_1 is grounded and V_2 is supplied with the input voltage , then High Pass output is available at V_{out1} and Band Pass output is available at V_{out2} terminal. The transfer functions are written as given in equations 4.7 and 4.8.

If $V_2 = V_{in}$ and $V_1 = 0$, then

$$\text{High Pass} \rightarrow \frac{V_{out1}}{V_{in}} = \frac{s^2\, C_1\, C_2}{s^2\, C_1\, C_{2T} + s\, C_1 g_{m2} + g_{m1}g_{m2}} \tag{4.7}$$

$$\text{Band Pass} \rightarrow \frac{V_{out2}}{V_{in}} = \frac{s\, C_2\, g_{m2}}{s^2\, C_1\, C_{2T} + s\, C_1 g_{m2} + g_{m1}g_{m2}} \tag{4.8}$$

The natural frequency (ω_0) of this topology [1] is given in equation 4.9 and the Quality factor (Q) for the same [1] is given in equation 4.10.

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1\, C_{2T}}} \tag{4.9}$$

$$Q = \sqrt{\frac{C_{2T}\, g_{m1}}{C_1\, g_{m2}}} \tag{4.10}$$

SIMULATION RESULTS:

CMOS implementation of VDTA is as described in Figure 2. The circuit used here which is the circuit of topology 1 is simulated using PSPICE software with TSMC CMOS 18µm process parameters. The aspect ratios for the different transistors used are given in Table 1. The values of capacitors shown in Figure 9 used during this simulation are C_1=1.013pF and C_2=0.863pF.

First of all taking the case: $V_1 = V_{in}$ and $V_2 = 0$.

The circuit diagram used for the simulation of the filter of topology A for the case given above is shown in Figure 10.

Figure 11 shows the output at the node V_{01} which comes out to be a Band Pass filter as mentioned in the equation 4.5. The bandwidth that has been obtained here is approximately 103.24 MHz and the lower cut off frequency is 63.566 MHz and the upper cut off frequency is 166.329MHz.

Figure 12 shows the output at the node V_{02} which comes out to be a Low Pass filter as already mentioned in the equation 4.6. The bandwidth that has been obtained here is 120.405MHz.

Now taking the case: $V_2 = V_{in}$ and $V_1 = 0$.

The circuit diagram used for the simulation of the filter of topology A for the case mentioned above is shown in Figure 13.

Figure 14 shows the output at the node V_{01} which comes out to be a High Pass Filter as mentioned in the equation 4.7. The cut off frequency that has been obtained here is 88.466MHz.

Figure 15 shows the output at the node V_{02} which comes out to be a Band Pass Filter as mentioned in the equation 4.8. The Bandwidth that has been obtained here is approximately 115MHz. The upper cutoff frequency obtained here is 175.206MHz and the lower cutoff frequency obtained here is 60.346MHz. So using this topology we are able to realise the High Pass, Low Pass and the Band Pass Filters with cutoffs as mentioned above.

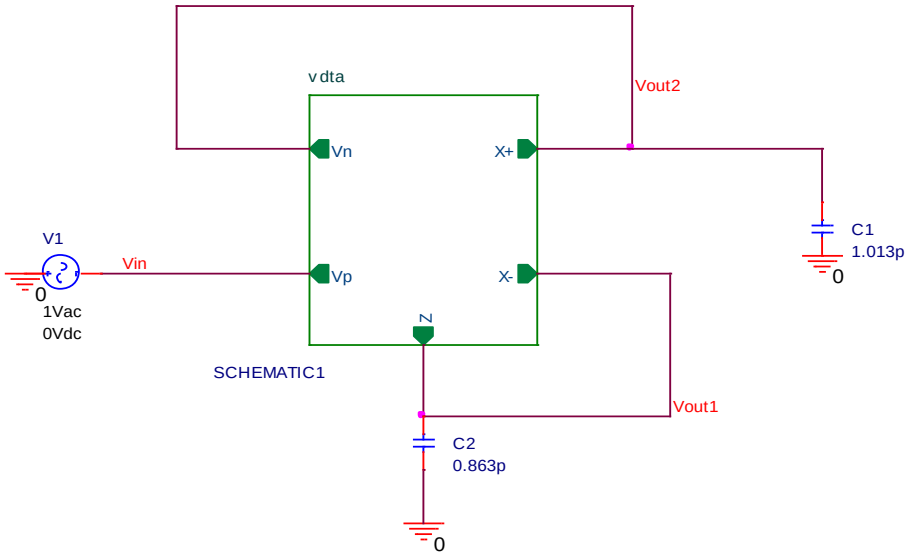

Figure 10 : PSPICE circuit diagram of Topology A ($V_1 = V_{in}$ and $V_2 = 0$).

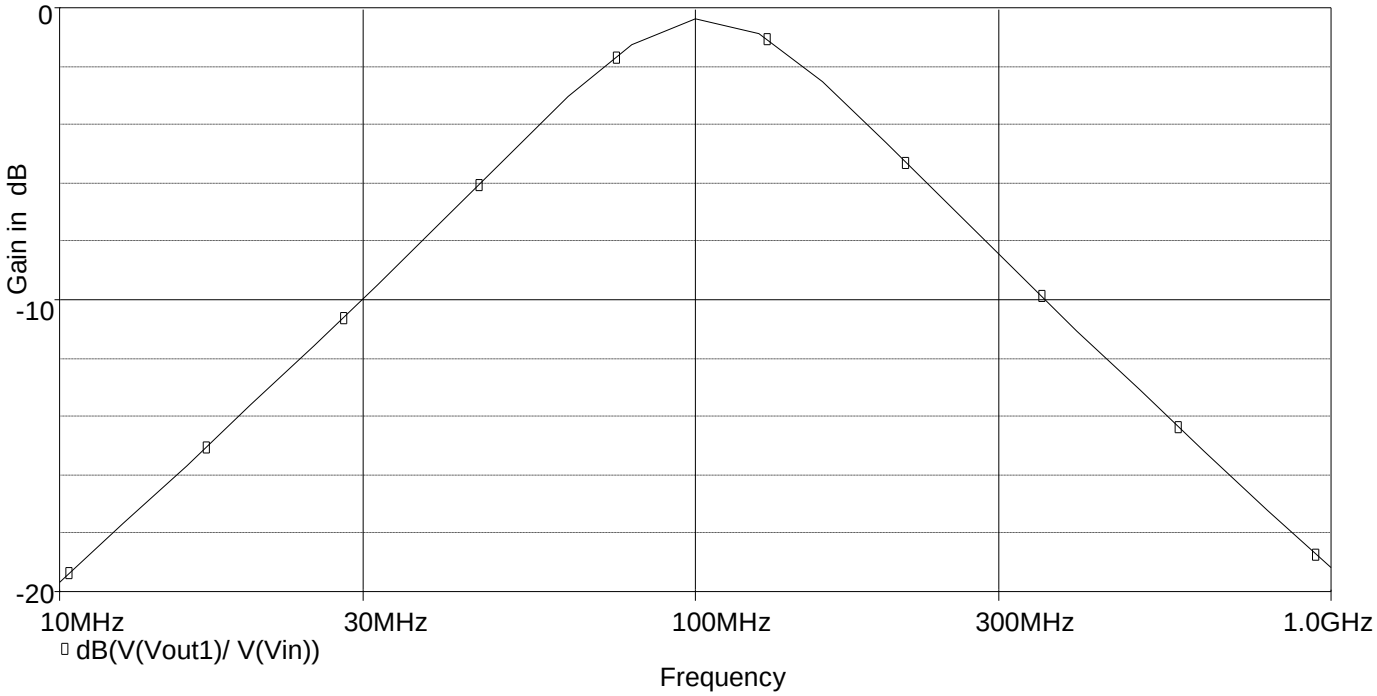

Figure 11 : Gain-Frequency response of Voltage mode Band Pass Signal.

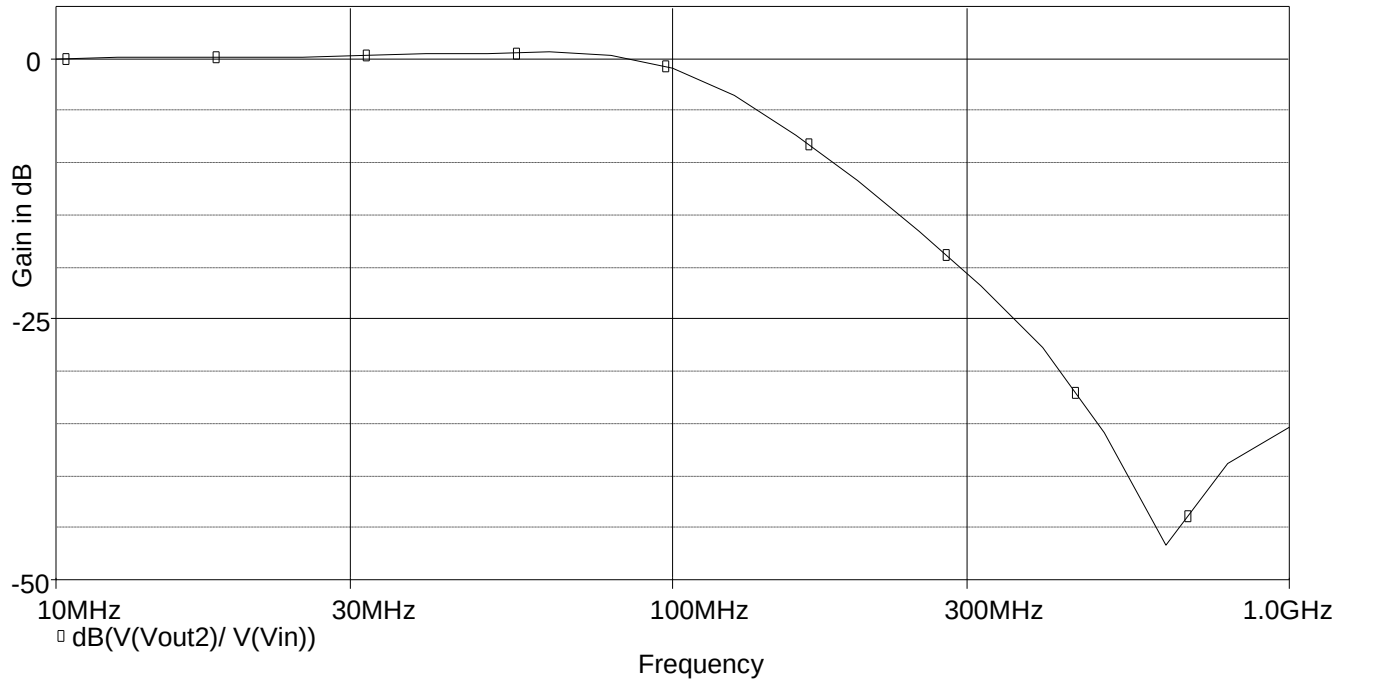

Figure 12 : Gain-Frequency response of Voltage mode Low Pass Signal

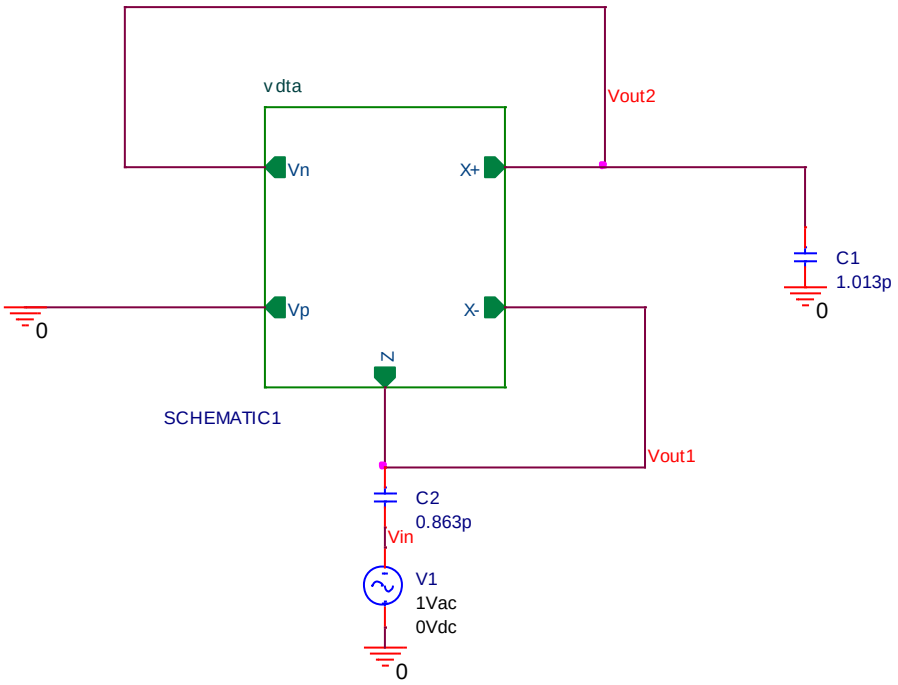

Figure 13 : PSPICE circuit diagram of Topology A ($V_1 = 0$ and $V_2 = V_{in}$).

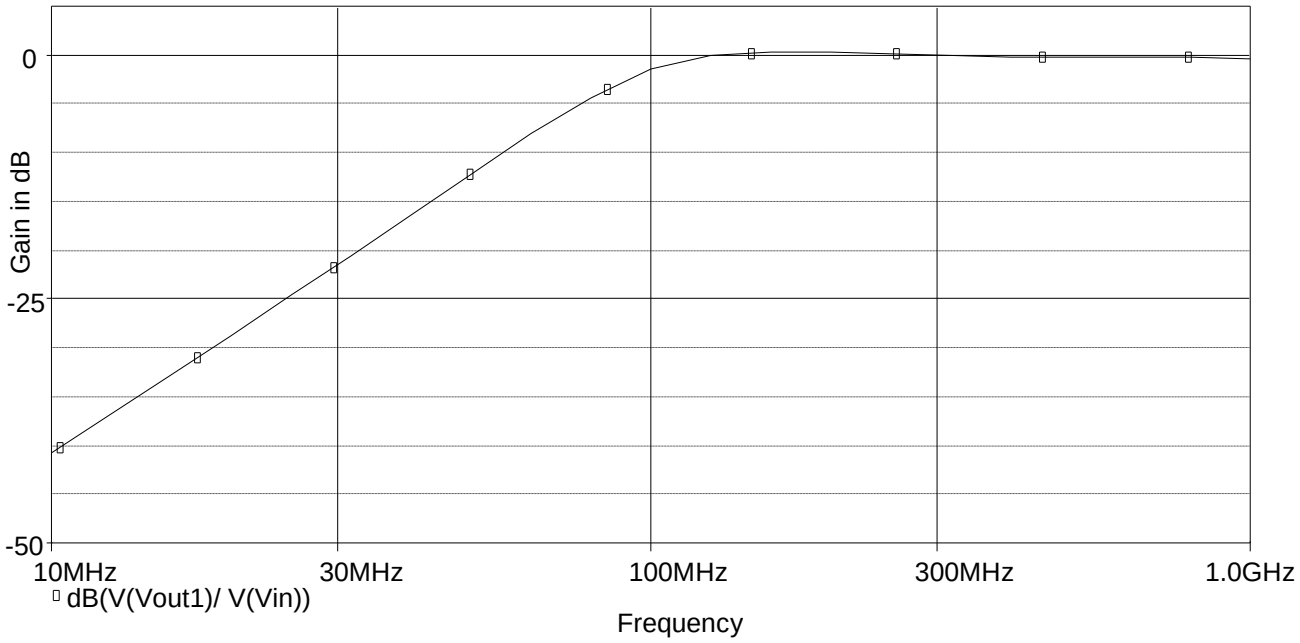

Figure 14 : Gain-Frequency response of Voltage mode High Pass Signal.

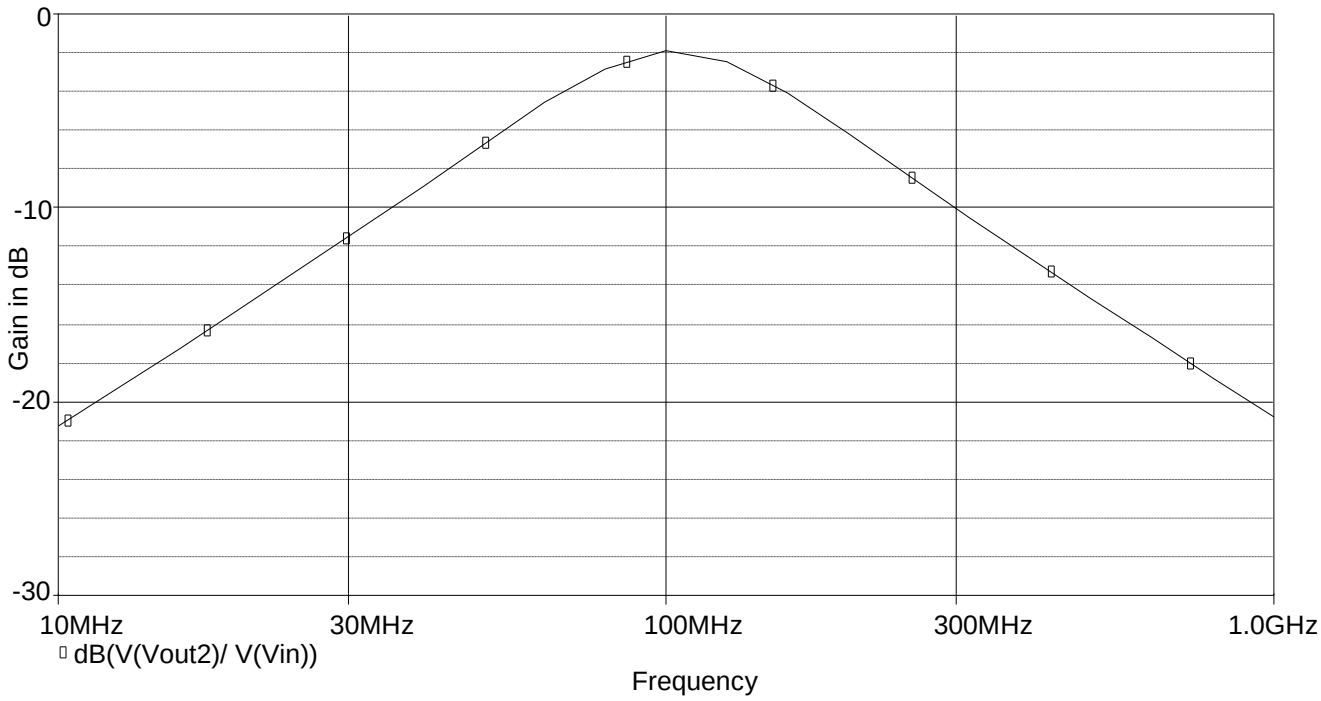

Figure 15 : Gain-Frequency response of Voltage mode Band Pass Signal.

4.2.2 TOPOLOGY B

The filter topology here named as Topology B was introduced in 2012[2]. This topology shows a current mode filter. It consists of one input node and three output nodes and at each node one filter output is available. This circuit is capable of implementing Low Pass, High Pass and Band Pass output. This circuit uses one VDTA block and two capacitors for its functioning. The circuit used to implement VDTA for this topology is shown in Figure 3. So here two opposite outputs for z in terms of z_c and z are made available as compared to the output z of circuit of VDTA as shown in Figure 2. The circuit used for this topology is shown in Figure 16. In Figure 16, I_{in} indicates the input current supplied by the source, I_{LP} indicates the Low Pass output of the filter, I_{BP} indicates the Band Pass output of the filter and I_{HP} indicates the High Pass output of the filter. After analysis is performed over the circuit in Figure 16, the equations of the output at different terminals obtained are as follows.

Low Pass Output → $$\mathrm{LP(s)} = \frac{I_{LP}(s)}{\mathrm{I}_{in}(s)} = \frac{(\frac{g_{mF}g_{mS}}{C_1C_2})}{D(s)} \quad (4.11)$$

High Pass Output → $$\mathrm{HP(s)} = \frac{I_{HP}(s)}{\mathrm{I}_{in}(s)} = \frac{s^2}{D(s)} \quad (4.12)$$

Band Pass Output → $$BP(s) = \frac{I_{BP}(s)}{I_{in}(s)} = \frac{\left(\frac{g_{mF}}{C_1}\right)s}{D(s)} \quad (4.13)$$

where, $$D(s) = s^2 + \left(\frac{g_{mF}}{C_1}\right)s + \left(\frac{g_{mF}\, g_{mS}}{C_1\, C_2}\right) \quad (4.14)$$

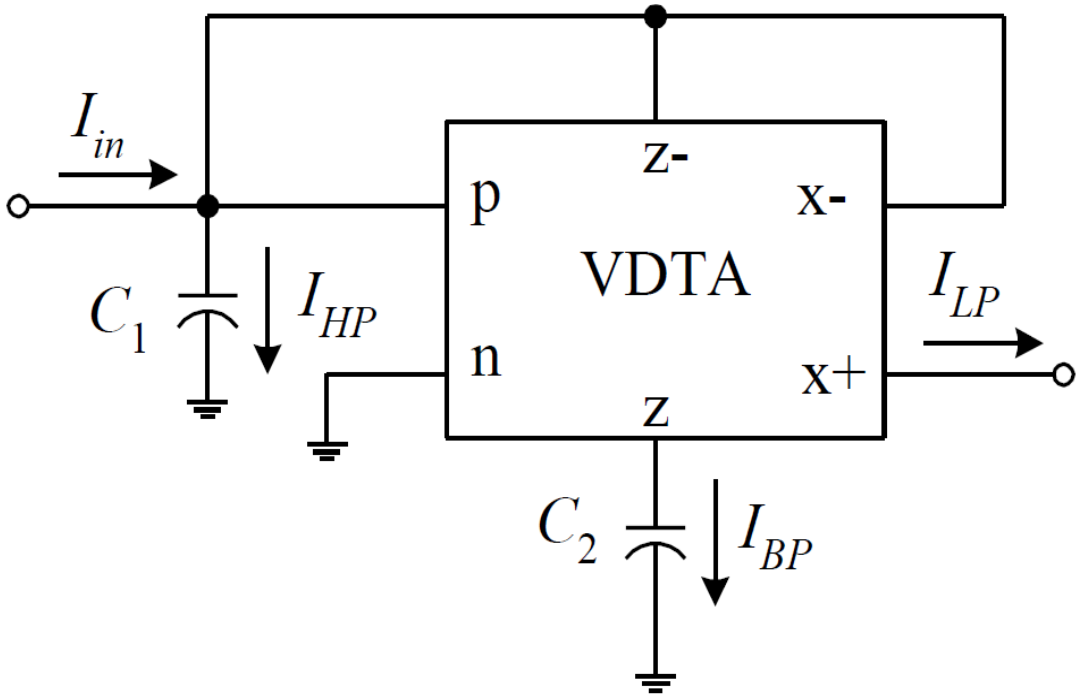

Figure 16 : Current mode Biquad Filter (Topology B)[2].

Equation 4.11 shows the ratio of the output at terminal I_{LP} and the input terminal I_{in} and since the numerator does not contain the term s, so it can easily be said that the output obtained at this terminal is Low Pass output. In a similar manner we can see that numerator in equation 4.12 contains the s^2 term included in itself, so it can be said that the output current at the terminal I_{HP} indicates the High pass output and the equation 4.13 contains only the s term in the numerator so again it can clearly be understood that the output at the terminal I_{BP} indicates the Band Pass output.

The natuaral frequency ω_0 for this topology [2] is given in equation 4.15 and the Bandwidth for this topology [2] is given in equation 4.16.

$$\omega_0 = \sqrt{\frac{g_{mF}\, g_{mS}}{C_1\, C_2}} \tag{4.15}$$

$$\text{BW} = \frac{g_{mF}}{C_1} \tag{4.16}$$

SIMULATION RESULTS:

For this simulation, CMOS implementation of VDTA given in Figure 3 is used. The simulation is done on PSPICE using 0.35µm TSMC CMOS process parameters. The aspect ratios for the PMOS and NMOS structures is given in Table 2. Supply voltages used for providing the biasing for the given circuit are +V = -V = 2 volts. The value of the capacitances indicated by C_1 and C_2 in Figure 16 are $C_1 = C_2 = 20$pF.

Transistors	W(µm)	L(µm)
M1-M2 , M5-M6	16.1	0.7
M3-M4 , M7-M8	28	0.7
M9-M12	21	0.7
M13-M16	7	0.7
M14-M15 , M17-M18	8.5	0.7

Table 2 : Aspect ratios of Transistors for VDTA structure of Figure 3 (0.35 µm) [2].

For this topology, the natural frequency of the filter for which simulations are done is selected to be $f_0 = 3.03$ MHz and the Quality factor is chosen to be Q=1. For achieving these values of natural frequency and Quality factor the two transconductance values of VDTA are selected to be $g_{mF} = g_{mS} = 381$µA/V [2]. For this purpose the biasing currents are taken to be $I_{BF} = I_{BS} \approx 40$µA [2].

The circuit used for the simulation in PSPICE software is given in Figure 17.

Figure 18 indicates the results of simulation which are obtained at the capacitor C_2 which is a Band Pass response. The lower cut off frequency obtained after simulation is equal to 1.849MHz and the higher cut off frequency is equal to 4.676 MHz. The Bandwidth of the filter is obtained to be 2.827 MHz.

Figure 19 indicates the results of simulation that are obtained at the capacitor C_1 which is a High Pass response. The cut off frequency of the filter is obtained to be 2.352 MHz.

Figure 20 indicates the results of simulation that are obtained at the terminal X+ which is a low pass response. The Bandwidth of the filter is obtained to be 3.677 MHz.

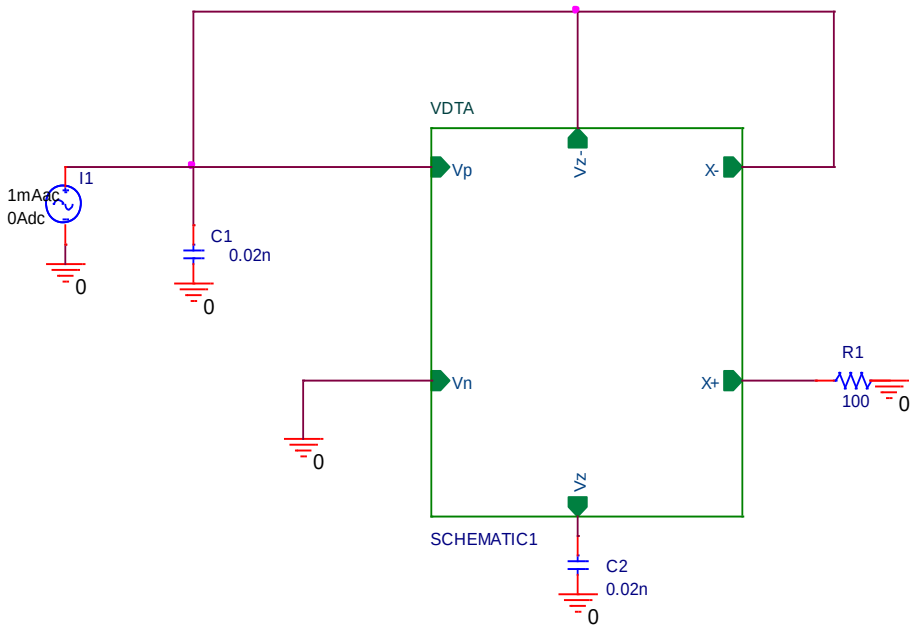

Figure 17 : PSPICE circuit diagram of Topology B

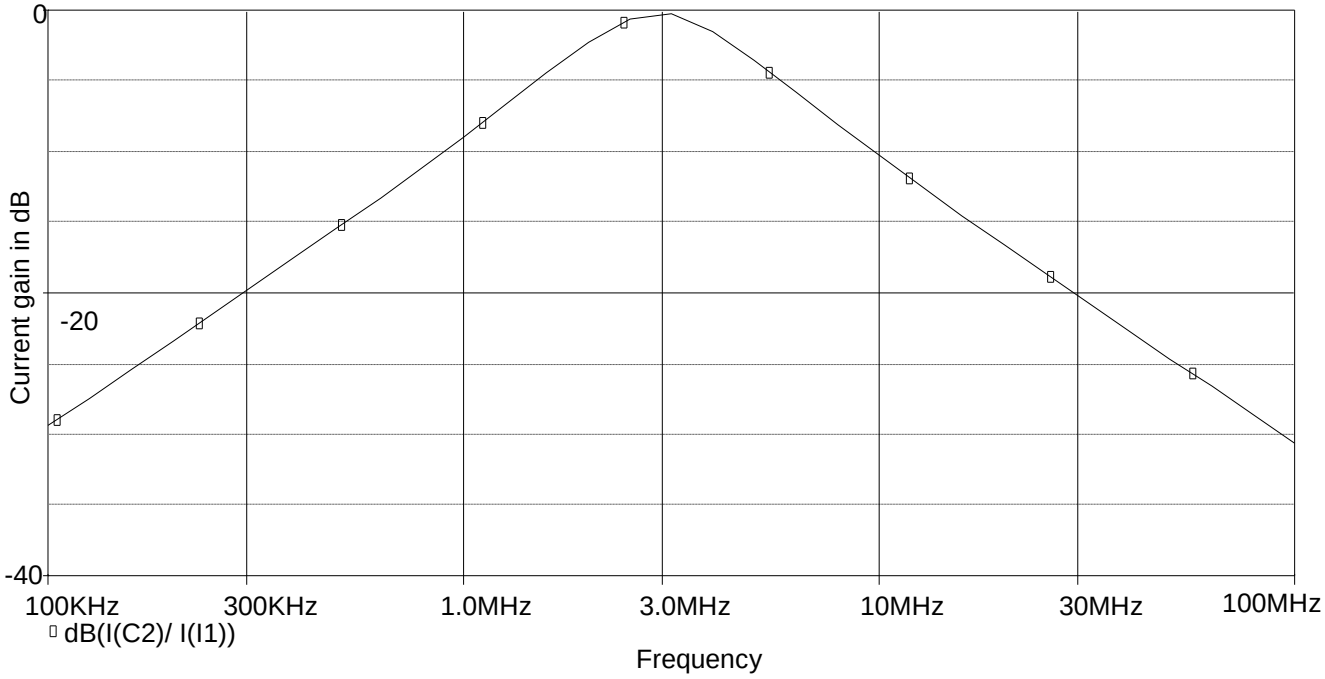

Figure 18 : Simulated Band Pass response for filter of Topology B

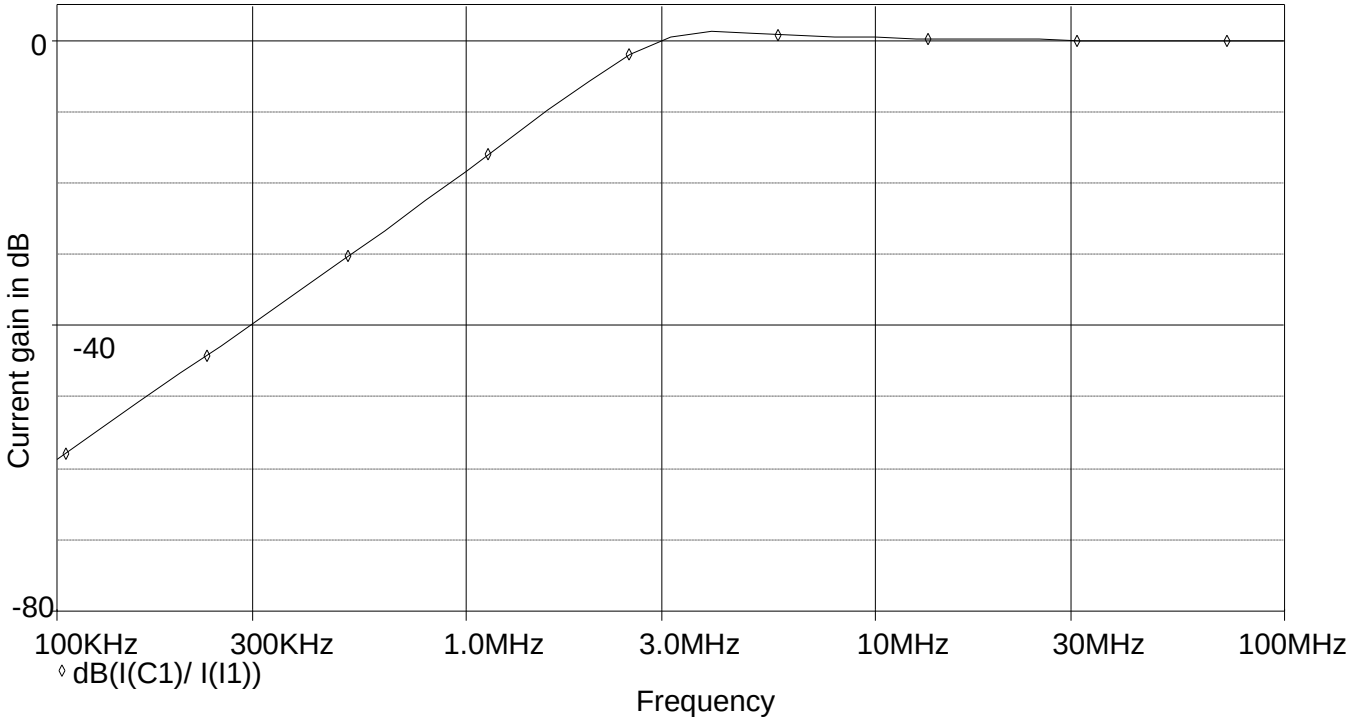

Figure 19 : Simulated High Pass Response for filter of Topology B

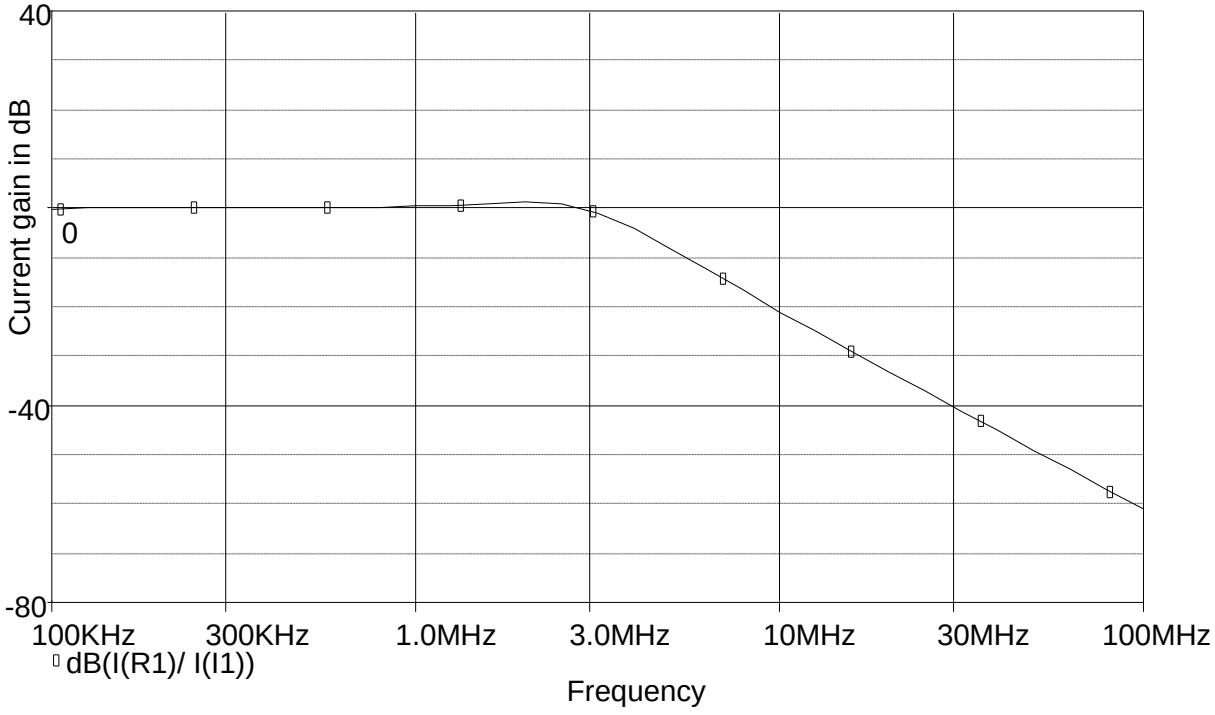

Figure 20 : Simulated Low Pass Response for filter of Topology B

4.2.3 TOPOLOGY C

The filter topology here named as Topology C was introduced in 2013 [3]. In this topology the filter shown is a current-mode filter. This filter has single input terminal and multiple output terminals. The filter uses a single VDTA, two capacitors which are grounded and a resistor which is also grounded. This circuit implements all the filter functions i.e Low Pass, High Pass, Band Pass, Notch and All Pass filter functions. So here we can see that as compared to previous filters this can implement all the filters implemented by previous two topologies and in addition to that it is implementing Band Stop and All Pass filter functions. Here in this filter the natural frequency and the Bandwidth are independently tunable. The CMOS implementation of VDTA that has been used by this topology is given in Figure 2 and the aspect ratios for the MOS transistors are clearly given in Table 1. The circuit used for this topology is given in Figure 21.

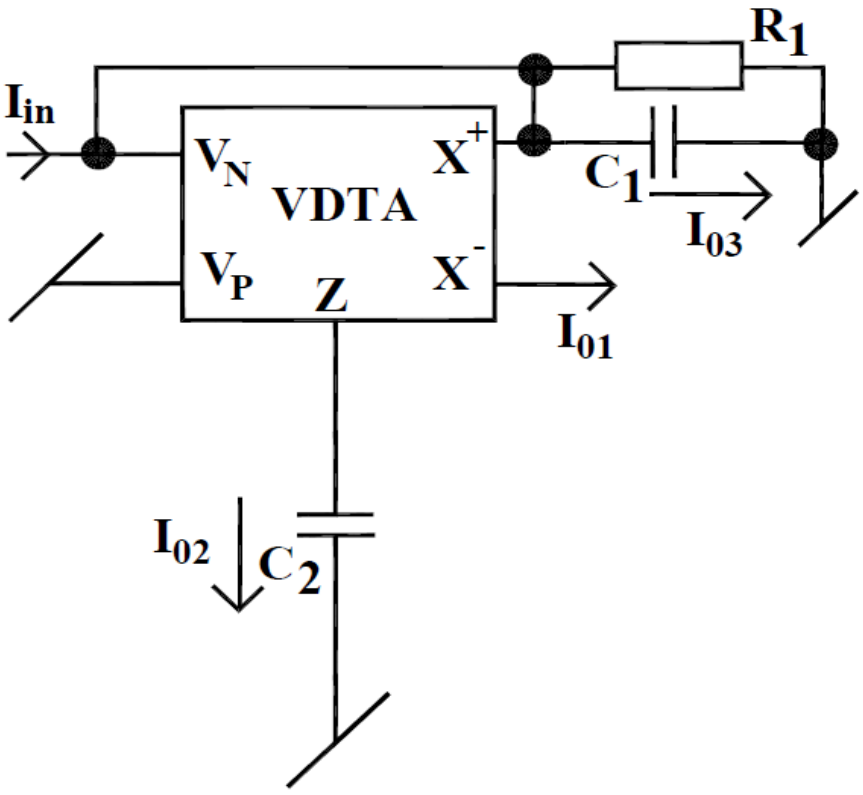

Figure 21 : Current Mode Biquad Filter (Topology C) [3]

Here I_{in} refers to the input current signal which as shown in Figure 21 is applied at V_N terminal. After the proper analysis of the circuit of Figure 21, the expression that is obtained at I_{01} terminal is given in equation 4.17. Equation 4.18 gives the expression for the current at

the terminal I_{02} and equation 4.19 gives the expression for the current at the terminal I_{03}. The equations that are obtained at different terminals are [3]

$$\frac{I_{01}}{I_{in}} = \frac{g_{m1}g_{m2}}{D(s)} \tag{4.17}$$

$$\frac{I_{02}}{I_{in}} = -\frac{s\left(\frac{g_{m1}}{C_1}\right)}{D(s)} \tag{4.18}$$

$$\frac{I_{03}}{I_{in}} = \frac{s^2}{D(s)} \tag{4.19}$$

The absence of the s term in the numerator of the equation 4.17 indicate that the signal obtained at the terminal indicated by I_{01} in Figure 21 is a Low Pass signal. In a similar way, upon seeing the presence of s term in the numerator of the equation 4.18 we can clearly state that signal represented by I_{02} in Figure 21 is a Band Pass signal. The presence of s^2 in the numerator of the equation 4.19 reveals that the signal indicated by I_{03} is a high pass signal. Now performing some operations on the equations 4.17, 4.18 and 4.19 we can obtain the equations 4.20 and 4.21. Out of these, equation 4.20 is a notch filter expression that is obtained after the addition of equations 4.17 and equation 4.19 whereas equation 4.21 is an All Pass filter expression and is obtained after the addition of all the three equations i.e equation 4.17 , 4.18 and 4.19. The expression of the function D(s) that is used in all the expressions here is given in 4.22.

$$\frac{I_{01}+I_{03}}{I_{in}} = \frac{s^2+\frac{g_{m1}g_{m2}}{C_1C_2}}{D(s)} \tag{4.20}$$

$$\frac{I_{01}+I_{02}+I_{03}}{I_{in}} = \frac{s^2-s\left(\frac{g_{m1}}{C_1}\right)+\frac{g_{m1}g_{m2}}{C_1C_2}}{D(s)} \tag{4.21}$$

Where

$$D(s) = s^2 + \left(\frac{1}{R_1C_1}\right)s + \left(\frac{g_{m1}\,g_{m2}}{C_1\,C_2}\right) \tag{4.22}$$

The expression for the natural frequency (ω_0) of this topology [3] is given in equation 4.23, the expression for Bandwidth (BW) [3] is given in equation 4.24 and the expression for the Quality factor (Q_0) [3] is given in equation 4.25.

$$\omega_0 = \sqrt{\frac{g_{m1}\, g_{m2}}{C_1\, C_2}} \tag{4.23}$$

$$\text{BW} = \frac{1}{R_1 C_1} \tag{4.24}$$

$$Q_0 = \sqrt{\frac{g_{m1}\, g_{m2} C_1 {R_1}^2}{C_2}} \tag{4.25}$$

SIMULATION RESULTS:

For this simulation, CMOS implementation of VDTA given in Figure 2 is used. The simulation is done on PSPICE using 0.18µm TSMC CMOS process parameters. The aspect ratios for the PMOS and NMOS structures is given in Table 1. Supply voltages used for providing the biasing for the given circuit are $+V_{DD} = -V_{SS} = 1$ volts. The value of the biasing currents used are $I_{B1} = I_{B2} = 150\mu A$ and $I_{B3} = I_{B4} = 42.38\ \mu A$ [3]. The values of the passive elements are chosen to be $C_1 = C_2 = 0.01$ nF and $R_1 = 1.58K\Omega$ [3].

The circuit used for the simulation in PSPICE software is given in Figure 22.

Figure 23 indicates the results of simulation which are obtained at the X- terminal which is a Low Pass response. The cut off frequency of the filter is obtained to be MHz.

Figure 24 indicates the results of simulation that are obtained at the terminals of capacitor C_2 which is a Band Pass response. The lower cut off frequency obtained after simulation is equal to 1.849MHz and the higher cut off frequency is equal to 4.676 MHz. The Bandwidth of the filter is obtained to be 2.827 MHz.

Figure 25 indicates the results of simulation that are obtained at the terminals of capacitor C_1 which is a High Pass response. The cut off of the filter is obtained to be 3.677 MHz.

Figure 26 indicates the results of simulation for the Notch response of the above filter in accordance with equation 4.20.

Figure 27 indicates the results of simulation for the All Pass response of the above filter in accordance with equation 4.21.

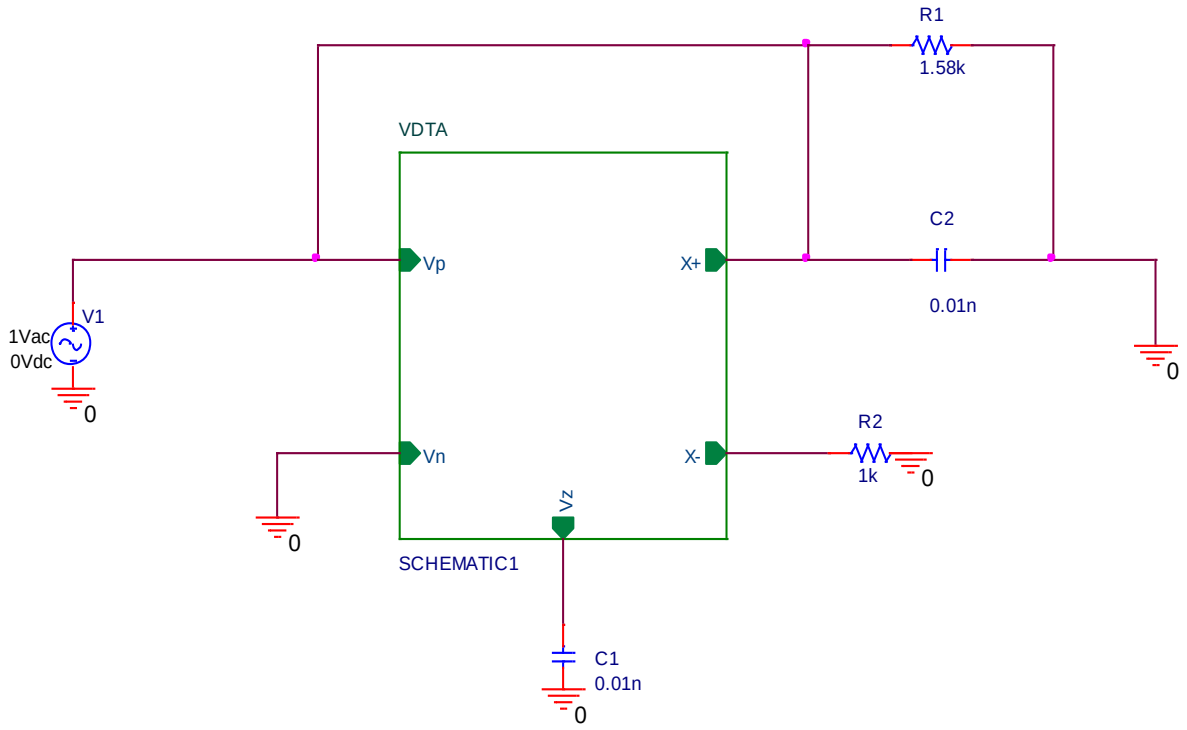

Figure 22 : PSPICE circuit diagram of Topology C

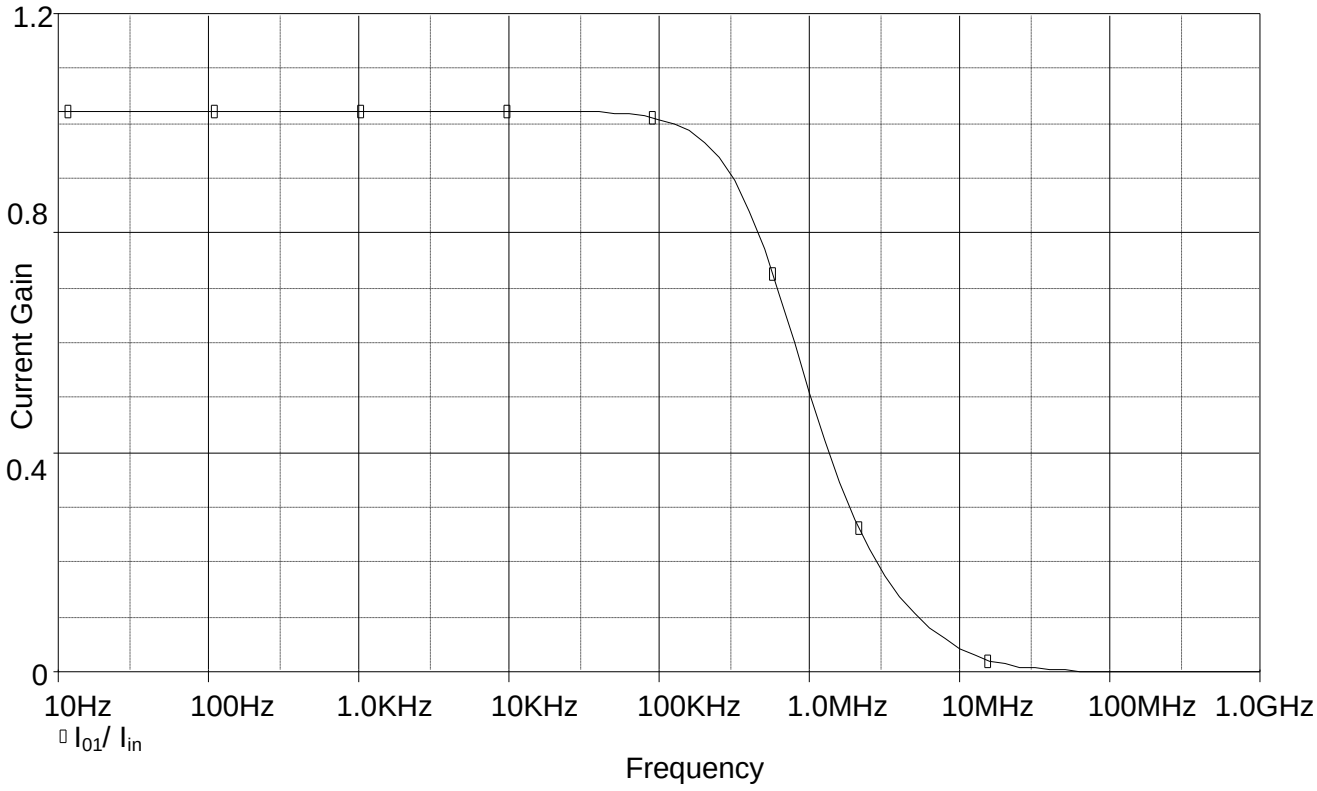

Figure 23 : Simulated Low Pass response of filter of Topology C

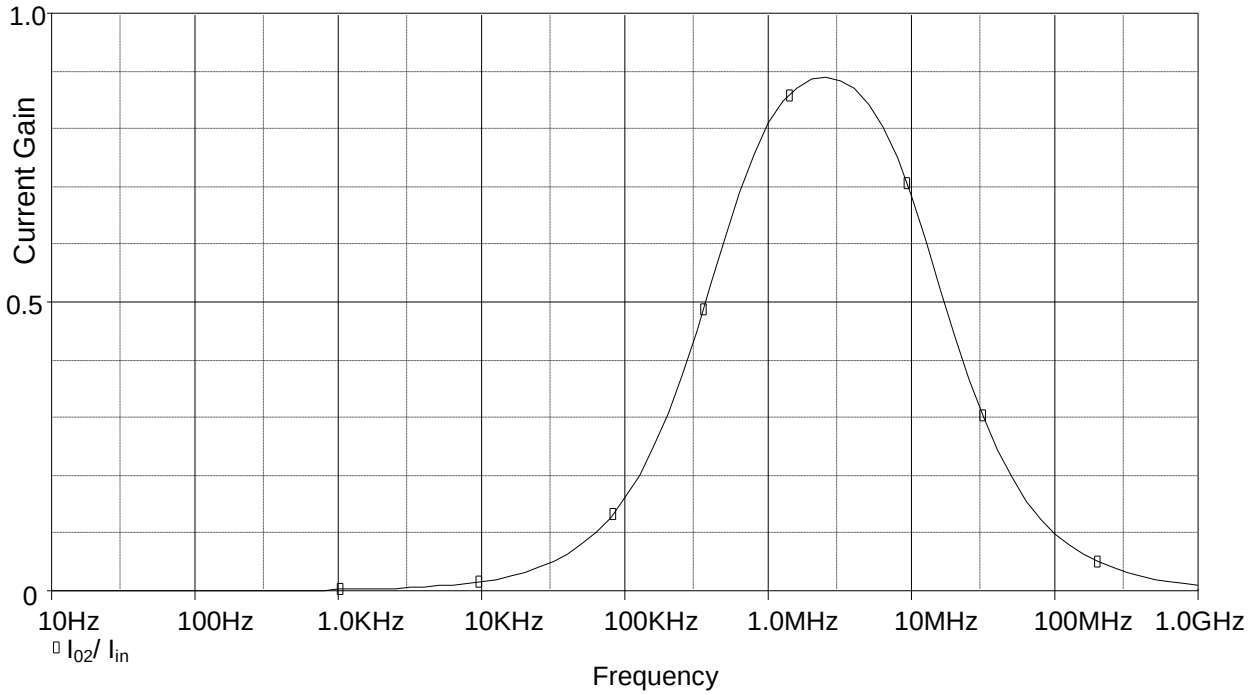

Figure 24 : Simulated Band Pass response of filter of Topology C

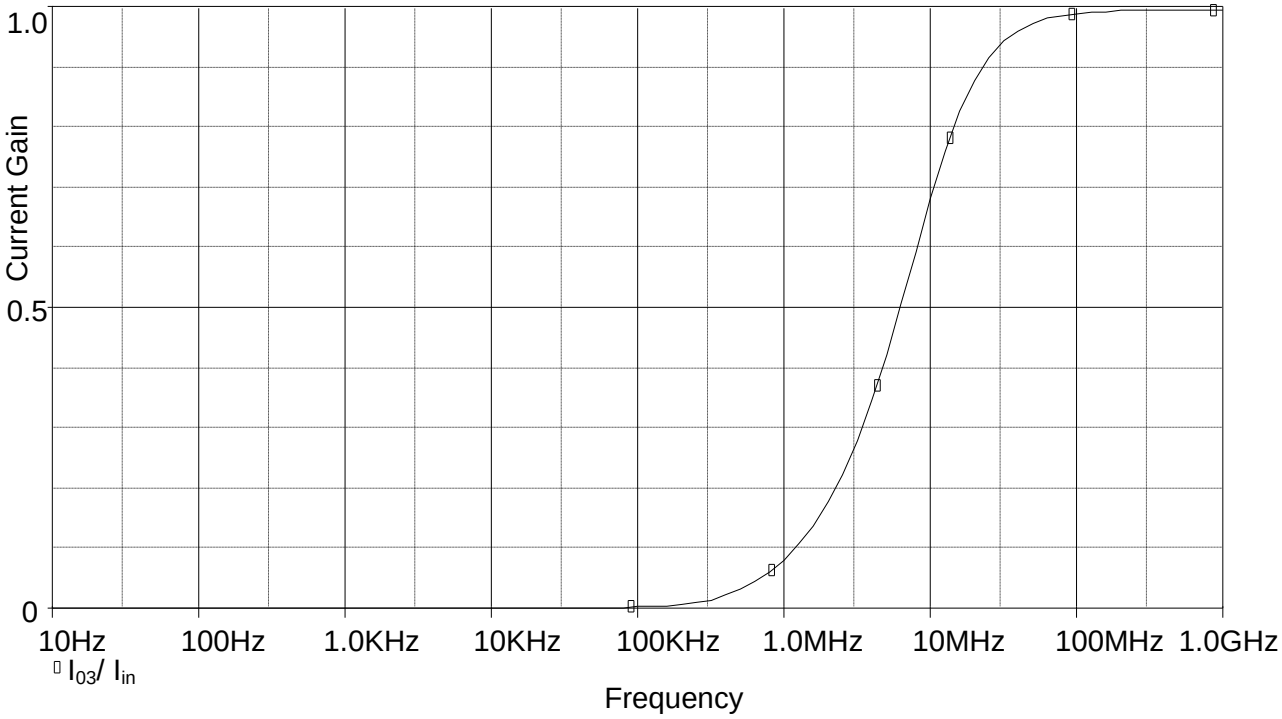

Figure 25 : Simulated High Pass response of Topology C

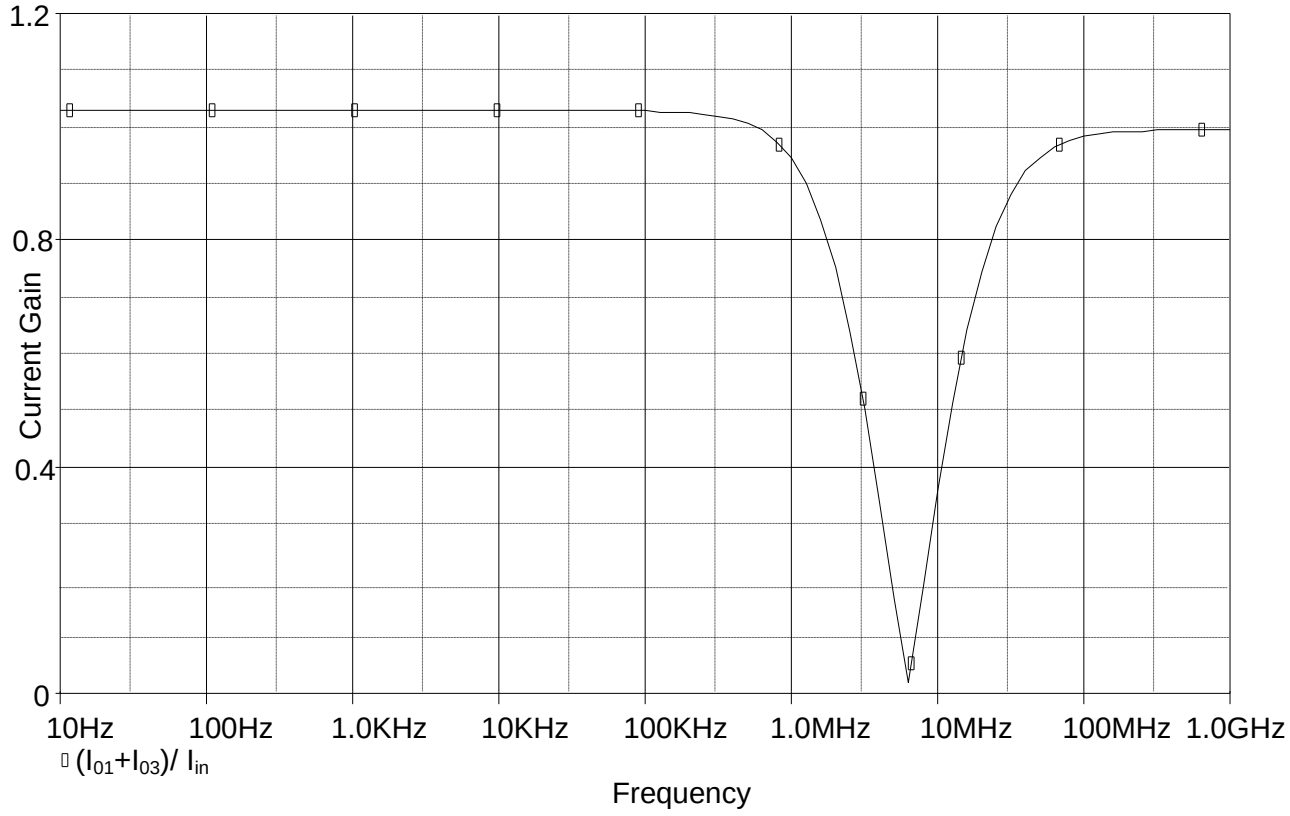

Figure 26 : Simulated Notch response of filter of Topology C

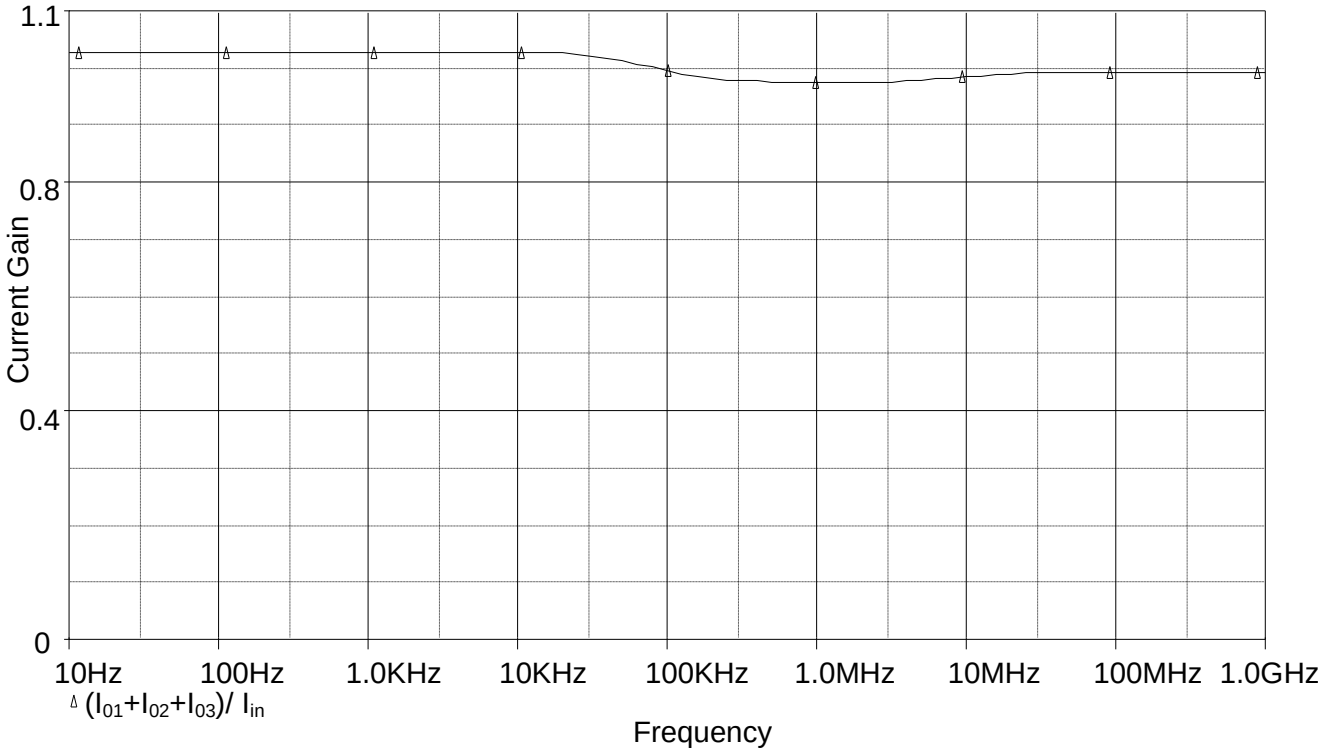

Figure 27 : Simulated All Pass magnitude response of filter of Topology C

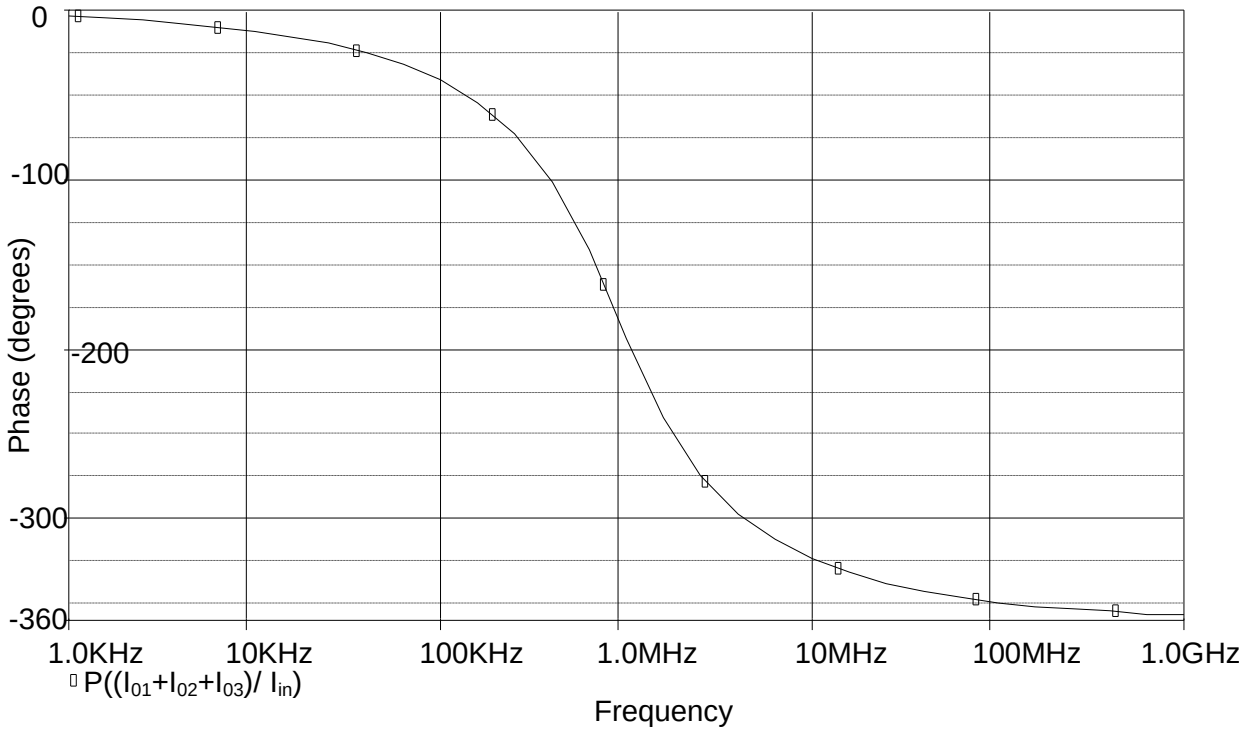

Figure 28 : Simulated All Pass phase response of filter of Topology C

4.2.4 TOPOLOGY D

The filter topology here named as Topology D was introduced in 2013 [4]. This topology here shows a filter that works in current mode but the working of this topology is quite different from the previous one. Here only one output terminal is present but there is a presence of three input terminals along with it. So the output that we get depends on the terminal on which input is applied. This topology is capable of implementing all the filters i.e Low Pass, Band Pass, High Pass, Band Stop and All Pass filters. This filter uses two VDTA's and two capacitors which are grounded. The CMOS implementation of VDTA that is used here is given in Figure 3 and the aspect ratios of both the NMOS and PMOS transistors that are used here are given in Table 2. The circuit used for this topology is given in Figure 29. Here we can see that there is no need of any external passive resistor which is one of the benefits of this topology. This filter is capable of giving an independent control to both the angular frequency (ω_0) and the Quality factor (Q). This control is provided through the transconductances of VDTA's.

In the Figure 29, the terminals represented by I_1, I_2 and I_3 are the input terminals and the terminal represented by I_{out} is the only output terminal. The filter that is implemented on the output terminal is dependent on the input terminal at which input is being applied.

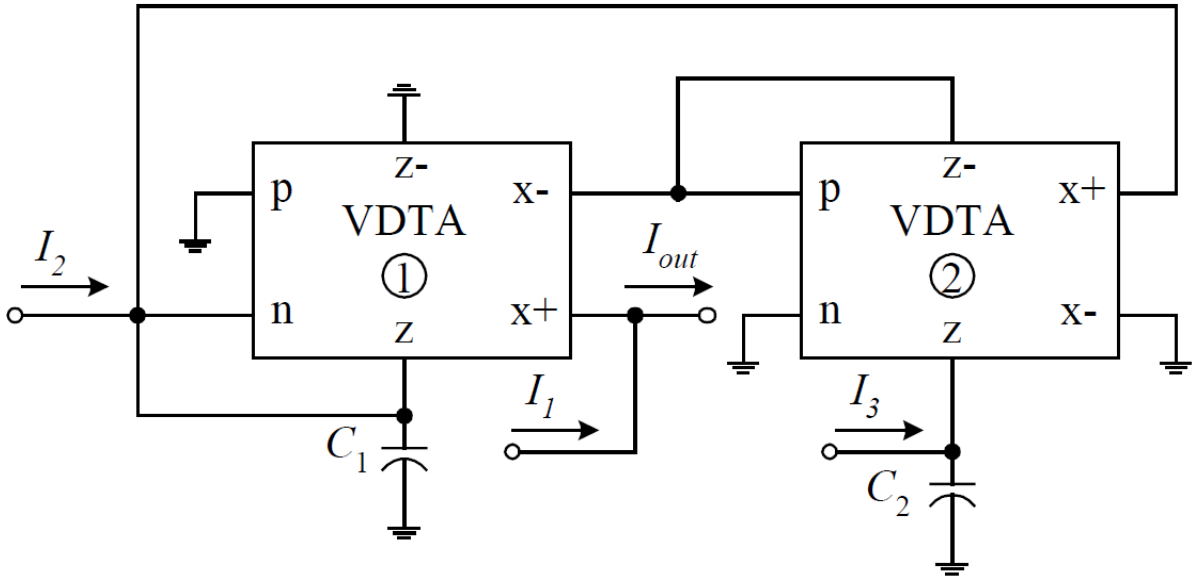

Figure 29 : Current Mode Universal Filter (Topology D) [4]

Upon the analysis of the above circuit, the representation in s - domain [4] can be done as

$$I_{out} = \frac{D(s)I_1 + \left(\frac{g_{mS1}}{C_1}\right)sI_2 + \left(\frac{g_{mS1}g_{mS2}}{C_1C_2}\right)I_3}{D(s)} \tag{4.26}$$

Where $$D(s) = s^2 + \left(\frac{g_{mF1}}{C_1}\right)s + \left(\frac{g_{mS1}g_{mS2}}{C_1C_2}\right) \tag{4.27}$$

So using above equation transfer function of any filter can be realised, so as to realise all the filters there are five different conditions [4] for the application of the input signal at the input terminals where each condition is going to realize a different function at the output terminal and are obtained using the equation 4.26.

1. If the current signal is being applied to the I_3 input terminal and the rest two terminals are devoid of any input signal i.e $I_3 = I_{in}$ and $I_1 = I_2 = 0$, then the response obtained at I_{out} is Low Pass and the gain obtained in the Pass Band is unity.
2. If the input current signal is supplied to the I_2 terminal and the rest two terminals are devoid of any input signal i.e $I_2 = I_{in}$ and $I_1 = I_3 = 0$, then the response obtained at I_{out} is Band Pass and the gain obtained in Pass Band is g_{mS1}/g_{mF1} where g_{mS1} and g_{mF1} are g_{mS} and g_{mF} of the first VDTA, where g_{mF} and g_{mS} are given as

$$g_{mF} = \frac{g_1g_2}{g_1+g_2} + \frac{g_3\,g_4}{g_3+g_4} \cong (g_{1,2} + g_{3,4})/2 \tag{4.28}$$

$$g_{mS} = \frac{g_5 g_6}{g_5 + g_6} + \frac{g_7 g_8}{g_7 + g_8} \cong (g_{5,6} + g_{7,8})/2 \quad (4.29)$$

Where g_i is the transconductance value of the i^{th} transistor of Figure 3.

3. If the input terminal is supplied at I_1 and the opposite of that signal is supplied at I_2 and I_3 terminal i.e $I_1 = -I_2 = -I_3 = I_{in}$ and $g_{mF1} = g_{mS1}$, the response obtained at I_{out} is High Pass and the gain obtained in the Pass Band is unity.
4. If I_1 is supplied with the current input signal and I_2 is supplied with the exact opposite of this signal i.e $I_1 = -I_2 = I_{in}$ and also $g_{mF1} = g_{mS1}$. Here I_3 is not supplied with any input i.e $I_3 = 0$, the response obtained at I_{out} is a Band Stop response and the gain obtained in the Pass Band is unity.
5. If the input is supplied at I_1 and I_2 is supplied with double of the input inverted at the terminal I_1 i.e $I_1 = -I_2/2 = I_{in}$, no input is given at I_3 i.e $I_3 = 0$ and $g_{mF1} = g_{mS1}$. Here the response obtained at I_{out} is an All Pass Response and the pass band gain is obtained to be unity.

For all of the above conditions, g_{mF1} and g_{mS1} are defined in equations 4.28 and 4.29.

The equations for the Quality factor and Angular frequency [4] are given as

$$Q = \frac{1}{g_{mF1}} \sqrt{\frac{g_{mS1} g_{mS2} C_1}{C_2}} \quad (4.30)$$

$$\omega_0 = \sqrt{\frac{g_{mS1} g_{mS2}}{C_1 C_2}} \quad (4.31)$$

Now for the sake of simplicity, if we go on to substitute $g_{mS1} = g_{mS2} = g_{m2}$ and $C_1 = C_2 = C$ in equations 4.30 and 4.31, the equations that we obtain[4] are

$$Q = \frac{g_{m2}}{g_{mF1}} \quad (4.32)$$

$$\omega_0 = \frac{g_{m2}}{C} \quad (4.33)$$

SIMULATION RESULTS:

For this simulation, CMOS implementation of VDTA given in Figure 3 is used. The simulation is done on PSPICE using 0.35µm TSMC CMOS process parameters. The aspect

ratios for the PMOS and NMOS transistor are given in Table 2. Supply voltages used for providing the biasing for the given circuit are $+V_{DD} = -V_{SS} = 2$ volts. The values of the passive elements are chosen to be $C_1 = C_2 = 20$ pF [4]. The natural frequency of the filter is chosen to be 3.03 MHz and Quality factor is chosen to be 1 [4]. For achieving these values the transconductance values are chosen [4] to be $g_{mF1} = g_{mS1} = g_{mF2} = g_{mS1} = 381\mu A/V$. For achieving these values the biasing currents are chosen [4] to be $I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 40\mu A$.

The circuit used for the simulation in PSPICE software is given in Figure 30. However this circuit is used only for case 1 indicated above and for the rest of the cases the changes on the three terminals is done as written above in those five points.

Figure 31 indicates the results of simulation which are obtained at the I_{out} terminal following the input conditions given in point no 1 and it is a Low Pass response. The cut off frequency of the filter is obtained to be 3.7488 MHz.

Figure 32 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 2 and it is a Band Pass response. The lower cut off frequency obtained after simulation is equal to 1.8596 MHz and the higher cut off frequency is equal to 4.872 MHz. The Bandwidth of the filter is obtained to be 3.0124 MHz.

Figure 33 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 3 and it is a High Pass response. The cut off of the filter is obtained to be 2.368 MHz.

Figure 34 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 4 and it is a Band Stop response. Frequency at the notch is obtained to be 3.157 MHz. The first 3-dB point is obtained at 1.798 MHz, the second 3-dB point is obtained at 4.934 MHz and the Bandwidth of the stop band is 3.136 MHz.

Figure 35 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 3 and it is a All Pass response. This figure indicates both the phase and magnitude response of All Pass filter in the same graph.

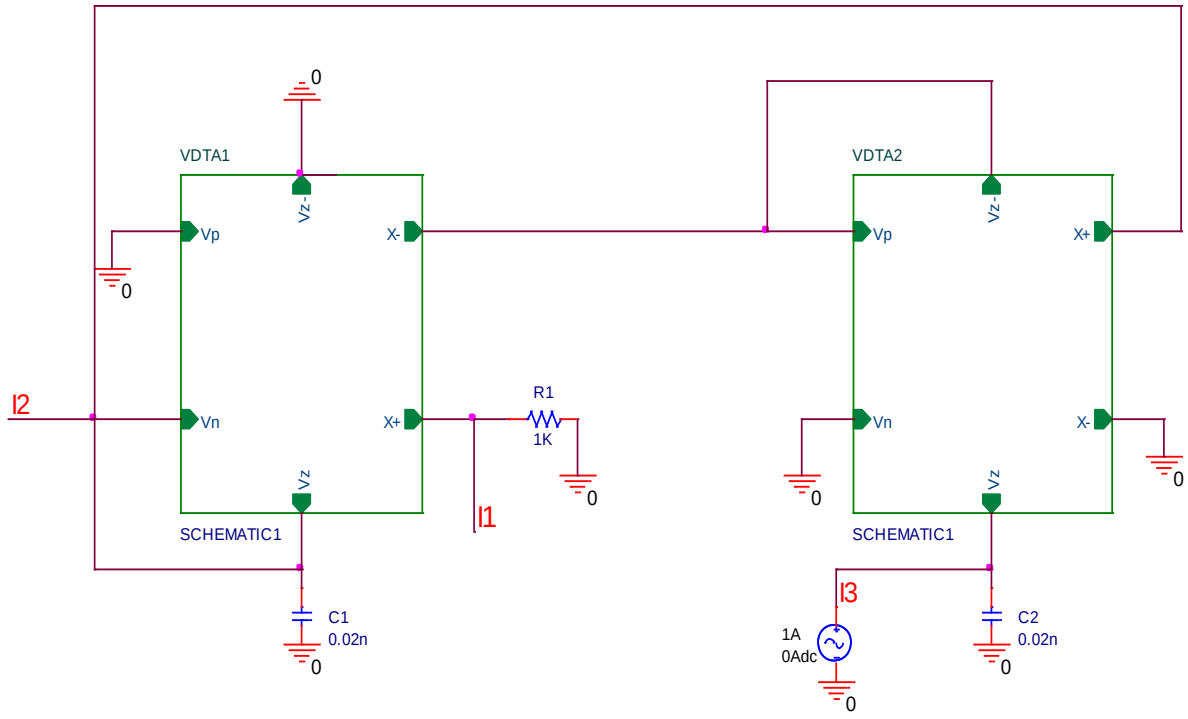

Figure 30 : PSPICE circuit diagram of Topology D (case 1)

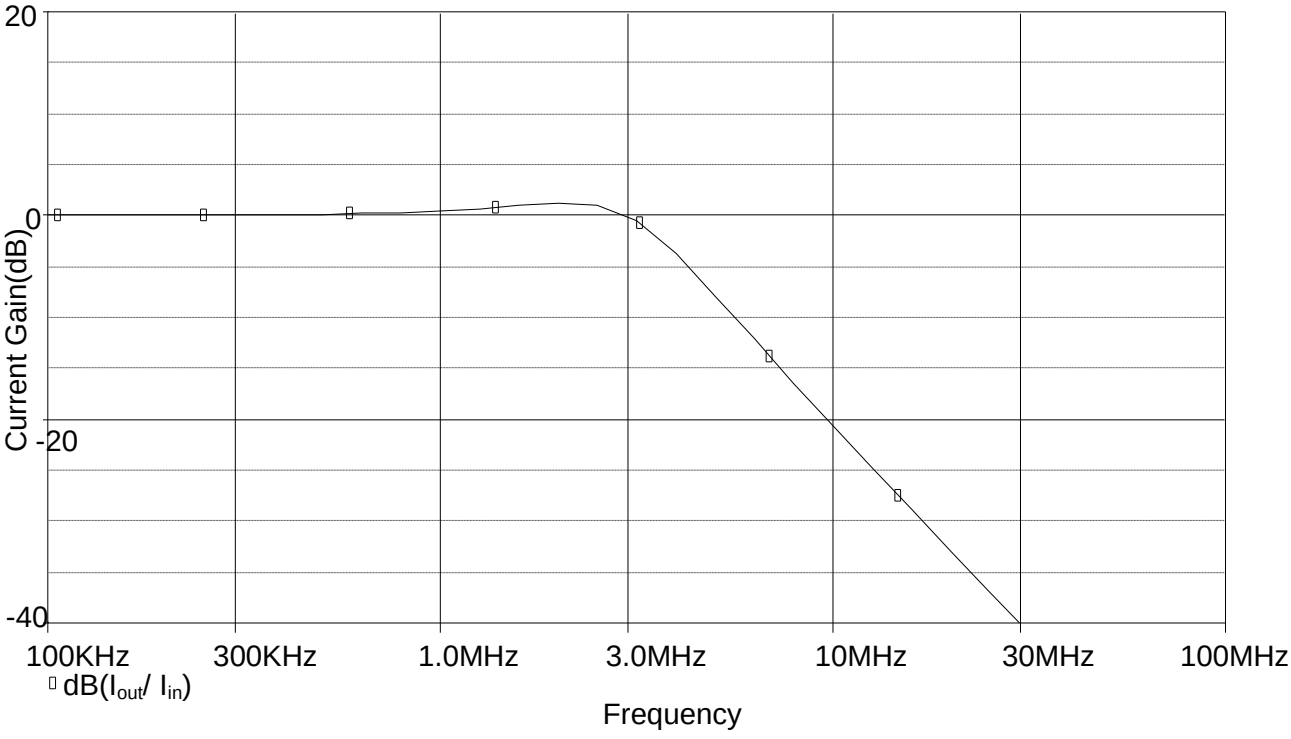

Figure 31 : Simulated Low Pass response of Topology D

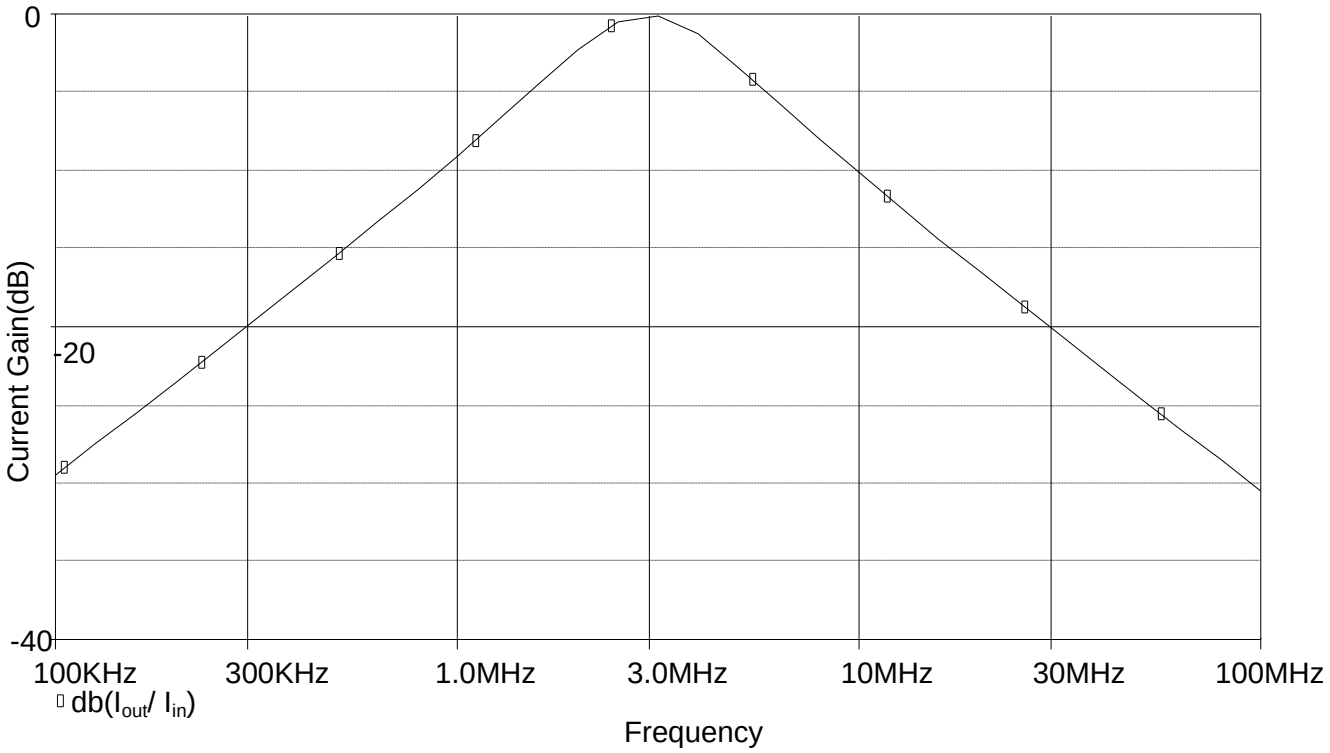

Figure 32 : Simulated Band Pass response of Topology D

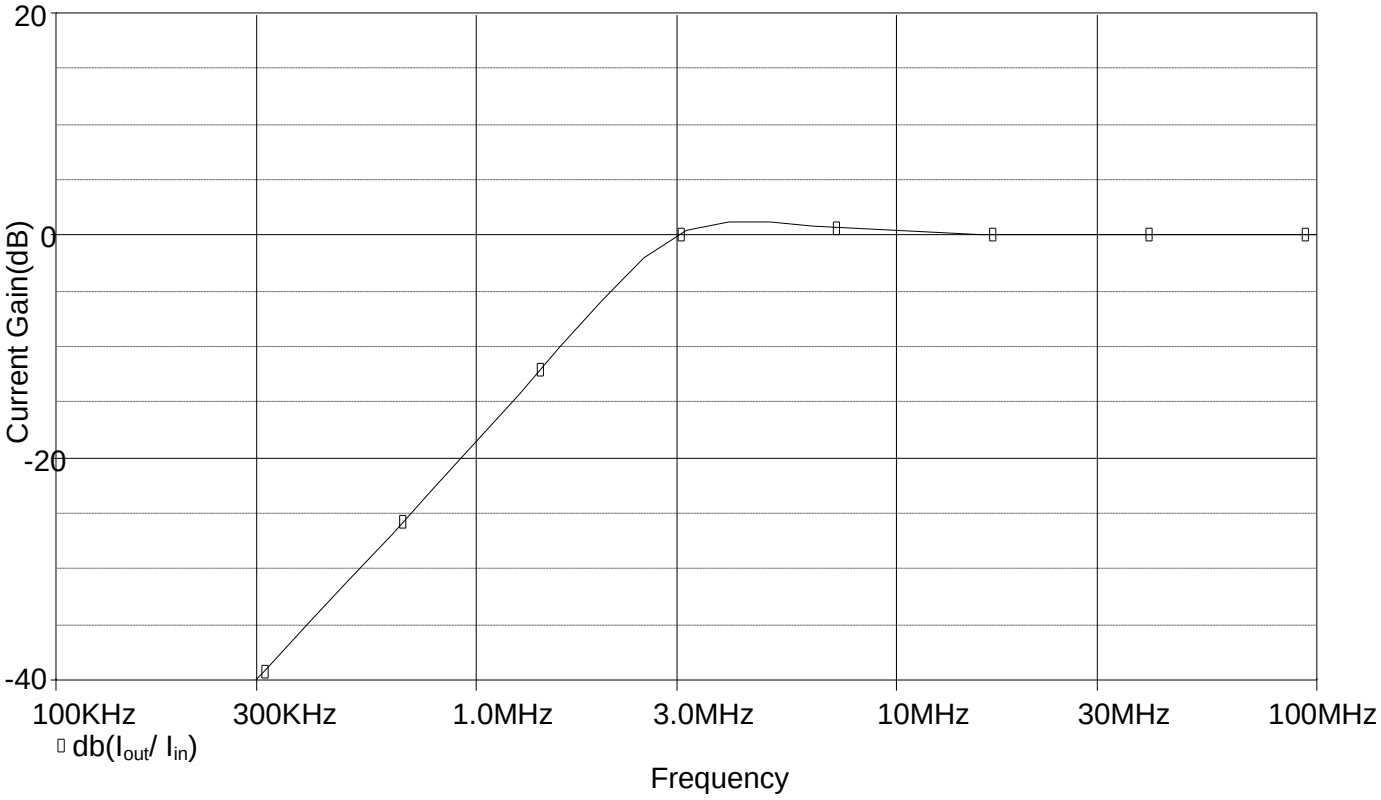

Figure 33 : Simulated High Pass response of Topology D

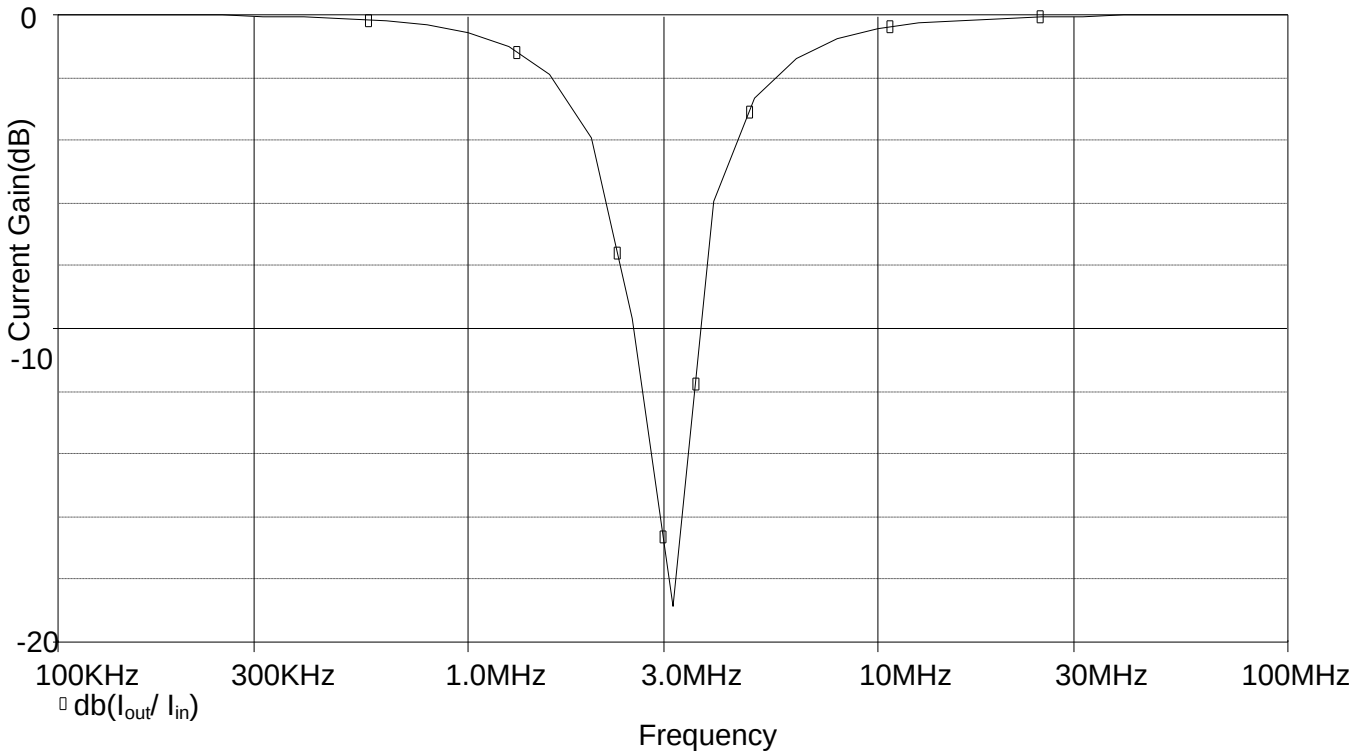

Figure 34 : Simulated Band Stop response of Topology D

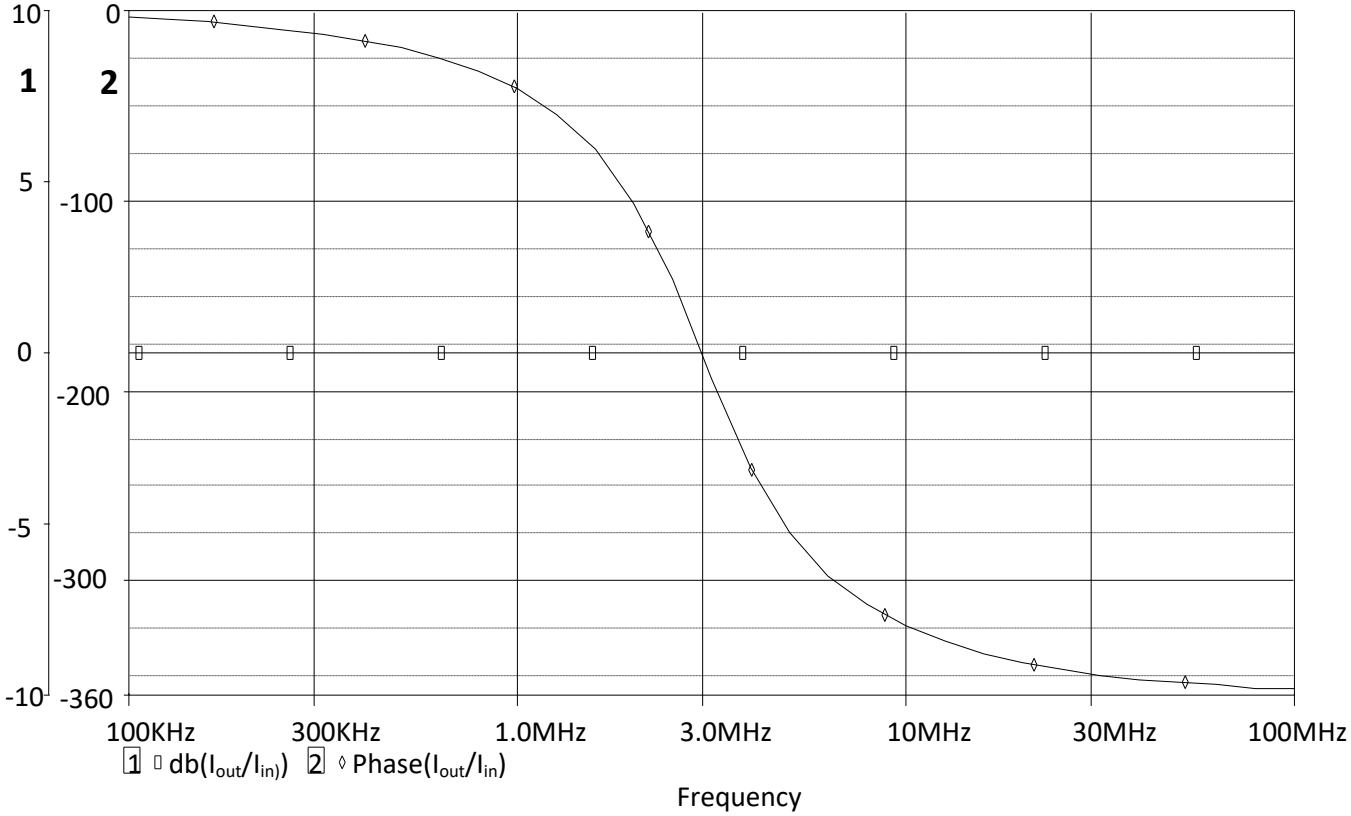

Figure 35 : Simulated All Pass response of Topology D

4.2.5 TOPOLOGY E

The filter topology here named as Topology E was introduced in 2012 [5]. This topology here shows a filter that works in voltage mode but the working of this topology is almost same as the previous one, only difference is that the previous topology is a current mode circuit. The filter here implemented is a Voltage Mode universal Biquad filter. Here also only one output terminal is present but there is a presence of three input terminals along with it. So the output that we get depends on the terminal on which input is applied. This topology is capable of implementing all the filters i.e Low Pass, Band Pass, High Pass, Band Stop and All Pass filters. This filter uses two VDTA's and two capacitors which are grounded. The CMOS implementation of VDTA that is used here is given in Figure 3 and the aspect ratios of both the NMOS and PMOS transistors that are used here are given in Table 2. The circuit used for this topology is given in Figure 36. Here we can see that there is no need of any external passive resistor which is one of the benefits of this topology. The angular frequency and the Bandwidth of the filter implemented in this topology can be independently tuned electronically.

In the Figure 36, the terminals represented by V_1, V_2 and V_3 are the input terminals and the terminal represented by V_{out} is the only output terminal. The filter that is implemented on the output terminal is dependent on the input terminal at which input is being applied.

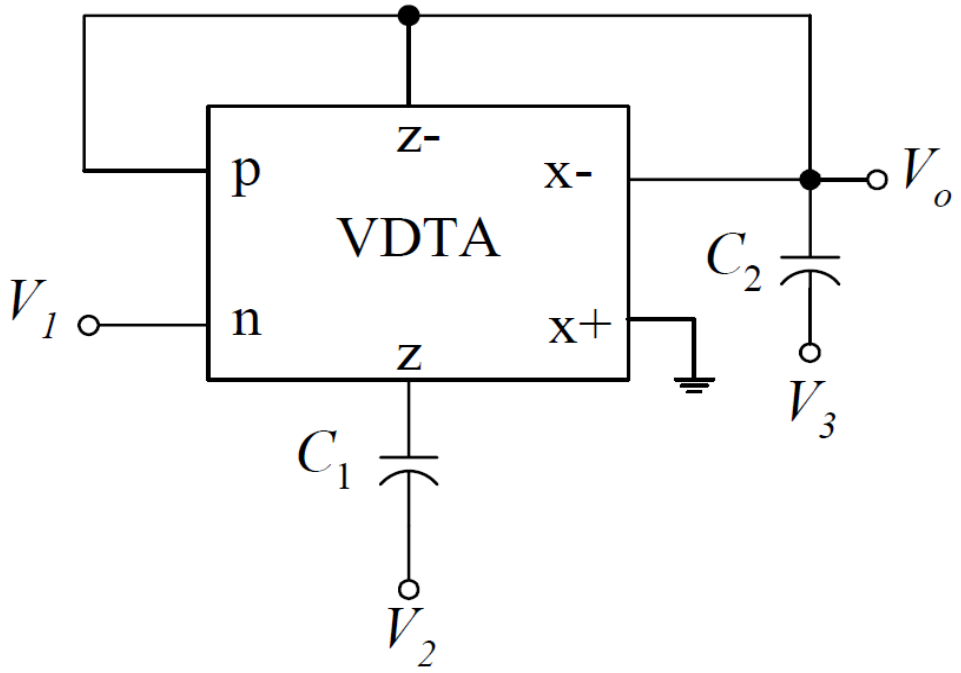

Figure 36 : Voltage Mode Universal Biquad filter (Topology E) [5]

Upon the analysis of the above circuit, the representation in s - domain [5] can be done as

$$V_{out} = \frac{s^2 V_3 - \left(\frac{g_{mS}}{C_2}\right) s V_2 + \left(\left(\frac{g_{mF}}{C_2}\right) s + \frac{g_{mS} g_{mF}}{C_1 C_2}\right) I_3}{D(s)} \tag{4.34}$$

Where $$D(s) = s^2 + \left(\frac{g_{mF}}{C_1}\right) s + \left(\frac{g_{mS} g_{mF}}{C_1 C_2}\right) \tag{4.35}$$

So using above equation transfer function of any filter can be realised, so as to realise all the filters there are five different conditions [5] for the application of the input signal at the input terminals where each condition is going to realize a different function at the output terminal and are obtained using the equation 4.34.

1. If the voltage signal is being applied at both the input terminals V_1 and V_2 i.e $V_1 = V_2 = V_{in}$ and no signal is applied at the terminal V_3 or in other words V_3 is grounded i.e V_3=0 and also both the transconductances are equal i.e g_{mF}=g_{mS} then the output obtained at V_{out} is a low pass response.
2. If the input is applied at the V_2 terminal i.e $V_2 = V_{in}$ and V_1 and V_3 both the terminals are grounded i.e $V_1 = V_3 = 0$, then the response obtained at the V_{out} terminal is a Band Pass response.
3. If the input is applied only at the V_3 terminal and both the V_1 and V_2 terminal are grounded i.e $V_1 = V_2 = 0$, then the response obtained at the V_{out} terminal is a High Pass response.
4. If the input is applied at all the three input terminals i.e $V_1 = V_2 = V_3 =$ Vin and also both the transconductances are equal i.e g_{mF}=g_{mS} then the output obtained at V_{out} is a Band Stop response.
5. If the voltage signal is being applied at both the input terminals V_1 and V_3 and half of the inputu voltage is applied at the V_3 terminal i.e $V_1 = 2V_2 = V_3 = V_{in}$ and also both the transconductances are equal i.e g_{mF}=g_{mS} then the output obtained at V_{out} is a All Pass response.

   For all of the above conditions, g_{mF} and g_{mS} are defined in equations 4.28 and 4.29.

The equations for the Angular frequency and the Bandwidth [5] are given as

$$\omega_0 = \sqrt{\frac{g_{mF} g_{mS}}{C_1 C_2}} \tag{4.36}$$

$$Q = \frac{g_{mF}}{C_2} \tag{4.37}$$

SIMULATION RESULTS:

For this simulation, CMOS implementation of VDTA given in Figure 3 is used. The simulation is done on PSPICE using 0.35µm TSMC CMOS process parameters. The aspect ratios for the PMOS and NMOS transistor are given in Table 2. Supply voltages used for providing the biasing for the given circuit are $+V_{DD} = -V_{SS} = 2$ volts. The values of the passive elements are chosen to be $C_1 = C_2 = 20$ pF [5]. The natural frequency of the filter is chosen to be 3.03 MHz and Quality factor is chosen to be 1 [5]. For achieving these values the transconductance values are chosen [5] to be $g_{mF1} = g_{mS1} = g_{mF2} = g_{mS1} = 381\mu A/V$. For achieving these values the biasing currents are chosen [4] to be $I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 40\mu A$.

The circuit used for the simulation in PSPICE software is given in Figure 37. However this circuit is used only for case 1 indicated above and for the rest of the cases the changes on the three terminals is done as written above in those five points.

Figure 38 indicates the results of simulation which are obtained at the V_{out} terminal following the input conditions given in point no 1 and it is a Low Pass response. The cut off frequency of the filter is obtained to be 3.782 MHz.

Figure 39 indicates the results of simulation that are obtained at the terminal V_{out} following the input conditions given in point no 2 and it is a Band Pass response. The lower cut off frequency obtained after simulation is equal to 1.886 MHz and the higher cut off frequency is equal to 4.808 MHz. The Bandwidth of the filter is obtained to be 2.929 MHz.

Figure 40 indicates the results of simulation that are obtained at the terminal V_{out} following the input conditions given in point no 3 and it is a High Pass response. The cut off of the filter is obtained to be at 2.3913 MHz.

Figure 41 indicates the results of simulation that are obtained at the terminal V_{out} following the input conditions given in point no 4 and it is a Band Stop response. Frequency at the notch is obtained to be 3.237 MHz. The first 3-dB point is obtained at 1.808 MHz, the second 3-dB point is obtained at 4.945 MHz and the Bandwidth of the stop band is 3.136 MHz.

Figure 42 indicates the results of simulation that are obtained at the terminal V_{out} following the input conditions given in point no 3 and it is a All Pass response. This figure indicates both the phase and magnitude response of All Pass filter in the same graph.

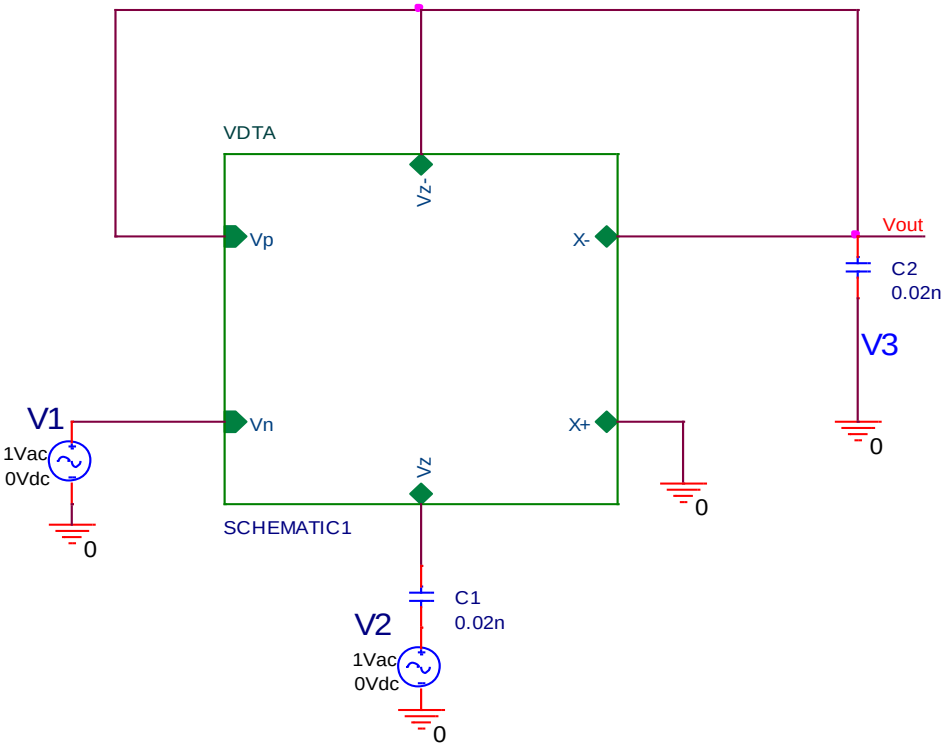

Figure 37 : PSPICE circuit diagram of Topology E (case 1)

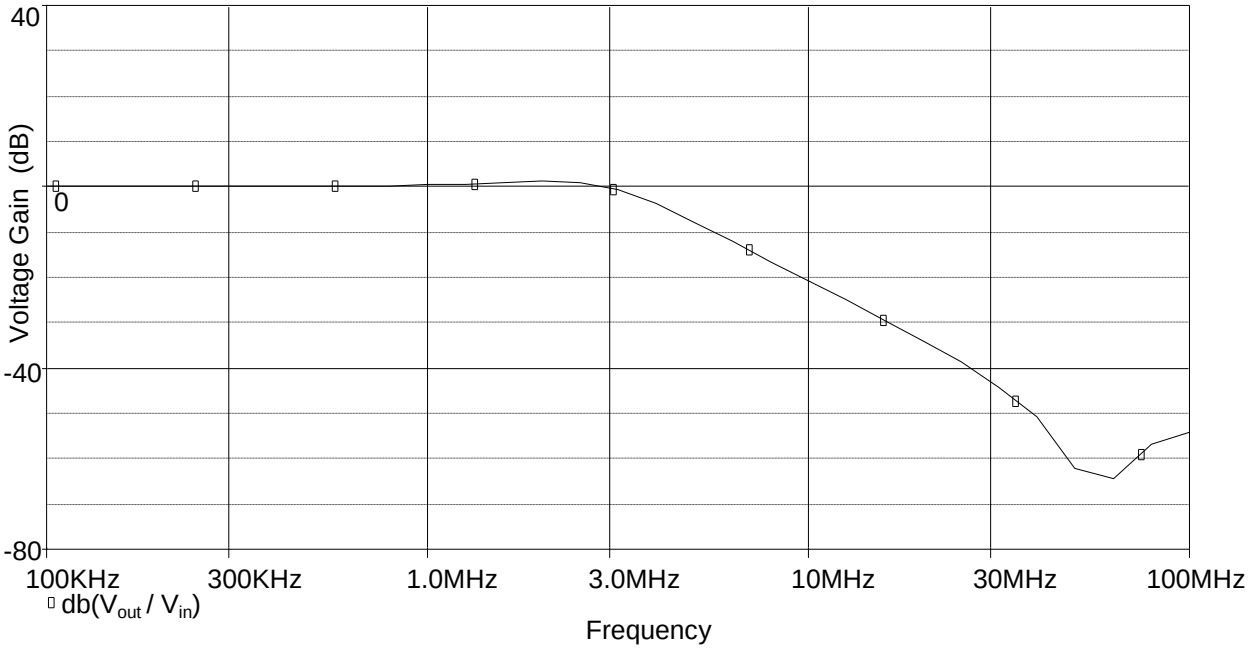

Figure 38 : Simulated Low Pass response of Topology E

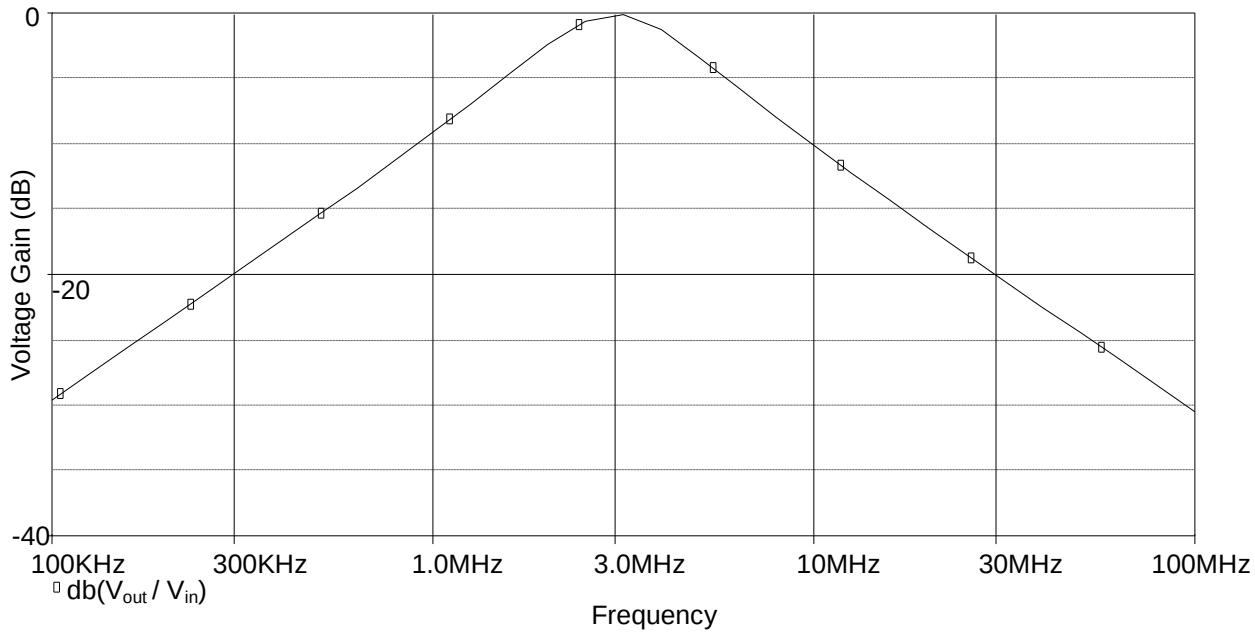

Figure 39 : Simulated Band Pass response of Topology E

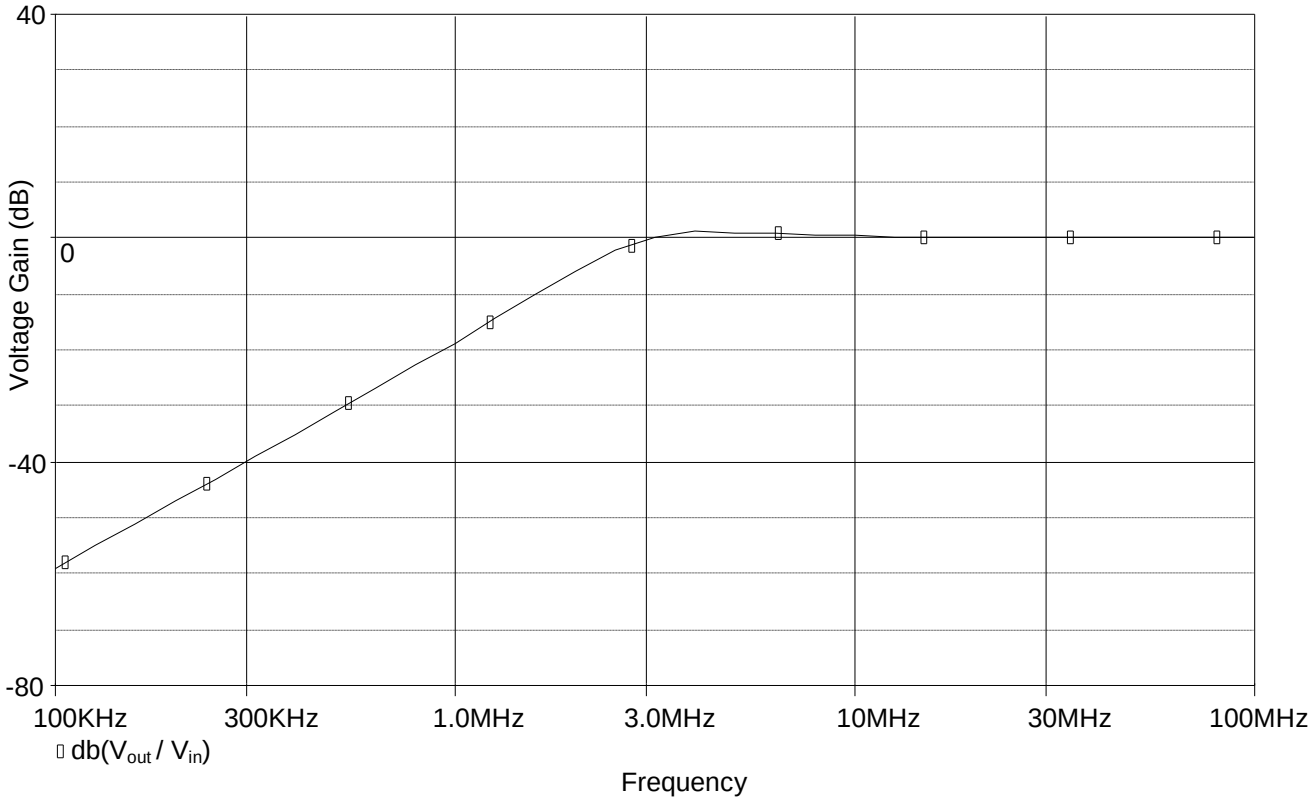

Figure 40 : Simulated High Pass response of Topology E

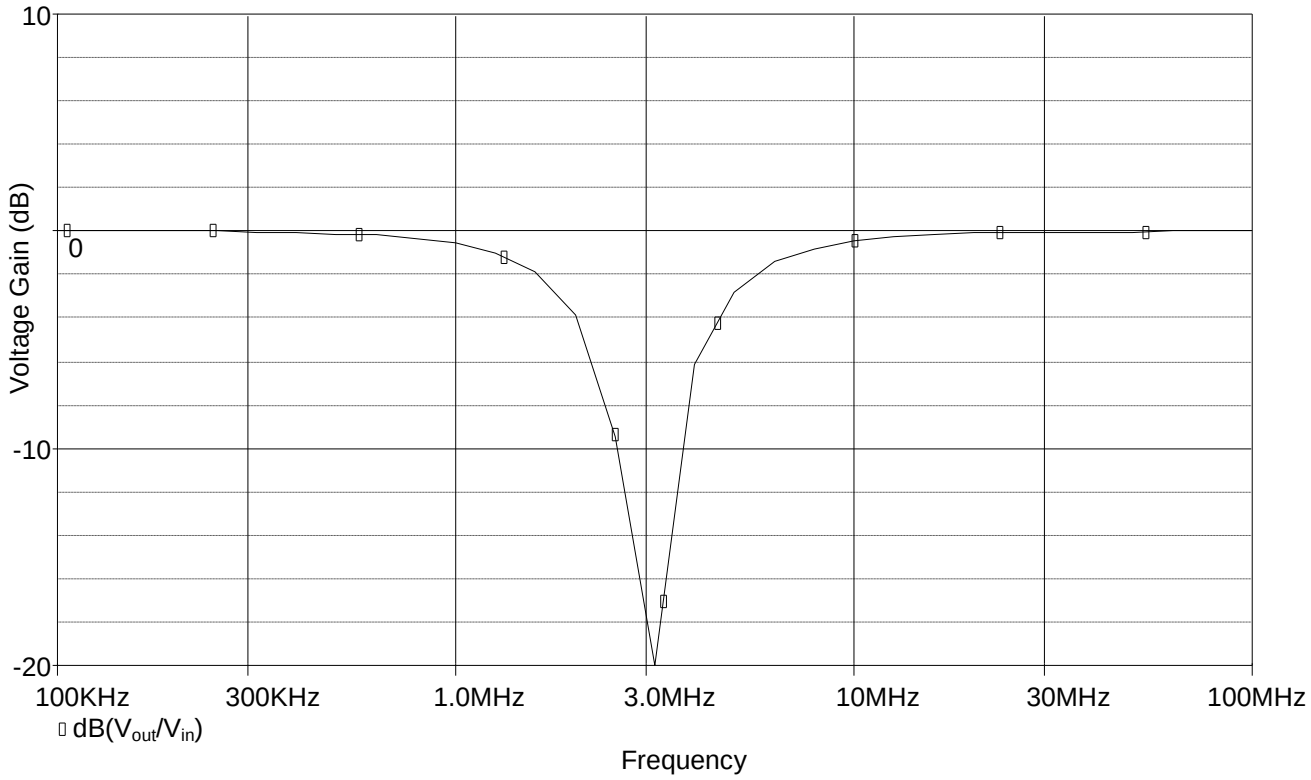

Figure 41 : Simulated Band Stop response of Topology E

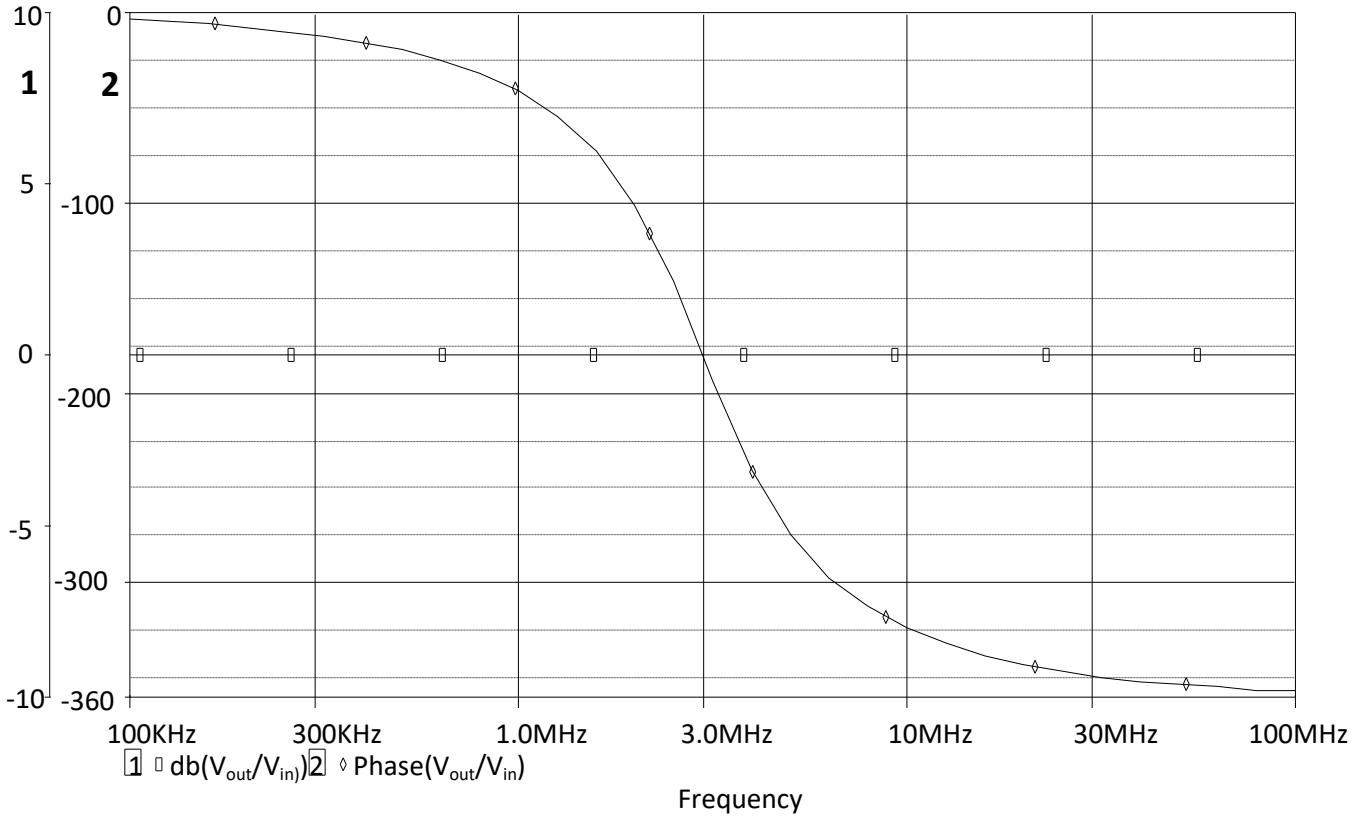

Figure 42 : Simulated All Pass response of Topology E

4.2.6 TOPOLOGY F

The filter topology here named as Topology F was introduced in 2014 [6]. This topology here shows a filter that works in current mode. Here only one output terminal is present but there is a presence of three input terminals along with it. So the output that we get depends on the terminal on which input is applied. This topology is capable of implementing all the filters i.e Low Pass, Band Pass, High Pass, Band Stop and All Pass filters. This filter uses two VDTA's and two capacitors which are grounded. The CMOS implementation of VDTA that is used here is given in Figure 3 and the aspect ratios of both the NMOS and PMOS transistors that are used here are given in Table 2. The circuit used for this topology is given in Figure 43. Here we can see that there is no need of any external passive resistor which is one of the benefits of this topology. This filter is capable of giving an independent control to both the angular frequency (ω_0) and the Quality factor (Q). This control is provided through the transconductances of VDTA's.

In the Figure 43, the terminals represented by I_1, I_2 and I_3 are the input terminals and the terminal represented by I_{out} is the only output terminal. The filter that is implemented on the output terminal is dependent on the input terminal at which input is being applied.

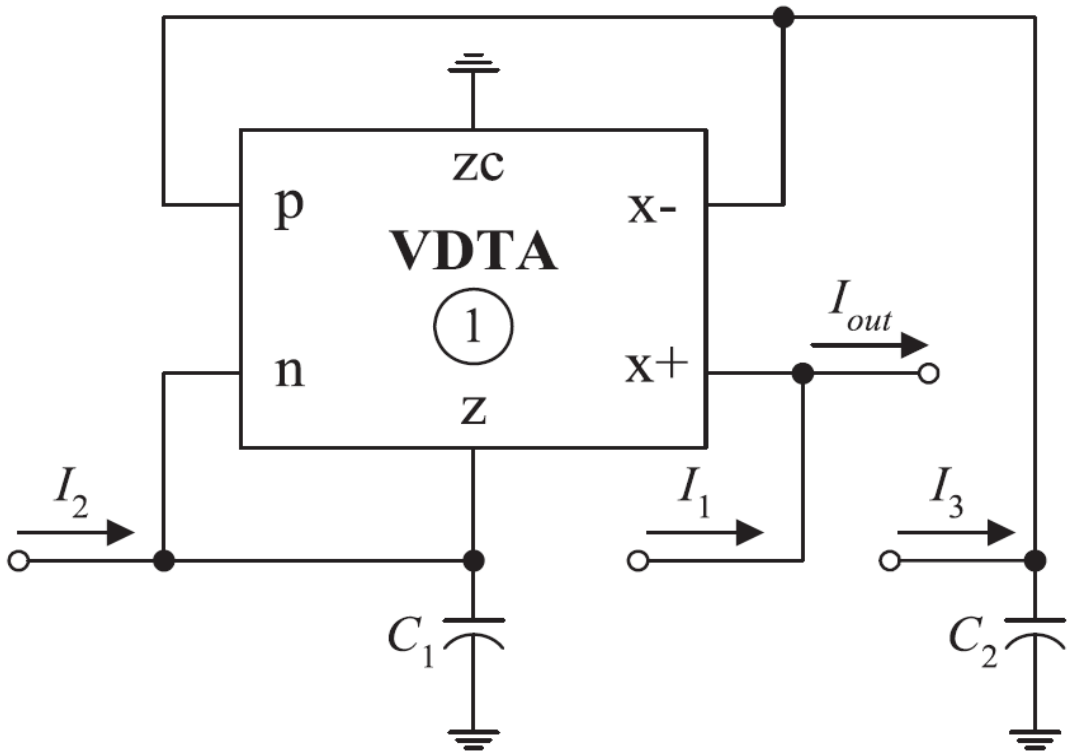

Figure 43 : Current Mode Universal filter (Topology F) [6]

Upon the analysis of the above circuit, the representation in s - domain [6] can be done as

$$I_{out} = \frac{D(s)I_1 + \left(\frac{g_{mS1}}{C_1}\right)sI_2 + \left(\frac{g_{mF1}g_{mS1}}{C_1C_2}\right)I_3}{D(s)} \tag{4.38}$$

Where $$D(s) = s^2 + \left(\frac{g_{mF1}}{C_1}\right)s + \left(\frac{g_{mF1}g_{mS1}}{C_1C_2}\right) \tag{4.39}$$

So using above equation transfer function of any filter can be realised, so as to realise all the filters there are five different conditions [6] for the application of the input signal at the input terminals where each condition is going to realize a different function at the output terminal and are obtained using the equation 4.38.

1. If the current signal is being applied to the I_3 input terminal and the rest two terminals are devoid of any input signal i.e $I_3 = I_{in}$ and $I_1 = I_2 = 0$, then the response obtained at I_{out} is Low Pass and the gain obtained in the Pass Band is unity.
2. If the input current signal is supplied to the I_2 terminal and the rest two terminals are devoid of any input signal i.e $I_2 = I_{in}$ and $I_1 = I_3 = 0$, then the response obtained at I_{out} is Band Pass and the gain obtained in Pass Band is g_{mS1}/g_{mF1}.
3. If the input terminal is supplied at I_1 and the opposite of that signal is supplied at I_2 and I_3 terminal i.e $I_1 = -I_2 = -I_3 = I_{in}$ and $g_{mF1} = g_{mS1}$, the response obtained at I_{out} is High Pass and the gain obtained in the Pass Band is unity.
4. If I_1 is supplied with the current input signal and I_2 is supplied with the exact opposite of this signal i.e $I_1 = -I_2 = I_{in}$ and also $g_{mF1} = g_{mS1}$. Here I_3 is not supplied with any input i.e $I_3 = 0$, the response obtained at I_{out} is a Band Stop response and the gain obtained in the Pass Band is unity.
5. If the input is supplied at I_1 and I_2 is supplied with double of the input inverted at the terminal I_1 i.e $I_1 = -I_2/2 = I_{in}$, no input is given at I_3 i.e $I_3 = 0$ and $g_{mF1} = g_{mS1}$. Here the response obtained at I_{out} is an All Pass Response and the pass band gain is obtained to be unity.

For all of the above conditions, g_{mF1} and g_{mS1} are defined in equations 4.28 and 4.29.

The equations for the Quality factor and Angular frequency [6] are given as

$$Q = \sqrt{\frac{g_{mF1}g_{mS1}}{C_1C_2}} \tag{4.40}$$

$$\omega_0 = \sqrt{\frac{g_{mS1}C_1}{g_{mF1}C_2}} \quad (4.41)$$

SIMULATION RESULTS:

For this simulation, CMOS implementation of VDTA given in Figure 3 is used. The simulation is done on PSPICE using 0.35µm TSMC CMOS process parameters. The aspect ratios for the PMOS and NMOS transistor are given in Table 2. Supply voltages used for providing the biasing for the given circuit are $+V_{DD} = -V_{SS} = 2$ volts. The values of the capacitors are chosen to be $C_1 = C_2 = 20$ pF [6]. The natural frequency of the filter is chosen to be 3 MHz and Quality factor is chosen to be 1 [6]. For achieving these values the transconductance values are chosen [6] to be $g_{mF1} = g_{mS1} = g_{mF2} = g_{mS1} = 380\mu A/V$. For achieving these values the biasing currents are chosen [4] to be $I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 40\mu A$.

The circuit used for the simulation in PSPICE software is given in Figure 44. However this circuit is used only for case 1 indicated above and for the rest of the cases the changes on the three terminals is done as written above in those five points.

Figure 45 indicates the results of simulation which are obtained at the I_{out} terminal following the input conditions given in point no 1 and it is a Low Pass response. The cut off frequency of the filter is obtained to be 3.76 MHz.

Figure 46 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 2 and it is a Band Pass response. The lower cut off frequency obtained after simulation is equal to 1.87 MHz and the higher cut off frequency is equal to 4.8088 MHz. The Bandwidth of the filter is obtained to be 2.9388 MHz.

Figure 47 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 3 and it is a High Pass response. The cut off of the filter is obtained to be 2.3886 MHz.

Figure 48 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 4 and it is a Band Stop response. Frequency at the notch is obtained to be 3.1637 MHz. The first 3-dB point is obtained at 1.808 MHz, the second 3-dB point is obtained at 4.934 MHz and the Bandwidth of the stop band is 3.127 MHz.

Figure 49 indicates the results of simulation that are obtained at the terminal I_{out} following the input conditions given in point no 3 and it is a All Pass response. This figure indicates both the phase and magnitude response of All Pass filter in the same graph.

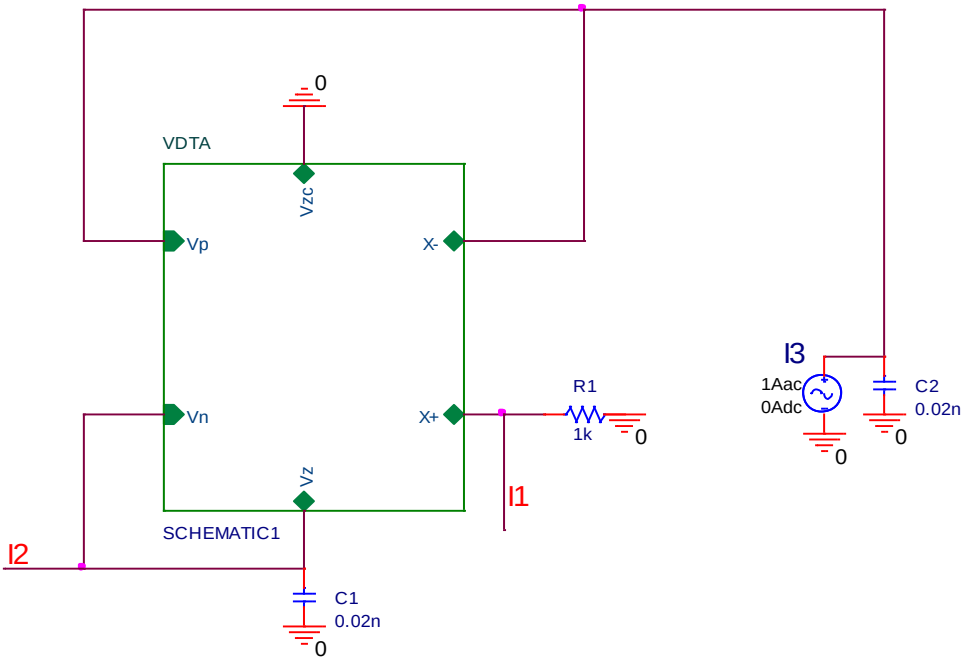

Figure 44 : PSPICE circuit diagram of Topology F (case 1)

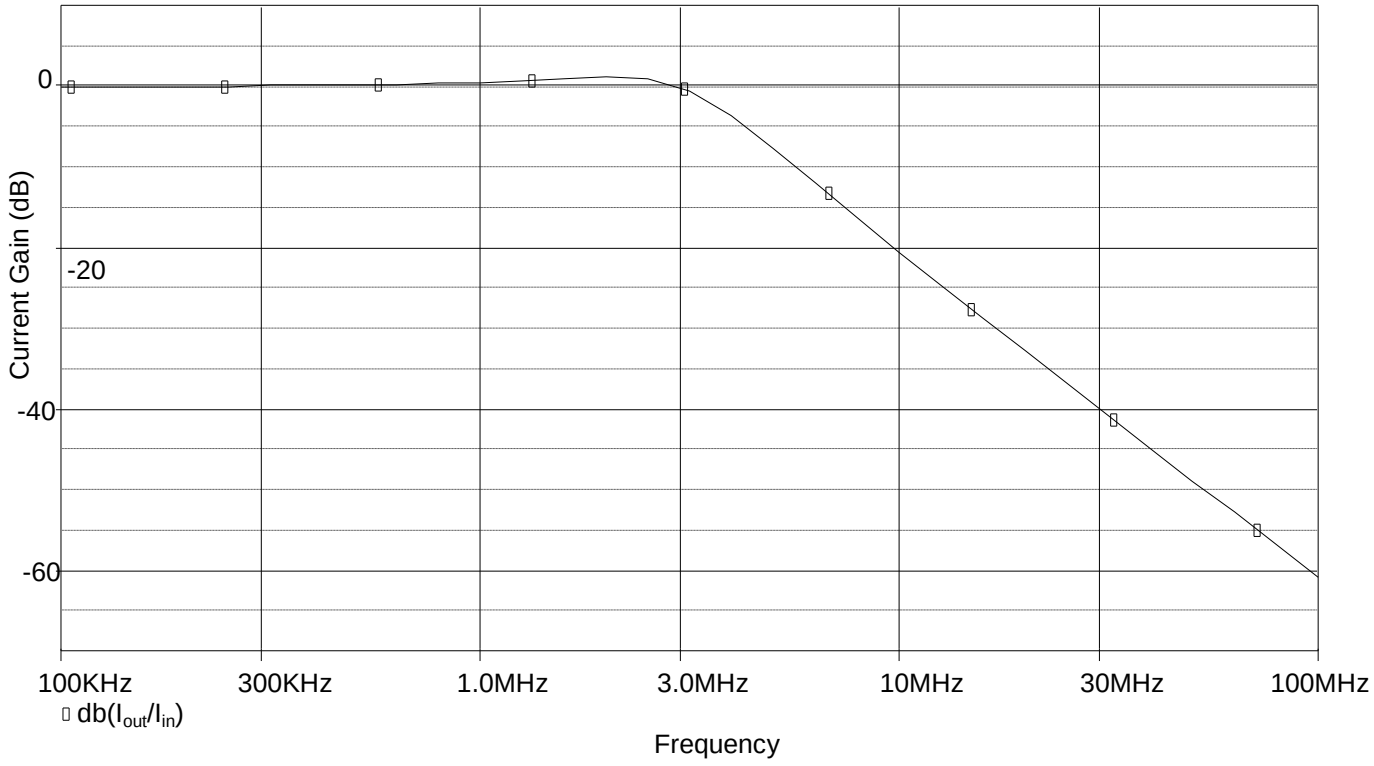

Figure 45 : Simulated Low Pass response of Topology F

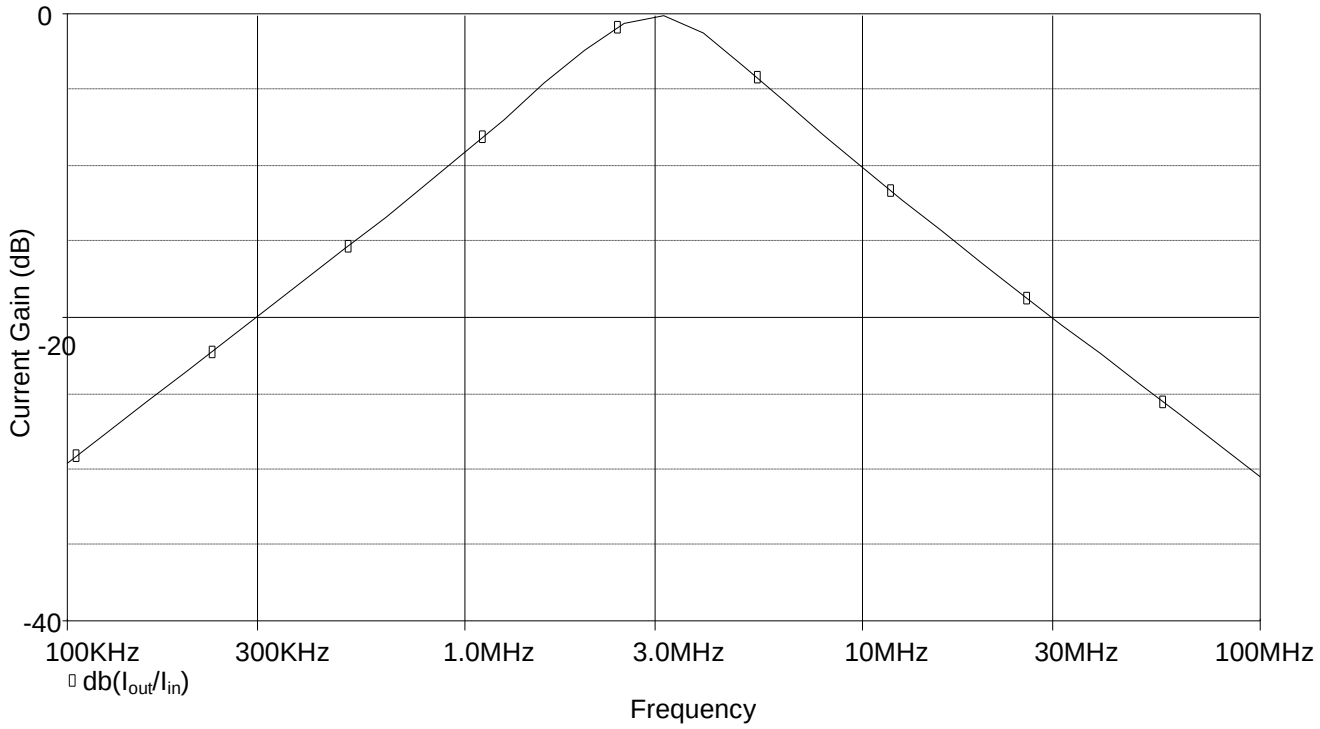

Figure 46 : Simulated Band Pass response of Topology F

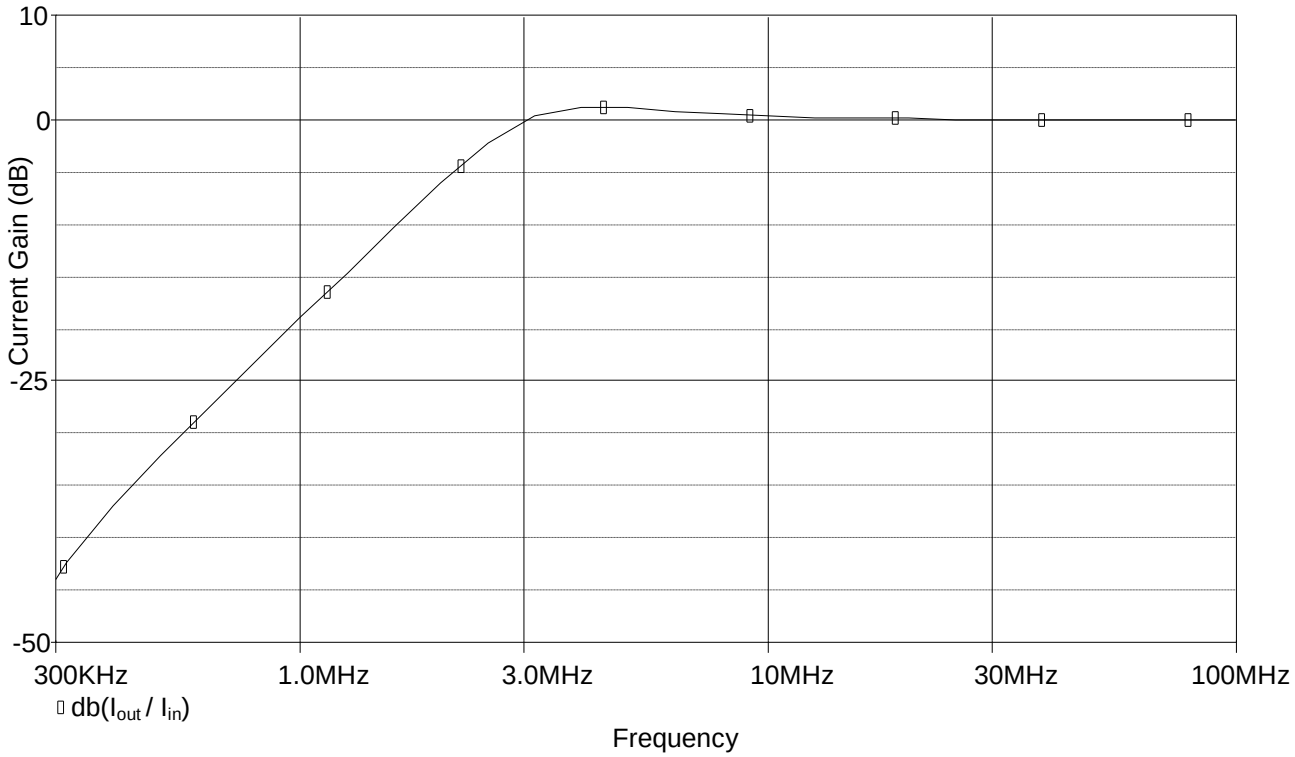

Figure 47 : Simulated High Pass response of Topology F

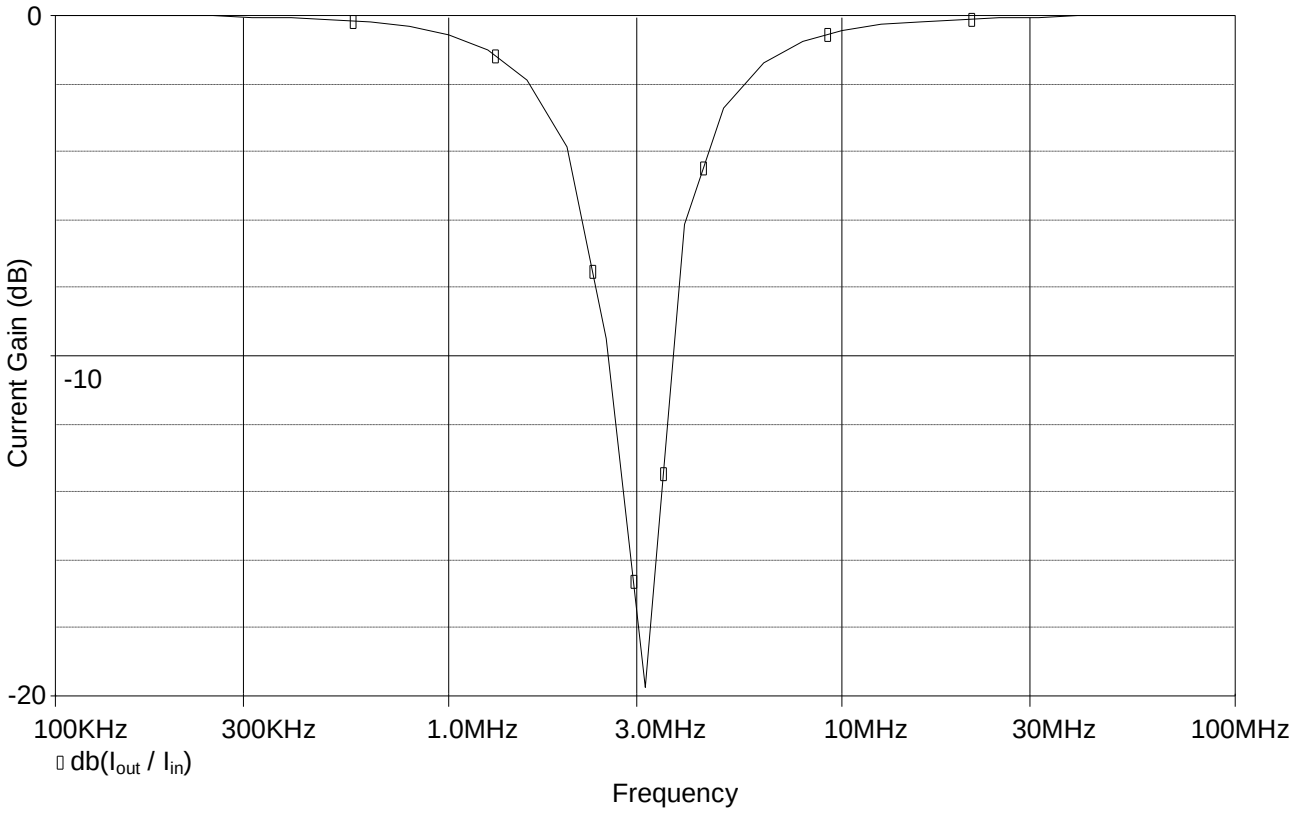

Figure 48 : Simulated High Pass response of Topology F

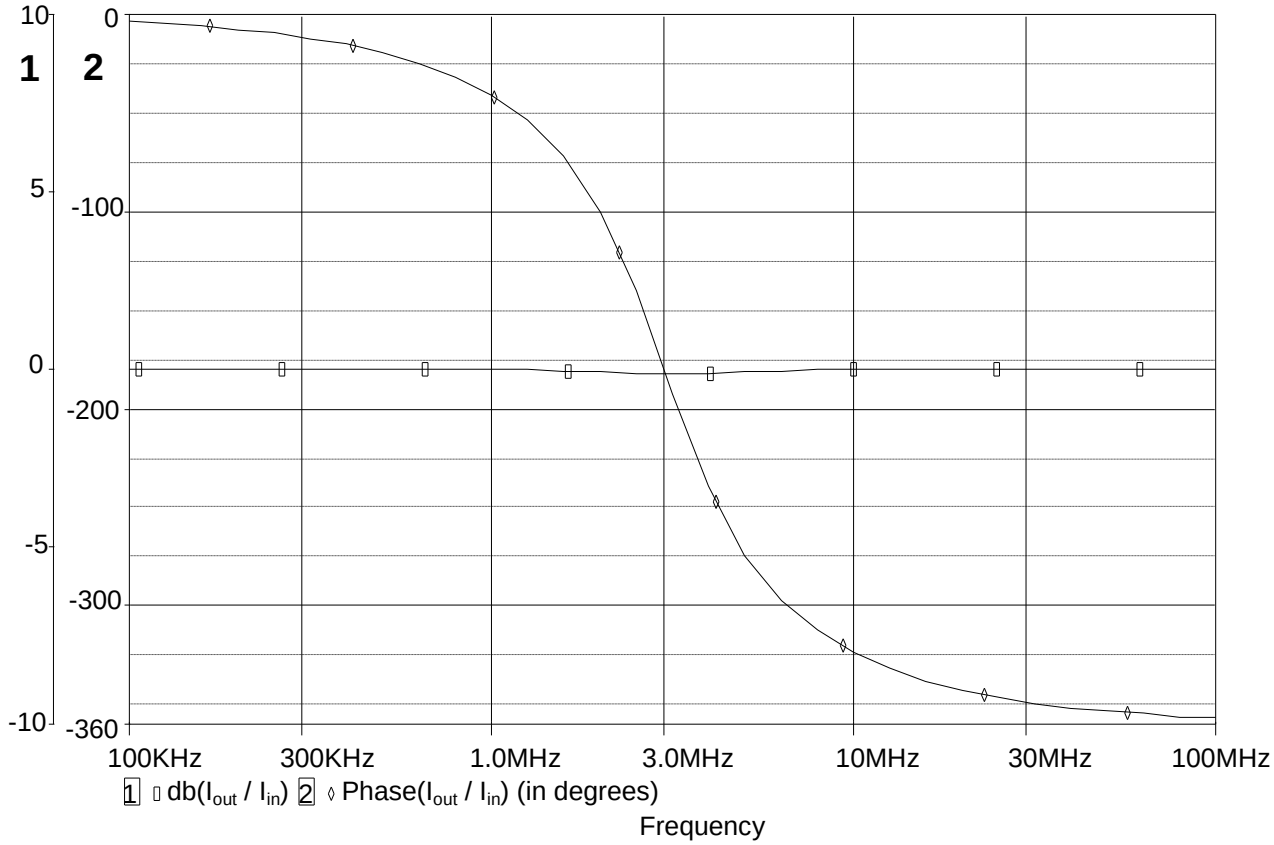

Figure 49 : Simulated All Pass response of Topology F

4.2.7 TOPOLOGY G

The filter topology here named as Topology G was introduced in 2014 [7]. This topology here shows a filter that works both in current mode and voltage mode. Here three output terminals are present and two input terminals are present. Out of two input terminals present one input terminal is for the voltage signal and one input terminal is for the current signal, on the other hand the output terminals are same for the current and the voltage output. This filter topology is capable of implementing three basic filter functions i.e Low Pass, Band Pass and High Pass filter. This topology uses a single VDTA accompanied by three capacitors and two resistors. The CMOS implementation of VDTA that is used in this topology is given in Figure 2 and the aspect ratios of the MOS transistors that are used here are given in Table 1. The circuit used in this topology is shown in Figure 50. This topology provides the capability of orthogonal tuning of the natural frequency and the Quality factor.

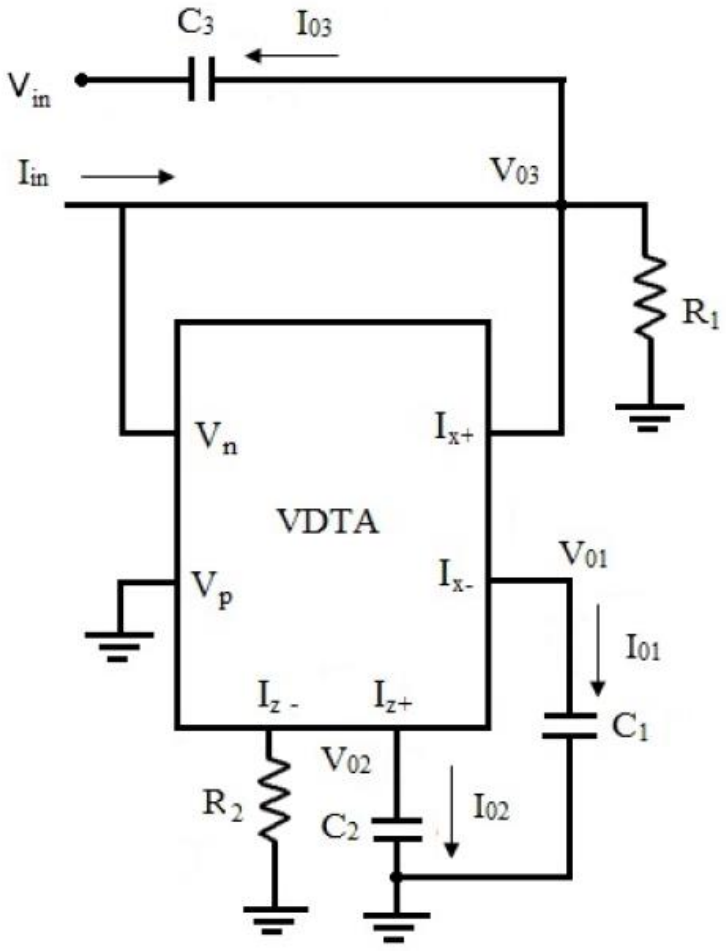

Figure 50 : Dual Mode Biquadratic filter (Topology G) [7]

In Figure 49, terminal represented by V_{in} is the input voltage terminal and the terminal represented by I_{in} is the input current terminal. V_{01}, V_{02} and V_{03} are the voltage output terminals and the terminals represented by I_{01}, I_{02} and I_{03} are the current output terminals.

This topology works in Voltage mode if I_{in} is removed and the transfer function at the different terminals after analysis [7] can be written as

Low Pass →
$$\frac{V_{01}}{V_{in}} = \frac{-\frac{g_{m1}\,g_{m2}}{C_1C_2}}{D(s)} \tag{4.42}$$

Band Pass →
$$\frac{V_{02}}{V_{in}} = \frac{\left(\frac{g_{m1}}{C_1}\right)s}{D(s)} \tag{4.43}$$

High Pass →
$$\frac{V_{03}}{V_{in}} = \frac{-\,g_{m1}\,R_3\,s^2}{D(s)} \tag{4.44}$$

Where
$$D(s) = s^2 + \left(\frac{1}{R_1C_2}\right)s + \left(\frac{g_{m1}g_{m2}}{C_2C_3}\right) \tag{4.45}$$

This topology works in Current mode if V_{in} is removed i.e V_{in} is shorted to the ground and the transfer function at the different terminals after the analysis [7] can be written as

Low Pass →
$$\frac{I_{01}}{I_{in}} = \frac{\frac{g_{m1}\,g_{m2}}{C_2C_3}}{D(s)} \tag{4.46}$$

Band Pass →
$$\frac{I_{02}}{I_{in}} = \frac{\left(\frac{g_{m1}}{C_1}\right)s}{D(s)} \tag{4.47}$$

High Pass →
$$\frac{I_{03}}{I_{in}} = \frac{s^2}{D(s)} \tag{4.48}$$

Where D(s) is given in equation 4.45.

The value of the natural frequency i.e ω_0 and the value of the Quality factor i.e Q is same in both the cases i.e in both the voltage mode and current mode. The value of the natural frequency and the Quality factor is given by

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_2C_3}} \tag{4.49}$$

$$Q = R_1\sqrt{\frac{g_{m1}g_{m2}C_2}{C_3}} \quad (4.50)$$

SIMULATION RESULTS:

For this simulation, CMOS implementation of VDTA given in Figure 2 is used. The simulation is done on PSPICE using 0.18µm TSMC CMOS process parameters. The aspect ratios for the PMOS and NMOS transistor are given in Table 1. Supply voltages used for providing the biasing for the given circuit are $+V_{DD} = -V_{SS} = 0.9$ Volts. The values of the capacitors and resistors are chosen as $C_1 = C_2 = C_3 = 1$ nF and $R_1 = R_2 = 1k\Omega$ [7]. The natural frequency of the filter is chosen to be 101.27 kHz and Quality factor is chosen to be 0.636 [7]. For achieving these values the transconductance values are chosen [7] to be $g_{m1} = g_{m2} =$ 636.3µA/V. For achieving these values the biasing currents are chosen [7] to be $I_{B1} = I_{B2} = I_{B3} = I_{B4} = 150\mu A$.

The circuit used for the simulation in PSPICE software for this topology in current mode is given in Figure 51.

Figure 52 indicates the results of simulation which are obtained at the I_{01} terminal and it is a Low Pass response. The cut off frequency of the filter is obtained to be 84.296 KHz.

Figure 53 indicates the results of simulation that are obtained at the terminal I_{02} and it is a Band Pass response. The lower cut off frequency obtained after simulation is equal to 49.014 KHz and the higher cut off frequency is equal to 211.742 KHz. The Bandwidth of the filter is obtained to be 162.728 KHz.

Figure 54 indicates the results of simulation that are obtained at the terminal I_{03} and it is a High Pass response. The cut off of the filter is obtained to be 117.752 KHz.

The circuit used for the simulation in PSPICE software for this topology in voltage mode is given in Figure 55.

Figure 56 indicates the results of simulation which are obtained at the V_{01} terminal and it is a Low Pass response. The cut off frequency of the filter is obtained to be 84.296 KHz.

Figure 57 indicates the results of simulation that are obtained at the terminal V_{02} and it is a Band Pass response. The lower cut off frequency obtained after simulation is equal to 49.38

KHz and the higher cut off frequency is equal to 210.175 KHz. The Bandwidth of the filter is obtained to be 160.795 KHz.

Figure 58 indicates the results of simulation that are obtained at the terminal V_{03} and it is a High Pass response. The cut off of the filter is obtained to be 117.752 KHz.

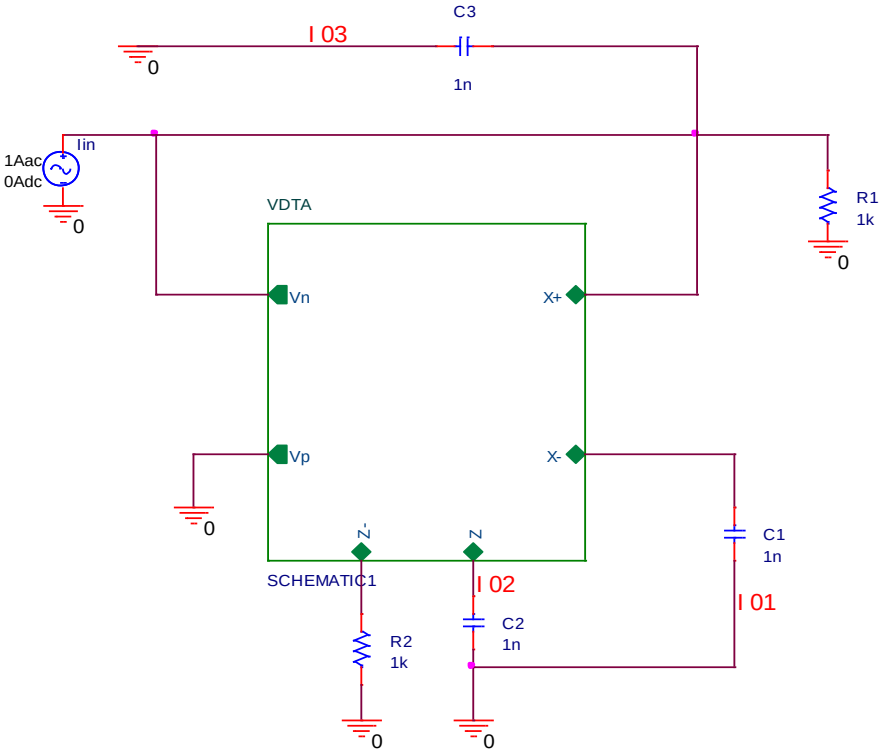

Figure 51 : PSPICE circuit diagram of Topology G for the current mode

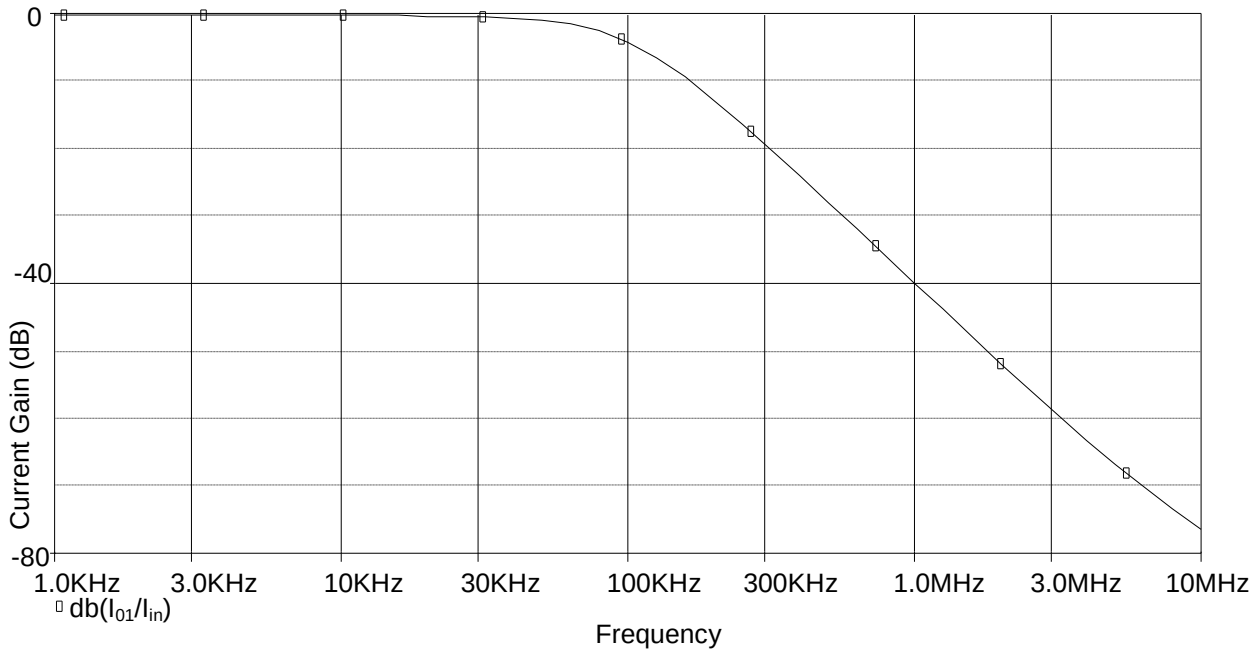

Figure 52 : Simulated Low Pass response of Topology G in current mode

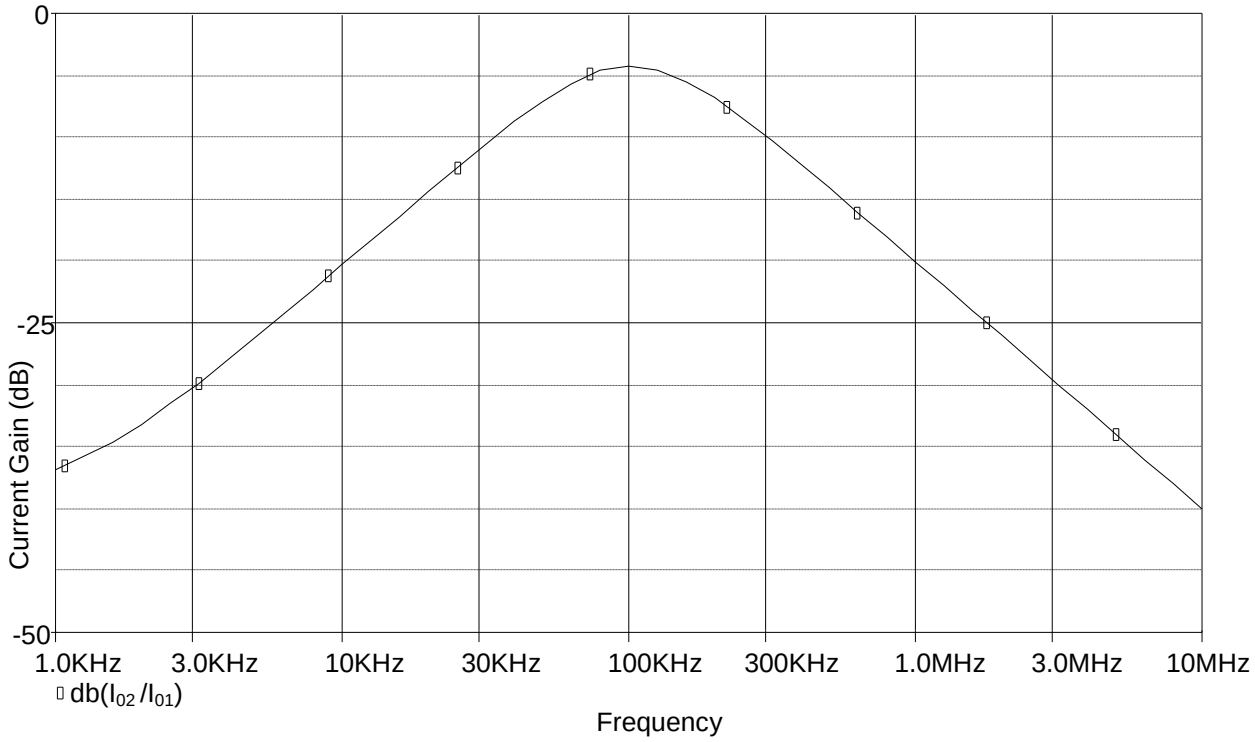

Figure 53 : Simulated Band Pass response of Topology G in current mode

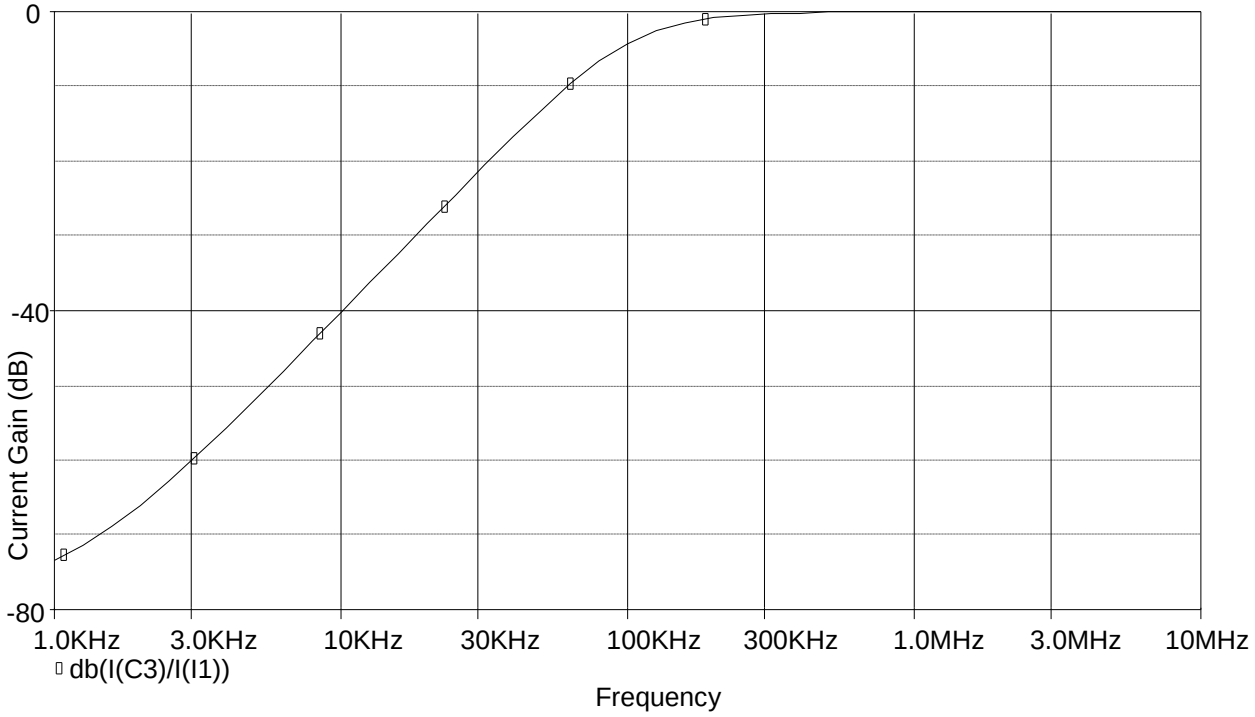

Figure 54 : Simulated High Pass response of Topology G in current mode

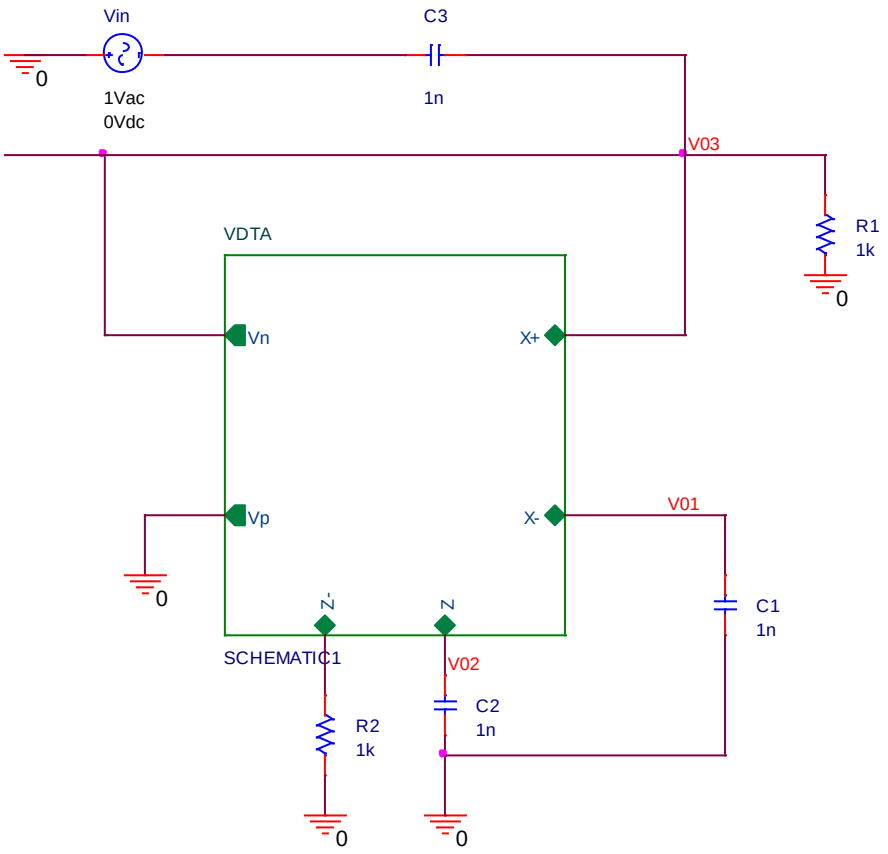

Figure 55 : PSPICE circuit diagram of Topology G for the Voltage mode

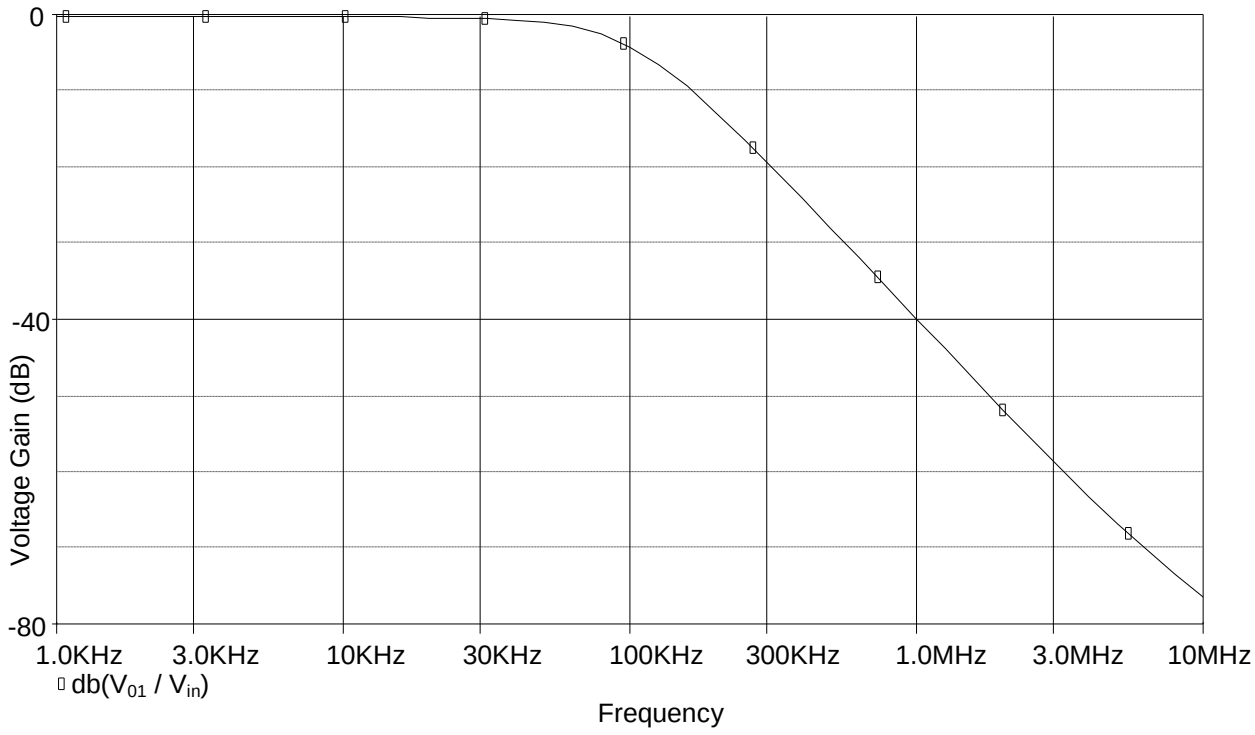

Figure 56 : Simulated Low Pass response of Topology G in voltage mode

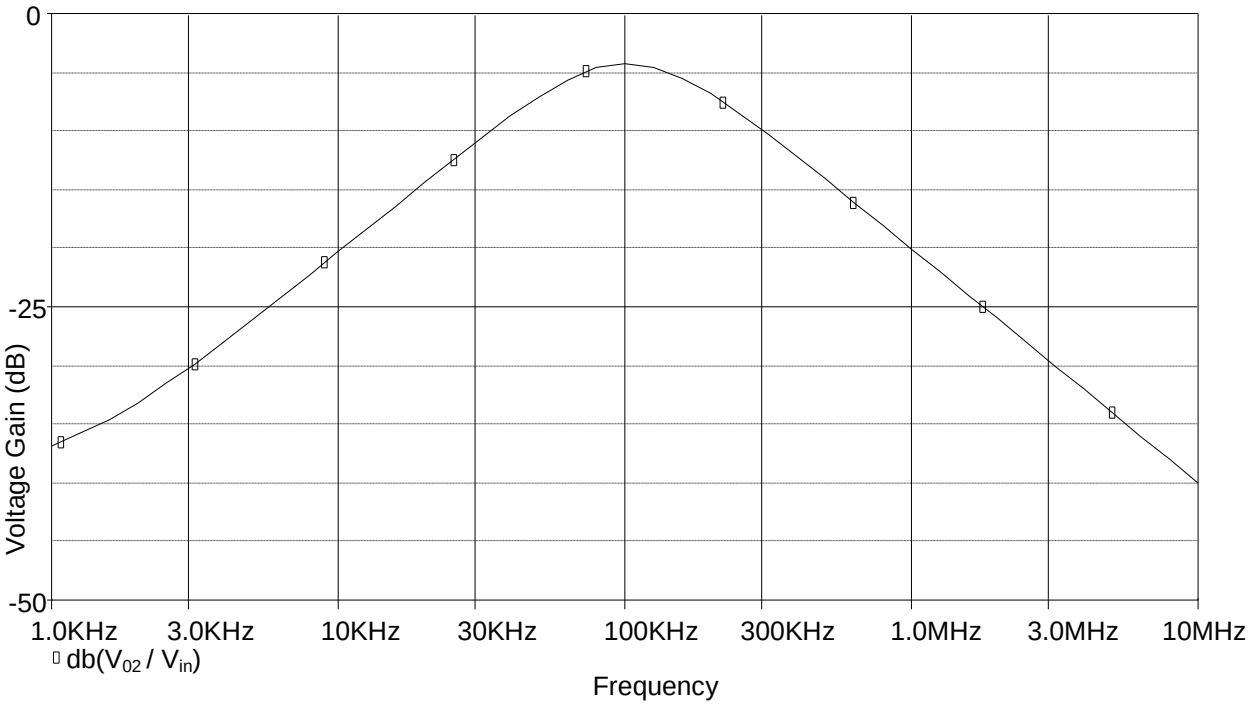

Figure 57 : Simulated Band Pass response of Topology G in voltage mode

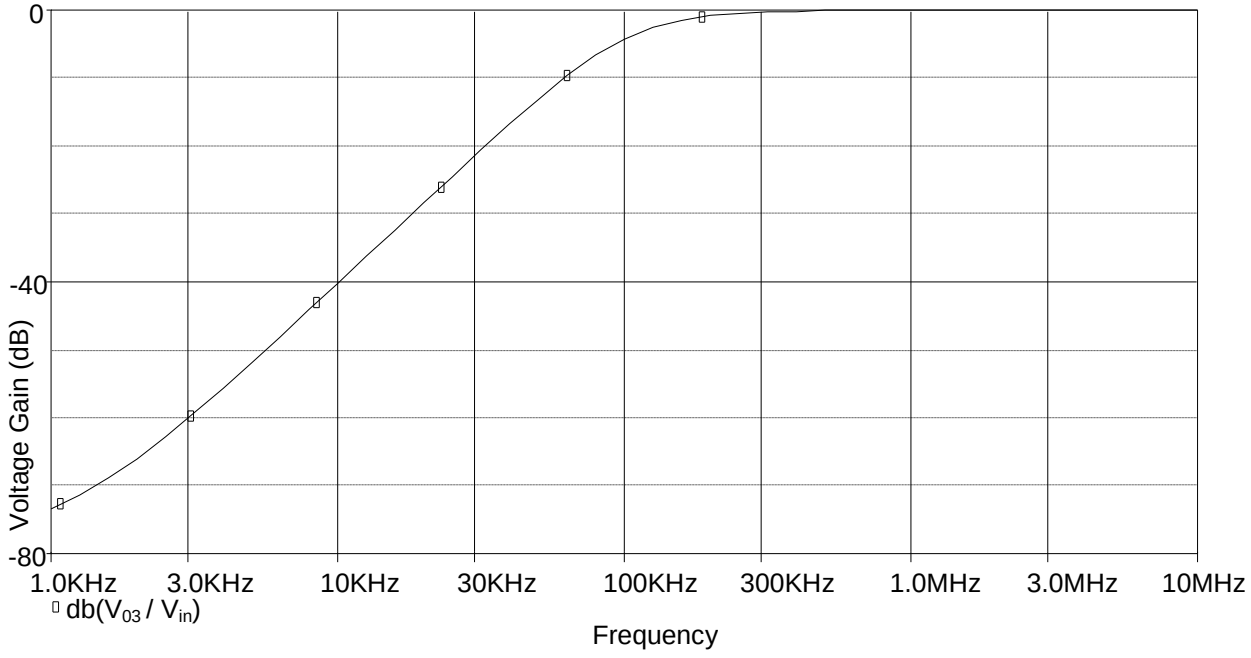

Figure 58 : Simulated High Pass response of Topology G in voltage mode

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CHAPTER 5

OSCILLATOR USING VDTA

5.1 INTRODUCTION

Many electronic systems and circuits which provide the central clock signal in order to control the operation of the system in a particular or defined sequence use an oscillator. Oscillators are the electronic circuits which use the DC supply as an input and the output which is generated is an AC waveform. This AC output have a big range of wave shapes and frequencies which can range from a simple sine wave output to the different complicated frequencies depending on application.

The signal that is generated as the output of the oscillator is of a non-varying amplitude. The shape of the generated wave and the amplitude of the generated wave are dependent on the design of the oscillator and the values of the component chosen. The frequency of wave present at the output can be a fixed or a varying value which totally depends on the design of the oscillator.

The oscillator can also be termed as an amplifier with Positive Feedback or a regenerative type of feedback (in phase). One of the basic problem in electronic circuit designing is to avoid the oscillations in case of the designing of amplifiers and on the other hand to make the oscillators to oscillate is again a challenge.

The working of an oscillator is possible because of their capability to overcome the losses which occur in the feedback resonator circuit which is in the form of inductor, capacitor or both in that circuit only by the application of DC energy at the desired frequency in the resonator circuit. It can also be said in the other way that an oscillator is basically an amplifier that uses a positive feedback which is capable of generating a frequency at the output without use of any oscillating input signal and is capable of sustaining it on its own.

An oscillator has a small signal amplifier in the feedback path which has a unity open loop gain or it may be chosen slightly greater than one for enabling the oscillator to start but to continue with the oscillations the loop gain must be one again. For designing an oscillator along with the reactive components, a device for amplification such as a Transistor or An

Operational Amplifier is also required. But in contrast to the amplifier there is no need of external AC input for the oscillator to function as the oscillator converts the DC energy supplied to it into the AC energy of the desired frequency. The block diagram for the sinusoidal oscillator is given in Figure 59.

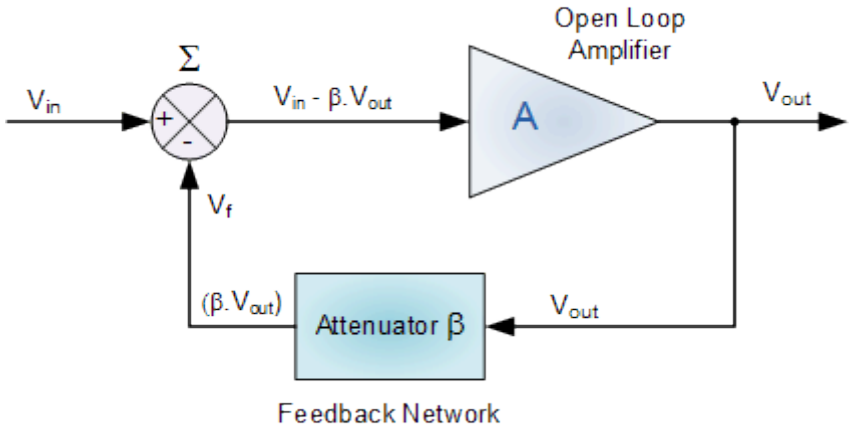

Figure 59 : Basic structure of an oscillator [1]

The frequency generated by the sinusoidal oscillator is that frequency at which the total shift of the entire path i.e the forward path and the feedback path in combination is zero or integral multiple of 2*Π.

For the oscillator to give the sustained oscillations, there is a criterion known as Barkhausen criterion which needs to be satisfied but this is a necessary condition , not a sufficient one i.e for a circuit to oscillate this condition must be satisfied but a circuit satisfying this condition need not necessarily oscillate. The criterion states that at the frequency of oscillation i.e $\omega = \omega_o$, $|A*\beta| = 1$ and the phase shift should be 0 or an integral multiple of 2*Π. Here 180^0 phase shift is provided by the feedback path and the rest of 180^0 is provided by the mixer.

In general the feedback path is designed using the resistive elements only and its function is frequency independent but on the other hand the gain provided by amplifier is frequency dependent.

The frequency of oscillation for an oscillator is mainly dependent on the value of passive elements used in the circuit such as inductance, resistance, capacitance etc. The main reason for the changes in the values of these elements is mainly because of the temperature variations and the compensation measures for the balance of these changes induced because of temperature are taken.

5.2 TOPOLOGY A

This topology shows a current mode electronically tunable third order quadrature oscillator using VDTA [3]. Figure 60 shows the circuit diagram of this oscillator. This is formed by cascading a second order low pass filter in loop with an inverting lossless integrator. The circuit uses three grounded capacitors in addition to two VDTA's. This circuit provides two outputs in form of current signals at a phase difference of 90^0 at its output terminals which are high impedence terminals. The electronic tuning of the frequency of oscillation and the condition of oscillation can be done by varying the biasing currents of VDTA's. Analysis of the circuit of Figure 60 considering $g_{mS1} = g_{mF2} = g_{mA}$ ($I_{BS1} = I_{BS2}$) gives the characteristic equation [3] as

$$s^3C_1C_2C_3 + s^2g_{mF1}C_3(C_1 + C_2) + sg_{mF1}g_{mA}C_3 + g_{mF1}g_{mS2}g_{mA} = 0 \quad (5.1)$$

Here, the variables g_{mFj} or g_{mSj} are the transconductances of the VDTA where j denotes the number of VDTA i.e j =1,2. The value of these transconductances are as given in equation 3.4 to 3.7. The condition of oscillation and the frequency of oscillation [3] are given as

C.O $$\frac{g_{mF1}(C_1+C_2)}{C_1C_2} = \frac{g_{mS2}}{C_3} \quad (5.2)$$

F.O $$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{mF1}g_{mA}}{C_1C_2}} \quad (5.3)$$

By looking on the above 2 equations it can be a clear observation that for electronic control of the condition of oscillation g_{mS2} is used which exercises the control using the bias current I_{BS2}. The frequency of oscillation can be varied using g_{mA} using VDTA bias currents and this does not disturb the condition of oscillation. This means that C.O and F.O are independently controlled. The relationship between two quadrature output currents at the oscillating frequency is

$$\frac{I_{02}(j\omega_0)}{I_{01}(j\omega_0)} = \frac{g_{mS2}}{\omega_0 C_3}e^{-j90^0} \quad (5.4)$$

The Phase Shift of 90^0 between the two current outputs clearly reveal that the circuit is providing quadrature current signals as its outputs. Since the output is being taken from the x terminals of VDTA which are the high impedence terminals, so the output can directly be connected to the next stage without any need of a buffering circuit in addition. Since the magnitude of the output signals is not same in both the cases, so for the applications which need equal magnitude of quadrature current signals other amplifying circuits would be needed.

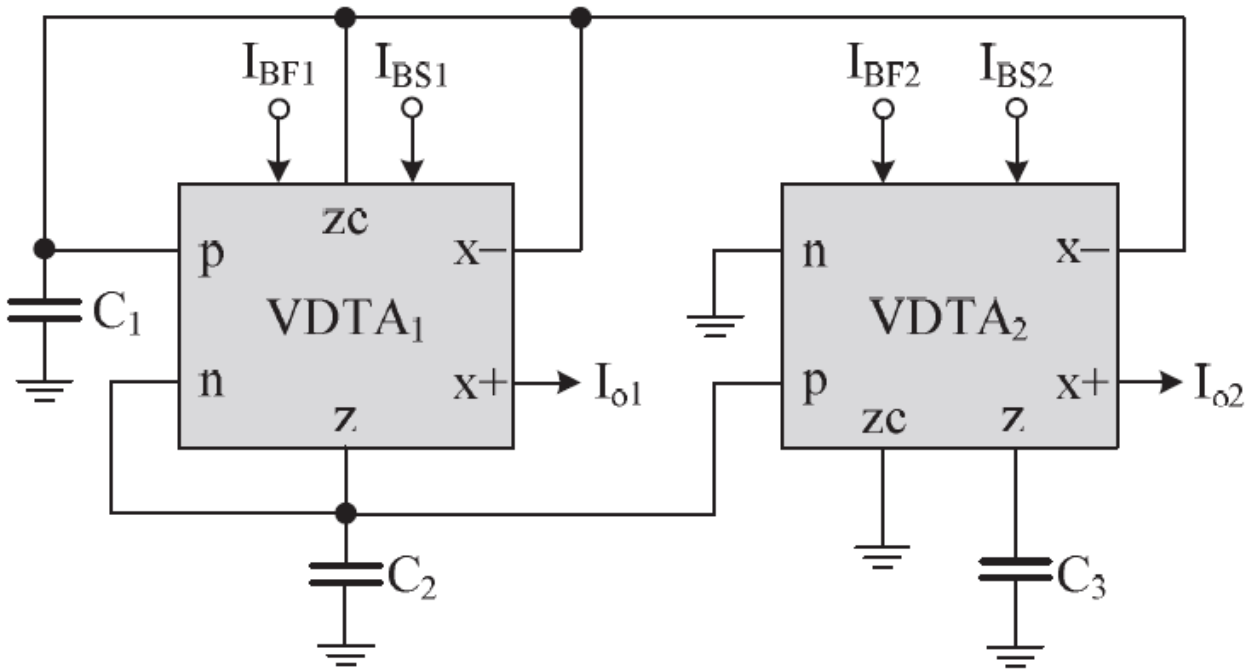

Figure 60 : Current mode third order quadrature oscillator [3].

SIMULATION RESULTS:

For this simulation, CMOS implementation of VDTA given in Figure 3 is used. The simulation is done on PSPICE using 0.35µm TSMC CMOS process parameters. The aspect ratios for the PMOS and NMOS transistor are given in Table 2. Supply voltages used for providing the biasing for the given circuit are $+V_{DD} = -V_{SS} = 2$ Volts. The values of the capacitors are chosen as $C_1 = C_2 = 60$ pF and $C_3 = 30$ pF [3]. The transconductances are chosen to be $g_{mF1} = g_{mS1} = g_{mF2} \approx 410\mu A/V$ and for setting these values of transconductances,

the biasing currents for the VDTA of Figure 3 are chosen to be I_{BF1}= I_{BS1}= I_{BF2}= 50µA and I_{BS2}=65 µA. Theoretically the frequency of the oscillator is 1.1 MHz.

The circuit diagram used for implementation of this topology in PSPICE software is shown in Figure 61.

The results of time domain simulation are shown in Figure 62 and Figure 63 for one of the quadrature outputs. Figure 62 shows the rising output of the topology i.e when the system starts the oscillation and the oscillating output continue to rise. Figure 63 shows the situation when the oscillating output attains a fixed value.

Figure 64 shows both the quadrature outputs of the oscillator.

Figure 65 shows the Lissagous figure of the oscillator.

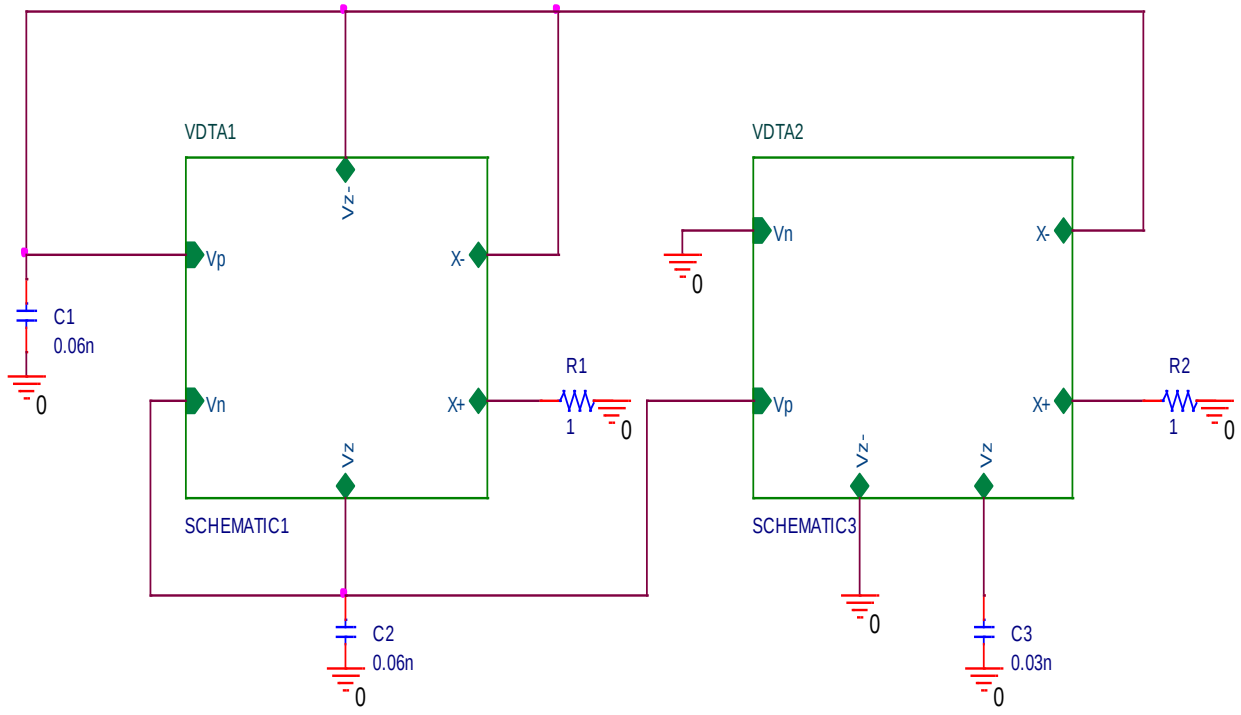

Figure 61 : PSPICE circuit diagram of the Topology A

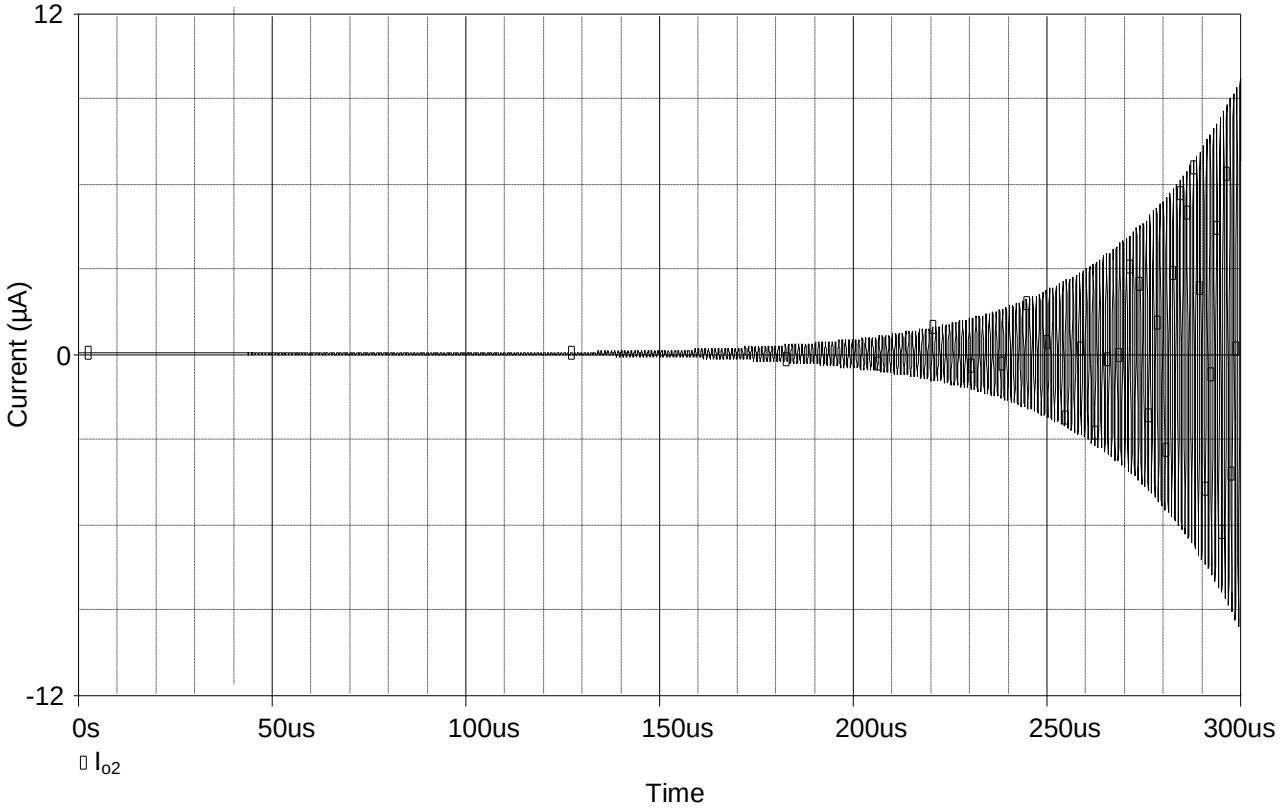

Figure 62 : Transient Response of Topology A (rising output)

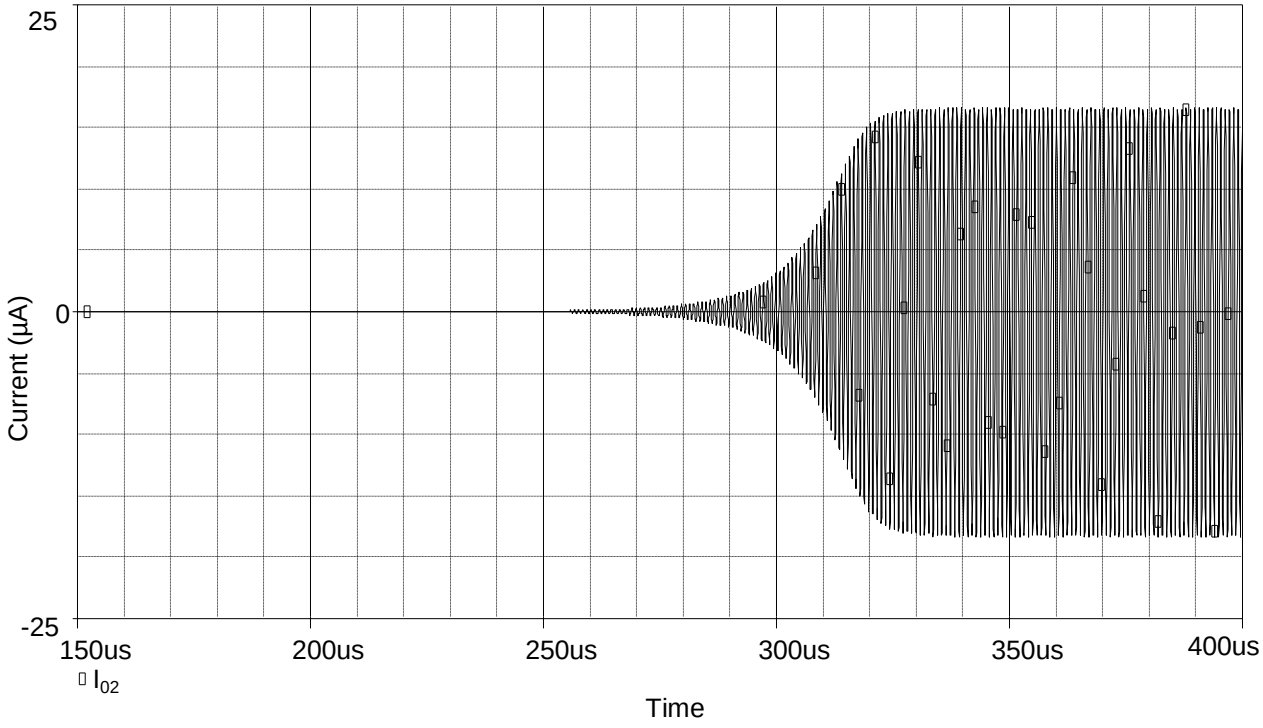

Figure 63 : Transient Response of Topology A (constant output)

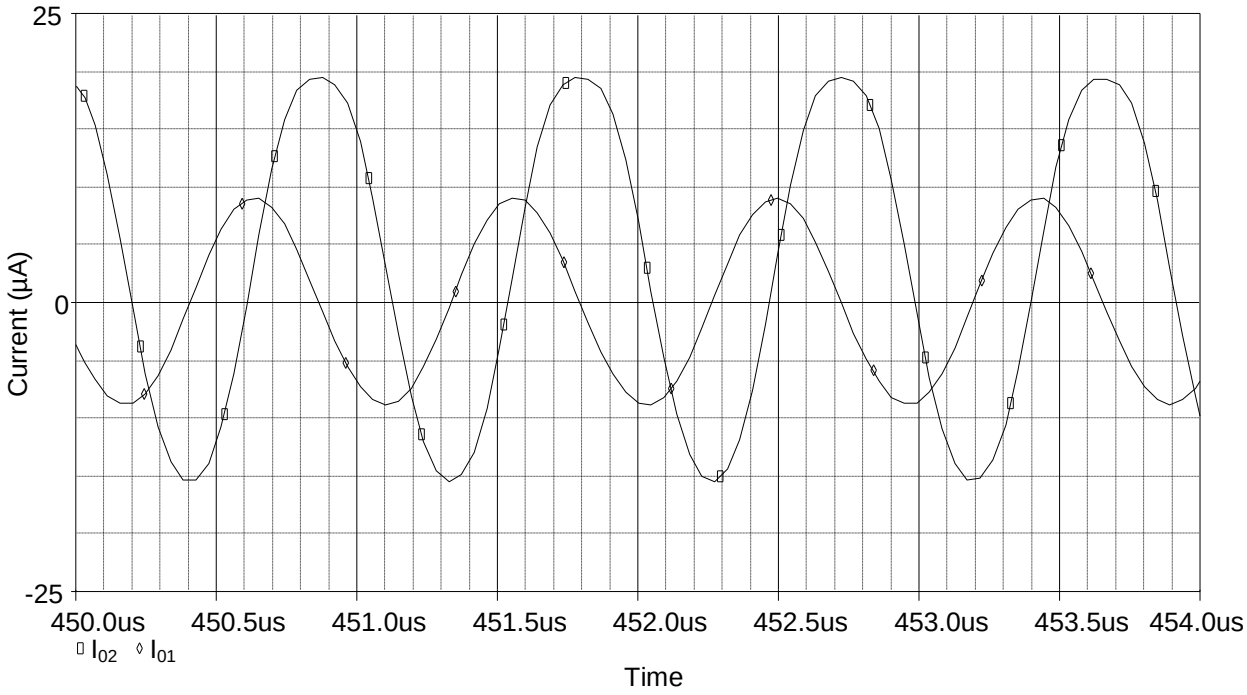

Figure 64 : Quadrature current output waveforms

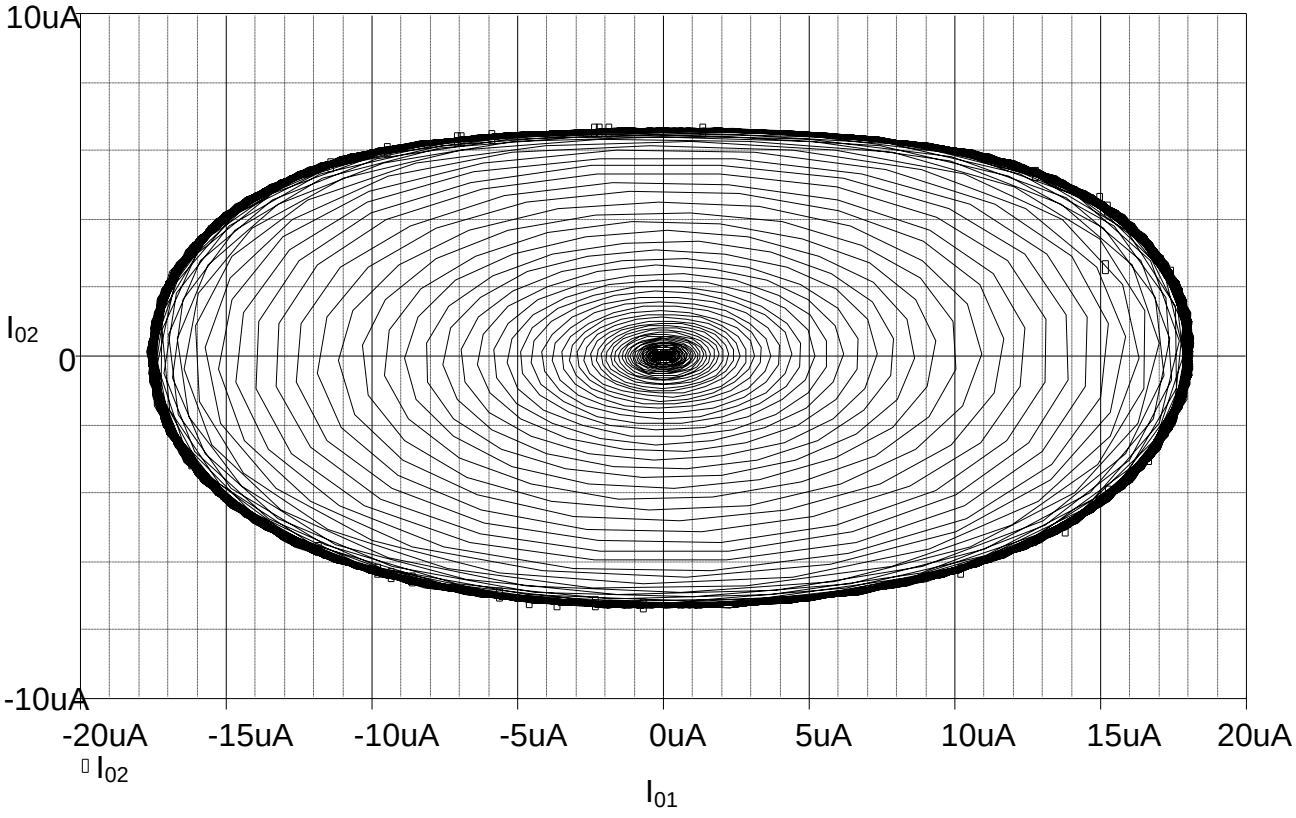

Figure 65 : Lissagous Figure for Topology A

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CHAPTER 6

PARALLEL R-L IMPEDANCE USING VDTA

6.1 INTRODUCTION

Parallel R-L circuit are less practically utilised as compared to series R-L circuit except the case when these are connected with the current source. The series R-L circuit and the frequency dependent negative resistances have been implemented previously using different active elements. Implementation of Frequency dependent negative resistance and R-L series circuit using Operational Amplifiers, Current Feedback Amplifiers and Current Conveyors are given in literature [1-4]. VDTA is an application whose CMOS realisation and its application as filter was proposed by Yesil [5]. A CMOS circuit implementating it is shown in Figure 2. A lot of applications of VDTA have been given till now and simulation of some of those applications have been done and presented in Chapter 4 and 5. In this chapter a grounded Parallel R-L impedance and a High Pass Filter as the application of this grounded Parallel R-L impedance has been simulated.

6.2 PARALLEL R-L IMPEDANCE

As the name suggests, the Parallel R-L impedance is a circuit in which two circuit elements an inductor and a resistor are in a parallel connection. A pictorial representation of this circuit is given in Figure 66.

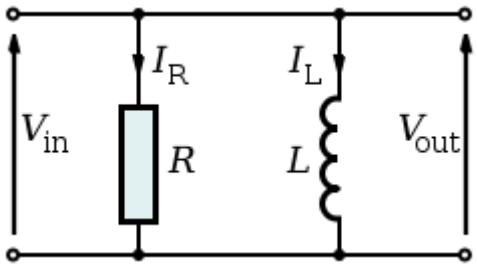

Figure 66 : Parallel R-L Impedance

The Admittance of this network can simply be written as

$$Y_{in} = \frac{1}{s\,L} + \frac{1}{R} \tag{6.1}$$

The circuit using VDTA whose symbolic representation is given in Figure 1 to implement a grounded parallel R-L impedance is shown in Figure 67 and is given in literature [6].

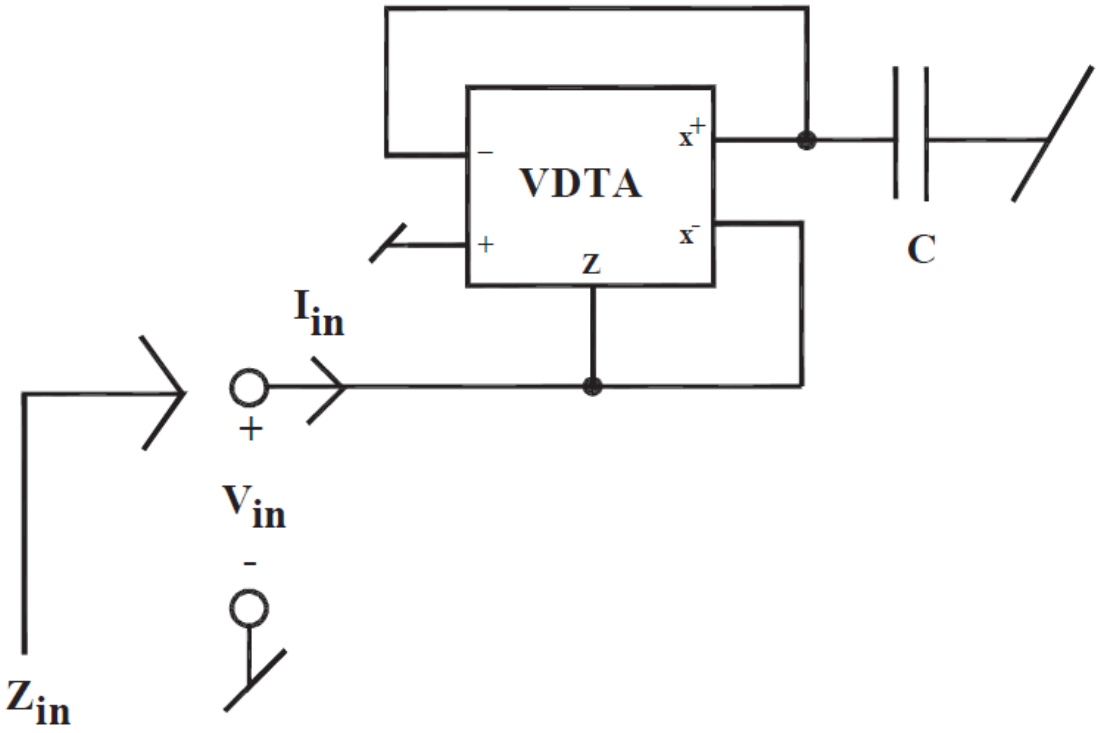

Figure 67 : Parallel R-L Impedance Configuration using VDTA [6]

A simple analysis of the circuit [6] of Figure 65 reveals that the input admittance of the network can be written as

$$Y_{in} = \frac{1}{s\left(\frac{C}{g_{m1}\,g_{m2}}\right)} + g_{m2} \tag{6.2}$$

Which is in clear resemblance with the equation 6.1 and thus clearly indicate the functioning of the circuit as a parallel R-L impedance with the equivalent values of R and L as

$$L_{eq} = \frac{C}{g_{m1}g_{m2}} \tag{6.3}$$

$$R_{eq} = \frac{1}{g_{m2}} \tag{6.4}$$

Circuit utilising this R-L Impedance to realise a High Pass Filter is given in literature [6] and iks shown in Figure 68. Now, after using the definition of VDTA and analysing the circuit [6] of Figure 67 reveals the voltage transfer function of the filter as

$$\frac{V_0}{V_{in}} = \frac{s^2}{s^2+s\left(\frac{g_{m2}}{C_2}\right)+\left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)} \tag{6.5}$$

Here the presence of s^2 term in the numerator of equation 6.5 makes it clear that the filter implementation shown in Figure 68 is a High Pass filter.

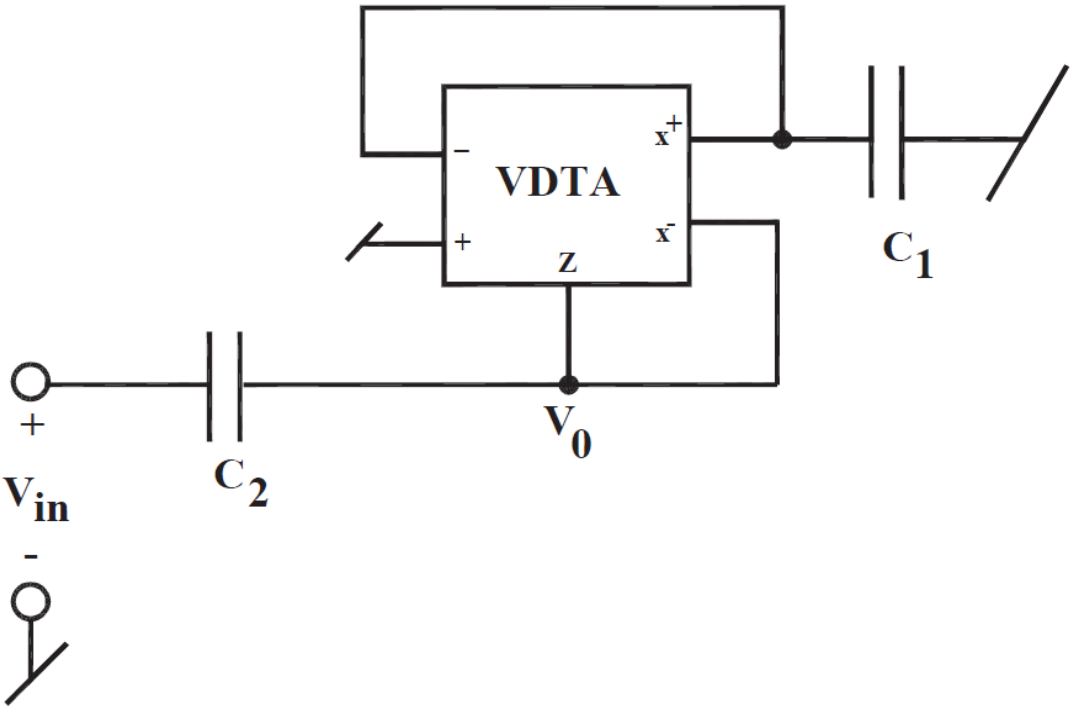

Figure 68 : High Pass Filter using Parallel R-L Impedance [6]

SIMULATION RESULTS:

For the simulation of R-L Impedance, the structure of VDTA shown in Figure 2 is used. The simulation is done on PSPICE using 0.18µm TSMC CMOS process parameters. The aspect ratios for the PMOS and NMOS transistor are given in Table 1. Supply voltages used for providing the biasing for the given circuit are $+V_{DD} = -V_{SS} = 0.9$ volts. The value of the capacitance is chosen [6] to be 0.01 nF and the values of transconductances are chosen to be

$g_{m1}=g_{m2}$= 631.7 µA/V and for this purpose the biasing currents are chosen [6] to be $I_{B1} = I_{B2} = I_{B3} = I_{B4}$ = 150 µA.

For the purpose of simulation of High Pass filter using R-L Impedance the structure of VDTA used, aspect ratios used, biasing currents, values of transconductances and biasing voltages are same as described above in case of R-L impedance. Here the values of capacitances chosen are C_1=0.02 nF and C_2=0.01 nF.

The circuit used for the simulation of R-L Impedance in PSPICE software is given in Figure 69. The graph showing the impedance of R-L Impedance with the frequency is given in Figure 70. The value of impedance is found to be 1.55 kΩ beyond 1 MHz and it is 17.388 Ω at the lower frequencies.

The circuit used for the simulation of the High Pass Filter in PSPICE software is given in Figure 71. The frequency response of the High Pass Filter is given in Figure 72 and the cutoff frequency is found to be 1.595 MHz.

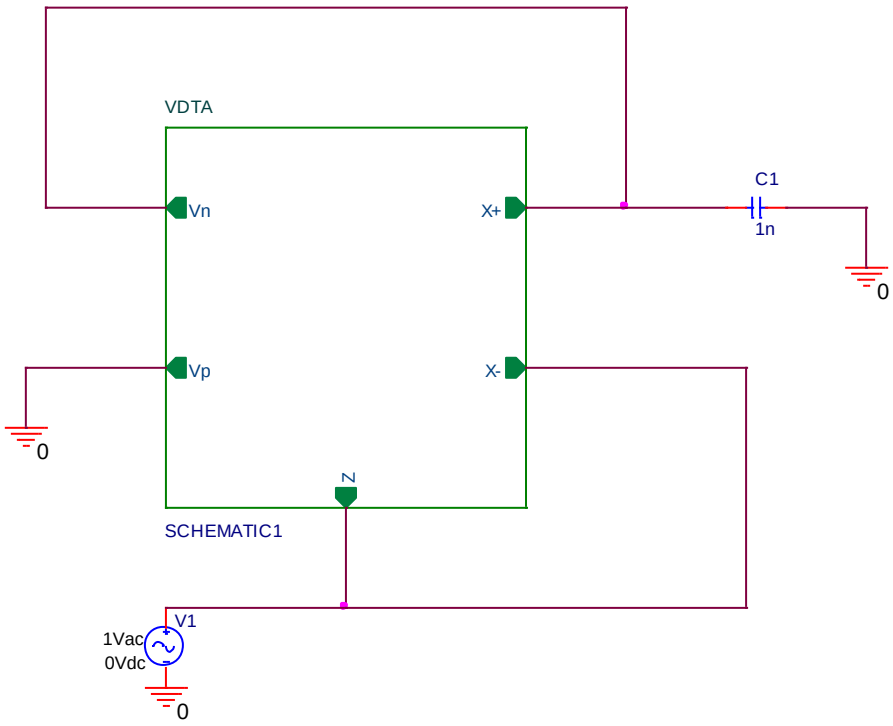

Figure 69 : PSPICE circuit diagram of R-L Impedance

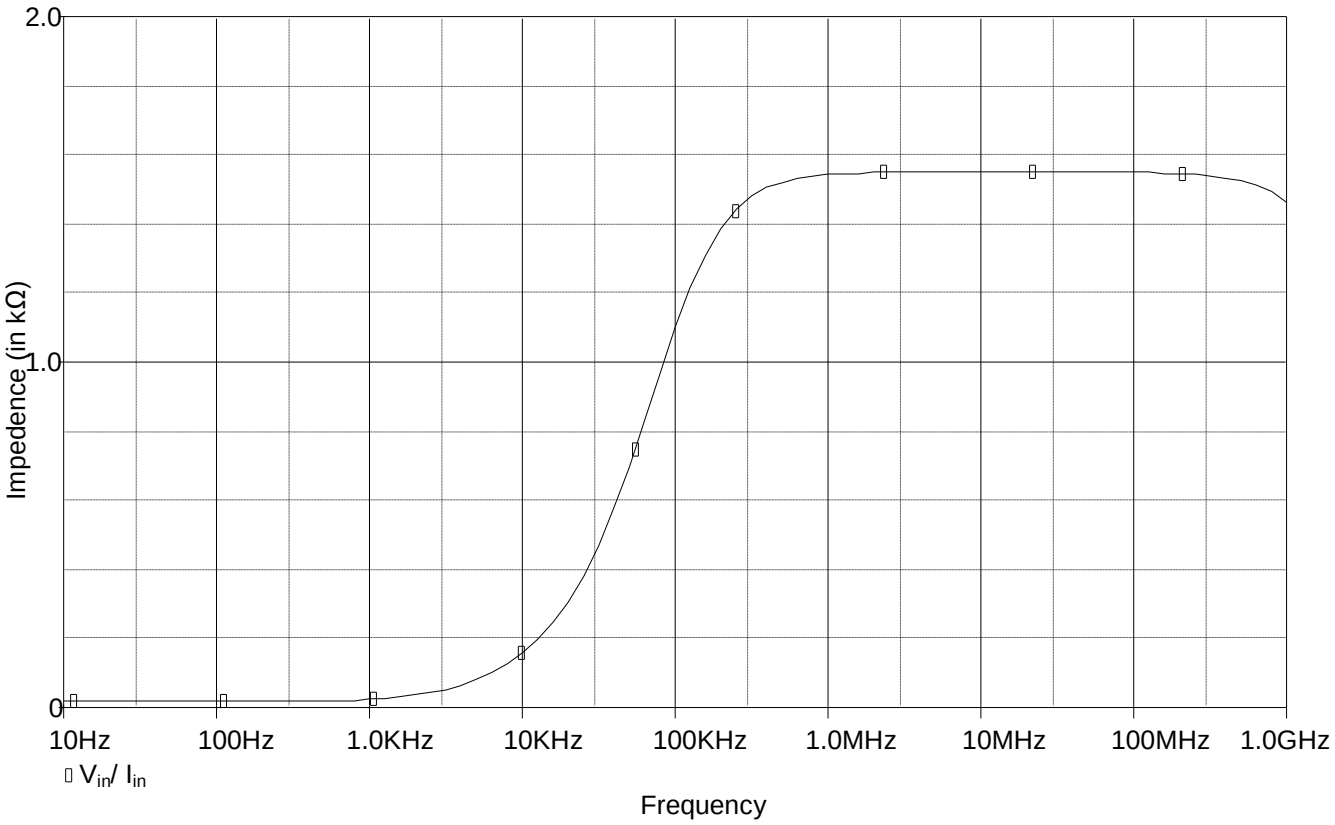

Figure 70 : Variation of Impedance with frequency for R-L Circuit

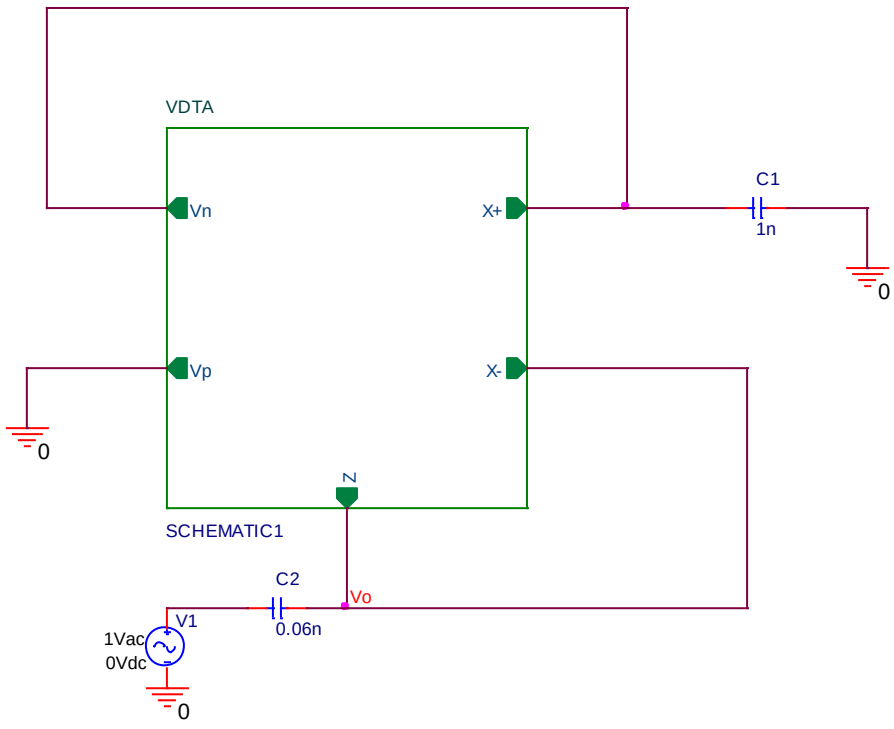

Figure 71 : PSPICE circuit diagram High Pass Filter using R-L Impedance

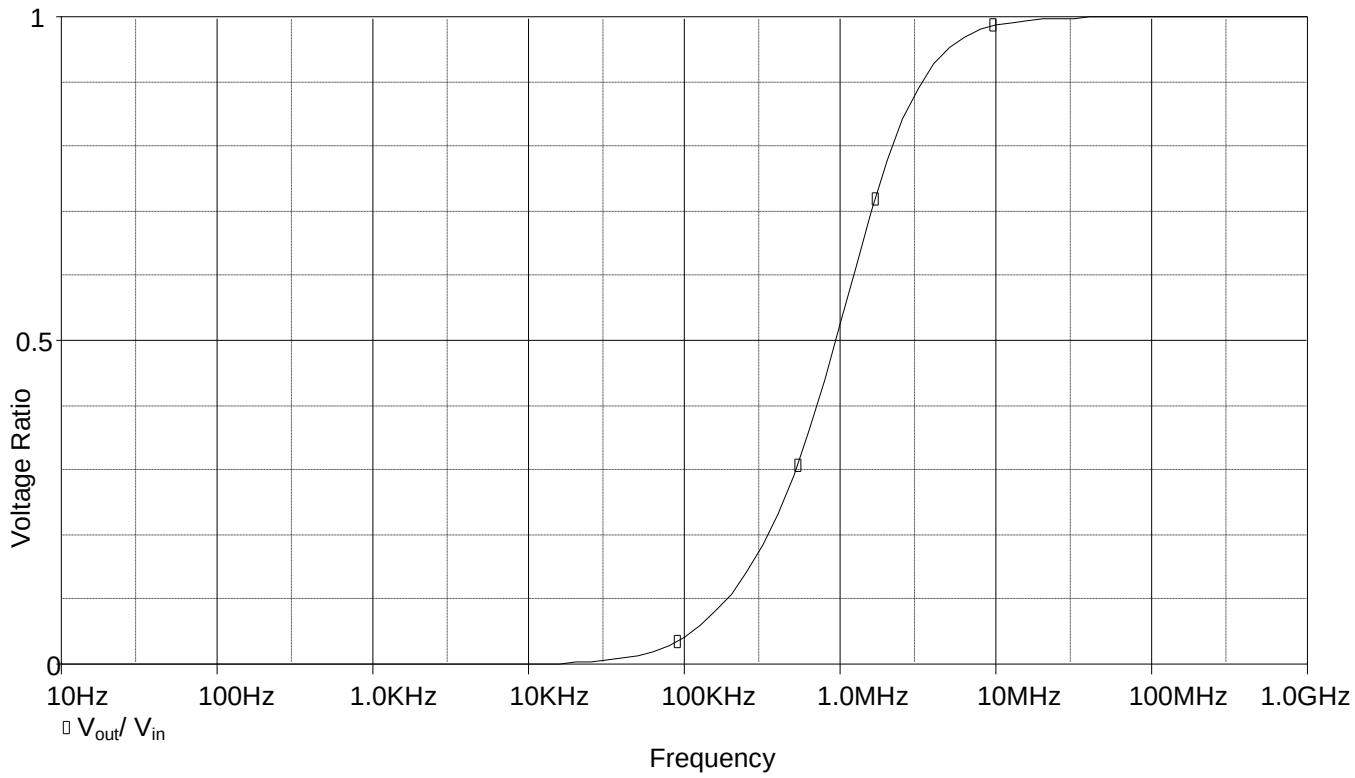

Figure 72 : Frequency Response of High Pass Filter using R-L Impedance

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CHAPTER 7

CONCLUSION

In this thesis, Voltage Differencing Transconductance Amplifier has been simulated at 0.18 µm CMOS technology and simulation results for its DC and AC characteristics have been presented. The topology of VDTA is very simple and it uses a very small number of transistors as compared to other building blocks. The frequency response of VDTA indicates its suitability for the high frequency applications. Also the supply voltage used is ±0.9 V which makes it suitable for the low voltage applications. Seven topologies of filters using VDTA out of which some also use 0.35 µm CMOS technology have been simulated and presented. The number of passive elements used in various topologies of filters required very few passive components which result in reduction in size and power consumption.

A Quadrature Oscillator has also been simulated using two VDTAs and three capacitors. The simulation results are given in the report. A parallel R-L impedance has also been simulated using one VDTA and one grounded capacitor. The circuit proves to be a very advantageous circuit in the way that it uses only single passive component and it also shows electronic tunability of the inductance. This R-L filter is further used in the simulation of a High Pass filter which again require only two capacitors. Simulation results that are obtained after the simulation of the circuits in PSPICE are close to the theoretical results obtained in case of all the applications presented in the report.

Thus, VDTA proves to be an active block which can be used in diversely many applications and due to presence of two different transconductances which can be varied by varying biasing currents, it provides independent electronic tunability for different parameters of different applications like independent tunability of natural frequency and bandwith in case of filters, the condition of oscillation and frequency of oscillation in case of filters etc.

APPENDIX A

TSMC 0.18 µm CMOS process parameters used for the Simulations in PSPICE are given below.

NMOS

LEVEL = 7
VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.354505 K1 = 0.5733393 K2= 3.177172E-3 K3 = 27.3563303 K3B = -10 W0 = 2.341477E-5 NLX = 1.906617E-7 DVT0W = 0 DVT1W = 0 DVT2W= 0 DVT0 = 1.6751718 DVT1 = 0.4282625 DVT2= 0.036004 U0 = 327.3736992 UA= 4.52726E-11 UB= 4.46532E-19 UC= -4.74051E-11 VSAT= 8.785346E4 A0 = 1.6897405 AGS= 0.2908676 B0= -8.224961E-9 B1= -1E-7 KETA= 0.021238 A1 = 8.00349E-4 A2= 1 RDSW= 105 PRWG = 0.5 PRWB= -0.2 WR = 1 WINT = 0 LINT = 1.351737E-8 XL = -2E-8 XW = -1E-8 DWG = 1.610448E-9 DWB = -5.108595E-9 VOFF = -0.0652968 NFACTOR = 2.4901845 CIT= 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 0.0231564 ETAB = -0.058499 DSUB = 0.9467118 PCLM = 0.8512348 PDIBLC1 = 0.0929526 PDIBLC2 = 0.01 PDIBLCB = -0.1 DROUT = 0.5224026 PSCBE1 = 7.979323E10 PSCBE2 = 1.522921E-9 PVAG = 0.01 DELTA = 0.01 RSH = 6.8 MOBMO = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2= 0.022 UA1 = 4.31E-9 UB1= -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL= 0 WLN= 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN= 1 LW = 0 LWN= 1 LWL= 0 CAPMOD = 2 XPART = 0.5 CGDO= 7.7E-10 CGSO = 7.7E-10 CGBO = 1E-12 CJ = 1.010083E-3 PB = 0.7344298 MJ = 0.3565066 CJSW = 2.441707E-10 PBSW = 0.8005503 MJSW = 0.1327842 CJSWG = 3.3E-10 PBSWG= 0.8005503 MJSWG = 0.1327842 CF = 0 PVTH0 = 1.307195E-3 PRDSW= -5 PK2= -1.022757E-3 WKETA = -4.466285E-4 LKETA = -9.715157E-3 PU0 = 12.2704847 PUA = 4.421816E-11 PUB = 0 PVSAT = 1.707461E3 PETA0 = 1E-4 PKETA = 2.348777E-3.

PMOS

LEVEL = 7
VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH= 4.1589E17 VTH0 = -0.4120614 K1 = 0.5590154 K2 = 0.0353896 K3 = 0 K3B= 7.3774572 W0 = 1E-6 NLX = 1.103367E-7 DVT0W = 0 DVT1W= 0 DVT2W= 0 DVT0 = 0.4301522 DVT1= 0.2156888 DVT2 = 0.1 U0= 128.7704538 UA = 1.908676E-9 UB= 1.686179E-21 UC = -9.31329E-11 VSAT= 1.658944E5 A0

= 1.6076505 AGS = 0.3740519 B0= 1.711294E-6 B1 = 4.946873E-6 KETA = 0.0210951 A1= 0.0244939 A2 = 1
RDSW = 127.0442882 PRWG= 0.5 PRWB= -0.5 WR= 1 WINT= 5.428484E-10 LINT = 2.468805E-8 XL= -2E-8 XW = -1E-8 DWG = -2.453074E-8 DWB = 6.408778E-9 VOFF = -0.0974174 NFACTOR = 1.9740447 CIT = 0 CDSC = 2.4E-4 CDSCD= 0 CDSC = 0 ETA0 = 0.1847491 ETAB = -0.2531172 DSUB = 1.5 PCLM = 4.8842961 PDIBLC1 = 0.0156227 PDIBLC2 = 0.1 PDIBLCB = -1E-3 DROUT = 0 PSCBE1 = 1.733878E9 PSCBE2 = 5.002842E-10 PVAG = 15 DELTA= 0.01 RSH = 7.7 MOBMOD= 1 PRT = 0 UTE = -1.5 KT1= -0.11 KT1L= 0 KT2 = 0.022 UA1 = 4.31E-9 UB1= -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL= 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN= 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO= 7.11E-10 CGSO= 7.11E-10 CGBO = 1E-12 CJ = 1.179334E-3 PB = 0.8545261 MJ = 0.4117753 CJSW= 2.215877E-10 PBSW = 0.6162997 MJSW = 0.2678074 CJSWG= 4.22E-10 PBSWG= 0.6162997 MJSWG = 0.2678074 CF = 0 PVTH0 = 2.283319E-3 PRDSW= 5.6431992 PK2 = 2.813503E-3 WKETA = 2.438158E-3 LKETA = -0.0116078 PU0 = -2.2514581 PUA = 7.62392E-11 PUB = 4.502298E-24 PVSAT = -50 PETA0 = 1E-4 PKETA = -1.047892E-4.

APPENDIX B

TSMC 0.35 µm CMOS process parameters used for the Simulations in PSPICE are given below.

NMOS

LEVEL=3
TOX=7.9E-9 NSUB=1E17 GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA =0 UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4 VMAX = 8.309444E4 KAPPA=0.2574081 RSH=0.0559398 NFS=1E12 TPG=1XJ=3E-7 LD = 3.162278E-11 WD=7.04672E-8 CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3 PB=0.9758533 MJ=0.3448504CJSW=3.777852E-10 MJSW=0.3508721

PMOS

LEVEL =3
TOX=7.9E-9 NSUB=1E17 GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA =0 UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774 KP=6.733755E-5 VMAX=1.181551E5KAPPA=1.5 RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD =5.000001E-13 WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10 CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5 CJSW=4.813504E-10 MJSW=0.5.