LEAKAGE POWER REDUCTION IN DYNAMIC DCVSL USING ONOFIC APPROACH

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BY

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CERTIFICATE

This is to certify that the dissertation titled **"Leakage Power Reduction in Dynamic DCVSL using ONOFIC Approach"** is a bonafide record of work done by **Jayesh Trivedi, Roll No. 2K15/VLS/08** at **Delhi Technological University** for partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI and Embedded Systems Engineering. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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ABSTRACT

Differential logic styles have been becoming popular over conventional CMOS logic because of they promise lower power consumption and high computational speed. DCVSL promises the advantages of both traditional CMOS logic and pseudo NMOS logic thus offering high speed area effective rail to rail swing logic option. The dynamic DCVSL logic family has been explored and leakage power and delay has been considered. Various dynamic versions of DCVSL logic have been introduced and their leakage power and delay have been studied.

Leakage power is an important issue in dynamic circuits and a leakage control technique (LECTOR) has been explored in context of two variations of dynamic DCVSL structures. The LECTOR technique is applied to other variants of dynamic DCVSL structures and performance in terms of leakage power dissipation, propagation delay time, power delay product, transistor number is examined.

In this thesis, a relatively new leakage reduction technique known as ONOFIC technique has been successfully proposed in various DCVSL structures. Various performance related parameters and transistor count has been reported.

This thesis includes relative performance comparison of dynamic DCVSL structures in their conventional format and with the introduction of LECTOR and ONOFIC approach.

The effectiveness and functionality of all dynamic DCVSL structures and proposed architectures are confirmed through intensive simulations on Symica Design Environment. The structures were implemented using Symica Design Environment (Symica DE) using 90 nm PTM model technology at 1.2V to analyse the variation in leakage power and delay.

Chapter 1

Introduction

(1.1) Topic Overview

Power dissipation in a MOS circuit can be classified in two types- Static Power Dissipation and Dynamic Power Dissipation. Dynamic Power Dissipation can be due to charging or discharging of capacitance (dominant at higher frequency) and power dissipation due to short-circuit current. While Static Power Dissipation can be due to Static Current and due to Leakage Currents. This is shown in Fig. 1.

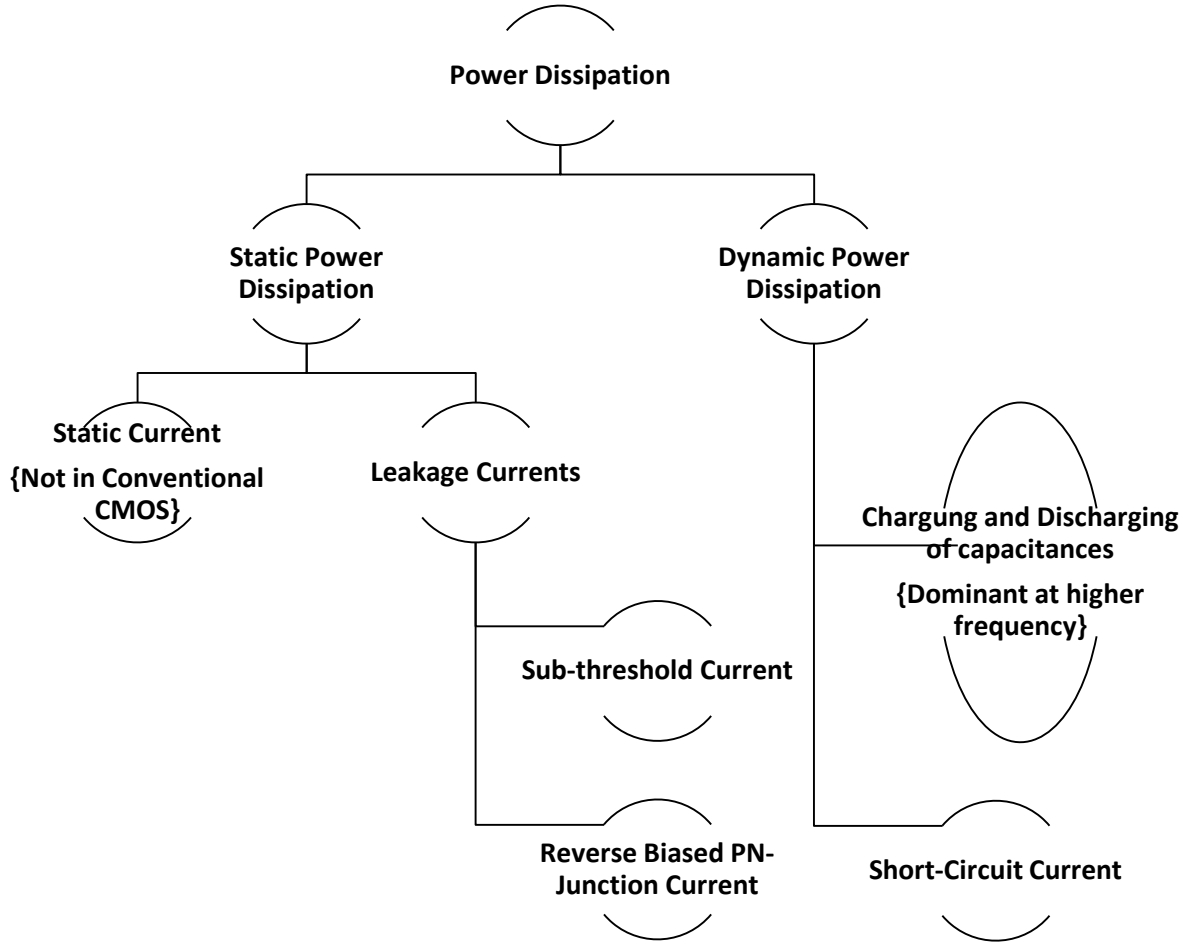

Figure 1: Power Dissipation in VLSI Circuits

With the technology scaling in nanometre regime, static power consumption (due to leakage current) has become a major concern. Along with technology scaling down (for higher operating speeds and higher device density) leakage current which constitutes reverse biased PN- junction current and sub-threshold current are becoming significant. This is shown in Fig. 2.

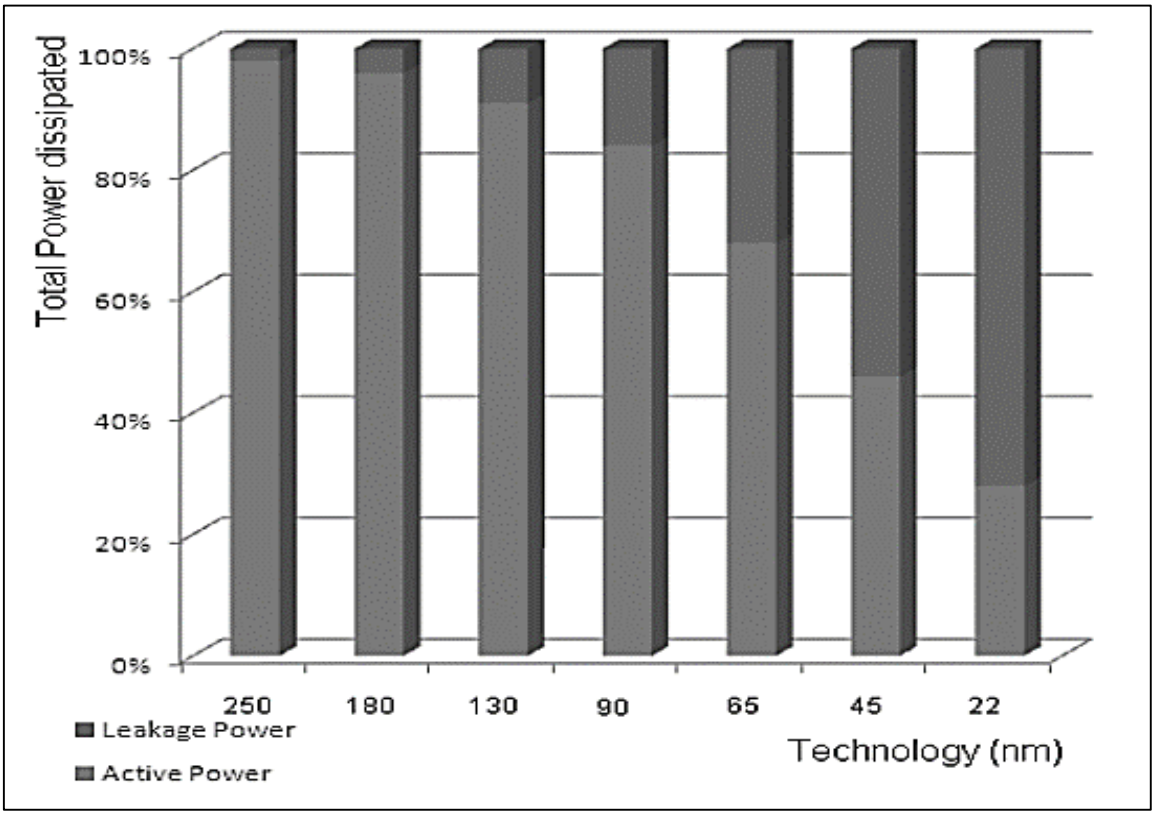

Figure 2: Leakage Power significance at lower technology nodes [5]

In recent years, differential logic design has emerged as a very promising alternative to standard CMOS logic. Several differential logic styles have been reported in the literature, since including the differential cascode voltage switch logic (DCVSL)**.** There are many factors that make the differential logic design more preferable compared to the standard CMOS design:

- High fan-in complex gates can be implemented using a single differential tree network. This results in reduced delay time and lower transistor count.
- Only NMOS devices are requires to perform a logic function which results in reduction in input loads.
- The differential circuits are preferred for self-timed architectures since the existence of complementary outputs makes the evaluation phase easily detectable.

Differential Cascode Voltage Switch Logic (DCVSL) is a widely known logic design style. DCVSL style offers several advantages over the conventional static CMOS logic design approach. The number of transistors required to implement an 'N' input logic in CMOS logic is '2N'. Subsequently, immense no. of transistors will be required to implement a complex logic.

Ratioed logic style seems an alternative to decrease the required transistor count. However, it suffers from a major drawback of static power dissipation (due to static current) and reduced logic swing because the pull up transistor is 'ON' unconditionally.

A potential ratioed logic style that totally eliminates static currents and offers rail-to-rail swing can be created. The potential logic design style combines two concepts: *differential logic* and *positive feedback*. A differential structure receives complementary inputs and generates complementary outputs. Through positive feedback mechanism the load device gets turned off when not required. *Differential Cascode Voltage Switch Logic* (or DCVSL) is an example of such a logic family.

Lot of literature on Leakage power reduction in CMOS logic approach has been already present. But study on leakage power aspect of DCVSL family specially their dynamic versions (due to the obvious advantages of dynamic circuits) is somewhat limited till date. Therefore, a sincere attempt has been made to explore various DCVSL structures and their performance is explored.

As the LECTOR technique has been investigated on only two variants of dynamic DCVSL structures [3], other variants are also examined. Also a relatively new leakage power reduction approach i.e. ONOFIC approach has been implemented in these structures.

The effectiveness and functionality of all dynamic DCVSL structures and proposed architectures are confirmed through intensive simulations on Symica Design Environment. The structures were implemented using Symica Design Environment (Symica DE) using 90 nm PTM model technology at 1.2V at a temperature of 27^{o}C.

(1.2) Thesis structure

Chapter 1 introduces the topic, discusses about the importance of DCVSL logic and gives thesis structure.

Chapter 2 starts with the details of the Differential Cascode Voltage Switch Logic (DCVSL), it shows the basic structure of DCVSL circuit and explains its operation. Apart from that, dynamic DCVSL is introduced and concept of leakage is explained.

Chapter 3 introduces various types of dynamic DCVSL structures, explains their operation. Simulation results has been reported to justify the functionality and various performance parameters has provided.

Chapter 4 introduces various dynamic DCVSL structures with LECTOR power reduction approach. Simulation results have been provided to justify the functionality and various performance related results are mentioned.

Chapter 5 explains a relatively new leakage power reduction ONOFIC approach, which promises a better power-delay product. This approach has been proposed in dynamic DCVSL structures. Detail study of each of these DCVSL structures, with parameters such as leakage power consumption, temperature, delay, PDP and transistor count has been done. Simulation results have been provided to justify the functionality and various performance related results are mentioned.

Chapter 6 provides relative performance analysis of conventional, LECTOR incorporated and proposed ONOFIC incorporated dynamic DCVSL structures.

Chapter 7 concludes the overall work done in this thesis. This chapter ends the thesis work.

Chapter 2

Differential Cascode Voltage Switch Logic

Differential Cascode Voltage Switch Logic (DCVSL) is a widely known differential logic design style. It offers several advantages courtesy of being a differential logic design - higher fan-in complex gates implementation by using a single differential tree network, requirement of only NMOS devices to perform a logic function, and are more preferable for self-timed architectures. DCVSL offers several other advantages which are mentioned in section (2.2).

(2.1) Operation

DCVSL logic design style is an amalgamation of two concepts: *differential logic* and *positive feedback*. Here, a differential gate is fed with complementary inputs which in turn generates complementary outputs. Positive feedback mechanism ensures that the load device gets turned off when not required.

A basic DCVSL logic gate is given in Fig. 3. The pull-down networks namely *PDN1* and *PDN2* are implemented using NMOS transistors only and are mutually exclusive (i.e. both are never 'ON' at the same time). This ensures such that the desired logic function and its complement are simultaneously realized by providing complementary inputs.

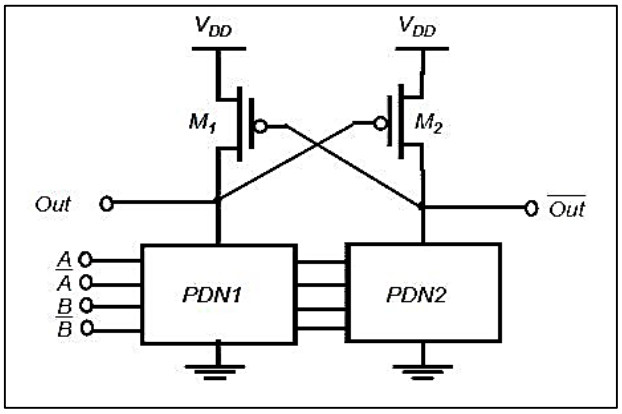

Figure 3: Basic DCVSL Circuit [1]

- We begin by assuming Out and $\overline{Out}$ at logic '1' and '0' respectively.
- Now, suppose that an input combination is applied such that *PDN1* turns 'ON' thus providing a discharge path to *Out*. $\overline{Out}$ which is at '0' initially is keeping M_1 turned 'ON'. This creates a contention between M_1 and *PDN1* and Out is not able to discharge completely during this phase. But, still discharging of *Out* starts at slower pace.

- As soon as *Out* falls below (V_{DD} -$|V_{TP}|$), M_2 turns 'ON' which is driven by *Out*. Now, charging path is provided by M_2 to $\overline{Out}$. As *PDN1* and *PDN2* are mutually exclusive and implement differential logic functions, therefore *PDN2* is 'OFF'. Thus, there is no discharge path for $\overline{Out}$. This results in M_2 successfully charging $\overline{Out}$ to $V_{DD.}$

- As $\overline{Out}$ exceeds (V_{DD}-V_T), M_1 turns off resulting in cutting of path between V_{DD} and ground. This eliminates any static power loss. Now *PDN1* can efficiently complete the discharge of *Out*. Eventually, both *Out* and $\overline{Out}$ attain correct logic state.

By sharing of common transistors among the two differential pull-down networks *PDN1* and *PDN2* (for realizing complex logic), implementation overhead can be reduced. The DCVSL circuit shows rail-to-rail swing, and there is an elimination of static power dissipation: in steady state, none of the stacked pull-down networks and load devices is in conduction mode simultaneously.

However, the DCVSL circuit is still ratioed logic and sizing of pull up transistors relatively to pull down devices critically affects both the performance as well as the functionality of the circuit.

(2.2) Advantages of DCVSL

i. High fan-in complex gates can be implemented using a single differential tree network. This results in reduced delay time and lower transistor count.

ii. Only NMOS devices are requires to perform a logic function which results in reduction in input loads.

iii. The differential circuits are preferred for self-timed architectures since the existence of complementary outputs makes the evaluation phase easily detectable.

iv. There is a speed improvement in DCVSL circuits similar to that in case of domino circuits due to the reduction in the parasitic capacitances at the output nodes (logic function is implemented using only pull down network which consists only NMOS transistors that provides a quicker response.

v. Static power consumption is reduced by employing positive feedback which is provided by two cross-connected PMOS transistors that ensures that pull up transistor and PDN are never on simultaneously.
vi. DCVSL allows sharing of the common transistors by both the PDN networks for implementing complex circuits. Provision for sharing of transistors by both PDN and requirement of only PDNs to implement logic function ensures significant saving of chip area when compared to conventional CMOS logic.

vii. Generations of output and its complement results in the elimination of inverting stage. This eliminates the problem of clock skew.
For E.g.: Using an inverter to complement the *Clock* signal when *Clock* and $\overline{Clock}$ are needed simultaneously will result in clock skew problem due to delay introduced by inverter.

(2.3) Disadvantages of DCVSL

Every design style has its merits and drawbacks and the case with DCVSL is no different. The advantages mentioned in section (2.2) comes at a price.

i. Additional area overhead.

ii. Additional complexity associated with differential logic networks which involve complementary signals.

iii. To add to above disadvantages, during transition, state of contention exists for a period of time when both PMOS and PDN are turned 'ON' simultaneously, producing a short circuit path. Therefore, it might be possible that static DCVSL circuit consume slightly more power than conventional CMOS circuits because of the dependency of charging and discharging times on the Turn-ON and the Turn-OFF paths within the DCVSL tree and these are usually asymmetrical.
iv. Asymmetry in rise and fall times resulting in extension of period of time for which current flows through the latch of the DCVSL circuit during the transient state increases the power dissipation.

Therefore, there is a need to employ circuit level power reduction techniques in the mainly very useful DCVSL circuits to achieve faster circuits while consuming less power.

(2.4) Dynamic DCVSL

The basic dynamic version of DCVSL is shown in Fig. 4 (b) along with basic version of static DCVSL. The dynamic DCVSL consists of two complementary PDNs and has positive feedback which is in the form of the two cross-coupled PMOS PUTs.

Operation

- When CLK signal is low, OUT and $\overline{OUT}$ are pre-charged to V_{DD}. This is called pre-charge phase.

- When CLK rises to logic high, NMOS pull down logic tree evaluates to its true and complementary output state on the basis of assertion of complimentary input signals. Positive feedback ensures proper switching of the logic gate which is being applied to PMOS PUTs (M3 and M4).

- M5 and M6 are used to improve the performance of the dynamic DCVSL gate.

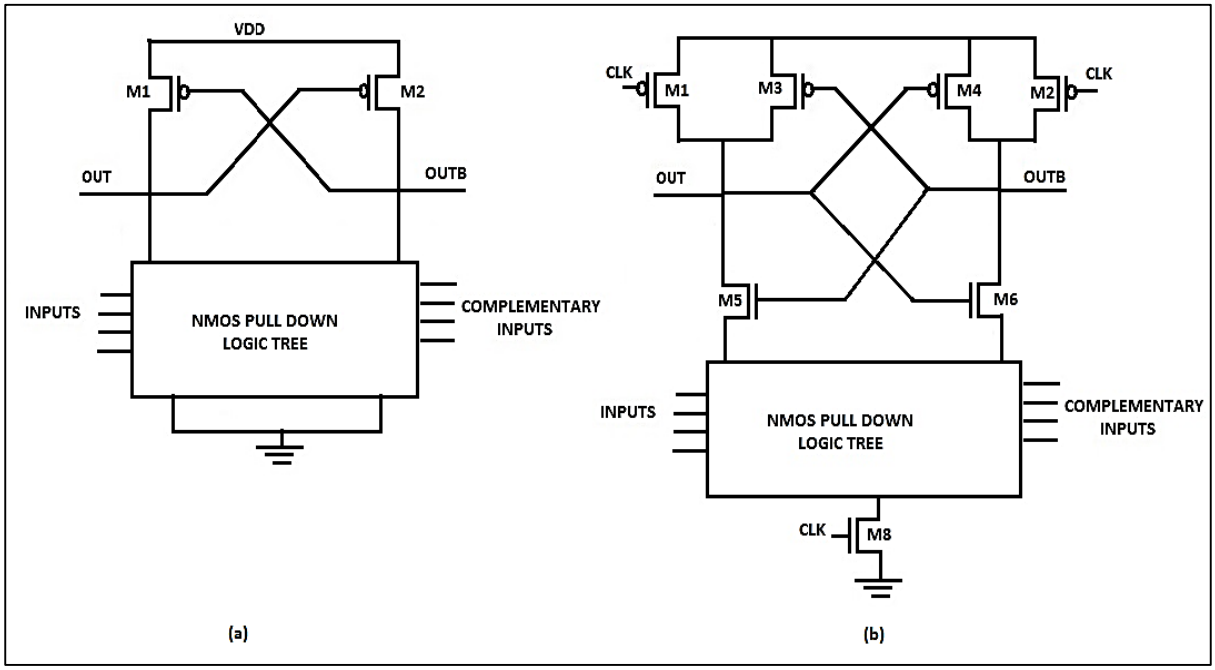

Figure 4: DCVSL: (a) Static version, and (b) Dynamic version [4]

Advantages of Dynamic DCVSL over Static DCVSL

- Dynamic DCVSL has an upper hand over static DCVSL in field of power dissipation. It consumes relatively lesser power over static DCVSL counterpart.

- The state of contention during switching as in case of static DCVSL does not occur in Dynamic DCVSL.

Explanation:

- In static DCVSL, Gate terminal of either of the PUTs is at logic '1' and other one is at logic '0' since they are connected to complementary output nodes. Referring Fig. 4 (a) consider the case when OUT has to switch from '1' to '0' ($\overline{OUT}$ has to make a switch from '0' to '1'). On assertion of inputs, PDN1 turns ON and trying to discharge OUT. But this task of discharging is made difficult by PUT1 which is still 'ON' since $\overline{OUT}$ is at logic '0'. This results in a state of conflict between PUT1 and PDN1. Consequence of contention is the undesired static power dissipation within that duration.

- In case of dynamic DCVSL, OUT and $\overline{OUT}$ are both charged to V_{DD} during pre-charge cycle. This implies that PUT1 and PUT2 both are initially 'OFF'. In the evaluation stage, PUTs get turned ON conditionally (depending upon input combination). Thus, the problem of contention is eliminated.

(2.5) Idea of Leakage in Dynamic DCVSL

Leakage Power is the power dissipation which is due to currents which flows in those portions of DCVSL logic which are logically 'OFF'. These current comprises of sub-threshold current and reverse biased PN-Junction current which ideally should not flow. This leakage current contributes in static power dissipation. There is no problem of contention, hence there is no static current in dynamic DCVSL.

This leakage current is dependent on input combinations. Consider the case when certain input combinations cause OUT at logic '1' and $\overline{OUT}$ at logic '0' in dynamic DCVSL shown in Fig. 4 (b) during evaluation (i.e. when CLK='1'). In this case, the current flowing from OUT node to ground and from V_{DD} to $\overline{OUT}$ constitute leakage current. In this thesis work leakage current during evaluation phase is only reported since during evaluation both OUT and $\overline{OUT}$ are at logic '1'and M8 is OFF. Thus, there is no path from OUT and $\overline{OUT}$ to ground.

In the thesis work, 2-input XOR with inputs 'A' and 'B' is used as a test circuit for performance analysis. In evaluation phase CLK= '1', therefore, before the active CLK edge inputs 'A' and 'B' should be stable. Since, leakage has been reported for evaluation phase in this thesis work, therefore 4 cases are possible as shown in Table 1.

Table 1

Leakage current is input dependent in Dynamic DCVSL: 4 cases possible in evaluation case (CLK= '1') for 2- input XOR

A	B
0	0
0	1
1	0
1	1

Chapter 3

Dynamic DCVSL Variations

Introduction

The basic dynamic DCVSL introduced in section (2.4) provides the basis for several alternative differential CMOS logic design styles. Although these circuits have evolved from the DCVSL structure, they have features that make them unique. In subsequent sections, various dynamic DCVSL variations are described and simulations are carried out to verify their functionality and performance in terms leakage power and delay is observed.

(3.1) Sample-Set Differential Logic (SSDL)

Sample-Set Differential Logic (SSDL) is a clocked differential logic style circuit. Its schematic is shown in Fig. 5. It consists of the differential logic tree, three sample transistors, a latching sense amplifier, two buffers, and two optional resistors as can be seen from the schematic.

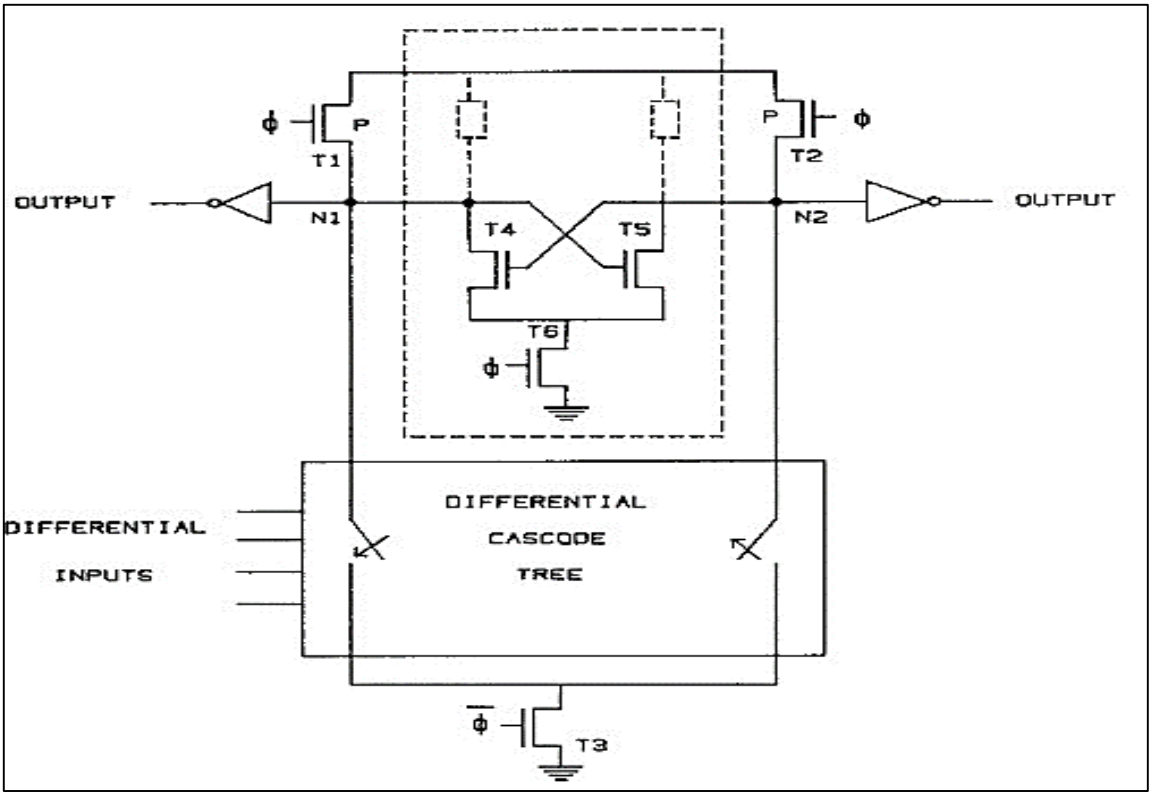

Figure 5: SSDL Schematic [6]

***Operation*:**

The operation of SSDL circuit consists of a sample and a set phase.

- During the sample phase (precharge phase), clock$\overline{\Phi}$ is high and thus NMOS T3 and PMOS T1 and T2 are turned 'ON' creating a path exists from either N1 or N2 to ground through one side of the differential tree only determined by the input combination. Thus, either node N1 or N2 will be at *VDD* or at a voltage less than *VDD.*
- In the next phase of operation i.e. the set phase (evaluation phase), where T1, T2, and T3 are 'OFF' and the portion consisting of the sense amplifier is turned 'ON' through T6. Now, the node (N1 or N2) at the lower voltage will get discharged quickly to ground. This discharge is rapid because of the large driving capabilities of the sense amplifier.
- There is a speed advantage of SSDL circuits over the domino and DCVSL circuits. This occurs because the node (N1 or N2), which has to go low, goes low through a large transistor (T4 or T5) in the SSDL circuit in contrast to a series connection of many transistors in the domino and DCVSL circuits. The differential gain of the sense amplifier used also assists this transition. In other words, the complexity of the logic circuitry has no effect to play on the evaluation time. This makes the idea of SSDL design very attractive to achieve high circuit density.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 6 shows the schematic for 2-input XOR with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

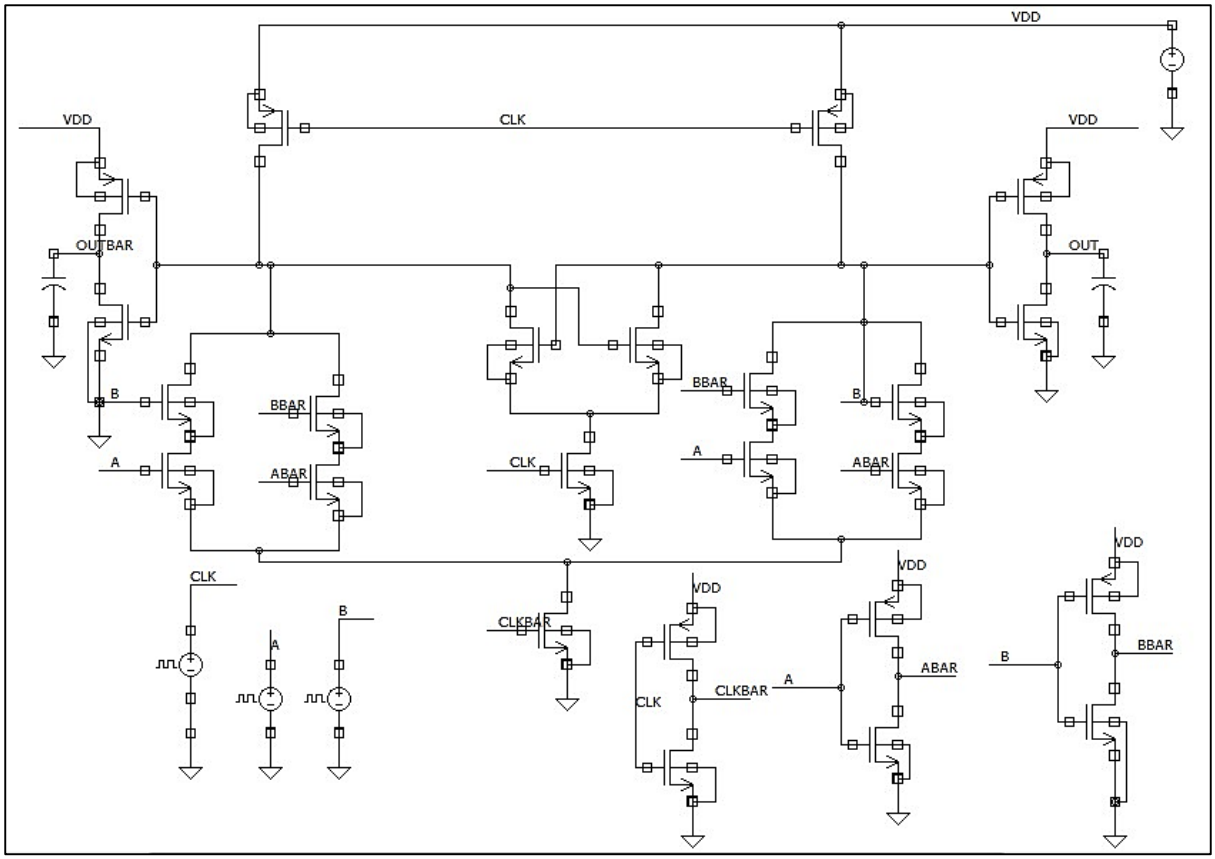

Figure 6: 2-input XOR using SSDL architecture

***Simulation Results*:**

Fig. 7 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 2 specifies simulation settings for 'CLK', 'A' and 'B' where the different parameter definition is given below.

v1- Initial Voltage Level at t=0ns

v2- Voltage Level after delay of td

per- Period of the pulse

td- Delay after which pulse makes first transition from v1 to v2

tr- Rise Time of the pulse

tf- Fall Time of the pulse

pw- Pulse Width of the pulse

Table 2:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	0
v2	1.2	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

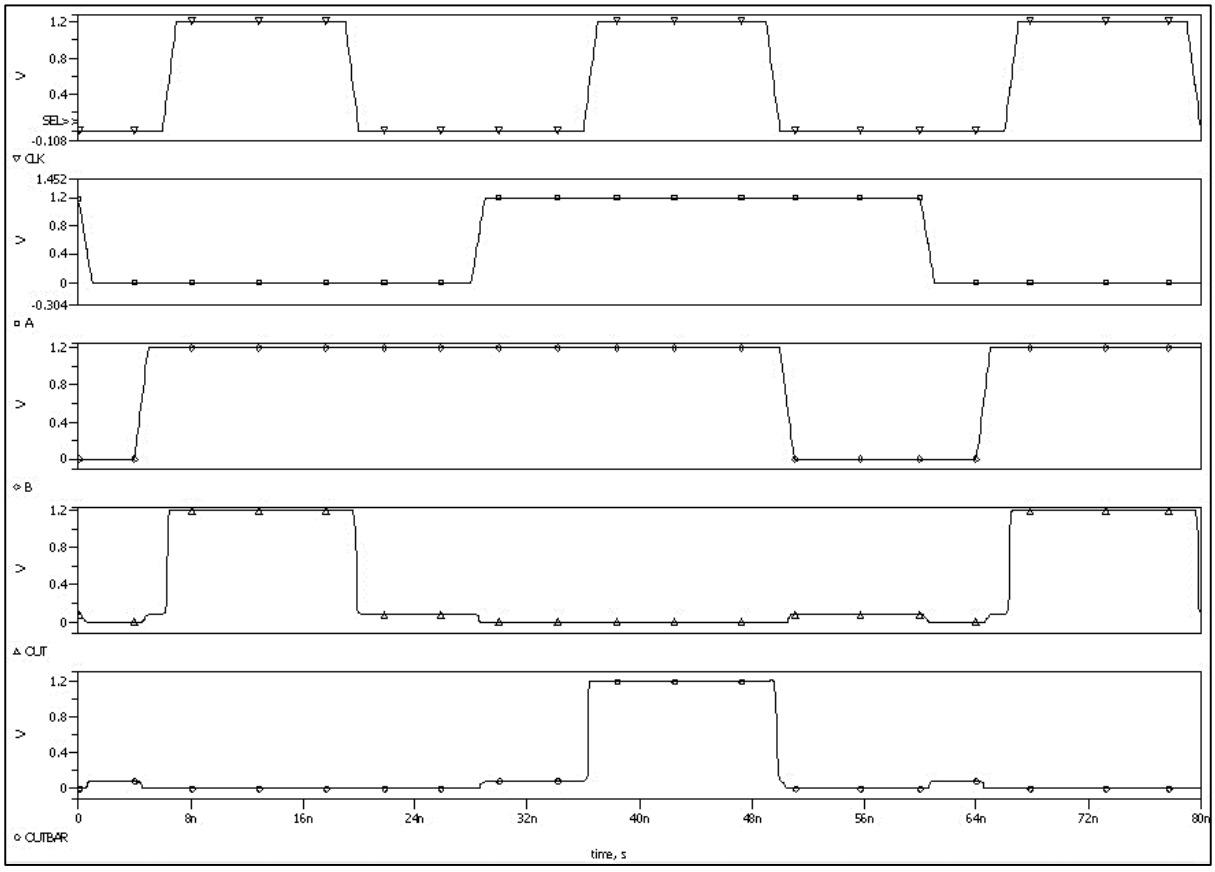

Figure 7: Simulation Output for 2-input XOR using SSDL

***Performance Measurement*:**

- Table 3 shows the leakage power for the 2-input XOR SSDL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 3:

Leakage Power in SSDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*0*	*0*	_	_
1	**0**	**0**	**0**	**1**	**3.86**	**4.632**
1	**0**	**1**	**1**	**0**	**3.756**	**4.5072**
1	**1**	**0**	**1**	**0**	**3.894**	**4.6782**
1	**1**	**1**	**0**	**1**	**3.848**	**4.6176**

- The delay performance of the 2-input XOR using SSDL structure is summarized in Table 4. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= 0 in SSDL. Therefore, delay will be '0' if OUT remains '0' in evaluation phase.

Table 4:

Delay in SSDL

CLK	A	B	OUT	Delay (ps)
0	X	X	0	_
1	**0**	**0**	0	0
1	**0**	**1**	1	74.242
1	**1**	**0**	1	76.853
1	**1**	**1**	0	0

(3.2) Modified Sample-Set Differential Logic (MSSDL)

The obvious problem with the SSDL circuit as described in Section 3.1 is the presence of a DC current flow path between the power supply (V_{DD}) and ground during the precharge phase resulting in power dissipation during that period. But this is an important aspect to the design, reducing voltage on one of the latch nodes which is required for proper operation during the evaluation phase.

Thus, a variation in the SSDL circuit is required (to prevent DC power dissipation). This feature is provided by **Modified Sample-Set Differential Logic (MSSDL)**. Its schematic is shown in Fig. 8. In this approach, static RAM cell, which is made up of two static inverters, replaces the dynamic latch. Extra clocking transistors M_{n4} and M_{n5} are introduced to control the DC current flow paths.

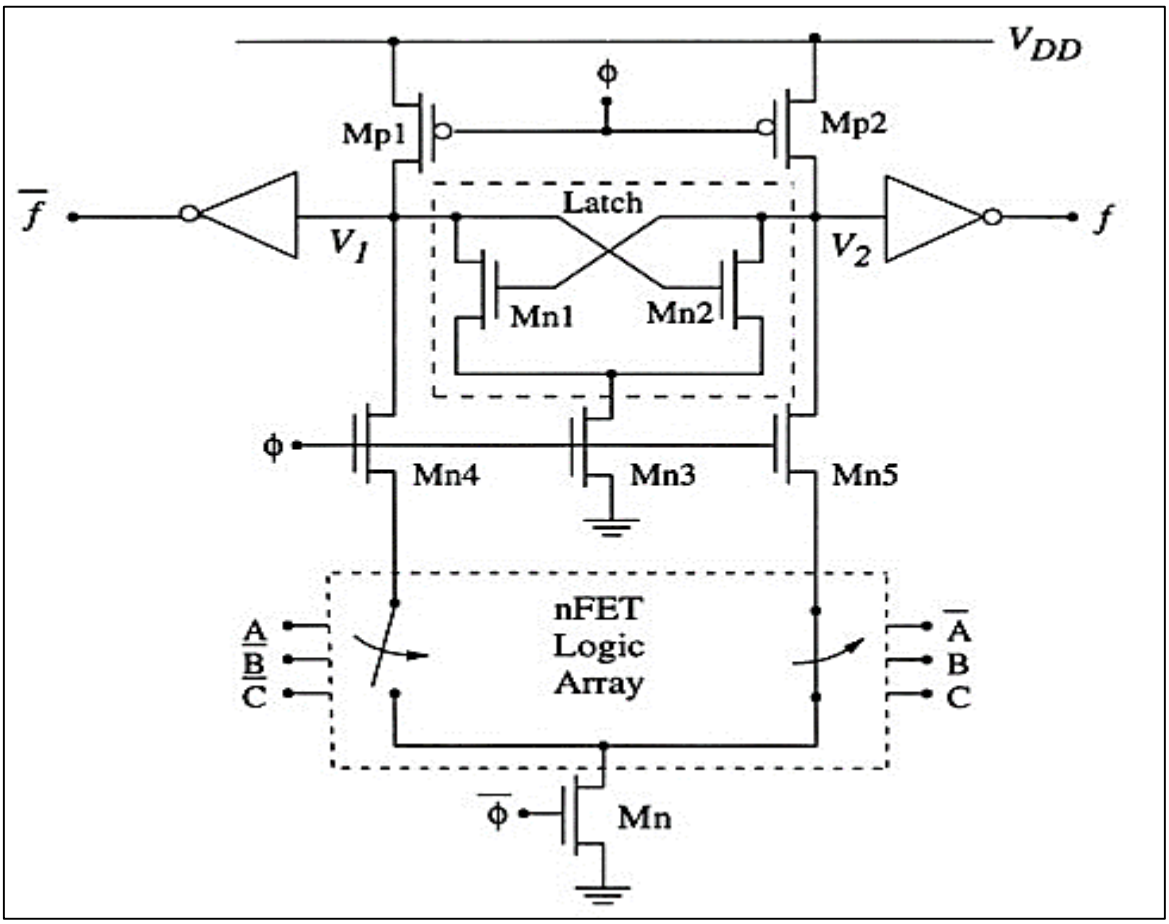

Figure 8: MSSDL Schematic [1]

***Operation*:**

- When ϕ = 0 (precharge phase), both the output nodes (V_1 and V_2) try to attain charge equal to V_{DD} which is not a stable state of the circuit.
- During this time, the logic array is disconnected from the circuit because of M_{n4} and $M_{n5.}$ In other words, the RAM will be in an unstable state.
- When the clock, ϕ makes a transition from '0' to '1', the logic tree switches into the circuit. The logic tree decides which side discharges to 0.
- Thus, the MSSDL circuit try to preserve the speed while lowering the power dissipation.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 9 shows the schematic for 2-input XOR with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

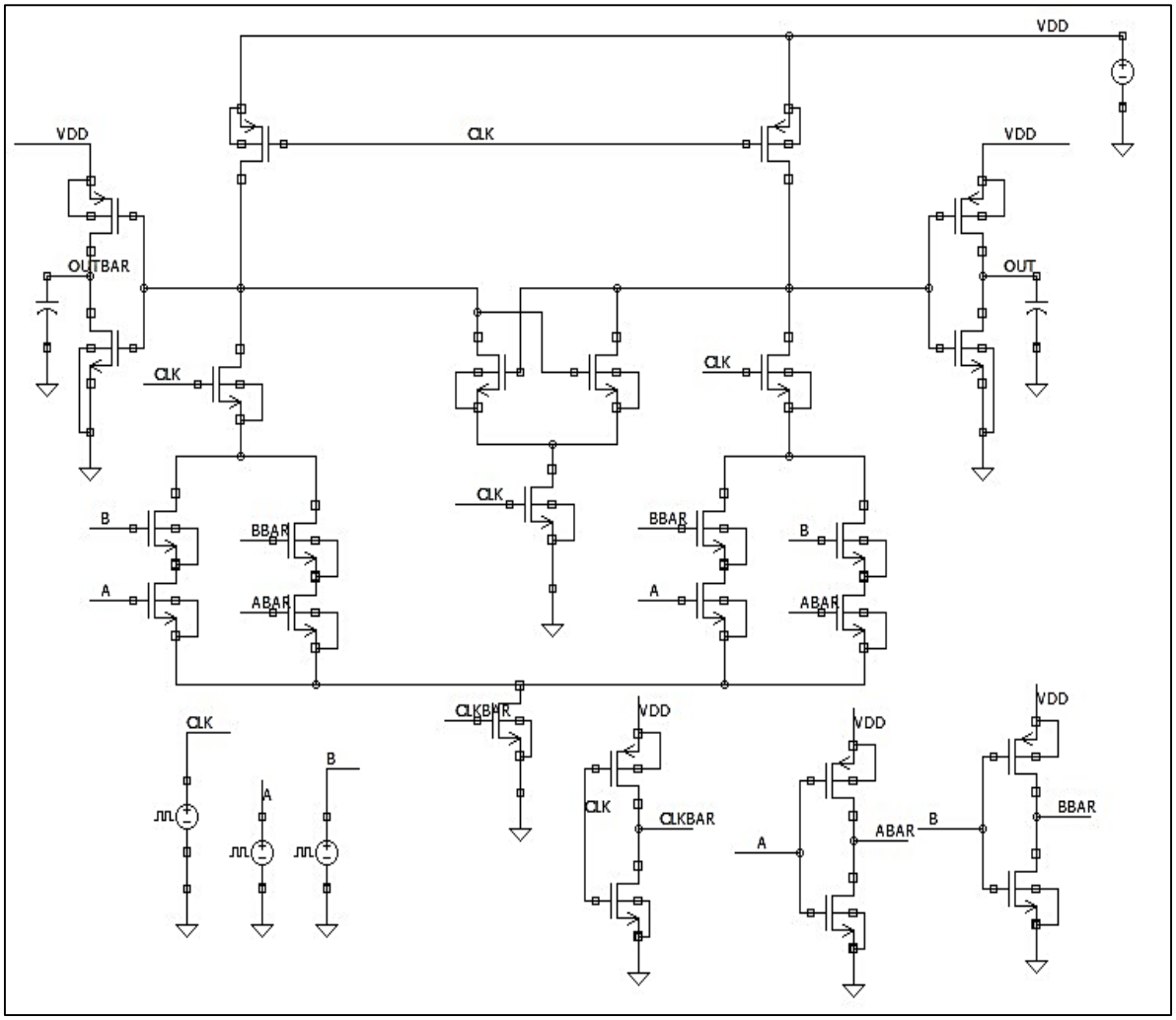

Figure 9: 2-input XOR using MSSDL architecture

***Simulation Results*:**

Fig. 10 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 5 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 5:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	0
v2	1.2	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

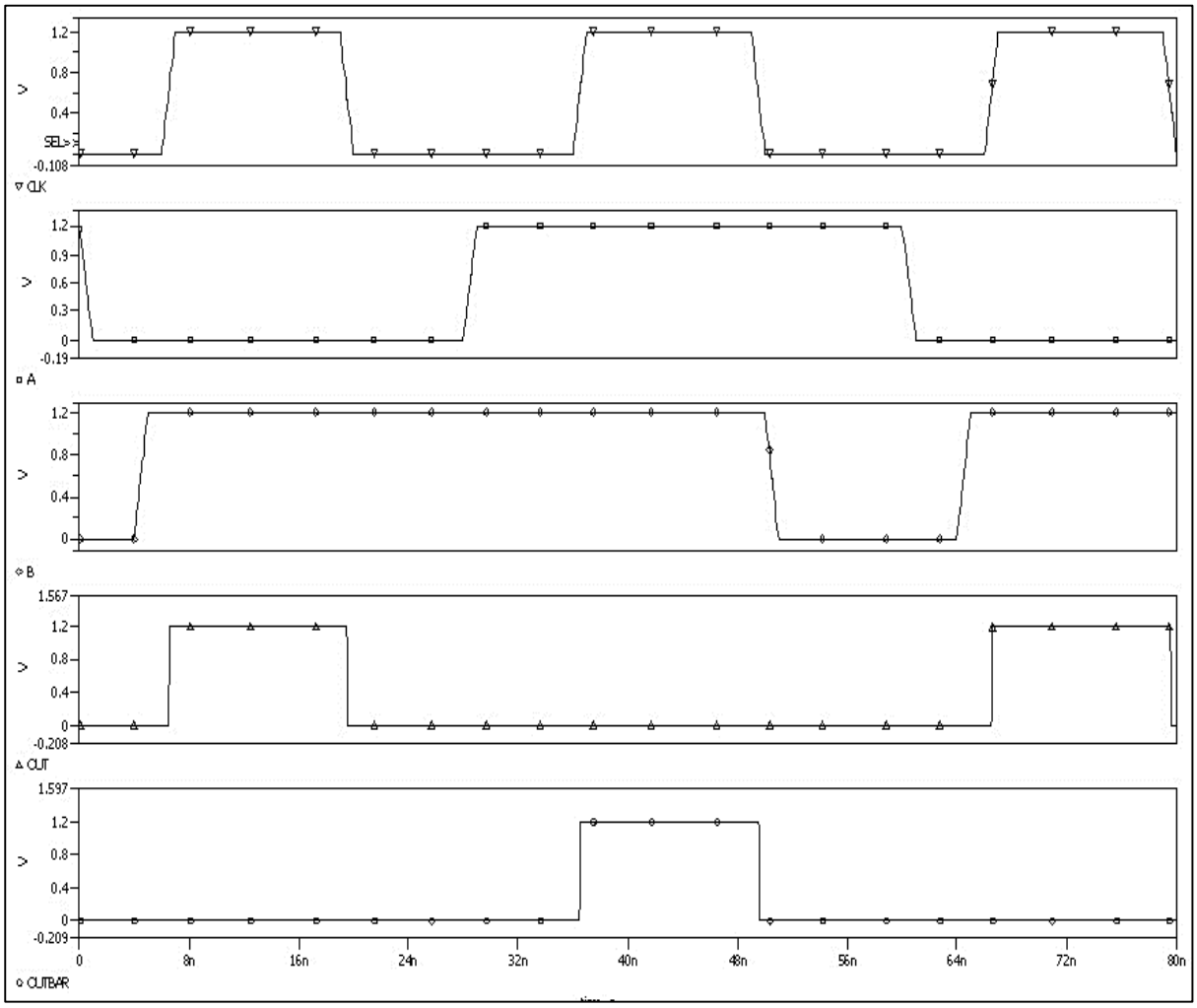

Figure 10: Simulation Output for 2-input XOR using MSSDL

***Performance Measurement*:**

- Table 6 shows the leakage power for the 2-input XOR MSSDL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 6:

Leakage Power in MSSDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*0*	*0*	_	_
1	**0**	**0**	**0**	**1**	**4.423**	**5.3076**
1	**0**	**1**	**1**	**0**	**4.791**	**5.7492**
1	**1**	**0**	**1**	**0**	**4.944**	**5.9328**
1	**1**	**1**	**0**	**1**	**4.45**	**5.340**

- The delay performance of the 2-input XOR using MSSDL structure is summarized in Table 7. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 0$ in MSSDL. Therefore, delay will be '0' if OUT remains '0' in evaluation phase.

Table 7:

Delay in MSSDL

CLK	A	B	OUT	Delay (ps)
0	X	X	0	_
1	**0**	**0**	0	0
1	**0**	**1**	1	18.026
1	**1**	**0**	1	18.054
1	**1**	**1**	0	0

(3.3) Enable/Disable CMOS Differential Logic (ECDL)

Enable/disable CMOS Differential Logic (ECDL) is another DCVSL variation. This design approach was developed to eliminate the static power dissipation problem in SSDL (eliminating the DC current flow path) and to reduce the transistor count. The general schematic of ECDL circuit is shown in Fig. 11.

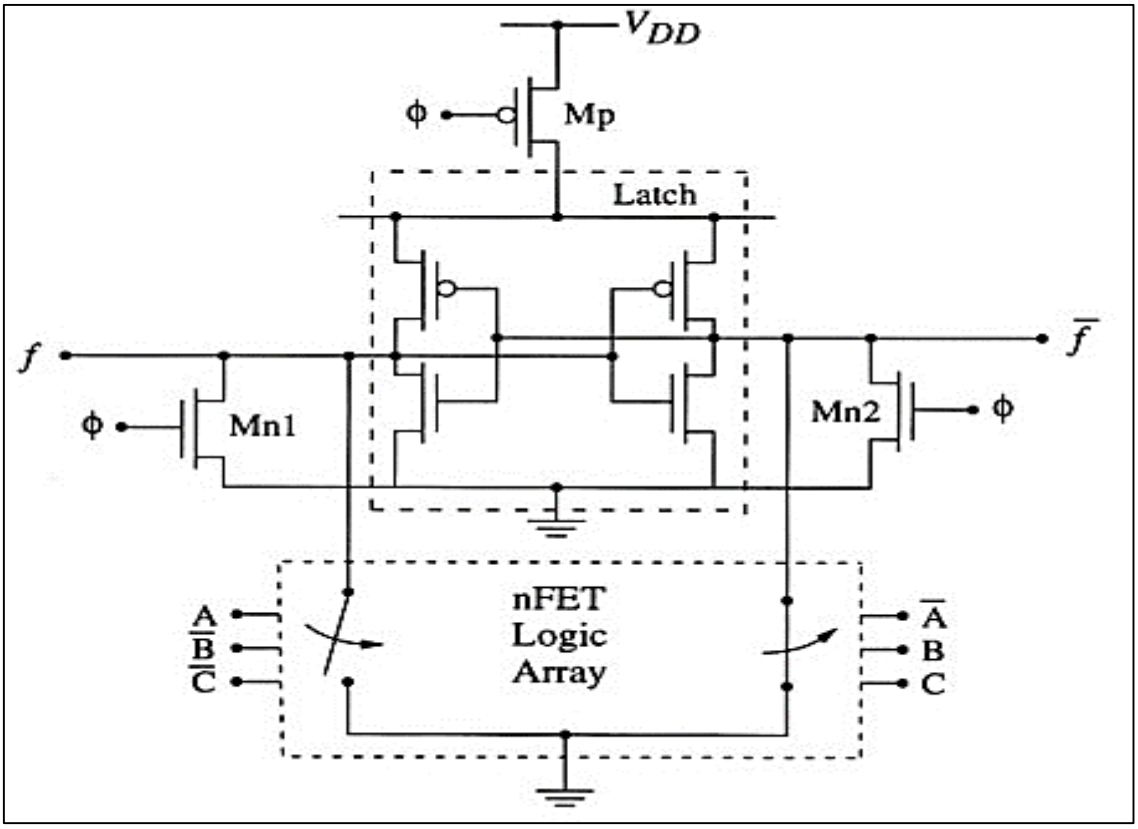

Figure 11: ECDL Schematic [1]

***Operation*:**

- The latching action is provided by a pair of cross-coupled static inverters which is basically an SRAM storage cell.
- The clock ϕ controls the precharge transistor M_p that connects the power supply V_{DD} to the latch.
- Two additional NMOS transistors M_{n1} and M_{n2} are included at the outputs to provide enable/disable feature.

- Let the clock $\phi = 1$ initially. This makes both M_{n1} and M_{n2} active, thus disabling the latch by making both output nodes as 0V i.e., resets the state of the circuit to ground.
- When the clock ϕ makes a transition to logic '0', transistors M_{n1} and M_{n2} gets turned 'OFF', allowing the output nodes to achieve other voltages. During this time, PMOS M_p conducts and supplies power to the latching circuit. Thus, the state of the logic array determines the state that the latch will settle in.
- The circuit eliminates the DC current flow path between the V_{DD} and ground, but the downside is that the circuit is designed to discharge the output nodes every half-cycle during the reset phase. This increases the dynamic power dissipation.
- In addition to the above drawback, the circuit relies on logic chains to discharge one of the output nodes, so that the RC delays may be a limiting factor.
- It has the advantage of being simple to design with reduced interconnect requirements. It also do not require inverted clock.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 12 shows the schematic for 2-input XOR with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

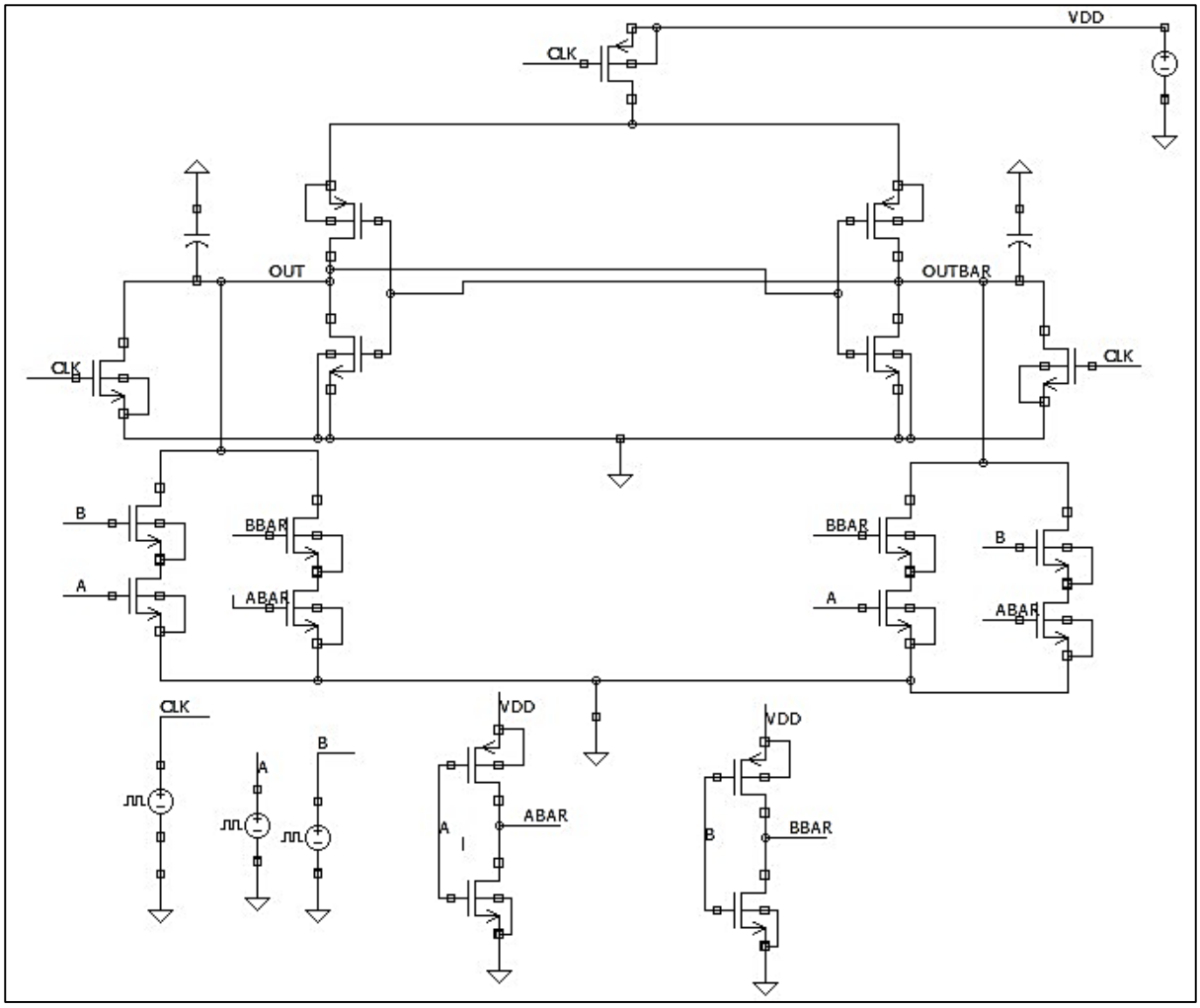

Figure 12: 2-input XOR using ECDL architecture

***Simulation Results*:**

Fig. 13 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 8 specifies simulation settings for 'CLK', 'A' and 'B.

Table 8:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	1.2	1.2	0
v2	0	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

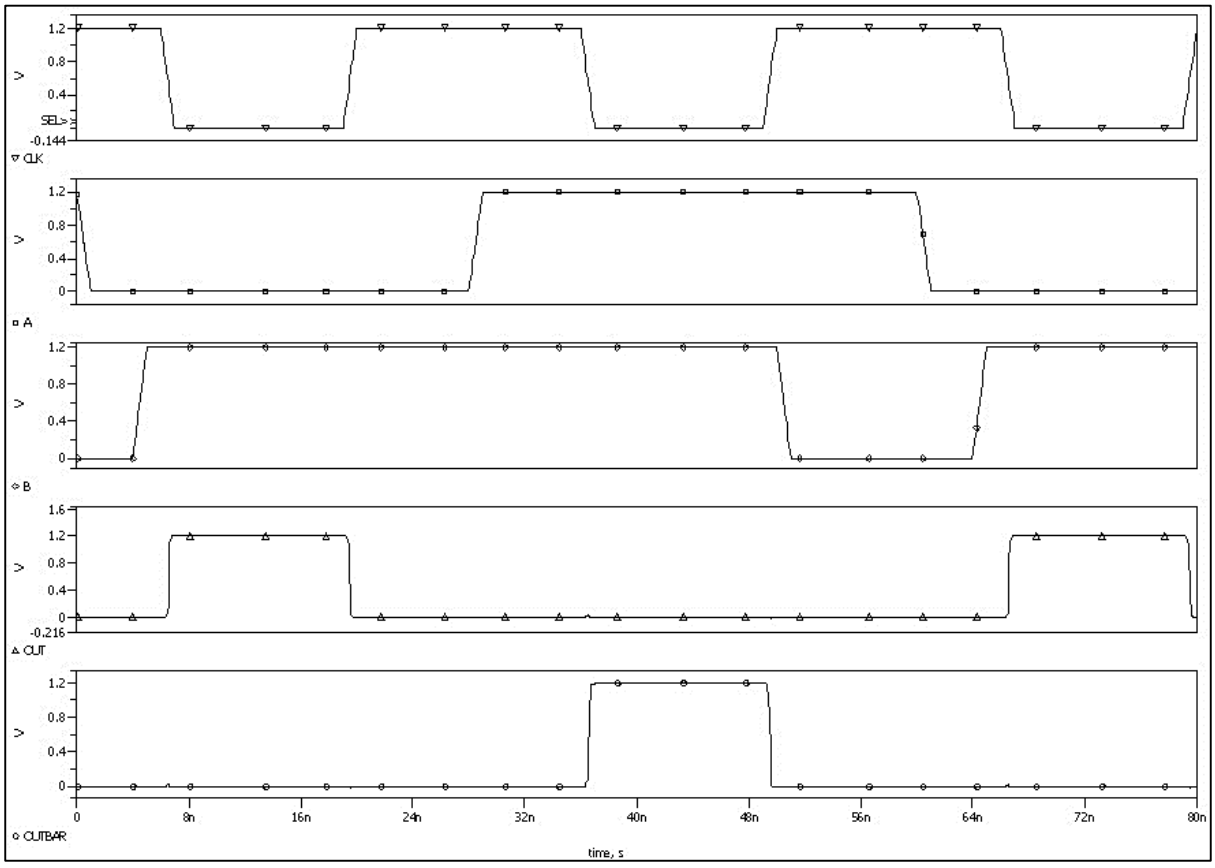

Figure 13: Simulation Output for 2-input XOR using ECDL

***Performance Measurement*:**

- Table 9 shows the leakage power for the 2-input XOR ECDL structure for various input combinations in enable phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 9:

Leakage Power in ECDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
1	*X*	*X*	*0*	*0*	_	_
0	**0**	**0**	**0**	**1**	**4.648**	**5.5776**
0	**0**	**1**	**1**	**0**	**3.95**	**4.74**
0	**1**	**0**	**1**	**0**	**4.529**	**5.4348**
0	**1**	**1**	**0**	**1**	**5.257**	**6.3084**

- The delay performance of the 2-input XOR using ECDL structure is summarized in Table 10. The input should be stable before the active edge of CLK (-ve edge) so that the OUT in enable stage is correct. In disable phase, OUT= $\overline{OUT} = 0$ in ECDL. Therefore, delay will be '0' if OUT remains '0' in enable phase.

Table 10:

Delay in ECDL

CLK	A	B	OUT	Delay (ps)
1	X	X	0	_
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**87.953**
0	**1**	**0**	**1**	**87.892**
0	**1**	**1**	**0**	**0**

(3.4) Differential Current Switch Logic (DCSL)

Differential Current Switch Logic (DCSL) is another variation of DCVSL that came into picture as a low-power approach to dual rail CMOS logic. Low power objective is met by limiting the voltage swings on internal nodes. Its drawback is that it requires a relatively high transistor count. Also the circuits are sensitive to circuit imbalances and noise. Different version of DCSL exist that offers trade-off in power and delay. Fig. 14 shows the schematic of one of DCSL version.

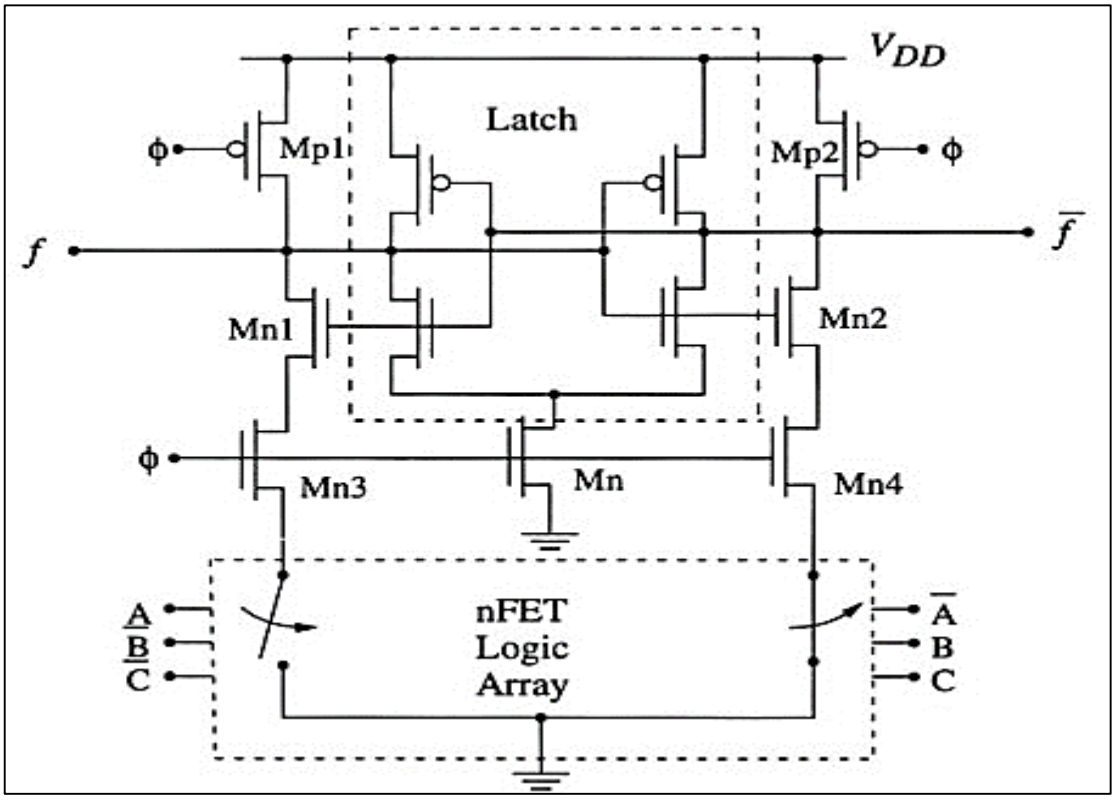

Figure 14: DCSL Schematic [1]

***Operation*:**

- There is a static latch in the centre made of cross-coupled invertors.
- Several clocking transistors have been added to the output nodes.
- M_{p1} and M_{p2} are precharge devices (governed by clock ϕ).
- M_n is a latch enable FET, and M_{n3} and M_{n4} are used to control the current between the latch and logic array. M_n, M_{n3} and M_{n4} are controlled by clock ϕ.

- M_{n1} and M_{n2} which are unique to this design and are controlled by the state of the latch. They help to limit the internal voltages which in turn reduces the power dissipation.
- Inverting clock is not required.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 15 shows the schematic for 2-input XOR with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

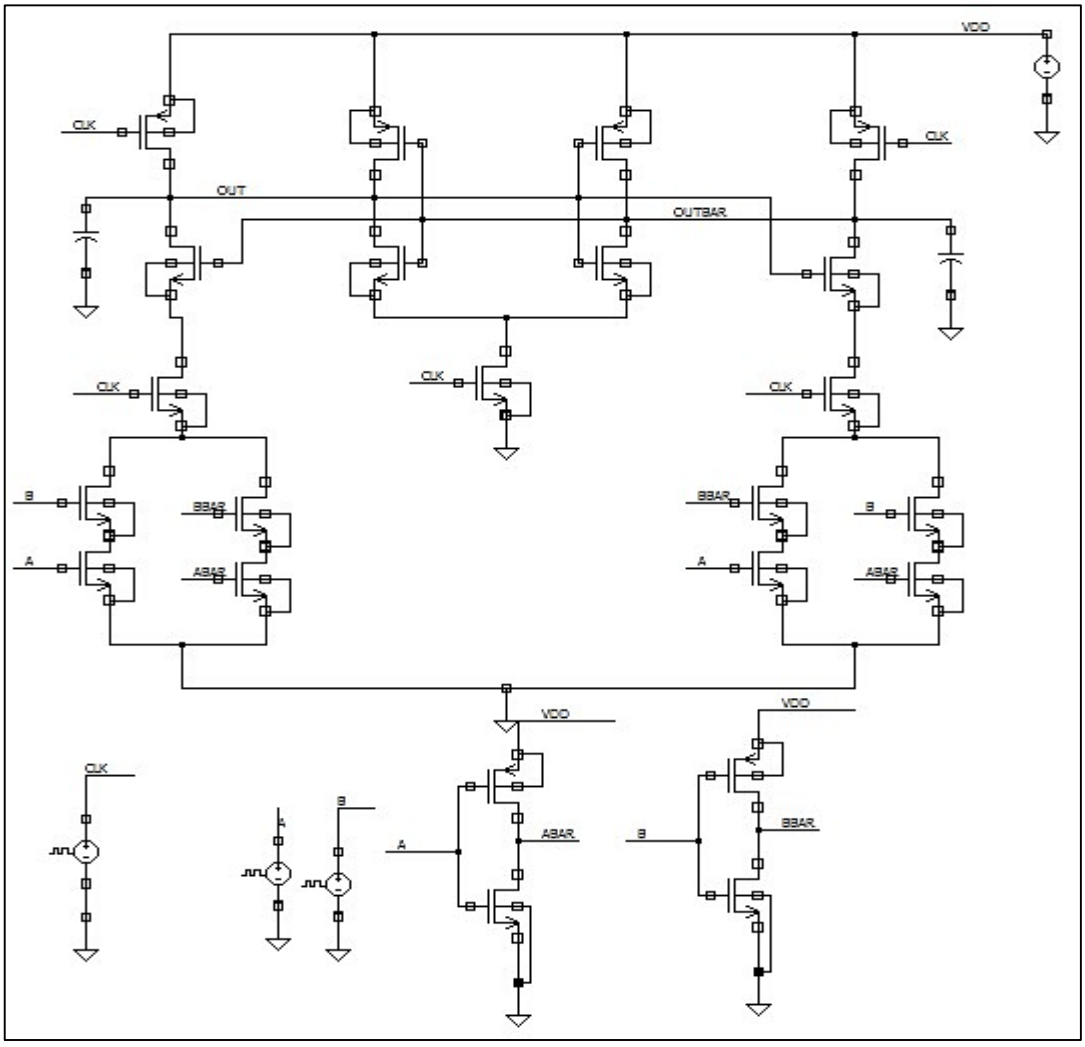

Figure 15: 2-input XOR using DCSL architecture

***Simulation Results*:**

Fig. 16 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 11 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 11:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

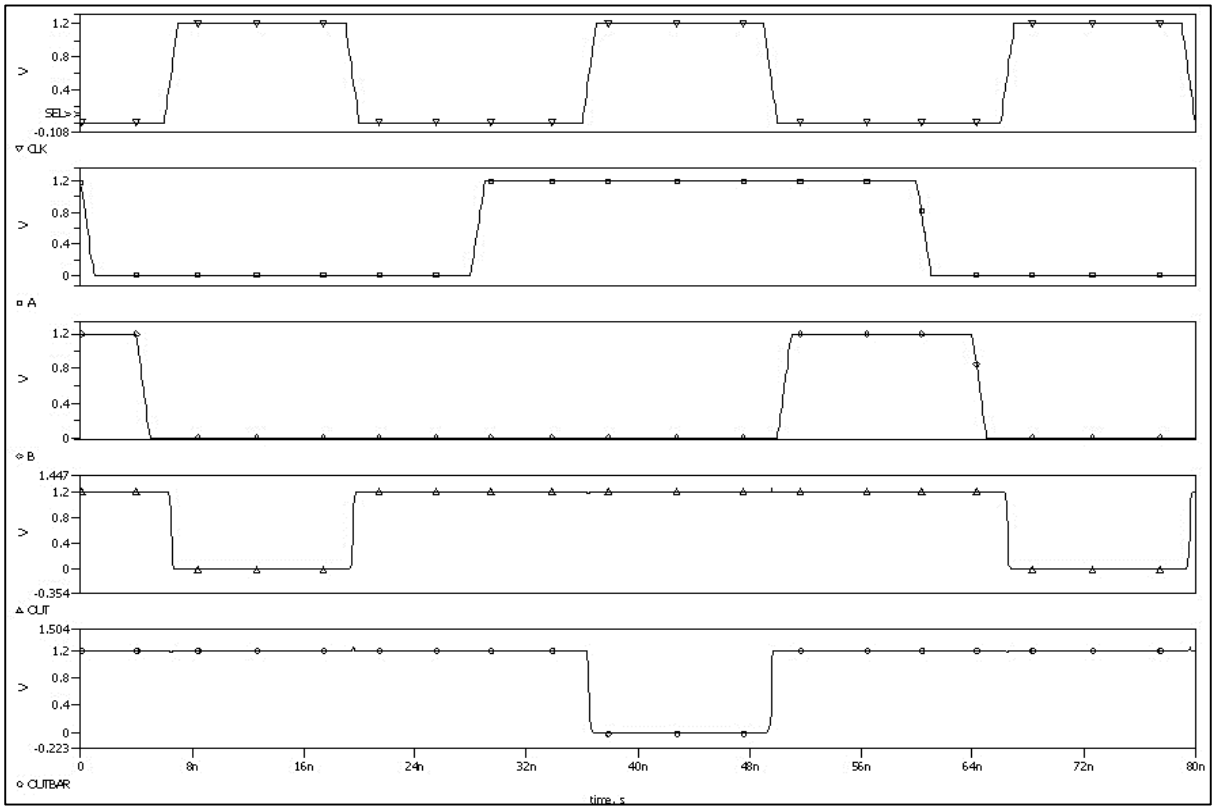

Figure 16: Simulation Output for 2-input XOR using DCSL

***Performance Measurement*:**

- Table 12 shows the leakage power for the 2-input XOR DCSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 12:

Leakage Power in DCSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**5.679**	**6.8148**
1	**0**	**1**	**1**	**0**	**6.201**	**7.4412**
1	**1**	**0**	**1**	**0**	**5.994**	**7.1928**
1	**1**	**1**	**0**	**1**	**5.542**	**6.6504**

- The delay performance of the 2-input XOR using DCSL structure is summarized in Table 13. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in DCSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 13:

Delay in DCSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**15.265**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**17.931**

(3.5) Enhanced Differential Cascode Voltage Switch Logic (EDCVSL)

Enhanced Differential Cascode Voltage Switch Logic (EDCVSL) as its name suggests is an improved version of dynamic DCVSL. EDCVSL circuits are basically have two versions. The two versions are called EDCVSL Type I and EDCVSL Type II. The two versions are shown in Fig. 17 and Fig. 18. In this thesis work, we have concentrated on EDCVSL Type II.

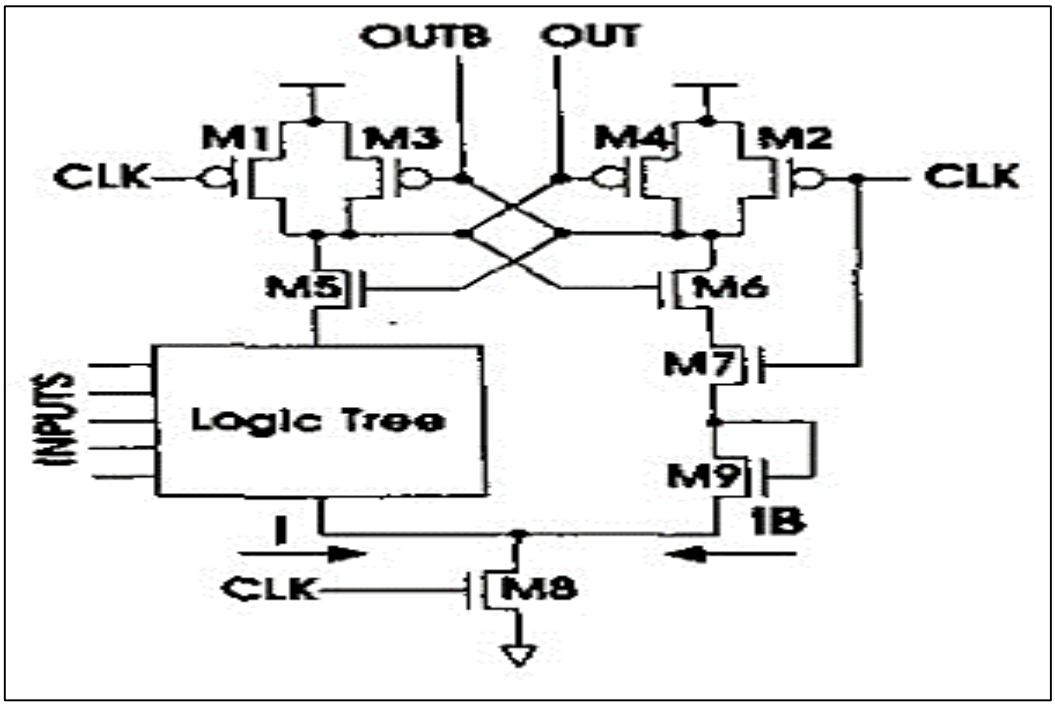

Figure 17: EDCVSL Type - I Structure [7]

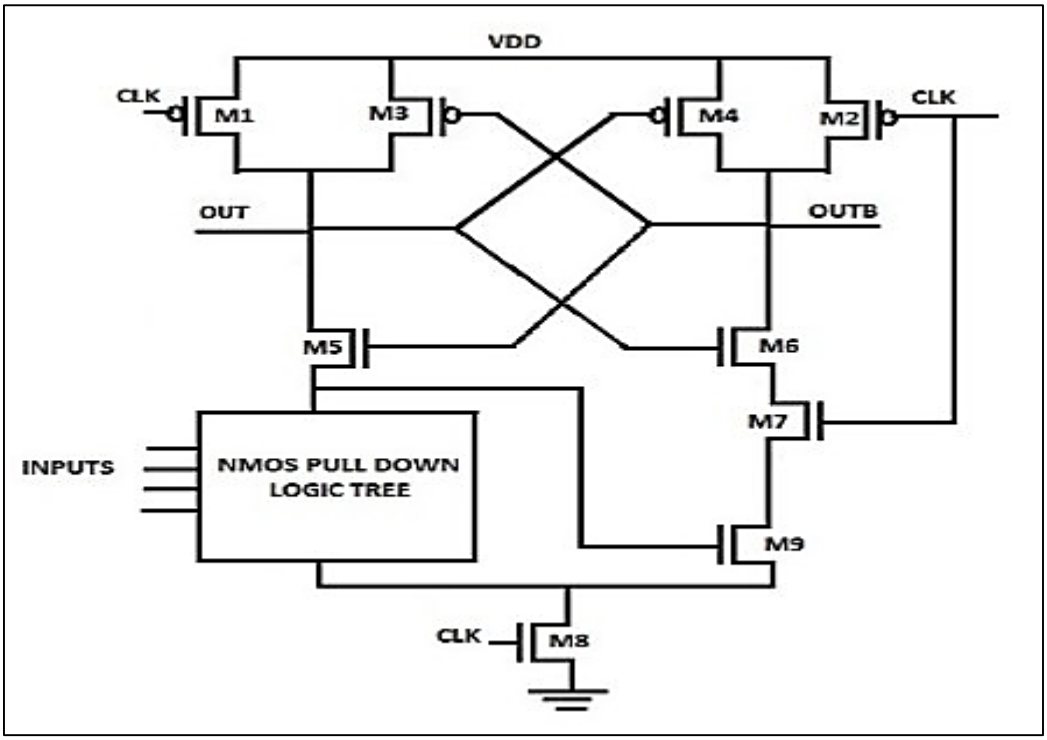

Figure 18: EDCVSL Type - II Structure [7]

***Operation*:**

- The EDCVSL Type II has been considered in this thesis work for performance analysis.
- In pre-charge phase, when CLK=0, output nodes OUT and OUTB gets precharged up to V_{DD} through transistors M1 and M2.
- The feedback transistors M3 and M4 are 'OFF' during this phase since their gates are logic high.
- During evaluation i.e. when CLK=1, the pre-charge transistors Ml and M2 get turned OFF.
- The transistors M7 and M8 that are driven by CLK signal get turned ON which builds a path from output nodes OUT and OUTB to ground via EDCVSL logic tree depending upon the inputs asserted.
- The feedback transistors M3 and M4 are used for speeding up the evaluation and helps in maintaining the correct logic levels.
- The complete complementary input network on the other differential rail is replaced by a single transistor M9. This transistor is controlled by voltage level at the intermediate output node i.e. source of transistor M5.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 19 shows the schematic for 2-input XOR with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

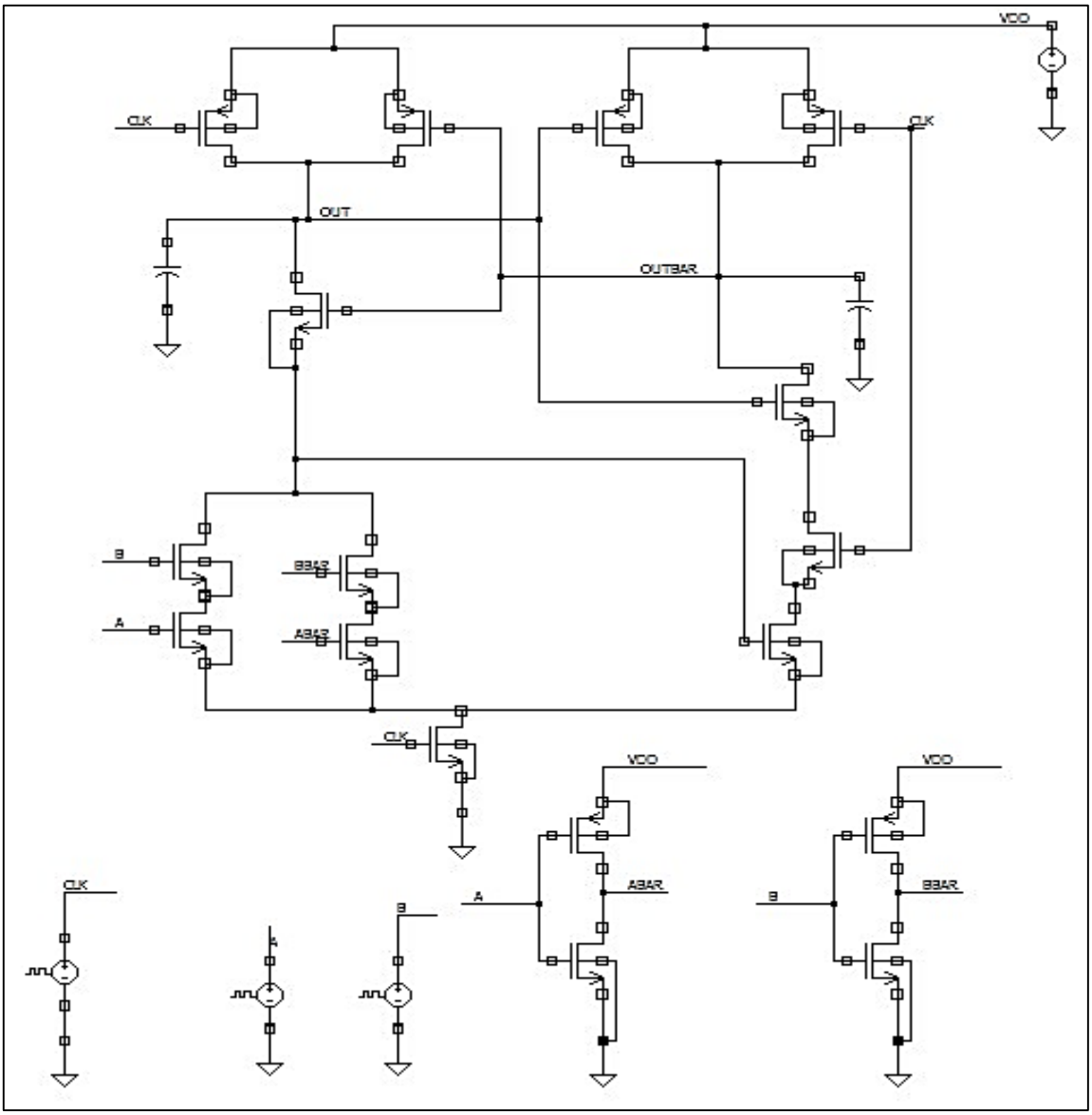

Figure 19: 2-input XOR using EDCVSL architecture

***Simulation Results*:**

Fig. 20 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 14 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 14:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

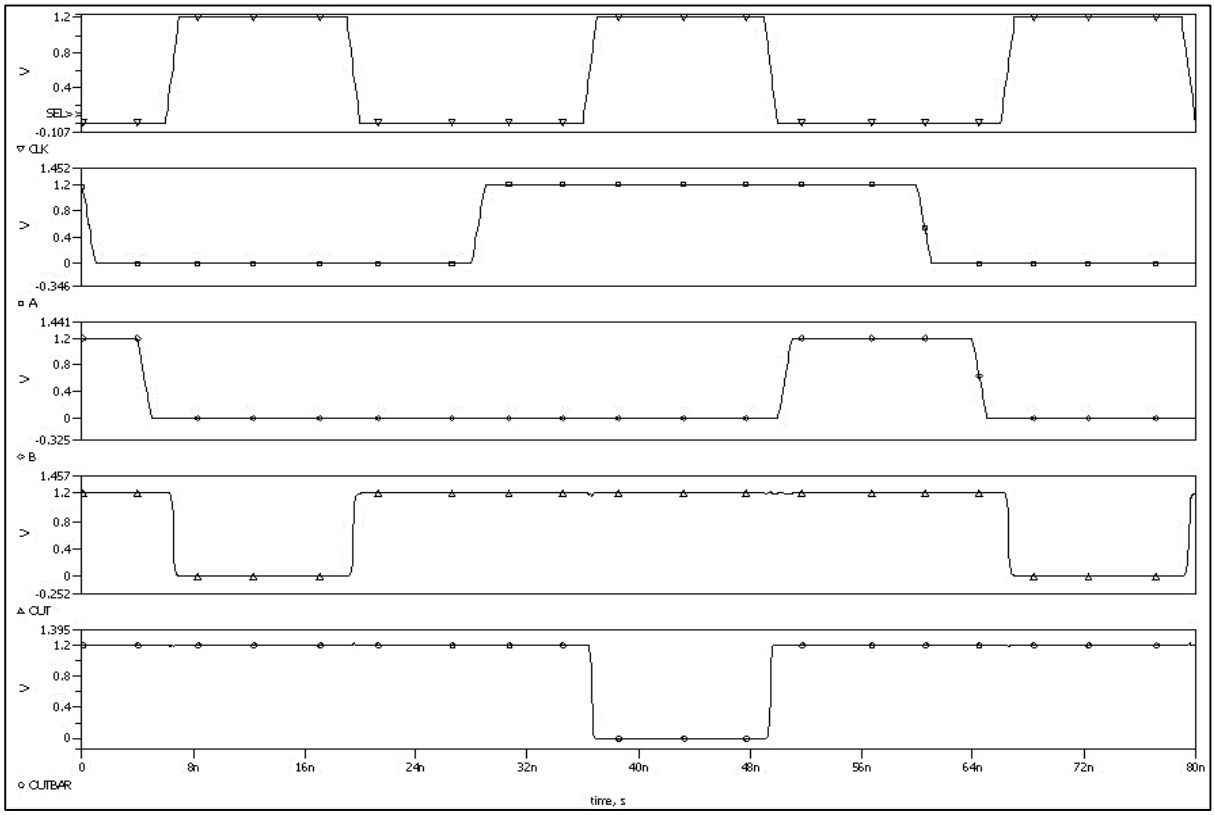

Figure 20: Simulation Output for 2-input XOR using EDCVSL

***Performance Measurement*:**

- Table 15 shows the leakage power for the 2-input XOR EDCVSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 15:

Leakage Power in EDCVSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**6.4**	**7.68**
1	**0**	**1**	**1**	**0**	**5.796**	**6.9552**
1	**1**	**0**	**1**	**0**	**6.056**	**7.2672**
1	**1**	**1**	**0**	**1**	**4.9605**	**5.9526**

- The delay performance of the 2-input XOR using EDCVSL structure is summarized in Table 16. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in EDCVSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 16:

Delay in EDCVSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**64.704**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**64.0743**

(3.6) NP- Mixed DCVSL

NP- Mixed DCVSL a technique that uses both N and P type transistors to build pull-down network. The reason behind introducing PMOS transistors in the logic is because PMOS transistors have relatively lesser sub threshold and gate oxide leakage currents i.e. PMOS transistors are far less leaky than NMOS transistors. But this advantage comes at a cost of decrease in speed.

A conventional DCVSL circuit can be converted into NP mixed DCVSL circuit by replacing those NMOS transistors (having complementary inputs) with PMOS transistors with their gate connected to true signal input instead of their complement. Thus, the extra inverters required to complement the original signals are not required which results in reducing power consumption contributed by these inverters. Also, inverted clock is also not required.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 21 shows the schematic for 2-input XOR with inputs ‘A’ and ‘B’ and clock ‘CLK’ using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

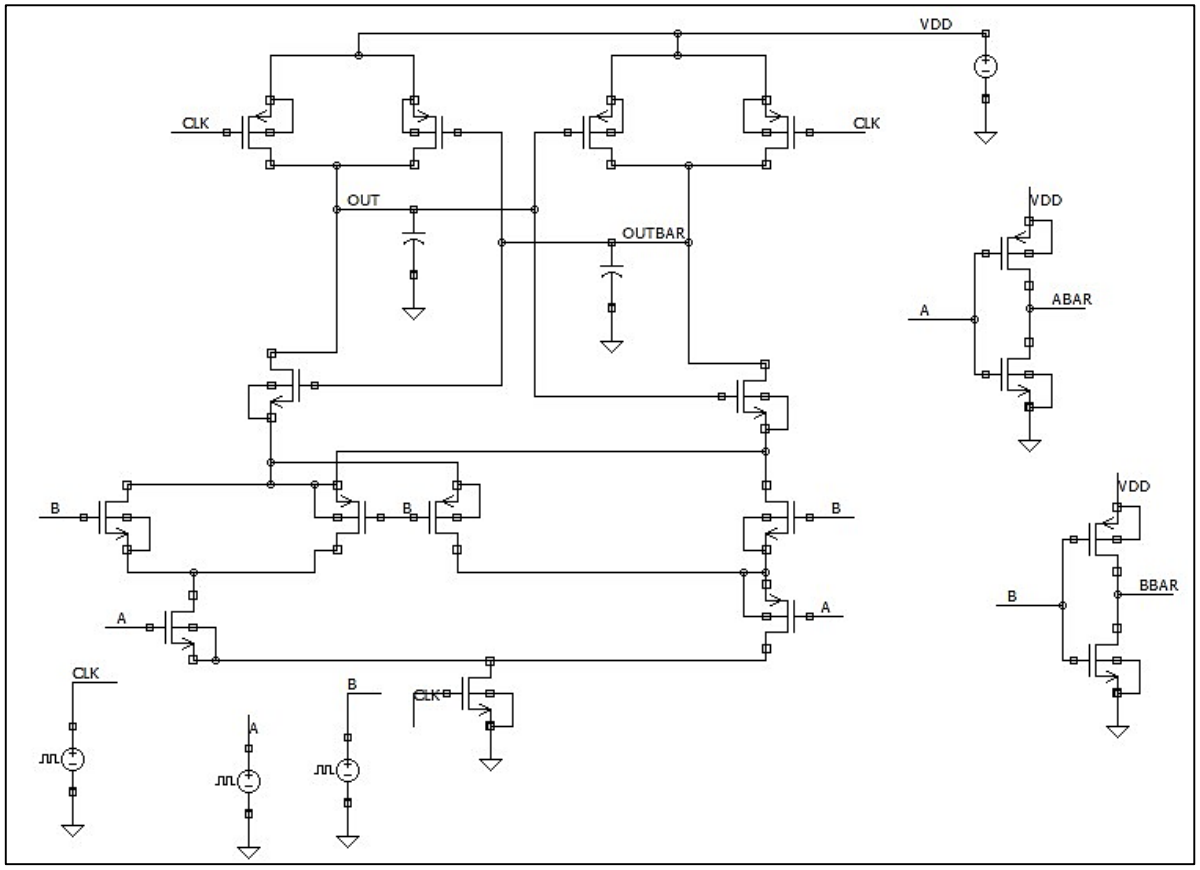

Figure 21: 2-input XOR using NP- Mixed DCVSL architecture

***Simulation Results*:**

Fig. 22 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 17 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 17:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

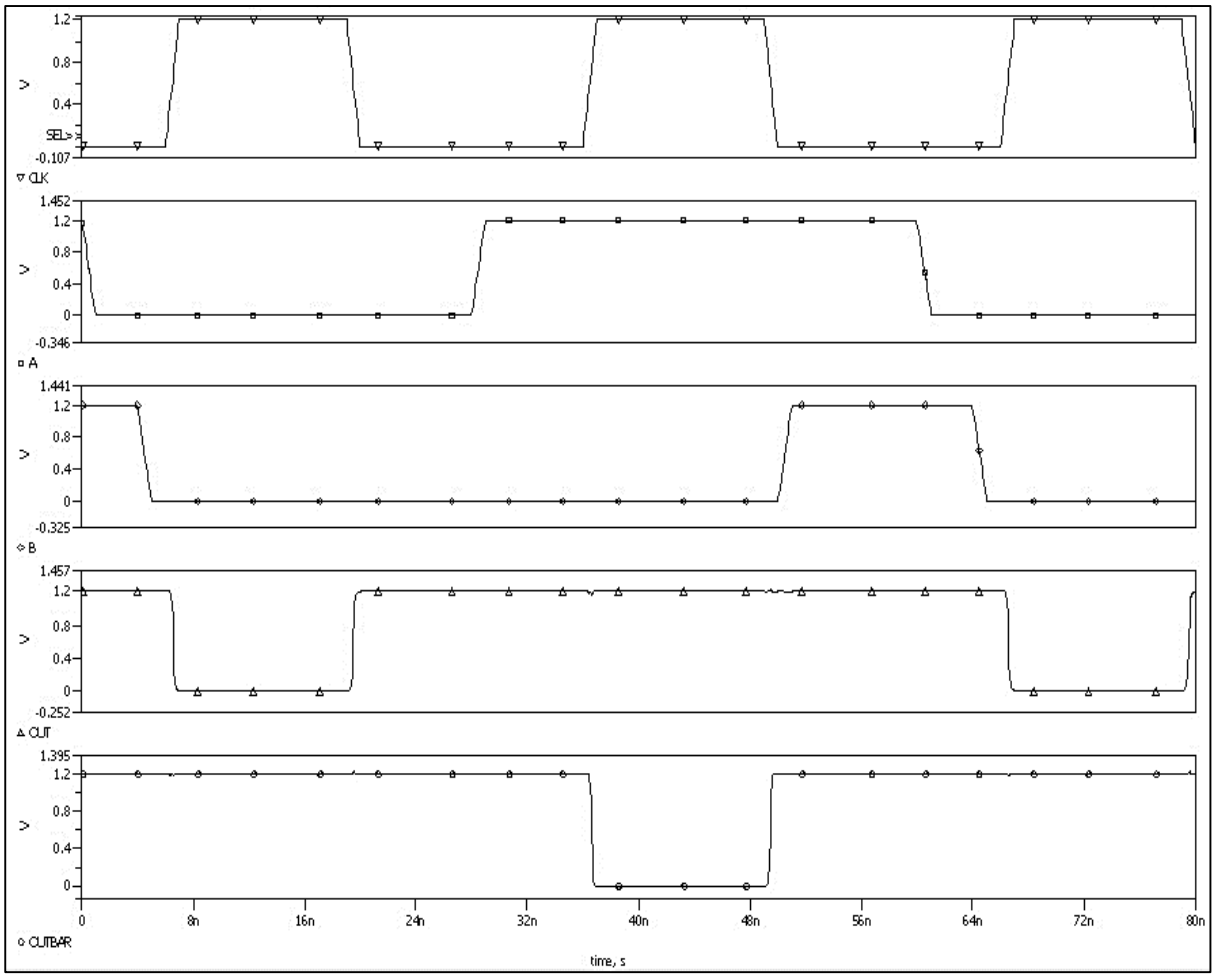

Figure 22: Simulation Output for 2-input XOR using NP- Mixed DCVSL

***Performance Measurement*:**

- Table 18 shows the leakage power for the 2-input XOR NP- Mixed DCVSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 18:

Leakage Power in NP- Mixed DCVSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**5.343**	**6.4116**
1	**0**	**1**	**1**	**0**	**5.722**	**6.8664**
1	**1**	**0**	**1**	**0**	**5.784**	**6.9408**
1	**1**	**1**	**0**	**1**	**5.331**	**6.3972**

- The delay performance of the 2-input XOR using NP- Mixed DCVSL structure is summarized in Table 19. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in EDCVSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 19:

Delay in NP- Mixed DCVSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**78.893**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**78.331**

Summary

In this chapter, variations of dynamic DCVSL are studied and their performance parameters are examined. Different DCVSL structure has their own merits and demerits [1] [6] [7] [13]. As an example, MSSDL decreases the delay of SSDL while sacrificing power dissipation area requirement [1] [6]. This can also be seen from results from Table 20. ECDL circuit eliminates the DC current flow path between V_{DD} and ground, but the downside is that the circuit is designed to discharge the output nodes very half-cycle during the reset phase. This increases the dynamic power dissipation. In addition to the above drawback, the circuit relies on logic chains to discharge one of the output nodes, so that the RC delays may be a limiting factor. It has the advantage of being simple to design with reduced interconnect requirements. It also do not require inverted clock [1]. In EDCVSL, the feedback transistors M3 and M4 are used for speeding up the evaluation and helps in maintaining the correct logic levels. Also, the complete complementary input network on the other differential rail is replaced by a single transistor [7]. In NP-Mixed DCVSL, the extra inverters required to complement the original signals are not required which results in reducing power consumption contributed by these inverters. Also, inverted clock is also not required.

2-input XOR is implemented in various dynamic DCVSL structures to test their functionality. The performance results depend on circuit topology (here 2-input XOR), so these results may not show similar trend always. Yet, these results gives an idea as to utilise a particular structure depending on design requirements. Table 20 tries to summarize results of this chapter.

Table 20:

Summarized Results of Chapter 3

2-input XOR using	No. of Transistors			Leakage Power (nW)	Delay (ps)	PDP (aJ)	Remarks
	NMOS	PMOS	Total				
SSDL	17	7	24	4.609	75.548	0.348	• Improvement in evaluation time over conventional DCVSL and domino structures. • Clock inversion required.
MSSDL	19	7	26	5.582	18.04	0.1	• Improves delay over SSDL. • Leakage Power and transistor count increases.

							• **Overall PDP improves.** • **Clock inversion required.**
ECDL	**14**	**5**	**19**	**5.515**	**87.923**	**0.485**	• **Simple to design with reduced interconnect.** • **Increased dynamic power dissipation.** • **Inverted clock is not required.**
DCSL	**17**	**6**	**23**	**7.025**	**16.598**	**0.116**	• **NMOS transistor introduced in PDN helps in limiting node voltages.** • **Delay reduced significantly offering good PDP.** • **Inverting clock is not required.**
EDCVSL	**11**	**6**	**17**	**6.963**	**64.389**	**0.448**	` • **Transistor count decreases significantly.** • **Complete complementary input network is replaced by a single transistor.** • **Inverting clock is not required.** • **Complex to design.**
NP-Mixed	**8**	**9**	**17**	**6.654**	**78.612**	**0.523**	• **Transistor count decreases significantly.** • **Inverting clock is not required.** • **Delay increases significantly.** • **Complex to design.**

Chapter 4

LECTOR Incorporated Dynamic DCVSL Variations

Introduction

To achieve reduction in leakage power in a circuit, the idea is to assemble transistors from supply V_{DD} to ground. LECTOR technique uses this idea by incorporating two leakage control transistors (LCTs), a PMOS and a NMOS that are positioned in between the PUN and PDN. The gate terminal of one LCT is controlled by the source terminal of other. Thus, there is no need of external circuit as these LCTs are self-controlled. The arrangement of these two LCTs ensures that one of the LCTs remains in "near cut-off region" for any possible combination of inputs. This increases resistance between V_{DD} and ground, thereby reducing the leakage current.

The most noteworthy feature of LECTOR technique that makes it one of the most popular leakage reduction technique is that it manages to have leakage suppression effectively in both active and idle states of the circuit. Making high V_{th} LCTs helps to achieve additional leakage control. Fig. 23 shows a NAND gate incorporated with LCTs to give the idea of this technique.

LECTOR technique is one of the most effective technique in reducing leakage power reduction. This is the reason this technique is used in this thesis to compare performance with the proposed ONOFIC approach for dynamic DCVSL to make a fair competition.

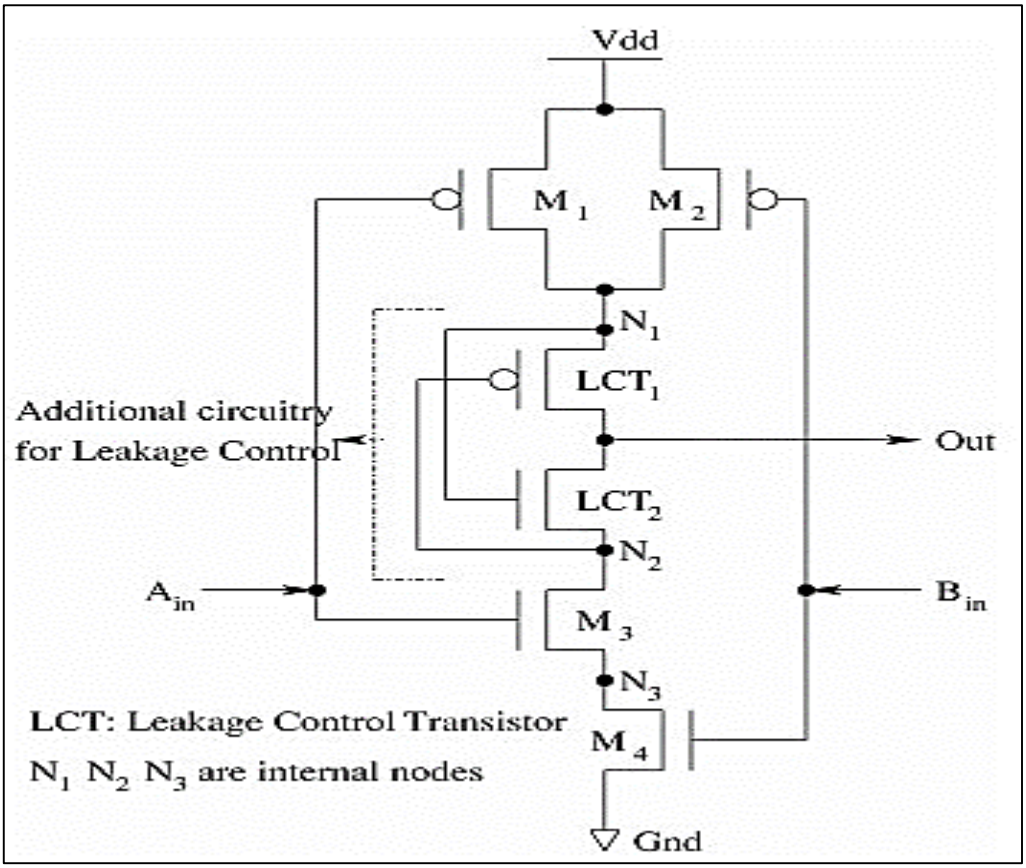

Figure 23: LECTOR incorporated CMOS 2-input NAND gate [9]

Operation

- Let the LECTOR incorporated CMOS 2-input NAND gate given in Fig. 23 is fed with input combination of (A_{in}, B_{in}) = (1, 0). This results in M_1 and M_4 turning 'OFF' and M_2 and M_3 turning 'ON'.

- The node voltages at N_1, N_2, Out and N_3 determines the status of LCT_1 and LCT_2.

- N_1 is at V_{DD}. LCT_1 being a PMOS passes good V_{DD} to 'Out' node.

- LCT_2 being a NMOS passes weak V_{DD} making N_2 at voltage V_{DD}-V_{th}.

- Voltage at node N_2 which is the source voltage of LCT_2, drives the gate of LCT_1. $V_{SG}=V_{th}$ for LCT_1. Thus, the transistor LCT_1 is in "near cut-off" state as there is no voltage difference between its drain ('Out' node) and source (node N_1).

- Similarly, the voltage at node N_1 which is the source voltage of LCT_1, drives the gate of LCT_2. Thus, the transistor LCT_2 turns 'ON' comfortably since its $V_{GS}=V_{th}$ and V_{DS} is also equal to V_{th}.

- This circuit can be analysed for other combinations of inputs in a similar way. Table 21 gives the status of all the transistors for different combinations of inputs to save some effort.

Table 21:

State Matrix of LECTOR incorporated 2-input NAND Gate

TRANSISTOR REFERENCE	INPUT VECTOR-(A_{in} , B_{in})			
	(0,0)	(0,1)	(1,0)	(1,1)
M_1	On state	On state	Off state	Off state
M_2	On state	Off state	On state	Off state
LCT_1	Near cut-Off state	Near cut-Off state	Near cut-Off state	On state
LCT_2	On state	On state	On state	Near cut-Off state
M_3	Off state	Off state	On state	On state
M_4	Off state	On state	Off state	On state

- Thus, it can be observed from Table 21 that one of the LCT is always in "Near cut-off state" for any combination of input. This reduces the leakage current increasing resistance through the path.

(4.1) LECTOR incorporated Sample-Set Differential Logic (L-SSDL)

The operation of LECTOR incorporated SSDL (L-SSDL) remains same as for conventional SSDL mentioned in Section 3.1. The only effect of incorporating LCTs in SSDL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 24 shows the schematic for 2-input XOR using L-SSDL with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

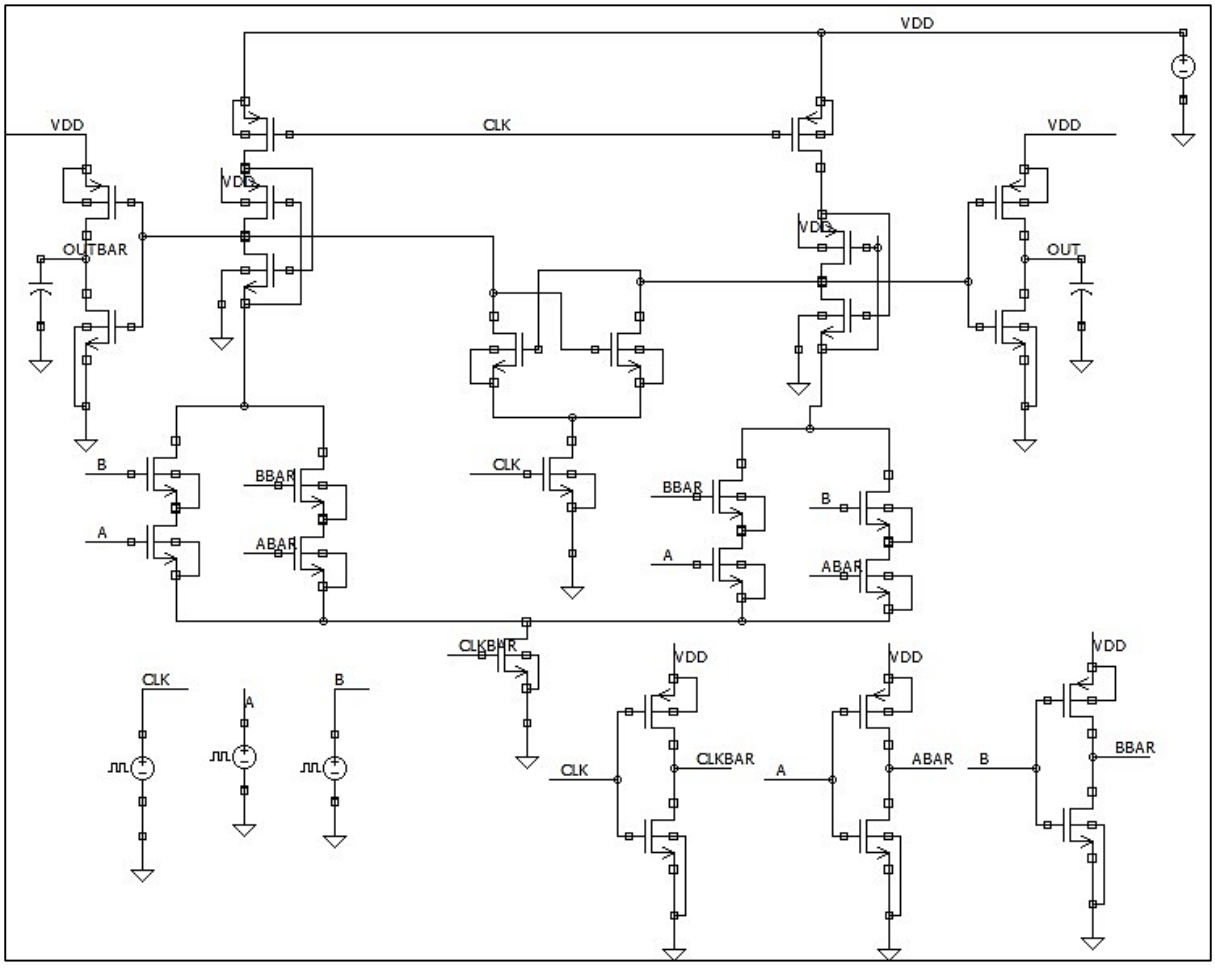

Figure 24: 2-input XOR using L-SSDL architecture

***Simulation Results*:**

Fig. 25 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'.

Table 22 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 22:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	0
v2	1.2	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

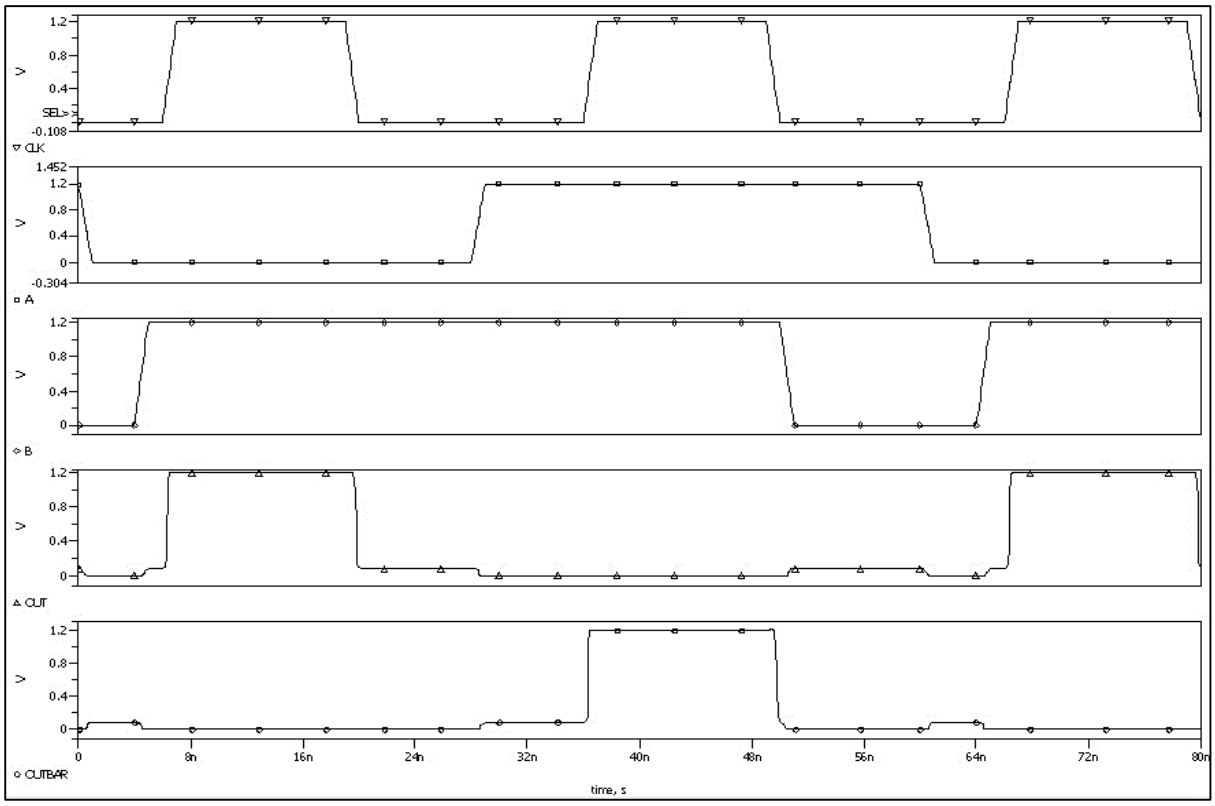

Figure 25: Simulation Output for 2-input XOR using L-SSDL

***Performance Measurement*:**

- Table 23 shows the leakage power for the 2-input XOR L-SSDL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 23:

Leakage Power in L-SSDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*0*	*0*	_	_
1	**0**	**0**	**0**	**1**	**2.812**	**3.374**
1	**0**	**1**	**1**	**0**	**2.866**	**3.4392**
1	**1**	**0**	**1**	**0**	**2.637**	**3.1644**
1	**1**	**1**	**0**	**1**	**2.572**	**3.0864**

- The delay performance of the 2-input XOR using L-SSDL structure is summarized in Table 24. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= 0 in SSDL architectures. Therefore, delay will be '0' if OUT remains '0' in evaluation phase.

Table 24:

Delay in L-SSDL

CLK	A	B	OUT	Delay (ps)
0	X	X	0	_
1	**0**	**0**	0	0
1	**0**	**1**	1	142.78
1	**1**	**0**	1	143.37
1	**1**	**1**	0	0

(4.2) LECTOR incorporated Modified Sample-Set Differential Logic (L- MSSDL)

The operation of LECTOR incorporated MSSDL (L-MSSDL) remains same as for conventional MSSDL mentioned in Section 3.2. The only effect of incorporating LCTs in MSSDL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 26 shows the schematic for 2-input XOR using L-MSSDL architecture with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

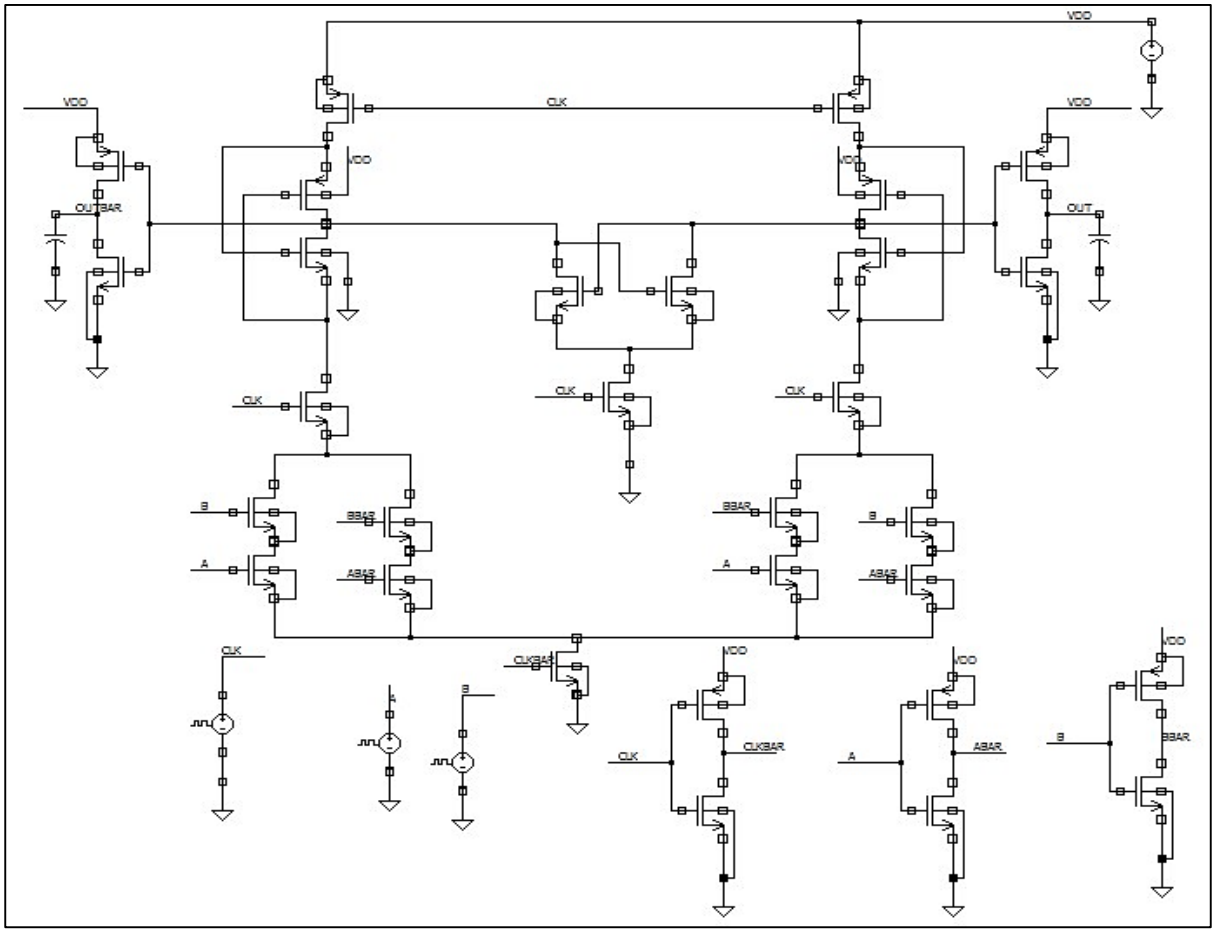

Figure 26: 2-input XOR using L-MSSDL architecture

***Simulation Results*:**

Fig. 27 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 25 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 25:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	0
v2	1.2	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

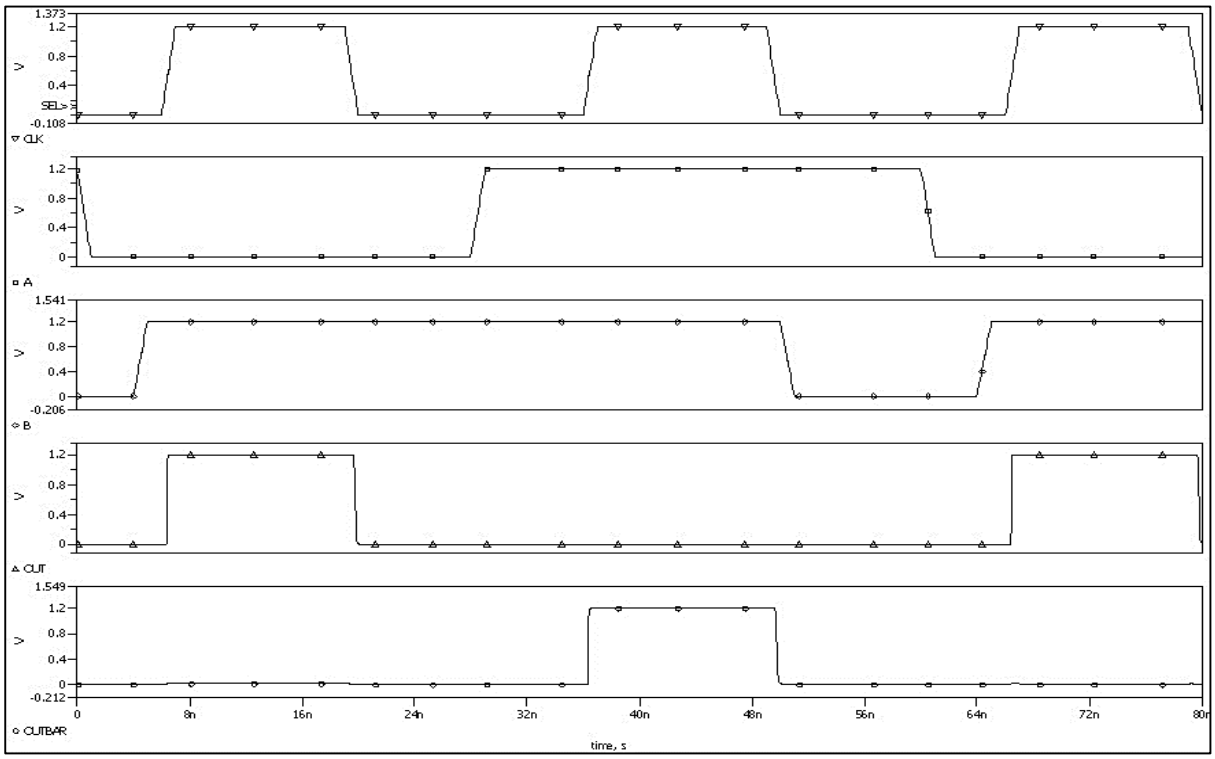

Figure 27: Simulation Output for 2-input XOR using L-MSSDL

***Performance Measurement*:**

- Table 26 shows the leakage power for the 2-input XOR L-MSSDL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 26:

Leakage Power in L-MSSDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*0*	*0*	_	_
1	**0**	**0**	**0**	**1**	**3.335**	**4.002**
1	**0**	**1**	**1**	**0**	**2.673**	**3.2076**
1	**1**	**0**	**1**	**0**	**2.896**	**3.4752**
1	**1**	**1**	**0**	**1**	**2.056**	**2.467**

- The delay performance of the 2-input XOR using L-MSSDL structure is summarized in Table 27. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 0$ in MSSDL. Therefore, delay will be '0' if OUT remains '0' in evaluation phase.

Table 27:

Delay in L-MSSDL

CLK	A	B	OUT	Delay (ps)
0	X	X	0	_
1	**0**	**0**	0	0
1	**0**	**1**	1	81.438
1	**1**	**0**	1	82.48
1	**1**	**1**	0	0

(4.3) LECTOR incorporated Enable/Disable CMOS Differential Logic (L-ECDL)

The operation of LECTOR incorporated ECDL (L-ECDL) remains same as for conventional ECDL mentioned in Section 3.3. The only effect of incorporating LCTs in ECDL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 28 shows the schematic for 2-input XOR using L-ECDL architecture with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

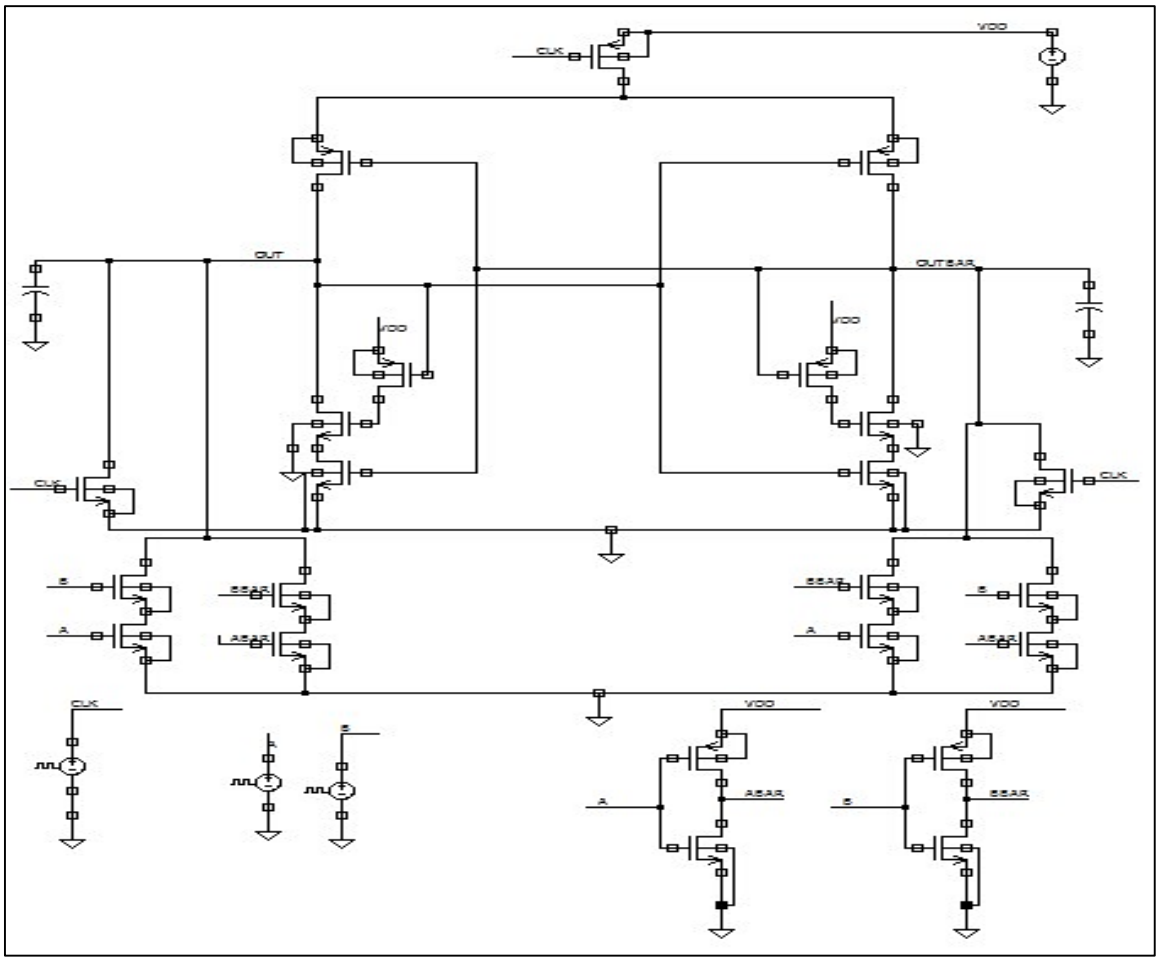

Figure 28: 2-input XOR using L-ECDL architecture

***Simulation Results*:**

Fig. 29 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 28 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 28:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	1.2	1.2	0
v2	0	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

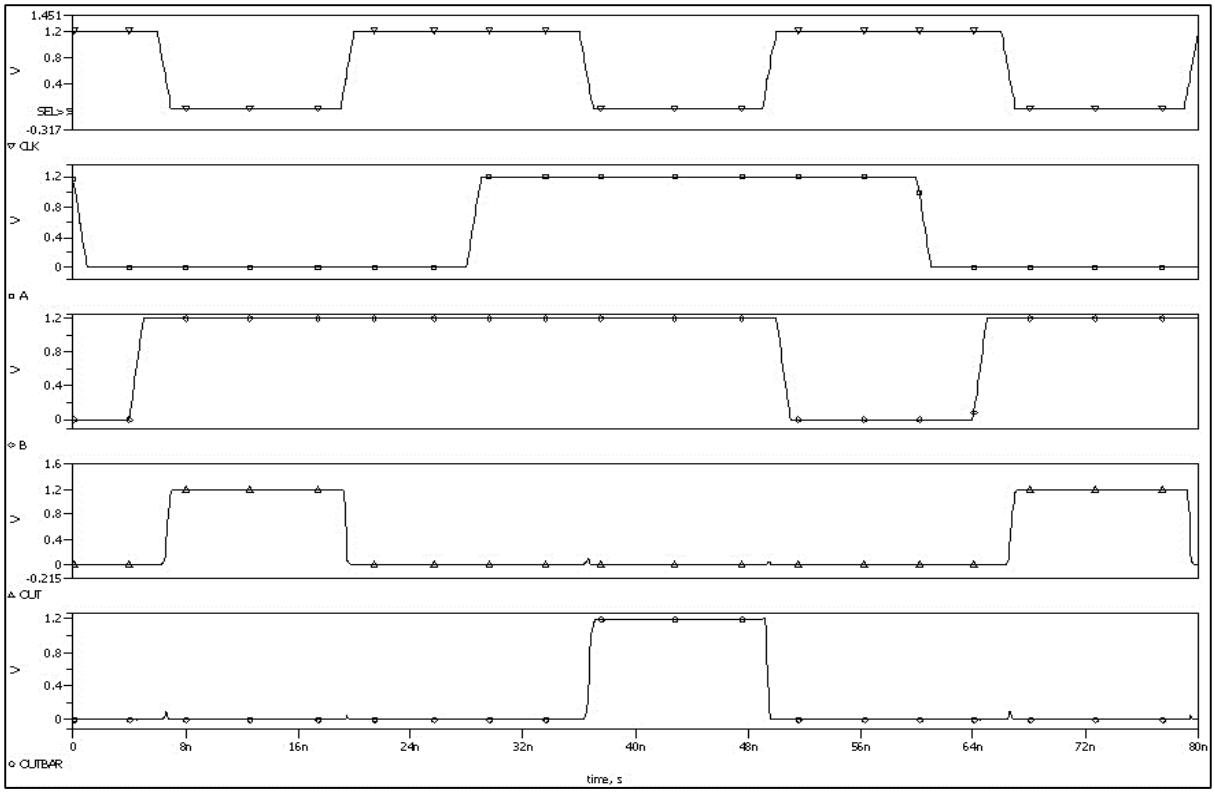

Figure 29: Simulation Output for 2-input XOR using L-ECDL

***Performance Measurement*:**

- Table 29 shows the leakage power for the 2-input XOR L-ECDL structure for various input combinations in enable phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 29:

Leakage Power in L-ECDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
1	*X*	*X*	*0*	*0*	_	_
0	**0**	**0**	**0**	**1**	**3.92**	**4.704**
0	**0**	**1**	**1**	**0**	**3.59**	**4.308**
0	**1**	**0**	**1**	**0**	**4.24**	**5.088**
0	**1**	**1**	**0**	**1**	**4.237**	**5.084**

- The delay performance of the 2-input XOR using L-ECDL structure is summarized in Table 30. The input should be stable before the active edge of CLK (-ve edge) so that the OUT in enable stage is correct. In disable phase, OUT= $\overline{OUT} = 0$ in ECDL. Therefore, delay will be '0' if OUT remains '0' in enable phase.

Table 30:

Delay in L-ECDL

CLK	A	B	OUT	Delay (ps)
1	X	X	0	_
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**200.62**
0	**1**	**0**	**1**	**200.665**
0	**1**	**1**	**0**	**0**

(4.4) LECTOR incorporated Differential Current Switch Logic (L-DCSL)

The operation of LECTOR incorporated DCSL (L-DCSL) remains same as for conventional DCSL mentioned in Section 3.4. The only effect of incorporating LCTs in DCSL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 30 shows the schematic for 2-input L-DCSL XOR with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

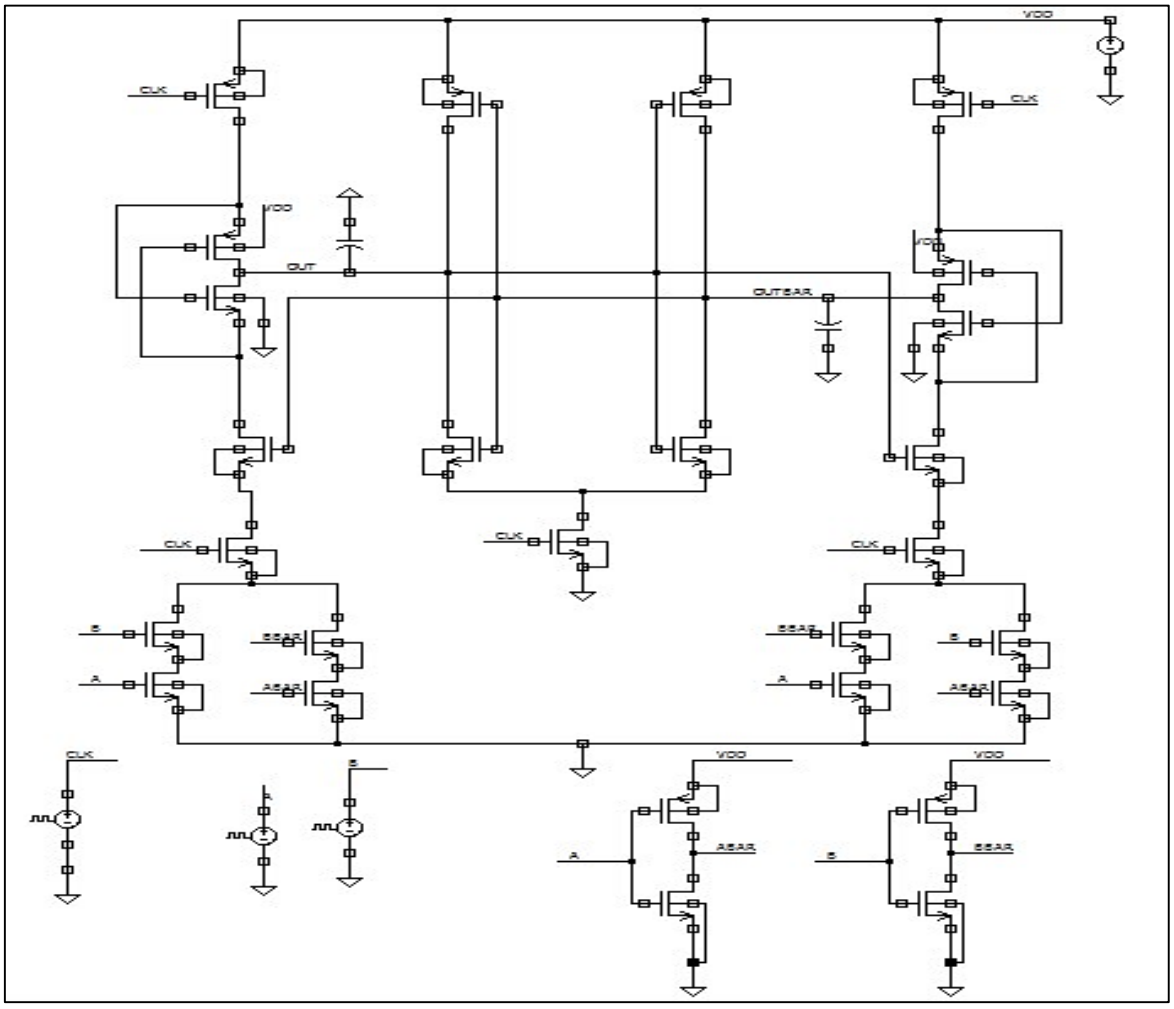

Figure 30: 2-input XOR using L-DCSL architecture

***Simulation Results*:**

Fig. 31 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 31 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 31:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

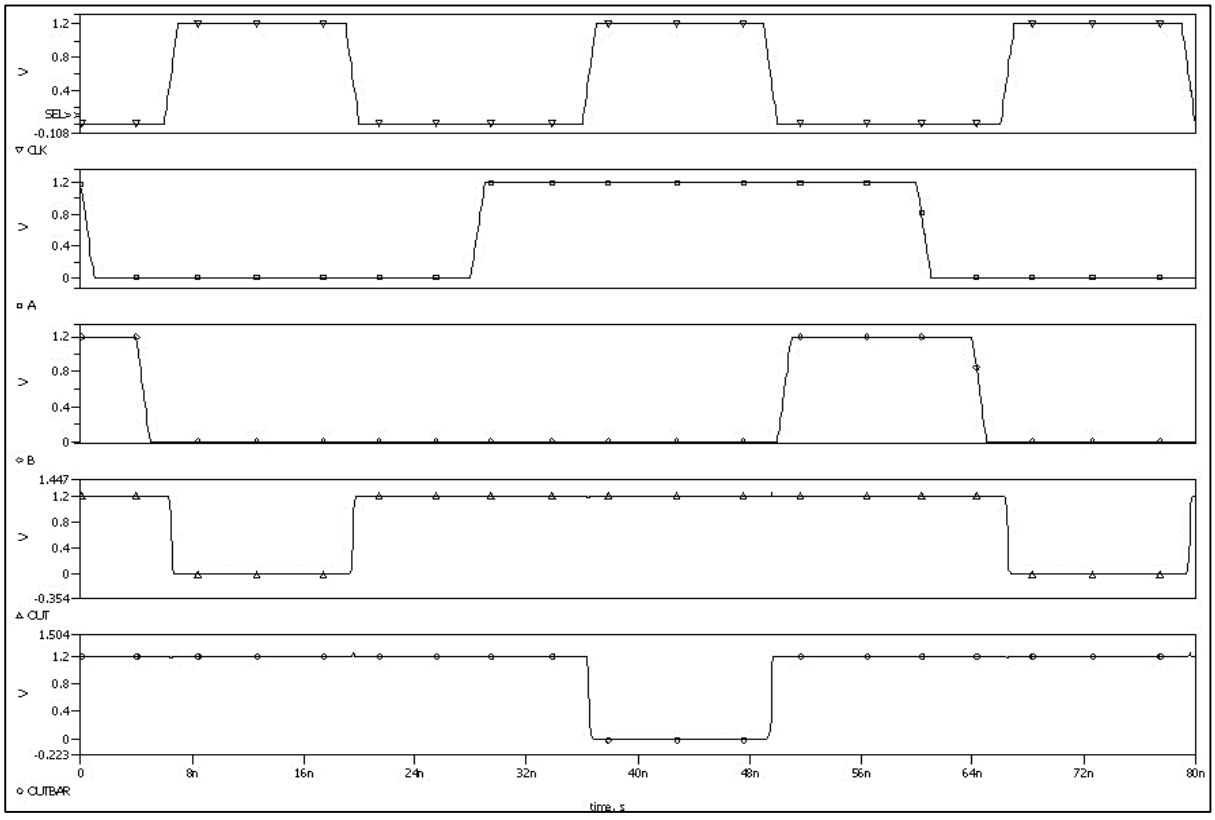

Figure 31: Simulation Output for 2-input XOR using L-DCSL

***Performance Measurement*:**

- Table 32 shows the leakage power for the 2-input XOR L-DCSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 32:
Leakage Power in L-DCSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**4.902**	**5.8824**
1	**0**	**1**	**1**	**0**	**3.953**	**4.7436**
1	**1**	**0**	**1**	**0**	**3.57**	**4.284**
1	**1**	**1**	**0**	**1**	**3.246**	**3.8952**

- The delay performance of the 2-input XOR using L-DCSL structure is summarized in Table 33. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in DCSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 33:
Delay in L-DCSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**78.61**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**80.816**

(4.5) LECTOR incorporated Enhanced Differential Cascode Voltage Switch Logic (L-EDCVSL)

The operation of LECTOR incorporated EDCVSL (L-EDCVSL) remains same as for conventional EDCVSL mentioned in Section 3.5. The only effect of incorporating LCTs in EDCVSL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 32 shows the schematic for 2-input XOR L-EDCVSL with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

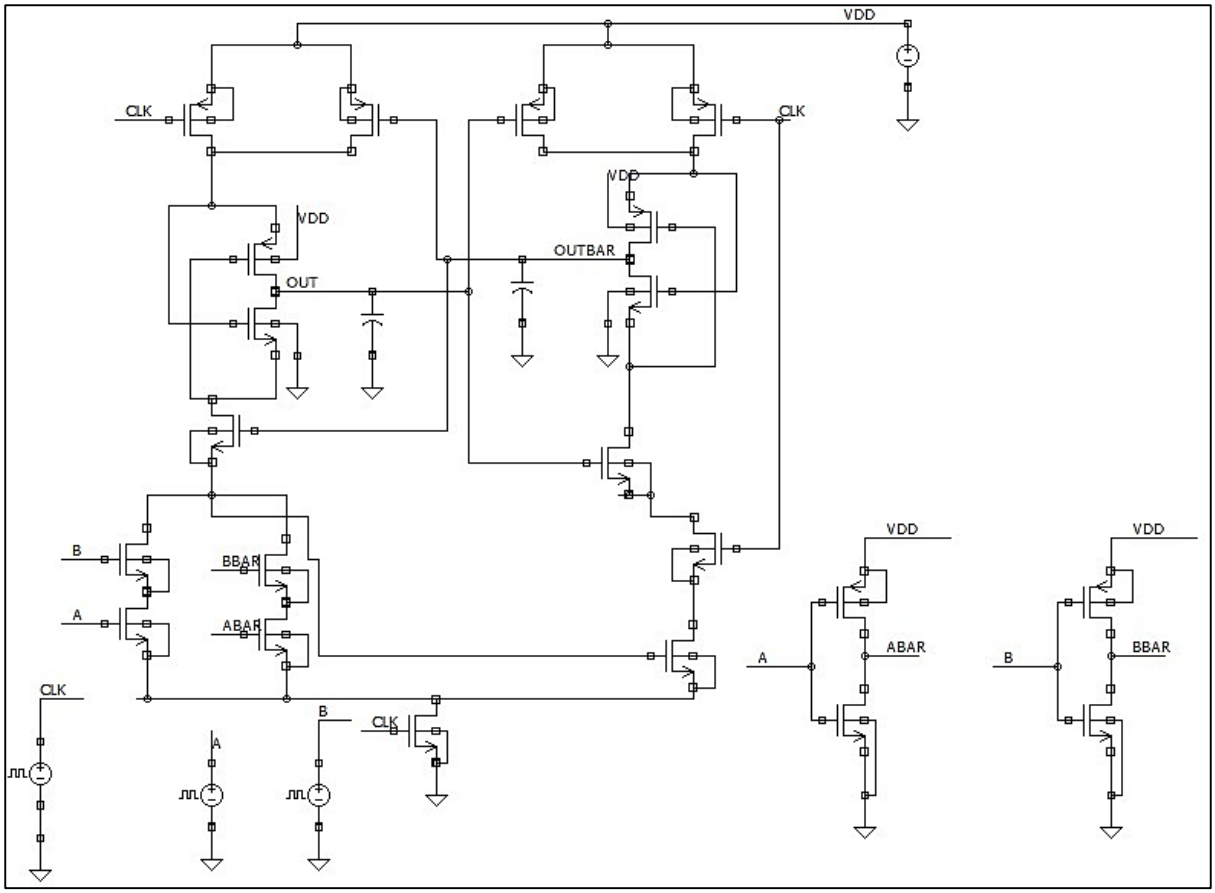

Figure 32: 2-input XOR using L-EDCVSL architecture

***Simulation Results*:**

Fig. 33 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 34 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 34:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

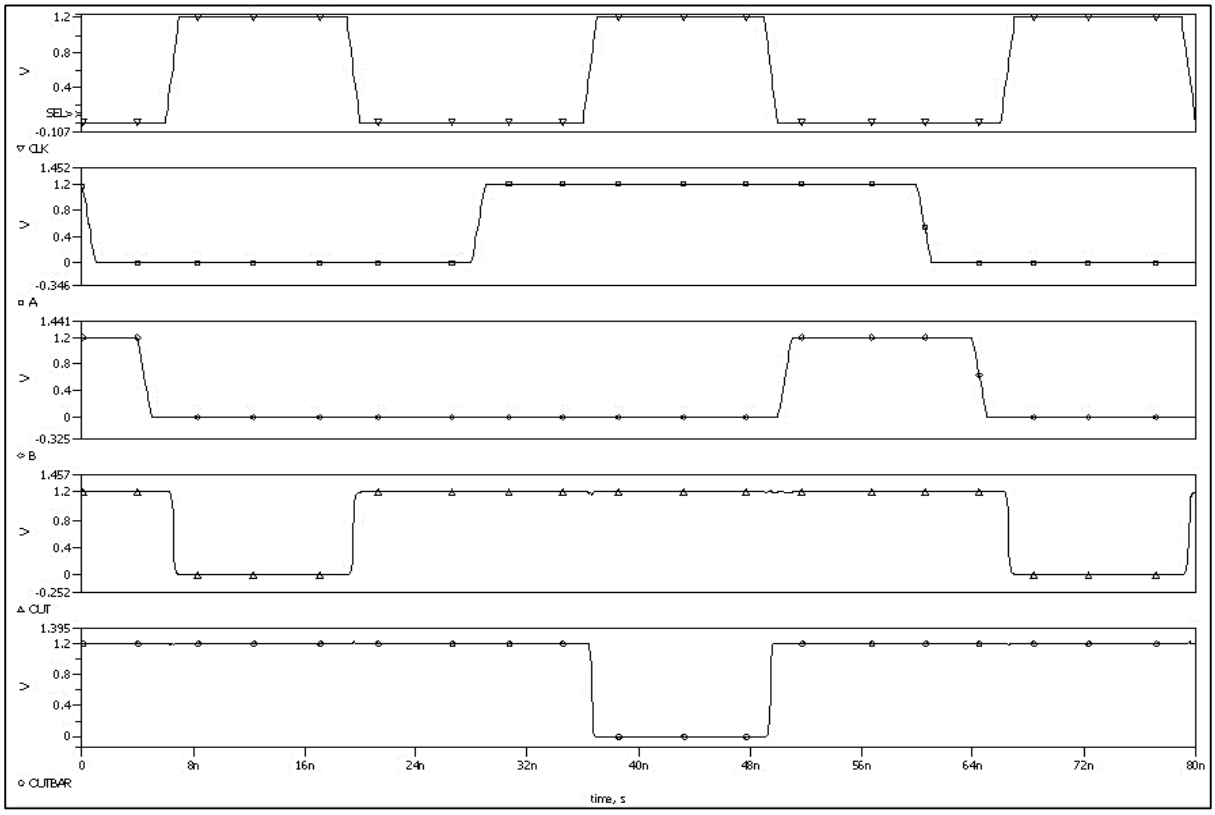

Figure 33: Simulation Output for 2-input XOR using L-EDCVSL

***Performance Measurement*:**

- Table 35 shows the leakage power for the 2-input XOR L-EDCVSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 35:
Leakage Power in L-EDCVSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**4.727**	**5.6724**
1	**0**	**1**	**1**	**0**	**6.28**	**7.536**
1	**1**	**0**	**1**	**0**	**3.269**	**3.9228**
1	**1**	**1**	**0**	**1**	**4.65**	**5.58**

- The delay performance of the 2-input XOR using L-EDCVSL structure is summarized in Table 36. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in EDCVSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 36:
Delay in L-EDCVSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**76.981**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**74.526**

(4.6) LECTOR incorporated NP- Mixed DCVSL

The operation of LECTOR incorporated NP-Mixed DCVSL (L-NP-Mixed) remains same as for conventional NP-Mixed DCVSL mentioned in Section 3.6. The only effect of incorporating LCTs in NP-Mixed DCVSL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 34 shows the schematic for 2-input XOR L-NP-Mixed DCVSL with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

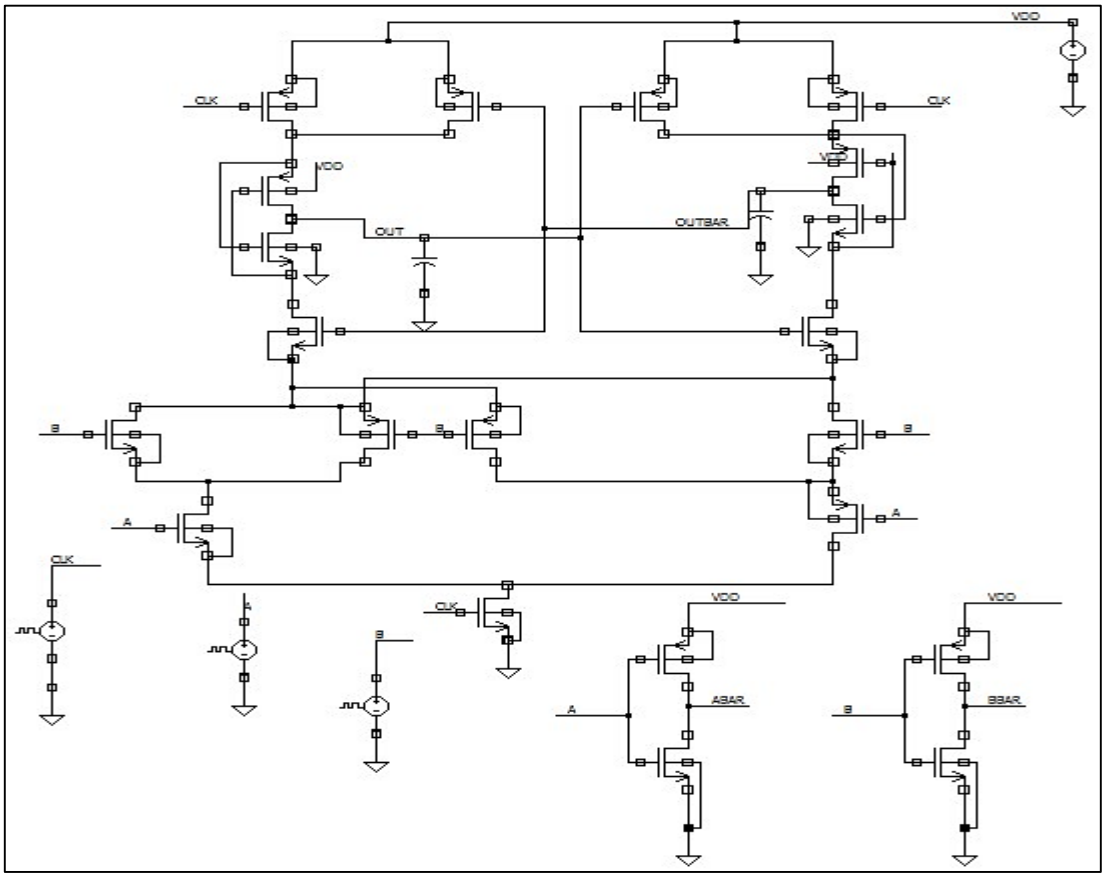

Figure 34: 2-input XOR using L-NP- Mixed DCVSL architecture

***Simulation Results*:**

Fig. 35 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 37 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 37:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

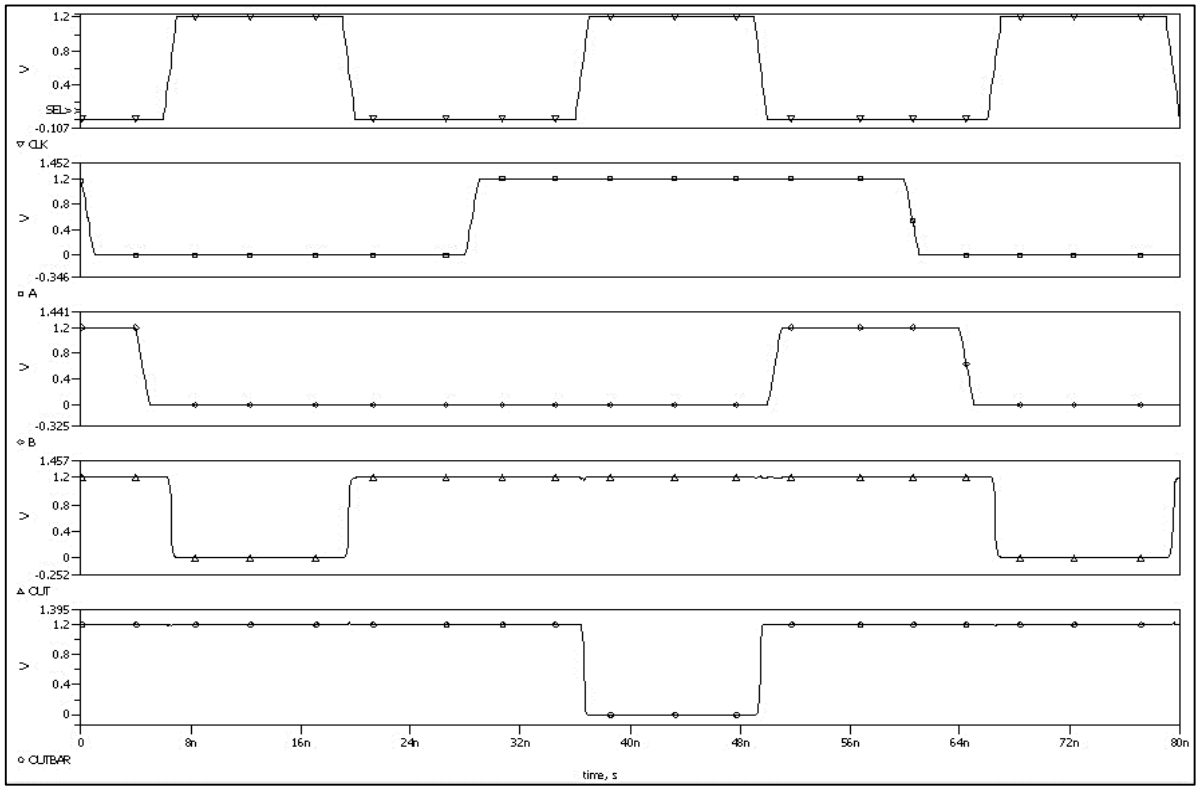

Figure 35: Simulation Output for 2-input XOR using L-NP- Mixed DCVSL

***Performance Measurement*:**

- Table 38 shows the leakage power for the 2-input XOR L-NP- Mixed DCVSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 38:

Leakage Power in L-NP- Mixed DCVSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**4.791**	**6.9492**
1	**0**	**1**	**1**	**0**	**5.224**	**6.2688**
1	**1**	**0**	**1**	**0**	**5.319**	**6.3828**
1	**1**	**1**	**0**	**1**	**4.811**	**5.7732**

- The delay performance of the 2-input XOR using L-NP- Mixed DCVSL structure is summarized in Table 39. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in EDCVSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 39:

Delay in L-NP- Mixed DCVSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**105.34**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**107.81**

Summary

In this chapter, LECTOR technique has been incorporated in dynamic DCVSL variants. The operation of different L-DCVSL structures will remain same as those of conventional dynamic DCVSL structures except for the changes in performance introduced by incorporating LECTOR block. LECTOR technique has been one of the best technique for leakage power reduction as reported in literature [3] [9]. LECTOR significantly reduces leakage power dissipation but the main drawback is that it increases delay up to the extent that the PDP deteriorates when compared to conventional dynamic DCVSL structures of Chapter 3. This can be seen in the summarized result of this chapter given in Table 40.

It can be inferred from Table 20 and Table 40 that leakage power decreases in case of LECTOR incorporated DCVSL variants when compared to conventional DCVSL variants. But the drawback of this is seen as a significant increase in delay. Thus, the PDP of LECTOR incorporated dynamic DCVSL is more than conventional dynamic DCVSL (except for the case of EDCVSL).

Table 40:

Summarized Results of Chapter 4

2-input XOR using	No. of Transistors			Leakage Power (nW)	Delay (ps)	PDP (aJ)
	NMOS	PMOS	Total			
L-SSDL	19	9	28	3.266	143.075	0.467
L-MSSDL	21	9	30	3.288	81.959	0.27
L-ECDL	16	7	23	4.796	200.643	0.962

L-DCSL	**19**	**8**	**27**	**4.701**	**79.713**	**0.614**
L-EDCVSL	**13**	**8**	**21**	**5.678**	**75.756**	**0.43**
L-NP-Mixed	**10**	**11**	**21**	**6.346**	**106.575**	**0.676**

Chapter 5

ONOFIC Incorporated Dynamic DCVSL Variations

Introduction

A new leakage reduction technique was introduced in [2]. ONOFIC is an acronym for **ON**/**OF**F LOG**IC** (ONOFIC). This is a simple approach that uses single threshold voltage circuitry for reducing the leakage current unlike LECTOR. Reduction in leakage current results in decrease in the leakage power which directly effects the total power dissipation of the logic circuit.

ONOFIC approach is an efficient technique for reducing leakage power in both the active and stand-by mode. Similar to LECTOR technique for leakage power reduction, it also introduces extra logic circuit between the PUN and PDN. This ONOFIC block contains an NMOS and a PMOS transistor. The ONOFIC transistors are connected as shown in Fig. 36.

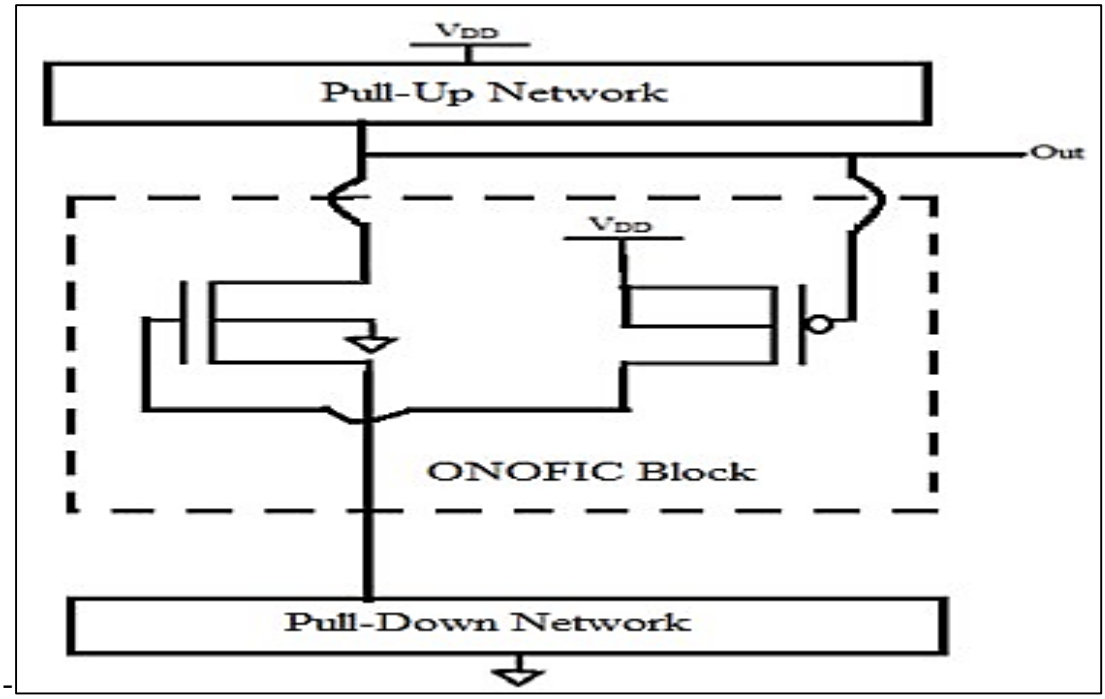

Figure 36: ONOFIC Schematic [2]

The logic block introduced is termed ONOFIC because for any 'Out' logic level, this block must remain in 'ON' or 'OFF' condition. Thus, the precise turning 'ON/Off' of this ONOFIC block directly affects the propagation delay and power dissipation of the circuit. The schematic of an ONOFIC 2-input NAND gate is shown in Fig. 37 as an example.

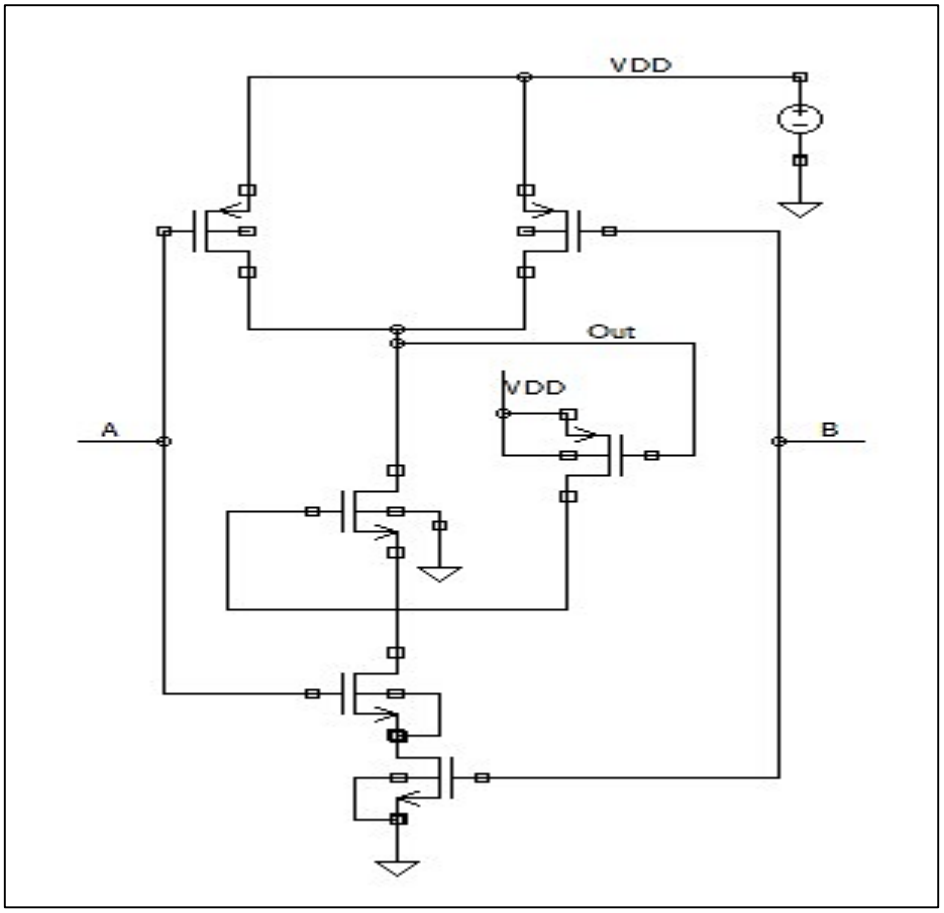

Figure 37: ONOFIC 2-input NAND Schematic

Operation

- The ONOFIC circuit uses the very popular concept of force stacking. This make sure that the ONOFIC block provides maximum resistance when it is in "OFF" state and minimum resistance in "ON". This helps in minimizing the leakage current.
- In ONOFIC block, the PMOS transistor regulates the function of the NMOS transistor.
- Depending on the logic level of 'Out' node, the ONOFIC NMOS/PMOS transistors must be in cut-off or in linear mode.

- The NMOS transistor in ONOFIC block is called *path transistor* while the PMOS transistor is called *forced transistor*. The forced transistor controls the operation of the path transistor.

- Precise regulation of the input of the NMOS (path transistor) by the PMOS (forced transistor) results in reduction of the leakage current at manageable propagation delay.

- Table 41 explains the operation of ONOFIC 2-input CMOS NAND gate. $PMOS_1$ and $PMOS_2$ are connected parallel in PUN while $NMOS_1$ and $NMOS_2$ are connected series in PDN. This technique focuses on its ideal ON/OFF property.

- We can see from the operating status of the transistors given in Table 41 that the ONOFIC block is completely "ON" or "OFF" for any input signal combination.

- When ONOFIC block is in "ON" condition, both ONOFIC transistors (PMOS and NMOS) are in linear region. Conversely, when ONOFIC block is in "OFF" state both ONOFIC transistors (PMOS and NMOS) are in cut-off mode.

Table 41:

Operating Status of transistors in ONOFIC 2-input NAND gate

Inputs	$PMOS_1$	$PMOS_2$	ONOFIC PMOS	ONOFIC NMOS	$NMOS_1$	$NMOS_2$
(0,0)	ON	ON	OFF	OFF	OFF	OFF
(0,1)	ON	OFF	OFF	OFF	OFF	ON
(1,0)	OFF	ON	OFF	OFF	ON	OFF
(1,1)	OFF	OFF	ON	ON	ON	ON

(5.1) ONOFIC incorporated Sample-Set Differential Logic (O-SSDL)

The operation of ONOFIC incorporated SSDL (O-SSDL) remains same as for conventional SSDL mentioned in Section 3.1. The only effect of incorporating ONOFIC block in SSDL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 38 shows the schematic for 2-input XOR using O-SSDL with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

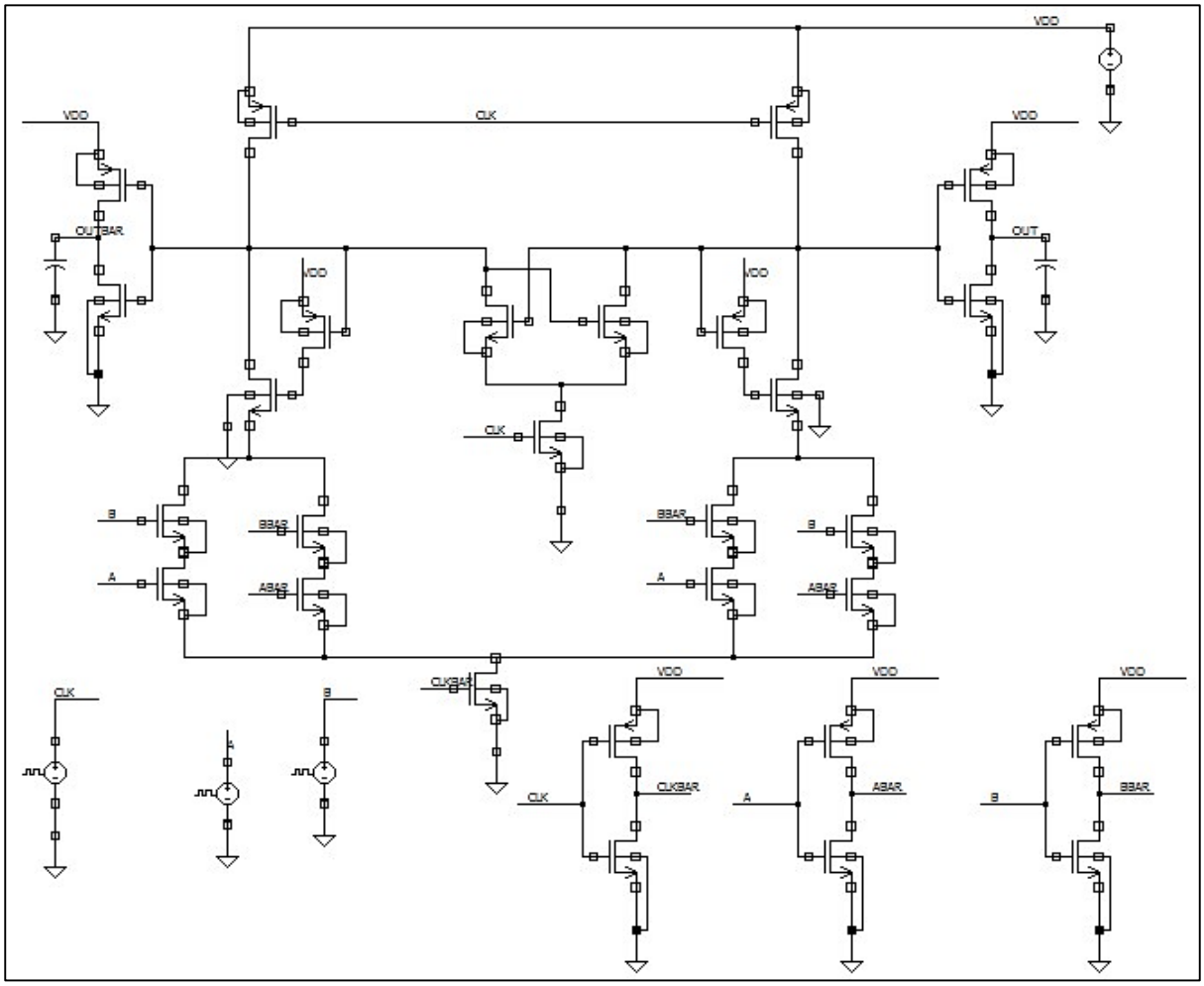

Figure 38: 2-input XOR using O-SSDL architecture

***Simulation Results*:**

Fig. 39 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'.

Table 42 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 42:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	0
v2	1.2	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

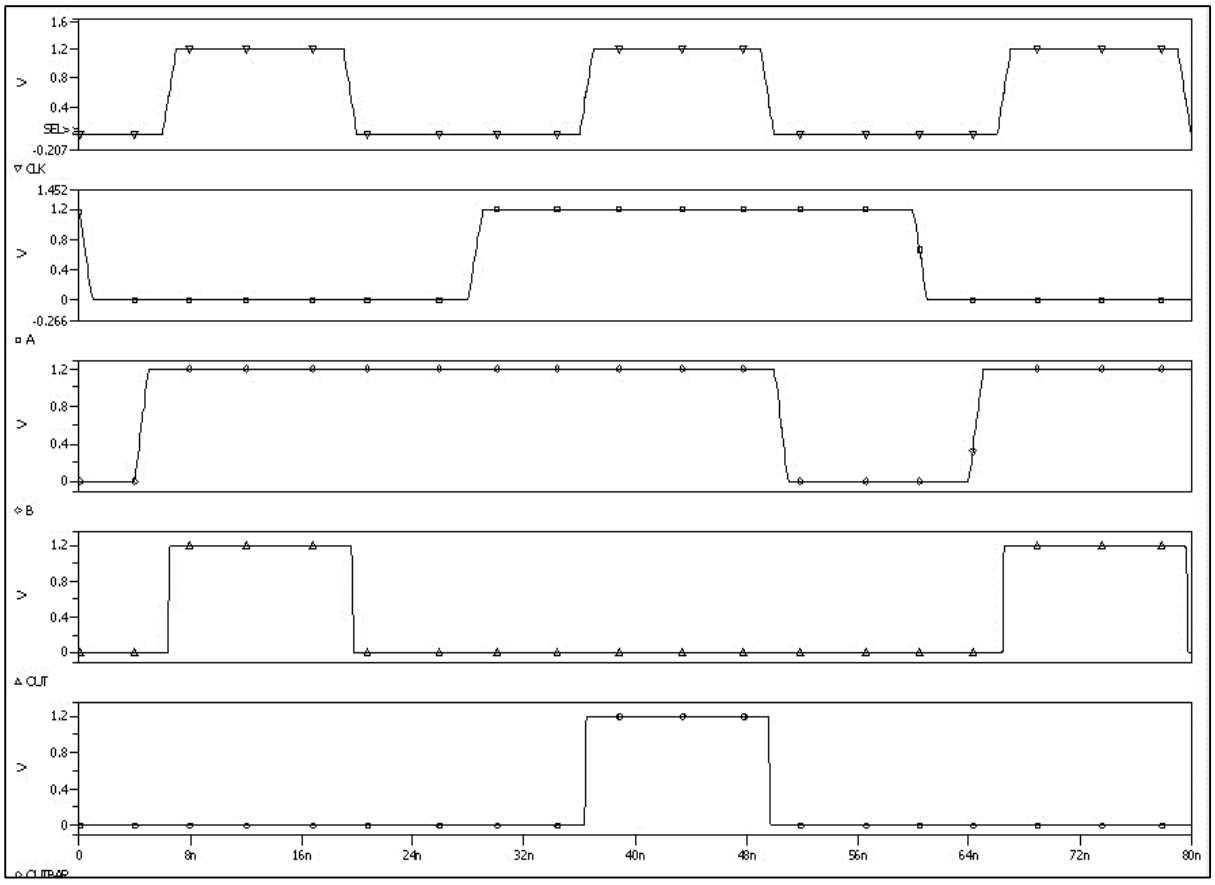

Figure 39: Simulation Output for 2-input XOR using O-SSDL

***Performance Measurement*:**

- Table 43 shows the leakage power for the 2-input XOR O-SSDL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 43:
Leakage Power in O-SSDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*0*	*0*	_	_
1	**0**	**0**	**0**	**1**	**3.614**	**4.3368**
1	**0**	**1**	**1**	**0**	**3.443**	**4.1316**
1	**1**	**0**	**1**	**0**	**3.057**	**3.6684**
1	**1**	**1**	**0**	**1**	**2.9268**	**3.5136**

- The delay performance of the 2-input XOR using O-SSDL structure is summarized in Table 44. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= 0 in SSDL architectures. Therefore, delay will be '0' if OUT remains '0' in evaluation phase.

Table 44:
Delay in O-SSDL

CLK	A	B	OUT	Delay (ps)
0	X	X	0	_
1	**0**	**0**	0	0
1	**0**	**1**	1	87.03
1	**1**	**0**	1	86.99
1	**1**	**1**	0	0

(5.2) ONOFIC incorporated Modified Sample-Set Differential Logic (O- MSSDL)

The operation of ONOFIC incorporated MSSDL (O-MSSDL) remains same as for conventional MSSDL mentioned in Section 3.2. The only effect of incorporating ONOFIC block in MSSDL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 40 shows the schematic for 2-input XOR using O-MSSDL architecture with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

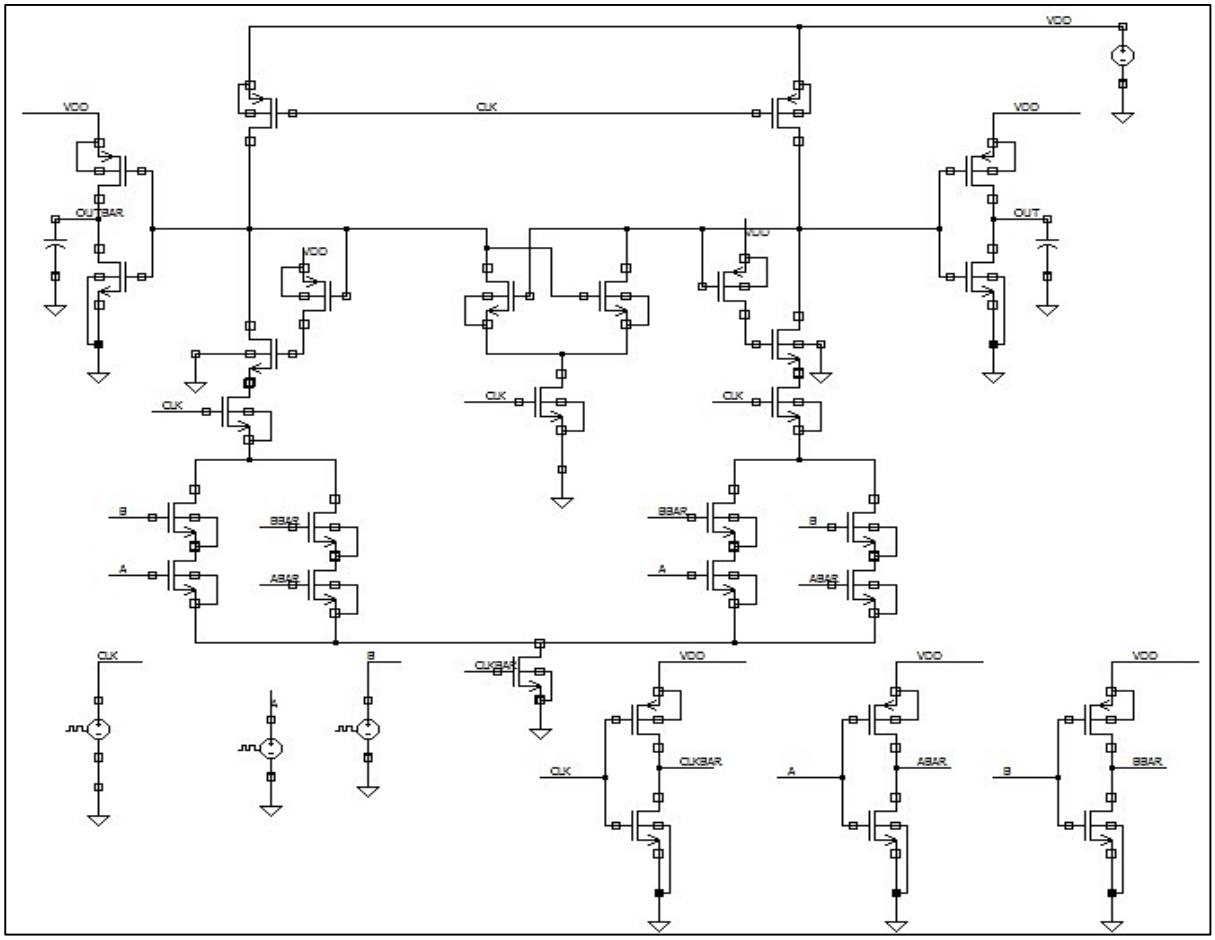

Figure 40: 2-input XOR using O-MSSDL architecture

***Simulation Results*:**

Fig. 41 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 45 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 45:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	0
v2	1.2	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

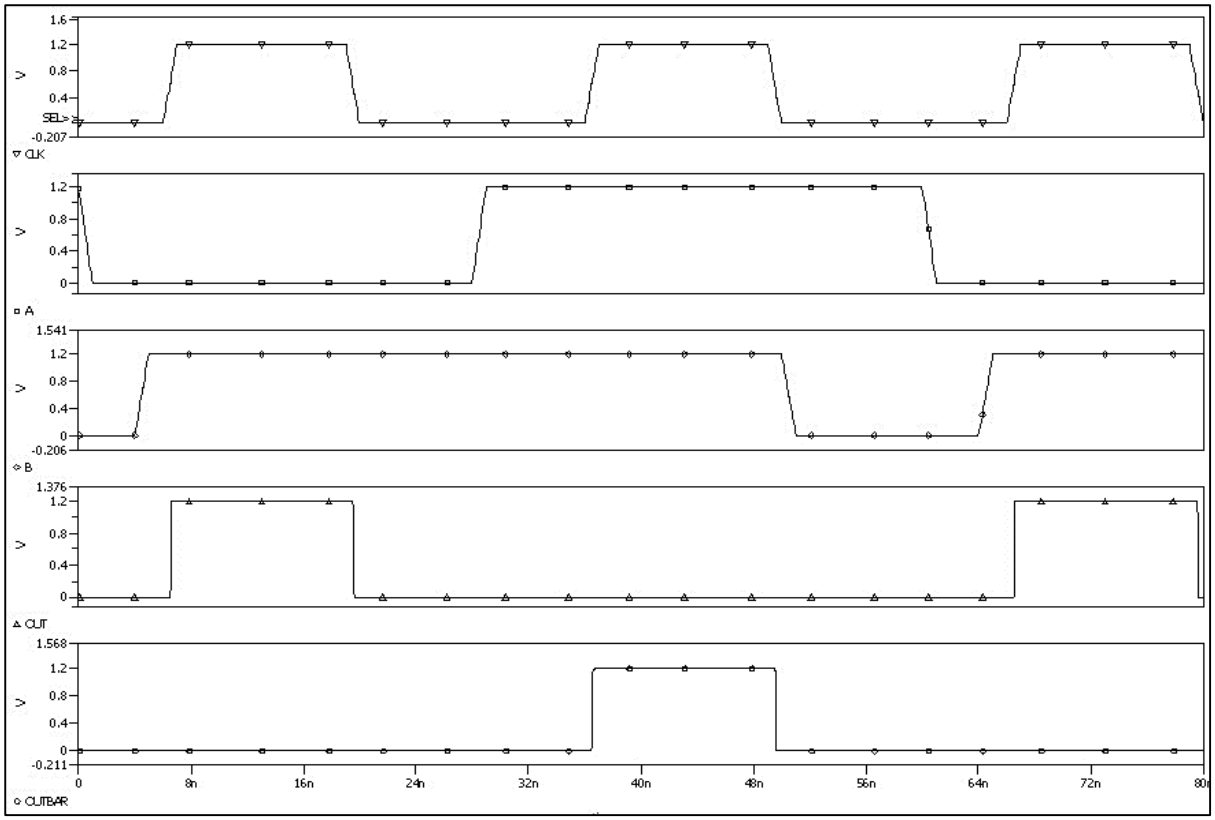

Figure 41: Simulation Output for 2-input XOR using O-MSSDL

***Performance Measurement*:**

- Table 46 shows the leakage power for the 2-input XOR O-MSSDL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 46:

Leakage Power in O-MSSDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*0*	*0*	_	_
1	**0**	**0**	**0**	**1**	**4.11**	**4.932**
1	**0**	**1**	**1**	**0**	**4.28**	**5.136**
1	**1**	**0**	**1**	**0**	**4.299**	**5.158**
1	**1**	**1**	**0**	**1**	**4.398**	**5.277**

- The delay performance of the 2-input XOR using O-MSSDL structure is summarized in Table 47. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 0$ in MSSDL. Therefore, delay will be '0' if OUT remains '0' in evaluation phase.

Table 47:

Delay in O-MSSDL

CLK	A	B	OUT	Delay (ps)
0	X	X	0	_
1	**0**	**0**	0	0
1	**0**	**1**	1	42.549
1	**1**	**0**	1	41.952
1	**1**	**1**	0	0

(5.3) ONOFIC incorporated Enable/Disable CMOS Differential Logic (O-ECDL)

The operation of ONOFIC incorporated ECDL (O-ECDL) remains same as for conventional ECDL mentioned in Section 3.3. The only effect of incorporating ONOFIC blocks in ECDL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 42 shows the schematic for 2-input XOR using O-ECDL architecture with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

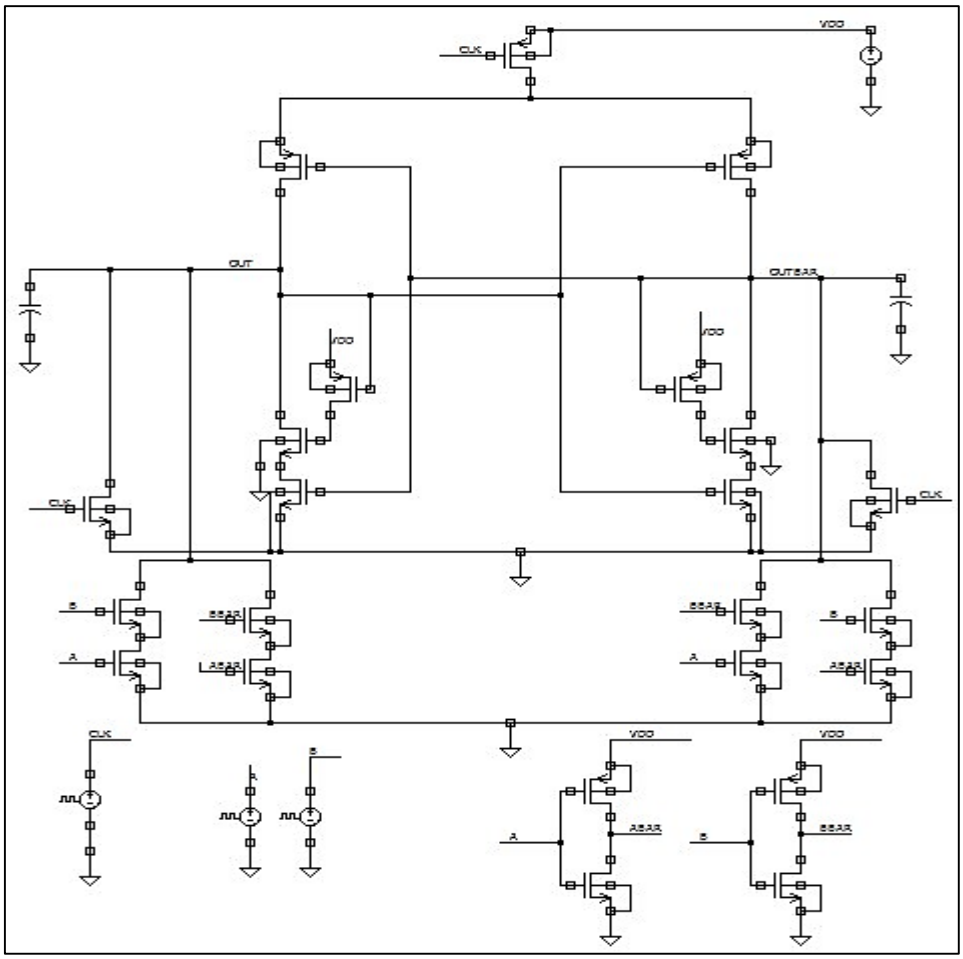

Figure 42: 2-input XOR using O-ECDL architecture

***Simulation Results*:**

Fig. 43 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 48 specifies simulation parameters for 'CLK', 'A' and 'B'.

Table 48:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	1.2	1.2	0
v2	0	0	1.2
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

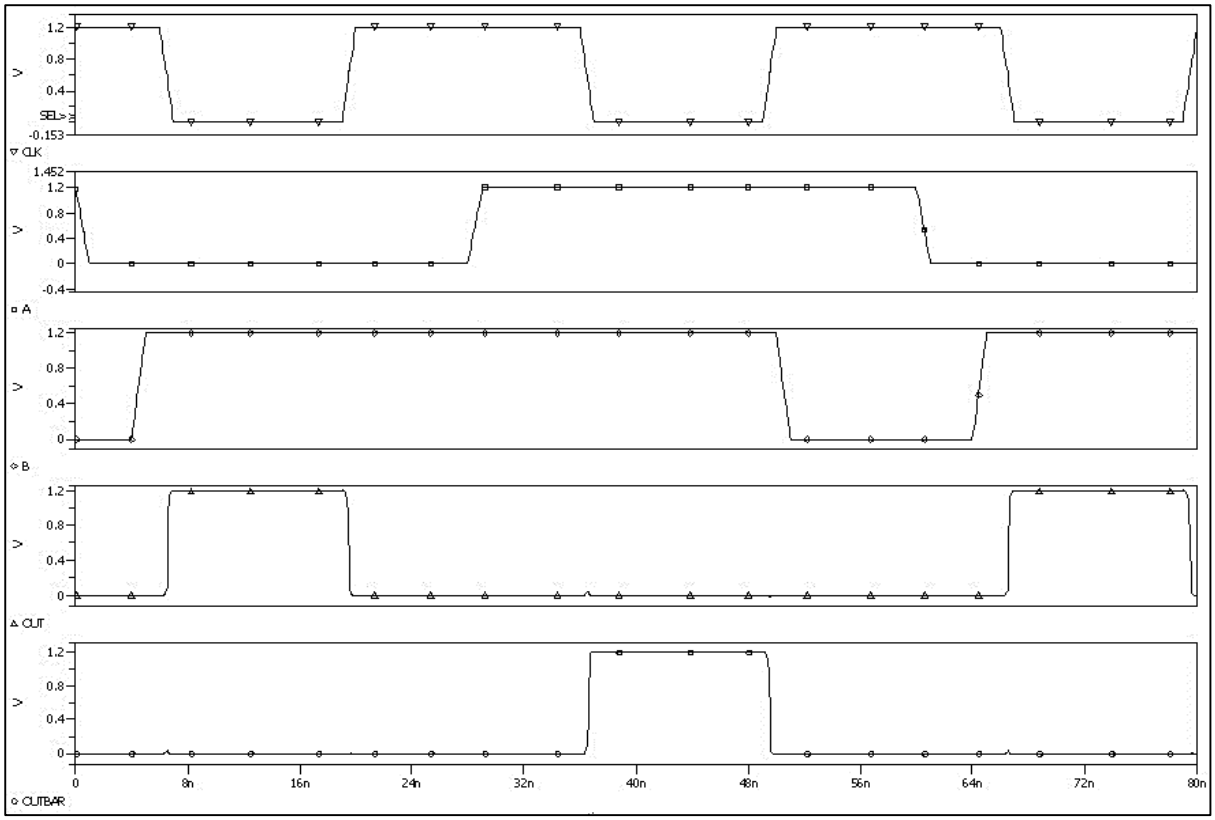

Figure 43: Simulation Output for 2-input XOR using O-ECDL

***Performance Measurement*:**

- Table 49 shows the leakage power for the 2-input XOR O-ECDL structure for various input combinations in enable phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 49:
Leakage Power in O-ECDL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
1	*X*	*X*	*0*	*0*	_	_
0	**0**	**0**	**0**	**1**	**3.872**	**4.646**
0	**0**	**1**	**1**	**0**	**3.49**	**4.188**
0	**1**	**0**	**1**	**0**	**3.872**	**4.6464**
0	**1**	**1**	**0**	**1**	**4.416**	**5.299**

- The delay performance of the 2-input XOR using O-ECDL structure is summarized in Table 50. The input should be stable before the active edge of CLK (-ve edge) so that the OUT in enable stage is correct. In disable phase, OUT= $\overline{OUT} = 0$ in ECDL. Therefore, delay will be '0' if OUT remains '0' in enable phase.

Table 50:
Delay in O-ECDL

CLK	A	B	OUT	Delay (ps)
1	X	X	0	_
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**93.472**
0	**1**	**0**	**1**	**93.468**
0	**1**	**1**	**0**	**0**

(5.4) ONOFIC incorporated Differential Current Switch Logic (O-DCSL)

The operation of ONOFIC incorporated DCSL (O-DCSL) remains same as for conventional DCSL mentioned in Section 3.4. The only effect of incorporating ONOFIC blocks in DCSL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 44 shows the schematic for 2-input O-DCSL XOR with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

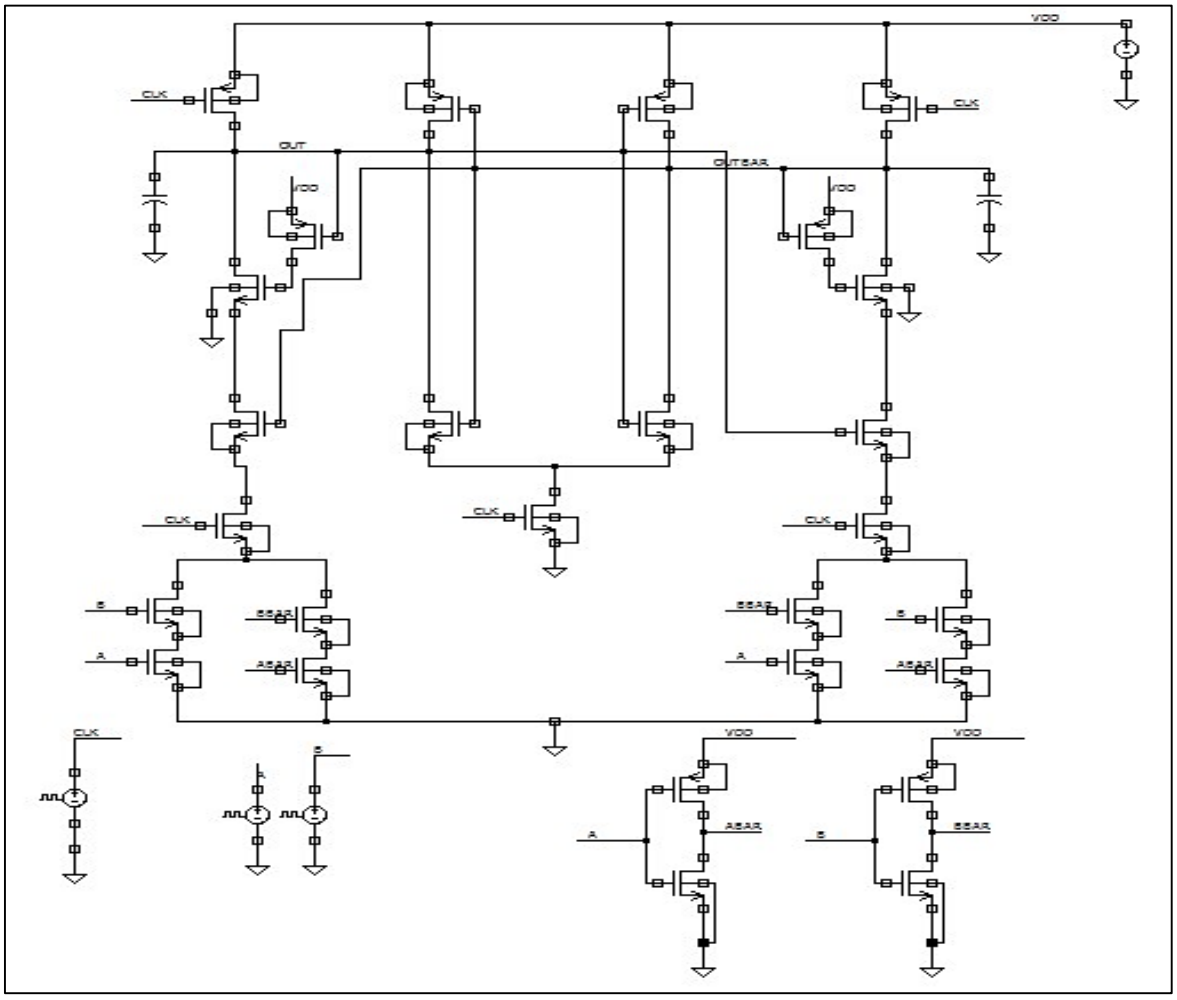

Figure 44: 2-input XOR using O-DCSL architecture

***Simulation Results*:**

Fig. 45 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 51 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 51:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

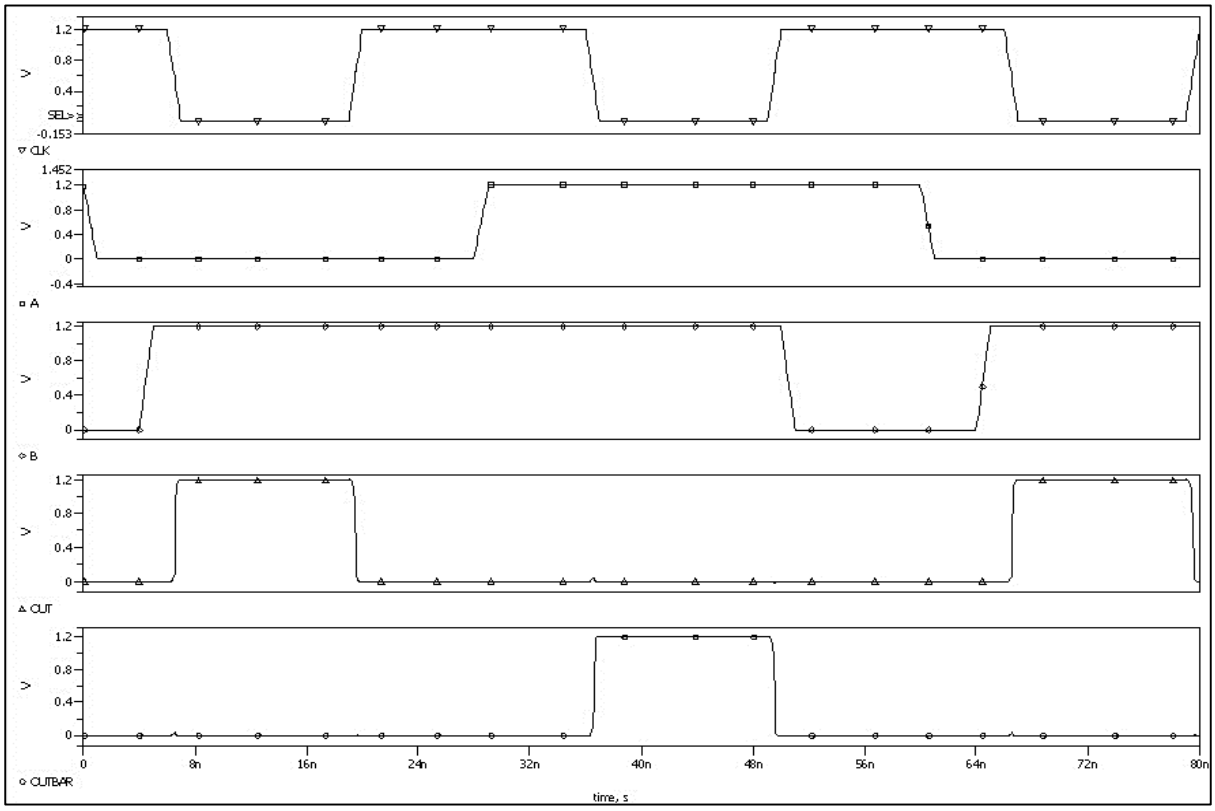

Figure 45: Simulation Output for 2-input XOR using O-DCSL

***Performance Measurement*:**

- Table 52 shows the leakage power for the 2-input XOR O-DCSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 52:
Leakage Power in O-DCSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**5.345**	**6.414**
1	**0**	**1**	**1**	**0**	**4.966**	**5.959**
1	**1**	**0**	**1**	**0**	**4.214**	**5.056**
1	**1**	**1**	**0**	**1**	**4.233**	**5.0793**

- The delay performance of the 2-input XOR using O-DCSL structure is summarized in Table 53. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in DCSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 53:
Delay in O-DCSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**19.991**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**18.757**

(5.5) ONOFIC incorporated Enhanced Differential Cascode Voltage Switch Logic (O-EDCVSL)

The operation of ONOFIC incorporated EDCVSL (O-EDCVSL) remains same as for conventional EDCVSL mentioned in Section 3.5. The only effect of incorporating ONOFIC block in EDCVSL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 46 shows the schematic for 2-input XOR O-EDCVSL with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

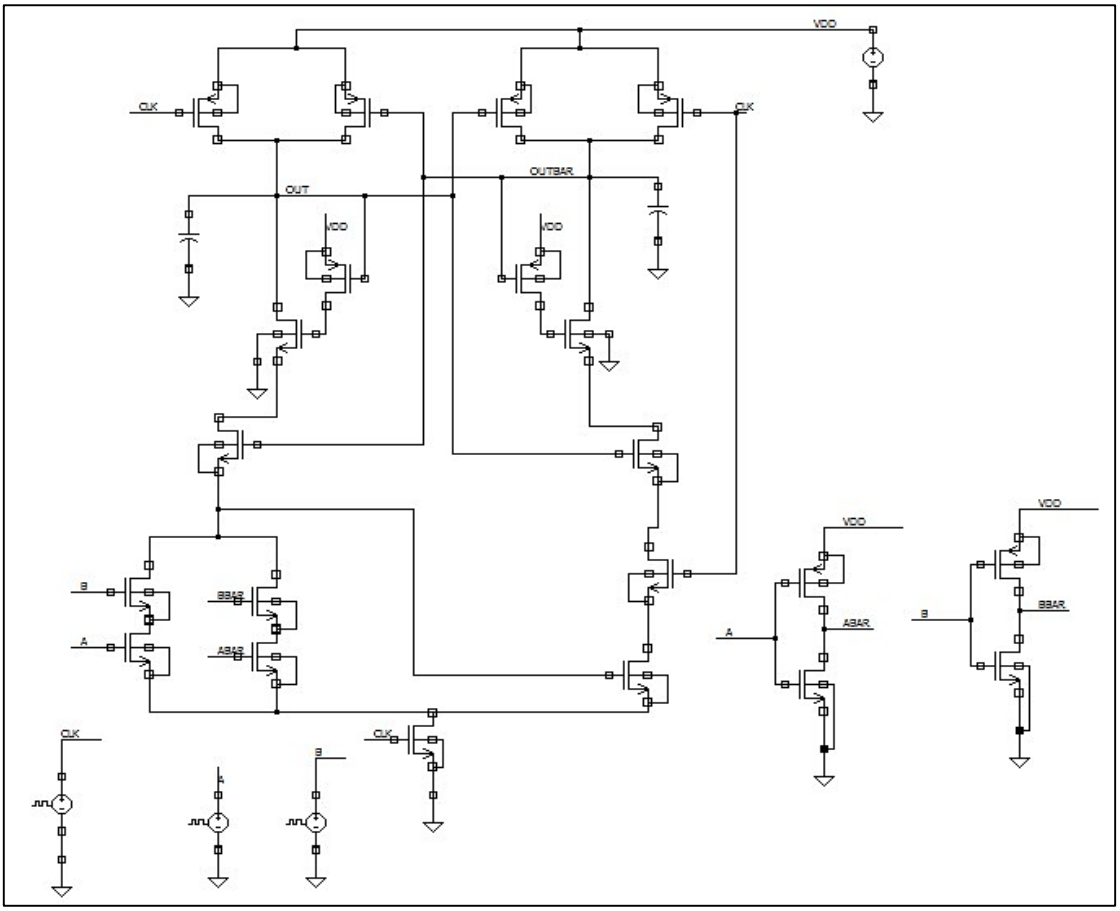

Figure 46: 2-input XOR using O-EDCVSL architecture

***Simulation Results*:**

Fig. 47 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 54 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 54:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

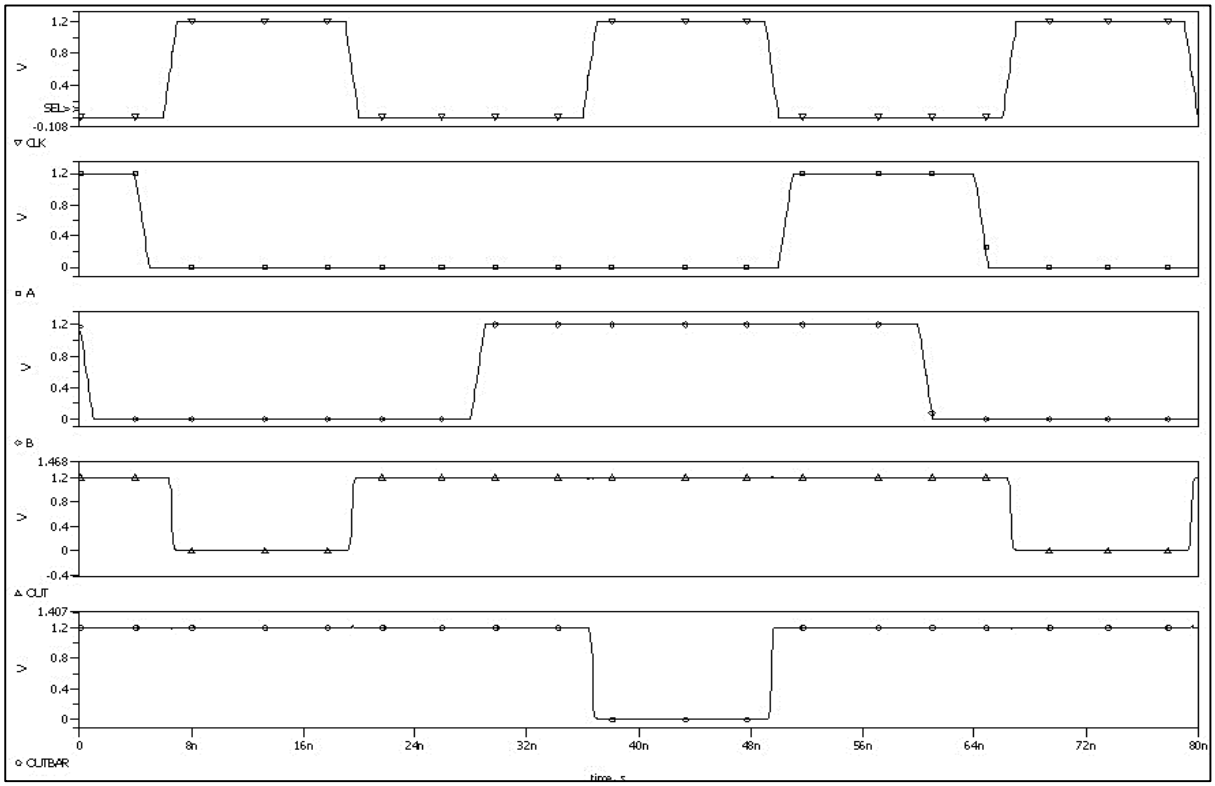

Figure 47: Simulation Output for 2-input XOR using O-EDCVSL

***Performance Measurement*:**

- Table 55 shows the leakage power for the 2-input XOR O-EDCVSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 55:

Leakage Power in O-EDCVSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**4.117**	**4.9404**
1	**0**	**1**	**1**	**0**	**4.361**	**5.233**
1	**1**	**0**	**1**	**0**	**3.479**	**4.1748**
1	**1**	**1**	**0**	**1**	**3.821**	**4.5852**

- The delay performance of the 2-input XOR using O-EDCVSL structure is summarized in Table 56. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in EDCVSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 56:

Delay in O-EDCVSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**81.99**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**92.08**

(5.6) ONOFIC incorporated NP- Mixed DCVSL

The operation of ONOFIC incorporated NP-Mixed DCVSL (O-NP-Mixed) remains same as for conventional NP-Mixed DCVSL mentioned in Section 3.6. The only effect of incorporating ONOFIC block in NP-Mixed DCVSL schematic is on performance of the circuit i.e. leakage power and delay.

***Schematic*:**

A 2-input XOR is used as a design example throughout this thesis to test as well as to compare the functionality and performance of various DCVSL variations. Fig. 48 shows the schematic for 2-input XOR O-NP-Mixed DCVSL with inputs 'A' and 'B' and clock 'CLK' using 90nm technology node at V_{DD} = 1.2V. The W/L for NMOS and PMOS are (135n/90n) and (337.5n/90n) respectively.

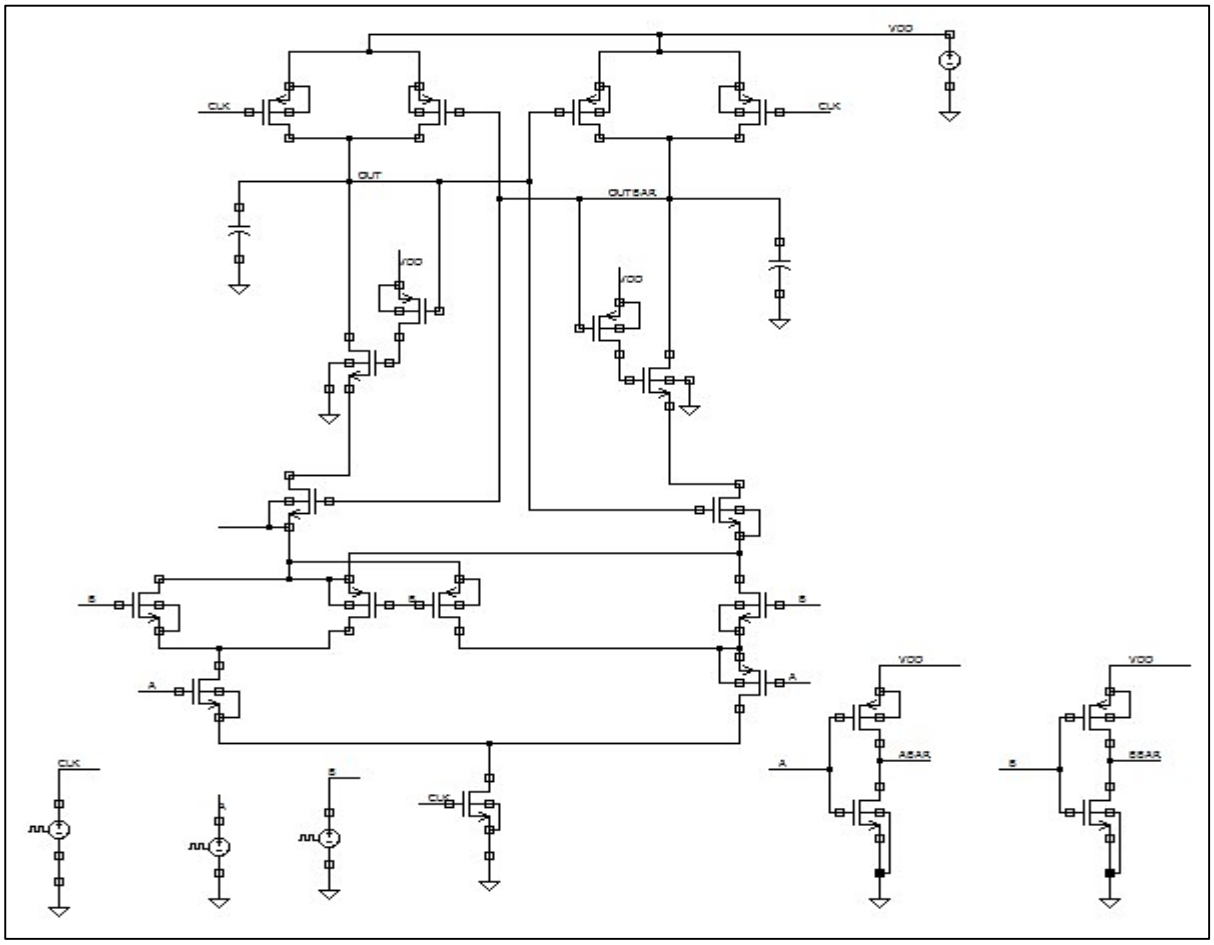

Figure 48: 2-input XOR using O-NP- Mixed DCVSL architecture

***Simulation Results*:**

Fig. 49 shows the waveform of 'OUT' and '$\overline{OUT}$' on the application of input 'A' and 'B'. Table 57 specifies simulation settings for 'CLK', 'A' and 'B'.

Table 57:

Clock and Input Pulse Parameters

Parameters	CLK	A	B
v1	0	1.2	1.2
v2	1.2	0	0
per	30ns	60ns	60ns
td	6ns	0ns	4ns
tr	1ns	1ns	1ns
tf	1ns	1ns	1ns
pw	12ns	27ns	45ns

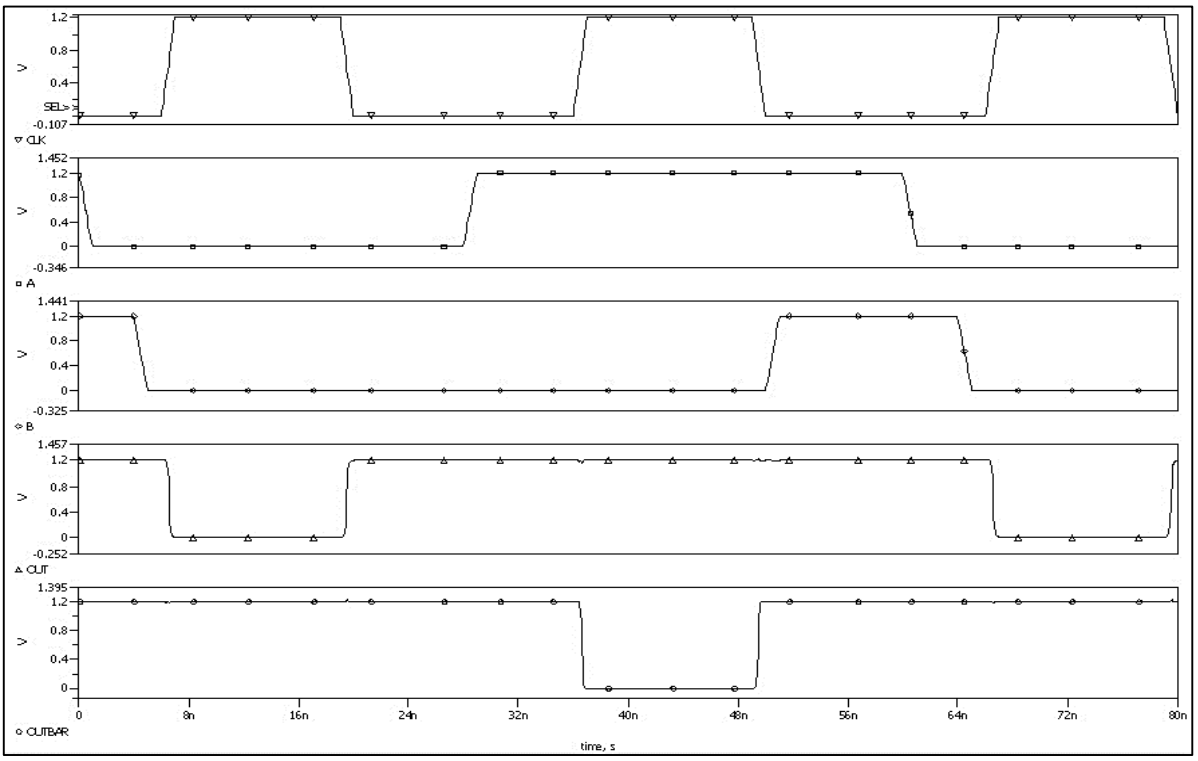

Figure 49: Simulation Output for 2-input XOR using O-NP- Mixed DCVSL

***Performance Measurement*:**

- Table 58 shows the leakage power for the 2-input XOR O-NP- Mixed DCVSL structure for various input combinations in evaluation phase. These results are carried out for 90nm technology node at a temperature of 27°C.

Table 58:

Leakage Power in O-NP- Mixed DCVSL

CLK	A	B	OUT	$\overline{OUT}$	Leakage Current (nA)	Leakage Power (nW)
0	*X*	*X*	*1*	*1*	_	_
1	**0**	**0**	**0**	**1**	**4.911**	**5.8932**
1	**0**	**1**	**1**	**0**	**5.113**	**6.1356**
1	**1**	**0**	**1**	**0**	**5.312**	**6.3744**
1	**1**	**1**	**0**	**1**	**4.998**	**5.9976**

- The delay performance of the 2-input XOR using O-NP- Mixed DCVSL structure is summarized in Table 59. The input should be stable before the active edge of CLK so that the OUT in evaluation stage is correct. In precharge phase, OUT= $\overline{OUT} = 1$ in EDCVSL. Therefore, delay will be '0' if OUT remains '1' in evaluation phase.

Table 59:

Delay in O-NP- Mixed DCVSL

CLK	A	B	OUT	Delay (ps)
0	X	X	1	_
1	**0**	**0**	**0**	**83.14**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**82.93**

Summary

In this chapter, we have seen different variations of ONOFIC incorporated dynamic DCVSL which will be compared with performance results with the conventional DCVSL structures (Chapter 3) and LECTOR incorporated DCVSL (Chapter 4). The operation of different O-DCVSL structures will remain same as those of conventional dynamic DCVSL structures except for the changes in performance introduced by incorporating ONOFIC block. ONOFIC significantly reduces leakage power dissipation (not as well as LECTOR) but the main advantage of this technique is that the increase in delay (not as much as LECTOR) is up to the extent that the PDP improves when compared to conventional dynamic DCVSL structures of Chapter 3. This can be seen in the summarized result of this chapter given in Table 60.

It can be inferred from Table 20, Table 40 and Table 60 that leakage power decreases in case of ONOFIC incorporated DCVSL variants when compared to conventional DCVSL variants. But the drawback of this is seen as an increase in delay which is lower than in the case of LECTOR incorporated DCVSL. Thus, this results in PDP of ONOFIC incorporated dynamic DCVSL below conventional dynamic DCVSL.

Table 60:

Summarized Results of Chapter 5

2-input XOR using	No. of Transistors			Leakage Power (nW)	Delay (ps)	PDP (aJ)
	NMOS	PMOS	Total			
O-SSDL	19	9	28	3.913	87.01	0.231
O-MSSDL	21	9	30	5.126	42.25	0.216

O-ECDL	**16**	**7**	**23**	**4.595**	**93.47**	**0.439**
O-DCSL	**19**	**8**	**27**	**5.627**	**19.374**	**0.109**
O-EDCVSL	**13**	**8**	**21**	**4.733**	**87.035**	**0.412**
O-NP-Mixed	**10**	**11**	**21**	**6.101**	**83.035**	**0.506**

Chapter 6

Relative Performance Results

In this chapter, a relative performance of dynamic DCVSL structures has been done in their conventional, LECTOR incorporated and ONOFIC incorporated form. As mentioned earlier, a two-input XOR has been implemented for a relative study. Symica DE has been used for simulation and performance measurement at 90nm technology node. The performance analysis is performed at V_{DD}= 1.2V, temperature of 27^{o}C and using 90nm PTM model. Leakage power dissipation, delay and PDP (figure of merit) has been shown in subsequent sections.

(6.1) SSDL vs. L-SSDL vs. O-SSDL

- **Leakage Power**

  Fig. 50 shows Leakage Power consumption in nW for 2-input XOR in SSDL, L-SSDL and O-SSDL. It can be seen that L-SSDL has least leakage power dissipation.

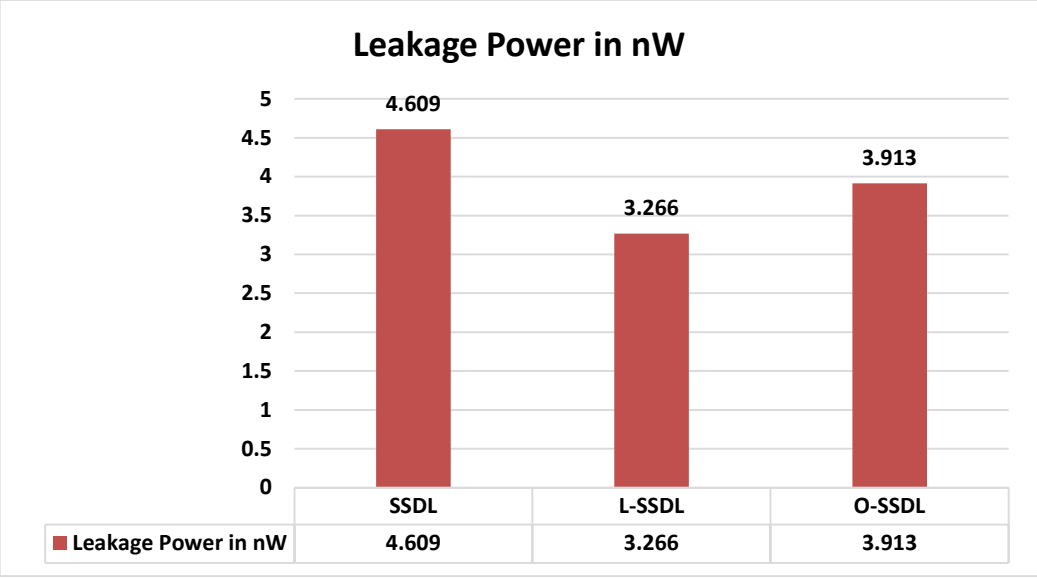

Figure 50: Leakage Power in SSDL structures

Delay

Fig. 51 shows delay in ps for 2-input XOR in SSDL, L-SSDL and O-SSDL. It can be seen that O-SSDL has delay between L-SSDL and conventional SSDL.

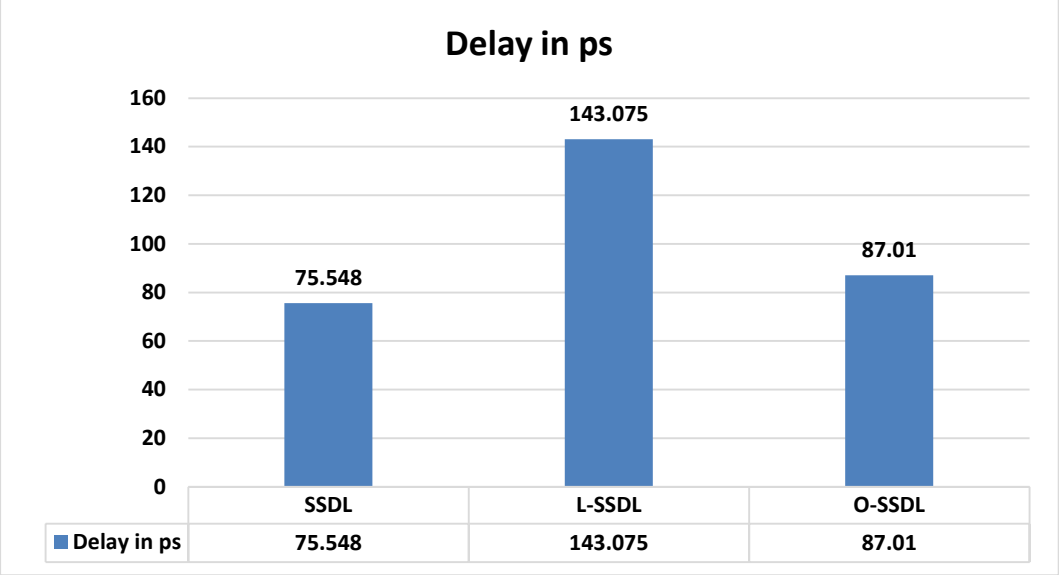

Figure 51: Delay in SSDL structures

- **Power-Delay Product (PDP)**

Fig. 52 shows power-delay product in aJ for 2-input XOR in SSDL, L-SSDL and O-SSDL. O-SSDL is the clear winner in this case.

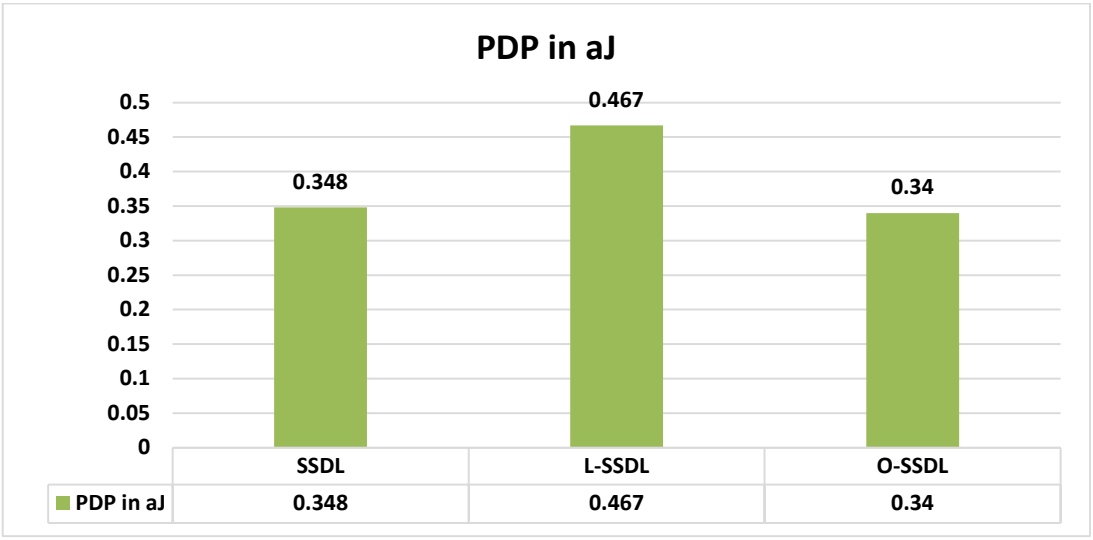

Figure 52: PDP in SSDL structures

(6.2) MSSDL vs. L-MSSDL vs. O-MSSDL

- **Leakage Power**

Fig. 53 shows Leakage Power consumption in nW for 2-input XOR in MSSDL, L-MSSDL and O-MSSDL. It can be seen that L-MSSDL has least leakage power dissipation.

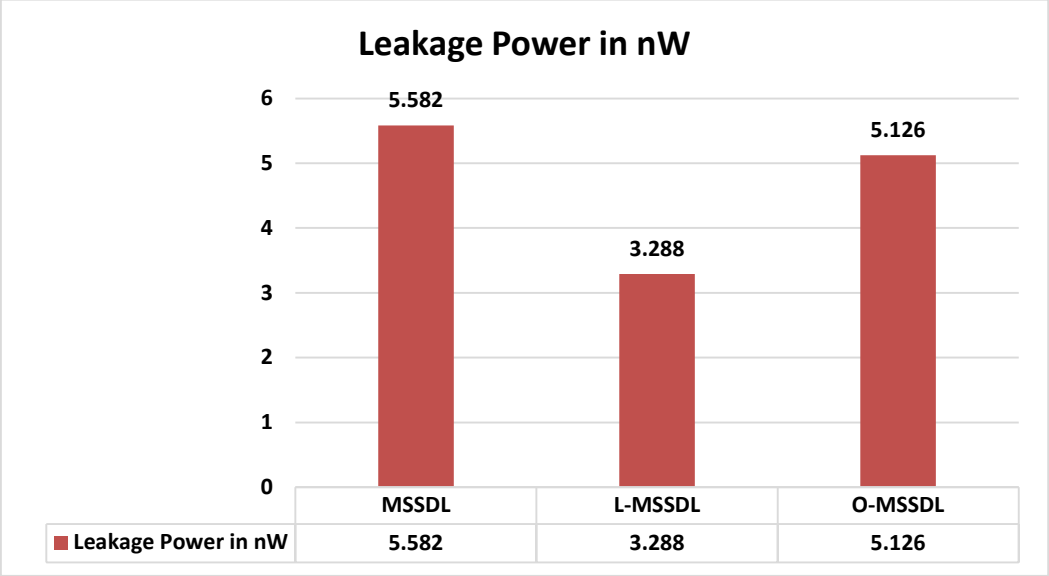

Figure 53: Leakage Power in MSSDL structures

- **Delay**

Fig. 54 shows delay in ps for 2-input XOR in MSSDL, L-MSSDL and O-MSSDL. O-MSSDL has delay between MSSDL and L-MSSDL. Clearly, MSSDL has delay between MSSDL and L-MSSDL.

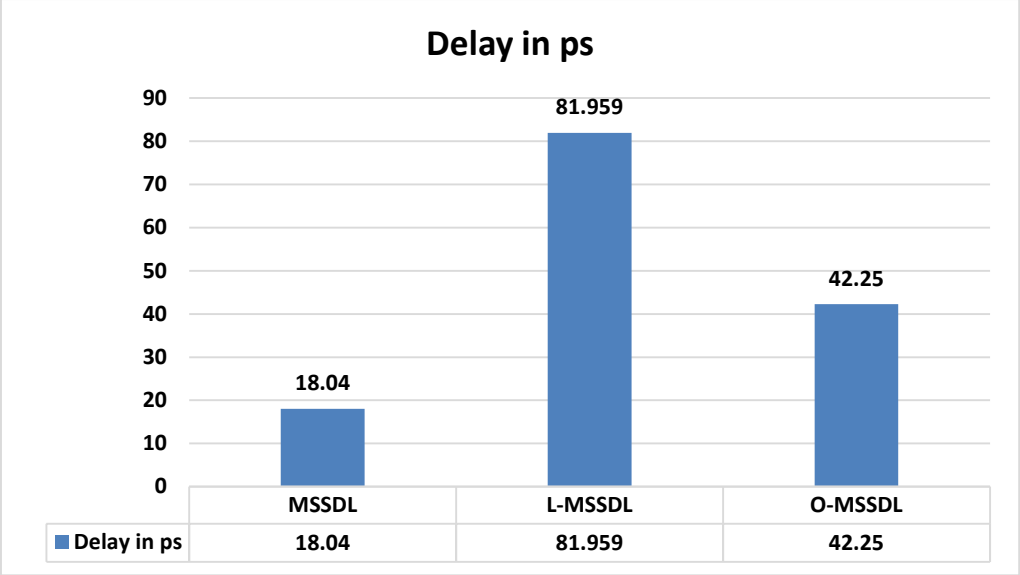

Figure 54: Delay in MSSDL structures

- **Power-Delay Product (PDP)**

Fig. 55 shows power-delay product in aJ for 2-input XOR in MSSDL, L-MSSDL and O-MSSDL. Both LECTOR and ONOFIC approach has more PDP than conventional MSSDL which is undesired.

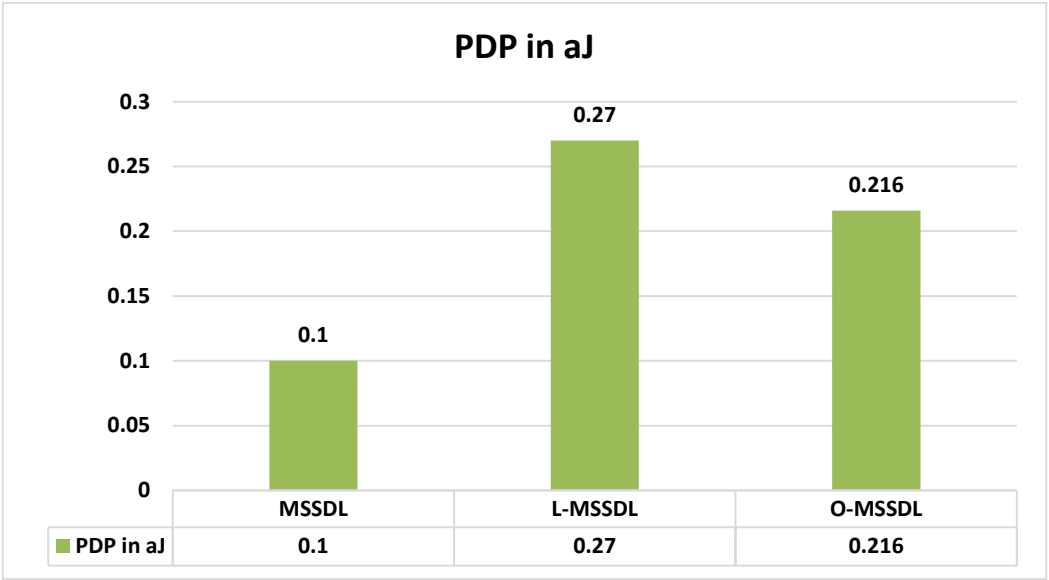

Figure 55: PDP in MSSDL structures

(6.3) ECDL vs. L-ECDL vs. O-ECDL

- **Leakage Power**

Fig. 56 shows Leakage Power consumption in nW for 2-input XOR in ECDL, L-ECDL and O-ECDL. It can be seen that O-ECDL has least leakage power dissipation.

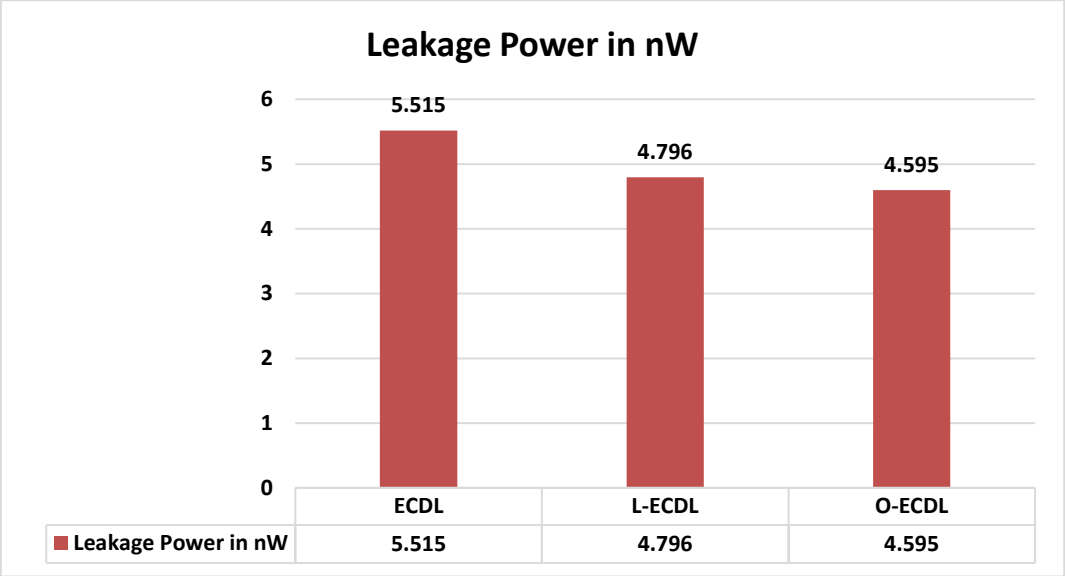

Figure 56: Leakage Power in ECDL structures

- **Delay**

Fig. 57 shows delay in ps for 2-input XOR in ECDL, L-ECDL and O-ECDL. O-ECDL has delay between ECDL and L-ECDL.

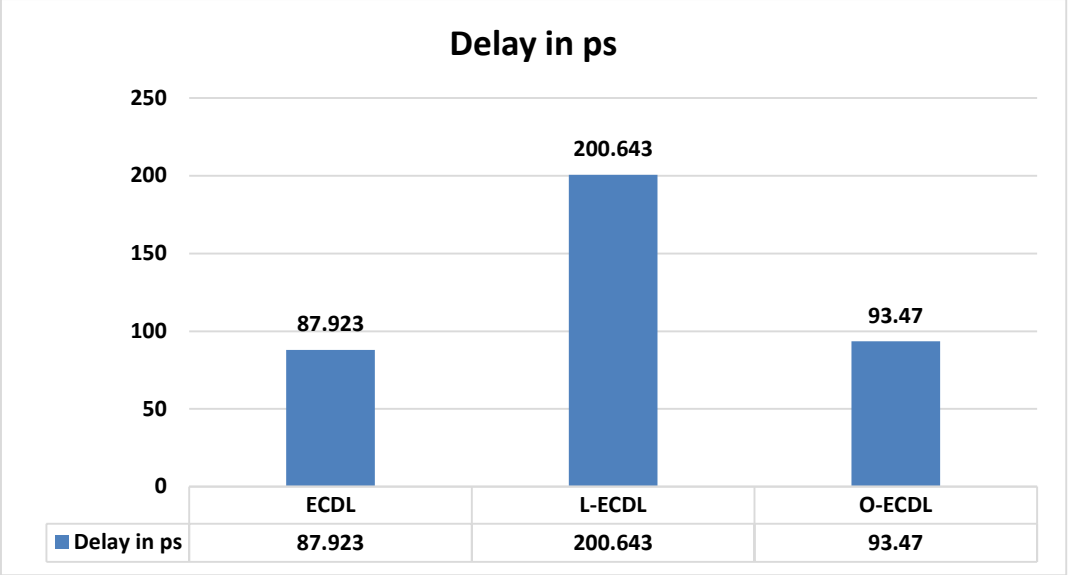

Figure 57: Delay in ECDL structures

- **Power-Delay Product (PDP)**

Fig. 58 shows power-delay product in aJ for 2-input XOR in ECDL, L-ECDL and O-ECDL. Clearly, O-ECDL offers best PDP.

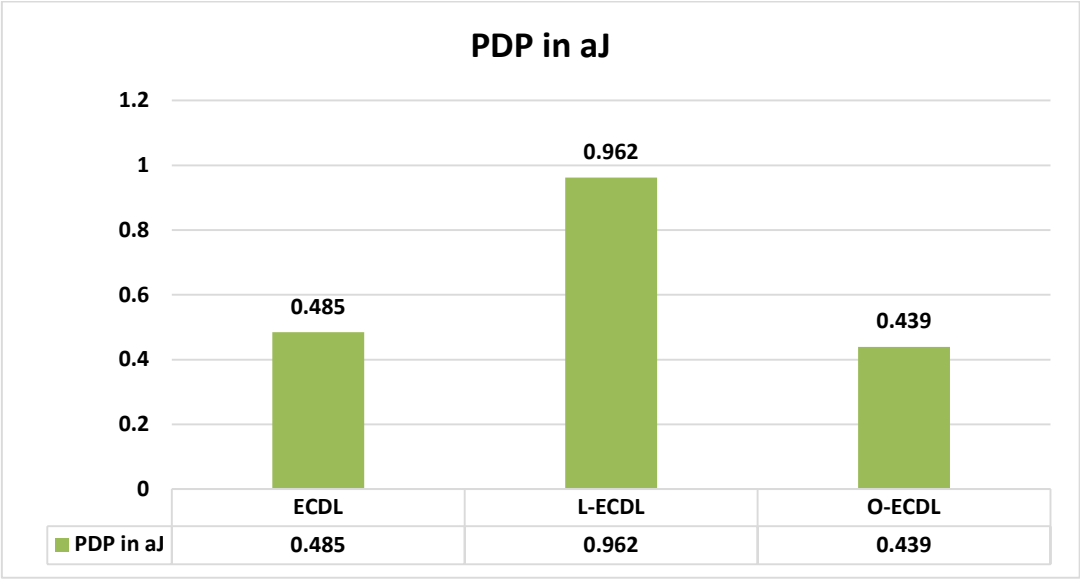

Figure 58: PDP in ECDL structures

(6.4) DCSL vs. L-DCSL vs. O-DCSL

- **Leakage Power**

Fig. 59 shows Leakage Power consumption in nW for 2-input XOR in DCSL, L-DCSL and O-DCSL. It can be seen that L-DCSL has least leakage power dissipation.

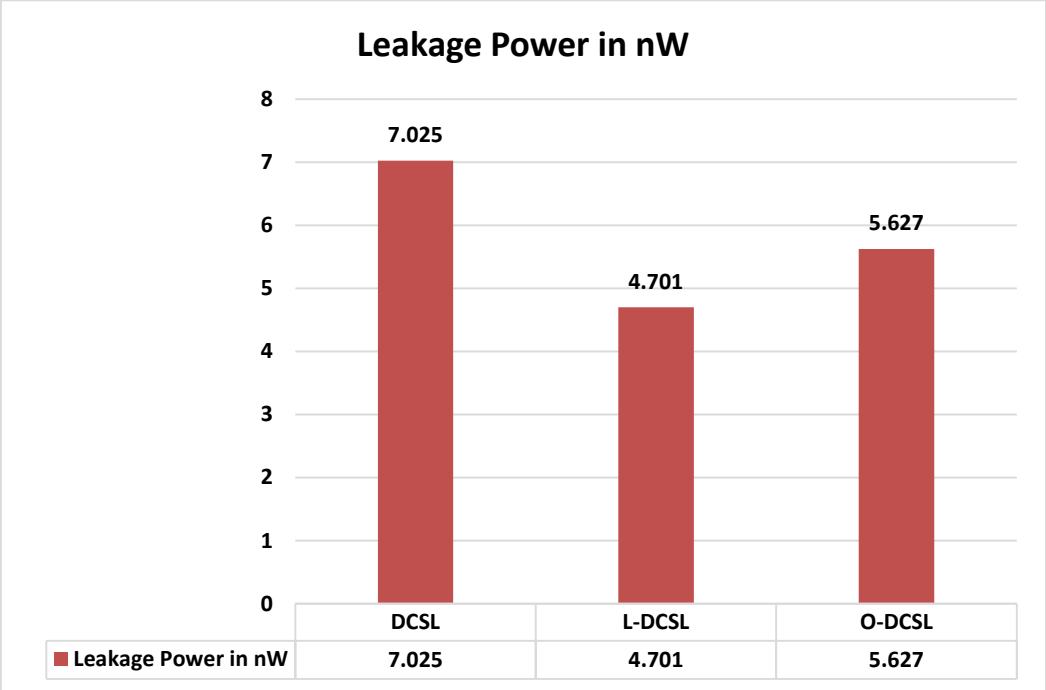

Figure 59: Leakage Power in DCSL structures

- **Delay**

Fig. 60 shows delay in ps for 2-input XOR in DCSL, L-DCSL and O-DCSL. O-DCSL has delay between DCSL and L-DCSL.

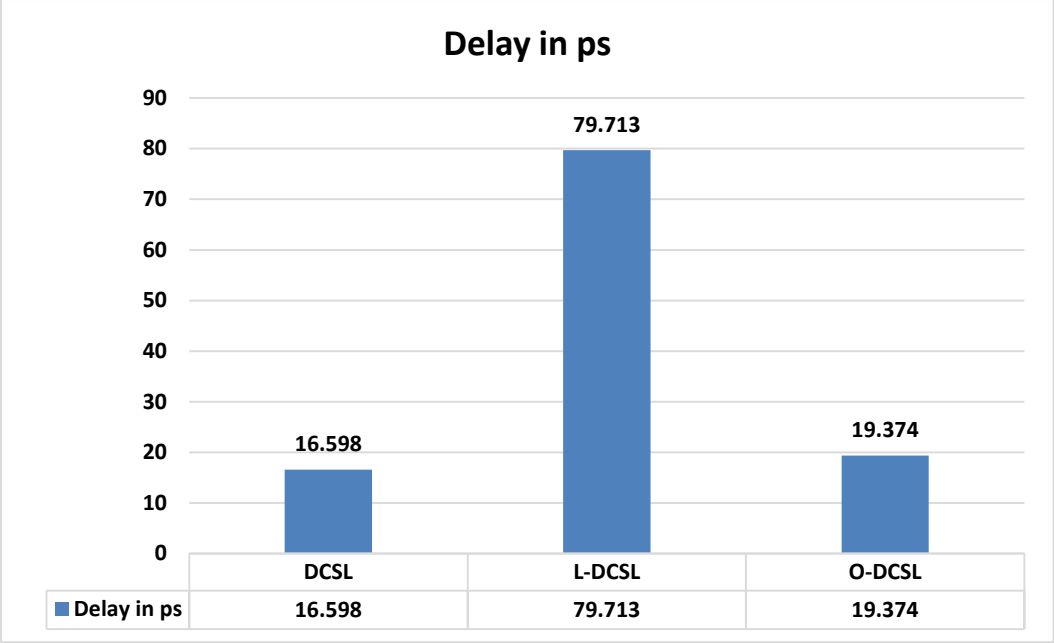

Figure 60: Delay in DCSL structures

- **Power-Delay Product (PDP)**

Fig. 61 shows power-delay product in aJ for 2-input XOR in DCSL, L-DCSL and O-DCSL. Clearly, O-DCSL offers best PDP. LECTOR in this configuration is not at all effective.

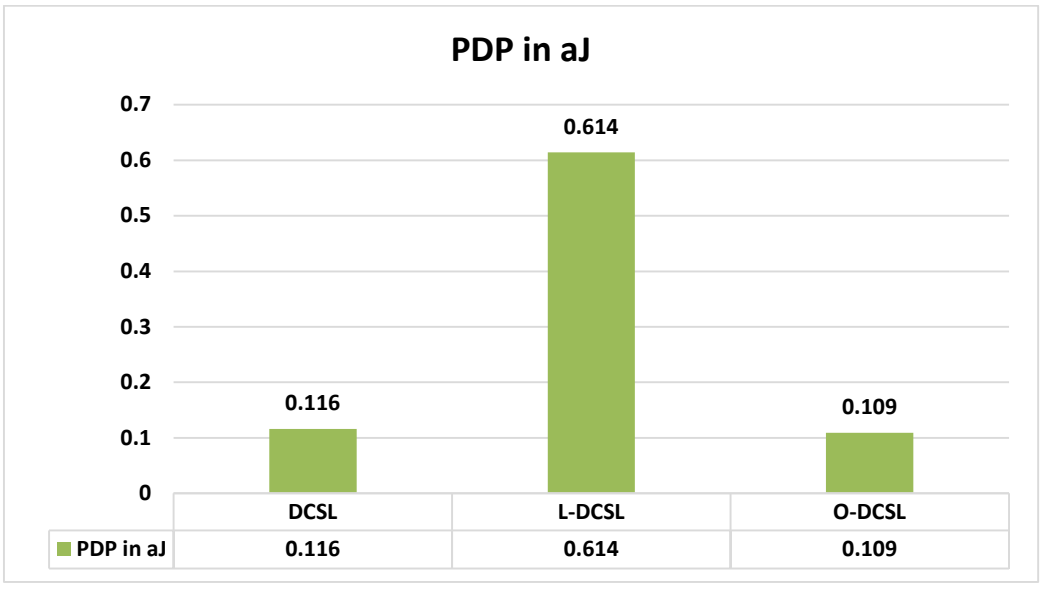

Figure 61: PDP in DCSL structures

(6.5) EDCVSL vs. L-EDCVSL vs. O-EDCVSL

- **Leakage Power**

Fig. 62 shows Leakage Power consumption in nW for 2-input XOR in EDCVSL, L-EDCVSL and O-EDCVSL. It can be seen that O-EDCVSL has least leakage power dissipation.

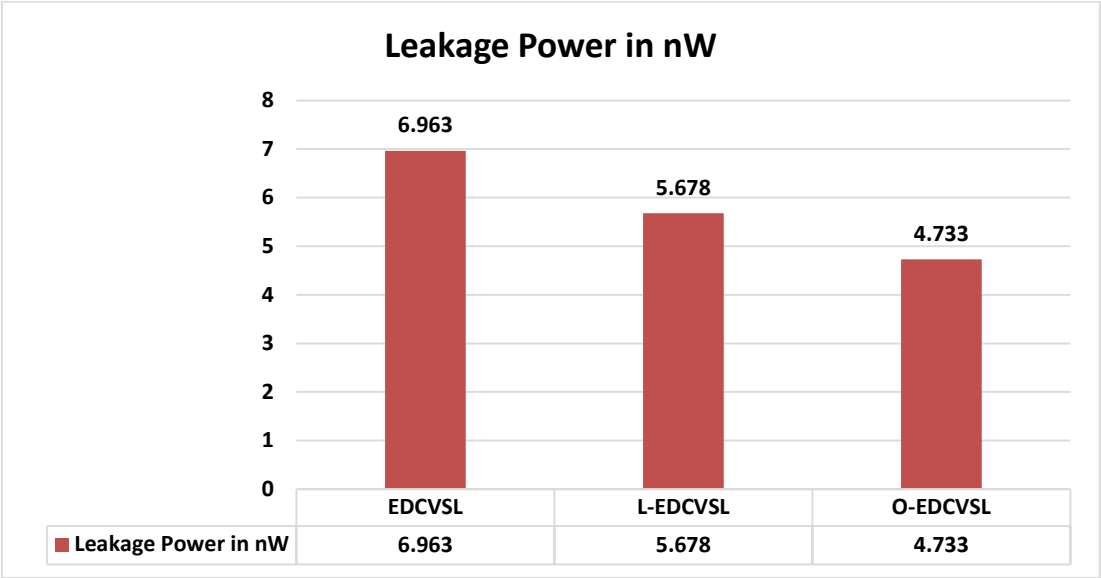

Figure 62: Leakage Power in EDCVSL structures

- **Delay**

Fig. 63 shows delay in ps for 2-input XOR in EDCVSL, L-EDCVSL and O-EDCVSL. O-EDCVSL has maximum delay.

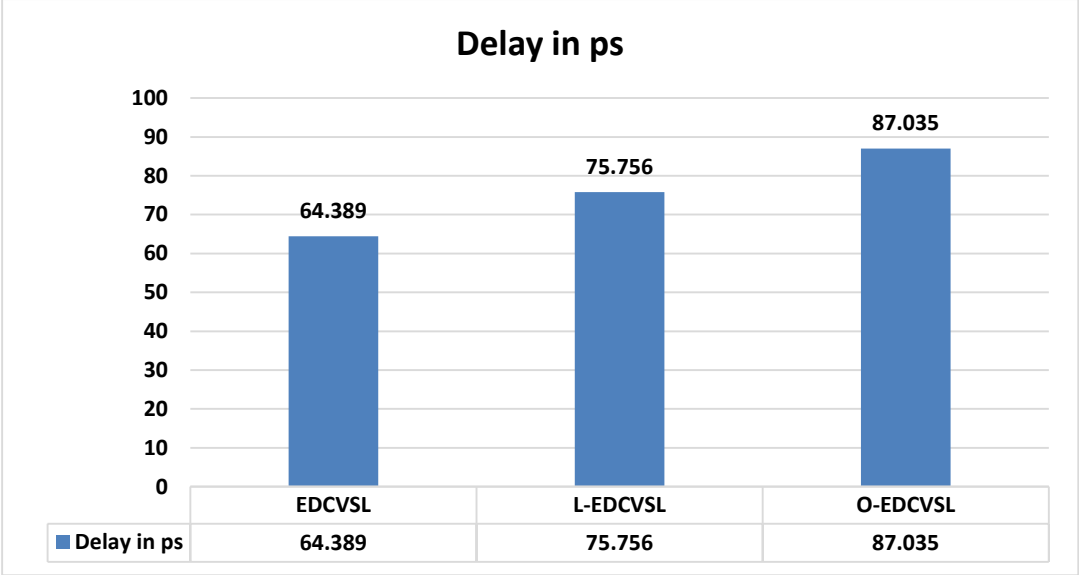

Figure 63: Delay in EDCVSL structures

- **Power-Delay Product (PDP)**

Fig. 64 shows power-delay product in aJ for 2-input XOR in EDCVSL, L-EDCVSL and O-DCVSL. Clearly, O-DCSL offers best PDP.

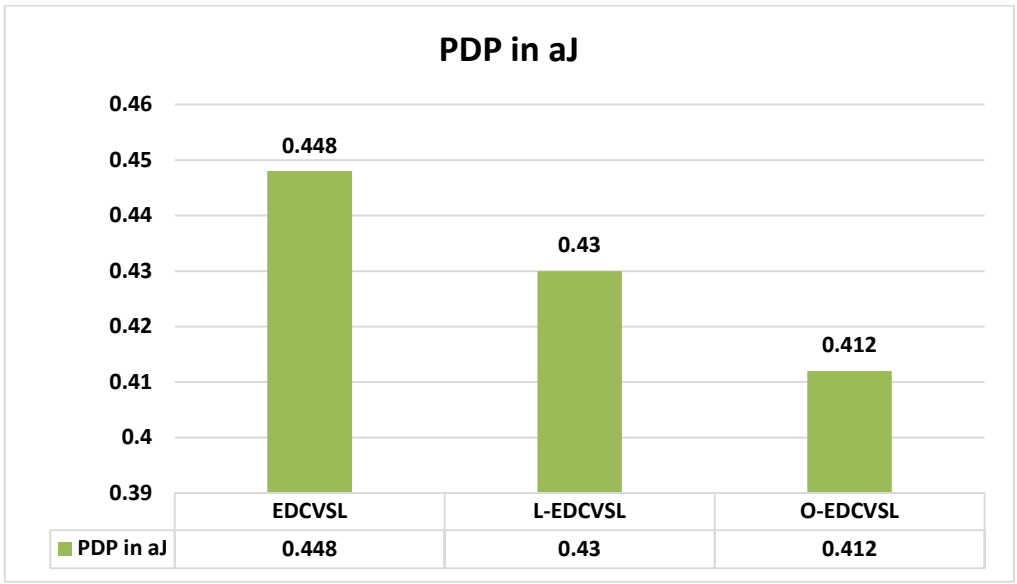

Figure 64: PDP in EDCVSL structures

(6.6) NP-Mixed vs. L-NP-Mixed vs. O-NP-Mixed

- **Leakage Power**

Fig. 65 shows Leakage Power consumption in nW for 2-input XOR in NP-Mixed, L-NP-Mixed and O-NP-Mixed. It can be seen that O-NP-Mixed has least leakage power dissipation.

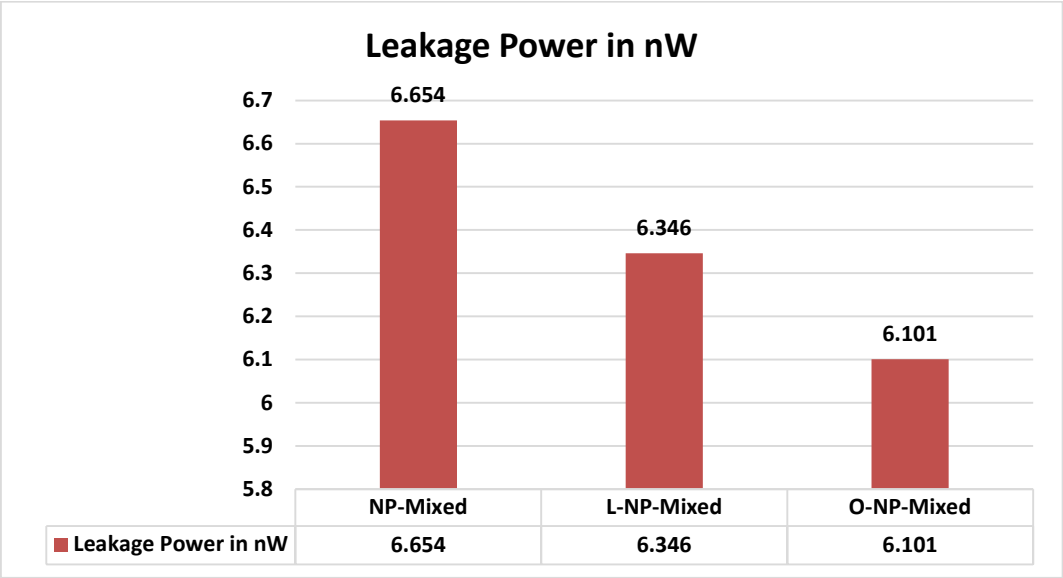

Figure 65: Leakage Power in NP-Mixed structures

- **Delay**

Fig. 66 shows delay in ps for 2-input XOR in NP-Mixed, L-NP-Mixed and O-NP-Mixed. O-NP-Mixed has delay between the other two.

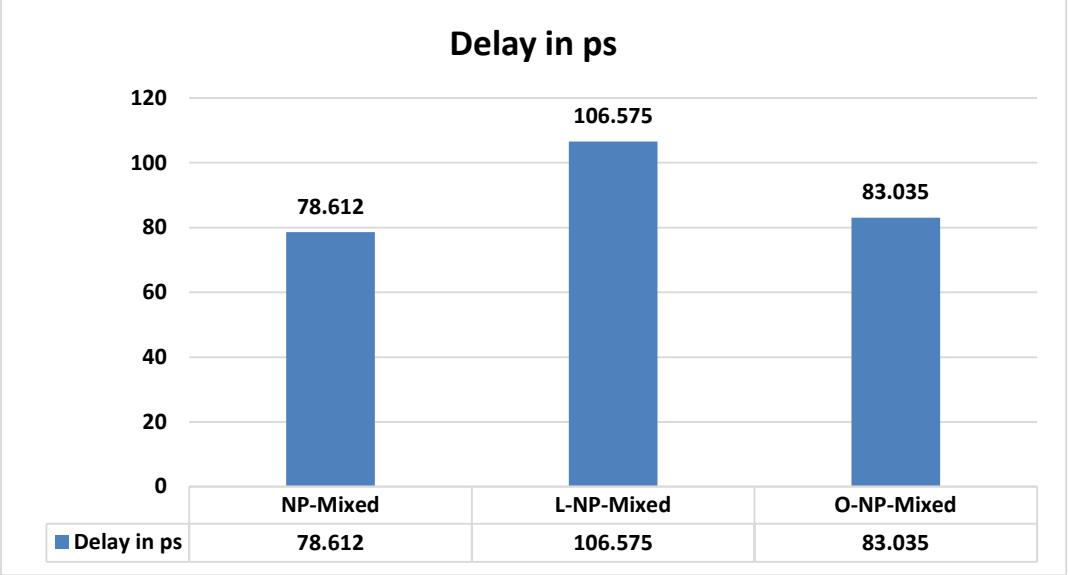

Figure 66: Delay in NP-Mixed structures

- **Power-Delay Product (PDP)**

Fig. 67 shows power-delay product in aJ for 2-input XOR in NP-Mixed, L-NP-Mixed and O-NP-Mixed. Clearly, O-NP-Mixed offers best PDP.

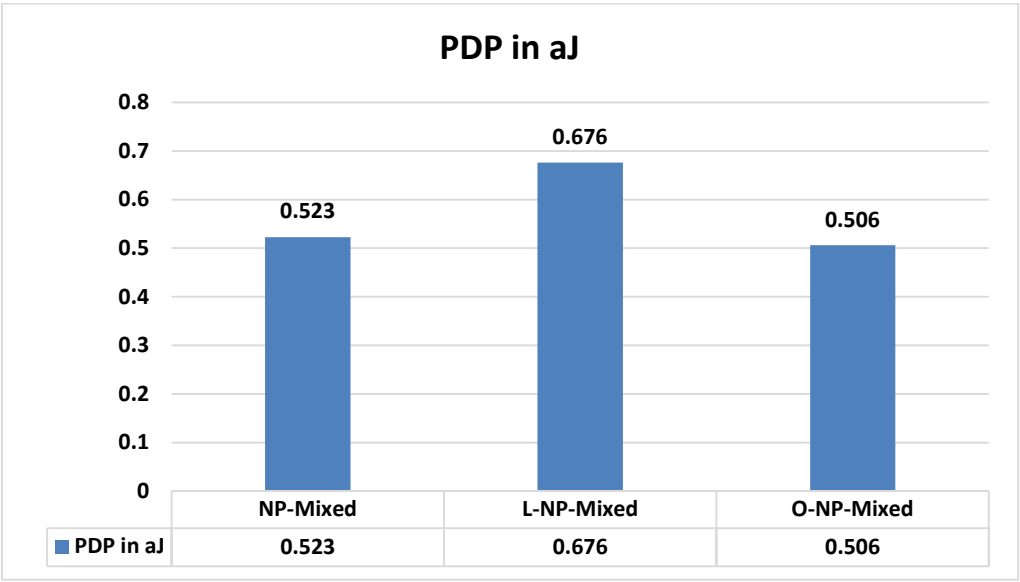

Figure 67: PDP in NP-Mixed structures

Chapter 7

Conclusion

This thesis work presents various dynamic DCVSL structures, explains their advantages over conventional techniques. The work also focuses on leakage power reduction technique which is the need of era. Thus, this work proposes ONOFIC leakage reduction technique which is implemented on various dynamic DCVSL structures. The ONOFIC incorporated structures proved to offer better power-delay product (PDP) when compared to conventional structures. The incorporation of ONOFIC block in these structures removed the drawback of some leakage power reduction technique like LECTOR technique which decreased the leakage power but failed to keep PDP of these structures below conventional structures. LECTOR technique has been one of the best leakage power reduction technique which is the reason behind including LECTOR incorporated structures in this thesis for a fair comparison.

2-input XOR have been used as a test circuit throughout the thesis. Simulations have been performed using Symica DE in 90nm technology node. Various dynamic DCVSL structures are proposed using ONOFIC block which have their own merits and demerits. Table 61 on the next page summarizes the final results observed. These results depend on circuit topologies so these results may not be similar always. Yet, these results gives sufficient information to understand the leakage power dissipation problem which is increasing with the decrease in technology node.

Table 61:

Final Results

2-input XOR using	No. of Transistors			Leakage Power (nW)	% Saving of leakage power dissipation	Delay (ps)	Delay Penalty	PDP (aJ)	% Change in PDP
	NMOS	PMOS	Total						
SSDL	17	7	24	4.609	----	75.548	----	0.348	----
L-SSDL	19	9	28	3.266	29.14	143.075	1.89X	0.467	+34.2
O-SSDL	19	9	28	3.913	15.10	87.01	1.15X	0.231	-33.6
MSSDL	19	7	26	5.582	----	18.04	----	0.1	----
L-MSSDL	21	9	30	3.288	41.09	81.959	4.54X	0.27	+170
O-MSSDL	21	9	30	5.126	8.17	42.25	2.34X	0.216	+116
ECDL	14	5	19	5.515	----	87.923	----	0.485	----
L-ECDL	16	7	23	4.796	13.04	200.643	2.28X	0.962	+93.4
O-ECDL	16	7	23	4.595	16.68	93.47	1.06X	0.439	-9.5
DCSL	17	6	23	7.025	----	16.598	----	0.116	----
L-DCSL	19	8	27	4.701	33.08	79.713	4.8X	0.614	+429.3
O-DCSL	19	8	27	5.627	19.90	19.374	1.16X	0.109	-6
EDCVSL	11	6	17	6.963	----	64.389	----	0.448	----
L-EDCVSL	13	8	21	5.678	18.45	75.756	1.18X	0.43	-4
O-EDCVSL	13	8	21	4.733	32.03	87.035	1.35X	0.412	-8.1
NP-Mixed	8	9	17	6.654	----	78.612	----	0.523	----
L-NP-Mixed	10	11	21	6.346	4.63	106.575	1.36X	0.676	+29.3
O-NP-Mixed	10	11	21	6.101	8.31	83.035	1.05X	0.506	-3.3

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