Major Project
Report

High Power Handling Tunable Low Pass Filter

Submitted in partial fulfillment of
the requirements for the award of the degree of

Master of Technology
in
Microwave and Optical Communication Engineering

Submitted by
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July 2017

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Certificate

This is to certify that the Major project report entitled **"HIGH POWER HANDLING TUNABLE LOW PASS FILTER"** is a bonafide work carried out by **Mr.Manisha Nand** bearing Roll No.**2K15/MOC/11**, a student of Delhi Technological University, in partial fulfillment of the requirements for the award of Degree in **Master of Technology** in **Microwave and Optical Communication Engineering.**

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Declaration

I hereby declare thay all the information in this document has been obtained and presented in accordance with academic rules and ethical conduct. This report is my own, unaided work. I have fully cited and referenced all material and results that are not original to this work. It is being submitted for the degree of Master of Technology in Engineering at Delhi Technological University. It has not been submitted before for any degree or examination in any other university.

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Abstract

The goal of high-efficiency power amplifier operation from 30-520 MHz has been addressed in the current design by the use of tunable reactive elements in the output resonant network. Filtering at the target harmonic frequencies will be achieved by maintaining a fixed inductance and utilizing a PIN diode switching circuit to selectively introduce different capacitance values, presenting the frequency-specific short and open circuits that will allow for power amplifier operation at the desired fundamental frequency. This approach allows the power amplifier to cover several octaves or more, achieving operation across a wide bandwidth and greatly increasing the flexibility of the design for possible use in other frequency ranges.

The first chapter gives the overview and objective of the filter. The specifications of the filter required is listed in this chapter.

The second chapter gives an idea about the literature, several types of technologies used for tuning, how pin diode can be used as a switch, variation of series resistance with frequency.

The third chapter has several methods of designing the filter ,filter banks, and which is suitable for desired specification.

The fourth chapter includes design of schematic in PADS and simulation in simulation software ADS, tuning process.

At the end the last two chapters includes the response output of network analyser and the project is concluded in the last chapter.

Acknowledgments

It gives me immense pleasure to express my deepest sense of gratitude and sincere thanks to my highly respected and esteemed guide **Asst. Professor Dr. Priyanka Jain**, for her valuable guidance, encouragement and help for completing this work. Her useful suggestions for this whole work and co-operative behavior are sincerely acknowledged.

I am very lucky to be able to work with **Mr. Arun Verma**, he was truly inspiring and such a humble person I owe a lot to him, his ideas inspired me a lot. Even when he was busy he spared time for clearing my doubts, giving me problems to solve. I am looking forward to work with new areas along with him. Along with that,I would like to thank **Mr. Akhil** for funding my project. He never hesitated to take my requirements and ensure timely delivery of the components.

I got a lot of support in designing my module from experts in respective areas. I am thankful to **Mr. Pranavesh** for clearing my doubts in course of designing the RF and digital schematic and **Miss. Vinusha** for helping me in PCB layout.

Finally I would like to express my sincere thanks to my parents and friends who helped me directly or indirectly during this project work.

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Chapter 1

Introduction

1.1 Overview

Filters play an important role in many applications RF / microwave. They are used to separate or combine different frequencies. The electromagnetic spectrum is limited and has to be shared. Filters are used to select or limit the spectrum RF / microwave within the limits assigned. Emerging applications such as wireless communications continue to challenge the filters RF / microwave with increasingly demanding requirements of higher performance, smaller size, lighter weight and lower cost. Depending on the requirements and specifications, filters RF / microwave may be designed as concentrated or distributed circuit elements [1], They can be made in various structures of transmission lines, such as a waveguide, the coaxial line and micro strip.

Filter type is defined with frequency, allowing or reject. There are low pass, high pass, bandpass and bandstop filters with different types of performing frequency selectivity. Historically, filters were first discrete inductors (L) and capacitors (C) for applying radio frequency (RF). Today, lumped element filters remain in use in the frequency range of 50 MHz to 2 GHz. The simplicity of design, production and low cost are the main advantages of using these type of filters. They can often be very compact compared to filters based on resonators half wave structures and have no "natural" appearing in modes other technologies such as planar filter resonator structures[2]. However, the output characteristics of lumped elements filters suffer from low quality factor (Q) components. Although the values of Q increase inductors and capacitors modern even hundreds, are kept well below Q of thousands that have cavity filters.

1.2 Objective

The main objective of this project is to design, simulate and fabricate a tunable low pass filter for wide frequency band in the V/UHF range of 30-520 MHz frequency band which meets the the specification requirements in software defined radios(SDRs) for military purpose. Agilent Advanced Designed System(ADS) is used for simulation of the filter and shows its response.

Requirements are:

- Design a Tunable low pass filter for frequency band 30-520 MHz with S21(RF_IN RF_OUT) > -1.8dB, S11 < -15dB, S21(All harmonics) < -60dB.
- Choose components within the constraints of available technology, i.e use of lumped elements, limit Q values of component to those that are commonly available for production.

1.3 Motivation

In today RF environments, tunable microwave filters are attracting more attention for research and development because of the emergence of multiple frequency bands in different regions and different applications.It is important for the receivers and transceivers that operate throughout the frequency spectrum to have maximum tuning range and save filtering features, While the frequency is tuned[3].

Common applications for tunable filters include software defined radios,multi-band transceivers, cognitive radio (CR) systems, next generation cell phones, wide-band radars and satellite payloads.

Chapter 2

Literature Review

2.1 Low Pass Filter

A Low Pass Filter can be a combination of capacitance, inductance or resistance intended to produce high attenuation above a specified frequency and little or no attenuation below that frequency. The frequency at which the transition occurs is called the "cut-off" or "corner" frequency. The simplest low pass filters consist of a resistor and capacitor but more sophisticated low pass filters have a combination of series inductors and parallel capacitors.

2.2 Tunable Filter Technology

Microwave tunable filters can be realized by different types of technologies by using:

- Mechanical tuning
- Yttrium-iron-garnet filter (YIG)
- Barium Strontium Titanate filter (BST)
- MEMS tunable capacitors (Micro-Electro-Mechanical System)
- Varactor diodes
- Digitally Tunable Capacitors

2.2.1 Mechanically tunable filters

Mechanically tunable filters are the earliest type of tunable filters. Generally speaking, the tuning mechanism is physically moving a material or tuning screws to affect the resonant frequency of a coaxial, cavity or waveguide resonator. As illustrative tuning methods presented in [4]-[5], by using piezoelectric transducers/actuators, a dielectric slab which can either be moved in the vertical direction above a microwave filter, or be utilized to deform a conductive film to tune dielectric resonator filters or evanescent-mode cavity filters. Usually this type of filters offers high-Q and high-power-handling capabilities. However, their bulky size and low tuning speed limit their applications in certain areas.

2.2.2 YIG filters

YIG filters utilizing yttrium-iron-garnet (YIG) spheres have been proved the most popular type among the magnetically tunable filters [6]-[7].

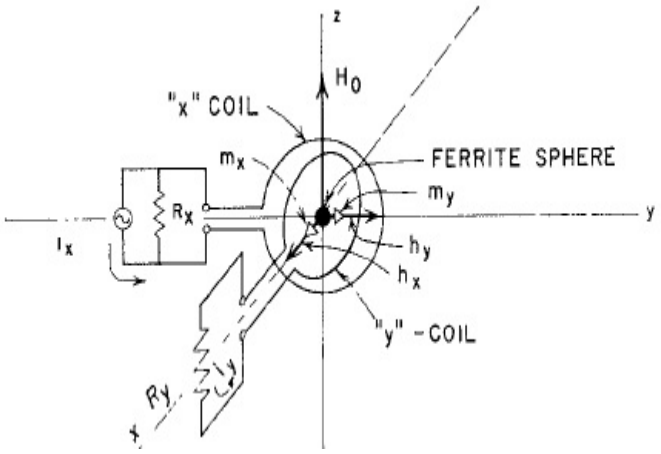


Figure 2.1: Magnetic resonance filter

A small section of YIG ferrite is placed at the center and the two coils are mutually perpendicular as shown in Figure 2.1. When the DC magnetic field is applied along the z -axis and RF driven current which is frequency dependent is provided at the terminal of x coil, magnetic dipole in the YIG ferrite precess around the x-axis, which induces RF magnetic moment along the y-axis and and voltage in the y circuit. Therefore, By changing the magnetic field and the current that are externally applied to the ferrite the resonant frequency of the YIG filter is tuned[8].

Drawbacks:- The main drawbacks are:

- Complex bias circuit to tune the device with high power consumption.
- Low tuning speed (ms)
- Large physical size, limiting their use in modern communication systems.

2.2.3 Barium Strontium Titanate (BST)

Barium Strontium Titanate (BST) is most intensively studied ferroelectric material in tunable applications at room temperature. Ferroelectric materials (are basically dielectric materials) known for their ability to achieve spontaneous polarization and it can be reversed in the presence of an external electric field. When an external field is applied to a regular dielectric material, the electric dipole moments will align themselves in accordance with the direction of the applied electric field. On the other hand, in materials such as ferro electrics, this polarization can take place without the external electric field. When the extrenal electric field (not exceeding the breakdown limit of the crystal) is applied to the ferroelectric, its dipole moments will reverse to align with the field.

When used in the para electric phase(i.e above curie temperature), BST thin film typically exhibits a large dielectric constant (=300-800) that can be changed

by an applied dc electric filed [9, 10, 11] . The high dielectric constant of BST film results in compact BST thin film varactors that are widely used to implement tunable filter, tunable matching networks and delay lines. BST tunable filters can be tuned at nanosecond speeds, and can be fabricated on a variety of substrates using standard semiconductor manufacturing process with ease of integrating microwave devices compatible with planar circuits.

Drawback:- Relatively high loss at room temperature limiting their microwave applications.

Inspite of continuous effort to improve the quality factors of BST varactors. But this is still challenging today.

2.2.4 RF MEMS (Micro-Electro-Mechanical System)

RF MEMS (Micro-Electro-Mechanical System) reconfigurable devices such as MEMS switches or MEMS varactors, are quite popularly used in filter topologies with discrete and continuous tuning [12, 13]. RF MEMS devices mostly utilize micrometer level movement to obtain a switching function or an adjustable capacitance with the applied dc voltage. In general, they can offer small size and good integration capabilities with microwave electronics. They also have the merit of low loss (about 0.05-0.2 dB from 1-100 GHz for switches [14]), high linearity with low signal distortion, low power consumption, high isolation (for switches) and high power-handling capability. However, the requirements of hermetic packaging and high voltage drive circuits (20-100 V) besides the reliability issues have prevented RF MEMS from being widely used in industry [15].

2.2.5 Varactor diode

Varactor diode or varicap diode, is a semiconductor whose capacitance varies as a function of the reverse voltage applied across its terminals.So this can be used where voltage controlled capacitance is required.

Under reverse bias condition, no current can flow and the diode's reverse resistance is almost infinity. The depletion region at the p-n junction acts like an insulating dielectric sandwiched between conductive plates of a capacitor. The symbol is given below in Figure 2.2

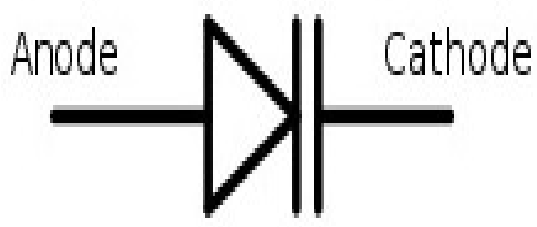


Figure 2.2: Varactor diode symbol

Generally, its operation is based on altering the width of the depletion region under a reverse voltage, thus similarly changing the distance between the two plates of a capacitor to vary the capacitance and is inversely proportional to the

square root of applied voltage [16]. The capacitance of varactor diode is described by:

$$C = \frac{C_o}{(\frac{V}{V_{bi}} + 1)^n} \tag{2.1}$$

In Equation (2.1), C is the varactor diode capacitance, C_o is the zero bias capacitance, V is the reverse bias voltage, V_{bi} is the built-in voltage potential, and n represents the slope of the Log C vs. Log V curve. From Equation(2.1) as the reverse bias increases the capacitance decreases and vice versa.It also depends on doping structure used at the time of wafer preparation.

Where,

$$n = \begin{cases} 0.33, \text{if the diode has graded junction} \\ 0.5, \text{if the diode has abrupt junction} \end{cases}$$

.

(2.2)

Due to fast tuning speed, high tunability, compact size and low cost. Varactor diodes have been used in Electronic Support Measure (E.S.M) systems.

Drawbacks:- The main drawbacks are:

- Low quality factor.
- Highly non-linear characteristics at higher frequencies.
- Poor power handling capabilities.

2.2.6 Digitally Tunable Capacitors (DTCs)

Digitally Tunable Capacitors (DTCs) are variable circuit components whose capacitance is controlled by a set of PIN diode switches in a combination with a NMOS interface [17]. The DTCs are made up of several high Q-factor capacitors and an array of digitally controlled PIN diode switches that determine the total value of the capacitors. This control setting is a digital input that feeds in a binary value corresponding to a certain number of switches to be turned on and hence determining how many capacitors will contribute to the total capacitance value. The DTC filter with PIN diode switch is given in Figure 2.3.

Capacitors are generally connected in parallel and each capacitor is connected to a PIN diode switch in series, which is connected to mosfet for biasing (i.e forward bias for ON switch and reverse bias for OFF switch). The maximum capacitance is achieved when all the switches are ON since the capacitors in parallel is additive. The minimum capacitance is achieved when all the switches are in off state.

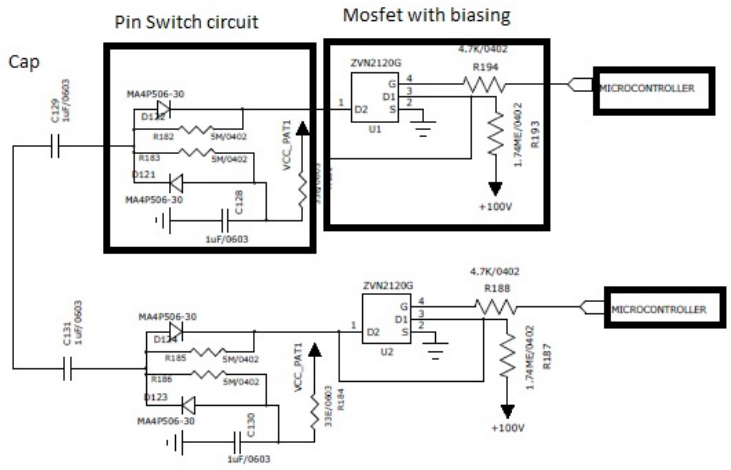


Figure 2.3: DTC PIN diode tuning

2.2.7 Comparison of Several Component Technologies

Tuning Technology	**Mech**	**YIG**	**BST**	**MEMS**	**Varactor**	**DTC**
Unload Q	>1000	>500	30-50	50-400	30-50	R_s=1-4 Ω
Tuning Speed	>10us	ns	ns	us	ns	ns
Bias	>100V	NA	<30V	20-100V	<30V	10-40mA
Linearity	high	<30	10-35	>60	10-35	>33
Power Handling	high	2W	mW	1-2W	mW	mW
Power consumption	high	high	negligible	negligible	low	medium
Size	large	large	small	small	small	small
Cost	high	high	low	medium	low	low
Integration	difficult	difficult	good	good	good	good

Table 2.1: Comparison of Typical Tunable Technologies [8, 10, 15, 16]

2.3 Pin Diode as an Rf Switch

A PIN diode is a current controlled semiconductor device having intrinsic layer sandwiched between two highly doped P and N layers [18]. A model of the basic structure of pin diode is given in Figure 2.4. In this a P-region is diffused to one side of the diode and n-region to the other side. The intrinsic region thickness is a function of silicon wafer used. Also the pin diode performance merely depends on the material used in the intrinsic region. At RF and microwave frequencies it

act as a variable resistor The forward biased dc current determines the resistance value of the PIN diode.

While using PIN diode as a switch the PIN diode should ideally control the RF signal level without introducing any distortion which might change the shape of the RF signal. Also a unique and important additional feature of the PIN diode is that it can control large RF signals while using much smaller levels of dc excitation.This is because for forward conduction it needs electrons in its intrinsic layers but before the amount of electrons crosses the cut off level the RF signals switches to opposite polarity so it needs dc current for overcoming the cut off level for forward conduction as DC is constant.

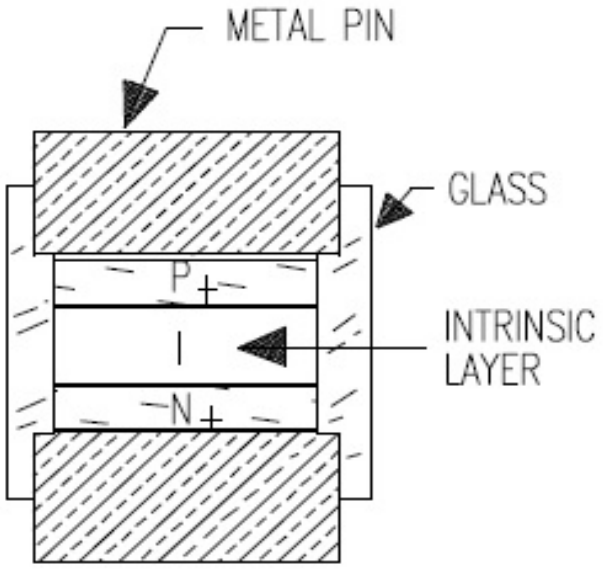


Figure 2.4: Cross Section Basic PIN Diode

2.3.1 Forward bias PIN diode

The equivalent circuit for the forward biased PIN diode is shown in Figure 1.1 (b). It basically consists of a series combination of the series resistance (R_s) and a small Inductance (L_s).

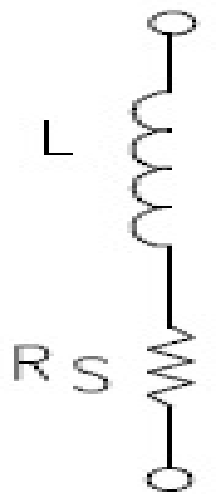


Figure 2.5: Forward biased equivalent model

When a PIN diode is forward biased, holes and electrons are injected from the P and N regions into the Intrinsic region. A finite quantity of charge always remains stored and results in a lowering of the resistivity of the I-region. The quantity of stored charge, Q, depends on the carrier life time,τ and the forward bias current I_F. Q is related to the carrier life time and forward current as follows:

$$Q = I_F \tau \tag{2.3}$$

The resistance of the intrinsic region under forward bias depends on the Q and is given by:

$$R_s = \frac{W^2}{(\mu_n + \mu_p)Q} \tag{2.4}$$

where W= intrinsic region width, μ_n is mobility of electron and μ_p is mobility of hole.

putting equation (4.1) in (4.2) we get,

$$R_s = \frac{W^2}{(\mu_n + \mu_p)I_F \tau} \tag{2.5}$$

From equation (4.3), it can be seen that the series resistance R_s of the diode is directly proportional to the square of the intrinsic region width W and inversely proportional to the forward bias current I_F.

Although in reality the R_s is slightly depends on the width of the intrinsic width. Generally it depends on the forward bias current I_F. This is shown in Figure 2.6 of macom MA4P506-1072T Pin diode.

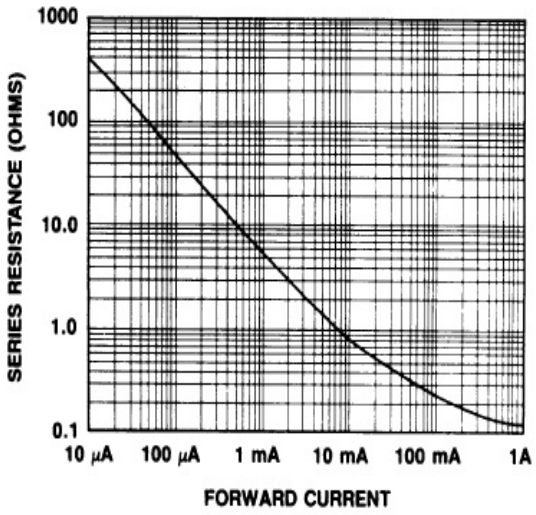


Figure 2.6: Forward Current vs. Series Resistance

Figure 2.6 shows that R_s is inversely proportional to the forward current I_F.

It should be noted that Skin effect is not a significant factor in PIN diodes below X-Band frequencies. his is because skin depth is proportional to the square root of the resistivity of the conducting material. Thus, RF signals penetrate deeply into the semiconductor and skin depth is insignificant. PIN diode act as normal PN junction diode when low frequencies or DC is applied.

2.3.2 Reverse bias PIN diode

The Reverse Bias Equivalent Circuit shown in Figure 2.7 . It consists a shunt loss element (R_p),a parasitic Inductance (L_s) and the Capacitance (C_T).

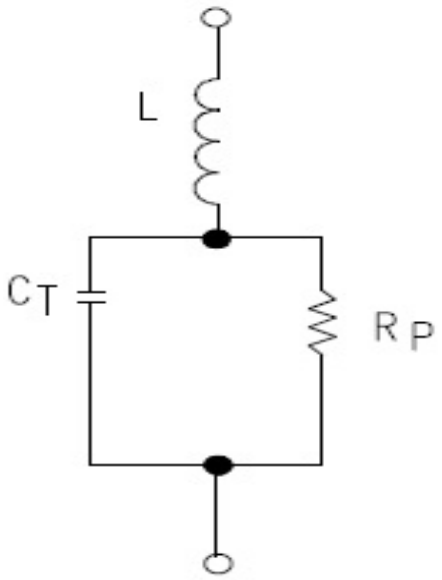


Figure 2.7: Reverse bias Equivalent circuit

At high RF frequencies when a PIN diode is at reverse bias, it appears as a

parallel plate capacitor. Also the capacitance is independent of reverse bias. (C_T) is given by:

$$C_T = \frac{\epsilon A}{W} \tag{2.6}$$

Where ϵ is dielectric constant of silicon A is junction area and W I-region thickness.The frequencies at which this effect begins is related to the dielectric relaxation frequency of the I-region (f_τ),which may be computed as

$$f_\tau = \frac{I}{2\pi\rho\epsilon} \tag{2.7}$$

where ρ is resistivity of Intrinsic region.

At frequencies much lower than f_τ, the capacitance characteristic of the PIN diode resembles a varactor diode.

2.3.3 Selecting Minimum Reverse Bias for a PIN diode

A PIN diode has ability to control large RF and microwave signal with much lower values of DC current or voltages. The instantaneous voltage across the PIN diode must never exceed the avalanche breakdown voltage because high reverse current may cause PIN diode to be burnt. The instantaneous value will include the self generated voltage of pin diode given in Equation and the Dc reverse bias voltage applied [19]. The unsafe condition is shown in Figure 2.8.

Condition:

$$V_{DC} + |V_{RF}| > V_{BR} \tag{2.8}$$

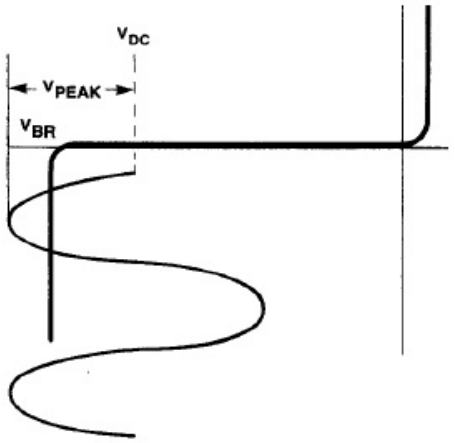


Figure 2.8: Unsafe Bias

Selection of minimum reverse bias is important as it should not be less so that it forces the diode to be forward conduction mode or not above the breakdown voltage which will cause failure of the diode [20]. This is safe region of operation shown in Figure 2.9

Conditions:

$$V_{DC} + |V_{RF}| < V_{BR} \tag{2.9}$$
$$V_{DC} > V_{RF} \tag{2.10}$$

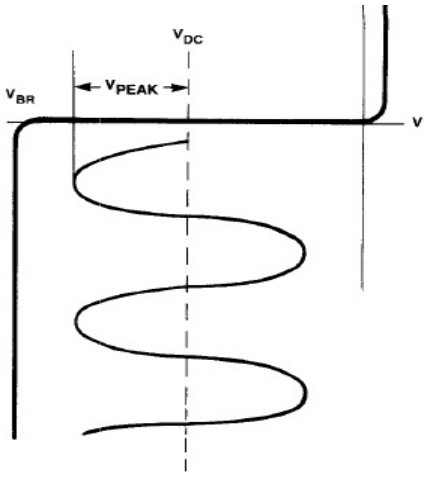


Figure 2.9: Safe bias

In safe region we apply large reverse bias which in some application isn't available. Also this can be too much costly. So PIN diode are used in conditionally safe region given in Figure 2.10.

Condition

$$V_{DC} + |V_{RF}| < V_{BR} \tag{2.11}$$
$$V_{DC} < V_{RF} \tag{2.12}$$

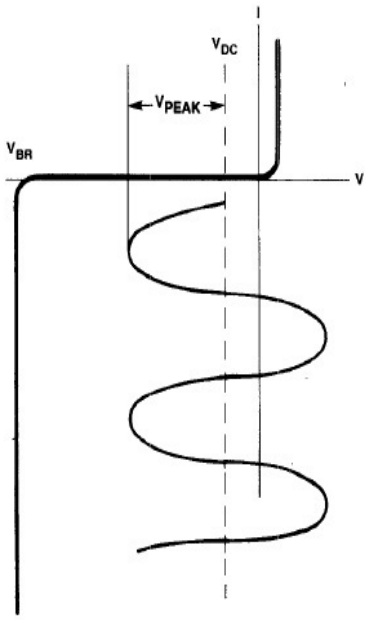


Figure 2.10: Conditionally safe bias

where an instantaneous spikes of voltage into the forward conducting region may be tolerated.The self-generated dc voltage was influenced by the peak RF voltage level, the frequency, and the thickness of the Intrinsic region and given in Equation(4.11) [21] [22] [23].

$$V_{dc} = \frac{|V_{RF}|}{[1 + (0.0285 f_{MHz} W_{mil}^2 / V_{RF}\sqrt{D})^2]^{0.5}} \tag{2.13}$$

The Self generated DC voltage V_{dc} can be considered as the minimum reverse bias to operate the diode in conditionally safe region. Also the devices may be selected at a voltage level below the breakdown voltage, which increases the reliability and lower the cost of PIN diodes.

Chapter 3

Approach

The current state-of-the-art of the RF section filter types, topologies, and tunable elements that can be used to adjust the cut off frequency of the filter has been researched. The filter topologies were using ideal lumped elements in ADS.

The next step was to investigate and compare the performance of different types of filters including Butterworth and Chebyshev. The filter response of were observed by plotting the S21 and S11 parameter in ADS. The responses and complexity of these filters were compared and the best solution that satisfies the desired specification is determined.

Once fully realized, the filter would not perform according to the ideal behavior of the virtual components. So, we decided to simulate the lumped elements with appropriate Q values. To determine the Q values of each component, we researched several available components in the market. It was expected that design modifications would become necessary in order for the filter to perform to specification with the lessened quality factor of the components.

Determining component values that provided the desired response was a key consideration in designing our filter configuration. In this section, we used the ADS/Genesis simulator as well as a mathematical model to determine values for the filter components. It was expected that the mathematical model would be more useful in the initial design phase.

3.1 Fundamental Filter Theory

For designing a filter with desired specifications first we have to take a normalized low pass filter or a prototype low pass filter, which can then be synthesized into unique filter performance[24].

A prototype Low pass filter has the cut-off frequency of 1 radian per second and is terminated by 1 Ω resistance. It can be realized in two ways:

- Minimum capacitor
- Minimum inductor

These two equivalent realization of low pass filter is given in Figure 3.1

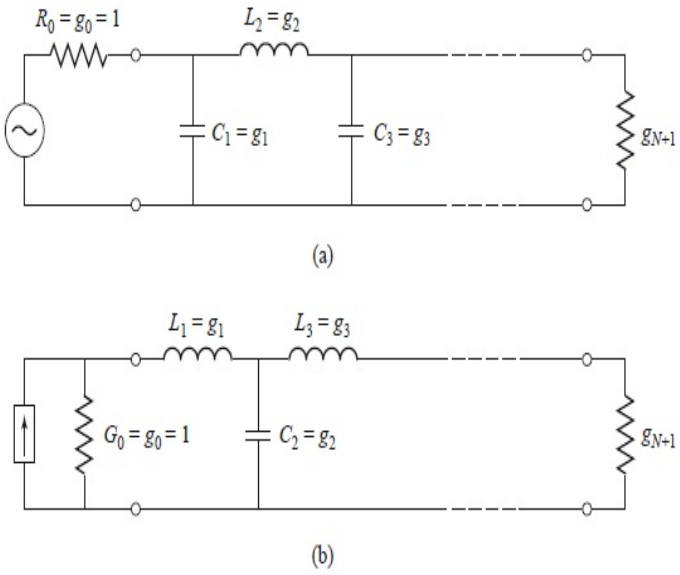


Figure 3.1: (a) Minimum inductor (b) Minimum capacitor

The values for the g's in Figure 3.1, involve inductors and capacitors in Henries and Farads, respectively and can be found in many pre-calculated tables for different types of filters [25]. In order to arrive at the realizable filters, these coefficients are de-normalized to meet realistic frequency and impedance requirements. Impedence and frequency scaling is done to transform normalized low pass filter to the desired low pass filter.

3.1.1 Impedence and Frequency scaling

These low pass filter were normalized designs having a source impedance of $R_s = 1\ Ohm$ and a cutoff frequency of $w_c = 1$ rad/sec. Now, we have to scale these designs in terms of frequency and impedence.

Impedence Scaling

In the normalized design, the load and source impedences are unity. A source resistance of R_0 can be obtained by multiplying all the impedances of the prototype design by R_0 Ω. So the new filter component values are given by:

$$L^{'} = R_0 L, \tag{3.1}$$

$$C^{'} = \frac{C}{R_0}, \tag{3.2}$$

$$R_s^{'} = R_0, \tag{3.3}$$

$$R_L^{'} = R_0 R_L \tag{3.4}$$

Where, L ,C ,R_L are the values of normalized low pass filter.

Frequency Scaling

In normalized design, the cut-off frequency is unity. A cut-off frequency of w_0 can be obtained by replacing w by w/w_c. So the new filter component values are given by:

$$L_k^{'} = \frac{L_k}{w_c}, \tag{3.5}$$

$$C_k^{'} = \frac{C_k}{w_c} \tag{3.6}$$

When both impedence and frequency scaling is applied at then the component values can be transformed as given below:

$$L_k^{'} = \frac{R_0 L_k}{w_c}, \tag{3.7}$$

$$C_k^{'} = \frac{C_k}{R_0 w_c} \tag{3.8}$$

3.2 Ideal filter simulation

Using ADS software tool, I investigated different ideal filter topologies which includes the Butterworth filter , the Chebyshev filter 0.5dB and 3dB [26]. Also I chose minimum inductor type prototype model low pass filter as given in Figure 3.2.

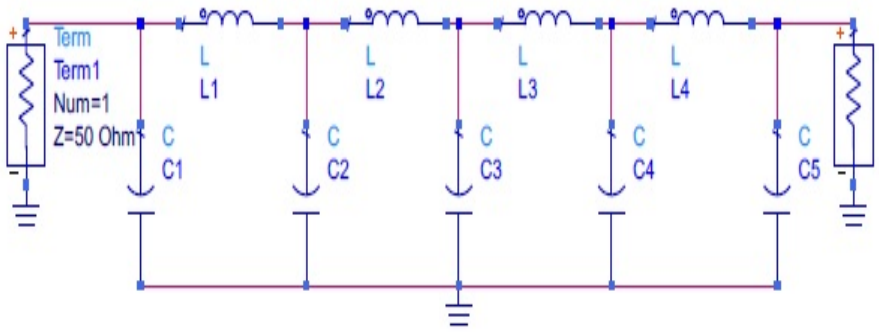


Figure 3.2: 9th Order Ideal Low Pass Filter

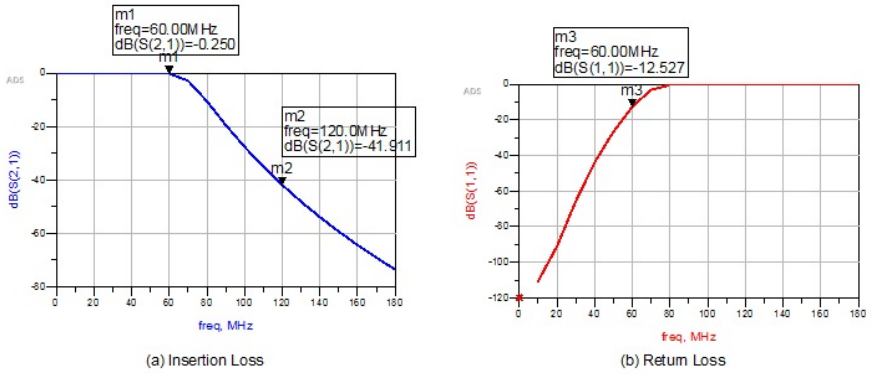
3.2.1 Butterworth Filter

In this section, insertion loss and return loss at cut-off frequency 60 MHz and input-output impedence of 50 Ω using the g coefficients for the maximally flat Butterworth filter design is presented. By using formulas in given equation(3.7)(3.8) and taking the g-values (given in Appendix B) from butterworth low pass filter we can calculate the inductors and capacitor values which is given in Table 3.1

Coefficients	Inductor(mH)	Capacitor(uF)
1	113.35	15.74
2	213.04	69.47
3	213.04	90.687
4	113.35	69.47
5	NA	15.74

Table 3.1: Component values for a 9th order Butterworth filters.

After using these component values in the filter shown in Figure 3.1 we get the following responses give in Figure,3.3



(a) Insertion Loss (b) Return Loss

Figure 3.3: 9th order butterworth filter response

In the above response we are getting only -41.911 dB rejection for second harmonics for 9th order butterworth filter. So we proceed to next type of filter.

3.2.2 Chebyshev (0.5dB)

By using formulas in given equation(3.7)(3.8) and taking the g-values from Chebyshev (0.5dB) low pass filter given in Appendix B, we can calculate the inductors and capacitor values which is given in Table 3.2

After using these component values in the filter shown in Figure 3.1 we get the following responses give in Figure 3.2.

Coefficients	Inductor(mH)	Capacitor(uF)
1	168.31	92.86
2	181.34	141.533
3	181.34	144.51
4	168.31	141.533
5	NA	92.86

Table 3.2: Component values for a 9th order Chebyshev (0.5 dB) filters.

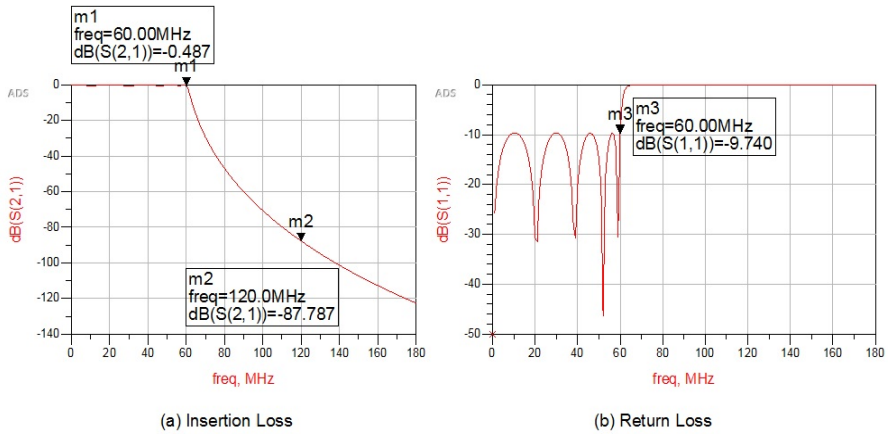


Figure 3.4: 9th order chebyshev(0.5 dB) filter response

In the above response we are getting rejection at second harmonics as per the desired specification but we are getting 0.5 dB Insertion loss at cut off which will increase above the desired specification after realization with ohysical compnents and return loss is also not as per the specification for 9th order chebyshev(0.5 dB) filter. So we proceed further to next type of filter.

3.2.3 Chebyshev (0.25 dB)

We have calculated the component values by g-values (Appendix B) in the chebyshev 0.25 dB ripple table.The component values we get is in Table 3.3

Coefficients	Inductor(mH)	Capacitor(uF)
1	176.61	57.04
2	197	102.83
3	197	131.89617155
4	176.61	102.830
5	NA	57.04

Table 3.3: Component values for a 9th order Chebyshev (0.25 dB) filters.

After using these component values in the filter shown in Figure 3.1 from Table 3.3 we get the following responses after simulating in ADS given in Figure 3.5

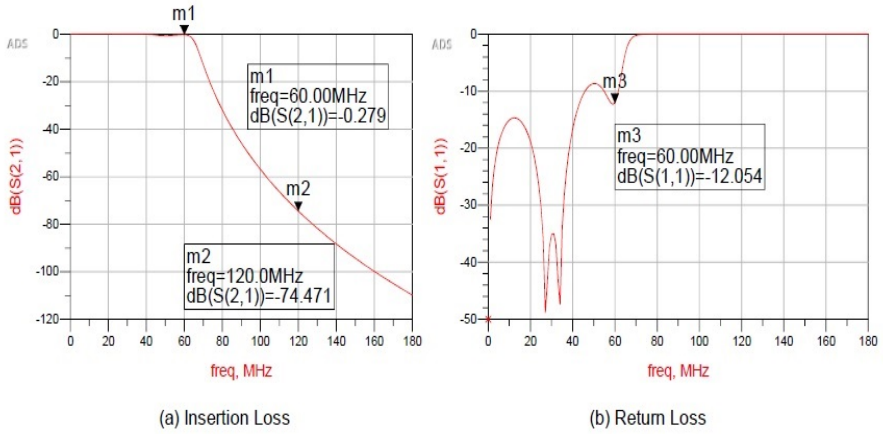


Figure 3.5: 9th order chebyshev(0.25 dB) filter response

In the above response we are getting insertion loss and rejection at second harmonics as per the desired specification. Although return loss is not as per the requirement but We can get it by tuning the capacitor a bit but in earlier two topologies(Butterworth Filter, Chebyshev (3dB)), we can't get the desired response even after tuning the capacitors.

3.3 Switched Filter Banks

This is very traditional technique of making filter tunable. Initially fixed frequency filter is made of different frequency bands. Then the tunability is achieved by using switches among these filters in both at input and output end [27]. An example of switched filter bank is illustrated in Figure 3.6. Although, this type of conventional filter banks is not cost and size effective. As the tuning range increases the cost and size increases. This led to the realization of a new and compact cost and size effective tunable low pass filter.

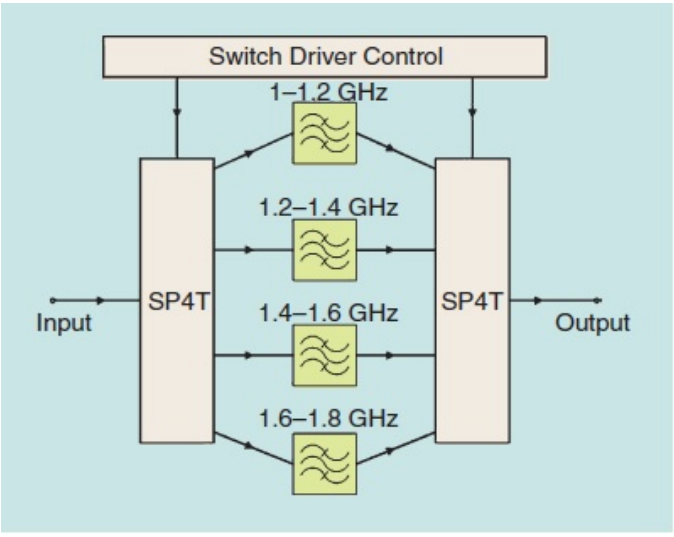


Figure 3.6: Electronically switchable filter bank block diagram

Chapter 4

Design and simulation of Tunable LPF

For desigining a tunable filter which can tune in the wide frequency band in the V/UHF range of 30-520 MHz [28]. Three individual tunable filters banks has been designed in ADS design using Chebyshev(0.25) topology, of the frequency range 30-90 MHz, 90-270 MHz, 270-520 MHz as shown in block diagram 4.1. These filters have pin diode switch connected to the shunt capacitor to tune the value of capacitance.For giving bias to the pin diode switching circuit mosfet are used. Here HV5533 Driver IC has been used to provide biasing to the switch. The Ic is digitally controlled by microcontroller PIC32MX695F512H. The single pole triple throw (SP3T) switch MASW-011040 is also controlled by the microcontroller quoted before.

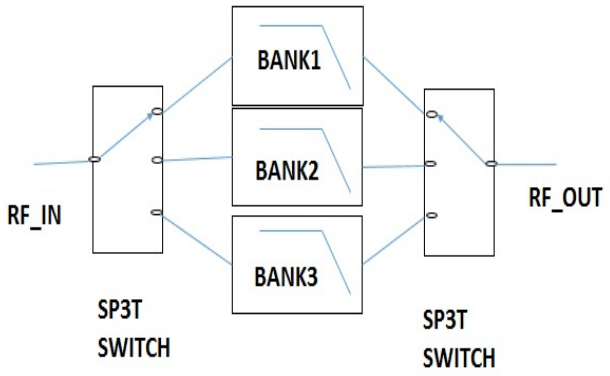


Figure 4.1: Tunable Filter Block Diagram(30-520 MHz)

Now the three filters banks are individually tuned in ADS designing tool for several values of capacitors. By tuning we can find the minimum and maximum value of capacitance required for tuning in desired frequency range. Then the switch is connected to each capacitor branch and tunning is done manually by switching the pin diode.

After simulation PADS design software is used to make the digital schematic diagram.

4.1 PIN diode Switch circuit

Using PIN diode as a switch the circuit requires two pin diode connected in opposite direction and parallel high value resistance for voltage divider. The circuit that has been used as a switch is given in Figure 4.2

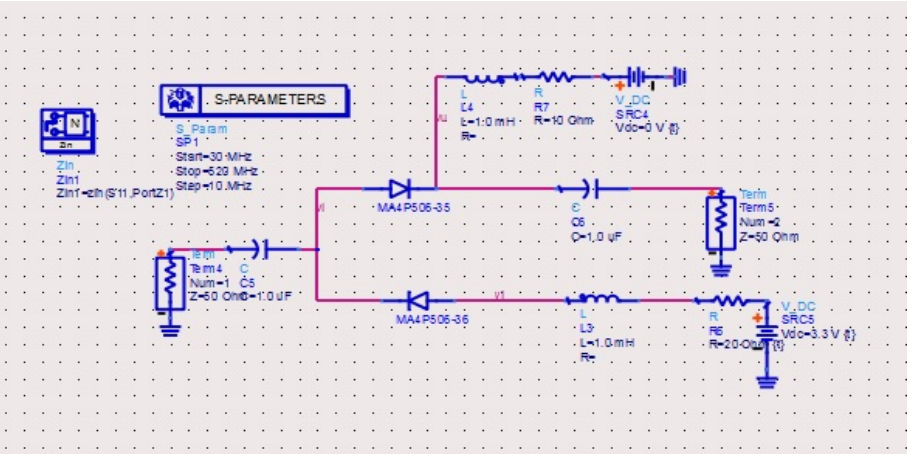


Figure 4.2: PIN diode switching circuit

After simulating the circuit in ADS , we can get the loss which can come by using the circuit as a switch [29]. The main advantage of using this circuit is that the loss when switch is ON is very less shown in Figure 4.3.

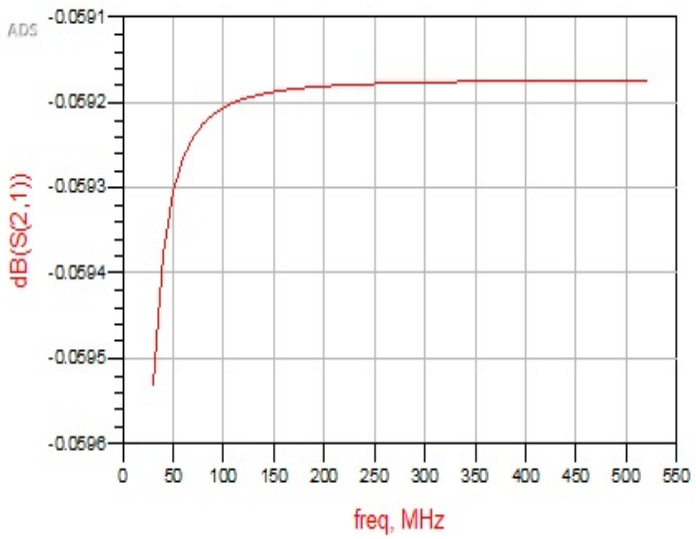


Figure 4.3: Loss when circuit is in conducting state

Also it has very less capacitance so it has very little effect to the overall capacitance of that branch which is switched on given in Figure 4.4 .

freq	Zin1
30.00 MHz	50.688 - j0.013
60.00 MHz	50.685 - j0.007
90.00 MHz	50.684 - j0.005
120.0 MHz	50.684 - j0.004
150.0 MHz	50.684 - j0.003
180.0 MHz	50.684 - j0.002
210.0 MHz	50.684 - j0.002
240.0 MHz	50.684 - j0.002
270.0 MHz	50.684 - j0.002
300.0 MHz	50.684 - j0.002
330.0 MHz	50.684 - j0.002
360.0 MHz	50.684 - j0.002
390.0 MHz	50.684 - j0.002
420.0 MHz	50.684 - j0.001
450.0 MHz	50.684 - j0.001
480.0 MHz	50.684 - j0.001
510.0 MHz	50.684 - j0.001
520.0 MHz	50.684 - j0.001

Figure 4.4: Impedence of the switching Circuit

While using simply PIN diode and biasing causes losses in RF signal as its reactive impedence value is inductive which has a property to block RF that is why the above circuit has been used.

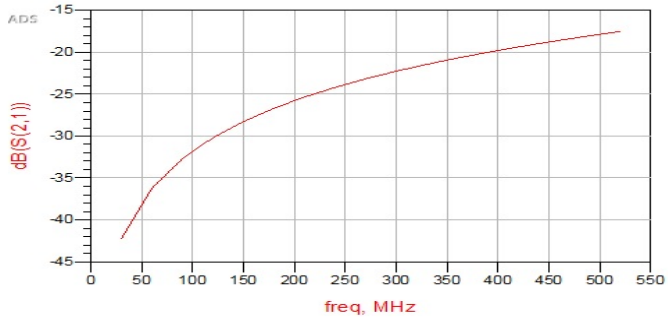


Figure 4.5: Isolation

For switching off the switch we have to give bias from the driver IC. Figure 4.5 shows the isolation when the switch is in OFF state.

4.2 Tuning Process

First filter is designed which can tune in the frequency range from 30 MHz to 90 MHz. For this frequency range, fixed filter is designed for the mid frequency i.e 60MHz. Which can be calculated from equation (4.1) Then the capacitor of this filter is tuned. To meet the specifications of the objective 9^{th} order chebyshev filter is designed as described in Section (3.2.3) [30].

As this is the chebvyshev filter so the filter is symmetric so only three values of capacitor is tuned. The filter which is tuned is shown in Figure 4.6 and Figure 4.7.

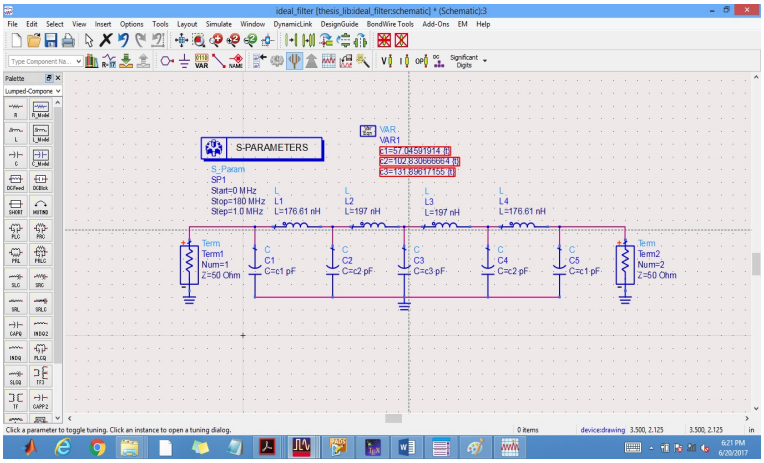


Figure 4.6: Tuning process(i)

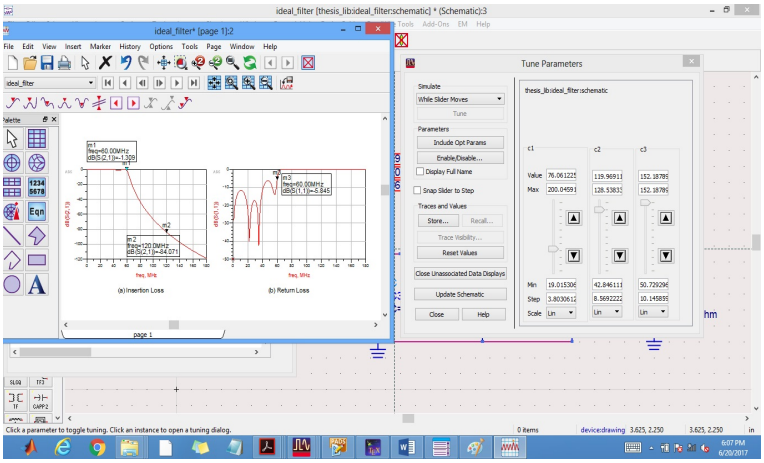


Figure 4.7: Tuning process(ii)

In tuning process we have taken some intermediate frequencies with equal interval and find each capacitance value at that intermediate frequency by tuning. Then by plotting capacitance value of intermediate cut off frequencies in graph we can get the approximate equation by which we can tune the filter for frequencies within the specified range.

To meet the capacitance requirement we have taken the lowest value capacitor fixed and then added capacitors values in binary. These capacitors are added in

parallel (As capacitors have additive property in parallel). So that we can get intermediate values of capacitor which is required.

4.3 Filter Bank (30-90 MHz)

For designing filter 30-90 MHz, we have made a fixed filter of the cut-off frequency of 60 MHz by Equation (4.1). A dc blocking capacitor is used at input and output of the filter which is connected to switch. The corresponding value of capacitors at intermediate frequency is given in Table 4.1:

$$f_{fixed} = \frac{f_H + f_L}{2} \tag{4.1}$$

S.No.	**Freq(MHz)**	**Capacitor1 (pF)**	**Capacitor2 (pF)**	**Capacitor3 (pF)**
1	30	151.4	342.8	304.2
2	35	111.3	251.8	238.3
3	40	85.3	192.8	192.8
4	45	67.5	152.3	160.0
5	50	54.7	123.4	135.4
6	55	45.2	102.0	116.5
7	60	38.0	85.7	101.5
8	65	32.4	73.0	89.4
9	70	28.0	63.0	79.5
10	75	24.4	54.8	71.2
11	80	21.4	48.2	64.3
12	85	19.0	42.7	58.4
13	90	17.01	38.1	53.4

Table 4.1: Tuned capacitor value FILTER 1

By plotting these values of capacitors, we can get the frequency dependent equation by which the capacitance is varying. The graph plotted for capacitor 1, capacitor 2 and capacitor 3 is given in Figure 4.8 (a)(b)(c) respectively.

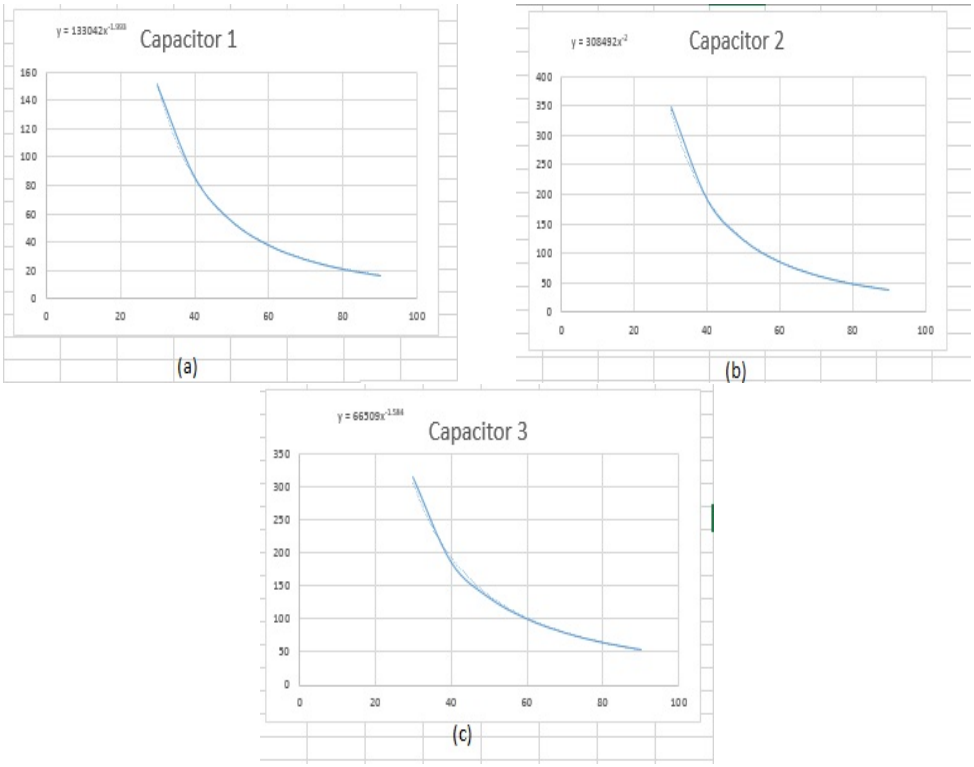


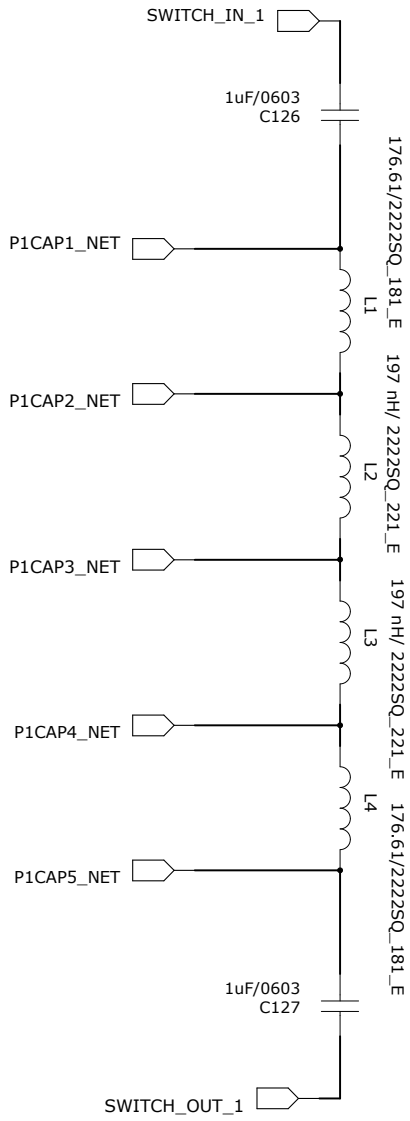
Figure 4.8: Tuned capacitor value plot

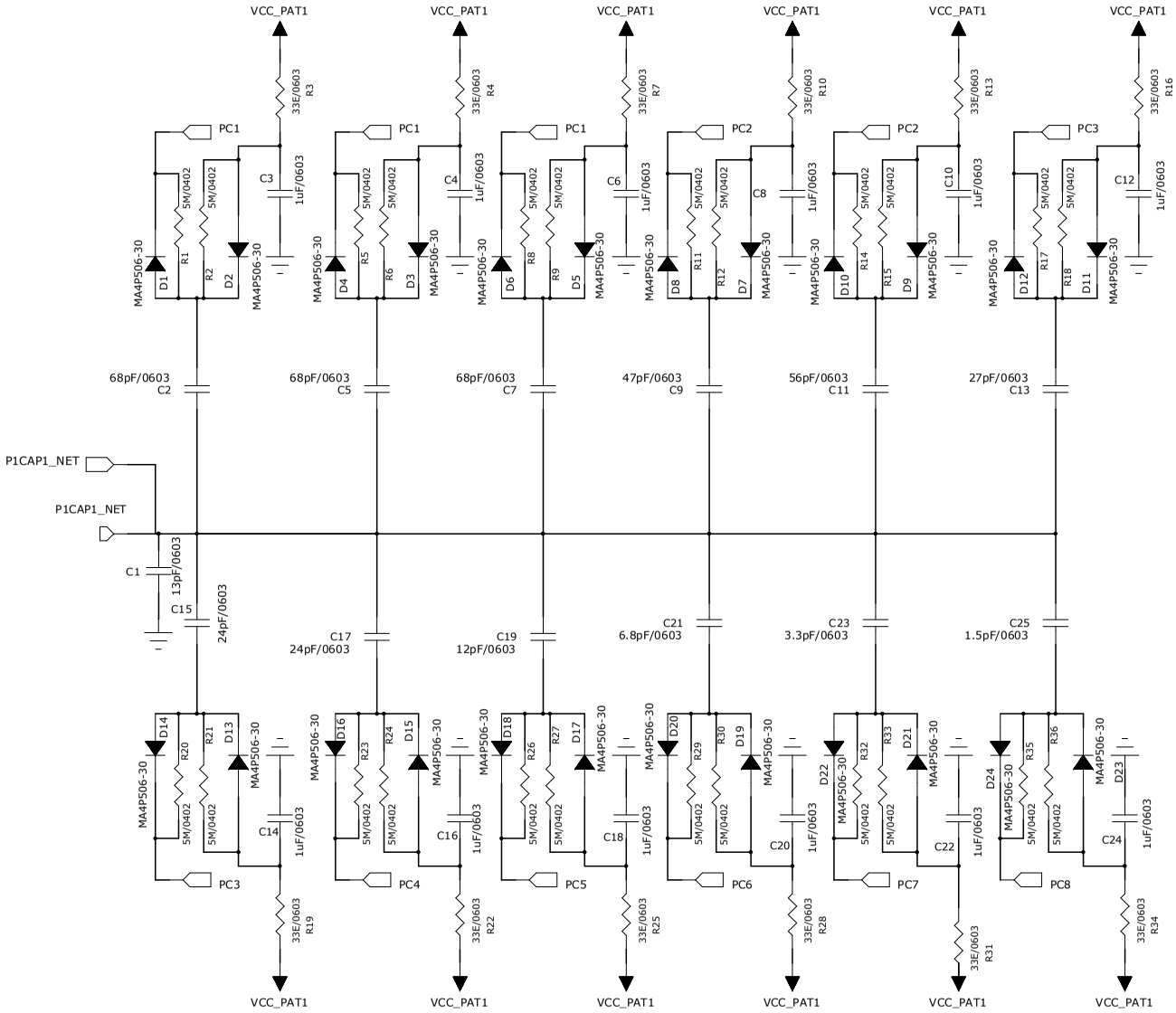
The equation which is generated after plotting these values which is mentioned in Table 4.1 is given below:

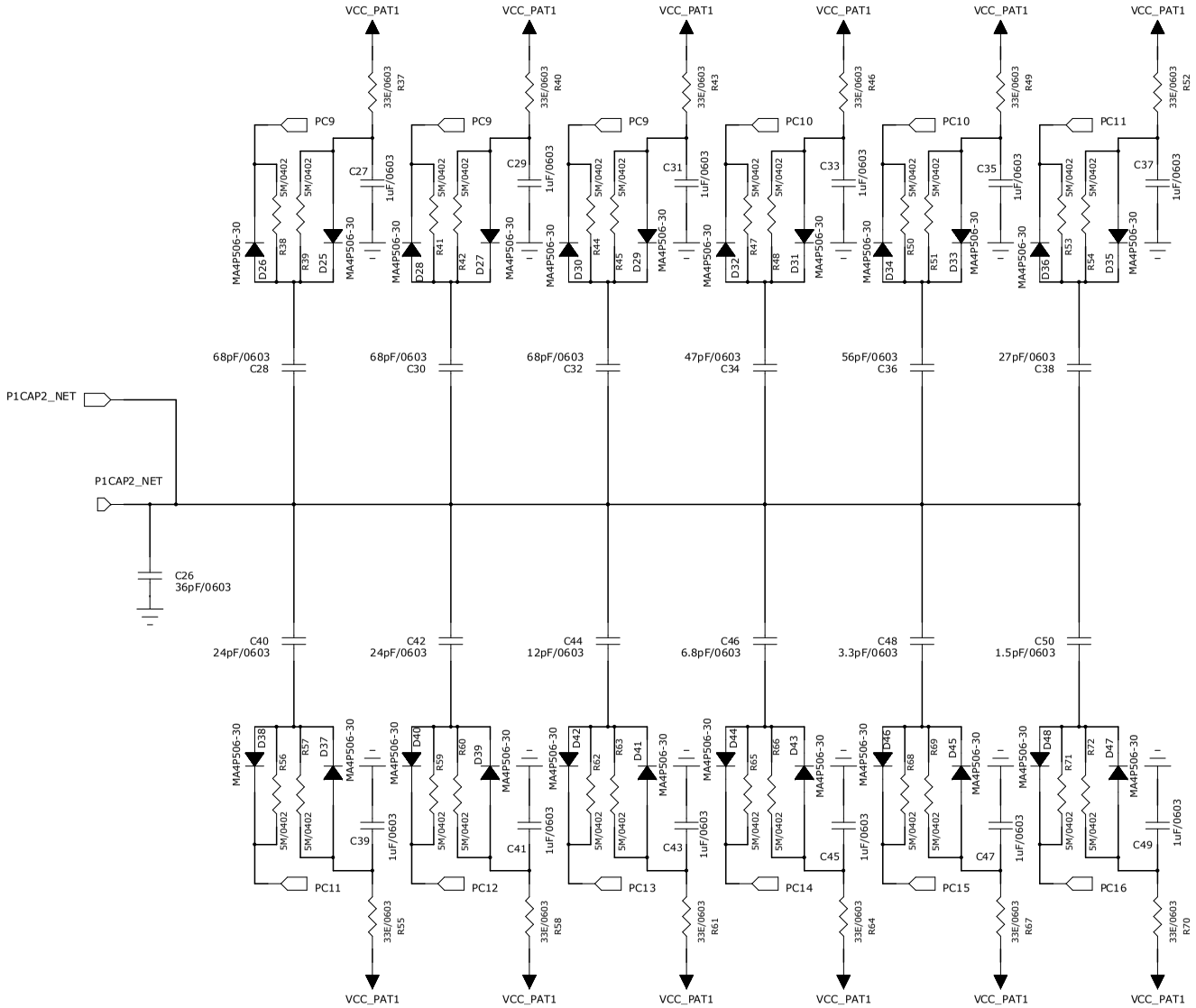
$$C_1 = 133042 f_c^{-1.993} \tag{4.2}$$
$$C_2 = 308492 f_c^{-2.000} \tag{4.3}$$
$$C_3 = 066509 f_c^{-1.584} \tag{4.4}$$

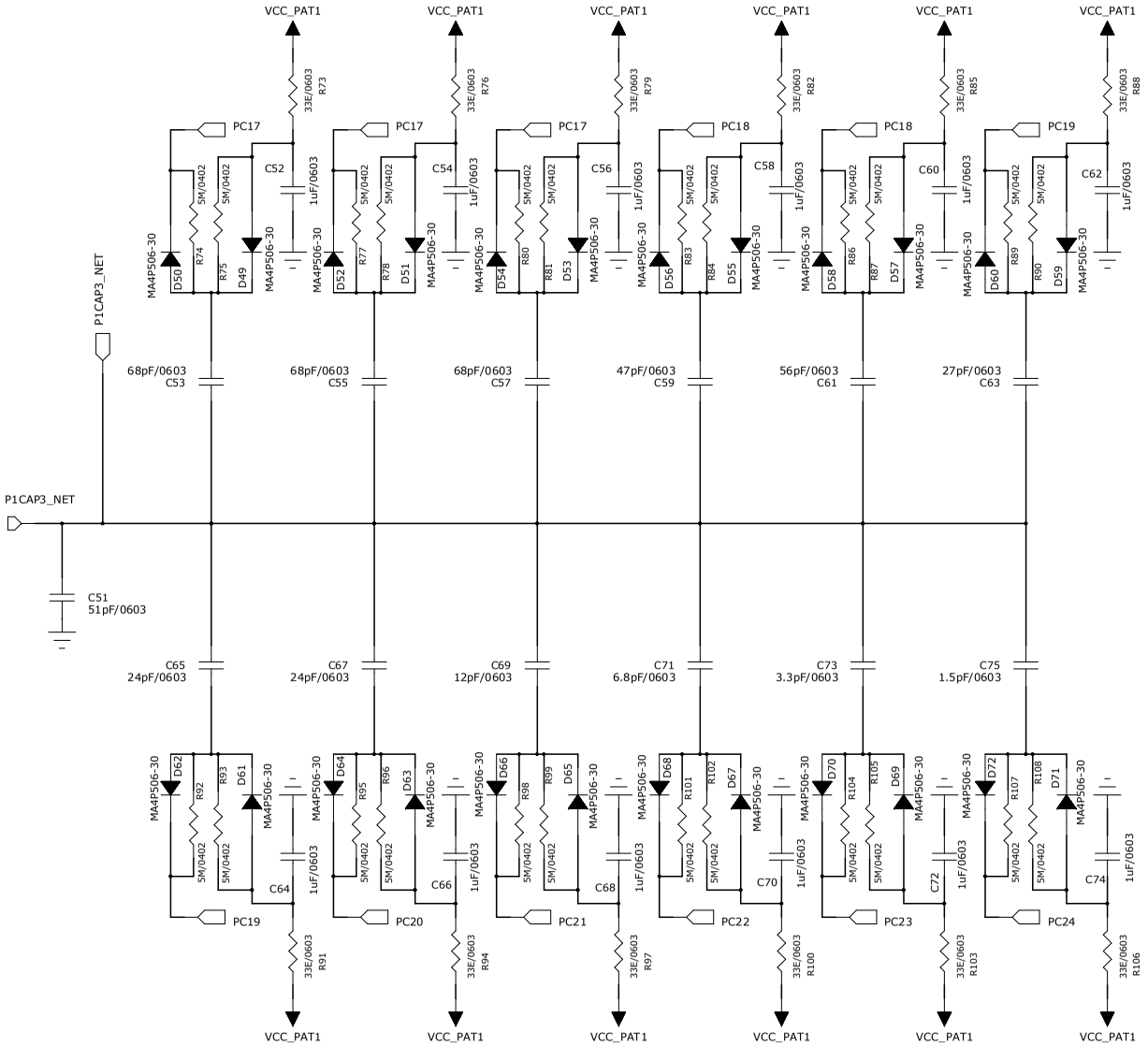
The schematic in PADS logic is given in Figure 4.9

4.3.1 Schematic of RF section




VCC_PAT1
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
MA4P506-30
5M/0402
33E/0603
1uF/0603
68pF/0603
47pF/0603
56pF/0603
27pF/0603
P1CAP1_NET
13pF/0603
24pF/0603
12pF/0603
6.8pF/0603
3.3pF/0603
1.5pF/0603


VCC_PAT1
PC9
PC10
PC11
PC12
PC13
PC14
PC15
PC16
33E/0603
5M/0402
1uF/0603
MA4P506-30
68pF/0603
47pF/0603
56pF/0603
27pF/0603
P1CAP2_NET
C26
36pF/0603
C40
24pF/0603
C42
24pF/0603
C44
12pF/0603
C46
6.8pF/0603
C48
3.3pF/0603
C50
1.5pF/0603


VCC_PAT1
PC17
PC18
PC19
PC20
PC21
PC22
PC23
PC24
P1CAP3_NET
MA4P506-30
5M/0402
1uF/0603
33E/0603
68pF/0603
47pF/0603
56pF/0603
27pF/0603
24pF/0603
12pF/0603
6.8pF/0603
3.3pF/0603
1.5pF/0603
51pF/0603

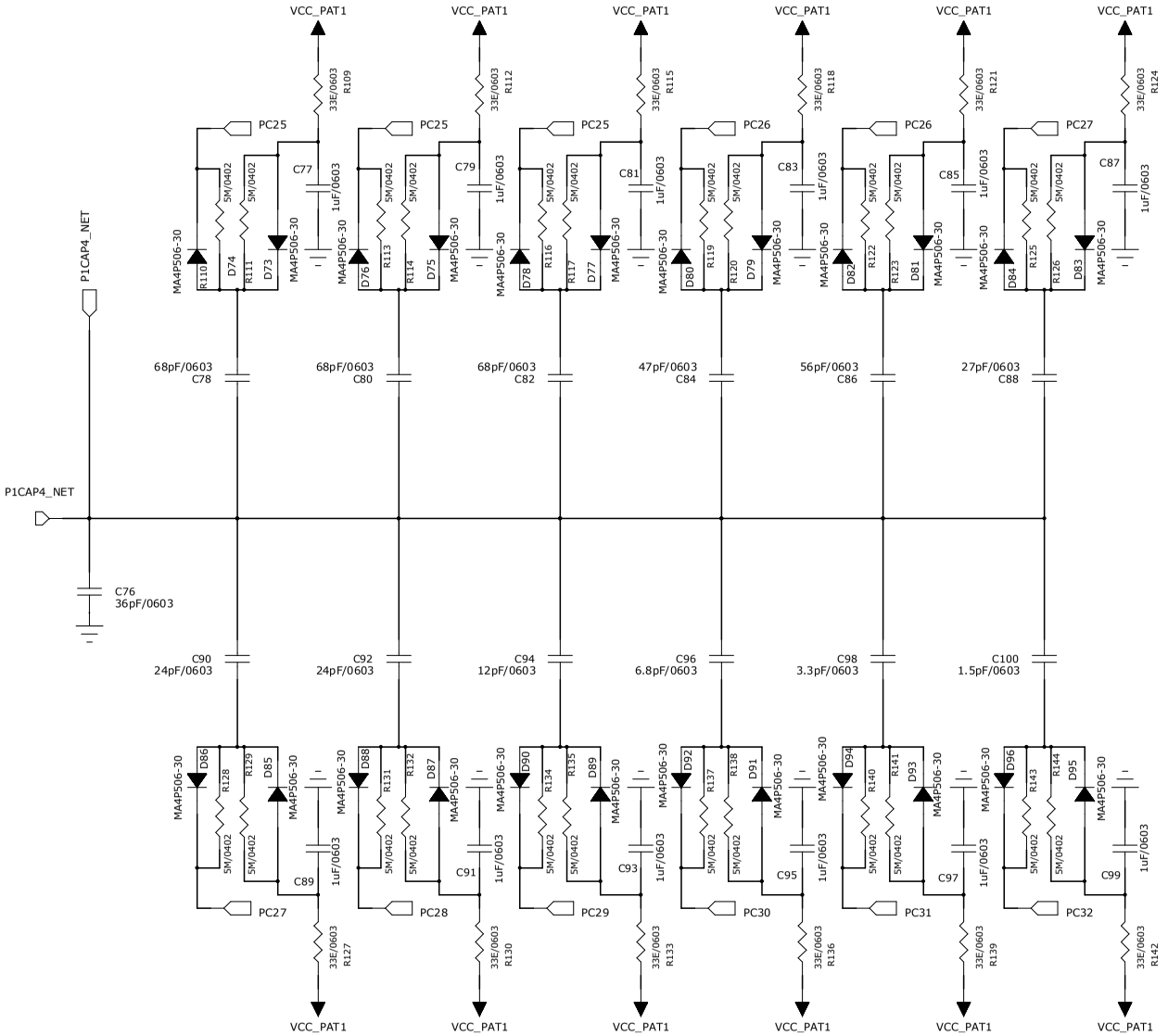
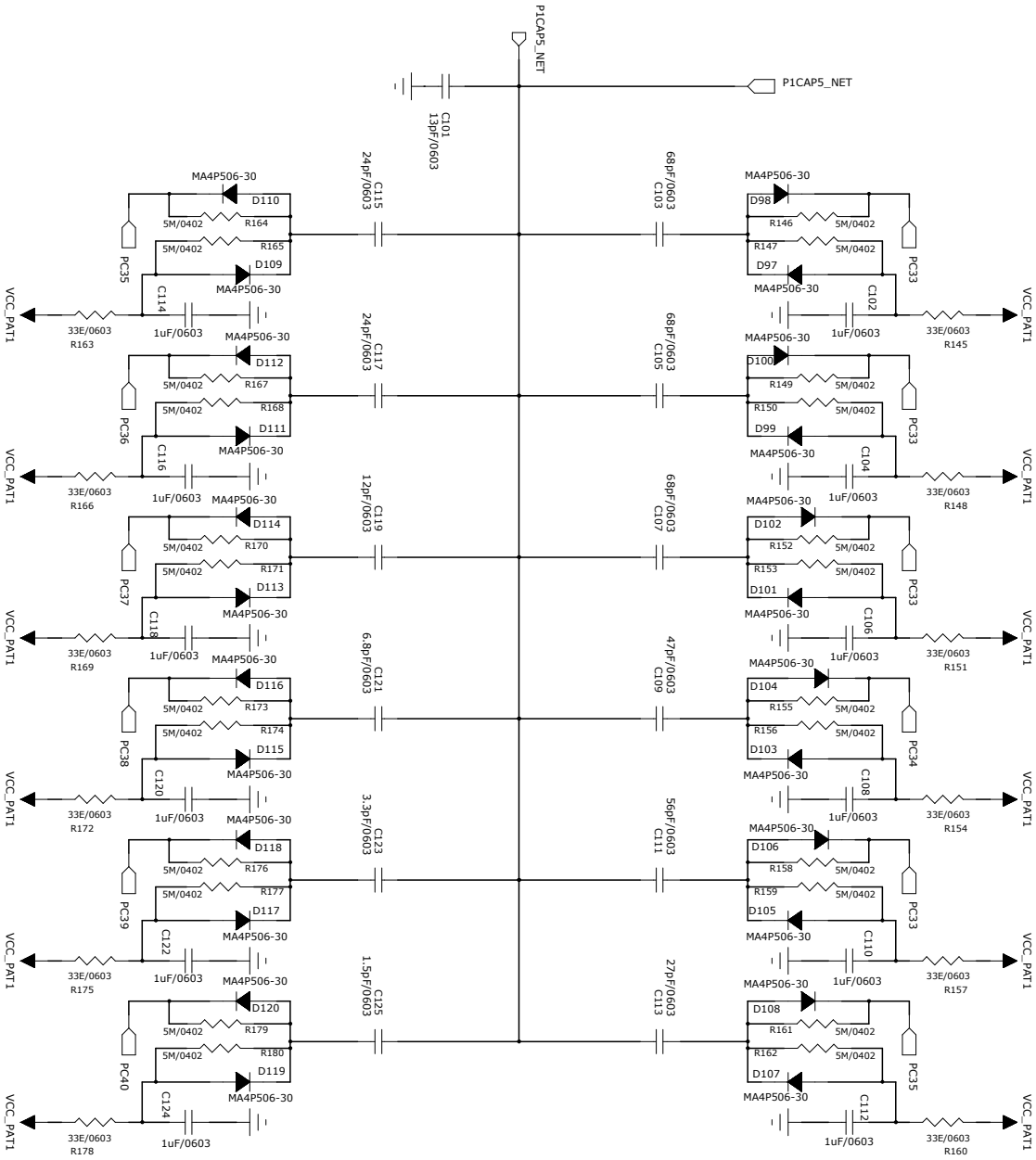

VCC_PAT1
P1CAP4_NET
C76
36pF/0603
68pF/0603
C78
68pF/0603
C80
68pF/0603
C82
47pF/0603
C84
56pF/0603
C86
27pF/0603
C88
C90
24pF/0603
C92
24pF/0603
C94
12pF/0603
C96
6.8pF/0603
C98
3.3pF/0603
C100
1.5pF/0603
PC25
PC26
PC27
PC28
PC29
PC30
PC31
PC32
MA4P506-30
5M/0402
1uF/0603
33E/0603

Figure 4.9: PADS schematic for Filter 1



4.3.2 ADS simulation (30-90 MHz)

Simulation schematic diagram in Agilent ADS is given in Figure 4.10 .

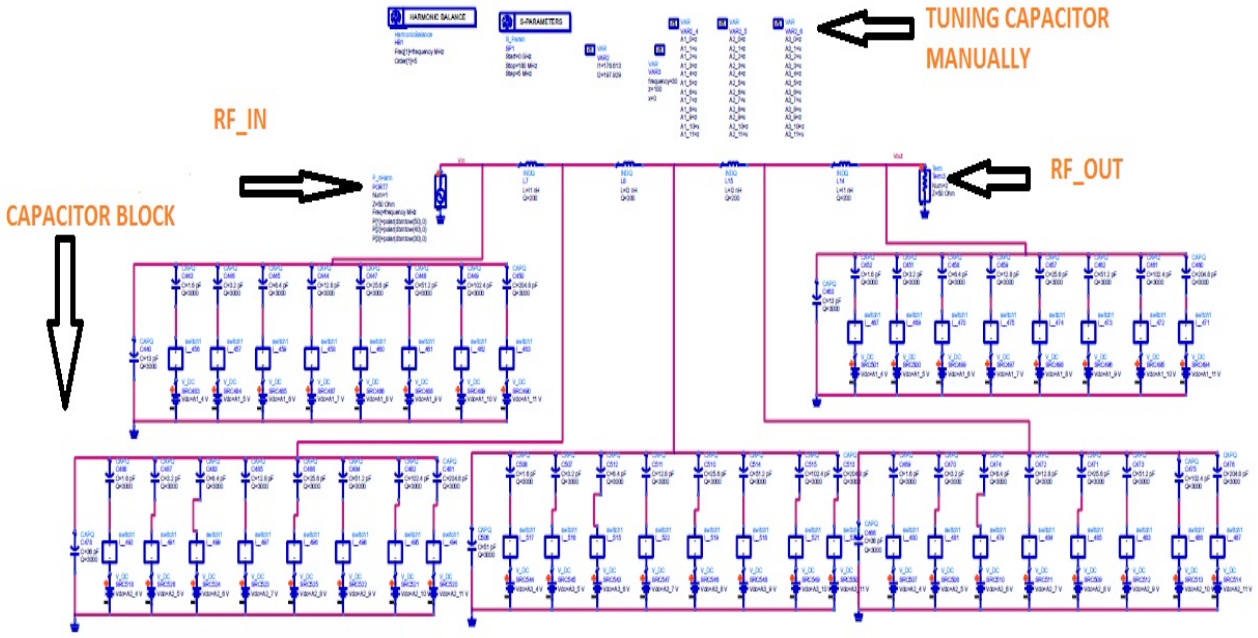


Figure 4.10: ADS schematic (30-90MHz)

In this in place of capacitor tuning capacitor block is used. In tuning block the one capacitor is fixed which is the lowest value of capacitance after tuning (i.e capacitance value when filter is tuned to the highest frequency). Then the capacitor is connected in parallel in binary form so that all the intermediate value is generated precision up to one places on decimal.

The capacitor block which is used in place of single capacitor is shown in Figure 4.11

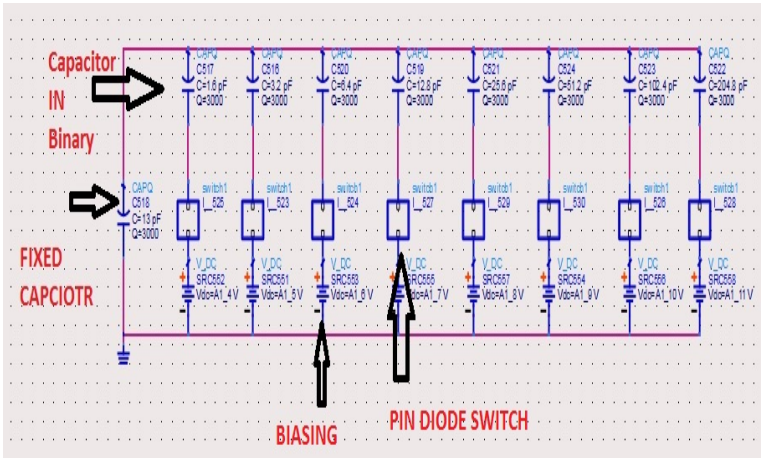


Figure 4.11: Equivalent Capacitor Block

In ADS, tuning is done manually by switching the PIN-Diode.The PIN diode switch shown in Figure 4.11 contains the circuit shown in Figure 4.2. Switching is done by changing the biasing of the diode. Bias is changed by taking the two variables (i.e. z=100 v and x= 0 V).

If Z=100 is selected then the switch is open and if x=0 is selected then the switch is closed. The manually tuning block is shown in Figure 4.12.

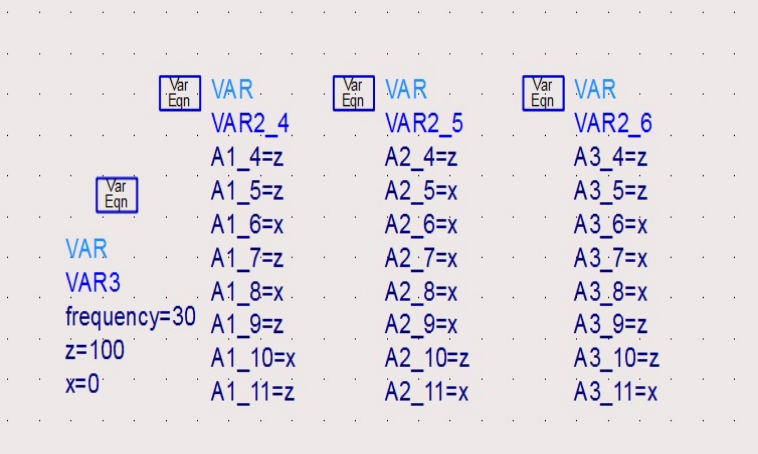


Figure 4.12: Manually Tuning Block

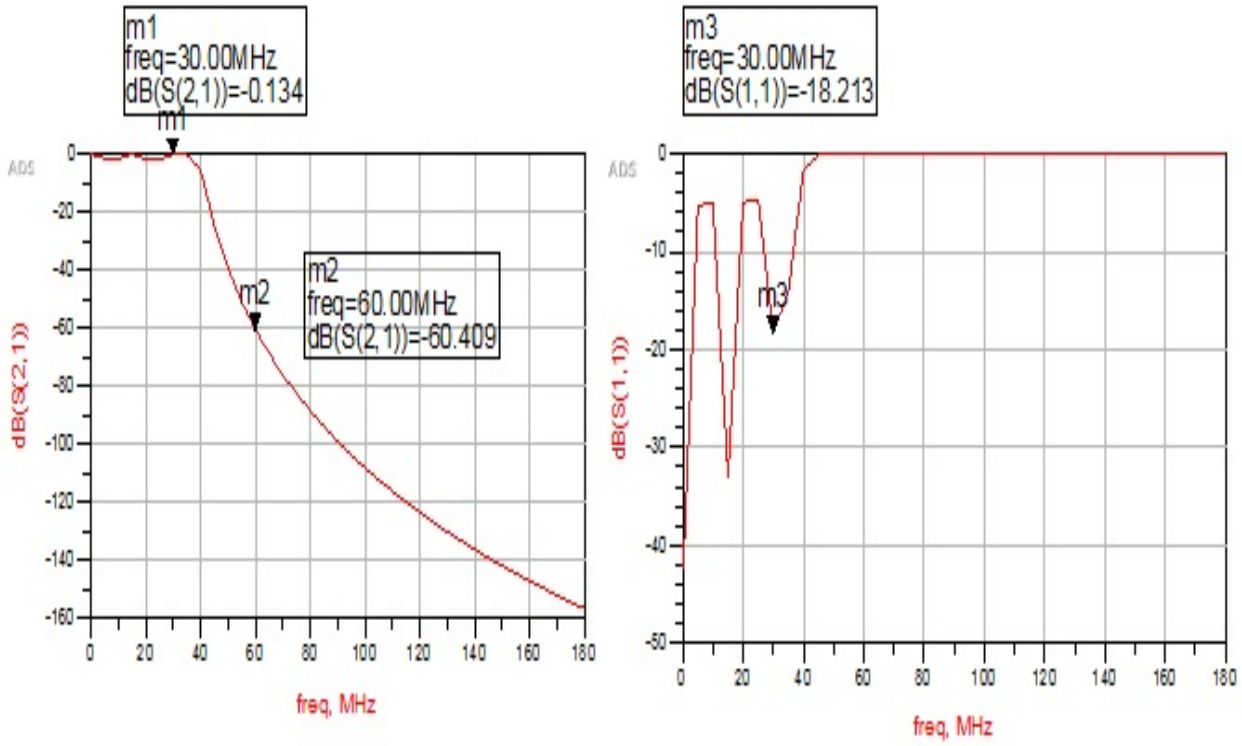
4.3.3 Simulation Response

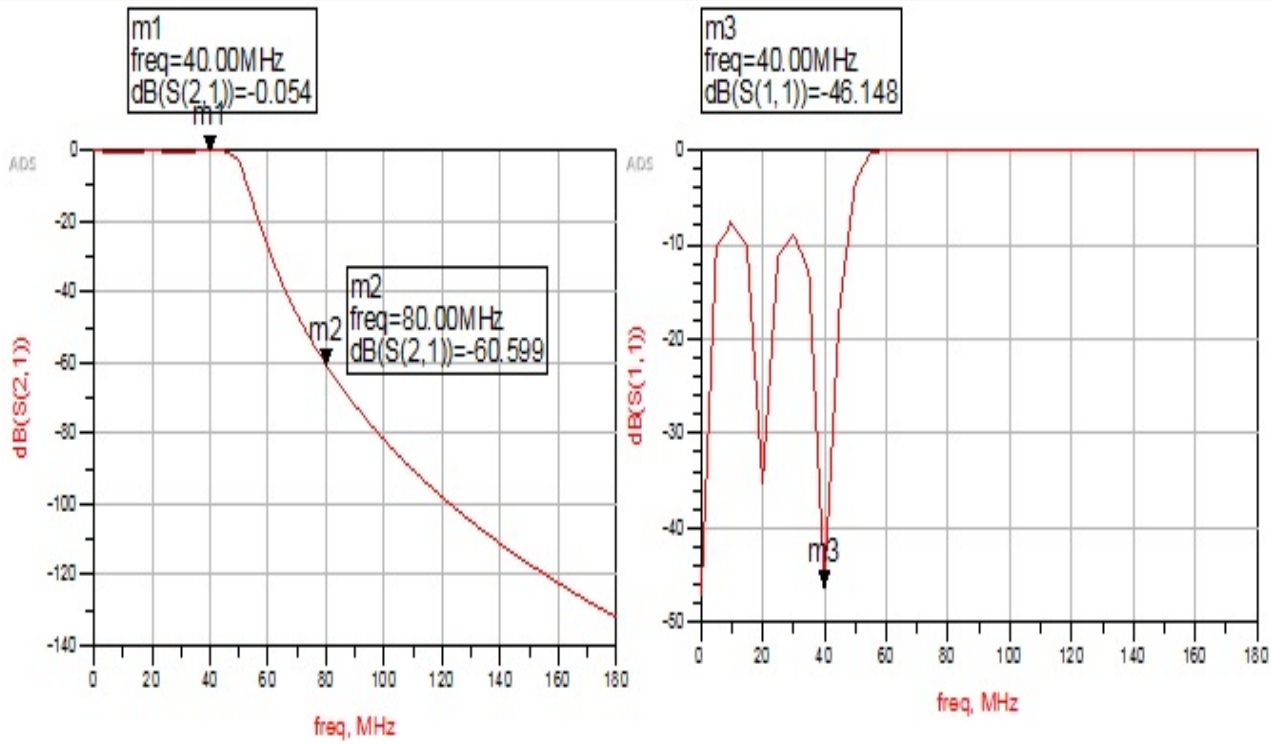
Filter is tuned by changing the value of capacitor according to the Equations(4.2)(4.3)(4.4). There are two types of simulation done in this schematic.

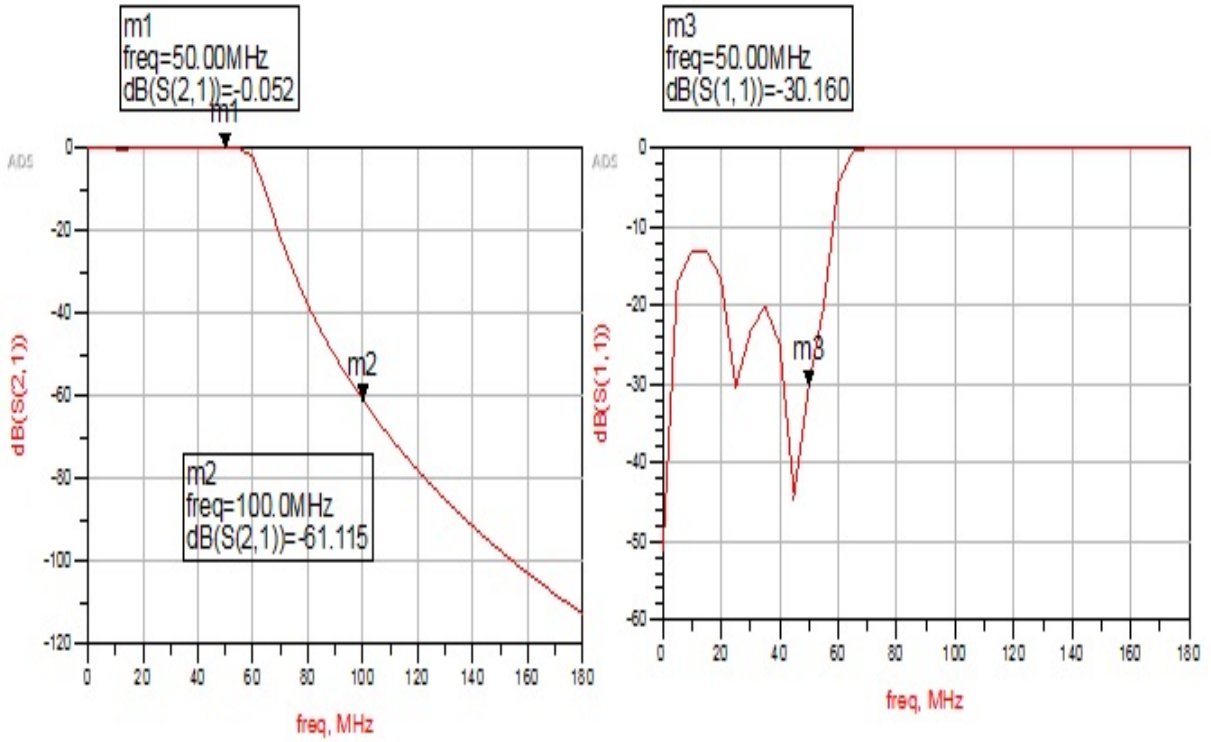
- S-Parameter simulation
- Harmonic Balance Simulation

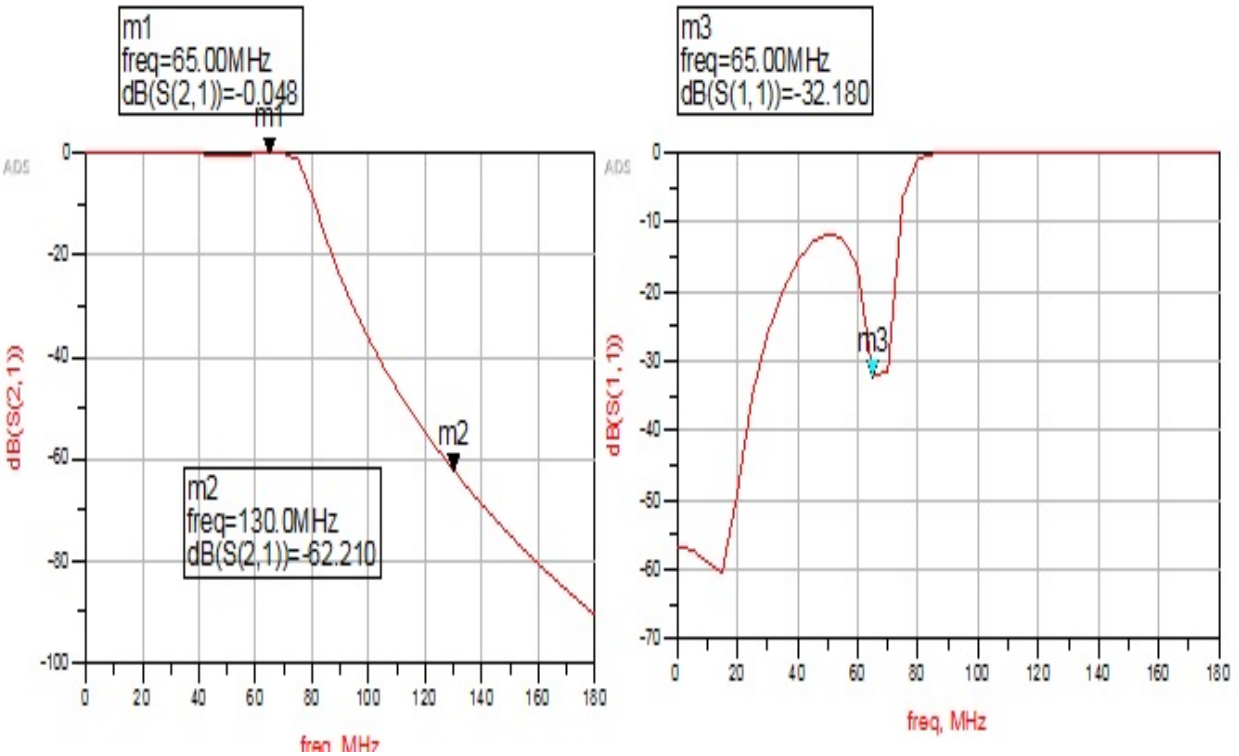
In S-Parameter simulation S(2,1) and S(1,1) is plotted in the responses shown in Figure 4.13 for several intermediate frequencies. While in Harmonic Balance simulation Input is given which is having harmonics and the output is observed. First response in Figure 4.14 shows the time domain input and output and the second one shows dBm input output.

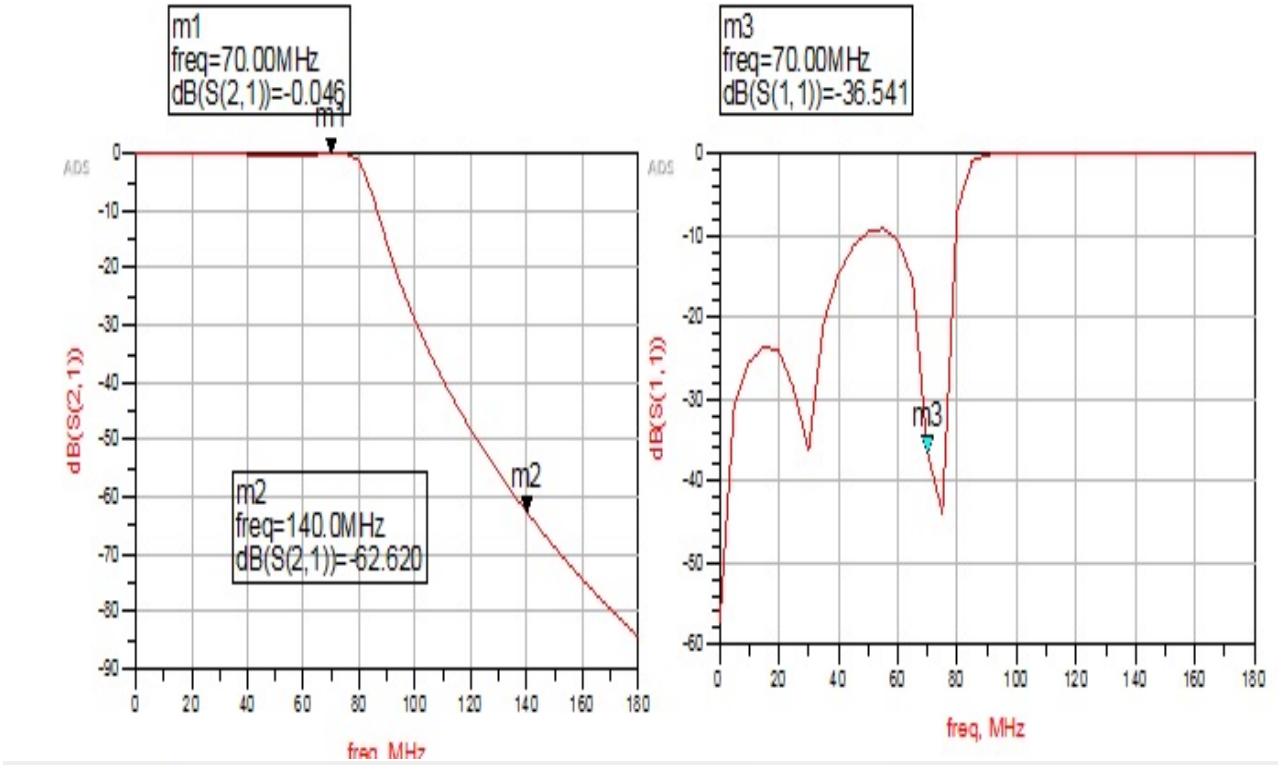
S-Parameter Simulation Response(30-90 MHz)

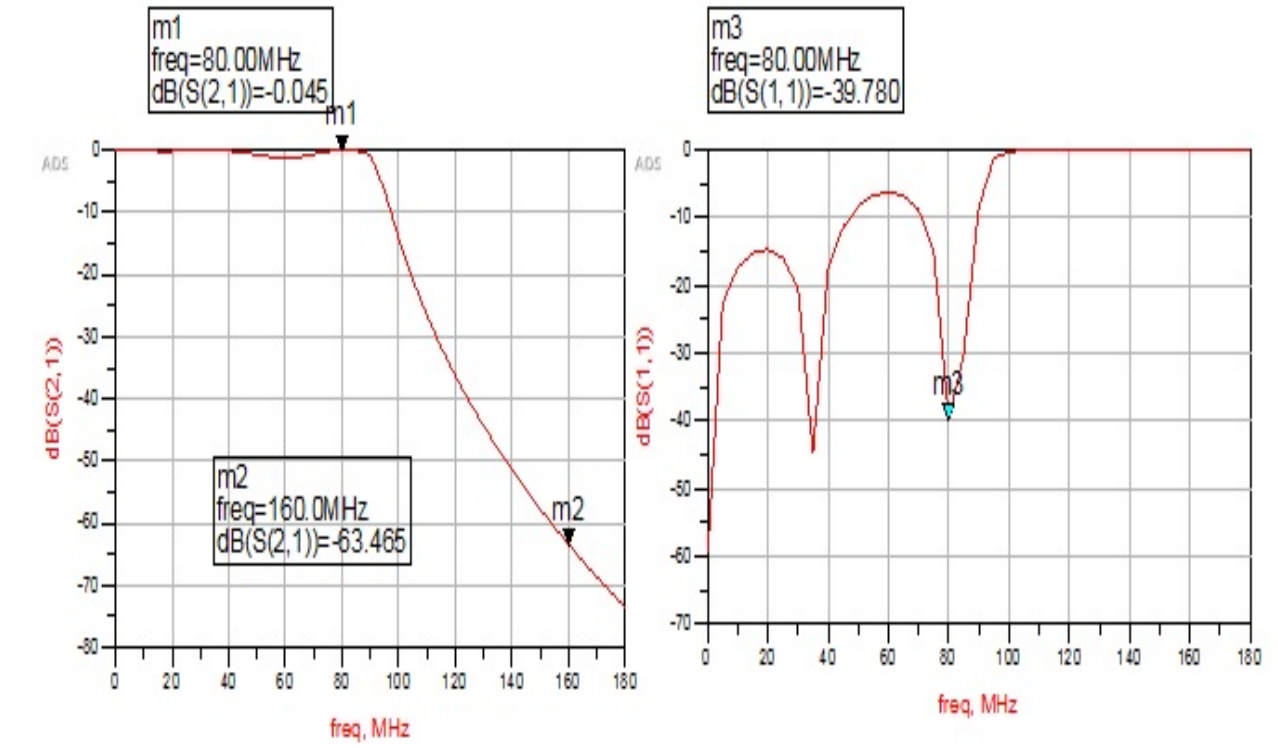





m1
freq=50.00MHz
dB(S(2,1))=-0.052
m1
m2
m2
freq=100.0MHz
dB(S(2,1))=-61.115
dB(S(2,1))
freq, MHz
m3
freq=50.00MHz
dB(S(1,1))=-30.160
m3
dB(S(1,1))
freq, MHz


m1
freq=65.00MHz
dB(S(2,1))=-0.048
m1
m2
m2
freq=130.0MHz
dB(S(2,1))=-62.210
dB(S(2,1))
m3
freq=65.00MHz
dB(S(1,1))=-32.180
m3
dB(S(1,1))
freq, MHz


m1
freq=70.00MHz
dB(S(2,1))=-0.046
m2
freq=140.0MHz
dB(S(2,1))=-62.620
dB(S(2,1))
freq, MHz
m3
freq=70.00MHz
dB(S(1,1))=-36.541
dB(S(1,1))
freq, MHz


m1
freq=80.00MHz
dB(S(2,1))=-0.045
m2
freq=160.0MHz
dB(S(2,1))=-63.465
dB(S(2,1))
freq, MHz
m3
freq=80.00MHz
dB(S(1,1))=-39.780
dB(S(1,1))
freq, MHz

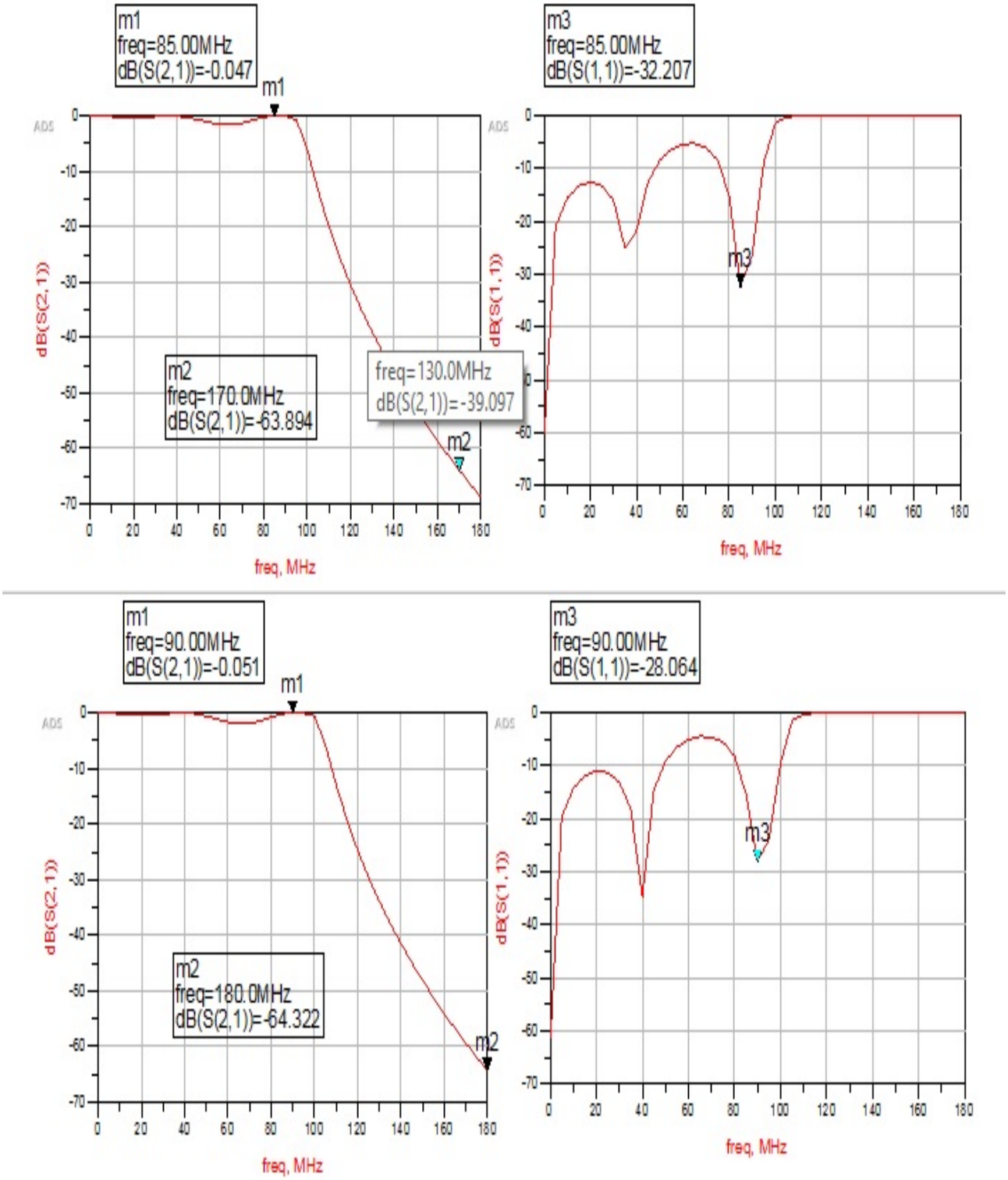
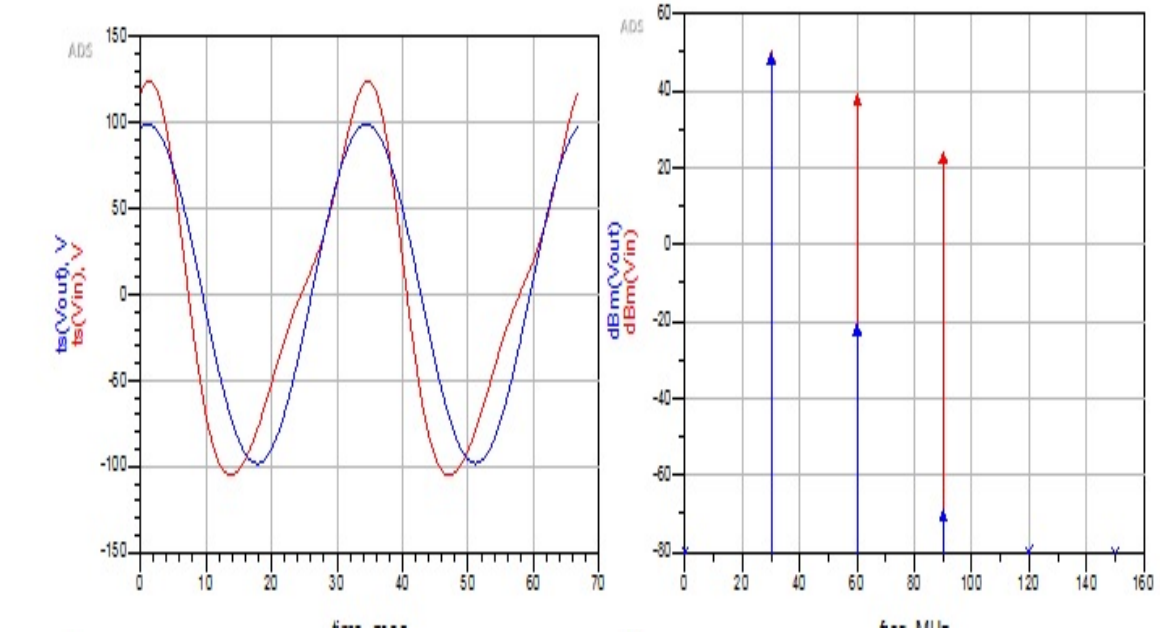
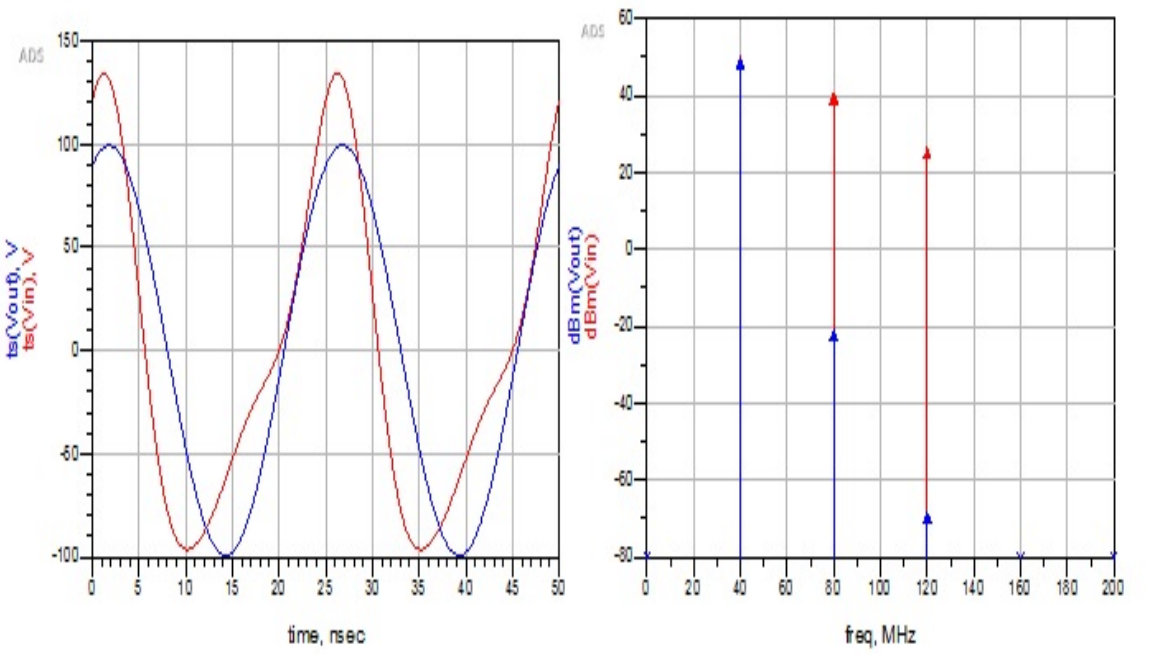
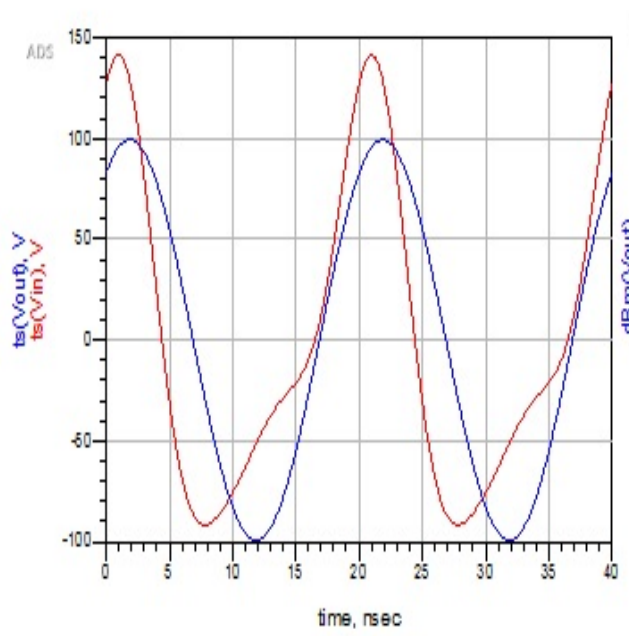


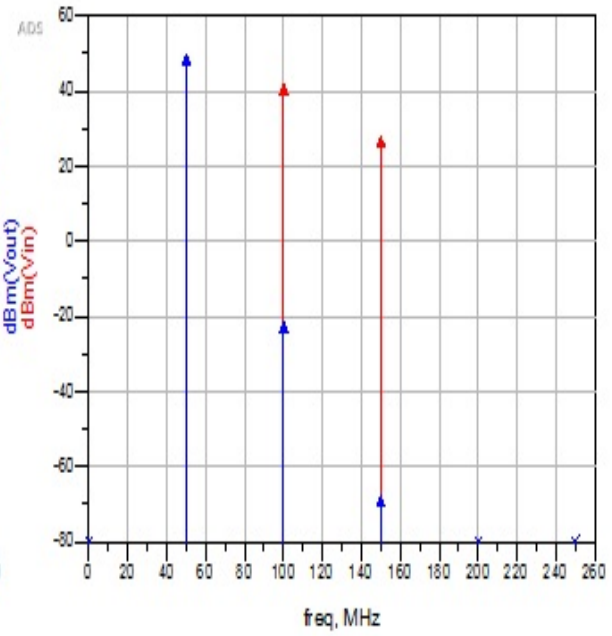
Figure 4.13: S Parameter simulation Response

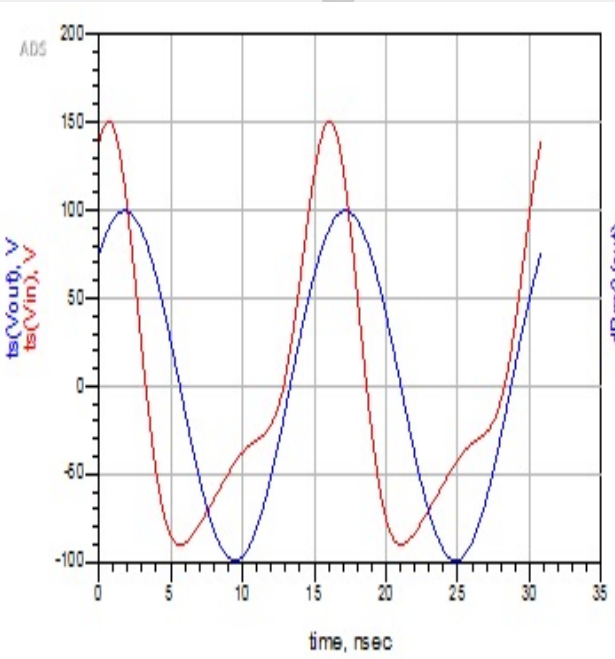
Harmonic Balance Simulation Response (30-90 MHz)

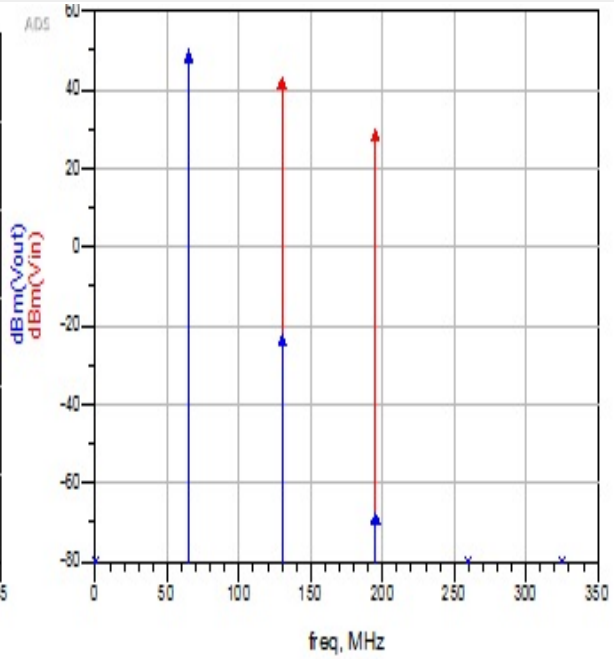


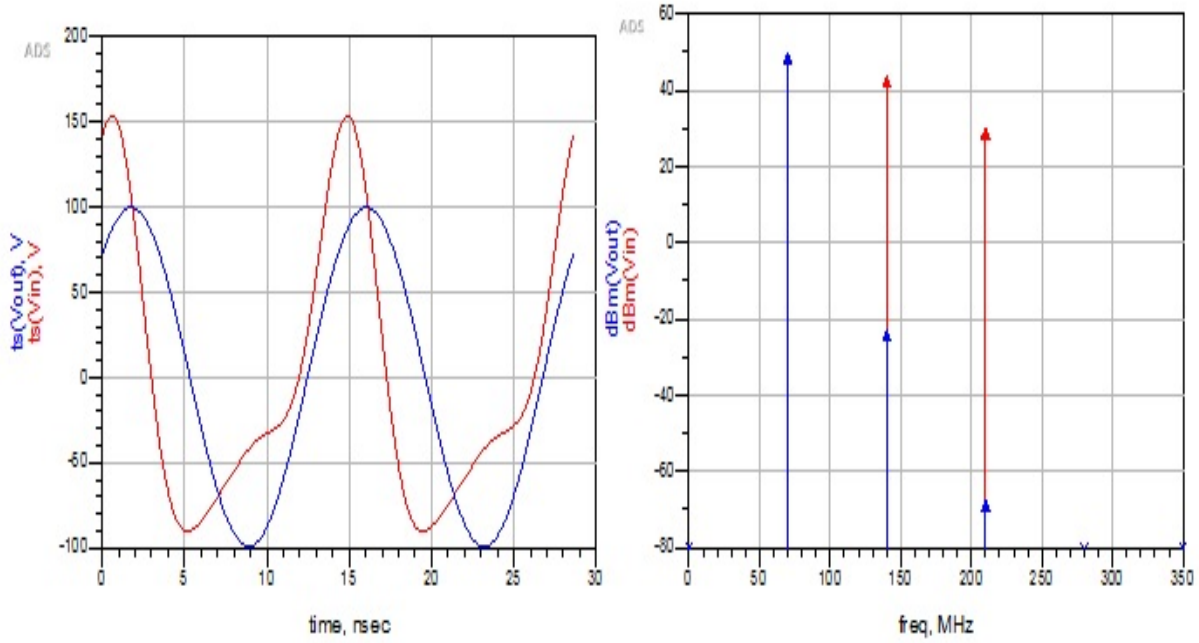


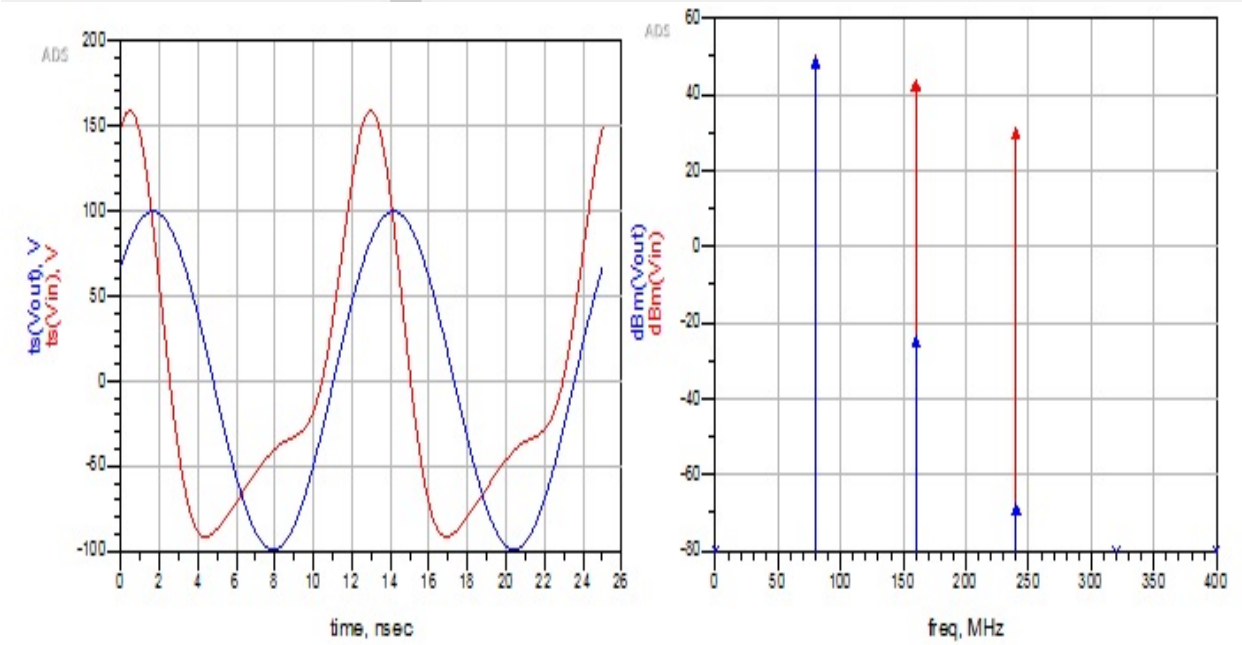

ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm(Vout)
dBm(Vin)
freq, MHz


ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm(Vout)
dBm(Vin)
freq, MHz


ADS
ts(Vout), V
ts(Vin), V
time, nsec
ADS
dBm(Vout)
dBm(Vin)
freq, MHz


ADS
ts(Vout), V
ts(Vin), V
time, nsec
ADS
dBm(Vout)
dBm(Vin)
freq, MHz

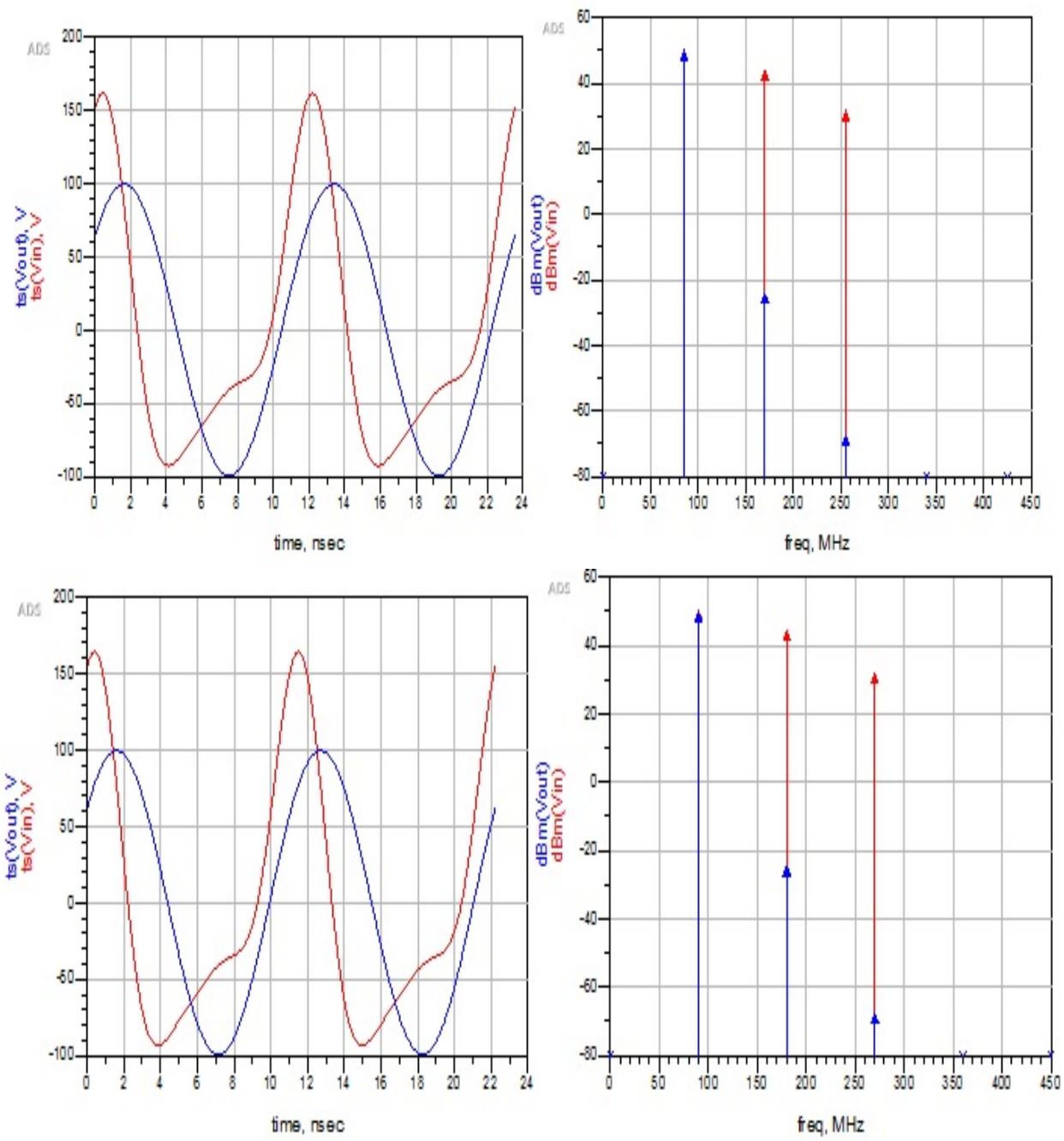


Figure 4.14: Harmonic Balance simulation Response

4.4 Filter Bank (90-270 MHz)

For filter bank from 90-270 MHz, fixed filter of 180 MHz has been made by the Equation (4.1). The capacitors and inductors values has been calculated as given in Section (3.2.3). The capacitance and inductance value is mentioned in Table 4.2.

Coefficients	Inductor(mH)	Capacitor(uF)
1	60.24	27.8
2	66.39	36.5
3	66.39	42.9
4	60.24	36.5
5	NA	27.8

Table 4.2: Component values of 180 MHz fixed filter.

Now tunning has been done as per section 4.2. The values of capacitors for intermediate frequencies is given in Table 4.3. The frequencies are taken in interval of 10 MHz.

S.No.	**Freq(MHz)**	**Capacitor1 (pF)**	**Capacitor2 (pF)**	**Capacitor3 (pF)**
1	90	53.2	125.9	111.1
2	100	49.2	102.2	94.0
3	110	45.4	84.7	80.8
4	120	41.7	71.3	70.4
5	130	38.3	60.9	62.0
6	140	35.1	52.6	55.2
7	150	32.0	45.9	49.4
8	160	29.2	40.4	44.6
9	170	26.6	35.8	40.6
10	180	24.1	32.0	37.0
11	190	21.9	28.7	34.0
12	200	19.9	26.0	31.3
13	210	18.0	23.6	29.0
14	220	16.4	21.5	27.0
15	230	15.0	19.7	25.1
16	240	13.7	18.1	23.5
17	250	12.7	16.7	22.0
18	260	11.9	15.5	20.7
19	270	11.2	14.3	19.5

Table 4.3: Tuned capacitor value FILTER 2

Now these values of capacitors are plotted in MS-excel, where we can get the equation by which it is varying. The graph is plotted in Fig 4.15 (a) (b) (c)

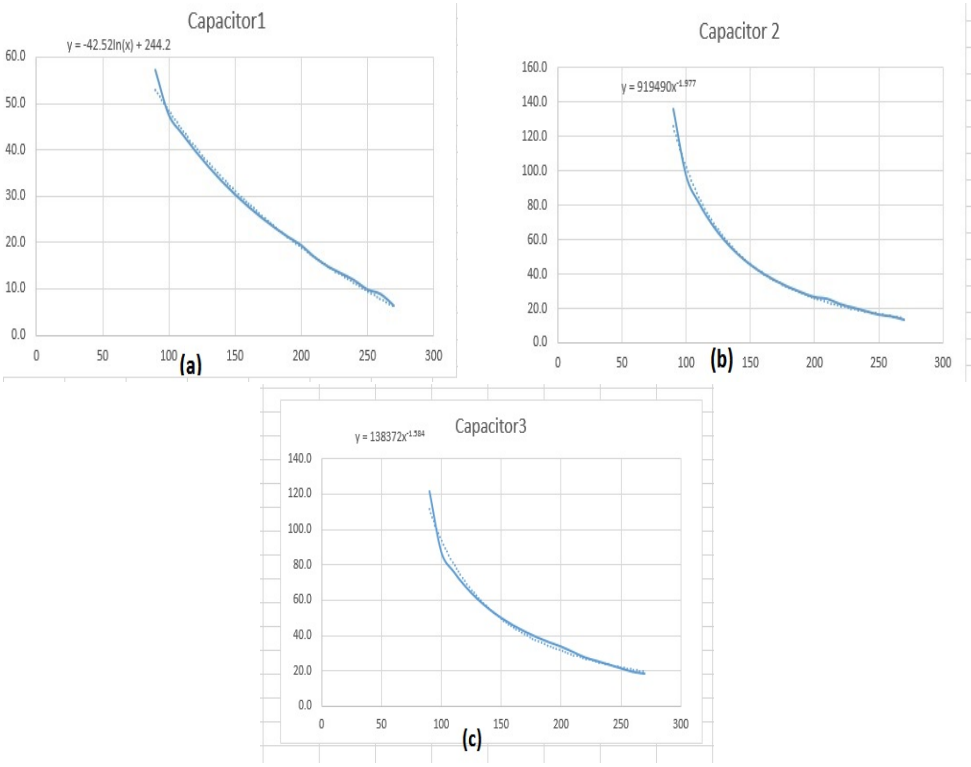


Figure 4.15: Tuned capacitor value plot Filter2

After plotting the values as shown above we get the frequency dependent equation of by which these capacitance vales varies with frequency.

The equations which we get is given below:

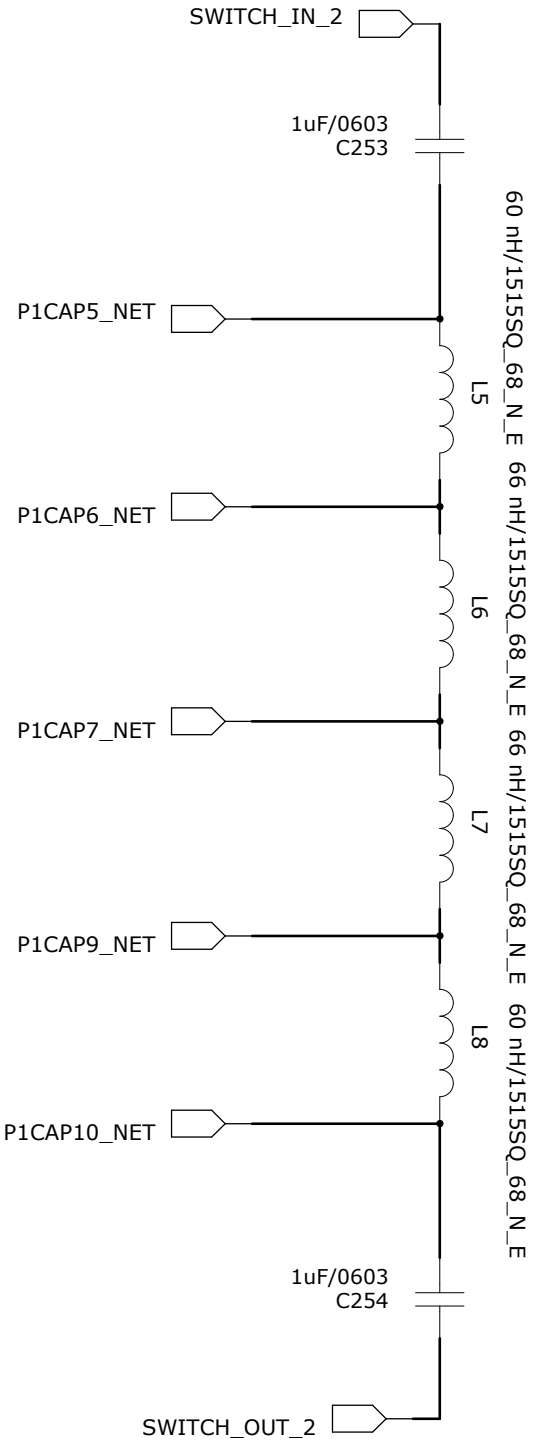
$$C_1 = -42.52 \ln(f_c) + 244.2 \tag{4.5}$$

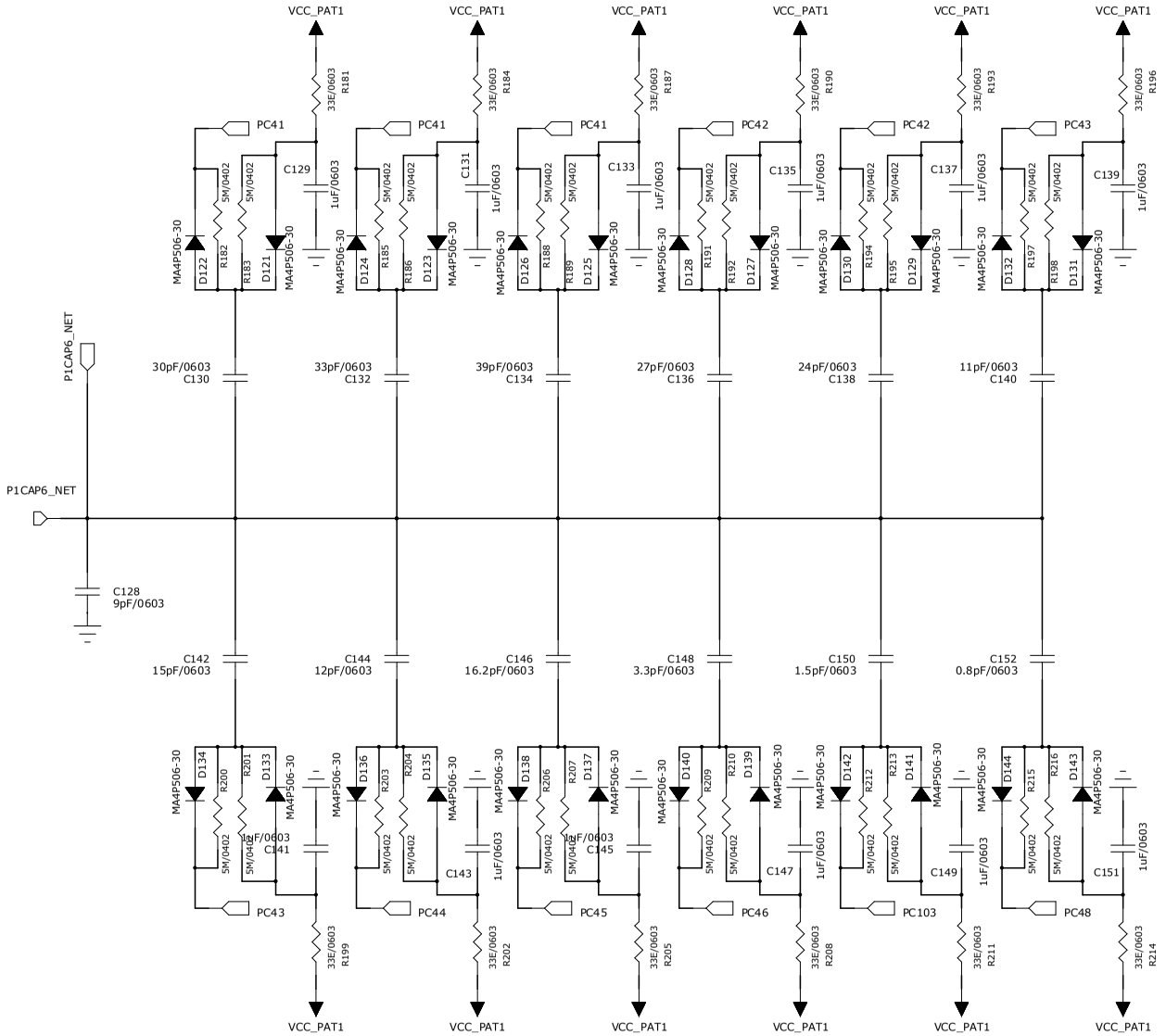
$$C_2 = 919490 f_c^{-1.997} \tag{4.6}$$

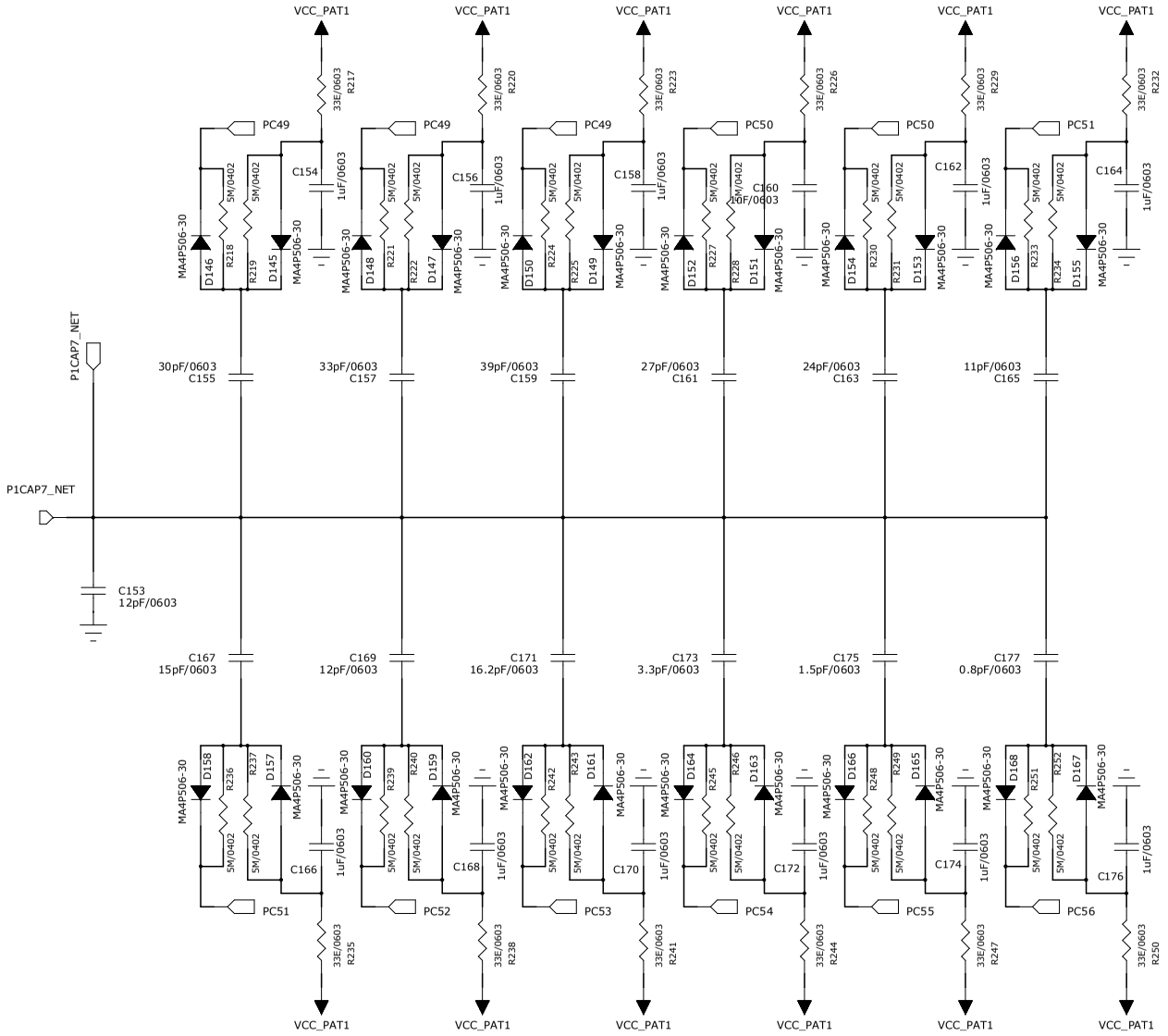
$$C_3 = 138372 f_c^{-1.584} \tag{4.7}$$

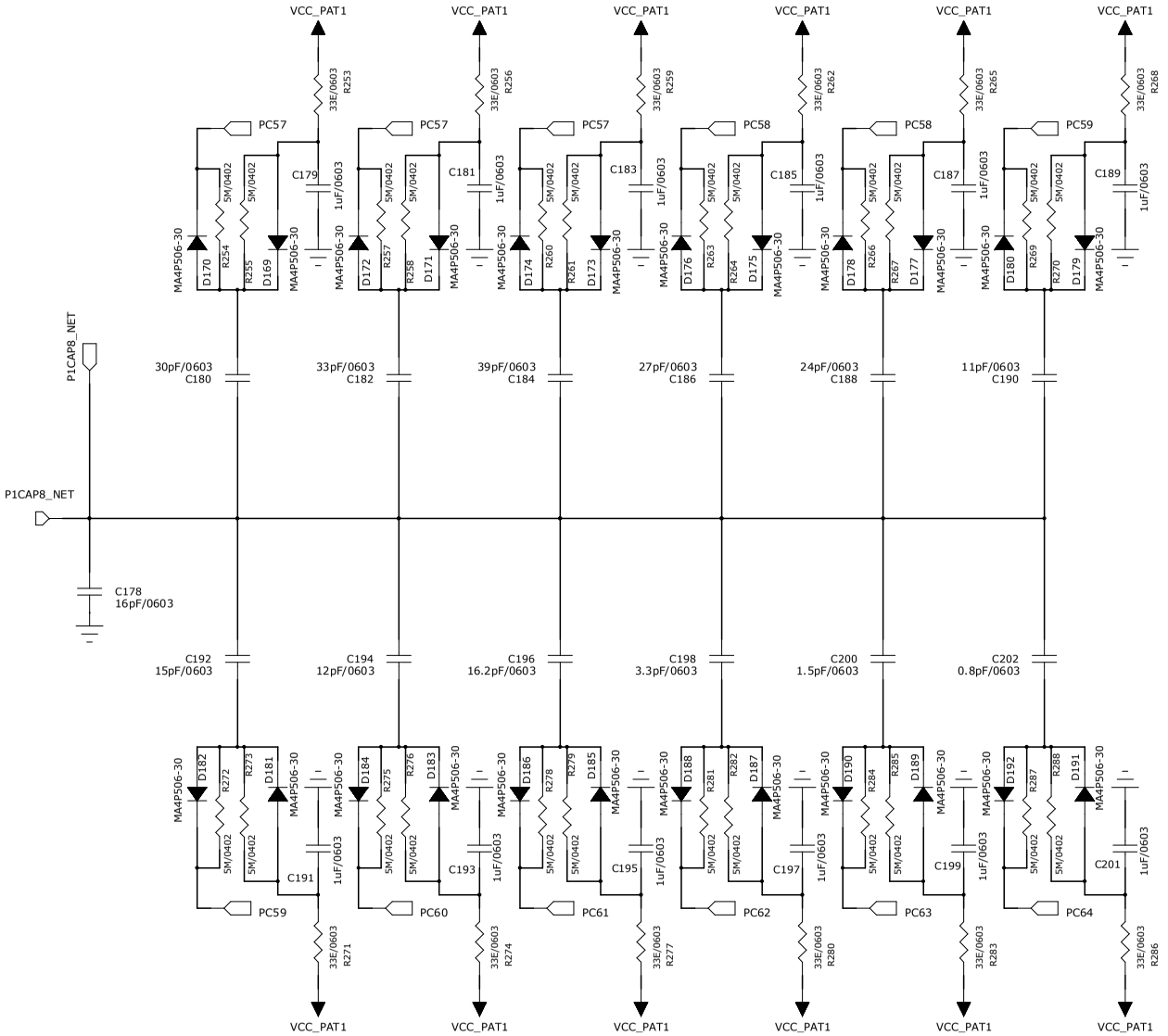
The schematic in PADS logic is given in Figure 4.16.

4.4.1 Schematic of RF section




VCC_PAT1
PC41
PC42
PC43
PC44
PC45
PC46
PC103
PC48
C129
C131
C133
C135
C137
C139
C141
C143
C145
C147
C149
C151
R181
R184
R187
R190
R193
R196
R199
R202
R205
R208
R211
R214
D122
D121
D124
D123
D126
D125
D128
D127
D130
D129
D132
D131
D134
D133
D136
D135
D138
D137
D140
D139
D142
D141
D144
D143
R182
R183
R185
R186
R188
R189
R191
R192
R194
R195
R197
R198
R200
R201
R203
R204
R206
R207
R209
R210
R212
R213
R215
R216
MA4P506-30
5M/0402
33E/0603
1uF/0603
P1CAP6_NET
C128
9pF/0603
C130
30pF/0603
C132
33pF/0603
C134
39pF/0603
C136
27pF/0603
C138
24pF/0603
C140
11pF/0603
C142
15pF/0603
C144
12pF/0603
C146
16.2pF/0603
C148
3.3pF/0603
C150
1.5pF/0603
C152
0.8pF/0603


VCC_PAT1
PC49
PC50
PC51
PC52
PC53
PC54
PC55
PC56
33E/0603
R217
R220
R223
R226
R229
R232
C154
C156
C158
C160
C162
C164
1uF/0603
10F/0603
5M/0402
MA4P506-30
D146
D145
D148
D147
D150
D149
D152
D151
D154
D153
D156
D155
R218
R219
R221
R222
R224
R225
R227
R228
R230
R231
R233
R234
P1CAP7_NET
C153
12pF/0603
30pF/0603
C155
33pF/0603
C157
39pF/0603
C159
27pF/0603
C161
24pF/0603
C163
11pF/0603
C165
C167
15pF/0603
C169
12pF/0603
C171
16.2pF/0603
C173
3.3pF/0603
C175
1.5pF/0603
C177
0.8pF/0603
D158
D157
D160
D159
D162
D161
D164
D163
D166
D165
D168
D167
R236
R237
R239
R240
R242
R243
R245
R246
R248
R249
R251
R252
C166
C168
C170
C172
C174
C176
R235
R238
R241
R244
R247
R250


VCC_PAT1
PC57
PC58
PC59
C179
C181
C183
C185
C187
C189
1uF/0603
33E/0603
R253
R256
R259
R262
R265
R268
5M/0402
MA4P506-30
D170
R254
R255
D169
D172
R257
R258
D171
D174
R260
R261
D173
D176
R263
R264
D175
D178
R266
R267
D177
D180
R269
R270
D179
P1CAP8_NET
30pF/0603
C180
33pF/0603
C182
39pF/0603
C184
27pF/0603
C186
24pF/0603
C188
11pF/0603
C190
C178
16pF/0603
C192
15pF/0603
C194
12pF/0603
C196
16.2pF/0603
C198
3.3pF/0603
C200
1.5pF/0603
C202
0.8pF/0603
D182
R272
R273
D181
D184
R275
R276
D183
D186
R278
R279
D185
D188
R281
R282
D187
D190
R284
R285
D189
D192
R287
R288
D191
C191
C193
C195
C197
C199
C201
PC60
PC61
PC62
PC63
PC64
R271
R274
R277
R280
R283
R286

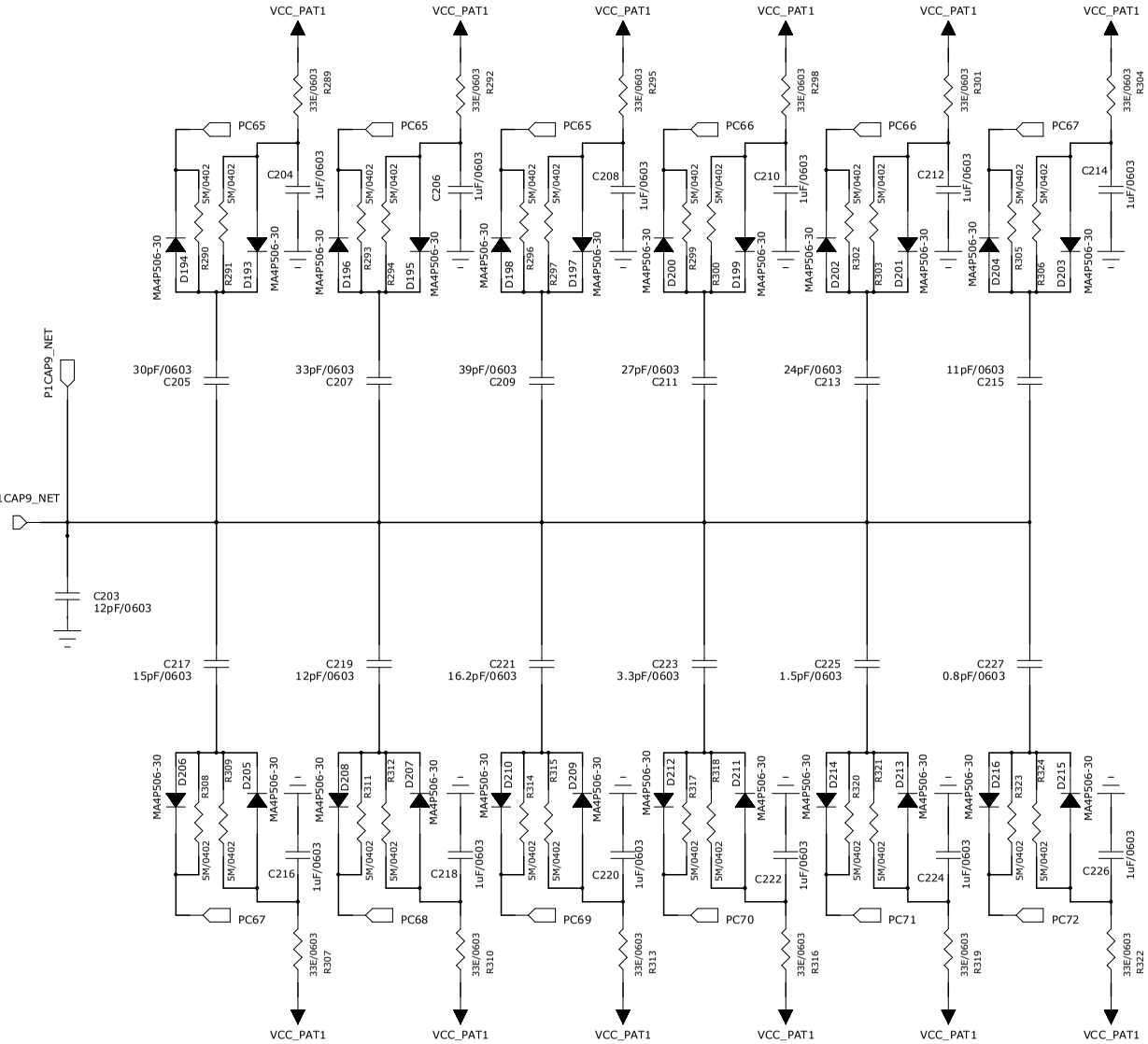
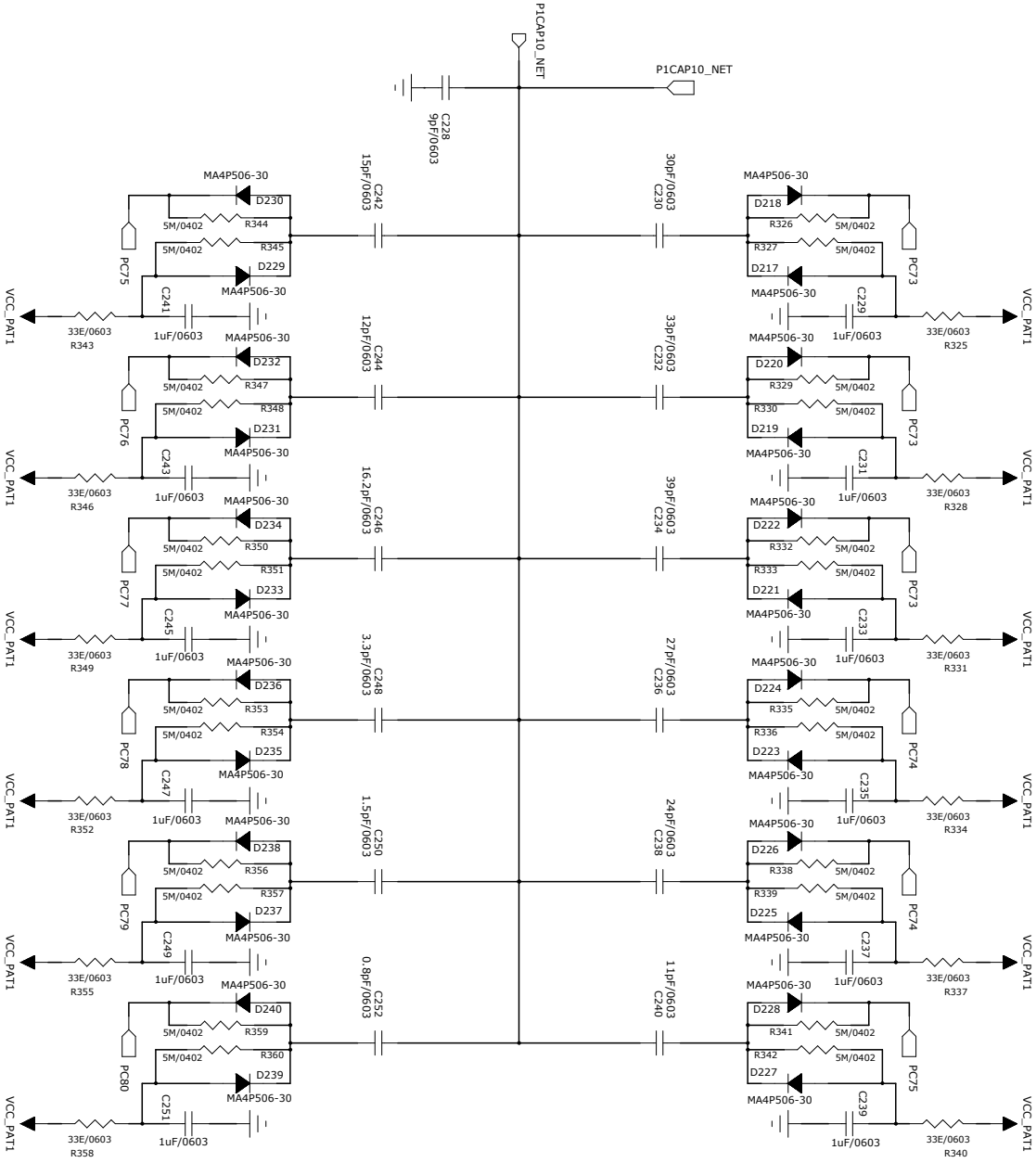

VCC_PAT1
P1CAP9_NET
C203
12pF/0603
30pF/0603
C205
33pF/0603
C207
39pF/0603
C209
27pF/0603
C211
24pF/0603
C213
11pF/0603
C215
C217
15pF/0603
C219
12pF/0603
C221
16.2pF/0603
C223
3.3pF/0603
C225
1.5pF/0603
C227
0.8pF/0603
PC65
PC66
PC67
PC68
PC69
PC70
PC71
PC72
MA4P506-30
5M/0402
1uF/0603
33E/0603

Figure 4.16: PADS schematic for Filter 2



4.4.2 ADS simulation (90-270 MHz)

Simulation schematic diagram in Agilent ADS is given in Figure 4.17 .

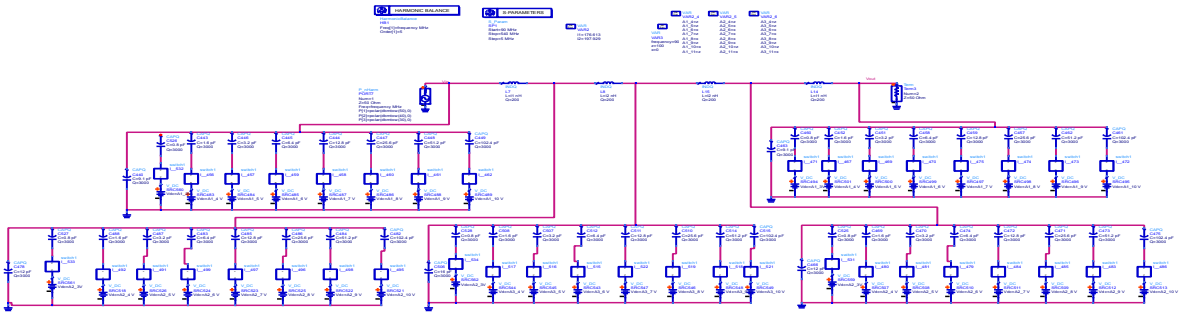


Figure 4.17: ADS schematic (90-270 MHz)

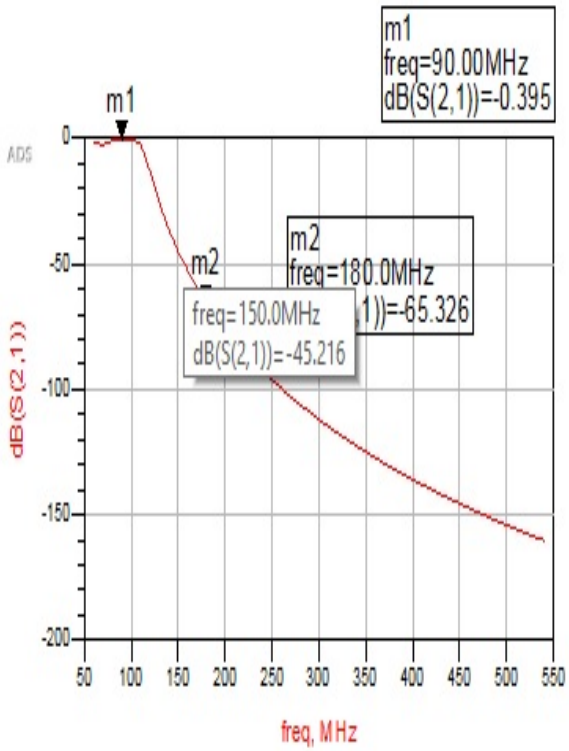
4.4.3 Simulation Response

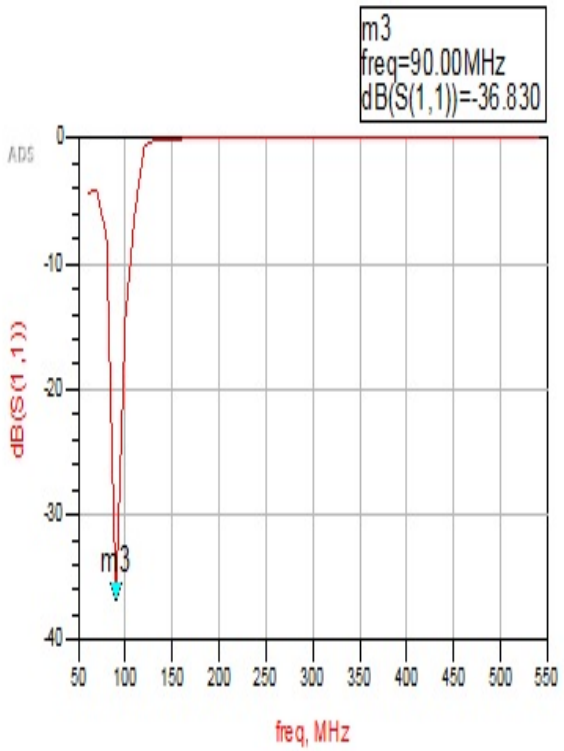
As we have done in section 4.3.2. Both the S-parameter and Harmonic balance simulation is done by manually tuning the capacitors in ADS.

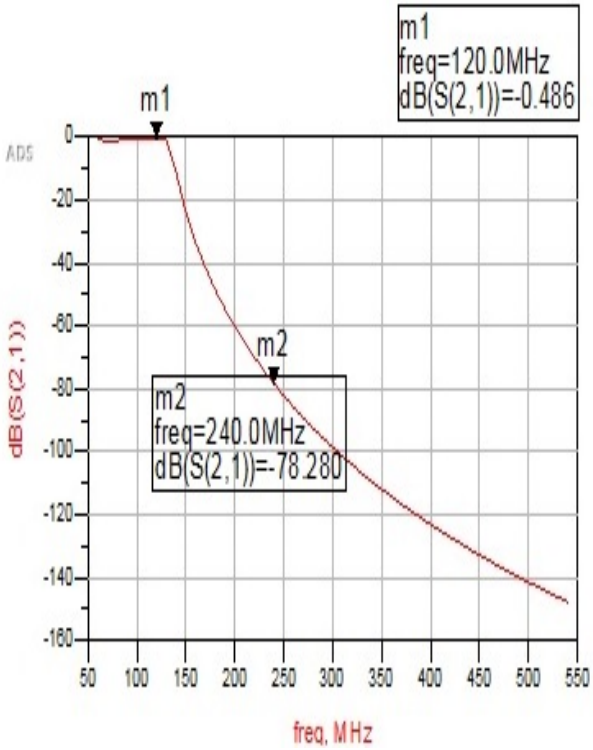
In S-parameter simulation we have find the S(2,1) and S(1,1) as it gives the insertion loss and return loss.

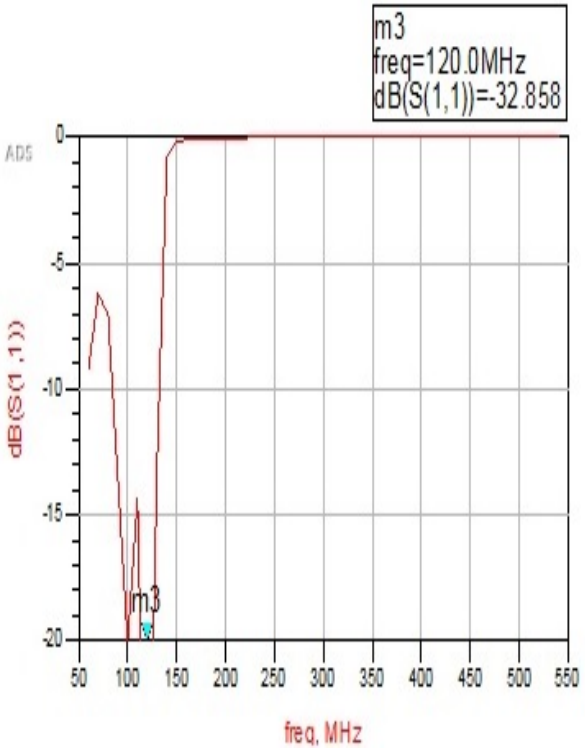
In Harmonic balance simulation we have given the a harmonic signal input and compared the output. First figure in harmonic simulation is time domain input output signals and the second one is input output signal in dBm.

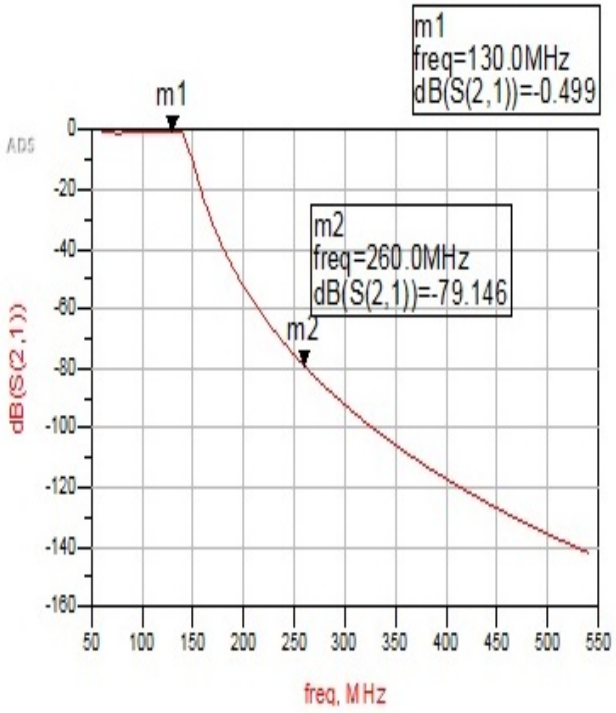
S-Parameter Simulation Response(90-270 MHz)

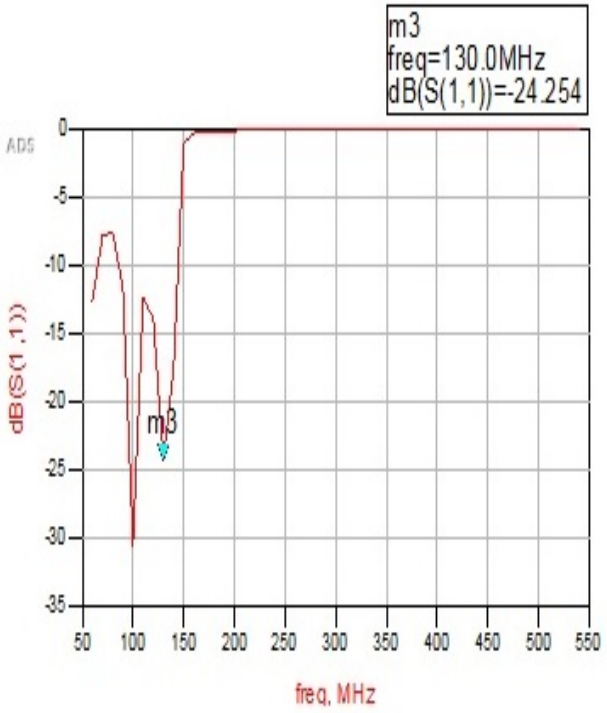


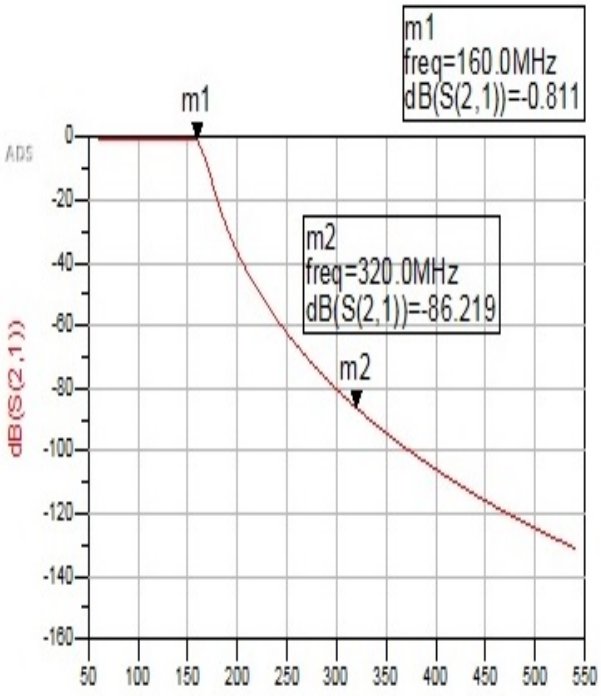


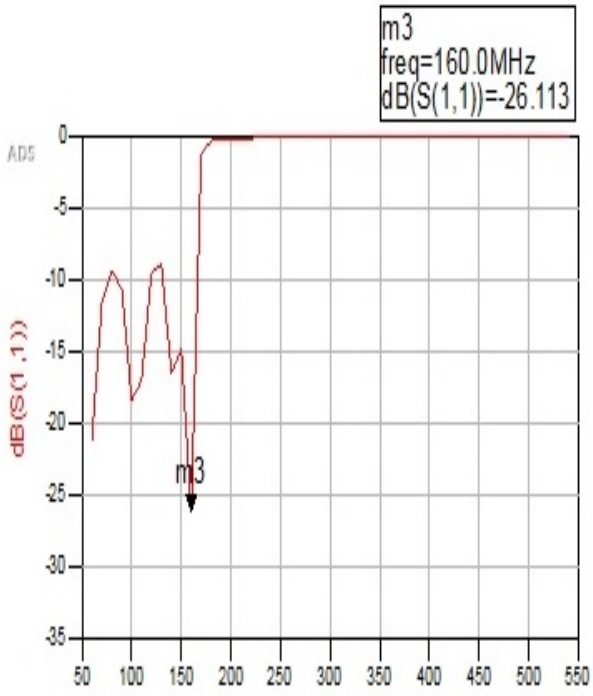


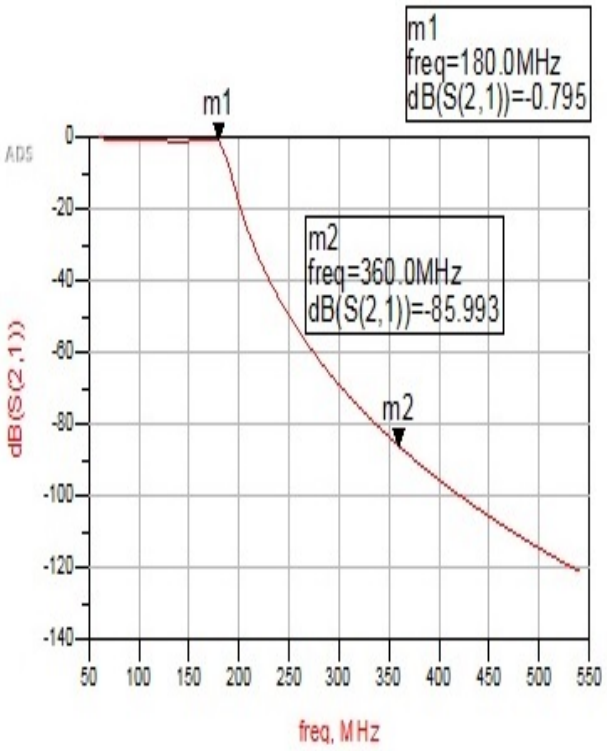


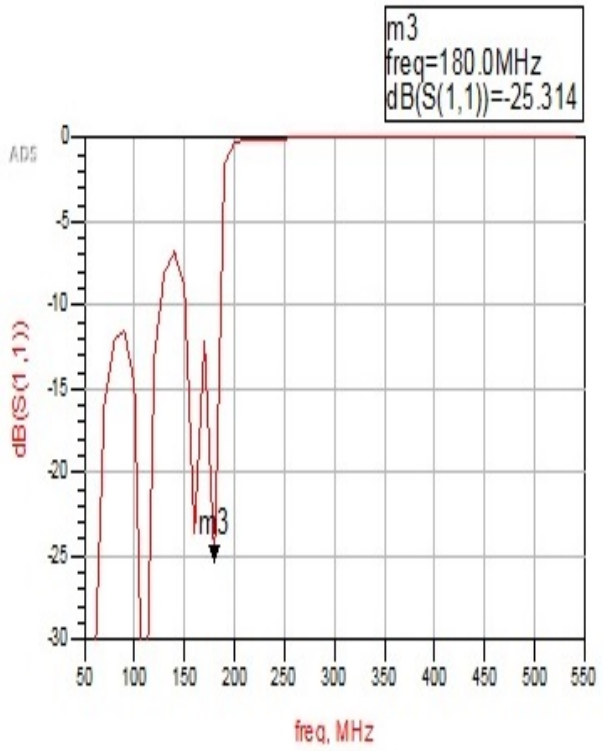

m1
freq=130.0MHz
dB(S(2,1))=-0.499
m2
freq=260.0MHz
dB(S(2,1))=-79.146
dB(S(2,1))
freq, MHz

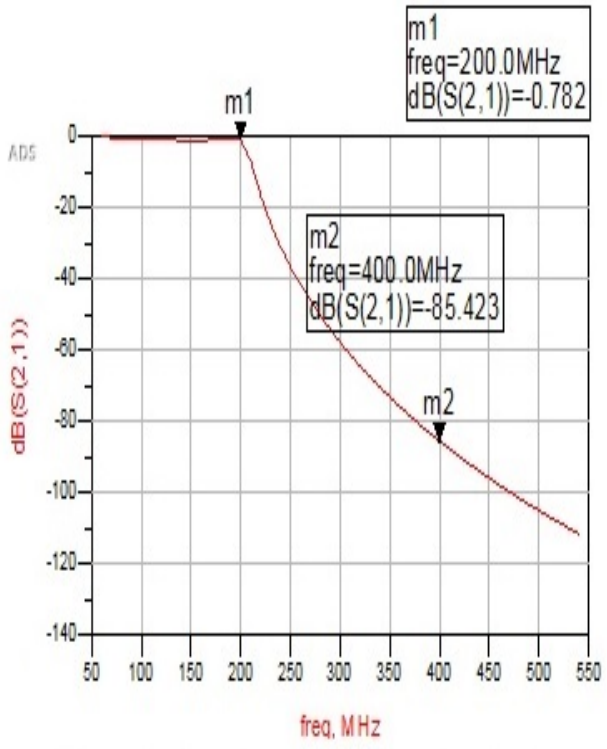

m3
freq=130.0MHz
dB(S(1,1))=-24.254
dB(S(1,1))
freq, MHz

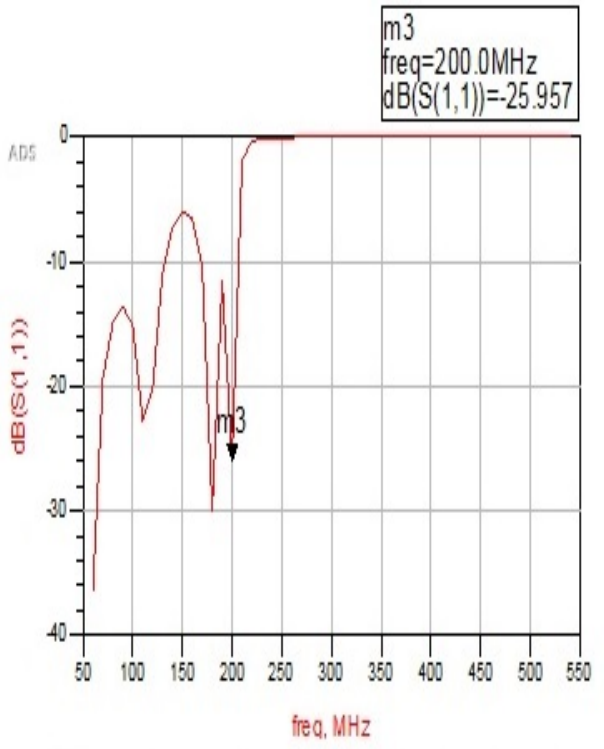

m1
freq=160.0MHz
dB(S(2,1))=-0.811
m2
freq=320.0MHz
dB(S(2,1))=-86.219
dB(S(2,1))

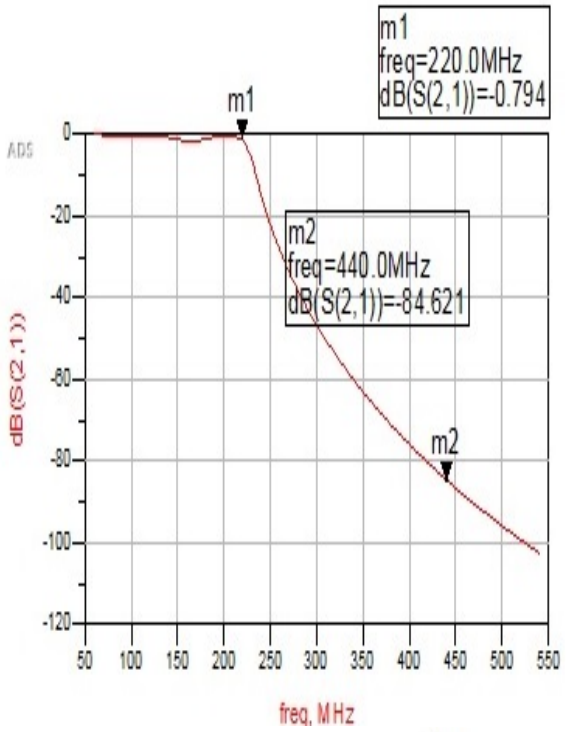

m3
freq=160.0MHz
dB(S(1,1))=-26.113
dB(S(1,1))

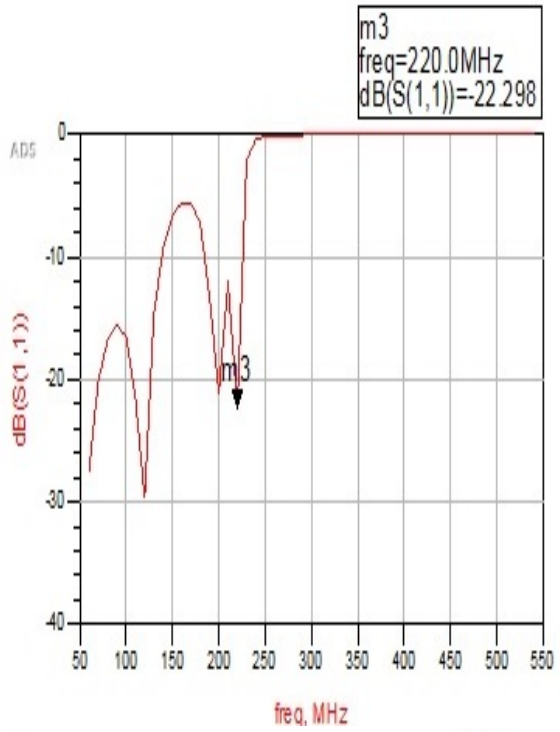

m1
freq=180.0MHz
dB(S(2,1))=-0.795
m2
freq=360.0MHz
dB(S(2,1))=-85.993
dB(S(2,1))
freq, MHz

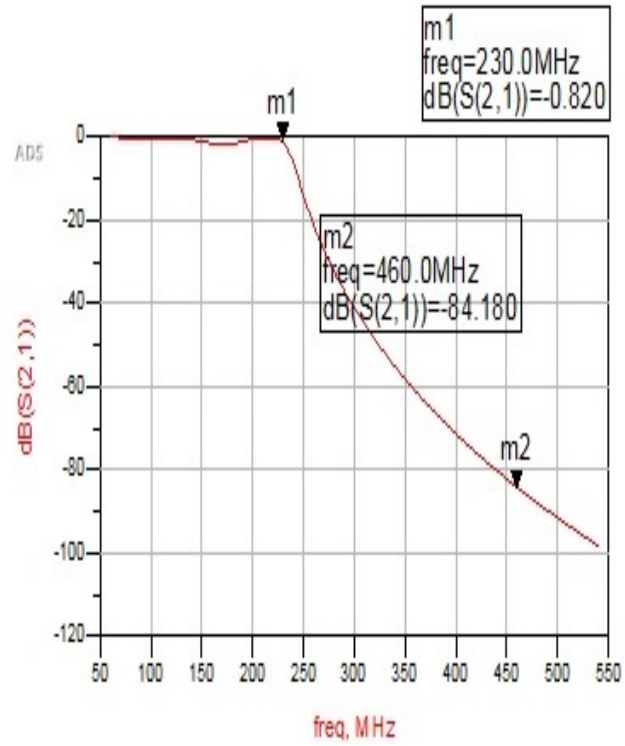

m3
freq=180.0MHz
dB(S(1,1))=-25.314
dB(S(1,1))
freq, MHz

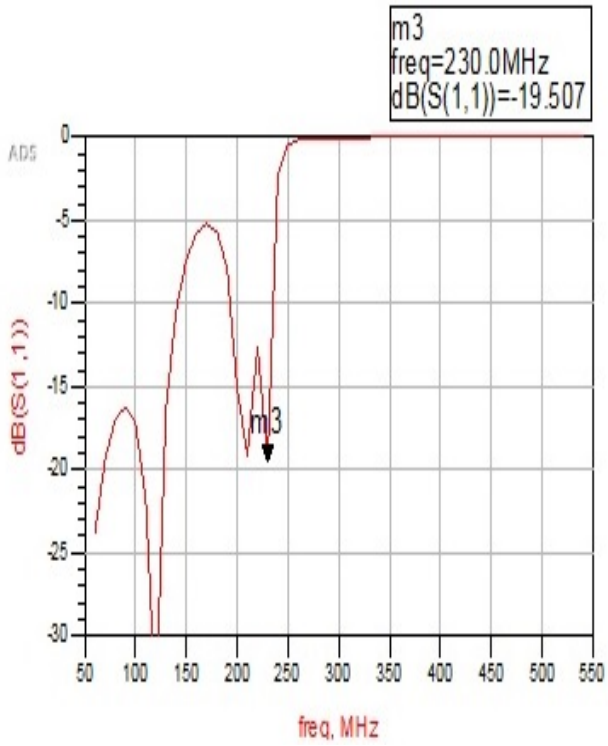

m1
freq=200.0MHz
dB(S(2,1))=-0.782
m2
freq=400.0MHz
dB(S(2,1))=-85.423
dB(S(2,1))
freq, MHz


m3
freq=200.0MHz
dB(S(1,1))=-25.957
dB(S(1,1))
freq, MHz


m1
freq=220.0MHz
dB(S(2,1))=-0.794
m2
freq=440.0MHz
dB(S(2,1))=-84.621
dB(S(2,1))
freq, MHz


m3
freq=220.0MHz
dB(S(1,1))=-22.298
dB(S(1,1))
freq, MHz


m1
freq=230.0MHz
dB(S(2,1))=-0.820
m2
freq=460.0MHz
dB(S(2,1))=-84.180
dB(S(2,1))
freq, MHz


m3
freq=230.0MHz
dB(S(1,1))=-19.507
dB(S(1,1))
freq, MHz

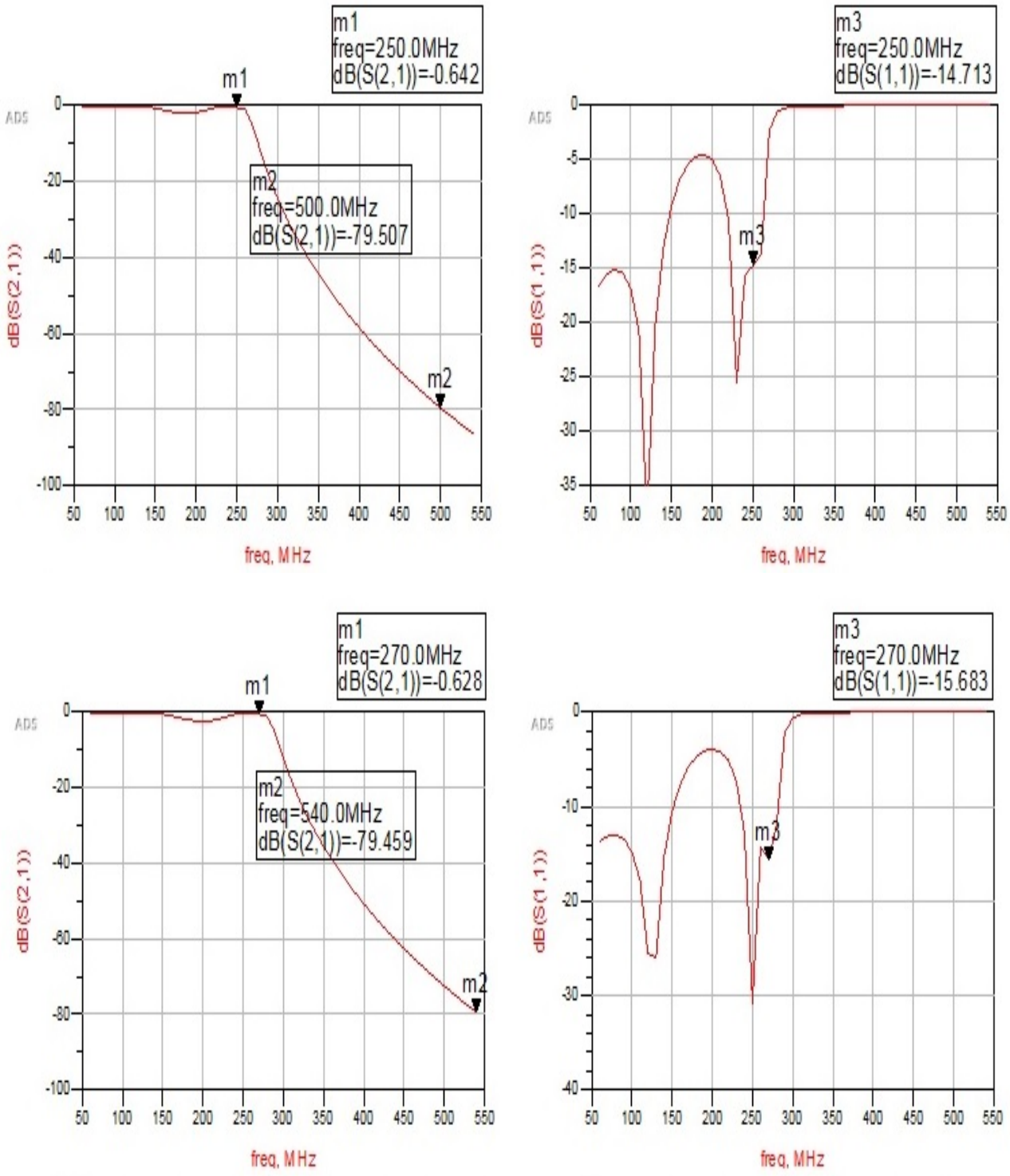
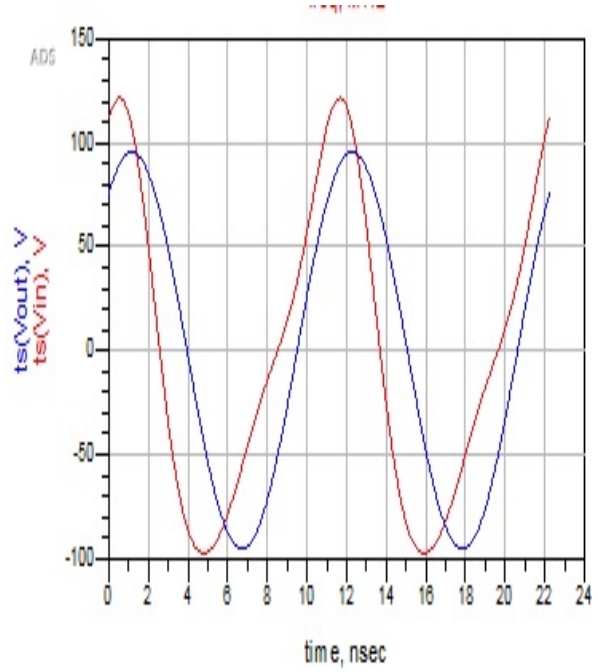
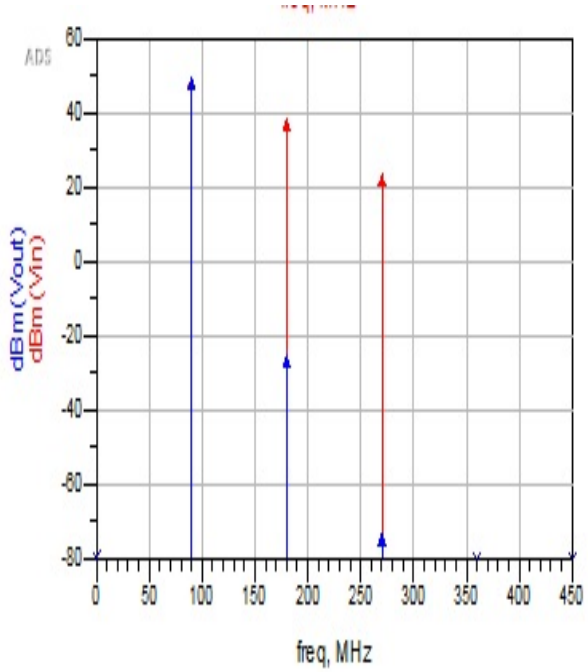
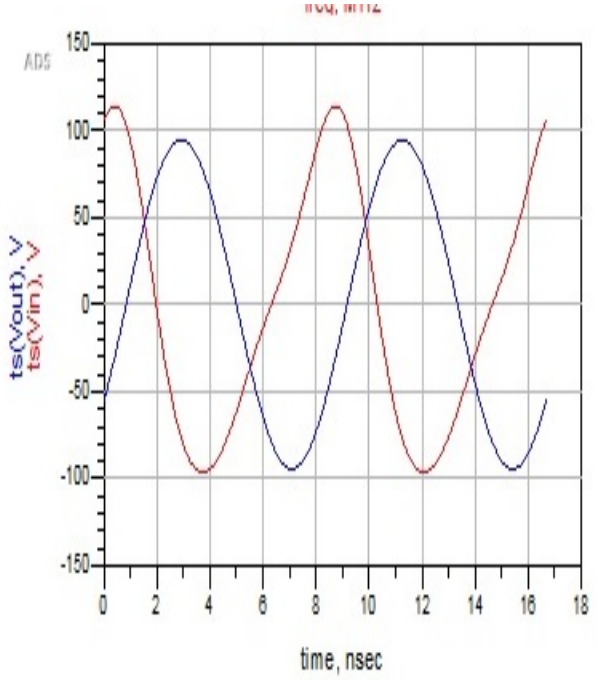


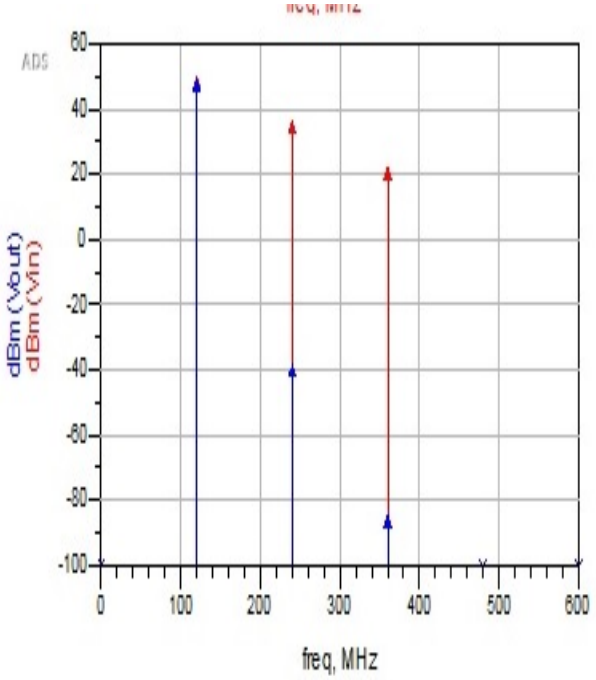
Figure 4.18: S Parameter simulation Response filter bank 2

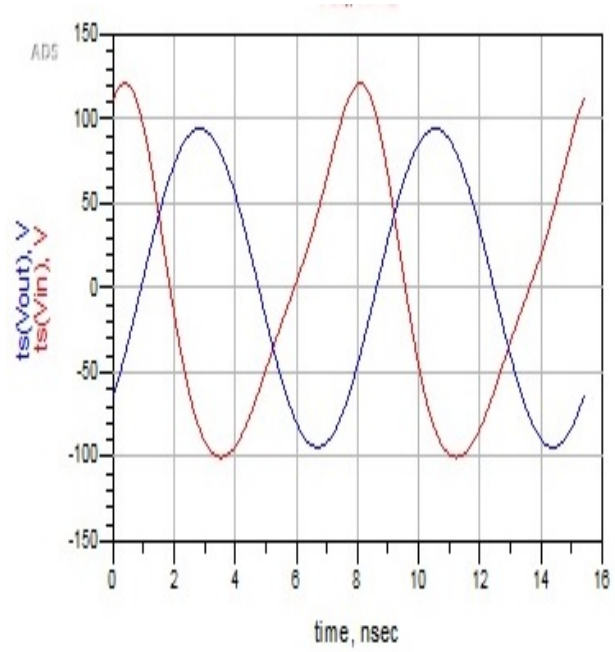
Harmonic Balance Simulation Response (90-270 MHz)

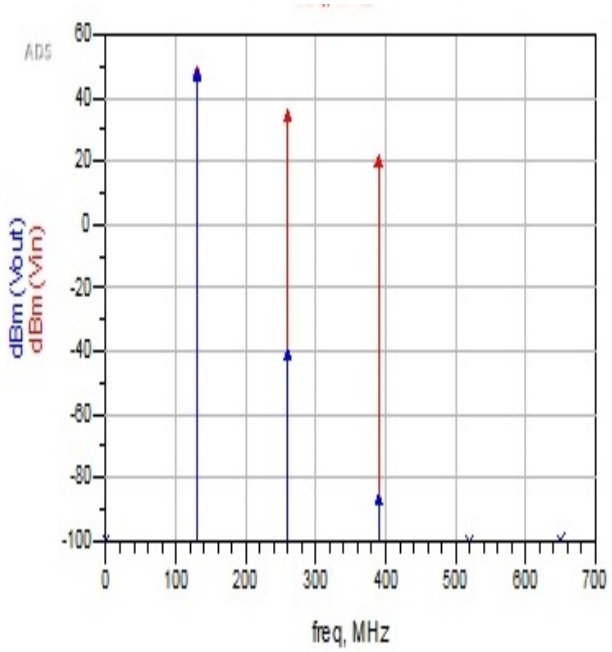


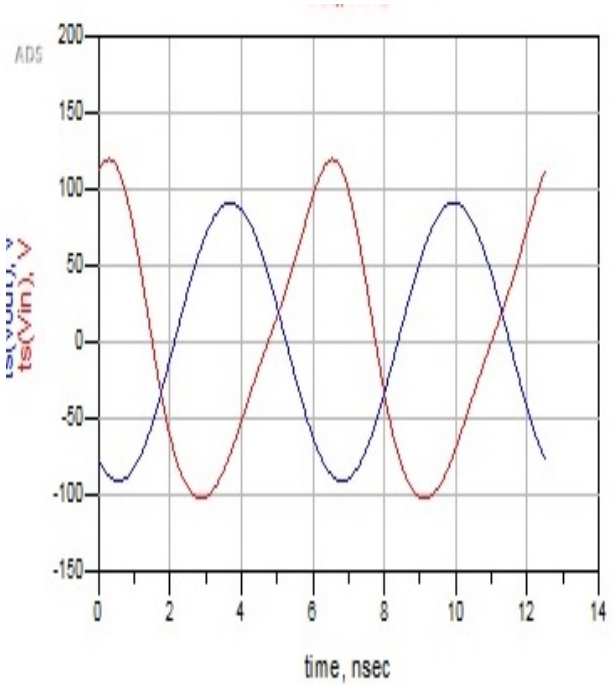


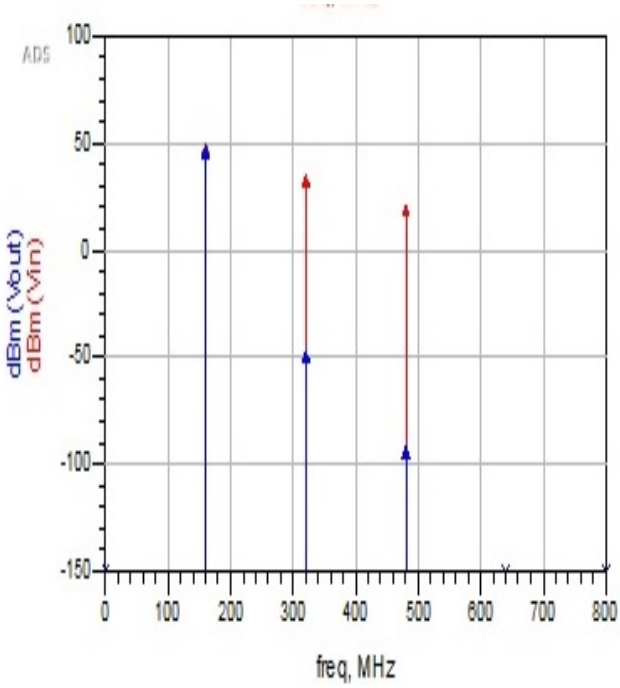


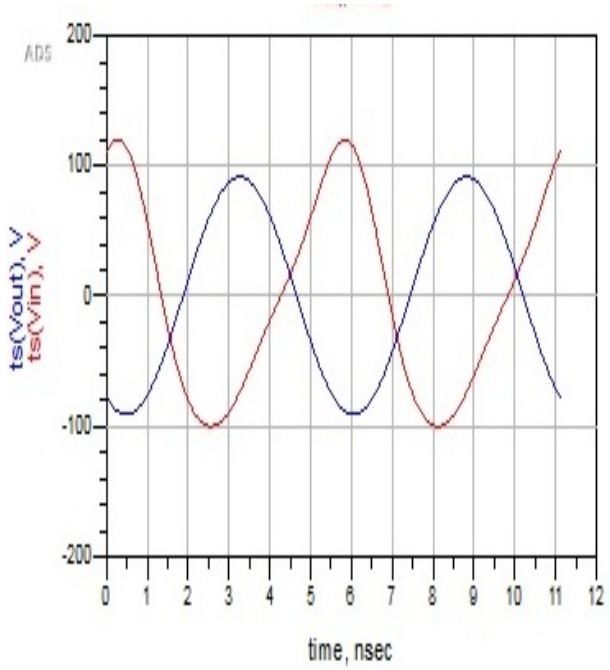


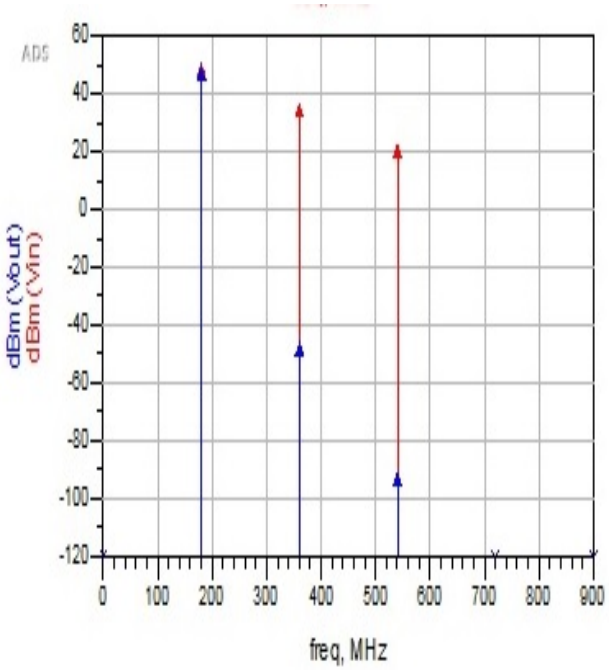

ADS
ts(Vout), V
ts(Vin), V
time, nsec

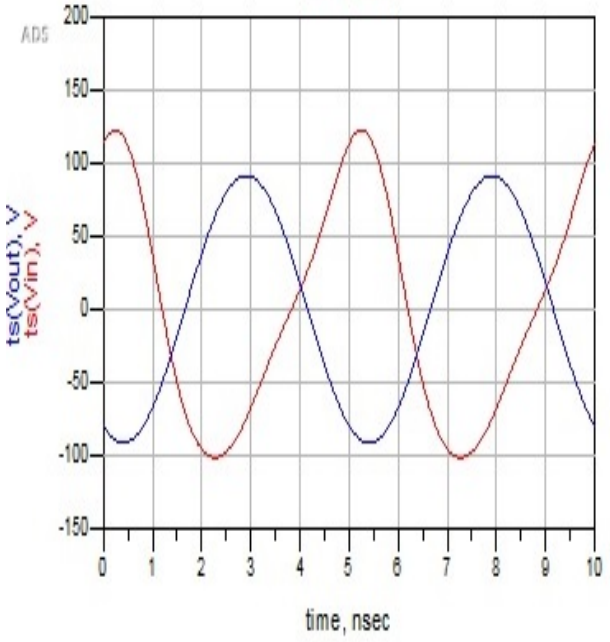

ADS
dBm (Vout)
dBm (Vin)
freq, MHz

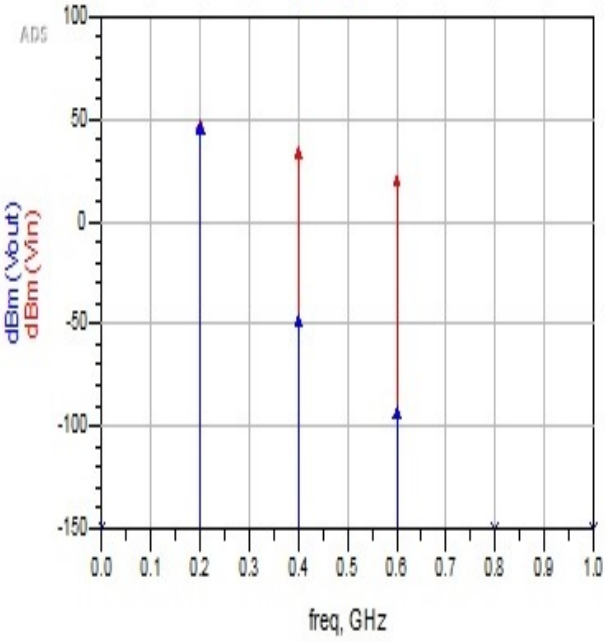

ADS
time, nsec

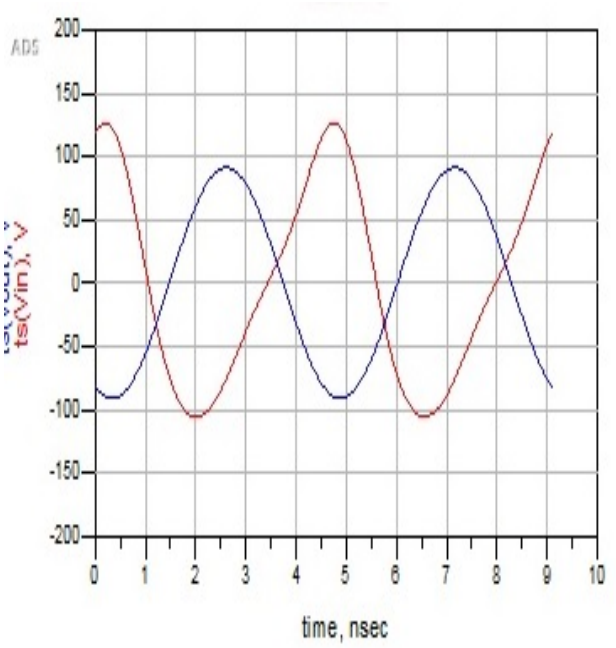

ADS
dBm (Vout)
dBm (Vin)
freq, MHz

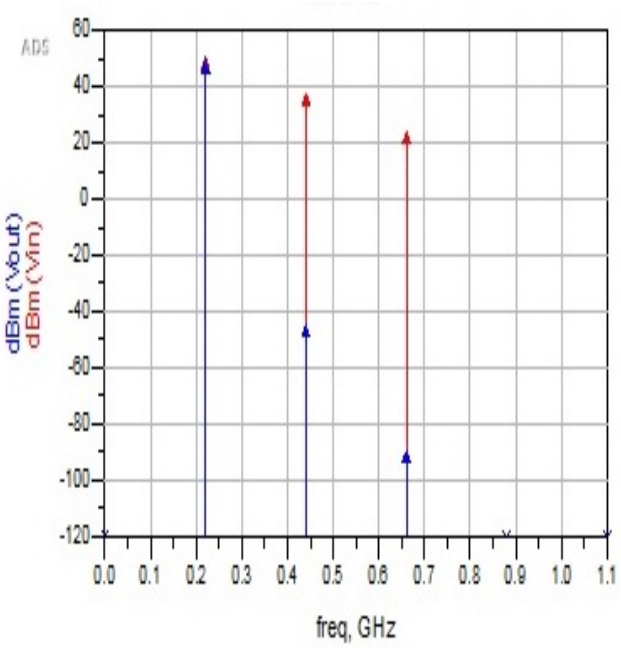

ADS
ts(Vout), V
ts(Vin), V
time, nsec

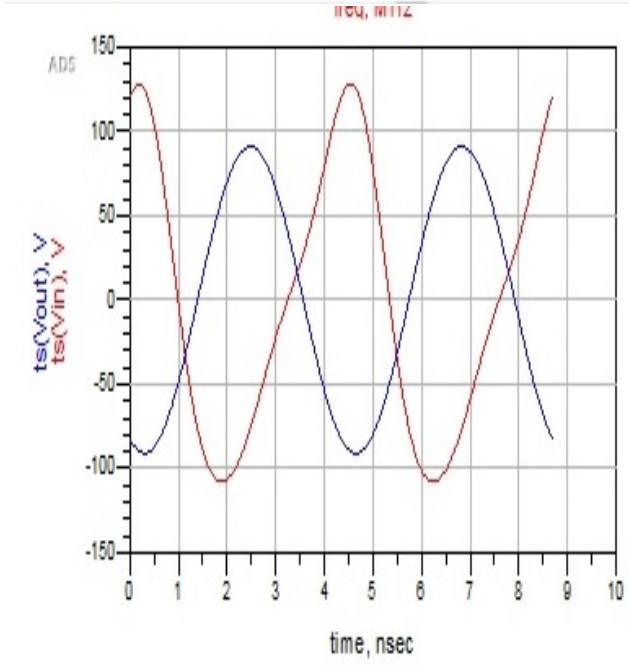

ADS
dBm (Vout)
dBm (Vin)
freq, MHz

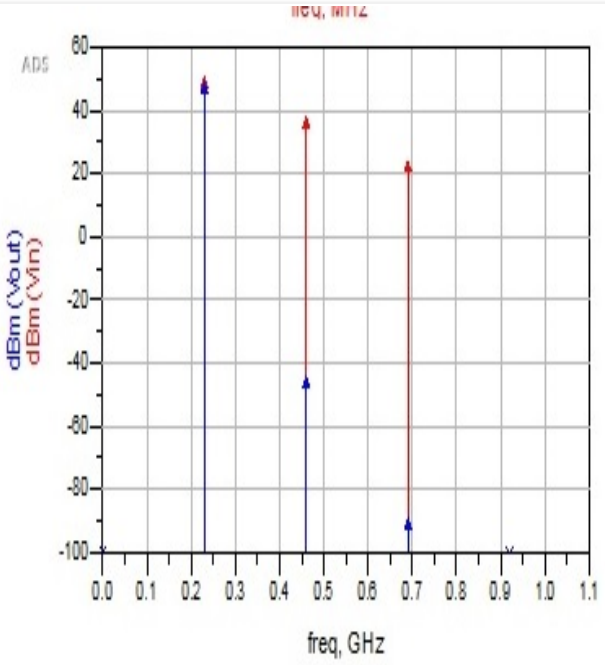

ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm (Vout)
dBm (Vin)
freq, GHz


ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm (Vout)
dBm (Vin)
freq, GHz


ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm (Vout)
dBm (Vin)
freq, GHz

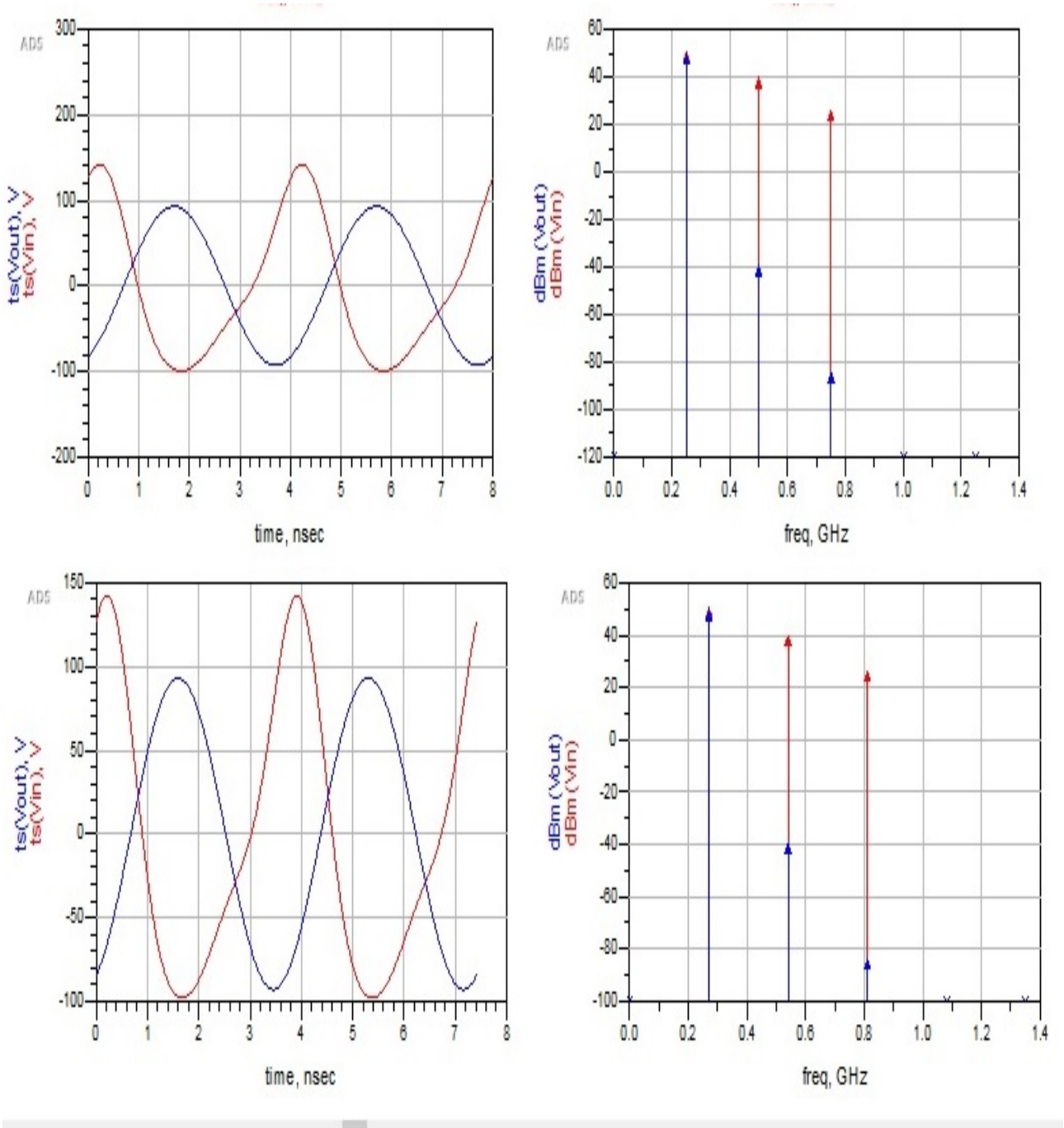


Figure 4.19: Harmonic Balance simulation Response filter bank 2

4.5 Filter Bank (270-520 MHz)

For filter bank from 270-520 MHz, fixed filter of 400 MHz has been made by the Equation (4.1). From equation 4.1 395 MHz frequency is coming. So we took its nearest decimal value. The capacitors and inductors values has been calculated as given in Section (3.2.3). The capacitance and inductance value is mentioned in Table 4.4.

Coefficients	Inductor(mH)	Capacitor(uF)
1	27	9.6
2	30.5	16.8
3	30.5	18.3
4	27	16.8
5	NA	9.6

Table 4.4: Component values of 400 MHz fixed filter.

Now tunning has been done as per section 4.2. The values of capacitors for intermediate frequencies is given in Table 4.5. The frequencies are taken in interval of 10 MHz.

S.No.	**Freq(MHz)**	**Capacitor1 (pF)**	**Capacitor2 (pF)**	**Capacitor3 (pF)**
1	270	20.0	32.5	28.3
2	290	18.1	29.4	26.1
3	310	16.4	26.6	24.1
4	330	14.8	24.1	22.2
5	350	13.4	21.8	20.5
6	370	12.1	19.7	18.9
7	390	11.0	17.8	17.5
8	400	10.4	17.0	16.8
9	420	9.4	15.4	15.5
10	440	8.5	13.9	14.3
11	460	7.7	12.6	13.2
12	480	7.0	11.4	12.2
13	500	6.3	10.3	11.3
14	520	5.7	9.3	10.4

Table 4.5: Tuned capacitor value FILTER 3

Now these values of capacitors are plotted in MS-excel, where we can get the equation by which it is varying. The graph is plotted in Fig 4.20 (a) (b) (c)

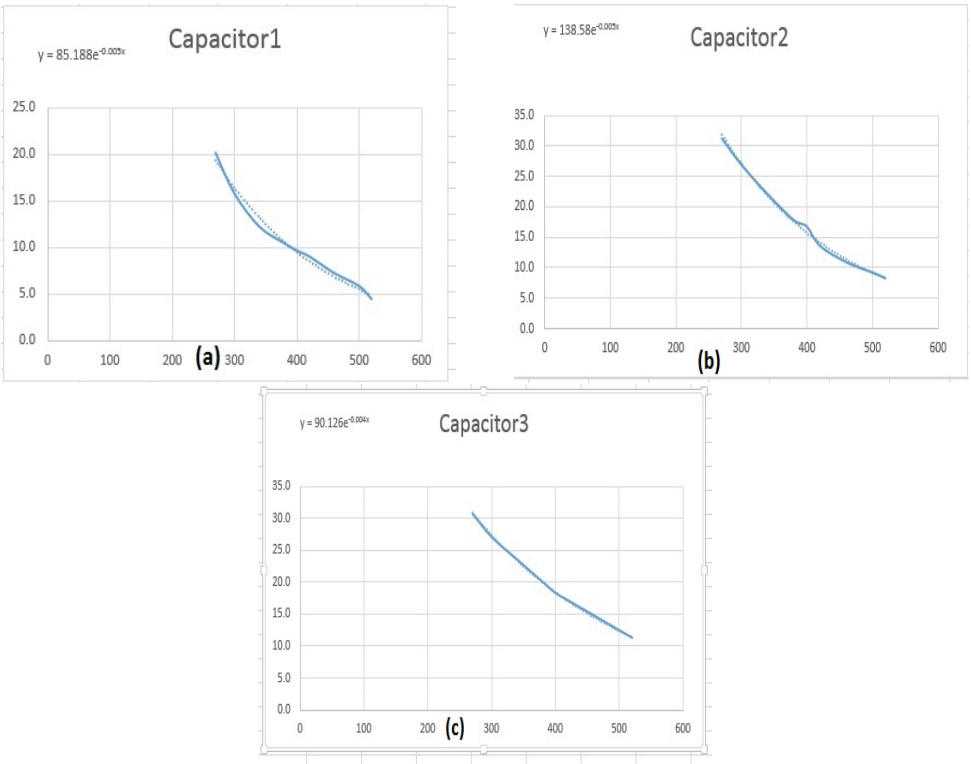


Figure 4.20: Tuned capacitor value plot Filter3

After plotting the values as shown above we get the frequency dependent equation by which these capacitance values varies with frequency. The equations which we get is given below:

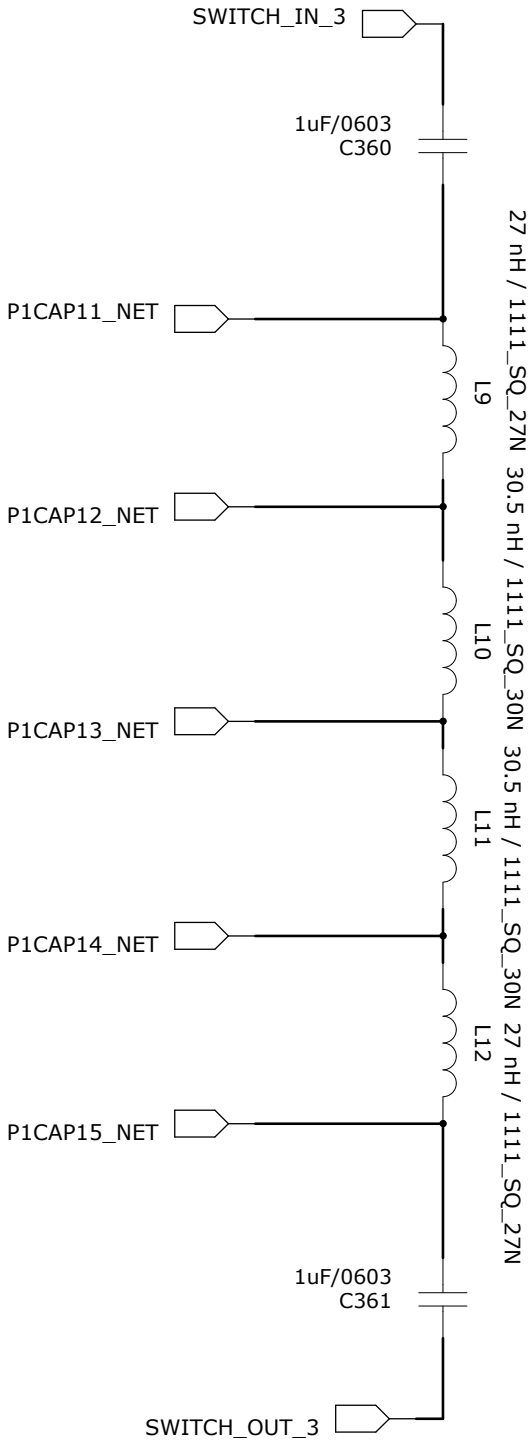
$$C_1 = 85.188e^{(-0.005f_c)} \tag{4.8}$$

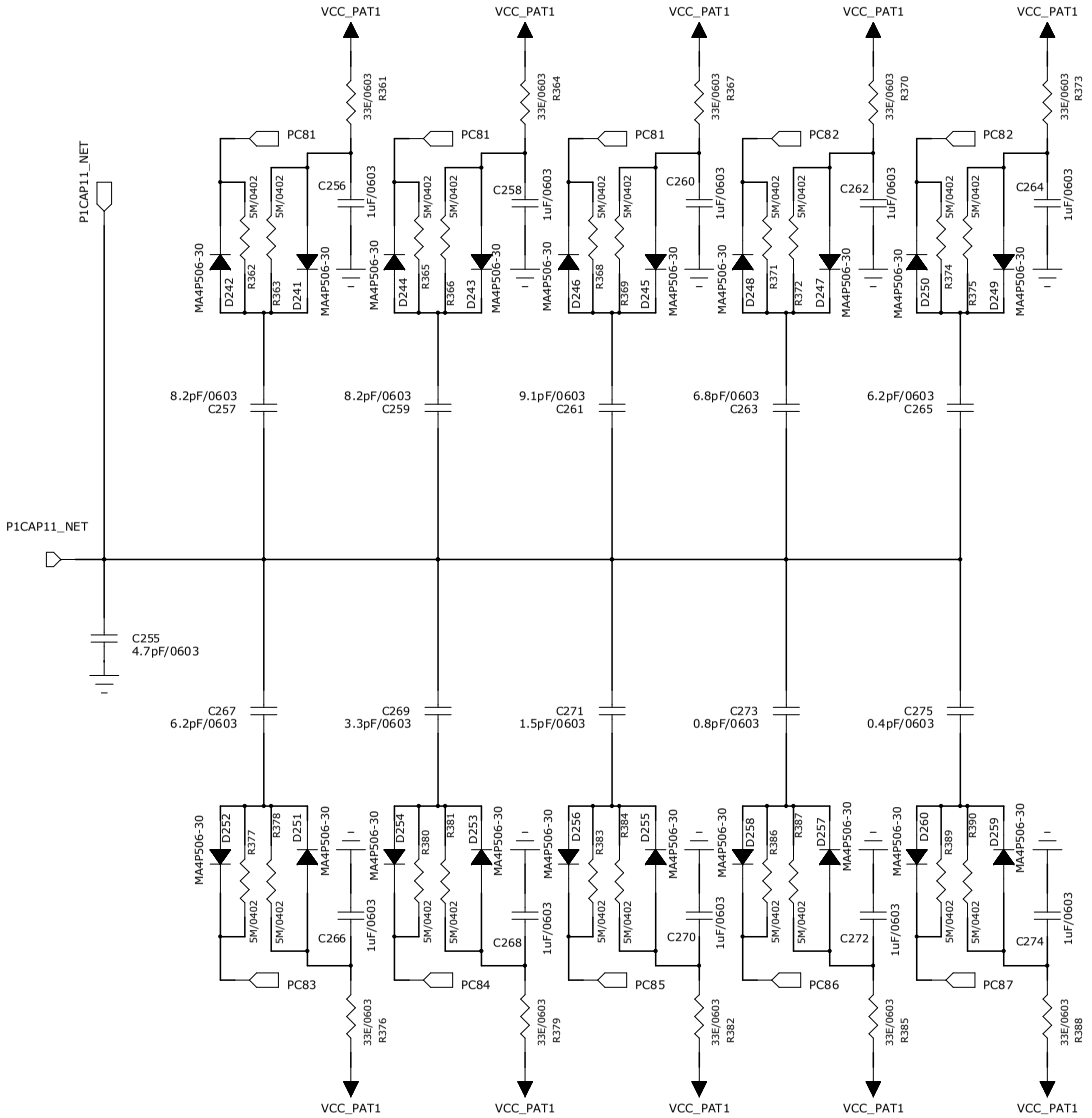
$$C_2 = 138.58e^{(-0.005f_c)} \tag{4.9}$$

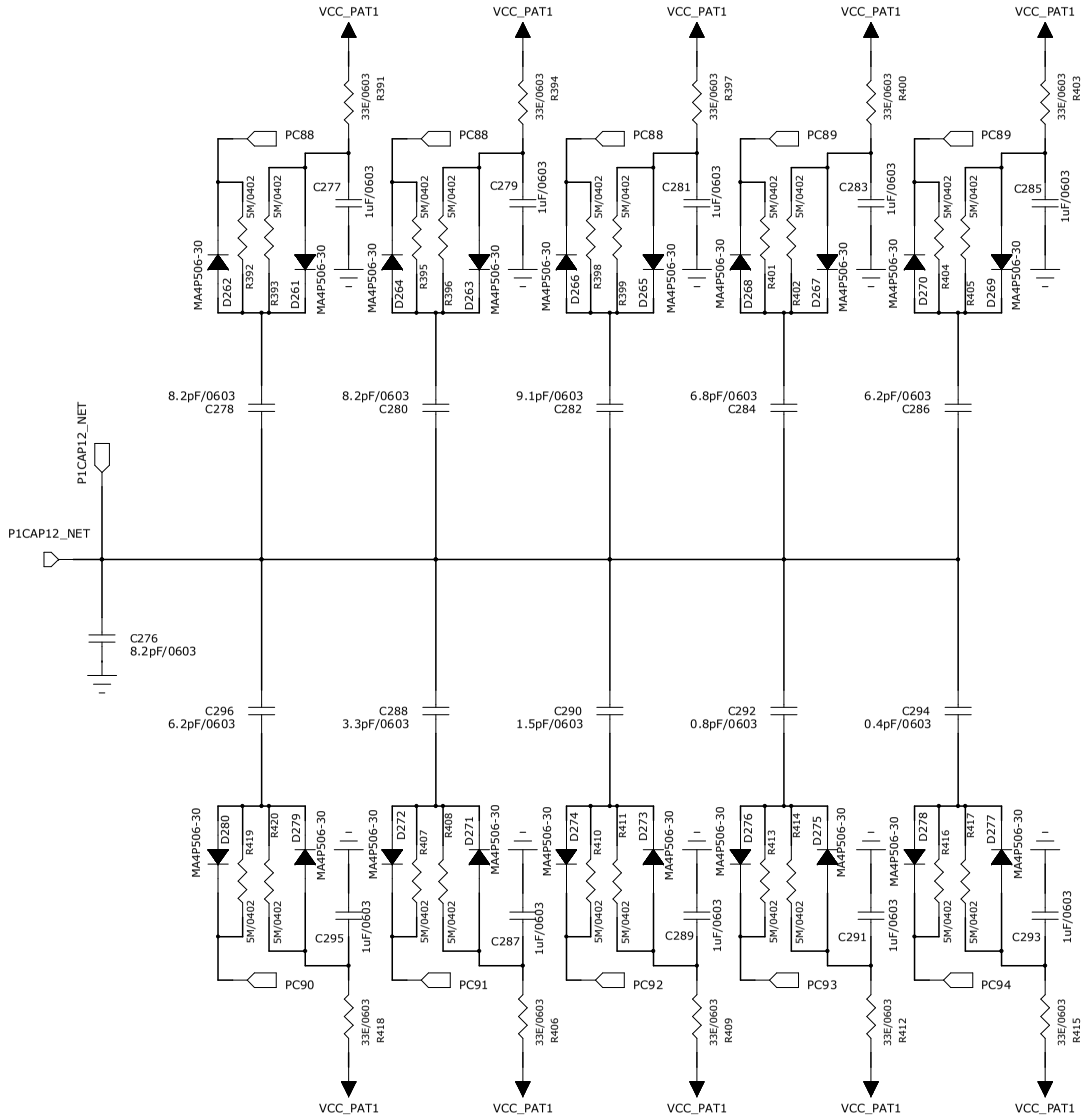
$$C_3 = 90.126e^{(-0.004f_c)} \tag{4.10}$$

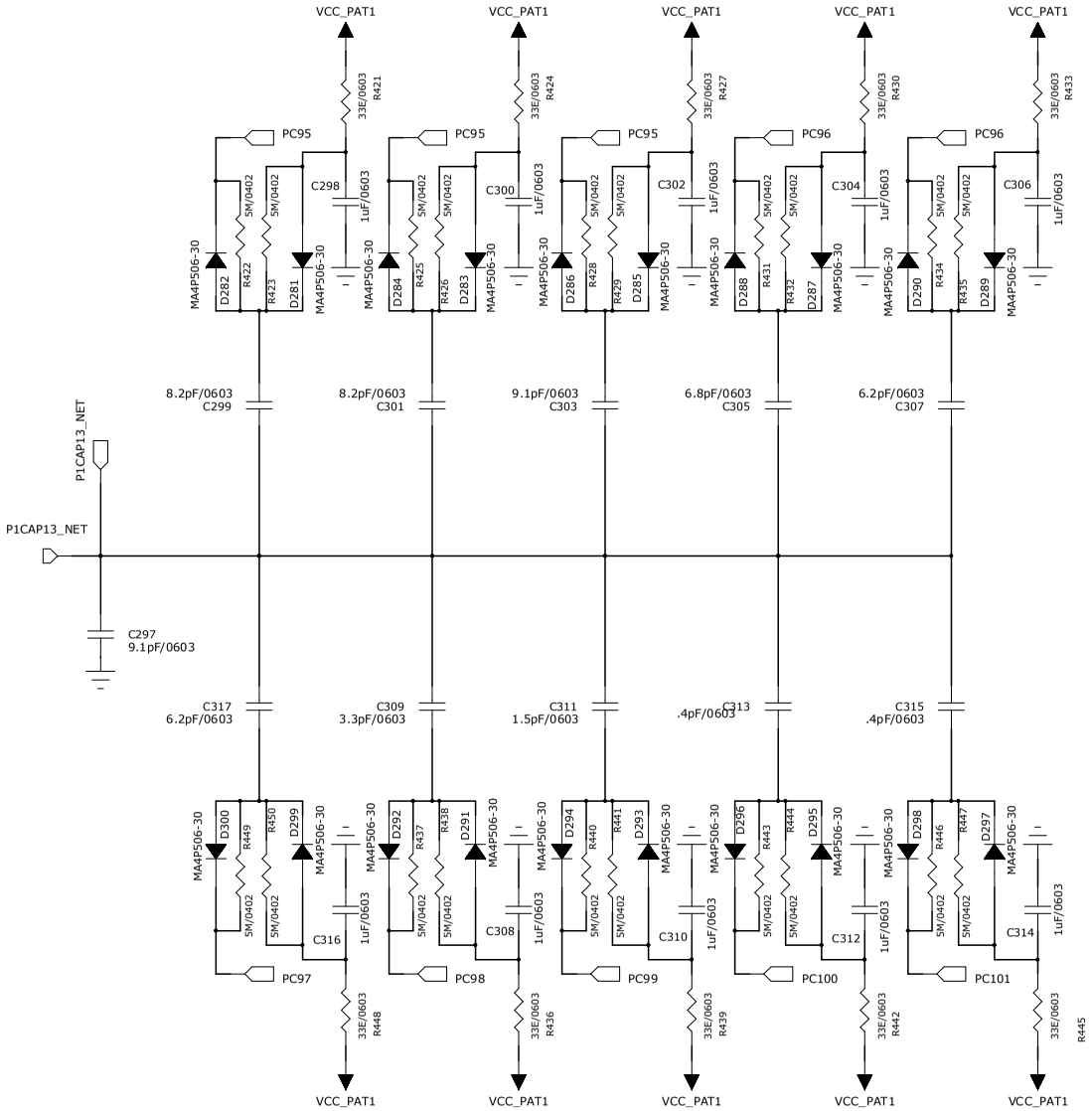
The schematic in PADS logic is given in Figure 4.21.

4.5.1 Schematic of RF section




VCC_PAT1
P1CAP11_NET
PC81
PC82
PC83
PC84
PC85
PC86
PC87
C255
4.7pF/0603
C256
C258
C260
C262
C264
C266
C268
C270
C272
C274
1uF/0603
C257
8.2pF/0603
C259
8.2pF/0603
C261
9.1pF/0603
C263
6.8pF/0603
C265
6.2pF/0603
C267
6.2pF/0603
C269
3.3pF/0603
C271
1.5pF/0603
C273
0.8pF/0603
C275
0.4pF/0603
R361
R364
R367
R370
R373
R376
R379
R382
R385
R388
33E/0603
5M/0402
MA4P506-30
D242
D241
D244
D243
D246
D245
D248
D247
D250
D249
D252
D251
D254
D253
D256
D255
D258
D257
D260
D259
R362
R363
R365
R366
R368
R369
R371
R372
R374
R375
R377
R378
R380
R381
R383
R384
R386
R387
R389
R390


VCC_PAT1
PC88
PC89
PC90
PC91
PC92
PC93
PC94
P1CAP12_NET
C276
8.2pF/0603
C278
8.2pF/0603
C280
9.1pF/0603
C282
6.8pF/0603
C284
6.2pF/0603
C286
C277
C279
C281
C283
C285
C287
C289
C291
C293
C288
3.3pF/0603
C290
1.5pF/0603
C292
0.8pF/0603
C294
0.4pF/0603
C295
C296
6.2pF/0603
1uF/0603
33E/0603
5M/0402
MA4P506-30


VCC_PAT1
PC95
PC96
PC97
PC98
PC99
PC100
PC101
P1CAP13_NET
C297
9.1pF/0603
C298
C300
C302
C304
C306
C308
C310
C312
C314
C316
1uF/0603
C299
8.2pF/0603
C301
8.2pF/0603
C303
9.1pF/0603
C305
6.8pF/0603
C307
6.2pF/0603
C309
3.3pF/0603
C311
1.5pF/0603
C313
.4pF/0603
C315
.4pF/0603
C317
6.2pF/0603
R421
R424
R427
R430
R433
R436
R439
R442
R445
R448
33E/0603
R422
R423
R425
R426
R428
R429
R431
R432
R434
R435
R437
R438
R440
R441
R443
R444
R446
R447
R449
R450
5M/0402
D281
D282
D283
D284
D285
D286
D287
D288
D289
D290
D291
D292
D293
D294
D295
D296
D297
D298
D299
D300
MA4P506-30

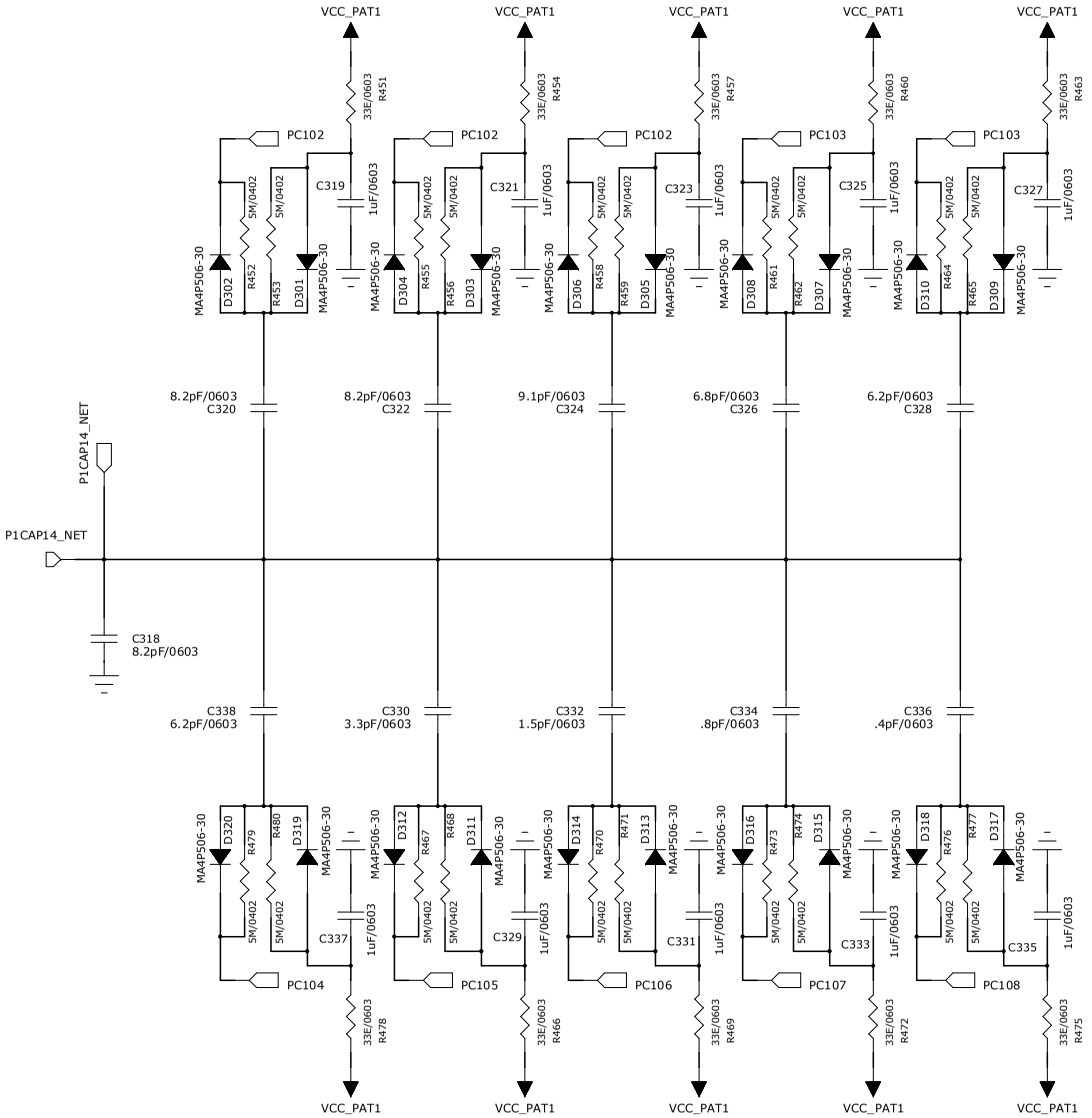
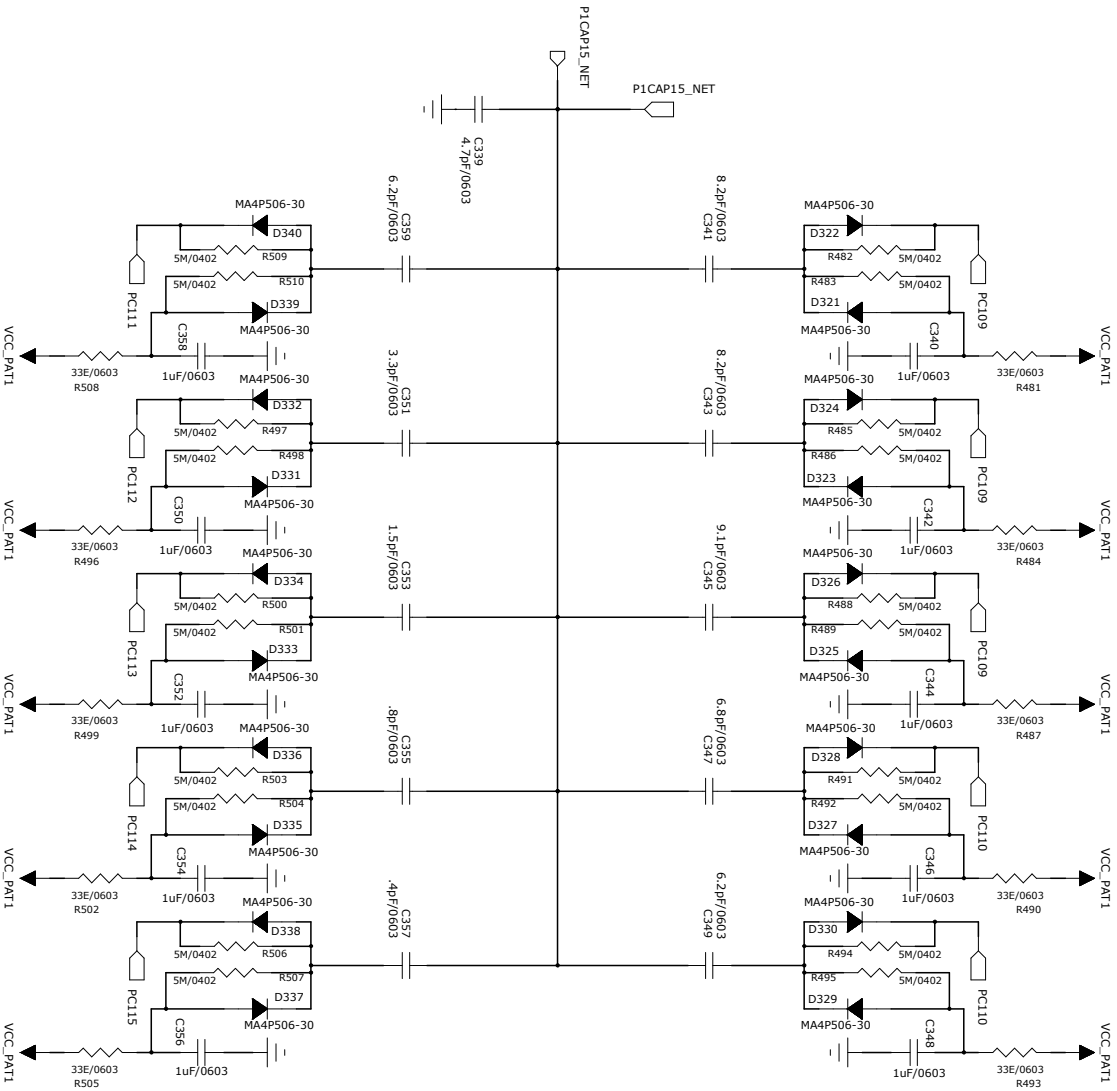

VCC_PAT1
PC102
PC103
PC104
PC105
PC106
PC107
PC108
P1CAP14_NET
C318
8.2pF/0603
MA4P506-30
5M/0402
1uF/0603
33E/0603
8.2pF/0603 C320
8.2pF/0603 C322
9.1pF/0603 C324
6.8pF/0603 C326
6.2pF/0603 C328
C338 6.2pF/0603
C330 3.3pF/0603
C332 1.5pF/0603
C334 .8pF/0603
C336 .4pF/0603

Figure 4.21: PADS schematic for Filter 3



4.5.2 ADS simulation (270-520 MHz)

Simulation schematic diagram in Agilent ADS is given in Figure 4.17 .

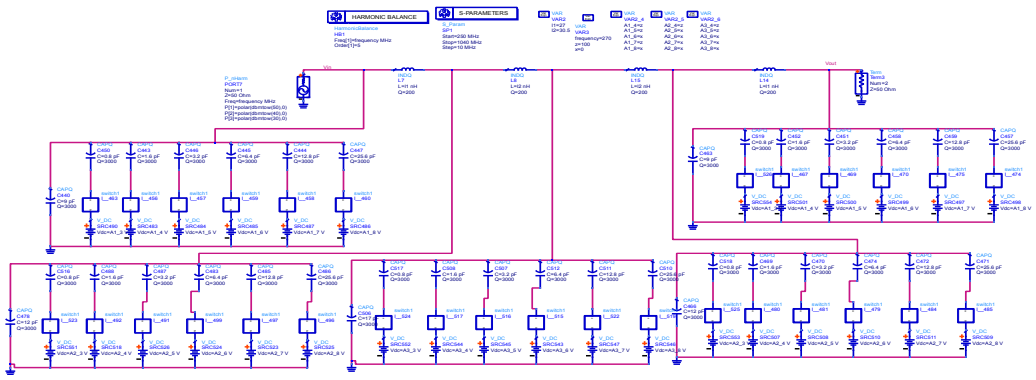


Figure 4.22: ADS schematic (270-520 MHz)

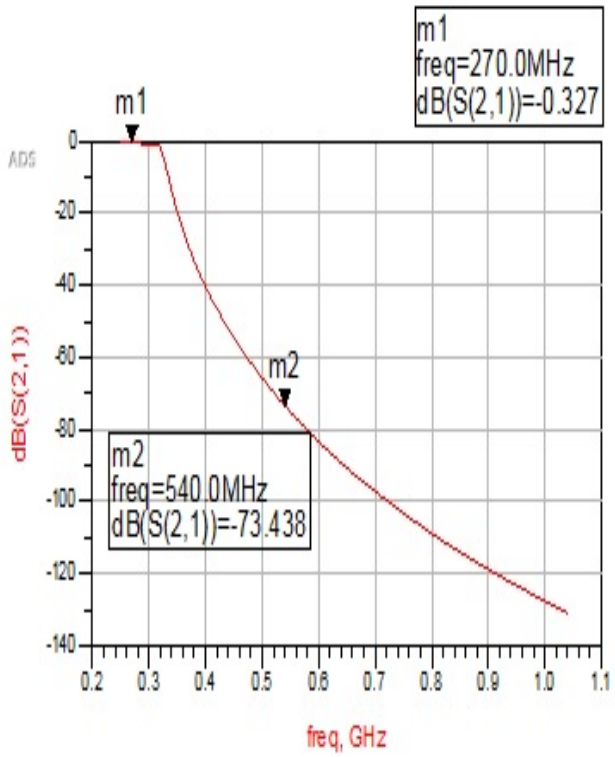
4.5.3 Simulation Response

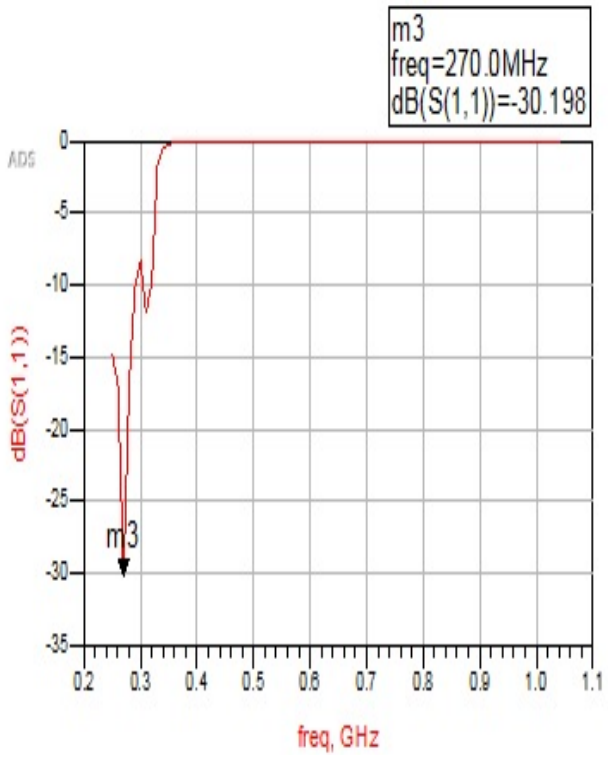
As we have done in section 4.3.2. Both the S-parameter and Harmonic balance simulation is done by manually tuning the capacitors in ADS.

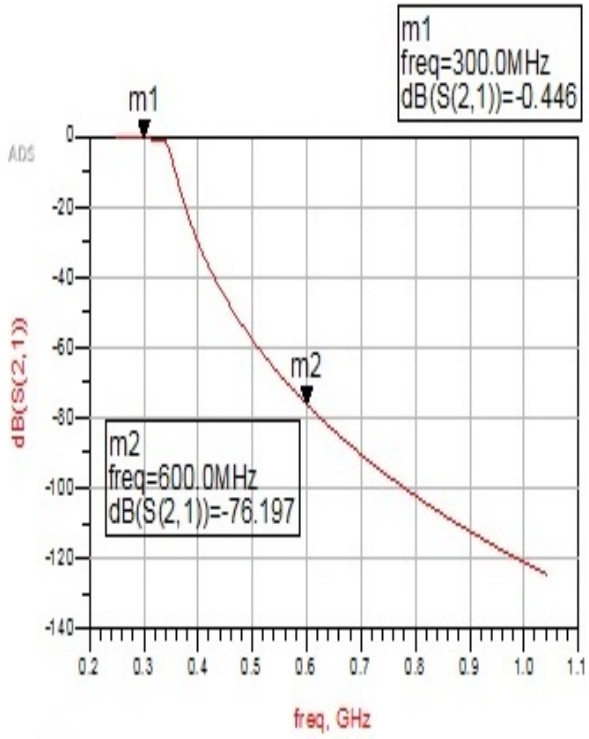
In S-parameter simulation we have find the S(2,1) and S(1,1) as it gives the insertion loss and return loss.

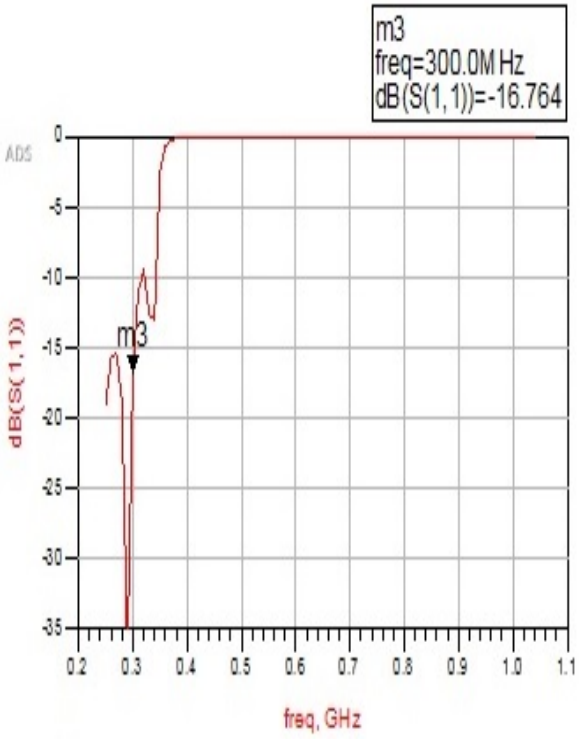
In Harmonic balance simulation we have given the a harmonic signal input and compared the output. First figure in harmonic simulation is time domain input output signals and the second one is input output signal in dBm.

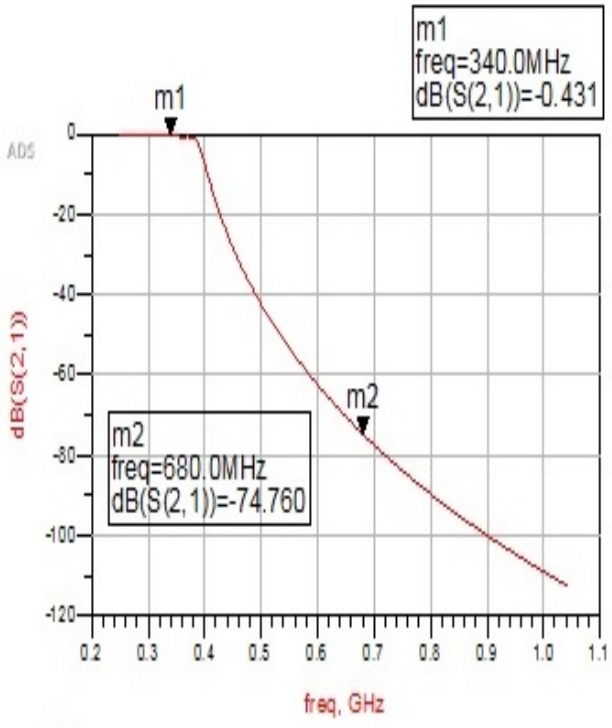
S-Parameter Simulation Response(270-520 MHz)

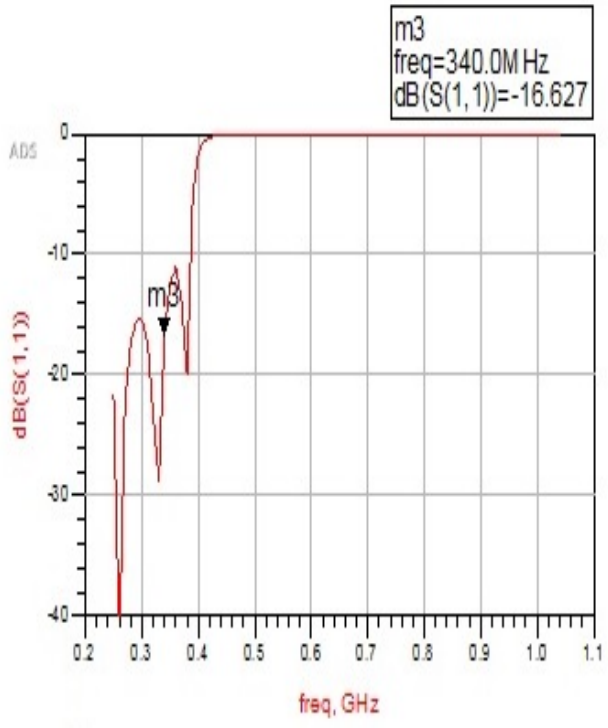


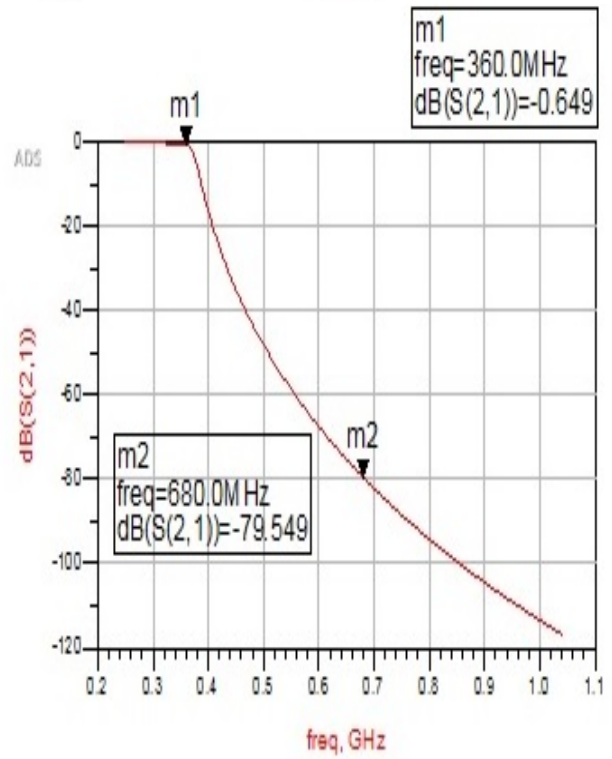


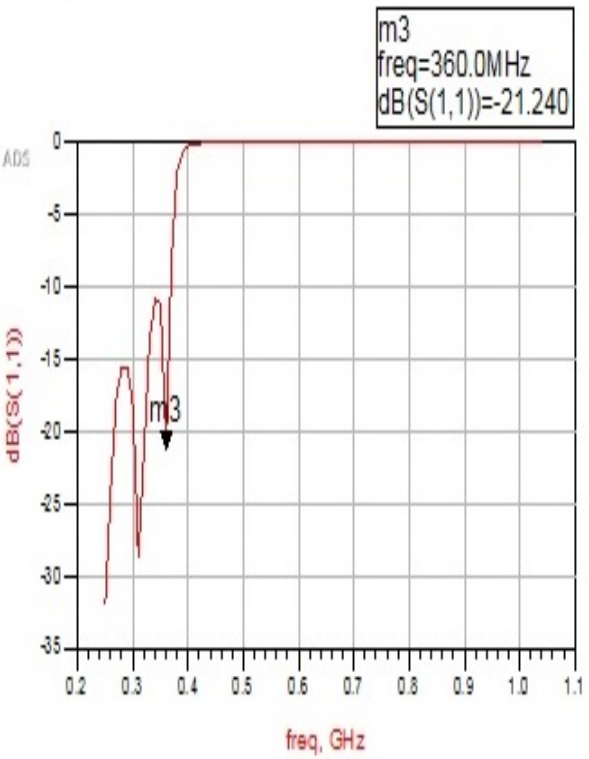


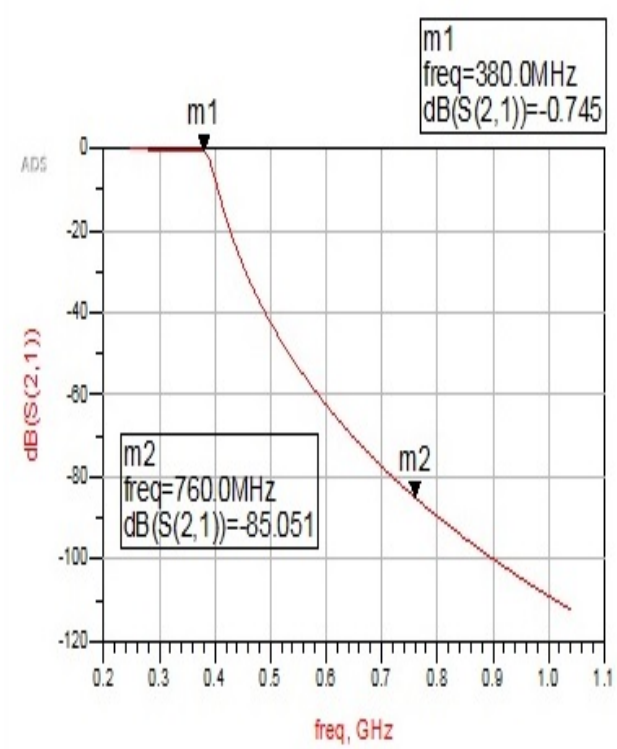


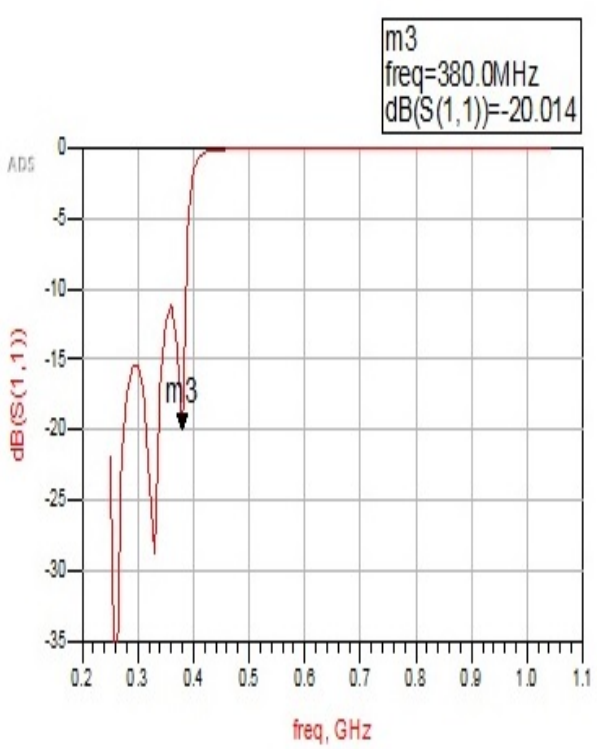

m1
freq=340.0MHz
dB(S(2,1))=-0.431
m2
freq=680.0MHz
dB(S(2,1))=-74.760
dB(S(2,1))
freq, GHz

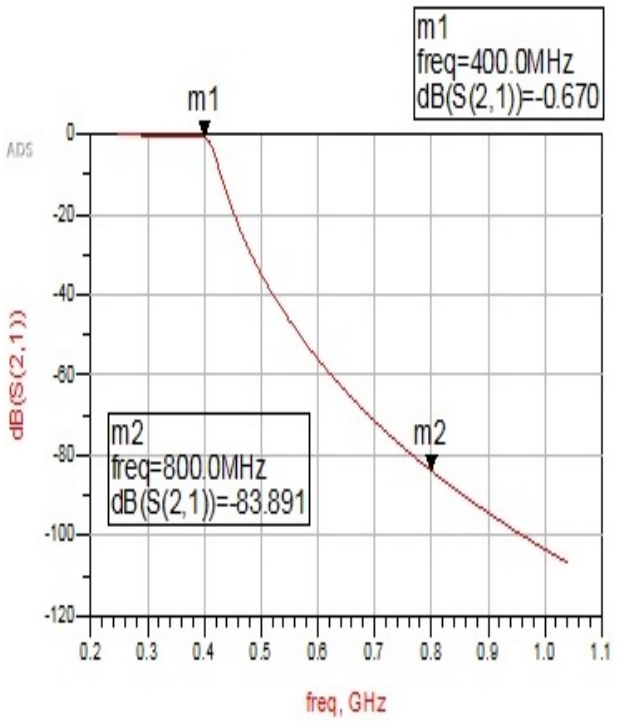

m3
freq=340.0MHz
dB(S(1,1))=-16.627
dB(S(1,1))
freq, GHz

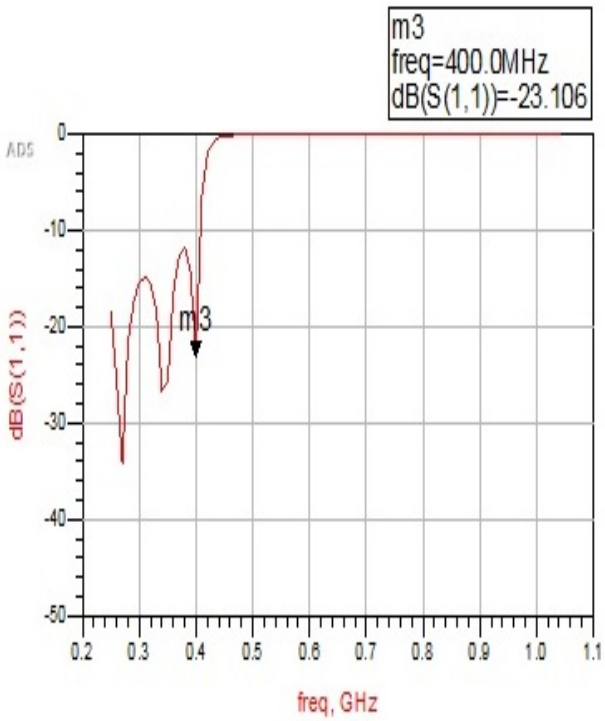

m1
freq=360.0MHz
dB(S(2,1))=-0.649
m2
freq=680.0MHz
dB(S(2,1))=-79.549
dB(S(2,1))
freq, GHz

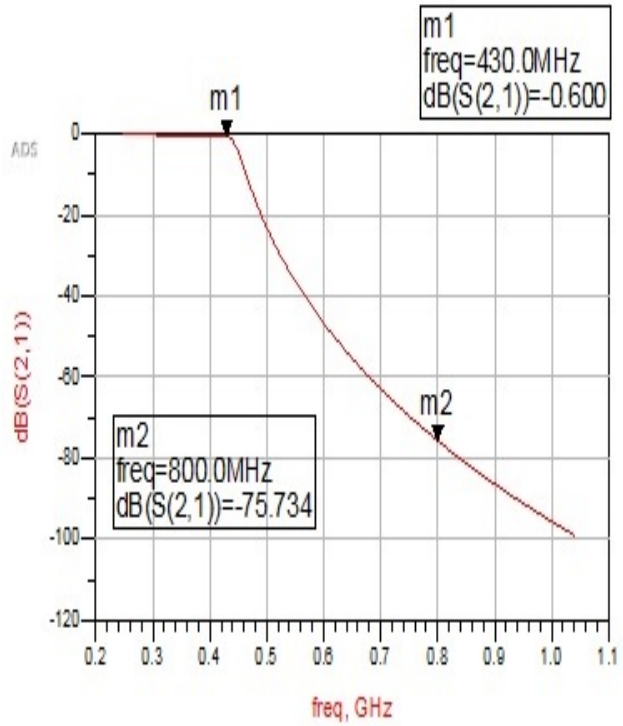

m3
freq=360.0MHz
dB(S(1,1))=-21.240
dB(S(1,1))
freq, GHz

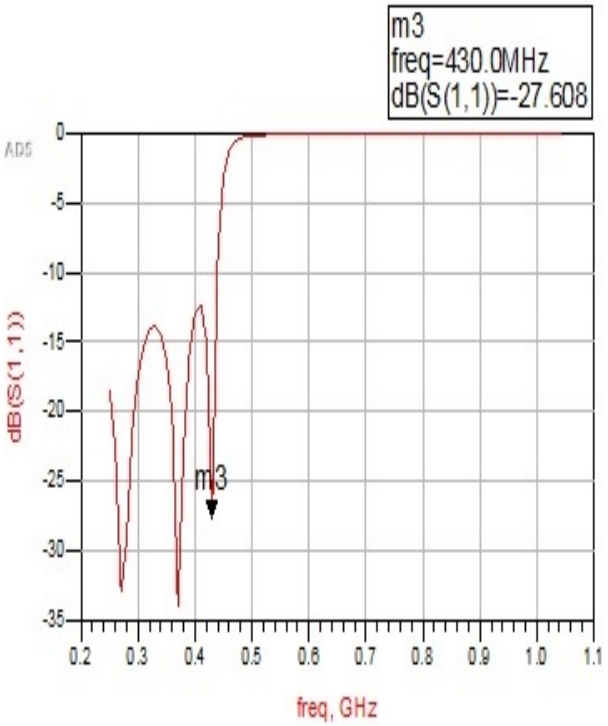

m1
freq=380.0MHz
dB(S(2,1))=-0.745
m1
m2
freq=760.0MHz
dB(S(2,1))=-85.051
m2
dB(S(2,1))
freq, GHz

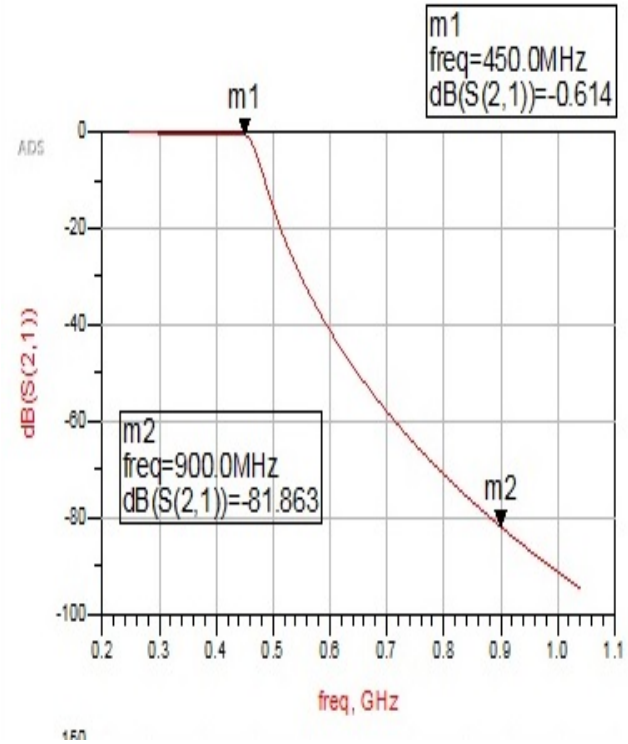

m3
freq=380.0MHz
dB(S(1,1))=-20.014
m3
dB(S(1,1))
freq, GHz

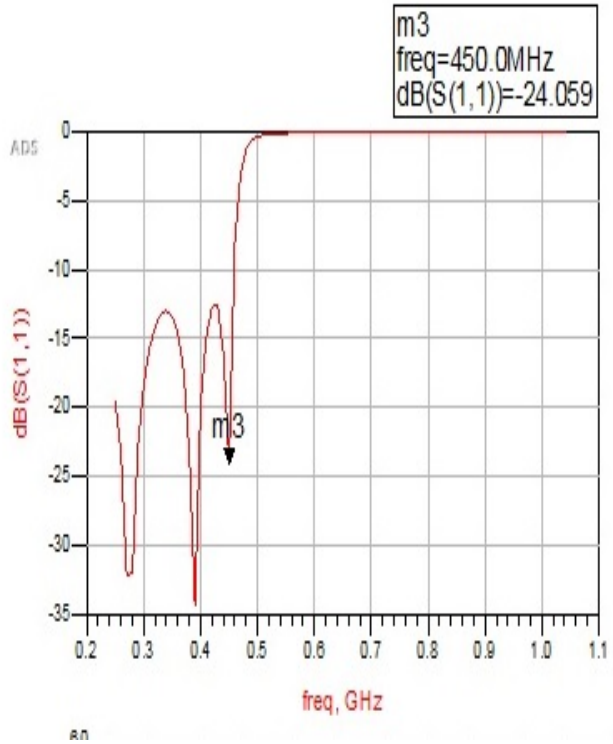

m1
freq=400.0MHz
dB(S(2,1))=-0.670
m1
m2
freq=800.0MHz
dB(S(2,1))=-83.891
m2
dB(S(2,1))
freq, GHz

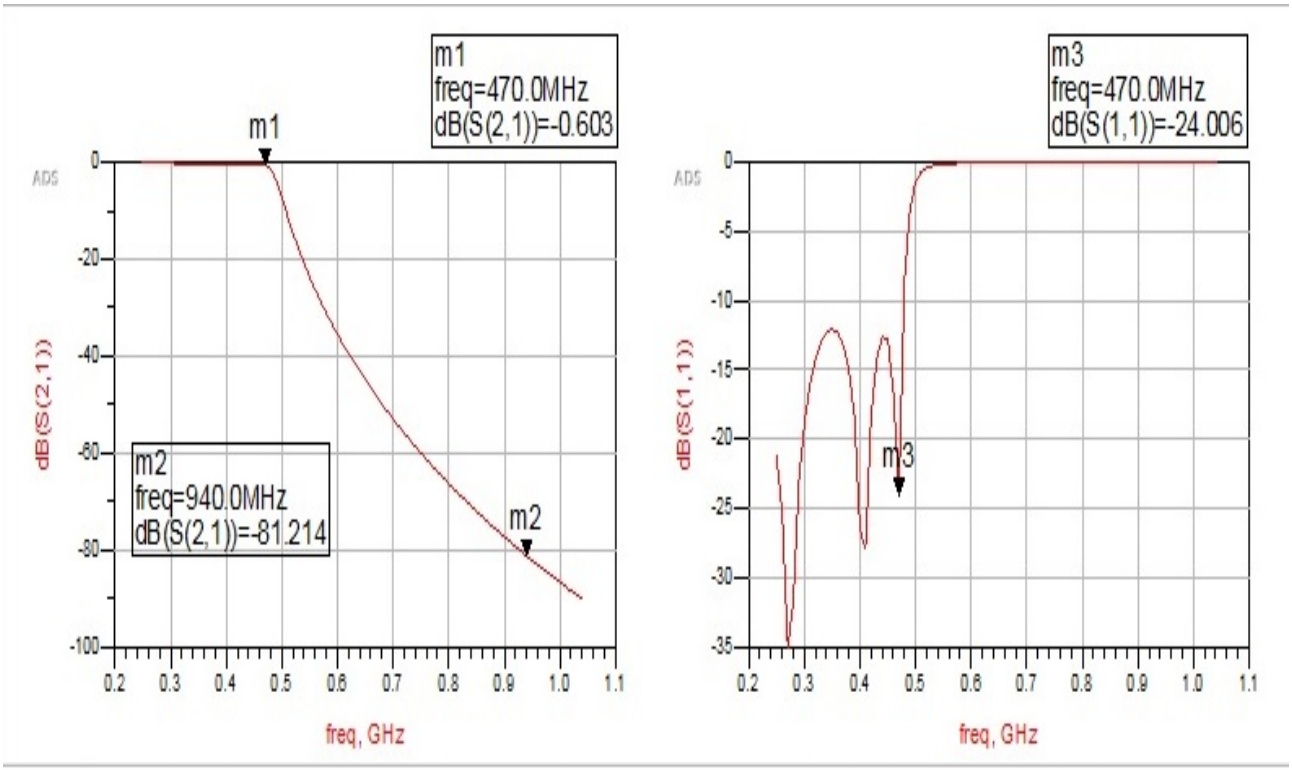

m3
freq=400.0MHz
dB(S(1,1))=-23.106
m3
dB(S(1,1))
freq, GHz

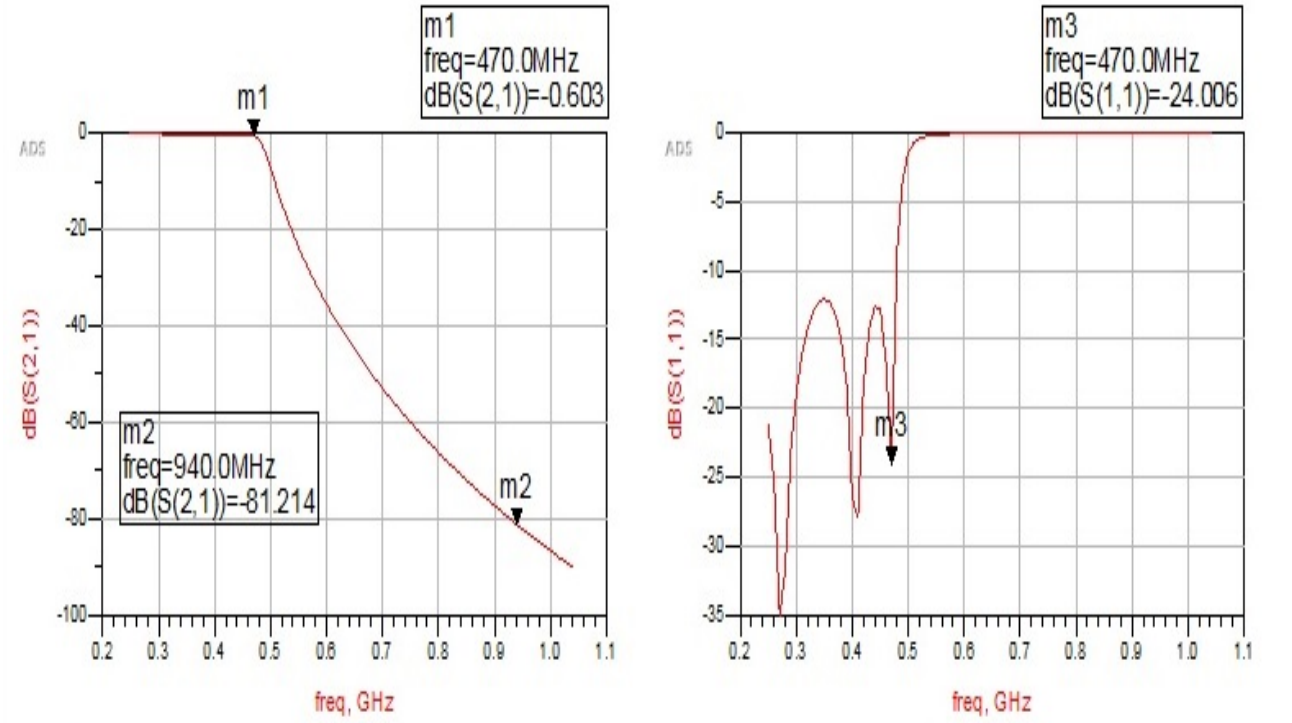

m1
freq=430.0MHz
dB(S(2,1))=-0.600
m2
freq=800.0MHz
dB(S(2,1))=-75.734
dB(S(2,1))
freq, GHz


m3
freq=430.0MHz
dB(S(1,1))=-27.608
dB(S(1,1))
freq, GHz


m1
freq=450.0MHz
dB(S(2,1))=-0.614
m2
freq=900.0MHz
dB(S(2,1))=-81.863
dB(S(2,1))
freq, GHz


m3
freq=450.0MHz
dB(S(1,1))=-24.059
dB(S(1,1))
freq, GHz


m1
freq=470.0MHz
dB(S(2,1))=-0.603
m1
m2
freq=940.0MHz
dB(S(2,1))=-81.214
m2
dB(S(2,1))
freq, GHz
m3
freq=470.0MHz
dB(S(1,1))=-24.006
m3
dB(S(1,1))
freq, GHz


m1
freq=470.0MHz
dB(S(2,1))=-0.603
m1
m2
freq=940.0MHz
dB(S(2,1))=-81.214
m2
dB(S(2,1))
freq, GHz
m3
freq=470.0MHz
dB(S(1,1))=-24.006
m3
dB(S(1,1))
freq, GHz

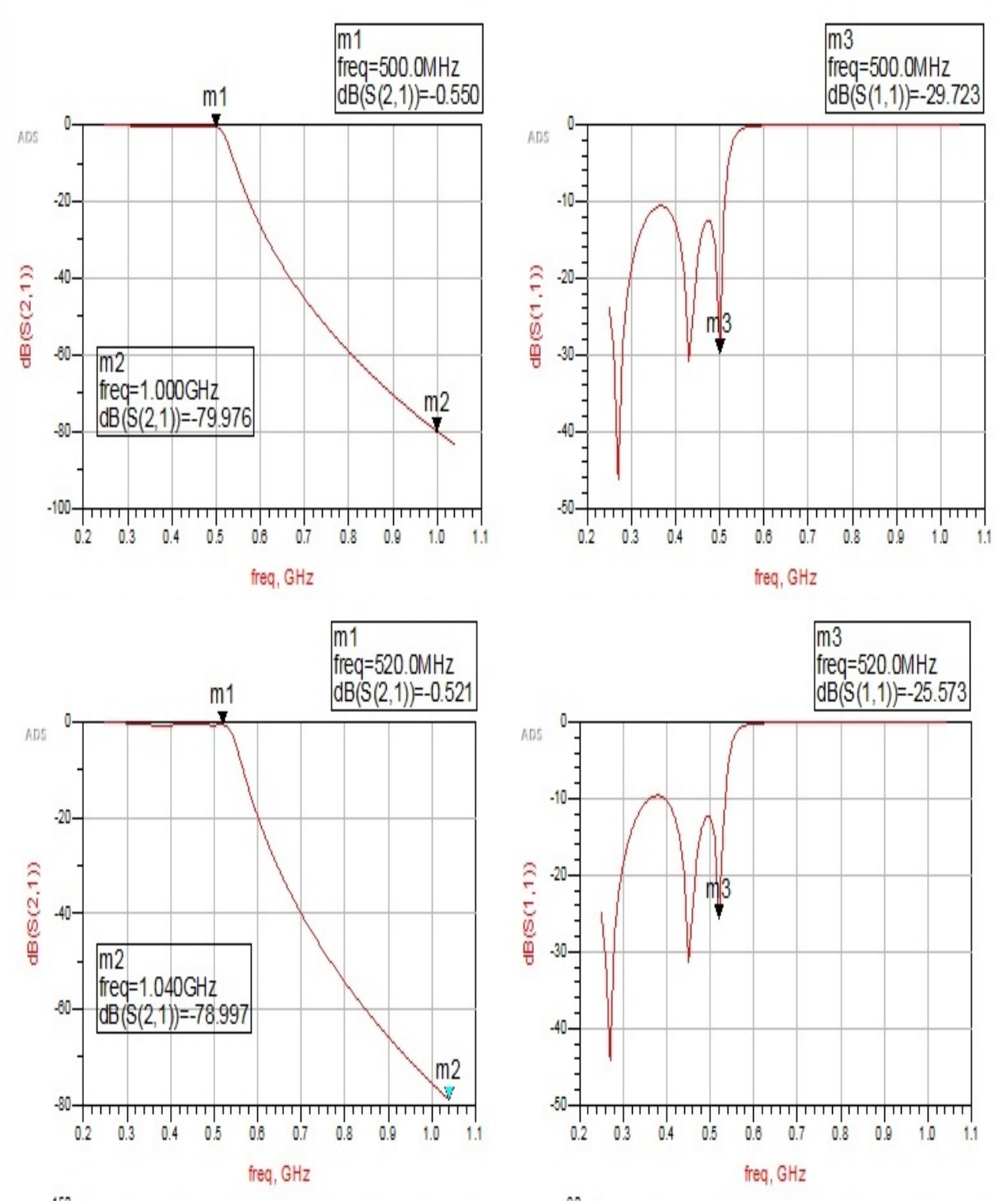
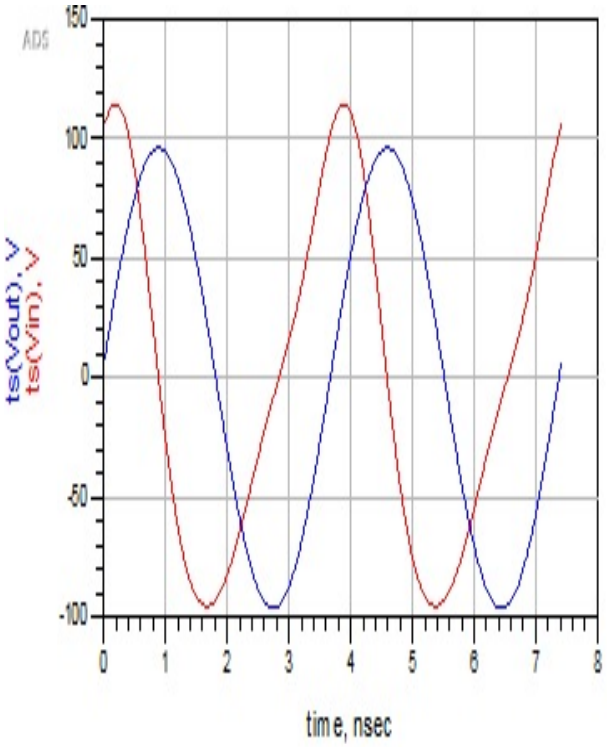
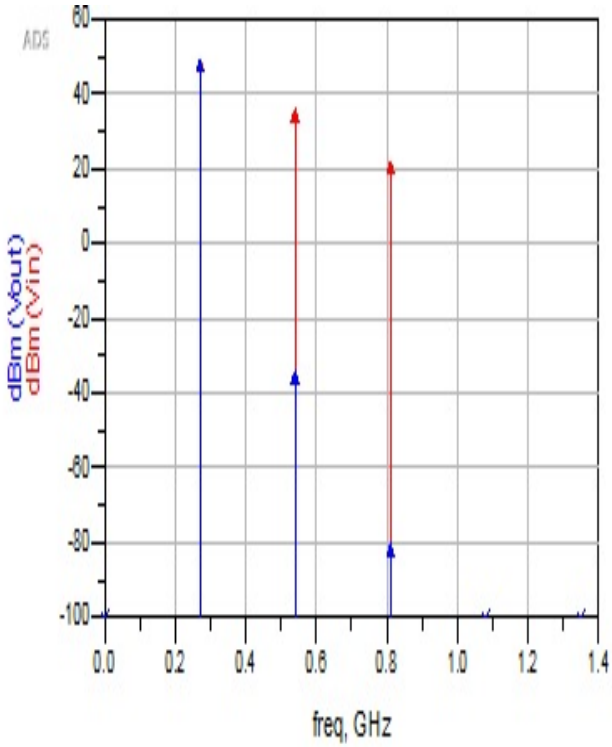
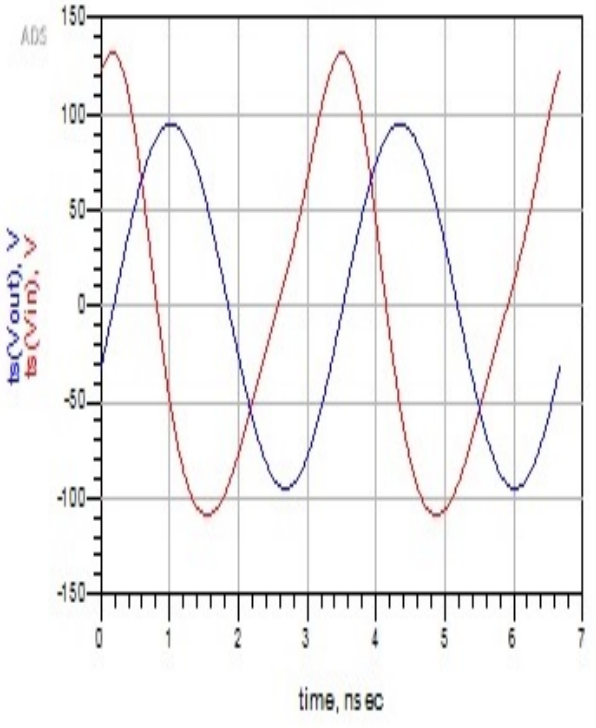


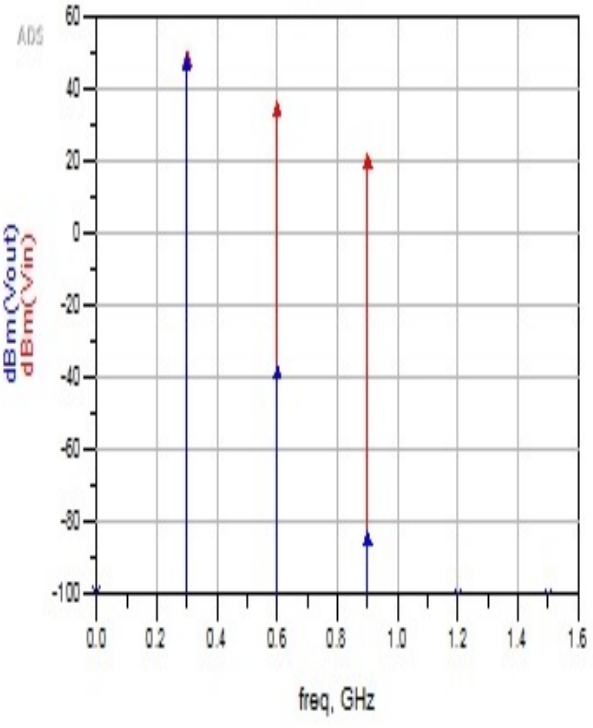
Figure 4.23: S Parameter simulation Response filter bank 3

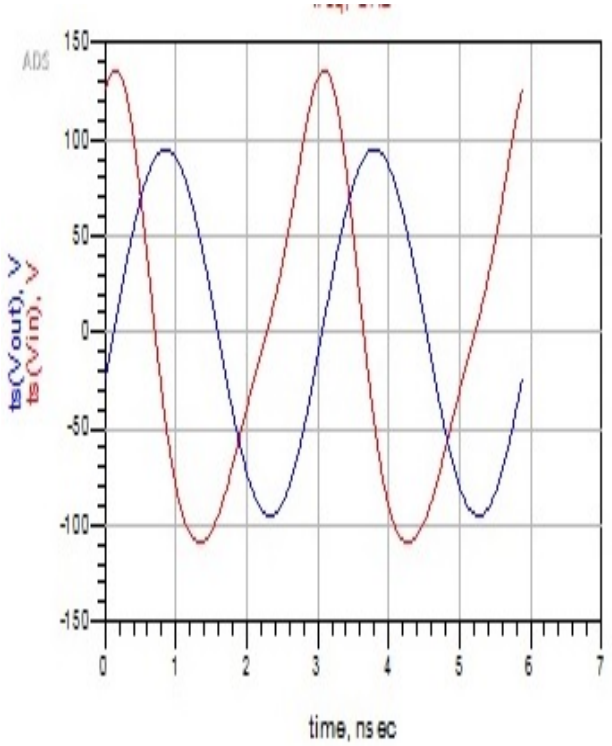
Harmonic Balance Simulation Response (270-520 MHz)

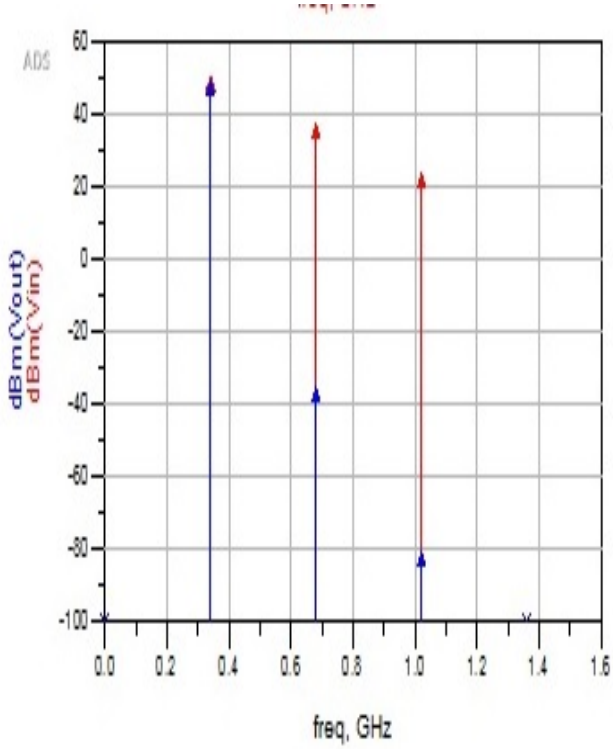


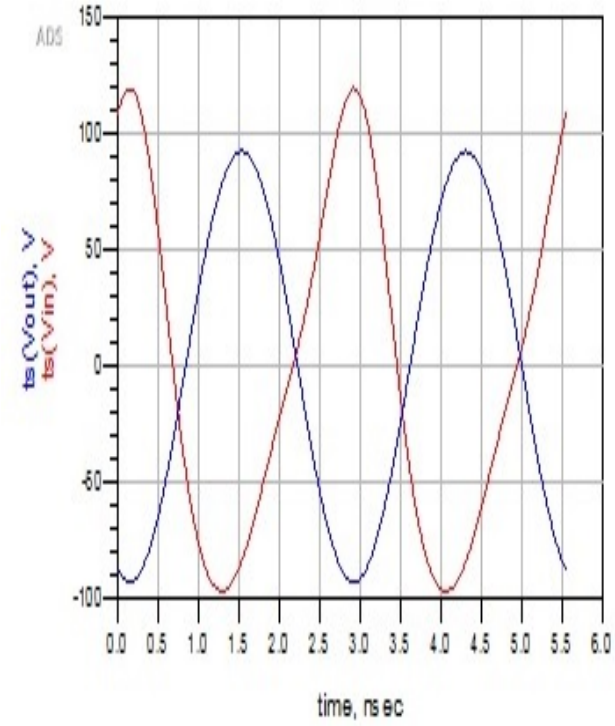


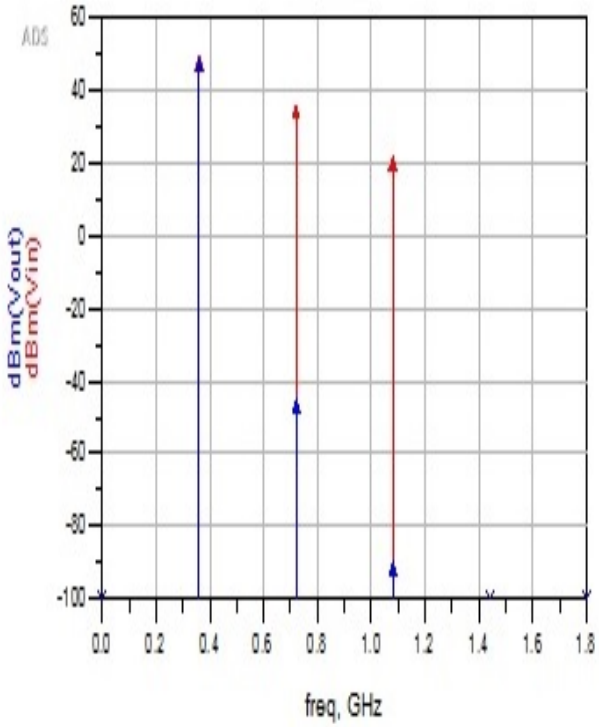


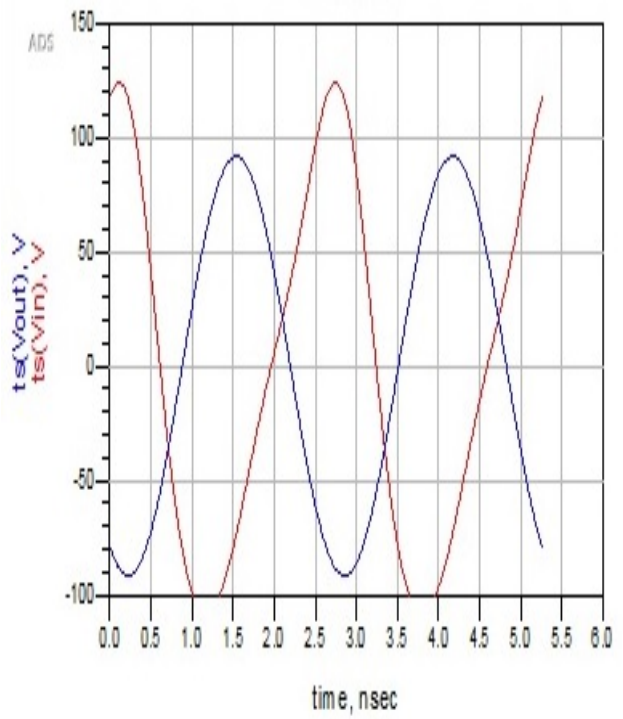


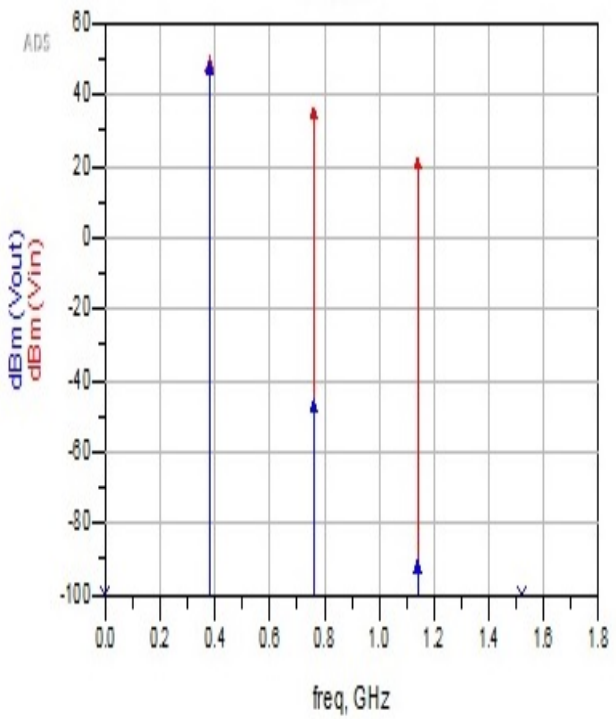

ADS
ts(Vout), V
ts(Vin), V
time, nsec

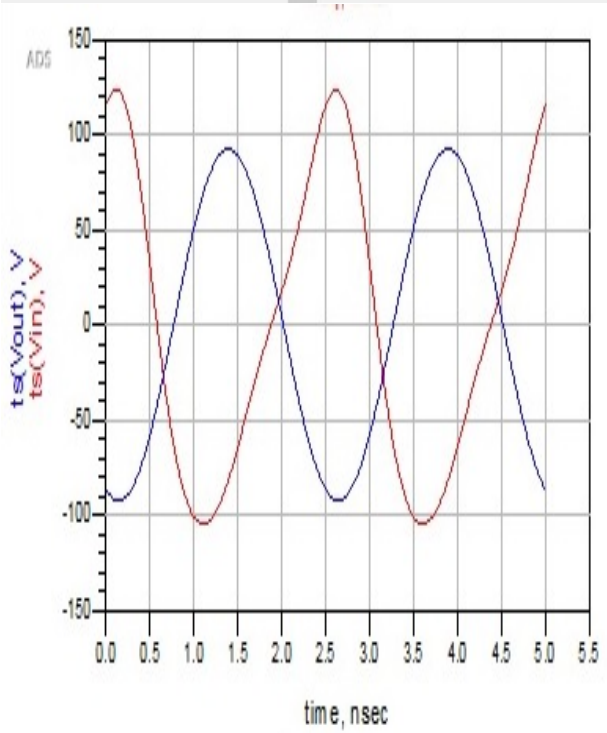

ADS
dBm(Vout)
dBm(Vin)
freq, GHz

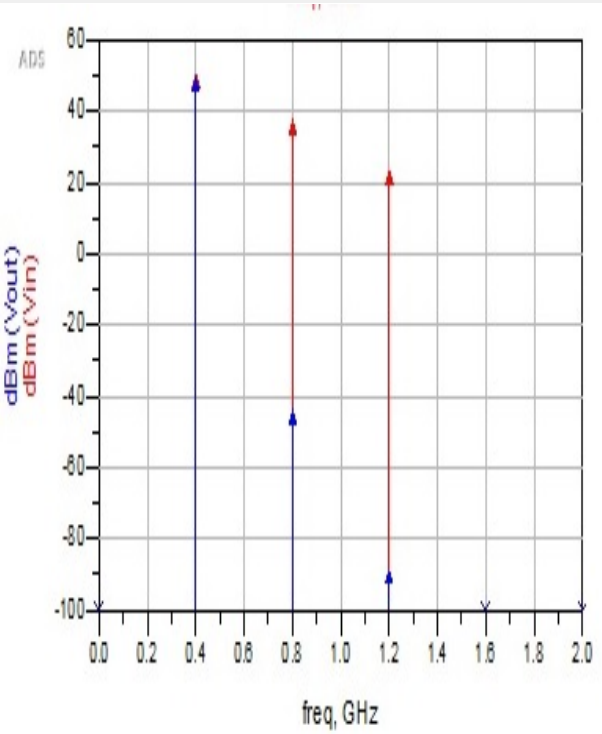

ADS
ts(Vout), V
ts(Vin), V
time, nsec

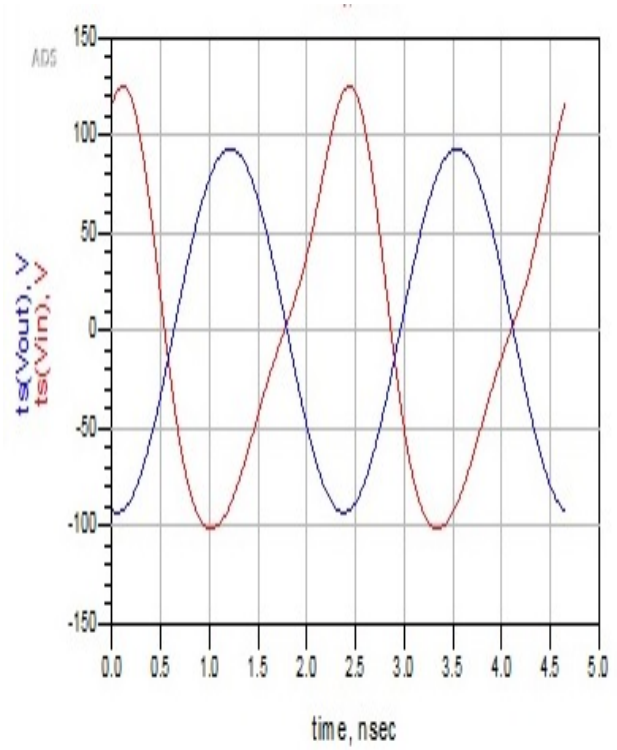

ADS
dBm(Vout)
dBm(Vin)
freq, GHz

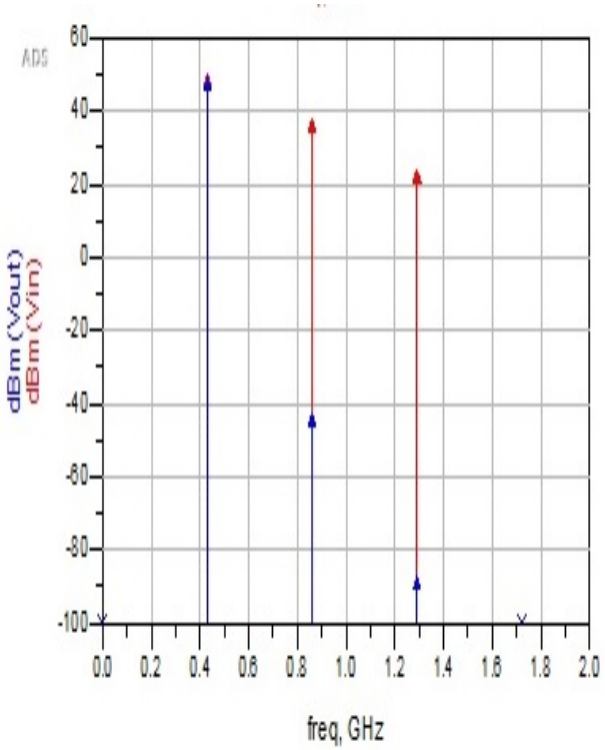

ADS
ts(Vout), V
ts(Vin), V
time, nsec

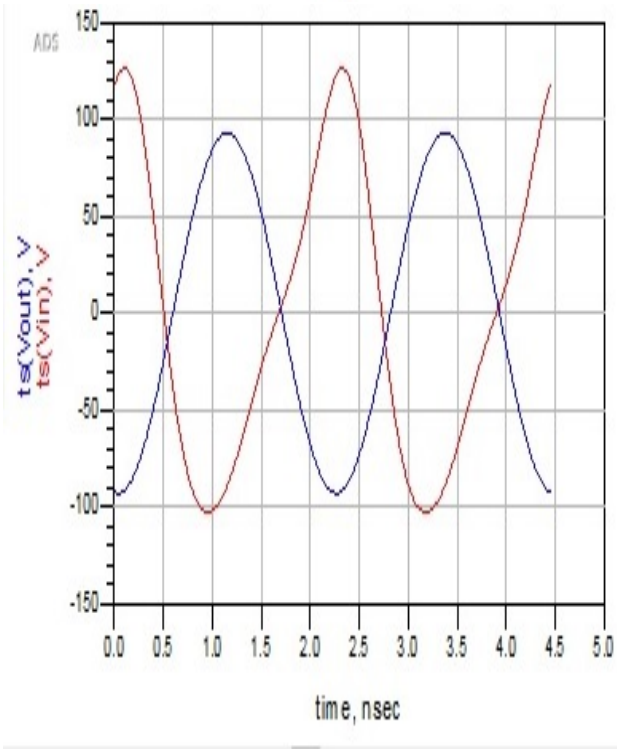

ADS
dBm(Vout)
dBm(Vin)
freq, GHz

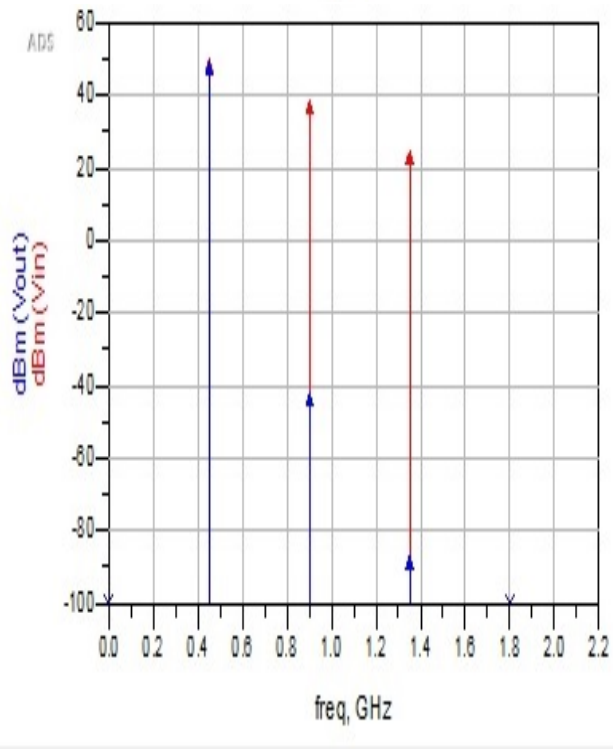

ADS
ts(Vout), V
ts(Vin), V
time, nsec

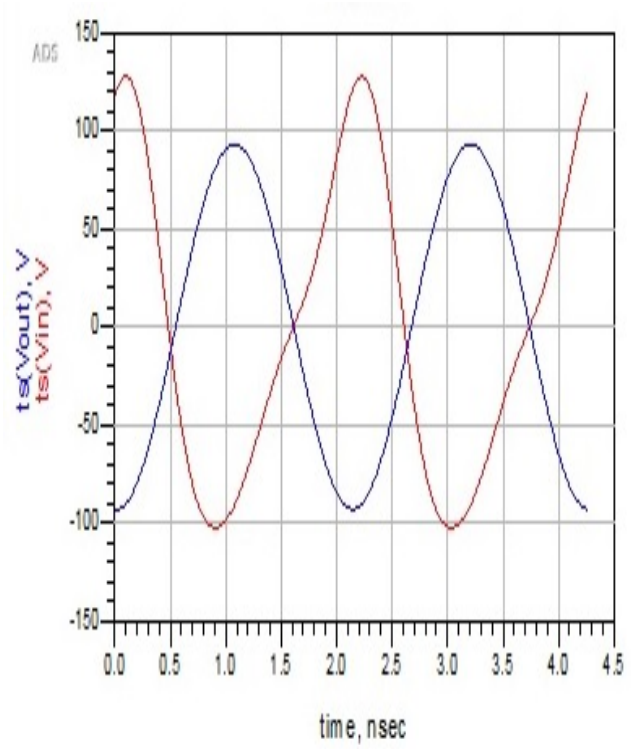

ADS
dBm(Vout)
dBm(Vin)
freq, GHz

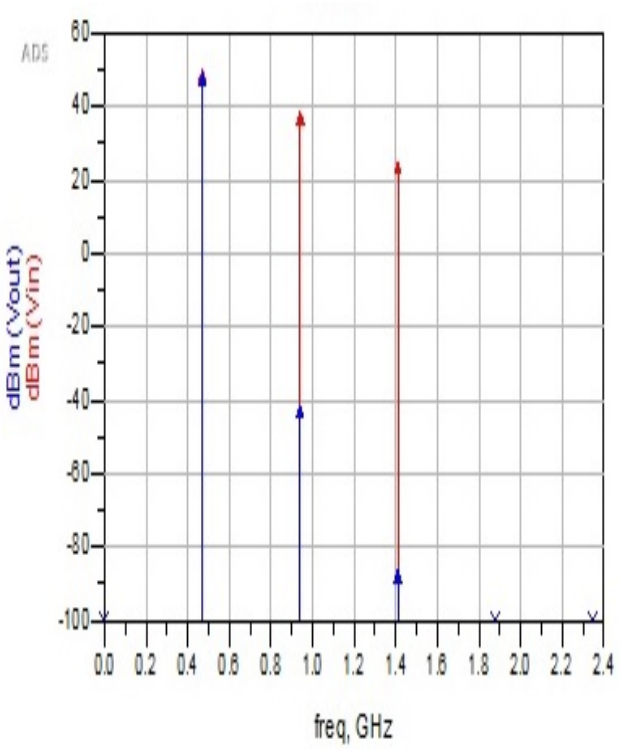

ADS
ts(Vout), V
ts(Vin), V
time, nsec

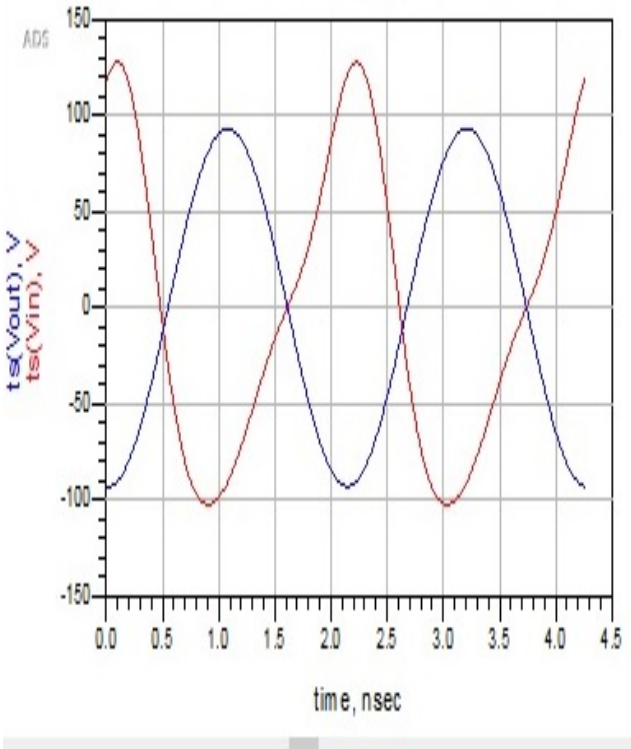

ADS
dBm(Vout)
dBm(Vin)
freq, GHz

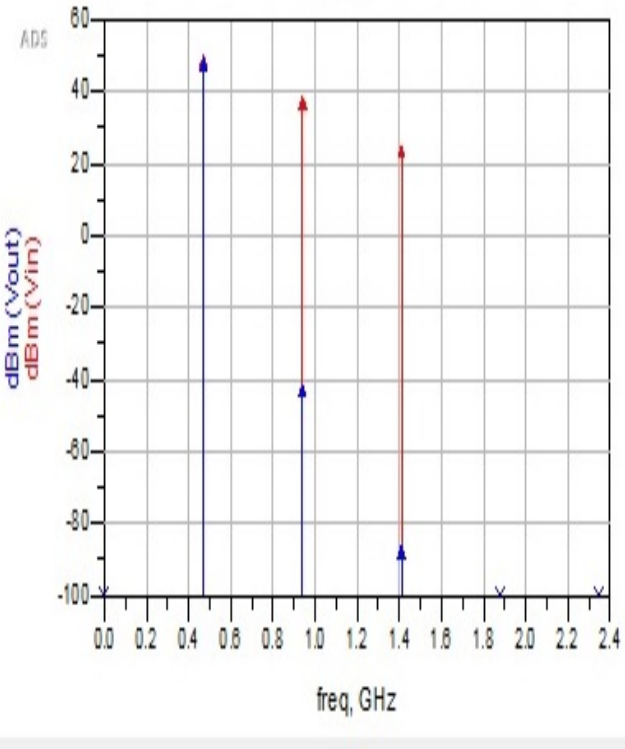

ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm(Vout)
dBm(Vin)
freq, GHz


ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm(Vout)
dBm(Vin)
freq, GHz


ADS
ts(Vout), V
ts(Vin), V
time, nsec


ADS
dBm(Vout)
dBm(Vin)
freq, GHz

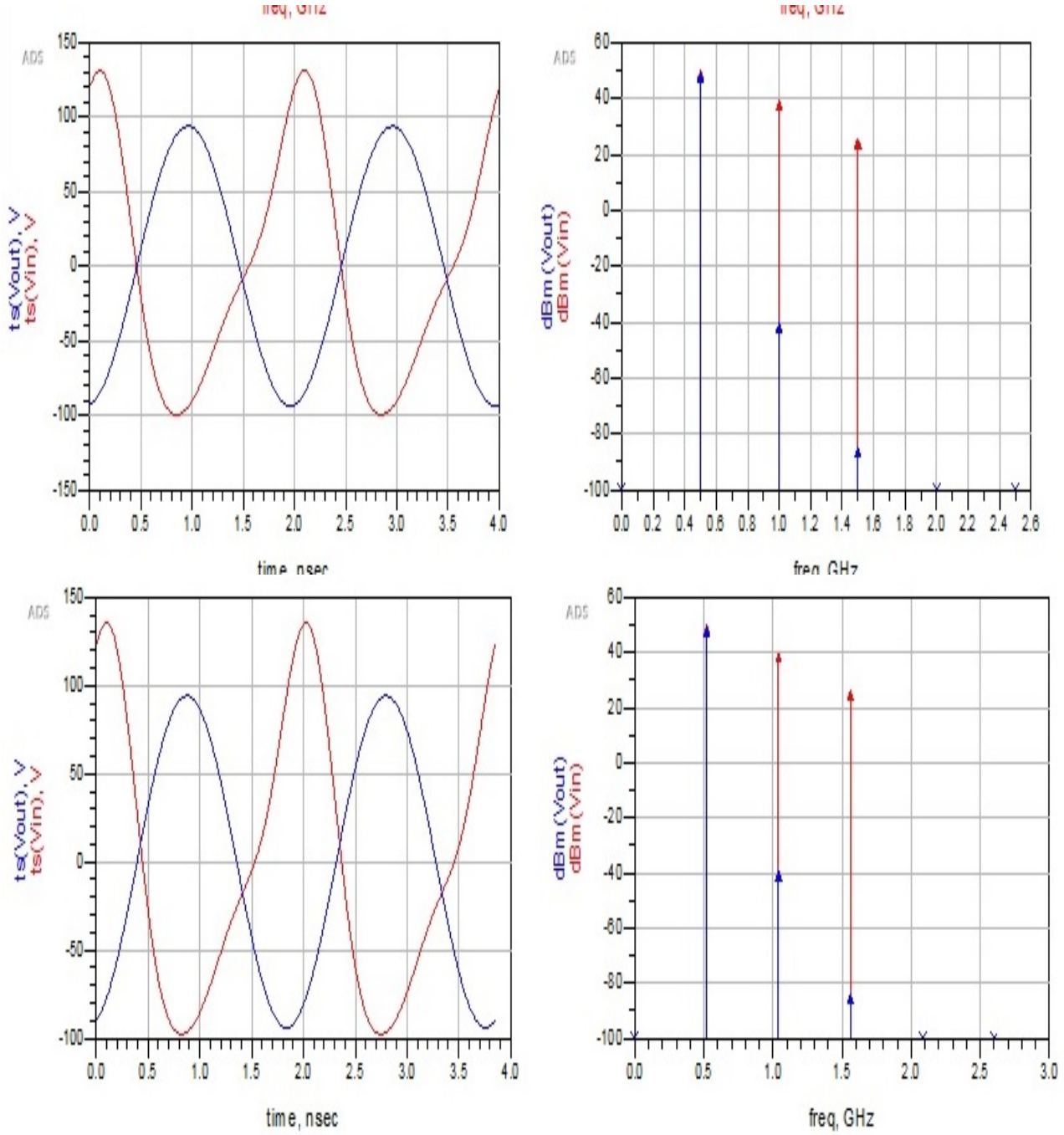


Figure 4.24: Harmonic Balance simulation Response filter bank 3

4.6 SP3T Switch

For switching the filter banks SP3T switches are used both at the input and output. Here in this project MACOM MASW-011040 SP4T switch has been used. This is a 20 PIN IC having one RF_{IN}/RF_{OUT} port and four switched port. Proper biasing of the ports is shown in Figure 4.25. For voltages V1 and B1 FDC3601N is used. This is a dual n channel 100 V specified MOSFET. Schematic is given in Figure 4.26.

The SP3T switch is used in both input and output end. MASW-011040 is SP4T switch. So the RF2 and RF3 port is shorted and then fed to the FILTER BANK 2. Also these two pins are low power pin so we have shorted two pins to fulfill the power requirement. The other two ports i.e. RF1 and RF2 are high power ports. The datasheet of this switch in given in Appendix A.

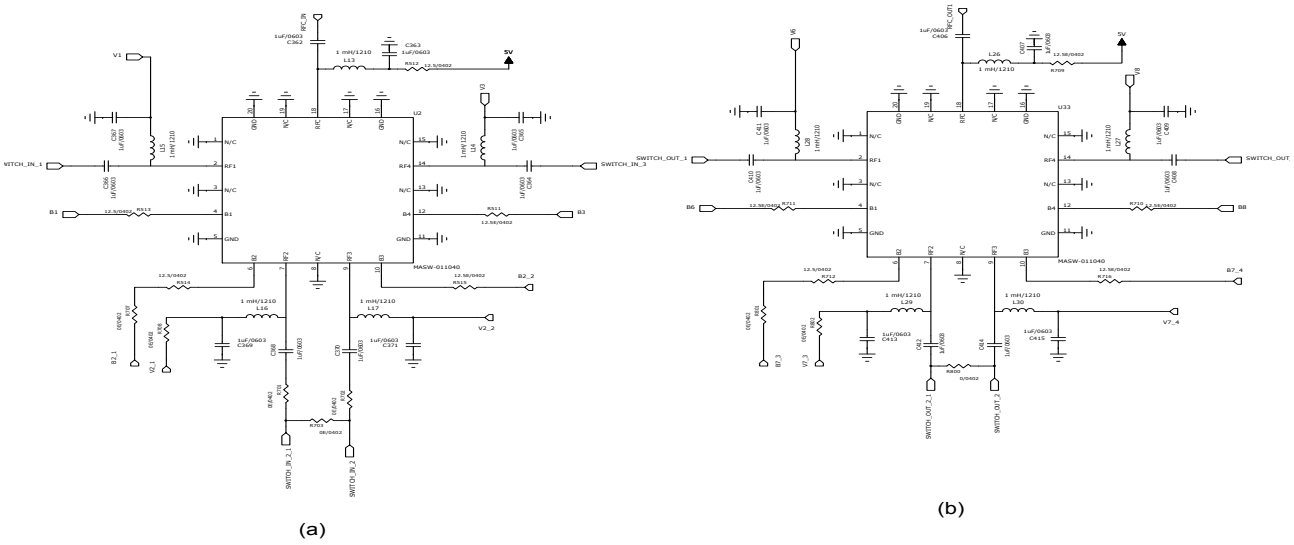


Figure 4.25: SP3T switch biasing schematic

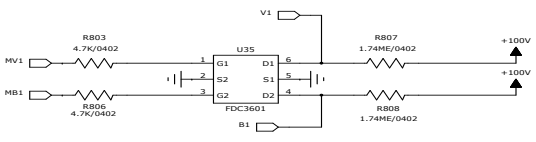


Figure 4.26: MOSFET biasing schematic

4.7 Digital Section

4.7.1 Driver

Drivers are used to for pin diode switching. In this project HV5523 is used. The datasheet is given in Appendix A. This is a low-voltage serial to high-voltage parallel converter with open drain outputs. The schematic and biasing is shown in Figure .The driver is connected to the microcontroller which sends serial data to the driver as per the frequency is tuned. Also remaining Pin diode is connected to the MOSFET (ZVN2120G) is used. This is 200V n-channel enhancement mode MOSFET.

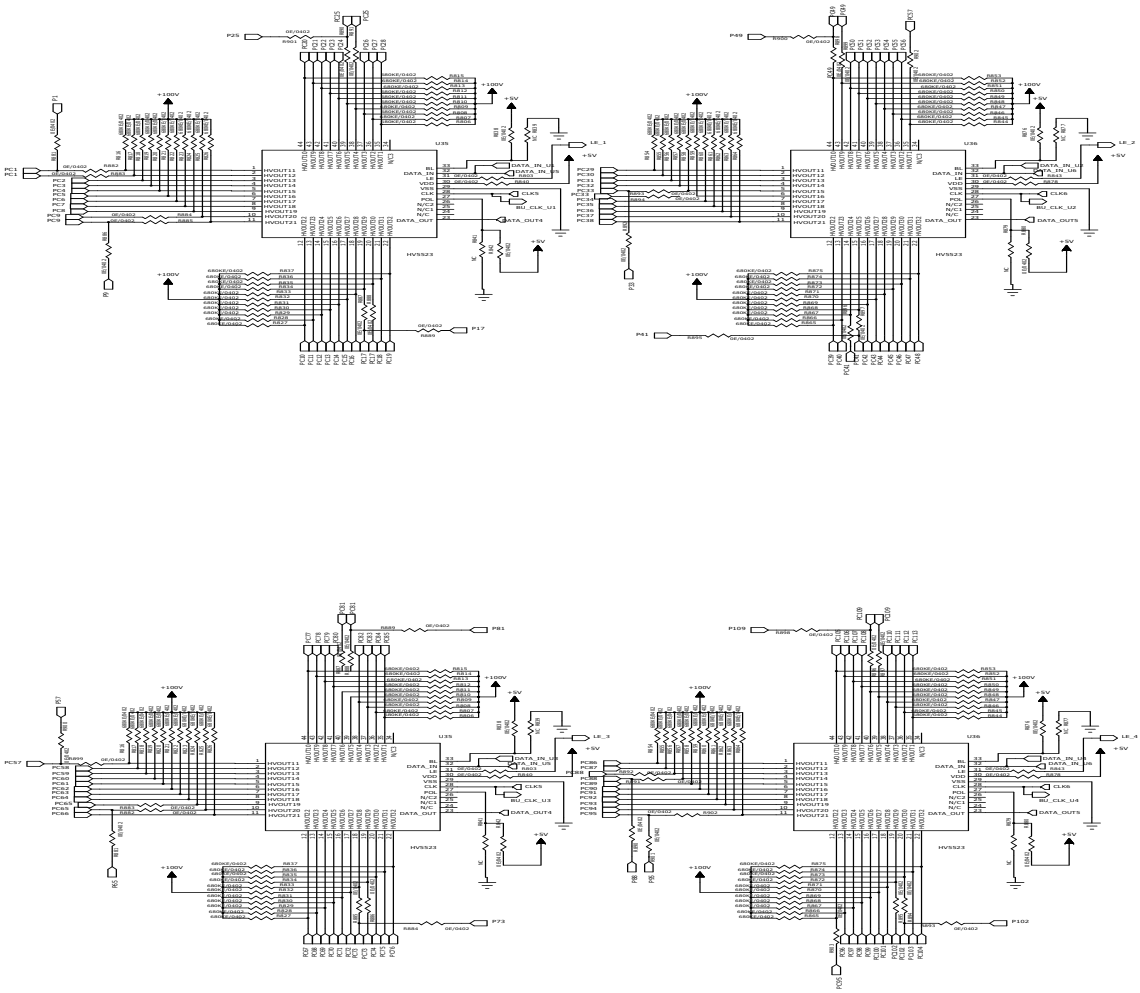


Figure 4.27: Driver schematic schematic

4.7.2 Microcontroller schematic

PIC32MX695F512H microcontroller is used to control the SP3T switch and the Driver ICs. For SP3T the MV1 and MB1 is is connected to the microcontroller which decides which one of the three filter banks to be selected.

For driver the DATA_IN , Latch enable/disable, Clock_IN pins are controlled by microcontroller. The biasing circuit is given in Figure 4.28.

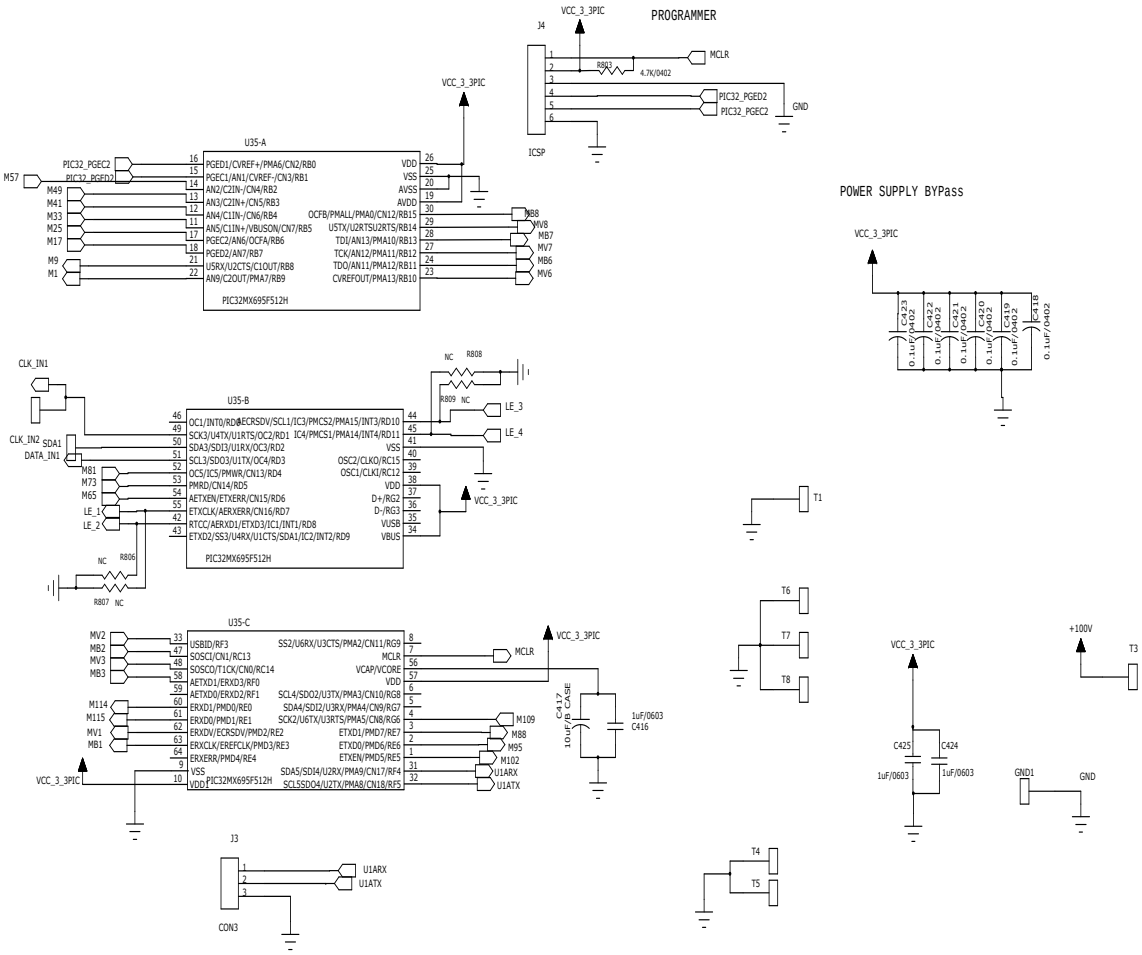


Figure 4.28: Microcontroller schematic schematic

4.8 Components Used

S. No.	Part Number	Description	Package /Case	Supplier	Supplier part number	Qty
1	MA4P506-1072T	DIODE PIN SMQ CERAMIC SI	2-SMD	digikey	1465-1232-1-ND	340
2	HV5523K7-G	IC 32BIT SRL PARALLEL 44WQFN	44-VFQFN Exposed Pad	digikey	HV5523K7-G-ND	4
3	PIC32MX695F512H-80V/MR	IC MCU 32BIT 512KB FLASH 64QFN	64-VFQFN Exposed Pad	digikey	PIC32MX695F512H-80V/MR-ND	2
4	SN74LV4T125PWR	IC BUFFDVR NON-INVERT 14TSSOP	14-TSSOP (0.173", 4.40mm Width)	digikey	296-40545-1-ND	2
5	LT3482EUD#PBF	IC REG BST SWITCHD CAP ADJ 16QFN	16-WFQFN Exposed Pad	digikey	LT3482EUD#PBF-ND	1

Table 4.6: Components Used

S. No.	Part Number	Description	Package /Case	Supplier	Supplier part number	Qty
6	ZVN2120GTA	MOSFET N-CH 200V 320MA SOT223	TO-261-4, TO-261AA	digikey	ZVN2120GCT-ND	5
7	2222SQ-181_E_	180nH	RF chip inductor	coilcraft		2
8	2222SQ-221_E_	220nH	RF chip inductor	coilcraft		2
9	1515SQ_68_N_E	68nH	RF chip inductor	coilcraft		4
10	1111_SQ_27N	27nH	RF chip inductor	coilcraft		2
11	1111_SQ_30N	30nH	RF chip inductor	coilcraft		2
12	251R14S130FV4T	CAP CER 13PF 250V NP0 0603	0603 (1608 Metric)	digikey	251R14S130FV4T-ND	2
13	251R14S360GV4T	CAP CER 36PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	251R14S360GV4T-ND	2
14	251R14S510FV4T	CAP CER 51PF 250V NP0 0603	0603 (1608 Metric)	digikey	251R14S510FV4T-ND	1
15	251R14S680GV4T	CAP CER 68PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1361-6-ND	15
16	251R14S470GV4T	CAP CER 47PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1353-1-ND	5
17	251R14S560JV4T	CAP CER 56PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1358-1-ND	5
18	251R14S270JV4T	CAP CER 27PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1334-6-ND	10
19	251R14S240JV4T	CAP CER 24PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1169-1-ND	15

Table 4.7: Components Used cont(I)

S. No.	Part Number	Description	Package /Case	Supplier	Supplier part number	Qty
20	251R14S120GV4T	CAP CER 12PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1313-1-ND	12
21	251R14S6R8CV4T	CAP CER 6.8PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1364-1-ND	10
23	251R14S3R3BV4T	CAP CER 3.3PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1348-1-ND	15
24	251R14S1R5BV4T	CAP CER 1.5PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1327-1-ND	15
25	251R14S9R1CV4T	CAP CER 9.1PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1369-1-ND	6
26	251R14S160GV4T	CAP CER 16PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1319-1-ND	1
27	251R14S300GV4T	CAP CER 30PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1339-1-ND	5
28	251R14S330JV4T	CAP CER 33PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1342-1-ND	5
29	251R14S390GV4T	CAP CER 39PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1345-1-ND	5

Table 4.8: Components Used cont(II)

S. No.	Part Number	Description	Package /Case	Supplier	Supplier part number	Qty
30	251R14S110GV4T	CAP CER 11PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1311-1-ND	5
31	251R14S150GV4T	CAP CER 15PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1317-1-ND	5
32	251R14S8R2CV4T	CAP CER 8.2PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1368-1-ND	12
33	251R14S6R2CV4T	CAP CER 6.2PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1363-1-ND	15
34	251R14S4R7BV4T	CAP CER 4.7PF 250V C0G/NP0 0603	0603 (1608 Metric)	digikey	712-1172-1-ND	2

Table 4.9: Components Used cont(III)

Chapter 5

PCB layout and Result

5.1 PCB layout

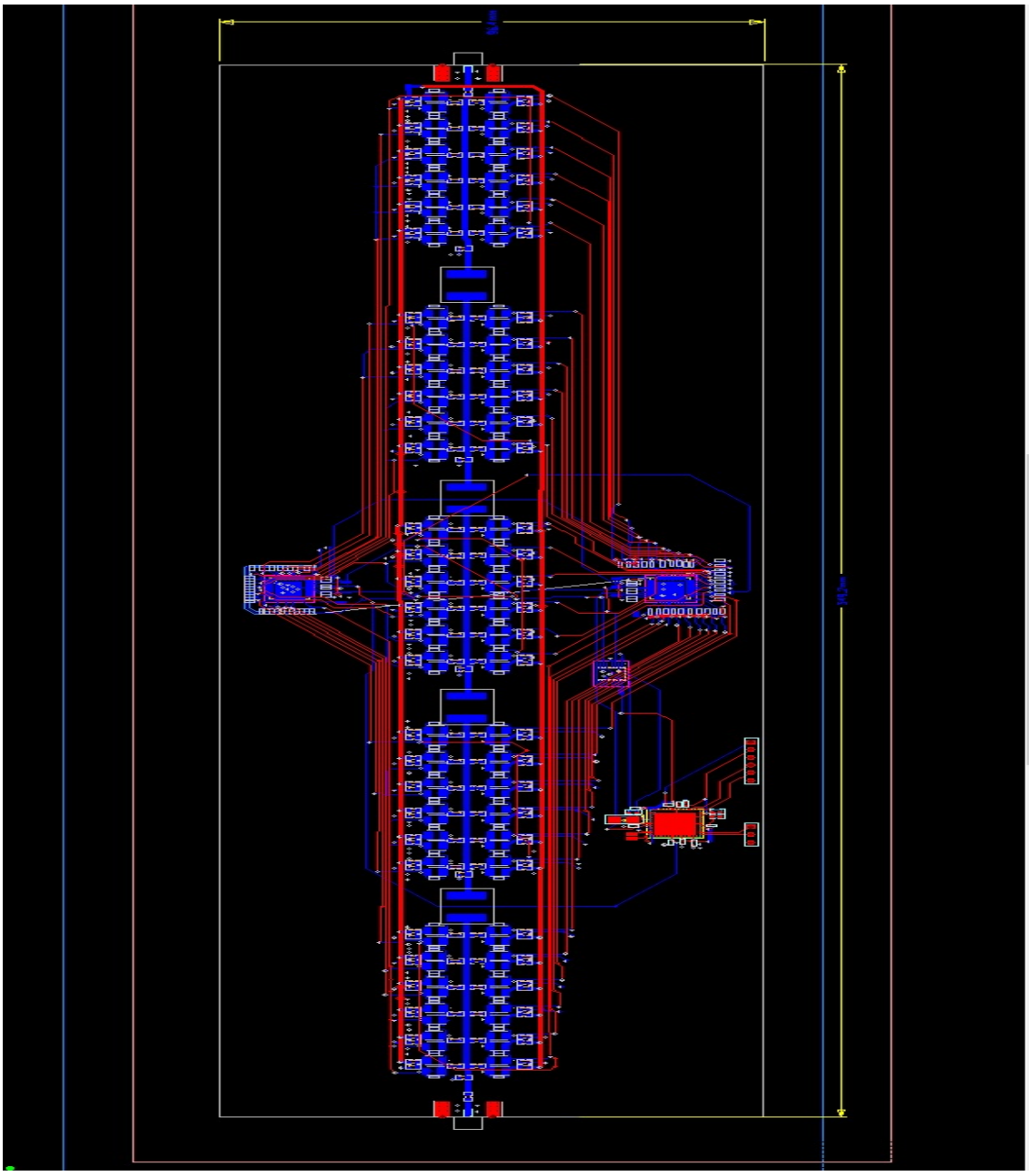


Figure 5.1: PCB Layout

PCB layout of one filter is given in Figure 5.1. Three same type of PCB has been individually made for the three tunable filter. In the PCB given upper and lower side has the drivers and there are five blocks of capacitor places side by side. In between respective inductors are there. RF board is fabricated on a 0.5mm thick Rogers 4350 substrate. At the top layers filters, switches, Drivers are there and the bottom layer include the digital section which has the micro-controller, buffer IC.

5.2 Result

We have connected the filter module to the network analyzer of Agilent technologies E5071B with the help of coaxial cable. Digital controls are given to the micro-controller through the respective pins. The response is given in Figure given below.

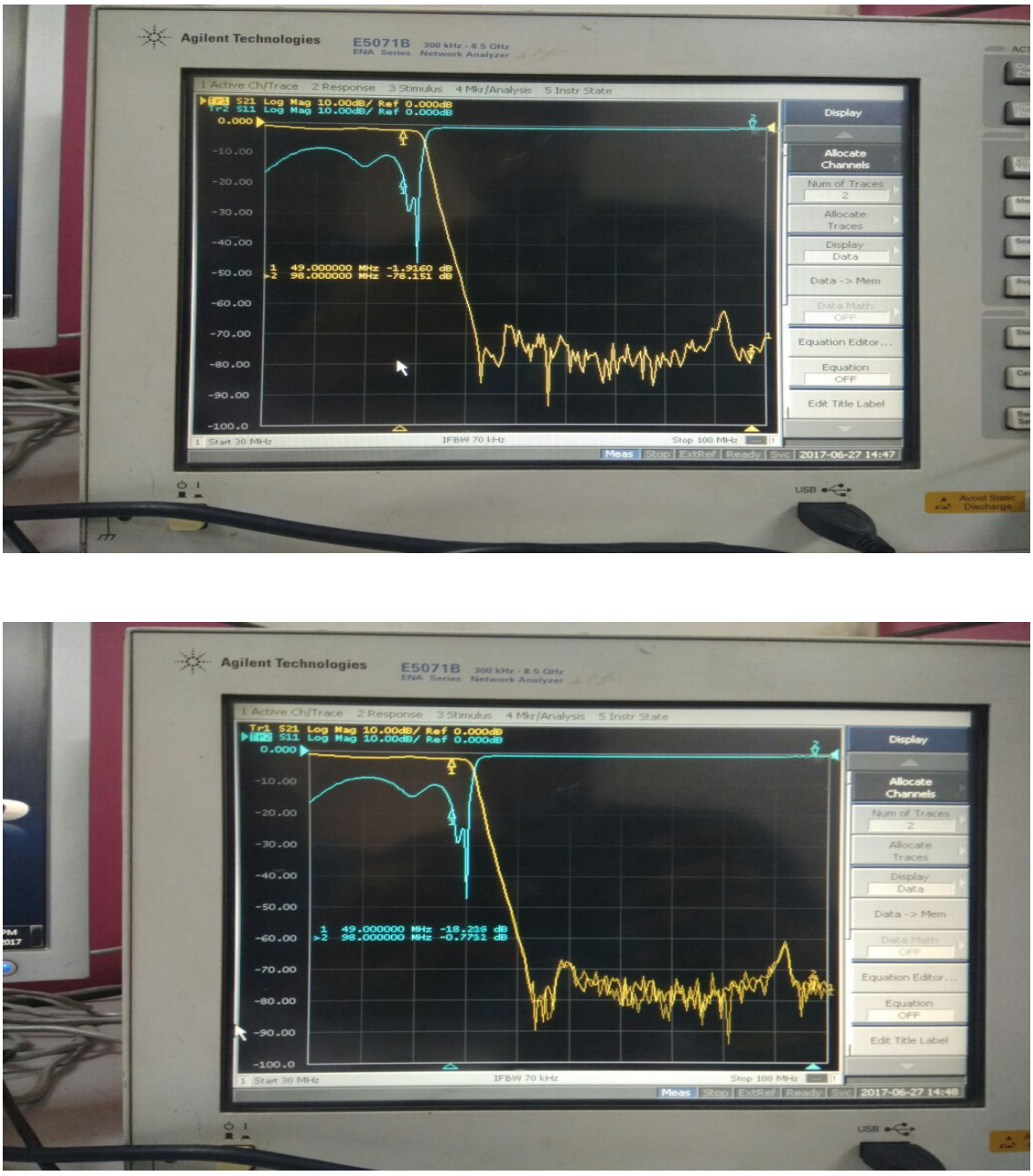
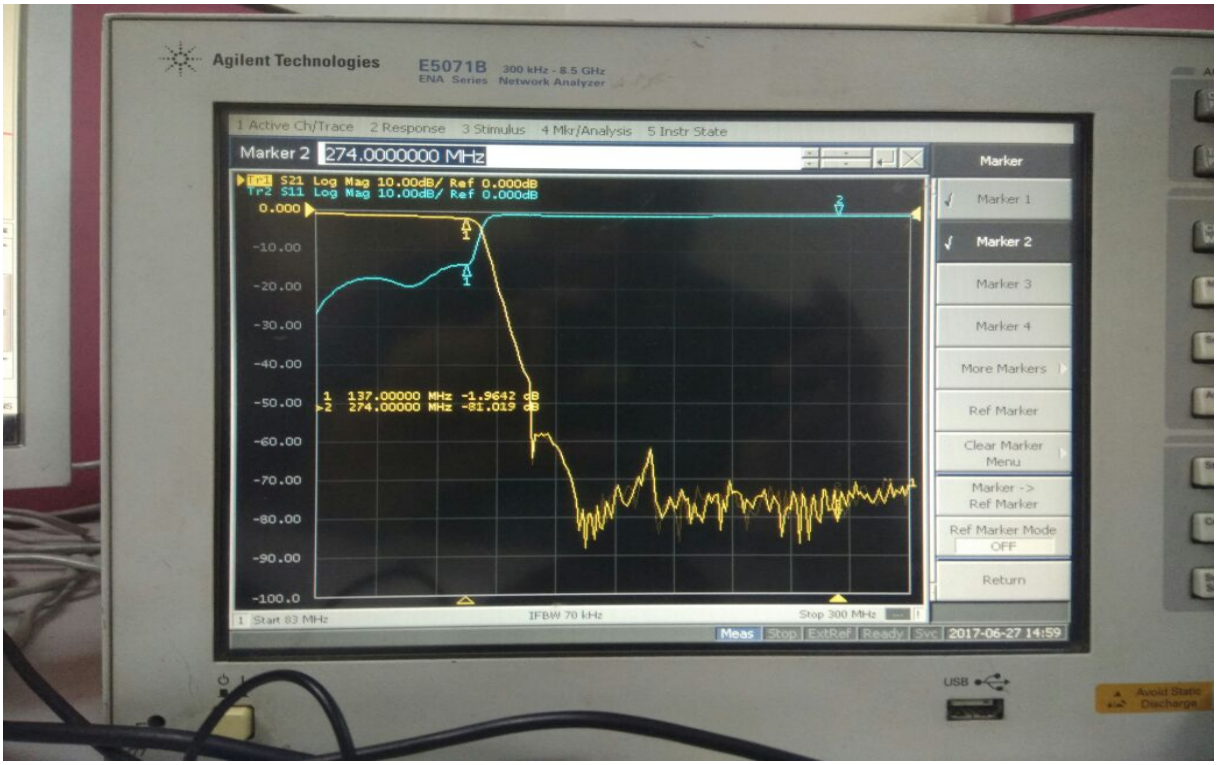


Figure 5.2: Respoonse at 49 MHz

Figure 5.3: Response at 81 MHz



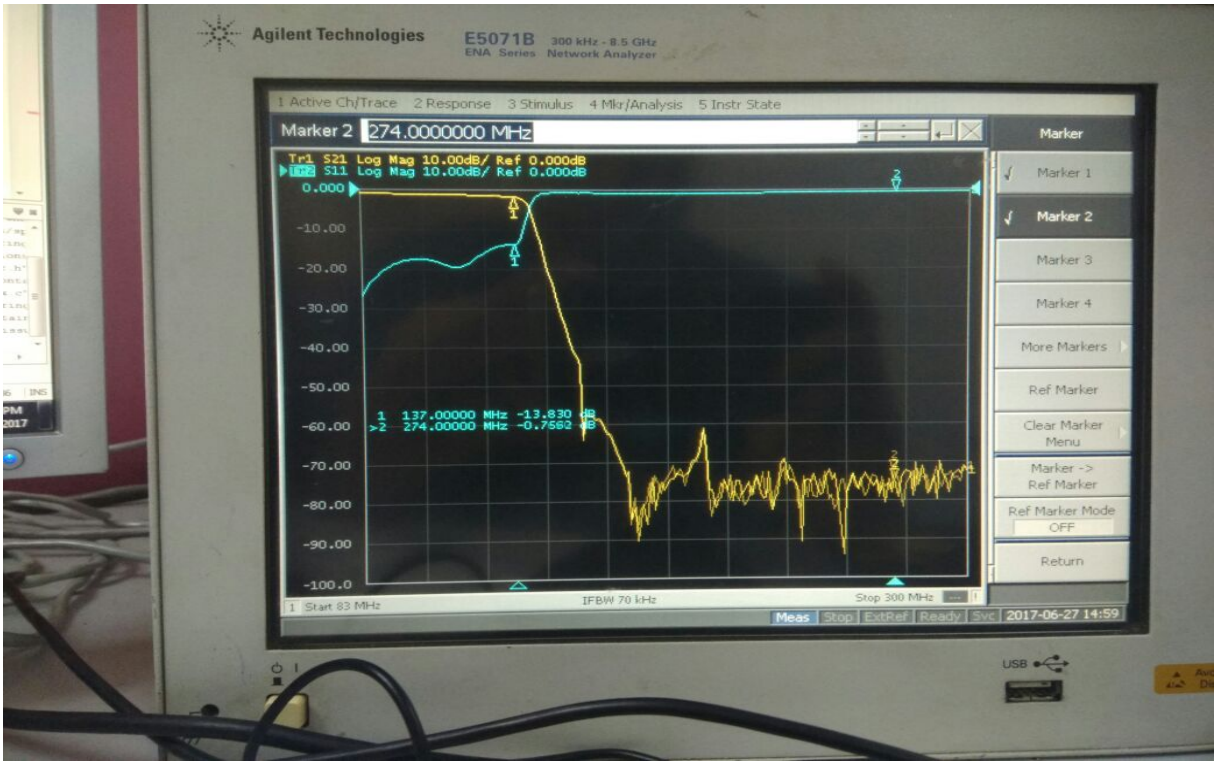
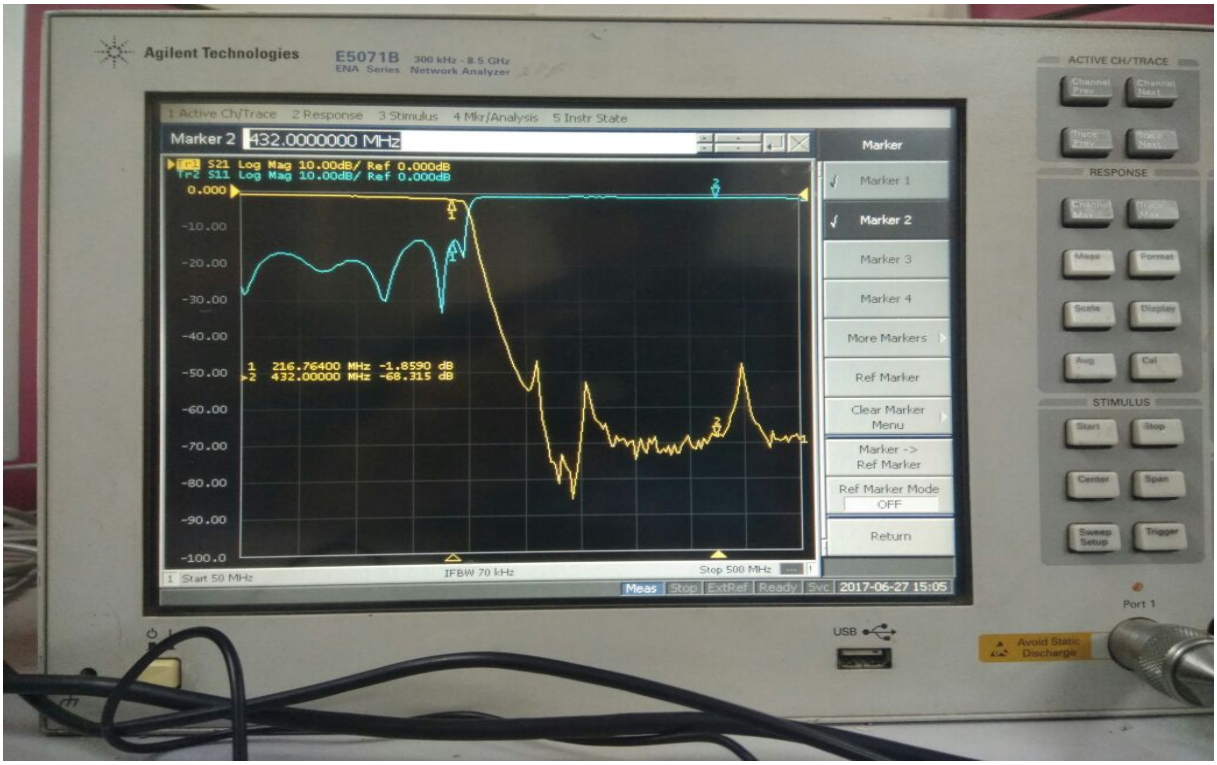


Figure 5.4: Response at 137 MHz



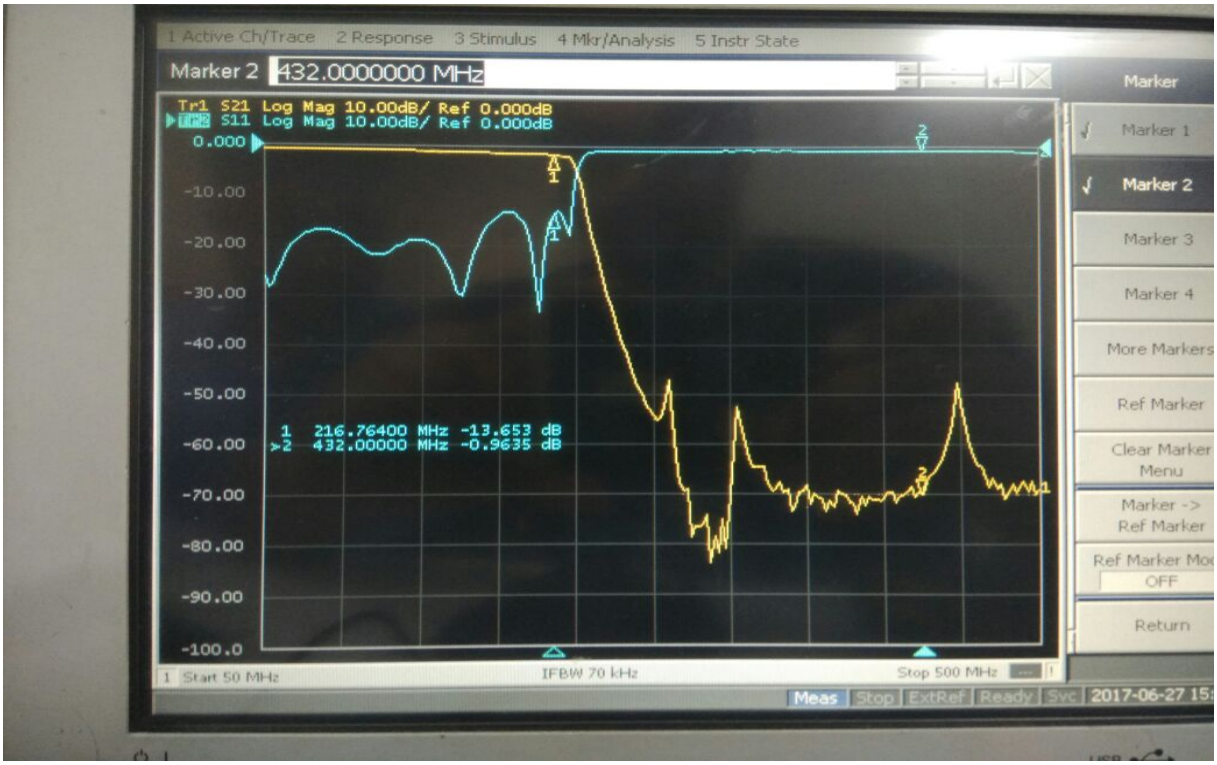
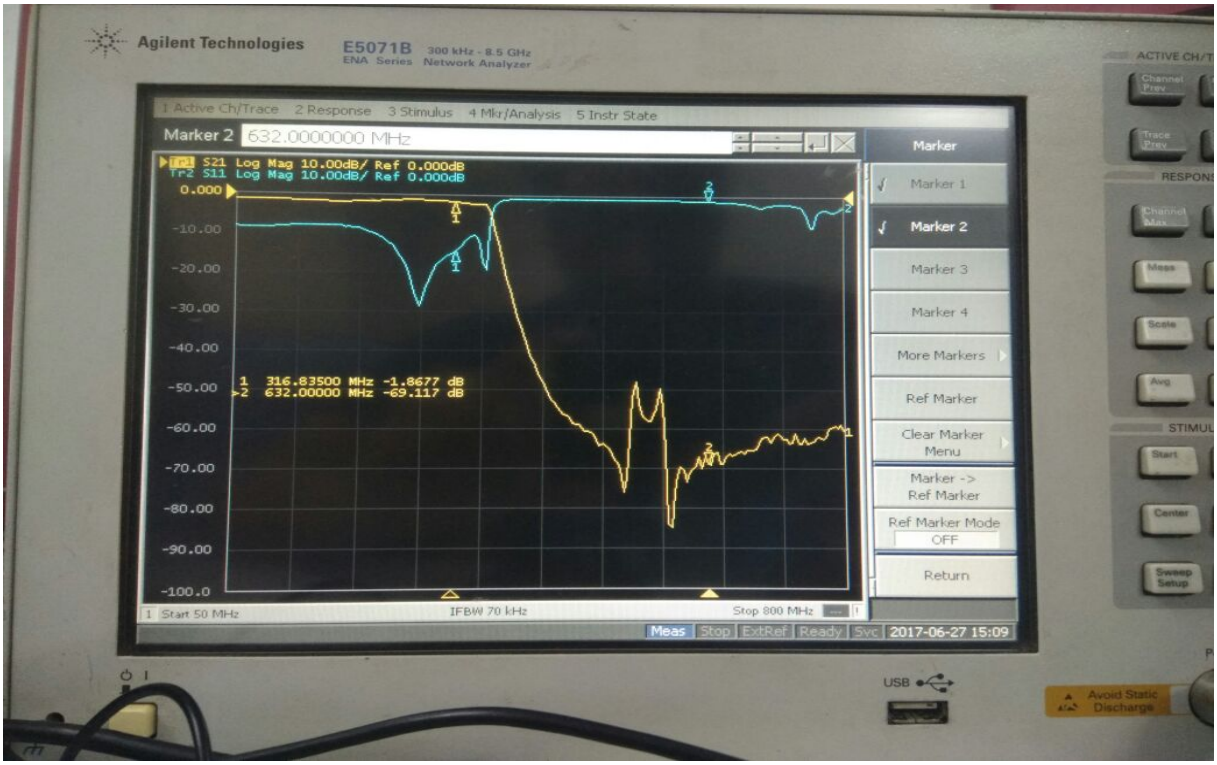


Figure 5.5: Response at 216 MHz



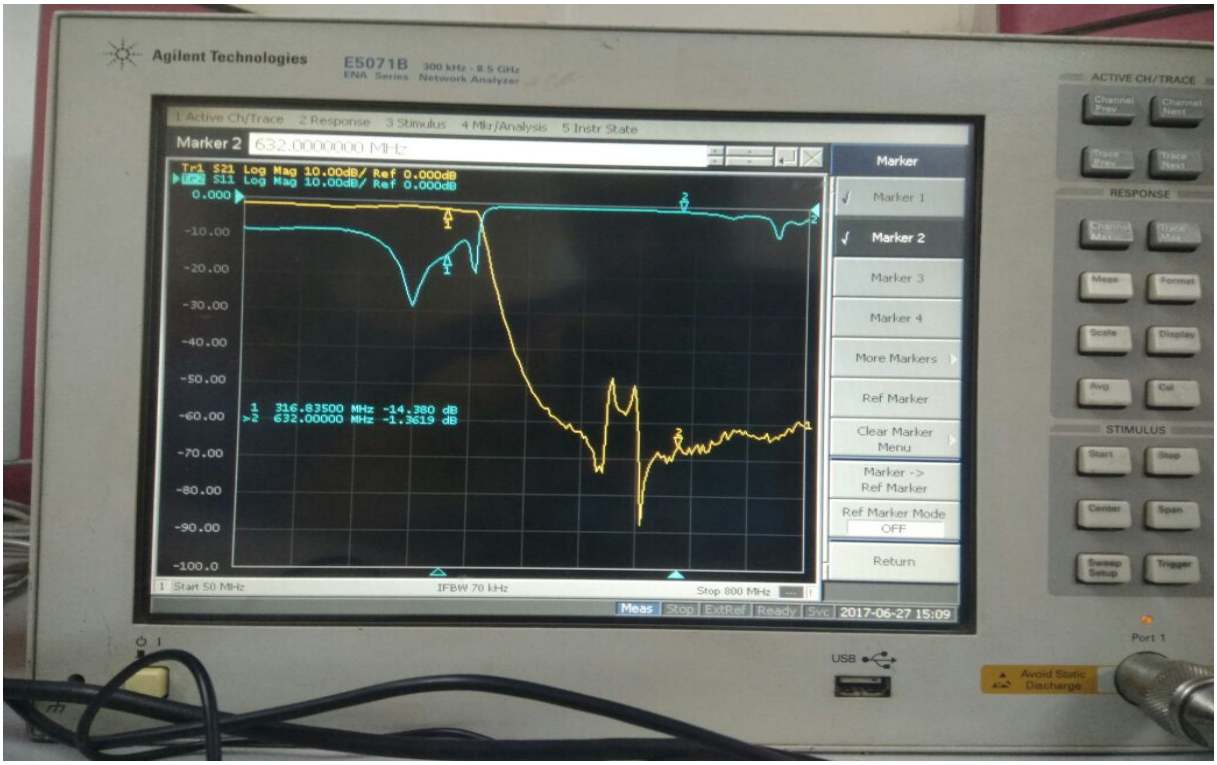
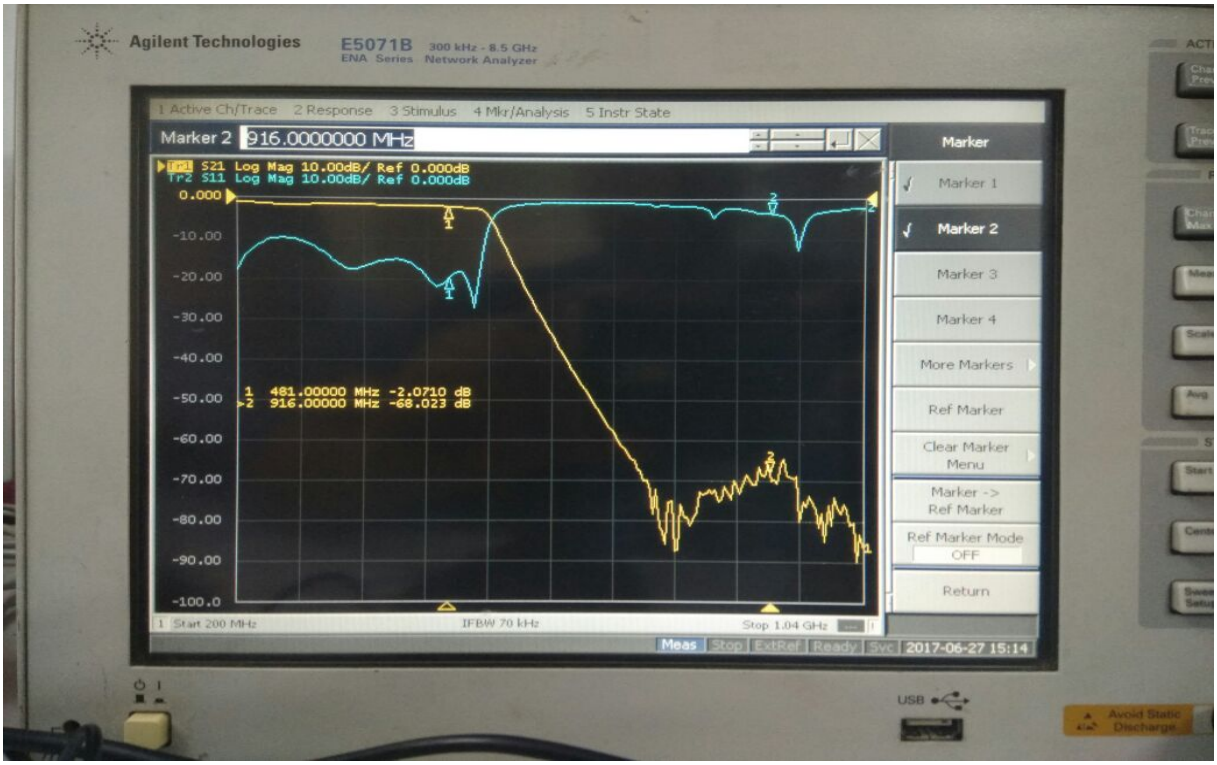


Figure 5.6: Response at 316 MHz



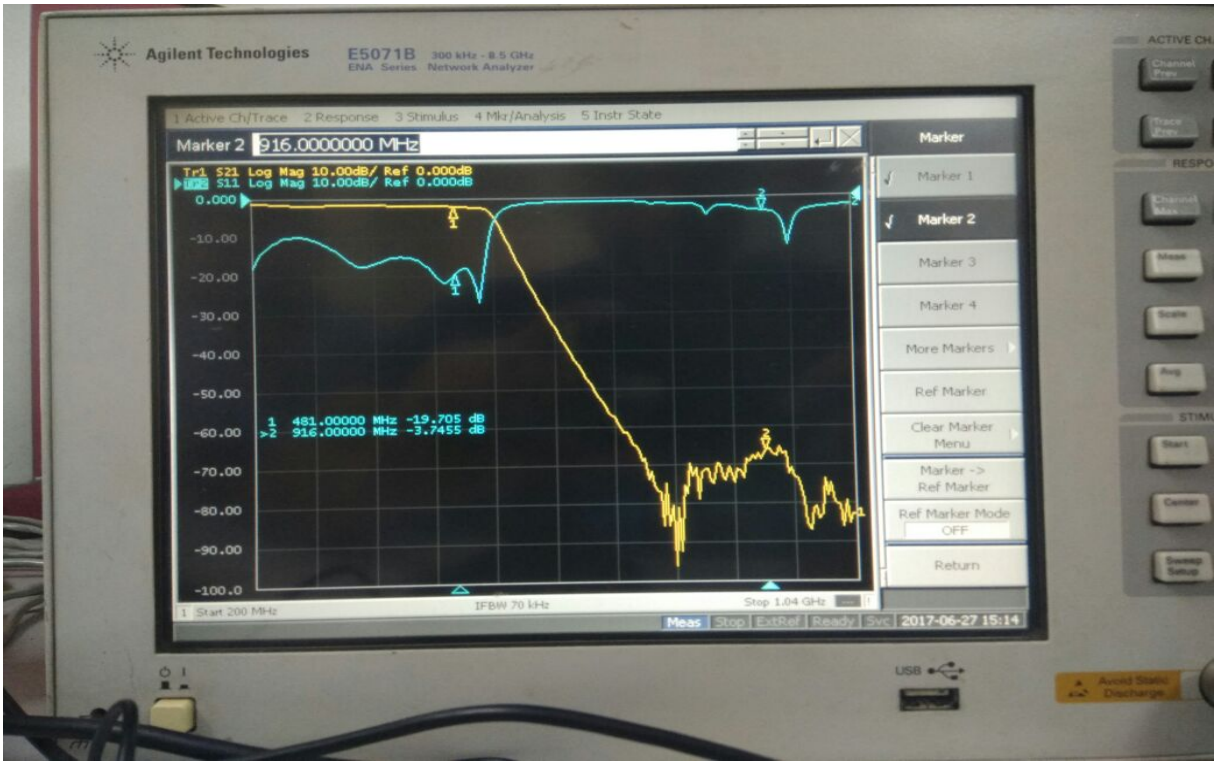


Figure 5.7: Response at 481 MHz

First figure is each page above gives the insertion loss and the second figure gives return loss. There are several problems faced while physically designing the filter with actual component. Some of the major problems are listed below:

- **Parasitic capacitance :** Initially components with large pads size were taken. But they were causing extra parasitic capacitance which was affecting the value of overall capacitance. This affects both insertion and return loss.

  So We have then used less pad sized components to make the parasitic capacitance as low as possible.

- **Quality factor:** At first large single valued capacitance were taken. But the quality factor is decreased by taking single high valued capacitor. This will increase the insertion as well as return loss.

  For this we have taken two or three smaller valued capacitance in parallel. So that the quality factor will increase which in turn gives the good response.

- **Power Dissipation:** As it is high power handling and also made up of passive components, so power dissipation is a major factor. This loss is in the form of heat. In the responses which is taken from network analyzer maximum insertion loss is 2 dB and return loss is 19 dB. If 100 W signal is applied to the filter then 64 watt power is transmitted and rest power is reflected back and dissipated in the form of heat.

  If return loss is 19 dB then the power reflected is nominal i.e. 1.2 Watts.

  So the remaining power loss is due to the power dissipation in form of heating effect. The value of that power which is lost is 34.8 Watts. In future we have to work on the power dissipation.

- **Switch isolation:** In stop band some spikes are coming, which is undesirable. This is because stop band of first filter is in pass band of other two filter. So this means isolation among the three ports are less.

  For further development we will try to design a switch which have higher isolation than the current one. So that it will not interfere with the stop band of other filter.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

The specifications provided in the project is for military applications in software defined radios. My intension behind this project is to create something like this specification. It is very challenging as well as motivational to create as per the industrial standards. Although many compromises were made to save time and reduce complexity.

In the beginning several designs were tested in ADS, and one is selected which suited best for the specifications. As it should be used in the transmitter side so it will require high power handling, so we cant use varactor diode based tuning. Earlier six fixed filter banks were there to meet the above specification. While my design reduced the number of filter banks by half. Also it is going to tune at each frequency individually so comparatively less sharp roll off will meet the specifications well which in turn result in the reduction of filter order. We used ROGERS 4350, 0.5mm thick substrate to reduce loss. With some compromise with the insertion loss other requirements has been achieved.

6.2 Future Scope

In this thesis we have used conventional and a relative simple chebyshev filter to design the tunable filter. An improvement in filter design will further enhance the insertion loss and increase the power handling capacity of the filter. It can be made for more wide band frequency. We can work on the miniaturization of the circuit board.

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