A

Dissertation

On

Study of

Low-Power Pulse-Triggered Flip-flops

Submitted in
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In

VLSI Design and Embedded System

Submitted

By

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CERTIFICATE

This is to certify that the dissertation titled **"Study of Low-Power Pulse-Triggered Flip-flops"** is a bonafide record of work done by **Vicky Kumar, Roll No. 2K15/VLS/19** at **Delhi Technological University** for partial fulfillment of the requirements for the degree of Master **of Technology in VLSI Design and Embedded System.** This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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DECLARATION

I hereby declare that the project entitled " **Study of Low-Power Pulse-triggered flip-flops**" being submitted by me is authentic work carried out under the supervision of **Dr. Neeta Pandey** (**Professor**), Electronics and Communication Department, Delhi Technological University, Delhi.

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ABBREVIATIONS

CLK	Clock Signal
CDFF	Conditional Discharge Flip Flop
DFFs	D-type-flip-flop
Ep-FF	Explicit-pulse-triggered flip flops
Ep-DCO	Explicit-pulse-data-close-to-output pulsed triggered flip-flop
EDP	Electronic data processing
FFs	Flip-Flops
HLFF	Hybrid Latch Flip-Flop
HFF	Semi dynamic hybrid Flip-Flop
Ip-FF	Implicit-pulse Triggered Flip-Flop
Ip-DCO	Implicit-pulse data-close-to-Output
MHLFF	Modified Hybrid Latch Flip-Flop
P-FF	Pulse Triggered Flip-Flop
PG	Pulse Generator
PUN	Pull-up Network
PDN	Pull-down Network
SDFF	Semi-Dynamic Flip-Flop

SCDFF	Static Conditional Discharge Flip-Flop
SFTFF	Signal Feed-Through Pulsed triggered flip-flop
SAFF	Sense Amplifier based Flip-Flop
TG	Transmission Gate
TSPC	True Single Phase Clocked flip-flop

ABSTRACT

Flip-flops and latches are important elements of a digital system design in terms of both a delay and energy stand point. The choice of flip-flop implementation is of essential importance in design of VLSI integrated circuits for high speed, low power and high performance CMOS circuits. In this work, low-power pulse triggered flip-flop (P-FF) designs namely Explicit Type Data-close-to-output (ep-DCO), Conditional Discharge Flip-flop (CDFF), static CDFF and a true single phase clock latch based on a signal feed-through scheme (SFTFF) are studied. Former three fall under conventional P-FF and have limitation of long discharging path issue whereas SFTFF design successfully resolves this and achieves better speed and power performance. The timing parameters for Simulation results are obtained using PTM BSIM4 CMOS 90-nm technology, SFTFF design performs better than the conventional P-FF designs in view of data-to-Q delay.

Chapter -1

Introduction

1.1 Topic overview

Through the past decades, Moore's law runs the VLSI technology to ceaselessly increase the transistor densities, there are hundred millions of transistors concerning a chip at the present time, which to have an issue in that constantly the power consumption of VLSI chip has been being increased. Despite the fact that the capacitances and the power supply reduce during the same time, the power consumption of the VLSI chip is still increasing ceaselessly. With the increasing of the transistor densities and the technology scaling, the circuits are more and more sensitive to the externally induced phenomena, which we refer as a soft-error. Over the extent of the smaller node capacitance and the lower V_{DD}, the quantity of charge placed on a circuit node is getting more and more smaller, this results that the circuits have become more easily affected to unauthentic voltage variations caused by externally induced phenomena, the occurrence of this kind of faults will affect the fidelity of the data, and the flip-flop would create malfunction.

In industry, the expense as long as to keep away from transient faults is significant entire year. So how to design a circuit which can have a high soft-error tolerance is very popular today. In the VLSI circuit as compared to distinct elements, flip-flops are the most important source of the power consumption in synchronous system. In addition to what has been said, flip-flops have a large influence on circuit speed.

The realization of this flip-flop is accomplished by following three timing and delay definitions such as setup time, hold time and the propagation delay (Clock-to-Output). These parameters influence the performance of the entire circuit. Because of that, the exploration of Flip-Flop becomes more and more in recent years.

It is approximated that the power consumption of the clock system, which usually used with in of clock distribution networks and storage elements, is as high as twenty to forty five percentage of the total system power [1]. In addition to what has been said, in order to keep up the tendency of higher performance & throughput, extra timing elements should be used in extensive pipelining belongs to data-path sections, and global bus interconnects, as a result power dissipation of the

clock system turns extra predominant. To have an issue for reducing the power consumption by the flip-flops would make a bad effect on the total power consumption. Other than, in respect of timing definitions, the latency of flip-flop utilizes the largest portion of the cycle time as long as increase in operating frequency .similarly, the choice & design of flip-flop have a deep outcome in respect of providing more slack time as well as in respect of easier time budgeting in high-performance systems. Above explanations leading a major interest in flip-flop design and its analysis.

A broad picking of various flip-flops can be presented in the literature [1]–[11]. Quite a few coexisting microprocessors particularly employ master-slave and pulse-triggered flip-flops [2].conventional master-slave flip-flops are constituted of two steps, earlier step is master and latter step is slave. Both are described by their hard-edge quality. Both Push pull D type flip flip [3],& true single phase clocked flip-flop are referred as a master-slave flip-flop [4].& the sense amplifier based flip-flop is edge-triggered flip-flop [5].above all hard-edged flip-flops are described through positive setup time, resulting larger D-to-Q delays. As matter of choice, pulse-triggered flip-flops reducing the following two stages into a single stage and depicted by the soft edge merits. Inside above pulse-triggered flip-flops the number of stages and logic complexity gets reduced which leads smaller D-to-Q delays due to zero or even negative setup time authorization of time borrowing across cycle boundaries which are major benefits of a pulse triggered flip-flop. Because of timing problems, pulse-triggered flip-flops delivered better performance as compare to the master-slave flip-flops. Because of single-latch structure pulse triggered flip-flop is additionally common as compare to the conventional transmission gate (TG) as well as master–slave based FFs among high-speed applications. Along the speed advantage, their simpler circuits lower the power consumption of the clock tree system. the Pulse triggered flip flop having a feature of a latch as well as pulse generator in which latch stand for data storage & pulse generator stand for strobe signal. let us assume the triggering pulses are short, the latch will performs like an edge-triggered FF.as let us assume only one latch, as contrary to two in the conventional master–slave configuration, is needed, a Pulse triggered flip-flop is not complex in circuit complexity. This leads to a higher toggle rate for high-speed operations. In despite of these advantages, pulse generation circuitry needs fragile pulse width control to match with practicable variations in process technology and signal distribution network.

1.2 Thesis Motivation

The essential approach for constructing a flip-flop using pulse signals. The design is to construct a short pulse through the falling or rising edge of the clock. This pulse behaves like a clock input to the latch, samples the input pulse in short window. The combining of a latch as well as a pulse generation circuitry give results in a positive edge triggered register. The pulse triggered flip-flop creates lesser the no. of latch steps into a single step. The no. of stages and logic complexity gets reduces in this pulse triggered flip-flop. The pulse triggered flip accompanies lesser D to Q delays. The important feature of these pulse triggered flip-flop is to allow time borrowing across clock cycle boundaries and give prominence to a zero or even negative setup time. Due to these advantages the pulse triggered flip-flop is preferred a well know back-up for traditional master-slave flip-flop.

1.3 Thesis Organization

The thesis is organized in six chapters including the introduction one. The content wise details of Chapter 2 to Chapter 6 is as follows:

Chapter-2 Explains prerequisite namely Static & Dynamic CMOS design, Pulse Generator, Modified pulse generator, Keeper circuit and techniques for reducing Switching activity, above all topics played an important role in completion of thesis.

Chapter-3 Focuses on various types of conventional explicit pulse triggered flip-flops such as Ep-DCO, CDFF & Static CDFF.

Chapter-4 Presents the Timing parameters of explicit pulse triggered flip-flops discussed in Chapter 3.

Chapter-5 Briefs about the Signal Feed-Through Pulsed triggered flip-flop Design and its timing parameters.

Chapter-6 Presents the concluding remarks with scope for further research work.

Chapter 2

PREREQUISITES

(2.1) Static CMOS Design:

The static CMOS gate are to be composed of the two networks in which the first network is referred as the pull-up network (PUN) and the other network is referred as pull-down network (PDN). Figure1 represents a 'n' inputs logic gate in which all inputs are assigned or delivered to the both networks. The pull-up and pull-down networks are designed in a mutually exclusive manner so that one & only one of the networks is operating in a steady state. As in this manner, at any one time the transients have been settled, a path continually happens during V_{DD} and the output F, attaining a high output as '1', or, an alternate way among V_{SS} and F for a low output as '0' [12].

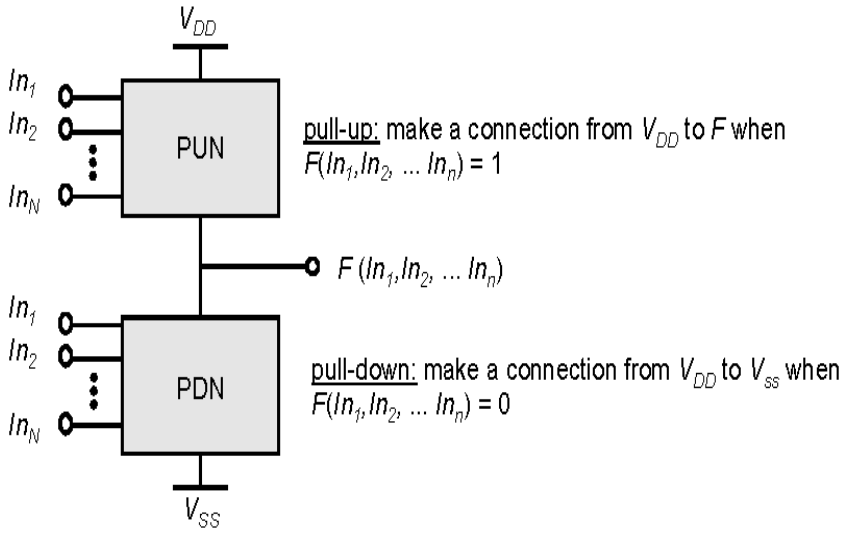

Figure 1 - Static CMOS n input gate

(2.2) Dynamic CMOS Design:

Dynamic CMOS design is preferred over static CMOS design because of the following reasons. For the complex gates the number of transistors is indeed lower as comparison with the static case: N + 2 contrary to 2N. The methods used to decrease the number of transistors (pseudo NMOS, Pass transistors) corresponds to static power dissipation. It is not a Ratioed logic design. It only use up dynamic power. Figure 2 depicts typical dynamic CMOS gate which uses pull-down network PDN, and two transistors M_p and M_e. Working of the above circuit is getting divided into two major stages: the first stage is the Pre-charge & the second phase is the Evaluation, by the mode of operation which is demarcated through the *CLK* the clock signal.

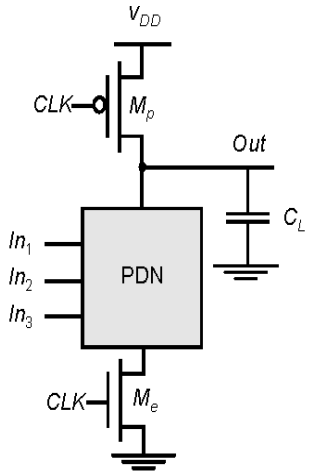

Figure 2 - Typical Dynamic n input gate

<u>Pre-charge</u>:

Just as *CLK* tend to '0', the output node 'Out' is pre-charged to V_{DD} through the PMOS transistor M_p. at the same time as, the evaluate NMOS transistor M_e is off, hence the pull-down path is disabled.

Evaluation:

When the *CLK* tends to 1, the pre-charge transistor M_p is gone off, and the evaluation transistor M_e gets turned on. The output is comparatively discharged rely upon the input values and the pull-down topologies.

Correctly, no static current path consistently takes place between V_{DD} and GND**.** The logic gates having the faster switching speeds, because of the diminished load capacitance has been assigned to the lower number of transistors per gate as well as the single-transistor load per fan-in[12].

(2.3) Dynamic stages

TSPC Latches and flip-flops are based on four basic dynamic stages which are depicted in Figure 3. The SN and SP stages are clocked inverter and provides inverted input data at output when clock signal is respectively high and low. Cascading SN with SP will result in negative edge triggered flip-flop. In case SP is cascaded with SN the resulting structure would be positive edge triggered flip-flop.

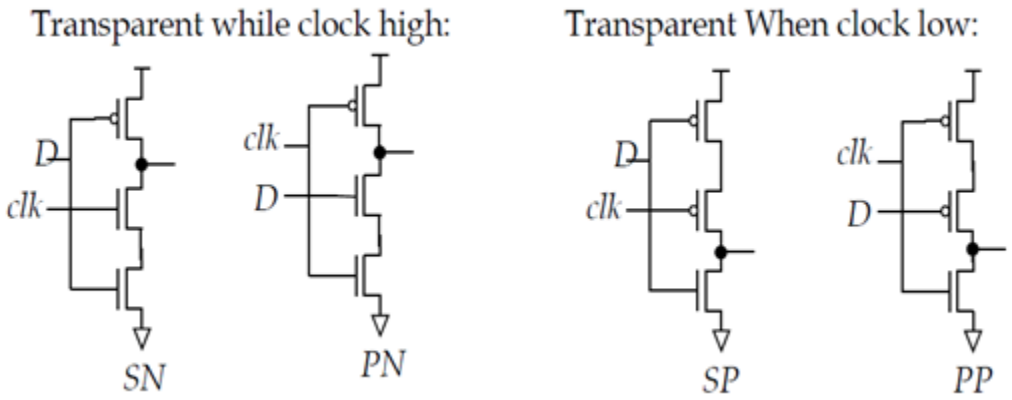

Figure 3 – Basic TSPC Dynamic Stages.

The PN and PP stages are dynamic in nature and based on pre-charge and evaluate principle. It may be noted that PN uses NMOS for evaluation whereas PP uses PMOS for evaluation purpose.

Edge Triggered flip-flops could be implemented through these latches with Masters-Slave Configuration. Hence in order to reduce the number of latches and circuit complexity, different combinations of TSPC dynamic stages can be employed [13].

(2.4) Pulse Generator

Figure 4 shows the sample circuit for constructing the lower deliberate glitch on each rising edge of the clock. On the rising edge of the clock, there is a short duration in which both the inputs of the AND gate tend to be high, making Pulse_CK high. The pulse's length is to be monitored from the delays of these three inverters. There exists a delay among the rising edges of the input clock (CLK) as well as in the glitch clock Pulse_CK. supposing each register at the chip employs the identical clock generation method, then this sampling delay does not be concern.

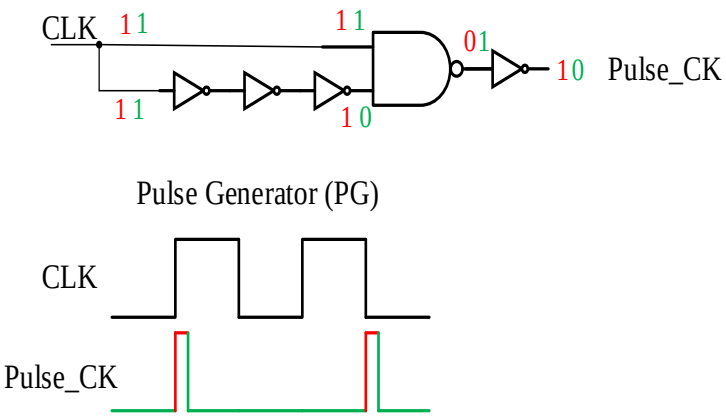

Figure 4 - Pulse Generator

(2.5) Modified Pulse Generator

It is a pulse generator with pass transistor logic. This pulse generator improves one disadvantages of the pulse generator as shown in the Figure 5. This pulse generator can generate a narrower pulse at both the rising edge of the clock; this could benefit the flip-flop reduce the

setup time and hold time efficiently. The only disadvantage of is that this pulse generator produces a pulse which can get near to the V_{DD} but not equal to it. [26]

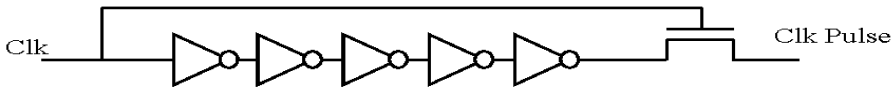

Figure 5 - Modified Pulse Generator [26]

(2.6) Technical approach for reducing switching activities

Almost all the flip-flops shown in this work are dynamic in behavior & a few internal nodes get pre-charged and is evaluated in every cycle without generating any usable activities in the output as the input sets to be stable. Restricting the redundant switching activity will have an intense impact in reducing the power dissipation, and so many publications were published on this technique in the literature[13]–[16].The main technical approaches are classified into following: Conditional pre-charge, Conditional discharge and Conditional capture.

(2.6.1) Conditional Pre-charge Technique

The common thought of this technique is that the pre-charging path is restrained to prevent the occurrence of pre-charging the internal node if it stays High. Figure 6 exhibits the common plan of the conditional pre-charge method. due to absence of the pMOS pre-charge control and it goes High for the long period of time, the path of discharging goes on through the evaluation time, which resulting node to discharge through any pre-charging phase.in order to get rid of this charging or discharging activity, the pMOS transistor have to put into pre-charging path in which it would to stop from happening of the pre-charging of node as the data input goes stable high.

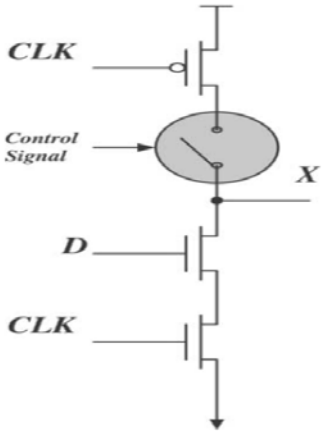

Figure 6 - Conditional Pre-charge Technique

(2.6.2) Conditional Capture Technique

It is based on the clock-gating concept, & Figure 7 shows the general scheme for this technique. This technique is basically employed for implicit pulse-triggered flip-flops. Necessary it is an internal clock-gating approach. Flip-flops in this category have a transparent window period which is employed for sampling the i/p. This window, created by an implicit pulse generator, is determined by the time when both clocked transistors in the 1st stage are simultaneously on. After sampling a HIGH state at the input, the output will be HIGH. This output state could be used to shut the transparent window as long as it is HIGH, preventing the redundant activities of the internal node.

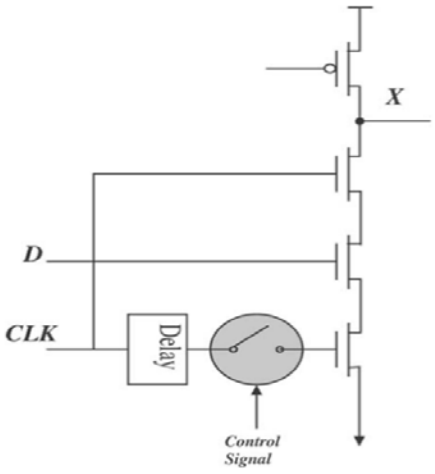

Figure 7 - Conditional Capture Technique

(2.6.3) Conditional Discharge Technique

In this process clock-gating played an important role which gives rise to the redundant power consumed through the medium of the gate regulating transmittal of the clock delay prior the flip-flop. Consequently, the conditional pre-charge method surpasses the conditional capture technique in respect of reduced FFs EDP. however individually conditional pre-charge method refers to use in implicit pulsed-FF,& unclearly for taking advantage of a double-edge triggering mechanism in consideration of these above flip-flops, so that would demand more transistors. Other different technique which is shown below the Figure 8, this method, should employ for both implicit pulsed triggered FF as well as explicit pulse-triggered flip-flops. This technique doesn't have any issues which is associated through the conditional capture technique. In this method the important features is that extra switching activity is excluded by the control of discharging path, as the input goes to stable High hence, name itself so called the Conditional Discharge Technique. for this method another important feature is that the nMOS transistor construct through inserted the discharge path of the stage which along having high-switching activity. as the input experiences the Low to High transition, the output changes to High & to the Low. This changed transition at output switches on separates the discharge path of the 1st stage which is for defend self from discharging or by doing evaluation for accomplishing cycles provided that the input is set to be stably High.

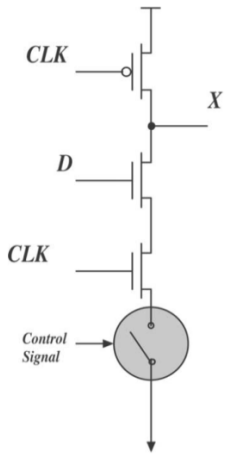

Figure 8 - Conditional Discharge Technique

Chapter 3

Conventional Pulsed triggered flip-flops

The Pulse triggered flip-flops are classified as Implicit and Explicit pulsed triggered flip-flop In case of implicit-pulse triggered flip-flop (ip-FF),the pulse is generated inside the flip-flop , the following pulse triggered flip flop such as HLFF , SDFF, MHLFF , SCCER & ip-DCO etc. are refers to the implicit pulsed triggered flip-flop. The Explicit Pulsed triggered flip-flop (ep-FF), the pulse is generated externally and ep-DCO [9], SEPFF and STC-EPFF are examples of such flip-flop. More apparently, explicit pulsed flip-flop employs more energy as the result of the explicit pulse generator. Still, explicit pulsed flip-flop have a certain advantages. First, the explicit pulsed flip-flop has pulse generator which is belonging to or contributed by neighboring flip-flops, simply this sharing method not employed for ip-FF. This sharing technique could have benefits in delivers power which is overhead of the pulse generator over all kinds of explicit pulse Flip-Flop, & system employs the advantages of ep-FF would have more energy efficient than the system employing the benefit of ip-FF. Second advantage is that, explicit pulse triggered-Flip Flop has the important feature of effective performance since top part of the MOS stack via explicit pulsed-FF is having less when compares with implicit pulsed-FF [2]. For that characteristic on study it is to accept that topology of explicit pulsed triggered flip flop is more suitable in respect of low-power & high-performance designs.

Implicit Pulsed Flip-flops

Concerning the application of high-performance , in a way that the almost all the fault-finding design's path, accomplishing the smaller delay in flip flops are most important although less concerning about power consumption .as in case of concerning or representing an implicit-pulsed triggered flip flop such as ip-DCO , HFF [17] & Semi-dynamic hybrid flip-flop SDFF [18-19]. It has been noticed that the ip-DCO flip-flop propose an efficient D to Q delay in

comparison to SDFF & HFF and it also advances the efficient capability of time borrowing capability (that is negative setup time is more). Most essential cause in back for this improved performance is because transistor has driven through input data of 3 transistor stack which has been placed at the center concerning Hybrid Flip Flop and Semi-Dynamic flip-flop, and it is situated near the ip-DCO's o/p node. In which it enhances the performance during the 1 sampling on account of that explanation the nodes of intermediate slack nodes are discharged if there is arrival of data signal. now including that, this design permits the more negative setup '0' time due to this the stack node is pre-charged initially during which the arrival of rising clock edge and hence prevents false evaluation until data changes to 'Zero'.

Explicit Pulsed Flip-flops

Here the Pulse-triggered flip-flops surpass hard-edged flip-flops, because it provides the smaller D-Q delays & it also supplies soft edge, negative setup time, hence, above these properties or characteristics benefits in reduces the delay penalty to these flip-flops which incur on cycle time & it also benefits in respect of absorbing the clock skew [6], [20-21]. in most cases comparison to the implicit pulse triggered Flip flop, explicit pulsed triggered FF don't offer any efficient performance & it also consumes more energy because of explicit pulse generator [7]. In whatever way, pulse generator power dissipation aloft in which it could give or delivers among flip-flop's group. Some of the conventional ep-FFs are ep-DCO, CDFF, Static CDFF and MHLFF. The modified TSPC latch which is stand on SFTFF is also introduced. These flip-flops are studied and analyzed in this work to compare their performance on the basis of setup and hold time, min Data-Q delay and overall power consumption.

The remaining section of this chapter operation of conventional explicit pulse triggered flip-flop designs is explained.

(3.1) Explicit Type Data-close-to-output P-FF (ep-DCO)

(3.1.1) Operation:

The schematic diagram of the ep-DCO flip-flop is depicted in Figure 9. It comprises the pulse generator which based on NAND logic & the semi dynamic TSPC structured latch design which is to be composed of 2 stages in which 1^{st} phase refers to the dynamic stage & the 2^{nd} one refers to the static stage. In this PFF design, the roles of inverters I_3 & inverters I_4 is to latch data. The roles of the inverters I_1 as well as inverter I_2 are to hold value at internal node *X*. Pulse width is being controlled through three inverter's delay. in pursuit of clock's rising edge ,then the transistors MN2 & transistors MN3 get starts for short time, that is equivalent to delay incurred by pulse generator .although, transparent flip-flop & the input data gets propagating towards the o/p. later on After transparent period, in both stages the path of pull-down gets turned off by means of the transistors MN2 and MN3.therefore any change in input should not pass through output. when the circuits are in hold mode Keepers are mostly employed to maintain the function of output as well as internal node by means of charging & Discharging the internal node x. The cautious examination of ep-DCO circuit discloses the heavy amount of power being consumed .in each clock cycle Node X is going to charge as well as discharged if the input Data goes for no change. The valuable operation is not produced through these internal activities, as the charging as well as discharging process hasn't. provide the circuit's operation then part of power gets dissipated in every 'clock' cycle, since at high output, continuous way of charging & discharging at node X always resulting a glitches which is arise at output, while though this brings the discharging path for the process of internal node x .which is pre-charged high the output node . which carries little time behind the starting period of evaluation[12]; these path resulting the output to lose some charge additionally glitches are propagating through driven gates which resulting increases the Switching power consumption plus also creates noise issues which gives direction through the system to malfunctions. To overcome this problem, many remedial measures can be used. One of them is conditional discharge [22].

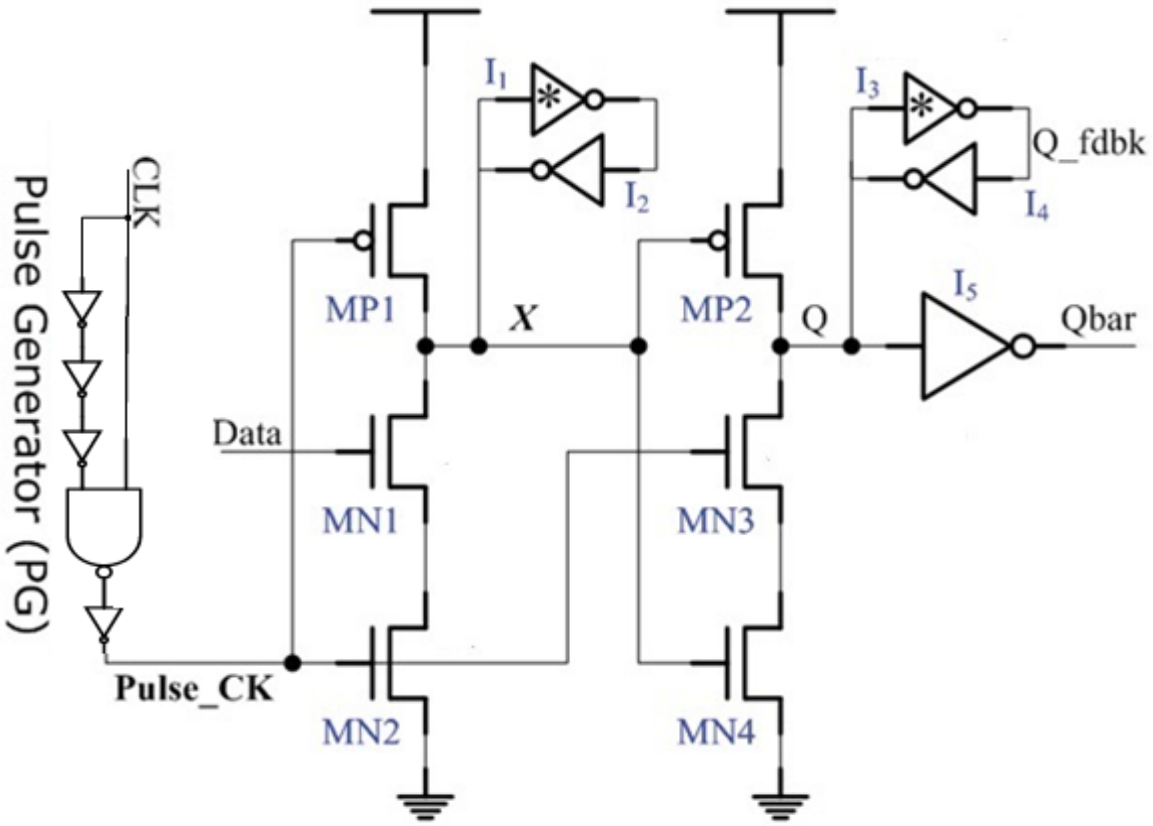

Figure 9 – Schematic of Ep-DCO

(3.1.2) Switching activity:

Simulations were performed for checking switching activity i.e. charging and discharging at node X and glitches at output Q. The simulation setting for clock input are listed in Table 1 where symbols have usual meaning. The power supply of 1.2 V is used and data input is tied at logic '1' i.e. 1.2V. The technology parameters of 90 nm PTM CMOS are used.

Table 1:

Clock and Input Pulse Parameters for ep-DCO

Parameters	CLK
v_1	1.2v
v_2	0v
Per	2ns
t_d	0ns
t_r	1ps
t_f	1ps
pw	2ps
frequency	500MHz

Figure 10 shows that Node X is charged and discharged at every clock cycle especially when the input is not changing and The output is high, the repeated charging or discharging of node x in each clock cycles causes glitches to appear at the output. And these glitches increase the switching power consumption and also cause noise problem.

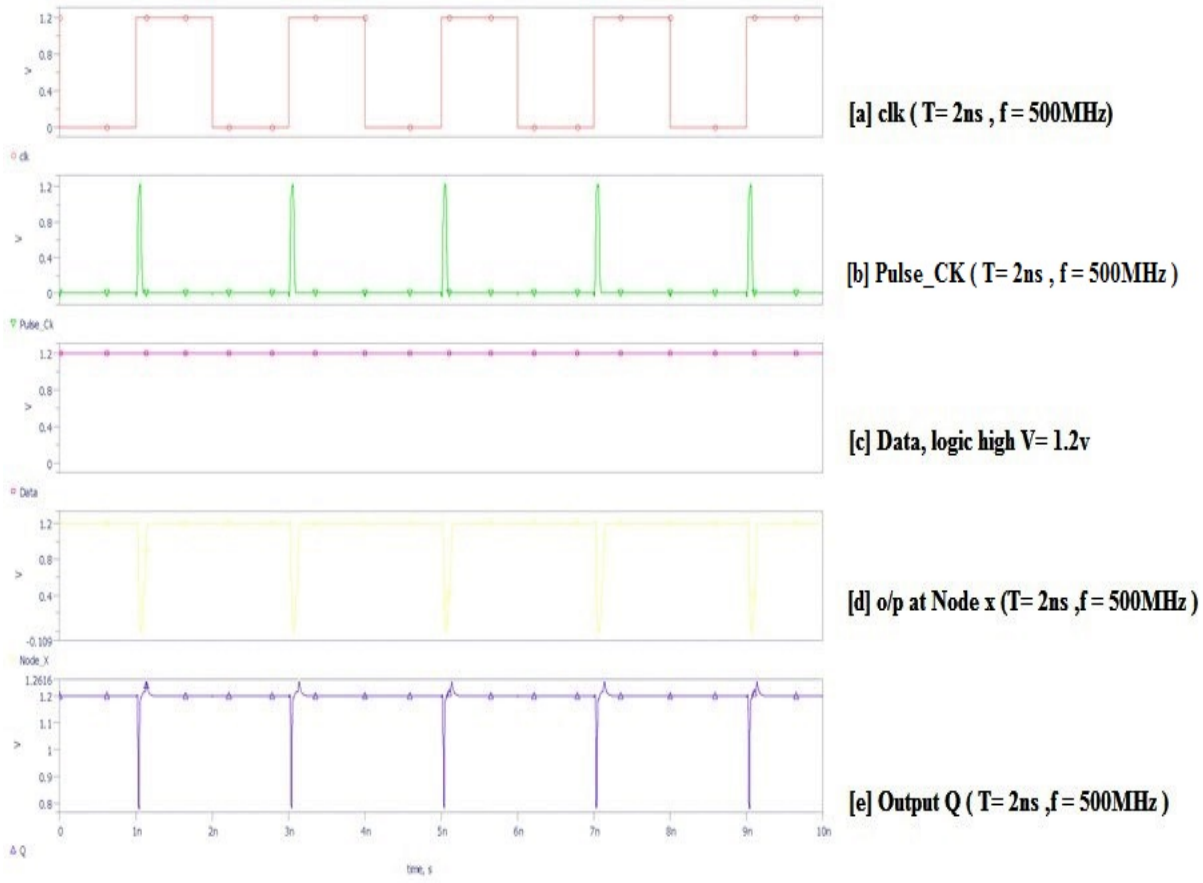

Figure 10 - Waveforms of Ep-DCO showing charging and discharging at Node X and glitches at output Q

(3.2) Conditional Discharge Flip-flop (CDFF)

(3.2.1) Operation

The schematic diagram of a CDFF is placed in a Figure 11. Further, NMOS transistor MN3 is managed through o/p signal in which Q_fdbk gets applied thus there is no occurrence of Discharging in case that data input stays 'one'. Flip-flop generally made up of two stages. The first stage manages to carry off Low to High transition. Assuming that in case of sampling window the high Input data ,Internal node x going to discharged, presumptuous (Q and Q bar) that were at first (Low, High)of discharging .Consequently, at second stage for charging the o/p

node to high through the MP3. The 2nd stage played an important role for holding the High input transition to-Low input transition. If data inputs are Low in the meanwhile the period of sampling, next first stage gets disabled, & node X plays a role of holding the pre-charge state. in case of input node of the MN5 should goes high,& in case of 2nd stage discharging path should be enabled through the period of sampling, which helps in allowing the output node to gets discharge and capturing the data input.

In CDFF we use a conditional discharge technique in which a discharge control transistor (MN3) is employed at the 1st stage discharge path which reduces the redundant switching power. As Q bar equals to High, it means that Q is equal to Low & X is equal to High, the MN3 gets turned on, & enables the discharge path . if data input creates the Low transition to High transition,& high Pulse_CK , the MN1, MN2 and MN3 starts the function which is switched on , the node X internally goes to discharged to the Low, and Q gets pulled up to High & the Q bar is pulled down to Low, which is at 1st n MOS stack gets closed. On behalf of data transition i.e. Low transition to High transition, X goes discharged once it means that at D High level would not goes to sampled since path of discharging is restrained through Q bar. To make sure that Data High transition to Low transition are being sampled through flip-flop, dual path gets employed.to remember from past that rise transition of output which goes to be slow path it means the critical path on using dual path, it reduces the capacity at node X , and hence lessen the Low to High delay.

After all at every clock all node X does not charged & discharged, if the data input goes to high there appears no glitches on the o/p node Q (Figure 12), & Q would not discharged at starting of any calculation. Correspondingly, Conditional Discharge flip-flop characteristic is lessens noise generation of switching that is the critical issues in circuits of mixed signal. However, node X attains High or pre-charged as several cases, it helps in simplifying the structure of keeper and consisting of an inverter & pull-up p MOS transistor only, & at node x that also reduces the capacitive load .

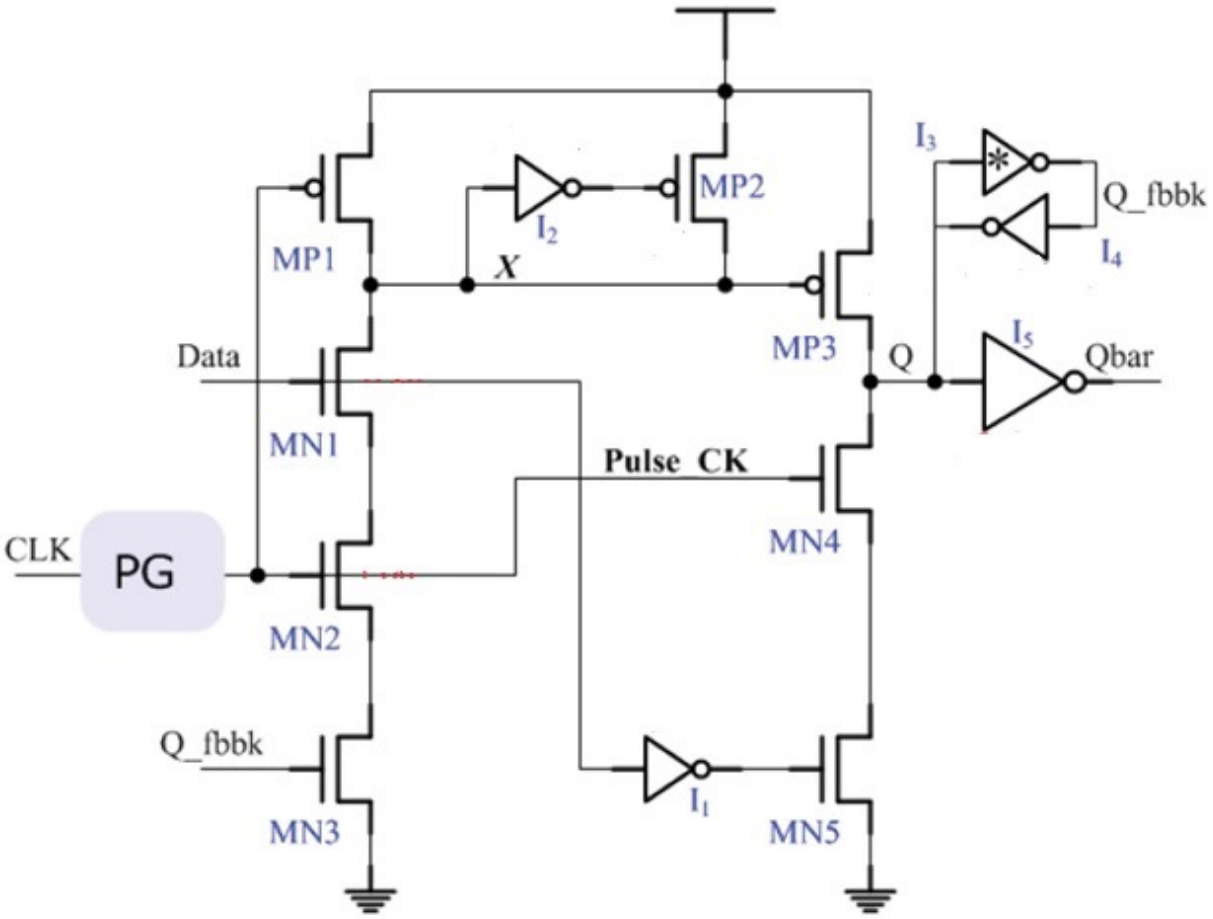

Figure 11 - circuit diagram of a CDFF

(3.2.2) Switching activity:

Simulations were performed for checking switching activity i.e. charging and discharging at node X and glitches at output Q. The simulation setting for clock and data input are listed in Table 2 where symbols have usual meaning. The power supply of 1.2 V is used and data input is tied at logic '1' i.e. 1.2V. The technology parameters of 90 nm PTM CMOS are used.

Table 2:

Clock and Input Pulse Parameters for CDFF

Parameters	CLK	Data
v_1	1.2v	1.2v
v_2	0v	0
per	2ns	4ns
t_d	0ns	0ns
t_r	1ps	1ps
t_f	1ps	1ps
pw	1ns	2ns
frequency	500MHz	250MHz

Figure 12 shows that Node X is not charged and discharged at every clock cycle and no glitches appear on the output node Q when the input data stays high. Hence this flip-flop has reduced switching activity at the output.

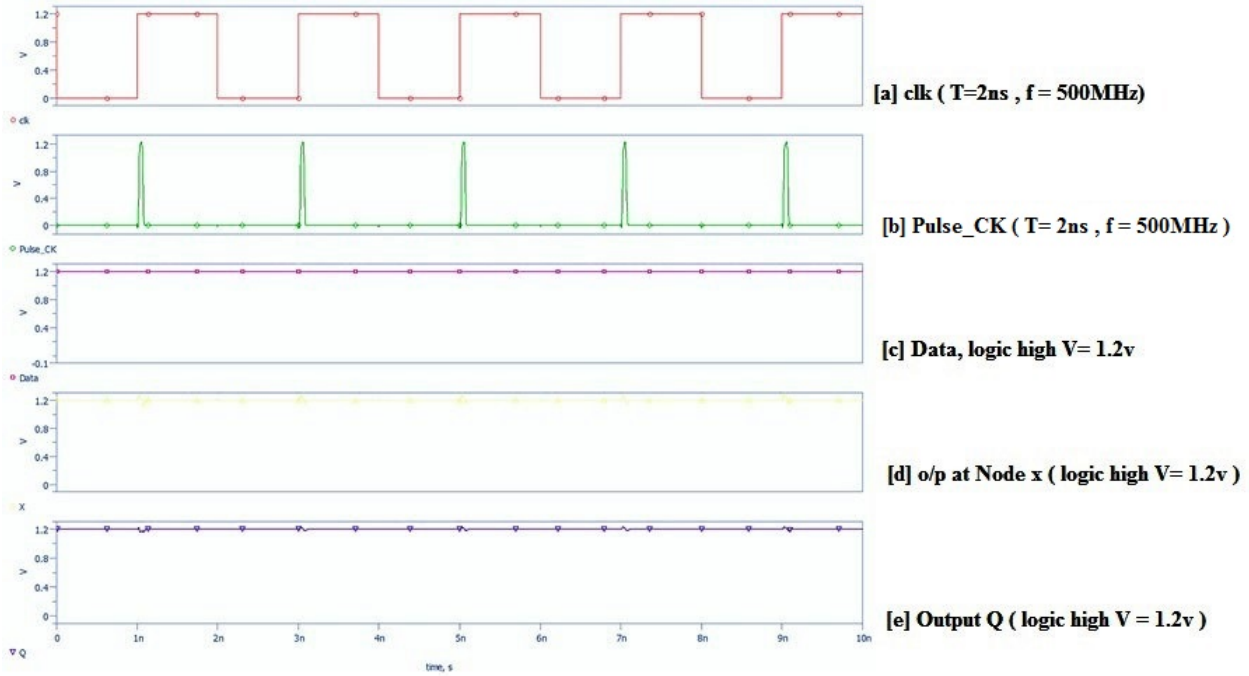

Figure 12 -Waveforms of CDFF showing NO charging and discharging at Node X & No glitches at output Q

(3.3) Static Conditional Discharge Flip-flop (SCDFF)

(3.3.1) Operation

The diagram of SCDFF is shown in Figure 13, in which the principal structure of SCDFF consist of two stages, through the elimination of pre-charge at node x SCDFF reduces activities of internal switching, and for reducing power dissipation it uses inverted output Q bar which acts as discharge control signal, it benefits to, in spite of input data activity, in terms of reducing the capacitive load (at node x) , node x lifts the capacitive load at node x, nodes x drives the MP2(pull transistor) only in the 2^{nd} stage at the sampling period ,that is the delay increases through the dual PG , transistor MN1 and MP4 turn on, which carry the i/p D to propagate to the o/p. The keepers (that is $I_2 – I_3$ and $I_4 –I_{5)}$ are employed for holding the o/p stages.as i/p D = high & Q = low (assume) at the sampling period, node x gets discharge by the pull down path (MN1, MN2 and MN3), when the transistor output will be pulled high by MP2 (pull transistor), in 2^{nd} stage node x stays low as D is high. during sampling period When input D = low during , node x is held at the pre-charge voltage ,MN5(pull down transistor) sees a high at the gate which is the internal signal D bar generated for the input D via an inverter MN5 transistor forms part of pull down section of the output Q, unlike CDFF, SCDFF doesn’t employ pre-charging at each clock cycle & SCDFF switching depends on data switching activity, in addition SCDFF is able to reduce the load on the dual PG o/p from 3 to 2 transistor per FFs (at MN1 & MP4).[here PG refers as pulse generator]

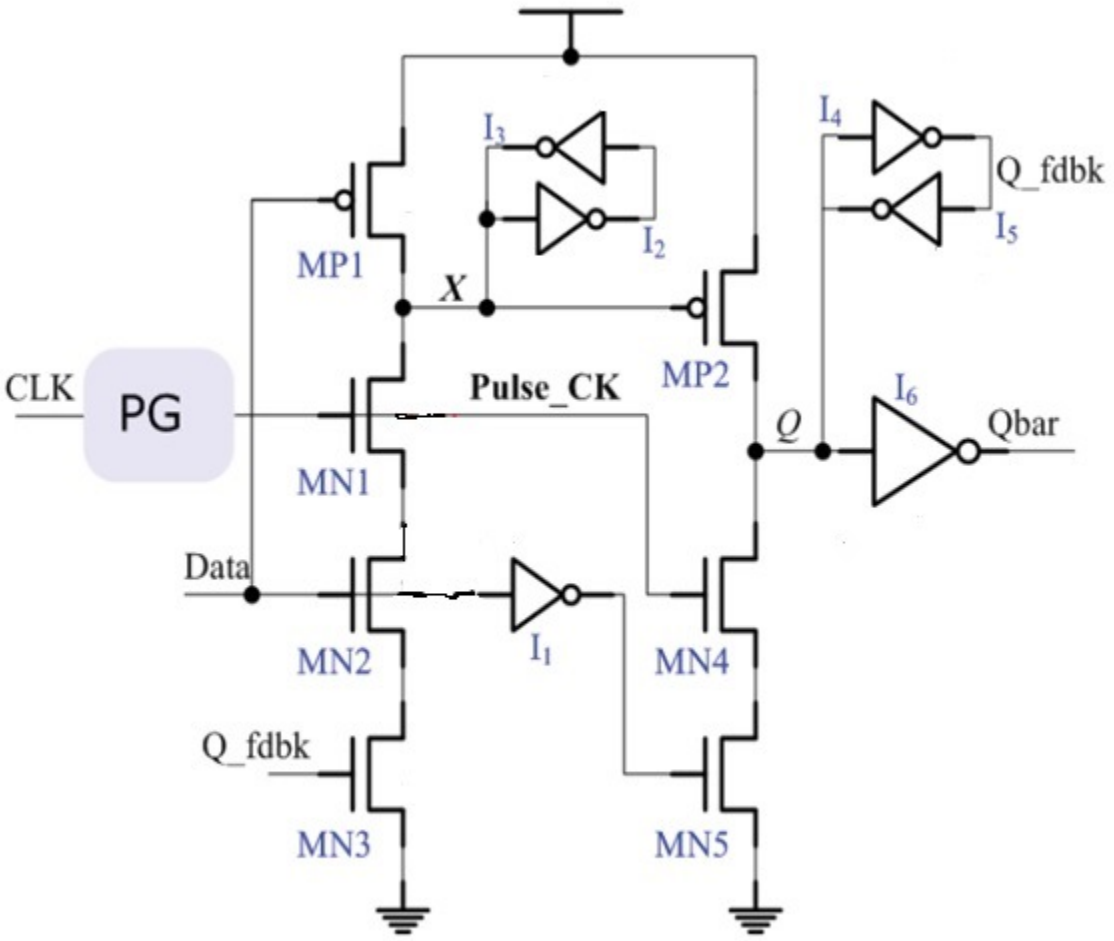

Figure 13 - Static CDFF schematic

(3.3.2) Switching activity:

Simulations were performed for checking switching activity i.e. charging and discharging at node X and glitches at output Q. The simulation setting for clock and data input are listed in Table 3 where symbols have usual meaning. The power supply of 1.2 V is used and data input is tied at logic '1' i.e. 1.2V. The technology parameters of 90 nm PTM CMOS are used.

Table 3:

Clock and Input Pulse Parameters for Static-CDFF

Parameters	CLK	Data
v_1	1.2v	1.2v
v_2	0v	0v
per	2ns	4ns
t_d	0ns	0ns
t_r	1ps	1ps
t_f	1ps	1ps
pw	1ns	2ns
frequency	500MHz	250MHz

Figure 14 shows the waveforms of Static-CDFF in which it displays the NO immediate pre-charging after discharge at node x and it basically reduces the internal switching activity by removing the pre-charging at node x, makes as use of the inverted output Q as a discharge control signal.

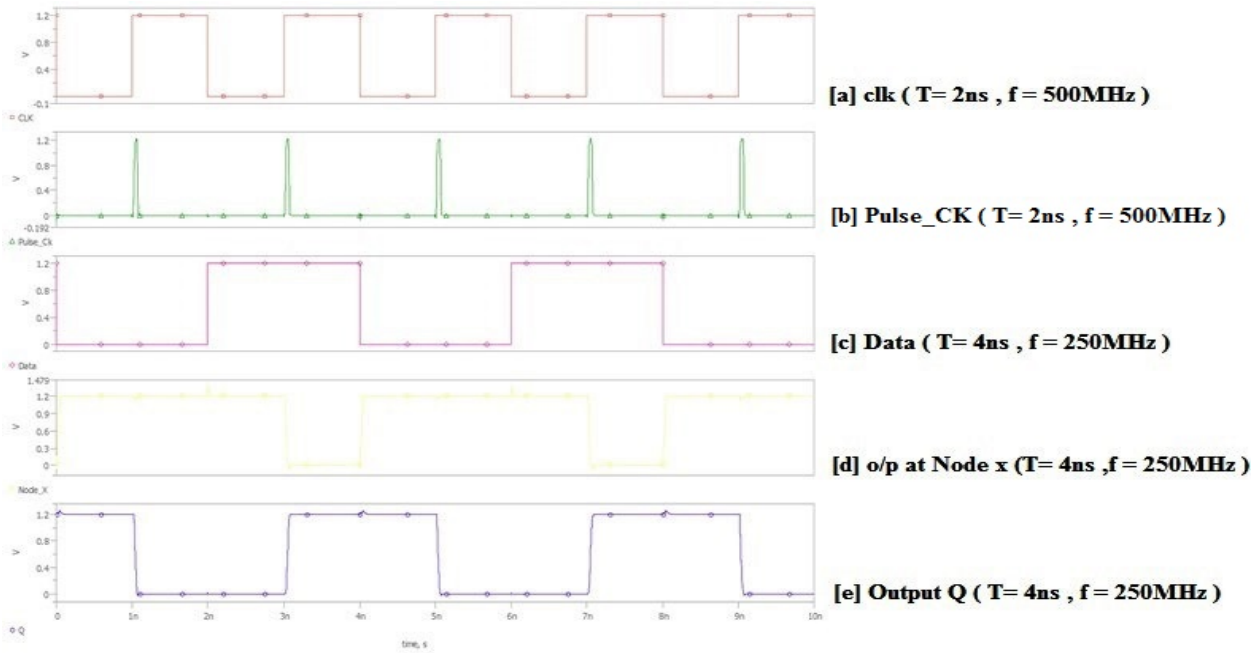

Figure 14 - Waveforms of SCDFF showing NO immediate pre-charging after discharge at Node X

Chapter 4

Evaluation of timing parameters of Conventional Pulsed triggered flip-flops

The timing parameters of conventional Pulsed triggered flip-flops are evaluated in this chapter. The definition of timing parameters is given first followed by simulation results for all three flip flops explained in Chapter 3.

4.1 Timing parameters: The timing parameters are described as follows:

1. Setup time: It is minimum time amount before the active of clock cycle during which the stability of data is must so that it can be correctly latched at output. In general each flip – flop needs a certain amount of time before the clock's active edge arrives during which data transition should not occur so that it can be captured reliably at the output.

The setup time violation occurs when the signal arrives late and misses the time it should have been arrived at.

The pictorial representation for set up time is given in Figure 15. There may be different setup time for different transition of data i.e. low to high or high to low. The setup time is maximum of these two and is expressed as

$$t_{setup} = \max (t_{setup\ LH} , t_{setup\ HL})$$

where,

$t_{setup\ LH}$ is setup time for low to high transition.

$t_{setup\ HL}$ is setup time for high to low transition.

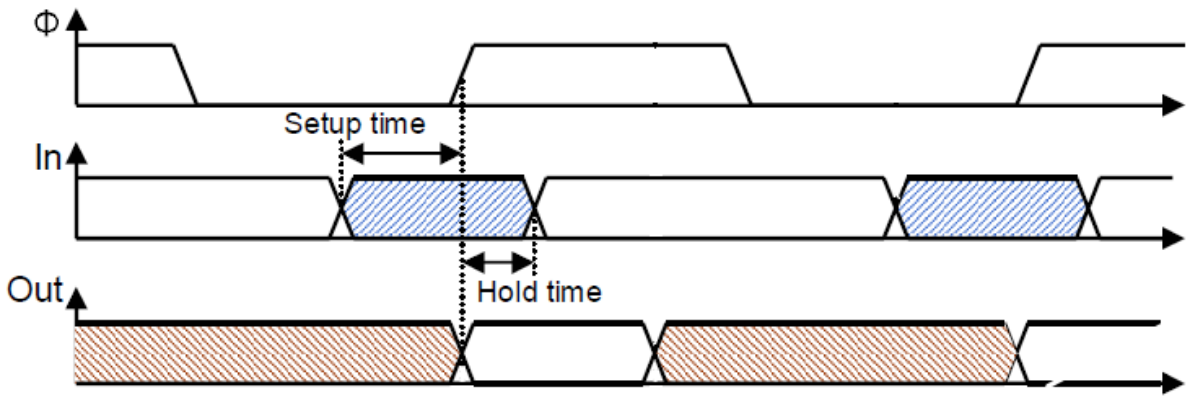

Figure 15 Waveforms depicting setup and hold time.

2. Hold time: It is the minimum time amount after the active edge of clock cycle during which the data must be stable in order to be captured reliably at output.

The hold time violation occurs when the input signal transition takes place too soon after arrival of clock active edge.

The pictorial representation for hold up time is given in Figure 15. Similar to the setup time hold time may differ for different transitions. Therefore

$$t_{hold} = \max(t_{hold\ LH} , t_{hold\ HL})$$

Where,

$t_{hold\ LH}$ is hold time for low to high transition.

$t_{hold\ HL}$ is hold time for high to low transition.

Φ is the clock signal in Figure 15.

3. Data to Q delay: In FF when an input is applied the amount of time it takes to produce the corresponding output is called as data to output delay. It is explained by Figure 16

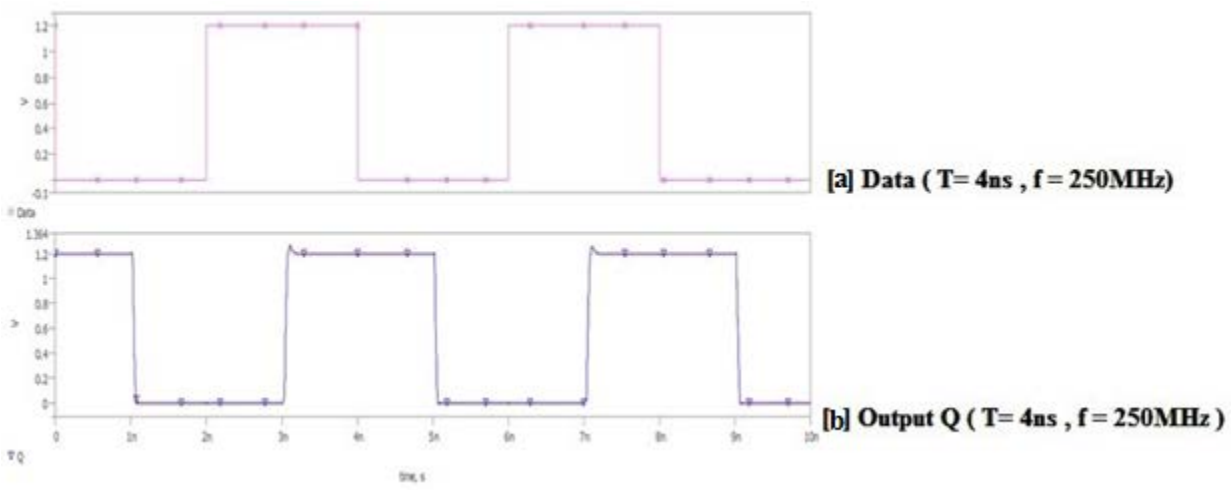

Figure 16 Input and output of a D flip – flop

In this Figure 16 we can see that at the first input data transition from 0 – 1 occurs at time instant of 2ns whereas in output it occurs at 3ns. So 1ns time duration is taken by the flip – flop to produce output for the corresponding input. Thus its D to Q delay is 1ns.

4.2 Evaluation of timing parameter of ep-DCO

1. Minimum D to Q delay: Figure 17 shows the simulated waveforms for calculation of Min. Data-Q delay of ep-DCO schematic. In this a pulse clock is applied at a certain point of time and then the point of time where data changes from low to high is made to reach as close as possible to the point of time of clock such that output Q correctly follows the data. Now by studying the graph time difference between Data and output Q is calculated, this is the min. D to Q delay. The calculated result of min. D to Q delay for ep-DCO is 25.5ns.

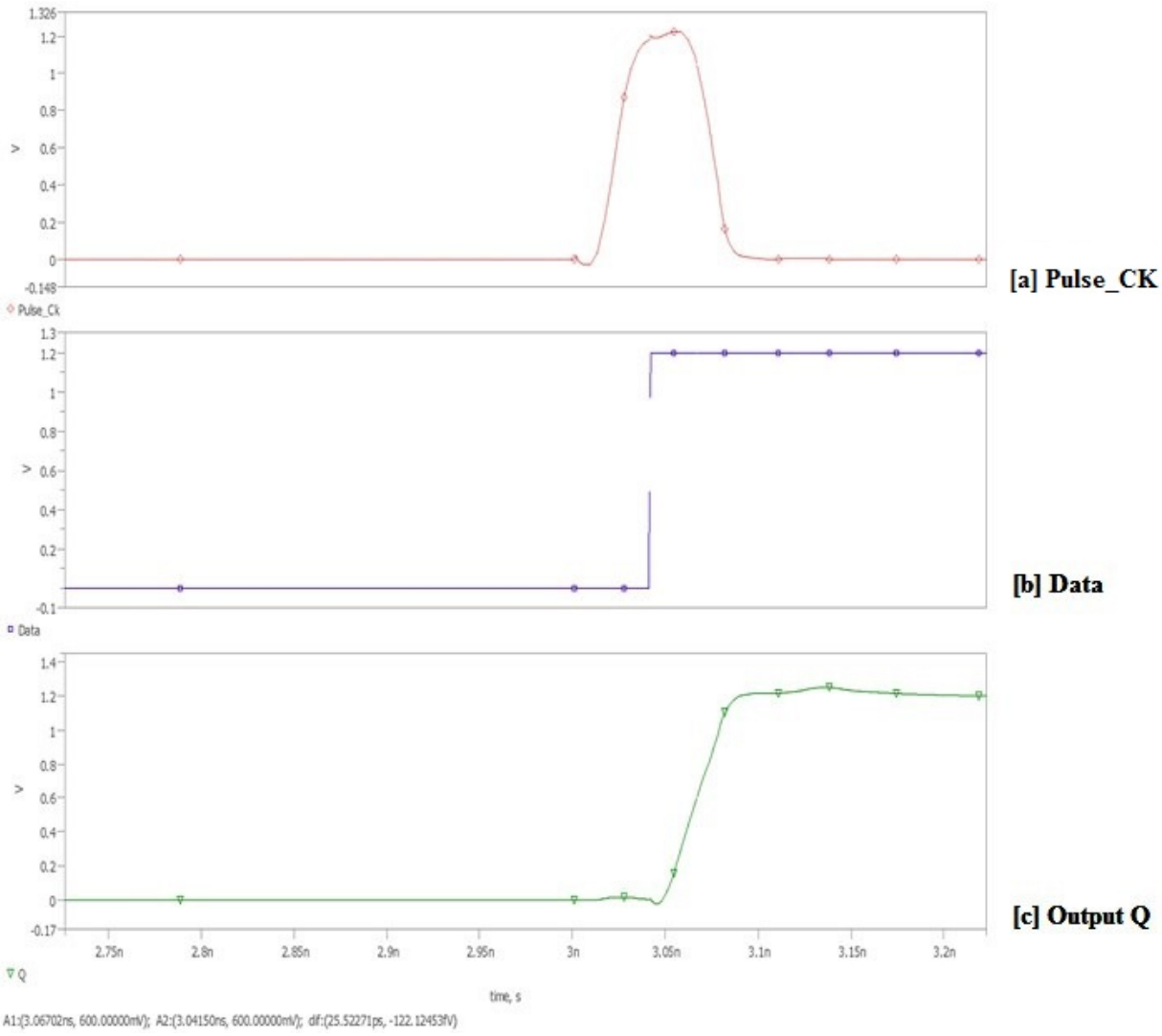

Figure 17 - Waveforms of ep-DCO for the calculation of Min Data-Q Delay

2. Setup time: Figure 18 shows the simulated waveforms for calculation of setup time. In this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. Figure 18[a] shows two graphs of data, for one graph the output follows the input correctly., while for other output doesn't follow input correctly , so the one with correct output is used to calculate the setup time ,Figure 18[a] shows two instant of data transition, Figure 18[b] shows the pulse clock , Figure 18[c] shows the two output one of which is correct while other is false, Figure 18[d] shows the same graph of Figure 18[a] for which output is correct , Figure 18[e] is same clock pulse as shown in Figure 18[b], Figure 18[f] shows the output for input shown in Figure 18[d]. Now by studying the graph of Figure 18[d] and Figure 18[e] setup time is calculated and it is mentioned in table [5], for ep-DCO the calculated setup time is -36.9ns.

3. Hold time: Figure 19 shows the simulated waveforms for calculation of hold time. In this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. Figure 19[a] shows two graphs of data, for one graph the output follows the input correctly, while for other input doesn't follow output correctly so the one with correct output is used to calculate the hold time ,Figure 19[a] shows two instant of data transition, Figure 19[b] shows the pulse clock . Figure 19[c] shows two outputs one of which is correct while other is false, Figure 19[d] shows the same graph of Figure 19[a] for which output is correct, Figure 19[e] is same clock pulse as shown in Figure 19[b], Figure 19[f] shows the output for input shown in Figure 19[d]. Now by studying the graph of Figure19 [d] and Figure 19[e] hold time is calculated and it is mentioned in table [5], for ep-DCO the calculated hold time is 14.1ns.

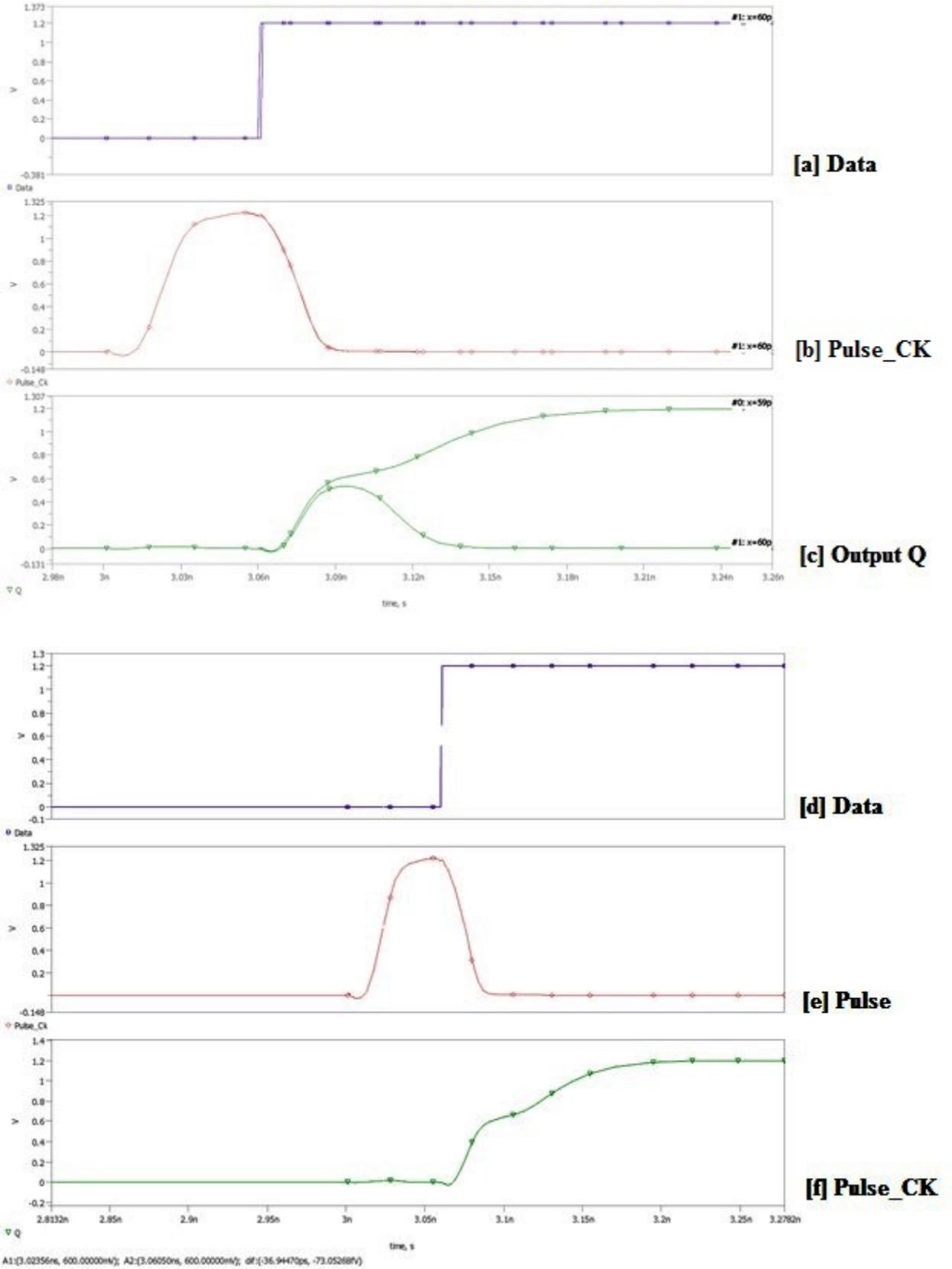

Figure 18 - Waveforms of ep-DCO for the calculation of Setup time.

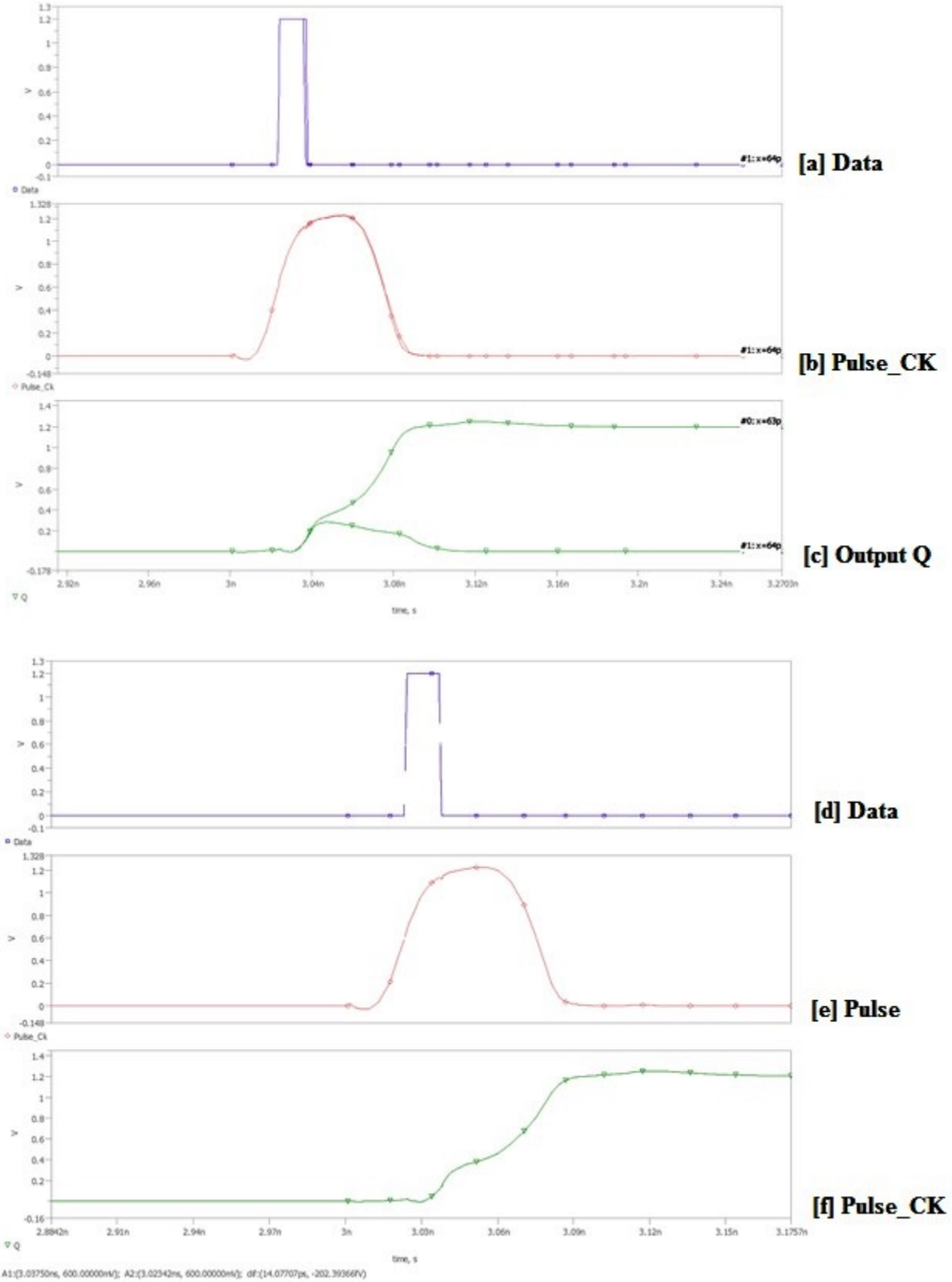

Figure 19 - Waveforms of ep-DCO for the calculation of Hold time

4.3 Evaluation of timing parameter of CDFF

1. Minimum D to Q delay: Figure 20 shows the simulated waveforms for the calculation of Min Data-Q delay of CDFF circuit. In this a pulse clock is applied at a certain point of time and then the point of time where data changes from low to high is made to reach as close as possible to the point of time of clock such that output Q correctly follows the data. Now by studying the graph time difference between Data and output Q is calculated, this is the min. D to Q delay. The calculated result of min. D to Q delay for CDFF is 24.4ns.

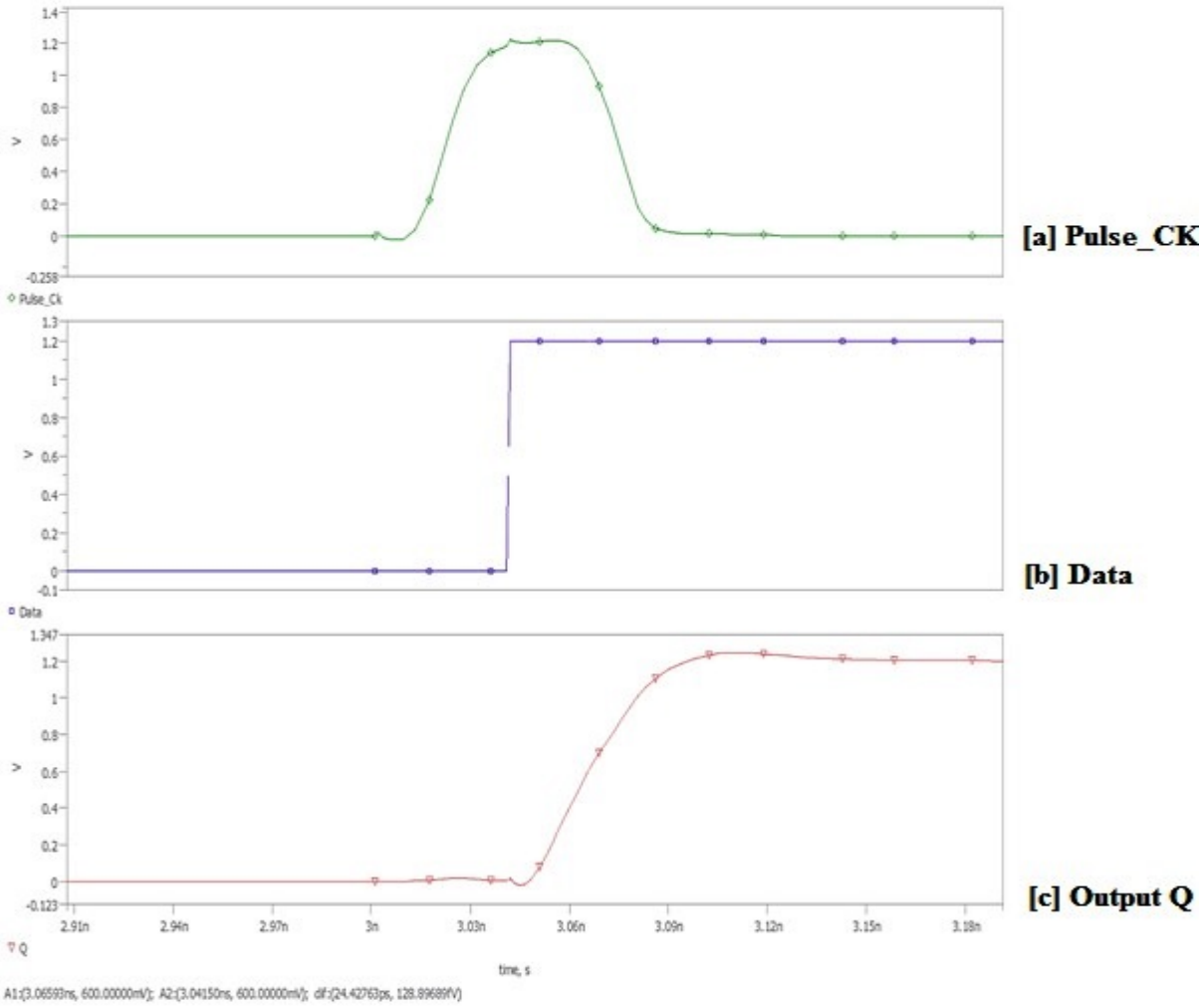

Figure 20 - Waveforms of CDFF for the calculation of Min Data-Q Delay

2. Setup time: Figure 21 shows the simulated waveforms for the calculation of setup time. In this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. Figure 21[a] shows two graphs of data, for one graph the output follows the input correctly., while for other output doesn't follow input correctly , so the one with correct output is used to calculate the setup time ,Figure 21[a] shows two instant of data transition, Figure 21[b] shows the pulse clock , Figure 21[c] shows the two output one of which is correct while other is false, Figure 21[d] shows the same graph of Figure 21[a] for which output is correct , Figure 21[e] is same clock pulse as shown in Figure 21[b], Figure 21[f] shows the output for input shown in Figure 21[d]. Now by studying the graph of Figure21[d] and Figure 21[e] setup time is calculated and for CDFF the calculated setup time is -32.3ns.

3. Hold time: Figure 22 shows the simulated waveforms for the calculation of Hold time. In this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. Figure 22[a] shows two graphs of data, for one graph the output follows the input correctly, while for other input doesn't follow output correctly so the one with correct output is used to calculate the hold time ,Figure 22[a] shows two instant of data transition, Figure 22[b] shows the pulse clock . Figure 22[c] shows two output one of which is correct while other is false, Figure 22[d] shows the same graph of Figure 22[a] for which output is correct , Figure 22[e] is same clock pulse as shown in Figure 22[b], Figure 22[f] shows the output for input shown in Figure 22[d]. Now by studying the graph of Figure22[d] and Figure 22[e] hold time is calculated which is 18.6 ns.

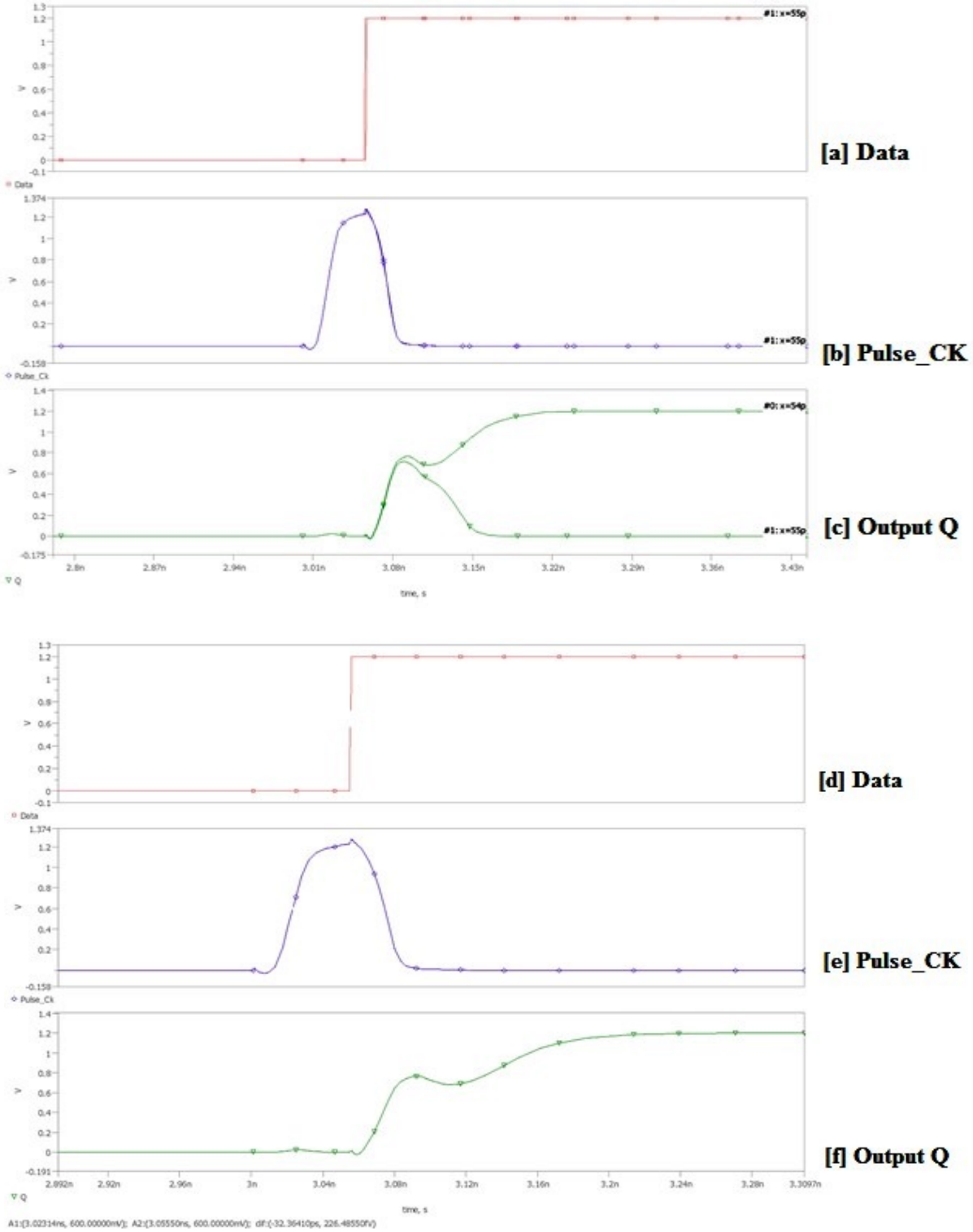

Figure 21 - Waveforms of CDFF for the calculation of Setup time

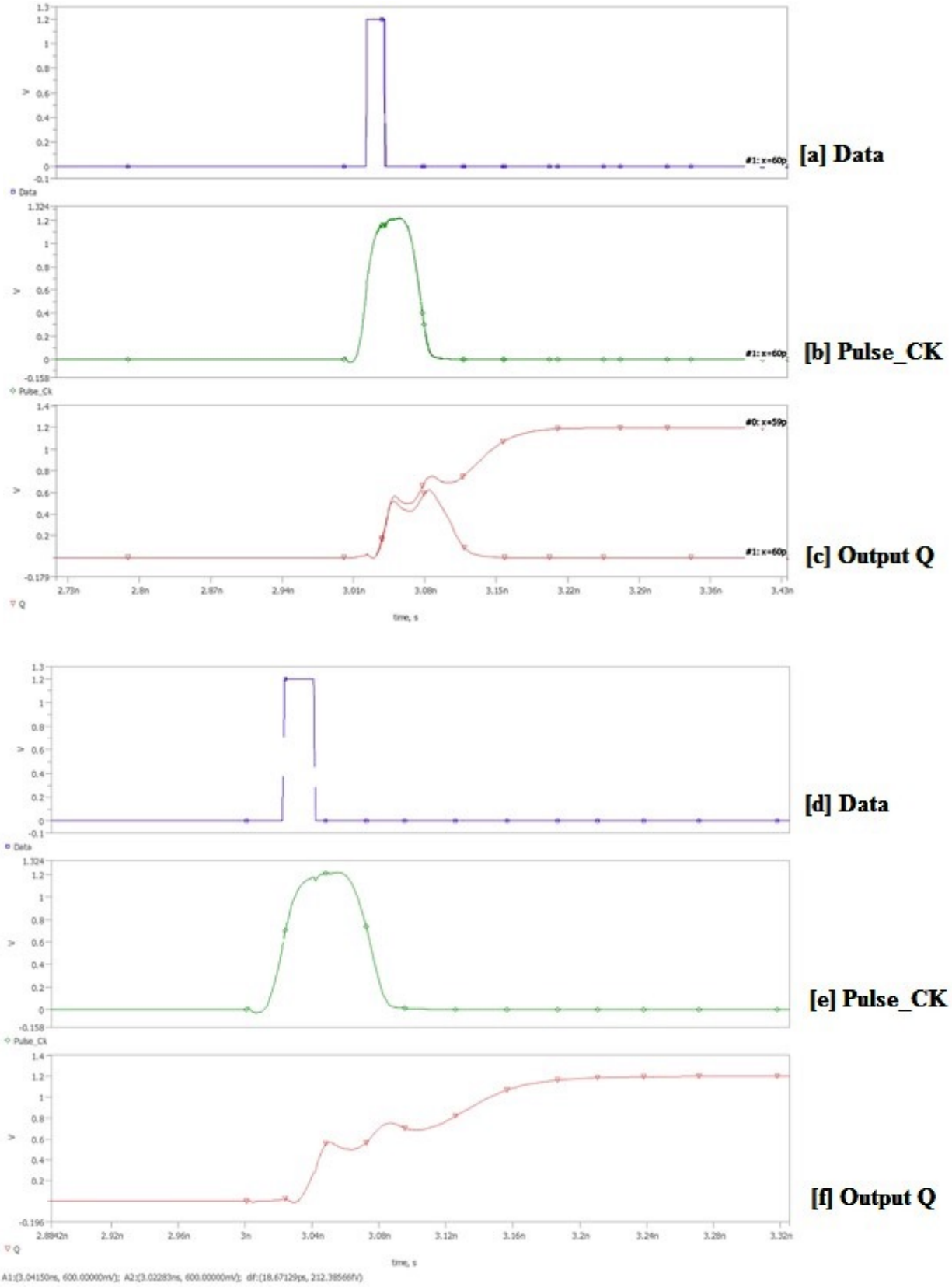

Figure 22 - Waveforms of CDFF for the calculation of Hold time

4.4 Evaluation of timing parameter of SCDFF

1. Minimum D to Q delay: Figure 23 shows the simulated waveforms for the calculation of Min Data-Q delay of SCDFF. In this a pulse clock is applied at a certain point of time and then the point of time where data changes from low to high is made to reach as close as possible to the point of time of clock such that output Q correctly follows the data. Now by studying the graph time difference between Data and output Q is calculated, this is the min. D to Q delay. The calculated result of min. D to Q delay for SCDFF is 27.7ns.

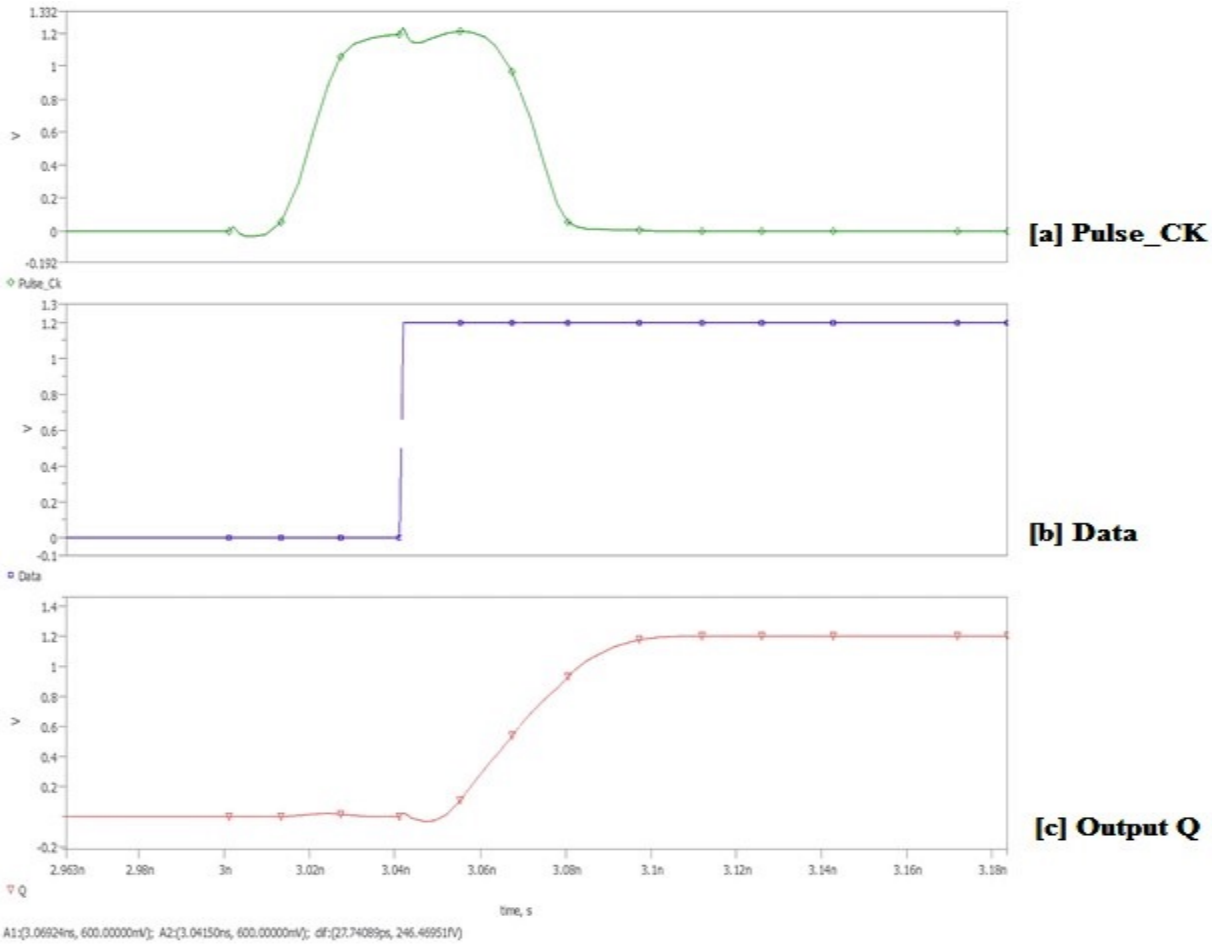

Figure 23 -Waveforms of SCDFF for the calculation of Min Data-Q Delay

2. Setup time: Figure 24 shows the simulated waveforms for the calculation of setup time. In this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. Figure 24[a] shows two graphs of data, for one graph the output follows the input correctly., while for other output doesn't follow input correctly , so the one with correct output is used to calculate the setup time ,Figure 24[a] shows two instant of data transition, Figure 24[b] shows the pulse clock , Figure 24[c] shows the two output one of which is correct while other is false, Figure 24[d] shows the same graph of Figure 24[a] for which output is correct , Figure 24[e] is same clock pulse as shown in Figure 24[b], Figure 24[f] shows the output for input shown in Figure 24[d]. Now by studying the graph of Figure 24[d] and Figure 24[e] setup time is calculated thus for Static-CDFF the calculated setup time is -34.5ns.

3. Hold time: figure 25 shows the simulated waveforms for the calculation of Hold time. In this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. figure 25[a] shows two graphs of data, for one graph the output follows the input correctly, while for other input doesn't follow output correctly so the one with correct output is used to calculate the hold time ,figure 25[a] shows two instant of data transition, figure 25[b] shows the pulse clock . figure 25[c] shows two output one of which is correct while other is false, figure 25[d] shows the same graph of figure 25[a] for which output is correct , figure 25[e] is same clock pulse as shown in figure 25[b], figure 25[f] shows the output for input shown in figure 25[d]. Now by studying the graph of figure 25[d] and figure 25[e] hold time is calculated thus for SCDFF the calculated hold time is 28.6ns.

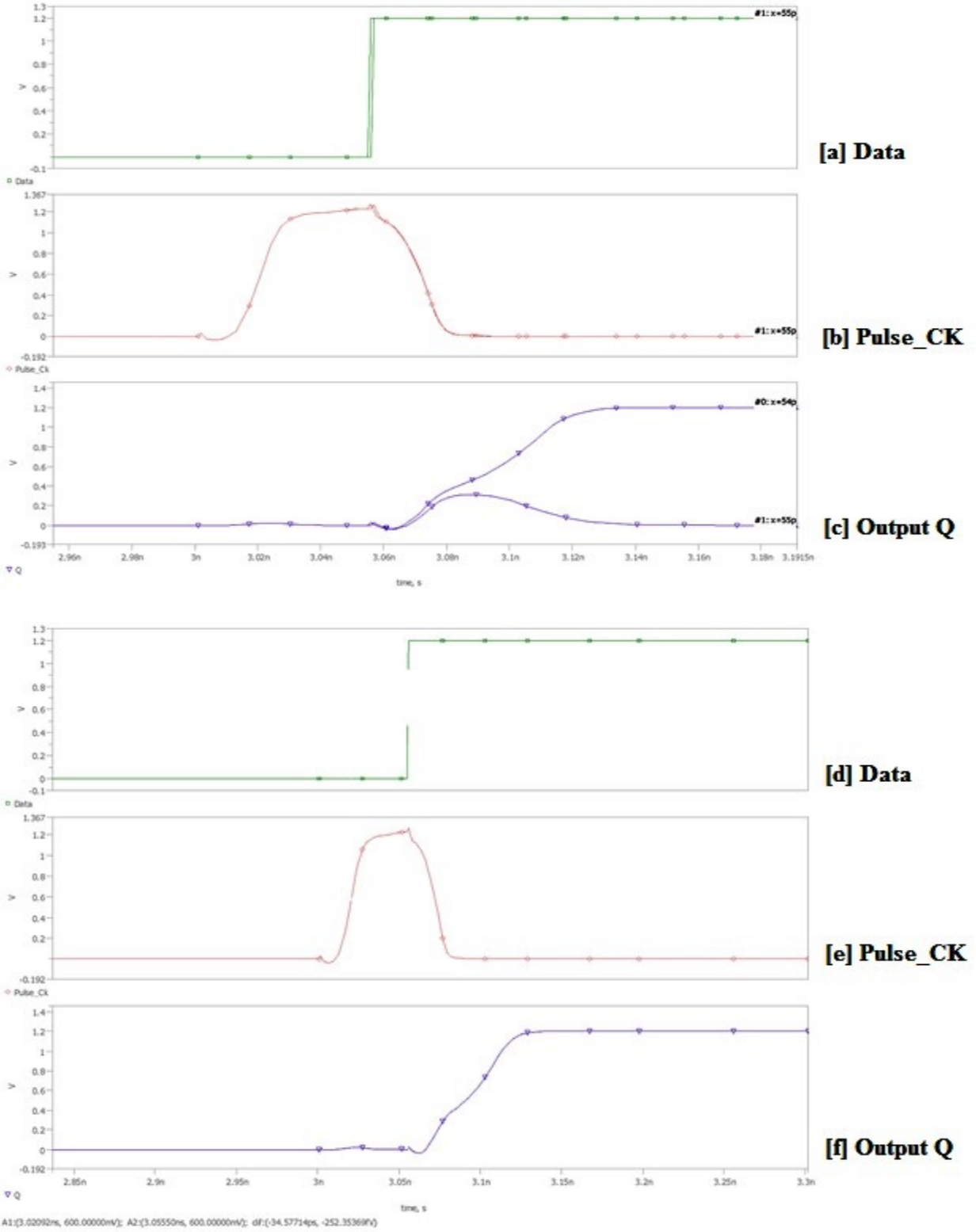

Figure 24 - Waveforms of SCDFF for the calculation of Setup time

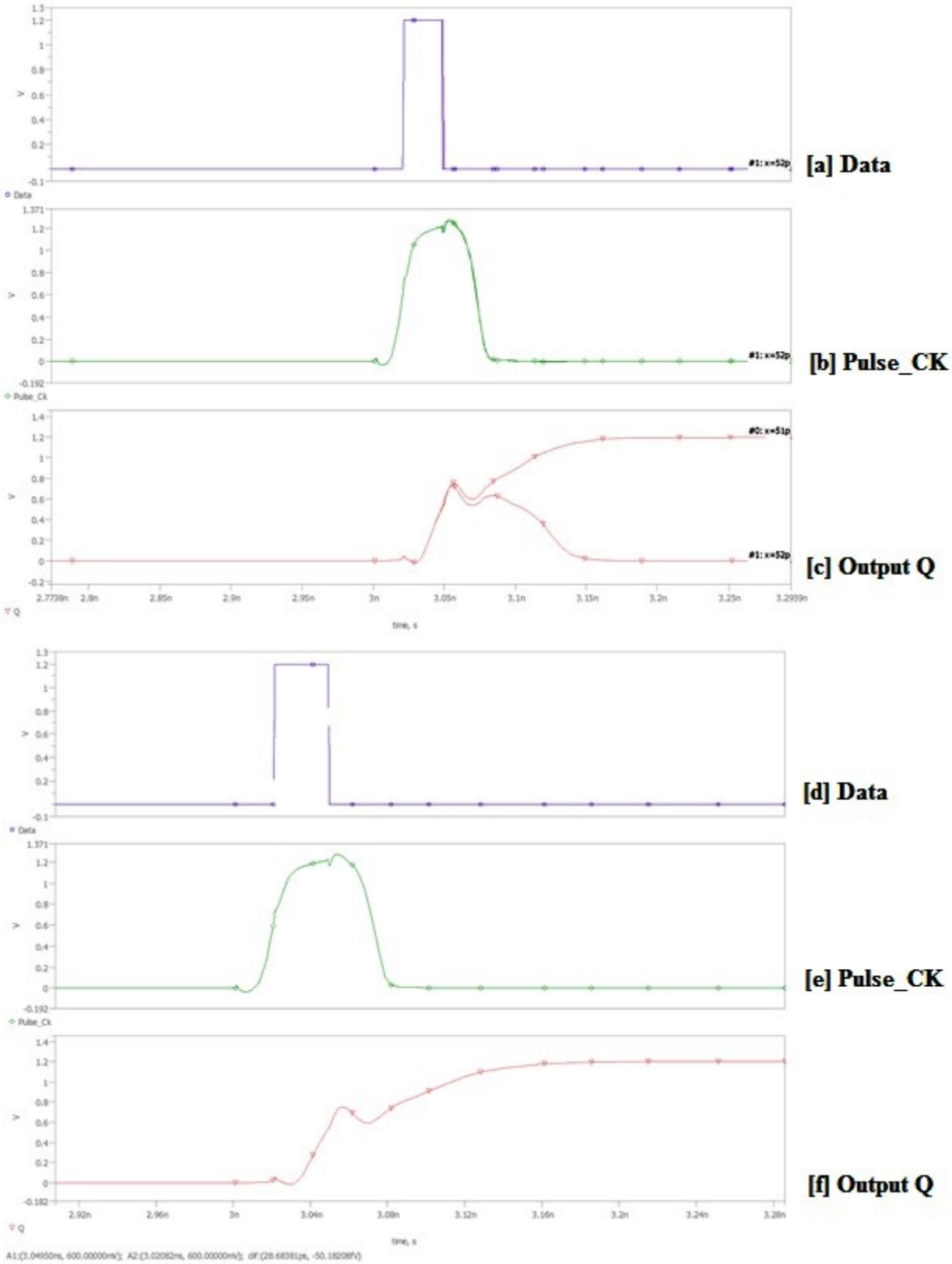

Figure 25 - Waveforms of SCDFF for the calculation of Hold time

4.5 Comparison between three conventional pulsed triggered flip-flops.

The timing parameters of conventional pulse triggered flip-flops given in Chapter 4 are summarized in Table 4.

Table 4:

Timing parameter comparison of conventional PFFs

Parameter	Ep-DCO	CDFF	SCDFF
Setup Time(ns)	-36.9	-32.3	-34.5
Hold Time(ns)	14.1	18.6	28.6
Min Data-Q Delay(ns)	25.5	24.4	27.7

Thus from Table 4 we have following conclusions:

1. The setup time is best for Ep-DCO among the three flip-flops.

2. The hold time is maximum for SCDFF and minimum for Ep-DCO. Thus Ep-DCO is superior among the three flip-flops in terms of hold time.

3. The maximum D – Q delay is for SCDFF and minimum for CDFF. Thus CDFF is the best among the three flip- flops in terms of delay.

Chapter -5

SIGNAL FEED-THROUGH P-FF (SFTFF)

Conventional explicit pulsed triggered flip flop circuits are explained in Chapter 3 and their timing parameters are studied through simulation in Chapter 4. These P-FFs suffer from worst case timing problems, when data transition takes place from 'zero' to 'one'. The signal feed through technique used in SFTFF results in improved delay. Further, in order to avoid the unnecessary switching at the internal node the SFTFF design uses conditional discharging technique and latch structure (static) in a similar way as used by the SCDFF design.

This chapter details the operation of SFTFF and simulation results for its timing parameters.

5.1 Operation of SFTFF

The schematic of SFTFF is depicted in Figure 26. As the clock pulses reaches, let occurs no transition of data that is the node Q as well as input data are present at the same level, on current passing by pass transistor (MN_X) in which it keeps the input stage of flip flop in respect of any driving effort. During same time, the i/p data & o/p feedback Q_fdbk assuming signal levels are complementary and at node x pull down path if off. Hence in internal node no signal switching happens. On other side, as occurring of zero to one data transition happens, the node x gets discharged to turn on transistor (MP2), and next pulls the node Q to high. As pointing to the CDFF circuit, it corresponds to worst case timing of the flip flop operations since the discharge path conduct for duration of pulse, since through the technique of signal feedthrough , a boost can get through i/p source via MN_X(pass transistor) and delay can be shorten.as it seems laden the i/p source along the responsibility of charging or discharging., it a common hidden danger of every pass transistor logic, in this case scenario is different due to that for short period MN_X conducts only, as pointing to the static CDFF circuit, as during one to zero data transition happens, the MN_X gets turn on through clock pulse plus node Q gets discharge through the input

stage by this route, as the other case of zero to one data transition, the i/p source bears the sole discharge responsibility. MN_X gets turn on for short time slot, loading effect to i/p source is not important. particularly discharge is not similar to critical path delay and suggest no transistor sizing pull to raise the speed, other as keeper logic is placed at node Q, discharging duty of i/p source hike once keeper logic state gets inverted.

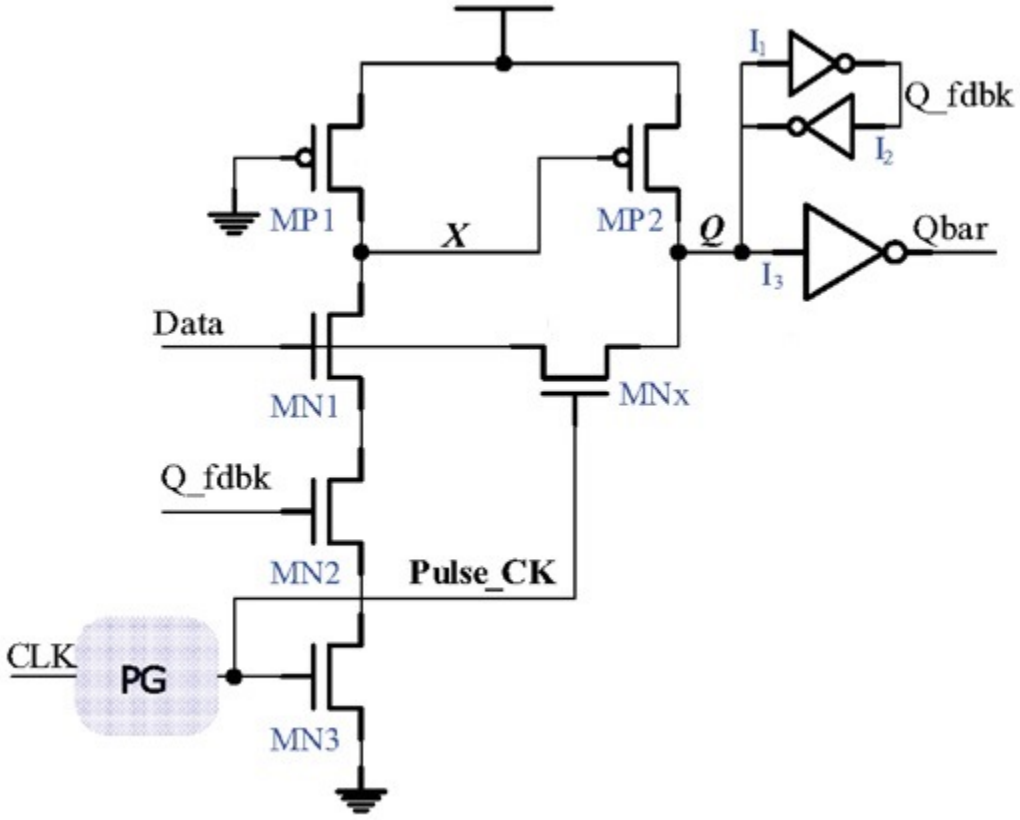

Figure 26- Schematic of SFTFF

It may be noted that there are three major features of SFTFF which makes it much different from the conventional one. These are

1. The TSPC latch in its first state uses a pull up PMOS (weak) transistor named as MP1.gate of this MP1 is connected to ground, it leads to logic style design-pseudo NMOS and for the node x, the charge keeper circuitry can be saved. It makes circuit simpler and the capacitance at node x is also reduced. [as circuit given in Figure 26]

2. The pulse clock controlled pass transistor (MN_X) is employed. It makes the node Q of the latch to be derived directly by the input data in order to facilitate the auxiliary signal driven from input source to Q node, an MP_X pull up transistor is employed in 2^{nd} stage inverter. The delay of data transition can be reduced by quickly pulling up the node level. [as circuit given in Figure 26]

3. There is no pull down network of the 2^{nd} stage inverter, it is removed completely here the discharging path is provided by the pass transition (MN_X). Thus MN_X has two roles.

    - When data transition occurs from ‘zero’ to ‘one’, the extra driving at output node Q is given by MN_X
    - When data transition occurs from ‘one’ to ‘zero’, MN_X provides charging of node Q [as circuit given in figure 26]

In comparison with the SCDFF design, the SFTFF circuit design has one charge keeper which is two inverter, one 2 NMOS transistor pull down network and one control inverter. The pass transistor (NMOS) is the only component extra which supports feed through of signal, thus the delay of 0 to 1 transition is actually improved by SFTFF technique, thus the difference between rise and fall time is reduced. Thus this SFTFF design as comparison to the conventional design gives the most balanced behavior in terms of delay.

Advantages of SFTFF over conventional explicit pulse triggered flip flops

1. As in explicit pulse triggered flip flop design more power is consumed so conventional explicit pulse triggered flip flop is less power economical, where as in SFTFF power consumption is less so, it is more power economical.

2. Since in conventional explicit pulse triggered flip flop there is a long discharging path problems thus speed is less and timing characteristics are poor, but in SFTFF design it overcomes the long discharging path problems thus improves the speed and performance.

3. SFTFF design is a lower power pulse triggered flip flop which employs signal feed through technique and it consist of pass transistor and pseudo NMOS logic, it manages to reduce delay in latching the data 'one' and 'zero', it also reduced longer delay through feeding the input signal directly to an internal node of the latch design that fasten the data transition hence SFTFF design performs better than the conventional pulse triggered flip flop design in terms of data to Q delay. Where as in conventional pulse triggered flip flop design having the longer delay so it doesn't perform better.

5.2 Timing parameters of SFTFF

The Signal pulsed triggered flip flop's operation is studied and timing parameters are evaluated through SPICE simulations on Symica DE. Timing parameters are also compared with conventional Pulsed triggered flip-flop designs through The technology used in simulation is the PTM BSIM4 90nm CMOS process. The power supply of 1.2 V is used.

The working of SFTFF is shown in Figure 27 Following inputs are applied: Clock with time period of 2ns and frequency of 500MHz, which generates a pulse clock of same frequency that is

500MHz and the time period of 2ns but it has smaller width of high logic level. Data applied is a clock signal frequency of 250MHz and the time period of 4ns, the output is produced by the circuit which is same as data applied along with a delay.

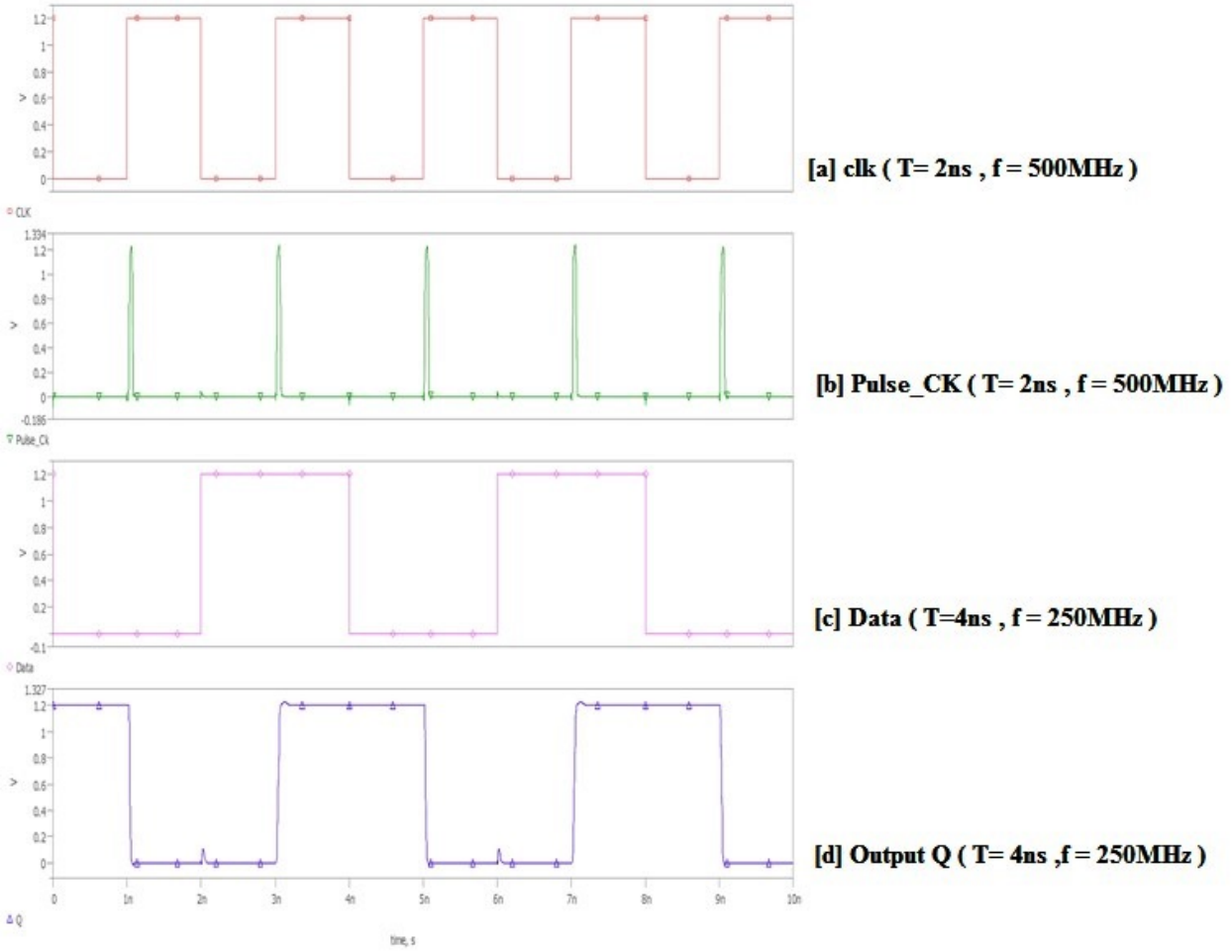

Figure 27 - Waveforms depicting the working of SFTFF

Simulation waveforms of Figures 28 -30 show the calculation of Min. D to Q delay, setup time and hold time respectively.

Figure no. 28 shows the simulated waveforms for the calculation of Min Data-Q delay of SFTFF schematic.in which a pulse clock is applied at a certain point of time and then the point of time

where data changes from low to high is made to reach as close as possible to the point of time of clock such that output Q correctly follows the data. Now by studying the graph time difference between Data and output Q is calculated, this is the min. D to Q delay. The calculated result of min. D to Q delay for SFTFF is 15.32ns.

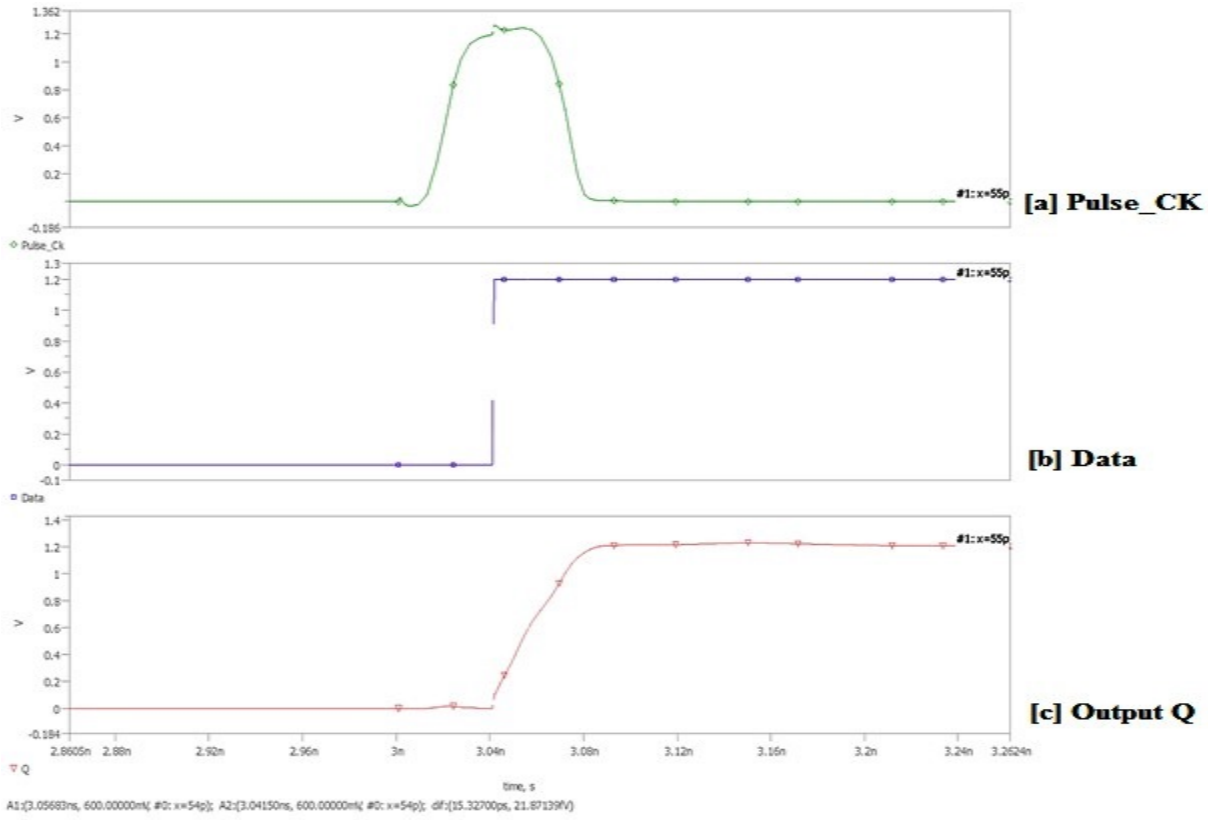

Figure 28 - Waveforms of SFTFF for the calculation of Min Data-Q Delay

.Figure 29 explains about the simulated waveforms of SFTFF for the calculation of setup time, in this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. Figure 29[a] shows two graphs of data, for one graph the output follows the input correctly., while for other output doesn't follow input correctly , so the one with correct output is used to calculate the setup time ,Figure 29[a] shows two instant of data transition, Figure 29[b] shows the pulse clock ,Figure 29[c] shows the two output one of which is correct while other is false, Figure 29[d] shows the same graph of Figure 29[a] for which output is correct ,Figure 29[e] is

same clock pulse as shown in Figure 29[b], Figure 29[f] shows the output for input shown in Figure 29[d]. Now by studying the graph of Figure 29[d] and Figure 29[e] setup time is calculated and for SFTFF the calculated setup time is -43.8ns.

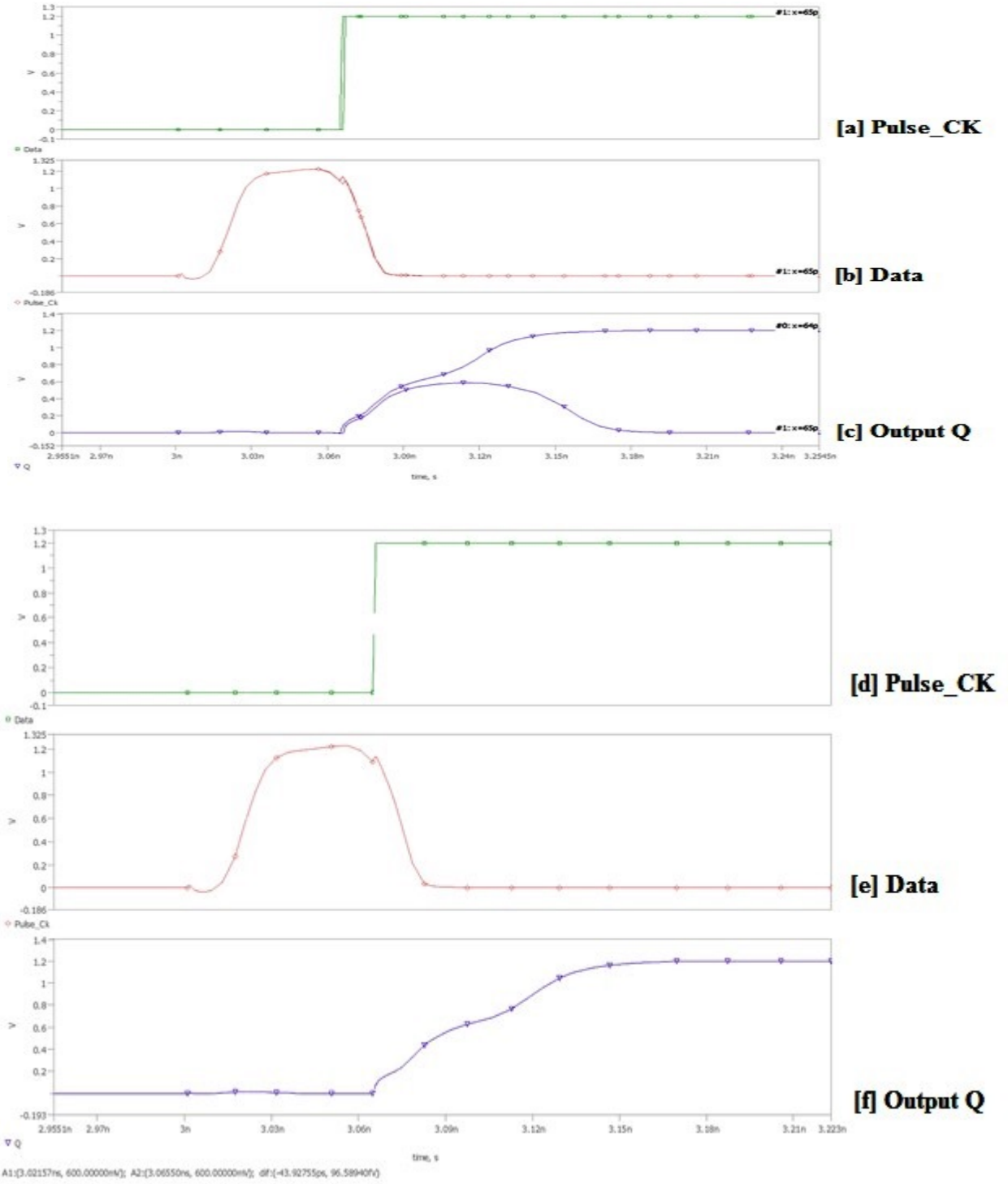

Figure 29 - Waveforms of SFTFF for the calculation of Setup time

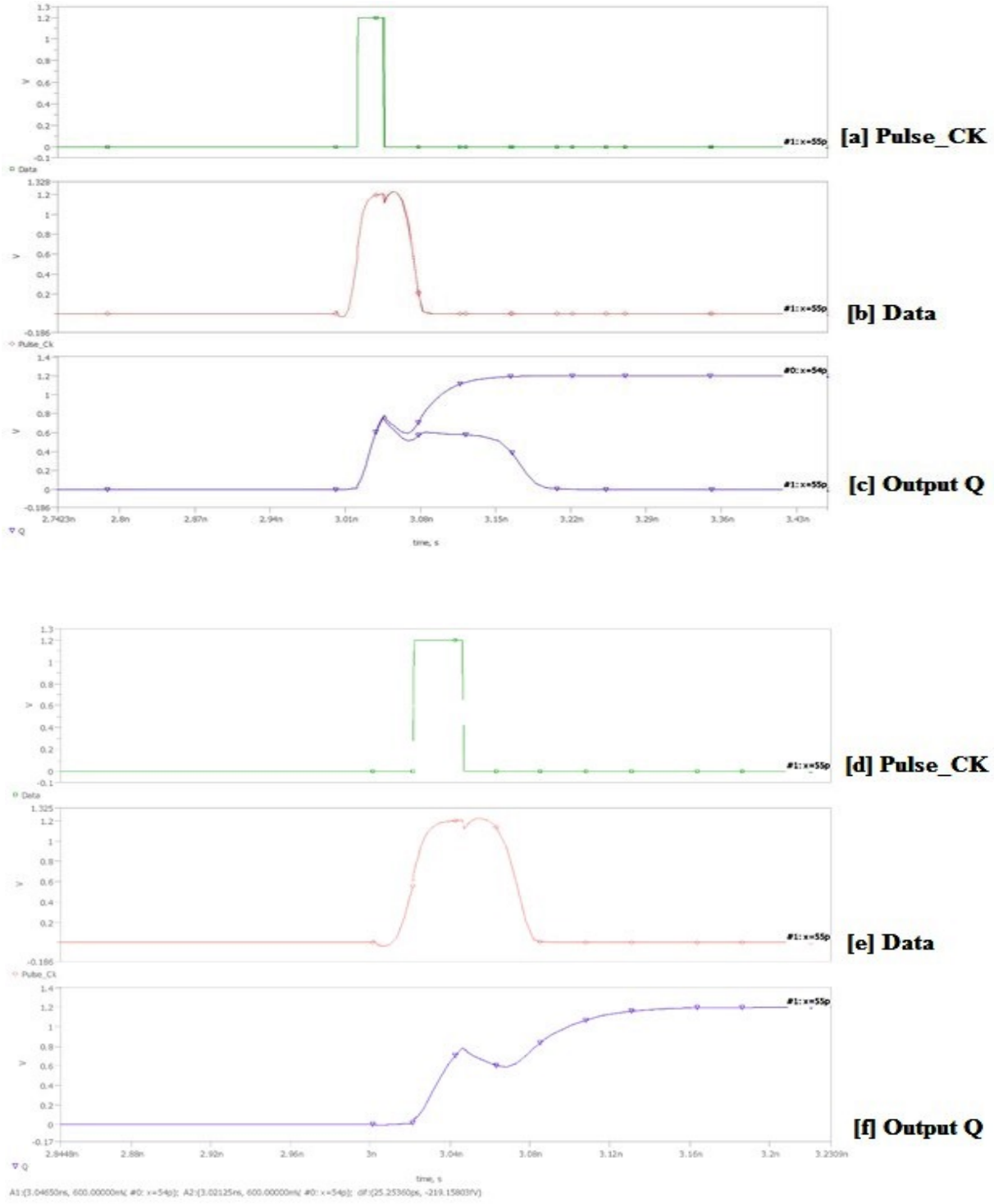

Figure 30 - Waveforms of SFTFF for the calculation of Hold time

Figure no. 30 explains about the simulated waveforms of SFTFF for the calculation of Hold time, in this clock is kept fixed and the data is shifted. The time instant at which data transition takes place is made to reach as close as possible to the clock till the output follows input correctly. Figure 30[a] shows two graphs of data, for one graph the output follows the input correctly, while for other input doesn't follow output correctly so the one with correct output is used to calculate the hold time ,Figure 30[a] shows two instant of data transition, Figure 30[b] shows the pulse clock. Figure 30[c] shows two outputs one of which is correct while other is false; Figure 30[d] shows the same graph of Figure 30[a] for which output is correct, Figure 30[e] is same clock pulse as shown in Figure 30[b], Figure 30[f] shows the output for input shown in figure 30[d]. Now by studying the graph of Figure 30[d] and Figure 30[e] hold time is calculated and for SFTFF the calculated hold time is 25.2ns.

5.3 Comparison of Timing parameters

The timing parameters of SFTFF and the one given in Chapter 4 are summarized in Table 5.

Table 5:

FEATURE COMPARISION OF VARIOUS FF DESIGN

Parameter	Ep-DCO	CDFF	SCDFF	SFTFF
Setup Time(ns)	-36.9	-32.3	-34.5	-43.8
Hold Time(ns)	14.1	18.6	28.6	25.2
Min Data-Q Delay(ns)	25.5	24.4	27.7	15.32

It is clear from Table 5 that the simulation and evaluated results of pulse triggered flip-flop designs such as ep-DCO, CDFF, SCDFF and SFTFF etc. in consideration of data to Q delay SFTFF and CDFF have the smallest delay. In comparison between SCDFF and CDFF, SCDFF exhibits the longer D to Q delay than the CDFF. Among these four low power pulse triggered flip flops, the SFTFF design exhibits the most balanced behavior in terms of delay.

Chapter 6

CONCLUSION AND FUTURE SCOPE

In this work, conventional explicit type P-FFs (ep-DCO, CDFF and SCDFF) and the particular Pulsed triggered-FF design by means of assigning a improved TSPC latch structure assimilating a hybrid design style be composed of a pass transistor and also a pseudo-nMOS logic (SFTFF) were studied and simulated prior to assimilate their performances. Simulation results shows that SFTFF gives minimum Data-Q delay among all other conventional FFs. The preeminent thoughts were to deliver a signal feedthrough from input source to the internal node of the latch, which desire to make more driving to make shorter the transition time later on heighten the power performance as well as speed performance. The design was skillfully accomplished through the use of a convenient pass transistor. Future work will include other methods to reduce power consumption and improve performance of FFs by reducing Data-Q delay.

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