VOLTAGE DIFFERENCING CURRENT CONVEYOR (VDCC) AND ITS APPLICATIONS

Dissertation submitted in
Partial fulfilment of the requirement
For the award of the degree of

Master of Technology
in
VLSI and Embedded System Design
by

TARUN TAMRAKAR

University Roll No. 2K15/VLS/18

Under the guidance of

Mr. A. K. SINGH
Associate Professor,
Electronics and Communication Engineering Department, DTU

2015-2017

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT
DELHI TECHNOLOGICAL UNIVERSITY
DELHI-110042, INDIA

Electronics and Communication Engineering Department

Delhi Technological University

Delhi-110042

www.dce.edu

CERTIFICATE

This is to certify that the dissertation titled "**VOLTAGE DIFFERENCING CURRENT CONVEYOR AND ITS APPLICATIONS**" is a bona-fide record of work done by **TARUN TAMRAKAR, Roll No. 2K15/VLS/18** at **Delhi Technological University** for partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI and Embedded systems Engineering. This project was carried out under my supervision and has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

Date: _____

(Mr. A. K. SINGH)
Associate Professor
Department of Electronics and Communication Engineering
Delhi Technological University

DECLARATION

I hereby declare that the project entitled **"VOLTAGE DIFFERENCING CURRENT CONVEYOR AND ITS APPLICATIONS"** being submitted by me is a authentic work carried out under the supervision of **Mr. A. K. SINGH (Associate Professor),** Electronics and Communication Engineering Department, Delhi Technological University, Delhi.

TARUN TAMRAKAR

(2K15/VLS/18)

ACKNOWLEDGEMENT

Generally, individuals set aims, but more often than not, their conquest are by the efforts of not just one but many determined people. This complete project could be accomplished because of contribution of a number of people. I take it as a privilege to appreciate and acknowledge the efforts of all those who have, directly or indirectly, helped me achieving my aim.

I take great pride in expressing my unfeigned appreciation and gratitude to my learned mentor **Mr. A. K. SINGH,** Department of Electronics and Communication Engineering, DTU for this invaluable inspiration, guidance and continuous encouragement throughout this project work. His critics and suggestions on my experiments have always guided me towards perfection. This work is simply the reflection of their thoughts, ideas, concepts and above all his efforts. Working under their guidance has been a privilege and an excellent learning experience that I will cherish for a long time.

I am also grateful to Prof. S.Indu, HOD, Department of Electronics and Communication Engineering, DTU for his immense support. I would also acknowledge DTU for providing the right academic resources and environment for this work to be carried out.

Finally, I extend my deep appreciation to my family and friends, for all that they meant to me during the crucial times of the completion of my project.

TARUN TAMRAKAR

(2K15/VLS/18)

(VLSI and Embedded System)

TABLE OF CONTENTS

LIST OF FIGURES

ABSTRACT

Precisely tailored frequency filters can be produced with standard operational amplifiers however for audio application only. In higher frequency range, use of some of modern active functional blocks is preferred. Recently, various active building blocks have been presented in which versatile and powerful building blocks are the Voltage Differencing Current Conveyor (VDCC). Active filters based on the VDCC have recently found attractive considerable attention. This stems from inherent incognito advantages of the current conveyor circuits and OTA circuits, namely low supply voltages and power, current operational mode possibility, well-developed IC topology and particularly a frequency range of the signal processing which can be higher than with circuits with the standard operational amplifiers. Since their introduction, the VDCC have led to a great number of applications in signal processing circuits, especially many oscillators and filters.

Tow Thomas Biquad based on VDCC is a new voltage mode biquad circuit. This circuit uses two voltage differencing current conveyors (VDCC) along with five resistors and two capacitors as passive elements. KHN Biquad filter using VDCC is a current mode universal biquad filter using voltage differencing current conveyor (VDCC). This filter circuit uses all grounded passive elements. The pole frequency (ω_o) and quality factor (Q) can be tuned independently in the presented filter structure. In VDCC Based TISO (three input single output) and SIDO (single input dual output) Biquad Filter, three voltage mode biquad structure is analysed. The first structure is three input single output biquad structure and the other two structures are single input dual output biquad structures whose quality factor can be adjusted by adjusting one resistor without changing pole frequency. Pole frequency of all the filters can be electronically tuned by varying biasing current. VDCC based Inductance Simulator is an actively simulated grounded inductor. It has been used in innumerable applications beginning from filter to oscillator design as well as cancellation of parasitic inductances. Moreover, new grounded inductance simulators using only one voltage differencing current conveyor (VDCC) and two passive elements are presented. This inductance simulators can be tuned electronically by changing the biasing current of the VDCC. These circuits do not require any component matching conditions. VDCC based floating inductance simulator is also presented. Using grounded inductance simulator, a third-order high-pass filter is constructed. Fifth order Low-Pass and High-Pass Ladder Filters based on VDCC are presented which employs two Voltage Differencing Current Conveyors (VDCCs), four resistors and five capacitors. The workability of all the filters has been verified using PSPICE simulations.

Chapter 1

Introduction

1.1 Overview

Need of electronic circuit with extremely low supply voltage and lower power consumption is an important aspect in the development of microelectronic circuits. Requirement of extreme speed and accuracy are must in many applications, to fulfill the above needs many tradeoff solutions are used in practice.

In the process of development of technologies which is used in analog signal processing trend of current mode circuits are added. In current mode circuits, all the information available is in the form of electric current, on the other hand all information's are available in the form of voltage in voltage mode circuits. But current mode circuits are having several advantages over voltage mode circuits such as it has low power consumption at higher frequency, less affected by voltage fluctuations, low cross talk and switching noise and high speed of operation and it is well suited for low voltage and low power applications.

Since with the emergence of current mode applications, mixed mode circuits also gain attention because of the necessity required for optimization of the interfaces between the sub-blocks, which is having working capability in different modes. Due to advancement in the integrated circuit technology, current mode circuits are gain its importance because of its efficient solutions to various circuit designing problems and having advantages like lower power consumption, linearity, better accuracy, high slew rate and higher frequency range of operation.

For many applications of analog signal processing active elements are required, hence development of active elements is very important aspect in analog signal processing. In recent many active elements are introduced which is having electronically controllable property. They provide facility to single parameter control like input resistance, voltage gain, current gain, transconductance and transresistance. But recently many methodologies are introduced for multi parameter control. General approach of voltage difference voltage at input is rectify to present VDCC (Voltage Differencing Current Conveyor). It is very useful device which consists of OTA (operational transconductance amplifier) and second generation of current conveyors (CCII) both as the sub blocks of VDCC. The transconductance of the OTA and current input terminal input resistance of the second-generation current conveyor (CCII) provides independent controlling of two parameters. But all the details in the VDCC are hypothetical and only simulation based. It is used in many applications many times. The CMOS based VDCC is as shown in Fig.3. But only transconductance control has been added. Many applications use CMOS based configuration of VDCC.

There are two active elements used in VDCC one is OTA (operational transconductance amplifier) and other one is MO-CCII (multiple output current conveyor II). Inside blocks of the VDCC structure is shown in Fig.1.

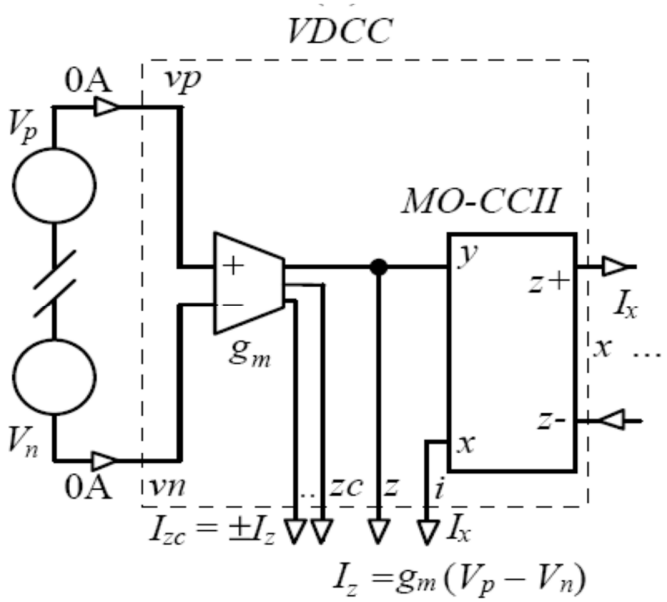


Fig.1 Active elements of the VDCC [1]

1.2 Voltage Differencing Current Conveyor (VDCC)

The circuit description of VDCC is as shown in Fig.2, It has input terminals P and N and output terminals Wp, Wn, Z, X except X terminal all terminals are having high input impedance.

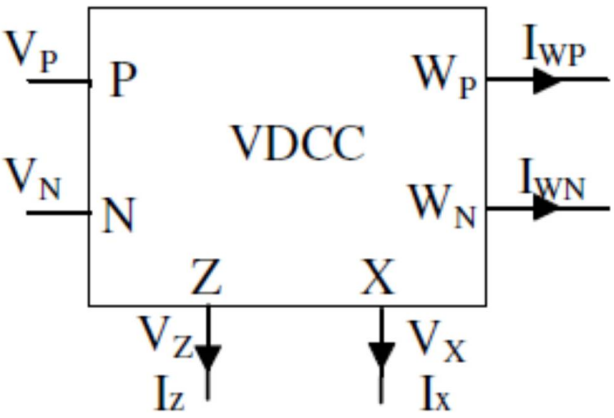


Fig.2 Circuit symbol of the VDCC [5]

Port matrix of ideal VDCC is as shown in below:

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}$$

From the above matrix equations for currents and voltages are:

$$I_Z = g_m (V_P - V_N)$$

$$V_X = V_Z$$

$$I_{WP} = I_X$$

$$I_{WN} = -I_X$$

From above matrix equation transconductance gain (g_m) can be obtained by converting differential input voltage (Vp-Vn) to output current (Iz) and next stage is current conveyor which is used for transferring current from X terminal to Wp and Wn terminals. For CMOS (complementary metal oxide semiconductor) transconductance gain is given by

$$g_m = \sqrt{I_{B1} \mu_n C_{ox} \left(\frac{W}{L}\right)_1}$$

Here μ_n is the carrier mobility of NMOS transistor, Cox is oxide capacitance per unit area, W and L is effective channel width and length respectively and I_B is the bias current. CMOS implementation of VDCC is as shown in Fig.3, It is 22 transistor circuit as shown with V_{DD} and V_{SS} are supply voltages and I_{B1} and I_{B2} are biasing currents. Aspect ratios of the transistors are adjusted as per the application requirements.

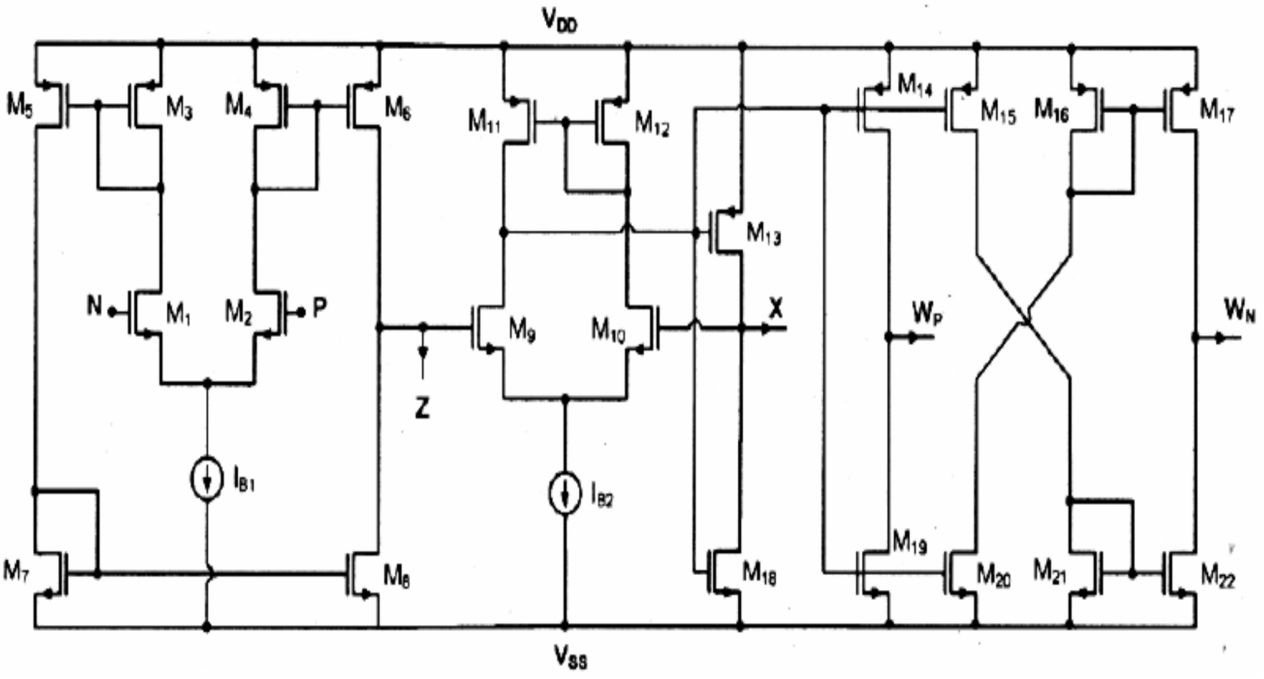


Fig.3 CMOS implementation of the VDCC [5]

BJT implementation of VDCC is shown in Fig.4 here transconductance value g_m at Z terminal of VDCC can be controlled with the help of bias current I_{B2}. Transconductance value is given by $g_m = I_{B2}/2V_T$, here V_T is volt equivalent temperature or thermal voltage its value is 25.6 mV at 25ºC and k is Boltzmann's constant, T is temperature in Kelvin and electron charge is q.

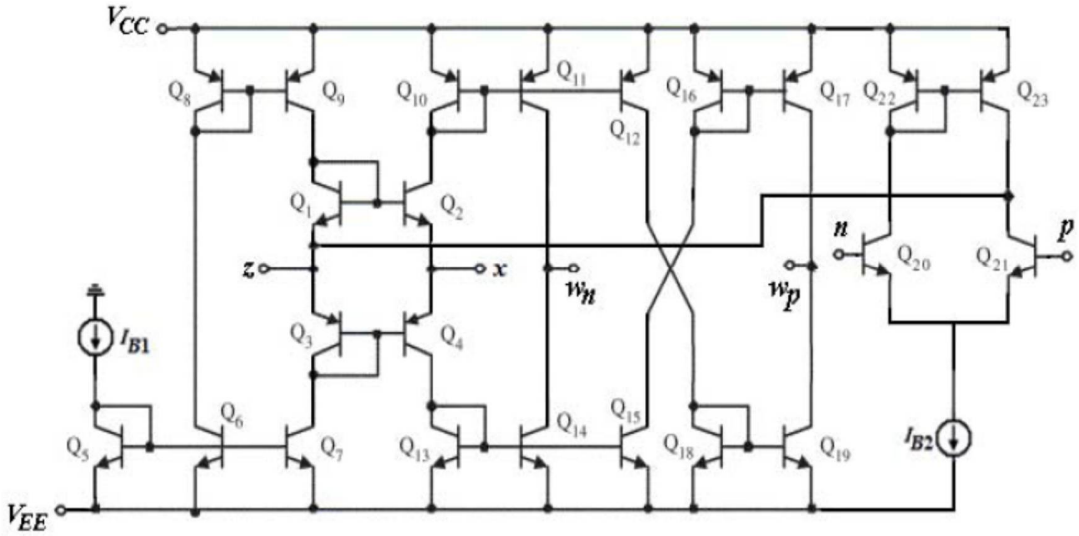


Fig.4 BJT implementation of VDCC [10]

Chapter 2

Literature Review

Voltage differencing current conveyor is a versatile active building block. VDCC relates to the family of novel hybrid elements which was presented by Biolek et al. [14]. It has various applications like used in designing of filter, used as inductance simulator, oscillator, signal generators, floating inductance simulator, capacitance multiplier and it is able to provide multifunction filter structure.

In the year 2008, Dalibor BIOLEK, Raj SENANI, Viera BIOLKOVÁ, Zdeněk KOLKA [1] presented a paper on various active elements for Analog Signal Processing and its classification, Review and New Proposals.

In the year 2014, Dinesh Prasad, Javed Ahmad [7] presented a paper on electronically controllable floating inductance which did not require any matching condition. This circuit consist of a single VDCC along with one grounded capacitor and resistor. Floating inductance simulator is electronically controllable by varying the bias current.

In the year 2014, Dinesh Prasad, D. R. Bhaskar and Mayank Srivastava [8] presented a paper on single resistance controlled sinusoidal oscillator (SRCO) which uses a single voltage differencing current conveyor (VDCC) structure along with two grounded resistor and capacitors. Presented circuit is having following advantages:

1. Current mode output and independent control in oscillation condition and frequency of oscillation.
2. Passive and active sensitivities are low.
3. Frequency stability is very good.

Presented circuit can also be configured as trans admittance band pass and low pass filter and quadrature oscillator.

In the year 2014, R. Sotner, N. Herencsar, J. Jerabek, R. Prokop, A. Kartci, T. Dostal, K.Vrba [9] presented a paper on modified version of the VDCC (Voltage Differencing Current Conveyor) which is named as ZC-CGVDCC (Z-copy controlled gain voltage differencing current conveyor). This structure provides us independent electronic control of three parameters such as current input terminal intrinsic resistance, transconductance and output stage current gain which is not possible with the conventional VDCC.

In the year 2015, Mehmet Sagbas, Umut E. Ayten, Muhammet Koksal, and Norbert Herencsar [10] presented a paper on voltage mode universal filter, which is having single input and four outputs. Presented structure consists of a single VDCC along with two resistors and two capacitors. This structure provides various filtering functions such as low pass, high pass, bandpass, notch. Quality factor and pole frequency can be adjusted electronically without any variation in passive components. Also component matching condition is not required and sensitivity performance is also good with respect to passive components tracking errors.

In the year 2015, Aslihan Kartci, Umut Engin Ayten, Norbert Herencsar, Roman Sotner, Jan Jerabek, Kamil Vrba [11] presented a paper on low voltage design of floating element simulator circuit for realization of floating frequency dependent negative resistor (FDNR), floating resistor, floating capacitor and floating inductor depends on passive component selection. This circuit uses two VDCC blocks along with three passive components while low supply (±0.45 V). it shows electronically controllable property while changing the bias currents or by the grounded resistor or capacitors. It does not require any passive component matching condition.

In the year 2015, A. Kartci, U. E. Ayten, R. Sotner, R. Arslanalp [12] presented a paper on grounded capacitance multiplier. It consists two VDCC blocks along with two resistors and one grounded capacitor. By varying the bias current value this circuit can be tuned electronically and component matching condition is not required.

In the year 2015, A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek, K. Vrba [13] presented paper on new electronically controllable floating lossless capacitance multiplier (C-Multiplier). It uses single VDCC structure along with one grounded resistor and capacitor. Since this structure uses a grounded capacitor hence it is suitable for IC fabrication.

In the year 2015, R. Sotner, J. Jerabek, N. Herencsar, T. Dostal, K. Vrba [14] presented a paper on new active element named as ZC-CGVDCC (Z-copy controlled gain voltage differencing current conveyor) and its application as function generators (square and triangular wave).

In the year 2016, Mayank Srivastava, Priyanka Bhanja and Suhaib Fayaz Mir [15] presented a paper on floating element simulator structure, which consist of two VDCC structures along with three grounded passive component. This circuit is able to realize floating inductor, capacitor and resistor depends upon the choice passive components. The presented circuit does not require any component matching condition. By changing the transconductance value the floating inductor, capacitor and resistor are tuned electronically.

Chapter 3

Tow Thomas Biquad structure based on VDCC

3.1 Introduction

Tow Thomas biquad is one of the famous biquad structure which uses two integrators configuration which is connected in loop topology. It uses operational amplifier as active element, here Op-Amp is used as single ended amplifier whereas in KHN biquad structure Op-Amp is used as differential amplifier. The above structure can be obtained by using various active element structure such as current conveyor (CCII), Operational transconductance amplifier (OTA), Differential voltage current conveyor (DVCC). Recently a new active building block is introduced which is basically a combination of basic cells of analog such as voltage differencing units and current differencing units also uses voltage buffers and current mirrors.

VDCC is one of the examples of this which provides electronically tunable transconductance property. It is also used for implementation of various types of active filters, Oscillators and simulated inductors.
VDCC based Analog active RC filters are gaining importance because of several advantages like it uses OTA and CCII both having low supply and power. It has well introduced IC topology and it is also having possibility of current mode operation. A voltage mode Tow Thomas biquad filter is introduced which uses optimal numbers of active and passive components.

3.2 VDCC based Tow Thomas Biquad circuit structure

The pictorial representation of the Tow Thomas biquad is shown in Fig.5 here two outputs lead two filter responses which is band pass and low pass. Including this one ideal and one lossy integrator are used.

Hierarchical structure of VDCC based voltage mode biquad filter is presents. From integration point this circuit is ideal because all the passive components are ground referred which compensates by source resistance partially.

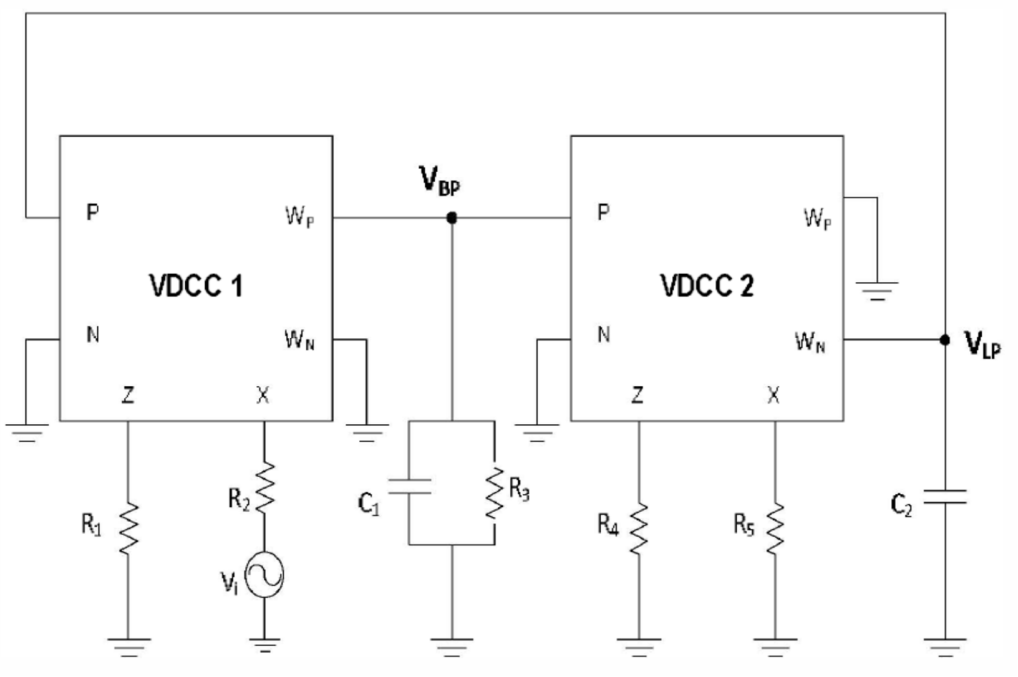


Fig.5 Tow Thomas biquad filter based on VDCC [2]

Band pass filter transfer function is shown below

$$\frac{V_{obp}}{V_{in}} = \frac{-\frac{s}{C_1R_2}}{s^2 + \frac{s}{C_1R_3} + \frac{g_{m1}g_{m2}R_1R_4}{C_1C_2R_5R_2}}$$

Low pass filter transfer function is shown below

$$\frac{V_{olp}}{V_{in}} = \frac{\frac{g_{m2}R_4}{C_1C_2R_5R_2}}{s^2 + \frac{s}{C_1R_3} + \frac{g_{m1}g_{m2}R_1R_4}{C_1C_2R_5R_2}}$$

Here g_{m1} and g_{m2} are transconductance gain of VDCC1 and VDCC2 respectively from above transfer function we obtained values of quality factor (Q), pole frequency (ω_0), bandwidth (BW)

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}R_1R_4}{C_1C_2R_5R_2}}$$

$$Q = R_3 C_1 \omega_0$$

Or

$$Q = R_3 C_1 \sqrt{\frac{g_{m1} g_{m2} R_1 R_4}{C_1 C_2 R_5 R_2}}$$

$$BW = \frac{1}{R_3 C_1}$$

Center frequency gain for band pass filter response is given by

$$\text{Center frequency gain} = -\frac{R_3}{R_2}$$

Dc gain value for low pass filter response is given by

$$\text{DC gain} = \frac{1}{g_{m1} R_1}$$

For separate tuning of bandwidth, gain and pole frequency we consider $R_2=R_4=R'$ and $R_1=R_5=R''$

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}$$

$$BW = \frac{1}{R_3 C_1}$$

$$Q = R_3 C_1 \omega_0$$

Or

$$Q = R_3 C_1 \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}$$

Center frequency gain for band pass filter response is given by

$$\text{Center frequency gain} = -\frac{R_3}{R'}$$

Dc gain value for low pass filter response is given by

$$\text{DC gain} = \frac{1}{g_{m1}R''}$$

Sensitivities results are as follows

$$S^{\omega_0}_{C_1,C_2} = -\frac{1}{2}$$

$$S^{\omega_0}_{R_3,R',R''} = 0$$

$$S^{\omega_0}_{g_{m1},g_{m2}} = +\frac{1}{2}$$

$$S^{Q}_{g_{m1},g_{m2},C_1} = +\frac{1}{2}$$

$$S^{Q}_{C_2} = -\frac{1}{2}$$

$$S^{Q}_{R_3} = +1$$

$$S^{Q}_{R',R''} = 0$$

From the above results, it is shown that for low pass filter configuration pole frequency and dc gain varies independently similarly for band pass filter configuration pole frequency and dc gain varied independent to each other.

3.3 Simulation Results

PSPICE simulation is used to check the workability of the circuit. This design has pole frequency (f_0) =3MHz and having quality factor (Q)=0.707. Values of Passive elements such as resistors $R_2=R_4=R'=3.66K\Omega$, $R_1=R_5=R''=3.66K\Omega$ and capacitors $C_1=C_2=14.5pf$ are chosen. Biasing current which we are using is $I_{B1}=50\mu A$ and $I_{B2}=100\mu A$. TSMC CMOS 180nm parameter model is used for analysis of the circuit. Width to length ratios of the transistor is shown below in Table 1.

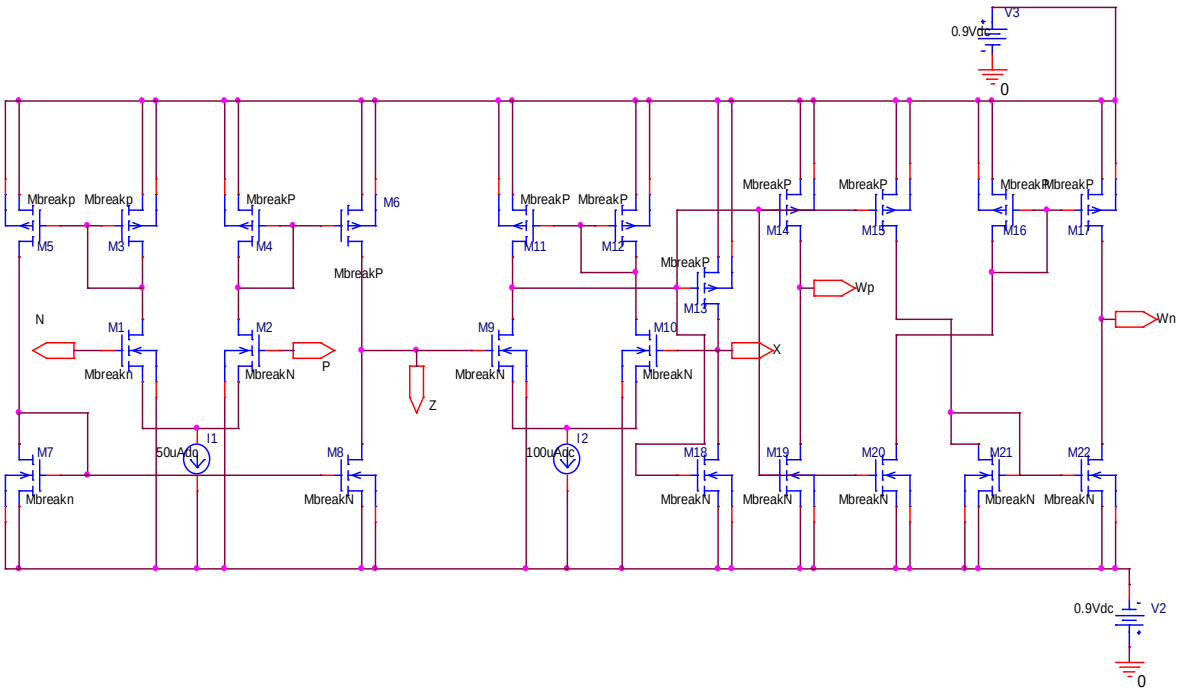


Fig.6 CMOS implementation of the VDCC schematic [5]

Table 1

Transistors	W/L(μm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{17}	14.4/0.72
M_{18}-M_{22}	0.72/0.72

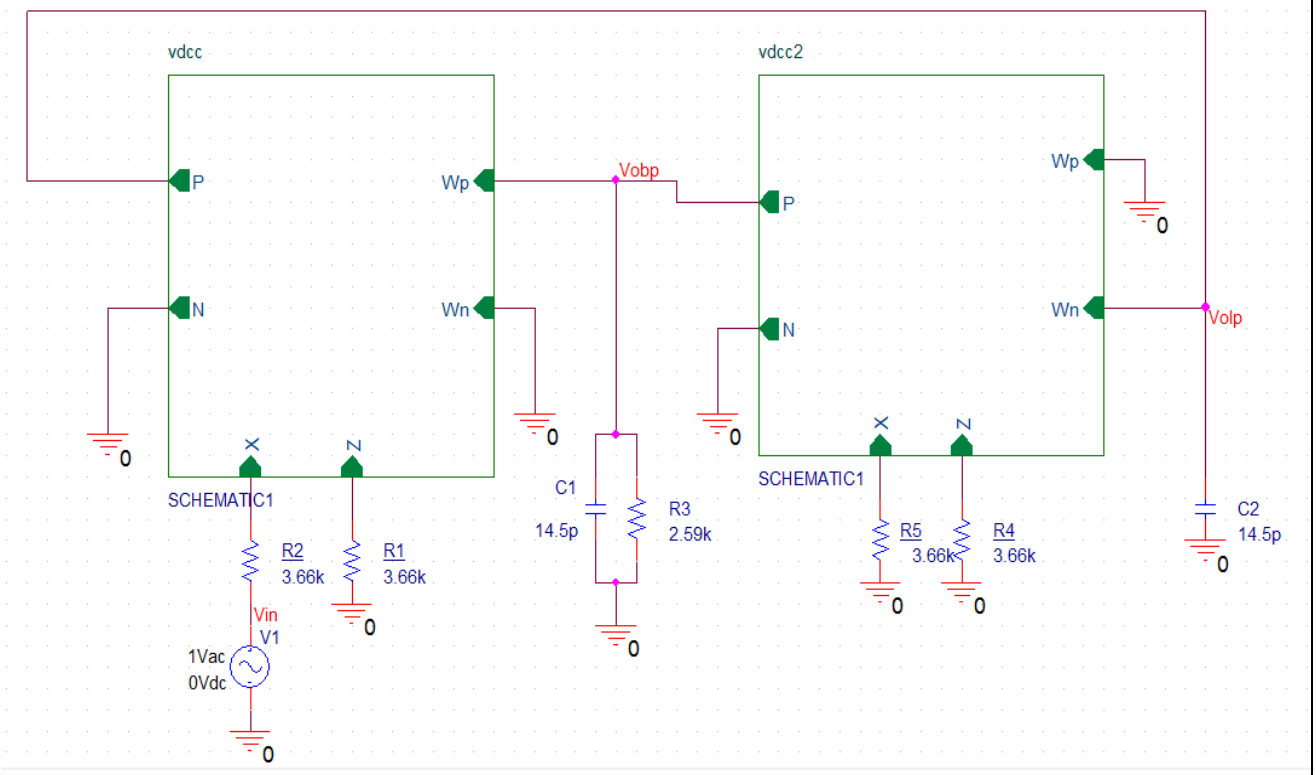


Fig.7 Tow Thomas biquad filter based on VDCC schematic [2]

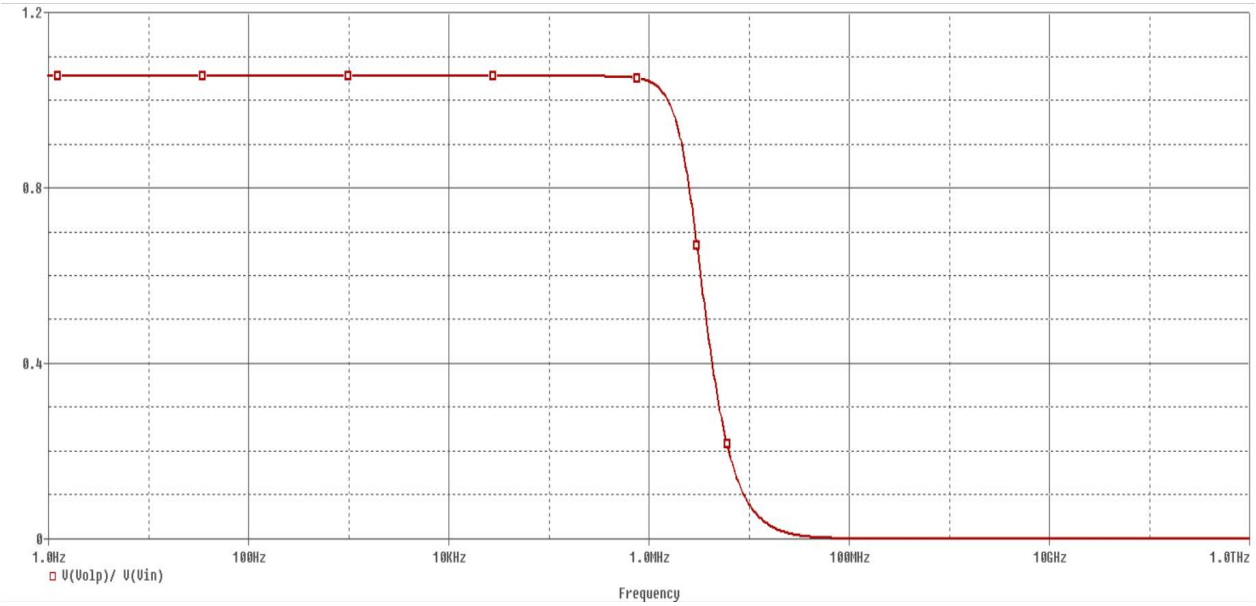


Fig. 7[a] Frequency response of Tow Thomas biquad filter based on VDCC(LPF(fc=3.3Mhz))

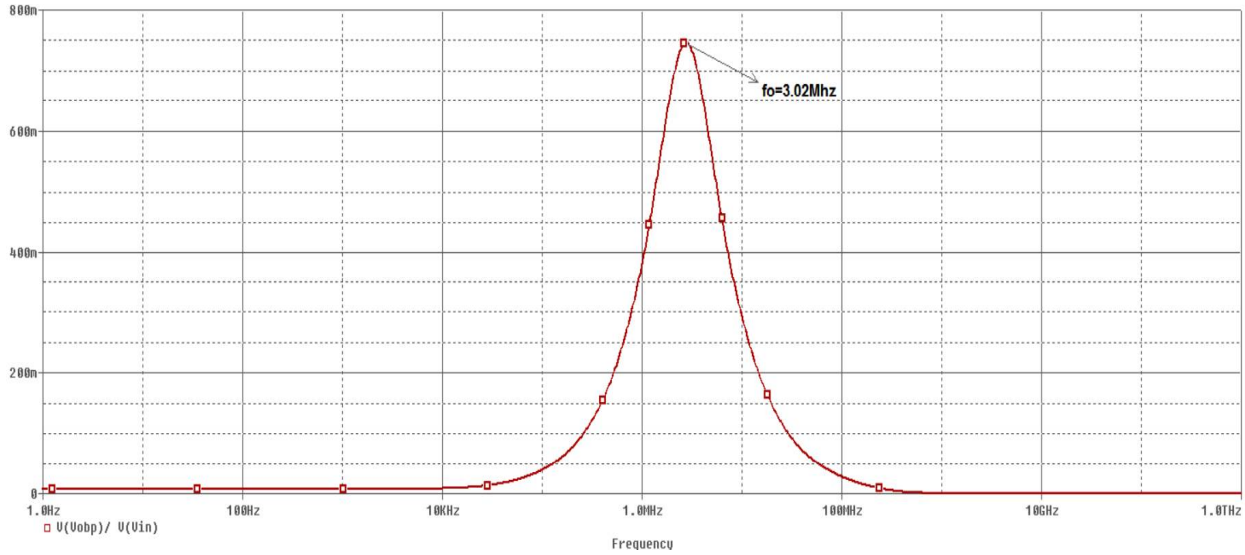


Fig. 7[b] Frequency response of Tow Thomas biquad filter based on VDCC (BPF)

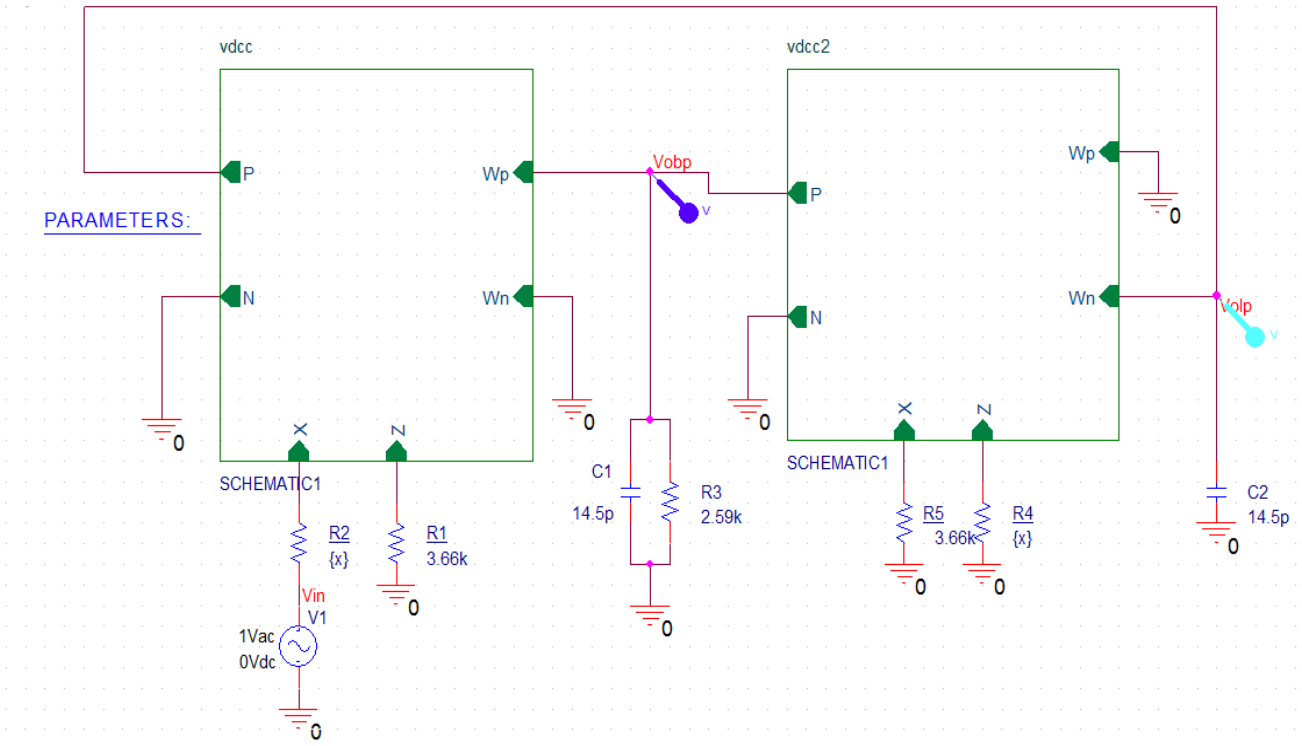


Fig.8 Center Frequency Gain Variation While Other Parameters are Constant schematic [2]

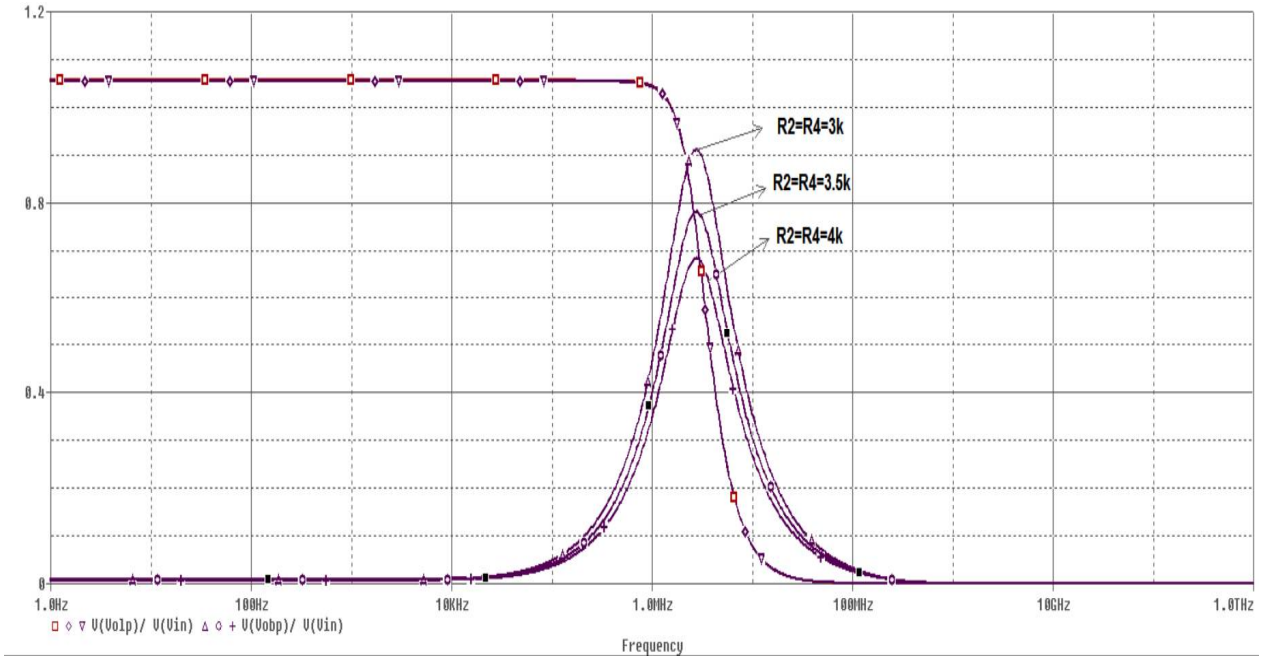


Fig. 8[a] Frequency response of Center Frequency Gain Variation While Other Parameters are Constant

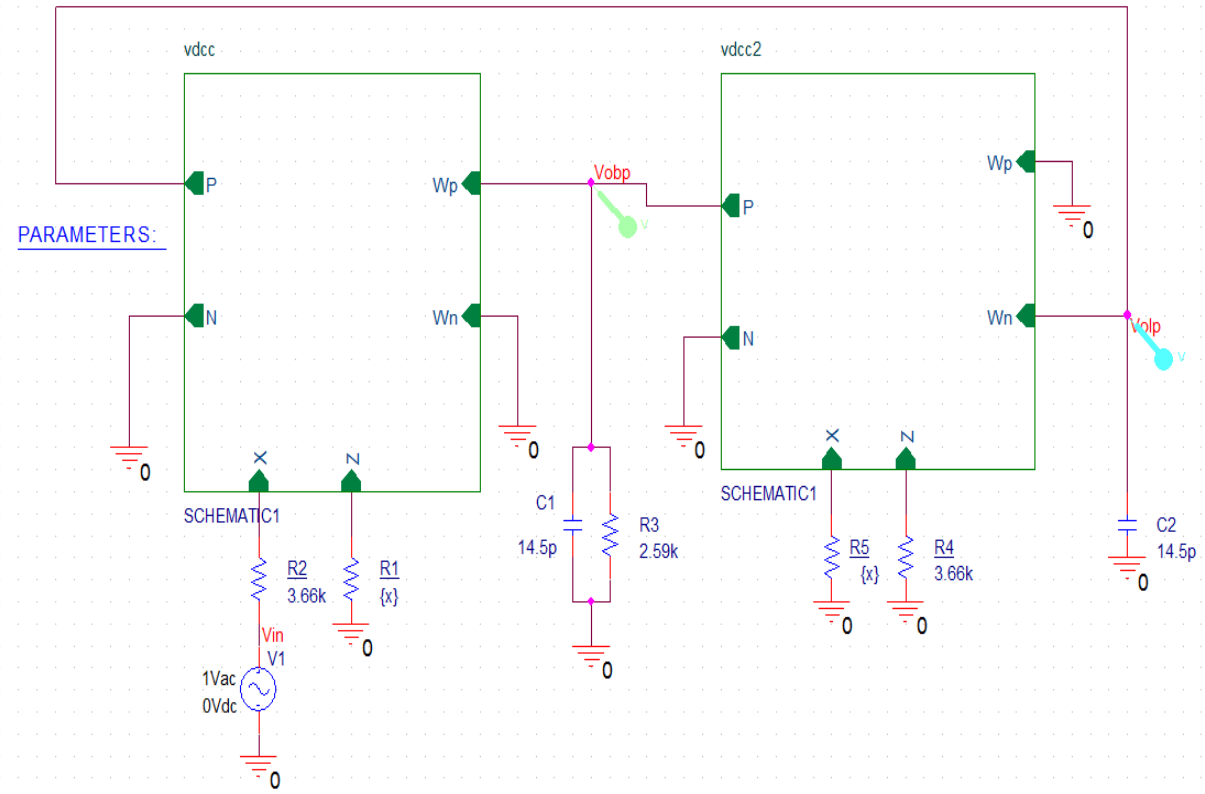


Fig.9 DC Gain Variation While Other Parameters are Constant schematic [2]

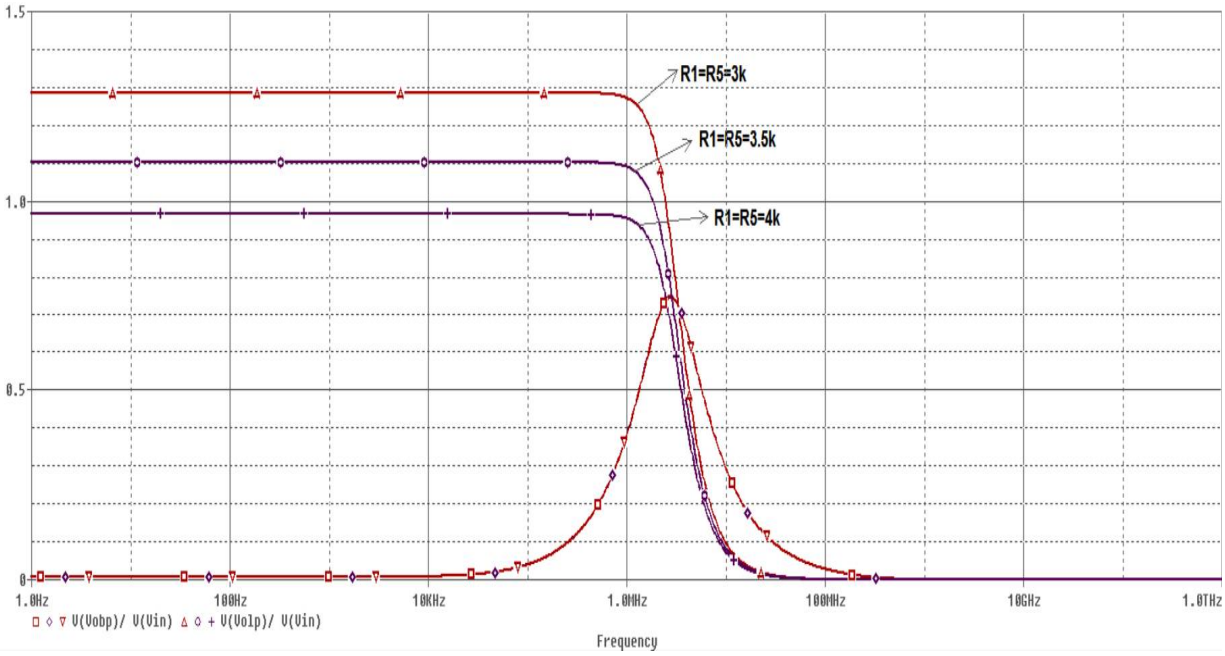


Fig. 9[a] Frequency response of DC Gain Variation While Other Parameters are Constant

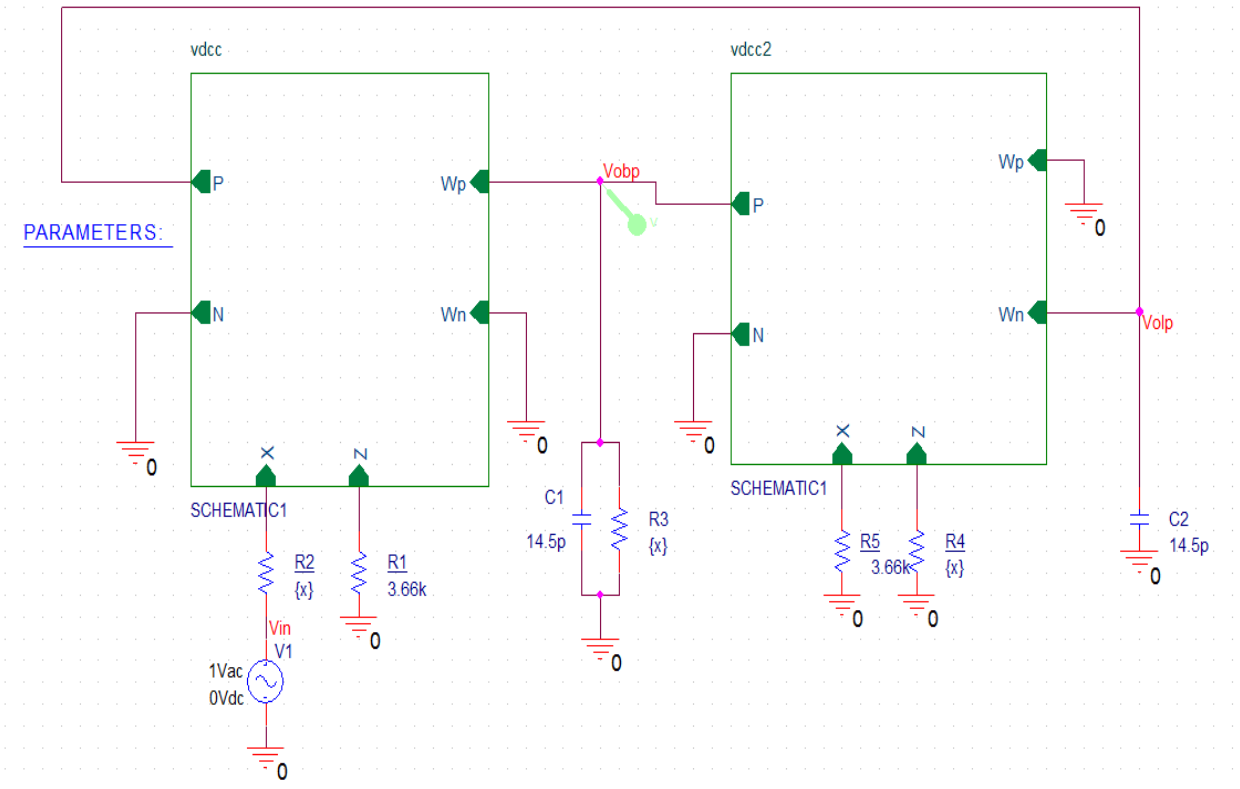


Fig.10 Bandwidth Variation While Other Parameters are Constant schematic [2]

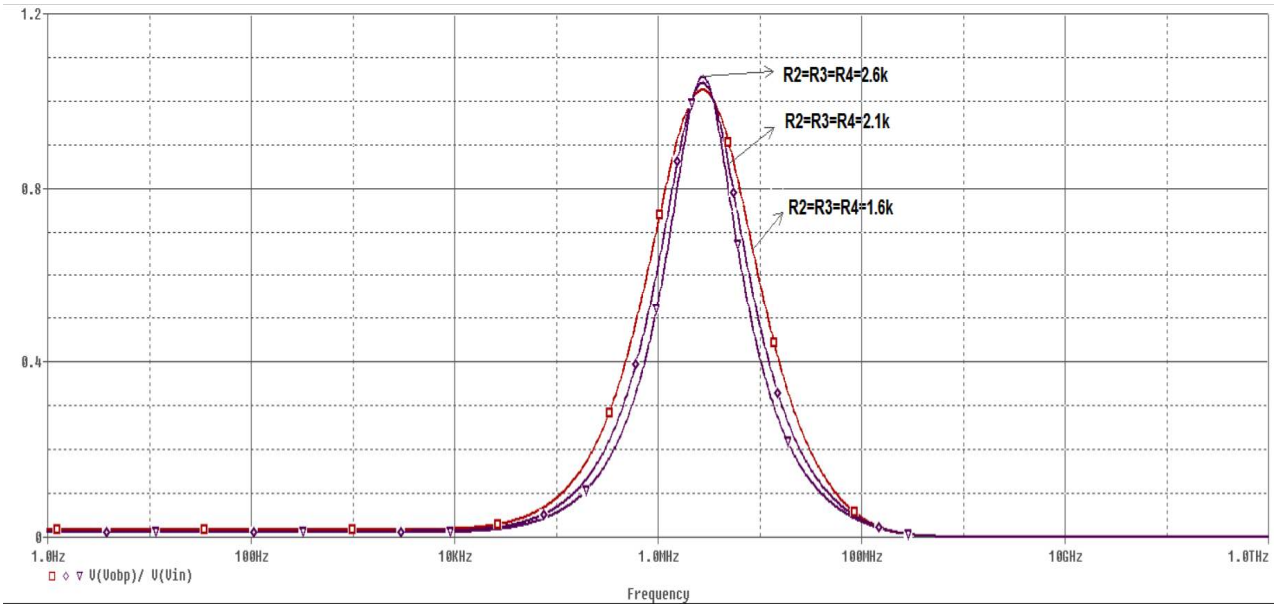


Fig. 10[a] Frequency response of Bandwidth Variation While Other Parameters are Constant

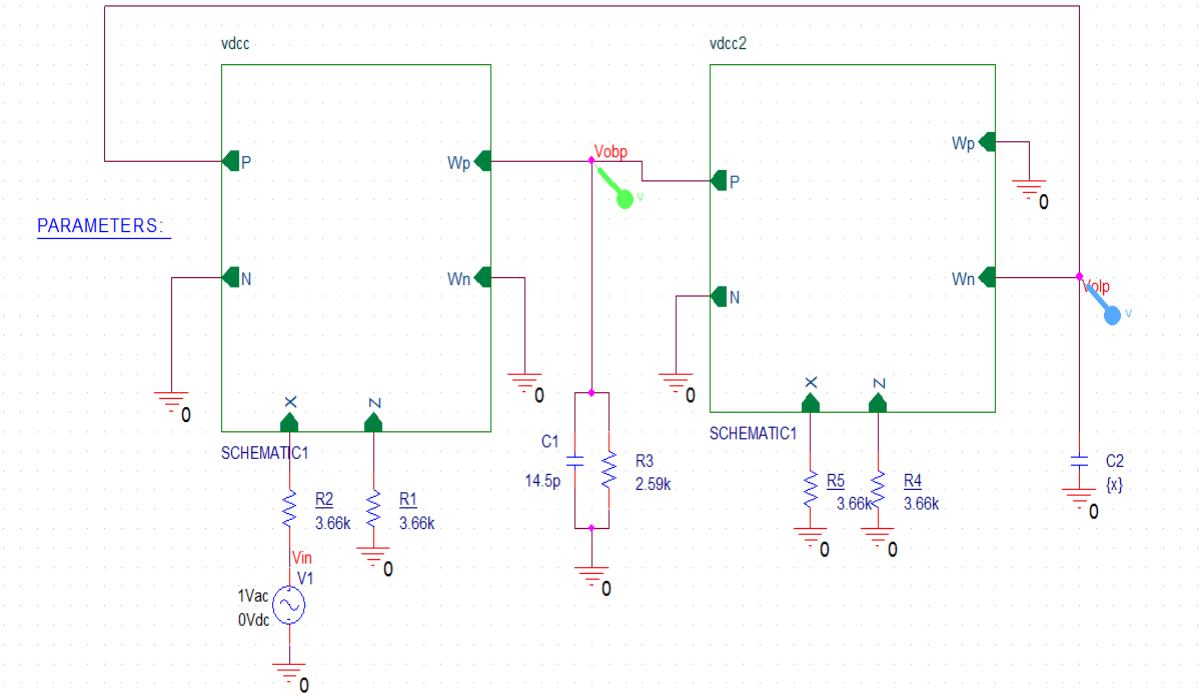


Fig.11 Pole Frequency Variation While Other Parameters are Constant schematic [2]

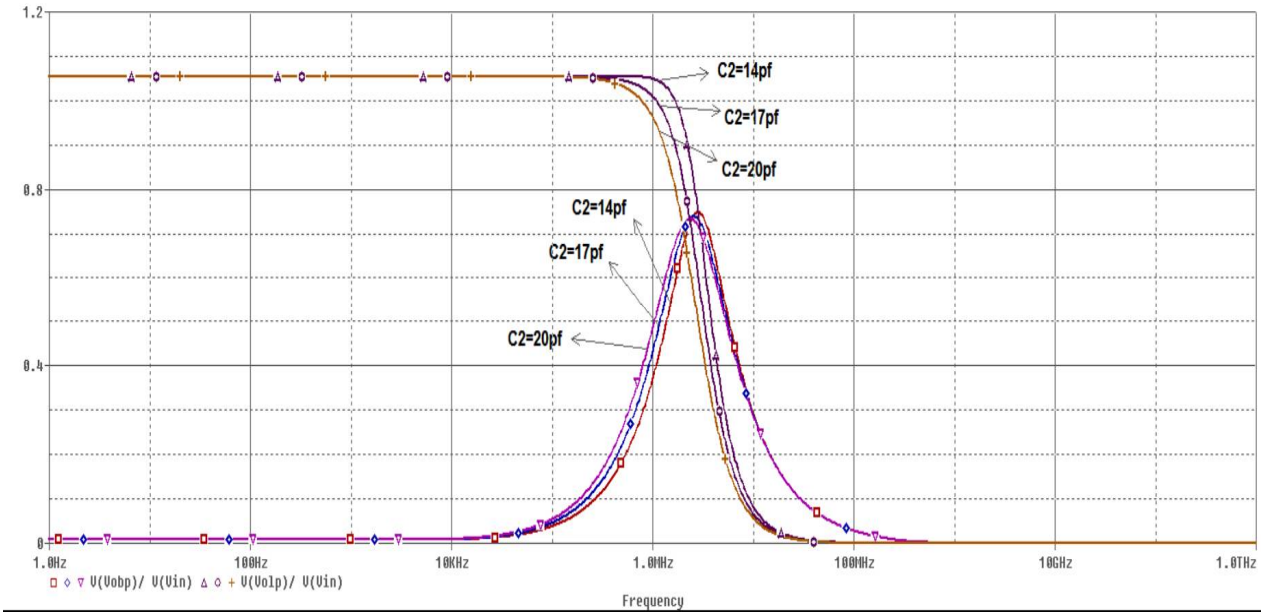


Fig. 11[a] Frequency response of Pole Frequency Variation While Other Parameters are Constant

Chapter 4

KHN Biquad filter using VDCC

4.1 Introduction

The Kerwin-Huelsman-Newcomb (KHN) is a multifunction biquad filter structure. Realization of this structure is done by placing two integrators in the feedback loop. KHN biquad filters circuit is having various advantageous features compared to other biquad structures such as low spreading occurs in component values, sensitivities are low and response are stable. On the other view, current mode circuits are having several advantages such as simplicity in circuit designing and lower power consumption and having wider bandwidth in comparison with the voltage mode circuits. The motivation behind designing of such two integrators in the feedback loop is the outcome of the limitations faced by the current mode filters such as

1. Need of more number of active element in designing of KHN biquad.
2. Need of large number of passive components.
3. Interdependence of the quality factor and pole frequency.

4.2 KHN Biquad structure using VDCC

The basic structure of CMOS based VDCC is as shown in Fig.3. KHN biquad structure is shown in Fig.13, it is consisting of two blocks one of them is VDCC and other one is ZC-VDCC (Z-copy voltage differencing current conveyor). In order to add more versatility previous structure of CMOS based VDCC has been modified by adding two z-copy terminals which carries complementary differential current of z terminal. The basic structure of ZC-VDCC is as shown in Fig.12.

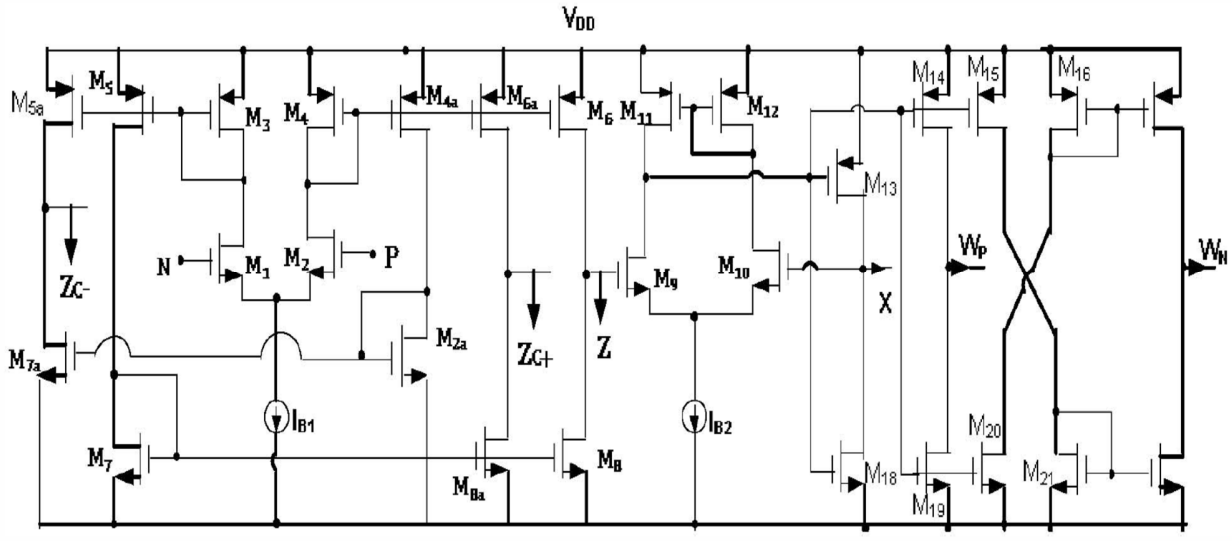


Fig.12 Z-Copy VDCC using CMOS [3]

These Currents of Fig.12is given by

$$I_{ZC+}=I_{ZC-}=I_Z$$

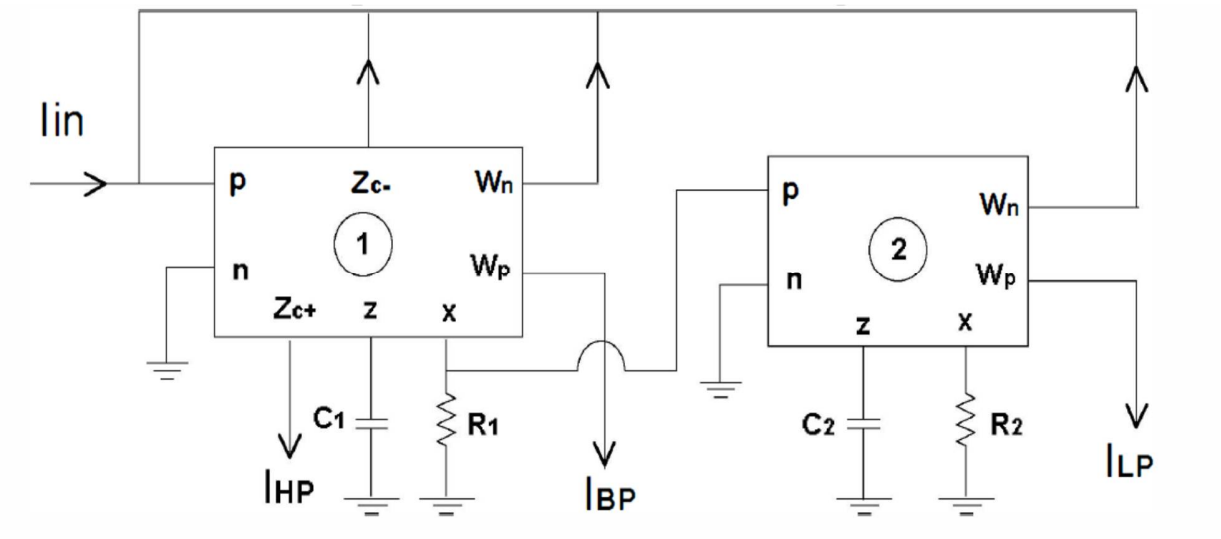


Fig.13 VDCC based Current Mode KHN Biquad filter [3]

Circuit analysis of Fig.13results the expressions derived for different filter outputs which are as follows:

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{D(s)}$$

$$\frac{I_{BP}}{I_{in}} = \frac{\frac{s}{C_1R_1}}{D(s)}$$

$$\frac{I_{LP}}{I_{in}} = \frac{\frac{g_{m2}}{C_1C_2R_2}}{D(s)}$$

$$D(s) = s^2 + \frac{s}{C_1R_1} + \frac{g_{m2}}{C_1C_2R_2}$$

By adding high pass, low pass output and high pass, inverted band pass and low pass output respectively, BandReject (BR) and AllPass (AP) output can be acquired. Note that all the outputs are obtainable at high output impedance nodes which is a required property of a current mode filter.

$$I_{BR} = I_{HP} + I_{LP}$$

$$I_{AP} = I_{HP} + I_{LP} - I_{BP}$$

$\boldsymbol{\omega_0}$ & Q can be varied independently in below equations

$$\omega_0 = \sqrt{\frac{g_{m2}}{C_1 C_2 R_2}}$$

$$Q = R_1 \sqrt{\frac{g_{m2} C_1}{C_2 R_2}}$$

Without influencing pole frequency, the quality factor of the filter can be varied by varying R_1. For tuning of quality factor, passive resistance is used instead of active resistance which results in high value of quality factor, a highly desirable property of filter structure. Following variations can be taken up to retain constant Q for controlling pole frequency:

$$g_{m2} R_1 = 1$$

and

$$R_1 = R_2$$

Different value of g_{m2} will result from varied values of R_2 which could be varied by adjusting value of bias current I_{B1}. Therefore, without disturbing quality factor, any pole frequency can be set using value of R_2 and the expressions shown in equation.
Evaluation of the sensitivities of quality factor Q and center frequency $\boldsymbol{\omega_0}$ of the circuit are as follows:

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_2}^{\omega_0} = -\frac{1}{2}$$

$$S_{g_{m2}}^{\omega_0} = +\frac{1}{2}$$

$$S_{g_{m1}}^{\omega_0} = S_{R_1}^{\omega_0} = 0$$

$$S_{C_2}^{Q} = S_{R_2}^{Q} = -\frac{1}{2}$$

$$S_{g_{m2}}^{Q} = S_{C_1}^{Q} = +\frac{1}{2}$$

$$S_{R_1}^{Q} = 1$$

$$S_{g_{m1}}^{Q} = 0$$

It can be concluded from above sensitivity calculations**;** all active and passive sensitivities are at most unity or less than unity in magnitude**.**

4.3 Simulation Results

By simulating the structure using PSPICE program, the theoretical verification of Fig.13 can be performed. Using 0.18µm TSMC process parameters, MOS transistors present in VDCC and ZC-VDCC are simulated. Table 2 gives aspect ratio for different MOS transistors of Fig.6. V_{DD}= -V_{SS} =0.9V, I_{B1} = 50µA and I_{B2} =100µA are used. The pole frequency (f_0) =1.59 MHz and quality factor (Q) =1 are set to justify the working of biquad structure that results into values of passive elements as R_1=6.67kΩ, R_2=12.33kΩ, C_2=15pF and C_3=15pF.

Table 2

Transistors	W/L(µm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{17}	14.4/0.72
M_{18}-M_{22}	0.72/0.72

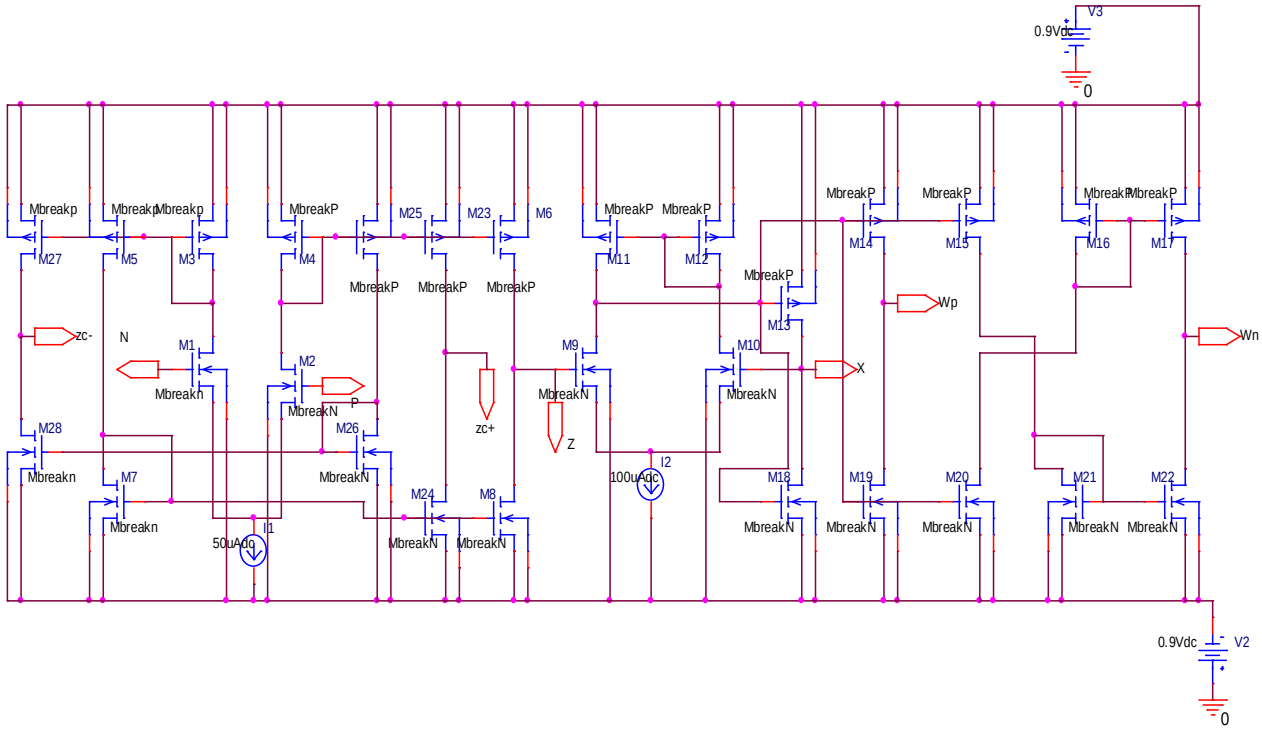


Fig.14 Schematic diagram of Z-Copy VDCC [3]

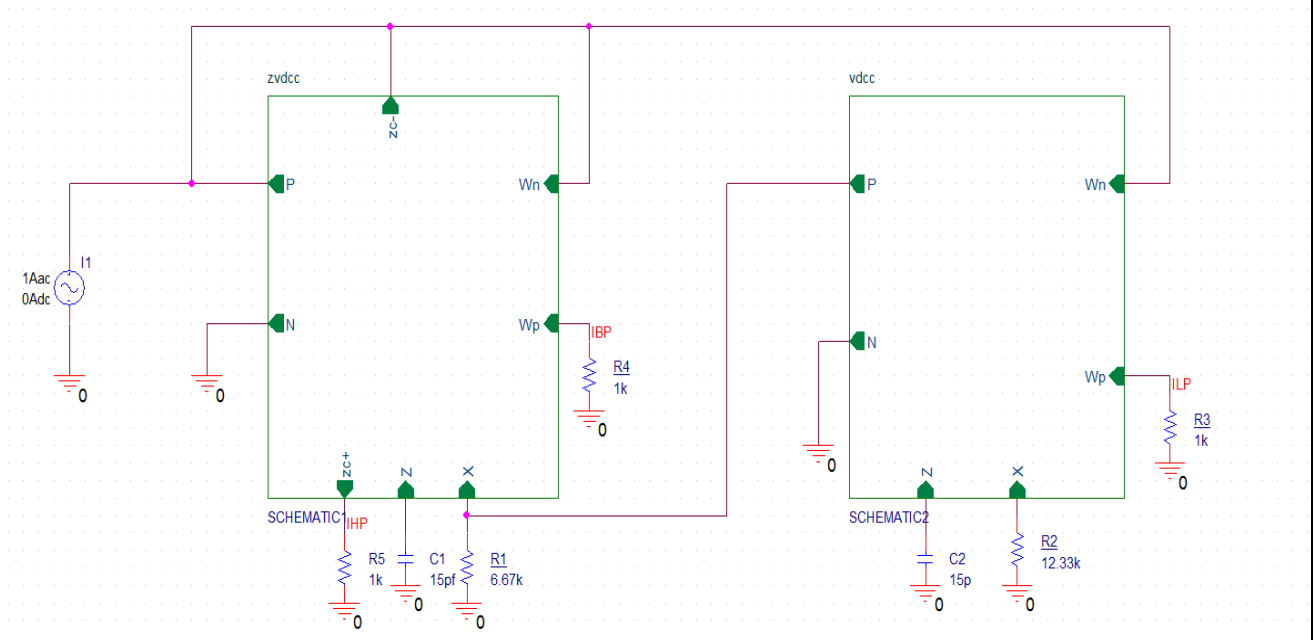


Fig.15 VDCC based Current Mode KHN Biquad filter schematic [3]

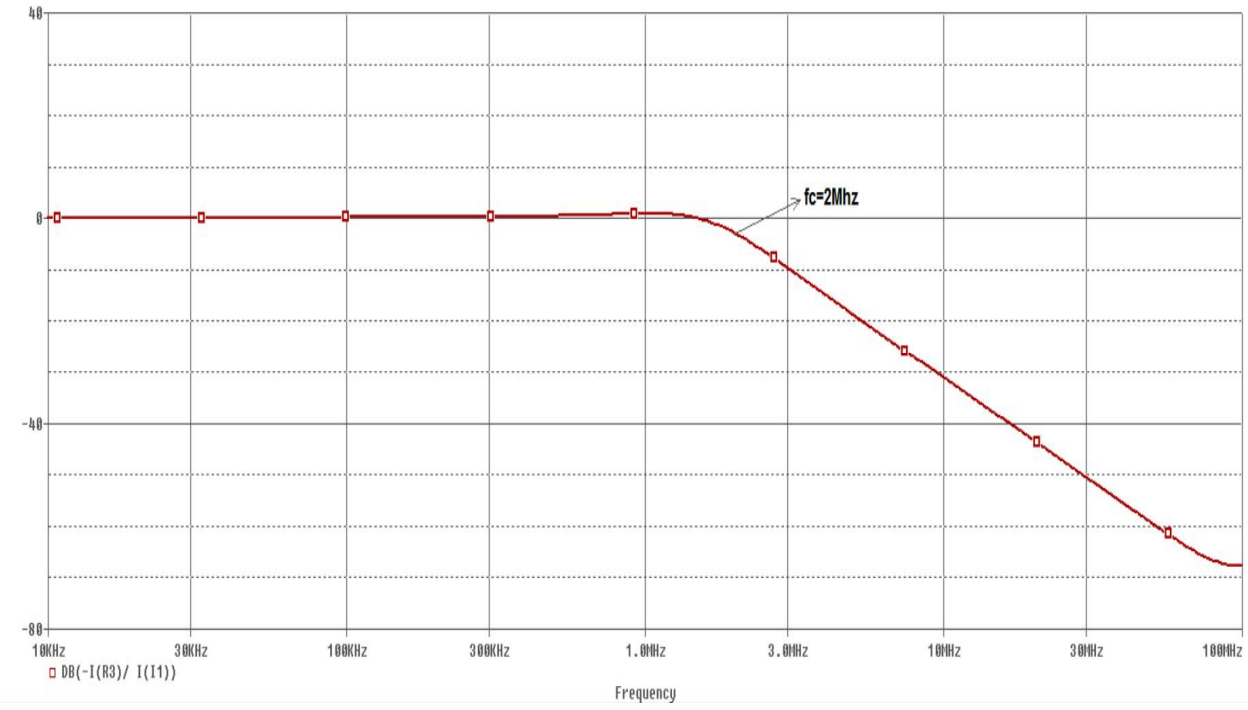


Fig. 15[a] Frequency response of LPF

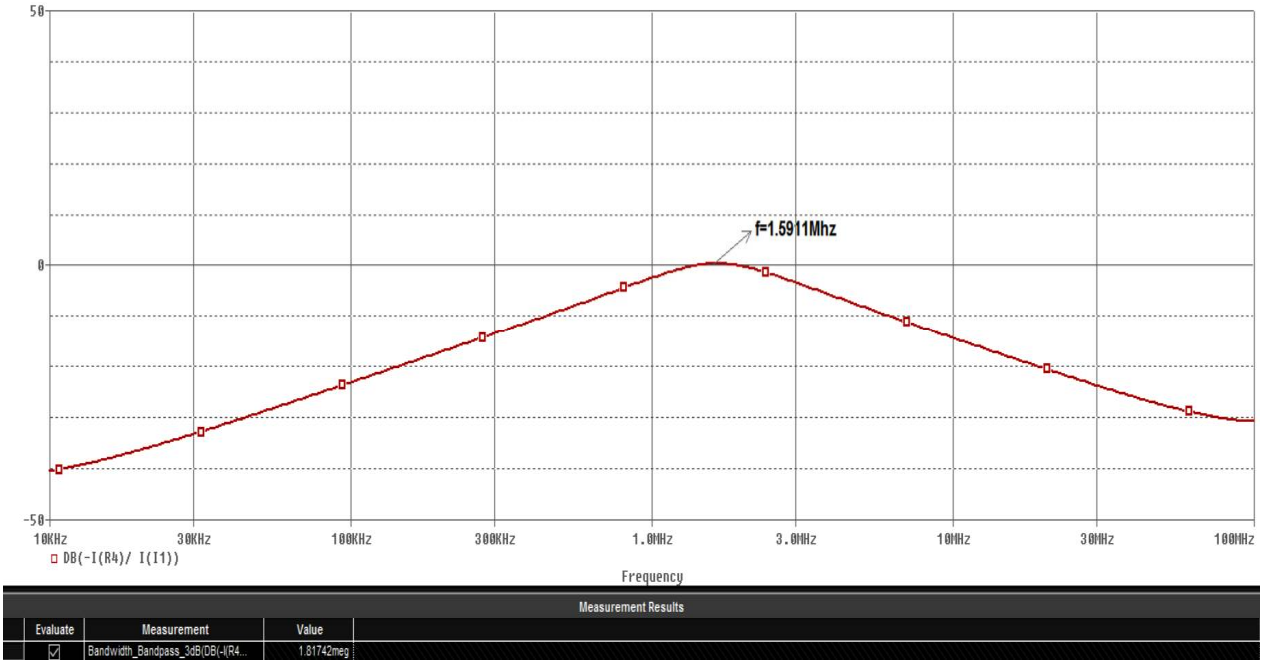


Fig. 15[b] Frequency response of BPF

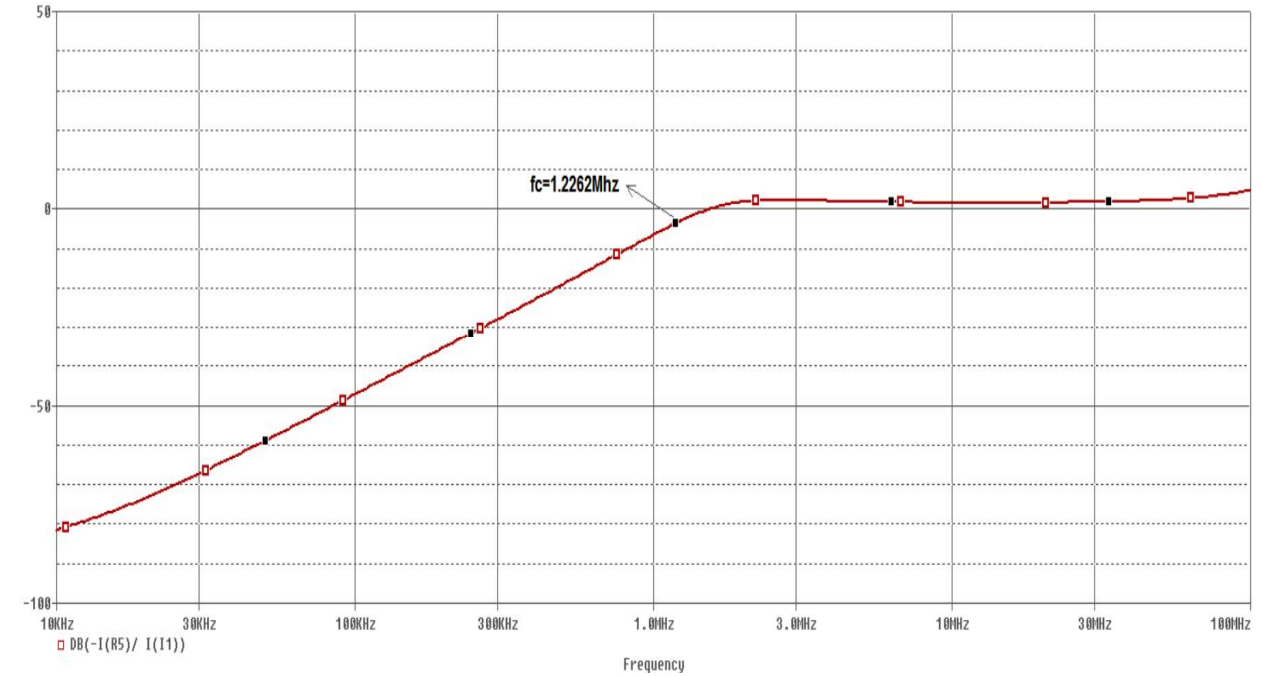


Fig. 15[c] Frequency response of HPF

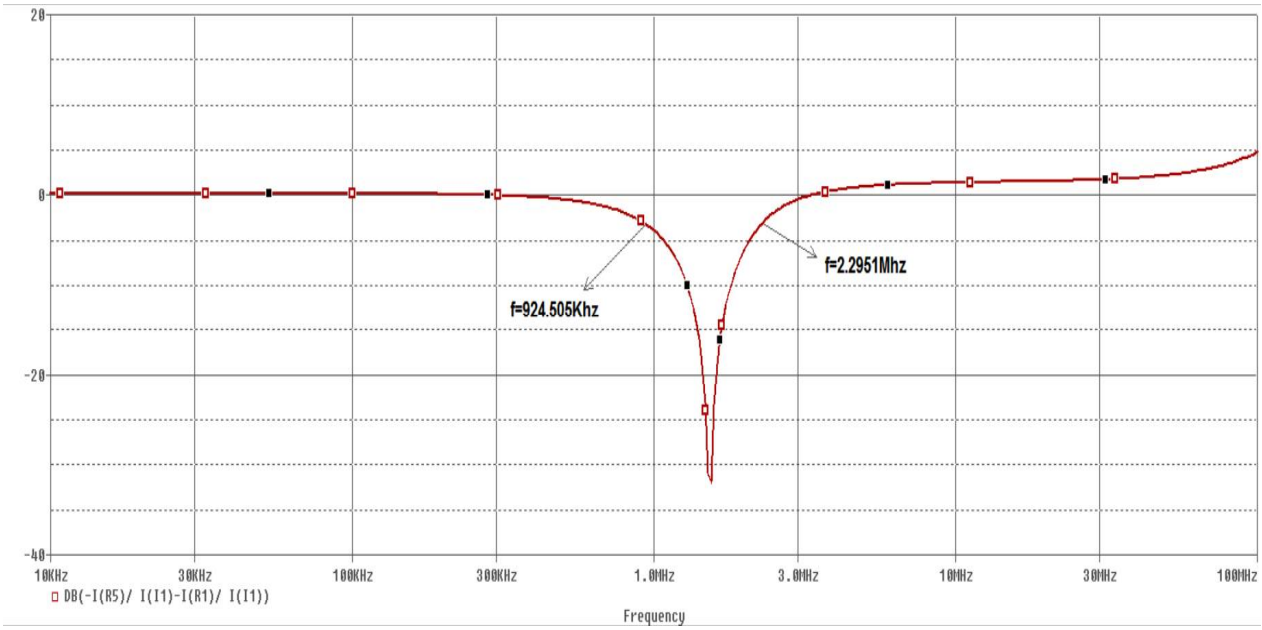


Fig. 15[d] Frequency response of BSF

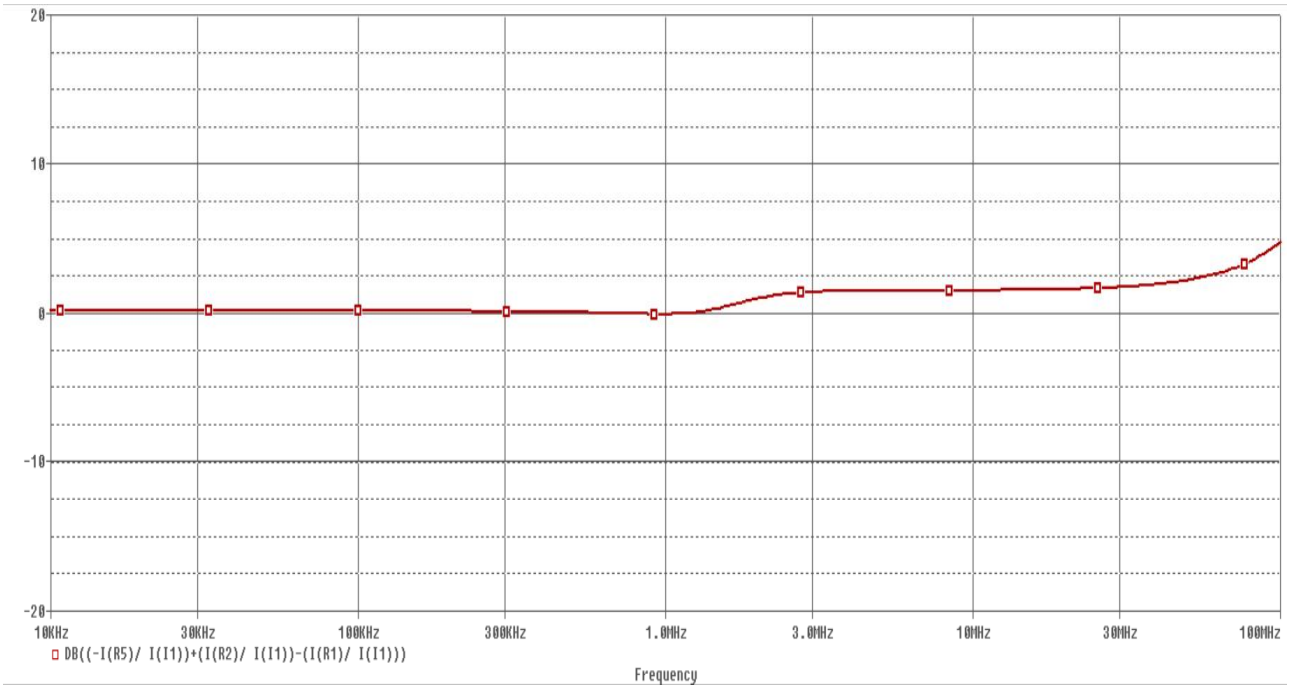


Fig. 15[e] Frequency response of APF

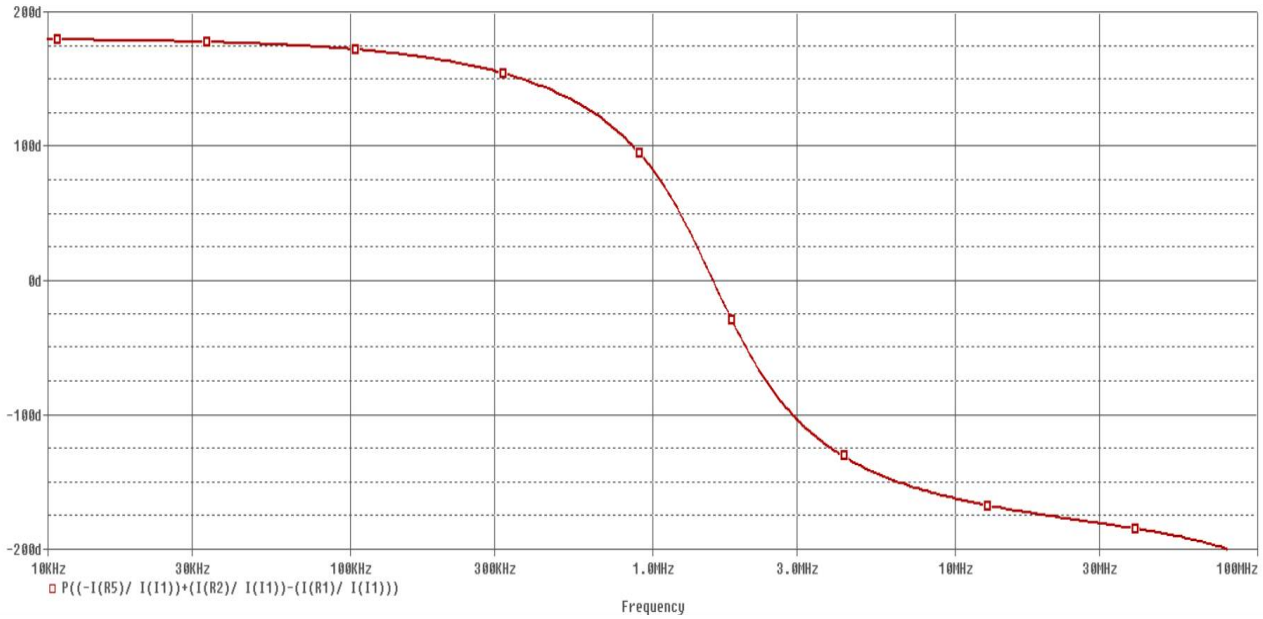


Fig. 15[f] Phase -frequency response of APF

Fig.15[a, b, c, d, e] shows frequency response of band pass, low pass, band stop and high pass filters. Fig.15[f] shows phase response of all pass filter. The plots show that simulated and ideal behavior of the structure is closely similar. The output of band pass filter is obtained which verifies independent tuning of filter parameters defined as f_0 and Q. The resistance R_1 values are selected as 6.67kΩ, 20kΩ, 33.35kΩ and 66.7kΩ which results in quality factor values as 1, 3, 5 and 10 respectively as represented in Fig.16 which thereby verifies that quality factor can be varied without varying pole frequency.

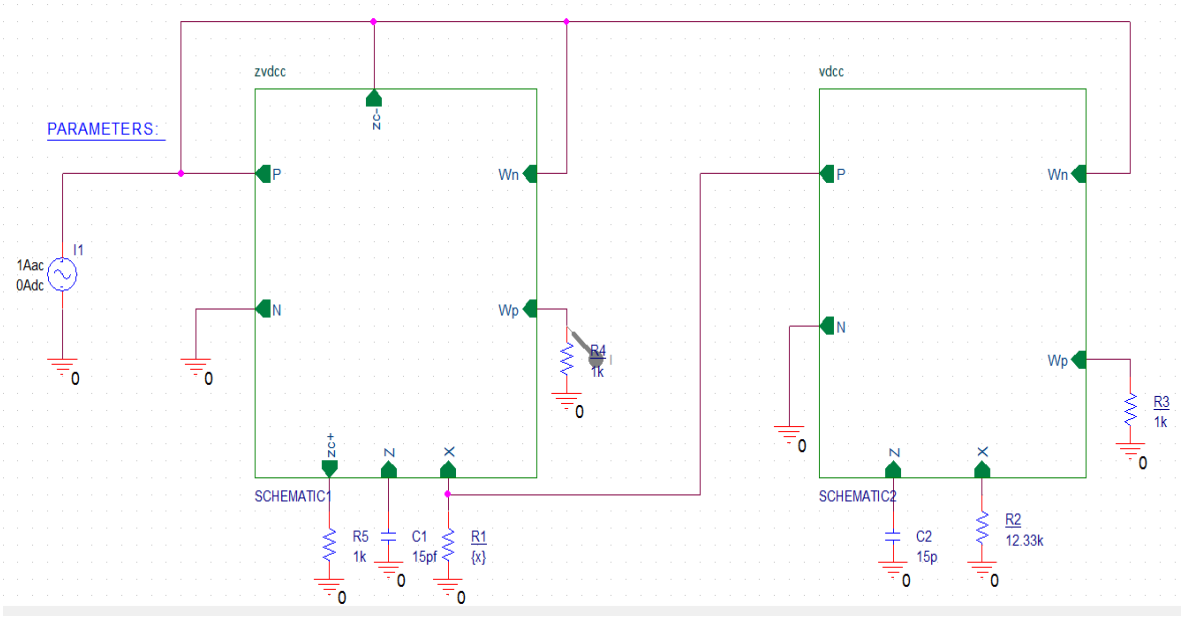


Fig.16 Quality Factor Controllability of BP Filter Output schematic [3]

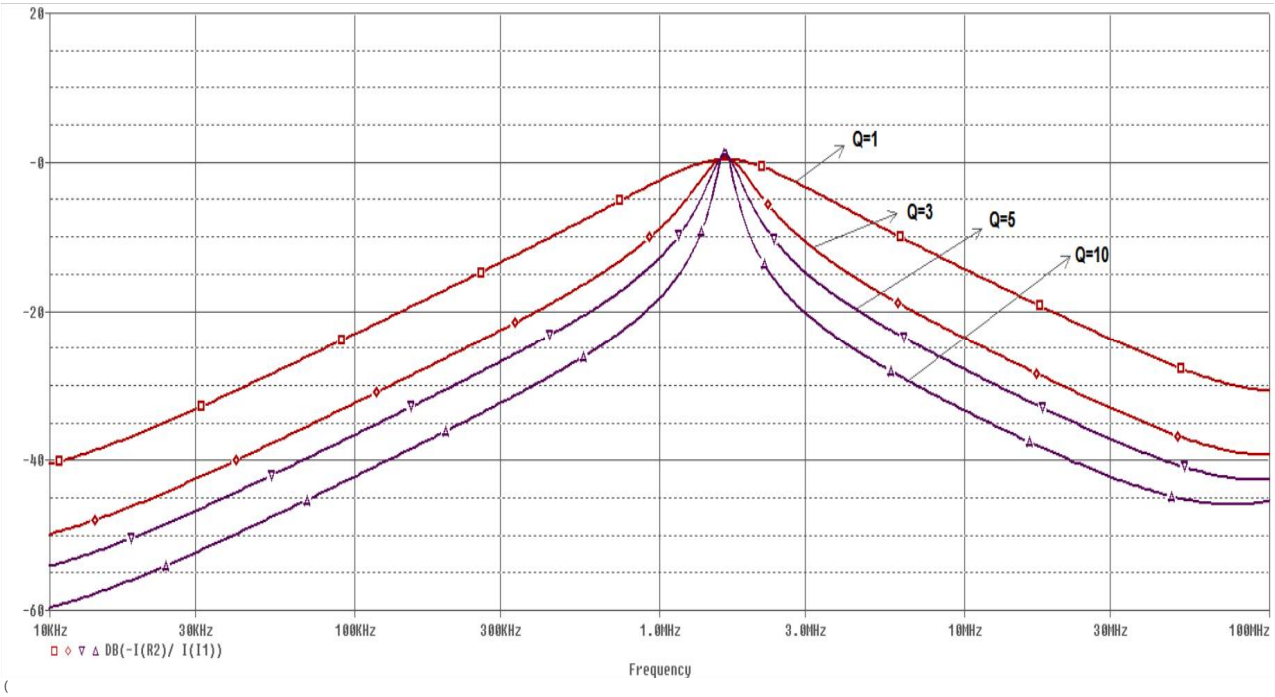


Fig. 16[a] Frequency response of Quality Factor Controllability of BP Filter Output

Chapter 5

VDCC Based TISO and SIDO Biquad Filter

5.1 Introduction

There are various voltage-mode biquad structures presented earlier by using various different active elements like current conveyor (CCI), second generation current conveyor (CCII), inverting second generation current conveyor (ICCII), four terminal floating nullors (FTFNs), current differencing buffered amplifier (CDBAs), current feedback operational amplifier (CFOAs), voltage differencing buffered amplifier (VDBA) etc. is being studied in comparison with the voltage mode biquad filters such as TISO and SIDO, they have following drawbacks

(i) They require more numbers of active components;
(ii) They use more number of passive components;
(iii) Their Pole frequency is not electronically tunable;
(iv) Quality factor depends upon frequency so it cannot be adjusted independently.

VDCC based TISO (three input single output) and SIDO (single input dual output) biquad filter circuit are presented here which uses small numbers of passive elements. The first circuit is having three inputs and single output with a single VDCC structure gives voltage mode high pass, low pass, bandpass, notch and all pass filter responses. The second circuit is having single input and dual output with a single VDCC structure gives bandpass and high pass filters responses. The third circuit is having single input and dual output with a single VDCC structure gives low pass and bandpass filter responses. Quality factor of the last two filter is adjusted by varying one resistor value only without disturbing pole frequency. Realization of whole structure uses minimum numbers of passive and active components with no passive component matching needed. All type of filters gives electronically tunable pole frequency which can be tuned by varying bias current.

5.2 TISO Biquad structure

The basic TISO (Three input single output) voltage mode biquad structure is as shown in Fig.17. It is having three inputs asV_1, V_2 and V_3 and single output V_{OUT} with passive components C_1, C_2 and G.

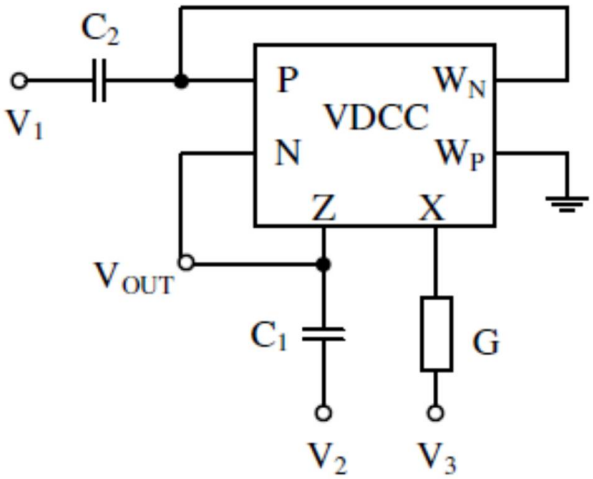


Fig.17 TISO biquad filter [4]

Analysis of the circuits gives output voltage given by

$$V_{OUT} = \frac{V_2 s^2 C_1 C_2 + V_1 sC_2 g_{m1} + V_3 g_m G}{s^2 C_1 C_2 + sC_2 g_m + g_m G}$$

Now from above equation depending on the status of voltages V_1, V_2 and V_3 in numerator there are five filters is being realized

(i) LP: $V_1 = V_2 = 0$, $V_3 = V_{IN}$
(ii) BP: $V_2 = V_3 = 0$, $V_1 = V_{IN}$
(iii) HP: $V_1 = V_3 = 0$, $V_2 = V_{IN}$
(iv) BS: $V_1 = 0$, $V_2 = V_3 = V_{IN}$
(v) AP: $V_2 = V_3 = -V_1 = V_{IN}$

Quality factor (Q)of the circuit and pole frequency can be given by

$$Q = \sqrt{\frac{GC_1}{g_m C_2}}$$

$$w_o = \sqrt{\frac{g_m G}{C_1 C_2}}$$

5.3 SIDO Biquad structure

The basic SIDO (single input dual output) voltage mode biquad structure is as shown in Fig. 18[a]. It is having a single input as V_1 and two outputs V_{01} and V_{02} with passive components C_1, C_2, G_1, and G2. There are two SIDO configurations; one of them is shown in Fig. 18[a].

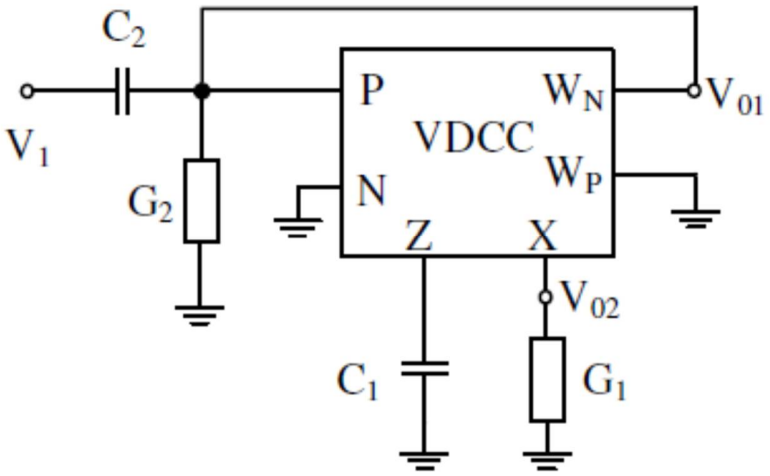


Fig. 18[a] SIDO biquad filters [4]

Analysis of the circuits gives transfer functions of high pass and bandpass filter which is given by

$$HP \rightarrow \frac{V_{01}}{V_1} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s C_1 G_2 + g_m G_1}$$

$$BP \rightarrow \frac{V_{02}}{V_1} = \frac{s C_2 g_m}{s^2 C_1 C_2 + s C_1 G_2 + g_m G_1}$$

The second SIDO configuration is shown in Fig. 18[b]. It is having similar structure as first SIDO structure except position of G_2 and C_2 are interchanged.

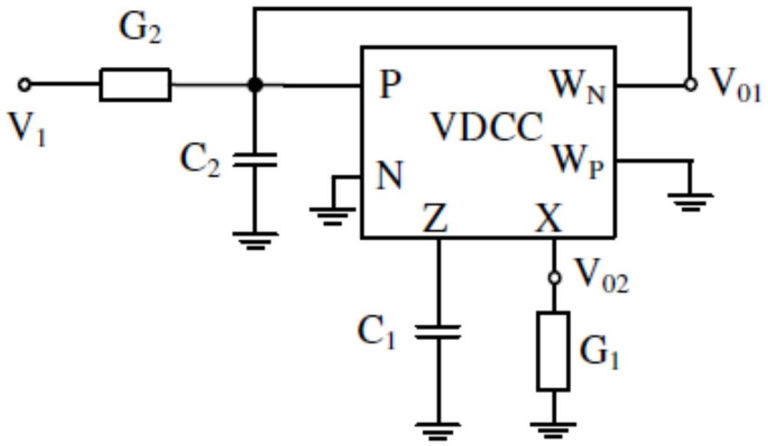


Fig. 18[b] SIDO biquad filters [4]

Analysis of the circuits gives transfer functions of bandpass and low pass filter which is given by

$$BP \rightarrow \frac{V_{01}}{V_1} = \frac{sC_1G_2}{s^2C_1C_2 + sC_1G_2 + g_mG_1}$$

$$LP \rightarrow \frac{V_{02}}{V_1} = \frac{g_mG_2}{s^2C_1C_2 + sC_1G_2 + g_mG_1}$$

Quality factor (Q) and pole frequency ($\boldsymbol{\omega}_o$) of the two filters are given by

$$Q = \frac{1}{G_2}\sqrt{\frac{g_mG_1C_2}{C_1}}$$

$$\omega_o = \sqrt{\frac{g_mG_1}{C_1C_2}}$$

From the above equations, it is clear that above filter is useful for obtaining high quality factor, now to obtain high Q value select G_2 value low from above equations indicates inverse relation between G_2 and Q. Further, G_2 can be adjusted electronically by control voltage by employing NMOS transistors.

5.4 Parasitic Impedances Effect in VDCC

In order to analyze the performance of the filter, parasitic impedance effects on quality factor and pole frequency is also taken into consideration. First, analysis of TISO biquad filter is taken into consideration and the modified circuit diagram of the TISO voltage mode biquad is as shown in Fig.19. From figure port W_N is having high parasitic resistance R_{P2} in parallel with the low capacitance C_{P2}, port X is having low parasitic resistance R_{P1} and port Z is having high parasitic resistance R_{P3}. All of these parasitic elements taken into care, Transfer function of TISO biquad with parasitic effect is:

$$V_{OUT} = V_2 \frac{s^2 C_1 C_{T2} + sC_1 G_{P2}}{\Delta s} + V_1 \frac{sC_2 g_{m1}}{\Delta s} + V_3 \frac{g_m G_1}{\Delta s}$$

Here $C_{T2}=C_2+C_{P2}$ and Δs is the characteristic equation given as:

$$\Delta s = s^2 C_1 C_{T2} + s(C_{T2}(g_m + G_{P3}) + C_1 G_{P2}) + g_m G_1 + G_{p2}(g_m + G_{P3})$$

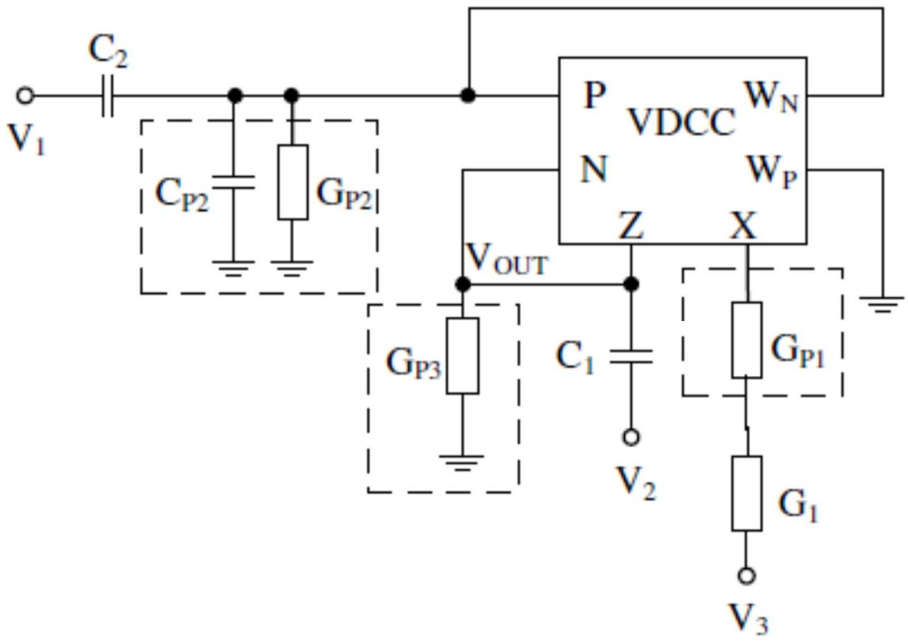


Fig.19 Parasitic impedance of VDCC affecting filter of Fig.17 [4]

From the denominator of the transfer function equations for Q' and ω_0' considering the parasitic effects are given by:

$$Q' = \frac{\sqrt{C_1 C_{T2}}\sqrt{g_m G_1 + G_{p2}(g_m + G_{P3})}}{C_{T2}(g_m + G_{P3}) + C_1 G_{P2}}$$

$$w_O' = \sqrt{\frac{g_m G_1 + G_{p2}(g_m + G_{P3})}{C_1 C_{T2}}}$$

Now under these circumstances simulation shows that transconductance value g_m=277μA/V for VDCC and the parasitic capacitance and resistances are C_{P2}=0.92pF and R_{P1}=43Ω, R_{P2}=141kΩ, R_{P3}=362kΩ respectively. Now from the above observations parasitic effects can be minimum on Q' and ω_0' if G_{P2}, G_{P3} selects smaller as compare to g_m and G.

5.5 Simulation Results

A CMOS based VDCC is shown in Fig.3. Here, supply voltages are chosen as $V_{DD}=-V_{SS}=0.9V$, and biasing currents are $I_{B1}=50\mu A$ and $I_{B2}=100\mu A$. Widths to Length (W/L) ratio of the transistors are given in Table 3. To verify the functionality of the filter circuit, circuit is simulated using PSPICE software using TSMC 180nm technology parameter.

The TISO voltage mode biquad is shown in Fig.17**,** It is designed for pole frequency $f_0=1.165$ MHz and quality factor of Q=1.34 by selecting $R_1=2k\Omega$ and $C_1=C_2=50pF$ and transconductance gain $g_m=277\mu A/V$. Simulation response of low pass, high pass, bandpass, notch and all pass filters are shown in Figures from Fig.20 to Fig.24 and their parasitic effect simulation response are shown from Fig.25 to Fig.29.

The SIDO voltage mode biquad is shown in Fig.18(a and b). These two SIDO biquad is designed for pole frequency $f_0=1.165$ MHz and quality factor of Q=1.86 by selecting $R_1=2k\Omega$, $R_2=5\ k\Omega$ and $C_1=C_2=50pF$ and transconductance gain $g_m=277\mu A/V$. Simulation response of bandpass and high pass for first SIDO biquad and bandpass and low pass for second SIDO biquad is shown in figures from Fig.30 to Fig.33.

Table 3

Transistors	W/L(μm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{17}	14.4/0.72
M_{18}-M_{22}	0.72/0.72

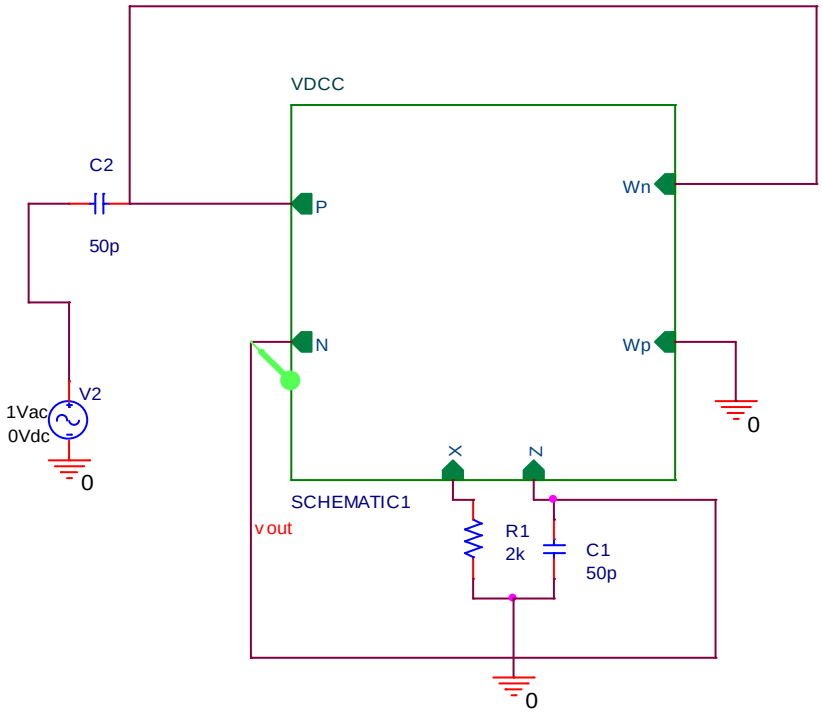


Fig.20 TISO biquad filter (BPF) [4]

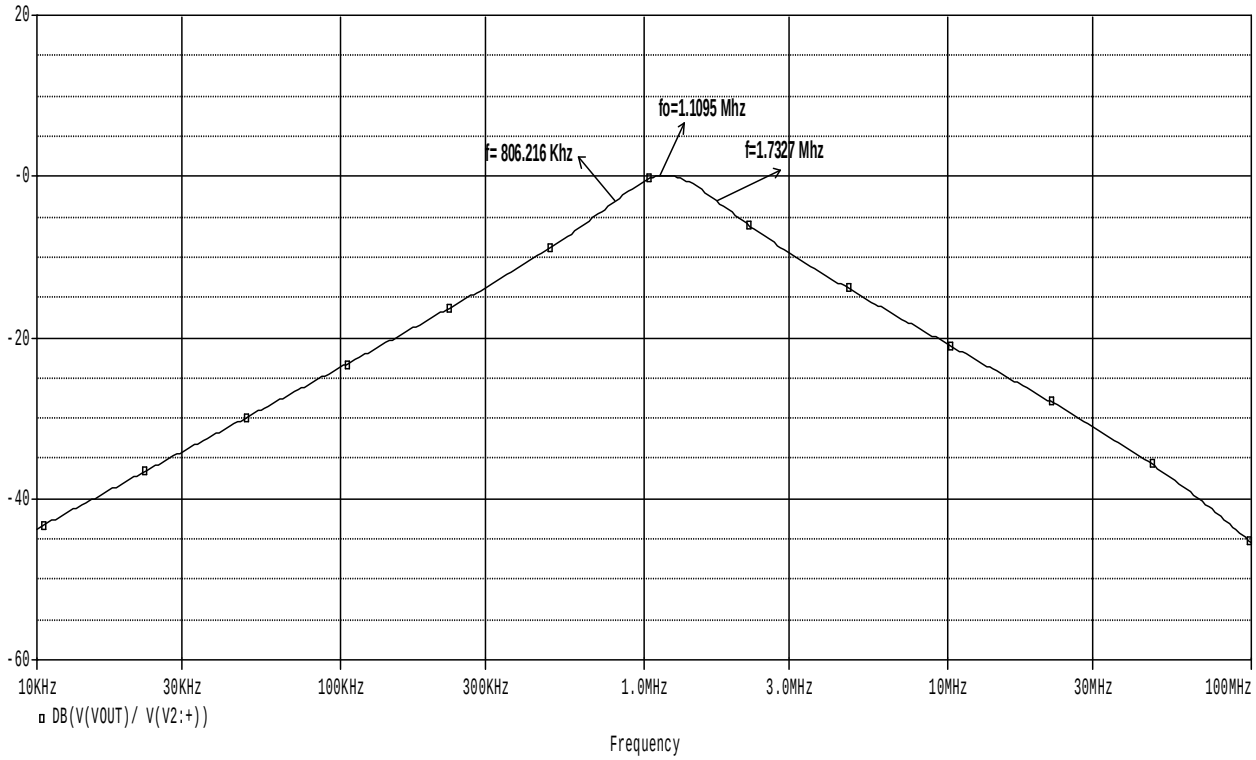


Fig. 20[a] Frequency response of BPF

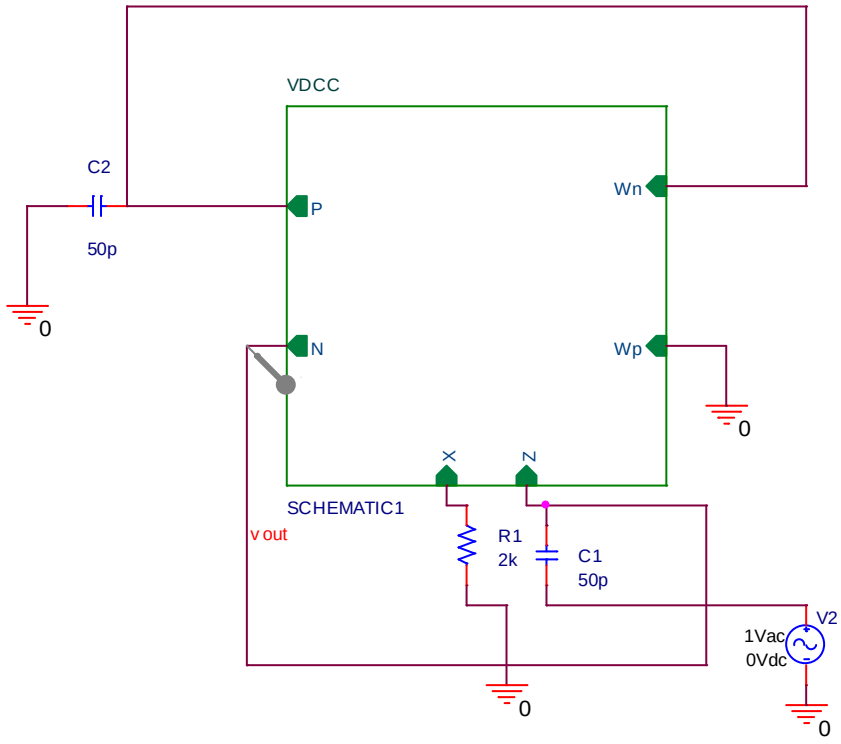


Fig. 21 TISO biquad filter (HPF) [4]

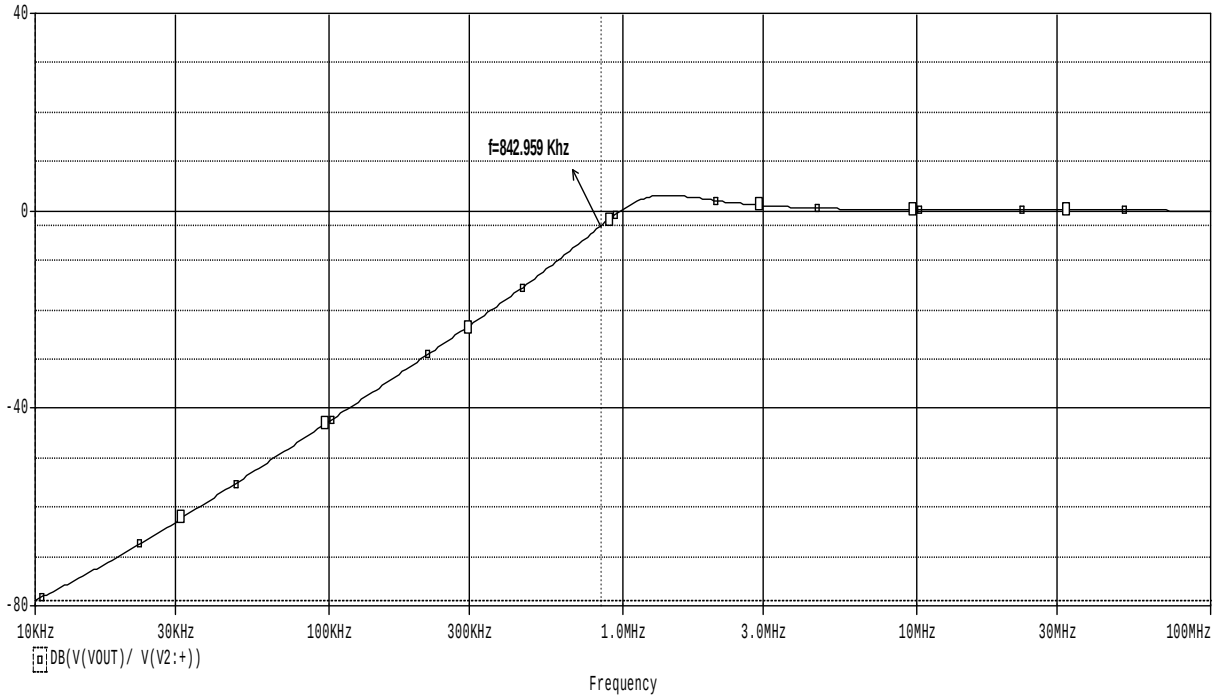


Fig. 21[a] Frequency response of HPF

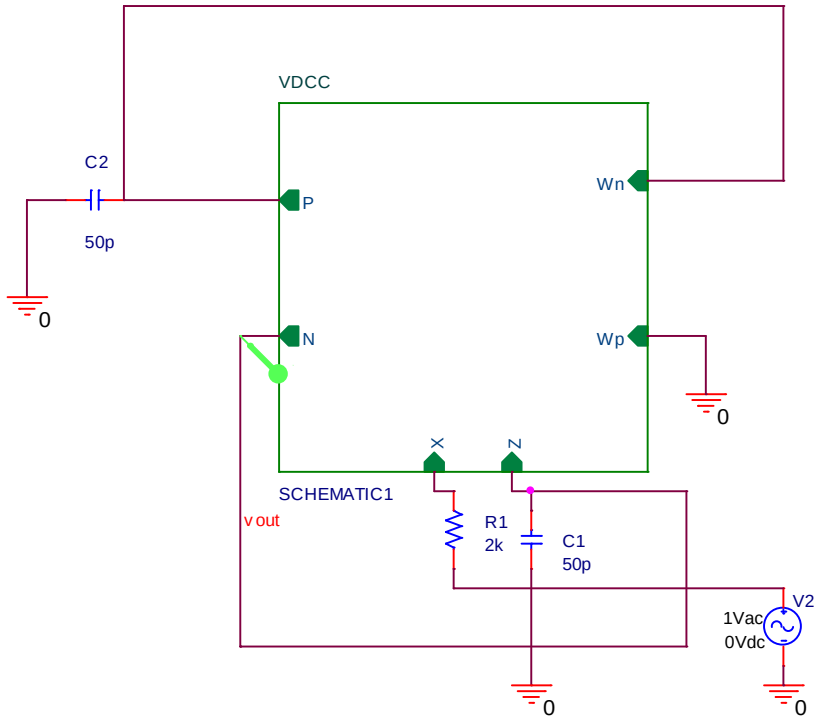


Fig.22 TISO biquad filter (LPF) [4]

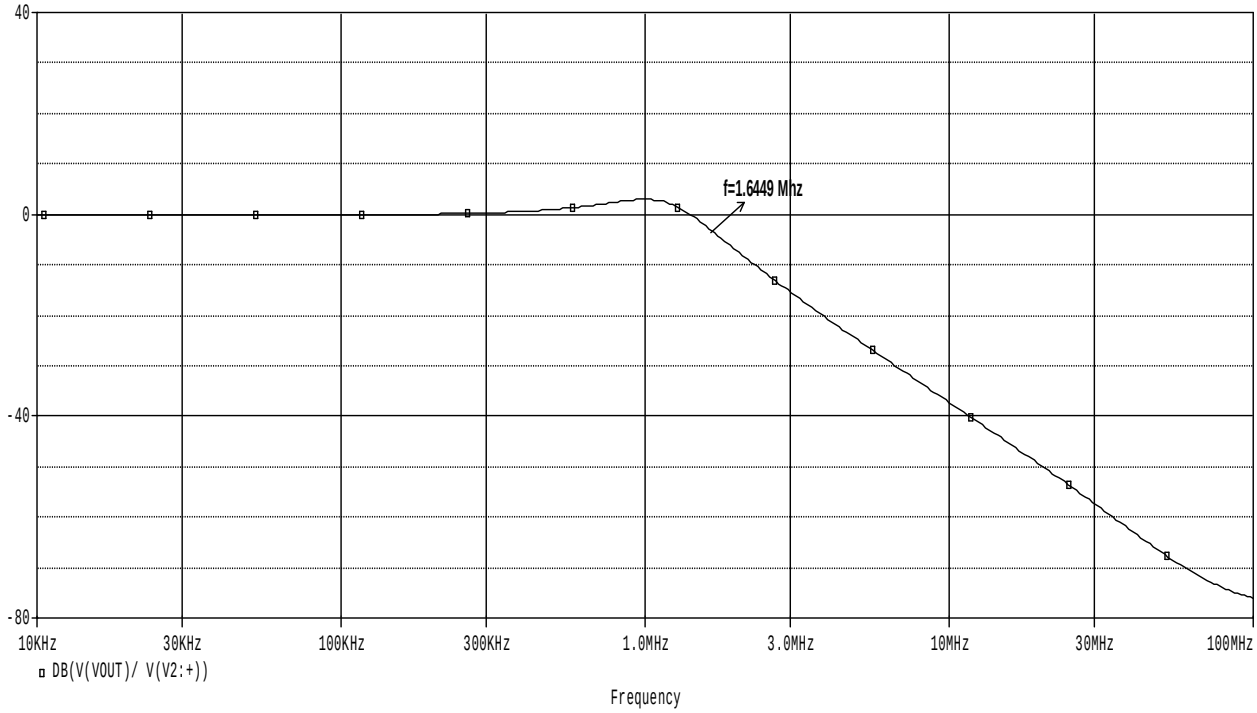


Fig. 22[a] Frequency response of LPF

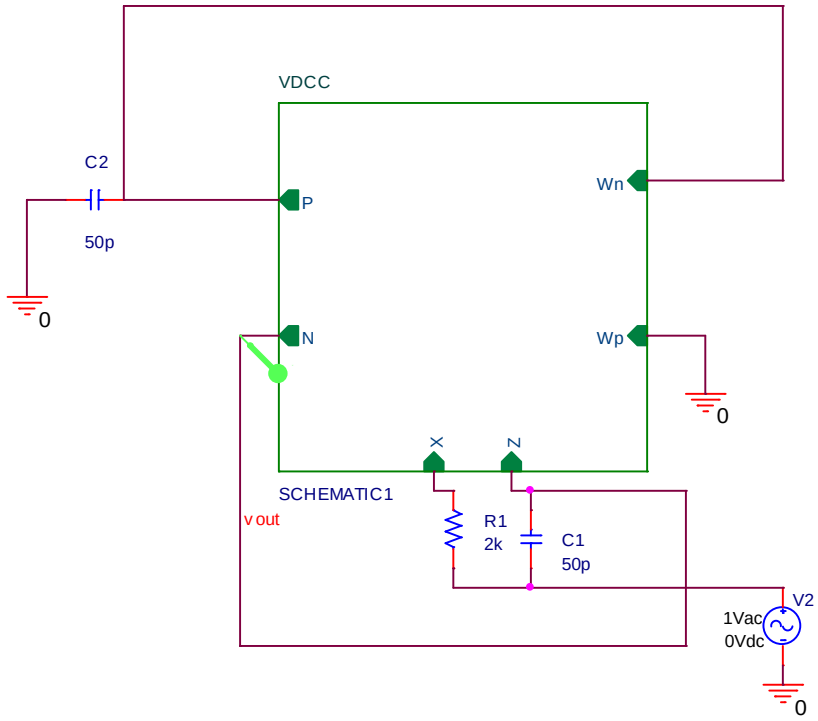


Fig.23 TISO biquad filter (BSF) [4]

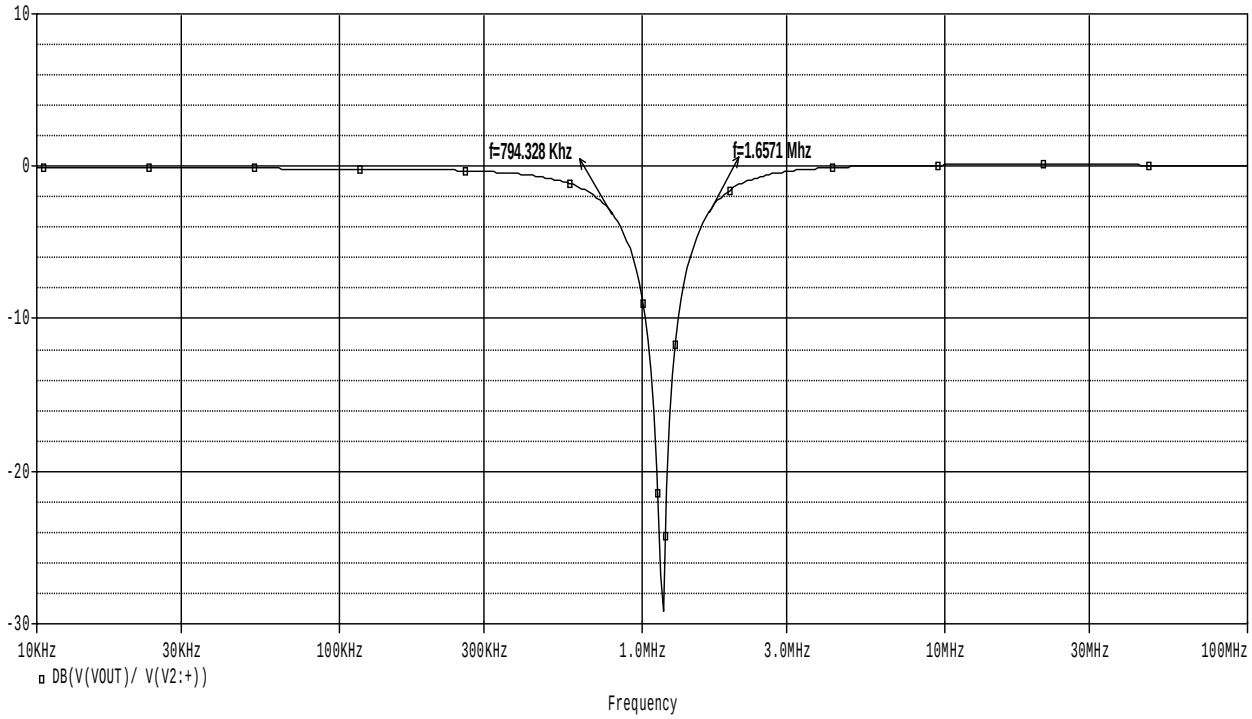


Fig. 23[a] Frequency response of BSF

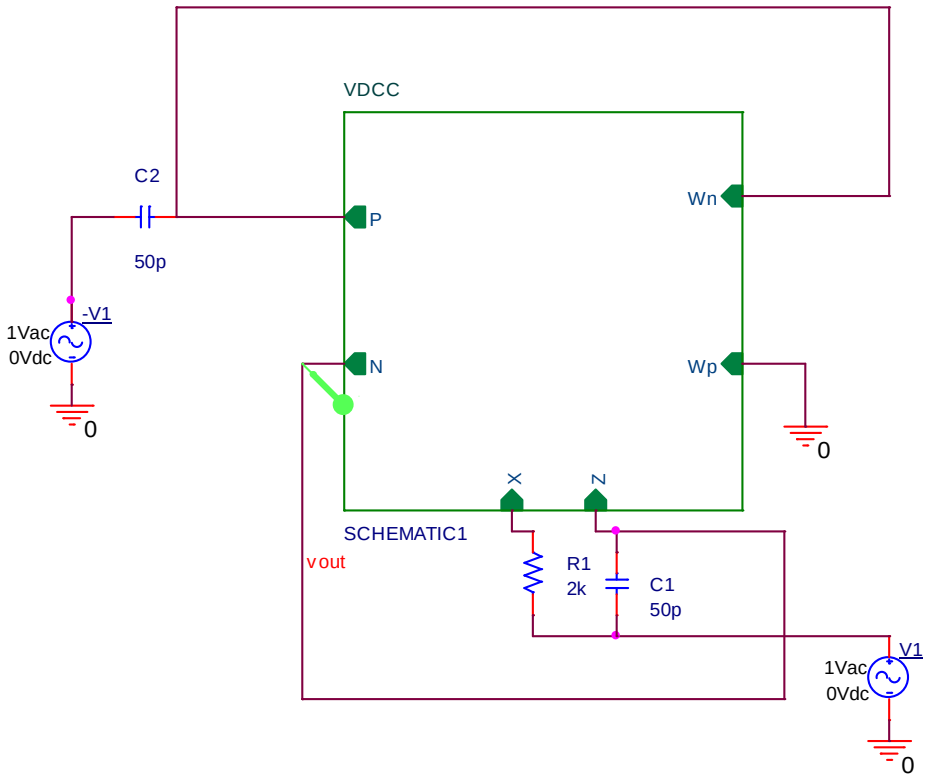


Fig. 24 TISO biquad filter (APF) [4]

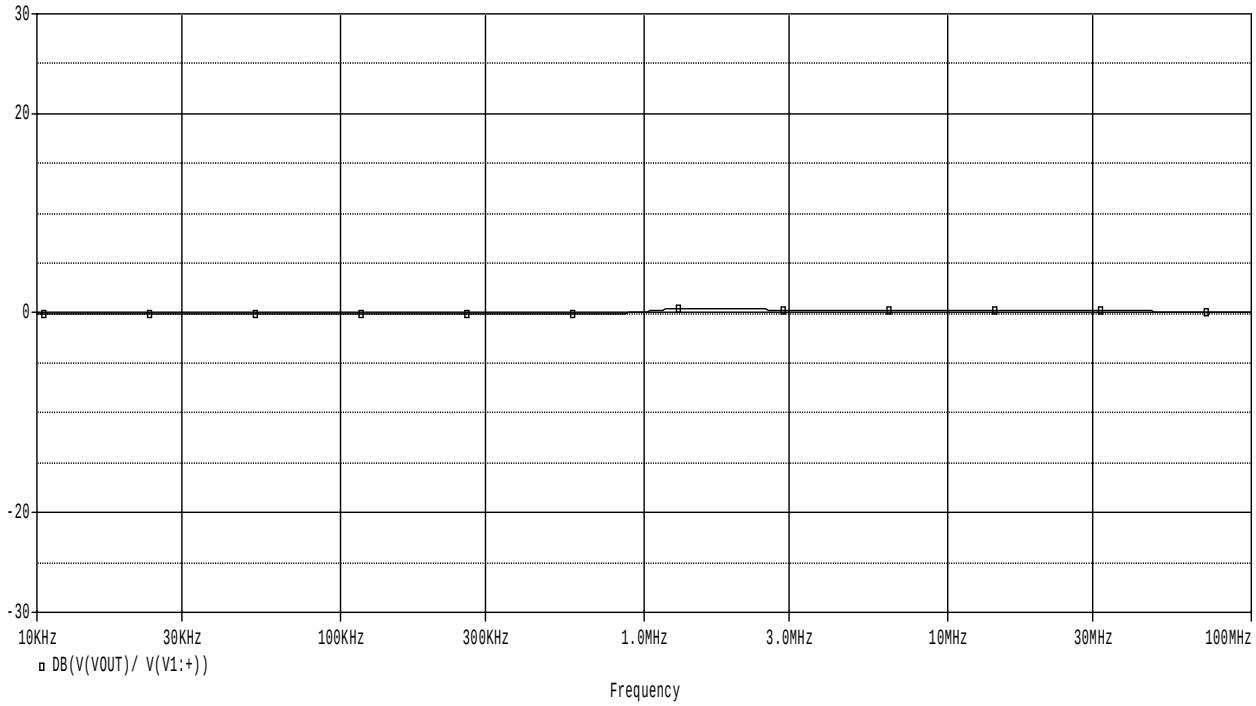


Fig. 24[a] Frequency response of APF

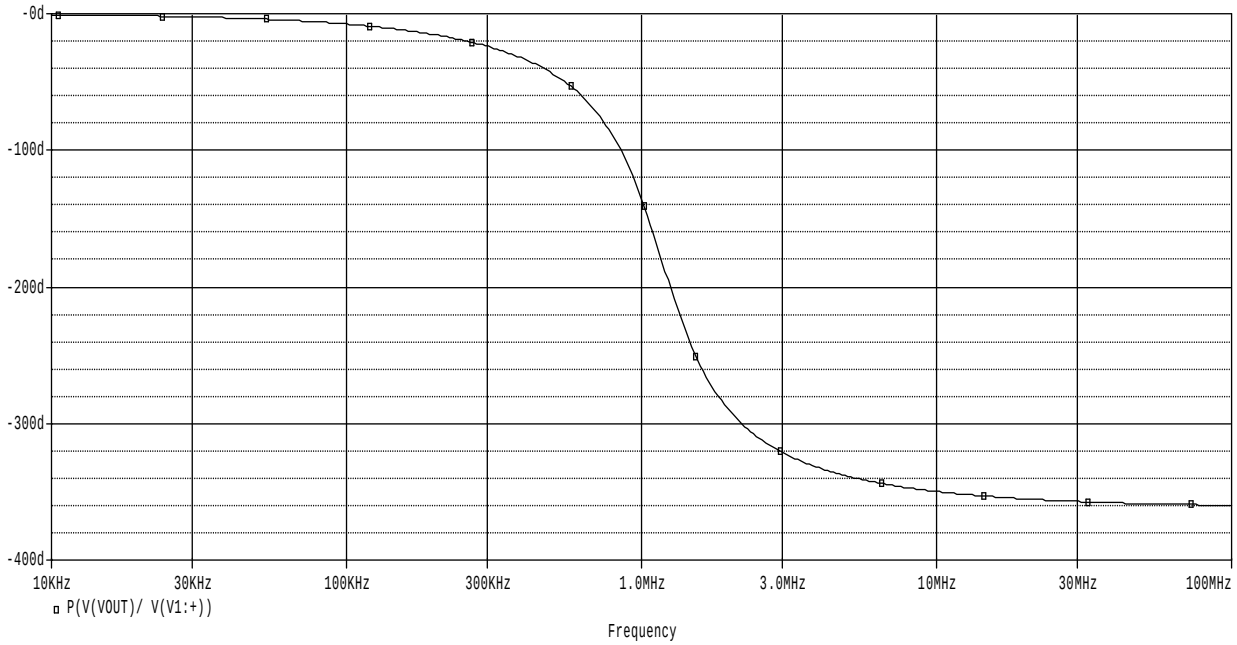


Fig. 24[b] Phase-frequency response of APF

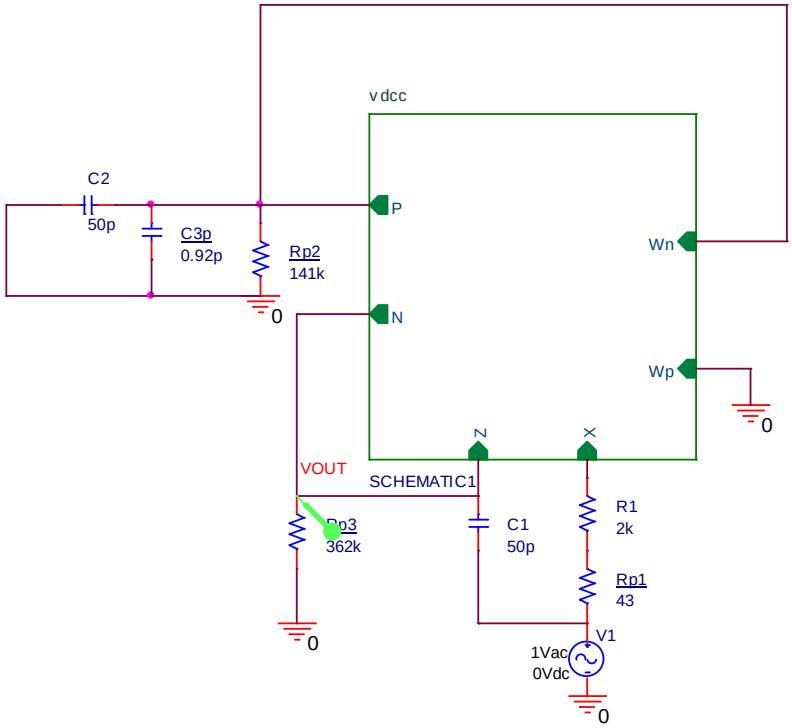


Fig. 25 TISO biquad filter with Parasitic impedance (BSF) [4]

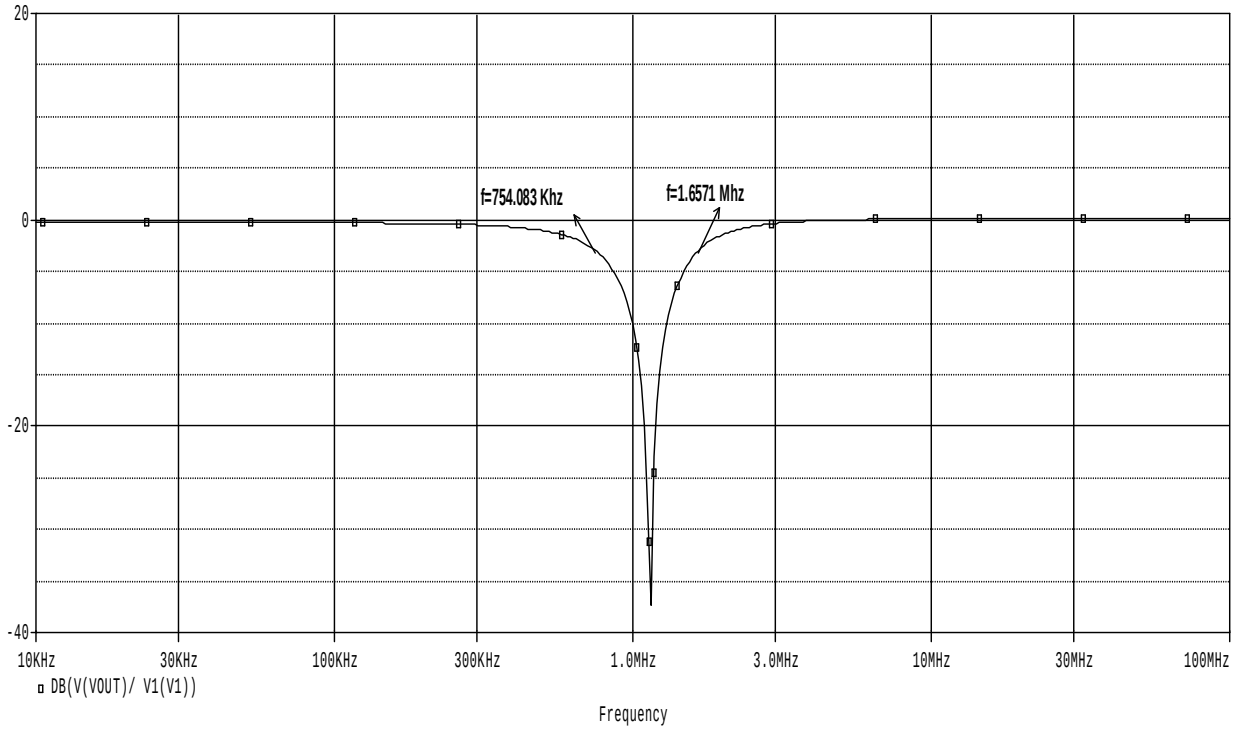


Fig. 25[a] Frequency response of BSF

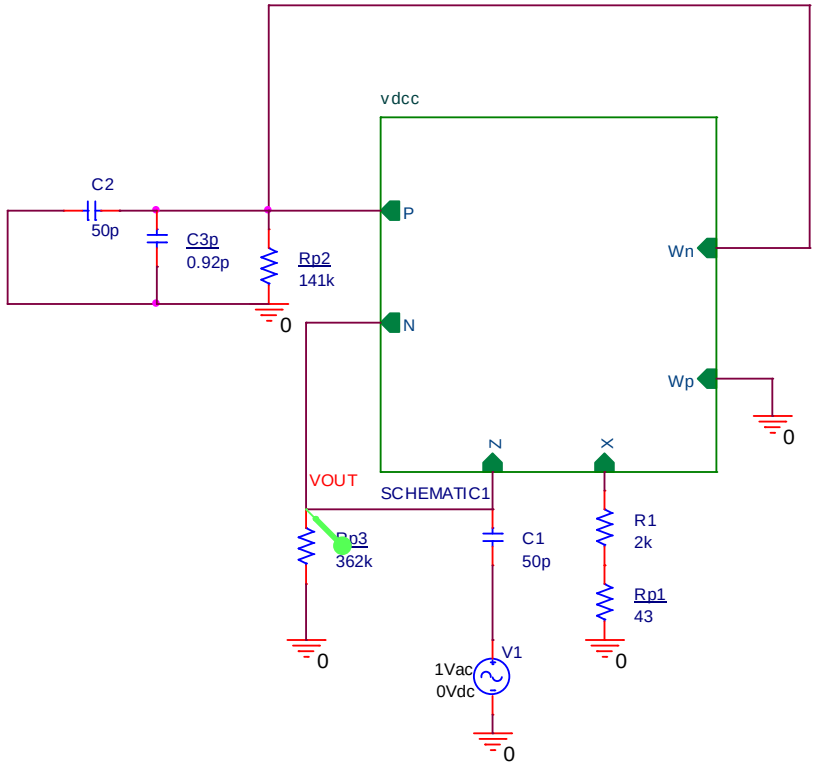


Fig.26 TISO biquad filter with Parasitic impedance (HPF) [4]

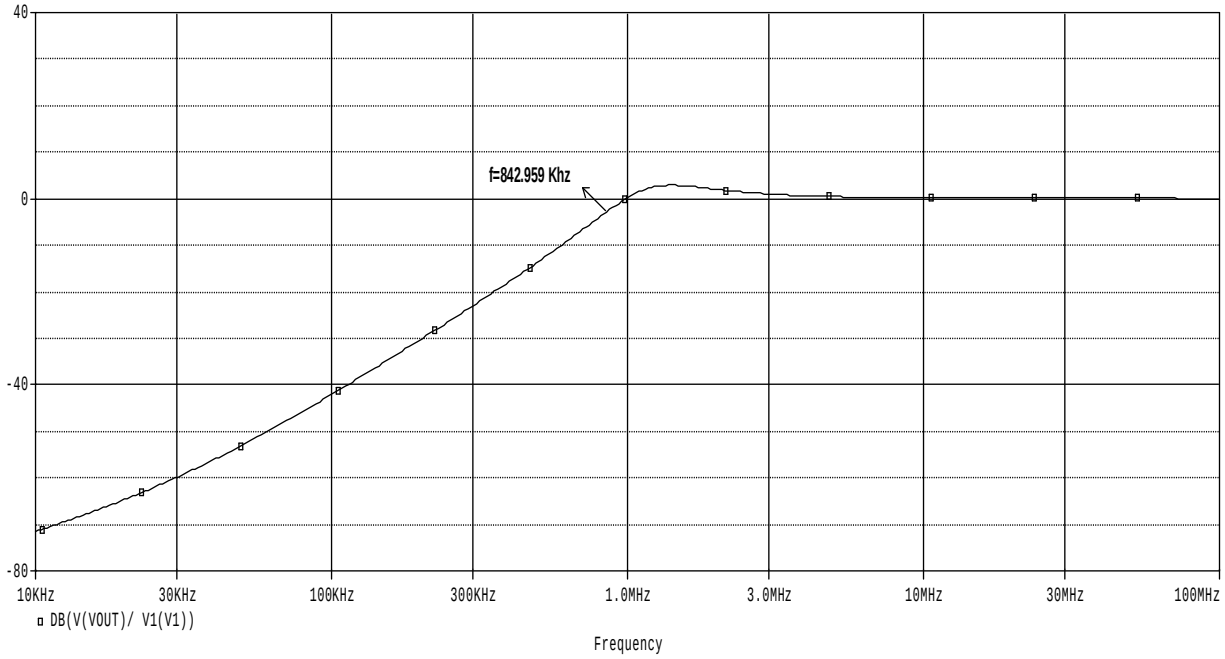


Fig. 26[a] Frequency response of HPF

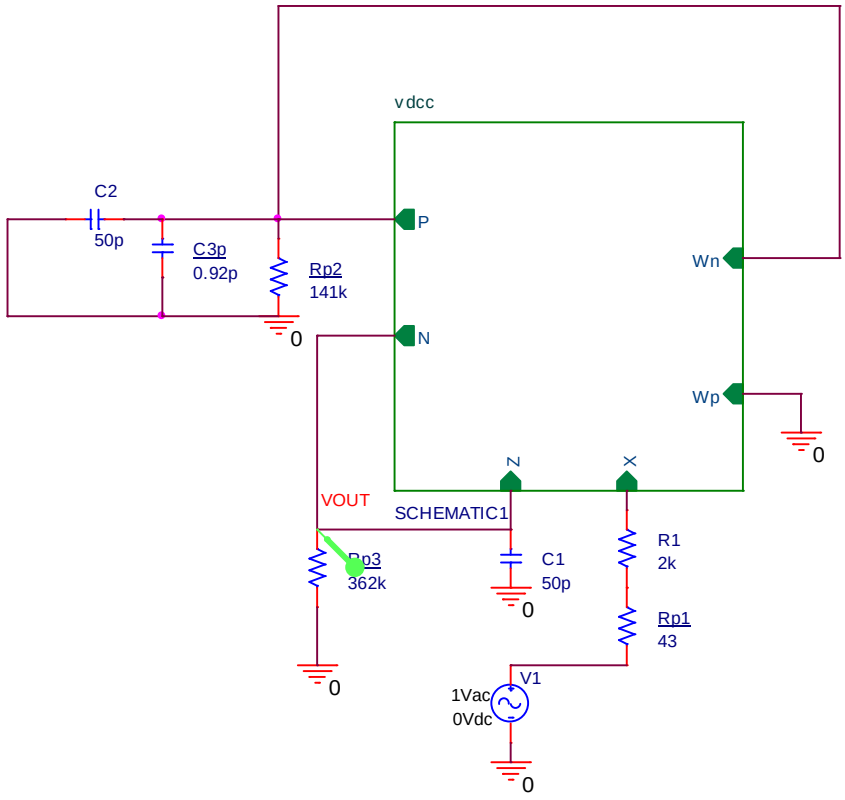


Fig.27 TISO biquad filter with Parasitic impedance (LPF) [4]

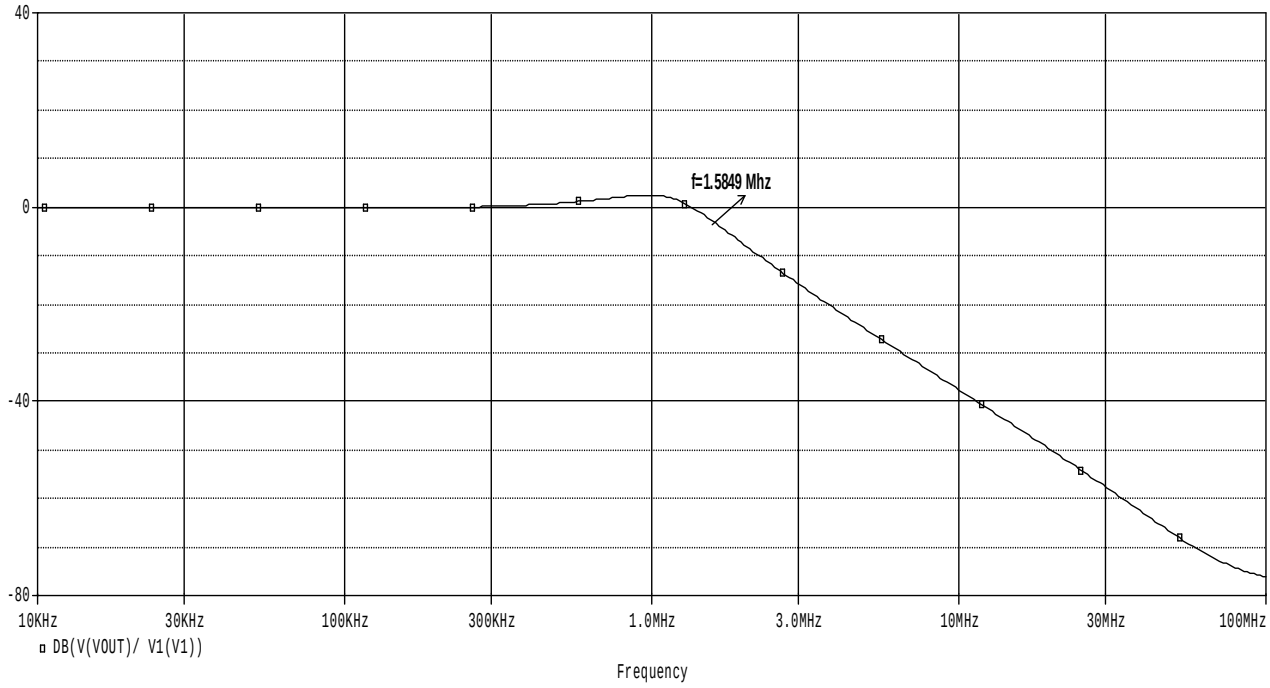


Fig. 27[a] Frequency response of LPF

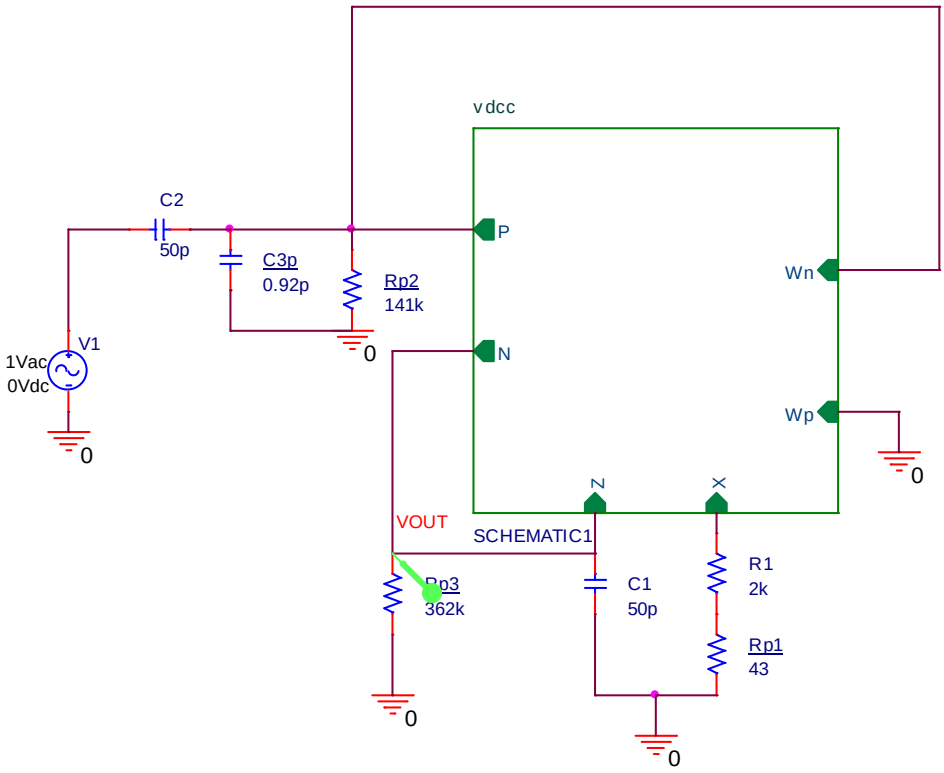


Fig.28 TISO biquad filter with Parasitic impedance (BPF) [4]

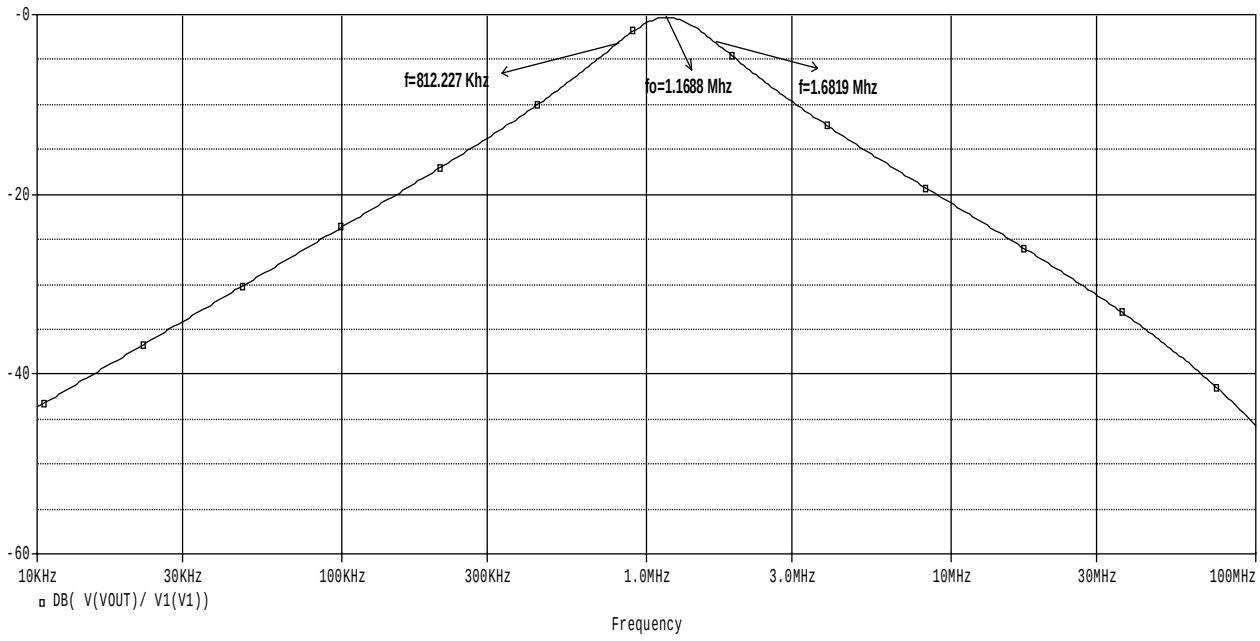


Fig. 28[a] Frequency response of BPF

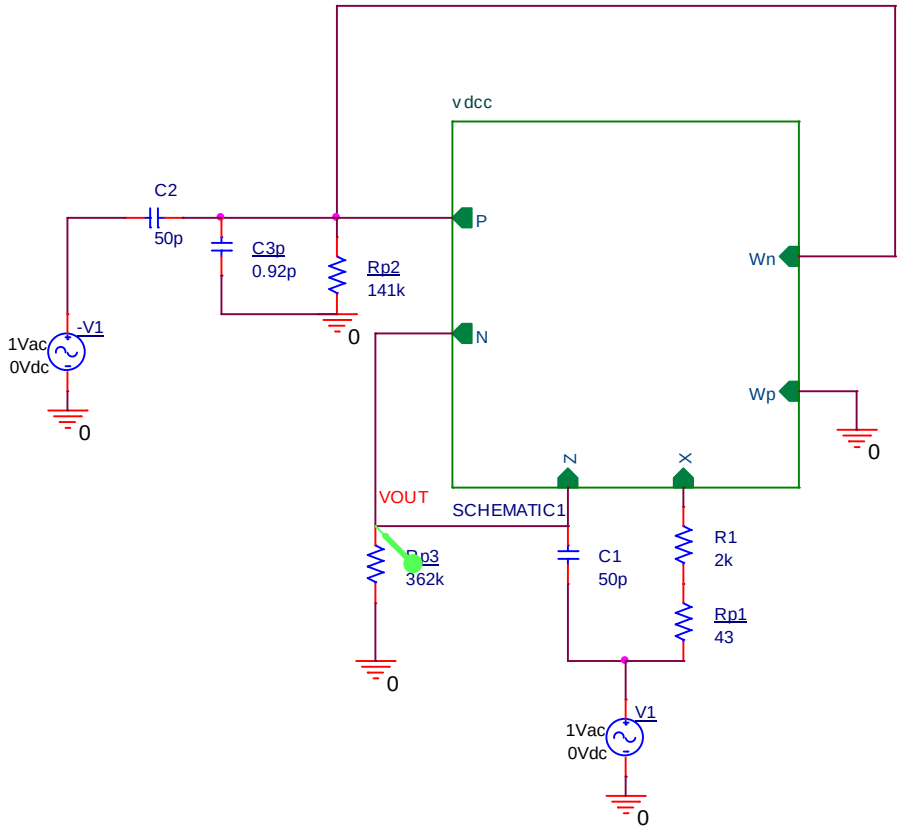


Fig.29 TISO biquad filter with Parasitic impedance (APF) [4]

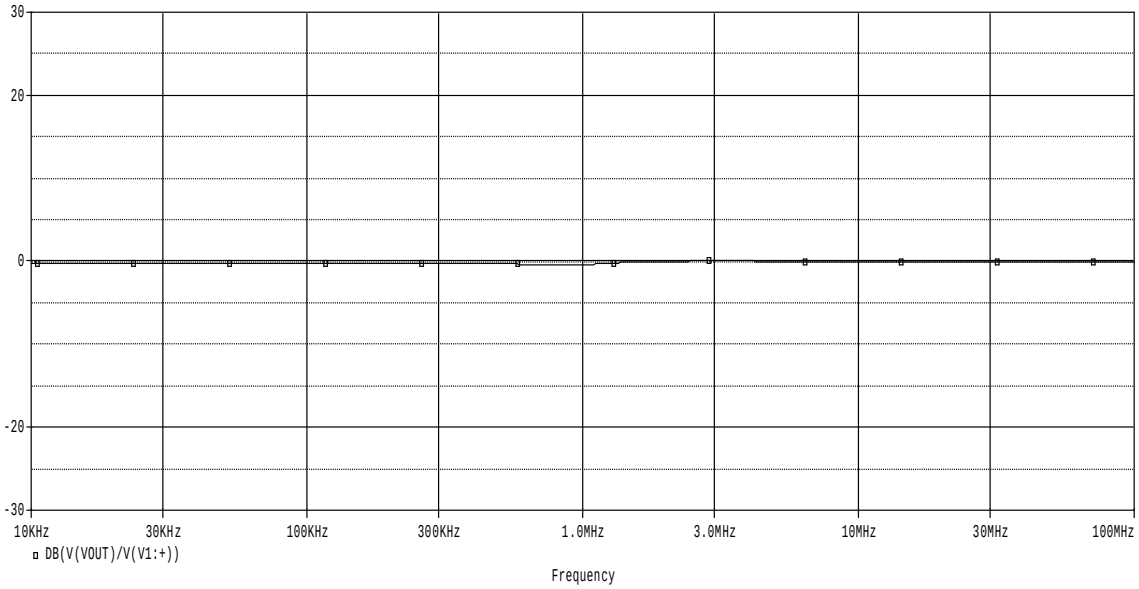


Fig. 29[a] Frequency response of APF

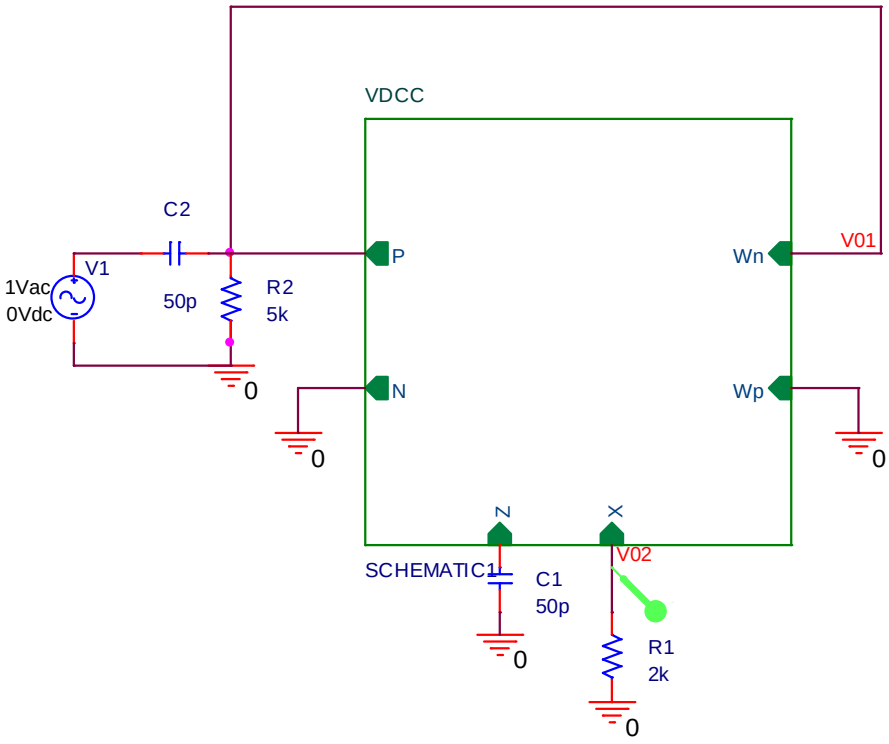


Fig.30 SIDO biquad filters (BPF) [4]

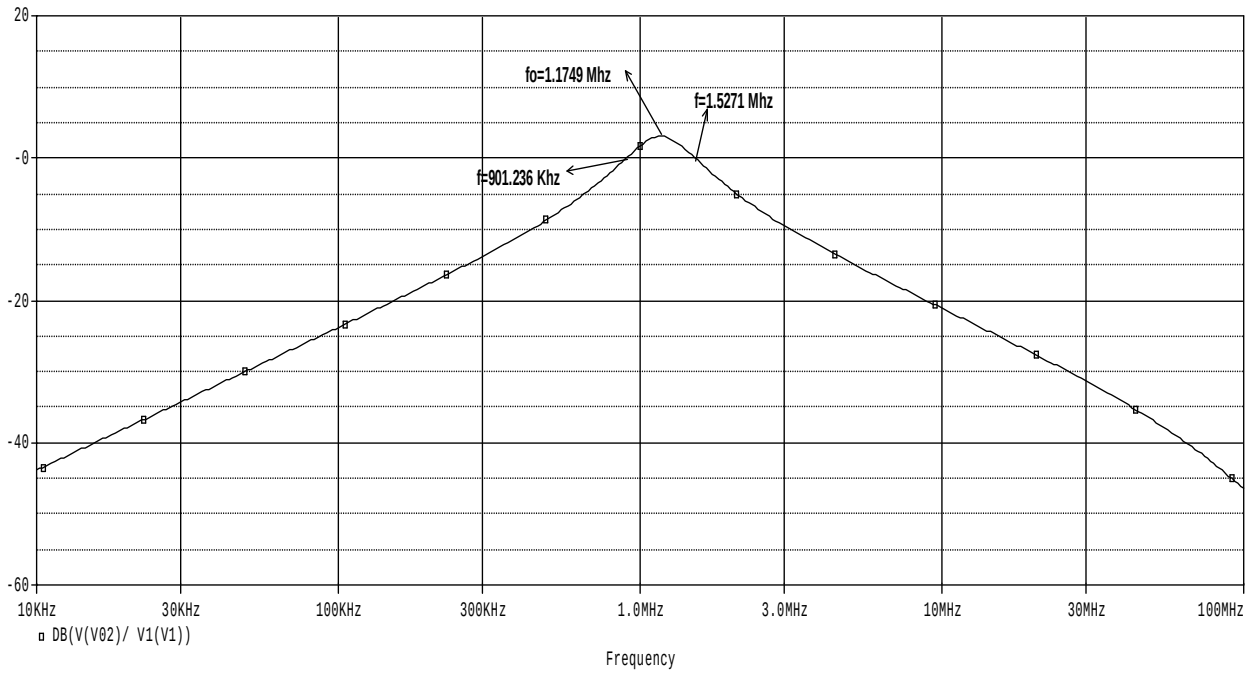


Fig. 30[a] Frequency response of BPF

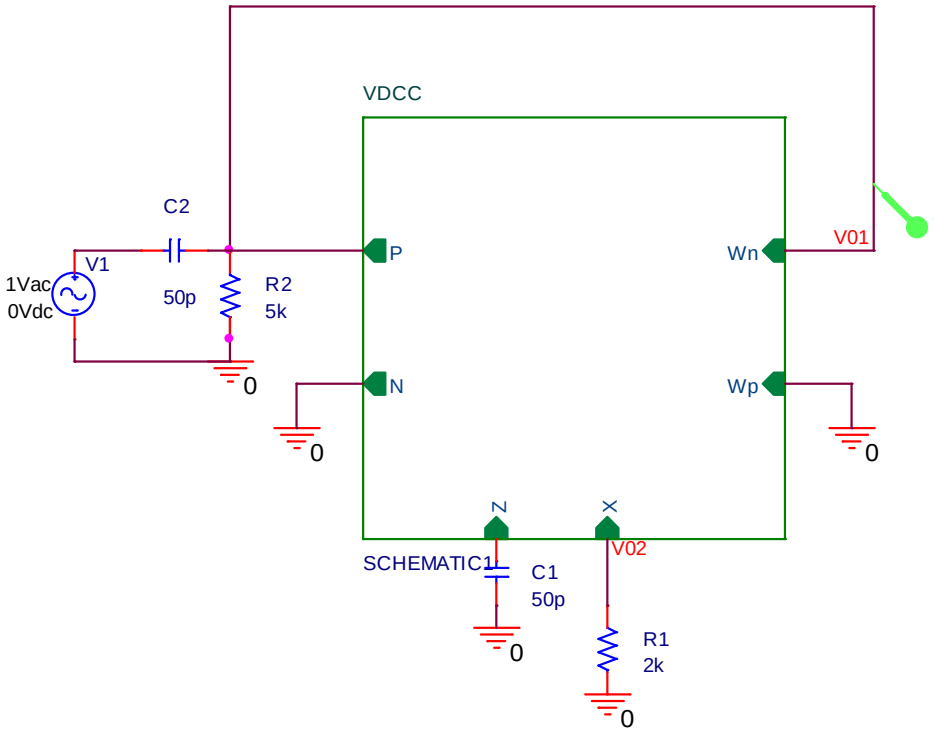


Fig.31 SIDO biquad filters (HPF) [4]

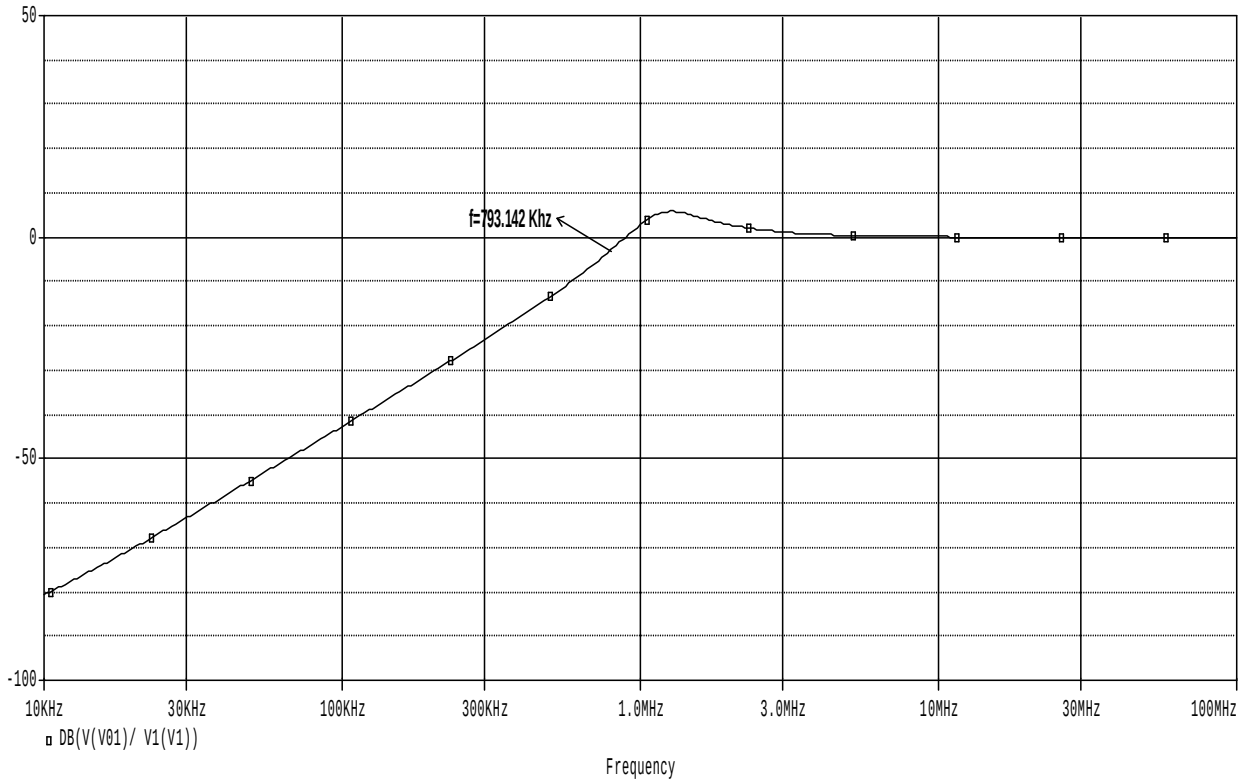


Fig. 31[a] Frequency response of HPF

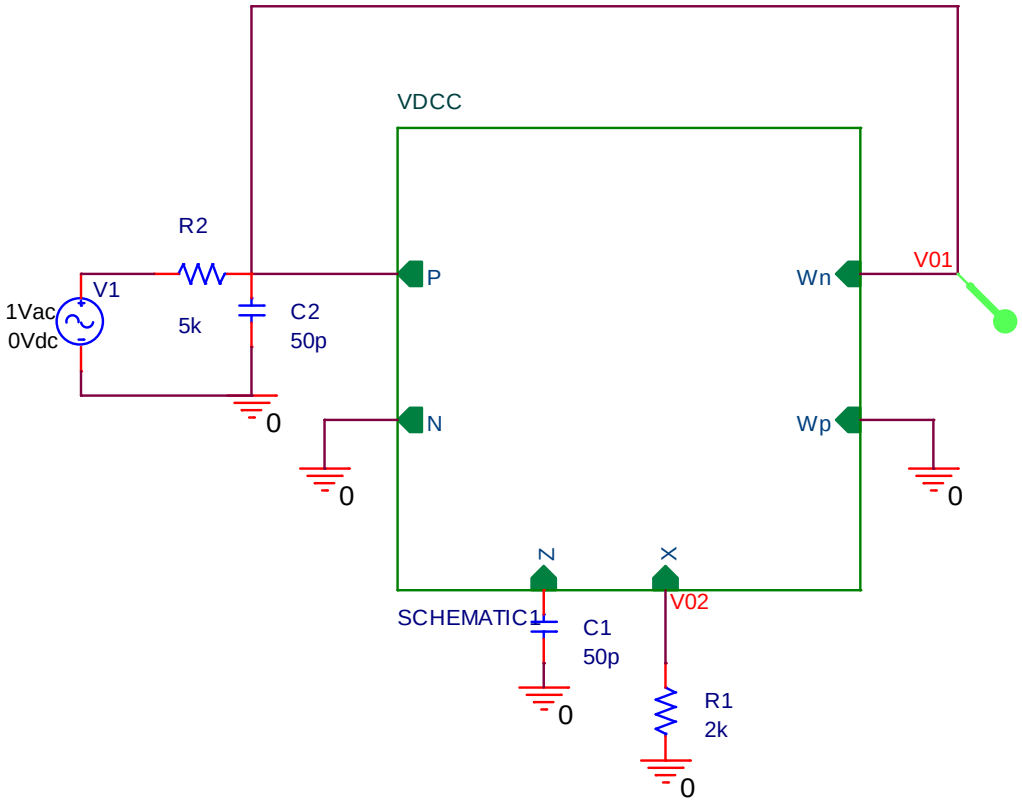


Fig.32 SIDO biquad filters (BPF) [4]

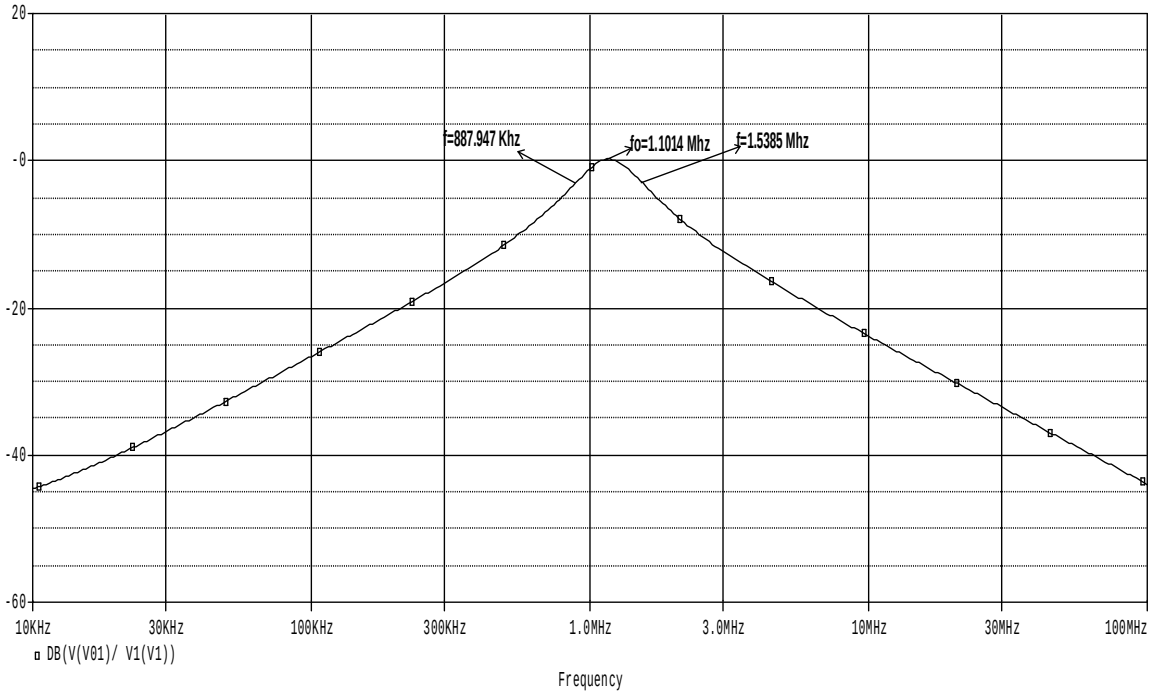


Fig. 32[a] Frequency response of BPF

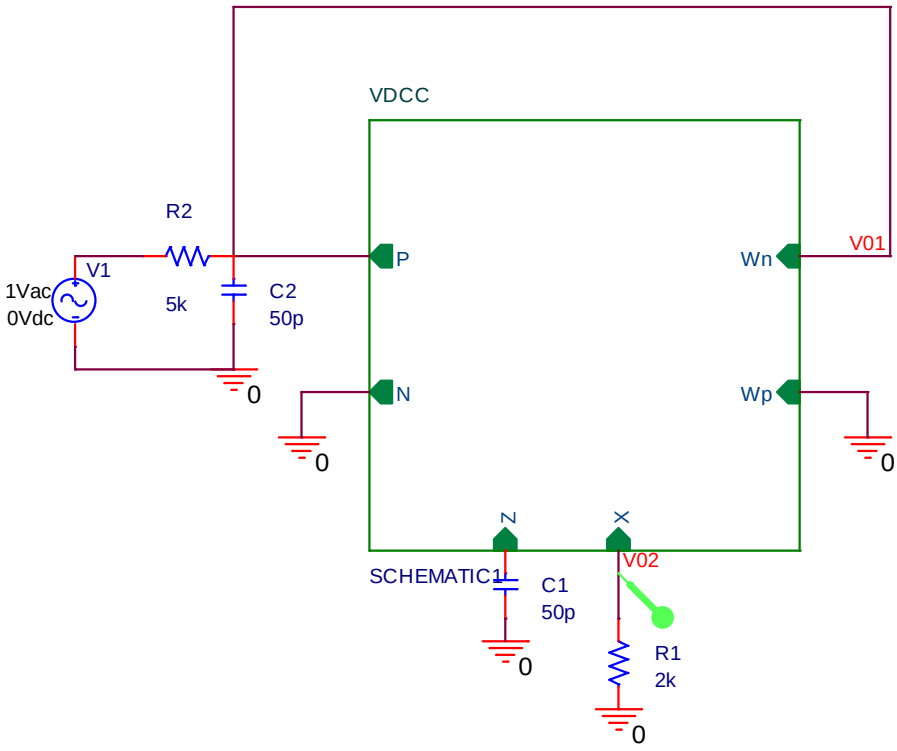


Fig.33 SIDO biquad filters (LPF) [4]

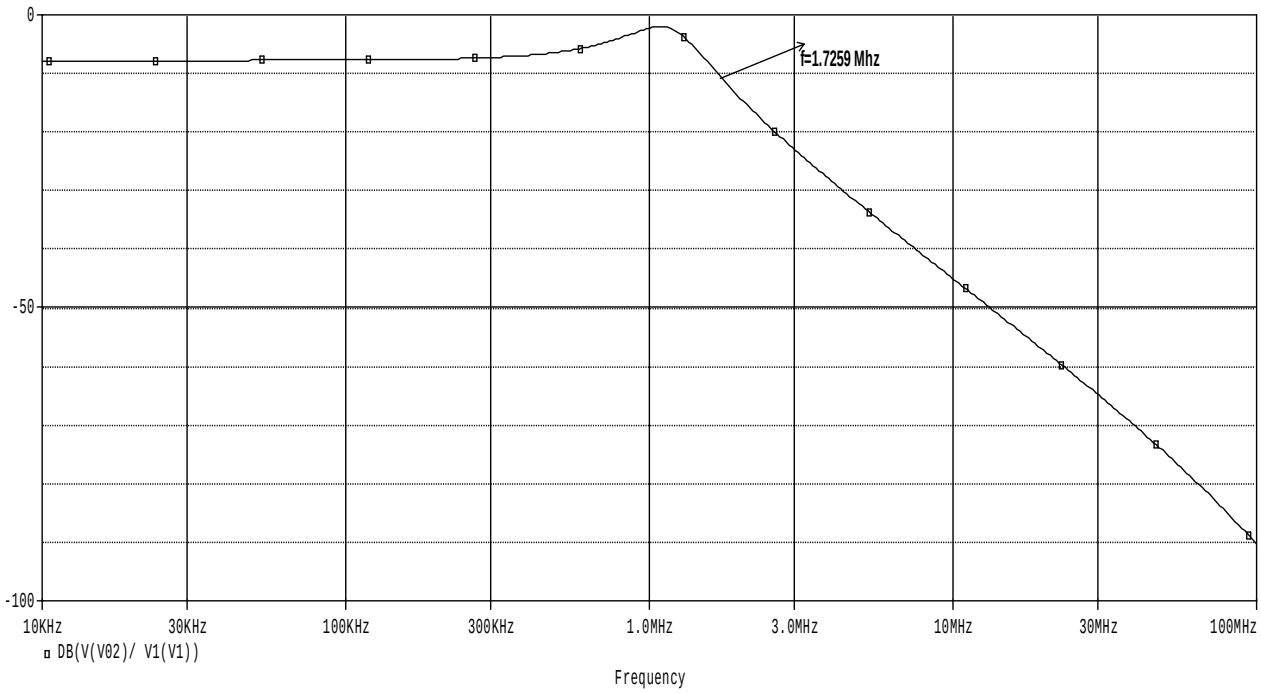


Fig. 33[a] Frequency response of LPF

Chapter 6

VDCC based Inductance Simulator and Third-order High-Pass Butterworth Filter

6.1 Introduction

Inductance realization in integrated circuits creates various difficulties in electronics circuits. At high frequency inductance simulators are used in place of passive inductance due to several reasons such as passive inductors spread magnetic energy and cause more parasitic effect than other elements and its bulkiness in IC. There are several types of floating and grounded inductance simulator is being implemented by using various active blocks such as operational amplifiers, current conveyors, current controlled conveyors, current feedback operational amplifiers, current differencing buffered amplifiers (CDBA) etc. In contrast previously introduced inductance simulators are suffered from the following drawbacks:

1. Requires matching condition for passive components.
2. Use of more number of passive components.
3. Use of more numbers of passive components

Recently there are various numbers of active blocks are introduced, Voltage Differencing Current Conveyor (VDCC) is one of the active blocks which provides electronically tunable transconductance gain and it transfers both current and voltage in its respective terminals and it is also used in designing of several types of active filters and inductance simulators.

6.2 VDCC based Inductance Simulator structure

VDCC based inductance simulator is as shown in Fig.34. It uses a single VDCC structure with one grounded resistor and capacitor. P and W_N terminal of the VDCC is grounded as shown.
Inductor which is shown in Fig.34 is a grounded inductor. Floating inductor structure is also shown in Fig.35, which also use a single VDCC structure with one resistor and capacitor.

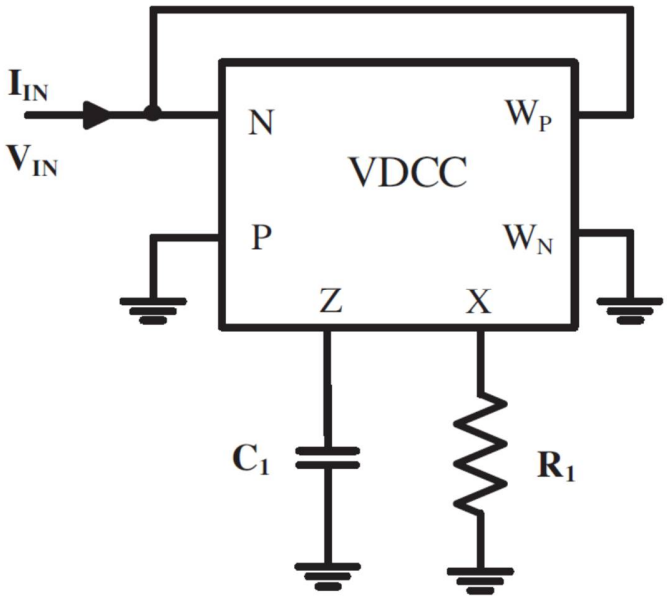


Fig.34 Inductance simulator using single VDCC (grounded inductor) [5]

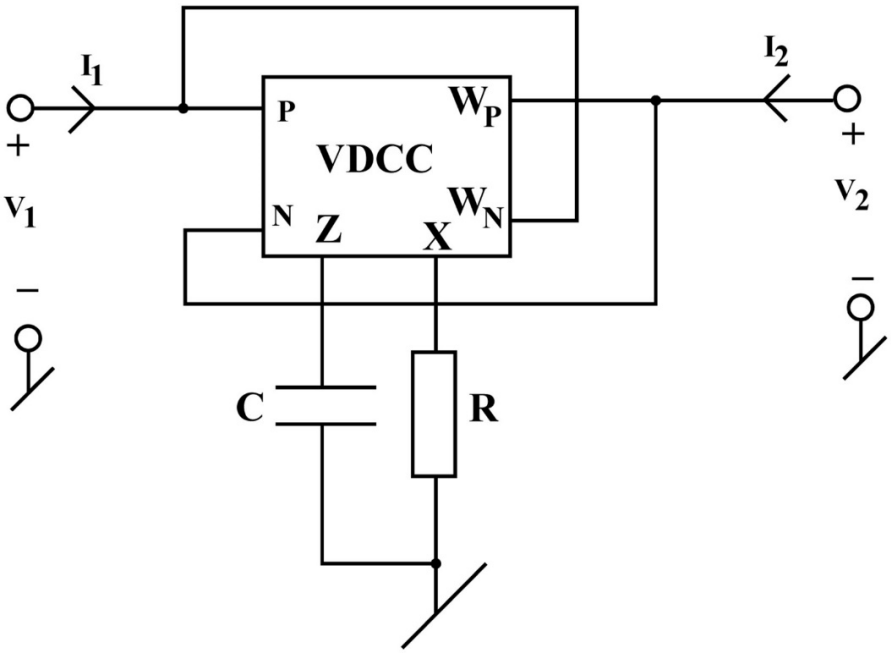


Fig.35 Inductance simulator using single VDCC (floating inductor) [6]

6.3 Influence of the Parasitic Impedances in VDCC

In order to find the performance of the inductance simulator, influence of parasitic impedance is inspected with various regions of frequencies. Due to this, dominant parasitic are mentioned. Fig.34 shows the pure inductance simulator considering modified topology with parasitic impedances and non-ideal equivalent circuits as shown in Fig.36 respectively. According to Fig. 36[a], R_{P3} is at Z terminal resulting output resistance of the first stage whereas R_{P1}, R_{P2}, C_{P1} and L_x are at second stage at W_P and X terminals. Considering these effects, inductance simulator impedance can be formulated as:

$$Z_{IN} = R_{P1} \,//\, \frac{1}{sC_{P1}} \,//\, [\, s(\frac{C_1(R_1 + R_{P2})}{g_m} + \frac{L_x}{R_{P3}g_m}) + \frac{(R_1 + R_{P2})}{R_{P3}g_m} + \frac{s^2C_1L_x}{g_m}\,]$$

From above equation circuit elements are obtained as of Fig. 36[b]

$$L_{Eqe} = \frac{C_1(R_1 + R_{P2})}{g_m} + \frac{L_x}{R_{P3}g_m}$$

$$R_s = \frac{(R_1 + R_{P2})}{R_{P3}g_m} - \frac{\omega^2C_1L_x}{g_m}$$

$$C_p = C_{P1}$$

$$R_p = R_{P1}$$

One factor that affects L_{Equ} is parasitic inductance L_x. From Fig. 36[b], the series resistance R_S whose value depends on the parasitic resistances R_{P2} and R_{P3} limits low frequency region of the inductance. With decrease in resistance R_S value increases the output impedance at port Z (R_{P3}). It can be implemented using cascade techniques. Also, negative resistance achieved by active elements can be mated to the terminal Z to balance R_{P3} and increase low frequency range. Whereas, circuit's high frequency performance is governed by R_P and C_P which are equivalent to R_{P1} and C_{P1} respectively. Note that lower values of C_{P1} and higher values of R_{P1} will refine the circuit's high frequency performance. Also, from above equations value of resistance R_S in high frequency region is dominated by ω^2 and L_x. Therefore, the value of resistance R_S in high frequencies can be negative which can finally affect the stability.

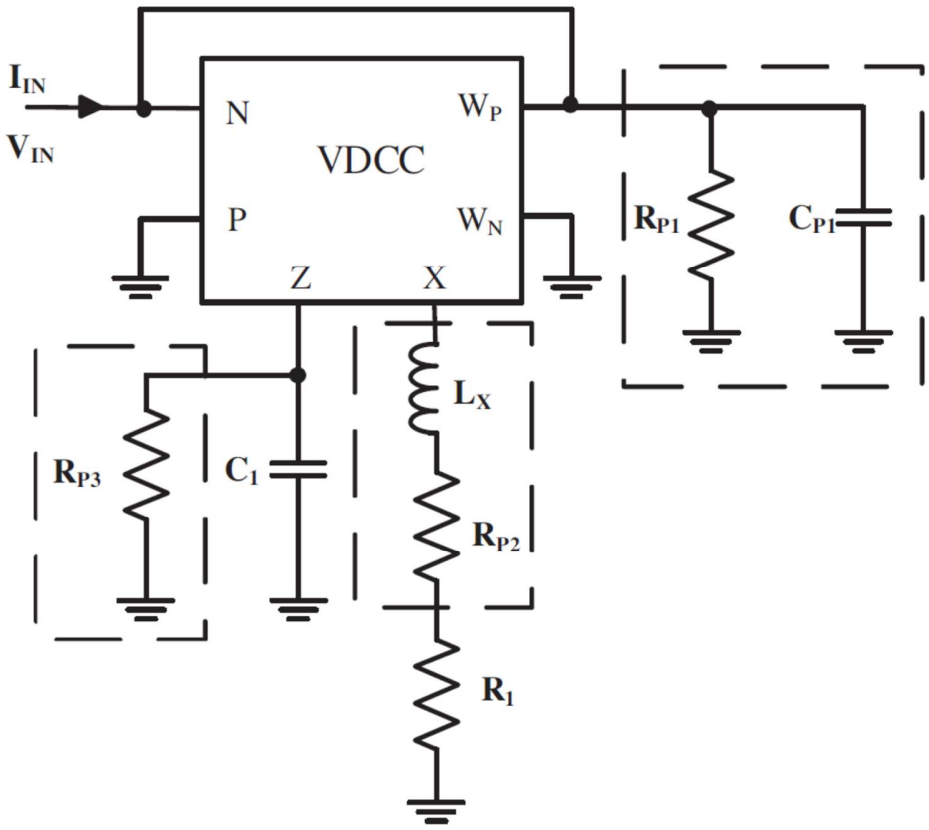
To avoid this, relation $R_S>0$ should be satisfied which results into following inequality:

$$\frac{(R_1 + R_{P2})}{R_{P3}} > (2\pi f)^2 C_1 L_x$$

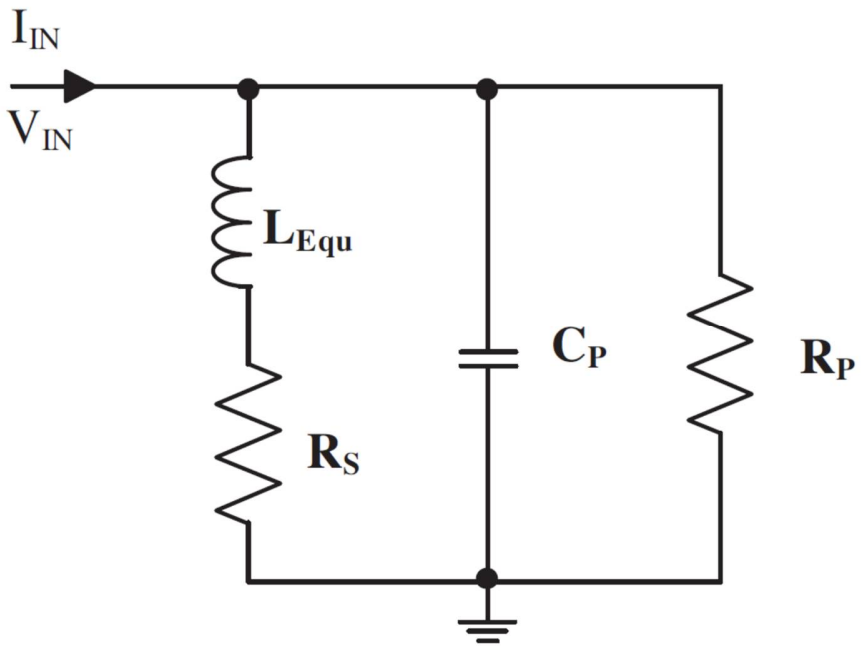
Where f is operating frequency and maximum frequency of operation without affecting stability

$$f_{max} = \frac{1}{2\pi}\sqrt{\frac{(R_1 + R_{P2})}{C_1 L_x R_{P3}}}$$

Now to increase the maximum frequency of, X terminal parasitic inductance (L_x) need to be decrease.



(a) Inductance simulator shown in Fig.34 with parasitic components



(b) Its equivalent circuit

Fig.36[a and b] Parasitic impedances effect on VDCC [5]

6.4 Simulation Results

To verify the workability of the circuit simulation is performed using PSPICE software using TSMC 0.18µm technology parameter. Width to length (W/L) ratios of the transistors used in CMOS realization of VDCC is shown in Table 4. The supply voltages are V_{DD}= −V_{SS}= 0.9 V and biasing current I_{B1}= 50µA and I_{B2}= 100µA, Hence transconductance value obtained is g_m=277µA/v. for Fig.36 parasitic elements value are R_{P1}= 141kΩ, R_{P2}= 43Ω, R_{P3}= 362kΩ, C_{P1}= 0.92pF and Lx= 2.28µH. The power consumption is 0.869mW. Simulation is performed to the circuit shown in Fig.34 with the passive components values R_1= 4 kΩ and C_1= 20 pF, which is corresponds to L_{eq}= 0.29mH.

The ideal and VDCC based inductor is simulated and its impedance vs frequency characteristics is shown in figures from Fig.37 to Fig.38. and it is found that the ideal and VDCC based simulated responses are very much close within the frequency range 30kHz to 20MHz. To examine the performance of VDCC based inductance simulator, apply this structure to third order high pass filter by replacing its inductor by a VDCC based inductance simulator. Passive elements values are R_L= R_S= 10 kΩ and C_1= C_2= 15.9 pF and L_1= 795.77µH. Which results 3db frequency 1MHz. Now circuit shown in Fig.34 is simulated with the following passive components R_1= 4kΩ, C_3= 20pF and I_{B1}= 6.75µA which gives g_m= 100.5µA/V, which correspondence to L_{eq}= 796µH. Ideal and VDCC based simulated response of third order high pass filter is as shown in Fig.41and Fig.42 respectively.

Table 4

Transistors	W/L(µm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{17}	14.4/0.72
M_{18}-M_{22}	0.72/0.72

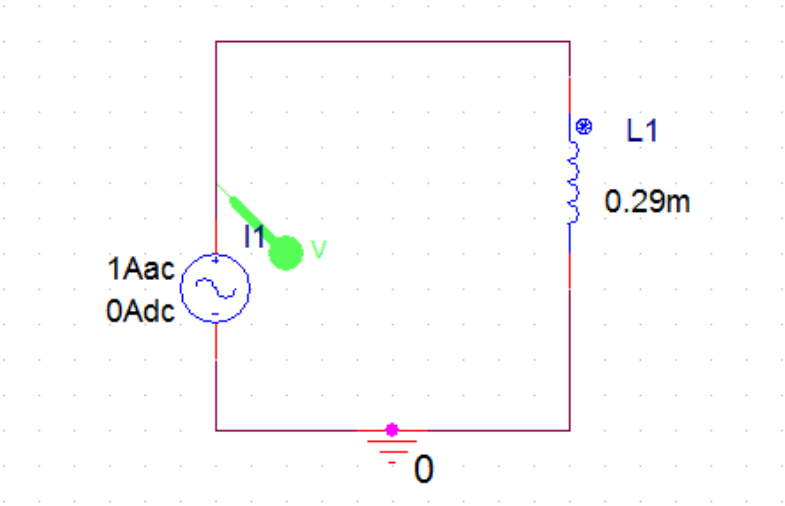


Fig.37 Passive inductor schematic [5]

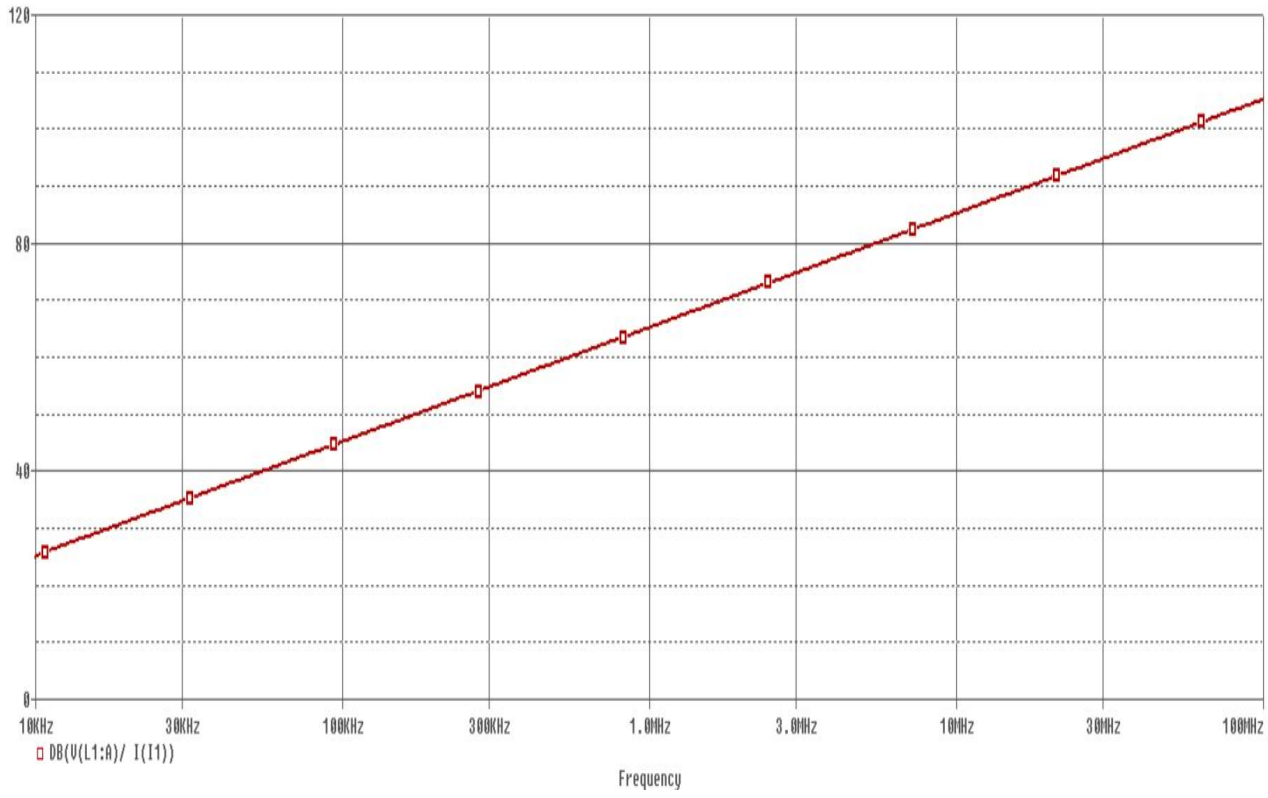


Fig.37[a] Impedance vs frequency response of passive inductor

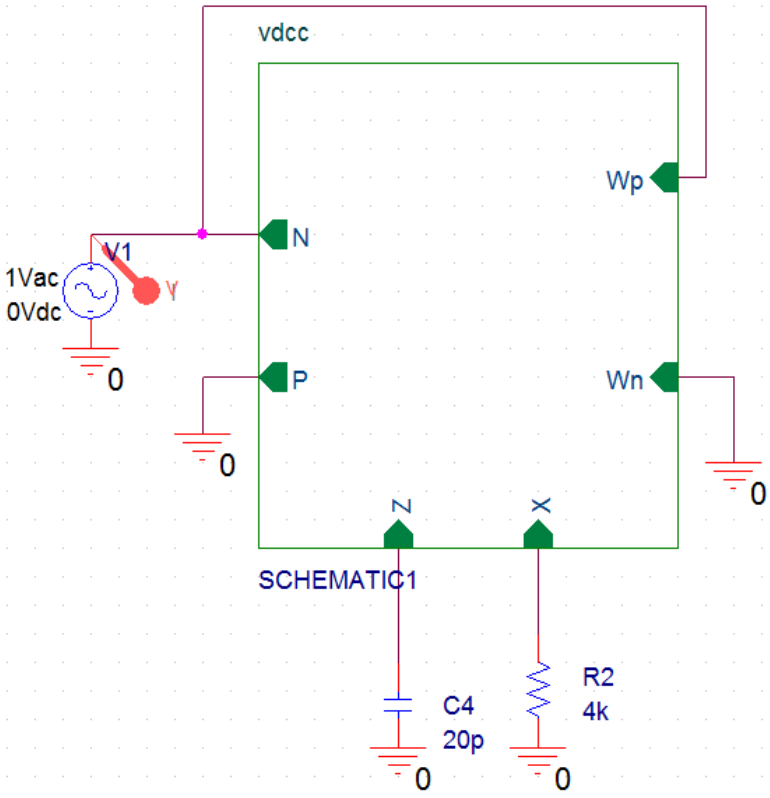


Fig. 38 VDCC based inductance simulator schematic [5]

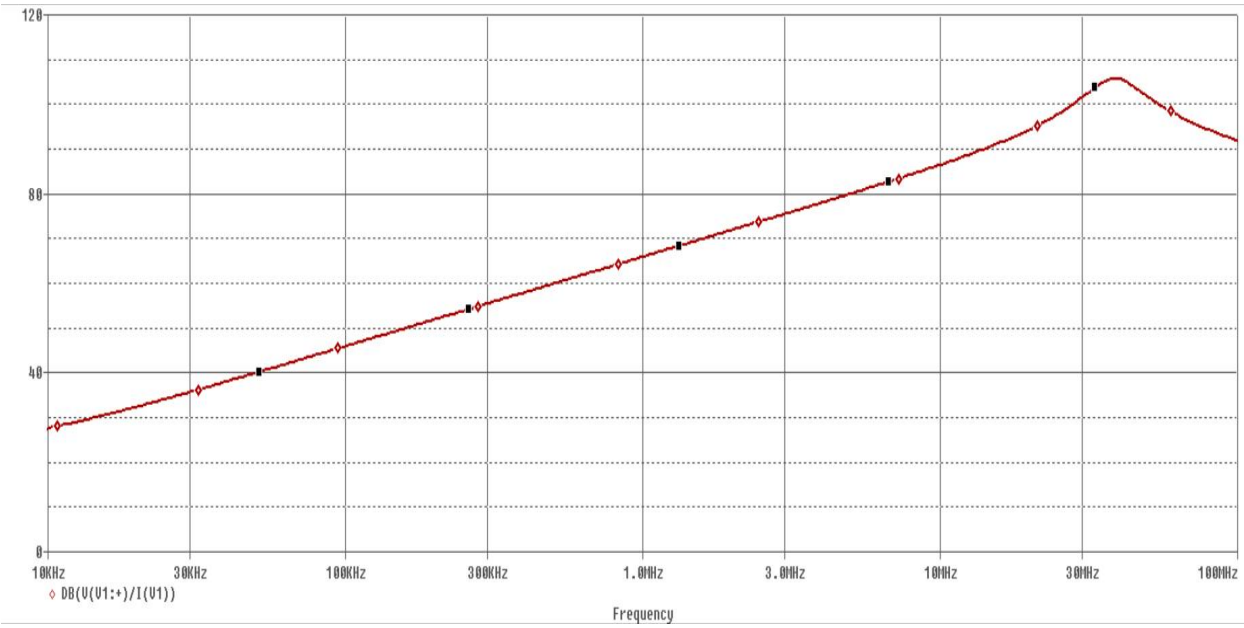


Fig.38[a] Impedance vs frequency response of VDCC based inductance simulator

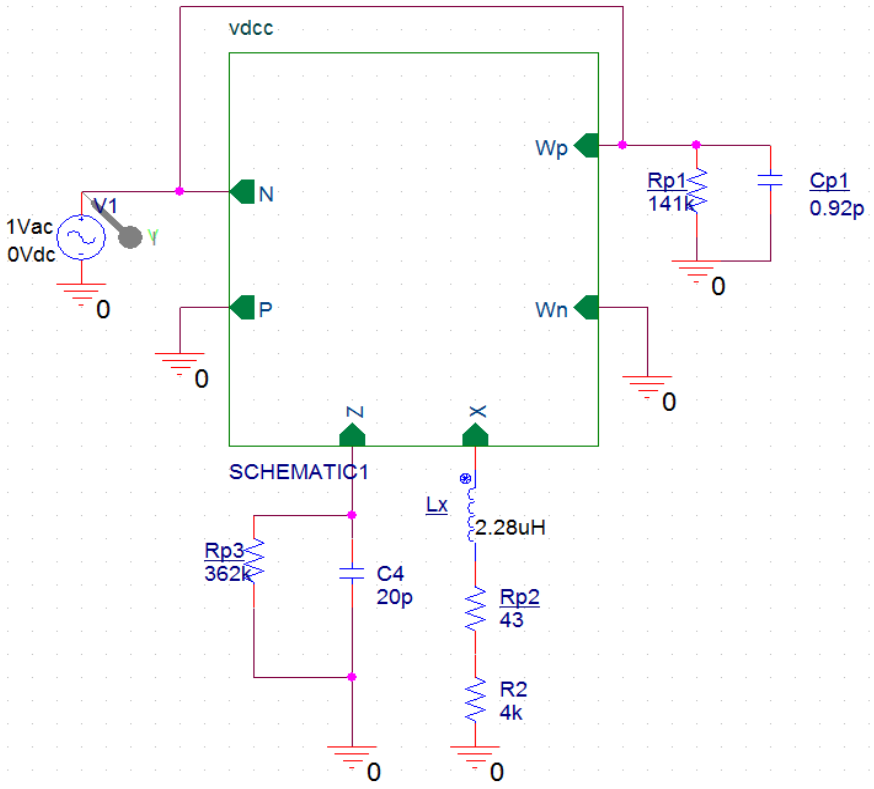


Fig.39 VDCC based inductance simulator with parasitic elements schematic [5]

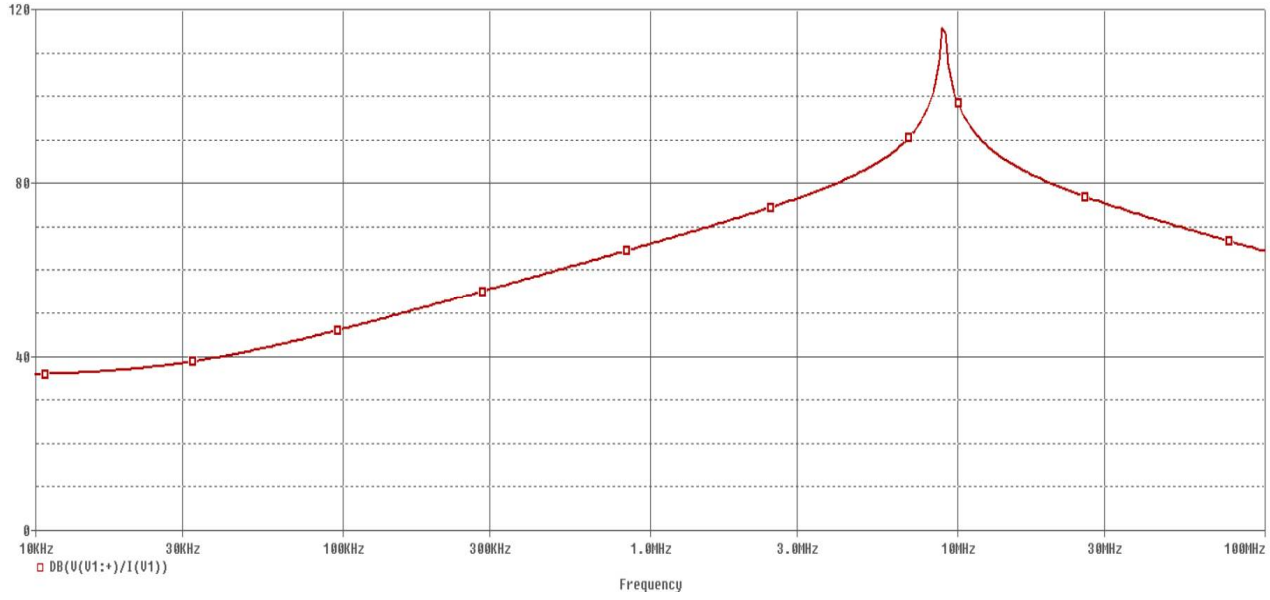


Fig. 39[a] Impedance vs frequency response of VDCC based inductance simulator with parasitic elements

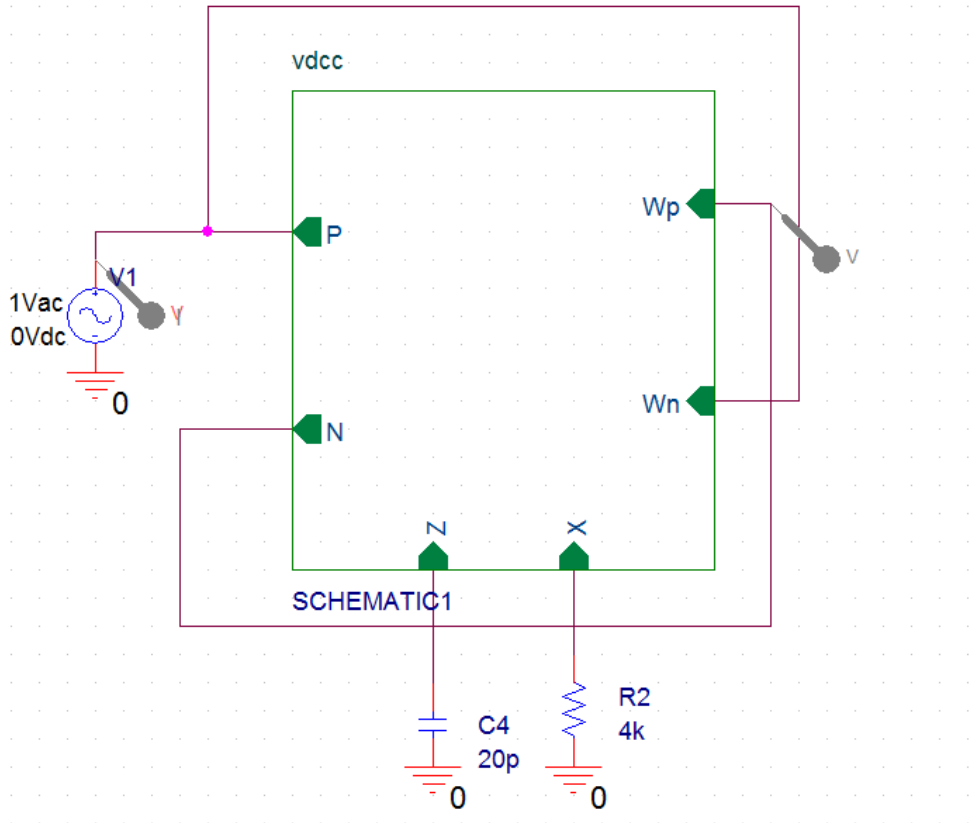


Fig.40 VDCC based floating inductance simulator [6]

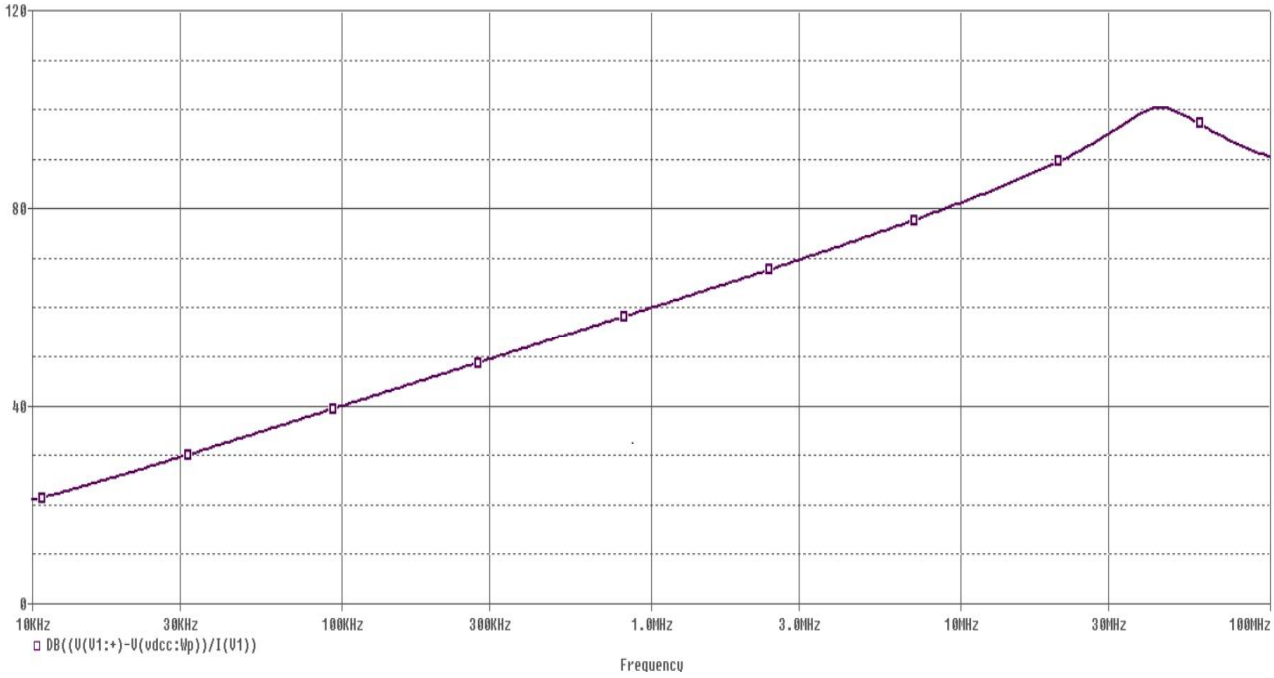


Fig. 40[a] Impedance vs frequency response of VDCC based floating inductance simulator

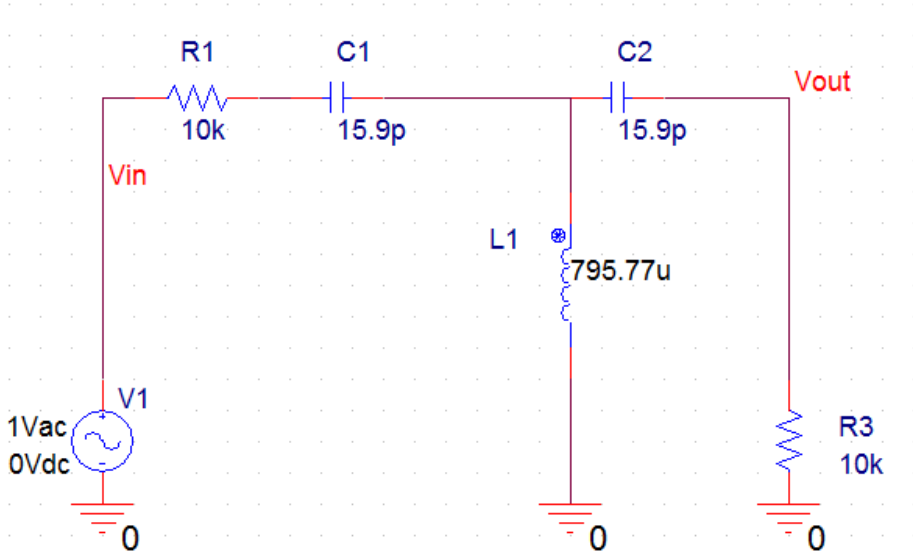


Fig.41 Passively realized Third-order high-pass Butterworth filter schematic [5]

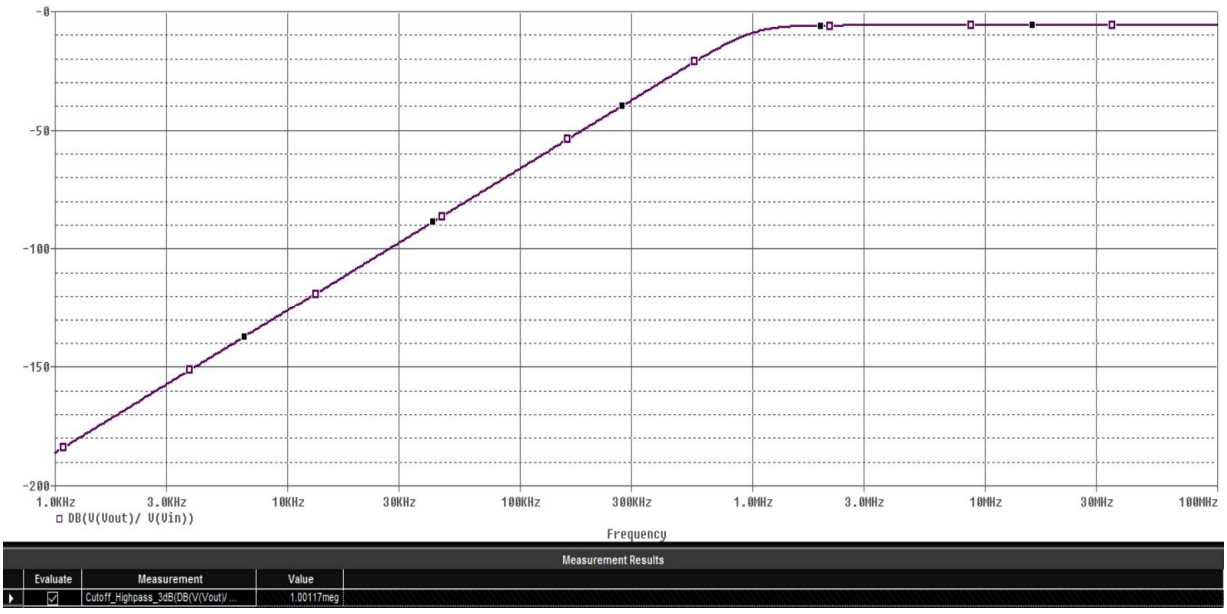


Fig. 41[a] Impedance vs frequency response of Passively realized Third-order high-pass Butterworth filter

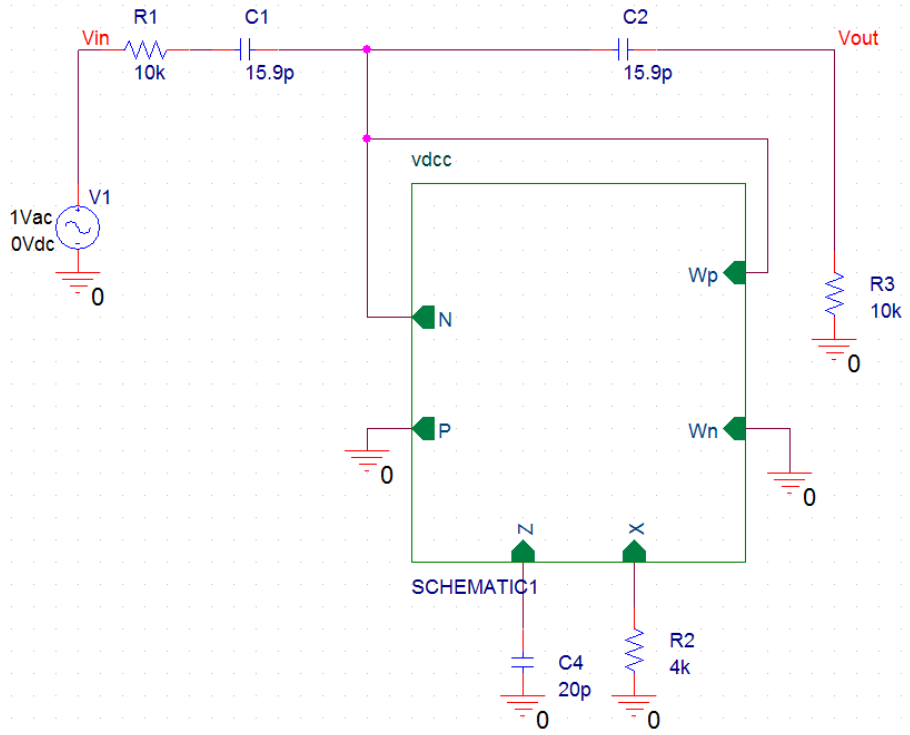


Fig.42 VDCC-based inductance simulator based realization of Third-order high-pass Butterworth filter schematic [5]

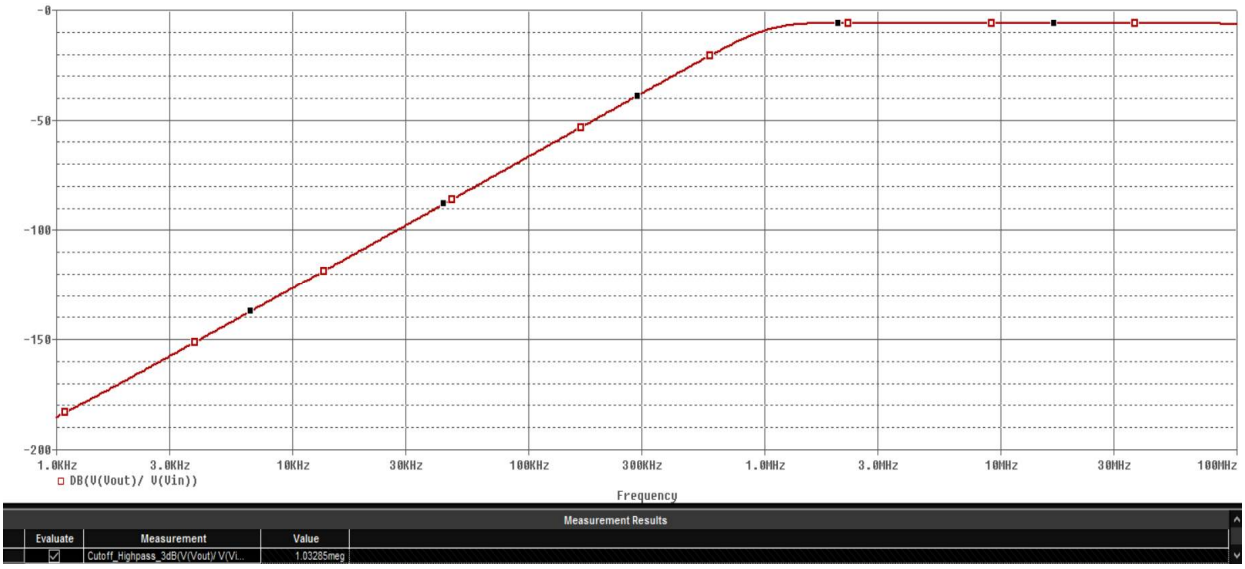


Fig. 42[a] Impedance vs frequency response of VDCC based inductance simulator based realization of Third-order high-pass Butterworth filter

Chapter 7

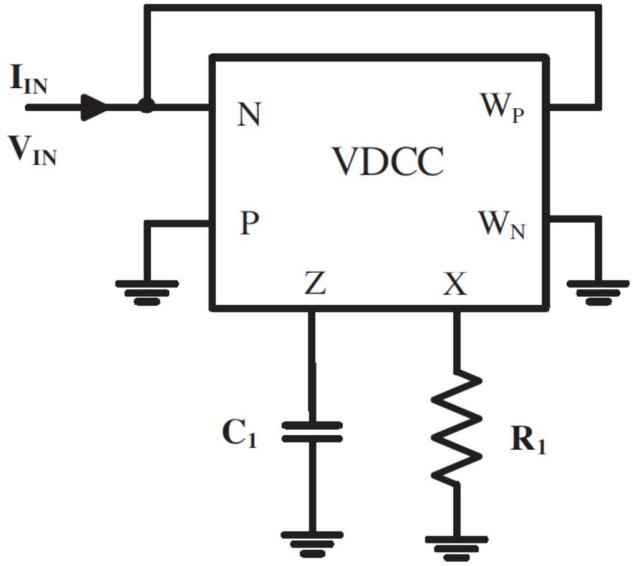
Fifth order Low-Pass and High-Pass Ladder Filters based on VDCC

7.1 Introduction

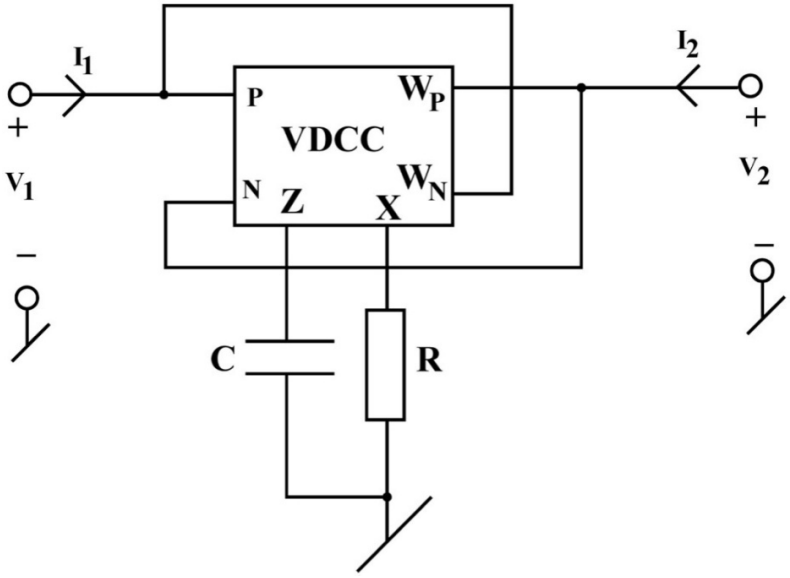
Circuits which are operating in ultralow power are needed to study and is useful in operation despite the necessities like mosfet operating under weak inversion region and having low current requirements. for filtering purpose in analogue domain LC ladder filters structure which is doubly terminated is used because it is having very low value of sensitivities with respect to component values and very minimal effect regarding the non-exact values which is realizes in the transfer function. In LC ladder type of filter structure where we realize and simulates transfer function through lossless inductors and capacitors, which is having connections between terminating resistances also it is having low sensitivity towards nonexact values of components. VDCC is very useful for designing of various types of filters, oscillators and inductor simulator because of its property of providing electronically tunable transconductance gain value.

7.2 Ladder Filters structure

In order to improve the characteristics of filter, inductors used in the ladder filter structure is being replaced with the help of VDCC based inductors so that no passive inductors are used in this circuit. In the realization of HP filter, we require grounded inductors. VDCC based realization of grounded inductor is as shown in Fig. 43[a]. It uses a single VDCC structure in addition with one grounded resister and capacitor. In the realization of LP filter, we require floating inductors. VDCC based realization of floating inductor is as shown in Fig. 43[b]. It uses a single VDCC structure along with one grounded resistor and capacitor.



(a) Grounded Inductor



(b) Floating Inductor

Fig. 43[a and b] Inductors using VDCC [6]

Now the equivalent inductance for both types (grounded and floating) is

$$L_{eq} = \frac{CR}{g_m}$$

Hence transfer function of LP filter and HP filter is

$$T_{LPF}(s) = \frac{R_2}{\begin{array}{c} s^5L_1L_2C_1C_2C_3R_1R_2 + s^4C_2L_1L_2(R_1C_1 + R_2C_3) + \\ s^3[R_1R_2\{L_1(C_1C_2 + C_1C_3L_2 + C_1C_3)C_2C_3L_2\}L_1L_2C_2R_1] \\ +s^2[R_1(L_1C_1 + L_2C_2 + L_2C_1) + R_2(L_1C_3 + L_1C_2 + L_1L_2C_3)] \\ +s[R_1R_2(C_1 + C_2 + C_3) + L_1 + L_2] + R_1 + R_2 \end{array}}$$

$$T_{HPF}(s) = \frac{s^5C_1C_2C_3L_1L_2R_2}{\begin{array}{c} s^5L_1L_2C_1C_2C_3(R_1 + R_2) + \\ s^4[C_1C_2C_3R_1R_2(L_1 + L_2) + L_1L_2(C_1C_2 + C_2C_3 + C_3C_1)] + \\ s^3(L_1 + L_2)[R_1C_1C_2 + R_2C_2C_3 + C_3C_1(R_1 + R_2)] \\ +s^2[C_3C_1R_1R_2R_2 + L_2C_2 + L_2C_3 + L_1C_1 + L_2C_1] \\ +s[(C_1R_1 + C_3R_2)] + 1 \end{array}}$$

7.3 Simulation Results

For analysis of LP and HP filter structure, SPICE simulation is performed using TSMC 180nm model parameter. CMOS implementation of VDCC is as shown in Fig.3. We used supply voltages V_{DD} = -V_{SS}=0.9v and bias currents I_{B1}=50µA and I_{B2}=100µA.

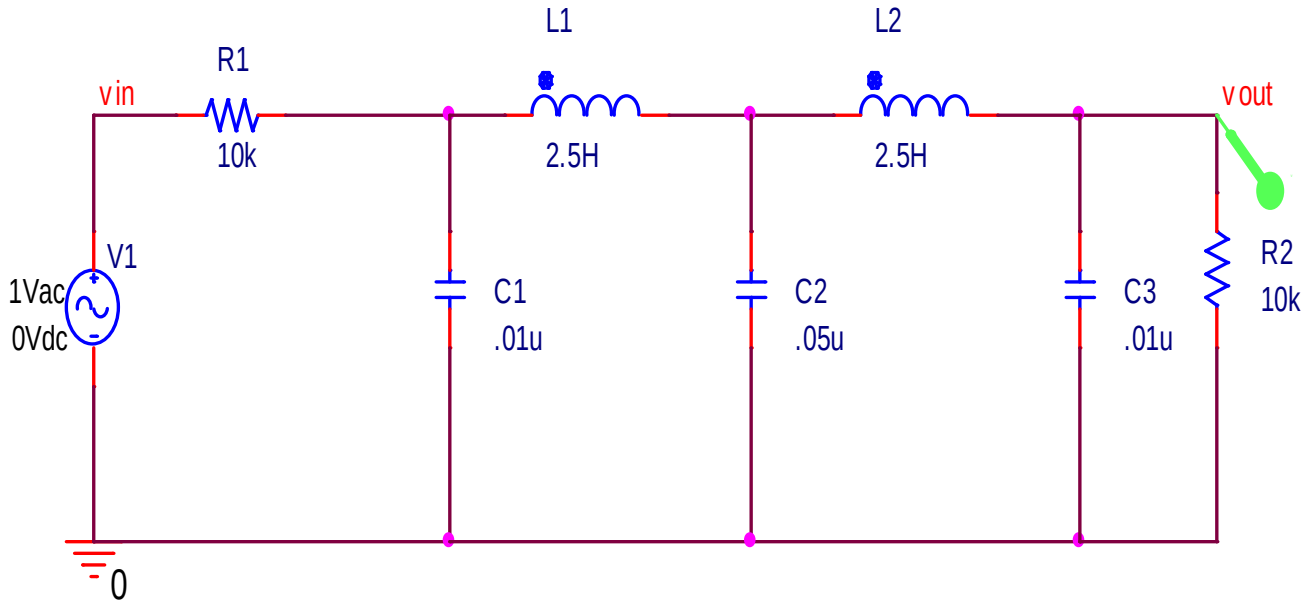


Fig.44 Passive Low Pass LC ladder filter schematic [6]

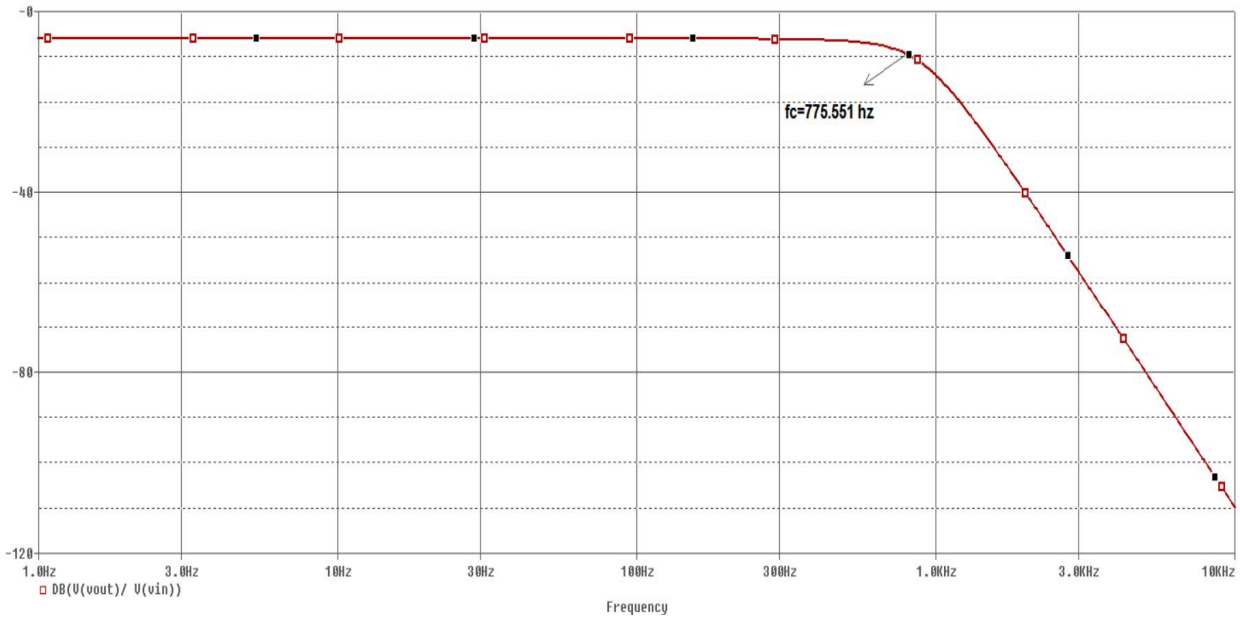


Fig. 44[a] Frequency response of passive LC Low Pass ladder Filter

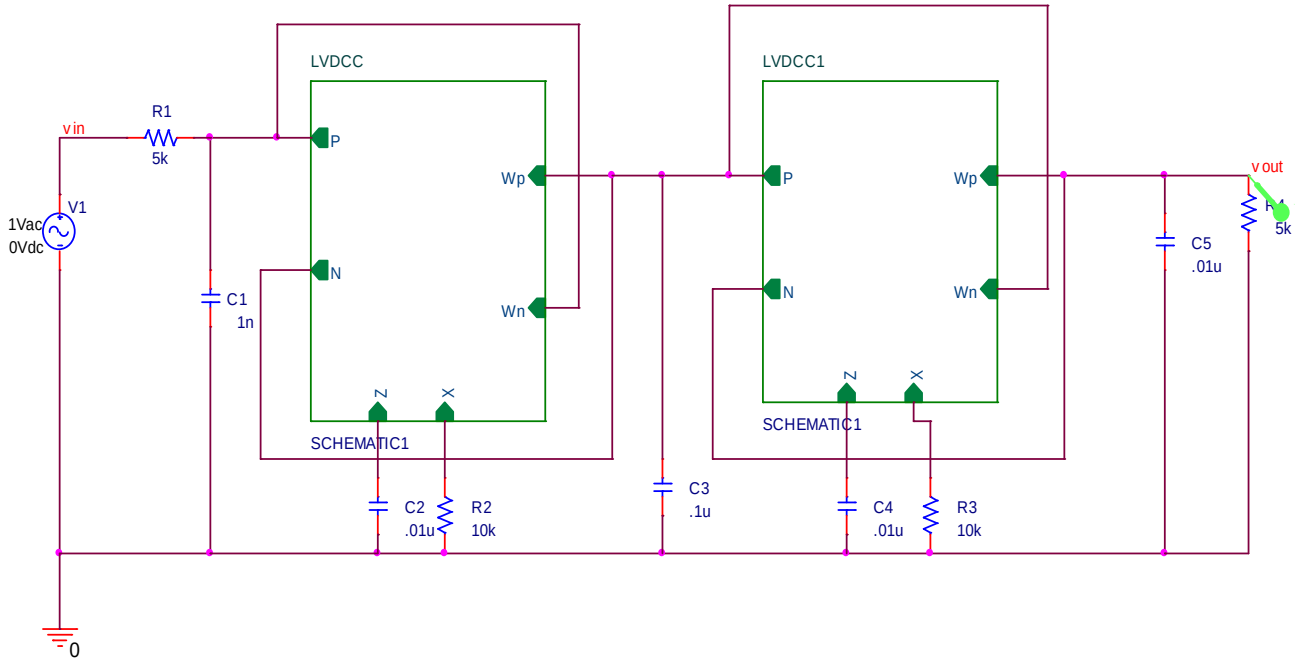


Fig. 45 Low-Pass ladder filter based on VDCC schematic [6]

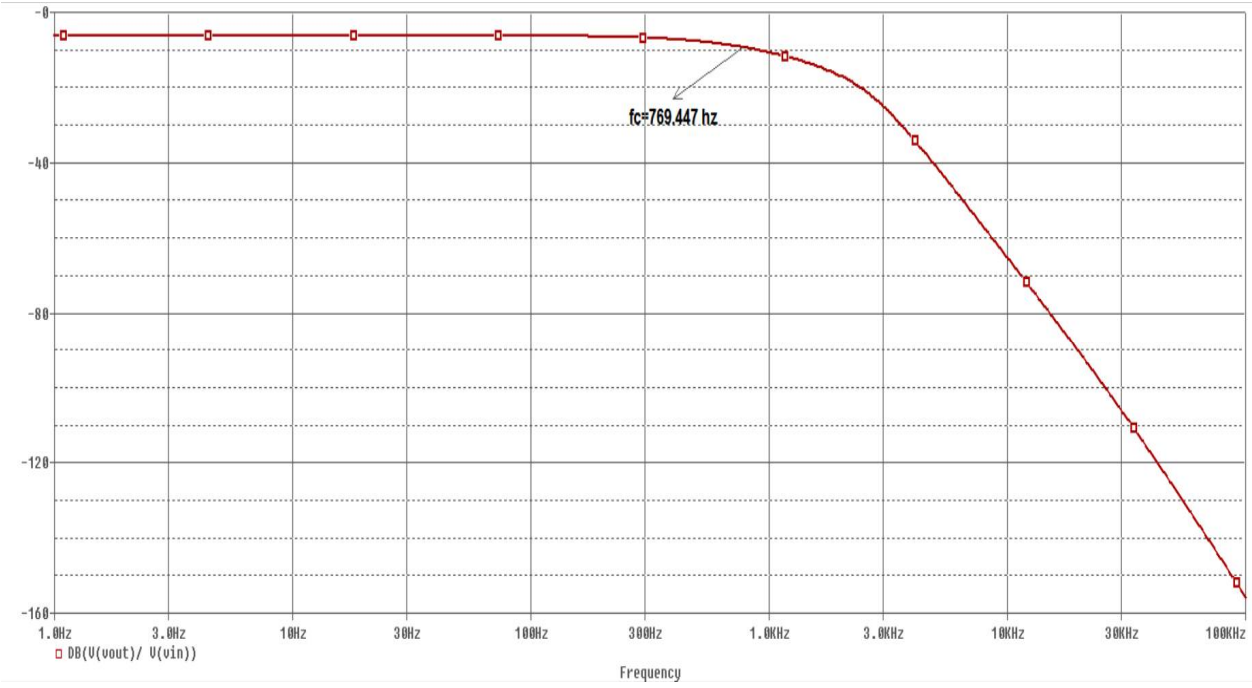


Fig. 45[a] Frequency response of Low-Pass ladder filter based on VDCC

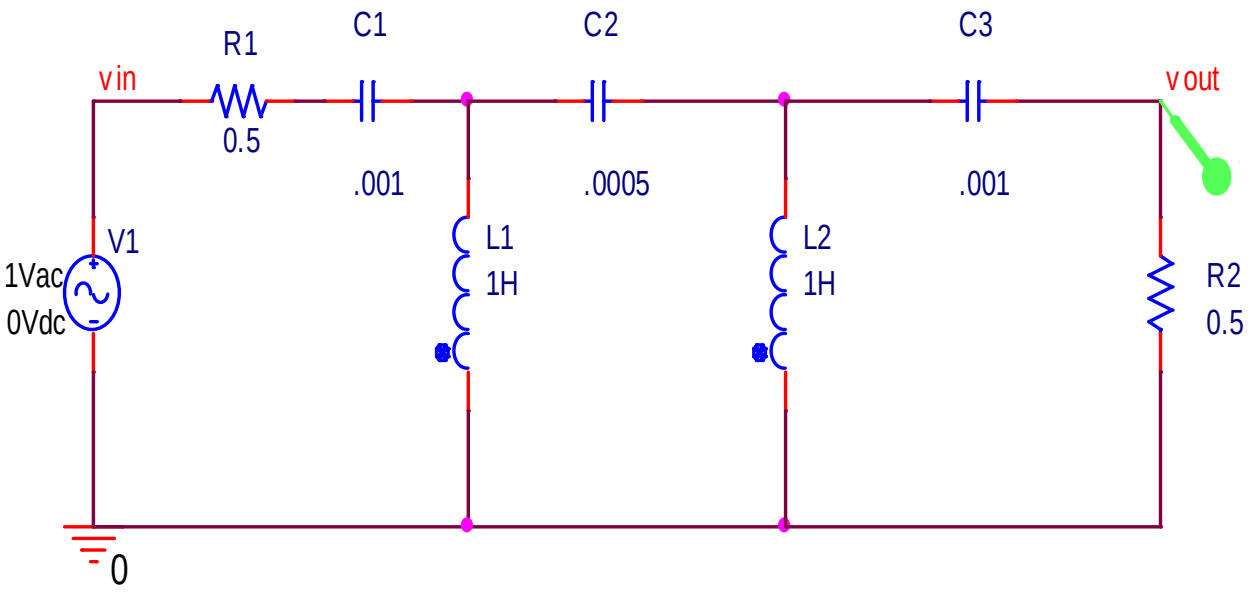


Fig.46 Passive High Pass LC ladder filter schematic [6]

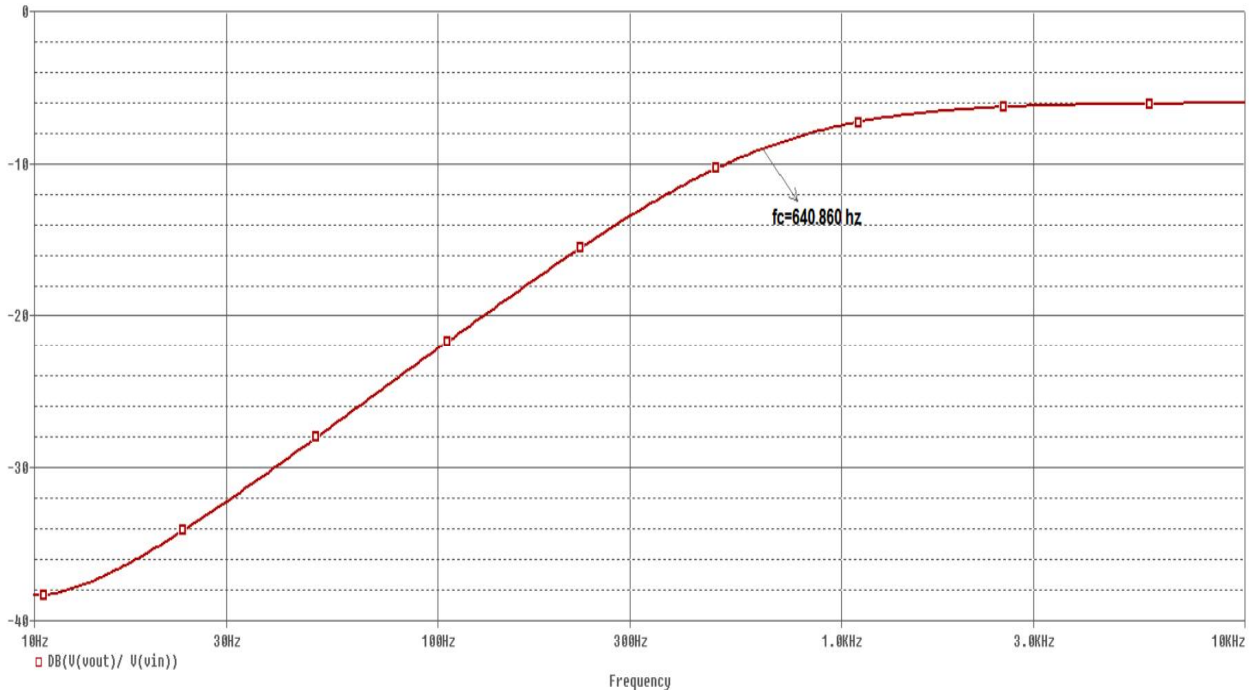


Fig. 46[a] Frequency response of passive LC High Pass ladder Filter

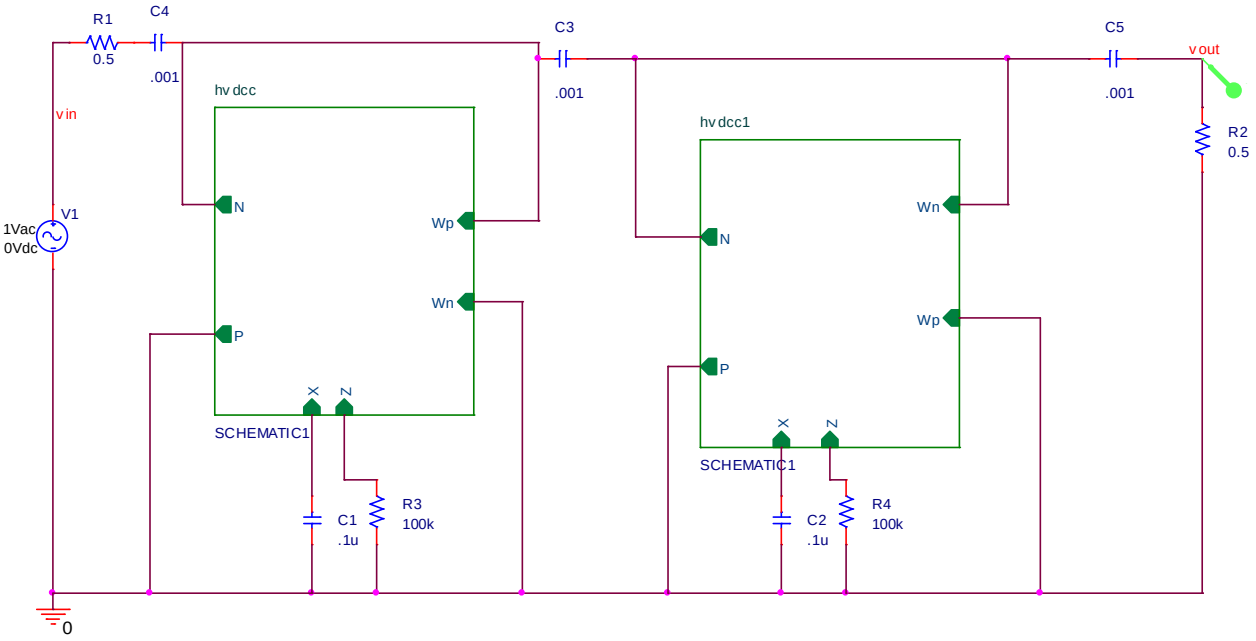


Fig.47 High-Pass ladder filter based on VDCC schematic [6]

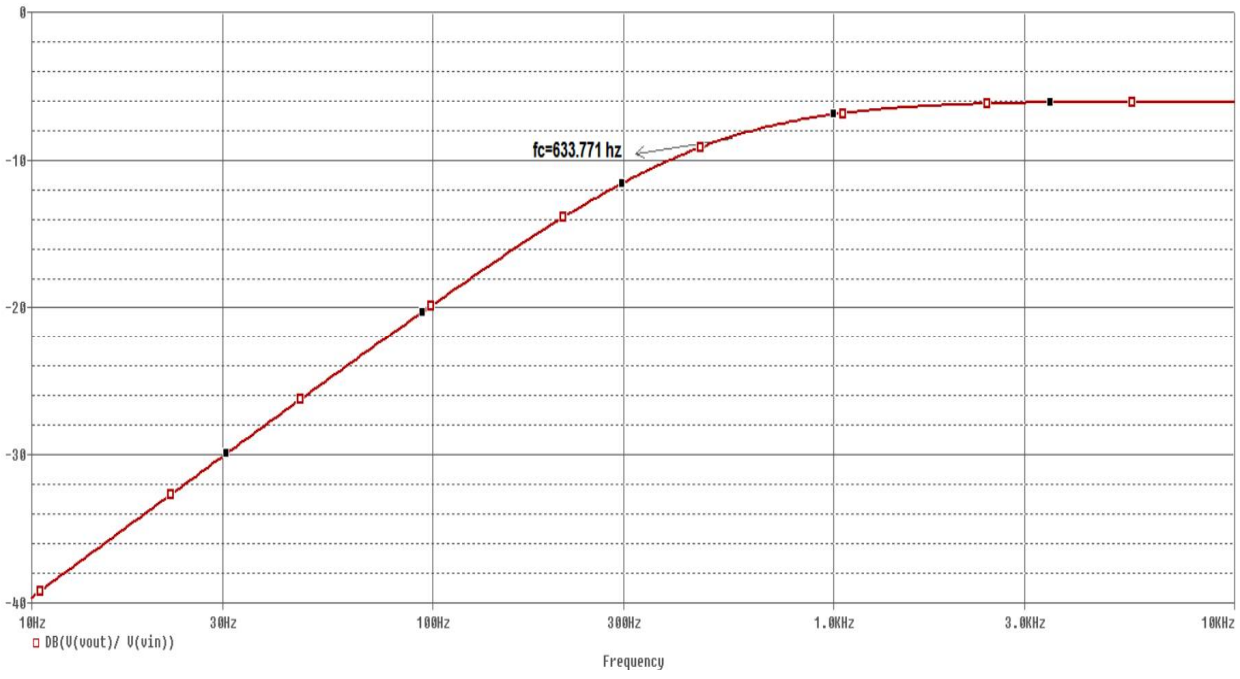


Fig. 47[a] Frequency response of High-Pass ladder filter based on VDCC [2]

Chapter 8

Conclusion

Among the various building blocks used in the analog signal processing, VDCC is emerging as a versatile and flexible building block in the analog circuit design. Tow Thomas biquad structure based of VDCC is studied which uses an optimal number of passive and active components. Workability of the circuit is analysed with the help of PSPICE simulation. Tunable property of the biquad circuit is also shown by PSPICE simulation. KHN biquad filter using VDCC has been studied and to analyse the proper functioning of the circuit simulation is performed using PSPICE software. In VDCC Based TISO and SIDO Biquad Filter three voltage mode biquad structure is analysed. The first structure is three input single output biquad structure and the other two structures are single input dual output biquad structures whose quality factor can be adjusted by adjusting one resistor without changing pole frequency. Pole frequency of all the filters can be electronically tuned by varying biasing current. Simulation is performed to check the functioning of the structure. VDCC based inductance simulator and Third-order high-pass Butterworth filter is studied. The presented inductance simulator is having several advantages such as:(i) using minimum number of passive and active components, (ii) using only grounded resistor/capacitor, which is useful for integration and absorbing series/shunt parasitic, respectively, (iii) electronically tuning ability by varying biasing current, (iv) no passive component matching condition is required. The workability of the circuit is confirmed by SPICE simulation. Fifth order Low-Pass and High-Pass Ladder Filters based on VDCC is studied. Low pass and High pass filter circuit uses two VDCCs which simulates two floating inductors and two grounded inductors respectively. The behavior of the circuit is verified by SPICE simulation.

References

[1] D. Biolek, R. Senani, V. Biolkova and Z. Kolka, “Active Elements for Analog Signal Processing; Classification, Review and New Proposals,” Radioengineering, vol. 17, no. 4, 2008, pp. 15-32.

[2] R. Jain and P. Kumar, "VDCC based voltage mode Tow-Thomas biquad filter," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, 2016, pp. 1-4.

[3] S. Rana, A. K. Kumawat and P. Kumar, "A universal current mode KHN biquad filter using voltage differencing current conveyor," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, 2016, pp. 1-5.

[4] F. Kacar, A. Yesil, and K. Gurkan, "Design and experiment of VDCC based voltage mode universal filter," Indian Journal of Pure & Applied Physics, vol. 53, pp.341-349, May 2015.

[5] F. Kacar, A. Yesil, S. Minaei, H. Kuntman, “Positive/negative lossy/lossless grounded inductance simulators employing single VDCC, and only two passive elements,” AEU – Int. Journal of Electronics and Communications, vol. 68, no. 1, pp. 73-78, 2014.

[6] D. Prasad, A. Ahmad, A. Shukla, A. Mukhopadhyay, B. B. Sharma, “Novel VDCC Based Low-Pass and High-Pass Ladder Filters,” In Proc. of Annual IEEE India Conference (INDICON 2015), 2015, p. 1-3.

[7] D. Prasad and J. Ahmad, “New Electronically-Controllable Lossless Synthetic Floating Inductance Circuit Using Single VDCC” Circuits and Systems, vol. 5, no. 1, pp. 13-17, 2014.

[8] D. Prasad, D. R. Bhaskar, M. Srivastava, “New Single VDCC-based Explicit Current-Mode SRCO Employing All Grounded Passive Components,” Electronics, vol. 18, no. 2, pp. 81-88, 2014.

[9] R. Sotner, N. Herencsar, J. Jerabek, R. Prokop, A. Kartci, T. Dostal, K.Vrba, “Z-copy controlled-gain voltage differencing current conveyor: advanced possibilities in direct electronic control of first-order filter, ”Elektronika Ir Elektrotechnika, vol. 20, no. 6, pp. 77-83, 2014.

[10] M. Sagbas, U. E. Ayten, M. Koksal and N. Herencsar, "Electronically tunable universal biquad using a single active component," 2015 38th International Conference on Telecommunications and Signal Processing (TSP), Prague, 2015, pp. 698-702.

[11] A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek and K. Vrba, " Application possibilities of VDCC in general floating element simulator circuit," 2015 European Conference on Circuit Theory and Design (ECCTD), Trondheim, 2015, pp. 1-4.

[12] A. Kartci, U. E. Ayten, R. Sotner and R. Arslanalp, " Electronically tunable VDCC-based floating capacitance multiplier," 2015 23nd Signal Processing and Communications Applications Conference (SIU), Malatya, 2015, pp. 2474-2477.

[13] A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek and K. Vrba, " Floating capacitance multiplier simulator for grounded RC colpitts oscillator design," 2015 International Conference on Applied Electronics (AE), Pilsen, 2015, pp. 93-96.

[14] Roman Sotner, Jan Jerabek, Norbert Herencsar, Tomas Dostal, Kamil Vrba, " Design of Z-copy controlled-gain voltage differencing current conveyor based adjustable functional generator," Microelectronics Journal, Volume 46, Issue 2, 2015, pp. 143-152.
[15] M. Srivastava, P. Bhanja and S. F. Mir, " A new configuration for simulating passive elements in floating state employing VDCCs and grounded passive elements," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, 2016, pp. 1-4.