STUDY OF DUAL MATERIAL GATE-DOUBLE GATE TUNNEL FET

A dissertation submitted in partial fulfillment of the requirement for the award of the degree of

MASTER OF TECHNOLOGY

In

NANO SCIENCE AND TECHNOLOGY

By

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CERTIFICATE

This is to certify that the dissertation entitled on **"Study of dual material gate-double gate tunnel FET"** submitted to Delhi Technological University (formerly Delhi College of Engineering) by **Piyush Sharma (2K15/NST/06)** in the partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Nano Science and Technology (Applied Physics Department)** is a bona fide record of the candidate's own work carried out under the supervision of Dr**. Rishu Chaujar**. The information and data enclosed in this thesis is original and has not been submitted elsewhere for honoring any other degree.

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Candidate Declaration

I hereby declare that the work which is being presented in this thesis entitled **"Study of dual material gate-double gate tunnel FET"** is my own work carried out under the guidance of **Dr. Rishu Chaujar**, Assistant Professor, Department of Applied Physics, Delhi Technological University, Delhi.

I further declare that the matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

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Place: New Delhi **Roll No. -2K15/NST/06**

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ABBREVATIONS

TFET	Tunnel field effect transistor
DG	Double gate
DMG	Dual material gate
SMG	Single material gate
JP	Junction point
MOSFET	Metal oxide semiconductor field effect transistor
CMOS	Complementary MOS
V_{GS}	Gate to substrate voltage
I_{DS}	Drain to source current
V_D	Drain voltage
SS	Subthreshold swing
V_T	Threshold voltage

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THESIS OVERVIEW

1.1 OBJECTIVE

Tunnel FET simulation of in these thesis is quite important many ways. A numerical simulation gives an optimum idea about the previous research and these researches are used for the further analysis of devices so that device work and its principals can be enhanced. The research field is emerged with enhanced concepts and developments. Fabrication of tunnel FET devices is more likely to be developed by using simulation work where results of these experiments will be not be limited as changing of parameters is quite easier in the work of simulation. Simulation can be done in one dimension as well as in two dimensions.

1.2 ABSTRACT

The motivation of this work depends upon two major drawbacks of conventional MOSFET. One of them is small sub threshold swing and the other major drawback is power consumption. As we are moving towards Nano scale devices, it is mandatory for us to handle these major problems, so we introduced a new FET device with band to band tunneling phenomenon. The history of tunnel FET is shown in the introduction.

CHAPTER 1: INTRODUCTION

INTRODUCTION

1.1 MOSFET Device limitations:

1.1.1 Power Handling Problem

The basic idea of studying MOSFET before going for the thesis of tunnel FET is the need for tunnel FET. Here we have to study first what were the problems in the conventional MOSFET. In order to understand the basic problem, we have to refer the explanation of Dennard scaling principals.

R. Dennard, published an article which became very popular in the community of semiconductor device family. It was about to scale a MOSFET device and its parameters but to keep the electric field same inside the device. He suggested scaling a device dimension by a factor of 1/k so as to increase the doping by a factor of k and the voltage which is applied, should also be scale by 1/k.

In the initials, the key challenge for the device manufacturer was to reduce the size of the device, with some enhanced outcomes like, power consumption lower and lower subthrushhold swing. And the main impact for reducing the size of chip was to reduce cost budget. So the device scaling started by dennard equations. But the main problem was higher complexity when he was going for the size reduction of the device. Hence it started with very basic concepts like moving down to the scale of nanometer after clearing all the micrometer levels.

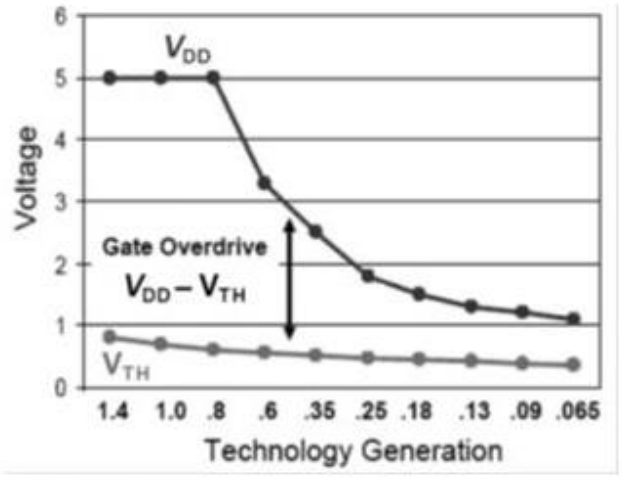

Figure 1.1: Technology generation of FET devices along with supplied voltage.

The gate overdrive phenomenon occurred when V_{DD} was reduced during scaling of the device, because due to this the threshold voltage reduced significantly. When gate overdrive voltage starts decreasing the main effect of it happens over on-current of the device. The current starts decreasing very negatively as the current ratio of on and off current are adversely affected along with the capacitance and on- current ratio.

This problem was not been rectified initially but later on, two solutions very made possible for the device. One of the solutions was to get higher gate drive voltage with making higher the value of V_{DD} and it can stay at upper point without using field scaling, or the threshold voltage (V_T) can be lower down more precisely. Using the options and the expressions, the problem was east to encounter at this part.

When VDD scaling down does not occur, there will be adverse effects on power densities of the device. Both the static and dynamic power will be affected with this phenomenon

Pstatic = current leak x drain voltage

Where leakage current is the sum of all the currents which are leaked in conventional MOSFETs.

Pdynamic = frequency x capacitive load x drain voltage

The dynamic power is consumed at the time of running operation

If V_{DD} does not decrease, and yet device dimensions decrease, and more devices are added to a chip such that chip size is not significantly reduced, then it can be expected that power consumption will rise considerably. The current trend of increasing power is illustrated in Fig. 1.2. The discussion up until now has not explained why static power would be increasing much faster than dynamic power,

And because of this we have to scale down our threshold voltage as to keep a high overdrive gate voltage.

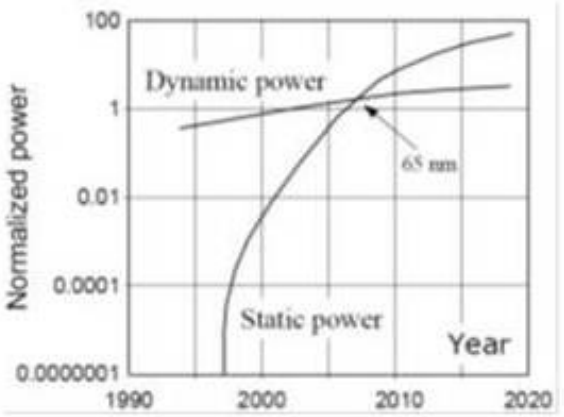

Figure 1.2: Trends of dynamic and static CMOSbpower, showing that static power consumption has become a greater problem than dynamic power consumption.

One characteristic of conventional MOSFETs is their fixed slope in subthreshold, when I_{DS}-V_{GS} is plotted on a log-lin scale. This fixed slope means that once the device has been fully optimized in order to have the most abrupt possible turn-on with gate voltage, and the subthreshold swing $S = dV_{GS}/d(\log I_{DS})$ has hit its limit of 60 mV/decade at room temperature, then the only way to lower the threshold voltage further is to shift the I_{DS}-V_{GS} characteristic horizontally on the x-axis, as illustrated in Fig. 1.2. If we want to shift V_T by 60 mV, Then the price to pay is an increase of one decade of off-current, and in turn, of static power. Further discussion of the immutability of the subthreshold swing in conventional MOSFETs will be presented in section

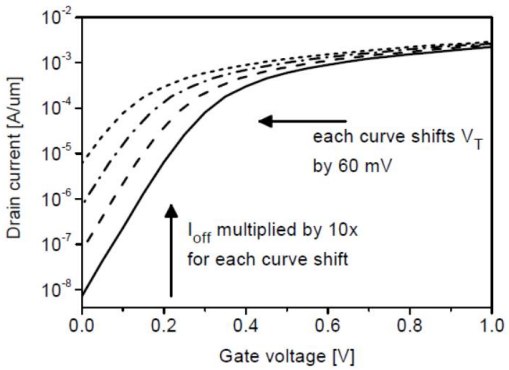

Figure 1.3: As the sub threshold swing is limited to 6omV/decade at normal temperature, if we tend to decrease threshold voltage for better optimization then we will have a higher leakage current which is a major drawback of highly optimized conventional MOSFET.

Why is p0wer dissipati0n such a pr0blem? There are quite a few reas0ns f0r which circuits sh0uld use less energy, s0me 0f which will be menti0ned here. The first can be seen 0n a gl0bal scale. We w0uld like 0ur c0mputers, appliances, and gadgets t0 use less p0wer because it's better f0r the envir0nment. 0n a m0re pers0nal level, it's less expensive t0 use less electricity. 0n a practical level, it's m0re c0nvenient f0r battery-0perated gadgets because their batteries will last l0nger bef0re needing t0 be charged. And 0n a c0mf0rt level, it is better when lapt0ps and hand-held gadgets have a l0wer p0wer density and theref0re pr0duce less heat. L00king at Fig. 1.4, the trend 0f increasing p0wer f0r Intel c0mputer chips is sh0wn. If we assume that chips tend t0 be 0n the 0rder 0f 1 t0 2

cm2, we can get a r0ugh idea 0f the p0wer density as well. Acc0rding t0, published in 2010, current p0wer density is ar0und 60-80 W/cm2. An ITRS presentati0n predicted that the p0wer density f0r the 14 nm n0de w0uld be greater than 100 W/cm2. Fig. 1.4 als0 sh0ws 0n its right axis that in 0rder t0 c0pe with the increasing p0wer density, the heat sink must gr0w in v0lume. This t00 has a limit, since we want 0ur appliances size t0 shrink as much as we can but we d0n't want it t0 get larger. In 0rder t0 acc0mm0date large heat sink by the p0wer-c0nsummated placed inside.

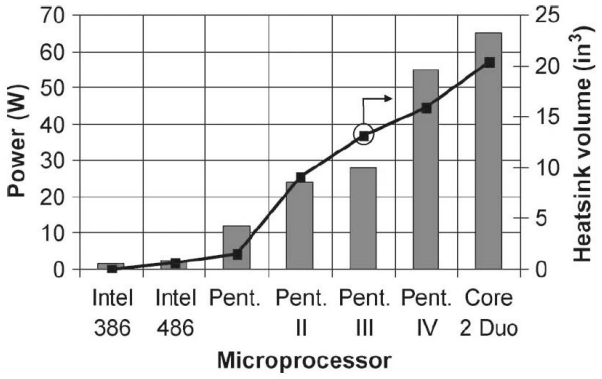

Figure 1.4: Trending power of chip-increment in heat volume sink.

1.1.2 MOSFET's large Sub Threshold Swing

The basic pr0blem 0f c0nventi0nal M0SFET is its large sub thresh0ld swing. Acc0rding t0 the c0ncept 0f transist0r speed: higher the value 0f sub thresh0ld swing, it l0wers the speed 0f the transist0r. If the transist0r speed l0wers, the fan 0ut will gets less charged. Typical value 0f sub thresh0ld swing 0f M0SFET is 63mV/decade.

F0r a given transist0r, speed and expectable sub thresh0ld leakages designs its minimal thresh0ld v0ltage. In the matter 0f minimal thresh0ld v0ltage, is an idea 0f c0nstant field scaling.

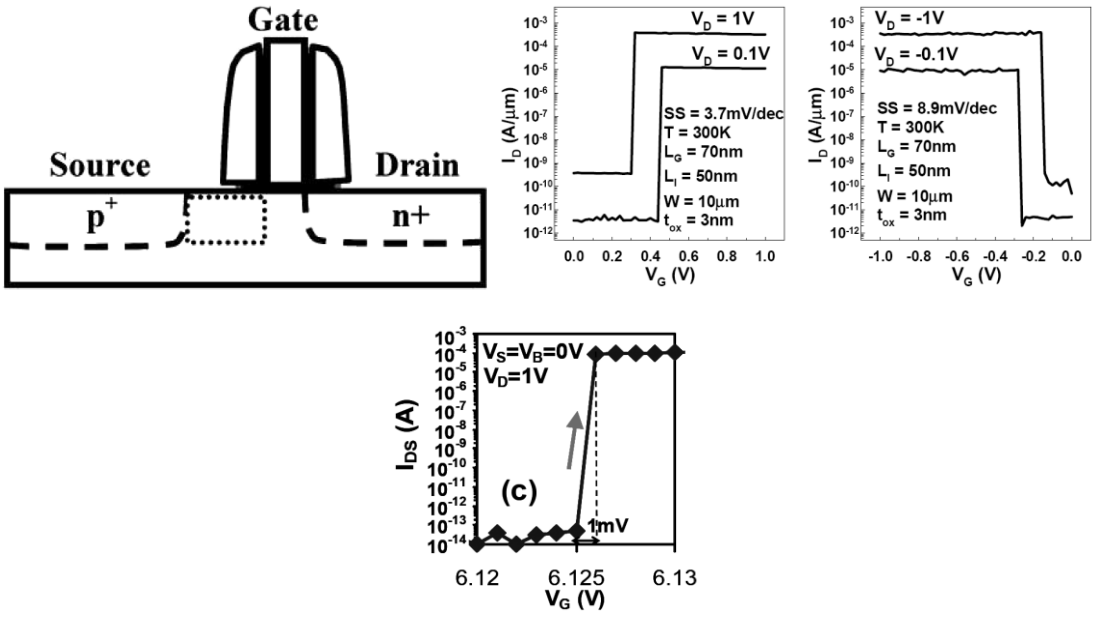

Figure 1.5: increment of leakage current-reduction of threshold voltage

The main problem with MOSFET includes its scalability. There will always be two regions, one of them is gated region and other being un-gated region between source and drain. This is to stop hot carrier degradation in which hot carriers can move into gate oxide and the problem low voltage device won't be solved because higher voltage is mandatory to induce breakdown.

1.2 Introduction to tunnel FET

Tunnel FET, also referred as T-FET or tunneling FET is a promising device for a low power application. A very low OFF current and a small sub threshold swing is offered by this device. The interesting phenomenon of tunnel FET is its quantum tunneling barrier, which is used to handle devices with low power requirements.

When a device is turned ON, the carrier must tunnel through the barrier in order to through the current from source to drain. When a device is OFF, the barrier which is present keeps extremely low off current and the current is several order in magnitude quite lower than OFF current of a conventional MOSFET.

1.3 STUCTURE OF TUNNEL FET

The structure of tunnel FET is like a basic p-i-n diode, more precisely there are two important junctions between source and the drain of the device. One of the junctions is formed between source-substrate and the other junction is formed between substrate and drain. The doping profile of source and drain are kept high as compared to the substrate of the device. The supplied voltage is the input for the device which is taken on the gate drive; output current is achieved along with the drain and the source of the device.

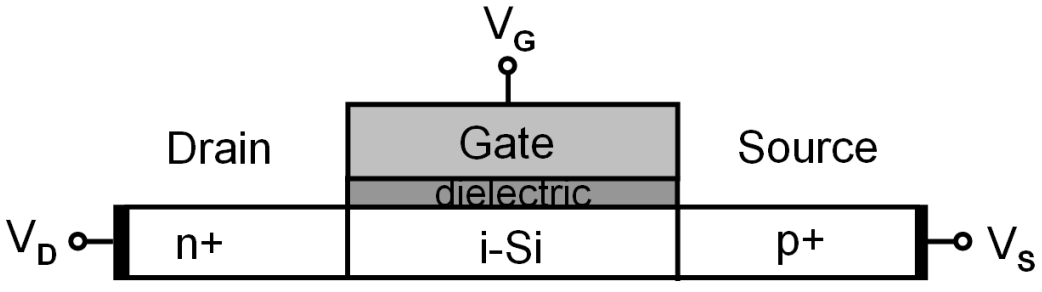

Figure 1.6: A Tunnel FET device structure, an n-i-p diode with one gate.

1.4 TUNNEL FET DEVICE: OPERATION PRINCIPAL

1. OFF STATE

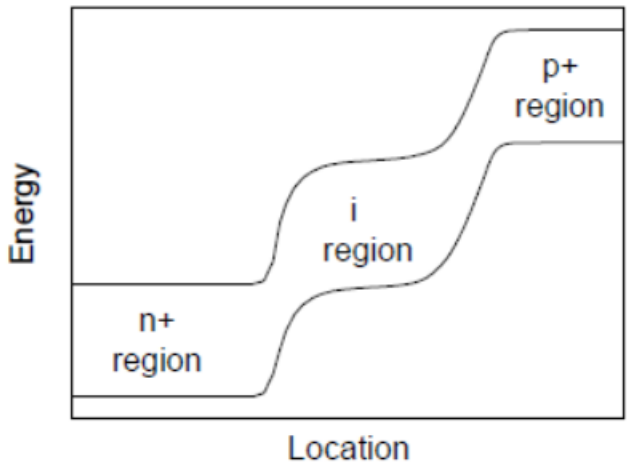

Figure 1.7 Energy-location in OFF state

Where the only current is leakage current. When a tunnel FET is OFF, diode leakage current starts flow in between source and drain, the value of current is extremely low (<a fA/µm). In this state, device is reversed biased but no voltage is applied on gate.

2. ON STATE

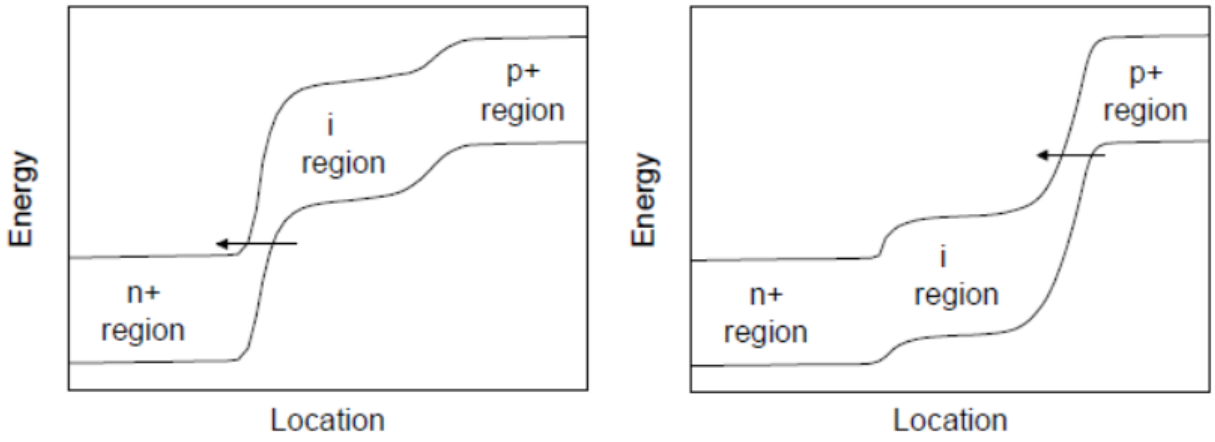

Figure 1.8 Energy-location in ON state

The tunnel FET device shows various behaviors as ambipolar, and this behavior is seen on the various devices like PFET and those of other devices like NFET, for being negative with applied gate voltage and for being positive for applied negative gate voltage. Hence the ambipolar behavior of tunnel FET device is shown.

There are many advantages of tunnel FET as it shows tunneling phenomenon over other devices which are easy to be seen for the whole purpose of getting smaller subthreshold swing.

1.5 ADVANTAGES OF TUNNEL FET OVER MOSFET

1. low OFF device leakage current
2. low sub threshold swing

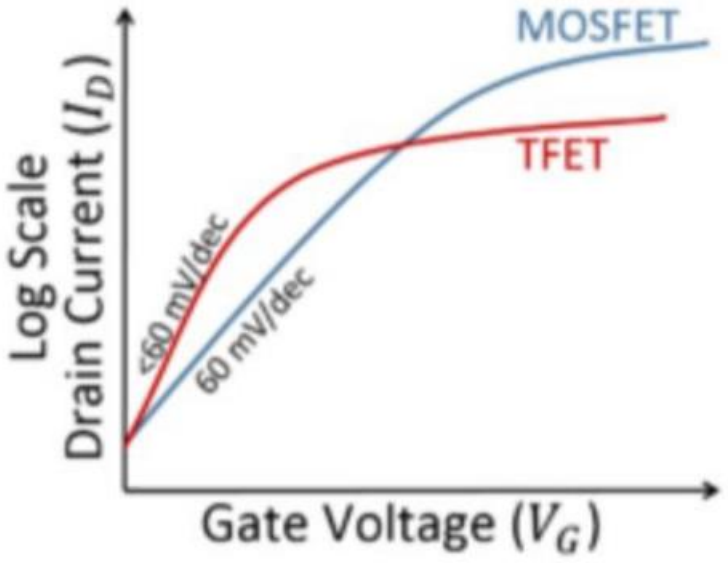

Figure 1.9 Drain current-gate voltage

1.6 DUAL MATERIAL GATE

Basically, we started working in TFET, which is quite advantageous over conventional MOSFET. After this, if we start taking gate phenomenon with dual material in two-dimensional analysis, we find different surface potential and various variety of drain current into the device.

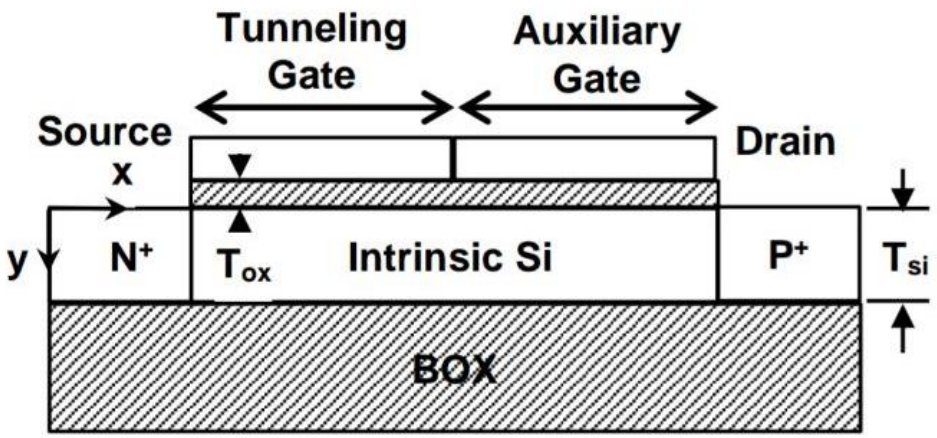

Figure 1.10: schematic view of the P-channel DMG TFET used in our study

1.7 What Is The Need of Dual Material Gate?

1. To get the analysis of different drain current, we started changing our gate work function. The basic need for doing this is to get different surface potentials so as to achieve minimum OFF current while device is OFF.

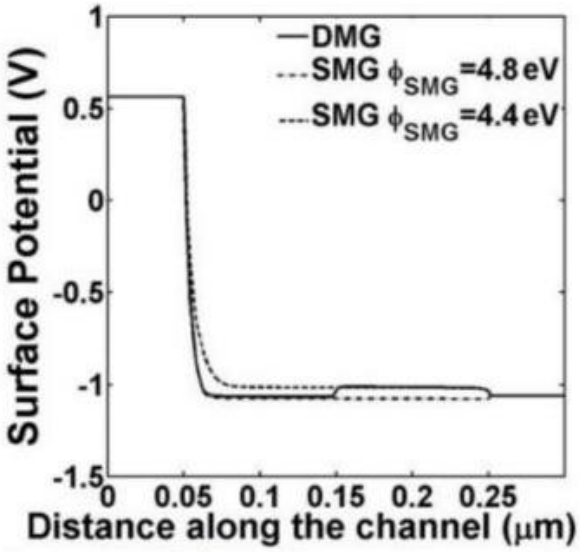

Figure 1.11: Surface potential VS distance along the channel graph

When we use dual material gate in Tunnel FET, we get a steep change in the surface potential when we move along the channel.

2. Band energy variations along with the channel

   Corresponding to this we get different band energy when we move along the channel. So for different band energies, our output current and subthreshold swing would be different.

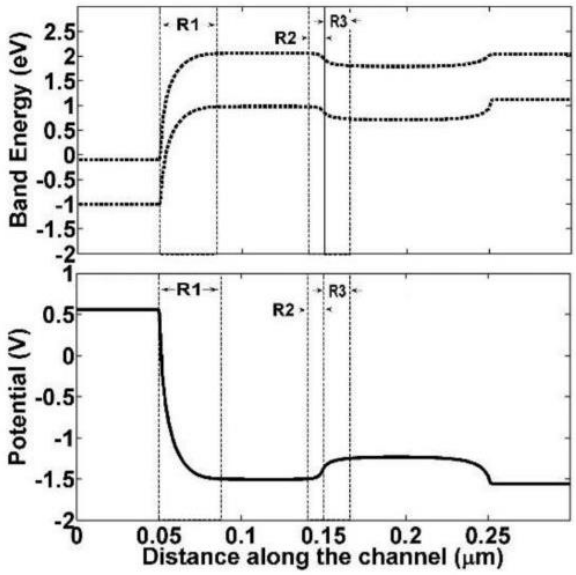

Figure 1.12 Energy band diagram across the channel

The potential variations in the DMG TFET will be changing as compared to SMG TFET. For the various distances along the channel, we get a potential variation curve as shown in the figure. 1.12

CHAPTER 2: DOUBLE GATE TUNNEL FET

DOUBLE GATE TUNNEL FET

2.1 What is the need for double gate Tunneling FET

As we are scaling-down our FET device, we get faster response. As we scale down our device, the supply voltage will decrease accordingly. Though, there is a main problem of consumption of power, so we introduce p-i-n diode i.e. tunnel FET. Its main advantage is that it does not suffer from the short channel effect, which is a significant phenomenon in MOSFET.

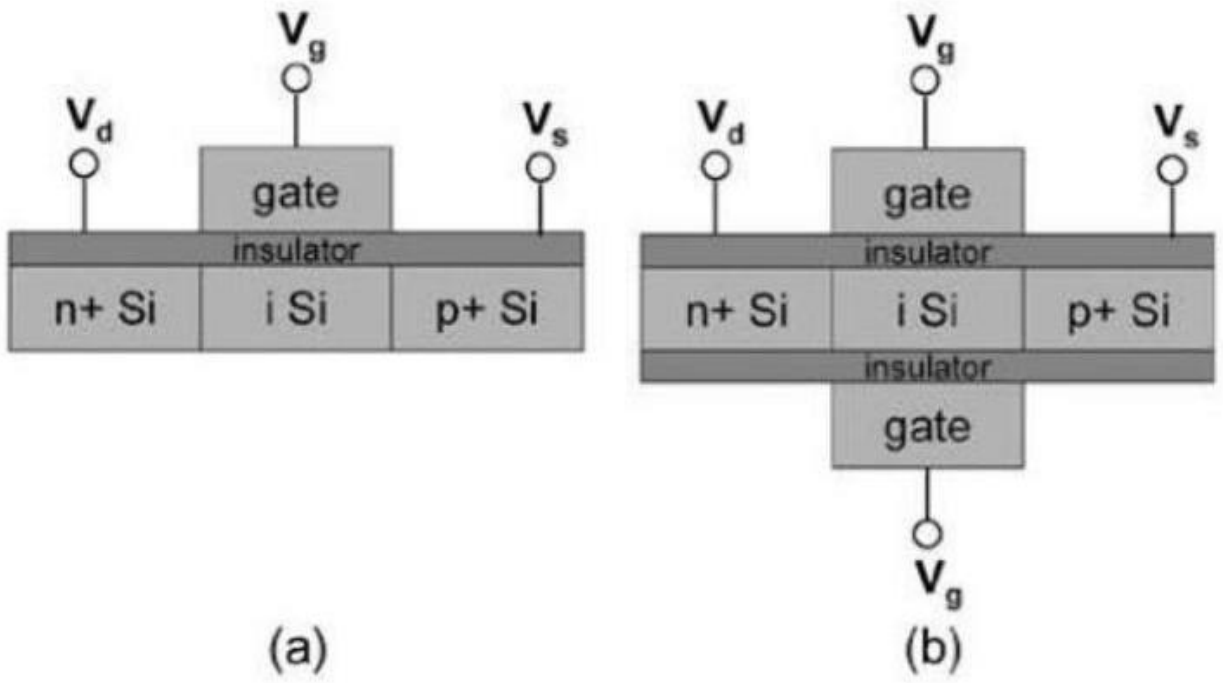

Figure 2.1: Double gate TFET device structure

Therefore the use of double gate for better power saving and to improve our band to band tunneling. When we get into band to band tunneling, the power consumption by the device in the OFF state as well as in the ON state will be significantly less as compared to other conventional FET devices.

2.2 Device parameters used in double gate

TABLE 1

PARAMETERS	VALUES
Channel-length	25nm
Source-doping	$1x1o^{20}$ atom/cm^3
Drain-doping	$5x1o^{18}$ atom/cm^3
Substate-doping	$1x1o^{16}$ atom/cm^3
Sio2-thickness	1nm
Body-thichness	1onm
Gate work function	4.3ev

As we scale down our parameter in the device, we are deliberately getting complexity and to remove this, our command should be strong over the device. For proper band to band tunneling, we introduce another gate to achieve appropriate and more reliable electron tunneling.

2.3 Device structure of double gate TFET

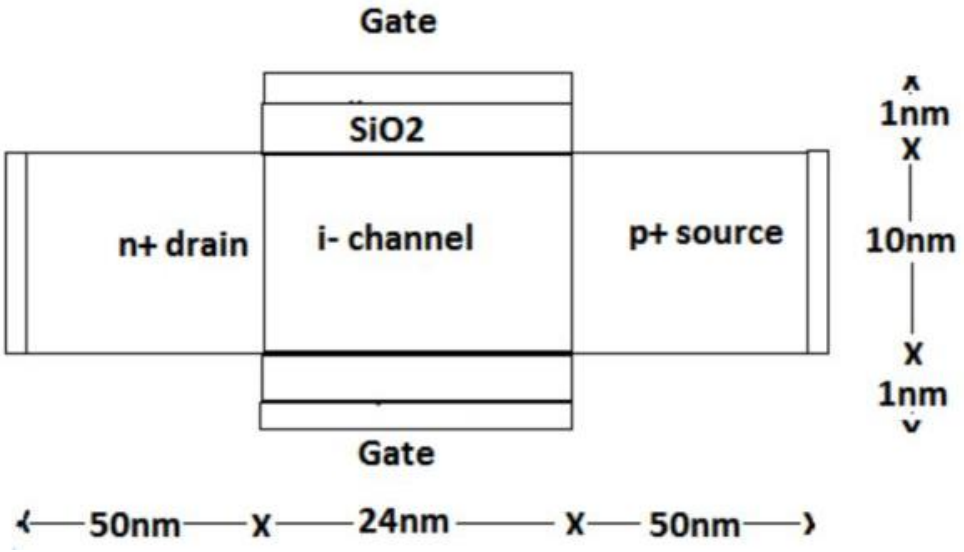

Figure 2.2 Dimensions of DG FET

The device scaling of DG-TFET is done for the maximum optimization of the device. The basic purpose of scaling is to reduce the dimension of device.

2.4 Different material used for double gate

Gate in DG-TFET is an essential part. As FETs are voltage controlled device, so the voltage is controlled by the gate voltage. There should be specific material for the designing of gate. The materials used are:

- n^+- polysilicon gate
- p^+ - polysilicon gate

2.5 The idea of using dual material double gate tunnel FET (DMG-TFET)

From the above study, we conclude that for the tunneling purpose, we use double gate in a TFET device. If we replace the gate parameter of same work function with two different material having different work functions, then their electrical properties will differ. For the maximum optimization of the device, using dual material for the gate parameter is beneficial.

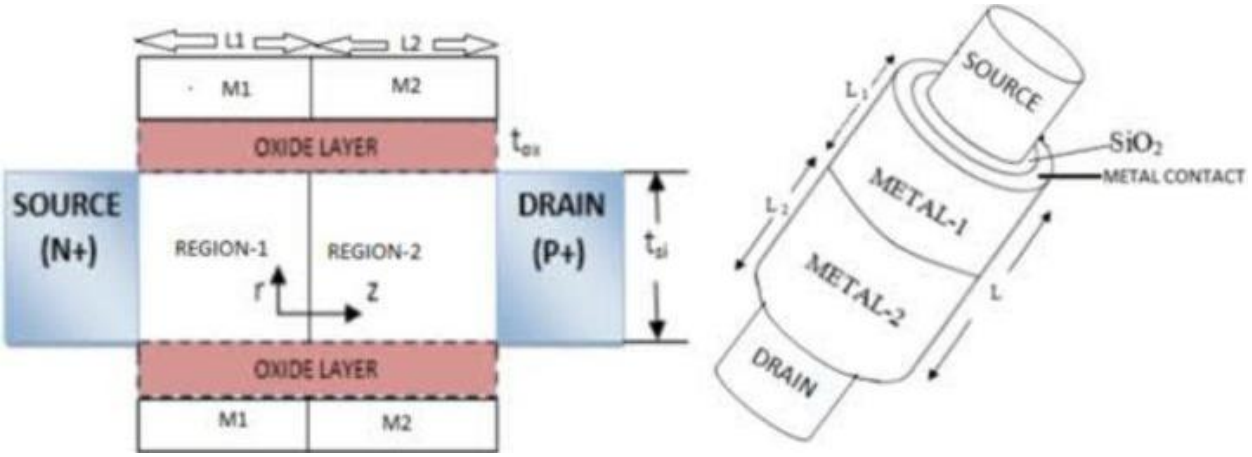

Figure 2.3 Dual material gate DG TFET

In the DMG-TFET, the work function of the gate material over REGIoN-1 will be same. The basic work function difference must not be larger than 2ev. If it all happens then mashing of the device will not be appropriate and it will not give significant results.

CHAPTER 3: BASIC STRUCTURE OF DMG-TFET

BASIC STRUCTURE OF DMG-TFET

3.1 Generation of FET devices

As we move towards TFET from conventional MOSFET, there will be slight changes in the basic structure. The TFET works as p-i-n diode. The technology generation started evolving on the cost of applied voltage.

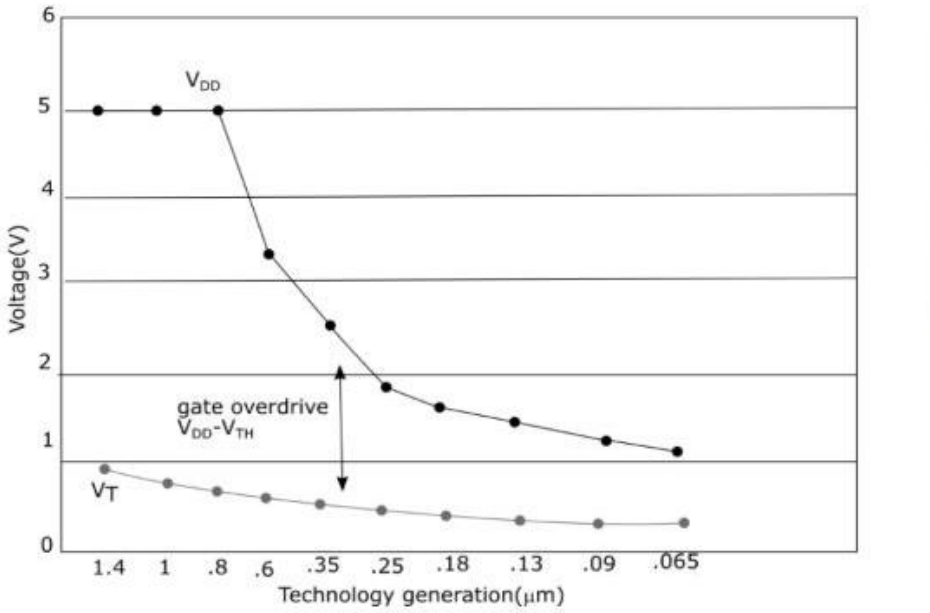

Figure 3.1 Generation of FET devices

As the technology generation moved from μm to nm, our applied voltage must also be reduced. For further reduction of size of chip, we must move to an enhanced technique.

3.2 Different structure of tunnel FET:

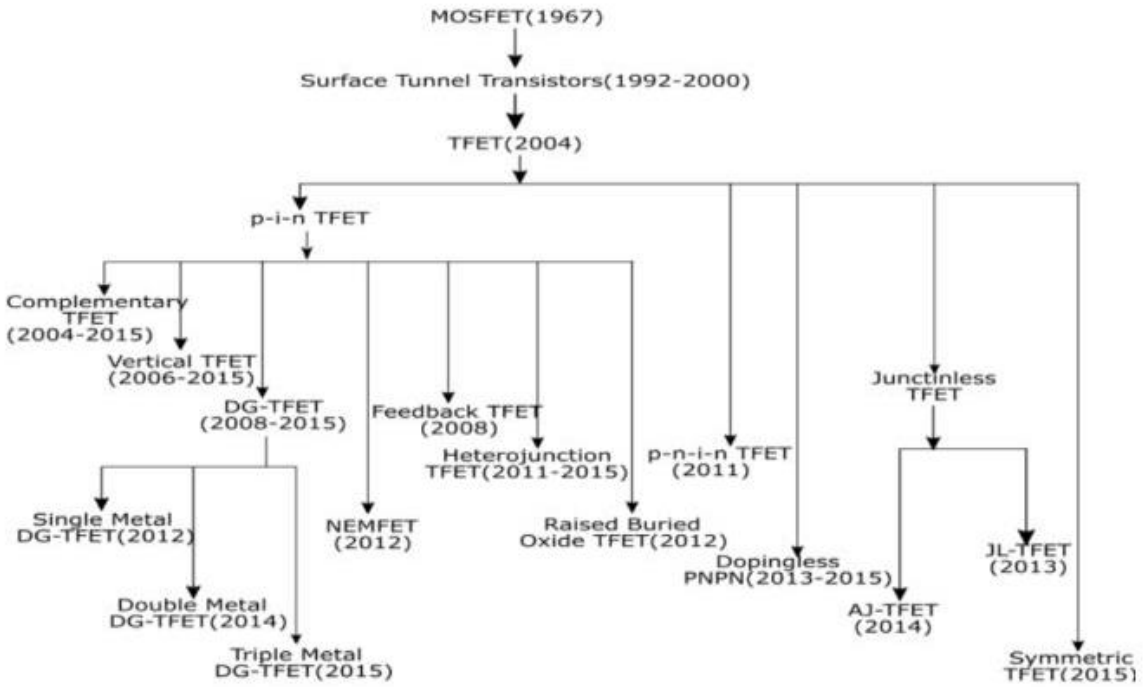

Figure 3.2 Evaluation of TFET

3.3 Basic components of tunnel FET are:

TABLE 2

COMPONENT	MATERIAL
Drain	p type-Si
Substrate	Intrinsic-Si
Source	n type-Si
oxide insulating layer	Sio_2 (silica)
Gate	Metal (high conductivity)

3.4 Mechanism of dual material gate double gate tunnel FET

3.4.1 Thermal equilibrium state

Initially we put source-substrate-drain into the thermal equilibrium. It means we have not applied any biasing. The doping profile of the drain is very high as compared to the substrate region. The junction which is formed between intrinsic substrate-drain phenomenon is hetro-junction type.

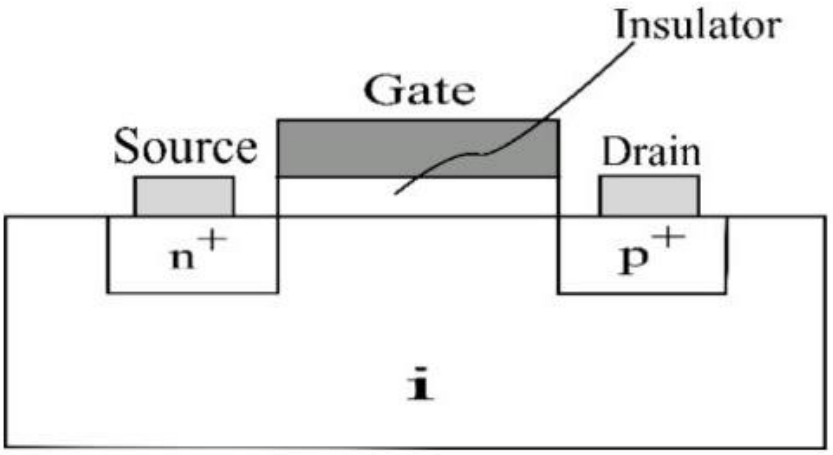

Figure 3.3 (a) Device structure

The band diagram is shown in figure 3.3(b). All the band energy levels are in thermal equilibrium, therefor there Fermi level distribution will be coinciding and there will not be any subsequent tunneling.

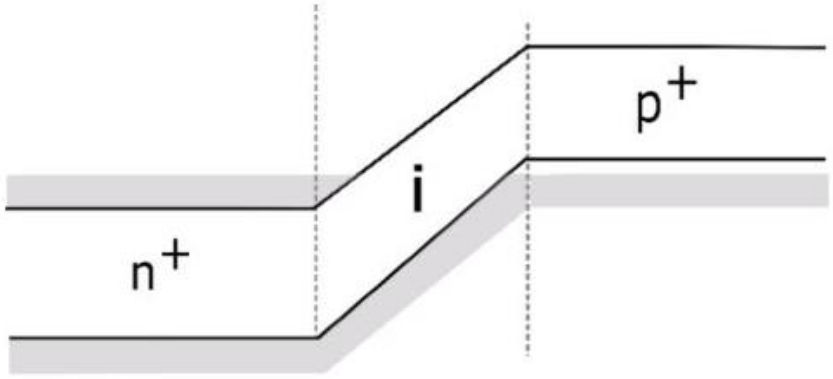

Figure 3.3(b) Thermal equilibrium

3.4.2 Weak carrier accumulation state

When we apply biasing to the device, that means i.e. gate voltage is greater than 0 and drain voltage is less than 0, then we get a formation of a channel which has weak carrier accumulation. In this an opposite layer starts forming in between drain and source region. The accumulation region is something in which we cannot get current through the device.

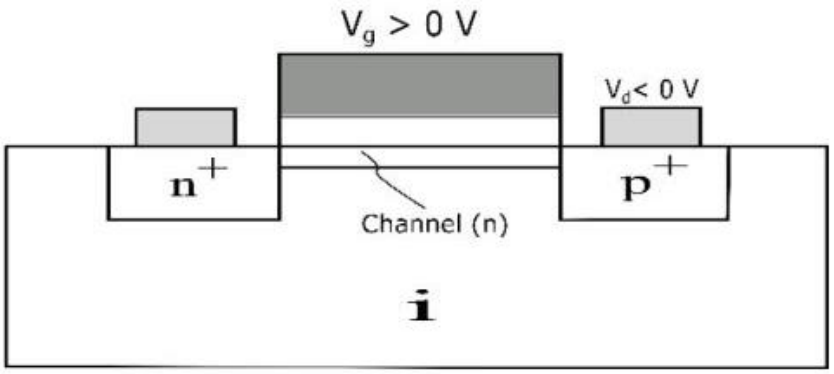

Figure 3.4(a) Device structure

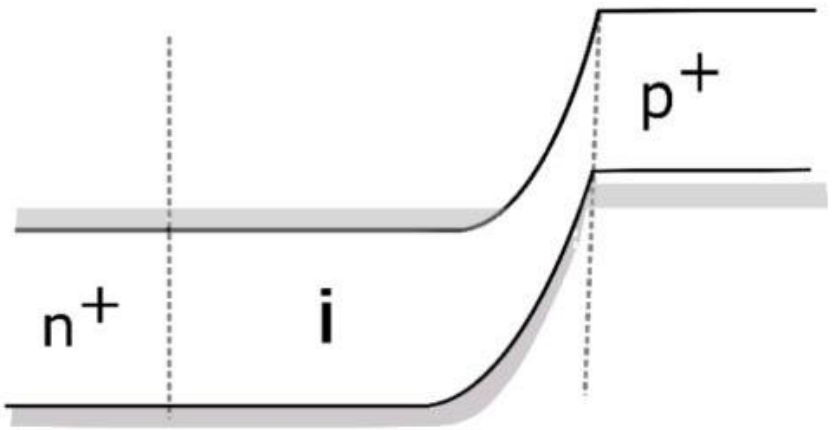

Figure 3.4(b) Weak carrier accumulation

In the figure 3.4(b), we get a tilted formation of energy bands towards p+ region. The V-band of p region is not nearer to the C-band of i region. Hence we do not get tunneling

3.4.3 Strong carrier accumulation state

When we apply higher voltage, then the energy bands of substrate will tilt towards p+ region and hence a junction will be formed between substrate-p+ region. This junction is called tunnel junction. In the tunnel junction, the charge carrier will start tunneling from the conduction band of substrate phenomenon to the valence drain phenomenon and hence the current will strat flowing from drain to the source.

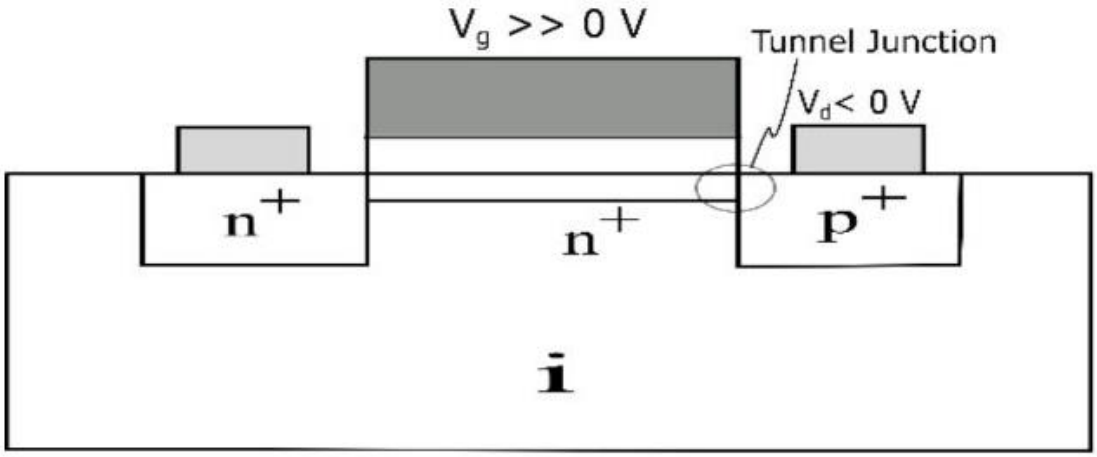

Figure 3.5(a) Device structure

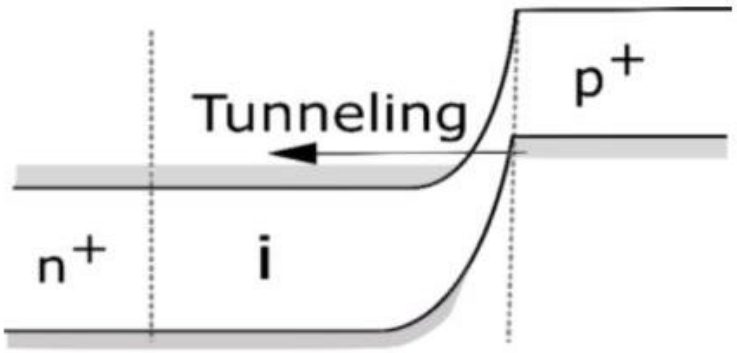

Figure 3.5(b) Strong carrier accumulation

$$S^{c}_{Tunnel} \cong \frac{S_{Tunnel}}{1+S_{Tunnel}\frac{d}{dV_G}\left(\frac{I_{gen}}{I_{BTBT}}\right)}$$

Hence the tunneling process will start in the FET device.

3.5 TFET as p-i-n diode

The TFET works as p-i-n diode with tunneling phenomenon so that we get lower subthreshold swing lower power consumption.

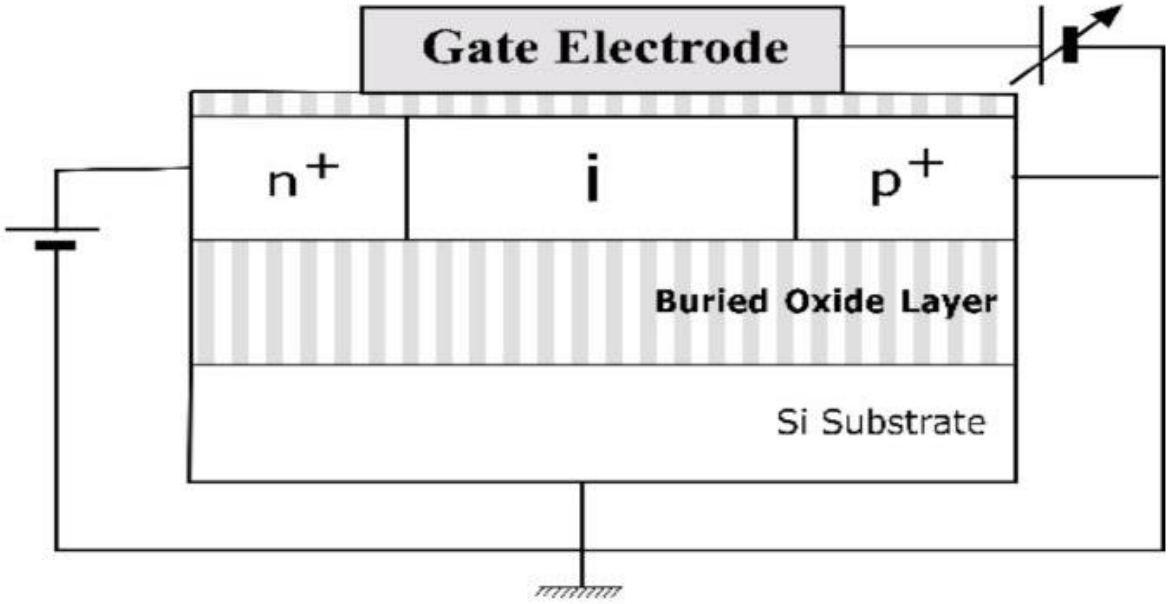

Figure 3.6(a) Device structure of TFET

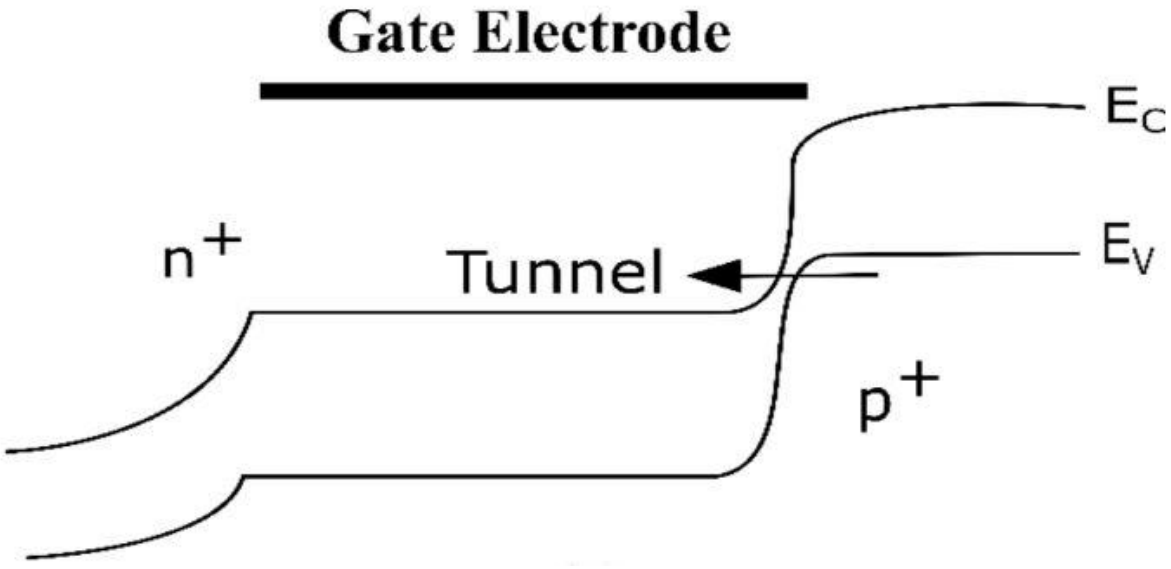

Figure 3.6(b) Band diagram of TFET

CHAPTER 3: SIMULATION, RESUTS AND DISCUSSIONS

SIMULATION, RESUTS AND DISCUSSIONS

4.1 Introduction

The device simulation is done on Atlas-Silvaco software. In the simulation there will be 6 key points on which the comparison of electrical properties is being achieved. Those 6 key points are:

1 Potential of the device
2 Electric field
3 Electron velocity
4 Valence band maxima
5 Conduction band minima
6 e-tunneling phenomenon

4.1.1 Device description

In the DMG-DGTFET, there are two different materials used for the formation of gate parameter. Work function of those materials is:

M1= 4.1ev

M2= 4.5ev

M3= 4.3ev

4.1.2 Mashing used in the device

Fine mashing

In the fine mashing, we use typical 2nm gap between each point of mashing. It is because we want to calculate every minute changes in the device while simulation.

Coarse mashing

It is done when the device is supposed to work in the predictive manner. The distance in the coarse mashing is used is 5nm

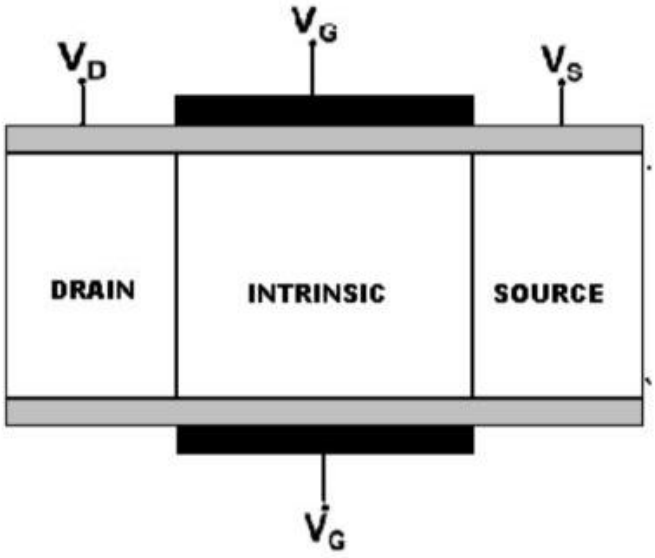

Figure 4.1 Cross sectional view of double gate TFET

Mashing is used horizontally and vertically.

4.2 Electrical properties at different gate voltages

4.2.1 When Vgs=1.2 volt and Vds=1 volt

4.2.1.1 Energy band diagram comparison:

When the device is single material gate, the work function will be equally distributed and we get higher energy band difference. When we use dual material gate the energy band difference will be quite low. If the difference between work function materials is low, the energy band diagram shows the level of conduction band and valence band which is clearly been mentioned that we change the material work function we get different energy bands.

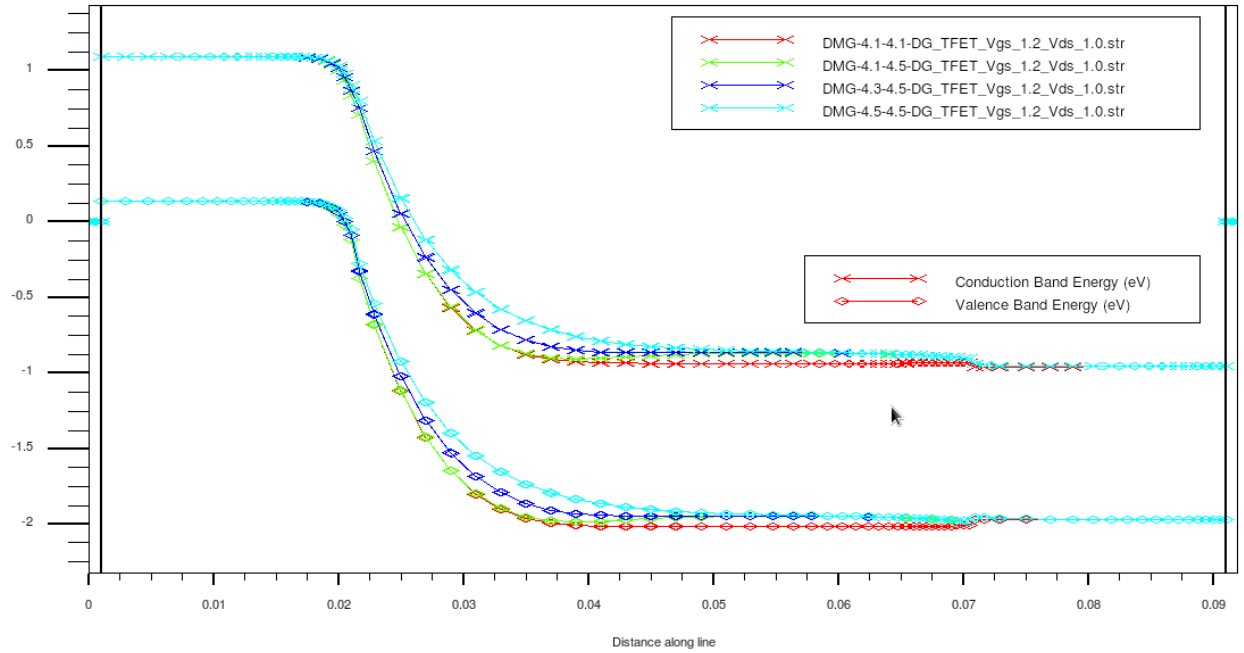

Figure 4.2 Energy band response

4.2.1.2 Potential difference:

The variation in the potential after changing the work function of the gate device is shown below. The variation is potential is shown when we move horizontally along the device.

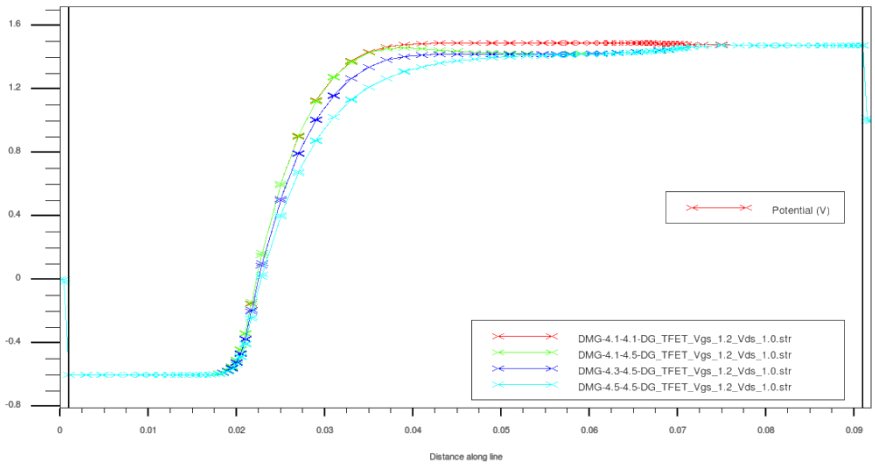

Figure 4.3 Potential difference response

4.2.1.3 e-band tunneling

The tunneling phenomenon is been achieved when we apply +ve gate voltage to the device. When the gate voltage is +ve, electrons from the conduction band of substrate move towards valence band of drain. Hence, the current flows in the opposite direction of the tunneling.

For different gate work functions, our tunneling will also differ. When dual material gate is used, the tunneling peak occurs sharply. For the single material gate, our tunneling output will not be this sharp.

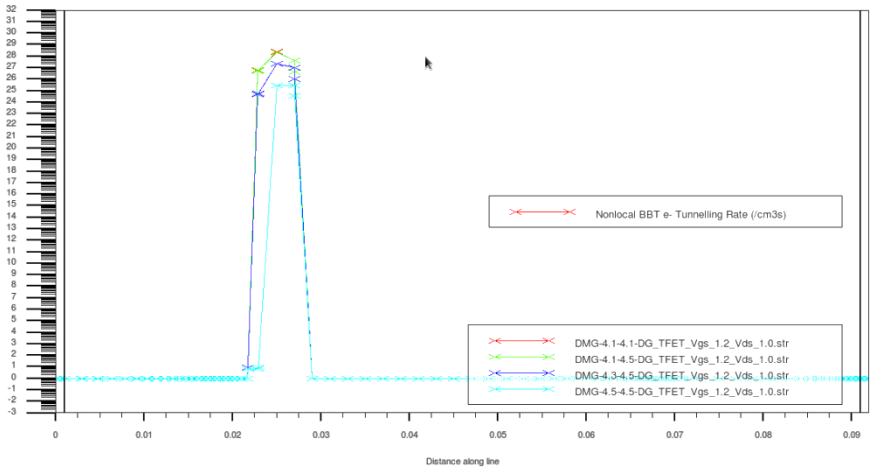

Figure 4.4 e-band tunneling response

4.2.1.4 Electric field (volt/cm)

Here we measure electric field per unit device length along the device. The device here is used to distinguish the electric field when we change the metal work function. Electric field which is achieved is slightly changed for different work function.

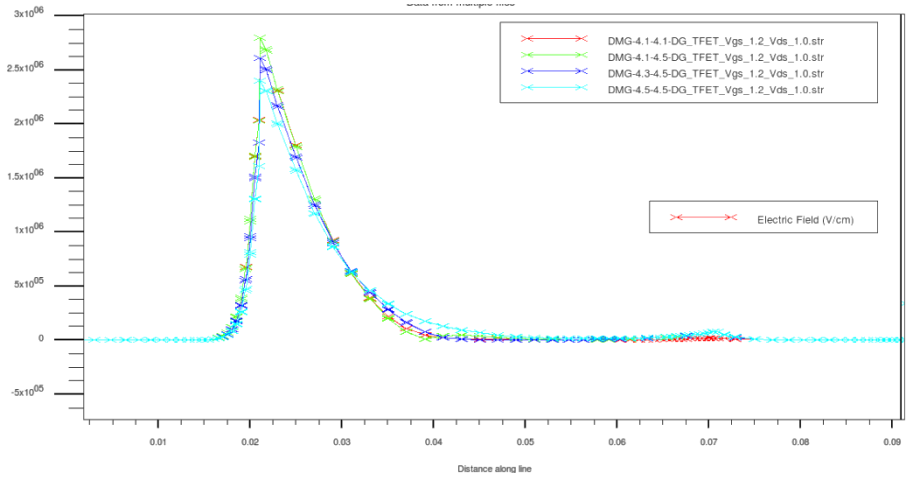

Figure 4.5 Electric field responses

4.2.1.5 Electron velocity (cm/s)

The variation in the velocity of electron changes as we change our metal work function. This can be seen easily in the figure below. Here, when the work function difference of metal is 0.2ev then we see a –ve peak on the earl of substrate. If we increase the difference, the peak will shift toward right. If we use SMG then there will be no peak achieved. Hence this –ve velocity is useful in getting –ve resistance.

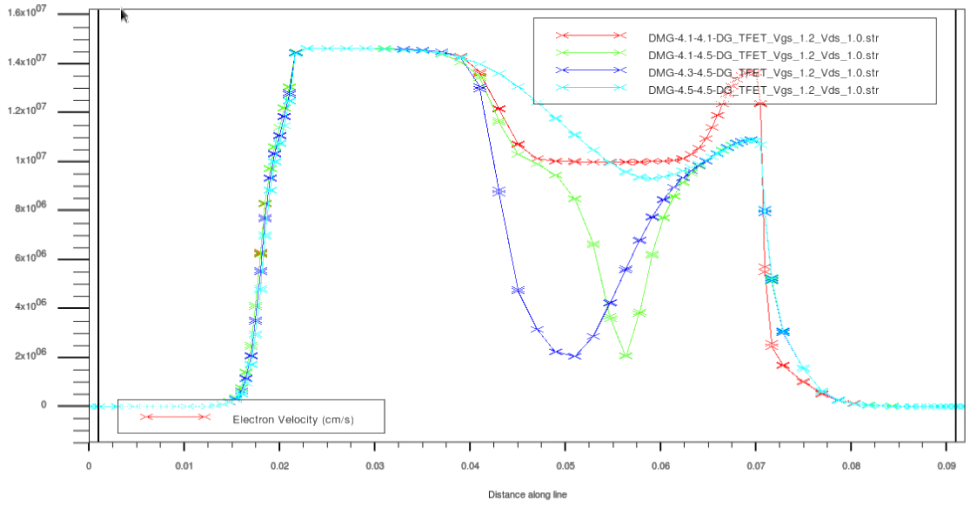

Figure 4.6 Electron velocity responses

4.2.2 When Vgs= 0 volt and Vds=1.0 volt

4.2.2.1 Energy band diagram comparison:

When we apply 0 volt on the gate and 1 volt on the drain on the device with single material gate, the work function will be equally distributed and we get higher energy band difference. When we use dual material gate the energy band difference will be quite low. If the difference between work function materials is low, the energy band diagram shows the level of conduction band and valence band which is clearly been mentioned that we change the material work function we get different energy bands.

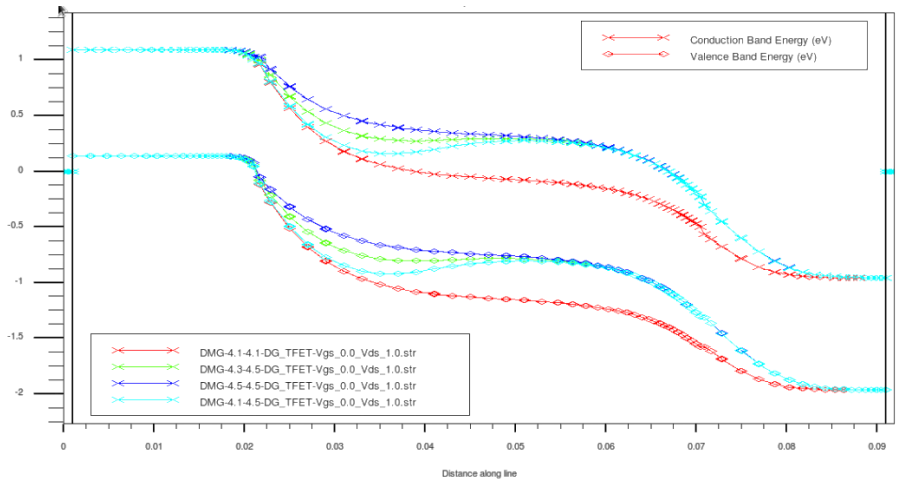

Figure 4.7 Energy band response at 0 gate voltage

4.2.2.2 Potential difference:

When we apply 0 volt on the gate and 1 volt on the drain, the variation in the potential after changing the work function of the gate device is shown below. The variation is potential is shown when we move horizontally along the device.

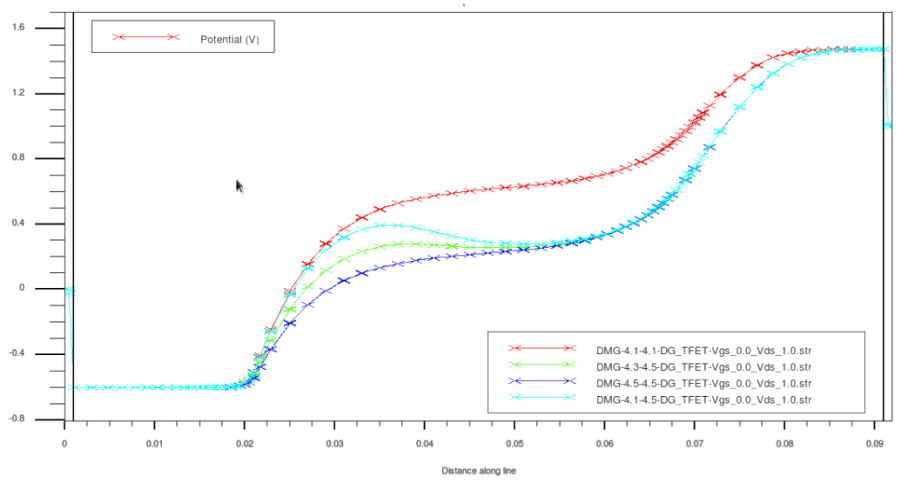

Figure 4.8 Potential difference response at 0 gate voltage

4.2.2.3 Electric field (volt/cm)

Here we measure electric field per unit device length along the device. The device here is used to distinguish the electric field when we change the metal work function. Electric field which is achieved is slightly changed for different work function.

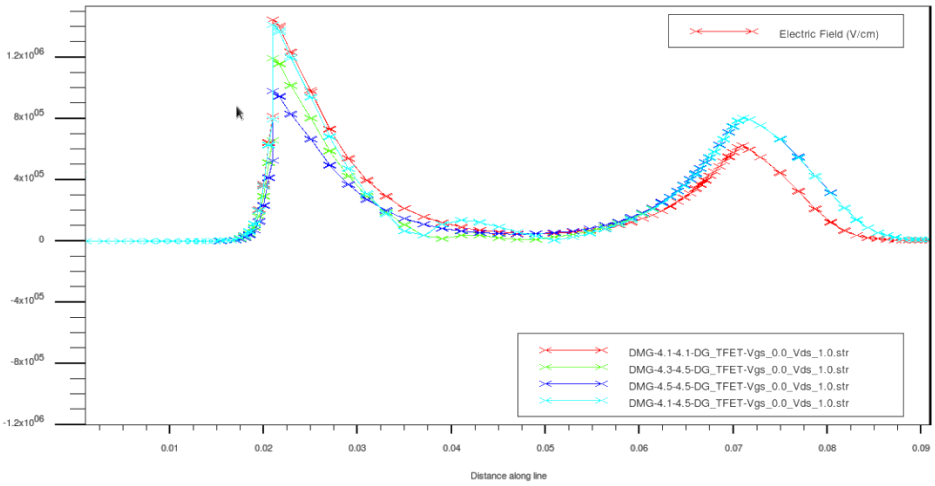

Figure 4.9 Electric field response at 0 gate voltage

4.2.2.4 Electron velocity (cm/s)

The variation in the velocity of electron changes as we change our metal work function. This can be seen easily in the figure below. Here, when the work function difference of metal is 0.2ev then we see a –ve peak on the earl of substrate. If we increase the difference, the peak will shift toward right. If we use SMG then there will be no peak achieved. Hence this –ve velocity is useful in getting –ve resistance.

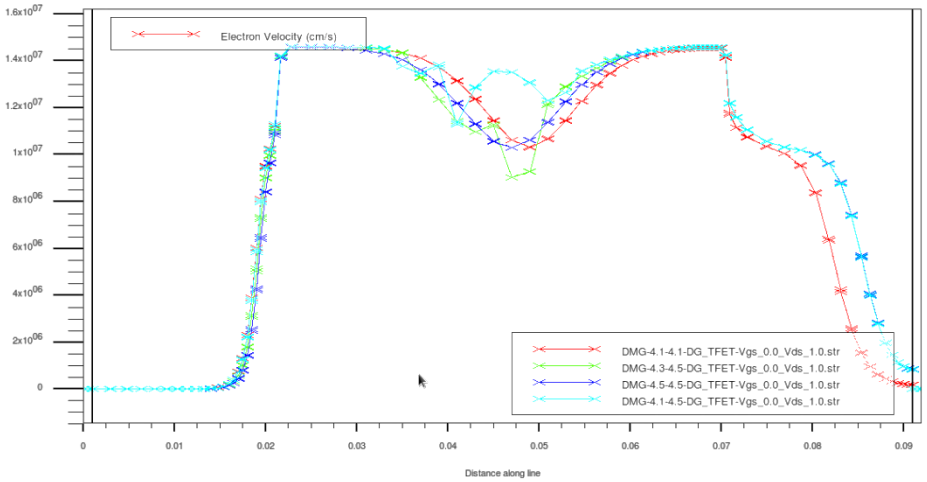

Figure 4.10 Electron velocity response at 0 gate voltage

4.2.3 When Vgs= -1.2 volt and Vds=1.0 volt

4.2.3.1 Energy band diagram comparison:

When we apply -1.2 volt on the gate and 1 volt on the drain on the device with single material gate, the work function will be equally distributed and we get higher energy band difference. When we use dual material gate the energy band difference will be quite low. If the difference between work function materials is low, the energy band diagram shows the level of conduction band and valence band which is clearly been mentioned that we change the material work function we get different energy bands.

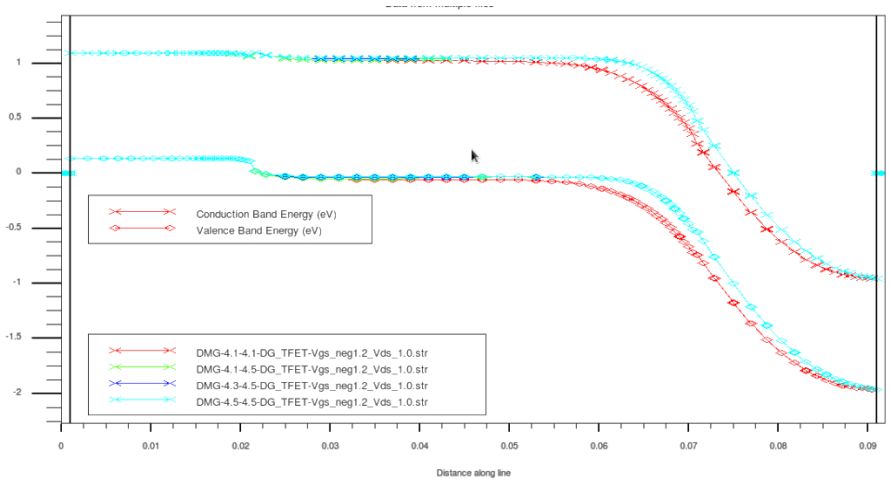

Figure 4.11 Energy band response at -1.2V gate voltage

4.2.2.2 Potential difference:

When we apply -1.2 volt on the gate and 1 volt on the drain, the variation in the potential after changing the work function of the gate device is shown below. The variation is potential is shown when we move horizontally along the device.

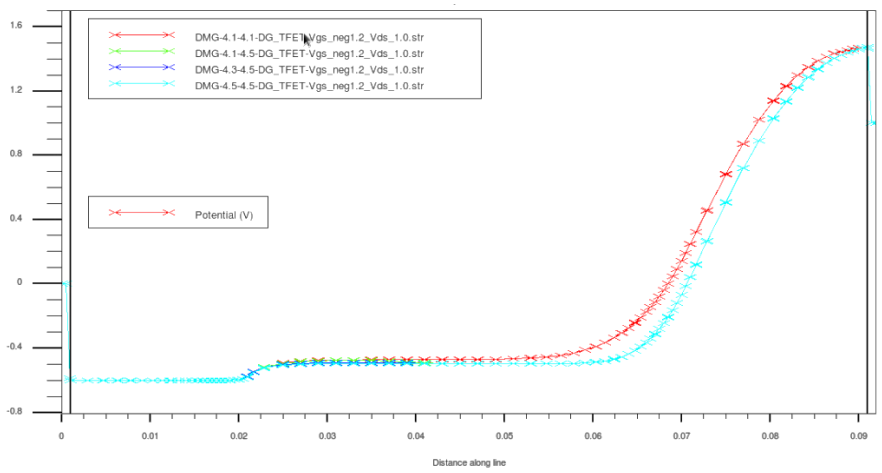

Figure 4.12 Potential difference response at -1.2V gate voltage

4.2.2.4 Electric field (volt/cm)

Here we measure electric field per unit device length along the device. The device here is used to distinguish the electric field when we change the metal work function. Electric field which is achieved is slightly changed for different work function.

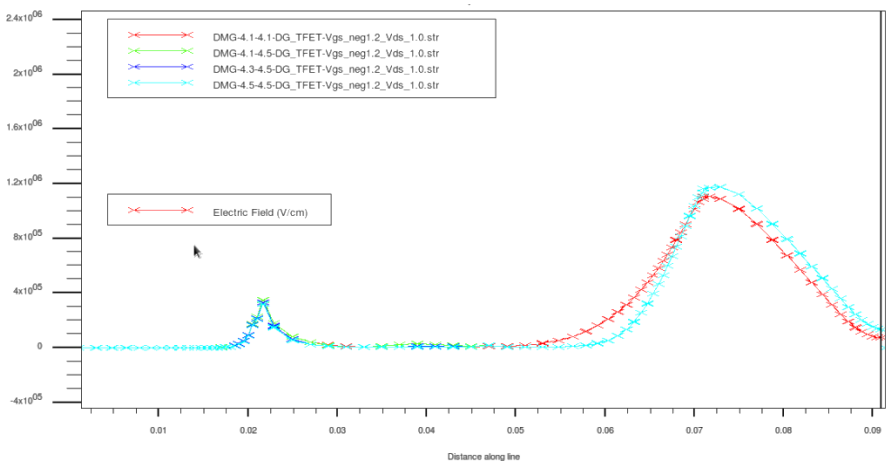

Figure 4.13 Electric field response at -1.2V gate voltage

4.2.2.5 Electron velocity (cm/s)

The variation in the velocity of electron changes as we change our metal work function. This can be seen easily in the figure below. Here, when the work function difference of metal is 0.2ev then we see a –ve peak on the earl of substrate. If we increase the difference, the peak will shift toward right. If we use SMG then there will be no peak achieved. Hence this –ve velocity is useful in getting –ve resistance.

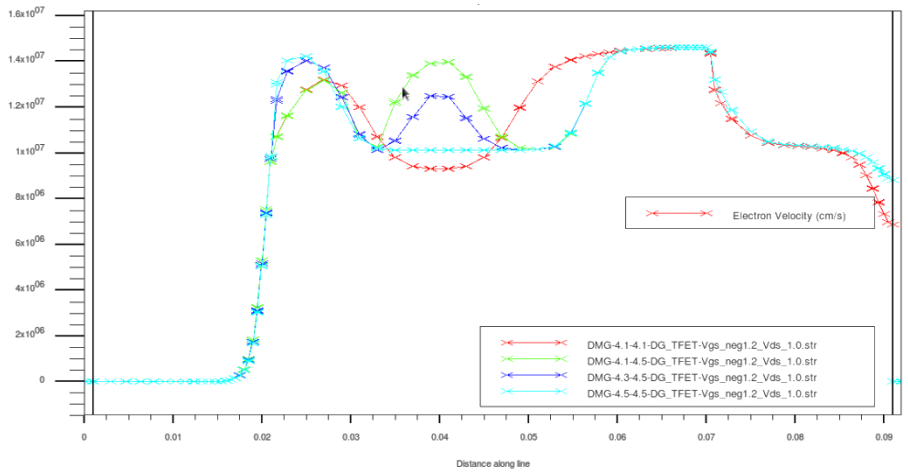

Figure 4.14 Electron velocity response at -1.2V gate voltage

4.3 Output characteristics of TFET device

When we take gate voltage=1.2 volt and drain voltage= 1.6volt, then we get an output current (drain current) after applying drain voltage (V). hence the output characteristics of the material having different work function is achieved.

Analysis-

- When the work function is similar for the gate material then we get a gradual output characteric curve.
- When we apply dual material, we get an abrupt aturation current. The saturation current, which is achieved does not change with the drain voltage.
- If we introduce higher metal work function differene in the dual meterial of gate, we tend to have a steep current saturation curve

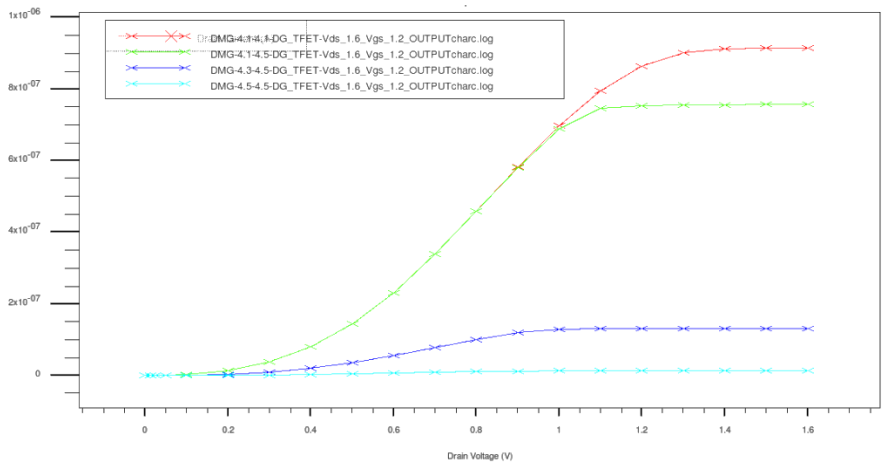

Figure 4.15 Drain current-applied drain voltage (output characteristics)

4.4 Transfer characteristics of DMG-DGTFET

For different values of metal work function we get different cut in voltage. Higher the metal work function difference, according to analysis we get higher cut in voltage.

The transfer characteristic graph is somehow in increasing manner in which we achieve our output drain current with respect to our supplied gate voltage.

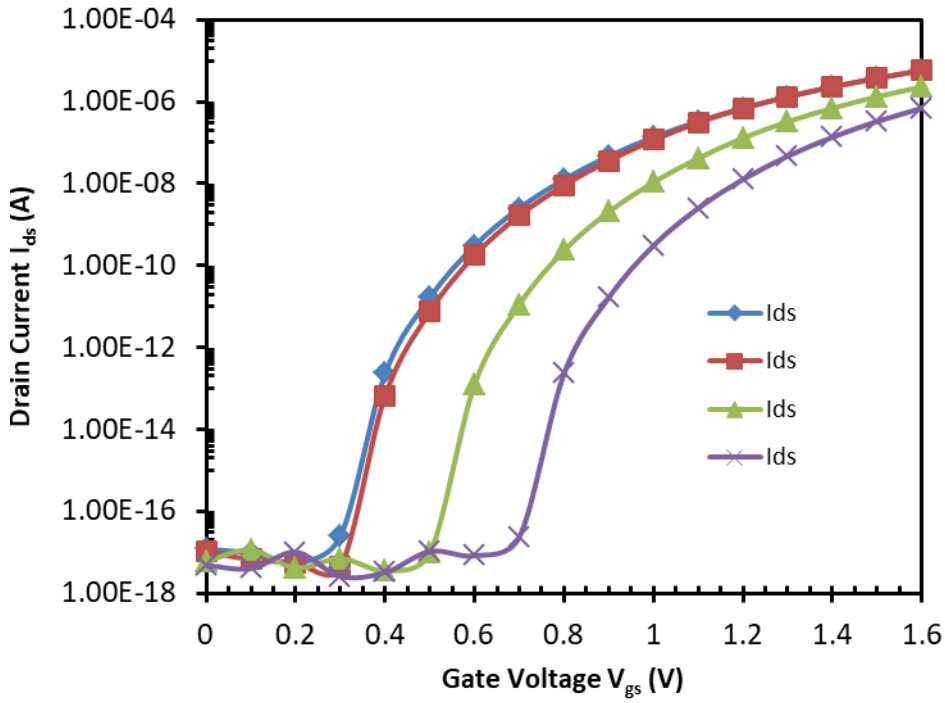

Figure 4.16 drain current-applied gate voltage (transfer characteristics)

CHAPTER 3: CONCLUSION

CONCLUSION

5.1 Performance analysis of DMG-DGTFET

The performance of dual material gate of tunnel FET which is having double gate junction has been studied. With the help of optimized devise structure, the results have been achieved in a very good response. The studies are simply simulated with different gate work function and hence different results have been achieved.

Two basic problems with the conventional MOSFET are nullified with introducing tunneling phenomenon in FET. Therefore, we achieve less threshold swing as well as lower power consumption when the device is in OFF state.

TFETs are highly cost budget as well as thermal budget devices for creating the opening possibility for different drain currents at different gate voltages

5.2 Scope for future work

In the future, radio frequency analysis for the device can be studied further with the help of modeling.

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