CURRENT DIFFERENCING DIFFERENTIAL INPUT TRANSCONDCUTANCE AMPLIFIER AND ITS APPLICATION

A

DISSERTATION

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Candidate's Declaration

I, **Anil Parmar**, Roll No. **2K15/C&I/04**, student of **M. Tech (Control & Instrumentation)**, herewith declare that the dissertation entitled "**Current differencing differential input transconductance amplifier and its application**", under the supervision of Prof. Pragati Kumar of Electrical Engineering Department, Delhi Technological University, in partial fulfilment of the need for the award of the degree of Master of Technology, has not been submitted elsewhere for the award of any degree.

I herewith solemnly and sincerely affirm that all the particulars declared above by me are true and correct to the best of my knowledge and belief.

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Certificate

This is to certify that the dissertation entitled **"Current differencing differential input transconductance amplifier and its application"** submitted by **Anil Parmar** in completion of major project dissertation for the master of Technology degree in **Control & Instrumentation** at Delhi Technological University is an authentic work carried out by him underneath my superintendence and guidance.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Place: Delhi

Date: .07.2017

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ABSTRACT

Ever since the introduction of current conveyor as basic building block in analog signal processing, several alternative active building blocks have been introduced so far. This has become attainable due to the developments in the semiconductor manufacturing technologies (both bipolar as well as CMOS). throughout the last twenty years, various modifications have been done in the architecture of the current conveyor and many derivatives of this block have appeared in the literature. Current differencing differential input transconductance amplifier combines the features of a current differencing unit (current conveyor) and an operational transconductance amplifier. Current differencing differential input transconductance amplifier can be used to perform the entire regular signal processing application such as amplifier, integrator, differentiator and filters etc. The present work deals with the signal processing application of current differencing differential input transconductance amplifier in filters. In this thesis, we have proposed various circuits which is based on current differencing differential input transconductance amplifier. All the circuits given during this thesis are simulated in PSpice.

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LIST OF SYMBOLS, ABBREVIATIONS

S. No	Symbols	Descriptions
1.	g_m	Transconductance
2.	Z_{in}	Input Impedance
3.	V_{in}	Input voltage
4.	I_{in}	Input current
5.	I_{B1}, I_{B2}	Bias currents
6.	I_o	Bias current
7.	R_n, R_p	Internal resistance of port n and p
8.	I_p, I_n	Input currents at p and n
9.	I_{x+}, I_{x-}	Output currents at x+ and x-
10.	W/L	Width to length ration
11.	V_{SS}	Source supply voltage
12.	V_{DD}	Drain supply voltage
13.	Q	Quality factor
14.	w_o	Cut off frequency
15.	CDDITA	Current differencing differential input transconductance amp.
16.	CDU	Current differencing unit
17.	OTA	Operational transconductance amplifier
18.	BJT	Bipolar junction transistor
19.	CMOS	Complementary metal oxide semiconductor
20.	DVCVS	Differential input voltage controlled current source

21.	CFA	Current feedback amplifier
22.	CDTA	Current differencing transconductance amplifier
23.	OTRA	Operational transresistance amplifier
24.	CCCDTA	Current controlled current differencing transconductance amp.
25.	CCIII	Current conveyor 3rd generation
25.	CDCC	Current differencing current conveyor
26.	CIDITA	Current inverting differential input transconductance amplifier

CHAPTER-1
Introduction

1.1 Introduction:

The dissertation deals with implementation of current differencing differential input transconductance amplifier (CDDITA) and its application in analog filter design. In this thesis, we present current differencing differential input transconductance amplifier (CDDITA) and its application in design of I^{st} order filters and lossless grounded inductor.

The advent of integrated circuit analog signal processing may be traced to the introduction of integrated circuit operational amplifier in the mid-sixties. The classical internally compensated operational amplifiers were initially used in analog signal processing and almost all conceivable applications in signal processing were developed around the classical integrated circuit operational amplifier.

This amplifier was a bipolar implementation of the differential input voltage controlled voltage source (DVCVS). The DVCVS is a good choice if the input source is having a very low output impedance and the load is also having a very high impedance. But there are many signal processing situations where a very high output impedance signal source is to drive a very low impedance load or very low impedance signal source is to drive a low output impedance load. In that case, the DVCVS is not a suitable amplifier configuration to be used is such application.

With the rapid advancement in digital technologies CMOS has become the preferred choice for fabrication of the integrated circuits, because of its very high packing density and low power requirements.

During the past few decades, various current mode active blocks have been introduced due to their better performance compared to voltage mode active building blocks (operational amplifiers). They have better bandwidth, broader dynamic range, higher slew rate and greater linearity than voltage mode active blocks.

Before we outline the work presented in this dissertation, it is worthwhile to discuss the context in which the work has been undertaken.

1.2 Voltage mode, current mode and mixed mode signal processing:

Over the past couple of decades, the area of analog signal processing has been viewed in terms of the dominant variables of a circuit viz voltage and current. The signal processing

of any electronics and electrical circuits where voltages and currents are important variables. The main cause of using voltage and current in signal processing is that the active devices which are operate usually with resistances or conductance [3].

Voltage mode signal processing

In signal processing circuits, there are two main parameters that are mostly considered: either voltage or current. While others are considered as an unwanted parasitic. In the past, voltage has been considered as the main variable in signal processing. Approach in terms of voltages instead of current is very easier and simpler for the designers [3]. The input impedance of voltage mode device is very high, ideally it is infinity, so that there is no loss of signal power. Through this arrangement, it is possible to connect more input terminals parallelly with only single output terminal. The output impedance of the terminals of voltage mode device are ideally zero. Having low output impedance makes it possible to drive heavy load by single output [3]. There are parasitic resistances as well as capacitances present at input terminals of voltage mode circuit, which may affect performance of circuit. These parasitic also affect output terminals, which is not allowed to drive heavy load at output terminals. The effect of inductance parasitic has not significant meaning in VLSI processing. The main advantage of voltage mode circuits that a single voltage-output terminal could supply more input terminals which are connected parallelly.

Current mode signal processing

In current mode signal processing, the dominant variable is current (both input as well as output). The devices used (amplifiers) have very low input impedance, ideally zero and very high output impedance, ideally infinity. As a result, cascading of inputs and outputs with voltage device are not possible. These devices are characterized by very small voltage swings which result in fast speed. Also, the signal processing circuitry becomes simpler and lesser number of components are required (for adding currents no extra amplifiers is needed). Another important feature of the current mode device is large dynamic range of the input quantity.

Mixed mode signal processing

In this mode of signal processing both current as well as voltage variables are the integral part of the signal space of the application and help in matching the impedance levels at the input and output side.

1.3 Various current mode active building blocks used in Analog Signal Processing:

As we deal with CDDITA which is current mode active building block for which the input is differential configuration and output is also differential stage, we now present a summary of different active building block proposed recently so that the terminal behavior CDDITA may be compared with similar building block proposed recently. These blocks have been categories in terms of the nature of the input configuration (single/ differential), nature of the output stage (single ended /differential), the level of the impedance of the input/ output terminals.

Table 1.1 Comparison of current mode active building blocks

DEVICE NAME	INPUT QUANTITY		OUTPUT QUANTITY		IMPEDANCE	
	Voltage or Current	Single ended or Differential	Single ended or Differential	Voltage or Current	Input	Output
1.OTRA Operational transconductance amplifier	Current	Differential	Single	Voltage	Low	Low
2.CDBA Current differencing buffered amplifier	Current	Differential	Single	Voltage	Low	Low
3.CCCDBA Current controlled CDBA	Current	Differential	Single	Voltage	Low	Low
4.DC-CDBA Digitally controlled CDBA	Current	Differential	single	voltage	Low	Low
5.CDTA Current differencing transconductance amplifier	Current	Differential	Double	Current	Low	High

6.CCCDTA Current controlled CDTA	Current	Differential	Double	Current	Low	High
7.DC-CDTA Digitally controlled CDTA	Current	Differential	Double	Current	Low	High
8.CTTA Current through transconductance amplifier	Current	Through	Double	Current	Low	High
9.CCTA Current conveyor transconductance amplifier	Current	Single	Double	Current	Low	High
10.CCCCTA Current controlled CCTA	Current	Single	Double	Current	Low	High
11.GCMI Generalized current mirror and inverter	Current	Single	Double	Current	Low	High
12. CDCC Current differencing current conveyor	Current	Differential	Double	Current	Low	High
13. CFTA Current follower transconductance amplifier	Current	Single	Double	Current	Low	High
14. CITA Current inverter transconductance amplifier	Current	Single	Double	Current	Low	High
15. CFCC Current follower current conveyor	Current	Single	Double	Current	Low	High

16. CICC Current inverter current conveyor	Current	Single	Double	Current	Low	High
17. CDDIBA Current differencing differential input buffered amplifier	Current	Differential	Single	Voltage	Low	Low
18. CDDITA Current differencing differential input transconductance amplifier	Current	Differential	Double	Current	Low	Low
19. CDDOBA Current differencing differential output buffered amplifier	Current	Differential	Double	Voltage	Low	High
20. CDDIDOBA Current differencing differential input differential output buffered amplifier	Current	Differential	Double	Voltage	Low	High

1.4 Outline of the dissertation:

In this dissertation, first chapter describes basic concept of current mode, voltage mode and mixed mode signal processing. The context in which the present work has been carried out is established in this chapter. In the second chapter, we have briefly discussed about current differencing differential input transconductance amplifier and its implementation in CMOS and verified all characteristics using PSPICE simulation. The third chapter introduces realization of a novel lossless grounded inductor and the performance of this inductor has been verified using PSPICE simulation. In the fourth chapter, we have proposed first order low pass filter, high pass filter and all pass filter and verified results with PSpice simulation. In the fifth chapter the summary of the work carried out in this dissertation has been presented along with scope for extension of the work carried out in this dissertation.

1.5 References:

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CHAPTER-2

Current differencing differential input transconductance amplifier

2.1 Introduction:

In the present chapter, we introduce a CMOS implementation of CDDITA. CDDITA was first introduced in [1]. It is a 6- terminals current mode active building block. It is current amplifier with an intermediate current to voltage conversion stage. Its port relationships are given below.

$$\begin{bmatrix} I_V \\ I_Z \\ I_X^+ \\ I_X^- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & g_m & -g_m \\ 0 & 0 & -g_m & g_m \end{bmatrix} \begin{bmatrix} I_P \\ I_N \\ V_Z \\ V_V \end{bmatrix}$$

The block diagram and its behavioral model are given in Fig 2.1.

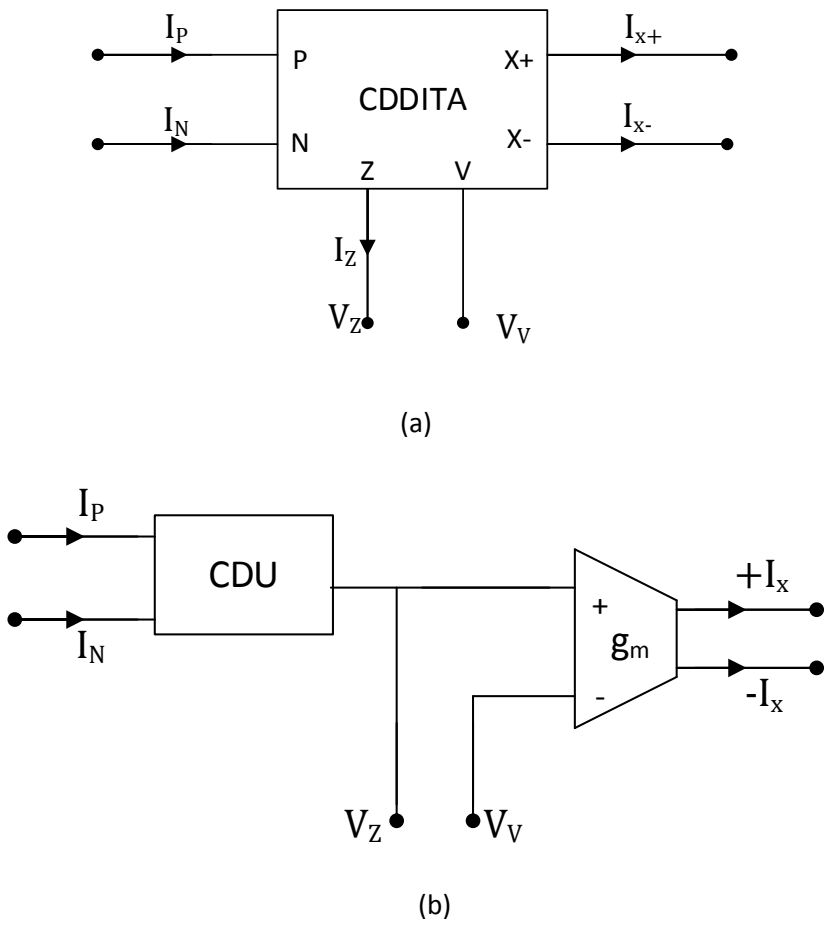

Figure 2.1. (a) Circuit symbol of CDDITA device (b) Behavioral model of circuit [3]

Dinesh Prasad, Kuldeep Panwar, D. R. Bhaskar and Mayank Srivastava proposed a BJT implementation of the CDDITA in [3] and its given below in figure 2.2.

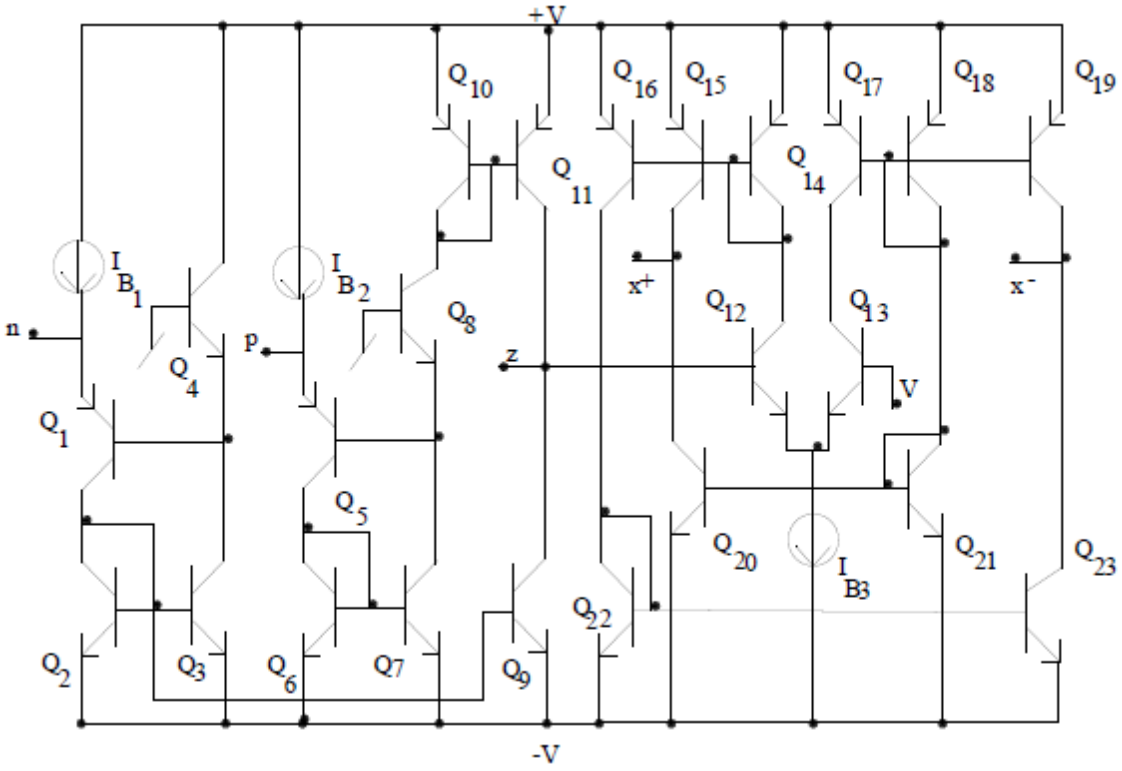

Figure 2.2. Bipolar implementation of CDDITA [3]

2.2 CMOS realization of CDDITA:

We have used the behavioral model of the CDDITA given above to purpose the CMOS realization of CDDITA given in figure 2.3. It is based on cascade connection of the CDU (current differencing unit) and OTA (operational transconductance amplifier). Transistors M1 to M12 construct the current differencing unit stage (CDU), through this stage we get difference of input currents at z terminal and adding an external impedance at z terminal and we can get the voltage V_Z at z terminal. The transistors M13 to M18 construct the multiple output OTA (operation transconductance amplifier). Let M13 and M14 are perfectly matched, all the current mirrors have unity gain and all the transistors are operated in saturation mode. V_{in} is small signal differential input (v_1-v_2), I_{x+} and I_{x-} are output currents, and I_B is bias current.

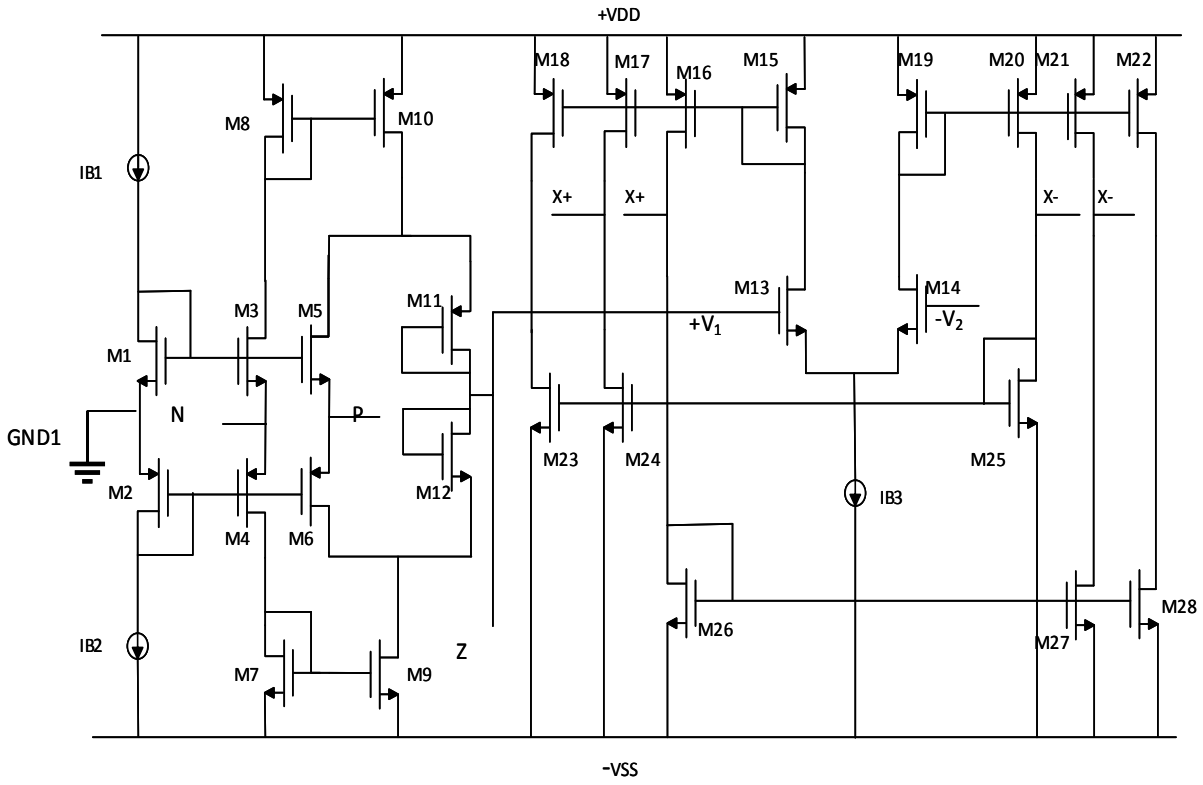

Figure 2.3. CMOS implementation of CDDITA

2.2.1 Simulation results:

The performance of CDDITA is verified using PSpice A/D simulator. The MOS transistors use 0.5µm CMOS process model parameters. The W/L ratio of all transistors are given in table 2.1. The supply voltage used for simulation of CDDITA is +/-1.5V and I_{B1}, I_{B2} and I_{B3} are respectively 100uA,100uA and 100uA.

The following analysis has been carried out:

(1) DC sweep (to check the linear range of the circuit)

(2) AC sweep (to check the bandwidth of the circuit)

Table 2.1. Aspect ratio of the CMOS Transistor [2]

Transistors	W/L (µm/µm)
M1-M6	8/1
M7-M10	5/1
M11-M12	20/1
M13-M14	16/1
M15-M22	6/1
M23-M28	4/1

The transfer characteristic of input current I_p or I_n vs output current I_z of CDDITA is shown in figure 2.4 and figure 2.5, we obtained this characteristic anyone input is open. The CDU stage transfers difference of two input currents to z terminals with a good accuracy, as we can see in figure 2.4 and Figure 2.5.

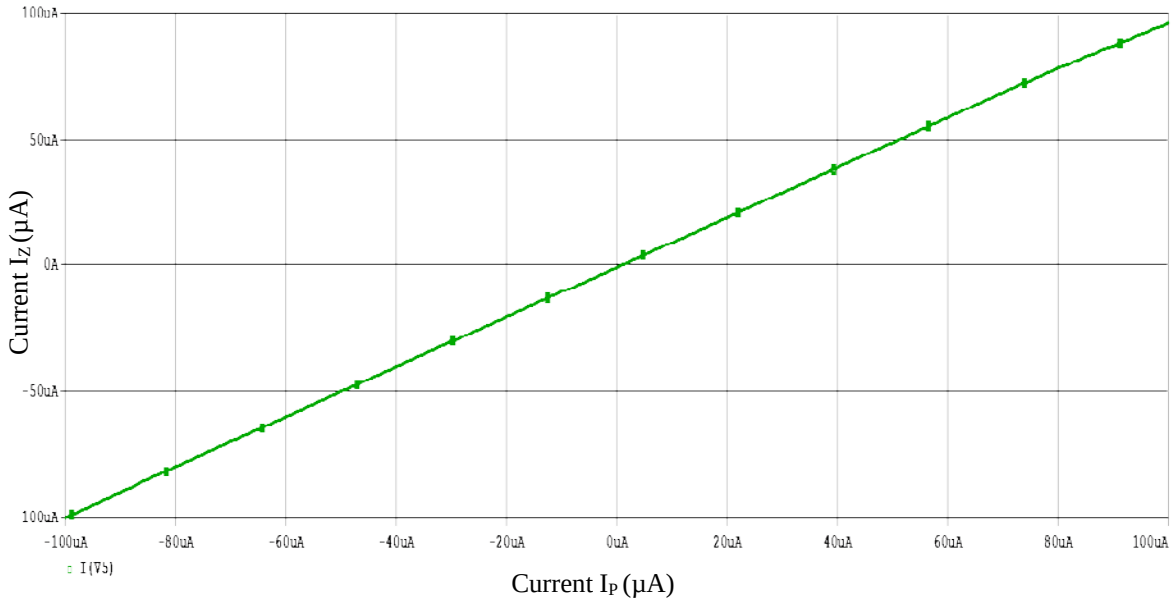

Figure 2.4. Frequency response of I_z /I_p

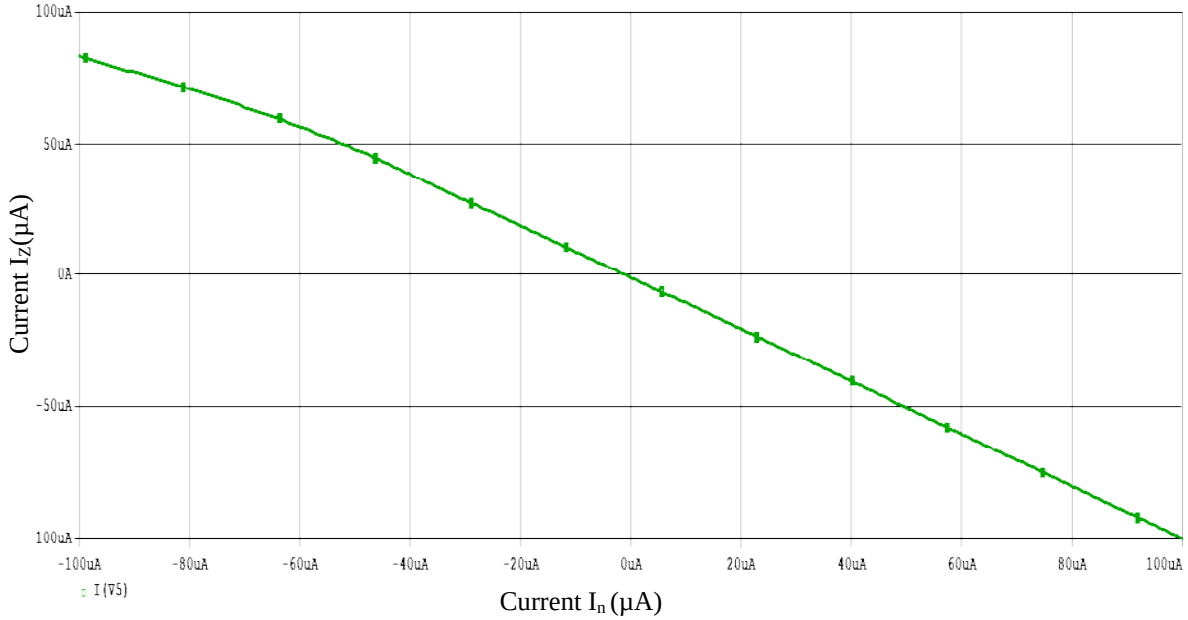

Figure 2.5. Transfer characteristic of I_z vs I_n

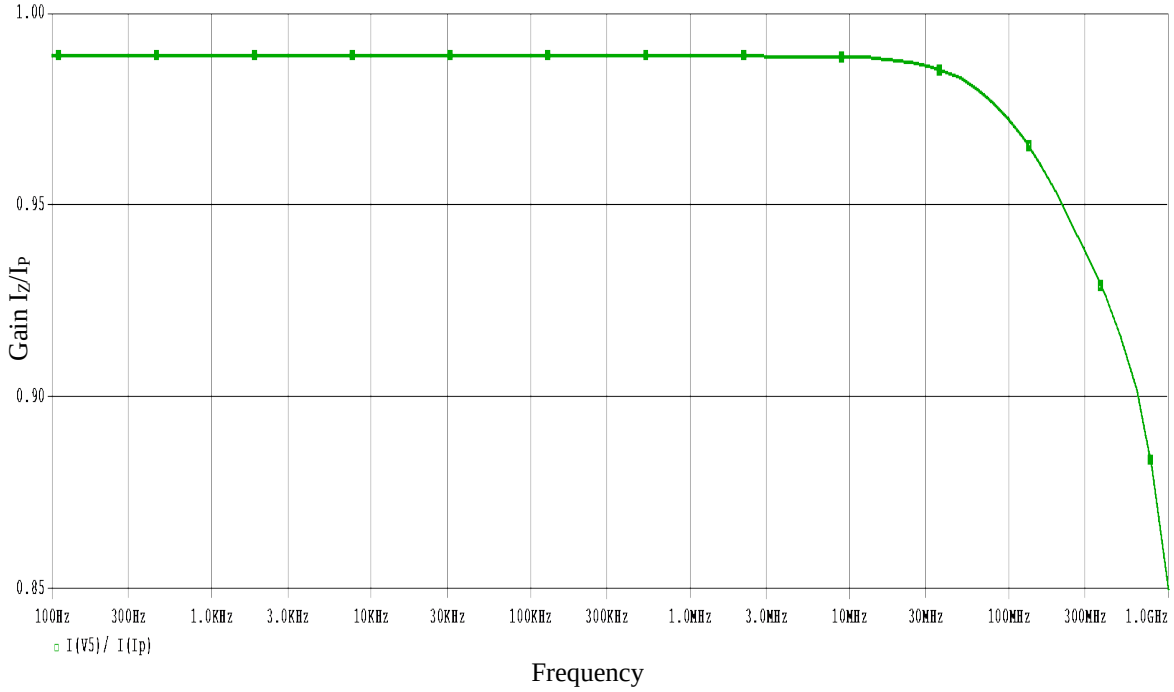

Figure 2.6. Transfer characteristic of I_z vs I_p

OTA (operational transconductance amplifier) is playing a main role in analog and mixed signal systems. It is mainly divided into two categories 1) single ended output OTA, 2) Fully differential OTA. In this dissertation, we considered a fully differential OTA [8]. The OTA structure, we used in the CDDITA active block is basically CMOS OTA and its input differential stage use an NMOS transistor to get a high transconductance gain g_m. We used

0.5µm model parameter to implement CMOS based multiple output OTA []. The W/L ratio of all transistors are given in Appendix 1.

In the Figure 2.7, we can see that the DC characteristic of OTA. We can also observe our linear range of differential input of OTA.

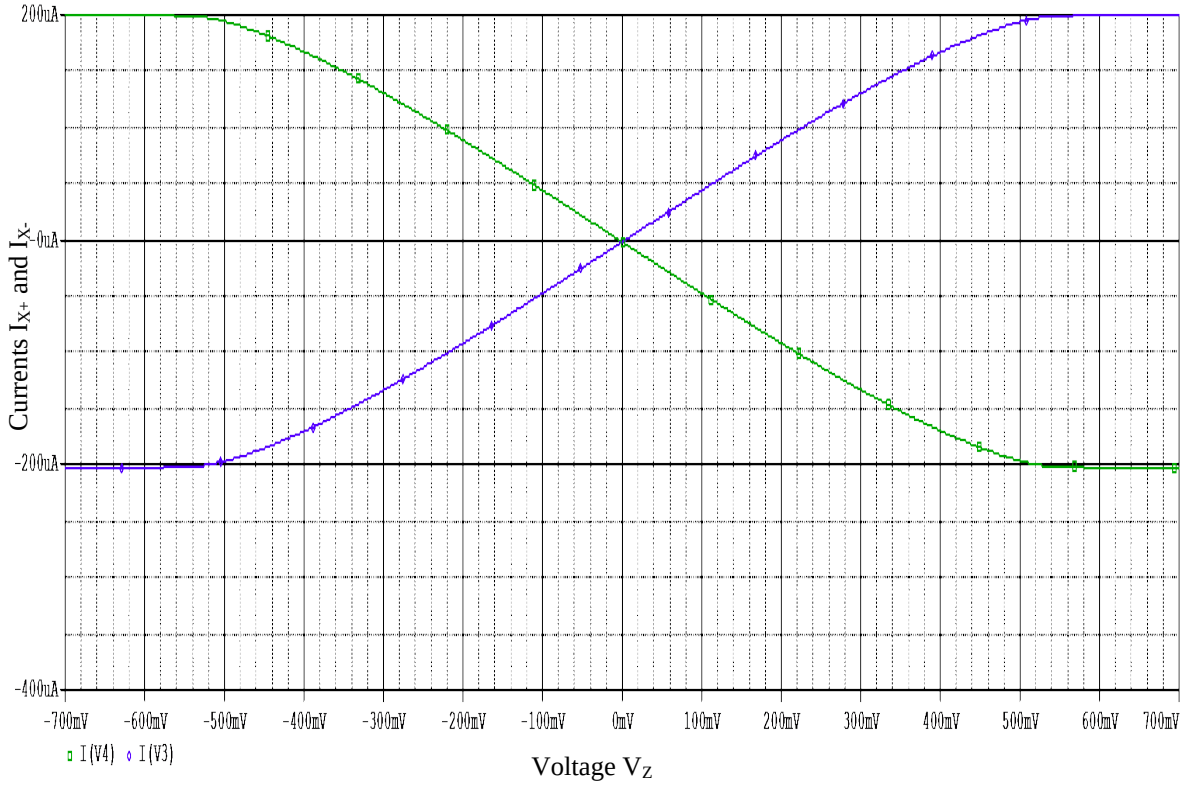

Figure 2.7 DC transfer characteristic of OTA

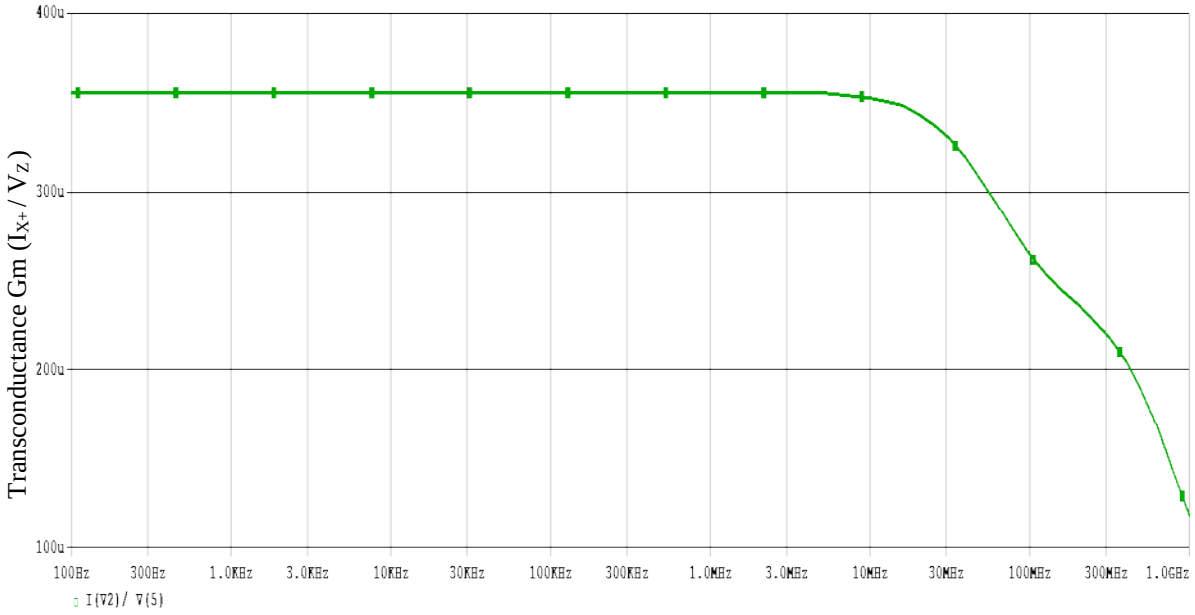

Figure 2.8 AC transfer characteristic(Transconductance) of OTA

Table 2.2 Characteristic parameter of CDDITA

Characteristic Parameters	Simulated value
Input current linear range I_p	-100µA to 100µA
Input current linear range I_n	-100µA to 100µA
Bandwidth I_z/I_p	1.64 GHz
Bandwidth I_{x+}/V_z	133MHz
Differential input voltage linear range (V_z-V_v)	-500mV to 500mV
Transconductance g_m	348 µI/V at 100µA biasing

2.3 Conclusion:

In the beginning of this chapter, we have discussed CDDIT A device in detail. The AC and DC characteristic of CDDITA have been discussed and verified with PSpice simulation.

2.4 References:

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CHAPTER-3

Grounded inductor realization using CDDITA and its application

3.1 Introduction:

In the previous chapter we have presented a CMOS implementation of the CDDITA along with its complete characterization. In this chapter, we present a novel realization of lossless grounded inductor using CDDITA. PSPICE simulations have confirmed the workability of the simulated inductor.

Simulated inductors are used in low to medium frequency integrated circuit applications such as signal amplification, filtering and wave form generation. Passive inductors are quite bulky and the quality factor of the integrated circuit passive inductor is very poor. This had led to the development of a very large body of literature on the topic of simulated inductors using various types of active building blocks. To describe in detail, the different grounded inductance simulation circuits is beyond the scope of the dissertation. However to put our work in proper perspective we present below some of the important inductance simulation circuits using recently proposed active building blocks, namely operational transresistance amplifier (OTRA), current differencing transconductance amplifier (CDTA), current controlled current differencing transconductance amplifier (CCCDTA), current conveyor third generation (CCIII), current controlled current follower transconductance amplifier (CCCFTA), current differencing current conveyor (CDCC).

3.1.1 Inductor simulator using OTRA:

A OTRA [1] is current controlled voltage source and is characterized by the following port relations.

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & R_m \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_0 \end{bmatrix}$$

A lossless grounded inductor realized with OTRA is shown below in figure 3.1, which was purposed in [2].

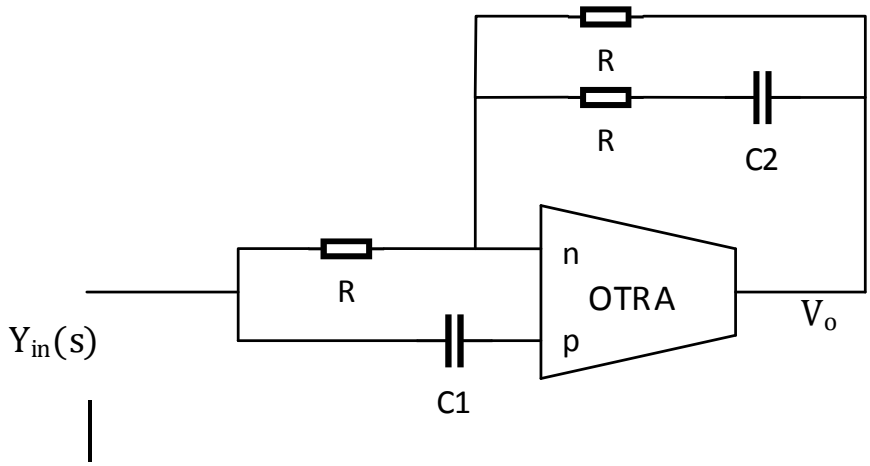


Figure 3.1 Lossless Grounded inductor [2]

From fig 3.1, equation of input admittance is given as [2]

$$Y_{in}(s) = \left(3G - \frac{C_1 G}{C_2}\right) + \frac{G^2}{sC_2} \text{ , where } G = 1/R \tag{3.1}$$

If following condition is met $C_1 = 2C_2$

$$Y_{in}(s) = \frac{G^2}{sC_2} \tag{3.2}$$

The inductance value is given as

$$L_{eq} = \frac{C_2}{G^2} = C_2 R^2 \tag{3.3}$$

The impedance magnitude response of grounded inductor is shown is figure 3.2,

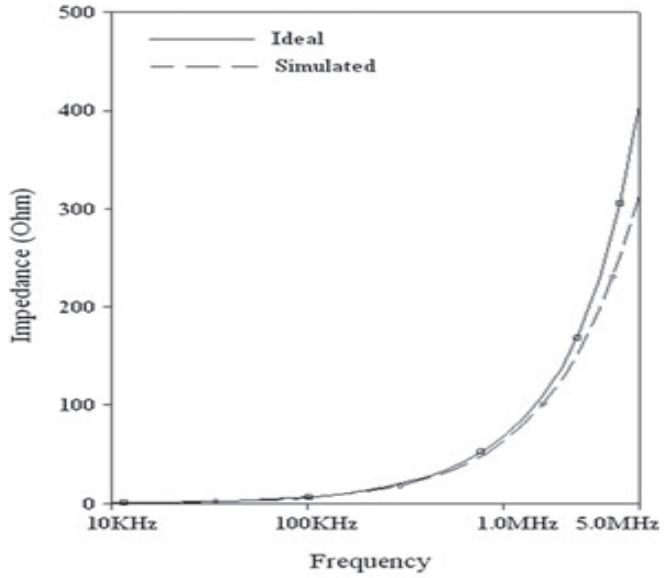


Figure 3.2 Impedance magnitude response Grounded inductor [2]

3.1.2 Inductor simulator using CDTA:

A CDTA [3] is current differencing transconductance amplifier and is characterized by the following port relations.

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 \\ g_m & 0 & 0 & 0 & 0 \\ g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_p \\ I_n \end{bmatrix}$$

A lossless grounded inductor realized with CDTA is shown below in figure 3.3, which was purposed in [4].

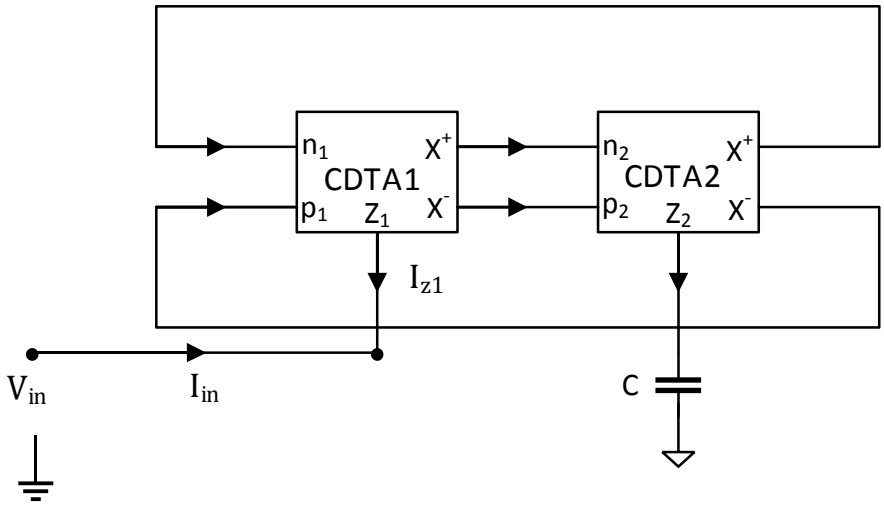


Figure 3.3 Grounded inductor simulation configuration [4]

The equation is given as [4]

$$Z_{in}(s) = \frac{V_{In(s)}}{I_{in}(s)} = s\left(\frac{C}{4g_{m1}g_{m1}}\right) \tag{3.4}$$

The inductance value is given as

$$L_{eq} = \frac{C}{4g_{m1}g_{m2}} \tag{3.5}$$

Where g_{m1} and g_{m2} are transconductance of CDTA1 and CDTA2 respectively.

The frequency response of grounded inductance simulator is shown in figure 3.4.

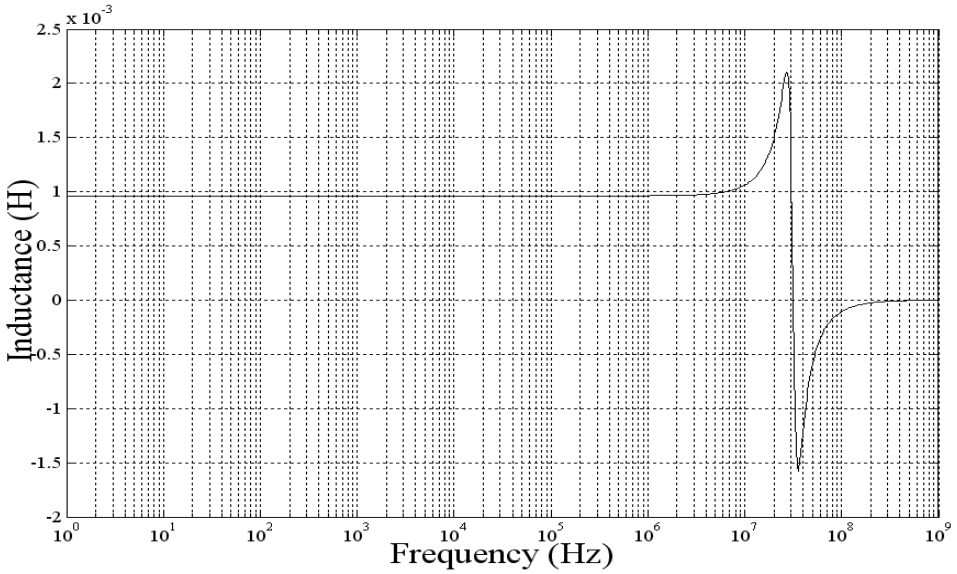


Figure 3.4 Frequency response of simulated Grounded inductor [4]

3.1.3 Inductor simulator using CCCDTA:

A CCCDTA [5] is current controlled current differencing transconductance amplifier. It is quite similar to CDTA block. In CDTA, we considered input voltages zero and input resistances R_P and R_N are infinity but in case of CCCDTA we do not consider input voltages zero and has finite input resistances [5]. It is characterized by the following port relations.

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix}$$

A grounded inductor realized with CCCDTA is shown below in figure 3.5, which was purposed in [5]

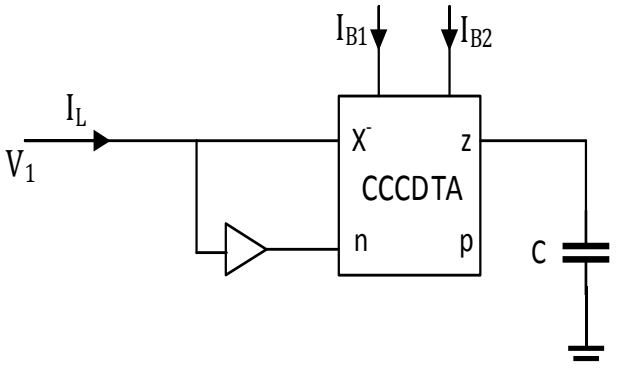


Figure 3.5 Grounded inductor simulation configuration [5]

Input impedance is given as

$$Z_{in} = \frac{V_1}{I_L} = \frac{sCR_n}{g_m} \tag{3.6}$$

Grounded inductance is given as

$$L_{eq} = \frac{CR_n}{g_m} \tag{3.7}$$

Impedance value with respect to frequency is shown in figure 3.6

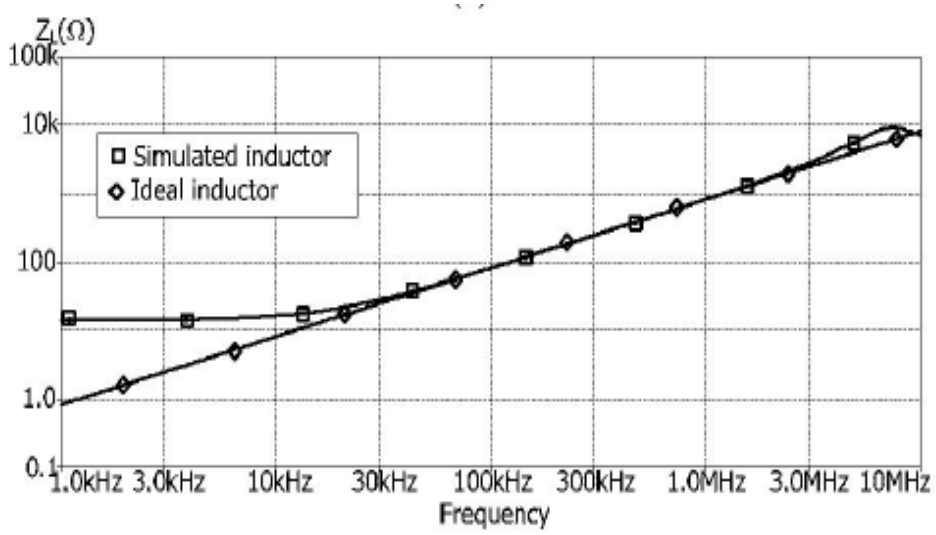


Figure 3.6 Impedance magnitude response [5]

3.1.4 Inductor simulator using CCIII:

Recently, a new current conveyor called the third-generation current conveyor (CCIII) was introduced in [6]. It is characterized by the following port relations.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

A number of grounded lossy inductor realized with CCIII are shown below in figure 3.7, which were purposed in [6].

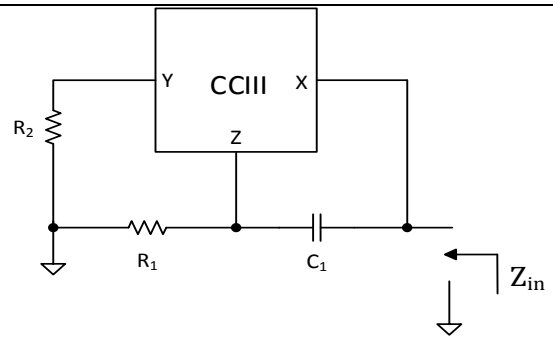
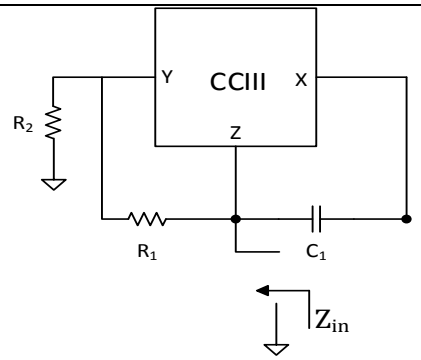
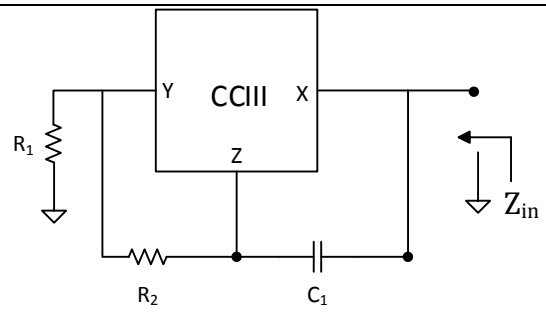
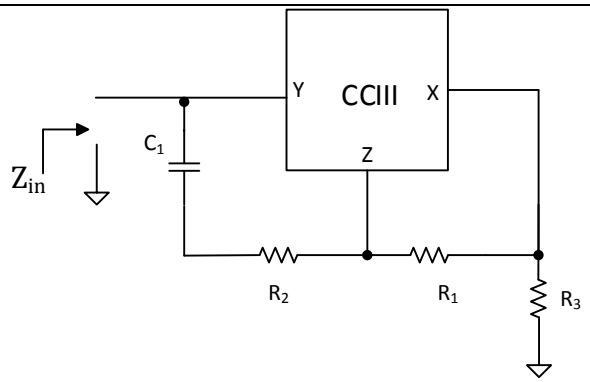
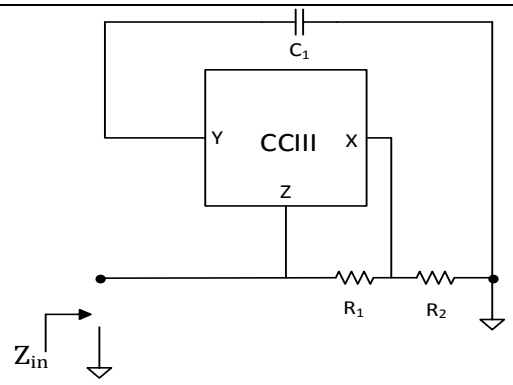
	(3.7 a) $Z_{in} = sC_1R_1R_2 + 2R_2$ $L_{eq} = C_1R_1R_2 \; and \; R_{eq} = R_2$ L with series R
	(3.7 b) $Z_{in} = sC_1R_1R_2 + R_1 + R_1$ $L_{eq} = C_1R_1R_2 \; and \; R_{eq} = R_1 + R_2$ L with series
	(3.7 c) $Z_{in} = sC_1R_1R_2 + 2R_1$ $L_{eq} = C_1R_1R_2 \; and \; R_{eq} = 2R_1$ L with series R
	(3.7 d) $Z_{in} = sC_1R_1R_3/(sC_1(2R_1 + R_2) + 1)$ $L_{eq} = C_1R_1R_3 \; and \; R_{eq} = \frac{R_1R_3}{2R_1 + R_2}$ L with parallel R
	(3.7 b) $Z_{in} = sC_1R_1R_2 + R_1 + R_2$ $L_{eq} = C_1R_1R_2 \; and \; R_{eq} = R_1 + R_2$ L with series

Figure 3.7 lossy grounded inductor topologies [6]

3.1.5. Inductor simulator using CCCFTA:

A CCCFTA [8] is current controlled current follower transconductance amplifier. It is purely current mode active device because its inputs and outputs signals are current. It is obtained from first generation CFTA (current follower transconductance amplifier). It is characterized by the following port relations.

$$\begin{bmatrix} V_f \\ I_{z,zc} \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_f \\ V_x \\ V_z \end{bmatrix}$$

A grounded inductor realized with CCCFTA is shown below in figure 3.8, which was purposed in [8].

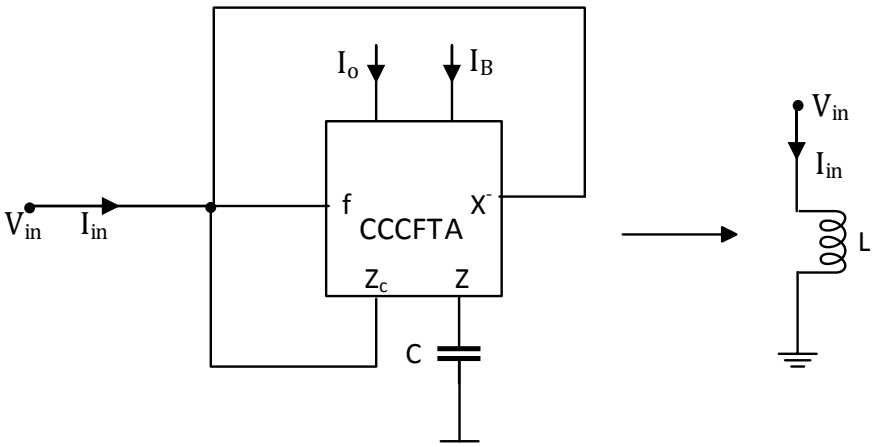


Figure 3.8 Grounded inductor topology [8]

The impedance value of above circuit is given as

$$V_{in} = \frac{V_{in}}{I_{in}} = \frac{sCR_f}{g_m} \tag{3.8}$$

The grounded inductor value is given as

$$L_{eq} = \frac{CR_f}{g_m} \tag{3.9}$$

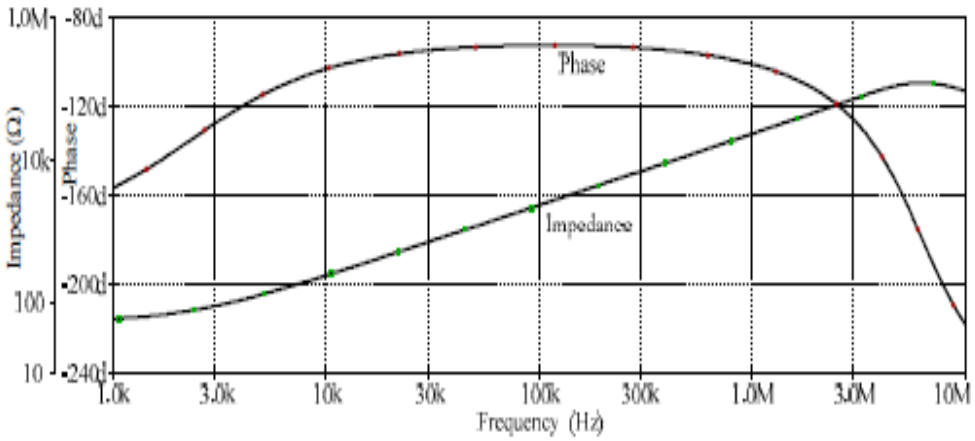


Figure 3.9 Impedance magnitude response [8]

3.1.6 Inductor simulator using CDCC:

A CDCC is current differencing current conveyor block. It is alternative form of VDCC (voltage differencing current conveyor) [9]. It is characterized by the following port relations.

$$\begin{bmatrix} V_N \\ V_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} I_P \\ I_N \\ V_Z \\ I_X \end{bmatrix}$$

Inductor realized with CDCC is shown below in figure 3.10, which was purposed in [10].

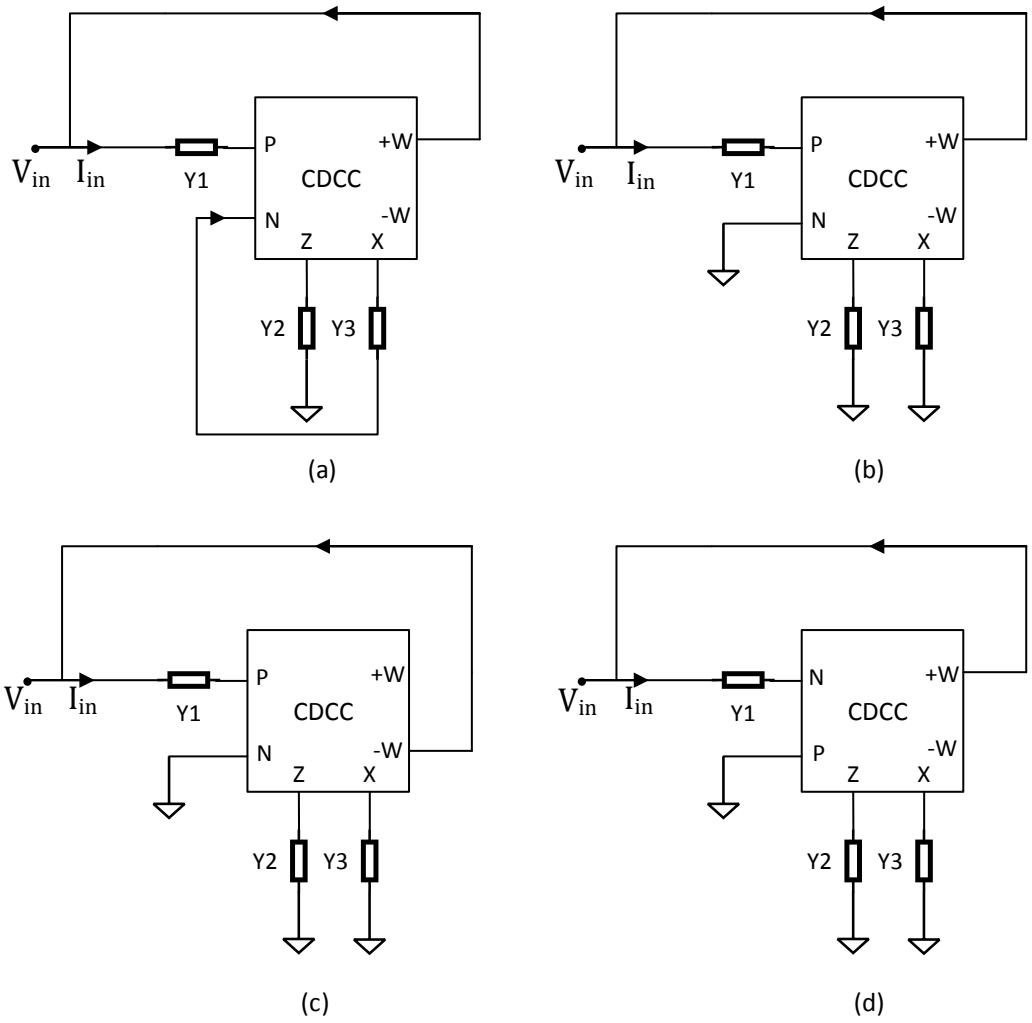


Figure 3.10 lossy grounded inductor topologies [10]

Table 3.1 All inductance forms [10]

Circuit	**L_{eq}**	**G_{eq}**	**Type**
Fig 3.10 a	$L_{eq} = \frac{sC}{G_1 G_2}$	$G_{eq} = G_1$	+L parallel with +R
Fig 3.10 b	$L_{eq} = \frac{sC}{G_1 G_2}$	$G_{eq} = G_1$	+L parallel with +R
Fig 3.10 c	$L_{eq} = -\frac{sC}{G_1 G_2}$	$G_{eq} = G_1$	-L parallel with +R
Fig 3.10 d	$L_{eq} = -\frac{sC}{G_1 G_2}$	$G_{eq} = G_1$	-L parallel with +R

3.2 The proposed lossless grounded inductor using CDDITA:

A lossless grounded inductor realization circuit using CDDITA is shown in figure 3.11. The circuit is designed with two CDDITA block, a grounded capacitor and two grounded resistors. CDDITA port relationships are given below.

$$\begin{bmatrix} I_V \\ I_Z \\ I_X^+ \\ I_X^- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & g_m & -g_m \\ 0 & 0 & -g_m & g_m \end{bmatrix} \begin{bmatrix} I_P \\ I_N \\ V_Z \\ V_V \end{bmatrix}$$

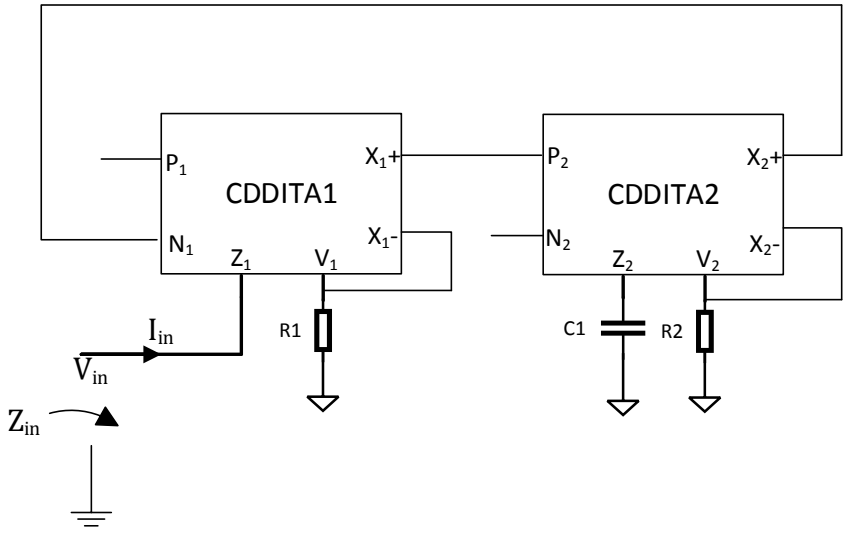


Figure 3.11 The proposed circuit of grounded inductance

The simulated grounded inductor circuit impedance is expressed as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC(1+g_{m1}R_1)(1+g_{m2}R_2)}{g_{m1}g_{m2}} \tag{3.10}$$

or $$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{4sC}{g_{m1}g_{m2}} \tag{3.11}$$

$$if \quad g_{m1} = g_{m2} = \frac{1}{R_1} = \frac{1}{R_2}$$

Grounded inductance value can be expressed as

$$L_{eq} = \frac{C(1+g_{m1}R_1)(1+g_{m2}R_2)}{g_{m1}g_{m2}} \tag{3.11}$$

or $$L_{eq} = \frac{4C}{g_{m1}g_{m2}} \tag{3.12}$$

Where, g_{m1} and g_{m2} are transconductance of CDTA1 and CDTA2 respectively.

3.2.1 Simulation results of lossless grounded inductor:

To simulate the proposed circuit in figure 4.11, we used PSpice simulation and the following passive components value: C_1=100pF and $R_1=1/g_{m1}=1/g_{m2}$=2.87kΩ. After putting passive components values in equation (3.12), we get theoretically inductor value L_{eq} = 3.30 mH. The response of grounded inductance simulator is shown in figure 3.12. It can be observed that simulated value of inductance is constant up to 3 MHz and is approximately equal to theoretical value of inductance.

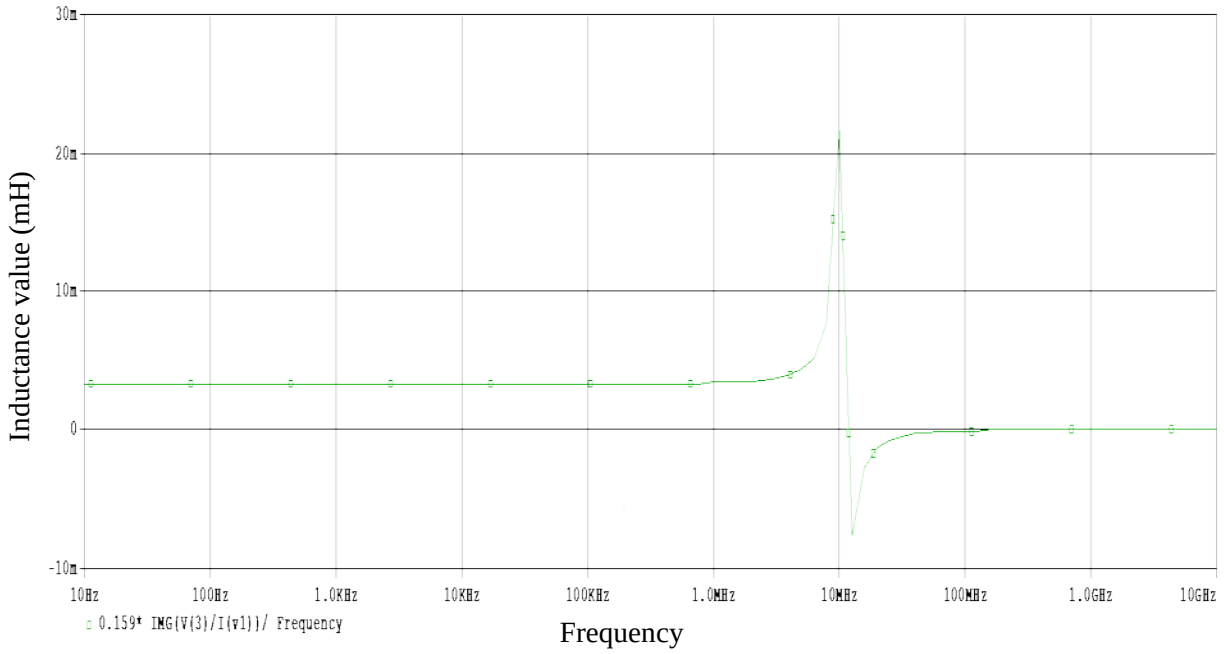


Figure 3.12 The response of grounded inductance simulator

3.3 Parallel resonant circuit:

To verify the workability of the proposed inductor we have used simulate it in a parallel resonant circuit that is shown in figure 3.13

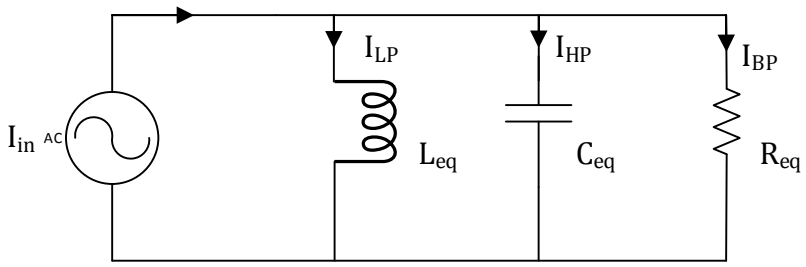


Figure 4.13 The parallel resonant circuit

The different current transfer functions obtained from the circuit are gives as

$$\frac{I_{LP}}{I_{in}} = \frac{{}^{1}/_{L_{eq}C_{eq}}}{s^2+\frac{s}{C_{eq}R_{eq}}+\frac{1}{L_{eq}C_{eq}}} \tag{3.13}$$

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2+\frac{s}{C_{eq}R_{eq}}+\frac{1}{L_{eq}C_{eq}}} \tag{3.14}$$

$$\frac{I_{BP}}{I_{in}} = \frac{{}^{s}/_{C_{eq}R_{eq}}}{s^2+\frac{s}{C_{eq}R_{eq}}+\frac{1}{L_{eq}C_{eq}}} \tag{3.15}$$

Where $w_o = \frac{1}{L_{eq}C_{eq}}$, $\frac{w_o}{Q} = \frac{1}{C_{eq}R_{eq}}$ and $Q = R_{eq}\sqrt{\frac{C_{eq}}{L_{eq}}}$

3.3.1 Simulation results of parallel resonant circuit:

The parallel RLC circuit was simulated with the following components values are C_{eq}=1nF, L_{eq} =3.30mH is obtained from equation (3.12) using R_1 =R_2 =2.87KΩ and C_1=100pF and R_{eq}=1.3kΩ and cut-off frequency is 87.5 kHz. The simulation results have been carried out with PSpice simulation.

The current characteristic of parallel resonant circuit is shown in figure 3.14. The transient analysis for low pass filter, high pass filter and band pass filter are also shown in figure 3.15, 3.16 and 3.17 respectively.

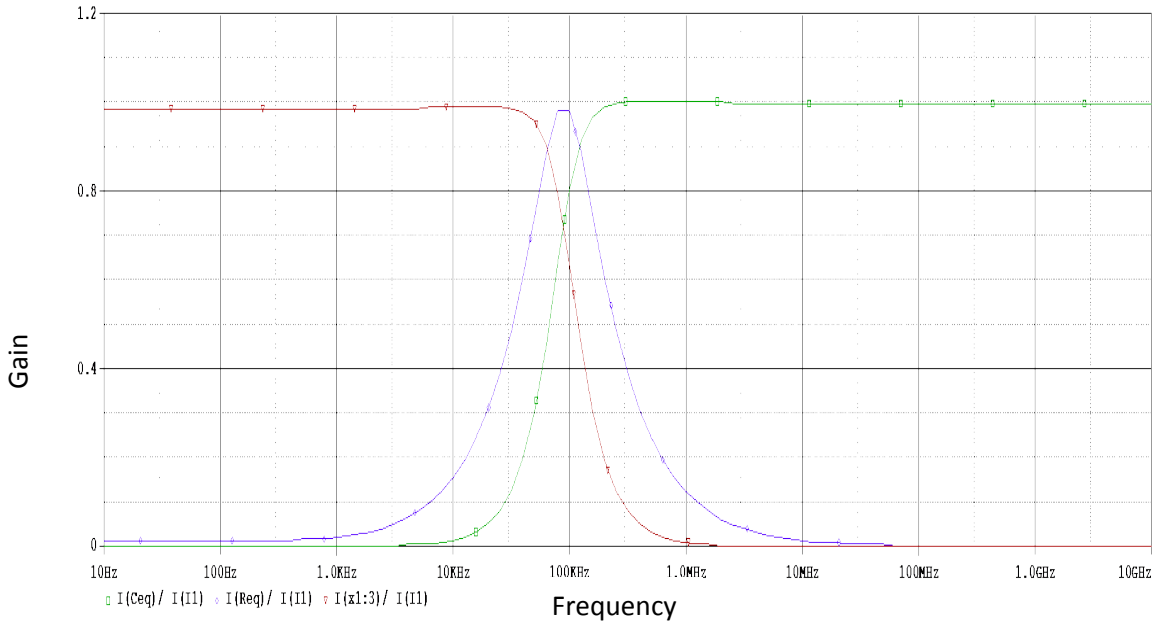


Figure 3.14 The frequency response of parallel resonant circuit

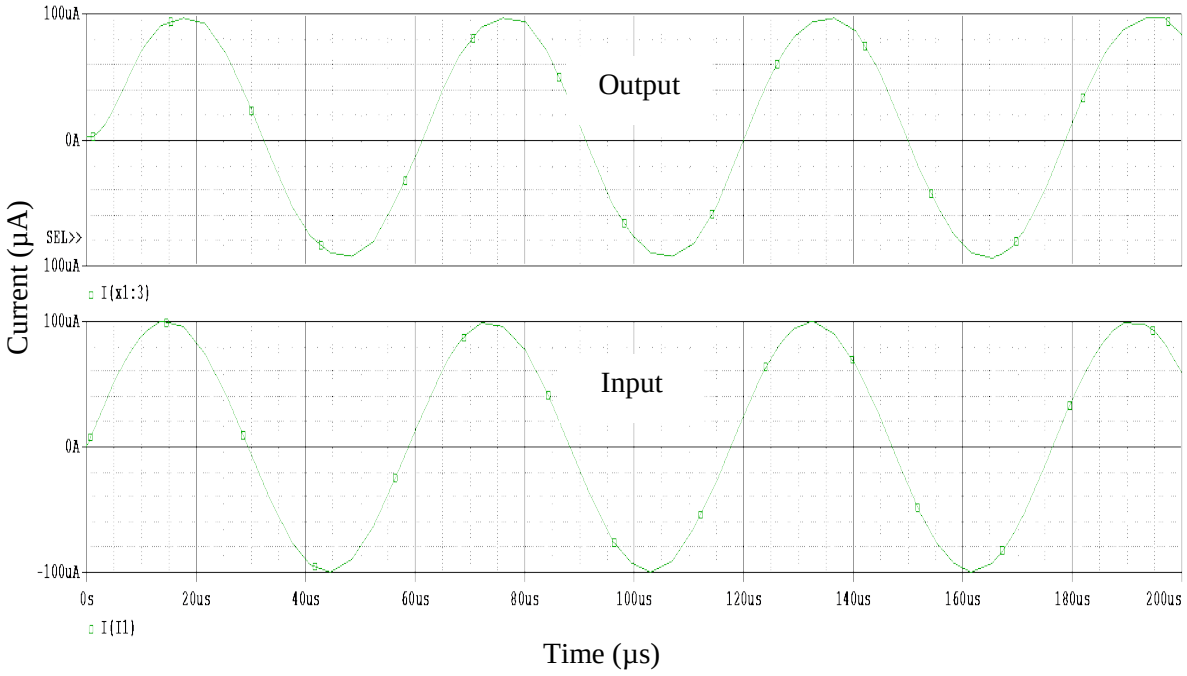


Figure 3.15 The transient response of low pass filter

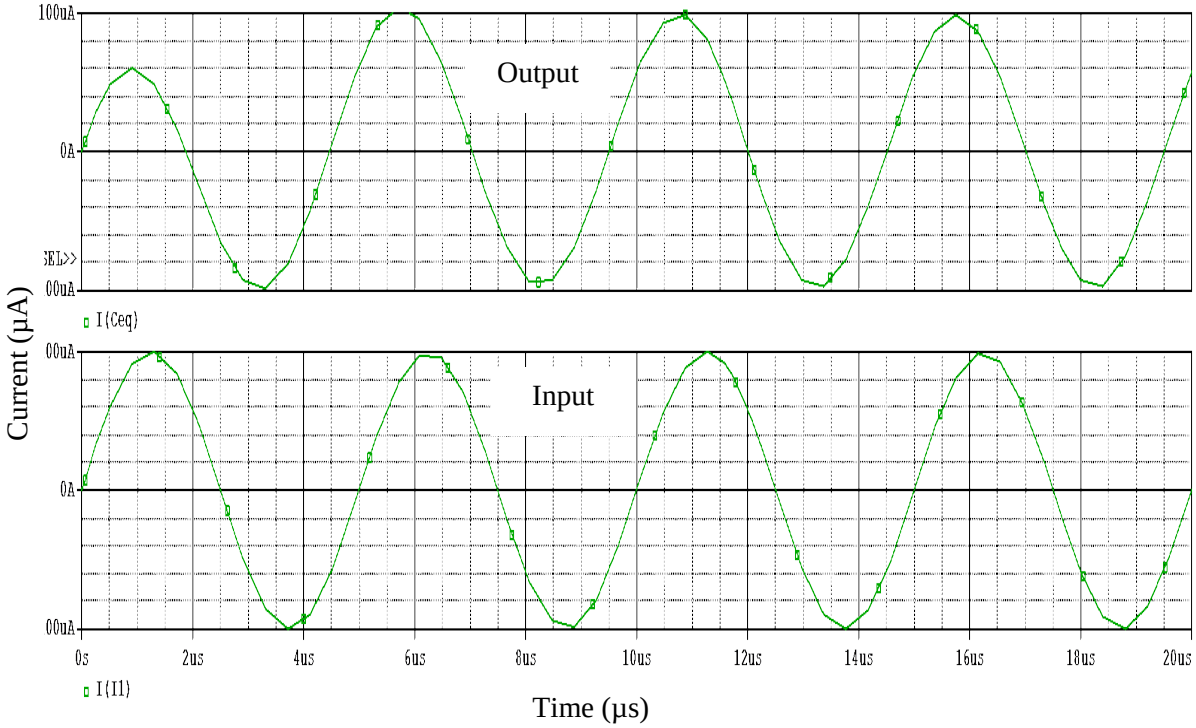


Figure 3.16 The transient response of High pass filter

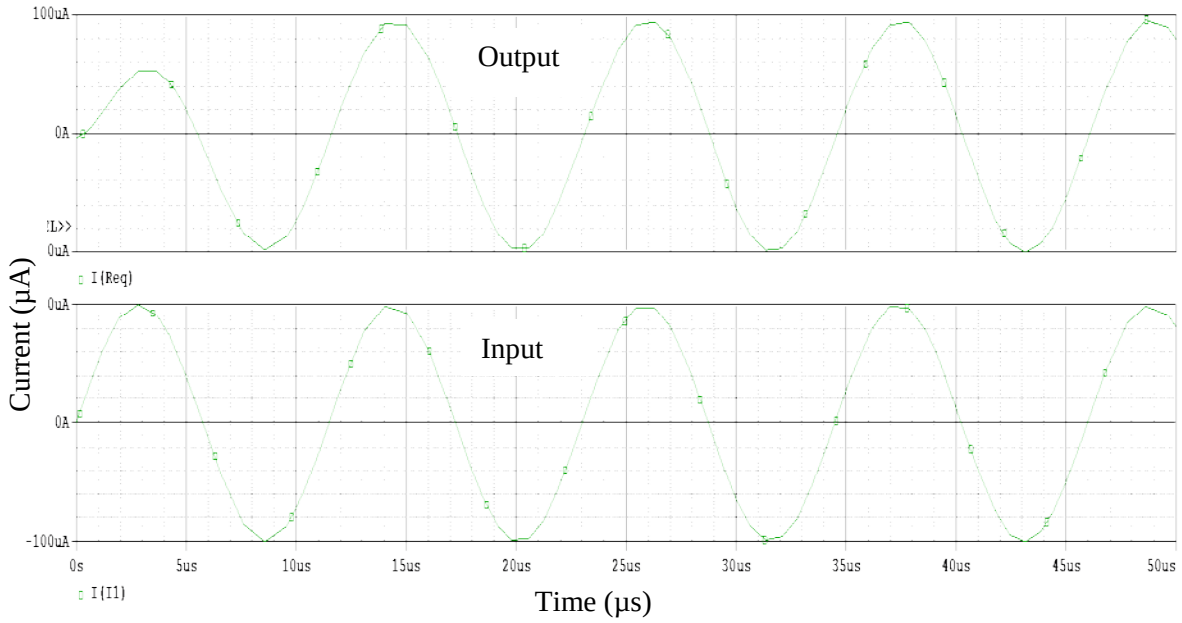


Figure 3.17 The transient response of band pass

3.4 Conclusion:

In this chapter, we have discussed some existing research papers on inductance simulator using various existing active blocks such as OTRA, CDTA, CCCDTA, CCIII, CCCFTA and CDCC etc. And we have implemented inductance simulator using CDDITAs active block. To check the performance of the implemented inductance simulator, we simulated parallel RLC circuit and obtained some results that are shown above. Then we verified all our results which are obtained using PSpice simulation with theoretical values.

3.5 References:

[1] Salama, K.N. and Soliman, A.M., 1999. CMOS operational transresistance amplifier for analog signal processing. *Microelectronics Journal*, *30*(3), pp.235-245.

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[12] Kilinc, S., Salama, K.N. and Cam, U., 2006. Realization of fully controllable negative inductance with single operational transresistance amplifier. *Circuits, systems, and signal processing*, *25*(1), pp.47-57.

CHAPTER-4

Implementation of 1st order filter structures using CDDITA

4.1 Introduction:

In the previous chapter we had presented a novel lossless grounded inductor employing two CDDITA and all grounded passive elements. In this chapter, we present a brief review of (Ist order filter structures using similar building blocks. We also present novel filter structures first order low pass, first order high pass and first order all pass filter) employing CDDITA.

The major drawback of passive filters is the loss of signal during signal transmission and the loading of the filter output by the load. This results in the modification of the filters characteristics. RC active filters do not suffer from any of these limitations. First order RC active filters are an integral part of many signal processing application as they can be used in cascade with biquadratic sections to realize higher order filters [19]. First order RC active filters have been realized with different active building blocks viz, operational amplifier (op-amp), operational transconductance amplifier (OTA), current conveyors, operational transresistance amplifier(OTRA), current feedback amplifier(CFA) and a host of other active building blocks proposed recently [1]. It is worthwhile to present a brief review of some of the Ist order RC active filters realized with active building blocks of recent origin, to place our work in proper perspective.

4.1.1 First order all pass filter using CDTA:

We now present various all pass filter configurations using CDTA (current differencing transconductance amplifier) active block. The characteristics equation of CDTA is given as,

$$\begin{bmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 \\ g_m & 0 & 0 & 0 & 0 \\ g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_p \\ I_n \end{bmatrix}$$

The first configuration is shown in figure 4.1, which is CDTA based current mode all pass filter [2].

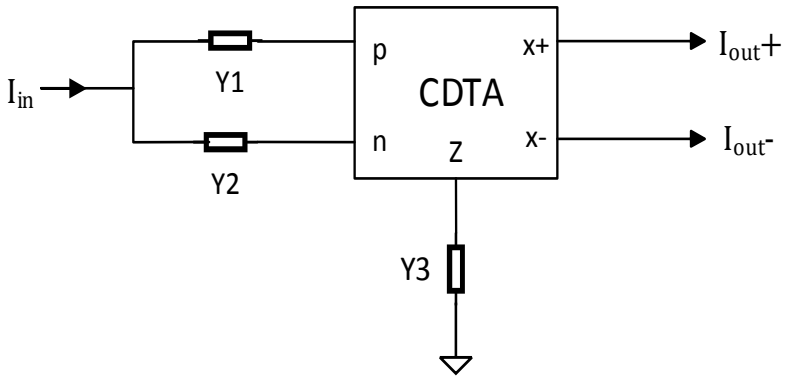

Figure 4.1 circuit of all pass filter [2]

The transfer function of above circuit is given as [2]

$$\frac{I_{out-}}{I_{in}} = \left({g_m}/{Y_3}\right)\frac{Y_2-Y_1}{Y_1+Y_2} \tag{4.1}$$

If choosing Y_2=G, Y_1=sC and G=1/R

$$\frac{I_{out-}}{I_{in}} = \frac{1-sCR}{1+sCR} \tag{4.2}$$

The magnitude and phase response of figure 4.2,

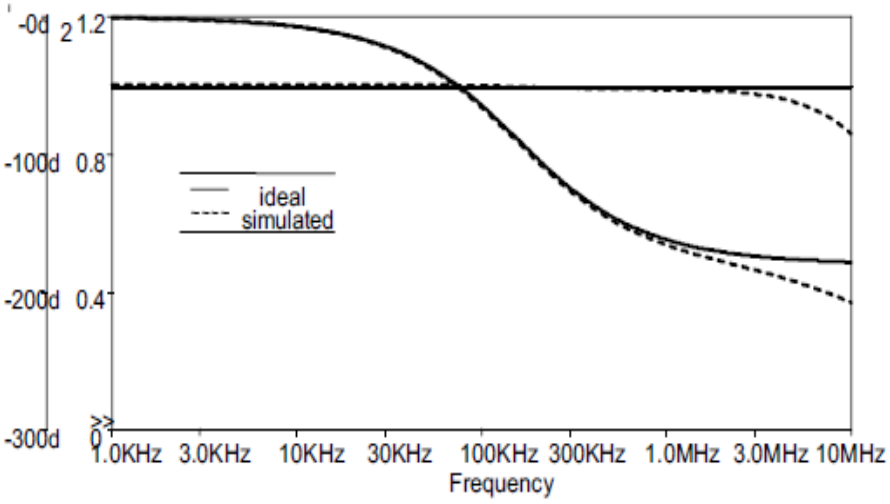

Figure 4.2 The magnitude and phase response of all pass filter [2]

The next configuration of all pass filter is shown in figure 4.3 [3]. It is a resistor less current mode all-pass filters [3]. The shown configuration uses two CDTAs and one virtually grounded capacitor.

The current transfer function of given configuration is,

$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{\left(1 - s\frac{C_1}{g_{m1}}\right)}{\left(1 + s\frac{C_1}{g_{m1}}\right)} \quad (4.3)$$

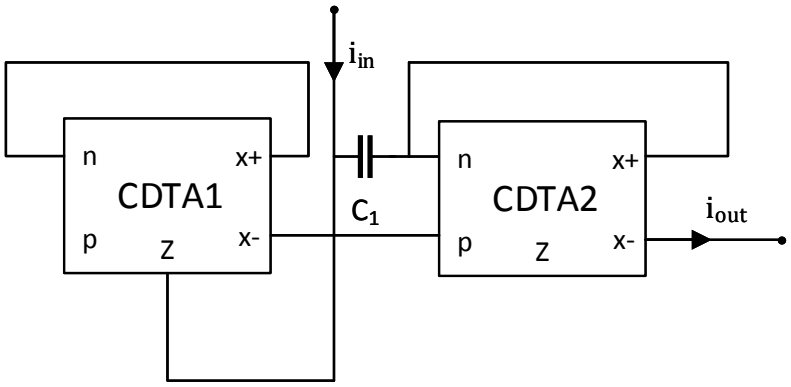

Figure 4.3 circuit of all pass filter [3]

The phase and magnitude response of above circuit is shown in figure 4.4,

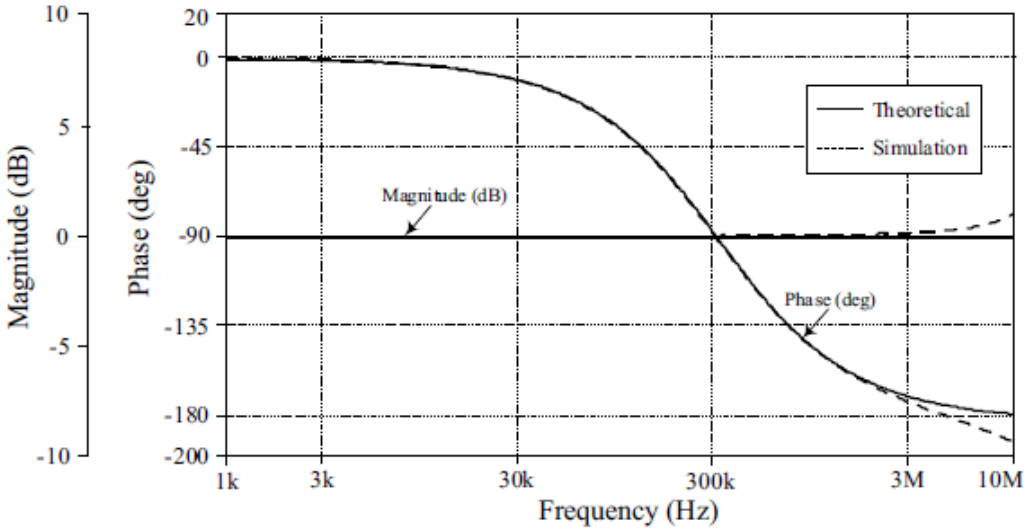

Figure 4.4 The magnitude and phase response [3]

The next configuration is again showing a current mode all pass filter using CDTA active block with different topology [4]. In this topology, we can see that there is single CDTA active block and one single grounded capacitor is used to make current mode all pass filter configuration which is shown in figure 4.5,

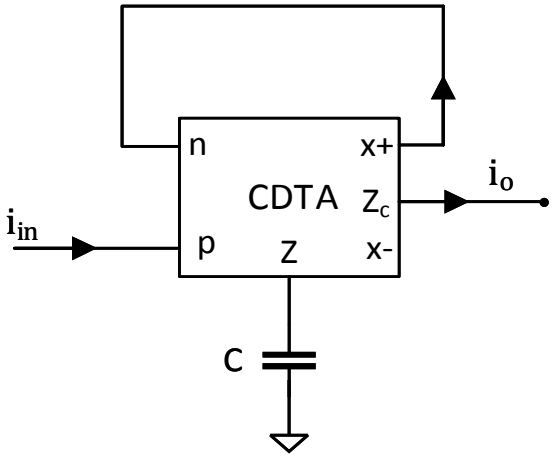

Figure 4.5 circuit of all pass filter [4]

The current transfer function for all pass filter is given as

$$\frac{I_{out}}{I_{in}} = \frac{sC-g_m}{sC+g_m} \tag{4.4}$$

The magnitude and phase response are shown in figure 4.6

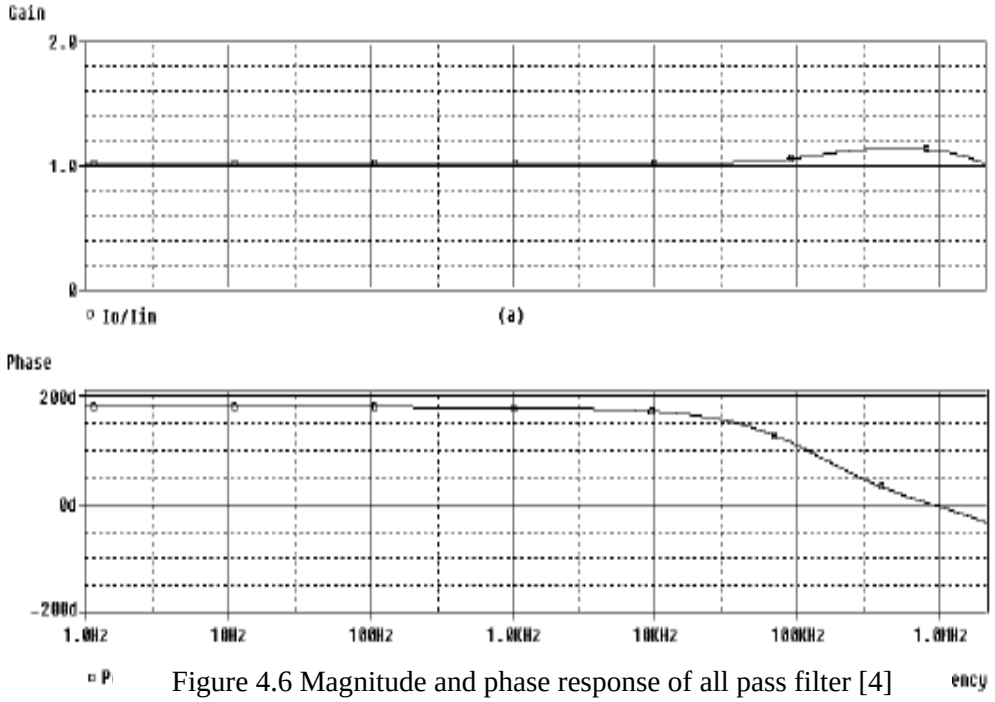

Figure 4.6 Magnitude and phase response of all pass filter [4]

4.1.2 First order All pass filter using CCCDTA:

A CCCDTA is current controlled current differencing transconductance amplifier active block. The characteristics equation of CCCDTA is given as,

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix}$$

The configuration of all pass filter is shown in figure 4.7 which is proposed in [5] with one grounded capacitor and one grounded resistor.

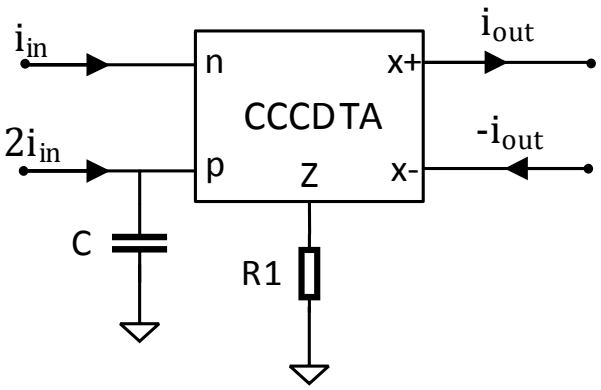

Figure 4.7 Configuration of all pass filter [5]

Current transfer function of above configuration is given as,

$$\frac{I_{o1}}{I_{in}} = -\frac{I_{o2}}{I_{in}} = R_1 g_m \left(\frac{1-sCR_p}{1+sCR_p}\right) \quad (4.5)$$

The magnitude and phase response of configuration [5] is shown in figure 4.8,

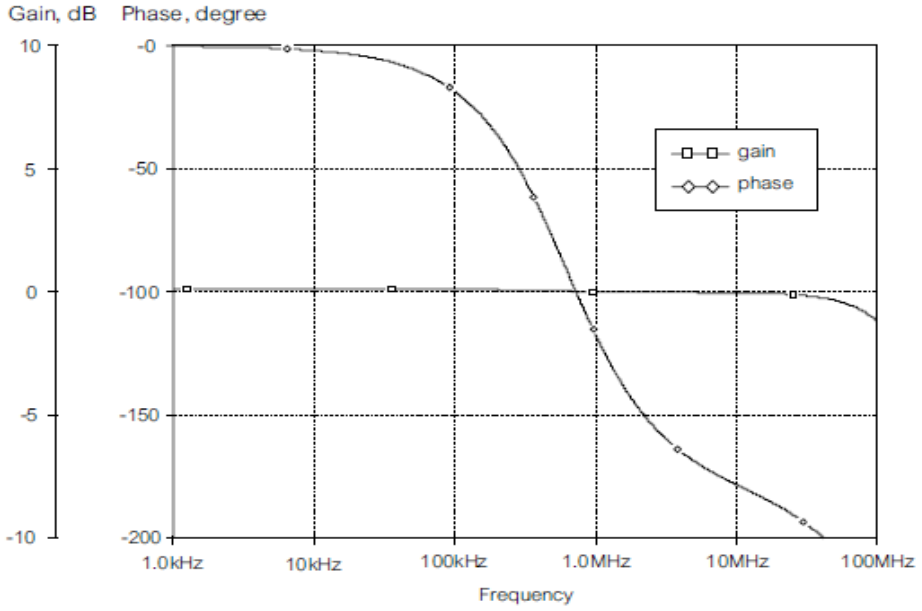

Figure 4.8 Magnitude and phase response of all pass filter [5]

4.1.3 First order All pass filter using CFTAs:

CFTA is current follower transconductance amplifier active block. It is three terminal active block. It has one low impedance input port [6]. The characteristics equation of CFTA is given as,

$$\begin{bmatrix} V_f \\ i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & g_m & 0 & 0 \\ 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ V_z \\ V_{x+} \\ V_{x-} \end{bmatrix}$$

In this paper [6], the current gain and phase shift can be electronically controlled: the circuit employs 2 CFTAs, 1 resistor and 1 grounded capacitor, which is suitable for fabricating in monolithic chip [6]. It has high output impedances and low input impedances, so we can easily cascade it with another circuit. The configuration of current mode all pass filter is shown in figure 4.9, which is proposed in [6].

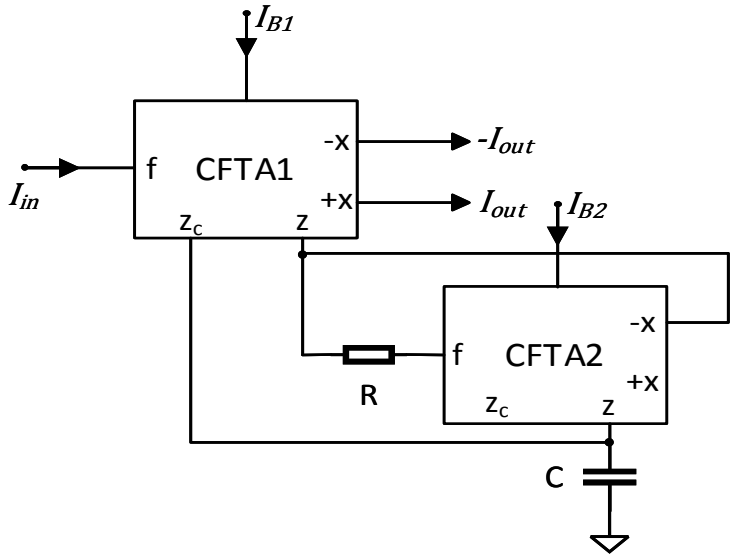

Figure 4.9 Configuration of all pass filter [6]

Transfer function equation is given as

$$\frac{I_{out}(s)}{I_{in}(s)} = \pm g_{m1} R \left(\frac{sC - g_{m2}}{sC + g_{m2}}\right) \tag{4.6}$$

Gain and phase response of figure 4.9 [6]

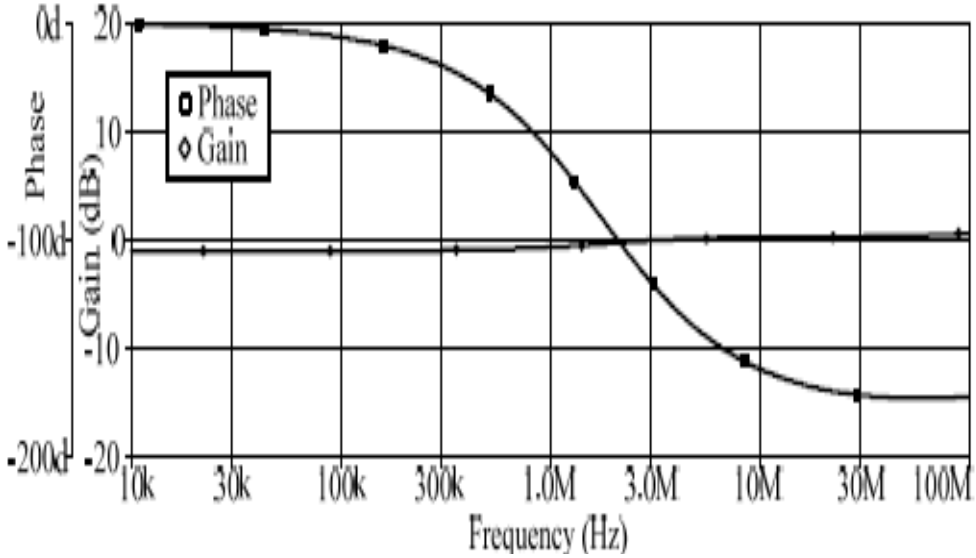

Figure 4.10 Magnitude and phase response of all pass filter [6]

4.1.4 First order All pass filter using CIDITA:

CIDITA is a current inverting differential transconductance amplifier. It has one input terminal at low impedance and others terminals are at high impedance. The characteristics equation of CFTA is given as,

$$\begin{bmatrix} I_v \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & g_m & -g_m & 0 \end{bmatrix} \begin{bmatrix} I_n \\ V_v \\ V_z \\ V_x \end{bmatrix}$$

The configuration of all pass filter based on CIDITA is shown in figure 4.11 which is proposed in [9] with grounded passive elements.

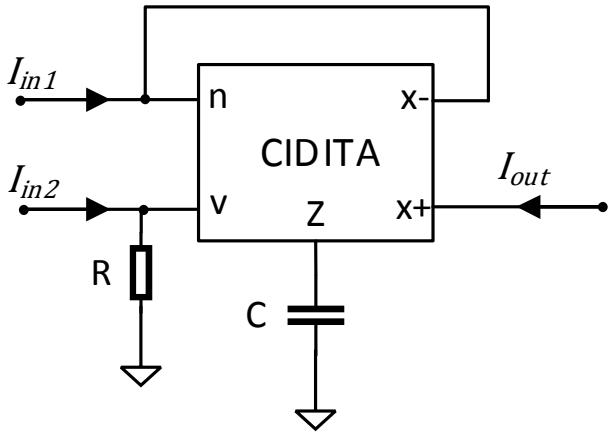

Figure 4.11 Configuration of all pass filter [9]

Transfer function equation is given as

$$\frac{I_{out}}{I_{in}} = -\frac{g_m(sCR-1)}{sC+g_m} \tag{4.7}$$

Where g_m transconductance of CIDITA

Gain and phase response of figure 4.11 [9] and transient response, both are shown in figure

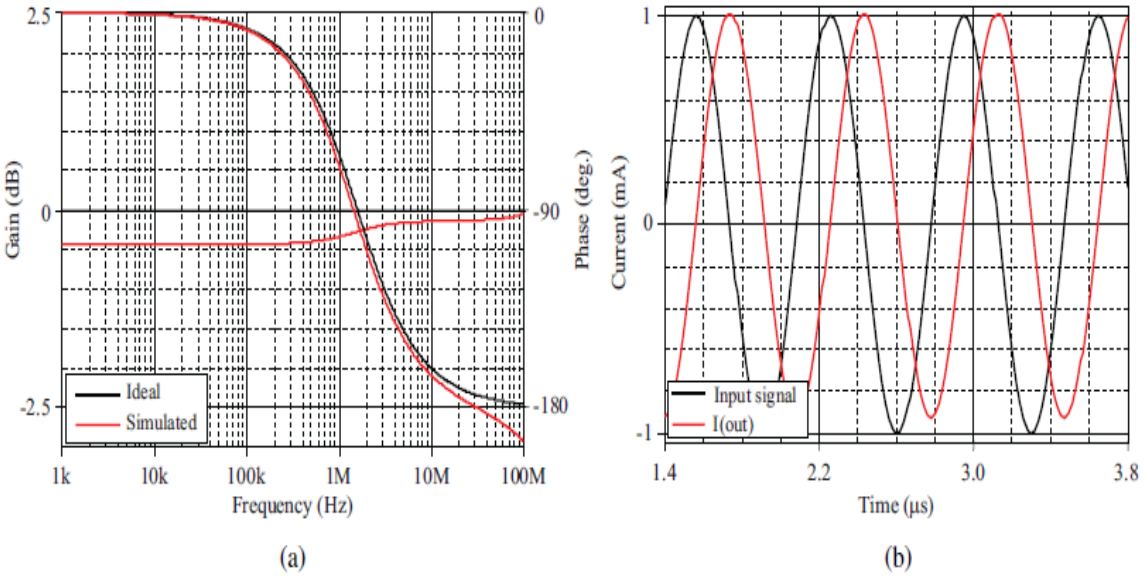

Figure 4.12 a) Magnitude and phase response of all pass filter [9] b) transient response [9]

4.2 The proposed first order Low-pass filter:

The proposed Ist order low pass filter configuration is shown below in figure 4.13. It uses a CDDITA and two passive components C_1 and C_2. As shown in figure 4.13, the input voltage is given at terminal V and the output voltage is taken from terminal x-.

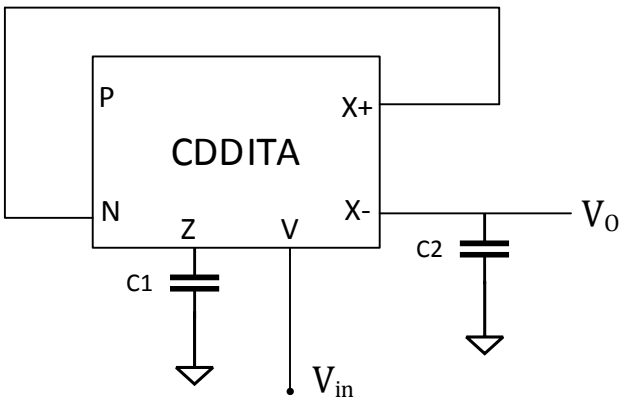

Figure 4.13 The proposed circuit of First order low pass filter

In the s-domain, the output voltage V_O across the capacitor C_2 is given by

$$V_O(s) = \frac{1}{\frac{sC}{g_m}+1} V_{in}(s) \tag{4.8}$$

$$\frac{V_O(s)}{V_{in}(s)} = \frac{1}{\frac{sC}{g_m}+1} \tag{4.9}$$

Where, $w_o = \frac{g_m}{C}$ and $C_1 = C_2$

4.2.1 Simulation results of low pass filter:

We designed a low pass filter having cut-off frequency 55.33kHz. The component values are choosing as C_1=1nf =C_2 and transconductance of CDDITA is g_m= 348µI/V.

In figure 4.15, we observed that practically cut-off frequency is more than theoretically cut-off. Simulated result is shown cut-off 57.18kHz and theoretically calculated frequency is 55.33kHz. The simulation results are carried out through PSpice simulation. The transient and frequency analysis of the proposed low pass filter is shown in figure 4.14 and 4.15 respectively.

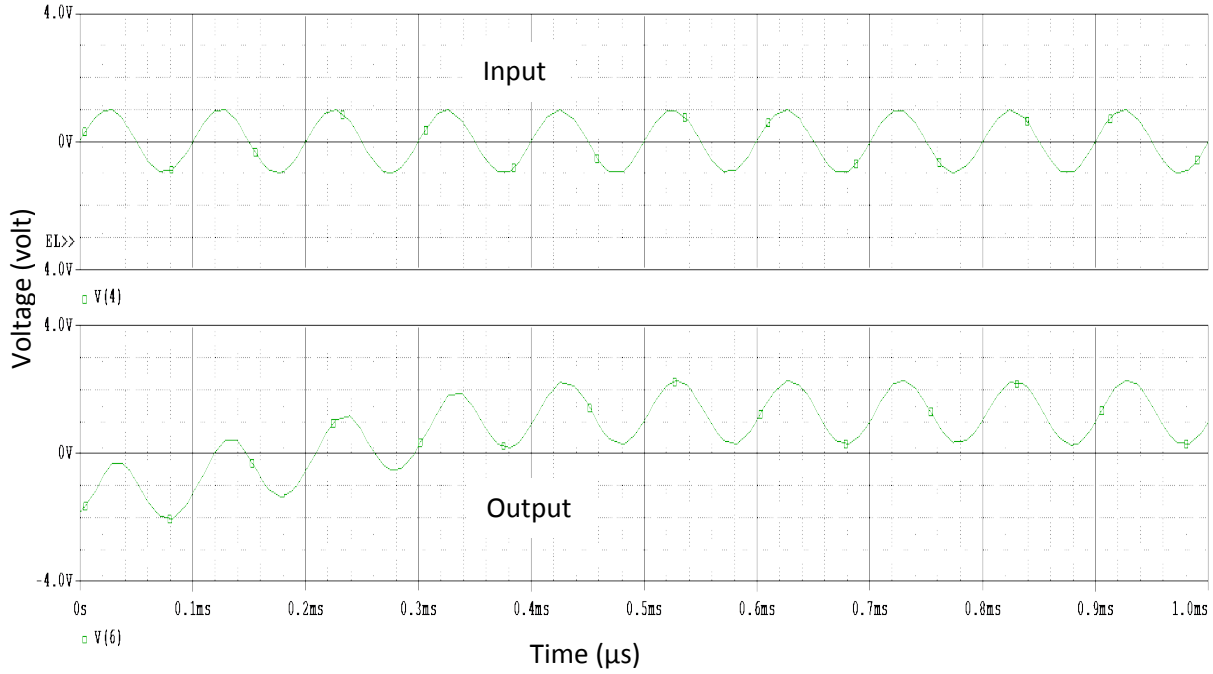

Figure 4.14 Transient response of low pass filter

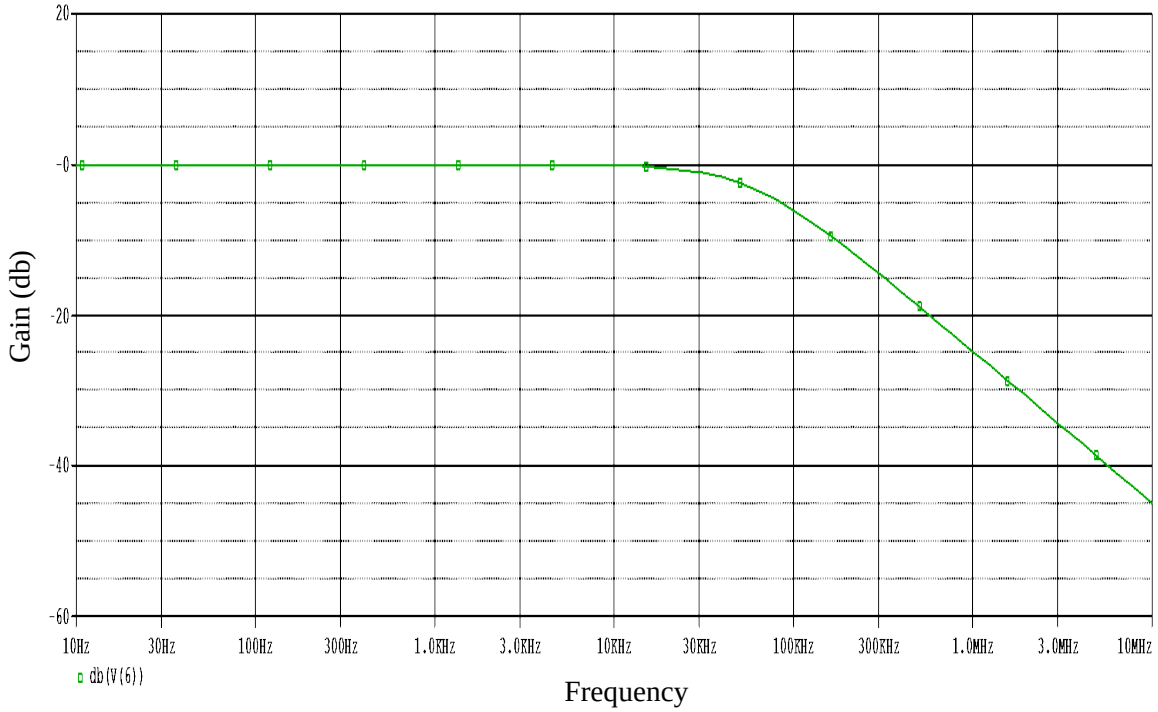

Figure 4.15 Frequency response of first order low pass filter

4.3 The proposed first order High-pass filter:

The proposed circuit is shown in Figure 4.16, is first order High pass filter with using single CDDITA. Where, we used two passive components R_1 and C_2. As shown in Fig. 4.16, the input voltage is given at terminal V and the output voltage is taken from terminal x- or across resistor R_1.

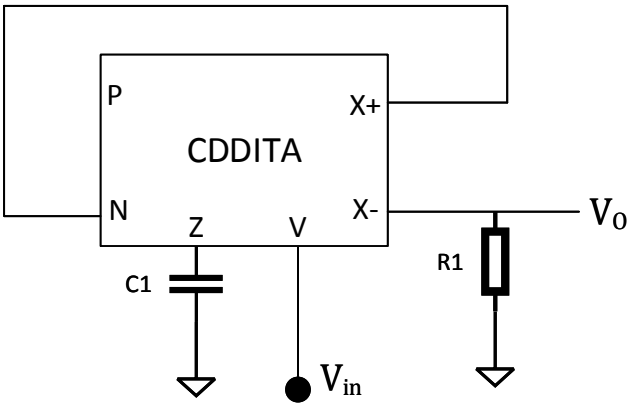

Figure 4.16 The proposed circuit of First order high pass filter

In the s-domain, the output voltage V_O across the capacitor R_1 is given by

$$V_O(s) = \frac{SRC}{SCR+1} V_{in}(s) \qquad (4.10)$$

So,

$$\frac{V_O(s)}{V_{in}(s)} = \frac{SCR}{SCR+1} \tag{4.11}$$

Where, $w_o = \frac{g_m}{C}$ and $g_m = \frac{1}{R}$

4.3.1 Simulation results of High pass filter:

We designed a high pass filter having cut-off frequency 55.33kHz. The component values are choosing as C_1=1nf, R_1=2.87 kΩ and transconductance of CDDITA is g_m= 348µI/V. In figure 3.4, we observed that practically cut-off frequency more than theoretically cut-off. Simulated result is shown cut-off 57.82kHz and theoretically calculated frequency is 55.33kHz.

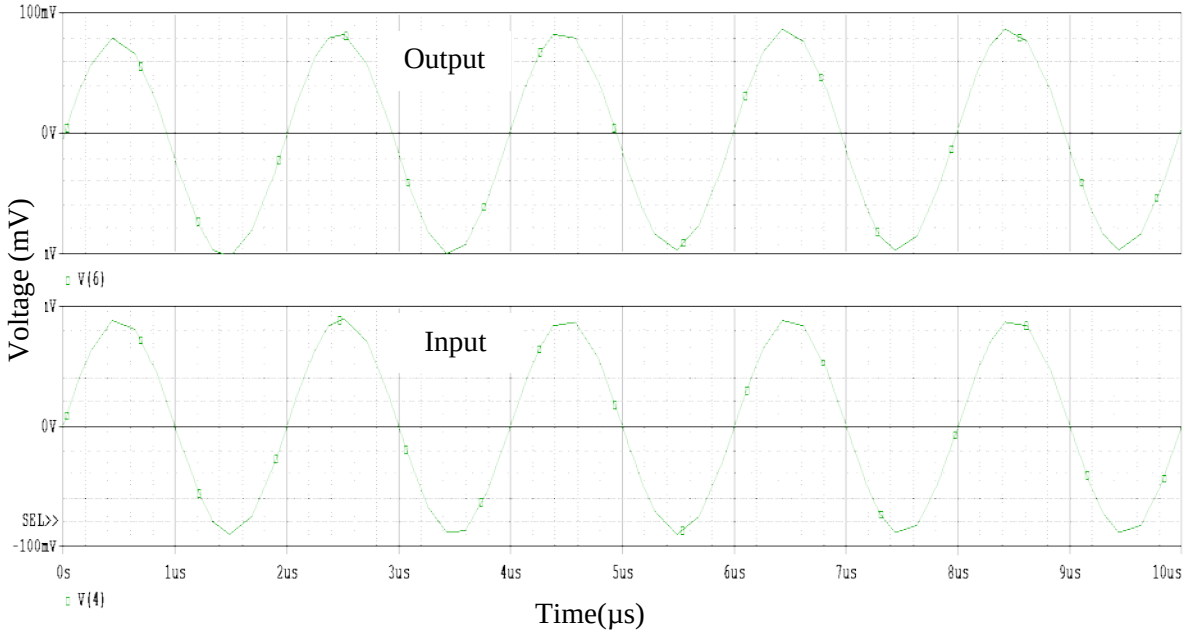

Figure 4.17 Transient response of high pass filter

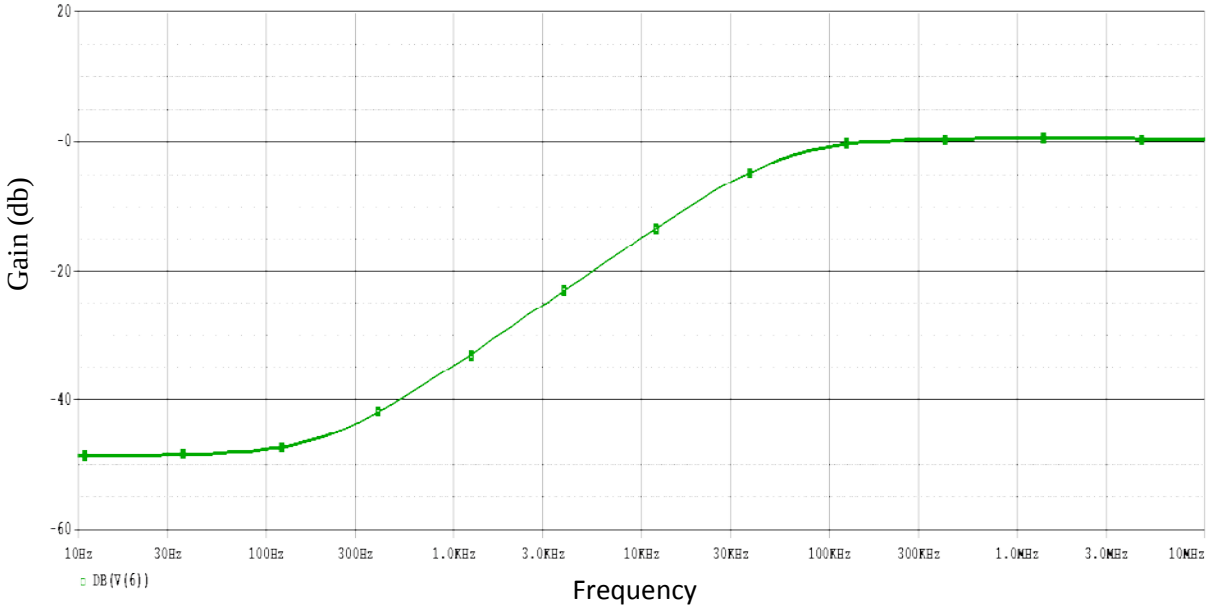

Figure 4.18 Frequency response of first order high pass filter

4.4 The proposed current-mode first order All pass filter

An all pass filter is one of the most important building block of many analog signal applications. There are lots of research paper on voltage/current mode all pass filter [13,2,3,4,5,6,14,15,16,17,18]. They have been implemented with different active building blocks like CDTA [3], CCCDTA [4], CFTA [6], CCCCTA [16,18] CDDITA [14] and CIDITA [9] etc. The all pass filter is mostly used in phase shifting application.

The proposed current mode all pass filter is shown in figure 4.19.

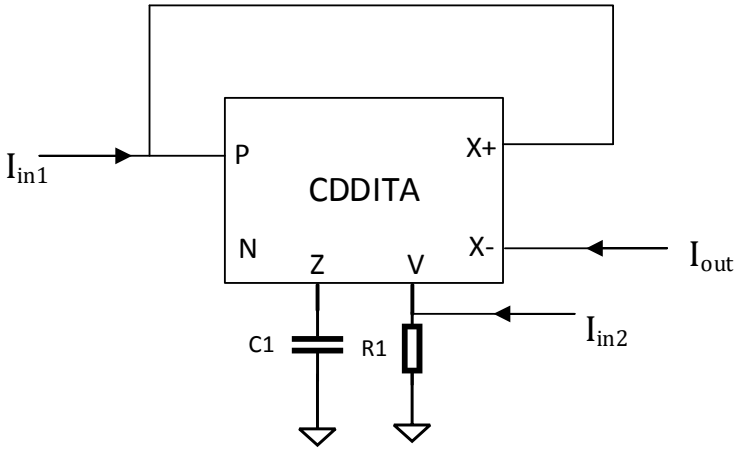

Figure 4.19 The proposed Circuit of first order high pass filter

We used a single CDDITA active block and two passive component R_1 and C_1 to make this circuit. There are two current input and one current output in the circuit. The transfer function of this circuit is as follow

$$\frac{I_{out}}{I_{in}} = \frac{g_m(SCR-1)}{(SC+g_m)} \tag{4.12}$$

Or

$$\frac{I_{out}}{I_{in}} = \frac{(SC-g_m)}{(SC+g_m)} \tag{4.13}$$

Where $g_m = \frac{1}{R}$

From equation (4.13) is shown that the current gain is unity. The pole frquency and phase angle can be obtained from equation (4.13)

$$w_o = \frac{g_m}{C} \tag{4.14}$$

$$\phi(w) = -2\tan^{-1}\left(\frac{wC}{g_m}\right) = -2\tan^{-1}(wCR) \tag{4.15}$$

From equation(4.14),we can see tha the pole frequency depends on transconductance g_m and phase shift for the circuit is 0^o to 180^o .

4.4.1 Simulation results of all pass filter

To design a current mode all pass filter, the following parameters were taken: $R_1=1/g_m=2.86k\Omega$ and C_1= 5nF and input $I_{in1}=I_{in2}$=20uA to give the pole frequency of 10kHz. The transient reponse of all pass filter is shown in figure 4.20.The gain and phase response is shown in figure 4.21.

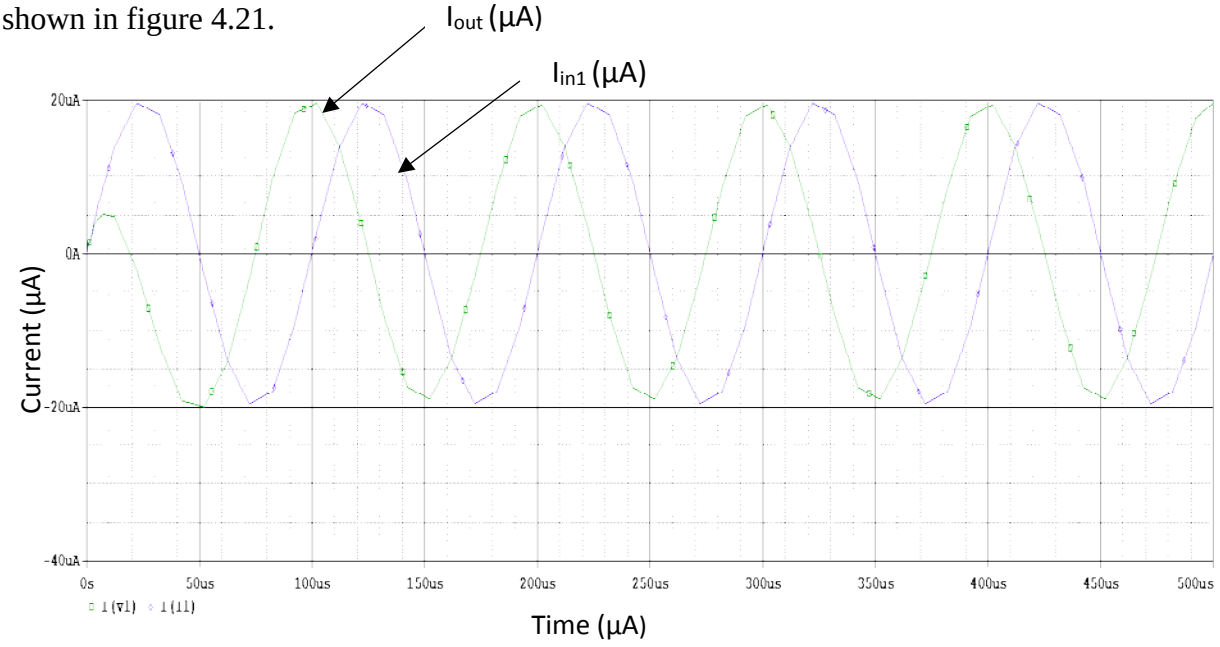

Figure 4.20 Transient response of all pass filter I_{in1} and I_{out}

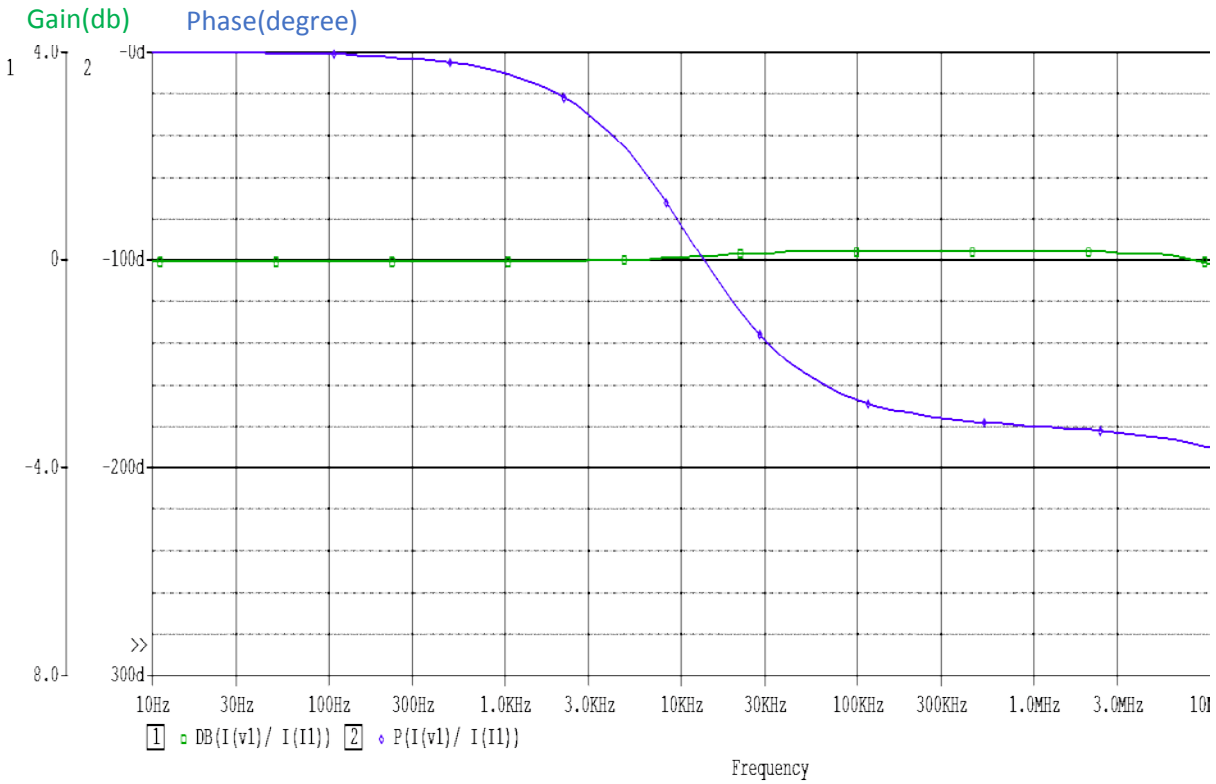

Figure 4.21 Gain and Phase response of all pass filter

4.5 Conclusion:

In the current chapter we presented a brief review of some of the Ist order RC active filters realized with active building blocks of recent origin and introduced three first order RC active filters realized with CDDITA. All of the realized filters use a single active building block and all grounded passive elements.

4.6 References

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CHAPTER-5

Conclusion and future scope

5.1 Conclusion:

In this chapter, we present the summary of the work done in this dissertation and list some of the directions in which the present work can be extended.

Chapter 1: first chapter describes basic concept of current mode, voltage mode and mixed mode signal processing. The context in which the present work has been carried out is established in this chapter.

Chapter 2: In this chapter, we have discussed basic characteristics of current differencing differential input trans conductance amplifier (CDDITA) and its implementation using CMOS and carried out some important characteristic like AC and DC sweep of CDDITA using PSpice simulation.

Chapter 3: In this chapter, we have discussed some existing research papers on inductance simulator using various existing active blocks such as OTRA, CDTA, CCCDTA, CCIII, CCCFTA and CDCC etc. We have implemented inductance simulator using CDDITAs active block. To check the performance of the implemented inductance simulator, we simulated parallel RLC circuit and obtained some results that are shown above. Then we verified all our results which are obtained using PSpice simulation with theoretical values.

Chapter 4: In this chapter we presented a brief review of some of the I^{st} order RC active filters realized with active building blocks of recent origin and introduced three first order RC active filters realized with CDDITA. All of the realized filters use a single active building block and all grounded passive elements.

CDDITA is an active building block whose terminal charcteristics are similar to other building block like CDTA and CIDITA. We have not carried out a detailed comparitive study of the advantages of using CDDITA over other similar works. A rigorous comparison of the characteristic of these similar active building blocks may be needed before recommended this block for commercial use.

5.3 Scope for future work:

This block may be used for realization of various types of sinusoidal oscillators including single resistance controlled oscillators (SRCOs) and quadrature oscillators. Similarly integrated realized with CDDITA may be used in the realization of higher order filters.
Thus, there is enough scope for extension of the work carried out in this dissertation.

Appendix

PSpice model file used for simulation is CMOS 0.5 µm process which has following model parameters -

. MODEL nmos_transistor **NMOS** (LEVEL=3 UO=460.5 TOX=1E-8 TPG=1 VTO=.62 +JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73 LD=4E-8 ETA=0 VMAX=130E3 +NSUB=1.71E17 PB=.761 PHI=.905 THETA=.129 GAMMA=.69 KAPPA=0.1 AF=1 +WD=1.1E-7CJ=76.4E-5 MJ=.357 CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-10 +CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42 NFS=1.2E11)

. MODEL pmos_transistor **PMOS** (+ LEVEL=3 UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=.1E-6 RS=886 RSH=1.81 LD=3E-8 ETA=0 VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=.905 THETA=.12 GAMMA=.76 KAPPA=2 AF=1 WD=1.4E-7CJ=85E-5 MJ=.429 CJSW=4.67E-10 MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81 NFS=.52E11)